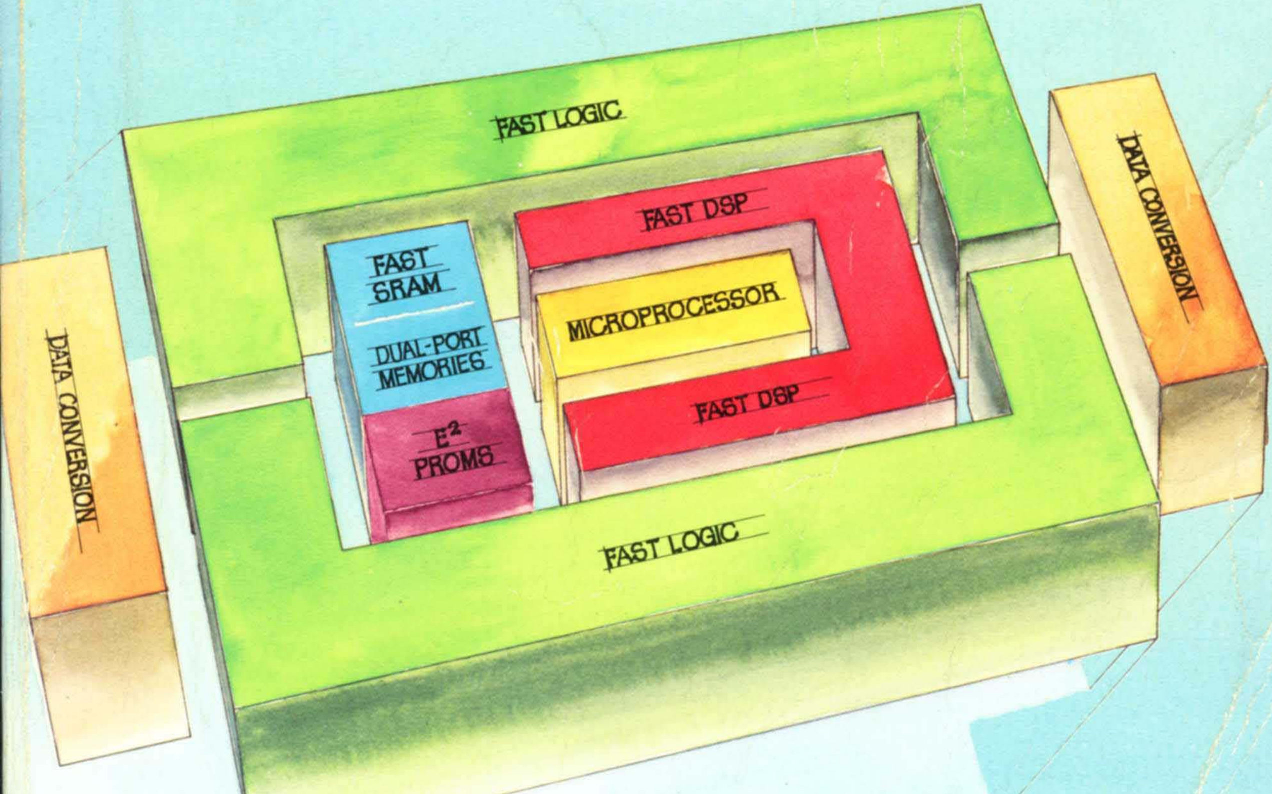
Integrated
Device
Technology

High Performance CMOS

DATA BOOK
1988



Integrated Device Technology, Inc.

HIGH-SPEED CMOS DATA BOOK

3236 Scott Boulevard, Santa Clara, California 95054
Telephone: (408) 727-6116 • TWX: 910-338-2070 • FAX: (408) 988-3029
Printed in U.S.A. 1/88

CONTENTS OVERVIEW

The block diagram on the cover of this book pictorially illustrates the multiple product lines offered by Integrated Device Technology, a recognized leader in high-speed CMOS technology. IDT's broad line of products enables us to provide a complete CMOS solution to designers of high-performance digital systems. Our products include industry standard devices as well as products with speed, lower-power, package and/or architectural benefits that allow the designer to achieve significantly improved system performance.

Use this book to find ordering information: Start with the Ordering Information chart at the back of each datasheet, or Cross Reference Guides (p 1-13) along with Package Diagram Outlines (p 15-3), to compose the complete IDT part number. Reference data on our Technology Capabilities and Quality Commitments are included in separate sections (2, 3) respectively).

Use this book to find product data: Start with the Table of Contents, organized either alphanumerically by product line (p ii) or numerically across all products (p xiv); for a more complete summary of product line offerings, use the Product Selector Guide (p 1-2). These indexes will direct you to the page on which the complete technical data sheet can be found, and may in some cases refer you to related Application or Technical Notes (p 14-1). Data sheets may be of the following type:

ADVANCE INFORMATION—contain initial descriptions, subject to change, for products that are in development, including features and block diagrams.

PRELIMINARY—contain descriptions for products soon to be or recently released to production, including features, pinouts and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

FINAL—contain minimum and maximum limits specified over the complete supply and temperature range for full production devices.

New Products, product performance enhancements, additional package types and new product families are being introduced frequently. Please contact your local IDT sales representative or 1-800-IDT CMOS to determine latest device specifications, package types and product availability.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support device or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

TABLE OF CONTENTS

TABLE OF CONTENTS (CONT'D)

CONTENTS **PAGE**

TABLE OF CONTENTS (CONT'D)

TABLE OF CONTENTS (CONT'D)

CONTENTS PAGE

TABLE OF CONTENTS (CONT'D)

TABLE OF CONTENTS (CONT'D)

TABLE OF CONTENTS (CONT'D)

CONTENTS **PAGE**

NUMERIC TABLE OF CONTENTS

NUMERIC TABLE OF CONTENTS (CON'T.)

NUMERIC TABLE OF CONTENTS (CON'T.)

NUMERIC TABLE OF CONTENTS (CON'T.)

NUMERIC TABLE OF CONTENTS (CON'T.)

Product Selector and Cross Reference Guides

1

Technology/Capabilities

Quality and Reliability

Static RAMs

Dual-Port RAMs

FIFO Memories

Digital Signal Processing (DSP)

Bit-Slice Microprocessor Devices (MICROSLICE™) and EDC

Reduced Instruction Set Computer (RISC) Processors

Logic Devices

Data Conversion

E^2PROMS-Electrically Erasable Programmable Read Only Memories

Subsystems Modules

Application and Technical Notes

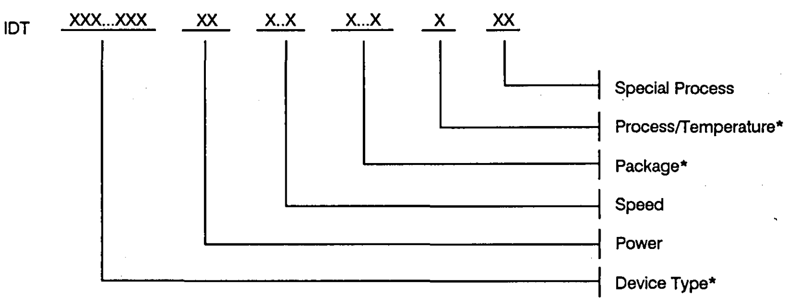
Package Diagram Outlines

PART NUMBER DESCRIPTION

IDT's part number identifies the basic product, speed, power, package(s) available, operating temperature and processing grade. Each data sheet has a detailed description, using the part number, on ordering the proper product for the user's application. The part number is comprised of a series of alpha-numeric characters:

1. An "IDT" corporate identifier for Integrated Device Technology, Inc.
2. A basic device part number composed of alpha-numeric characters.
3. A device power identifier, composed of one or two alpha characters, is used to identify the power options. In most cases, the following alpha characters are used:
   "S" or "SA" is used for the standard product's power.
   "L" or "LA" is used for lower power than the standard product.
4. A device speed identifier, when applicable, is either alpha characters, such as "A" or "B", or numbers, such as 20 or 45. The speed units, depending on the product, are in nanoseconds or megahertz.
5. A package identifier, composed of one or two alpha characters. The data sheet should be consulted to determine the packages available and the package identifiers for that particular product.
6. A temperature/process identifier. The product is available in either the commercial or military temperature range, processed to a commercial specification, or the product is available in the military temperature range with full compliance to MIL-STD-883. Many of IDT's products have burn-in included as part of the standard commercial process flow.
7. A special process identifier, composed of alpha characters, is used for products which require radiation enhancement (RE) or tolerance (RT).

Example:



* Field Identifier Applicable To All Products

High-Speed CMOS MICROSLICE™ Products

- CMOS microprogrammable bit-slice microprocessor family
- CMOS Error Detection and Correction product family
- IDT49C000 products offer dramatically improved system performance through new innovative architectures
- IDT39C000 products are pin-compatible, performance-enhanced 2900 family replacements
- Meets or exceeds bipolar speeds and output drive at a small fraction of the power consumption
- Sequential letter suffix designates 20%-40% speed upgrade
- Instruction set/operation codes functionally identical to 2900 family

	Part Number	Description	Replaces	Oper. Power (max.) (mW) Com'l.	Mil.
MICROPROCESSORS	IDT39C01C IDT39C01D IDT39C01E	4-Bit μP Slice	Am2901B,C; Am29C01C; CY7C901	157 184 210	192 220 247
	IDT39C03A IDT39C03B	4-Bit μP Slice	Am2903A	265	330
	IDT39C203 IDT39C203A	4-Bit μP Slice	Am29203	265	330
	IDT49C401 IDT49C401A	16-Bit μP Slice	IMI4X2901B	945	1200
	IDT49C402 IDT49C402A	16-Bit μP Slice, Quad 2901 with 8 additional destination functions and a 64 × 16 dual-port memory capacity	Four 2901s & One 2902; Am29C101; CY7C9101; WSI59016	945	1200
	IDT49C403 IDT49C403A	16-Bit μP Slice, Quad 2903/29203 with 64 × 16 register file, 4 Q-registers, word/BYTE control, BYTE swap, cascadable	Four 2903/29203s & One 2902	1180	1375
	IDT49C404 **IDT49C404A**	32-Bit μP Slice, 3-port device with 32-Bit ALU, 64 × 32 register file, cascadable funnel shifter, priority encoder, merge logic and mask generator	Two Am29334s & One Am29332	**1500**	**2000**
SEQUENCERS	IDT39C09A IDT39C09B	4-Bit Sequencer	Am2909A; CY7C909	236	302
	IDT39C10B IDT39C10C	12-Bit Sequencer with 33-Deep Stack	Am2910A; CY7C910	395	495
	IDT39C11A IDT39C11B	4-Bit Sequencer	Am2911A; CY7C911	236	302
	IDT49C410 IDT49C410A	16-Bit Sequencer with 33-Deep Stack	Am2910; Am29C10; CY7C910	395	495
REG. FILES	IDT39C705A IDT39C705B	16 × 4 Register File Extension	Am29705A	210	275
	IDT39C707 IDT39C707A	16 × 4 Register File Extension	Am29707	210	275
EDC	IDT39C60 IDT39C60-1 IDT39C60A	16-Bit Cascadable Error Detection Correction Unit	Am2960,-1,A; N2960; MC74F2960,-1,A	446	550
	IDT49C460 IDT49C460A **IDT49C460B**	32-Bit Cascadable Error Detection Correction Unit	DP8402; 74AS632; ALS632	500	690
OTHER	IDT39C02A	Carry Lookahead Generator	Am2902A	30	30
	IDT49C25	Microcycle Length Controller	Am2925	30	30

High-Speed CMOS Static RAMs

- Extremely fast access times
- Low power consumption
- 2V data retention battery backup on all low-power devices
- Three-state outputs
- 'M' type ceramic RAM modules are built with monolithic RAMs in LCC packages surface mounted onto multi-layered, co-fired ceramic substrates using IDT's high-reliability vapor phase reflow soldering process
- 'MP' type commercial plastic modules are built using IDT monolithic RAMs in SMD plastic packages, surface mounted onto epoxy laminate (FR4) substrates

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Power (typical) Oper. (mW)	Power (typical) Standby (μW)
MONOLITHIC					
IDT6167	16K (16K × 1)	15	12	**150**	10
IDT6168	16K (4K × 4)	15	15	225	10
IDT71681	16K (4K × 4) with separate data inputs and outputs; outputs track inputs during write mode	25	20	225	10
IDT71682	16K (4K × 4) with separate data inputs and outputs; outputs in high impedance state during write mode	25	20	225	10
IDT6116	16K (2K × 8)	25	15	**160**	**20**
IDT7187	64K (64K × 1)	25	15	250	30
IDT100490	64K (64K × 1) with ECL 100K compatible I/O	—	15	320	—
IDT7188	64K (16K × 4)	20	15	300	30
IDT6198	64K (16K × 4) with output enable $(\overline{OE})$ for added system flexibility	20	15	300	30
IDT7198	64K (16K × 4) output enable $(\overline{OE})$ and second chip select $(\overline{CS_2})$ for added system flexibility and memory control	20	15	300	30
IDT71981	64K (16K × 4) with separate data inputs and outputs; outputs track inputs during write mode	20	15	300	30
IDT71982	64K (16K × 4) with separate data inputs and outputs; outputs in high impedance state during write mode	20	15	300	30
IDT7164	64K (8K × 8)	35	30	**250**	30
IDT7165	64K (8K × 8) with asynchronous clear and high-speed chip select	35	30	**250**	30
IDT71C65	64K (8K × 8) with CMOS compatible I/O	35	30	250	30
IDT7186	64K (4K × 16)	55	45	300	30
IDT71257	256K (256K × 1)	35	25	350	100
IDT71258	256K (64K × 4)	35	25	350	100
IDT61298	256K (64K × 4) with output enable $(\overline{OE})$ for added system flexibility	35	25	350	100
IDT71281	256K (64K × 4) with separate data inputs and outputs; outputs track inputs during write mode	35	25	350	100
IDT71282	256K (64K × 4) with separate data inputs and outputs; outputs in high impedance state during write mode	35	25	350	100
IDT71256	256K (32K × 8)	45	35	**250**	**15**
IDT71027	1 Megabit (1024 × 1)	55	45	500	200
IDT71028	1 Megabit (256K × 4)	55	45	500	200
IDT71024	1 Megabit (128K × 8)	55	45	500	200
IDT6178	16K (4K × 4) cache-tag with cache address comparator and asynchronous clear	15	12	300	—
IDT7174	64K (8K × 8) with cache address comparator, asynchronous clear and high-speed chip select	45	35	250	—
IDT71501	64K (64K × 1) synchronous RAM; all inputs and outputs latched	45	35	385	—
IDT71502	64K (4K × 16) registered RAM for writable control store use; has on-board serial load, parity, breakpoint and trace logic	45	35	350	30

CONTINUED

High-Speed CMOS Static RAMs (continued)

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Power (max.) Oper. (mW)	Power (max.) Standby (mW)
MODULES					
IDT7MP564	80K (16K × 5) static RAM module (plastic SIP)	—	15	550	110
IDT8MP628	128K (8K × 16) plastic SIP RAM module	—	40	1650	165
IDT8M628	128K (8K × 16) RAM module with monolithic pinout	50	40	1650	220
IDT7MP156	256K (256K × 1) plastic SIP RAM module	—	25	1375	330
IDT7MC156	256K (256K × 1) static RAM module (ceramic SIP)	—	25	1485	330
IDT7MP456	256K (64K × 4) plastic SIP RAM module	—	25	1705	330
IDT7M856	256K (32K × 8) RAM module with monolithic pinout	50	40	2090	440
IDT8M856	256K (32K × 8) RAM module with monolithic pinout (low-power)	55	45	880	66
IDT8MP656	256K (16K × 16) plastic SIP RAM module	—	40	1870	330
IDT8M656	256K (16K x 16) RAM module with monolithic pinout	60	40	1870	440
IDT7M656	256K (16K × 16, 32K × 8, 64K × 4) RAM module – customer configurable organization	25	15	7040	85
IDT7M812	512K (64K × 8) RAM module offering maximum addressable memory required by 8-Bit MPs	35	25	5280	880
IDT7M912	512K (64K × 9) RAM module offering maximum addressable memory required by 8-Bit MPs	35	25	5940	990
IDT8MP612	512K (32K × 16) plastic SIP RAM module	—	40	1650	165
IDT8M612	512K (32K × 16) RAM module with monolithic pinout	60	40	1650	275
IDT7MC4032	512K (16K × 32) RAM module with separate I/O (ceramic dual SIP)	—	30	5940	660
IDT7MC4001	1 Megabit (1024K × 1) static RAM module (ceramic SIP)	—	TBD	1348	330
IDT8MP824	1 Megabit (128K × 8) plastic SIP RAM module	—	40	1210	440
IDT8M824	1 Megabit (128K × 8) RAM module with monolithic pinout	60	40	1210	550
IDT8MP624	1 Megabit (64K × 16) plastic SIP RAM module	—	40	1925	440
IDT8M624	1 Megabit (64K × 16) RAM module with monolithic pinout	60	40	1925	495
IDT7MB624	1 Megabit (64K × 16, 128K × 8, 256K × 4) plastic RAM module – customer configurable organization	—	25	10725	1320
IDT7M624	1 Megabit (64K × 16, 128K × 8, 256K × 4) RAM module – customer configurable organization	35	25	10725	1320
IDT7M4017	2 Megabit (64K × 32) RAM module	60	40	TBD	TBD
IDT7MP4008	4 Megabit (512K × 8) static RAM module (plastic SIP)	—	40	2585	380
IDT7M4016	4 Megabit (256K × 16) RAM module	—	45	TBD	TBD
IDT7MP6025	512K (64K × 8) registered static RAM module	—	25MHz	TBD	TBD
IDT7M824	1 Megabit (128K × 8) RAM module with registered buffered/latched addresses and I/Os	60	45	2640	935
IDT7M6001	32K × 20 double buffered RAM module with registered, multiplexed address	20MHz	25MHz	TBD	TBD
IDT7M6032	16K × 32 high-speed writable control store with SPC™	TBD	TBD	TBD	TBD
IDT7MB6042	8K × 112 high-speed writable control store with SPC™	—	TBD	TBD	TBD

High-Speed CMOS Dual-Port RAMs

- High-speed, low-power
- Independent read or write access to any memory location from either port
- Each port has separate controls, address and I/O
- On-chip port arbitration logic
- Fully asynchronous operation from either port
- $\overline{\text{INT}}$ and $\overline{\text{BUSY}}$ flags ($\overline{\text{BUSY}}$ only in IDT7132/7142)
- Automatic power-down feature controlled by $\overline{\text{CE}}$
- 2V data retention battery back-up on all low-power devices
- Dual-port RAM modules built with IDT monolithic dual-port RAMs in LCC packages, surface mounted to multi-layered, co-fired ceramic substrates using IDT's high-reliability vapor phase reflow soldering process

1

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Power (typical) Oper. (mW)	Standby (mW)
IDT7130	8K (1K × 8) replaces Synertek SY2130	**45**	**35**	325	1
IDT7140	8K (1K × 8) functions as slave with IDT7130 to provide 16-Bit words or wider; pin compatible with IDT7130	**45**	**35**	325	1
IDT7132	16K (2K × 8) fastest available speeds in this industry standard product; now multiple sourced	45	35	325	1
IDT7142	16K (2K × 8) functions as slave with IDT7132 to provide 16-Bit words or wider; pin compatible with IDT7132	45	35	325	1
IDT71321	16K (2K × 8) high-speed dual-port with interrupt output (MASTER)	45	35	325	1
IDT71421	16K (2K × 8) functions as slave with IDT71321 to provide 16-Bit words or wider; pin compatible with IDT71321	45	35	325	1
IDT71322	16K (2K × 8) with Semaphore	**45**	45	500	1
IDT7133	32K (2K × 16)	70	55	375	1
IDT7143	32K (2K × 16) functions as slave with IDT7133 to provide 32-Bit words or wider	70	55	375	1
IDT7134	32K (4K × 8) high-speed operation in system where on-chip arbitration is not needed	**45**	45	500	1
IDT71342	32K (4K × 8) with Semaphore	**45**	45	500	1
IDT7M134	64K (8K × 8) dual-port RAM module	**60**	**45**	950	20
IDT7M144	64K (8K × 8) functions as slave with IDT7M134 to provide 16-Bit words or wider; pin compatible with IDT7M134	**60**	**45**	950	20
IDT7M135	128K (16K × 8) dual-port RAM module	**60**	**45**	1600	50
IDT7M145	128K (16K × 8) functions as slave with IDT7M135 to provide 16-Bit words or wider; pin compatible with IDT7M135	**60**	**45**	1600	50
IDT7M137	256K (32K × 8) dual-port RAM module where on-chip arbitration is not needed	**60**	**55**	1800	60

High-Speed CMOS FIFOs

- Extremely fast access and cycle times
- Low power consumption
- Asynchronous and simultaneous read and write
- Fully expandable in depth and width
- Single read and write line operation – IDT7200 family
- Empty, Full and Half-Full status flags – IDT7200 family
- Six pin-compatible versions of varying depth – IDT7200 family
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Auto retransmit capability – IDT7200 family
- FIFO modules are built with IDT monolithic FIFOs in LCC packages, surface mounted to a multilayer, co-fired ceramic substrate using IDT's high-reliability vapor phase reflow soldering process

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Max. Power (mW) Mil.	Com'l.
IDT72400 FIFO FAMILY					
IDT72401	64 × 4, replaces MMI 67401 at 1/4 power	**35MHz**	**45MHz**	250	195
IDT72402	64 × 5, replaces MMI 67402 at 1/4 power	**35MHz**	**45MHz**	250	195
IDT72403	64 × 4, replaces MMI 67401 at 1/4 power, with output enable	**35MHz**	**45MHz**	250	195
IDT72404	64 × 5, replaces MMI 67402 at 1/4 power, with output enable	**35MHz**	**45MHz**	250	195
IDT72413	64 × 5, replaces MMI 67413 at 1/4 power, with output enable, Half-Full and Almost-Full/Empty flags	**35MHz**	**45MHz**	385	330
IDT7200 FIFO FAMILY					
IDT7200	256 × 9, 28-pin 300mil DIP	30	25	700	625
IDT7201A	512 × 9, replaces Mostek MK4501, with Half-Full Flag	**30**	**25**	700	625
IDT7202A	1K × 9, with Half-Full Flag	40	35	700	625
IDT72021	1K × 9, with Half-Full and Almost-Full/Empty flags and output enable	30	25	700	625
IDT7203	2K × 9, with Half-Full Flag	50	50	750	600
IDT7204	4K × 9, with Half-Full Flag, largest monolithic FIFO available	50	50	750	600
IDT72041	4K x 9, with Half-Full and Almost-Full/Empty flags and output enable	40	35	900	700
IDT7200 FIFO MODULE FAMILY					
IDT7M203	2K × 9 FIFO module using four IDT7201s	50	40	750	600
IDT7M204	4K × 9 FIFO module using four IDT7202s	50	40	750	600
IDT7M205	8K × 9 FIFO module using four IDT7203s	60	50	—	—
IDT7M206	16K × 9 FIFO module using four IDT7204s	60	50	—	—
IDT72100 SERIAL FIFO FAMILY					
IDT72103	2K × 9 parallel-serial input/output with Flexishift™, 40MHz serial rate	50	50	750	600
IDT72104	4K × 9 parallel-serial input/output with Flexishift™, 40MHz serial rate	50	50	750	600
IDT7250 BIDIRECTIONAL FIFO FAMILY					
IDT7252	1K × 18 – 2K × 9 BiFIFO™ 48-pin DIP	50	50	750	600

High-Speed CMOS DSP Building Blocks

- High speed, low power
- Highly integrated LSI building blocks
- Very fast 50MHz components
- Supports integer formats
- Inputs and outputs directly TTL-compatible

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Max. Power (mW) Mil.	Com'l.
IDT7320	16-Bit Eight-level deep pipeline register	15	10	400	300
IDT7381	16-Bit Cascadable DSP ALU	35	30	400	300
IDT7383	16-Bit Cascadable DSP ALU	25	20	400	300

High-Speed CMOS Parallel Multiplier-Accumulators

- High speed, low power
- Parallel multiplier-accumulators with selectable accumulation, rounding and preloading
- Extended product output for multiple accumulations
- Preload function allows output register to be preset
- All devices perform subtraction and double precision addition and multiplication
- Inputs and outputs directly TTL-compatible

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Max. Power (mW) Mil.	Com'l.
IDT7209	12 × 12-Bit–pin and functionally compatible with TRW TDC1009J	55	45	1000	750
IDT7210	16 × 16-Bit–with 35-Bit output; pin and functionally compatible with TRW TDC1010J	40	35	1450	1250
IDT7243	16 × 16-Bit–with 19-Bit output; pin and functionally compatible with TRW TDC1043	55	45	790	690

High-Speed CMOS Parallel Multipliers

- High speed, low power
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Inputs and outputs directly TTL-compatible
- Three-state output controls and separate register enables

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Max. Power (mW) Mil.	Com'l.
IDT7212	12 × 12-Bit–pin and functionally compatible with TRW MPY012H	40	35	875	685
IDT7213	12 × 12-Bit–with single clock architecture	40	35	875	685
IDT7216	16 × 16-Bit–pin and functionally compatible with TRW MPY016H/K and AMD Am29516	25	20	1400	1200
IDT7217	16 × 16-Bit–with single clock architecture; pin and functionally compatible with AMD Am29517	30	25	1400	1200
IDT7317	16 × 16-Bit–with single clock, 32-Bit output	25	20	1400	1200

High-Speed CMOS Floating-Point Products

- High speed, low power – 500mW typical
- Advanced CEMOS technology
- Full IEEE standard 754 conformance
- Single 5V supply
- Full 32-Bit and 64-Bit multiply and ALU operations
- Pipelined and flow-through modes
- 144-Pin Grid Array
- Full MIL-STD-883 compliant product available

Part Number	Description	Max. Speed (MFLOP) Mil.	Com'l.	Max. Power (mW) Mil.	Com'l.
IDT721264	32-/64-Bit Multiplier–pin and functionally compatible with Weitek WTL1264	12.5 (32-Bit) 6.2 (64-Bit)	16.7 (32-Bit) 8.3 (64-Bit)	750	625
IDT721265	32-/64-Bit ALU–pin and functionally compatible with Weitek WTL1265	12.5 (32-Bit) 12.5 (64-Bit)	16.7 (32-Bit) 16.7 (64-Bit)	750	625

High-Speed CMOS Data Conversion Products

- High speed – low power
- Available in military and commercial temperature ranges
- Produced with advanced CEMOS high-performance technology

VIDEO DACs

- IDT75C18 is pin and function compatible with TRW 1018 with half the power consumption
- IDT75C19 is world's first CMOS 9-Bit Video DAC
- IDT75C458 PaletteDAC™ is pin and function compatible with Brooktree BT458
- IDT75MB38 is a triple 8-Bit, 125MHz module with onboard voltage reference

FLASH A/D CONVERTERS

- IDT75C48 is pin and function compatible with TRW 1048 with half the power consumption, on-chip Error Detection and Correction, extended analog input range and improved output characteristics
- IDT75C58 has enhanced features such as overflow output and three-state control which allows stacking two devices for 9-Bit resolution
- IDT75M48 is a complete Flash ADC module product with input buffer amplifier, reference voltage generator and optimized layout and decoupling
- IDT75M49 is a complete 9-Bit ADC module using two IDT75C58 devices

	Part Number	Description	Replaces	Power (mW)
DAC	IDT75C18	8-Bit, 125MHz Video DAC with ECL inputs	TDC1018	400
DAC	IDT75C19	World's first 9-Bit, 125MHz Video DAC	—	400
DAC	IDT75MB38	Triple 8-Bit, 125MHz Video DAC Module	BT109, TDC1318	1500
DAC	IDT75C458	Triple 8-Bit, 125MHz PaletteDAC™	BT458	1000
ADC	IDT75C48	8-Bit, 20MHz Flash ADC	TDC1048	500
ADC	IDT75C58	8-Bit, 20MHz Flash ADC with Overflow output	—	500
ADC	IDT75M48	Complete 8-Bit, 20MHz Flash Module using IDT75C48	—	800
ADC	IDT75M49	9-Bit, 20MHz Flash Module using two IDT75C58s	—	1200

High-Speed CMOS E² PROMs

- Fast access times
- Internal address and data input latches
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1,000 cycles
- Serial access versions with SPC™ (IDT78C18A, IDT78C68A, IDT78C258A)
- On-chip timer, latches, charge pump
- Write protection circuitry, V_{CC} lockout for $V_{CC} = 4V$
- 5 volt operation
- $\overline{\text{DATA}}$ polling

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Power (typical) Oper. (mW)	Power (typical) Standby (mW)
IDT78C16A	2K × 8 E²PROM	90	70	600	4.5
IDT78C18A	2K × 8 E²PROM with Serial Protocol Channel (SPC™)	90	70	600	4.5
IDT78M64	8K × 8 E²PROM module with JEDEC E²PROM pinout	85	70	1250	20
IDT78C64A	8K × 8 E²PROM	70	55	500	4.5
IDT78C464A	8K × 8 Registered E²PROM	70	55	500	4.5
IDT78C564A	8K × 8 Registered E²PROM with Serial Protocol Channel (SPC™)	70	55	500	4.5
IDT78C256A	32K × 8 E²PROM	70	55	500	4.5
IDT78C4256A	32K × 8 Registered E²PROM	70	55	500	4.5
IDT78C5256A	32K × 8 Registered E²PROM with Serial Protocol Channel (SPC™)	70	55	500	4.5

High-Speed CMOS Logic Products

1

- FCTXXXA devices 35%-50% faster than FAST™ with equivalent output drive but at dramatically lower CMOS power over full temperature and voltage supply extremes
- FCT devices same speed and output drive as FAST™, but at dramatically lower CMOS power
- 54/74FCT8XXA devices same speed and output drive as 29800, but at dramatically lower CMOS power
- 54/74FCT8XXB devices 32%-38% faster than 29800 with equivalent output drive, but at dramatically lower CMOS power
- Both CMOS and TTL output compatible (eliminates need for pull-up resistors when driving CMOS static RAMs)
- Substantially lower input current levels than FAST™ or ALS (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Pin-compatible with industry standard MSI logic
- Devices formerly designated 39CXXX are now designated 54/74FCT8XXA or 29FCTXXX

		Max. Speed (ns)		Power (typical)	
				Oper.	Standby
Part Number	**Description**	**Mil.**	**Com'l.**	**(mW)**	**(μW)**
IDT29FCT52A	Octal Registered Transceiver	11.0	10.0	10.0	5.0
IDT29FCT53A	Octal Registered Transceiver	11.0	10.0	10.0	5.0
IDT29FCT52B	Octal Registered Transceiver	7.2	6.5	10.0	5.0
IDT29FCT53B	Octal Registered Transceiver	7.2	6.5	10.0	5.0
IDT29FCT520A	Multilevel Pipeline Register	16.0	14.0	10.0	5.0
IDT29FCT521A	Multilevel Pipeline Register	16.0	14.0	10.0	5.0
IDT49FCT601	16-Bit Bidirectional Latch w/Byte-Swap	—	—	20.0	10.0
IDT49FCT618	16-Bit Register with SPC™	14.0	12.5	20.0	5.0
IDT49FCT661	16-Bit Synchronous Binary Counter	—	—	20.0	10.0
IDT49FCT818A	Octal Register with SPC™	11.0	10.0	10.0	5.0
IDT54/74FCT138A	1-of-8 Decoder	7.8	5.8	10.0	5.0
IDT54/74FCT139A	Dual 1-of-4 Decoder	7.8	5.9	10.0	5.0
IDT54/74FCT161A	Synchronous Binary Counter	7.5	7.2	10.0	5.0
IDT54/74FCT163A	Synchronous Binary Counter	7.5	7.2	10.0	5.0
IDT54/74FCT182A	Carry Lookahead Generator	10.7	6.5	10.0	5.0
IDT54/74FCT191A	Up/Down Binary Counter	10.5	7.8	10.0	5.0
IDT54/74FCT193A	Up/Down Binary Counter	6.9	6.5	10.0	5.0
IDT54/74FCT240A	Octal Buffer	5.1	4.8	10.0	5.0
IDT54/74FCT241A	Octal Buffer	4.8	4.5	10.0	5.0
IDT54/74FCT244A	Octal Buffer	4.8	4.5	10.0	5.0
IDT54/74FCT245A	Octal Bidirectional Transceiver	4.9	4.6	10.0	5.0
IDT54/74FCT273A	Octal D Flip-Flop	8.3	7.2	10.0	5.0
IDT54/74FCT299A	Octal Universal Shift Register	9.5	7.2	10.0	5.0
IDT54/74FCT373A	Octal Transparent Latch	5.6	5.2	10.0	5.0
IDT54/74FCT374A	Octal D Flip-Flop	7.2	6.5	10.0	5.0
IDT54/74FCT377A	Octal D Flip-Flop	8.3	7.2	10.0	5.0
IDT54/74FCT399A	Quad Dual-Port Register	7.5	7.0	10.0	5.0
IDT54/74FCT521A	8-Bit Comparator	9.5	7.2	10.0	5.0
IDT54/74FCT533A	Octal Transparent Latch	5.6	5.2	10.0	5.0
IDT54/74FCT534A	Octal D Flip-Flop	7.2	6.5	10.0	5.0
IDT54/74FCT540A	Octal Inverting Buffer	—	—	10.0	5.0
IDT54/74FCT541A	Octal Non-inverting Buffer	—	—	10.0	5.0
IDT54/74FCT543A	Octal Non-inverting Latched Transceiver	7.7	6.3	10.0	5.0
IDT54/74FCT573A	Octal Transparent Latch	5.6	5.2	10.0	5.0
IDT54/74FCT574A	Octal D Register	7.2	6.5	10.0	5.0

CONTINUED

High-Speed CMOS Logic Products (continued)

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Power (typical) Oper. (mW)	Standby (μW)
IDT54/74FCT640A	Octal Bidirectional Transceiver	5.3	5.0	10.0	5.0
IDT54/74FCT645A	Octal Bidirectional Transceiver	4.9	4.6	10.0	5.0
IDT54/74FCT646A	Octal Non-inverting Registered Transceiver	7.7	6.3	10.0	5.0
IDT54/74FCT648A	Octal Inverting Registered Transceiver	6.3	5.6	10.0	5.0
IDT54/74FCT651A	Octal Non-inverting Registered Transceiver	–	–	10.0	5.0
IDT54/74FCT652A	Octal Inverting Registered Transceiver	–	–	10.0	5.0
IDT54/74FCT821A	10-Bit Non-inverting Register	12.0	12.0	10.0	5.0
IDT54/74FCT822A	10-Bit Inverting Register	12.0	12.0	10.0	5.0
IDT54/74FCT823A	9-Bit Non-inverting Register	12.0	12.0	10.0	5.0
IDT54/74FCT824A	9-Bit Inverting Register	12.0	12.0	10.0	5.0
IDT54/74FCT825A	8-Bit Non-inverting Register	12.0	12.0	10.0	5.0
IDT54/74FCT826A	8-Bit Inverting Register	12.0	12.0	10.0	5.0
IDT54/74FCT827A	10-Bit Non-inverting Buffer	10.0	8.0	10.0	5.0
IDT54/74FCT828A	10-Bit Inverting Buffer	9.5	7.5	10.0	5.0
IDT54/74FCT833A	8-Bit Transceiver w/Parity	14.0	10.0	10.0	5.0
IDT54/74FCT834A	8-Bit Transceiver w/Parity	14.0	10.0	10.0	5.0
IDT54/74FCT841A	10-Bit Non-inverting Latch	11.0	9.5	10.0	5.0
IDT54/74FCT842A	10-Bit Inverting Latch	12.0	10.0	10.0	5.0
IDT54/74FCT843A	9-Bit Non-inverting Latch	11.0	9.5	10.0	5.0
IDT54/74FCT844A	9-Bit Inverting Latch	12.0	10.0	10.0	5.0
IDT54/74FCT845A	8-Bit Non-inverting Latch	11.0	9.5	10.0	5.0
IDT54/74FCT846A	8-Bit Inverting Latch	12.0	10.0	10.0	5.0
IDT54/74FCT853A	8-Bit Transceiver w/Parity	14.0	10.0	10.0	5.0
IDT54/74FCT854A	8-Bit Transceiver w/Parity	14.0	10.0	10.0	5.0
IDT54/74FCT861A	10-Bit Non-inverting Transceiver	10.0	8.0	10.0	5.0
IDT54/74FCT862A	10-Bit Inverting Transceiver	9.5	7.5	10.0	5.0
IDT54/74FCT863A	9-Bit Non-inverting Transceiver	10.0	8.0	10.0	5.0
IDT54/74FCT864A	9-Bit Inverting Transceiver	9.5	8.5	10.0	5.0
IDT54/74FCT138	1-of-8 Decoder	12.0	9.0	10.0	5.0
IDT54/74FCT139	Dual 1-of-4 Decoder	12.0	9.0	10.0	5.0
IDT54/74FCT161	Synchronous Binary Counter	11.5	11.0	10.0	5.0
IDT54/74FCT163	Synchronous Binary Counter	11.5	11.0	10.0	5.0
IDT54/74FCT182	Carry Lookahead Generator	16.5	10.0	10.0	5.0
IDT54/74FCT191	Up/Down Binary Counter	16.0	12.0	10.0	5.0
IDT54/74FCT193	Up/Down Binary Counter	10.5	10.0	10.0	5.0
IDT54/74FCT240	Octal Buffer	9.0	8.0	10.0	5.0
IDT54/74FCT241	Octal Buffer	7.0	6.5	10.0	5.0
IDT54/74FCT244	Octal Buffer	7.0	6.5	10.0	5.0
IDT54/74FCT245	Octal Bidirectional Transceiver	7.5	7.0	10.0	5.0
IDT54/74FCT273	Octal D Flip-Flop	15.0	13.0	10.0	5.0
IDT54/74FCT299	Octal Universal Shift Register	14.0	10.0	10.0	5.0
IDT54/74FCT373	Octal Transparent Latch	8.5	8.0	10.0	5.0
IDT54/74FCT374	Octal D Flip-Flop	11.0	10.0	10.0	5.0

CONTINUED

High-Speed CMOS Logic Products (continued)

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Power (typical) Oper. (mW)	Standby (μW)
IDT54/74FCT377	Octal D Flip-Flop	15.0	13.0	10.0	5.0
IDT54/74FCT399	Quad Dual-Port Register	11.5	10.0	10.0	5.0
IDT54/74FCT521	8-Bit Comparator	15.0	11.0	10.0	5.0
IDT54/74FCT533	Octal Transparent Latch	12.0	10.0	10.0	5.0
IDT54/74FCT534	Octal D Flip-Flop	11.0	10.0	10.0	5.0
IDT54/74FCT540	Octal Inverting Buffer	9.0	8.0	10.0	5.0
IDT54/74FCT541	Octal Non-inverting Buffer	9.0	8.0	10.0	5.0
IDT54/74FCT543	Octal Non-inverting Latched Transceiver	10.0	8.5	10.0	5.0
IDT54/74FCT573	Octal Transparent Latch	8.5	8.0	10.0	5.0
IDT54/74FCT574	Octal D Register	11.0	10.0	10.0	5.0
IDT54/74FCT640	Octal Bidirectional Transceiver	8.0	7.0	10.0	5.0
IDT54/74FCT645	Octal Bidirectional Transceiver	11.0	9.5	10.0	5.0
IDT54/74FCT646	Octal Non-inverting Registered Transceiver	11.0	9.0	10.0	5.0
IDT54/74FCT648	Octal Inverting Registered Transceiver	9.0	8.0	10.0	5.0
IDT54/74FCT651	Octal Non-inverting Registered Transceiver	10.0	9.0	10.0	5.0
IDT54/74FCT652	Octal Inverting Registered Transceiver	9.0	8.0	10.0	5.0
IDT54/74FCT827	10-Bit Non-inverting Buffer	–	–	–	–
IDT54/74FCT828	10-Bit Inverting Buffer	–	–	–	–
IDT54/74FCT821B	10-Bit Non-inverting Register	8.5	7.5	10.0	5.0
IDT54/74FCT822B	10-Bit Inverting Register	8.5	7.5	10.0	5.0
IDT54/74FCT823B	9-Bit Non-inverting Register	8.5	7.5	10.0	5.0
IDT54/74FCT824B	9-Bit Inverting Register	8.5	7.5	10.0	5.0
IDT54/74FCT825B	8-Bit Non-inverting Register	8.5	7.5	10.0	5.0
IDT54/74FCT826B	8-Bit Inverting Register	8.5	7.5	10.0	5.0
IDT54/74FCT827B	10-Bit Non-inverting Buffer	6.5	5.0	10.0	5.0
IDT54/74FCT828B	10-Bit Inverting Buffer	6.5	5.5	10.0	5.0
IDT54/74FCT833B	8-Bit Transceiver w/Parity	10.0	7.0	10.0	5.0
IDT54/74FCT834B	8-Bit Transceiver w/Parity	10.0	7.0	10.0	5.0
IDT54/74FCT841B	10-Bit Non-inverting Latch	7.5	6.5	10.0	5.0
IDT54/74FCT842B	10-Bit Inverting Latch	9.0	8.0	10.0	5.0
IDT54/74FCT843B	9-Bit Non-inverting Latch	7.5	6.5	10.0	5.0
IDT54/74FCT844B	9-Bit Inverting Latch	9.0	8.0	10.0	5.0
IDT54/74FCT845B	8-Bit Non-inverting Latch	7.5	6.5	10.0	5.0
IDT54/74FCT846B	8-Bit Inverting Latch	9.0	8.0	10.0	5.0
IDT54/74FCT853B	8-Bit Transceiver w/Parity	10.0	7.0	10.0	5.0
IDT54/74FCT854B	8-Bit Transceiver w/Parity	10.0	7.0	10.0	5.0
IDT54/74FCT861B	10-Bit Non-inverting Transceiver	6.5	6.0	10.0	5.0
IDT54/74FCT862B	10-Bit Inverting Transceiver	6.5	5.5	10.0	5.0
IDT54/74FCT863B	9-Bit Non-inverting Transceiver	6.5	6.0	10.0	5.0
IDT54/74FCT864B	9-Bit Inverting Transceiver	6.5	5.5	10.0	5.0
IDT54AHCT138	1-of-8 Decoder	27.0	—	3.5	5.0
IDT54AHCT139	Dual 1-of-4 Decoder	25.0	—	3.5	5.0

CONTINUED

High-Speed CMOS Logic Products (continued)

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Power (typical) Oper. (mW)	Standby (μW)
IDT54AHCT161	Synchronous Binary Counter	20.0	—	3.5	5.0
IDT54AHCT163	Synchronous Binary Counter	20.0	—	3.5	5.0
IDT54AHCT182	Carry Lookahead Generator	20.5	—	3.5	5.0
IDT54AHCT191	Up/Down Binary Counter	22.0	—	3.5	5.0
IDT54AHCT193	Up/Down Binary Counter	19.0	—	3.5	5.0
IDT54AHCT240	Octal Buffer	12.0	—	3.5	5.0
IDT54AHCT244	Octal Buffer	13.0	—	3.5	5.0
IDT54AHCT245	Octal Bidirectional Transceiver	15.0	—	3.5	5.0
IDT54AHCT273	Octal D Flip-Flop	17.0	—	3.5	5.0
IDT54AHCT299	Universal Shift Register	17.0	—	3.5	5.0
IDT54AHCT373	Octal Transparent Latch	19.0	—	3.5	5.0
IDT54AHCT374	Octal D Flip-Flop	18.0	—	3.5	5.0
IDT54AHCT377	Octal D Flip-Flop	20.0	—	3.5	5.0
IDT54AHCT521	8-Bit Comparator	17.0	—	3.5	5.0
IDT54AHCT533	Octal Transparent Latch	24.0	—	3.5	5.0
IDT54AHCT534	Octal D Flip-Flop	18.0	—	3.5	5.0
IDT54AHCT573	Octal Transparent Latch	15.0	—	3.5	5.0
IDT54AHCT574	Octal D Register	15.0	—	3.5	5.0
IDT54AHCT640	Octal Bidirectional Transceiver	14.0	—	3.5	5.0
IDT54AHCT645	Octal Bidirectional Transceiver	15.0	—	3.5	5.0

Integrated Device Technology, Inc.

STATIC RAM CROSS REFERENCE GUIDE

AMD	IDT	AMD CONT.	IDT	AMD CONT.	IDT
AM2167-35DC	IDT6167SA35D	AM99C641-45LCB	IDT7187L45L22	AM9128-90/BUC	IDT6116SA90L32B
AM2168-55PCB	IDT6168SA55P	AM2167-55PC	IDT6167SA55P	AM99C641-70DEB	IDT7187L70CM
AM99C641-25DC	IDT7187L25C	AM2169-50LEB	IDT6169SA45LM	AM2168-45DEB	IDT6168SA45DM
AM2167-35DCB	IDT6167SA35D	AM99C641-45LE	IDT7187L45L22M	AM99C641-70LC	IDT7187L70L22
AM2168-70/BRA	IDT6168SA70DB	AM2167-70/BRA	IDT6167SA70DB	AM2168-45LE	IDT6168SA45LM
AM99C641-25DCB	IDT7187L25C	AM2169-50PC	IDT6169SA45P	AM99C164-35x	IDT7188L35x
AM2167-35LC	IDT6167SA35L	AM99C641-45LEB	IDT7187L45L22M	AM99C641-70LCB	IDT7187L70L22
AM2168-70/BUC	IDT6168SA70LB	AM2167-70/BUC	IDT6167SA70LB	AM2168-45LEB	IDT6168SA45LM
AM99C641-25LC	IDT7187L25L22	AM2169-50PCB	IDT6169SA45P	AM99C164-45x	IDT7188L45x
AM2167-35LCB	IDT6167SA35L	AM99C641-45PC	IDT7187L45P	AM99C641-70LE	IDT7187L70L22M
AM2168-70DE	IDT6168SA70DM	AM2167-70DC	IDT6167SA70D	AM2168-45PC	IDT6168SA45P
AM99C641-25LCB	IDT7187L25L22	AM2169-70/BRA	IDT6169SA55DB	AM99C164-55x	IDT7188L55x
AM2167-35PC	IDT6167SA35P	AM99C641-45PCB	IDT7187L45P	AM99C641-70LEB	IDT7187L70L22M
AM2168-70DEB	IDT6168SA70DM	AM2167-70DCB	IDT6167SA70D	AM2168-45PCB	IDT6168SA45P
AM99C641-25PC	IDT7187L25P	AM2169-70DE	IDT6169SA55DM	AM99C164-70x	IDT7188L70x
AM2167-35PCB	IDT6167SA35P	AM99C641-55/BWA	IDT7187L55CB	AM99C641-70PC	IDT7187L70P
AM2168-70LE	IDT6168SA70LM	AM2167-70DE	IDT6167SA70DM	AM2168-55/BRA	IDT6168SA55DB
AM99C641-25PCB	IDT7187L25P	AM2169-70DEB	IDT6169SA55DM	AM99C641-70PCB	IDT7187L70P
AM2167-45/BRA	IDT6167SA45DB	AM99C641-55/LMC	IDT7187L55L22B	AM2168-55/BUC	IDT6168SA55LB
AM2168-70LEB	IDT6168SA70LM	AM2167-70DEB	IDT6167SA70DM	AM99C165-35x	IDT6198L35x
AM99C641-35DC	IDT7187L35C	AM2169-70LE	IDT6169SA55LM	AM2168-55DC	IDT6168SA55D
AM2167-45/BUC	IDT6167SA45LB	AM99C641-55DC	IDT7187L55C	AM99C165-45x	IDT6198L45x
AM99C641-35DCB	IDT7187L25C	AM2167-70LC	IDT6167SA70L	AM99C68-45/BRA	IDT6168LA45DB
AM2167-45DC	IDT6167SA45D	AM2169-70LEB	IDT6169SA55LM	AM2168-55DCB	IDT6168SA55D
AM2169-40DC	IDT6169SA35D	AM99C641-55DCB	IDT7187L55C	AM99C165-55x	IDT6198L55x
AM99C641-35LC	IDT7187L35L22	AM2167-70PC	IDT6167SA70P	AM99C68-45DC	IDT6168LA45D
AM2167-45DCB	IDT6167SA45D	AM99C641-55DE	IDT7187L55CM	AM2168-55DE	IDT6168SA55DM
AM2169-40DCB	IDT6169SA35D	AM2167-70PCB	IDT6167SA70P	AM99C165-70x	IDT6198L70x
AM99C641-35LCB	IDT7187L35L22	AM9128-12/BJA	IDT6116SA120DB	AM99C68-45DCB	IDT6168LA45D
AM2167-45DE	IDT6167SA45DM	AM99C641-55DEB	IDT7187L55CM	AM2168-55DEB	IDT6168SA55DM
AM2169-40LC	IDT6169SA35L	AM9128-12/BUC	IDT6116SA120L32B	AM99C68-45PC	IDT6168LA45P
AM99C641-35PC	IDT7187L35P	AM99C641-55LC	IDT7187L55L22	AM2168-55LE	IDT6168SA55LM
AM2167-45DEB	IDT6167SA45DM	AM2168-35DC	IDT6168SA35D	AM99C328-45x	IDT71256L45x
AM2169-40LCB	IDT6169SA35L	AM9128-15/BJA	IDT6116SA150DB	AM99C68-45PCB	IDT6168LA45P
AM99C641-35PCB	IDT7187L35P	AM99C641-55LCB	IDT7187L55L22	AM2168-55LEB	IDT6168SA55LM
AM2167-45LC	IDT6167SA45L	AM2168-35DCB	IDT6168SA35D	AM99C328-55x	IDT71256L55x
AM2169-40PC	IDT6169SA35P	AM9128-15/BUC	IDT6116SA150L32B	AM99C68-55/BRA	IDT6168LA55DB
AM99C641-45/BWA	IDT7187L45CB	AM99C641-55LE	IDT7187L55L22M	AM2168-55PC	IDT6168SA55P
AM2167-45PC	IDT6167SA45P	AM2168-35LC	IDT6168SA35L	AM99C328-70x	IDT71256L70x
AM2169-40PCB	IDT6169SA35P	AM9128-70DC	IDT6116SA70D	AM99C68-55DC	IDT6168LA55D
AM99C641-45/LMC	IDT7187L45L22B	AM99C641-55LEB	IDT7187L55L22M	AM99C68-55DCB	IDT6168LA55D
AM2167-55/BRA	IDT6167SA55DB	AM2168-35LCB	IDT6168SA35L	AM99C88-12/BXC	IDT7164L120DB
AM2169-50/BRA	IDT6169SA45DB	AM9128-70DCB	IDT6116SA70D	AM99CS88-12/BXC	IDT7164L120DB
AM99C641-45DC	IDT7187L45C	AM99C641-55PC	IDT7187L55P	AM99C68-55DMB	IDT6168LA55DB
AM2167-55/BUC	IDT6167SA55LB	AM2168-35PC	IDT6168SA35P	AM99C88-15/BUC	IDT7164L150L32B
AM2169-50DC	IDT6169SA45D	AM9128-70DE	IDT6116SA70DM	AM99CS88-15/BUC	IDT7164L150L32B
AM99C641-45DCB	IDT7187L45C	AM99C641-55PCB	IDT7187L55P	AM99C68-55PC	IDT6168LA55P
AM2167-55DC	IDT6167SA55D	AM2168-35PCB	IDT6168SA35P	AM99C88-15/BXC	IDT7164L100DB
AM2169-50DCB	IDT6169SA45D	AM9128-70DEB	IDT6116SA70DM	AM99CS88-15/BXC	IDT7164L150DB
AM99C641-45DE	IDT7187L45CM	AM99C641-70/BWA	IDT7187L70CB	AM99C68-55PCB	IDT6168LA55P
AM2167-55DE	IDT6167SA55DM	AM2168-45/BRA	IDT6168SA45DB	AM99C88-20/BUC	IDT7164L200DB
AM2169-50DE	IDT6169SA45DM	AM9128-70LC	IDT6116SA70L32	AM99CS88-20/BUC	IDT7164L200L32B
AM99C641-45DEB	IDT7187L45CM	AM99C641-70/LMC	IDT7187L70L22B	AM99C68-70/BRA	IDT6168LA70DB
AM2167-55DEB	IDT6167SA55DM	AM2168-45/BUC	IDT6168SA45LB	AM99C88-20/BXC	IDT7164L200L32B
AM2169-50DEB	IDT6169SA45DM	AM9128-70LCB	IDT6116SA70L32	AM99CS88-20/BXC	IDT7164L200DB
AM99C641-45LC	IDT7187L45L22	AM99C641-70DC	IDT7187L70C	AM99C68-70DC	IDT6168LA70D
AM2167-55LC	IDT6167SA55L	AM2168-45DC	IDT6168SA45D	AM99C88-70/BUC	IDT7164L70L32B
AM2169-50LE	IDT6169SA45LM	AM9128-70PC	IDT6116SA70P	AM99CS88-70/BUC	IDT7164L70L32B
		AM99C641-70DCB	IDT7187L70C	AM99C68-70DCB	IDT6168LA70D
		AM2168-45DCB	IDT6168SA45D	AM99C88-70/BXC	IDT7164L70L32B
		AM9128-90/BJA	IDT6116SA90DB	AM99CS88-70/BXC	IDT7164L70DB
		AM99C641-70DE	IDT7187L70CM	AM99C68-70DMB	IDT6168LA70DB
		AM2168-45DE	IDT6168SA45DM	AM99C88-70DC	IDT7164L70D

NOTES:
A lower case ""x"" indicates the packages of the AMD part are unknown."
All AM99 series parts have 2 Volt data retention capability.

AMD CONT.	IDT
AM99C68-70PC	IDT6168LA70P
AM99C88-70DCB	IDT7164L70D
AM99C88H-35x	IDT7164L35x
AM99C68-70PCB	IDT6168LA70P
AM99C88-70DE	IDT7164L70DM
AM99C88H-45/x	IDT7164L45xB
AM99C88-70DEB	IDT7164L70DM
AM99CL68-45/BRA	IDT6168LA45DB
AM99C88-70LC	IDT7164L70L32
AM2130-10/BUC	IDT7130S100L52B*
AM99CL68-45DC	IDT6168LA45D
AM99C88-70LCB	IDT7164L70L32
AM2130-10/BXC	IDT7130S100CB
AM99CL68-45DCB	IDT6168LA45D
AM99C88-70LE	IDT7164L70L32M
AM2130-10DC	IDT7130S100C
AM99CL68-45PC	IDT6168LA45P
AM99C88-70LEB	IDT7164L70L32M
AM2130-10DCB	IDT7130S100C
AM99CL68-45PCB	IDT6168LA45P
AM99CL88-10/BUC	IDT7164L85L32B
AM2130-10JC	IDT7130S100J*
AM99CL68-55/BRA	IDT6168LA55DB
AM99CL88-10/BXC	IDT7164L85DB
AM2130-10LC	IDT7130S100L52*
AM99CL68-55DC	IDT6168LA55D
AM99CL88-12/BUC	IDT7164L85L32B
AM2130-10LCB	IDT7130S100L52*
AM99CL68-55DCB	IDT6168LA55D
AM99CL88-12/BXC	IDT7164L85DB
AM2130-10PC	IDT7130S100P
AM99CL68-55PC	IDT6168LA55P
AM99CL88-15/BUC	IDT7164L85L32B
AM2130-10PCB	IDT7130S100P
AM99CL68-55PCB	IDT6168LA55P
AM99CL88-15/BXC	IDT7164L85DB
AM2130-12/BUC	IDT7130S120L52B*
AM99CL68-70/BRA	IDT6168LA70DB
AM99CL88-70/BUC	IDT7164L70L32B
AM2130-12/BXC	IDT7130S120CB
AM99CL68-70DC	IDT6168LA70D
AM99CL88-70/BXC	IDT7164L70DB
AM2130-70/BXC	IDT7130S70CB
AM99CL68-70DCB	IDT6168LA70D
AM99CL88-70DC	IDT7164L70D
AM2130-70DC	IDT7130S70C
AM99CL68-70PC	IDT6168LA70P
AM99CL88-70DCB	IDT7164L70D
AM2130-70DCB	IDT7130S70C
AM99CL68-70PCB	IDT6168LA70P
AM99CL88-70LC	IDT7164L70L32
AM2130-70JC	IDT7130S70J*
AM99CL88-70LCB	IDT7164L70L32
AM2130-70LC	IDT7130S70L52*
AM99C88-10/BUC	IDT7164L100L32B
AM99CS88-10/BUC	IDT7164L100L32B
AM2130-70LCB	IDT7130S70L52*
AM99C88-10/BXC	IDT7164L100DB
AM99CS88-10/BXC	IDT7164L100DB
AM2130-70PC	IDT7130S70P
AM99C88-12/BUC	IDT7164L120L32B
AM99CS88-12/BUC	IDT7164L120L32B
AM2130-70PCB	IDT7130S70P

NOTES:
A lower case "x" indicates the packages of the AMD part are unknown.
All AM99 series parts have 2 Volt data retention capability.
An asterisk "*" indicates the IDT part is NOT pin for pin compatible.

LATTICE	IDT	LATTICE CONT.	IDT
SR16K4-25P	IDT6168SA25P	SR64K4-45CB	IDT7188SA45C
SR16K8-40R	IDT6116SA35L	SR16K4-40PB	IDT6168SA35P
SR64K1-45PB	IDT7187S45P	SR64E4-40P	IDT6198S35P
SR16K4-25PB	IDT6168SA25P	SR64K4-45CM	IDT7188SA45CB
SR16K8-40RB	IDT6116SA35L	SR16K4-40R	IDT6168SA35L
SR64K1-45R	IDT7187S45L	SR64E4-40P	IDT6198S35P
SR16K4-30C	IDT6168SA25D	SR64K4-45CMB	IDT7188SA45CB
SR16K8-40RM	IDT6116SA35LB	SR16K4-40RB	IDT6168SA35L
SR64K1-45RB	IDT7187S45L	SR64E4-40R	IDT6198S35L
SR16K4-30CB	IDT6168SA25D	SR64K4-45P	IDT7188SA45P
SR16K8-40RMB	IDT6116SA35LB	SR16K4-40RM	IDT6168SA35LB
SR64K1-45RM	IDT7187S45LB	SR64E4-40RB	IDT6198S35L
SR16K4-30CM	IDT6168SA25DB	SR64K4-45PB	IDT7188SA45P
SR16K8-40C	IDT6116SA35D	SR16K4-40RMB	IDT6168SA35LB
SR64K1-45RMB	IDT7187S45LB	SR64E4-40RM	IDT6198S35LB
SR16K4-30CMB	IDT6168SA25DB	SR64K4-55C	IDT7188SA55C
SR16K8-45CB	IDT6116SA45D	SR16K4-45C	IDT6168SA45D
SR64K1-55C	IDT7187S55C	SR64E4-40RMB	IDT6198S35LB
SR16K4-30P	IDT6168SA25P	SR64K4-55CB	IDT7188SA55C
SR16K8-45CM	IDT6116SA45DB	SR16K4-45CB	IDT6168SA45D
SR64K1-55CB	IDT7187S55C	SR64E4-45C	IDT6198S45C
SR16K4-30PB	IDT6168SA25P	SR64K4-55CM	IDT7188SA55CB
SR16K8-45CMB	IDT6116SA45DB	SR16K4-45CM	IDT6168SA45DB
SR64K1-55CM	IDT7187S55CB	SR64E4-45CB	IDT6198S45C
SR16K4-30R	IDT6168SA25L	SR64K4-55CMB	IDT7188SA55CB
SR16K8-45P	IDT6116SA45P	SR16K4-45CMB	IDT6168SA45DB
SR64K1-55CMB	IDT7187S55CB	SR64E4-45CM	IDT6198S45CB
SR16K4-30RB	IDT6168SA25L	SR64K4-55P	IDT7188SA55P
SR16K8-45PB	IDT6116SA45P	SR16K4-45P	IDT6168SA45P
SR64K1-55P	IDT7187S55P	SR64E4-45CMB	IDT6198S45CB
SR16K4-30RM	IDT6168SA25LB	SR64K4-55PB	IDT7188SA55P
SR16K8-45R	IDT6116SA45L	SR16K4-45PB	IDT6168SA45P
SR64K1-55PB	IDT7187S55P	SR64E4-45P	IDT6198S45P
SR16K4-30RMB	IDT6168SA25LB	SR16K4-45R	IDT6168SA45L
SR16K8-45RB	IDT6116SA45L	SR64E4-45P	IDT6198S45P
SR64K1-55R	IDT7187S55L	SR64K8-35P	IDT7164S35P
SR16K4-35C	IDT6168SA35D	SR16K4-45RB	IDT6168SA45L
SR16K8-45RM	IDT6116SA45LB	SR64E4-45R	IDT6198S45L
SR64K1-55RB	IDT7187S55L	SR64K8-35PB	IDT7164S35P
SR16K4-35CB	IDT6168SA35D	SR16K4-45RM	IDT6168SA45LB
SR16K8-45RMB	IDT6116SA45LB	SR64E4-45RB	IDT6198S45L
SR64K1-55RM	IDT7187S55LB	SR64K8-40C	IDT7164S35C
SR16K4-35CM	IDT6168SA35DB	SR16K4-45RMB	IDT6168SA45LB
SR64K1-55RMB	IDT7187S55LB	SR64E4-45RM	IDT6198S45LB
SR16K4-35CMB	IDT6168SA35DB	SR64K8-40CB	IDT7164S35C
SR256K1-x	IDT71257x	SR64E4-45RMB	IDT6198S45LB
SR16K4-35P	IDT6168SA35P	SR64K8-40CM	IDT7164S35CB
SR64K4-35P	IDT7188SA35P	SR16K8-30C	IDT6116SA30D
SR16K4-35PB	IDT6168SA35P	SR64E4-55C	IDT6198S55C
SR256K4-x	IDT71258x	SR64K8-40CMB	IDT7164S35CB
SR64K4-35PB	IDT7188SA35P	SR16K8-30CB	IDT6116SA30D
SR16K4-35R	IDT6168SA35L	SR64E4-55CB	IDT6198S55C
SR64K4-40C	IDT7188SA35C	SR64K8-40P	IDT7164S35P
SR16K4-35RB	IDT6168SA35L	SR16K8-30CM	IDT6116SA30DB
SR256K8-x	IDT71256x	SR64E4-55CM	IDT6198S55CB
SR64K4-40CB	IDT7188SA35C	SR64K8-40PB	IDT7164S35P
SR16K4-35RM	IDT6168SA35LB	SR16K8-30CMB	IDT6116SA30DB
SR64K4-40CM	IDT7188SA35CB	SR64E4-55CMB	IDT6198S55CB
SR16K4-35RMB	IDT6168SA35LB	SR64K8-40R	IDT7164S35L32
SR64E4-35P	IDT6198S35P	SR16K8-30P	IDT6116SA30P
SR64K4-40CMB	IDT7188SA35CB	SR64E4-55P	IDT6198S55P
SR16K4-40C	IDT6168SA35D	SR64K8-40RB	IDT7164S35L32
SR64E4-35P	IDT6198S35P	SR16K8-30PB	IDT6116SA30P
SR64K4-40P	IDT7188SA35P	SR64E4-55PB	IDT6198S55P
SR16K4-40CB	IDT6168SA35D	SR64K8-40RM	IDT7164S35L32B
SR64E4-40C	IDT6198S35C	SR16K8-30R	IDT6116SA30L
SR64K4-40PB	IDT7188SA35P	SR64E4-55R	IDT6198S55L
SR16K4-40CM	IDT6168SA35DB	SR64K8-40RMB	IDT7164S35L32B
SR64E4-40CB	IDT6198S35C	SR16K8-30RB	IDT6116SA30L
SR64K4-40R	IDT7188SA35L	SR64E4-55RB	IDT6198S55L
SR16K4-40CMB	IDT6168SA35DB	SR64K8-45C	IDT7164S45C
SR64E4-40CM	IDT6198S35CB	SR16K8-30RM	IDT6116SA30LB
SR64K4-40RMB	IDT7188SA35LB	SR64E4-55RM	IDT6198S55LB
SR16K4-40P	IDT6168SA35P	SR64K8-45CB	IDT7164S45C
SR64E4-40CMB	IDT6198S35CB	SR16K8-30RMB	IDT6116SA30LB

LATTICE CONT.	IDT
SR64E4-55RMB	IDT6198S55LB
SR64K8-45CM	IDT7164S45CB
SR16K8-35C	IDT6116SA35D
SR64K8-45CMB	IDT7164S45CB
SR16K8-35CB	IDT6116SA35D
SR64K1-35C	IDT7187S35C
SR64K8-45P	IDT7164S45P
SR16K8-35CM	IDT6116SA35DB
SR64K1-35CB	IDT7187S35C
SR64K8-45PB	IDT7164S45P
SR16K8-35CMB	IDT6116SA35DB
SR64K1-35CM	IDT7187S35CM
SR64K8-45R	IDT7164S45L32
SR16K8-35P	IDT6116SA35P
SR64K1-35CMB	IDT7187S35CM
SR64K8-45RB	IDT7164S45L32
SR16K8-35PB	IDT6116SA35P
SR64K1-35P	IDT7187S35P
SR64K8-45RM	IDT7164S45L32B
SR16K8-35R	IDT6116SA35L
SR64K1-35PB	IDT7187S35P
SR64K8-45RMB	IDT7164S45L32B
SR16K8-35RB	IDT6116SA35L
SR64K1-35R	IDT7187S35L
SR64K8-55C	IDT7164S55C
SR16K8-35RM	IDT6116SA35LB
SR64K1-35RB	IDT7187S35L
SR64K8-55CB	IDT7164S55C
SR16K8-35RMB	IDT6116SA35LB
SR64K1-35RM	IDT7187S35LM
SR64K8-55CM	IDT7164S55CB
SR16K8-40C	IDT6116SA35D
SR64K1-35RMB	IDT7187S35LM
SR64K8-55CMB	IDT7164S55CB
SR16K8-40CB	IDT6116SA35D
SR64K1-45C	IDT7187S45C
SR64K8-55P	IDT7164S55P
SR16K8-40CM	IDT6116SA35DB
SR64K1-45CB	IDT7187S45C
SR64K8-55PB	IDT7164S55P
SR16K8-40CMB	IDT6116SA35DB
SR64K1-45CM	IDT7187S45CM
SR64K8-55R	IDT7164S55L32
SR16K8-40P	IDT6116SA35P
SR64K1-45CMB	IDT7187S45CM
SR64K8-55RB	IDT7164S55L32
SR16K8-40PB	IDT6116SA35P
SR64K1-45P	IDT7187S45P
SR64K8-55RM	IDT7164S55L32B
SR64K8-55RMB	IDT7164S55L32B

CYPRESS	IDT
CY7C128-25DC	IDT6116SA25D
CY7C161-25DC*	IDT71981S25C
CY7C164L-35DMB	IDT7188L35CB
CY7C128-25LC	IDT6116SA25L24
CY7C161-35DC*	IDT71981S35C
CY7C164L-35LC	IDT7188L35L
CY7C128-25PC	IDT6116SA25P
CY7C161-35DMB*	IDT71981S35CB
CY7C164L-35LMB	IDT7188L35LB
CY7C128-25SC	IDT6116SA25SO

NOTES:
A lower case "x" indicates the packages of the AMD part are unknown.
All AM99 series parts have 2 Volt data retention capability.
An asterisk "*" indicates the IDT part is NOT pin for pin compatible.

CYPRESS CONT.	IDT
CY7C161-35LC*	IDT71981S35L
CY7C164L-35PC	IDT7188L35P
CY7C128-35DC	IDT6116SA35D
CY7C161-35PC*	IDT71981S35P
CY7C164L-45DC	IDT7188L45C
CY7C128-35DMB	IDT6116SA35DB
CY7C161-45DC*	IDT71981S45C
CY7C164L-45DMB	IDT7188L45CB
CY7C128-35LC	IDT6116SA35L24
CY7C161-45DMB*	IDT71981S45CB
CY7C164L-45LC	IDT7188L35L
CY7C128-35LMB	IDT6116SA35L24B
CY7C161-45LC*	IDT71981S45L
CY7C164L-45LMB	IDT7188L45LB
CY7C128-35PC	IDT6116SA35P
CY7C161-45LMB*	IDT71981S45LB
CY7C164L-45PC	IDT7188L45P
CY7C128-35SC	IDT6116SA35SO
CY7C161L-25DC*	IDT71981L25C
CY7C128-45DC	IDT6116SA45D
CY7C161L-35DC*	IDT71981L35C
CY7C166-25DC	IDT6198S25C
CY7C128-45DMB	IDT6116SA45DB
CY7C161L-35DMB*	IDT71981L35CB
CY7C166-25PC	IDT6198S25P
CY7C128-45LC	IDT6116SA45L24
CY7C161L-35LC*	IDT71981L35L24
CY7C166-35DC	IDT6198S35C
CY7C128-45LMB	IDT6116SA45L24B
CY7C161L-35LMB*	IDT71981L35L24B
CY7C166-35DMB	IDT6198S35CB
CY7C128-45PC	IDT6116SA45P
CY7C161L-45DC*	IDT7198LS45C
CY7C166-35LC	IDT6198S35L
CY7C128-45SC	IDT6116SA45SO
CY7C161L-45DMB*	IDT71981L45CB
CY7C166-35LMB	IDT6198S35LB
CY7C128-55DC	IDT6116SA55D
CY7C161L-45LC*	IDT71981L45L24
CY7C166-35PC	IDT6198S35P
CY7C128-55DMB	IDT6116SA55DB
CY7C161L-45LMB*	IDT71981L45L24B
CY7C166-45DC	IDT6198S45C
CY7C128-55LC	IDT6116SA55L24
CY7C166-45DMB	IDT6198S45CB
CY7C128-55LMB	IDT6116SA55L24B
CY7C162-25DC*	IDT71982S25C
CY7C166-45LC	IDT6198S45L
CY7C128-55PC	IDT6116SA55P
CY7C162-35DC*	IDT71982S35C
CY7C166-45LMB	IDT6198S45LB
CY7C128-55SC	IDT6116SA55S0
CY7C162-35DMB*	IDT71982S35CB
CY7C166-45PC	IDT6198S45P
CY7C162-35LC*	IDT71982S35L
CY7C166L-25DC	IDT6198L25C
CY7C130-45DC	IDT7130S45C
CY7C162-35LMB*	IDT71982S35LB
CY7C166L-25PC	IDT6198L25P
CY7C130-45LC	IDT7130S45L52
CY7C162-45DC*	IDT71982S45C
CY7C166L-35DC	IDT6198L35C
CY7C130-45PC	IDT7130S45P
CY7C162-45DMB*	IDT71982S45CB
CY7C166L-35DMB	IDT6198L35CB
CY7C130-55DC	IDT7130S55C
CY7C162-45LC*	IDT71982S45L
CY7C166L-35LC	IDT6198L35L
CY7C130-55LC	IDT7130S55L52
CY7C162-45LMB*	IDT71982S45LB
CY7C166L-35LMB	IDT6198L35LB
CY7C130-55PC	IDT7130S55P
CY7C162L-25DC*	IDT71982L25C
CY7C166L-35PC	IDT6198L35P
CY7C162L-35DC*	IDT71982L35C

CYPRESS CONT.	IDT
CY7C166L-45DC	IDT6198L45C
CY7C132-35DC	IDT7132S35C
CY7C162L-35DMB*	IDT71982L35CB
CY7C166L-45DMB	IDT6198L45CB
CY7C132-35LC	IDT7132S35L52
CY7C162L-35LC*	IDT71982L35L
CY7C166L-45LC	IDT6198L45L
CY7C132-35PC	IDT7132S35P
CY7C162L-35LMB*	IDT71982L35LB
CY7C166L-45LMB	IDT6198L45LB
CY7C132-45DC	IDT7132S45C
CY7C162L-45DC*	IDT71982L45C
CY7C166L-45PC	IDT6198L45P
CY7C132-45LC	IDT7132S45L52
CY7C162L-45DMB*	IDT71982L45CB
CY7C132-45PC	IDT7132S45P
CY7C162L-45LC*	IDT71982L45L
CY7C167-25PC	IDT6167SA25P
CY7C132-55DC	IDT7132S55C
CY7C162L-45LMB*	IDT71982L45LB
CY7C167-25DC	IDT6167SA25D
CY7C132-55LC	IDT7132S55L52
CY7C167-25LC	IDT6167SA25L
CY7C132-55PC	IDT7132S55P
CY7C164-25DC	IDT7188S25C
CY7C167-35PC	IDT6167SA35P
CY7C164-25PC	IDT7188S25P
CY7C167-35DC	IDT6167SA35D
CY7C140-45DC	IDT7140S45C
CY7C164-35DC	IDT7188S35C
CY7C167-35LC	IDT6167SA35L
CY7C140-45LC	IDT7140S45L52
CY7C164-35DMB	IDT7188S35CB
CY7C167-35DMB	IDT6167SA35DB
CY7C140-45PC	IDT7140S45P
CY7C164-35LC	IDT7188S35L
CY7C167-35LMB	IDT6167SA35LB
CY7C140-55DC	IDT7140S55C
CY7C164-35LMB	IDT7188S35LB
CY7C167-45PC	IDT6167SA45P
CY7C140-55LC	IDT7140S55L52
CY7C164-35PC	IDT7188S35P
CY7C167-45DC	IDT6167SA45D
CY7C140-55PC	IDT7140S55P
CY7C164-45DC	IDT7188S45C
CY7C167-45LC	IDT6167SA45L
CY7C164-45DMB	IDT7188S45CB
CY7C167-45DMB	IDT6167SA45DB
CY7C142-35DC	IDT7142S35C
CY7C164-45LC	IDT7188S35L
CY7C167-45LMB	IDT6167SA45LB
CY7C142-35LC	IDT7142S35L52
CY7C164-45LMB	IDT7188S45LB
CY7C167L-25DC	IDT6167LA25D
CY7C142-35PC	IDT7142S35P
CY7C164-45PC	IDT7188S45P
CY7C167L-25LC	IDT6167LA25L
CY7C142-45DC	IDT7142S45C
CY7C164L-25DC	IDT7188L25C
CY7C167L-25PC	IDT6167LA25P
CY7C142-45LC	IDT7142S45L52
CY7C164L-25PC	IDT7188L25P
CY7C167L-35DC	IDT6167LA35D
CY7C142-45PC	IDT7142S45P
CY7C164L-35DC	IDT7188L35C
CY7C167L-35LC	IDT6167LA35L
CY7C142-55DC	IDT7142S55C
CY7C167L-35PC	IDT6167LA35P
CY7C142-55LC	IDT7142S55L52
CY7C142-55PC	IDT7142S55P
CY7C168-25DC	IDT6168SA25D
CY7C171-45LC	IDT71681SA45L
CY7C186-35DC	IDT7164S35D
CY7C168-25LC	IDT6168SA25L
CY7C171-45LMB	IDT71681SA45LB

CYPRESS CONT.	IDT
CY7C186-35PC	IDT7164S35P
CY7C168-25PC	IDT6168SA25P
CY7C171-45PC	IDT71681SA45P
CY7C186-45DC	IDT7164S45D
CY7C168-25SC	IDT6168SA25SO
CY7C171L-25DC	IDT71681LA25D
CY7C186-45DMB	IDT7164S45DB
CY7C168-35DC	IDT6168SA35D
CY7C171L-25LC	IDT71681LA25L
CY7C186-45PC	IDT7164S45P
CY7C168-35DMB	IDT6168SA35DB
CY7C171L-25PC	IDT71681LA25P
CY7C186-55DC	IDT7164S55D
CY7C168-35LC	IDT6168SA35L
CY7C171L-35DC	IDT71681LA35D
CY7C186-55DMB	IDT7164S55DB
CY7C168-35LMB	IDT6168SA35LB
CY7C171L-35LC	IDT71681LA35L
CY7C186-55PC	IDT7164S55P
CY7C168-35PC	IDT6168SA35P
CY7C171L-35PC	IDT71681LA35P
CY7C186L-35DC	IDT7164L35D
CY7C168-35SC	IDT6168SA35SO
CY7C186L-35PC	IDT7164L35P
CY7C168-45DC	IDT6168SA45D
CY7C172-25DC	IDT71682SA25D
CY7C186L-45DC	IDT7164L45D
CY7C168-45DMB	IDT6168SA45DB
CY7C172-25LC	IDT71682SA25L
CY7C186L-45DMB	IDT7164L45DB
CY7C168-45LC	IDT6168SA45L
CY7C172-25PC	IDT71682SA25P
CY7C186L-45PC	IDT7164L45P
CY7C168-45LMB	IDT6168SA45LB
CY7C172-35DC	IDT71682SA35D
CY7C186L-55DC	IDT7164L55D
CY7C168-45PC	IDT6168SA45P
CY7C172-35DMB	IDT71682SA35DB
CY7C186L-55DMB	IDT7164L55DB
CY7C168-45SC	IDT6168SA45SO
CY7C172-35LC	IDT71682SA35L
CY7C186L-55PC	IDT7164L55P
CY7C168L-25DC	IDT6168LA25D
CY7C172-35LMB	IDT71682SA35LB
CY7C168L-25LC	IDT6168LA25L
CY7C172-35PC	IDT71682SA35P
CY7C187-25DC	IDT7187S25D
CY7C168L-25PC	IDT6168LA25P
CY7C172-45DC	IDT71682SA45D
CY7C187-25PC	IDT7187S25P
CY7C168L-25SC	IDT6168LA25SO
CY7C172-45DMB	IDT71682SA45DB
CY7C187-35DC	IDT7187S35D
CY7C168L-35DC	IDT6168LA35D
CY7C172-45LC	IDT71682SA45L
CY7C187-35DMB	IDT7187S35DB
CY7C168L-35LC	IDT6168LA35L
CY7C172-45LMB	IDT71682SA45LB
CY7C187-35LC	IDT7187S35L
CY7C168L-35PC	IDT6168LA35P
CY7C172-45PC	IDT71682SA45P
CY7C187-35LMB	IDT7187S35LB
CY7C168L-35SC	IDT6168LA35SO

CYPRESS CONT.	IDT
CY7C172L-25DC	IDT71682LA25D
CY7C187-35PC	IDT7187S35P
CY7C172L-25LC	IDT71682LA25L
CY7C187-45DC	IDT7187S45D
CY7C169-25DC	IDT6169SA25D
CY7C172L-25PC	IDT71682LA25P
CY7C187-45DMB	IDT7187S45DB
CY7C169-25LC	IDT6169SA25L
CY7C172L-35DC	IDT71682LA35D
CY7C187-45LC	IDT7187S45L
CY7C169-25PC	IDT6169SA25P
CY7C172L-35LC	IDT71682LA35L
CY7C187-45LMB	IDT7187S45LB
CY7C169-35DC	IDT6169SA35D
CY7C172L-35PC	IDT71682LA35P
CY7C187-45PC	IDT7187S45P
CY7C169-35DMB	IDT6169SA35DB
CY7C187L-25DC	IDT7187L25D
CY7C169-35LC	IDT6169SA35L
CY7C185-35DC	IDT7164S35D
CY7C187L-25PC	IDT7187L25P
CY7C169-35LMB	IDT6169SA35LB
CY7C185-35PC	IDT7164S35P
CY7C187L-35DC	IDT7187L35D
CY7C169-35PC	IDT6169SA35P
CY7C185-45DC	IDT7164S45D
CY7C187L-35DMB	IDT7187L35DB
CY7C169-40DC	IDT6169SA35D
CY7C185-45DMB	IDT7164S45DB
CY7C187L-35LC	IDT7187L35L
CY7C169-40DMB	IDT6169SA35DB
CY7C185-45LC	IDT7164S45L28
CY7C187L-35LMB	IDT7187L35LB
CY7C169-40LC	IDT6169SA35L
CY7C185-45LMB	IDT7164S45L28B
CY7C187L-35PC	IDT7187L35P
CY7C169-40LMB	IDT6169SA35LB
CY7C185-45PC	IDT7164S45P
CY7C187L-45DC	IDT7187L45D
CY7C169-40PC	IDT6169SA35P
CY7C185-55DC	IDT7164S55D
CY7C187L-45DMB	IDT7187L45DB
CY7C169L-25DC	IDT6169LA25D
CY7C185-55DMB	IDT7164S55DB
CY7C187L-45LC	IDT7187L45L
CY7C169L-25LC	IDT6169LA25L
CY7C185-55LC	IDT7164S55L28
CY7C187L-45LMB	IDT7187L45LB
CY7C169L-25PC	IDT6169LA25P
CY7C185-55LMB	IDT7164S55L28B
CY7C187L-45PC	IDT7187L45P
CY7C169L-35DC	IDT6169LA35D
CY7C185-55PC	IDT7164S55P
CY7C169L-35LC	IDT6169LA35L
CY7C185L-35DC	IDT7164L35D
CY7C198-45DC	IDT71256S45D
CY7C169L-35PC	IDT6169LA35P
CY7C185L-35PC	IDT7164L35P
CY7C198-45PC	IDT71256S45P
CY7C185L-45DC	IDT7164L45D
CY7C198-55DC	IDT71256S55D
CY7C171-25DC	IDT71681SA25D
CY7C185L-45DMB	IDT7164L45DB
CY7C198-55DMB	IDT71256S55DB
CY7C171-25LC	IDT71681SA25L
CY7C185L-45LC	IDT7164L45L28
CY7C198-55PC	IDT71256S55P
CY7C171-25PC	IDT71681SA25P
CY7C185L-45LMB	IDT7164L45L28B
CY7C171-35DC	IDT71681SA35D
CY7C185L-45PC	IDT7164L45P
CY7C194-35DC	IDT71258S35T
CY7C171-35DMB	IDT71681SA35DB
CY7C185L-55DC	IDT7164L55D
CY7C194-45DC	IDT71258S45T

CYPRESS CONT.	IDT
CY7C171-35LC	IDT71681SA35L
CY7C185L-55DMB	IDT7164L55DB
CY7C194-45DMB	IDT71258S45TB
CY7C171-35LMB	IDT71681SA35LB
CY7C185L-55LC	IDT7164L55L28
CY7C171-35PC	IDT71681SA35P
CY7C185L-55LMB	IDT7164L55L28B
CY7C197-35DC	IDT71257S35T
CY7C171-45DC	IDT71681SA45D
CY7C185L-55PC	IDT7164L55P
CY7C197-45DC	IDT71257S45T
CY7C171-45DMB	IDT71681SA45DB
CY7C197-45DMB	IDT71257S45TB

MATRA-HARRIS	IDT
HM1-2064-2	IDT7164L150DM
HM4-65261C-2	IDT6167SA100LM
HM1-65728N-5	IDT6116SA55D
HM1-2064-5	IDT7164L70D
HM4-65261C-5	IDT6167SA55L
HM3-65728K-5	IDT6116SA35TP
HM1-2064-8	IDT7164L150DB
HM4-65261C-8	IDT6167SA100LB
HM3-65728M-5	IDT6116SA45TP
HM3-2064-5	IDT7164L70P
HM4-65261S-2	IDT6167SA70LM
HM3-65728N-5	IDT6116SA55TP
HM3-2064U-5	IDT7164L70P
HM4-65261S-5	IDT6167SA55L
HM4-65728K-5	IDT6116SA35L24
HM4-2064-2	IDT7164L150L32M
HM4-65261S-8	IDT6167SA70LB
HM4-65728M-2	IDT6116SA45L24M
HM4-2064-5	IDT7164L70L32
HM1-65728M-5	IDT6116SA45L24
HM4-2064-8	IDT7164L150L32B
HM1-65263-2	IDT6167LA55DM
HM1-65728N-2	IDT6116SA55L24M
HMT-2064-5	IDT7164L70SO
HM1-65263-5	IDT6167LA45D
HM1-65728N-5	IDT6116SA55L24
HMT-2064U-5	IDT7164L70S0
HM3-65263-5	IDT6167LA45P
HM4-65263-2	IDT6167LA55LM
HM1-65767H-5	IDT6167SA25D
HM1-6116-2	IDT6116SA90DM
HM4-65263-5	IDT6167LA45L
HM1-65767K-2	IDT6167SA35DM
HM1-6116-5	IDT6116SA90D
HM1-65767K-5	IDT6167SA35D
HM1-6116-8	IDT6116SA120DB
HM1-65641-2	IDT7164L85DM
HM1-65767K-8	IDT6167SA35DB
HM1-6116L-2	IDT6116LA90DM
HM1-65641-5	IDT7164L55D
HM1-65767M-2	IDT6167SA45DM
HM1-6116L-5	IDT6116LA90D
HM1-65641-8	IDT7164L85DB
HM1-65767M-5	IDT6167SA45D
HM1-6116L-8	IDT6116LA120DB
HM1-65641S-2	IDT7164L55DM
HM1-65767M-8	IDT6167SA45DB
HM3-6116-5	IDT6116SA90P
HM1-65641S-5	IDT7164L45D
HM3-65767H-5	IDT6167SA25P
HM3-6116L-5	IDT6116LA90P
HM1-65641S-8	IDT7164L55DB
HM3-65767K-5	IDT6167SA35P
HM4-6116-2	IDT6116SA90L32M
HM3-65641-5	IDT7164L55P
HM3-65767M-5	IDT6167SA45P
HM4-6116-5	IDT6116SA90L32
HM4-65641-2	IDT7164L85L32M
HM4-65767H-5	IDT6167SA25L

NOTES:
A lower case "x" indicates the speed and/or package of the part are unknown."
*The CY7C161/162 come in a 300 mil package vs. 400 mil IDT71981/982.

MATRA-HARRIS CONT.	IDT
HM4-6116-8	IDT6116SA120L32B
HM4-65641-5	IDT7164L55L32
HM4-65767K-2	IDT6167SA35LM
HM4-6116L-2	IDT6116LA90L32M
HM4-65641-8	IDT7164L85L32B
HM4-65767K-5	IDT6167SA35L
HM4-6116L-5	IDT6116LA90L32
HM4-65767K-8	IDT6167SA35LB
HM1-65681-2	IDT6168LA85DM
HM4-65767M-2	IDT6167SA45LM
HM1-65161-2	IDT6116LA90DM
HM1-65681-5	IDT6168LA55D
HM4-65767M-5	IDT6167SA45L
HM1-65161-5	IDT6116LA70D
HM1-65681-8	IDT6168LA85DB
HM4-65767M-8	IDT6167SA45LB
HM1-65161-8	IDT6116LA90DB
HM1-65681B-2	IDT6168LA70DM
HM3-65161-5	IDT6116LA70P
HM1-65681B-5	IDT6168LA55D
HM1-65768H-5	IDT6168SA25D
HM4-65161-2	IDT6116LA90L32M
HM1-65681C-2	IDT6168SA85DM
HM1-65768K-2	IDT6168SA35DM
HM4-65161-5	IDT6116LA70L32
HM1-65681C-5	IDT6168SA55D
HM1-65768K-5	IDT6168SA35D
HM4-65161-8	IDT6116LA90L32B
HM1-65681C-8	IDT6168SA85DB
HM1-65768K-8	IDT6168SA35DB
HM1-65681S-2	IDT6168SA70DM
HM1-65768M-2	IDT6168SA45DM
HM1-65163-2	IDT6116LA85DM
HM1-65681S-5	IDT6168SA55D
HM1-65768M-5	IDT6168SA45D
HM1-65163-5	IDT6116LA55D
HM1-65681S-8	IDT6168SA70DB
HM1-65768M-8	IDT6168SA45DB
HM1-65163-8	IDT6116LA85DB
HM3-65681-5	IDT6168LA55P
HM3-65768H-5	IDT6168SA25P
HM3-65163-5	IDT6116LA45P
HM3-65681B-5	IDT6168LA55P
HM3-65768K-5	IDT6168SA35P
HM4-65163-2	IDT6116LA55LM
HM3-65681C-5	IDT6168SA55P
HM3-65768M-5	IDT6168SA45P
HM4-65163-5	IDT6116LA45L
HM3-65681S-5	IDT6168SA55P
HM4-65768H-5	IDT6168SA25L
HM4-65163-8	IDT6116LA45LB
HM4-65681-2	IDT6168LA85LM
HM4-65768K-2	IDT6168SA35LMHM
4-65681-5	IDT6168LA55L
HM4-65768K-5	IDT6168SA35L
HM1-65261-2	IDT6167LA85DM
HM4-65681-8	IDT6168LA85LB
HM4-65768K-8	IDT6168SA35LB
HM1-65261-5	IDT6167LA55D
HM4-65681B-2	IDT6168LA70LM
HM4-65768M-2	IDT6168SA45LM
HM1-65261-8	IDT6167LA85DB
HM4-65681B-5	IDT6168LA55L

NOTES:
A lower case "x" indicates the speed and/or package of the part are unknown."
*The CY7C161/162 come in a 300 mil package vs. 400 mil IDT71981/982.

MATRA-HARRIS CONT.	IDT
HM4-65768M-5	IDT6168SA45L
HM1-65261B-2	IDT6167LA70DM
HM4-65681C-2	IDT6168SA85LM
HM4-65768M-8	IDT6168SA45LB
HM1-65261B-5	IDT6167LA55D
HM4-65681C-5	IDT6168SA55L
HM1-65261B-8	IDT6167LA70DB
HM4-65681C-8	IDT6168SA85LB
HM1-65769H-5	IDT6169SA25D
HM1-65261C-2	IDT6167SA100DM
HM4-65681S-2	IDT6168SA70LM
HM1-65769K-2	IDT6169SA35DM
HM1-65261C-5	IDT6167SA55D
HM4-65681S-5	IDT6168SA55L
HM1-65769K-5	IDT6169SA35D
HM1-65261C-8	IDT6167SA100DB
HM4-65681S-8	IDT6168SA70LB
HM1-65769K-8	IDT6169SA35DB
HM1-65261S-2	IDT6167SA70DM
HM1-65769M-2	IDT6169SA45DM
HM1-65261S-5	IDT6167SA55D
HM1-65682-2	IDT6168LA55DM
HM1-65769M-5	IDT6169SA45D
HM1-65261S-8	IDT6167SA70DB
HM1-65682-5	IDT6168LA45D
HM1-65769M-8	IDT6169SA45DB
HM3-65261-5	IDT6167LA55P
HM1-65682-8	IDT6168LA45DB
HM3-65769H-5	IDT6169SA25P
HM3-65261B-5	IDT6167LA55P
HM3-65682-5	IDT6168LA45P
HM3-65769K-5	IDT6169SA35P
HM3-65261C-5	IDT6167SA55P
HM4-65682-2	IDT6168LA55LM
HM3-65769M-5	IDT6169SA45P
HM3-65261S-5	IDT6167SA55P
HM4-65682-5	IDT6168LA45L
HM4-65769H-5	IDT6169SA25L
HM4-65261-2	IDT6167LA85LM
HM4-65682-8	IDT6168LA55LB
HM4-65769K-2	IDT6169SA35LM
HM4-65261-5	IDT6167LA55L
HM4-65769K-5	IDT6169SA35L
HM4-65261-8	IDT6167LA85LB
HM1-65728K-5	IDT6116SA35D
HM4-65769K-8	IDT6169SA35LB
HM4-65261B-2	IDT6167LA70LM
HM1-65728M-2	IDT6116SA45DM
HM4-65769M-2	IDT6169SA45LM
HM4-65261B-5	IDT6167LA55L
HM1-65728M-5	IDT6116SA45D
HM4-65769M-5	IDT6169SA45L
HM4-65261B-8	IDT6167LA70LB
HM1-65728N-2	IDT6116SA55DM
HM4-65769M-8	IDT6169SA45LB

PERFORMANCE	IDT
P4C116-25CC	IDT6116SA25TD
P4C168-35CC	IDT6168SA35D
P4C1681L-25LM	IDT71681LA25LM
P4C116-25LC	IDT6116SA25L24
P4C168-35CM	IDT6168SA35DM
P4C1681L-25LMB	IDT71681LA25LB
P4C116-25PC	IDT6116SA25TP
P4C168-35CMB	IDT6168SA35DB
P4C1681L-25PC	IDT71681LA25P
P4C116-30CC	IDT6116SA30TD
P4C168-35LC	IDT6168SA35L
P4C1681L-35CC	IDT71681LA35D
P4C116-30LC	IDT6116SA30L24
P4C168-35LM	IDT6168SA35LM
P4C1681L-35CM	IDT71681LA35DM
P4C116-30PC	IDT6116SA30TP

PERFORMANCE CONT.	IDT
P4C168-35LMB	IDT6168SA35LB
P4C1681L-35CMB	IDT71681LA35DB
P4C116-35CC	IDT6116SA35TD
P4C168-35PC	IDT6168SA35P
P4C1681L-35LC	IDT71681LA35L
P4C116-35CM	IDT6116SA35TDM
P4C168-45CM	IDT6168SA45DM
P4C1681L-35LM	IDT71681LA35LM
P4C116-35CMB	IDT6116SA35TDB
P4C168-45CMB	IDT6168SA45CB
P4C1681L-35LMB	IDT71681LA35LB
P4C116-35LC	IDT6116SA35L24
P4C168-45LM	IDT6168SA45LM
P4C1681L-35PC	IDT71681LA35P
P4C116-35LM	IDT6116SA35L24M
P4C1681L-45CC	IDT71681LA45D
P4C116-35LMB	IDT6116SA35L24B
P4C168-45LMB	IDT6168SA45LB
P4C1681L-45CM	IDT71681LA45DM
P4C116-35PC	IDT6116SA35TP
P4C168L-20CC	IDT6168LA20D
P4C1681L-45CMB	IDT71681LA45CB
P4C116L-25CC	IDT6116LA25TD
P4C168L-20LC	IDT6168LA20L
P4C1681L-45LC	IDT71681LA45L
P4C116L-25LC	IDT6116LA25L24
P4C168L-20PC	IDT6168LA20P
P4C1681L-45LM	IDT71681LA45LM
P4C116L-25PC	IDT6116LA25TP
P4C168L-25CC	IDT6168LA25D
P4C1681L-45LMB	IDT71681LA45LB
P4C116L-30CC	IDT6116LA30TD
P4C168L-25CM	IDT6168LA25DM
P4C1681L-45PC	IDT71681LA45P
P4C116L-30LC	IDT6116LA30L24
P4C168L-25CMB	IDT6168LA25DB
P4C116L-30PC	IDT6116LA30TP
P4C168L-25LC	IDT6168LA25L
P4C1682-20CC	IDT71682SA20D
P4C116L-35CC	IDT6116LA35TD
P4C168L-25LM	IDT6168LA25LM
P4C1682-20LC	IDT71682SA20L
P4C116L-35CM	IDT6116LA35TDM
P4C168L-25LMB	IDT6168LA25LB
P4C1682-20PC	IDT71682SA20P
P4C116L-35CMB	IDT6116LA35TDB
P4C168L-25PC	IDT6168LA25P
P4C1682-25CC	IDT6116LA35L24
P4C168L-35CC	IDT6168LA35D
P4C1682-25CM	IDT71682SA25DM
P4C116L-35LM	IDT6116LA35L24M
P4C168L-35CM	IDT6168LA35DM
P4C1682-25CMB	IDT71682SA25DB
P4C116L-35LMB	IDT6116LA35L24B
P4C168L-35CMB	IDT6168LA35DB
P4C1682-25LC	IDT71682SA25L
P4C116L-35PC	IDT6116LA35TP
P4C168L-35LC	IDT6168LA35L
P4C1682-25LM	IDT71682SA25LM
P4C168L-35LM	IDT6168LA35LM
P4C1682-25LMB	IDT71682SA25LB
P4C164-30CC	IDT7164S30TC
P4C168L-35LMB	IDT6168LA35LB
P4C1682-25PC	IDT71682SA25P
P4C164-30LC	IDT7164S30L28
P4C168L-35PC	IDT6168LA35P
P4C1682-35CC	IDT71682SA35D
P4C164-30PC	IDT7164S30TP
P4C168L-45CM	IDT6168LA45DM
P4C1682-35CM	IDT71682SA35DM
P4C164-35CC	IDT7164S35TC
P4C168L-45CMB	IDT6168LA45CB
P4C1682-35CMB	IDT71682SA35DB
P4C164-35CM	IDT7164S35TCM
P4C168L-45LM	IDT6168LA45LM

PERFORMANCE CONT.	IDT	PERFORMANCE CONT.	IDT	PERFORMANCE CONT.	IDT
P4C1682-35LC	IDT71682SA35L	P4C164L-45LM	IDT7164L45L28M	P4C198L-55LMB	IDT6198L55LB
P4C164-35CMB	IDT7164S35TCB	P4C1681-45CMB	IDT71681SA45CB	P4C187L-2LC	IDT7187L25L22
P4C168L-45LMB	IDT6168LA45LB	P4C1682L-35CM	IDT71682LA35DM	P4C188L-45PC	IDT7188L45P
P4C1682-35LM	IDT71682SA35LM	P4C164L-45LMB	IDT7164L45L28B	P4C187L-30CM	IDT7187L30CM
P4C164-35LC	IDT7164S30L28	P4C1681-45LC	IDT71681SA45L	P4C188L-55CM	IDT7188L55CM
P4C1682-35LMB	IDT71682SA35LB	P4C1682L-35CMB	IDT71682LA35DB	P4C1981-25CC	IDT71981S25C
P4C164-35LM	IDT7164S35L28M	P4C1681-45LM	IDT71681SA45LM	P4C187L-30CMB	IDT7187L30CB
P4C1681-20CC	IDT71681SA20D	P4C1682L-35LC	IDT71682LA35L	P4C188L-55CMB	IDT7188L55CB
P4C1682-35PC	IDT71682SA35P	P4C168-20CC	IDT6168SA20D	P4C1981-25LC	IDT71981S25L
P4C164-35LMB	IDT7164S35L28B	P4C1681-45LMB	IDT71681SA45LB	P4C187L-30LM	IDT7187L30L22M
P4C1681-20LC	IDT71681SA20L	P4C1682L-35LM	IDT71682LA35LM	P4C188L-55LM	IDT7188L55LM
P4C1682-45CC	IDT71682SA45D	P4C168-20LC	IDT6168SA20L	P4C1981-30CC	IDT71981S30C
P4C164-35PC	IDT7164S35TP	P4C1681-45PC	IDT71681SA45P	P4C187L-30LMB	IDT7187L35L22B
P4C1681-20PC	IDT71681SA20P	P4C1682L-35LMB	IDT71682LA35LB	P4C188L-55LMB	IDT7188L55LB
P4C1682-45CM	IDT71682SA45DM	P4C168-20PC	IDT6168SA20P	P4C1981-30CM	IDT71981S30CM
P4C164-45CM	IDT7164S45TCM	P4C1681L-20CC	IDT71681LA20D	P4C187L-35CM	IDT7187L35CM
P4C1681-25CC	IDT71681SA25D	P4C1682L-35PC	IDT71682LA35P	P4C1981-30CMB	IDT71981S30CB
P4C1682-45CMB	IDT71682SA45CB	P4C168-25CC	IDT6168SA25D	P4C187L-35CMB	IDT7187L35CB
P4C164-45CMB	IDT7164S45TCB	P4C1681L-20LC	IDT71681LA20L	P4C198-25CC	IDT6198S25C
P4C1681-25CM	IDT71681SA25DM	P4C1682L-45CC	IDT71682LA45D	P4C1981-30LC	IDT71981S30L
P4C1682-45LC	IDT71682SA45L	P4C168-25CM	IDT6168SA25DM	P4C187L-35LM	IDT7187L30L22M
P4C164-45LM	IDT7164S45L28M	P4C1681L-20PC	IDT71681LA20P	P4C198-25LC	IDT6198S25L
P4C1681-25CMB	IDT71681SA25DB	P4C1682L-45CM	IDT71682LA45DM	P4C1981-30LM	IDT71981S30LM
P4C1682-45LM	IDT71682SA45LM	P4C168-25CMB	IDT6168SA25DB	P4C187L-35LMB	IDT7187L35L22B
P4C164-45LMB	IDT7164S45L28B	P4C1681L-25CC	IDT71681LA25D	P4C198-25PC	IDT6198S25P
P4C1681-25LC	IDT71681SA25L	P4C1682L-45CMB	IDT71682LA45CB	P4C1981-30LMB	IDT71981S30LB
P4C1682-45LMB	IDT71682SA45LB	P4C168-25LC	IDT6168SA25L	P4C198-30CC	IDT6198S30C
P4C164L-30CC	IDT7164L30TC	P4C1681L-25CM	IDT71681LA25DM	P4C1981-35CC	IDT71981S35C
P4C1681-25LM	IDT71681SA25LM	P4C1682L-45LC	IDT71682LA45L	P4C188-25CC	IDT7188S25C
P4C1682-45PC	IDT71682SA45P	P4C168-25LM	IDT6168SA25LM	P4C198-30CM	IDT6198S30CM
P4C164L-30LC	IDT7164L30L28	P4C1681L-25CMB	IDT71681LA25DB	P4C1981-35CM	IDT71981S35CM
P4C1681-25LMB	IDT71681SA25LB	P4C1682L-45LM	IDT71682LA45LM	P4C188-25LC	IDT7188S25L
P4C1682L-20CC	IDT71682LA20D	P4C168-25LMB	IDT6168SA25LB	P4C198-30CMB	IDT6198S30CB
P4C164L-30PC	IDT7164L30TP	P4C1681L-25LC	IDT71681LA25L	P4C1981-35CMB	IDT71981S35CB
P4C1681-25PC	IDT71681SA25P	P4C1682L-45LMB	IDT71682LA45LB	P4C188-25PC	IDT7188S25P
P4C1682L-20LC	IDT71682LA20L	P4C168-25PC	IDT6168SA25P	P4C198-30LC	IDT6198S30L
P4C164L-35CC	IDT7164L35TC	P4C1682L-45PC	IDT71682LA45P	P4C1981-35LC	IDT71981S35L
P4C1681-35CC	IDT71681SA35D	P4C187-25CC	IDT7187S25C	P4C188-30CC	IDT7188S30C
P4C1682L-20PC	IDT71682LA20P	P4C188L-35CC	IDT7188L35C	P4C198-30LM	IDT6198S30LM
P4C164L-35CM	IDT7164L35TCM	P4C198L-35LMB	IDT6198L35L	P4C1981-35LM	IDT71981S35LM
P4C1681-35CM	IDT71681SA35DM	P4C187-25PC	IDT7187S25P	P4C188-30CM	IDT7188S30CM
P4C1682L-25CC	IDT71682LA25D	P4C188L-35CM	IDT7188L35CM	P4C198-30LMB	IDT6198S30LB
P4C164L-35CMB	IDT7164L35TCB	P4C198L-35PC	IDT6198L35P	P4C1981-35LMB	IDT71981S35LB
P4C1681-35CMB	IDT71681SA35DB	P4C187-2LC	IDT7187S25L22	P4C188-30CMB	IDT7188S30CB
P4C1682L-25CM	IDT71682LA25DM	P4C188L-35CMB	IDT7188L35CB	P4C198-30PC	IDT6198S30PC
P4C164L-35LC	IDT7164L30L28	P4C198L-45CC	IDT6198L45C	P4C1981-45C	IDT71981S45C
P4C1681-35LC	IDT71681SA35L	P4C187-30CM	IDT7187S30CM	P4C188-30LC	IDT7188S30L
P4C1682L-25CMB	IDT71682LA25DB	P4C188L-35LC	IDT7188L35L	P4C198-35CC	IDT6198S35C
P4C164L-35LM	IDT7164L35L28M	P4C198L-45CM	IDT6198L45CM	P4C1981-45CM	IDT71981S45CM
P4C1681-35LM	IDT71681SA35LM	P4C187-30CMB	IDT7187S30CB	P4C188-30LM	IDT7188S30LM
P4C1682L-25LC	IDT71682LA25L	P4C188L-35LM	IDT7188L35LM	P4C198-35CM	IDT6198S35CM
P4C164L-35LMB	IDT7164L35L28B	P4C198L-45CMB	IDT6198L45CB	P4C1981-45CMB	IDT71981S45CB
P4C1681-35LMB	IDT71681SA35LB	P4C187-30LM	IDT7187S30L22M	P4C188-30LMB	IDT7188S30LB
P4C1682L-25LM	IDT71682LA25LM	P4C188L-35LMB	IDT7188L35LB	P4C198-35CMB	IDT6198S35CB
P4C164L-35PC	IDT7164L35TP	P4C198L-45LC	IDT6198L45L	P4C1981-45LC	IDT71981S45L
P4C1681-35PC	IDT71681SA35P	P4C187-30LMB	IDT7187S35L22B	P4C188-30PC	IDT7188S30P
P4C1682L-25LMB	IDT71682LA25LB	P4C188L-35PC	IDT7188L35P	P4C198-35LC	IDT6198S35L
P4C164L-45CM	IDT7164L45TCM	P4C198L-45LM	IDT6198L45LM	P4C1981-45LM	IDT71981S45LM
P4C1681-45CC	IDT71681SA45D	P4C187-35CM	IDT7187S35CM	P4C188-35CC	IDT7188S35C
P4C1682L-25PC	IDT71682LA25P	P4C188L-45CC	IDT7188L45C	P4C198-35LM	IDT6198S35LM
P4C164L-45CMB	IDT7164L45TCB	P4C198L-45LMB	IDT6198L45LB	P4C1981-45LMB	IDT71981S45LB
P4C1681-45CM	IDT71681SA45DM	P4C187-35CMB	IDT7187S35CB	P4C188-35CM	IDT7188S35CM
P4C1682L-35CC	IDT71682LA35D	P4C188L-45CM	IDT7188L45CM	P4C198-35LMB	IDT6198S35LB
		P4C198L-45PC	IDT6198L45P	P4C1981-55CM	IDT71981S55CM
		P4C187-35LM	IDT7187S30L22M	P4C188-35CMB	IDT7188S35CB
		P4C188L-45CMB	IDT7188L45CB	P4C198-35PC	IDT6198S35P
		P4C198L-55CM	IDT6198L55CM	P4C1981-55CMB	IDT71981S55CB
		P4C187-35LMB	IDT7187S35L22B	P4C188-35LC	IDT7188S35L
		P4C188L-45LC	IDT7188L45L	P4C198-45CC	IDT6198S45C
		P4C198L-55CMB	IDT6198L55CB	P4C1981-55LM	IDT71981S55LM
		P4C187L-25CC	IDT7187L25C	P4C188-35LM	IDT7188S35LM
		P4C188L-45LM	IDT7188L45LM	P4C198-45CM	IDT6198S45CM
		P4C198L-55LM	IDT6198L55LM	P4C1981-55LMB	IDT71981S55LB
		P4C187L-25PC	IDT7187L25P	P4C188-35LMB	IDT7188S35LB
		P4C188L-45LMB	IDT7188L45LB	P4C198-45CMB	IDT6198S45CB

NOTES:
A lower case "x" indicates the speed and/or package of the part are unknown."
*The CY7C161/162 come in a 300 mil package vs. 400 mil IDT71981/982.

PERFORMANCE CONT.	IDT
P4C1981L-25CC	IDT71981L25C
P4C188-35PC	IDT7188S35P
P4C198-45LC	IDT6198S45L
P4C1981L-25LC	IDT71981L25L
4C188-45CC	IDT7188S45C
P4C198-45LM	IDT6198S45LM
P4C1981L-30CC	IDT71981L30C
P4C188-45CM	IDT7188S45CM
P4C198-45LMB	IDT6198S45LB
P4C1981L-30CM	IDT71981L30CM
P4C188-45CMB	IDT7188S45CB
P4C198-45PC	IDT6198S45P
P4C1981L-30CMB	IDT71981L30CB
P4C188-45LC	IDT7188S45L
P4C198-55CM	IDT6198S55CM
P4C1981L-30LC	IDT71981L30L
P4C188-45LM	IDT7188S45LM
P4C198-55CMB	IDT6198S55CB
P4C1981L-30LM	IDT71981L30LM
P4C188-45LMB	IDT7188S45LB
P4C198-55LM	IDT6198S55LM
P4C1981L-30LMB	IDT71981L30LB
P4C188-45PC	IDT7188S45P
P4C198-55LMB	IDT6198S55LB
P4C1981L-35CC	IDT71981L35C
P4C188-55CM	IDT7188S55CM
P4C198L-25CC	IDT6198L25C
P4C1981L-35CM	IDT71981L35CM
P4C188-55CMB	IDT7188S55CB
P4C198L-25LC	IDT6198L25L
P4C1981L-35CMB	IDT71981L35CB
P4C188-55LM	IDT7188S55LM
P4C198L-25PC	IDT6198L25P
P4C1981L-35LC	IDT71981L35L
P4C188-55LMB	IDT7188S55LB
P4C198L-30CC	IDT6198L30C
P4C1981L-35LM	IDT71981L35LM
P4C188L-25CC	IDT7188L25C
P4C198L-30CM	IDT6198L30CM
P4C1981L-35LMB	IDT71981L35LB
P4C188L-25LC	IDT7188L25L
P4C198L-30CMB	IDT6198L30CB
P4C1981L-45CC	IDT71981L45C
P4C188L-25PC	IDT7188L25P
P4C198L-30LC	IDT6198L30L
P4C1981L-45CM	IDT71981L45CM
P4C188L-30CC	IDT7188L30C
P4C198L-30LM	IDT6198L30LM
P4C1981L-45CMB	IDT71981L45CB
P4C188L-30CM	IDT7188L30CM
P4C198L-30LMB	IDT6198L30LB
P4C1981L-45LC	IDT71981L45L
P4C188L-30CMB	IDT7188L30CB
P4C198L-30PC	IDT6198L30P
P4C1981L-45LM	IDT71981L45LM
P4C188L-30LC	IDT7188L30L
P4C198L-35CC	IDT6198L35C
P4C1981L-45LMB	IDT71981L45LB
P4C188L-30LM	IDT7188L30LM
P4C198L-35CM	IDT6198L35CM
P4C1981L-55CM	IDT71981L55CM
P4C188L-30LMB	IDT7188L30LB
P4C198L-35CMB	IDT6198L35CB
P4C1981L-55CMB	IDT71981L55CB
P4C188L-30PC	IDT7188L30P
P4C198L-35LC	IDT6198L35L
P4C1981L-55LM	IDT71981L55LM

NOTES:
A lower case "x" indicates the speed and/or package of the part are unknown."
*The CY7C161/162 come in a 300 mil package vs. 400 mil IDT71981/982.

PERFORMANCE CONT.	IDT
P4C198L-35LM	IDT6198L35LM
P4C1981L-55LMB	IDT71981L55LB
P4C1982-25CC	IDT71982S25C
P4C1982L-35LC	IDT71982L35L
P4C198A-45LM	IDT7198S45LM
P4C1982-25LC	IDT71982S25L
P4C1982L-35LM	IDT71982L35LM
P4C198A-45LMB	IDT7198S45LB
P4C1982-30CC	IDT71982S30C
P4C1982L-35LMB	IDT71982L35LB
P4C198A-45PC	IDT7198S45P
P4C1982-30CM	IDT71982S30CM
P4C1982L-45CC	IDT71982L45C
P4C198A-55CM	IDT7198S55CM
P4C1982-30CMB	IDT71982S30CB
P4C1982L-45CM	IDT71982L45CM
P4C198A-55CMB	IDT7198S55CB
P4C1982-30LC	IDT71982S30L
P4C1982L-45CMB	IDT71982L45CB
P4C198A-55LM	IDT7198S55LM
P4C1982-30LM	IDT71982S30LM
P4C1982L-45LC	IDT71982L45L
P4C198A-55LMB	IDT7198S55LB
P4C1982-30LMB	IDT71982S30LB
P4C1982L-45LM	IDT71982L45LM
P4C198AL-25CC	IDT7198L25C
P4C1982-35CC	IDT71982S35C
P4C1982L-45LMB	IDT71982L45LB
P4C198AL-25LC	IDT7198L25L
P4C1982-35CM	IDT71982S35CM
P4C1982L-55CM	IDT71982L55CM
P4C198AL-25PC	IDT7198L25P
P4C1982-35CMB	IDT71982S35CB
P4C1982L-55CMB	IDT71982L55CB
P4C198AL-30CC	IDT7198L30C
P4C1982-35LC	IDT71982S35L
P4C1982L-55LM	IDT71982L55LM
P4C198AL-30CM	IDT7198L30CM
P4C1982-35LM	IDT71982S35LM
P4C1982L-55LMB	IDT71982L55LB
P4C198AL-30CMB	IDT7198L30CB
P4C1982-35LMB	IDT71982S35LB
P4C198AL-30LC	IDT7198L30L
P4C1982-45CC	IDT71982S45C
P4C198A-25CC	IDT7198S25C
P4C198AL-30LM	IDT7198L30LM
P4C1982-45CM	IDT71982S45CM
P4C198A-25LC	IDT7198S25L
P4C198AL-30LMB	IDT7198L30LB
P4C1982-45CMB	IDT71982S45CB
P4C198A-25PC	IDT7198S25P
P4C198AL-30PC	IDT7198L30P
P4C1982-45LC	IDT71982S45L
P4C198A-30CC	IDT7198S30C
P4C198AL-35CC	IDT7198L35C
P4C1982-45LM	IDT71982S45LM
P4C198A-30CM	IDT7198S30CM
P4C198AL-35CM	IDT7198L35CM
P4C1982-45LMB	IDT71982S45LB
P4C198A-30CMB	IDT7198S30CB
P4C198AL-35CMB	IDT7198L35CB
P4C1982-55CM	IDT71982S55CM
P4C198A-30LC	IDT7198S30L
P4C198AL-35LC	IDT7198L35L
P4C1982-55CMB	IDT71982S55CB
P4C198A-30LM	IDT7198S30LM
P4C198AL-35LM	IDT7198L35LM
P4C1982-55LM	IDT71982S55LM
P4C198A-30LMB	IDT7198S30LB
P4C198AL-35LMB	IDT7198L35LB
P4C1982-55LMB	IDT71982S55LB
P4C198A-30PC	IDT7198S30P
P4C198AL-35PC	IDT7198L35P
P4C1982L-25CC	IDT71982L25C
P4C198A-35CC	IDT7198S35C

PERFORMANCE CONT.	IDT
P4C198AL-45CC	IDT7198L45C
P4C1982L-25LC	IDT71982L25L
P4C198A-35CM	IDT7198S35CM
P4C198AL-45CM	IDT7198L45CM
P4C1982L-30CC	IDT71982L30C
P4C198A-35CMB	IDT7198S35CB
P4C198AL-45CMB	IDT7198L45CB
P4C1982L-30CM	IDT71982L30CM
P4C198A-35LC	IDT7198S35L
P4C198AL-45LC	IDT7198L45L
P4C1982L-30CMB	IDT71982L30CB
P4C198A-35LM	IDT7198S35LM
P4C198AL-45LM	IDT7198L45LM
P4C1982L-30LC	IDT71982L30L
P4C198A-35LMB	IDT7198S35LB
P4C198AL-45LMB	IDT7198L45LB
P4C1982L-30LM	IDT71982L30LM
P4C198A-35PC	IDT7198S35P
P4C198AL-45PC	IDT7198L45P
P4C1982L-30LMB	IDT71982L30LB
P4C198A-45CC	IDT7198S45C
P4C198AL-55CM	IDT7198L55CM
P4C1982L-35CC	IDT71982L35C
P4C198A-45CM	IDT7198S45CM
P4C198AL-55CMB	IDT7198L55CB
P4C1982L-35CM	IDT71982L35CM
P4C198A-45CMB	IDT7198S45CB
P4C198AL-55LM	IDT7198L55LM
P4C1982L-35CMB	IDT71982L35CB
P4C198A-45LC	IDT7198S45L
P4C198AL-55LMB	IDT7198L55LB

FUJITSU	IDT
MB81C67-35	IDT6167SA35P
MB81C69A-25C	IDT6169SA25L
MB81C78-45	IDT7164S45P
MB81C67-45	IDT6167SA45P
MB81C69A-25P	IDT6169SA25P
MB81C78-55	IDT7164S55P
MB81C67-45-W	IDT6167SA45xM
MB81C69A-25Z	IDT6169SA25D
MB81C78-70	IDT7164S70P
MB81C67-55	IDT6167SA55P
MB81C69A-30C	IDT6169SA25L
MB81C67-55-W	IDT6167SA55xM
MB81C69A-30P	IDT6169SA25P
MB81C78A-35CV	IDT7164S35L22
MB81C69A-30Z	IDT6169SA25D
MB81C78A-35P	IDT7164S35P
MB81C68-35C	IDT6168SA35L
MB81C69A-35C	IDT6169SA35L
MB81C78A-35PF	IDT7164S35SO
MB81C68-35P	IDT6168SA35P
MB81C69A-35P	IDT6169SA35P
MB81C68-35Z	IDT6168SA35D
MB81C69A-35Z	IDT6169SA35D
MB8416A-12x	IDT6116LA90P
MB81C68-45-W	IDT6168SA45xM
MB8416A-12x	IDT6116LA90D
MB81C68-45C	IDT6168SA45L
MB81C71-35	IDT7187S35P
MB8416A-12x	IDT6116LA90TP
MB81C68-45P	IDT6168SA45P
MB81C71-45C	IDT7187S45L22
MB81C68-45Z	IDT6168SA45D
MB81C71-45Z	IDT7187S45D
MB84256-10	IDT71256L70L
MB81C68-55-W	IDT6168SA55xM
MB81C71-55C	IDT7187S55L22
MB84256-10	IDT71256L70P
MB81C71-55Z	IDT7187S55D
MB84256-10	IDT71256L70SO
MB81C68A-25C	IDT6168SA25L

FUJITSU CONT.	IDT
MB81C68A-25P	IDT6168SA25P
MB81C74-25x	IDT7188S25x
MB8464-15-W	IDT7164S150DM
MB81C68A-25Z	IDT6168SA25D
MB81C74-35x	IDT7188S35x
MB8464-15-W	IDT7164S150L32M
MB81C68A-30C	IDT6168SA25L
MB8464-20-W	IDT7164S200DM
MB81C68A-30P	IDT6168SA25P
MB81C75-35	IDT7198S35P
MB8464-20-W	IDT7164S200L32M
MB81C68A-30Z	IDT6168SA25D
MB81C75-45	IDT7198S45P
MB81C68A-35C	IDT6168SA35L
MB81C75-55	IDT7198S55P
MB8464A-10-W	IDT7164L100DM
MB81C68A-35P	IDT6168SA35P
MB8464A-10-W	IDT7164L100L32M
MB81C68A-35Z	IDT6168SA35D
MB81C81-45	IDT71257S45P
MB8464A-15-W	IDT7164L150DM
MB81C81-55	IDT71257S55P
MB8464A-15-W	IDT7164L150L32M
MB8464A-70x	IDT7164L70L32
MB81C84-45	IDT71258S45P
MB8464A-70x	IDT7164L70P
MB81C84-55	IDT71258S55P
MB8464A-70x	IDT7164L70SO

FAIRCHILD	IDT
F1600DC45	IDT7187S45C
F1600DMQB70	IDT7187S70CB
F1601DC70	IDT7187L70C
F1600LC45	IDT7187S45L
F1600LC70	IDT7187S70L
F1601DMQB55	IDT7187L55CB
F1600DC55	IDT7187S55C
F1600LMQB70	IDT7187S70LB
F1601DMQB70	IDT7187L70CB
F1600DMQB55	IDT7187S55CB
F1601LC55	IDT7187L55L
F1600LC55	IDT7187S55L
F1601DC45	IDT7187L45C
F1601LC70	IDT7187L70L
F1600LMQB55	IDT7187S55LB
F1601LC45	IDT7187L45L
F1601LMQB55	IDT7187L55LB
F1600DC70	IDT7187S70C
F1601DC55	IDT7187L55C
F1601LMQB70	IDT7187L70LB

HARRIS	IDT
HM1-6516B-8	IDT6116SA120DB
HM1-65162S-5	IDT6116LA55D
HM4-65262-8	IDT6167SA70LB
HM4-65162-8	IDT6116LA90DB
HM4-65262B-8	IDT6167SA70LB
HM1-65162-8	IDT6116LA90DB
HM4-65162C-8	IDT6116SA90LB
HM1-65162B-8	IDT6116LA70DB
HM4-65162S-5	IDT6116LA55L

NOTES:
A lower case "x" indicates the speed and/or package of the part are unknown."
*The CY7C161/162 come in a 300 mil package vs. 400 mil IDT71981/982.

HARRIS CONT.	IDT
HM1-65642-8	IDT7164L150DB
HM1-65162C-8	IDT6116SA90DB
HM4-65642-8	IDT7164L150L32B
HM1-65262-8	IDT6167SA70DB
HM1-65262B-8	IDT6167SA70DB

HITACHI	IDT
HM6116-2	IDT6116SA90D
HM62256LFP-10SL	IDT71256L70P
HM6287CG-45	IDT7187S45L
HM6116FP-2	IDT6116SA90F
HM62256LFP-8	IDT71256L70SO
HM6287CG-55	IDT7187S55L
HM6116LFP-2	IDT6116LA90SO
HM62256LP-10SL	IDT71256L70P
HM6287CG-70	IDT7187S70L
HM6116LP-2	IDT6116LA90P
HM62256LP-8	IDT71256L70P
HM6287LP-45	IDT7187L45P
HM6116P-2	IDT6116SA90P
HM62256P-8	IDT71256S70P
HM6287LP-55	IDT7187L55P
HM6287LP-70	IDT7187L70P
HM6116ALP-12	IDT6116LA90P
HM6264FP-10	IDT7164S70SO
HM6287P-45	IDT7187S45P
HM6116ALSP-12	IDT6116LA90TP
HM6264LFP-10	IDT7164L70SO
HM6287P-55	IDT7187S55P
HM6116AP-12	IDT6116LA90P
HM6264LFP-10L	IDT7164L70SO
HM6287P-70	IDT7187S70P
HM6116ASP-12	IDT6116LA90TP
HM6264LP-10	IDT7164L70P
HM6264LP-10L	IDT7164L70P
HM6288P-35	IDT7188S35P
HM6167H-45	IDT6167SA45D
HM6264LP-10SL	IDT7164L70P
HM6288P-45	IDT7188S45P
HM6167H-55	IDT6167SA55D
HM6264P-10	IDT7164S70P
HM6288P-55	IDT7188S55P
HM6167HCG-45	IDT6167SA45L
HM6167HCG-55	IDT6167SA55L
HM6264AFP-12	IDT7164S70SO
HM65256AP-12	IDT71256S70P
HM6167HLP-45	IDT6167LA45P
HM6264ALFP-12	IDT7164L70SO
HM6167HLP-55	IDT6167LA55P
HM6264ALSP-12	IDT7164L70TC
HM6716	IDT6116SA25TD
HM6167HP-45	IDT6167SA45P
HM6264ASP-12	IDT7164S70TC
HM6716-30	IDT6116SA30TD
HM6167HP-55	IDT6167SA55P
HM6267CG-35	IDT6167SA35L
HM6787	IDT7187S25C
HM6168H-45	IDT6168SA45D
HM6267CG-45	IDT6167SA45L
HM6787-30	IDT7187S230C
HM6168H-55	IDT6168SA55D
HM6267LP-35	IDT6167LA35P
HM6787CG	IDT7187S25L22
HM6168HLP-45	IDT6168LA45P
HM6267LP-45	IDT6167LA45P
HM6787CG-30	IDT7187S30L22
HM6168HLP-55	IDT6168LA55P
HM6267P-35	IDT6167SA35P
HM6168HP-45	IDT6168SA45P
HM6267P-45	IDT6167SA45P
HM6788	IDT7188S25C
HM6168HP-55	IDT6168SA55P
HM6268LP-25	IDT6168LA25P

HITACHI CONT.	IDT
HM6789	IDT6198S25C
HM6268LP-35	IDT6168LA35P
HM6789-30	IDT6198S30C
HM6268P-25	IDT6168SA25P
HM6268P-35	IDT6168SA35P

INMOS	IDT
IMS1400P-35	IDT6167SA35P
IMS1420W-45	IDT6168SA45L
IMS1600W-70	IDT7187S70L
IMS1400P-45	IDT6167SA45P
IMS1420W-55	IDT6168SA55L
IMS1600W-70M	IDT7187S70LB
IMS1400P-55	IDT6167SA55P
IMS1420W-55M	IDT6168SA55LB
IMS1400P-70L	IDT6167LA55P
IMS1420W-70M	IDT6168SA70LB
IMS1601S-55	IDT7187L55C
IMS1400S-45	IDT6167SA45D
IMS1601S-70	IDT7187L70C
IMS1400S-45M	IDT6167SA45DB
IMS1421S-40	IDT71681SA35C
IMS1601W-55	IDT7187L55L
IMS1400S-55	IDT6167SA55D
IMS1421S-50	IDT71681SA45C
IMS1601W-70	IDT7187L70L
IMS1400S-55M	IDT6167SA55DB
IMS1421W-40	IDT71681SA35L
IMS1400S-70M	IDT6167SA70DB
IMS1421W-50	IDT71681SA45L
IMS1620S-45	IDT7188S45C
IMS1400W-35	IDT6167SA35L
IMS1620S-55	IDT7188S55C
IMS1400W-45	IDT6167SA45L
IMS1423P-25	IDT6168SA25P
IMS1620S-55M	IDT7188S55CB
IMS1400W-45M	IDT6167SA45LB
IMS1423P-35	IDT6168SA35P
IMS1620S-70	IDT7188S70C
IMS1400W-55	IDT6167SA55L
IMS1423P-45	IDT6168SA45P
IMS1620S-70M	IDT7188S70CB
IMS1400W-55M	IDT6167SA55LB
IMS1423S-25	IDT6168SA25D
IMS1400W-70M	IDT6167SA70LB
IMS1423S-35	IDT6168SA35D
IMS1624S-45	IDT7198S45C
IMS1423S-35M	IDT6168SA35DB
IMS1624S-55	IDT7198S55C
IMS1403P-25	IDT6167SA25P
IMS1423S-45	IDT6168SA45D
IMS1624S-55M	IDT7198S55CB
IMS1403P-35	IDT6167SA35P
IMS1423S-45M	IDT6168SA45DB
IMS1624S-70	IDT7198S70C
IMS1403P-45	IDT6167SA45P
IMS1423S-55M	IDT6168SA55LB
IMS1624S-70M	IDT7198S70CB
IMS1403P-55	IDT6167SA55P
IMS1423W-25	IDT6168SA25L
IMS1624W-45	IDT7198S45L
IMS1403S-25	IDT6167SA25D
IMS1423W-35	IDT6168SA35L
IMS1624W-55	IDT7198S55L
IMS1403S-35	IDT6167SA35D
IMS1423W-35M	IDT6168SA35LB
IMS1624W-55M	IDT7198S55LB
IMS1403S-45	IDT6167SA45D
IMS1423W-45	IDT6168SA45L
IMS1624W-70	IDT7198S70L
IMS1403S-55	IDT6167SA55D
IMS1423W-45M	IDT6168SA45LB
IMS1624W-70M	IDT7198S70LB

INMOS CONT.	IDT
IMS1403W-25	IDT6167SA25L
IMS1423W-55M	IDT6168SA55LB
IMS1403W-35	IDT6167SA35L
IMS1630S-45	IDT7164S45D
IMS1403W-45	IDT6167SA45L
IMS1433x-35	IDT6116SA35
IMS1630S-55	IDT7164S55D
IMS1403W-55	IDT6167SA55L
IMS1630S-70	IDT7164S70D
IMS1600S-45	IDT7187S45C
IMS1420P-45	IDT6168SA45P
IMS1600S-55	IDT7187S55C
IMS1800x-35	IDT71257S35x
IMS1420P-55	IDT6168SA55P
IMS1600S-55M	IDT7187S55CB
IMS1420P-70L	IDT6168LA55P
IMS1600S-70	IDT7187S70C
IMS1820P-35	IDT71258S35P
IMS1420S-45	IDT6168SA45D
IMS1600S-70M	IDT7187S70CB
IMS1820P-45	IDT71258S45P
IMS1420S-55	IDT6168SA55D
IMS1600W-45	IDT7187S45L
IMS1820P-55	IDT71258S55P
IMS1420S-55M	IDT6168SA55DB
IMS1600W-55	IDT7187S55L
IMS1420S-70M	IDT6168SA70DB
IMS1600W-55M	IDT7187S55LB
IMS1830x-45	IDT71256S45x

MITSUBISHI	IDT
M5M21C67P-35	IDT6167LA35P
M5M5178P-45	IDT7164L45P
M5M5188AP-25	IDT7188L25P
M5M21C67P-45	IDT6167LA45P
M5M5178P-55	IDT7164L55P
M5M5188AP-35	IDT7188L35P
M5M21C67P-55	IDT6167LA55P
M5M5188P-45	IDT7188L45P
M5M5187AD-25	IDT7187L25L22
M5M5188P-55	IDT7188L55P
M5M21C68P-35	IDT6168LA35P
M5M5187AD-35	IDT7187L35L22
M5M21C68P-45	IDT6168LA45P
M5M5187AP-25	IDT7187L25P
M5M5257P-35	IDT71257S35P
M5M21C68P-55	IDT6168LA55P
M5M5187AP-35	IDT7187L35P
M5M5257P-45	IDT71257S45P
M5M5187P-45	IDT7187L45P
M5M5257P-55	IDT71257S55P
M5M5165FP-70	IDT7164S70SO
M5M5187P-55	IDT7187L55P
M5M5165FP-70L	IDT7164L70SO
M5M5258P-35	IDT71258S35P
M5M5188AD-25	IDT7188L25L22
M5M5258P-45	IDT71258S45P
M5M5188AD-35	IDT7188L35L22
M5M5258P-55	IDT71258S55P

MOTOROLA	IDT
MCM2016P45	IDT6116SA45P
MCM6168P35	IDT6168SA35P
MCM6287P35	IDT7187S35P
MCM2016P55	IDT6116SA55P
MCM6168P45	IDT6168SA45P
MCM6287P45	IDT7187S45P

NOTES:
A lower case "x" indicates the speed and/or package of the part are unknown."
*The CY7C161/162 come in a 300 mil package vs. 400 mil IDT71981/982.

MOTOROLA	IDT
MCM2016P70	IDT6116SA70P
MCM6168P55	IDT6168SA55P
MCM6287P25	IDT7187S25P
MCM6168P70	IDT6168SA70P
MCM2167P45	IDT6167SA45P
MCM6288P25	IDT7188S25P
MCM2167P55	IDT6167SA55P
MCM6268P25	IDT6168SA25P
MCM6288P35	IDT7188S35P
MCM2167P70	IDT6167SA70P
MCM6268P35	IDT6168SA35P
MCM6288P45	IDT7188S45P
MCM6268P45	IDT6168SA45P
MCM6164P45	IDT7164S45P
MCM6268P55	IDT6168SA55P
MCM6164P55	IDT7164S55P
MCM6164P70	IDT7164S70P

NEC	IDT
5PD4311C-35	IDT6167SA35P
5PD43256G-10	IDT71256S70SO
5PD4362C-45	IDT7188SA45P
5PD4311C-45	IDT6167SA45P
5PD43256G-10L	IDT71256L70SO
5PD4362C-55	IDT7188SA55P
5PD4311C-55	IDT6167SA55P
5PD4362C-70	IDT7188SA70P
5PD4311D-35	IDT6167SA35D
5PD4361C-45	IDT7187S45P
5PD4311D-45	IDT6167SA45D
5PD4361C-45L	IDT7187L45P
5PD4364C-12	IDT7164S70P
5PD4311D-55	IDT6167SA55D
5PD4361C-55	IDT7187S55P
5PD4364C-12L	IDT7164L70P
5PD4361C-55L	IDT7187L55P
5PD4364G-12	IDT7164S70SO
5PD4314C-35	IDT6168SA35P
5PD4361C-70	IDT7187S70P
5PD4364G-12L	IDT7164L70SO
5PD4314C-45	IDT6168SA45P
5PD4361C-70L	IDT7187L70P
5PD4314C-55	IDT6168SA55P
5PD4361K-40	IDT7187S35L22
5PD446C	IDT6116LA70P
5PD4361K-45	IDT7187S45L22
5PD43256C-10	IDT71256S70P
5PD4361K-55	IDT7187S55L22
5PD4464C-x	IDT7164L70P
5PD43256C-10L	IDT71256L70P
5PD4464G-x	IDT7164L70SO

SARATOGA	IDT
SSM6116-25	IDT6116SA25TD
SSM6171-20	IDT71681S20D
SSM7162-25	IDT71982S25C
SSM6116L-25	IDT6116LA25TD
SSM6171-25	IDT71681S25D
SSM7162L-25	IDT71982L25C
SSM6171L-20	IDT71681L20D
SSM6167-20	IDT6167SA20D
SSM6171L-25	IDT71681L25D
SSM7164-25	IDT7164S25TC
SSM6167-25	IDT6167SA25D
SSM7164L-25	IDT7164L25TC
SSM6167L-20	IDT6167LA20D
SSM6172-20	IDT71682S20D
SSM6167L-25	IDT6167LA25D
SSM6172-25	IDT71682S25D
SSM7187-25	IDT7187S25C
SSM6172L-20	IDT71682L20D
SSM7187L-25	IDT7187L25C
SSM6168-20	IDT6168SA20D

SARATOGA CONT.	IDT
SSM6172L-25	IDT71682L25D
SSM6168-25	IDT6168SA25D
SSM7188-25	IDT7188S25C
SSM6168L-20	IDT6168LA20D
SSM7161-25	IDT71981S25C
SSM7188L-25	IDT7188L25C
SSM6168L-25	IDT6168LA25D
SSM7161L-25	IDT71981L25C
SSM7198-25	IDT7198S25C
SSM7198L-25	IDT7198L25C

SONY	IDT
CXK5416P-35	IDT6168LA35P
CXK5814P-35	IDT6116LA35TP
CXK58256P-10	IDT71256L70P
CXK5416P-45	IDT6168LA45P
CXK5814P-45	IDT6116LA45TP
CXK58256M-10	IDT71256L70SO
CXK5416P-55	IDT6168LA55P
CXK5814P-55	IDT6116LA55TP
CXK5864AP-70L	IDT7164L70P
CXK5464P-45	IDT7188L45P
CXK5818PN-10	IDT6116L90P
CXK5864AM-70L	IDT7164L70SO
CXK5464P-55	IDT7188L55P
CXK5818M-10	IDT6116L90SO
CXK5464P-70	IDT7188L70P
CXK5865P-45L	IDT7164L45P
CXK5865P-55L	IDT7164L55P

VITELIC	IDT
V61C16P35	IDT6116SA35P
V61C34P90	IDT71322S90P
V61C67P35	IDT6167SA35P
V61C16P35L	IDT6116LA35P
V61C67P35L	IDT6167LA35P
V61C16P45	IDT6116SA45P
V61C62P45	IDT7188S45P
V61C67P45	IDT6167SA45P
V61C16P45L	IDT6116LA45P
V61C62P45L	IDT7188L45P
V61C67P45L	IDT6167LA45P
V61C16P55	IDT6116SA55P
V61C62P55	IDT7188S55P
V61C67P55	IDT6167SA55P
V61C16P55L	IDT6116LA55P
V61C62P55L	IDT7188L55P
V61C67P55L	IDT6167LA55P
V61C16S35	IDT6116SA35TP
V61C62P70	IDT7188S70P
V61C16S35L	IDT6116LA35TP
V61C62P70L	IDT7188L70P
V61C68P35	IDT6168SA35P
V61C16S45	IDT6116SA45TP
V61C68P35L	IDT6168LA35P
V61C16S45L	IDT6116LA45TP
V61C64P45	IDT7164S45P
V61C68P45	IDT6168SA45P
V61C16S55	IDT6116SA55TP
V61C64P45L	IDT7164L45P
V61C68P45L	IDT6168LA45P
V61C16S55L	IDT6116LA55TP
V61C64P55	IDT7164S55P
V61C68P55	IDT6168SA55P
V61C64P55L	IDT7164L55P
V61C68P55L	IDT6168LA55P
V61C32P70	IDT7132SA70P
V61C64P70	IDT7164S70P
V61C32P70L	IDT7132LA70P
V61C64P70L	IDT7164L70P
V61C32P90	IDT7132SA90P
V61C32P90L	IDT7132LA90P

VTI	IDT
VT16H4-35	IDT71981-35
VT20C69-20	IDT6169SA20P
VT7132-55	IDT7132SA55D
VT16H4-45	IDT71981-45
VT20C69-25	IDT6169SA25P
VT7132-70	IDT7132SA70D
VT16H4-55	IDT71981-55
VT20C69-35	IDT6169SA35P
VT7132-90	IDT7132SA90D
VT20C69-45	IDT6169SA45P
VT7132A-35	IDT7132SA35D
VT20C18-20	ITD6116SA20TP
VT7132A-45	IDT7132SA45D
VT20C18-25	ITD6116SA25TP
VT2130	IDT7130SA100P
VT20C18-35	ITD6116SA35TP
VT7142-55	IDT7142SA55D
VT65KS4-25	IDT7188S25P
VT7142-70	IDT7142SA70D
VT20C19-20	IDT6120SA20TP
VT65KS4-35CC	IDT7188S35C
VT7142-90	IDT7142SA90D
VT20C19-25	IDT6120SA25TP
VT65KS4-45CC	IDT7188S45C
VT7142A-35	IDT7142SA35D
VT20C19-35	IDT6120SA35TP
VT65KS4-55CC	IDT7188S55C
VT7142A-45	IDT7142SA45D
VT20C68-20	IDT6168SA20P
VT20C68-25	IDT6168SA25P
VT20C68-35	IDT6168SA35P
VT20C68-45	IDT6168SA45P

NOTES:
A lower case "x" indicates the speed and/or package of the part are unknown."
*The CY7C161/162 come in a 300 mil package vs. 400 mil IDT71981/982.

Integrated Device Technology, Inc.

EEPROMs CROSS REFERENCE GUIDE

1

AMTEL	IDT
AT28C16A-15	IDT78C16A-150
AT28C16A-20	IDT78C16A-200
AT28C16A-25	IDT78C16A-250
AT28C16A-30	IDT78C16A-300
AT28C16A-35	IDT78C16A-350
EXEL	**IDT**
XLS2816AL-250	IDT78C16A-250
XLS2816AL-300	IDT78C16A-300
XLS2816AL-350	IDT78C16A-350
SEEQ	**IDT**
2816A-200	IDT78C16A-200
2816A-250	IDT78C16A-250
2816A-300	IDT78C16A-300
2816A-350	IDT78C16A-350
XICOR	**IDT**
X2816A-20	IDT78C16A-200
X2816A-25	IDT78C16A-250
X2816A-30	IDT78C16A-300
X2816A-35	IDT78C16A-350

Integrated Device Technology, Inc.

MICROSLICE CROSS REFERENCE GUIDE

FUNCTIONAL REPLACEMENTS

CYPRESS	IDT
7C901-23DC	IDT39C01DD
7C901-23PC	IDT39C01DP
7C901-27DMB	IDT39C01DDB
7C901-27LMB	IDT39C01DLB
7C901-31DC	IDT39C01CD
7C901-31JC	—
7C901-31PC	IDT39C01CP
7C901-32DMB	IDT39C01CDB
7C901-32LMB	IDT39C01CLB
7C909-30DC	IDT39C09BD
7C909-30DMB	IDT39C09BDB
7C909-30PC	IDT39C09BP
7C909-40DC	IDT39C09AD
7C909-40DMB	IDT39C09ADB
7C909-40LMB	IDT39C09ALB
7C909-40PC	IDT39C09AP
7C910-40DC	IDT39C10CD
7C910-40JC	IDT39C10CJ
7C910-40PC	IDT39C10CP
7C910-46DMB	IDT39C10CDB
7C910-50DC	IDT39C10BD
7C910-50JC	IDT39C10BJ
7C910-50PC	IDT39C10BP
7C910-51DMB	IDT39C10BDB
7C910-51LMB	IDT39C10BLB
7C9101-30DC	IDT49C401AC
"	IDT49C402AG
"	IDT49C402AXC
7C9101-30GC	—
7C9101-30JC	IDT49C402AL
7C9101-30PC	IDT49C401AC
"	IDT49C402AG
"	IDT49C402AXC
7C9101-35DMB	IDT49C401ACB
"	IDT49C402AXCB
"	IDT49C402AGB
7C9101-35GMB	—
7C9101-35LMB	IDT49C402ALB
7C9101-40DC	IDT49C401C
"	IDT49C402G
"	IDT49C402XC
7C9101-40GC	—
7C9101-40JC	—
7C9101-40PC	IDT49C401C
"	IDT49C402G
"	IDT49C402XC
7C9101-45DMB	IDT49C401CB
"	IDT49C402GB
"	IDT49C402XCB
7C9101-45GMB	—
7C9101-45LMB	IDT49C402LB
7C911-30DC	IDT39C11BD
7C911-30DMB	IDT39C11BDB
7C911-30PC	IDT39C11BP
7C911-40DC	IDT39C11AD
7C911-40DMB	IDT39C11ADB
7C911-40LMB	IDT39C11ALB
7C911-40PC	IDT39C11AP

NOTE:
BOLD FACE ITEMS ARE
FUNCTIONAL REPLACEMENTS.

AMD	IDT
Am2901C/BQA	IDT39C01CDB
Am2901C/BUC	IDT39C01CLB
Am2901C/BYC	—
Am2901CDC	IDT39C01CD
Am2901CDCB	IDT39C01CD
Am2901CLC	IDT39C01CL
Am2901CPC	IDT39C01CP
Am2901CPCB	IDT39C01CP
Am2903A/BXC	IDT39C03ACB
Am2903A/BYC	—
Am2903A/LMC	IDT39C03ALB
Am2903ADC	IDT39C03AC
Am2903ADCB	IDT39C03AC
Am2903ALC	IDT39C03AL
Am2909A/BXA	IDT39C09ADB
Am2909A/BYA	—
Am2909A/B3C	IDT39C09ALB
Am2909ADC	IDT39C09AD
Am2909ADCB	IDT39C09AD
Am2909ALC	IDT39C09AL
Am2909APC	IDT39C09AP
Am2909APCB	IDT39C09AP
Am2910A/BQA	IDT39C10BDB
Am2910A/BUC	IDT39C10BLB
Am2910A/BYC	—
Am2910ADC	IDT39C10BD
Am2910ADCB	IDT39C10BD
Am2910ALC	IDT39C10BL
Am2910APC	IDT39C10BP
Am2910APCB	IDT39C10BP
Am29C10A-10DC	IDT39C10BD
Am29C10A-10PC	IDT39C10BP
Am29C10A-10PCB	IDT39C10BP
Am29C101DC	IDT49C401C
"	IDT49C402G
"	IDT49C402XC
Am29C101PC	IDT49C401C
"	IDT49C402G
"	IDT49C402XC
Am29C101JC	—
Am2911A/BRA	IDT39C11ADB
Am2911A/BUC	IDT39C11ALB
Am2911A/B2C	IDT39C11ALB
Am2911ADC	IDT39C11AD
Am2911ADCB	IDT39C11AD
Am2911ALC	IDT39C11AL
Am2911APC	IDT39C11AP
Am2911APCB	IDT39C11AP
Am29203/BXC	IDT39C203CB
Am29203DC	IDT39C203C
Am29203DCB	IDT39C203C
Am2960/BUC	IDT39C60LB
Am2960/BXC	IDT39C60CB
Am2960DC	IDT39C60C
Am2960DCB	IDT39C60C
Am2960LC	IDT39C60L
Am2960PC	IDT39C60P
Am2960PCB	IDT39C60P
Am2960JC	IDT39C60J
Am2960JCB	IDT39C60J
Am2960-1/BXC	IDT39C60-1CB
Am2960-1/BUC	IDT39C60-1LB
Am2960-1/BYC	—
Am2960-1PC	IDT39C60-1P
Am2960-1PCB	IDT39C60-1P

AMD CONT.	IDT
Am2960-1LC	IDT39C60-1L
Am2960-1JC	IDT39C60-1J
Am2960-1JCB	IDT39C60-1J
Am2960-1DC	IDT39C60-1C
Am2960-1DCB	IDT39C60-1C
Am2960ADC	IDT39C60AC
Am2960ADCB	IDT39C60AC
Am2960APC	IDT39C60AP
Am2960APCB	IDT39C60AP
Am29705/BXA	IDT39C705ADB
Am29705/BYA	—
Am29705/B3C	IDT39C705ALB
Am29705DC	IDT39C705AD
Am29705DCB	IDT39C705AD
Am29705LC	IDT39C705AL
Am29705PC	IDT39C705AP
Am29705PCB	IDT39C705AP
Am29707DC	IDT39C707D
Am29707DCB	IDT39C707D
Am29707LC	IDT39C707L
Am29707PC	IDT39C707P
Am29707PCB	IDT39C707P

TI	IDT
SN54/74ALS632A/3/4/5JD	IDT49C460G
"	IDT49C460XC
SN54/74ALS632A/3/4/5FN	IDT49C460J
SN54/74ALS632BJD	IDT49C460AG
"	IDT49C460AXC
SN54/74ALS632BFN	IDT49C460AJ
SN54/74AS632AJD	IDT49C460AG
"	IDT49C460AXC
SN54/74AS632AFN	IDT49C460AJ

MOTOROLA	IDT
MC74F2960J	IDT39C60P
MC74F2960-1J	IDT39C60-1P
MC74F2960AJ	IDT39C60AP

NATIONAL	IDT
DP8402AD	IDT49C460XC
DP8402AV	IDT49C460J
DP8403D	IDT49C460XC
"	IDT49C460G
DP8403V	IDT49C460J
DP8404D	IDT49C460XC
"	IDT49C460G
DP8404V	IDT49C460J
DP8405D	IDT49C460XC
"	IDT49C460G

SIGNETICS	IDT
N2960	IDT39C60P

DIGITAL SIGNAL PROCESSING CROSS REFERENCE GUIDE

AMD	IDT
29C509/BXC	**7209**
29C509/BXC	7209L90CB
29C509DC	7209L70C
29510	**7210**
29510DC	7210L75C
29510DCB	7210L75C
29510XC	7210LU
29L510/BXC	7210L120CB
29L510DC	7210L100C
29L510DCB	7210L100C
29516	**7216**
29516/BYC	7216L75FB
29516/DMC	7216L75CB
29516ADC	7216L35C
29516ADCB	7216L35C
29516ALC	7216L35L
29516AXC	7216LU
29516DC	7216L65C
29516DCB	7216L65C
29516LC	7216L65L
29516XC	7216LU
29L516/BXC	7216L90CB
29L516/BYC	7216L90FB
29L516DC	7216L90C
29L516DCB	7216L90C
29L516JC	7216L90J
29L516LC	7216L90L
29L516LMB	7216L90LB
29L516PC	7216L90P
29L516PCB	7216L90P
29L516XC	7216LU
29517	**7217**
29517/BYC	7217L75FB
29517/DMC	7217L75CB
29517/LMC	7217L75LB
29517ADC	7217L35C
29517ALC	7217L35L
29517AXC	7217LU
29517DC	7217L65C
29517DCB	7217L65C
29517LC	7217L65L
29517XC	7217LU
29L517/BXC	7217L90CB
29L517DC	7217L90C
29L517DCB	7217L90C
29L517JC	7217L90J
29L517LC	7217L90L
29L517LMB	72176L90LB
29L517PC	7217L90P
29L517PCB	7217L90P
29L517XC	7217LU

ANALOG DEVICES	IDT
ADSP-1009	**7209**
ADSP-1009JD	7209L135C
ADSP-1009KD	7209L135C

NOTE:
BOLD FACE ITEMS ARE FUNCTIONAL REPLACEMENTS

ANALOG CONT.	IDT
ADSP-1009SD	7209L170CB
ADSP-1009TD	7209L170CB
ADSP-1012	**7212**
ADSP-1012	7212
ADSP-1012JD	7212L115C
ADSP-1012KD	7212LL115C
ADSP-1012SD	7212L140CB
ADSP-1012TD	7212L140CB
ADSP-1010	**7210**
ADSP-1010AKD	7210L75C
ADSP-1010AKG	7210L75G
ADSP-1010JD	7210L165C
ADSP-1010JG	7210L165G
ADSP-1010KD	7210L165C
ADSP-1010KG	7210L165G
ADSP-1010SD	7210L200CB
ADSP-1010SG	7210L200GB
ADSP-1010TD	7210L200CB
ADSP-1010TG	7210L200GB
ADSP-1016	**7216**
ADSP-1016AKD	7216L75C
ADSP-1016AKG	7216L75G
ADSP-1016JD	7216L140C
ADSP-1016JG	7216L140G
ADSP-1016KD	7216L140C
ADSP-1016KG	7216L140G
ADSP-1016SD	7216L185CB
ADSP-1016SG	7216L185GB
ADSP-1016TD	7216L120CB
ADSP-1016TG	7216L120GB

CYPRESS	IDT
7C401	**72401**
7C401-10DC	72401L10D
7C401-10DMB	74201L10DB
7C401-10LC	72401L10L
7C401-10LMB	72401L10LB
7C401-10PC	72401L10P
7C401-15DC	72401L15D
7C401-15DMB	72401L15DB
7C401-15LC	72401L15L
7C401-15LMB	72401L15LB
7C401-15PC	72401L15P
7C402	**72402**
7C402-10DC	72402L10D
7C402-10DMB	72402L10DB
7C402-10LC	72402L10L
7C402-10LMB	72402L10LB
7C402-10PC	72402L10P
7C402-15DC	72402L15D
7C402-15DMB	72402L15DB
7C402-15LC	72402L15L
7C402-15LMB	72402L15LB
7C402-15PC	72402L15P
7C403	**72403**
7C403-10DC	72403L10D
7C403-10DMB	72403L10DB
7C403-10LC	72403L10L
7C403-10LMB	72403L10LB
7C403-10PC	72403L10P
7C403-15DC	72403L15D

CYPRESS CONT.	IDT
7C403-15DMB	72403L15DB
7C403-15LC	72403L15L
7C403-15LMB	72403L15LB
7C403-15PC	72403L15P
7C403-25DC	72403L25D
7C403-25DMB	72403L25DB
7C403-25LC	72403L25L
7C403-25LMB	72403L25LB
7C403-25PC	72403L25P
7C404	**72404**
7C404-10DC	72404L10D
7C404-10DMB	72404L10DB
7C404-10LC	72404L10L
7C404-10LMB	72404L10LB
7C404-10PC	72404L10P
7C404-15DC	72404L15D
7C404-15DMB	72404L15DB
7C404-15LC	72404L15L
7C404-15LMB	72404L15LB
7C404-15PC	72404L15P
7C404-25DC	72404L25D
7C404-25DMB	72404L25DB
7C404-25LC	72404L25L
7C404-25LMB	72404L25LB
7C404-25PC	72404L25P
7C510	**7210**
7C510-45DC	7210L45D
7C510-45GC	7210L45G
7C510-45LC	7210L45L
7C510-45PC	7210L45P
7C510-55DC	7210L55D
7C510-55DMB	7210L55DB
7C510-55GC	7210L55G
7C510-55GMB	7210L55GB
7C510-55LC	7210L55L
7C510-55LMB	7210L55LB
7C510-55PC	7210L55P
7C510-65DC	7210L65D
7C510-65DMB	7210L65DB
7C510-65GC	7210L65G
7C510-65GMB	7210L65GB
7C510-65LC	7210L65L
7C510-65LMB	7210L65LB
7C510-65PC	7210L65P
7C510-75DC	7210L75D
7C510-75DMB	7210L75DB
7C510-75GC	7210L75G
7C510-75GMB	7210L75GB
7C510-75LC	7210L75L
7C510-75LMB	7210L75LB
7C510-75PC	7210L75P
7C516	**7216**
7C516-38DC	7216L35D
7C516-38GC	7216L35G
7C516-38LC	7216L35L
7C516-38PC	7216L35P
7C516-42DMB	7216L40DB
7C516-42GMB	7216L40GB
7C516-42LMB	7216L40LB
7C516-45DC	7216L45D
7C516-45GC	7216L45G
7C516-45LC	7216L45L

CYPRESS CONT.	IDT
7C516-45PC	7216L45P
7C516-55DC	7216L55D
7C516-55DMB	7216L55DB
7C516-55GC	7216L55G
7C516-55GMB	7216L55GB
7C516-55LC	7216L55L
7C516-55LMB	7216L55LB
7C516-55PC	7216L55P
7C516-65DC	7216L65D
7C516-65DMB	7216L65DB
7C516-65GC	7216L65G
7C516-65GMB	7216L65GB
7C516-65LC	7216L65L
7C516-65LMB	7216L65LB
7C516-65PC	7216L65P
7C516-75DC	7216L75D
7C516-75DMB	7216L75DB
7C516-75GC	7216L75G
7C516-75GMB	7216L75GB
7C516-75LC	7216L75L
7C516-75LMB	7216L75LB
7C516-75PC	7216L75P
7C517	**7217**
7C517-45DC	7217L45D
7C517-45GC	7217L45G
7C517-45LC	7217L45L
7C517-45PC	7217L45P
7C517-55DC	7217L55D
7C517-55DMB	7217L55DB
7C517-55GC	7217L55G
7C517-55GMB	7217L55GB
7C517-55LC	7217L55L
7C517-55LMB	7217L55LB
7C517-55PC	7217L55P
7C517-65DC	7217L65D
7C517-65DMB	7217L65DB
7C517-65GC	7217L65G
7C517-65GMB	7217L65GB
7C517-65LC	7217L65L
7C517-65LMB	7217L65LB
7C517-65PC	7217L65P
7C517-75DC	7217L75D
7C517-75DMB	7217L75DB
7C517-75GC	7217L75G
7C517-75GMB	7217L75GB
75C17-75LC	7217L75L
7C517-75LMB	7217L75LB
7C517-75PC	7217L75P

MMI	IDT
67401	**72401**
57401AJB	72401L15DB
57401BJB	72401L25DB
57401JB	72401L10DB
67401AJ	72401L15D
67401AN	72401L15P

NOTE:
BOLD FACE ITEMS ARE
FUNCTIONAL REPLACEMENTS

MMI CONT.	IDT
67401BJ	72401L25D
67401J	72401L10D
67401N	72401L10P
C57401AJB	72401L15DB
C57401BJB	72401L25DB
C57401JB	72401L10DB
C57L401DJB	72401L15DB
C67401AJ	72401L15D
C67401AN	72401L15P
C67401BJ	72401L25D
C67401J	72401L10D
C67401N	72401L10P
C67L401DJ	72401L15D
C67L401DN	72401L15P
67402	**72402**
57402AJB	72402L15DB
57402BJB	72402L25DB
57402JB	72402L10DB
67402AJ	72402L15D
67402AN	72402L15P
67402BJ	72402L25D
67402J	72402L10D
67402N	72402L10P
C57402AJB	72402L15DB
C57402BJB	72402L25DB
C57402JB	72402L10DB
C57L402DJB	72402L15DB
C67402AJ	72402L15D
C67402AN	72402L15P
C67402BJ	72402L25D
C67402J	72402L10D
C67402N	72402L10P
C67L402DJ	72402L15D
C67L402DN	72402L15P
67411	**72401**
57411JB	72401L25DB
67411AJ	72401L35D
67411J	72401L25D
67412	**72402**
57412JB	72402L25DB
67412AJ	72402L35D
67412J	72402L25D
67413	**72413**
57413JB	72413L25DB
67413AJ	72413L35D
67413J	72413L25D
67C401	**72401**
67C401-10N	72401L10P
67C401-10J	72401L10D
67C401-15N	72401L15P
67C401-15J	72401L15D
67C4013	**72403**
67C4013-10N	72403L10P
67C4013-10J	72403L10D
67C4013-15N	72403L15P
67C4013-15J	72403L15D
67C402	**72402**
67C402-10N	72402L10P
67C402-10J	72402L10D
67C402-15N	72402L15P
67C402-15J	72402L15D
67C4013	**72404**

MMI CONT.	IDT
67C4023-10N	72404L10P
67C4023-10J	72404L10D
67C4023-15N	72404L15P
67C4023-15J	72404L15D

THOMSON-MOSTEK	IDT
MK4501	**7201**
MK4501-10N	7201S80P
MK4501-12N	7201S120P
MK4501-65N	7201S65P
MK4501-8N	7201S80P
MK4503	**7203**
MK4503-10N	7203S80P
MK4503-12N	7203S120P
MK4503-65N	7203S65P
MK4503-8N	7203S80P

TRW	IDT
MPY012	**7212**
MPY012HJ1A	7212L140CB
MPY012HJ1C	7212L115C
MPY012HJ1G	7212L115C
MPY016	**7216**
MPY016HJ1A	7216L185CB
MPY016HJ1C	7216L140C
MPY016HJ1C	7216L140C
MPY016KJ1A	7216L45CB
MPY016KJ1A1	7216L45CB
MPY016KJ1C	7216L45C
MPY016KJ1C1	7216L35C
MPY016KJ1G	7216L45C
MPY016KJ1G1	7216L35C
TMC216H	**7216**
TMC216HC1A	7216L185LB
TMC216HC1C	7216L140L
TMC216HC1G	7216L140L
TMC216HJ3A	7216L185CB
TMC216HJ3C	7216L140C
TMC216HJ3G	7216L140C
TDC1009	**7209**
TDC1009C1A	7209170LB
TDC1009C1F	7209L170LB
TDC1009J1A	7209L170CB
TDC1009J1C	7209L135C
TDC1009J1F	7209L170CB
TDC1009J1G	7209L135C
TDC1010	**7210**
TDC1010C1A	7210L200LB
TDC1010C1F	7210L200LB
TDC1010J1A	7210L200CB
TDC1010J1C	7210L165C
TDC1010J1F	7210L200CB
TDC1010J1G	7210L165C
TDC1043	**7243**
TDC1043C1C	7243L100L
TDC1043C1G	7243L100L
TDC1043J3C	7243L100C
TDC1043J3G	7243L100C
TMC2009	**7209**

TRW CONT.	IDT
TMC2009C1A	7209L170LB
TMC2009C1C	7209L135L
TMC2009C1F	7209L120LB
TMC2009C1G	7209L135L
TMC2009J3A	7209L170CB
TMC2009J3C	7209L135C
TMC2009J3F	7209L120CB
TMC2009J3G	7209L135C
TMC2010	**7210**
TMC2010C1C	7210L165L
TMC2010C1C	7210L200LB
TMC2010C1F	7210L200LB
TMC2010C1G	7210L165L
TMC2010J3A	7210L200CB
TMC2010J3C	7210L165C
TMC2010J3F	7210L200CB
TMC2010J3G	7210165C
TMC2110	**7210**
TMC2110C1C	7210L100L
TMC2110C1C	7210L120LB
TMC2110C1F	7210L120LB
TMC2110C1G	7210L100L
TMC2110J3C	7210L100C
TMC2110J3C	7210L120CB
TMC2110J3F	7210L120CB
TMC2110J3G	7210L100C
TMC1043	**7243**
TDC1043C1C	7243L100L
TDC1043C1G	7243L100L
TDC1043J3C	7243L100C
TDC1043J3G	7243L100C
TMC2009	**7209**
TMC2009C1A	7209L170LB
TMC2009C1C	7209L135L
TMC2009C1F	7209L120LB
TMC2009C1G	7209L135L
TMC2009J3A	7209L170CB
TMC2009J3C	7209L135C
TMC2009J3F	7209L120CB
TMC2009J3G	7209L135C
TMC2010	**7210**
TMC2010C1C	7210L165L
TMC2010C1C	7210L200LB
TMC2010C1F	7210L200LB
TMC2010C1G	7210L165L
TMC2010J3A	7210L200CB
TMC2010J3C	7210L165C
TMC2010J3F	7210L200CB
TMC2010J3G	7210L165C
TMC2110	**7210**
TMC2110C1C	7210L100L
TMC2110C1C	7210L120LB
TMC2110C1F	7210L120LB
TMC2110C1G	7210L100L
TMC2110J3C	7210L100C
TMC2110J3C	7210L120CB
TMC2110J3F	7210L120CB
TMC2110J3G	7210L100C

NOTE:
BOLD FACE ITEMS ARE
FUNCTIONAL REPLACEMENTS

WEITEK	IDT
WTL2010	**7210**
WTL2010AGCD	7210L65G
WTL2010AGMD	7210L75GB
WTL2010AJC	7210L65C
WTL2010AJC	7210L65C
WTL2010AJM	7210L75CB
WTL2010ALCC	7210L65L
WTL2010ALMC	7210L75LB
WTL2010BGCD	7210L45G
WTL2010BGMD	7210L55GB
WTL2010BJC	7210L45C
WTL2010BJM	7210L55CB
WTL2010BLCC	7210L45L
WTL2010BLMC	7210L55LB
WTL2010GCD	7210L100G
WTL2010GMD	7210L120GB
WTL2010JC	7210L100C
WTL2010JM	7210L120CB
WTL2010LCC	7210L100L
WTL2010LMC	7210L120LB
WTL2016	**7216**
WTL2016AGCD	7216L65G
WTL2016AGMD	7216L75GB
WTL2016AJC	7216L65C
WTL2016AJM	7216L75CB
WTL2016ALCC	2716L65L
WTL2016ALMC	7216L75LB
WTL2016BGCD	7216L45G
WTL2016BGMD	7216L55GB
WTL2016BJC	7216L45C
WTL2016BJM	7216L55CB
WTL2016BLCC	7216L45L
WTL2016BLMC	7216L55LB
WTL2016CGCD	7216L35G
WTL2016CGMD	7216L45GB
WTL2016CJC	7216L35C
WTL2016CJM	7216L45CB
WTL2016CLCC	7216L35L
WTL2016CLMC	7216L45LB
WTL2016GCD	7216L90G
WTL2016GMD	7216L120GB
WTL2016JC	7216L90C
WTL2016JM	7216L120CB
WTL2016LCC	7216L90L
WTL2016LMC	7216L120LB
WTL2017	**7217**
WTL2017AGCD	7217L65G
WTL2017AGMD	7217L75GB
WTL2017AJC	7217L65C
WTL2017AJM	7217L75CB
WTL2017ALCC	7217L65L
WTL2017ALMC	7217L75LB
WTL2017BGCD	7217L45G
WTL2017BGMD	7217L55GB
WTL2017BJC	7217L45C
WTL2017BJM	7217L55CB
WTL2017BLCC	7217L45L
WTL2017BLMC	7217L55LB
WTL2017CGCD	7217L35G
WTL2017CGMD	7217L45GB
WTL2017CJC	7217L35C
WTL2017CJM	7217L45CB

WEITEK CONT.	IDT
WTL2017CLCC	7217L35L
WTL2017CLMC	7217L45LB
WTL2017GCD	7217L90G
WTL2017GMD	7217L120GB
WTL2017JC	7217L90C
WTL2017JM	7217L120CB
WTL2017LCC	7217L90L
WTL2017LMC	7217L120LB
WTL1264	**721264**
WTL1264GCD	721264L60G
WTL1265	**721265**
WTL1265GCD	721265L60G

Integrated Device Technology, Inc.

DATA CONVERSION CROSS REFERENCE GUIDE

EXACT PIN REPLACEMENTS	
TRW	**IDT**
TDC1018	IDT75C18
TDC1048	IDT75C48
HONEYWELL	**IDT**
HDAC10180	IDT75C18
SONY	**IDT**
CXA1096P	IDT78C48
BROOKTREE	**IDT**
BT458	IDT78C458

FUNCTIONAL EQUIVALENTS	
PART NO.	**IDT**
AD9700	IDT75C18
AD9768	IDT75C18
BT101	IDT75C18
BT102	IDT75C18
BT106	IDT75C18
BT108	IDT75C18
CA3308	IDT75C48
CX20052	IDT75C48
EDH-10605	IDT75C18
EDH-10805	IDT75C18
HA19209	IDT75C48
HA19210	IDT75C48
MB40548	IDT75C48
MC10318	IDT75C48
MC10319	IDT75C48
MN0605	IDT75C18
MN0805	IDT75C18
MP7683	IDT75C48
MP7684	IDT75C48
PNA7518	IDT75C18
RGB-DAC83	IDT78C18
SDA8005	IDT75C18
SP9768	IDT75C18
T1595	IDT75C48
TML1080	IDT75C48
TML1840	IDT75C18
VDAC-0605	IDT75C18
VDAC-0805H	IDT75C18
VDAC-888E	IDT75C18
VDAC-888T	IDT75C18

Integrated Device Technology, Inc.

SUBSYSTEMS CROSS REFERENCE GUIDE

EDI	IDT
EDH8M8128C100	8M824L100C
EDH8M8128C120	8M824L100C
EDH8M8128C150	8M824L100C
EDH8M8128C100CB*	8M824S100CB
EDH8M8128C120CB*	8M824S100CB
EDH8M8128C150CB*	8M824S100CB
EDH81H256C-55	8M156S55CS
EDH81H256C-70	8M156S70CS
EDH816H64C-55*	7M624S55CB
EDH816H64C-70*	7M624S65CB
EDH84H64C-55	8MP456S55S
EDH84H64C-70	8MP456S70S
EDH8808HC-55*	**8M864L55CB**
EDH8808HC-70*	**8M864L75CB**
EDH8808A-10*	7M864L85CB
EDH8808A-12*	7M864L120CB
EDH8808A-15*	7M864L150CB
EDH8808C-10*	8M864L85CB
EDH8808C-12*	8M864L120CB
EDH8808C-15*	8M864L150CB
EDH8808CL-20*	8M864L150CB
EDH8808CL-25*	8M864L150CB
EDH8808AL-20*	7M864L150CB
EDH8808AL-25*	7M864L150CB
EDH8832C-12	8M856L85C
EDH8832C-15	8M856L85C
EDH8832C-20	8M856L85C
EDH8832C-12*	8M856L100CB
EDH8832C-15*	8M856L100CB
EDH8832C-20*	8M856L100CB
EDH8832HC-70*	7M856S65CB
EDH8832HC-85*	7M856S75CB

DENSE PAC	IDT
DPS1024-XXX	**7M624**
DPS1026-XXX	**7M624**
DPS1027-XXX	7M624
DPS16X5-XXX	8MP564
DPS257-XXX	7M656
DPS32H8-XXX	7M856
DPS40256-XXX	**8M856**
DPS41257-XXX	8M856
DPS41288-XXX	8M824
DPS6432-XXX	7M4017
DPS8645-XXX	8MP456
DPS8088-XXX	7M864

OTHER VENDORS		IDT
MOSEL	MS88128	8M824
ZYREL	Z108	8M824
NEC	MC-120	8M824
HITACHI	HM66204	8M824

*MILITARY RAMS

NOTE:
BOLD FACE ITEMS ARE
FUNCTIONAL REPLACEMENTS

2

IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the 80's and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary CEMOS ™ technology, a twin-well dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, our product strategy has been to apply the advantages of our extremely fast CEMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost, weight, and size. Many of our innovative product designs offer higher levels of integration, advanced architectures, higher density packaging, and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Producing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is the leading U.S. supplier of high-speed CMOS circuits. The company's high-performance static RAMs, logic, DSP, MICROSLICE ™ bit-slice microprocessor products, data conversion devices, Electrically Erasable PROMs, and modular subsystem assemblies complement each other to provide high-speed CMOS solutions to a wide range of applications and systems.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufactuer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families and additional product lines will be introduced. Contact your IDT field representative or factory marketing at 1-800-IDT-CMOS to determine the latest product offerings. If you're building state-of-the-art equipment, IDT may be able to solve some of your design problems.

IDT MILITARY AND DESC-SMD PROGRAM

IDT is a leading supplier of military, high-speed CMOS circuits. The company's high-performance static RAMs, Logic, DSP, Microprocessor, Data Conversion, Electrically Erasable memories and Modular Subsystem product lines complement each other to provide high-speed CMOS solutions to a wide range of military applications and systems. Each product line offers products which are fully compliant to the latest revision of MIL-STD-883. In addition, IDT offers radiation tolerant, as well as enhanced, products.

IDT has an active program to have a Defense Electronic Supply Center (DESC) listing for Standard Military Drawings (SMD) of its products. The SMD program allows standardization of militarized products and reduction of the proliferation of nonstandard source control drawings. This program will go far toward reducing the need for each defense contractor to make separate specification control drawings for purchased parts. IDT plans to have SMDs for many of its product offerings. Presently, IDT has 22 devices which are listed or pending listing. The devices are from IDT's SRAM, DSP, Logic and Microprocessor product lines. Additional devices are being added from those product lines as well as from Data Conversion and EEPROMs. IDT expects the number of SMDs to be over 50 in 1988. Users should contact either IDT or DESC for current status of products in the SMD program.

SMD	
SRAM	**IDT**
5962-86705	IDT6168
5962-85525	IDT7164
84036	IDT6116
5962-84132	IDT6167
5962-86015	IDT7187
5962-86859	IDT7198
5962-86875	IDT7130/7140
5962-87002	IDT7132/7142
5962-88552	IDT71256
DSP	**IDT**
5962-87531	IDT7201
5962-86873	IDT7216
5962-86846	IDT72404
LOGIC	**IDT**
5962-87630	IDT54FCT244
5962-87629	IDT54FCT245
5962-86862	IDT54FCT299
5962-87644	IDT54FCT373
5962-87628	IDT54FCT374
5962-87627	IDT54FCT377
5962-87654	IDT54FCT138
5962-87655	IDT54FCT240
5962-87656	IDT54FCT273
MICROPROCESSOR	**IDT**
5962-87708	IDT39C10

RADIATION HARDENED TECHNOLOGY

IDT manufactures and supplies radiation hardened products for military/aerospace applications. Utilizing special processing and starting materials, IDT's radiation hardened devices are able to survive in hostile radiation environments. In total dose, dose rate and environments where single event upset is of concern, IDT products are designed to continue functioning without loss of performance. IDT can supply all of its products on these processes.

Total Dose radiation testing is performed in-house on an ARACOR X-Ray system. External facilities are utilized for device research on gamma cell, LINAC and other radiation equipment. IDT has an ongoing research and development program for improving radiation handling capabilities (See "IDT Radiation Tolerant/Enhanced Products for Radiation Environments" in Section 3) of IDT products/processes.

IDT LEADING EDGE CEMOS TECHNOLOGY

HIGH-PERFORMANCE CEMOS

CEMOS™ (the "E" stands for enhanced) is a state-of-the-art proprietary CMOS technology initially developed and continually refined by IDT to be at the leading-edge of new high-speed CMOS processes. It incorporates the best characteristics of traditional CMOS, including low power, high noise immunity and wide operating temperature range; it also achieves speed and output drive equal or superior to bipolar Schottky TTL.

The company has been producing CEMOS products in large volume for over six years. During this time, CEMOS technology has been re-engineered and refined from the original 2.5 micron CEMOS I to the present CEMOS III direct step-on-wafer, dry etch process providing gate lengths as small as submicron (Figure 1). Continual advancement of CEMOS technology allows IDT to implement progressively higher levels of integration and achieve increasingly faster speeds maintaining the company's established position as the leader in high-speed CMOS integrated circuits.

CEMOS is a technology designed to optimize high-speed, low-power and dense integration of advanced architecture VLSI and memory products.

	CEMOS I	CEMOS II			CEMOS III	
		A	B	C	A	B
Year	1981	1983	1984	1985	1986	1987
Drawn Feature Size	2.5μ	1.7μ	1.5μ	1.5μ/1.2μ	1.3μ	1.2μ
Leff	1.3μ	1.1μ	0.9μ	0.9μ	0.9μ	0.8μ
Basic Process	Dual Well Oxide Isolated Ion Implanted Wet Etch Projection Aligned	Dry Etch Stepper Aligned				
Enhancements			Shrink	Spacer	Silicide LDD BPSG	Shrink BiCEMOS™ Multi-Layer Metal

CEMOS IV = CEMOS III – scaled process optimized for high-speed logic.

Figure 1.

DUAL-WELL STRUCTURES

CEMOS is constructed using an advanced dual-well, or twin-well, process architecture (Figure 2) to optimize the overall characteristics of a high-performance CMOS process. CMOS processes using only "P-Wells" result in inferior P (or N) channel transistors or compromised P/N channels. This compromise is largely eliminated by utilizing both a deep underlying main "well" (in this case a "P-Well" in "N-substrate") and by altering the doping profile nearer the surface of the P-channel transistor regions. The latter region becomes the "N-Well" of the dual-well process. This technique allows the fabrication of high-performance transistors in both polarities.

The industry now recognizes that the best combination of balanced capabilities is achieved using this dual-well approach. This construction technique supresses punch-through, minimizes junction capacitance and transistor body effects and allows extremely fast speeds. In addition, it significantly reduces soft errors induced by high-energy alpha particles in fine line geometry memory products.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

Another traditional limitation associated with many MOS and bipolar products is electrostatic discharge induced failures. This problem has also been solved by a combination of IDT's CEMOS process and proper circuit design. All IDT products incorporate proprietary ESD protection circuitry on all inputs and outputs to ensure that they are insensitive to repeated application of ESD stress and do not exhibit the degradation found in other MOS or bipolar products which can eventually result in product failure.

IDT CEMOS
Device Cross Section

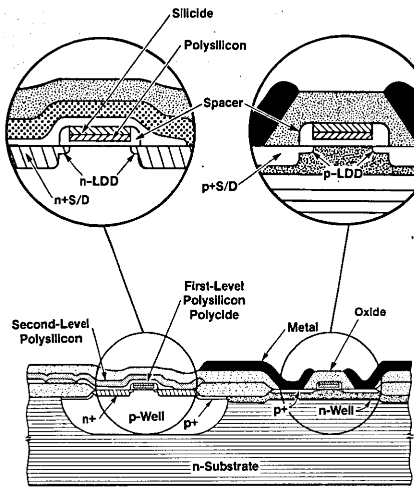


Figure 2.

IDT CEMOS
Built-In High Alpha Particle Immunity

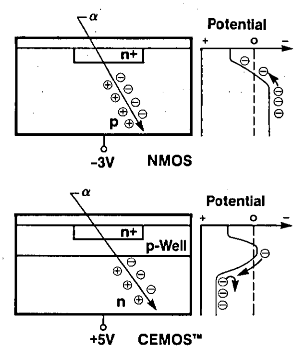


Figure 3.

ALPHA PARTICLES

Random alpha particles can cause memory cells to temporarily lose their contents or suffer a "soft error." Traveling with high energy levels, alpha particles penetrate deep into an integrated chip. As they burrow into the silicon, they leave a trail of free electron-hole pairs in their wake.

The cause of alpha particles in well documented and understood in the industry. IDT has considered various techniques to protect the cells from this hazardous occurrence. These techniques include dual-well structures (Figures 2 & 3) and a polymeric compound for die coating. Presently, a polymeric compound is used in many of IDT's SRAMs; however, the specific technique used may vary and change from device generation to the next as the industry and IDT improve the alpha particle protection technology.

LATCHUP IMMUNITY

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes (Figure 4). The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are utilized on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents form 10-20mA, IDT products inhibit latchup at trigger currents substantially greater than 700mA.

IDT CEMOS
Latchup Suppression

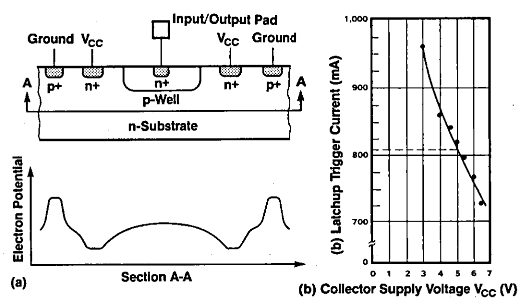


Figure 4.

SURFACE MOUNT TECHNOLOGY

To take full advantage of the low-power aspect of CMOS, and obtain two to three times the space savings, CMOS products should be used as SMDs (surface mount devices). However, most integrated circuits sold today are still packaged in the traditional DIP (dual in-line package) configuration and there is a tremendous support industry to handle thru-board assembly.

Determined to utilize CMOS advantages, IDT re-invented the DIP. This was accomplished by developing multilayered substrates (either co-fired ceramic or glass filled epoxy FR-4) with dual in-line (DIP) or single in-line (SIP) pins. An advanced vapor phase reflow surface mount technology was also developed after exhaustive evaluation proved vapor phase reflow to be the most efficient method of heat transfer and to produce the most reliable solder connections available.

Products that are to be interconnected to form larger electronic elements are electrically tested, environmentally screened, performance selected and then thermally matched to the appropriate ceramic or glass filled epoxy substrates. After modular assembly, the finished product is 100% re-tested to ensure that it completely performs to the specifications required.

As a result, IDT produces extraordinarily dense, high-speed combinations of monolithic ICs as complex subsystem modular assemblies. These modules convert SMDs to user-friendly DIPs/SIPs providing customers with the density advantages of surface mount in a format compatible with their extensive, thru-board, assembly expertise.

STATE-OF-THE-ART FACILITIES AND CAPABILITIES

Integrated Device Technology is headquartered in Santa Clara, California — the heart of the "Silicon Valley." The company's operations are housed in five facilities totaling close to 400,000 square feet. These facilities incorporate all aspects of business from research and development to design, wafer fabrication, assembly, environmental screening, test and administration. Inhouse capabilities incorporate scanning electron microscope (SEM) evaluation, particle impact noise detection (PIND), plastic packaging, military and commercial testing, burn-in, life test and a full complement of environmental screening equipment.

IDT's 54,000 square foot Corporate Headquarters houses technology and product research and development. Teams equipped with state-of-the-art computerized design and analytical tools conduct the continuous research and development required to push CEMOS technology forward and to create future product lines. This facility contains a 10,000 square foot Class 10 (no more than 10 particles larger than 0.2 micron per cubic foot) wafer fabrication clean room used to produce the Microprocessor, DSP and Logic product families, as well as support R&D.

Located adjacent to the headquarter facility, forming an IDT corporate campus, is a 100,000 square foot two-building complex that houses the DSP Division and Microprocessor product line. Design and product teams, along with administrative functions, are situated in these buildings.

A second small wafer fabrication area, used for research and development, is also located at this site. This facility houses its own design tools, laboratories, test and burn-in facilities and in-house plastic assembly.

IDT's Subsystem Division is housed in a third Santa Clara location, only a few blocks away from the other sites. This 37,000 square foot facility contains the development and product teams that produce IDT's FCT, AHCT, IDT39C800 logic families and modular assemblies. Included at this facility are a quick turnaround hermetic package assembly line and an advanced vapor phase reflow surface mounting module assembly area.

IDT's largest facility is located in Salinas, California, about an hour away from Santa Clara. This is the Static RAM Division's headquarters, a 100,000 square foot facility located on a 14 acre site. Constructed in 1985, this facility houses an ultra-modern 25,000 square foot high-volume wafer fabrication area measured at Class 2-to-3 clean room conditions (a maximum of 2 to 3 particles per cubic foot of 0.2 micron or larger). Careful design and construction created a clean room environment far beyond the average of U.S. fab areas (Class 100), capable of producing large volumes of very high-density submicron geometry, fast static RAMs. This facility also houses shipping areas for IDT's leadership family of CMOS static RAMs. This site has future expansion capabilities to accomodate a 250,000 square foot complex.

IDT's Packaging and Assembly Process Development teams are located at the Corporate Headquarters in Santa Clara. To keep pace with the development of new products and to enhance the IDT philosophy of "Innovation," these teams have ultra modern, integrated and correspondingly sophisticated equipment and environments at their disposal. All manufacturing is completed in dedicated clean room areas (Class 10K minimum), with all preseal operations accomplished under Class 100 Laminar Flow Hoods.

Development of assembly materials, processes and equipment is accomplished in these two facilities under a fully operational production environment to ensure reliability and repeatable product. The Hermetic Manufacturing and Process Development team is currently producing custom products to the strict requirements of MIL-STD-883. The fully automated plastic facility is currently producing high volumes of USA manufactured product while developing state-of-the-art surface mount technology, patterned after MIL-STD-883.

To extend these philosophies while maintaining strict control of our processes, IDT has acquired an operational Assembly and Test facility located in Penang, Malaysia. This facility is being upgraded to USA standards and will be fully operational mid-1988. As in the USA facility, all assemblies will be accomplished under laminar flow conditions (Class 100) until the silicon is encased in its final packaging. All products in this facility will be manufactured to the quality control requirements of MIL-STD-883.

IDT's facilities total nearly 400,000 square feet of floor space and house three wafer fabrication clean rooms, four assembly lines, five test areas and four burn-in areas. All of these facilities are aimed at increasing our manufacturing productivity to supply ever larger volumes of high-performance, cost-effective leadership CMOS products.

SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing—as opposed to being "tested-in" later—in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials and chemicals are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883 and MIL-M-38510.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

For module assemblies, additional screening of the fully assembled substrates is performed to assure package integrity and mechanical reliability. One-hundred percent electrical tests are performed on the finished module to ensure compliance with the defined "subsystem" specifications.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial and military grade products consistently meet customer requirements for quality, reliability and performance.

SPECIAL PROGRAMS

Class S. IDT also has all manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform complete Class S processing per MIL-STD-883 on all IDT products and has supplied Class S products on several programs.

Radiation Hardened. IDT has developed and supplied several levels of radiation hardened products for military/aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.

Product Selector and Cross Reference Guides

Technology/Capabilities

Quality and Reliability

3

Static RAMs

Dual-Port RAMs

FIFO Memories

Digital Signal Processing (DSP)

Bit-Slice Microprocessor Devices (MICROSLICE™) and EDC

Reduced Instruction Set Computer (RISC) Processors

Logic Devices

Data Conversion

E^2PROMS-Electrically Erasable Programmable Read Only Memories

Subsystems Modules

Application and Technical Notes

Package Diagram Outlines

MILITARY DATA SHEET PARAMETRIC TEST

For compliant MIL-STD-883 products, IDT tests all electrical parameters except those parameters which are footnoted in the data sheet as being guaranteed by design or as a summation of other parameters. There are no electrical tests performed in production or at Group A sample tests for those particular electrical parameters.

In this 1988 Data Book, IDT has identified the electrical parameters which are guaranteed by design. However, there were omissions is some of the data sheets and the following electrical parameters should have had a footnote identifying them as being untested but guaranteed by design.

PART NUMBER	PARAMETER
IDT39C01C/D/E	Cycle Time and Clock Characteristics: Read-Modify-Write Cycle, Maximum Clock Frequency to shift Q, Min. Clock Period
IDT39C03A/39C03B	V_{IH}, V_{IL}, Min. clock low time, Min. clock high time, Min. time CP and WE both low to write, Multiply Instructions table, Divide Instructions table, Sign magnitude to two's complement conversion table, single length normalization table
IDT39C60/-1/A	Combinational Propagation Delays: Generate (to $DATA_{0-15}$), LE_{DIAG} (to $DATA_{0-15}$), Internal control mode LE_{DIAG} (to $DATA_{0-15}$), Internal control mode $DATA_{0-15}$ (to $DATA_{0-15}$), Generate (to LE_{OUT}), Set-up and Hold Time Relative to Latch Enable
IDT39C203/39C203A	V_{IH}, V_{IL}, Min. clock low time, Min. clock high time, Min. time CP and WE both low to write, Multiply Instructions table, Divide Instructions table, BCD Instructions table, Sign magnitude to two's complement conversion table, single length normalization table
IDT39C705A/B	V_{IH}, V_{IL}
IDT39C707A/B	V_{IH}, V_{IL}
IDT49C401/A	V_{IH}, V_{IL}; Cycle time and clock characteristics: Read-modify-write cycle, Max. clock frequency to shift Q, Min. clock period
IDT49C402/A	V_{IH}, V_{IL}; Cycle time and clock characteristics: Read-modify-write cycle, Max. clock frequency to shift Q, Min. clock period
IDT49C403/A	V_{IH}, V_{IL}, Multiply Instructions table, BCD Instructions table, sign magnitude to two's complement conversion table, Divide Instruction table, single length normalization table
IDT49C460/A/B	Combinational Propagation Delays: Generate (to $DATA_{0-31}$), LE_{DIAG} (to $DATA_{0-31}$), Internal control mode LE_{DIAG} (to $DATA_{0-31}$), Internal control mode $DATA_{0-31}$ (to $DATA_{0-31}$)
IDT7200S/L	t_{RLZ}, t_{WLZ}, t_{RHZ}, t_{RPE}, t_{WPF}
IDT7201SA/LA	t_{RLZ}, t_{WLZ}, t_{RHZ}, t_{RPE}, t_{WPF}
IDT7202SA/LA	t_{RLZ}, t_{WLZ}, t_{RHZ}, t_{RPE}, t_{WPF}
IDT7203S/L	t_{RLZ}, t_{WLZ}, t_{RHZ}, t_{RPE}, t_{WPF}
IDT72103	t_{RLZ}, t_{WLZ}, t_{RHZ}, t_{PD1}, t_{PD2}, t_{SOHZ}, t_{SOLZ}, t_{OEHZ}, t_{OELZ}
IDT72401	t_{SIR}, t_{HIR}, t_{SOR}, t_{IPH}, t_{OPH}
IDT72402	t_{SIR}, t_{HIR}, t_{SOR}, t_{IPH}, t_{OPH}
IDT72403	t_{SIR}, t_{HIR}, t_{SOR}, t_{HZOE}, t_{IPH}, t_{OPH}
IDT72404	t_{SIR}, t_{HIR}, t_{SOR}, t_{HZOE}, t_{IPH}, t_{OPH}
IDT72413	t_{IPH}, t_{OPH}, t_{ORD}, t_{PHZ}, t_{PLZ}, t_{PZL}, t_{PZH}
IDT75C18	C_{REF}, C_I, V_{OCP}, V_{OCN}, R_O, C_O, F_S, t_{PWL}, t_{PWH}, t_H, t_{SI}, t_{RI}, BWR, TCG, DG, GC, GI, GE, FT_C, PSRR (with 60Hz ripple), V_{IL}, V_{IH}, V_{ICM}
IDT75C19	C_{REF}, C_I, V_{OCP}, V_{OCN}, R_O, C_O, F_S, t_{PWL}, t_{PWH}, t_H, t_{SI}, t_{RI}, BWR, TCG, DG, GC, GI, GE, FT_C, PSRR (with 60Hz ripple), V_{IL}, V_{IH}, V_{ICM}
IDT75C458	t_{CLKT}, t_{VT}, t_S, T_{SI}, FT, G_E, CT
IDT75C48	R_{IN}, C_{IN}, C_I, T_{CO}, T_{TR}, E_{AP}, V_{IL}, V_{IH}
IDT75C58	t_{HZ}, t_{LZ}, t_{ZH}, t_{ZL}, R_{IN}, C_{IN}, I_{OZ}, C_I, C_O, T_{CO}, T_{TR}, E_{AP}

IDT QUALITY CONFORMANCE PROGRAM

A COMMITMENT TO QUALITY

Integrated Device Technology's monolithic and modular assembly products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design and manufacturing criteria of the Quality and Reliability Assurance Program were developed and are being maintained to the most current revisions of MIL-M-38510 and MIL-STD-883 requirements.

Product flow and test procedures for all Class B *monolithic* hermetic Military Grade microcircuits are in full compliance with paragraph 1.2.1 of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all *modular* hermetic products are fully compliant with the MIL-STD-883 test procedures for electronic module assemblies on ceramic substrates.

Product flow and test procedures for all *plastic* and *commercial hermetic* products are in accordance with industry practices for producing highly reliable microcircuits to ensure that products meet the IDT requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our products consistently meet customer requirements for quality, reliability and performance.

SUMMARY

MONOLITHIC HERMETIC PACKAGE PROCESSING FLOW(1)

Refer to the Monolithic Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

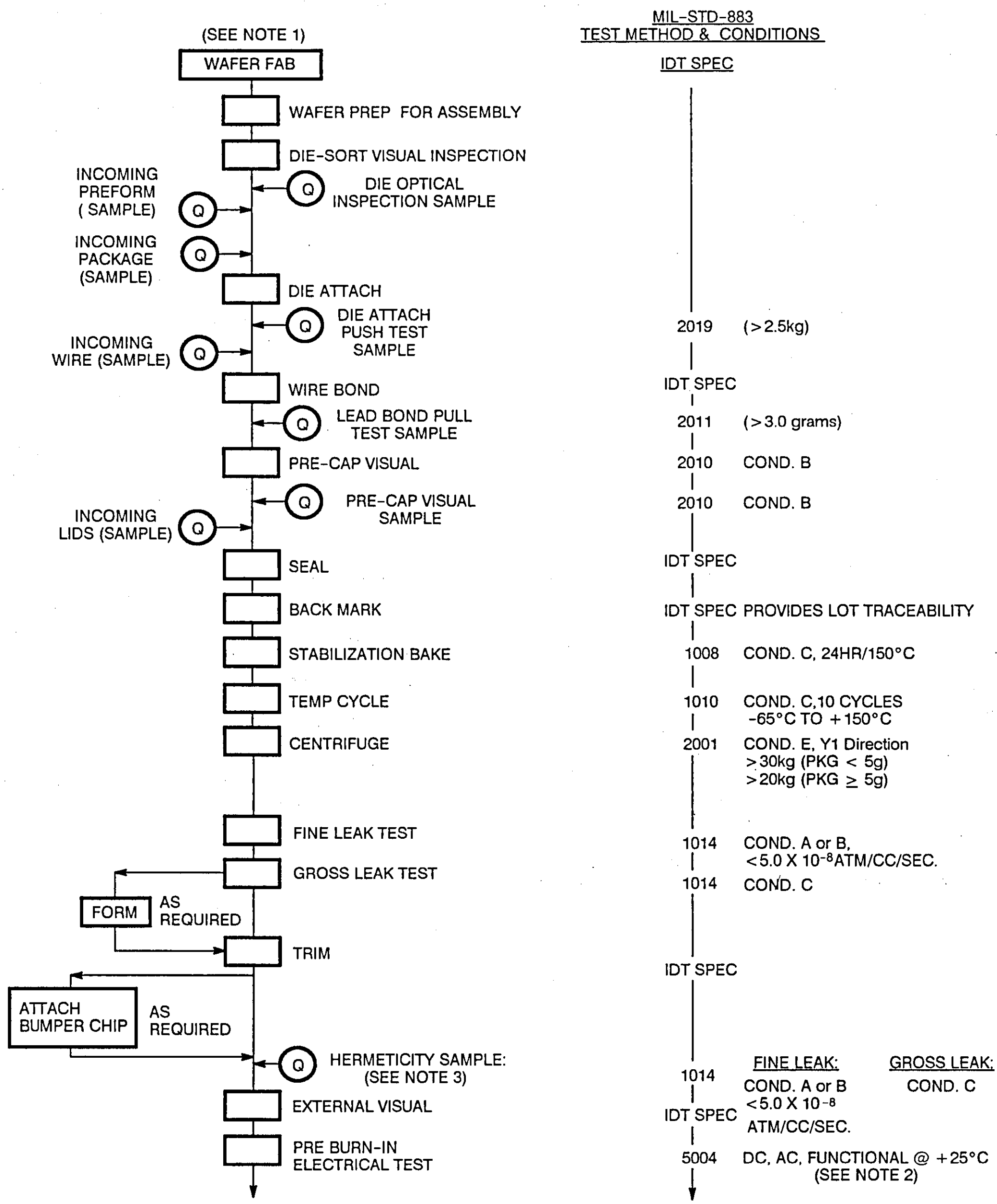
   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.
2. **Die-Sort Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict IDT defined internal criteria.
3. **Die Shear Monitor:** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.
4. **Wire Bond Monitor:** Products samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.
5. **Pre-Cap Visual:** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.
6. **Environmental Conditioning:** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical stress tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.
7. **Hermetic Testing:** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.
8. **Pre-Burn-In Electrical Test:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.
9. **Burn-In:** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D. Except for the time, Commercial Grade product is burned-in to the same conditions as Military Grade devices.
10. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the -55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.
11. **Mark:** All product is marked with product type and lot code indentifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliant code letter.
12. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

3

NOTE:

1. For quality requirements beyond Class B levels such as SEM analysis, X-Ray inspection, Particle Impact Noise Reduction (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

Monolithic Hermetic Package Processing Flow



SEE FINAL PROCESSING FLOW ON PAGE 3-3 FOR REMAINDER OF OPERATIONS AND NOTES

Monolithic Hermetic Package Final Processing Flow

Operation	MIL-STD-883 Test Method	Military Compliant	Commercial	
			Military Temp. Range	Commercial Temp. Range
Burn-In	1015/D at +125 °C Min. or Equivalent	100% 160 Hours	100% 16 Hours	100% 16 Hours
Post Burn-in Electrical: Static (DC), Functional and Switching (AC)(2)	IDT Spec.	100% +25, -55 & +125°C	100% +125°C	100% +70°C
Percent Defective Allowed (PDA)(4)	5004 or IDT Spec.	5%	10%	10%
Group A Electrical: Static (DC), Functional and Switching (AC)(2)	5005 & IDT Spec.	Sample -55 & +125°C	Sample +125°C	Sample +70°C
Mark/Lead Straighten	IDT Spec.	100%	100%	100%
+25°C Electrical(2)	IDT Spec.	100%(5)	100%	100%
Final Visual/Pack	IDT Spec.	100%	100%	100%
Quality Conformance Inspection	5005 (Group B, C, D)	Yes	–	–
Quality Shipping Inspection (Visual/Plant Clearance)	IDT Spec.	Sample	Sample	Sample

NOTES:

1. All screens are 100% unless otherwise noted.
2. All electrical test programs are per the applicable IDT test specification.
3. This hermeticity sample is performed after all lead finish operations.
4. If a lot fails the 5% PDA but is ≤10%, the lot may be resubmitted to burn-in one time only to the same time and temperature conditions as first submission. The subsequent post burn-in electrical test at +25°C will be performed to a PDA of 3%.
5. IDT performs a 100% electrical test at +25°C with a 2% PDA limit at this point to satisfy group A requirements, and considers this to be equivalent to the group A requirement of an LTPD of 2, with an accept number of 0. If a lot fails the 2% PDA limit, it may be rescreened one time only to a tightened PDA limit of 1.5%.
6. Q Quality sample inspection

SUMMARY

MONOLITHIC PLASTIC PACKAGE PROCESSING FLOW

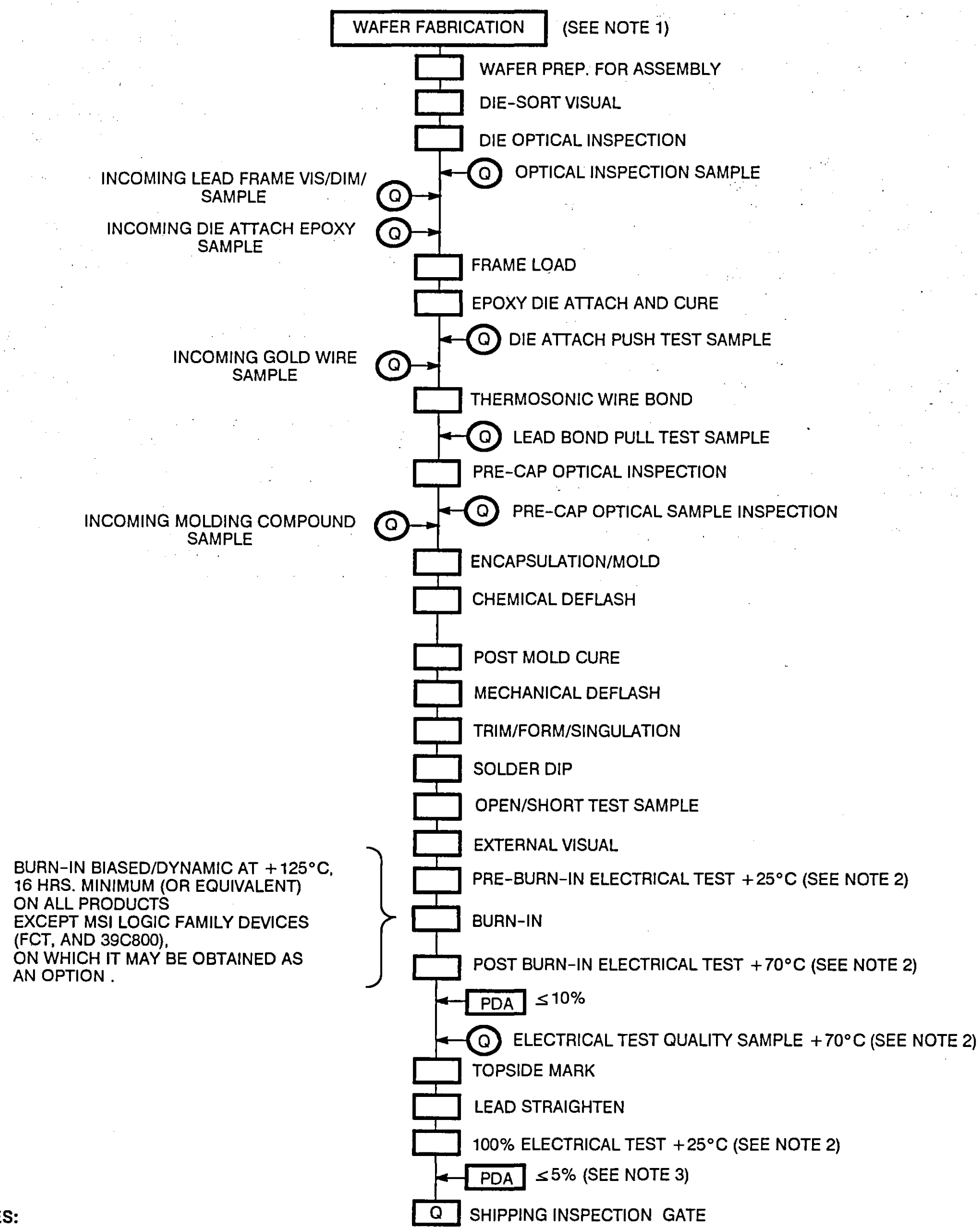
Refer to the Monolithic Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Topside silicon nitride passivation is applied to all wafers for better moisture barrier characteristics.

   Wafers from each wafer fabrication area are subjected to scanning electron microscope analysis on a periodic basis.
2. **Die-Sort Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict internal criteria.
3. **Die Push Test:** To ensure die attach integrity, product samples are routinely subjected to die push tests.
4. **Wire Bond Monitor:** Product samples are routinely subjected to wire bond pull tests to ensure the integrity of the lead bond process.
5. **Pre-cap Visual:** Before the package is molded, 100% of the product is visually inspected to criteria patterned after MIL-STD-883, Method 2010, Condition B.
6. **Post Mold Cure:** Plastic encapsulated devices are baked to insure an optimum plastic seal so as to enhance moisture barrier characteristics.
7. **Pre-Burn-In Electrical:** Each product is 100% electrically tested at an ambient temperature of $+25°C$ to IDT data sheet or the customer specification.
8. **Burn-In:** Except for MSI Logic family devices where it may be obtained as an option, all Commercial Grade plastic package products are burned-in 16 hours at $+125°C$ (or equivalent), utilizing the same burn-in circuit conditions as the Military Grade product.
9. **Post-Burn-In Electrical:** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at the maximum temperature extreme. The minimum temperature extreme is tested periodically on an audit basis.
10. **Mark:** All product is marked with product type and lot code identifiers.
11. **Quality Conformance Inspection:** Samples of the plastic product which have been processed to 100% screening requirements are subjected to the Periodic Quality Conformance Inspection Program. Where indicated the test methods are patterned after MIL-STD-883 criteria.

Monolithic Plastic Package Processing Flow



NOTES:

1) All screens are 100% unless otherwise noted.
2) All electrical test programs are per the applicable IDT test specification.
3) IDT performs a 100% electrical test at +25°C with a 5% PDA limit at this point.
4) Q = Quality sample inspection

SUMMARY

MODULE ASSEMBLY HERMETIC PACKAGE PROCESSING FLOW(1)

Refer to the Module Assembly Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

Components

1. ***Military Grade Class B monolithic microcircuit products*** utilized in Module Assembly products are manufactured and screened in compliance with the applicable demanding criteria of MIL-STD-883. (See the Monolithic Hermetic Package Processing Flow diagram.)
2. ***Commercial Grade monolithic microcircuit products*** utilized in Module Assembly products differ from Military Grade only in the burn-in time and electrical test temperatures.
3. ***Passive components*** such as chip capacitors are obtained from qualified vendors to the applicable military and IDT specifications.

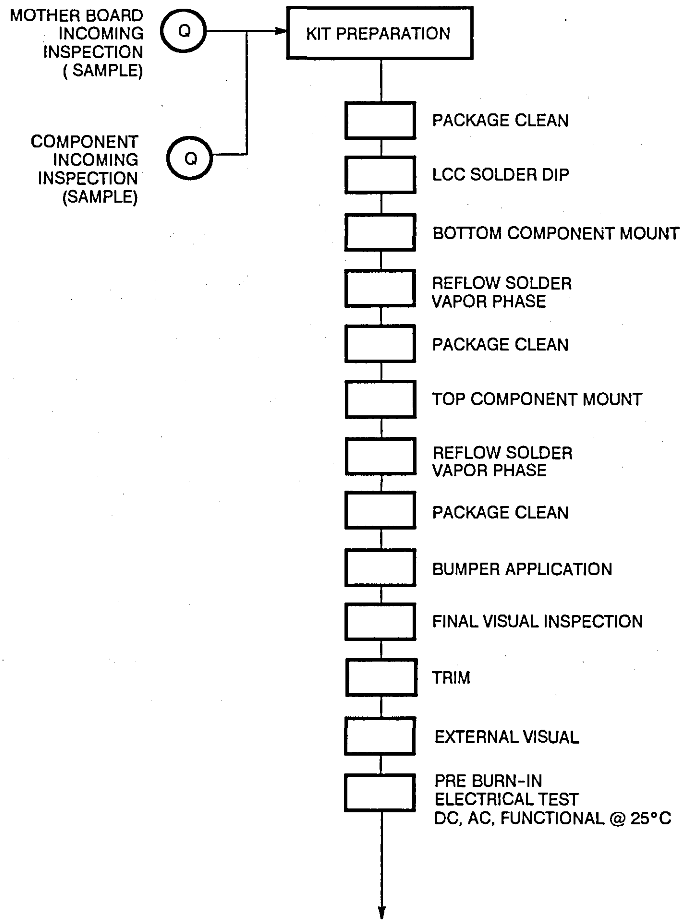
Modules

1. **Module Assembly:** The active and passive components and substrates used in the assembly of modules must pass incoming inspection requirements. The components are then mounted onto the substrate using the reflow solder vapor phase technique.
2. **Pre-Burn-In Electrical Test:** Each module is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.
3. **Burn-In:** 100% of Military Grade module product is burned-in under the dynamic electrical conditions of Method 1015, Condition D, for 44 ± 4 hours at a T_A of +125°C. Commercial Grade module products do not require burn-in.
4. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the -55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.
5. **PDA Calculation:** A PDA (Percent Defective Allowed) of 5% is imposed on all Military module products for the 25°C parameters after completion of burn-in.
6. **Mark:** All product is marked with product type and lot code identifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliancy code letter.
7. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to 100% screening tests are routinely subjected to the Quality Conformance Inspection requirements of MIL-STD-883 applicable to Module Assembly products.
8. **External Visual:** Product is 100% visually inspected prior to shipment to the applicable criteria for modules as required by MIL-STD-883.

NOTE:

1. For quality requirements beyond Class B levels, such as SEM analysis, X-ray inspection, Particle Impact Noise Detection (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

Module Assembly Hermetic Package Processing Flow



SEE FINAL PROCESSING FLOW ON PAGE 3-8 FOR REMAINDER OF OPERATIONS AND NOTES

3

Module Assembly Hermetic Package Final Processing Flow

Operation	MIL-STD-883 Test Method	Military Compliant	Commercial	
			Military Temp. Range	Commercial Temp. Range
Burn-In	1015/D at +125°C Min. or Equivalent	100% 44 ± 4 Hours	–	–
Post Burn-in Electrical: Static (DC), Functional and Switching (AC)(2)	IDT Spec.	100% +25, -55 & +125°C	100% +125°C	100% +70°C
Percent Defective Allowed (PDA)(3)	5004	5%	–	–
Group A Electrical: Static (DC), Functional and Switching (AC)(2)	IDT Spec.	Sample -55 & +125°C	Sample +125°C	Sample +70°C
Mark/Lead Straighten	IDT Spec.	100%	100%	100%
+25°C Electrical(2)	IDT Spec.	100%(4)	100%	100%
Final Visual/Pack	IDT Spec.	100%	100%	100%
Quality Conformance Inspection	(Note 5)	Yes	–	–
Quality Shipping Inspection (Visual/Plant Clearance)	IDT Spec.	Sample	Sample	Sample

NOTES:

1. All screens are 100% unless otherwise noted.
2. All electrical test programs are per the applicable IDT test specification.
3. If a lot fails the 5% PDA but is ≤10%, the lot may be resubmitted to burn-in one time only to the same time and temperature conditions as first submission. The subsequent post burn-in electrical test at +25°C will be performed to a PDA of 3%.
4. IDT performs a 100% electrical test at +25°C with a 2% PDA limit at this point to satisfy group A requirements, and considers this to be equivalent to the group A requirement of an LTPD of 2, with an accept number of 0. If a lot fails the 2% PDA limit, it may be rescreened one time only to a tightened PDA limit of 1.5%.
5. IDT presently utilizes QCI tests patterned after method 5005. A new method for module products is under development by the military.
6. Q Quality sample inspection

RADIATION TOLERANT/ENHANCED/HARDENED PRODUCTS FOR RADIATION ENVIRONMENTS

INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The lower power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

Total Dose Accumulation refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS(SI) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

Burst Radiation or Dose Rate refers to the amount of radiation, usually photons or electrons, experienced by devices in the system due to a pulse event, and is measured in RADS(SI) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

Single Event Upset (SEU) is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuits. As the ion passes through the silicon, charge is created either through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

Neutron Irradiation will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

RADIATION CATEGORY	PRIMARY PARTICLE	SOURCE	EFFECT
Total Dose	Gamma	Space or Nuclear Event	Permanent
DoseRate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-Up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

Figure 1.

DEVICE ENHANCEMENTS

Of the four radiation environments above, IDT has taken considerable data on the first two, Total Dose Accumulation and Dose Rate. IDT has developed a process that significantly improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as error checking and correction (ECC) circuitry, since the occurrance of SEUs is not particularly dependent on process technology. Through IDT's customer contracts, SEU data has been gathered on some devices. Little is yet known about the effects of neutron-induced damage. For more information on SEU testing, contact IDT's Radiation Hardened Product Group.

Figure 2 itemizes some of the enhancements that IDT has made to its standard process in creating a radiation enhanced process. The use of epi substrate material provides a lower substrate resistance environment to create latch-up free CMOS structures. Field and gate oxides are less susceptible to radiation damage (i.e., "hardened") by modifying the process architecture to allow lower-temperature processing. Device implants and Vts have been adjusted allowing more Vt margin.

	STANDARD	ENHANCED
Substrate Material	n-	n- epi/n+
Field Oxide	std	hardened
Gate Oxide	std	hardened
Vt, n	0.75 volts	1.0 volts
Vt, p	-0.75 volts	-0.6 volts
Process Temperature Post Gate Oxide	1000°C	900°C

Figure 2.

RADIATION HARDNESS CATEGORIES

With the process enhancements described above, IDT offers integrated circuits with varying grades of radiation tolerance, or radiation "hardness," shown in Figure 3. The level of radiation hardness is defined by IDT as follows:

- *Radiation Enhanced* integrated circuits are defined as being able to withstand a total dose of 30K RADs(Si) [memory devices, 100K RADs(Si) capability for non-memory products] without failure.
- *Radiation Tolerant* integrated circuits are defined as being able to withstand a total dose of 10K RADs(Si) without failure. Standard IDT products can be expected to exhibit radiation tolerance of (withstand) a total dose of 4K-6K RADs(Si) without failure.

TYPE OF RADIATION	UNITS	PRODUCT TYPES: MEMORY	PRODUCT TYPES: MEMORY+ LOGIC	PRODUCT TYPES: LOGIC	IDT PROCESS
Total Dose	K RADs(Si) Rate: 10K RADs(Si)/min.	≤6K >10K >30K	≤6K >10K >30K	≤15K >10K >30K	Standard Tolerant Enhanced
Dose Rate (Latchup)	RADs(Si)/sec. pulse width = 50ns	1.0E8 1.0E8 >2.4E10	 >2.4E10	 >2.4E10	Standard Tolerant Enhanced
		--------------No Latchup--------------			

Figure 3.

Integrated Device Technology now offers devices processed to each of these radiation tolerant levels across the full product line. The appropriate part number corresponding to these radiation hardness categories is defined in Figure 4.

IDT XXXXX (DEVICE TYPE) A (POWER) 999 (SPEED) A (PACKAGE) A (PROCESS) AA (RAD HARD)

MIL-STD-883, CLASS B

Standard — Blank
Radiation Tolerant — RT
Radiation Enhanced — RE

Figure 4.

Please contact your local IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

CONCLUSION

There has been widespread interest within the military and space community in IDT's CMOS product line for its radiation hardness levels, as well as its high-performance and low power dissipation. To serve this growing need for CMOS circuits that must operate in a radiation environment, IDT has created a separate group within the company to concentrate on supplying products for these applications. Continuing research and development of process and products, including the use of in-house radiation testing capability, will allow Integrated Device Technology to offer continuously increasing levels of radiation-tolerant solutions.

Product Selector and Cross Reference Guides

Technology/Capabilities

Quality and Reliability

Static RAMs

4

Dual-Port RAMs

FIFO Memories

Digital Signal Processing (DSP)

Bit-Slice Microprocessor Devices (MICROSLICE™) and EDC

Reduced Instruction Set Computer (RISC) Processors

Logic Devices

Data Conversion

E²PROMS-Electrically Erasable Programmable Read Only Memories

Subsystems Modules

Application and Technical Notes

Package Diagram Outlines

SRAM INTRODUCTION

Integrated Device Technology is the major U.S. supplier of high-performance Static Random Access Memories. Leading edge CEMOS and BiCEMOS process technology, coupled with advanced design techniques, enables IDT to supply our military and commercial customers with production volumes of the industry's fastest SRAMs. IDT is committed to providing our customers with early access to innovative circuit designs, taking full advantage of this advanced process technology. This results in the broadest range of SRAM speeds, densities and organizations available in today's market.

Integrated with performance leadership at IDT is a commitment to provide our customers with a wide selection of SRAM organizations. 16K, 64K and 256K devices are offered in x1, x4 and x8 organizations. This year, these offerings will be expanded to include x16 and x9 devices, as well as 1 Megabit densities. To further match IDT SRAMs with system architectural needs, several devices are available with separate inputs and outputs, additional control features and functions.

Leadership products offered by IDT include BiCEMOS devices, incorporating both TTL and ECL compatible inputs and outputs, as well as CEMOS devices offering true CMOS I/O levels. These products confirm our charter to offer technology to system designers in its most friendly and usable form.

Our intensive and innovative process technology development effort has resulted in truly outstanding advances in device performance. Over the past 7 years, as an example, our 2K x 8 SRAM has been redesigned in successively advanced CEMOS processes, progressing from 2µ geometries to less than 1µ. This resulted in access time being improved by about a factor of 10, to the currently available 15 nanosecond devices. This continuing dedication to advancement will result in 1 Megabit CEMOS devices and 256K bit BiCEMOS devices this year.

IDT's advanced SRAMs are available in a wide variety of packages, ranging from commercial surface mount through DIPs and LCCs to military flatpacks. This continually expanding package offering is in direct response to critical second-level interconnect issues confronting today's system designer. Our commitment to technology extends to advanced, cost-effective packaging techniques.

Both commercial and military versions of all IDT SRAMs are available. Our military devices are manufactured and processed strictly in conformance with all the administrative, processing and performance requirements of MIL-STD-883. Having anticipated increased military radiation resistance requirements, all devices are also offered with special radiation resistant processing and guarantees. As a leading supplier of military SRAMs, IDT provides performance and quality levels second to none. Our commercial products, in fact, share most processing steps with military devices.

IDT's continuing commitment to cutting edge technology and performance will assure the availability of SRAMs most compatible with the exacting needs of today's systems. Look to IDT SRAMs for performance, technology, quality and imaginative solutions to memory system problems.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (16K x 1-BIT)

IDT6167SA
IDT6167LA

FEATURES:

- High-speed (equal access and cycle time)
  - Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - Commercial: 12/15/20/25/35ns (max.)
- Low power consumption
  - IDT6167SA
    Active: 200mW (typ.)
    Standby:100μW (typ.)
  - IDT6167LA
    Active: 150mW (typ.)
    Standby:10μW (typ.)
- Battery backup operation—2V data retention voltage (IDT6167LA only)
- Available in 20-pin CERDIP and plastic DIP, 20-pin Flatpack or CERPACK, 20-pin SOIC and 20-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Separate data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-84132 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT6167 is a 16,384-bit high-speed static RAM organized as 16K x 1. The part is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

Access times as fast as 12ns are available with maximum power consumption of only 660mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 10μW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off a 2V battery.

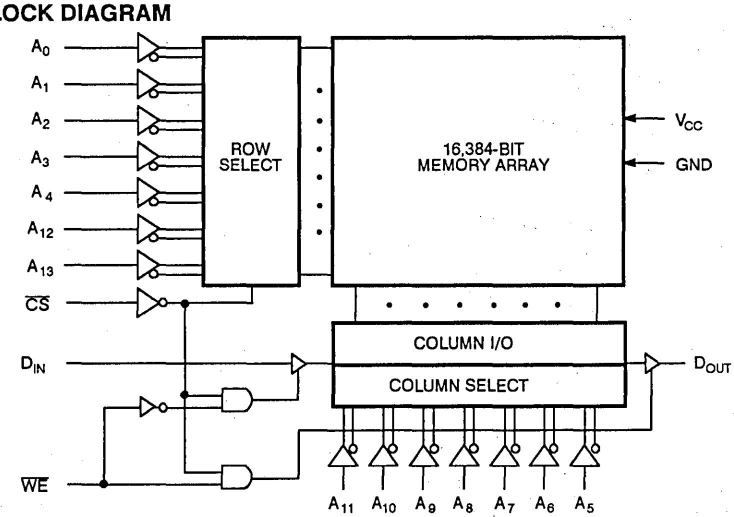
All inputs and the output of the IDT6167 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT6167 is packaged in a space-saving 20-pin, 300 mil Plastic DIP or CERDIP, plastic 20-pin SOIC, 20-pin flatpack or CERPACK and 20-pin leadless chip carrier, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

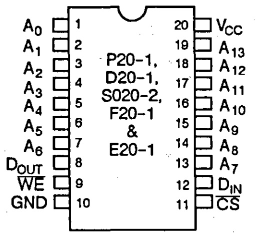
4

FUNCTIONAL BLOCK DIAGRAM

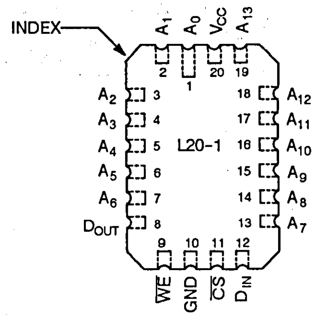


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

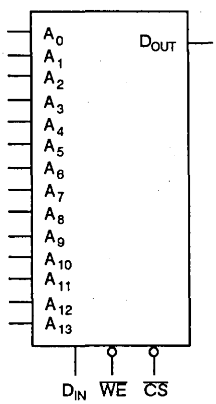


DIP/SOIC/FLATPACK/CERPACK
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0–A_{13}	Address Inputs	D_{IN}	$DATA_{IN}$
$\overline{CS}$	Chip Select	D_{OUT}	$DATA_{OUT}$
$\overline{WE}$	Write Enable	GND	Ground
V_{CC}	Power		

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT6167SA MIN.	IDT6167SA TYP.(1)	IDT6167SA MAX.	IDT6167LA MIN.	IDT6167LA TYP.(1)	IDT6167LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1) V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	6167SA12(4) 6167LA12(4) COM'L.	MIL.	6167SA15 6167LA15 COM'L.	MIL.	6167SA20/25 6167LA20/25 COM'L.	MIL.	6167SA35 6167LA35 COM'L.	MIL.	6167SA45(5) 6167LA45(5) COM'L.	MIL.	6167SA55(5) 6167LA55(5) COM'L.	MIL.	6167SA70(5) 6167LA70(5) COM'L.	MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(3)	SA	90	–	90	90	90	90	90	90	–	90	–	90	–	90	mA
		LA	55	–	55	60	55	60	55	60	–	60	–	60	–	60	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL} Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	120	–	100	120	100	110/100	100	100	–	100	–	100	–	100	mA
		LA	100	–	85	90	80/70	85/75	65	70	–	65	–	60	–	60	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}(3)	SA	45	–	45	50	35	35	35	35	–	35	–	35	–	35	mA
		LA	35	–	35	35	30/25	30/25	20	20	–	20	–	20	–	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC} f = 0(3)	SA	10	–	5	10	5	10	5	10	–	10	–	10	–	10	mA
		LA	0.9	–	0.9	2	0.05	2/0.9	0.05	0.9	–	0.9	–	0.9	–	0.9	

NOTES:
1. All values are maximum guaranteed values.
2. Also available: 85ns and 100ns Military devices
3. f = f_{MAX} (All inputs cycling at f = $1/t_{RC}$). f = 0 means no address control lines change.
4. 0°C to +70°C temperature range only.
5. -55°C to +125°C temperature range only.

4

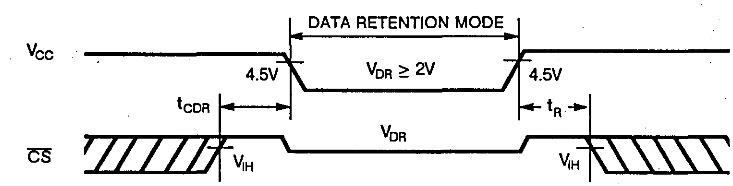
DATA RETENTION CHARACTERISTICS

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.[1] V_{CC}@ 2.0V	TYP.[1] V_{CC}@ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	0.5	1.0	200	300	μA
			COM'L.	–	0.5	1.0	20	30	μA
t_{CDR}	Chip Deselect to Data Retention Time			0	–		–		ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–		–		ns
$\|I_{LI}\|$[3]	Input Leakage Current			–	–		2		μA

NOTES:
1. T_A= +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

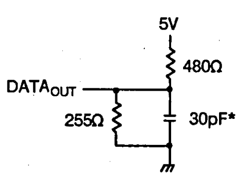


Figure 1. Output Load

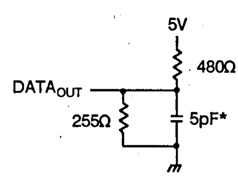


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

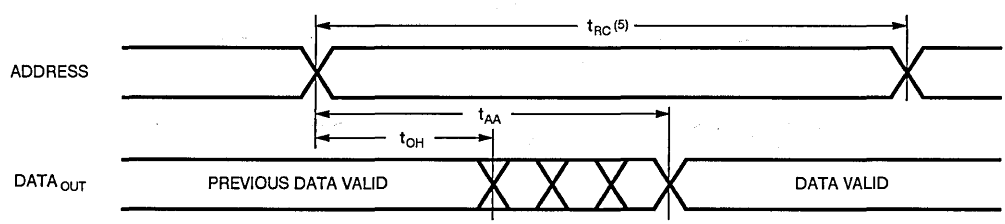
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ±10%, All Temperature Ranges)

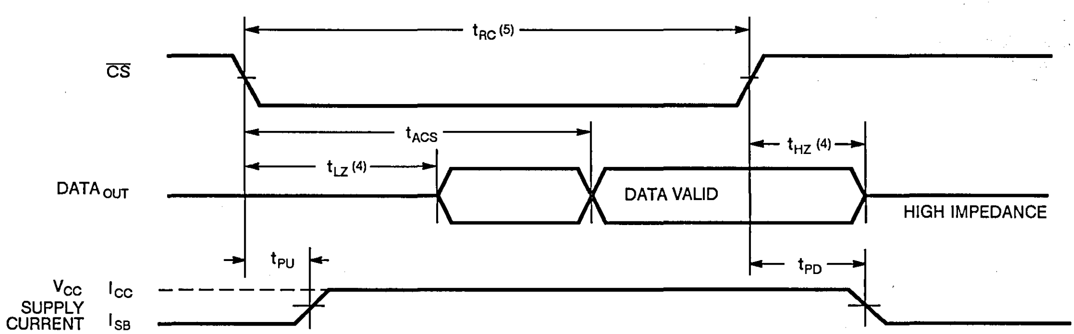
SYMBOL	PARAMETER	6167SA12[1] 6167LA12[1] MIN.	MAX.	6167SA15 6167LA15 MIN.	MAX.	6167SA20/25 6167LA20/25 MIN.	MAX.	6167SA35/45[2] 6167LA35/45[2] MIN.	MAX.	6167SA55[2]/70[2] 6167LA55[2]/70[2] MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	12	–	15	–	20/25	–	35/45	–	55/70	–	ns
t_{AA}	Address Access Time	–	12	–	15	–	20/25	–	35/45	–	55/70	ns
t_{ACS}	Chip Select Access Time	–	12	–	15	–	20/25	–	35/45	–	55/70	ns
t_{OH}	Output Hold from Address Change	3	–	3	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Deselect to Output in Low Z[3]	3	–	3	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Select to Output in High Z[3]	–	8	–	10	–	10	–	15/30	–	40	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	12	–	15	–	20/25	–	35	–	55/70	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 85 and 100ns Military devices.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1 [1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 3]



NOTES:
1. $\overline{WE}$ is High for READ Cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

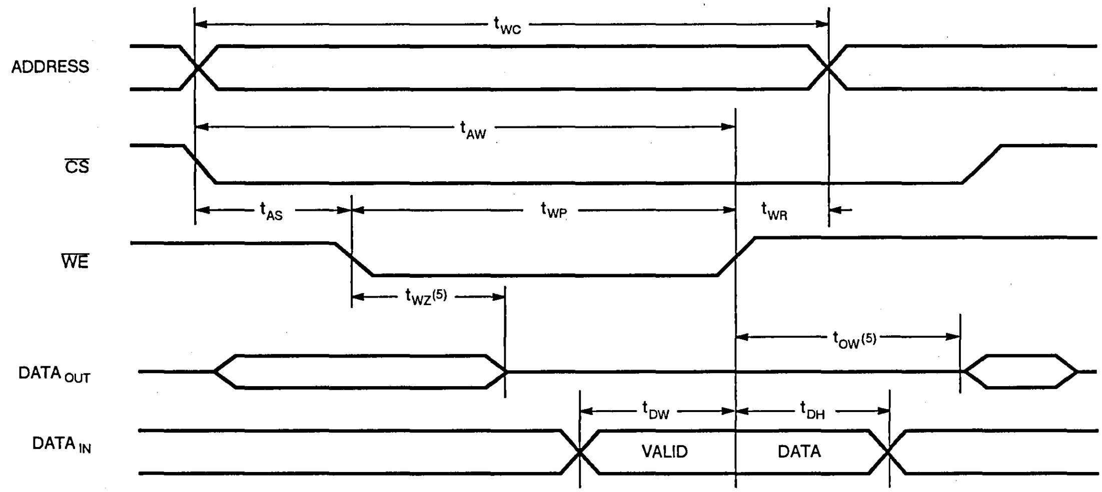
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6167SA12[1] 6167LA12[1]		6167SA15 6167LA15		6167SA20/25 6167LA20/25		6167SA35/45[2] 6167LA35/45[2]		6167SA55[2]/70[2] 6167LA55[2]/70[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE												
t_{WC}	Write Cycle Time	12	–	15	–	20/20	–	30/45	–	55/70	–	ns
t_{CW}	Chip Select to End of Write	12	–	15	–	15/20	–	30/40	–	45/55	–	ns
t_{AW}	Address Valid to End of Write	12	–	15	–	15/20	–	30/40	–	45/55	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	12	–	13	–	15/20	–	30	–	35/40	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	10	–	12	–	13/15	–	20/25	–	25/30	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enable to Output in High Z[3]	–	8	–	10	–	10	–	15/30	–	40	ns
t_{OW}	Output Active from End of Write[3]	0	–	0	–	0	–	0	–	0	–	ns

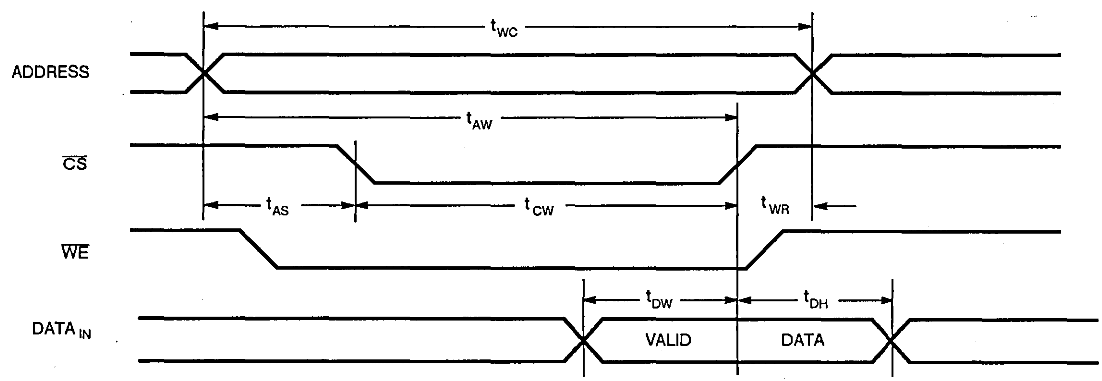
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 85 and 100ns Military devices.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 4)

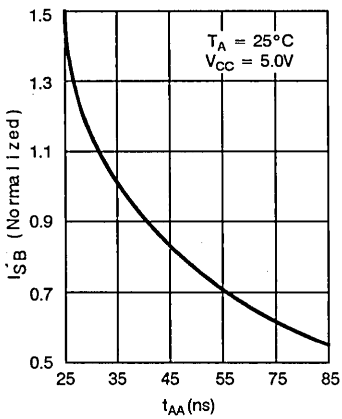


NOTES:

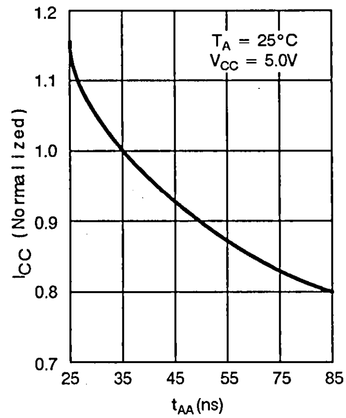
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

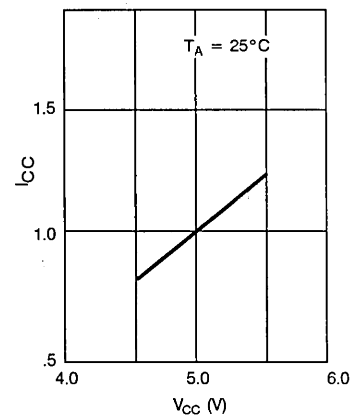
I_{SB} vs. t_{AA} (35ns Device)



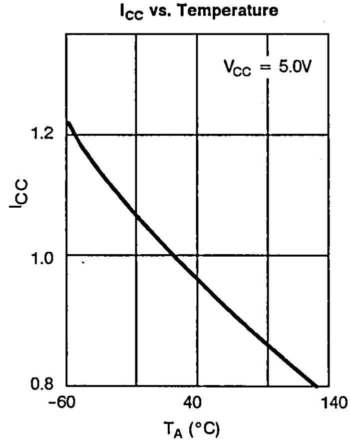
I_{CC} vs. t_{AA} (35ns Device)



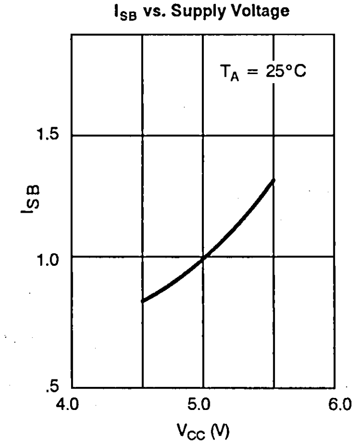
I_{CC} vs. Supply Voltage



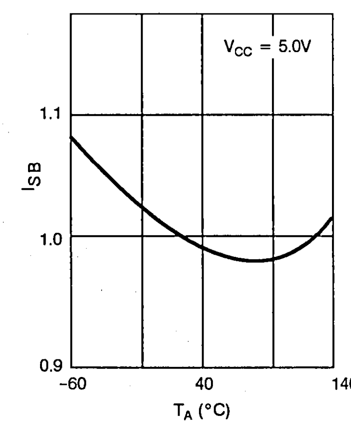
I_{CC} vs. Temperature



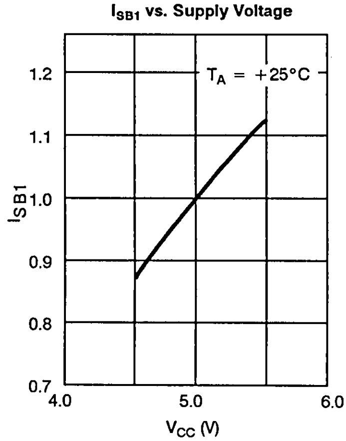
I_{SB} vs. Supply Voltage



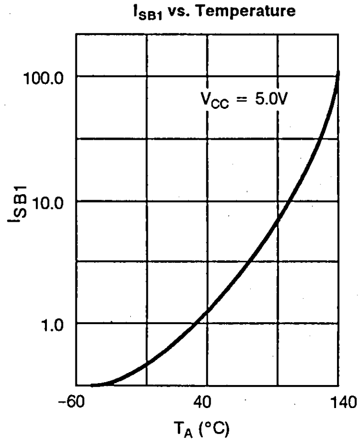
I_{SB} vs. Temperature



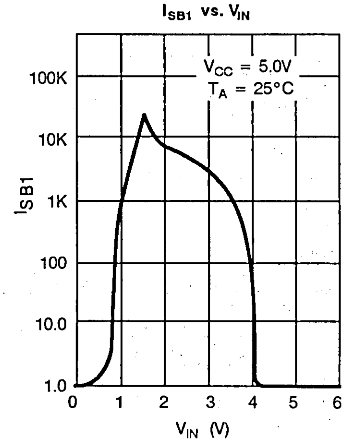
I_{SB1} vs. Supply Voltage



I_{SB1} vs. Temperature

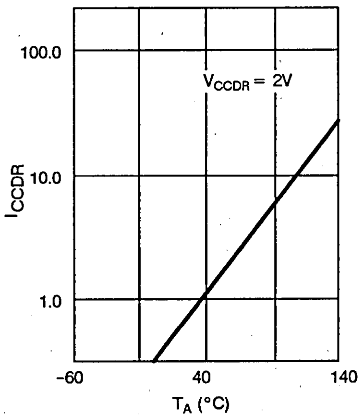


I_{SB1} vs. V_{IN}

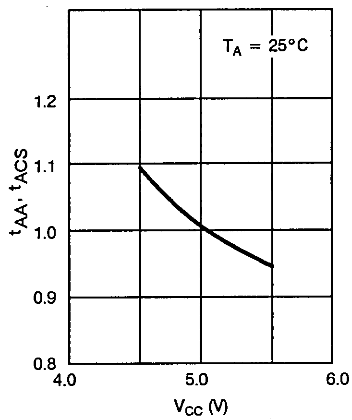


NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

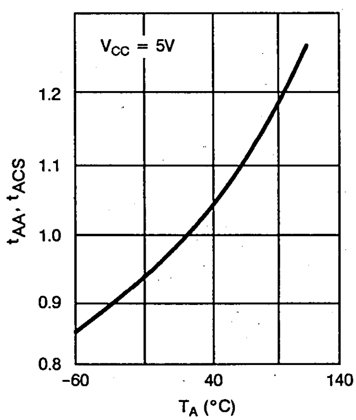
I_{CCDR} vs. Temperature



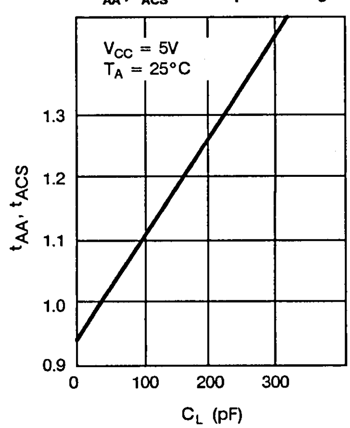
t_{AA}, t_{ACS} vs. Supply Voltage



t_{AA}, t_{ACS} vs. Temperature



t_{AA}, t_{ACS} vs. Output Loading



4

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is determined by device characterization and is not production tested.

ORDERING INFORMATION

IDT	XXXX	A	999	A	A
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

P	Plastic DIP
D	CERDIP
L	Leadless Chip Carrier
SO	Small Outline IC
E	CERPACK
F	Flatpack

Speed (Speed in Nanoseconds)

12	Commercial Only
15	
20	
25	
35	
45	Military Only
55	Military Only
70	Military Only
85	Military Only
100	Military Only

Power

SA	Standard Power
LA	Low Power

Device Type

6167	16K (16K x 1-Bit) CMOS Static RAM

Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (4K x 4-BIT)

IDT6168SA
IDT6168LA

FEATURES:

- High-speed (equal access and cycle time)
  - Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - Commercial: 15/20/25/35ns (max.)
- Low power consumption
  - IDT6168SA
    Active: 225mW (typ.)
    Standby: 100μW (typ.)
  - IDT6168LA
    Active: 225mW (typ.)
    Standby: 10μW (typ.)
- Battery backup operation—2V data retention voltage (IDT6168LA only)
- Available in high-density 20-pin CERDIP and plastic DIP, 20-pin SOIC, 20-pin Flatpack and CERPACK and 20-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Bidirectional data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state outputs
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86705 is listed on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

Access times as fast as 15ns are available with maximum power consumption of only 550mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 10μW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off a 2V battery.

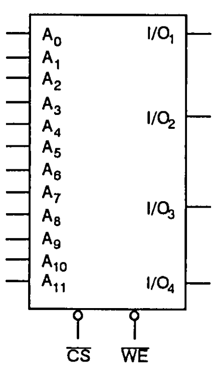
All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT6168 is packaged in either a space saving 20-pin, 300 mil CERDIP or plastic DIP, 20-pin flatpack or CERPACK, 20-pin SOIC, or 20-pin leadless chip carrier, providing high board-level packing densities.

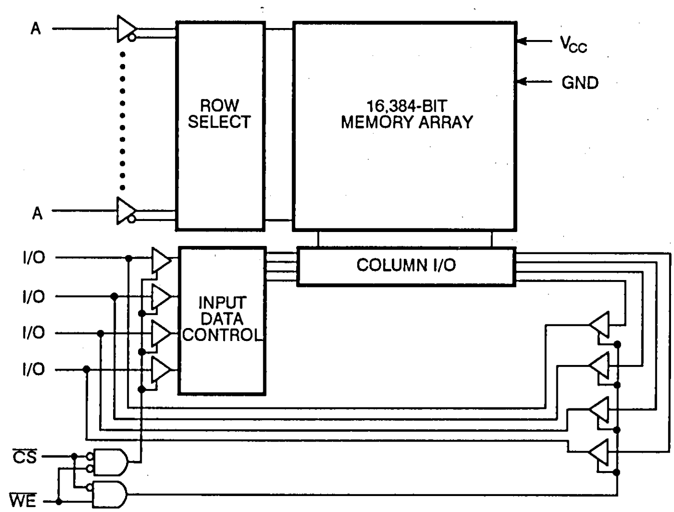
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

4

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM

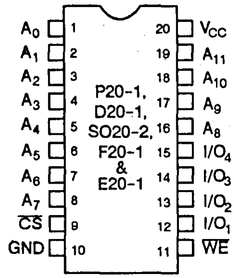


CEMOS is a trademark of Integrated Device Technology, Inc.

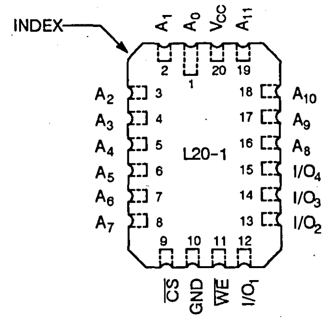
MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-1008/-

PIN CONFIGURATIONS



DIP/SOIC/FLATPACK/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN NAMES

A_0–A_{11}	Address Inputs	I/O_1 – I/O_4	Data Input/Output
$\overline{CS}$	Chip Select	V_{CC}	Power
$\overline{WE}$	Write Enable	GND	Ground

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT6168SA MIN.	IDT6168SA TYP.(1)	IDT6168SA MAX.	IDT6168LA MIN.	IDT6168LA TYP.(1)	IDT6168LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	2	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	2	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	6168SA15 6168LA15 COM'L.	MIL.	6168SA20 6168LA20 COM'L.	MIL.	6168SA25 6168LA25 COM'L.	MIL.	6168SA35/45(4) 6168LA35/45(4) COM'L.	MIL.	6168SA55 6168LA55 COM'L.	MIL.	6168SA70(2) 6168LA70(2) COM'L.	MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(3)	SA	90	100	90	100	90	100	90	100	–	100	–	100	mA
		LA	70	80	70	80	70	80	70	80	–	80	–	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX} (3)	SA	120	130	120	120	110	120	100	110	–	110	–	110	mA
		LA	110	120	100	110	90	100	80	90/80	–	80	–	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(3)	SA	45	50	45	45	35	45	30	35	–	35	–	35	mA
		LA	35	40	30	35	25	30	20	25	–	20	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0 (3)	SA	20	20	20	20	2	10	2	10	–	10	–	10	mA
		LA	0.2	5	2	5	0.05	0.3	0.05	0.3	–	0.3	–	0.3	

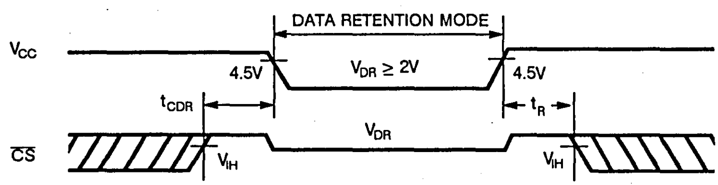
NOTES:
1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. f = f_{MAX} (All inputs except Chip Select cycling at f = $1/t_{RC}$). f = 0 means no address or control lines change.
4. -55°C to +125°C temperature range only.

DATA RETENTION CHARACTERISTICS (LA Version Only)

SYMBOL	PARAMETER	TEST CONDITION		IDT6168LA MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Retention Data			2.0	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $\leq$ 0.2V	MIL.	– –	0.5[2] 1.0[3]	100[2] 150[3]	µA
			COM'L.	– –	0.5[2] 1.0[3]	20[2] 30[3]	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time			0	–	–	ns
t_R[5]	Operation Recovery Time			t_{RC}[2]			ns

NOTES:
1. $T_A = +25°C$
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time
5. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

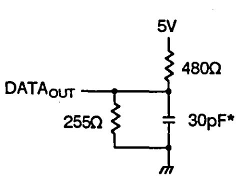


Figure 1. Output Load

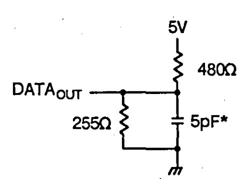


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

* Including scope and jig.

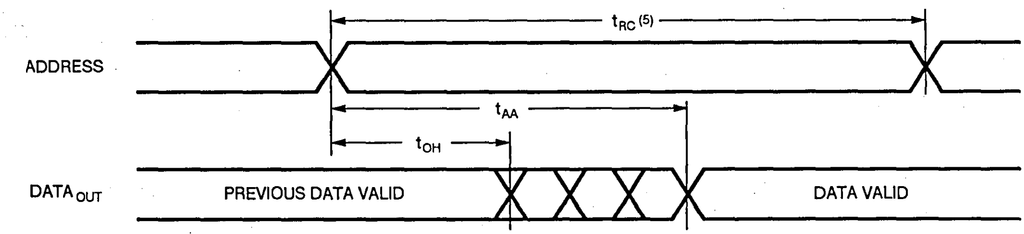
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6168SA15 6168LA15 MIN.	MAX.	6168SA20/25 6168LA20/25 MIN.	MAX.	6168SA35/45[1] 6168LA35/45[1] MIN.	MAX.	6168SA55[1] 6168LA55[1] MIN.	MAX.	6168SA70[1] 6168LA70[1] MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	15	–	20/25	–	35/45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	15	–	20/25	–	35/45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time	–	15	–	20/25	–	35/45	–	55	–	70	ns
t_{OH}	Output Hold from Address Change	3	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Select to Output in Low Z[2]	3	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselect to Output in High Z[2]	–	8	–	10	–	15	–	25	–	30	ns
t_{PU}	Chip Select to Power Up Time[2]	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[2]	–	15	–	20/25	–	35/40	–	50	–	60	ns
t_{RCS}	Read Command Set-up Time	-5	–	-5	–	-5	–	-5	–	-5	–	ns
t_{RCH}	Read Command Hold Time	-5	–	-5	–	-5	–	-5	–	-5	–	ns

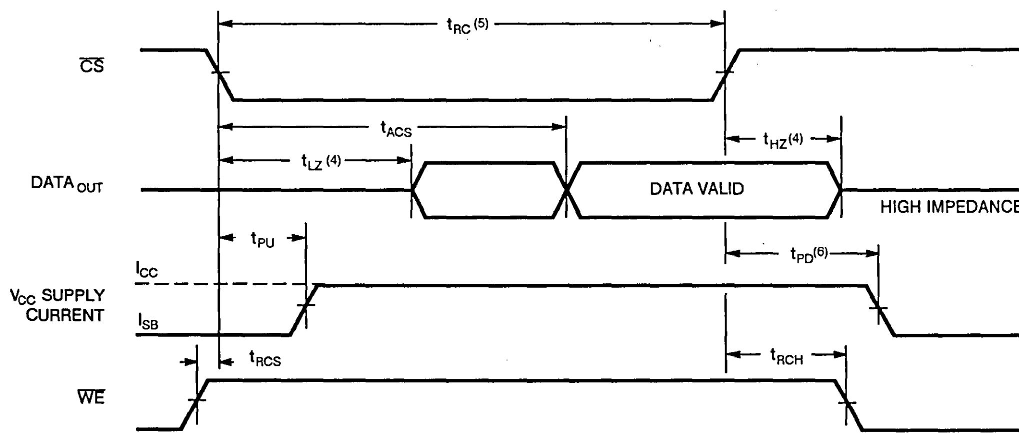
NOTES:
1. -55°C to -125°C temperature range only. Also available 85 and 100ns military devices.
2. This parameter is guaranteed but not tested.

4

TIMING WAVEFORM OF READ CYCLE NO. 1[1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 3]



NOTES:

1. $\overline{WE}$ is High for READ Cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. This parameter is guaranteed and not 100% tested.

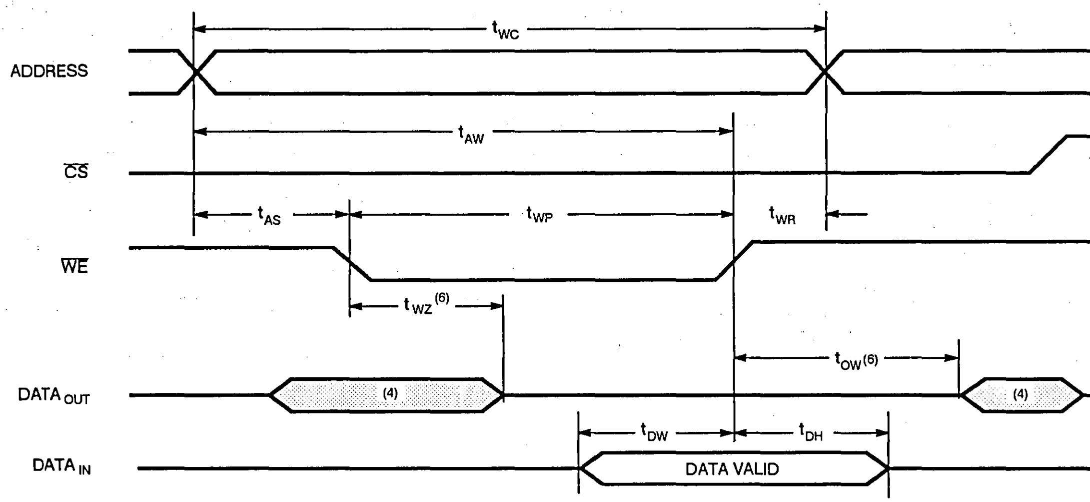
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6168SA15 6168LA15 MIN.	MAX.	6168SA20/25 6168LA20/25 MIN.	MAX.	6168SA35/45[1] 6168LA35/45[1] MIN.	MAX.	6168SA55[1] 6168LA55[1] MIN.	MAX.	6168SA70[1] 6168LA70[1] MIN.	MAX.	UNIT
WRITE CYCLE												
t_{WC}	Write Cycle Time	15	–	20	–	30/40	–	50	–	60	–	ns
t_{CW}	Chip Select to End of Write	15	–	20	–	30/40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	15	–	20	–	30/40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	15	–	20	–	30/40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	9	–	13	–	17/20	–	20	–	25	–	ns
t_{DH}	Data Hold Time	3	–	3	–	3	–	3	–	3	–	ns
t_{WZ}	Write Enable to Output in HighZ[2]	–	6	–	7	–	13/20	–	25	–	30	ns
t_{OW}	Output Active from End of Write[2]	0	–	0	–	0	–	0	–	0	–	ns

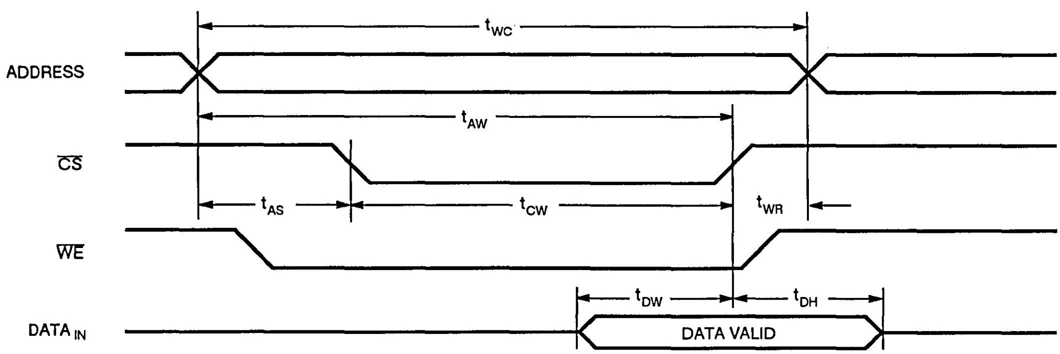
NOTES:
1. –55°C to –125°C temperature range only. Also available 85 and 100ns military devices.
2. This parameter is guaranteed but not tested.

4

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{\text{WE}}$ CONTROLLED TIMING) [1, 2, 3]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{\text{CS}}$ CONTROLLED TIMING) [1, 2, 3, 5]



NOTES:

1. $\overline{\text{WE}}$ or $\overline{\text{CS}}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP} or t_{CW}) of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.
3. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals should not be applied.
5. If the $\overline{\text{CS}}$ low transition occurs simultaneously with or after the $\overline{\text{WE}}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

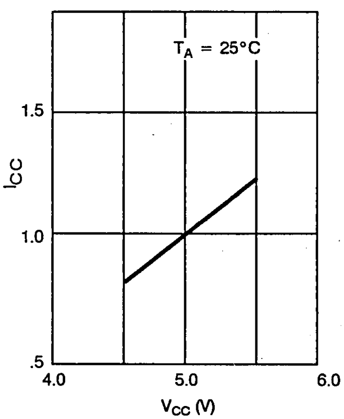
SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

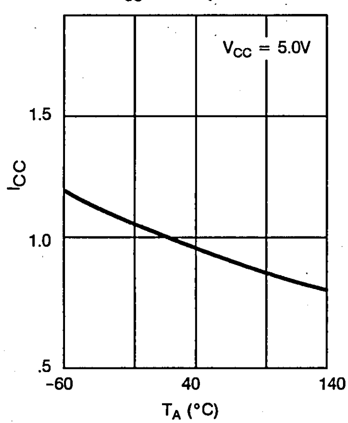
1. This parameter is determined by device characterization, but is not production tested.

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

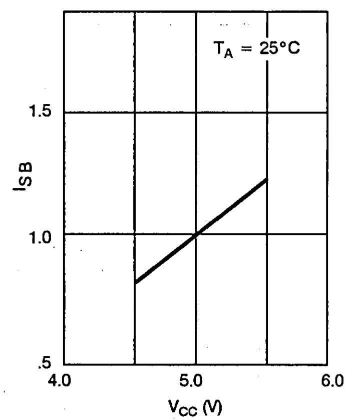
I_{CC} vs. Supply Voltage



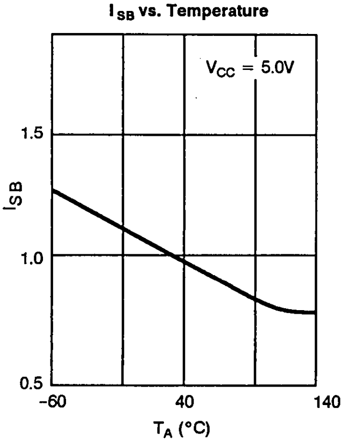
I_{CC} vs. Temperature



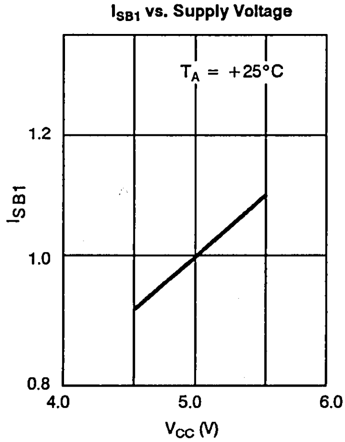
I_{SB} vs. Supply Voltage



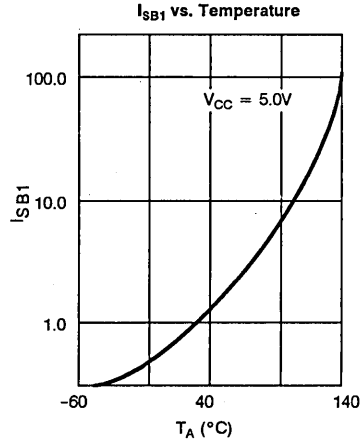
I_{SB} vs. Temperature



I_{SB1} vs. Supply Voltage

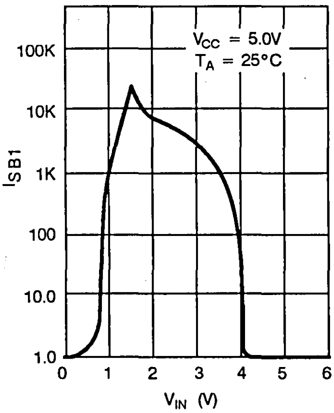


I_{SB1} vs. Temperature

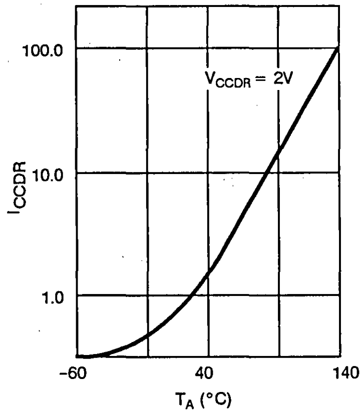


NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

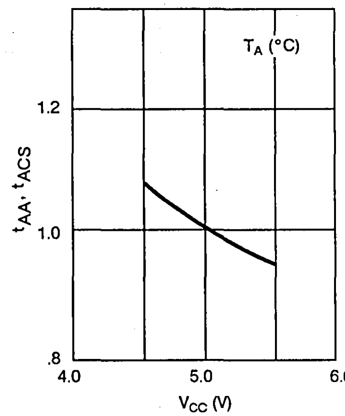
I_{SB1} vs. V_{IN}



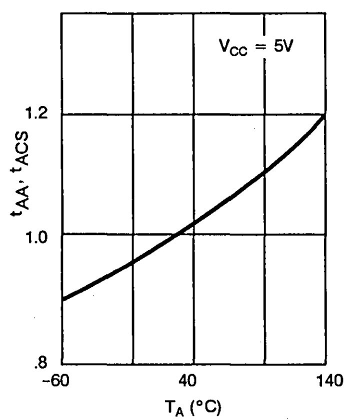
I_{CCDR} vs. Temperature



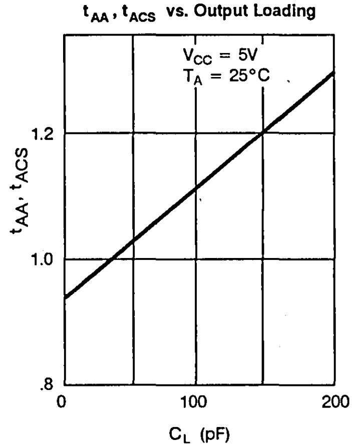
t_{AA}, t_{ACS} vs. Supply Voltage



t_{AA}, t_{ACS} vs. Temperature



t_{AA}, t_{ACS} vs. Output Loading



ORDERING INFORMATION

IDT XXXXX A 999 A A

IDT	XXXXX	A	999	A	A
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

P	Plastic DIP
D	CERDIP
L	Leadless Chip Carrier
SO	Small Outline IC
F	Flatpack
E	CERPACK

Speed (Speed in Nanoseconds)

15	
20	
25	
35	
45	Military Only
55	Military Only
70	Military Only
85	Military Only
100	Military Only

Power

SA	Standard Power
LA	Low Power

Device Type

6168	16K (4K x 4-Bit)

4

Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (4K x 4-BIT)

Separate Data Inputs and Outputs

IDT71681SA/LA
IDT71682SA/LA

FEATURES:

- Separate data inputs and outputs
- IDT71681SA/LA: outputs track inputs during write mode
- IDT71682/SA/LA: high impedance outputs during write mode
- High-speed (equal access and cycle time)
  - Military: 25/35/45/55/70/85/100ns (max.)
  - Commercial: 20/25/35/45ns (max.)
- Low power consumption
  - IDT71681/2SA
    Active: 225mW (typ.)
    Standby: 100µw (typ.)
  - IDT71681/2LA
    Active: 225mW (typ.)
    Standby: 10µw (typ.)
- Battery backup operation—2V data retention (L version only)
- High-density 24-pin 300-mil CERDIP and plastic DIP, 24-pin Flatpack and CERPACK, 24-pin SOIC and 28-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71681/IDT71682 are 16,384-bit high-speed static RAMs organized as 4K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

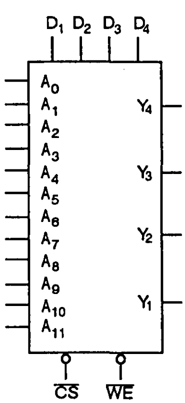
Access times as fast as 20ns are available, with maximum power consumption of only 550mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, this standby mode as long as $\overline{CS}$ remains high. In the ultra-low-power standby mode (I_{SB1}), the devices consume less than 10µW, typically. This capability provides significant system-level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery.

All inputs and outputs of the IDT71681/IDT71682 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

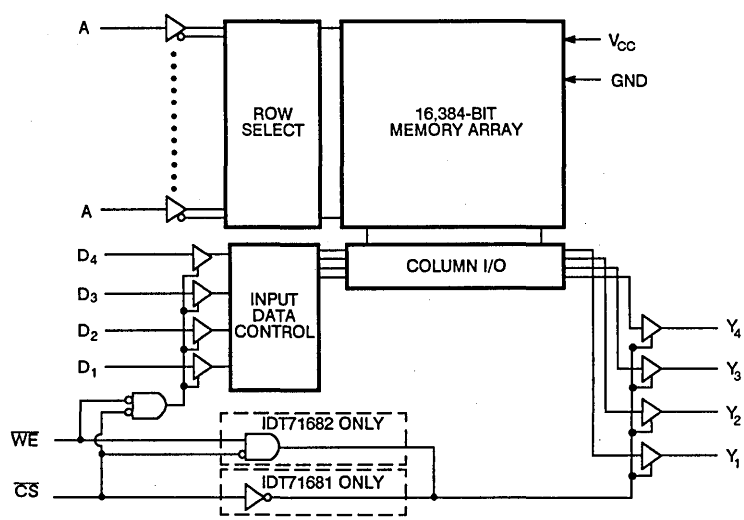
The IDT71681/IDT71682 are packaged in either space-saving 24-pin 300 mil DIPs, SOICs, Flatpacks, CERPACKS, or 28-pin leadless chip carriers, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

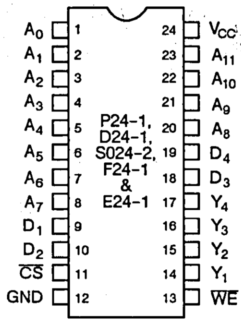
LOGIC SYMBOL



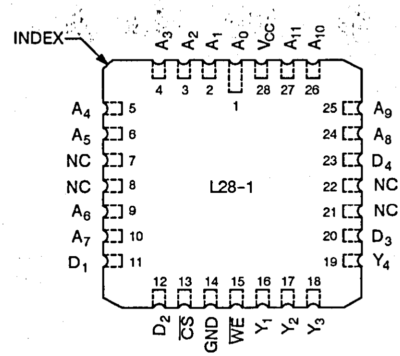
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/FLATPACK/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN NAMES

A_0–A_{11}	Address Inputs	D_1 – D_4	$DATA_{IN}$
$\overline{CS}$	Chip Select	Y_1 – Y_4	$DATA_{OUT}$
$\overline{WE}$	Write Enable	GND	Ground
V_{CC}	Power		

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT71681SA IDT71682SA MIN.	TYP.[1]	MAX.	IDT71681LA IDT71682LA MIN.	TYP.[1]	MAX.	UNIT
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	71681x20[5] 71682x20[5] COM'L.	MIL.	71681x25 71682x25 COM'L.	MIL.	71681x35 71682x35 COM'L.	MIL.	71681x45 71682x45 COM'L.	MIL.	71681x55[6] 71682x55[6] COM'L.	MIL.	71681x70[2, 6] 71682x70[2, 6] COM'L.	MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[3]	SA	90	–	90	100	90	100	90	100	–	100	–	100	mA
		LA	70	–	70	80	70	80	70	80	–	80	–	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	120	–	110	120	100	110	100	110	–	110	–	110	mA
		LA	100	–	90	100	80	90	70	80	–	80	–	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open f = f_{MAX}[3]	SA	45	–	35	45	30	35	30	35	–	35	–	35	mA
		LA	30	–	25	30	20	25	20	25	–	20	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0[3]	SA	20	–	2	10	2	10	2	10	–	10	–	10	mA
		LA	2	–	0.05	0.3	0.05	0.3	0.05	0.3	–	0.3	–	0.3	

NOTES:

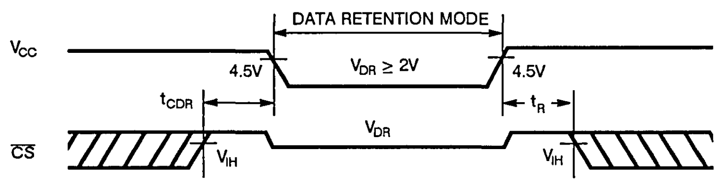
1. All values are maximum guaranteed values.
2. Also available: 85ns and 100ns Military devices.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. "x" in part numbers indicates power rating (SA or LA).
5. 0°C to +70°C temperature range only.
6. -55°C to +125°C temperature range only.

DATA RETENTION CHARACTERISTICS
(L Version Only)

SYMBOL	PARAMETER	TEST CONDITION		IDT71681LA - IDT71682LA MIN.	TYP(1)	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$		2.0	–	–	V
I_{CCDR}	Data Retention Current		MIL.	–	0.5(2)	100(2)	µA
				–	1.0(3)	150(3)	
			COM'L.	–	0.5(2)	20(2)	µA
				–	1.0(3)	30(3)	
t_{CDR}(5)	Chip Deselect to Data Retention Time			0	–	–	ns
t_R(5)	Operation Recovery Time			t_{RC}(4)	–	–	ns

NOTES:
1. $T_A = +25°C$
2. at $V_{CC} = 2V$
3. at $V_{CC} = 3V$
4. t_{RC} = Read Cycle Time
5. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

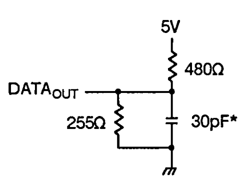


Figure 1. Output Load

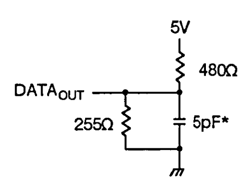


Figure 2. Output Load
(for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

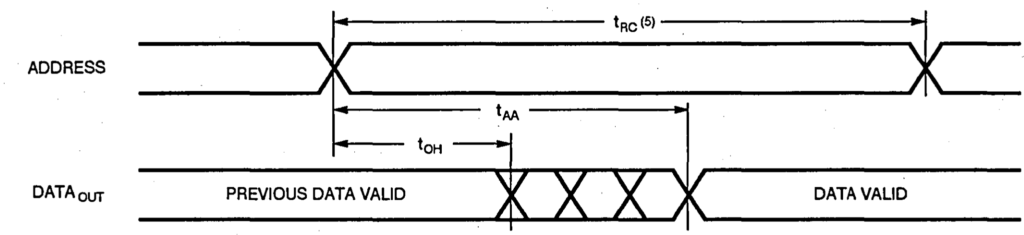
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS[4] (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	71681x20[1] 71682x20[1]		71681x25 71682x25		71681x35 71682x35		71681x45 71682x45		71681x55[2] 71682x55[2]		71681x70[2] 71682x70[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	20	–	25	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Select to Output in Low Z[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselect to Output in High Z[3]	–	10	–	10	–	15	–	20	–	25	–	30	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	20	–	25	–	35	–	40	–	50	–	60	ns
t_{RCS}	Read Command Set-Up Time	-5	–	-5	–	-5	–	-5	–	-5	–	-5	–	ns
t_{RCH}	Read Command Hold Time	-5	–	-5	–	-5	–	-5	–	-5	–	-5	–	ns

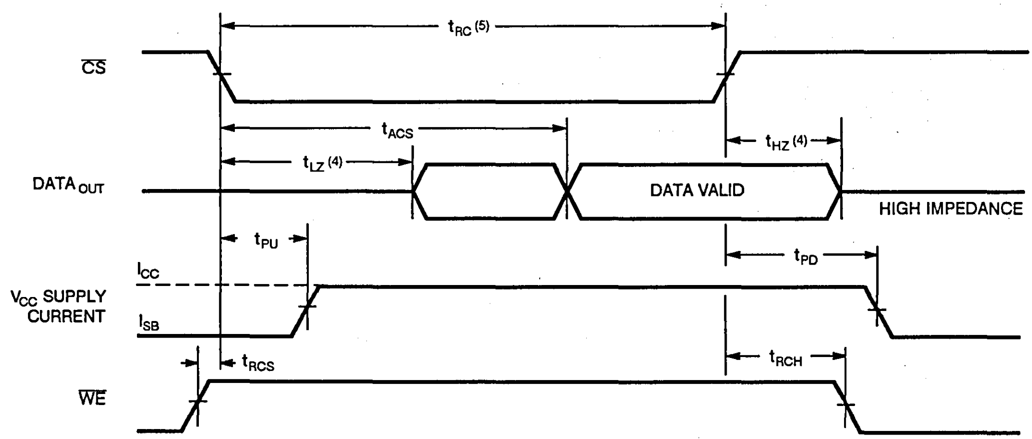
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. "x" in part numbers represents SA or LA.

TIMING WAVEFORM OF READ CYCLE NO. 1[1, 2]



4

TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 3]



NOTES:

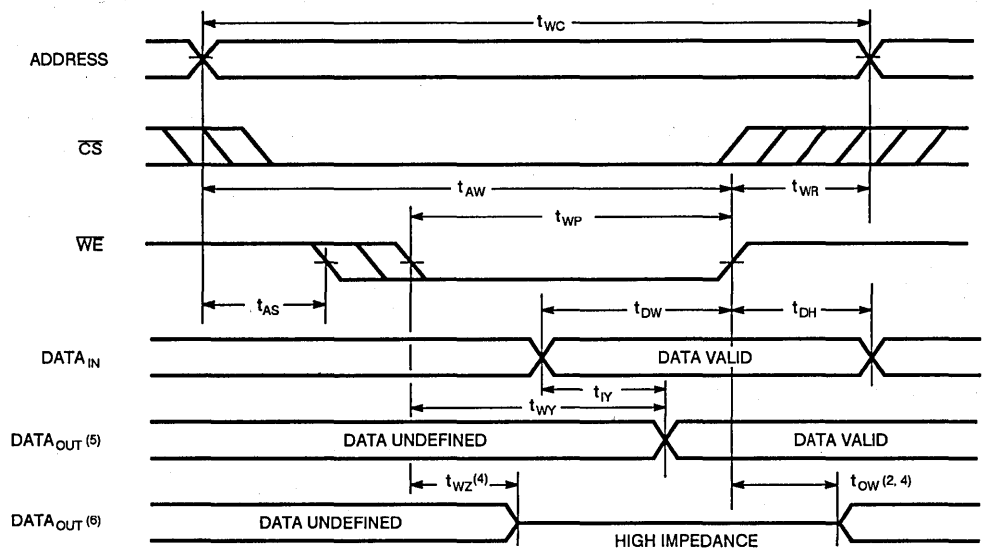
1. $\overline{WE}$ is High for READ Cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

AC ELECTRICAL CHARACTERISTICS[4] (V_{CC} = 5V ±10%, All Temperature Ranges)

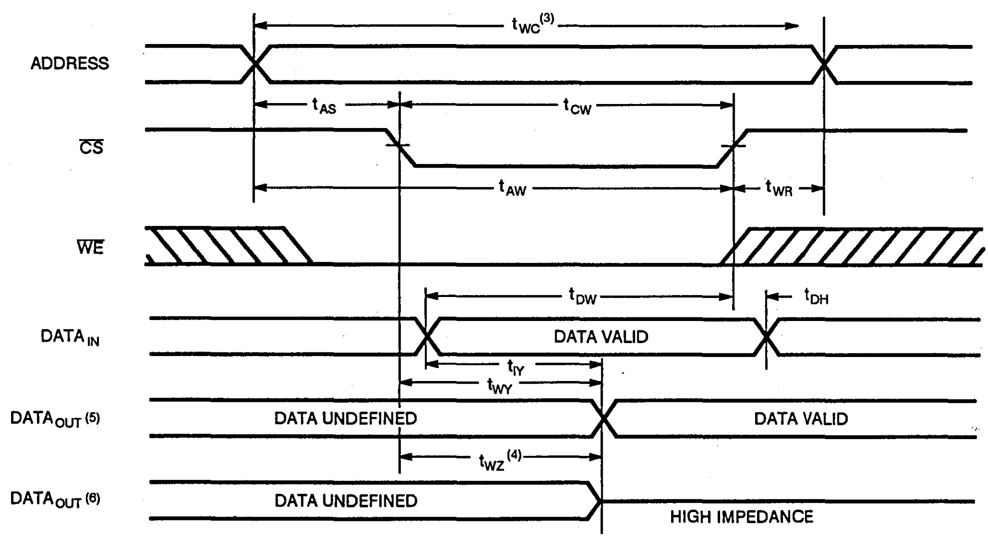
SYMBOL	PARAMETER	71681x20[1] 71682x20[1] MIN.	MAX.	71681x25 71682x25 MIN.	MAX.	71681x35 71682x35 MIN.	MAX.	71681x45 71682x45 MIN.	MAX.	71681x55[2] 71682x55[2] MIN.	MAX.	71681x70[2] 71682x70[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{CW}	Chip Select to End of Write	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	25	–	30	–	35	–	40	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	13	–	13	–	17	–	20	–	20	–	25	–	ns
t_{DH}	Data Hold Time	3	–	3	–	3	–	3	–	3	–	3	–	ns
t_{IY}	Data Valid to Output Valid (71681 only)[3]	–	20	–	25	–	30	–	35	–	35	–	40	ns
t_{WY}	Write Enable to Output Valid (71681 only)[3]	–	20	–	25	–	30	–	35	–	35	–	40	ns
t_{WZ}	Write Enable to Output in HIGH Z (71682 only)[3]	–	7	–	7	–	13	–	20	–	25	–	30	ns
t_{OW}	Output Active from End of Write (71682 only)[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. "x" in part numbers represents SA or LA.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 2.
5. For IDT71681 only.
6. For IDT71682 only.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write [1]	L	L	D_{IN}	Active
Write [2]	L	L	High Z	Active

NOTES:

1. For IDT71681 only.
2. For IDT71682 only.

CAPACITANCE (T_A= +25°C, f = 1.0MHz)

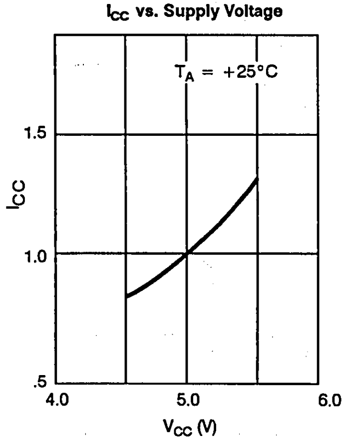
SYMBOL	PARAMETER [1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

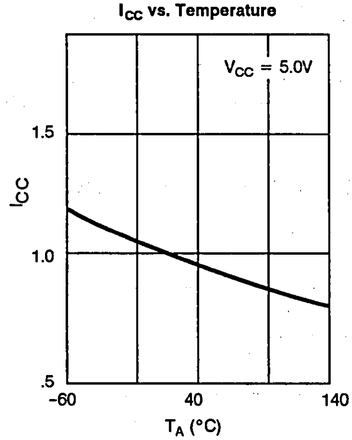
1. This parameter is determined by device characterization but is not production tested.

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

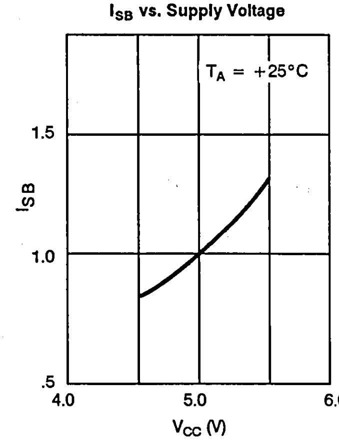
I_{CC} vs. Supply Voltage



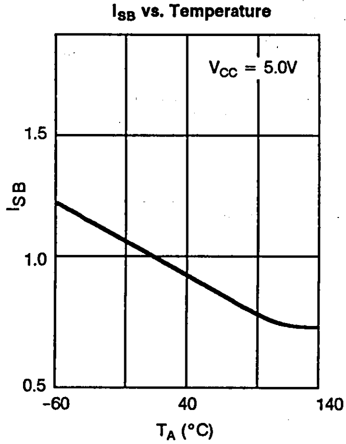
I_{CC} vs. Temperature



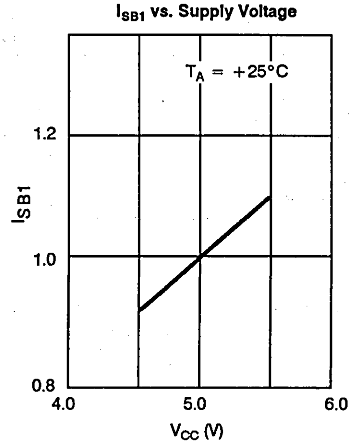
I_{SB} vs. Supply Voltage



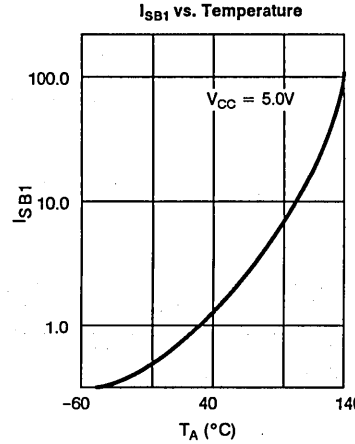
I_{SB} vs. Temperature



I_{SB1} vs. Supply Voltage

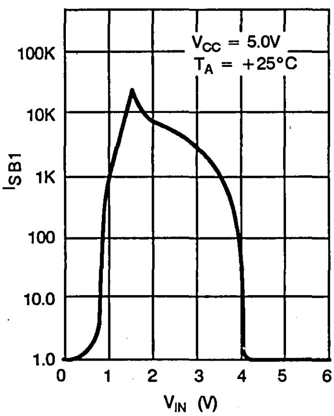


I_{SB1} vs. Temperature

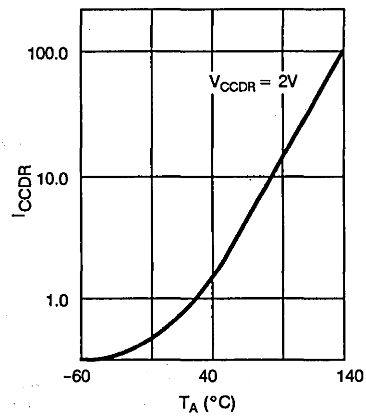


NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

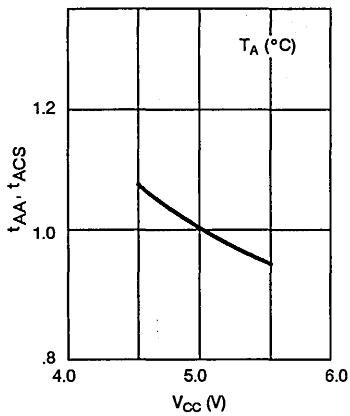
I_{SB1} vs. V_{IN}



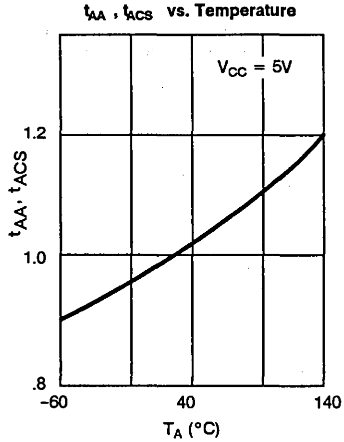
I_{CCDR} vs. Temperature



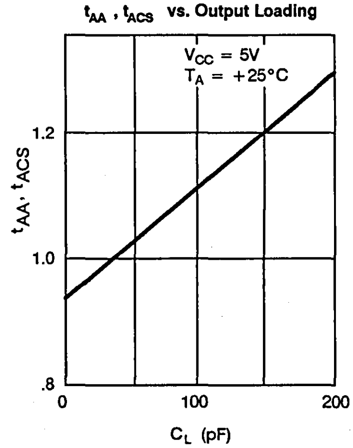
t_{AA}, t_{ACS} vs. Supply Voltage



t_{AA}, t_{ACS} vs. Temperature



t_{AA}, t_{ACS} vs. Output Loading



ORDERING INFORMATION

IDT XXXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	L	Leadless Chip Carrier
	SO	Small Outline IC
	E	CERPACK
	F	Flatpack
Speed (Speed in Nanoseconds)	20	Commercial only
	25	
	35	
	45	
	55	Military Only
	70	Military Only
	85	Military Only
	100	Military Only
Power	SA	Standard Power
	LA	Low Power
Device Type	71681	16K (4K x 4-Bit) Outputs Follow Inputs
	71682	16K (4K x 4-Bit) High Impedance Outputs

CMOS STATIC RAM 16K (2K x 8-BIT)

IDT6116SA IDT6116LA

FEATURES:

- High-speed
  - Military: 25/30/35/45/55/70/90/120/150ns (max.)
  - Commercial: 15/20/25/30/35/45ns (max.)
- Low-power operation
  - IDT6116SA
    Active: 180mW (typ.)
    Standby: 100μW (typ.)
  - IDT6116LA
    Active: 160mW (typ.)
    Standby: 20μW (typ.)
- Battery backup operation—2V data retention voltage (LA version only)
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 24-pin DIP, 24-pin THINDIP and plastic DIP, 24-, 28- and 32-pin LCC, 24-pin SOIC and 24-lead CERPACK and Flatpack
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 84036 is listed on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

Access times as fast as 25ns are available with maximum power consumption of only 666mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby power mode as long as $\overline{CS}$ remains high. In the standby mode, the low-power device consumes less than 20μW typically. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1μW to 4μW operating off a 2V battery.

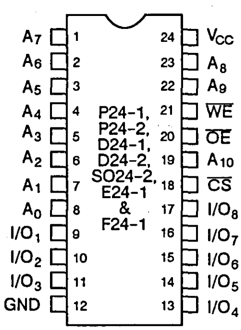
All inputs and outputs of the IDT6116SA/LA are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP, 24-, 28- and 32-pin leadless chip carriers, 24-lead CERPACK and flatpack, and a 24-lead gull-wing SOIC, providing high board-level packing densities.

Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

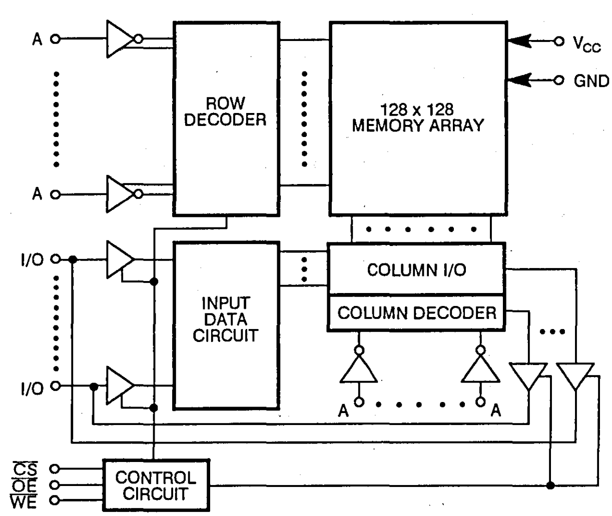
4

PIN CONFIGURATION



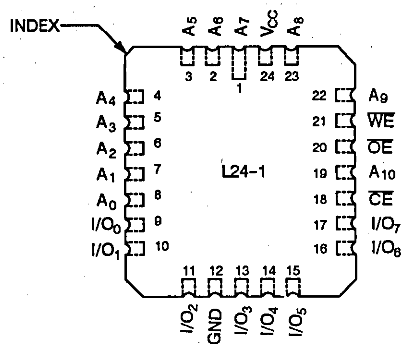
DIP/SOIC/FLATPACK/CERPACK
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM

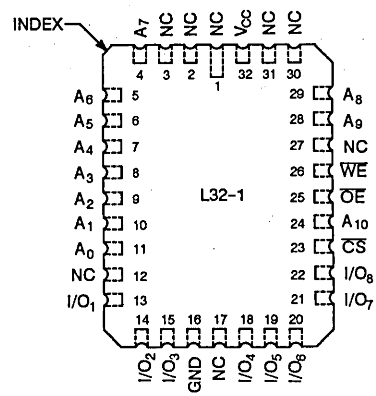


CEMOS is a trademark of Integrated Device Technology, Inc.

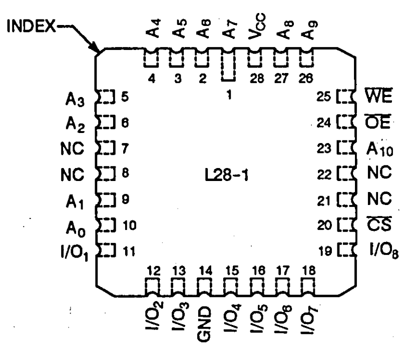
PIN CONFIGURATIONS



**24-PIN LCC
TOP VIEW**



**32-PIN LCC
TOP VIEW**



**28-PIN LCC
TOP VIEW**

PIN NAMES

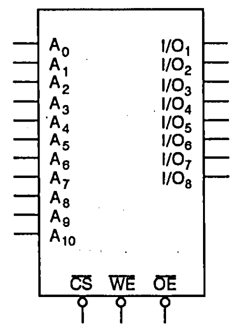
A_0 - A_{10}	Address	$\overline{WE}$	Write Enable
I/O_1 - I/O_8	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	GND	Ground
V_{CC}	Power		

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

LOGIC SYMBOL



RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-1.0[1]	–	0.8	V
C_L	Output Load	–	–	30	pF

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6116SA MIN.	TYP.(1)	MAX.	IDT6116LA MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

4

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	6116SA15(2)/20(2) 6116LA15(2)/20(2) COM'L.	MIL.	6116SA25/30 6116LA25/30 COM'L.	MIL.	6116SA35 6116LA35 COM'L.	MIL.	6116SA45/55 6116LA45/55 COM'L.	MIL.	6116SA70/90 6116LA70/90 COM'L.	MIL.	6116SA120/150(3) 6116LA120/150(3) COM'L.	MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0	SA	120/110	–	100/80	110	80	90	80/–	90	–	90	–	90	mA
		LA	110/100		90/75	105	75	85	75/–	85	–	85	–	85	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX} (4)	SA	140/130	–	120/110	135	100	115	100/–	100	–	100	–	100/90	mA
		LA	130/120	–	110/105	125	95	105	90/–	95/90	–	90/85	–	85	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX} (4)	SA	40	–	40/35	45	25	35	25/–	25	–	25	–	25	mA
		LA	35	–	35/30	40	25	30	20/–	20	–	20/15	–	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0	SA	2	–	2	10	2	10	2/–	10	–	10	–	10	mA
		LA	0.1	–	0.1	0.9	0.1	0.9	0.1/–	0.9	–	0.9	–	0.9	

NOTES:
1. All values are maximum guaranteed values.
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. f_{MAX} = $1/t_{RC}$

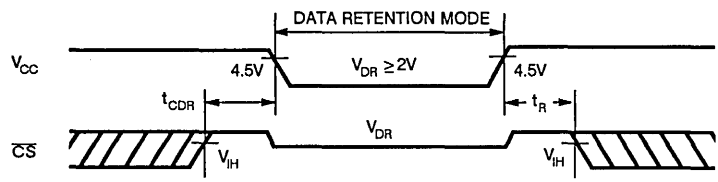
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.[1] V_{CC} @ 2.0V	TYP.[1] V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$, $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	0.5	1.5	200	300	µA
			COM'L.	–	0.5	1.5	20	30	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–		–		ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–		–		ns
$\|I_{LI}\|$	Input Leakage Current			–	–		2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed, but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

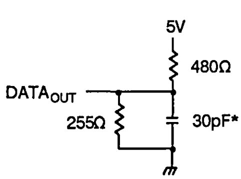


Figure 1. Output Load

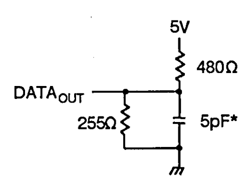


Figure 2. Output Load (for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, t_{OW})

*Including scope and jig.

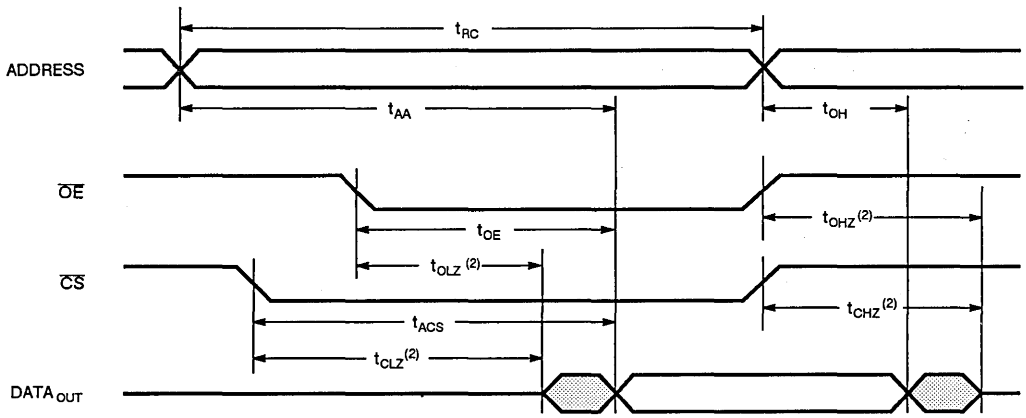
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6116SA15/20(1) 6116LA15/20(1)		6116SA25/30 6116LA25/30		6116SA35/45 6116LA35/45		6116SA55(2) 6116LA55(2)		6116SA70/90(2) 6116LA70/90(2)		6116SA120/150(2) 6116LA120/150(2)		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	15/20	—	25/30	—	35/45	—	55	—	70/90	—	120/150	—	ns
t_{AA}	Address Access Time	—	15/20	—	25/30	—	35/45	—	55	—	70/90	—	120/150	ns
t_{ACS}	Chip Select Access Time	—	15/20	—	25/30	—	35/45	—	50	—	65/90	—	120/150	ns
t_{CLZ}	Chip Select to Output in Low Z(3)	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	16/18	—	20/25	—	40	—	50/65	—	80/100	ns
t_{OLZ}	Output Enable to Output in Low Z(3)	0	—	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Deselect to Output in High Z(3)	—	10/14	—	16/18	—	20/25	—	30	—	35/40	—	40	ns
t_{OHZ}	Output Disable to Output in High Z(3)	—	8/12	—	16/18	—	20/25	—	30	—	35/40	—	40	ns
t_{OH}	Output Hold from Address Change	3	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

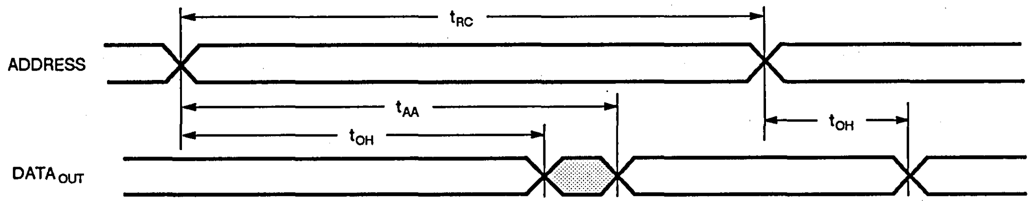
4

TIMING WAVEFORM OF READ CYCLE NO. 1 (1)

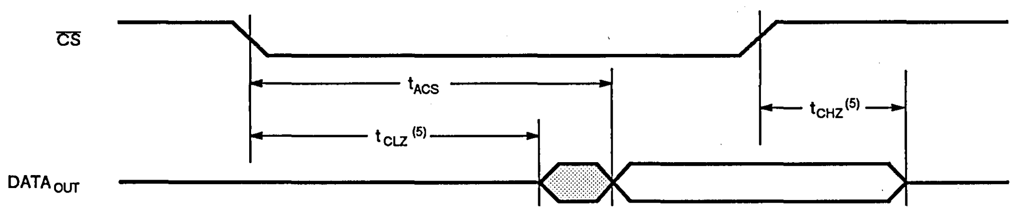


NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

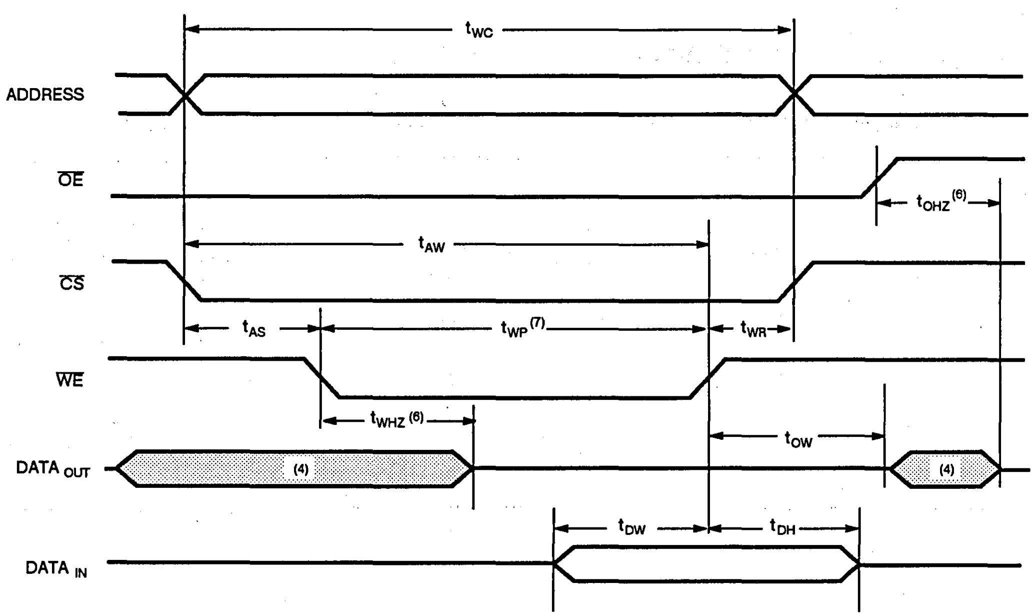
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

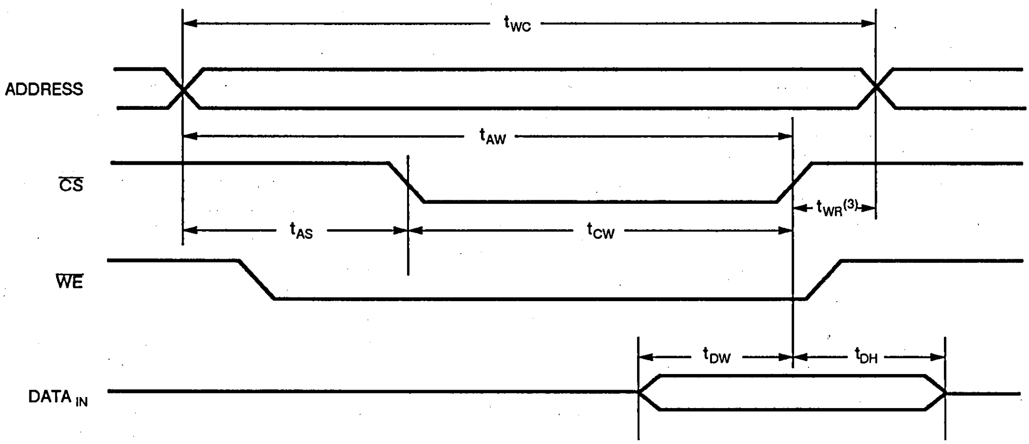
SYMBOL	PARAMETER	6116SA15/20[1] 6116LA15/20[1]		6116SA25/30 6116LA25/30		6116SA35/45 6116LA35/45		6116SA55[2] 6116LA55[2]		6116SA70/90[2] 6116LA70/90[2]		6116SA120/150[2] 6116LA120/150[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE														
t_{WC}	Write Cycle Time	15/20	–	25/30	–	35/45	–	55	–	70/90	–	120/150	–	ns
t_{CW}	Chip Select to End of Write	14/15	–	17/20	–	25/30	–	40	–	40/55	–	70/90	–	ns
t_{AW}	Address Valid to End of Write	14/15	–	17/20	–	25/30	–	45	–	65/80	–	105/120	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	5	–	15	–	20	–	ns
t_{WP}	Write Pulse Width	10/12	–	15	–	20/25	–	40	–	40/55	–	70/90	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	5	–	5	–	5/10	–	ns
t_{OHZ}	Output Disable to Output in High Z[3]	–	8/12	–	16/18	–	20/25	–	30	–	35/40	–	40	ns
t_{WHZ}	Write to Output in High Z[3]	–	7/10	–	16/18	–	20/25	–	30	–	35/40	–	40	ns
t_{DW}	Data to Write Time Overlap	10/12	–	15	–	15/20	–	25	–	30	–	35/40	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	5	–	5	–	5/10	–	ns
t_{OW}	Output Active from End of Write[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]

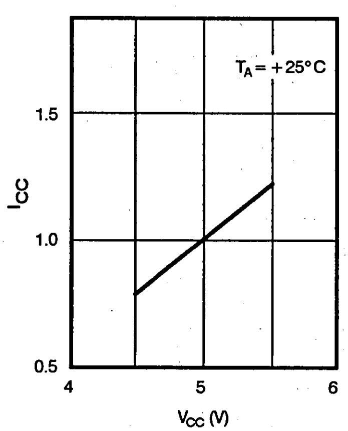


NOTES:

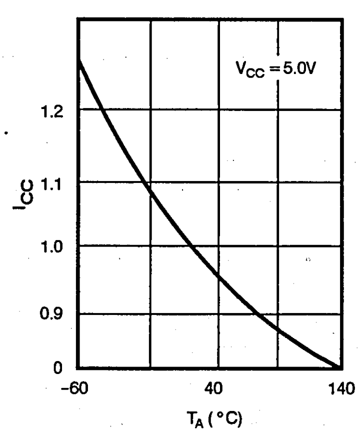
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ}+ t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

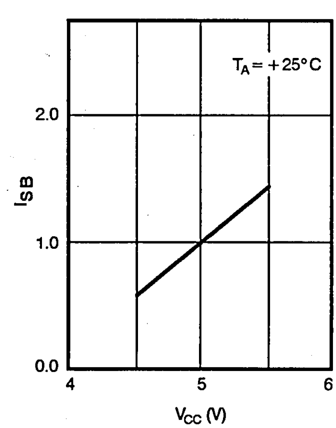
I_{CC} vs. Supply Voltage



I_{CC} vs. Temperature

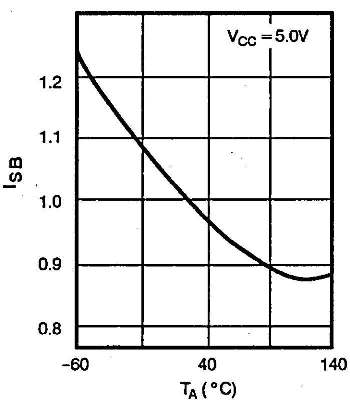


I_{SB} vs. Supply Voltage

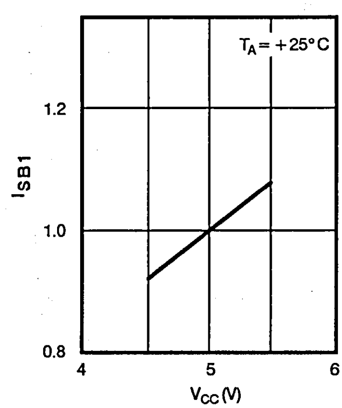


NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

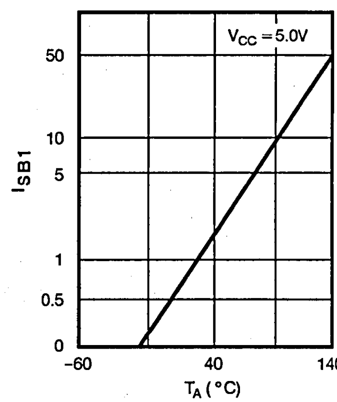
I_{SB} vs. Temperature



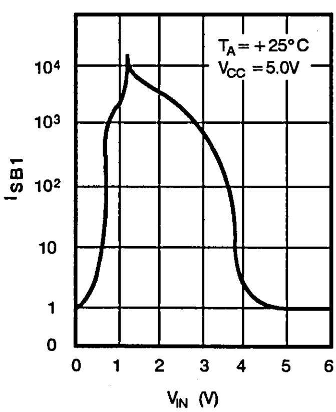
I_{SB1} vs. Supply Voltage



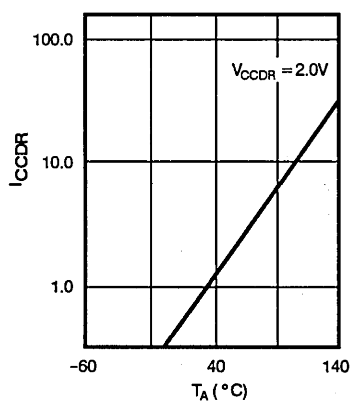
I_{SB1} vs. Temperature



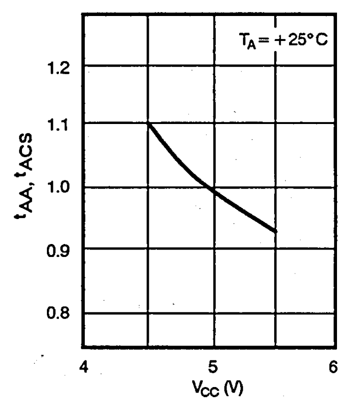
I_{SB1} vs. V_{IN}



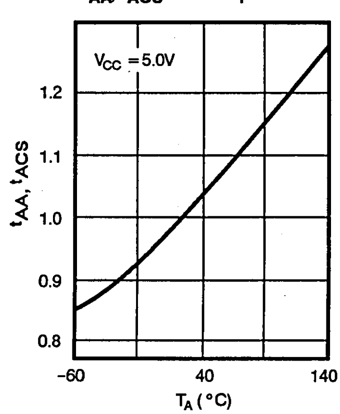
I_{CCDR} vs. Temperature



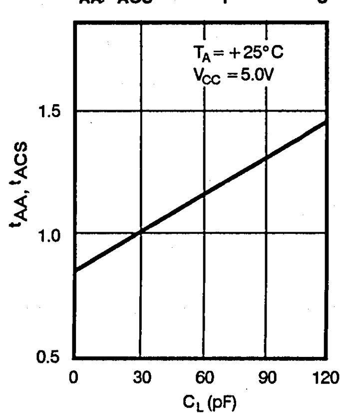
t_{AA}, t_{ACS} vs. Supply Voltage



t_{AA}, t_{ACS} vs. Temperature



t_{AA}, t_{ACS} vs. Output Loading



TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High Z
Read	L	L	H	$DATA_{OUT}$
Read	L	H	H	High Z
Write	L	X	L	$DATA_{IN}$

PINOUT CONFIGURATION
16K CMOS SRAM
IDT6116 (2K x 8)

FUNCTION	LOGIC SYMBOL	PIN NUMBER 24 DIP/ SOIC/ LCC/ FLATPACK	28 LCC	32 LCC
Address Line	A_7	1	1	4
Address Line	A_6	2	2	5
Address Line	A_5	3	3	6
Address Line	A_4	4	4	7
Address Line	A_3	5	5	8
Address Line	A_2	6	6	9
Address Line	A_1	7	9	10
Address Line	A_0	8	10	11
Input/Output	I/O_1	9	11	13
Input/Output	I/O_2	10	12	14
Input/Output	I/O_3	11	13	15
Power Ground	GND	12	14	16
Input/Output	I/O_4	13	15	18
Input/Output	I/O_5	14	16	19
Input/Output	I/O_6	15	17	20
Input/Output	I/O_7	16	18	21
Input/Output	I/O_8	17	19	22
Chip Select/ Data Retention	$\overline{CS}$	18	20	23
Address Line	A_{10}	19	23	24
Output Enable	$\overline{OE}$	20	24	25
Write Enable	$\overline{WE}$	21	25	26
Address Line	A_9	22	26	28
Address Line	A_8	23	27	29
Power Supply	V_{CC}	24	28	32

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

THERMAL RESISTANCE (Typical)

PACKAGE	PIN COUNT	θ_{JA}	θ_{JC}	UNIT
300 MIL PLASTIC DIP	24	54-58	28-32	°C/ WATT
600 MIL PLASTIC DIP	24	53-56	25-30	
300 MIL CERDIP	24	48-52	24-28	
600 MIL CERDIP	24	50-55	17-25	
FLATPACK	24	85-90	24-28	
LCC	24	85-110	30-45	
LCC	28	85-90	28-35	
LCC	32	80-90	25-35	
SOIC	24	45-70	25-30	

ORDERING INFORMATION

IDT	XXXX	A	999	A	A
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

TP	Plastic THINDIP
P	Plastic DIP (600 MIL)
TD	THINDIP (CERDIP)
D	CERDIP (600 MIL)
L	Leadless Chip Carrier (Indicate 24-, 28- or 32-pin)
SO	Small Outline IC
E	CERPACK
F	Flatpack

Speed — Speed in Nanoseconds

25	Commercial Only
30	Commercial Only
35	
45	
55	Military Only
70	Military Only
90	Military Only
120	Military Only
150	Military Only

Power

LA	Low Power
SA	Standard Power

Device Type

6116	16K (2K x 8-Bit) Static RAM

4

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (64K x 1-BIT)

IDT7187S
IDT7187L

FEATURES:

- High speed (equal access and cycle time)
  - Military: 25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT7187S
    Active: 300mW (typ.)
    Standby: 100μw (typ.)
  - IDT7187L
    Active: 250mW (typ.)
    Standby: 30μw (typ.)
- Battery backup operation—2V data retention (L version only)
- JEDEC standard high-density 22-pin plastic and hermetic DIP, 24-pin plastic SOIC, 22-pin and 28-pin leadless chip carrier and 24-pin flatpack and CERPACK
- Produced with advanced CEMOS ™ high-performance technology
- Separate data input and output
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86015 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

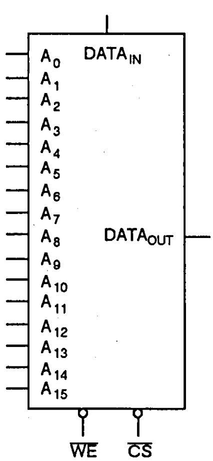
The IDT7187 is a 65,536-bit high-speed static RAM organized as 64K x 1. It is fabricated using IDT's high-performance, high-reliability technology, CEMOS. Access times as fast as 15ns are available with maximum power consumption of 880mW.

Both the standard (S) and low-power (L) versions of the IDT7187 provide two standby modes—I_{SB} and I_{SB1}. I_{SB} provides low-power operation (358mW max.); I_{SB1} provides ultra-low-power operation (5mW max.). The low-power (L) version also provides the capability for data retention using battery backup. When using a 2V battery, the circuit typically consumes only 30μW.

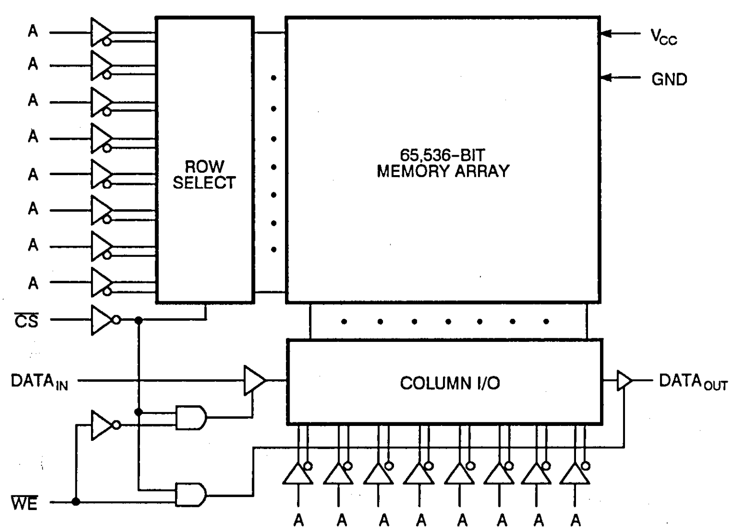
Ease of system design is achieved by the IDT7187 with full asynchronous operation, along with matching access and cycle times. The device is packaged in an industry standard 22-pin, 300 mil plastic or hermetic DIP, 24-pin plastic SOIC, 22- and 28-pin leadless chip carriers, or 24-pin flatpack or CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

LOGIC SYMBOL

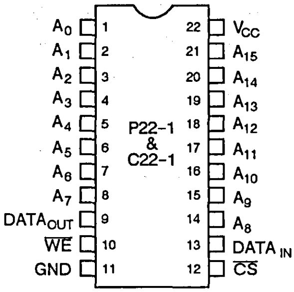


FUNCTIONAL BLOCK DIAGRAM

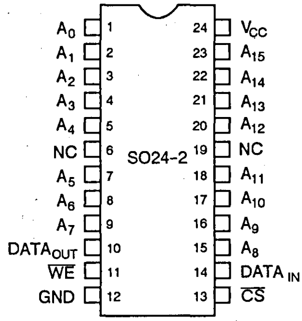


CEMOS is a trademark of Integrated Device Technology, Inc.

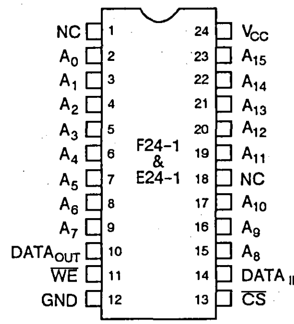
PIN CONFIGURATIONS



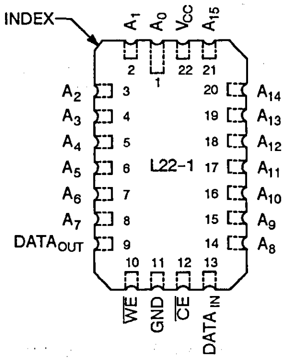
DIP
TOP VIEW



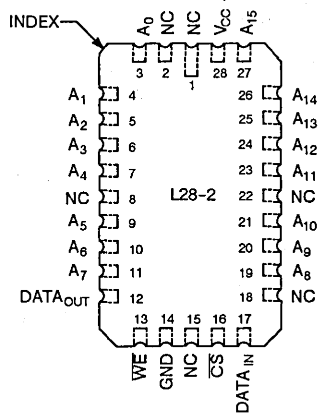
SOIC
TOP VIEW



FLATPACK/CERPACK
TOP VIEW



22-PIN LCC
TOP VIEW



28-PIN LCC
TOP VIEW

PIN NAMES

A_0–A_{15}	Address Inputs	$DATA_{IN}$	Data Input
$\overline{CS}$	Chip Select	$DATA_{OUT}$	Data Output
$\overline{WE}$	Write Enable	GND	Ground
V_{CC}	Power		

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT7187S MIN.	IDT7187S TYP.[1]	IDT7187S MAX.	IDT7187L MIN.	IDT7187L TYP.[1]	IDT7187L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	7187S15 7187L15 COM'L.	MIL.	7187S20 7187L20 COM'L.	MIL.	7187S25 7187L25 COM'L.	MIL.	7187S30/35 7187L30/35 COM'L.	MIL.	7187S45/55[3] 7187L45/55[3] COM'L.	MIL.	7187S70 7187L70 COM'L.	MIL.	7187S85 7187L85 COM'L.	MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0[2]	S	135	–	120	140	90	105	90	105	90	105	–	105	–	105	mA
		L	115	–	105	125	70	85	70	85	70	85	–	85	–	85	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	S	165	–	150	170	120	130	110	120	110	120	–	120	–	120	mA
		L	150	–	135	155	100	110	95/90	110/100	85	95	–	90	–	90	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}[2]	S	65	–	60	65	55	55	45	50	45	50	–	50	–	50	mA
		L	55	–	50	55	45	50	40/35	45/40	30/25	35/30	–	28	–	28	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0[2]	S	25	–	20	25	15	20	15	20	15	20	–	20	–	20	mA
		L	2.5	–	1.0	2.0	0.3	1.5	0.3	1.5	0.3	1.5	–	1.5	–	1.5	

NOTES:

1. All values are maximum guaranteed values.
2. f = f_{MAX} (All inputs except Chip Select cycling at f = $1/t_{RC}$). f = 0 means no address or control lines change.
3. –55°C to +125°C temperature range only.

DATA RETENTION CHARACTERISTICS

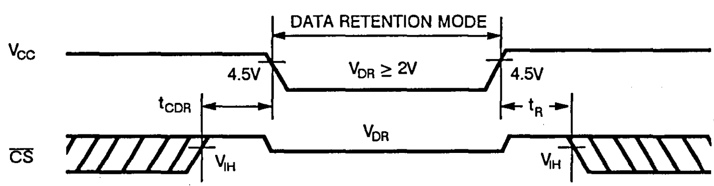
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	10	15	600	900	µA
			COM'L.	–	10	15	150	225	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

4

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

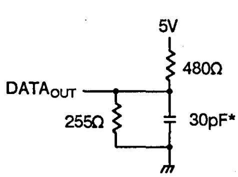


Figure 1. Output Load

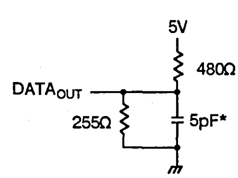


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

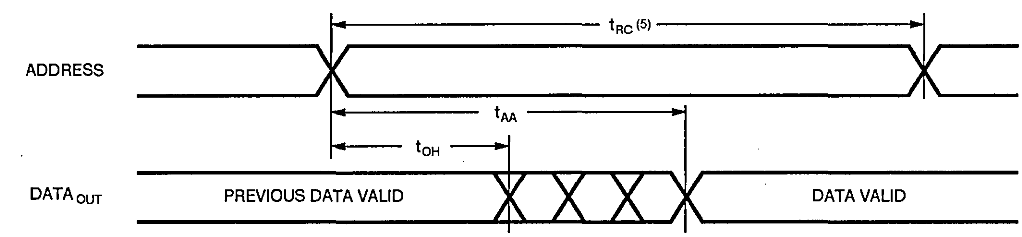
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

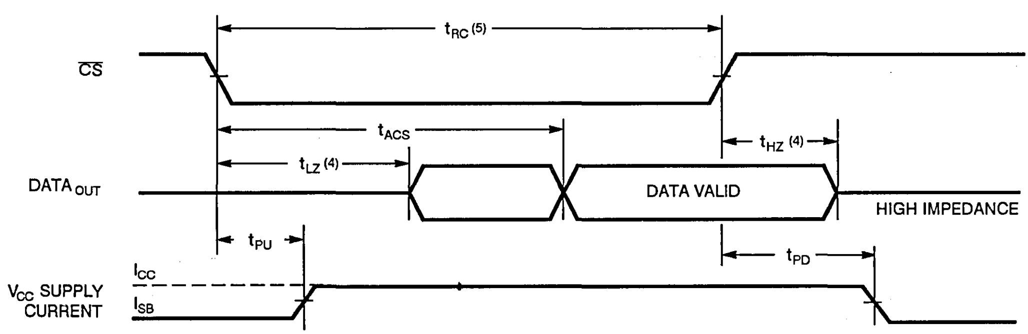
SYMBOL	PARAMETER	7187S15(1)/20 7187L15(1)/20		7187S25/30 7187L25/30		7187S35/45 7187L35/45		7187S55(2) 7187L55(2)		7187S70(2) 7187L70(2)		7187S85(2) 7187L85(2)		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	15/20	–	25/30	–	35/45	–	55	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	15/20	–	25/30	–	35/45	–	55	–	70	–	85	ns
t_{ACS}	Chip Select Access Time	–	15/20	–	25/30	–	35/45	–	55	–	70	–	85	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Select to Output in Low Z (3)	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselect to Output in High Z (3)	–	7/8	–	20/25	–	25/30	–	30	–	30	–	40	ns
t_{PU}	Chip Select to Power Up Time (3)	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time (3)	–	15/20	–	20/30	–	30/35	–	35	–	35	–	40	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1 (1, 2)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 3)



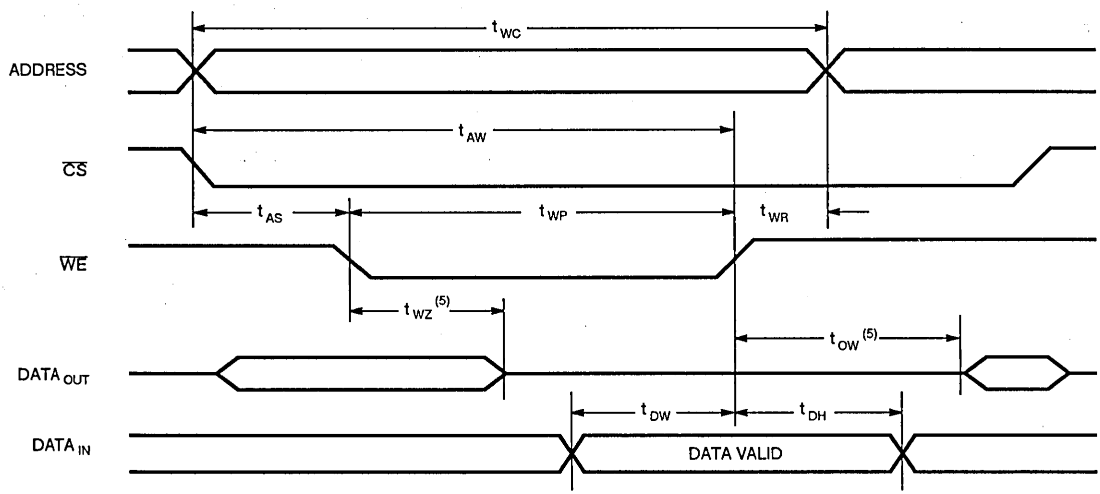
NOTES:
1. $\overline{WE}$ is High for READ Cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

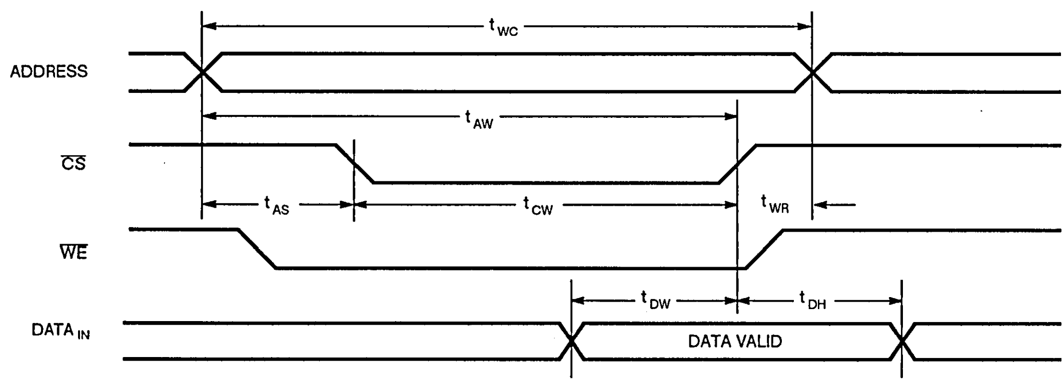
SYMBOL	PARAMETER	7187S15[1]/20 7187L15[1]/20 MIN.	MAX.	7187S25/30 7187L25/30 MIN.	MAX.	7187S35/45 7187L35/45 MIN.	MAX.	7187S55[2] 7187L55[2] MIN.	MAX.	7187S70[2] 7187L70[2] MIN.	MAX.	7187S85[2] 7187L85[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	13/17	—	25/30	—	35/45	—	55	—	70	—	85	—	ns
t_{CW}	Chip Select to End of Write	13/17	—	20/25	—	30/40	—	50	—	55	—	65	—	ns
t_{AW}	Address Valid to End of Write	13/17	—	20/25	—	30/40	—	50	—	55	—	65	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	13/17	—	20	—	25/30	—	35	—	40	—	45	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	8/10	—	15/20	—	20/25	—	25	—	30	—	35	—	ns
t_{DH}	Data Hold Time	0	—	5	—	5	—	5	—	5	—	5	—	ns
t_{WZ}	Write Enable to Output in High Z[3]	—	5/6	—	20/25	—	25/30	—	30	—	30	—	40	ns
t_{OW}	Output Active from End of Write[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 4)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

4

ORDERING INFORMATION

IDT XXXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range:

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

P	Plastic DIP
C	Sidebraze DIP
L	Leadless Chip Carrier (specify 22 or 28 pins)
SO	Small Outline IC
E	CERPACK
F	Flatpack

Speed (Speed in Nanoseconds):

15	Commercial Only
20	Commercial Only
25	
30	
35	
45	
55	Military Only
70	Military Only
85	Military Only

Power:

S	Standard Power
L	Low Power

Device Type:

7187	64K (64K x 1-Bit)

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (64K x 1-BIT)

PRELIMINARY
IDT100490

FEATURES:

- 65,536-words x 1-bit organization
- Low power dissipation: 320mW (typ.)
- Fully compatible with 100K logic level
- Address access time: 15/20ns (max.)
- Write pulse width: 10ns (min.)
- Open emitter output for ease of memory expansion
- Static operation: no clocks or refresh required
- Separate data input and output
- JEDEC standard high-density 22-pin plastic and sidebraze DIP and 24-pin Small Outline IC

DESCRIPTION:

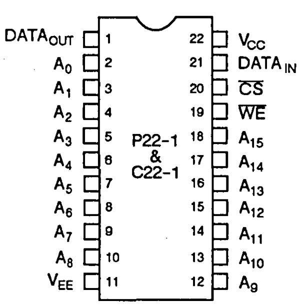
The IDT100490 is a 100K compatible 65,536-bit high-speed BiCEMOS™ ECL static RAM organized as 64K x 1.

The IDT100490 is available with address access times as fast as 15ns with a typical power consumption of only 320mW. This product offers the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to reduce package count in an ECL system without increasing either power dissipation or access time.

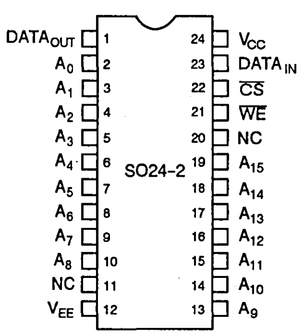
Designed for very high-speed applications, the IDT100490 is fully compatible with standard ECL 100K logic levels and offers extremely fast access times. The address access time of 15ns and write pulse width of 10ns assure that operations of this BiCEMOS part will be as fast as those available with less dense parts requiring external address decoding.

The IDT100490 is fabricated using IDT's high-performance, high-reliability BiCEMOS technology. Operating power dissipation is extremely low compared with most ECL-compatible bipolar devices, lowering power supply and cooling requirements.

PIN CONFIGURATIONS

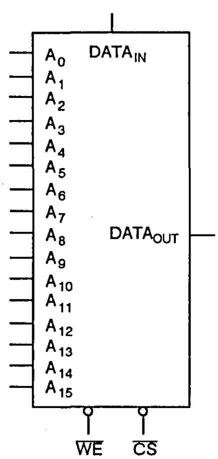


DIP, TOP VIEW

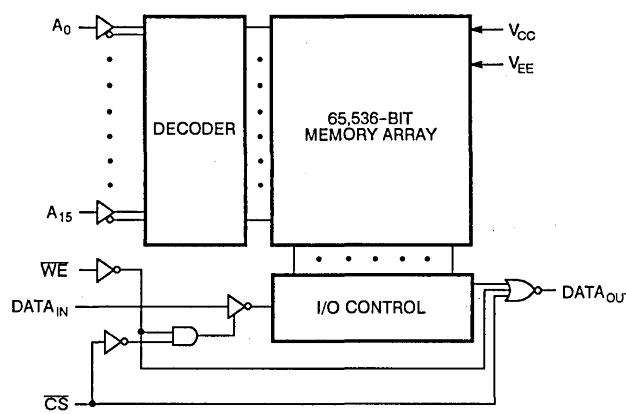


SOIC, TOP VIEW

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



BiCEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING		VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Hermetic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	–	6	pF
C_{OUT}	Output Capacitance	–	6	pF

TRUTH TABLE [1]

$\overline{CS}$	$\overline{WE}$	$DATA_{OUT}$	FUNCTION
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:

1. H = High, L = Low, X = Don't Care

4

DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, RL = 50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2m/sec)

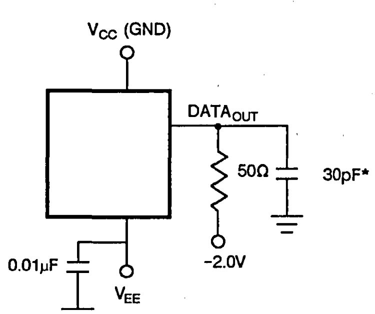
SYMBOL	PARAMETER	TEST CONDITIONS		MIN. (B)	TYP.[1]	MAX. (A)	UNIT
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$		–	–	220	µA
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	–	µA
I_{EE}	Supply Current	All inputs and outputs open		-120	-70	–	mA

NOTE:

1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

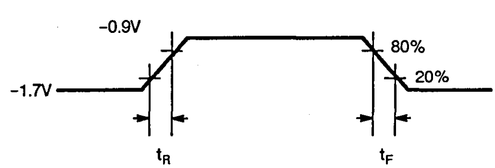
LOAD CONDITION

Test Circuit



*Includes probe and jig capacitance.

INPUT PULSE

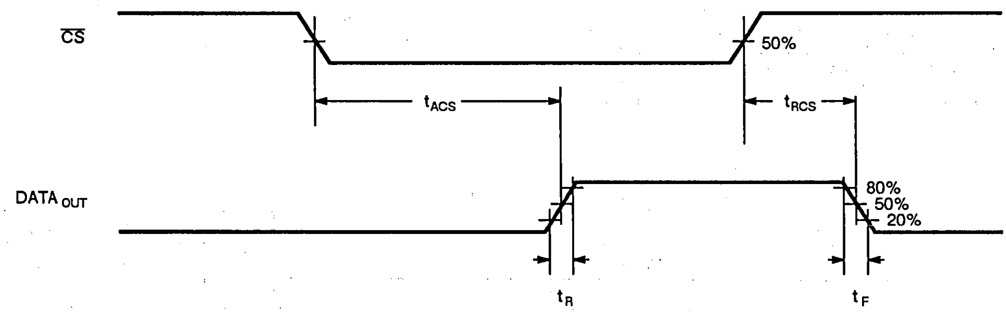


$t_R = t_F$ = 2.0ns typ.

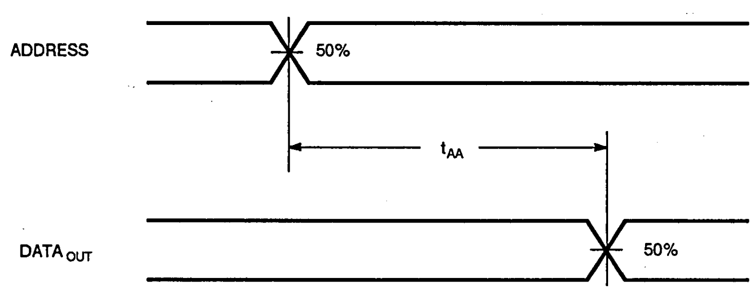
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -4.5V ±5%, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT100490S15 MIN.	IDT100490S15 MAX.	IDT100490S20 MIN.	IDT100490S20 MAX.	UNIT
READ CYCLE							
t_{ACS}	Chip Select Access Time	–	–	10	–	10	ns
t_{RCS}	Chip Select Recovery Time	–	–	10	–	10	ns
t_{AA}	Address Access Time	–	–	15	–	20	ns

TIMING WAVEFORM OF READ CYCLE NO. 1



TIMING WAVEFORM OF READ CYCLE NO. 2



RISE/FALL TIME

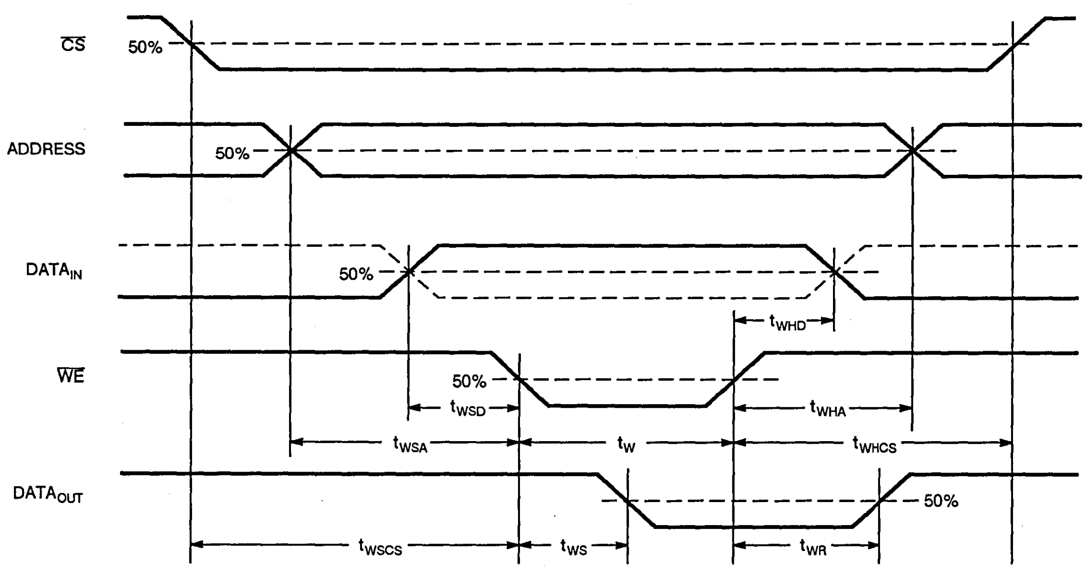
SYMBOL	PARAMETER	TEST CONDITION	IDT100490 MIN.	IDT100490 TYP.	IDT100490 MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

AC ELECTRICAL CHARACTERISTICS (V_{EE} = -4.5V ±5%, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT100490S15 MIN.	IDT100490S15 MAX.	IDT100490S20 MIN.	IDT100490S20 MAX.	UNIT
WRITE CYCLE							
t_W	Write Pulse Width	t_{WSA} = minimum	10	–	15	–	ns
t_{WSD}	Data Set-up Time	–	2	–	3	–	ns
t_{WHD}	Data Hold Time	–	3	–	4	–	ns
t_{WSA}	Address Set-up Time	t_W = minimum	2	–	3	–	ns
t_{WHA}	Address Hold Time	–	3	–	4	–	ns
t_{WSCS}	Chip Select Set-up Time	–	2	–	3	–	ns
t_{WHCS}	Chip Select Hold Time	–	3	–	4	–	ns
t_{WS}	Write Disable Time	–	–	10	–	10	ns
t_{WR}	Write Recovery Time	–	–	18	–	23	ns

4

TIMING WAVEFORM OF WRITE CYCLE



ORDERING INFORMATION

IDT XXXXX A 999 A A

IDT	XXXXX	A	999	A	A
	Device Type	Power	Speed	Package	Process/ Temperature Range

Code	Description
Blank	Commercial (0°C to +70°C)
P	Plastic DIP
C	Sidebraze DIP
SO	Small Outline IC
15	Speed in Nanoseconds
20	
S	Standard Power
100490	64K (64K x 1-Bit) BiCMOS ECL Static RAM

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (16K x 4-BIT)

IDT7188S
IDT7188L

FEATURES:

- High-speed (equal access and cycle times)
  - Military: 20/25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT7188S
    Active: 350mW (typ.)
    Standby: 100μW (typ.)
  - IDT7188L
    Active: 300mW (typ.)
    Standby: 30μW (typ.)
- Battery backup operation—2V data retention (L version only)
- Available in high-density industry standard 22-pin, 300 mil ceramic and plastic DIP, 24-pin SOIC, 24-pin Flatpack and CERPACK
- Produced with advanced CEMOS™ technology
- Single 5V (±10%) power supply
- Inputs/outputs TTL-compatible
- Three-state outputs
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7188 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

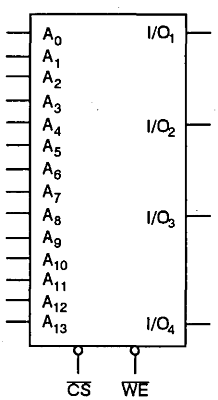
Access times as fast as 15ns are available, with typical power consumption of only 300mW. The IDT7188 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power version (L) version also offers a battery backup data retention capability where the circuit typically consumes only 30μW operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5V supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

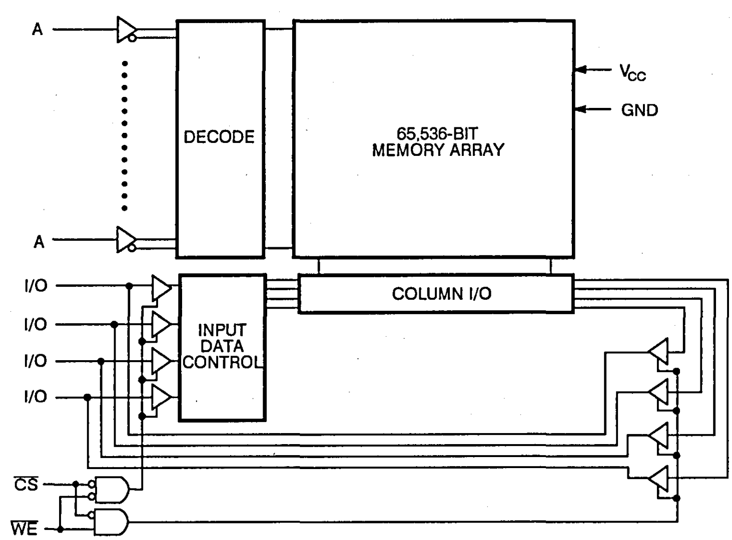
The IDT7188 is packaged in 22-pin, 300 mil ceramic and plastic DIPs, 24-pin SOICs, flatpacks and CERPACKs, providing excellent board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

LOGIC SYMBOL

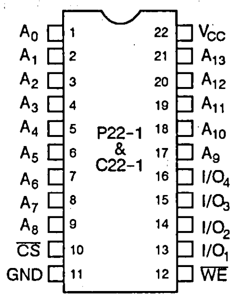


FUNCTIONAL BLOCK DIAGRAM

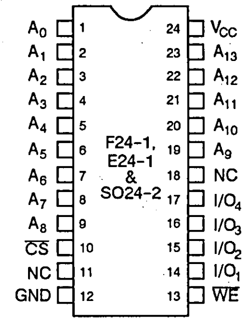


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



FLATPACK/CERPACK/SOIC
TOP VIEW

PIN NAMES

A_0–A_{13}	Address Inputs	I/O_1–I/O_4	Data I/O
$\overline{CS}$	Chip Select	V_{CC}	Power
$\overline{WE}$	Write Enable	GND	Ground

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT7188S MIN.	IDT7188S TYP.(1)	IDT7188S MAX.	IDT7188L MIN.	IDT7188L TYP.(1)	IDT7188L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	POWER	7188S15 7188L15 COM'L.	MIL.	7188S20 7188L20 COM'L.	MIL.	7188S25 7188L25 COM'L.	MIL.	7188S30/35 7188L30/35 COM'L.	MIL.	7188S45/55(3) 7188L45/55(3) COM'L.	MIL.	7188S70 7188L70 COM'L.	MIL.	7188S85 7188L85 COM'L.	MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(2)	S	135	–	120	140	100	125	100	110	100	110	–	110	–	110	mA
		L	115	–	105	125	85	110	85	95	85	95	–	95	–	95	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	S	175	–	150	170	135	155	125	140	125	140	–	140	–	140	mA
		L	160	–	140	155	125	145	115/105	125/115	100	110	–	110	–	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}(2)	S	75	–	60	70	55	60	50/45	55/50	45	50	–	50	–	50	mA
		L	65	–	50	60	45	50	40/35	45/40	30	35	–	35	–	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC} f = 0(2)	S	25	–	20	25	15	20	15	20	15	20	–	20	–	20	mA
		L	2.5	–	1.0	2.0	0.5	1.5	0.5	1.5	0.5	1.5	–	1.5	–	1.5	

NOTES:

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.
3. -55°C to +125°C temperature range only.

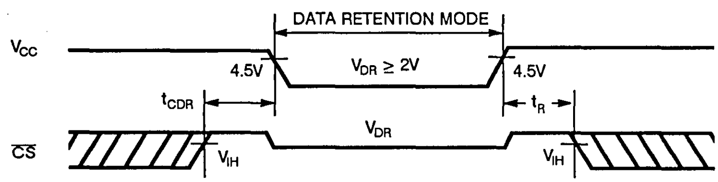
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	10	15	600	900	µA
			COM'L.	–	10	15	150	225	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\lvert I_{LI} \rvert$(3)	Input Leakage Current			–	–		2		µA

NOTES:
1. $T_A = 25°C$
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

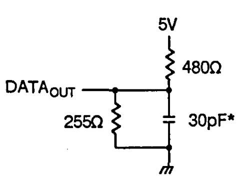


Figure 1. Output Load

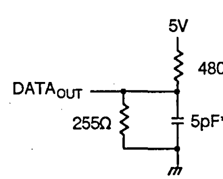


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

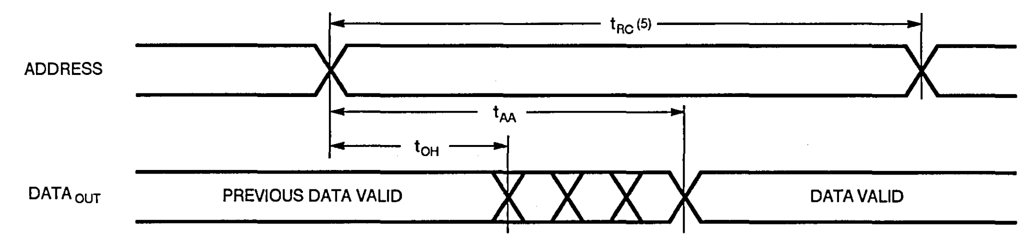
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

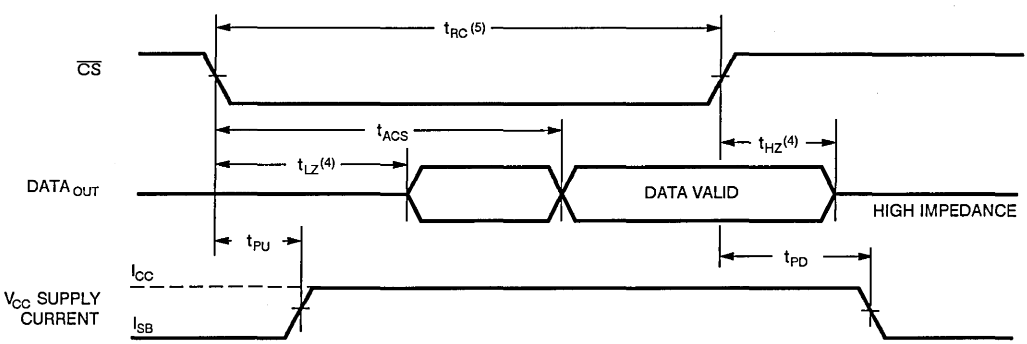
SYMBOL	PARAMETER	7188S15[1] 7188L15[1] MIN.	MAX.	7188S20[4] 7188L20[4] MIN.	MAX.	7188S25/30 7188L25/30 MIN.	MAX.	7188S35/45 7188L35/45 MIN.	MAX.	7188S55/70[2] 7188L55/70[2] MIN.	MAX.	7188S85[2] 7188L85[2] MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	15	–	20	–	25/30	–	35/45	–	55/70	–	85	–	ns
t_{AA}	Address Access Time	–	15	–	20	–	25/30	–	35/45	–	55/70	–	85	ns
t_{ACS}	Chip Select Access Time	–	15	–	20	–	25/30	–	35/45	–	55/70	–	85	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Selection to Output in Low Z[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselect to Output in High Z[3]	–	7	–	8	–	10/13	–	15	–	20/25	–	30	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	15	–	20	–	25/30	–	35/45	–	55/70	–	85	ns

NOTES:
1. 0°C to –70°C temperature range only.
2. –55°C to –125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Preliminary data only for military devices.

TIMING WAVEFORM OF READ CYCLE NO. 1[1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 3]



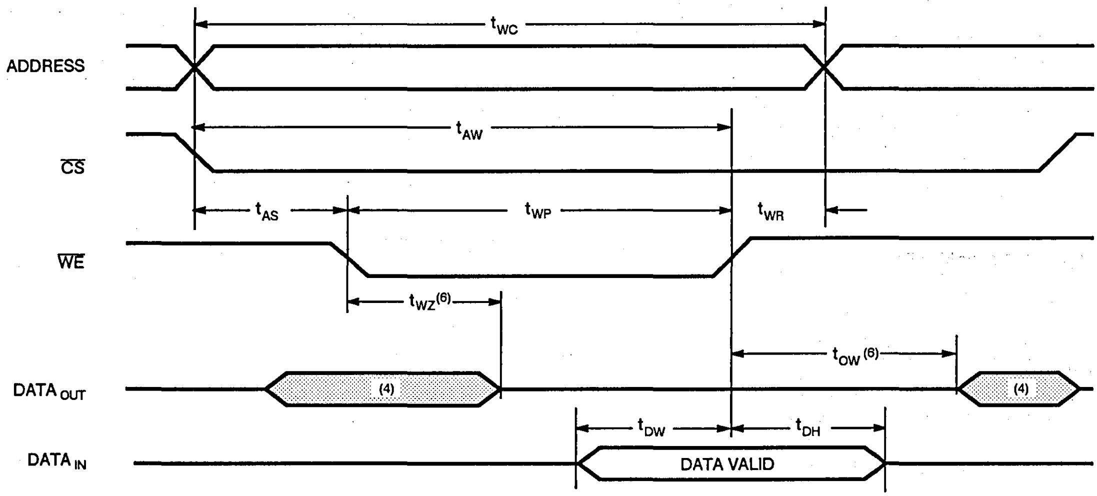
NOTES:
1. $\overline{WE}$ is high for READ Cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

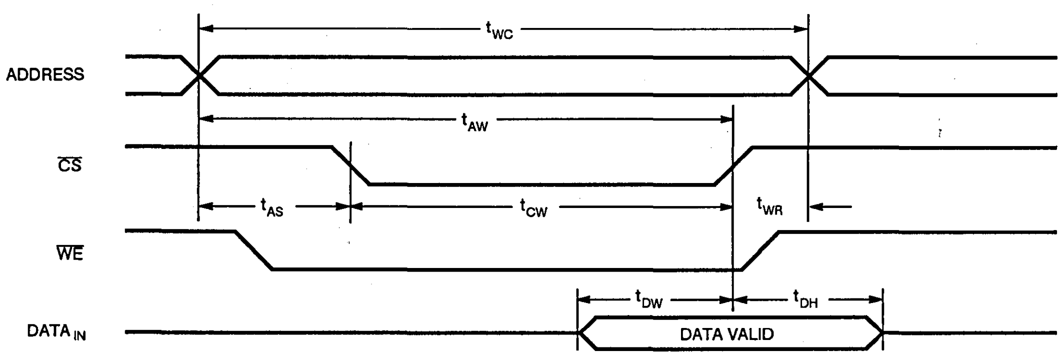
SYMBOL	PARAMETER	7188S15(1) 7188L15(1) MIN.	MAX.	7188S20(4) 7188L20(4) MIN.	MAX.	7188S25/30 7188L25/30 MIN.	MAX.	7188S35/45 7188L35/45 MIN.	MAX.	7188S55/70(2) 7188L55/70(2) MIN.	MAX.	7188S85(2) 7188L85(2) MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	14	–	17	–	20/25	–	30/40	–	50/60	–	75	–	ns
t_{CW}	Chip Select to End of Write	14	–	17	–	20/25	–	25/35	–	50/60	–	75	–	ns
t_{AW}	Address Valid to End of Write	14	–	17	–	20/25	–	25/35	–	50/60	–	75	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	14	–	17	–	20/25	–	25/35	–	50/60	–	75	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	8	–	10	–	13/15	–	15/20	–	25/30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enable to Output in High Z(3)	–	6	–	7	–	7/10	–	10/15	–	25/30	–	40	ns
t_{OW}	Output Active from End of Write(3)	5	–	5	–	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to -70°C temperature range only.
2. -55°C to -125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Preliminary data only for military devices.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals should not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200 mV from steady state.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	I/O	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

ORDERING INFORMATION

IDT XXXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/ Temperature Range)

Process/Temperature Range:

- Blank — Commercial (0°C to +70°C)
- B — Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

- P — Plastic DIP
- C — Sidebraze DIP
- SO — Small Outline IC (Gull Wing)
- Y — Small Outline IC (J-Bend)
- F — Flatpack
- E — CERPACK

Speed (Speed in Nanoseconds):

- 15 — Commercial Only
- 20
- 25
- 30
- 35
- 45
- 55 — Military Only
- 70 — Military Only
- 85 — Military Only

Power:

- S — Standard Power
- L — Low Power

Device Type:

- 7188 — 64K (16K x 4-Bit)

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (16K x 4-BIT)

IDT6198S IDT6198L

FEATURES:

- Output Enable ($\overline{OE}$) pin available for added system flexibility
- High-speed (equal access and cycle times)
  - Military: 20/25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/20/25/30/35/45ns (max.)
- Low-power consumption
  - IDT6198S
    Active: 350mW (typ.)
    Standby: 100μW (typ.)
  - IDT6198L
    Active: 300mW (typ.)
    Standby: 30μW (typ.)
- JEDEC compatible pinout
- Battery back-up operation—2V data retention (L version only)
- 24-pin THINDIP, 24-pin plastic DIP, high-density 28-pin leadless chip carrier and 24-pin SOIC
- Produced with advanced CEMOS™ technology
- Bidirectional data inputs and outputs
- Inputs/Outputs TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT6198 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for memory intensive applications.

The IDT6198 features two memory control functions: chip select ($\overline{CS}$) and output enable ($\overline{OE}$). These two functions greatly enhance the IDT6198's overall flexibility in high-speed memory applications.

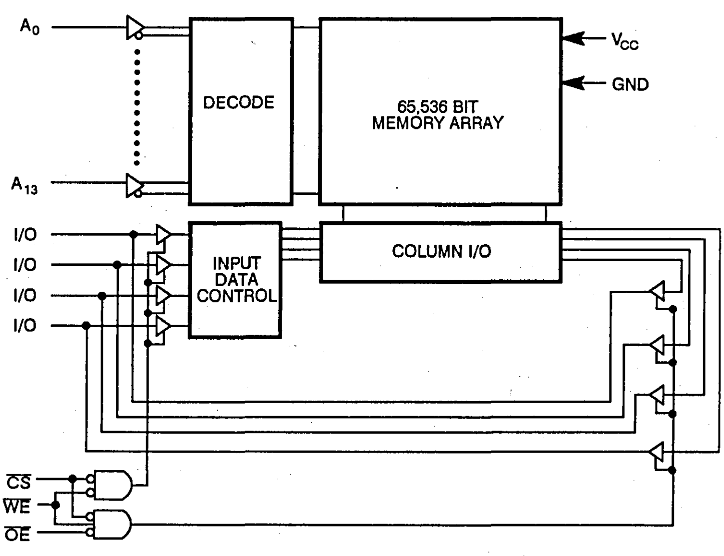
Access times as fast as 15ns are available, with typical power consumption of only 300mW. The IDT6198 offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 30μW when operating from a 2 volt battery.

All inputs and outputs are a TTL-compatible and operate from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT6198 is packaged in either a 24-pin THINDIP, 24-pin plastic DIP, 28-pin leadless chip carrier or 24-pin small outline IC, providing improved board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

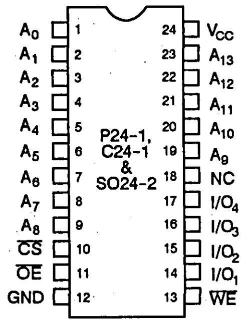
FUNCTIONAL BLOCK DIAGRAM



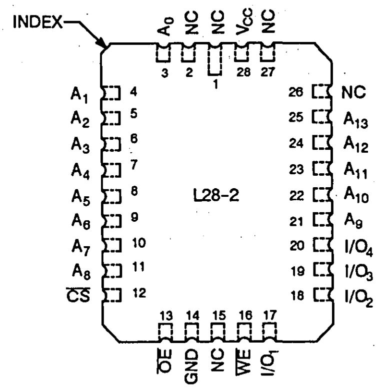
CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES — DECEMBER 1987

PIN CONFIGURATIONS

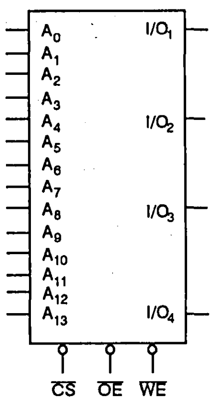


DIP/SOIC
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_{0-13}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_{1-4}	Data Input/Output
V_{CC}	Power
GND	Ground

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} min. = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6198S MIN.	IDT6198S TYP.(1)	IDT6198S MAX.	IDT6198L MIN.	IDT6198L TYP.(1)	IDT6198L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	6198S15(2, 5) 6198L15(2, 5) COM'L.	MIL.	6198S20(2) 6198L20(2) COM'L.	MIL.	6198S25 6198L25 COM'L.	MIL.	6198S30/35 6198L30/35 COM'L.	MIL.	6198S45/55(4) 6198L45/55(4) COM'L.	MIL.	6198S70(4)/85(4) 6198L70(4)/85(4) COM'L.	MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(3)	S	135	–	120	140	100	125	100	110	100	110	–	110	mA
		L	115	–	105	125	85	110	85	95	85	95	–	95	
I_{CC2}	Dynamic Operating Current, $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	S	175	–	150	170	135	155	125	140	125	140	–	140	mA
		L	160	–	140	155	125	145	115/105	125/115	100	110	–	110/105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}(3)	S	75	–	60	70	55	60	50/45	55/50	45	50	–	50	mA
		L	65	–	50	60	45	50	40/35	45/40	30	35	–	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(3)	S	25	–	20	25	15	20	15	20	15	20	–	20	mA
		L	2.5	–	1.0	2.0	0.5	1.5	0.5	1.5	0.5	1.5	–	1.5	

NOTES:
1. All values are maximum guaranteed values.
2. Preliminary data for Military devices only.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. -55°C to +125°C temperature range only.
5. 0°C to +70°C temperature range only.

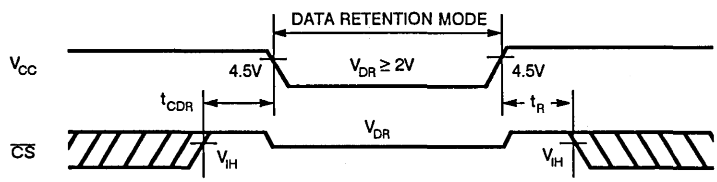
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	10	15	600	900	μA
			COM'L.	–	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\lvert I_{LI} \rvert$(3)	Input Leakage Current			–	–		2		μA

NOTES:
1. $T_A = +25°C$
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

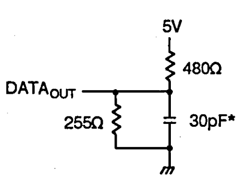


Figure 1. Output Load

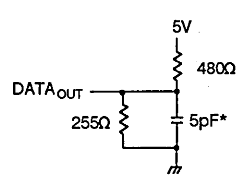


Figure 2. Output Load (for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, t_{OW})

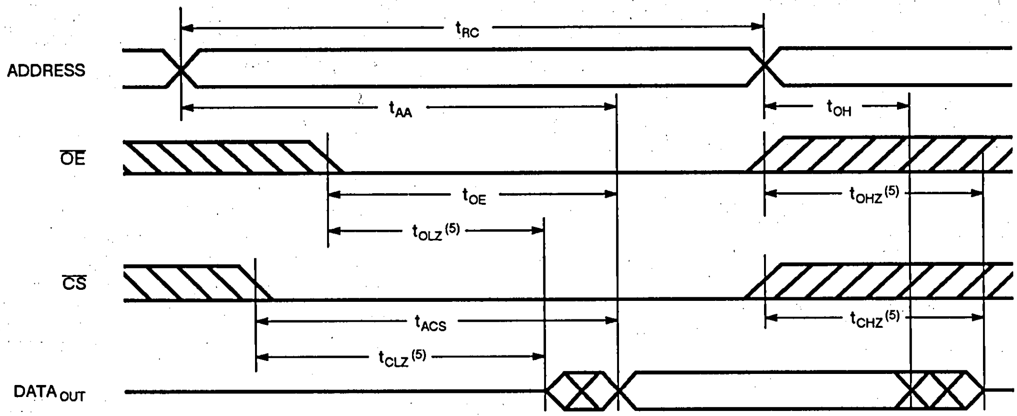
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

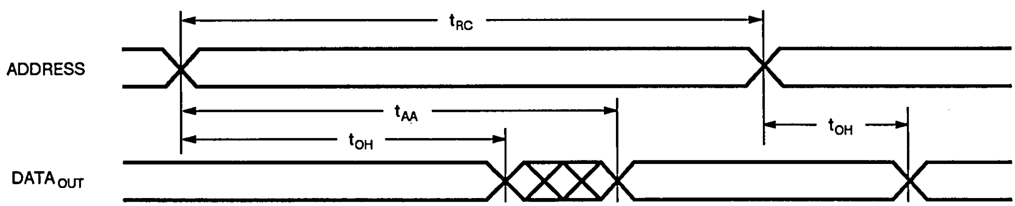
SYMBOL	PARAMETER	6198S15(1) 6198L15(1)		6198S20 6198L20		6198S25 6198L25		6198S30/35 6198L30/35		6198S45/55(2) 6198L45/55(2)		6198S70(2)/85(2) 6198L70(2)/85(2)		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	15	–	20	–	25	–	30/35	–	45/55	–	70/85	–	ns
t_{AA}	Address Access Time	–	15	–	20	–	25	–	30/35	–	45/55	–	70/85	ns
t_{ACS}	Chip Select Access Time	–	15	–	20	–	25	–	30/35	–	45/55	–	70/85	ns
t_{CLZ}	Chip Select to Output in Low Z(3)	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	12	–	15	–	15	–	20	–	25/35	–	45/55	ns
t_{OLZ}	Output Enable to Output in Low Z(3)	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Select to Output in High Z(3)	–	7	–	8	–	10	–	13/15	–	15/20	–	25/30	ns
t_{OHZ}	Output Disable to Output in High Z(3)	–	7	–	8	–	15	–	15	–	15/20	–	25/30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time(3)	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time(3)	–	15	–	20	–	25	–	30/35	–	45/55	–	70/85	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.

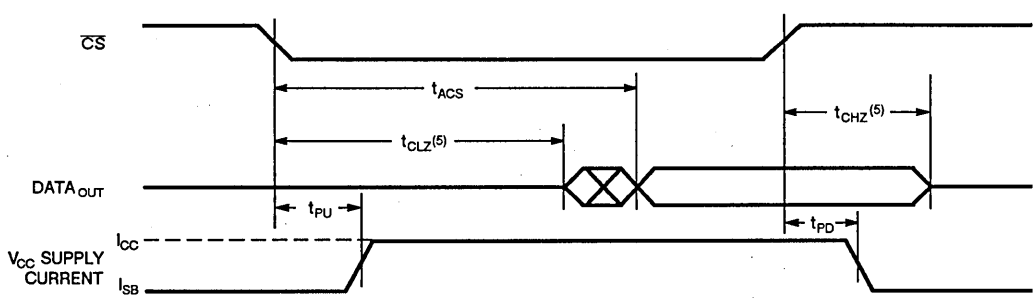
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.

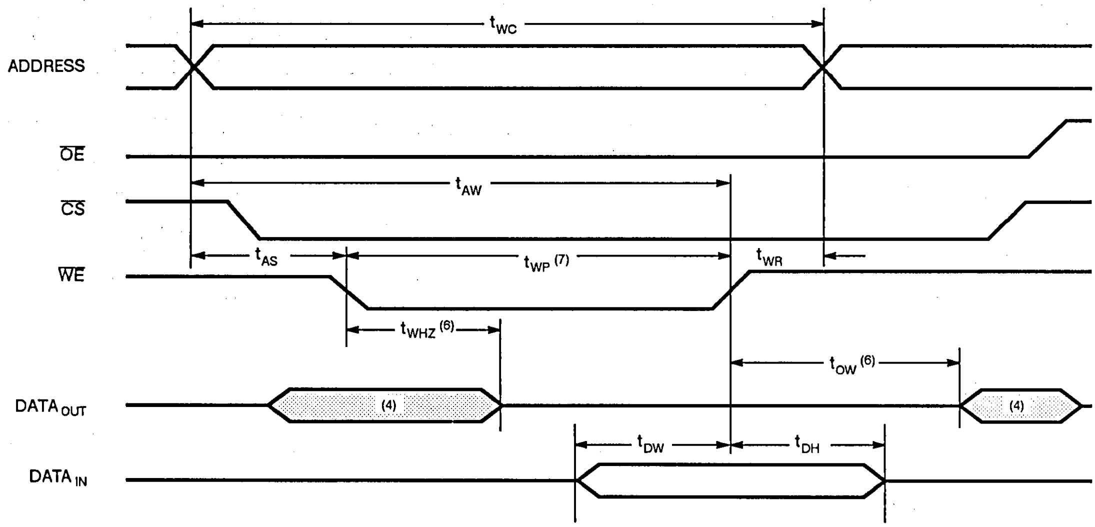
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6198S15[1] 6198L15[1] MIN.	MAX.	6198S20[4] 6198L20[4] MIN.	MAX.	6198S25 6198L25 MIN.	MAX.	6198S30/35 6198L30/35 MIN.	MAX.	6198S45/55[2] 6198L45/55[2] MIN.	MAX.	6198S70[2]/85[2] 6198L70[2]/85[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	14	–	17	–	20	–	25/30	–	40/50	–	60/75	–	ns
t_{CW}	Chip Select to End of Write	14	–	17	–	20	–	25	–	35/50	–	60/75	–	ns
t_{AW}	Address Valid to End of Write	14	–	17	–	20	–	25	–	35/50	–	60/75	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	14	–	17	–	20	–	25	–	35/50	–	60/75	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output in High Z[3]	–	6	–	7	–	7	–	10	–	15/25	–	30/40	ns
t_{DW}	Data Valid to End of Write	8	–	10	–	13	–	15	–	20/25	–	30/35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns

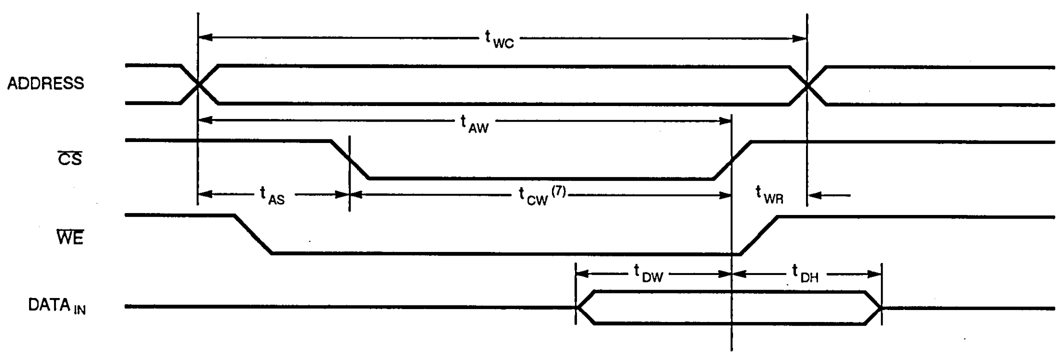
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Preliminary data only for military devices.

4

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5, 8)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200 mV from steady state.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. $\overline{OE} = V_{IH}$

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	POWER
Standby	H	X	X	High Z	Standby
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active
Read	L	H	H	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/ Temperature Range)

Process/Temperature Range:

- Blank — Commercial (0°C to +70°C)
- B — Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

- C — Sidebraze THINDIP (300 mil.)
- P — Plastic DIP
- L — Leadless Chip Carrier
- SO — Small Outline IC (Gull Wing)
- Y — Small Outline IC (J-bend)

Speed (Speed in Nanoseconds):

- 15 — Commercial Only
- 20
- 25
- 30
- 35
- 45
- 55 — Military Only
- 70 — Military Only
- 85 — Military Only

Power:

- S — Standard Power
- L — Low Power

Device Type:

- 6198 — 16K x 4-Bit

Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (16K x 4-BIT)

IDT7198S
IDT7198L

Added Chip Select and Output Enable Controls

FEATURES:

- Fast Output Enable ($\overline{OE}$) pin available for added system flexibility
- Multiple Chip Selects ($\overline{CS}_1$, $\overline{CS}_2$) simplify system design and operation
- High speed (equal access and cycle times)
  - Military: 20/25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT7198S
    Active: 350mW (typ.)
    Standby: 100μw (typ.)
  - IDT7198L
    Active: 300mW (typ.)
    Standby: 30μw (typ.)
- Battery back-up operation—2V data retention (L version only)
- 24-pin THINDIP, 24-pin plastic DIP, high-density 28-pin leadless chip carrier, 24-pin SOIC, flatpack and CERPACK
- Produced with advanced CEMOS™ technology
- Bidirectional data inputs and outputs
- Inputs/outputs TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86859 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT7198 is a 65,536 bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

The IDT7198 features three memory control functions: Chip Select 1 ($\overline{CS}_1$), Chip Select 2 ($\overline{CS}_2$) and Output Enable ($\overline{OE}$). These three functions greatly enhance the IDT7198's overall flexibility in high-speed memory applications.

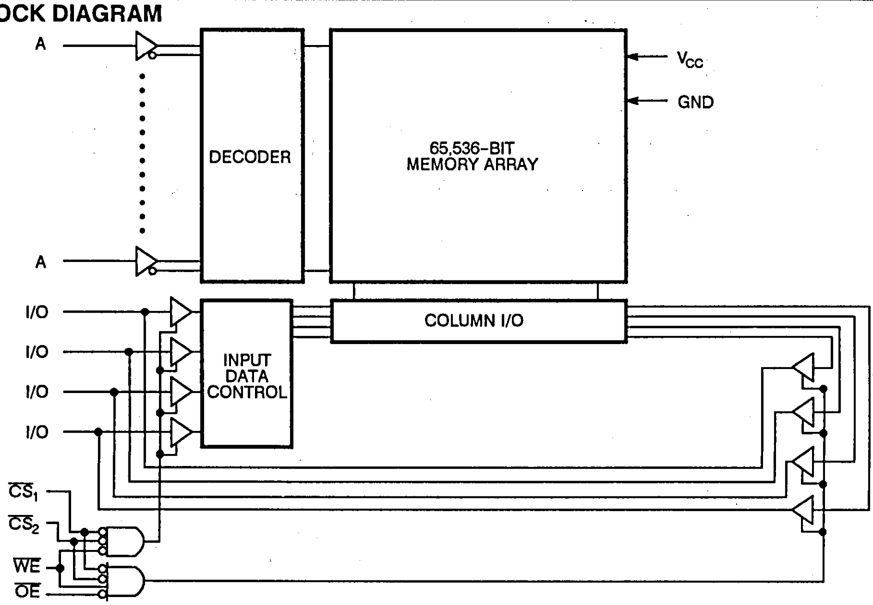
Access times as fast as 15ns are available, with typical power consumption of only 300mW. The IDT7198 offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 30μW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT7198 is packaged in either a 24-pin ceramic DIP, 24-pin plastic DIP, 28-pin leadless chip carrier, 24-pin SOIC and 24-pin flatpack or CERPACK, providing improved board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

MEMORY CONTROL:

The IDT7198 64K high-speed CEMOS static RAM incorporates two additional memory control features (an extra chip select and an output enable pin) which offer additional benefits in many system memory applications.

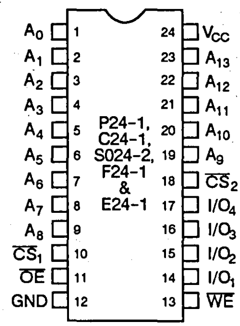
The dual chip select feature ($\overline{CS}_1$, $\overline{CS}_2$) now brings the convenience of improved system speeds to the large memory designer by reducing the external logic required to perform decoding. Since external decoding logic is reduced, board space is saved, system speed is enhanced by approximately 10-20ns and system reliability improves as a result of lower parts count. (See technical note 1 "Using Two Chip Selects on the IDT7198.")

Both chip selects, Chip Select 1 ($\overline{CS}_1$) and Chip Select 2 ($\overline{CS}_2$), must be in the active-low state to select the memory. If either chip select is pulled high, the memory will be deselected and remain in the standby mode.

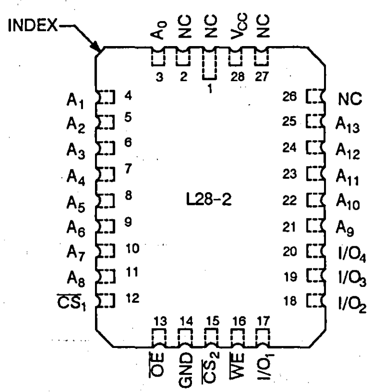
The fast output enable function ($\overline{OE}$) is also a highly desirable feature of the IDT7198 high-speed common I/O static RAM. This function is designed to eliminate problems associated with data bus contention by allowing the data outputs to be controlled independent of either chip select. Its speed permits further decreases in overall read cycle timing.

These added memory control features provide improved system design flexibility, along with overall system speed performance enhancements.

PIN CONFIGURATION

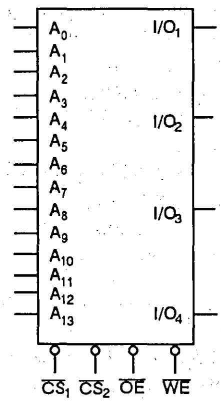


DIP/SOIC/FLATPACK/CERPACK
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0-A_{13}	Address Inputs	$\overline{OE}$	Output Enable
$\overline{CS}_1$	Chip Select 1	I/O_1 - I/O_4	Data I/O
$\overline{CS}_2$	Chip Select 2	V_{CC}	Power
$\overline{WE}$	Write Enable	GND	Ground

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT7198S MIN.	IDT7198S TYP.[1]	IDT7198S MAX.	IDT7198L MIN.	IDT7198L TYP.[1]	IDT7198L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	POWER	7198S15 7198L15 COM'L	MIL.	7198S20 7198L20 COM'L	MIL.	7198S25 7198L25 COM'L	MIL.	7198S30/35 7198L30/35 COM'L	MIL.	7198S45/55[3] 7198L45/55[3] COM'L	MIL.	7198S70[3] 7198L70[3] COM'L	MIL.	7198S85[3] 7198L85[3] COM'L	MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS} = V_{IL}$, Outputs Open V_{CC} = Max., f = 0[2]	S	135	–	120	140	100	125	100	110	100	110	–	110	–	110	mA
		L	115	–	105	125	85	110	85	95	85	95	–	95	–	95	
I_{CC2}	Dynamic Operating Current $\overline{CS} = V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	S	175	–	150	170	135	155	125	140	125	140	–	140	–	140	mA
		L	160	–	140	155	125	145	115/105	125/115	100	110	–	110	–	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open f = f_{MAX}[2]	S	75	–	60	70	55	60	50/45	55/50	45	50	–	50	–	50	mA
		L	65	–	50	60	45	50	40/35	45/40	30	35	–	35	–	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0[2]	S	25	–	20	25	15	20	15	20	15	20	–	20	–	20	mA
		L	2.5	–	1.0	2.0	0.5	1.5	0.5	1.5	0.5	1.5	–	1.5	–	1.5	

NOTES:

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
3. –55°C to +125°C temperature range only.

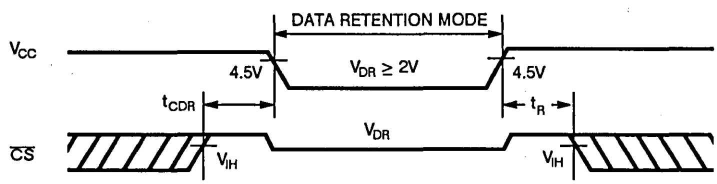
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.[1] V_{CC} @ 2.0V	TYP.[1] V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$, $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	10	15	600	900	µA
			COM'L.	–	10	15	150	225	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–		–		ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–		–		ns
$\|I_{LI}\|$[3]	Input Leakage Current			–	–		2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

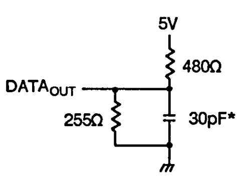


Figure 1. Output Load

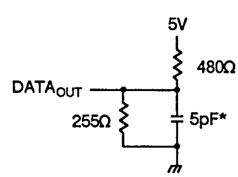


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

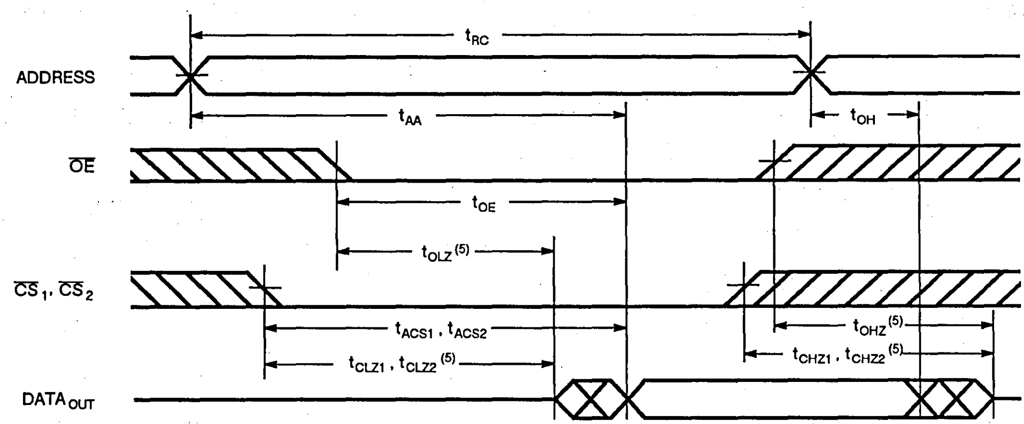
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7198S15(1)/20(5) 7198L15(1)/20(5) MIN.	MAX.	7198S25/30 7198L25/30 MIN.	MAX.	7198S35/45 7198L35/45 MIN.	MAX.	7198S55(2) 7198L55(2) MIN.	MAX.	7198S70(2) 7198L70(2) MIN.	MAX.	7198S85(2) 7198L85(2) MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	15/20	–	25/30	–	35/45	–	55	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	15/20	–	25/30	–	35/45	–	55	–	70	–	85	ns
$t_{ACS1,2}$	Chip Select-1, 2 Access Time (3)	–	15/20	–	25/30	–	35/45	–	55	–	70	–	85	ns
$t_{CLZ1,2}$	Chip Select-1, 2 to Output in Low Z(4)	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	12/15	–	15/20	–	20/25	–	35	–	45	–	55	ns
t_{OLZ}	Output Enable to Output in Low Z(4)	5	–	5	–	5	–	5	–	5	–	5	–	ns
$t_{CHZ1,2}$	Chip Select-1, 2 to Output in High Z(4)	–	7/8	–	10/13	–	15	–	20	–	25	–	30	ns
t_{OHZ}	Output Disable to Output in High Z(4)	–	7/8	–	15	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time (4)	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time(4)	–	15/20	–	25/30	–	35/45	–	55	–	70	–	85	ns

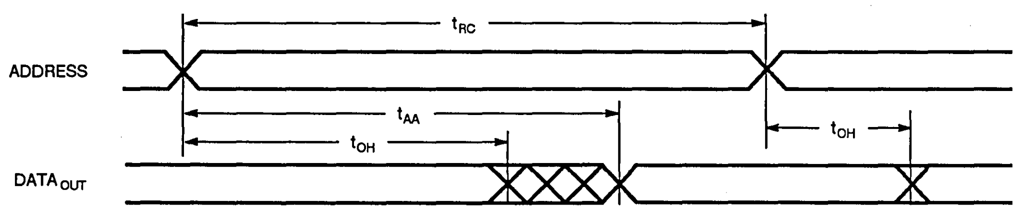
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.
5. Preliminary data only for military devices.

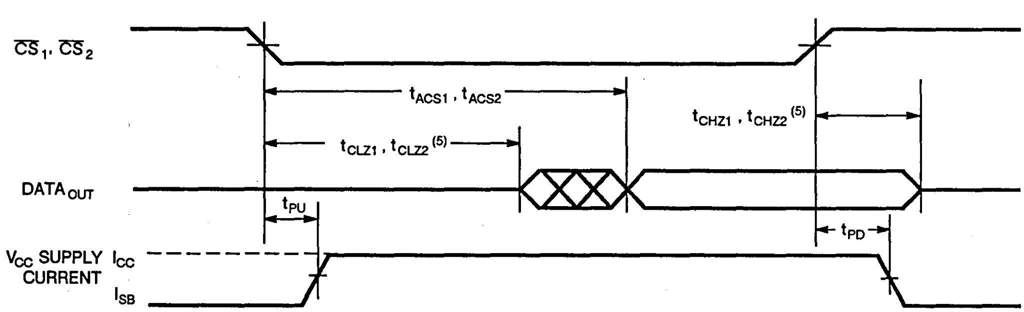
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 3 [1, 3, 4]



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $\overline{CS}_2 = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ and or $\overline{CS}_2$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.

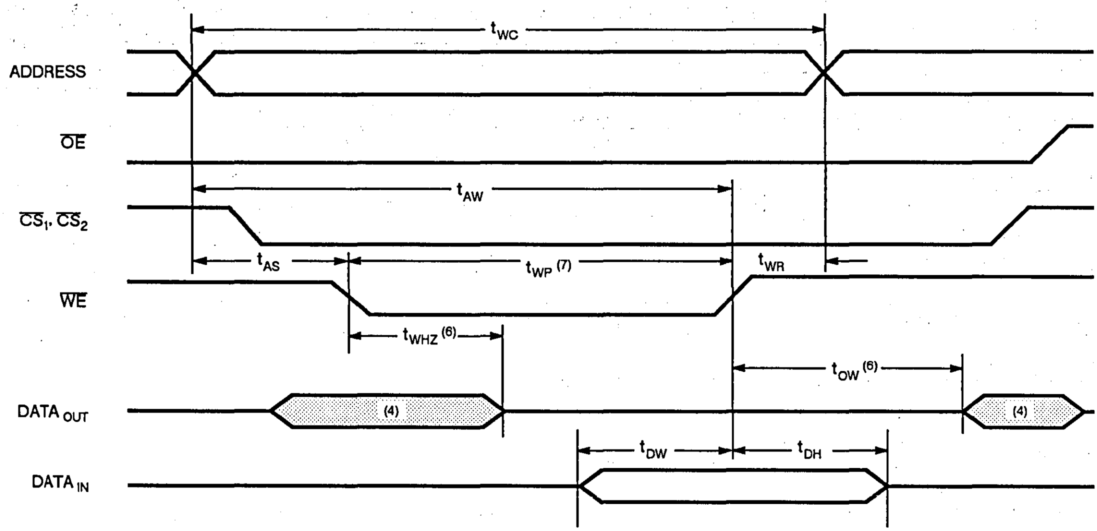
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7198S15[1]/20[5] 7198L15[1]/20[5] MIN.	MAX.	7198S25/30 7198L25/30 MIN.	MAX.	7198S35/45 7198L35/45 MIN.	MAX.	7198S55[2] 7198L55[2] MIN.	MAX.	7198S70[2] 7198L70[2] MIN.	MAX.	7198S85[2] 7198L85[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	13/17	–	20/25	–	30/40	–	50	–	60	–	75	–	ns
$t_{CW1,2}$	Chip Select to End of Write [3]	13/17	–	20/25	–	25/35	–	50	–	60	–	75	–	ns
t_{AW}	Address Valid to End of Write	13/17	–	20/25	–	25/35	–	50	–	60	–	75	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	13/17	–	20/25	–	25/35	–	50	–	60	–	75	–	ns
$t_{WR1,2}$	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output High Z [4]	–	6/7	–	7/10	–	10/15	–	25	–	30	–	40	ns
t_{DW}	Data Valid to End of Write	8/10	–	13/15	–	15/20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write [4]	5	–	5	–	5	–	5	–	5	–	5	–	ns

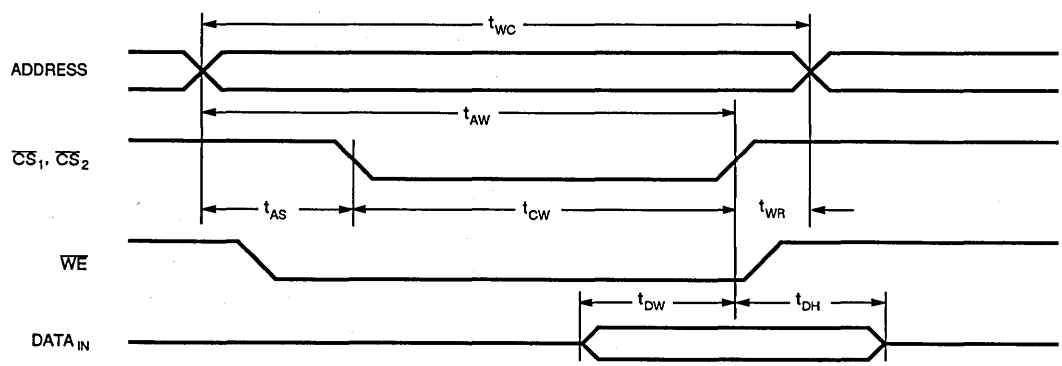
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.
5. Preliminary data only for military devices.

4

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5, 8)



NOTES:

1. $\overline{WE}$, $\overline{CS}_1$ or $\overline{CS}_2$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}_1$, a low $\overline{CS}_2$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}_1$, $\overline{CS}_2$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. $\overline{OE}$ = V_{IH}

TRUTH TABLE

MODE	$\overline{CS_1}$	$\overline{CS_2}$	$\overline{WE}$	$\overline{OE}$	I/O	POWER
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	D_{OUT}	Active
Write	L	L	L	X	D_{IN}	Active
Read	L	L	H	H	High Z	Active

CAPACITANCE ($T_A = +25°C$, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	7	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	7	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

4

ORDERING INFORMATION

IDT XXXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range

Blank	Commercial (0°C to +70°C)	
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B	

Package

P	Plastic DIP
C	Sidebraze DIP
L	Leadless Chip Carrier
SO	Small Outline IC (Gull Wing)
Y	Small Outline IC (J-bend)
E	CERPACK
F	Flatpack

Speed (Speed in Nanoseconds)

15	Commercial Only
20	
25	
30	
35	
45	
55	Military Only
70	Military Only
85	Military Only

Power

S	Standard Power
L	Low Power

Device Type

7198	64K (16K x 4-Bit)

Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (16K x 4-BIT)
Separate Data Inputs and Outputs

IDT71981S/L
IDT71982S/L

FEATURES:

- Separate data inputs and outputs
- IDT71981S/L: outputs track inputs during write mode
- IDT71982S/L: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - Military: 20/25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT71981/2S
    Active: 350mW (typ.)
    Standby: 100μw (typ.)
  - IDT71981/2L
    Active: 300mW (typ.)
    Standby: 30μw (typ.)
- Battery backup operation—2V data retention (L version only)
- High-density 28-pin hermetic and plastic DIP, 28-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71981/IDT71982 are 65,536-bit high-speed static RAMs organized as 16K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

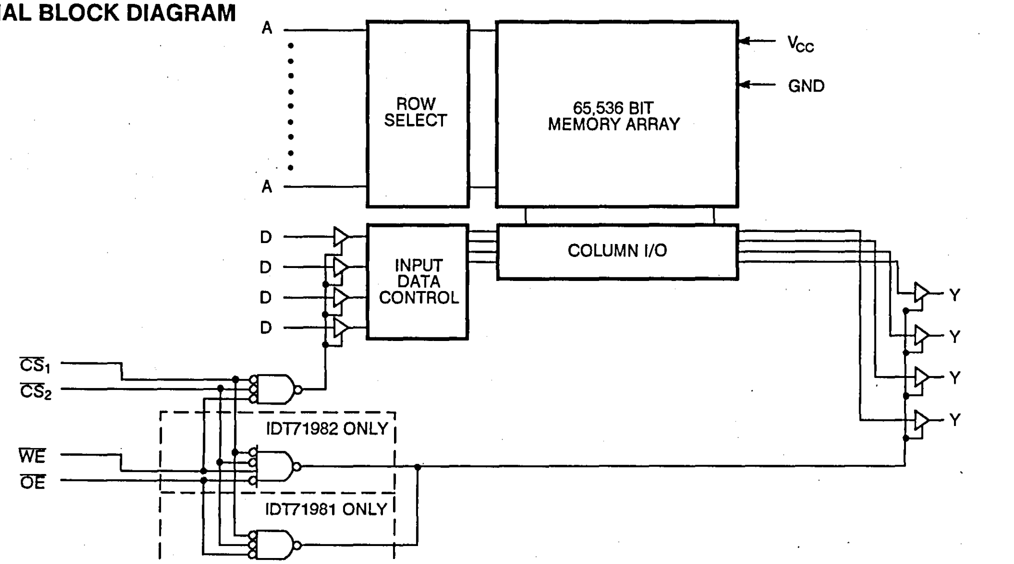
Access times as fast as 15ns are available with typical power consumption of only 300mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}_1$ goes high, the circuit will automatically go to, and remain in, this standby mode. In the ultra-low-power standby mode (I_{SB1}), the devices consume less than 2.5mW, typically. This capability provides significant system-level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 30μW operating off a 2V battery.

All inputs and outputs of the IDT71981/IDT71982 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT71981/IDT71982 are packaged in either space-saving 28-pin, 400 mil hermetic DIPs, 28-pin 300 mil plastic DIPs or 28-pin leadless chip carriers, providing high board-level packing densities.

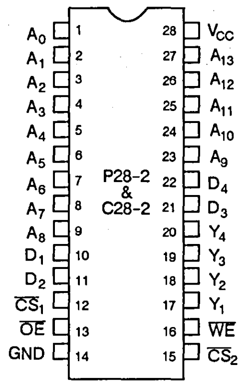
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

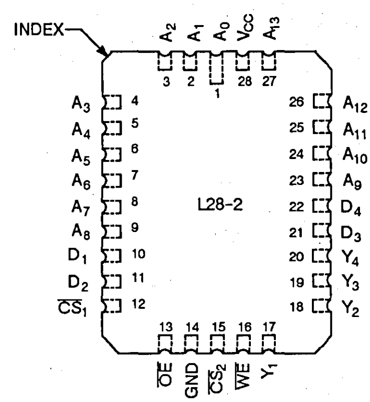


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

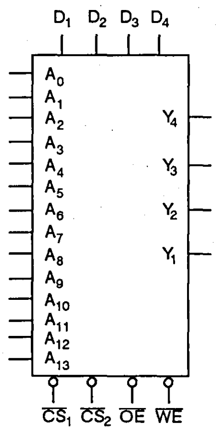


DIP
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



4

PIN NAMES

A_0–A_{13}	Address Inputs	D_1–D_4	$DATA_{IN}$
$\overline{CS}_1$, $\overline{CS}_2$	Chip Selects	Y_1–Y_4	$DATA_{OUT}$
$\overline{WE}$	Write Enable	GND	Ground
$\overline{OE}$	Output Enable	V_{CC}	Power

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT71981/2S MIN.	IDT71981/2S TYP.(1)	IDT71981/2S MAX.	IDT71981/2L MIN.	IDT71981/2L TYP.(1)	IDT71981/2L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OL} = –4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	71981/2S15 71981/2L15 COM'L.	71981/2S15 71981/2L15 MIL.	71981/2S20 71981/2L20 COM'L.	71981/2S20 71981/2L20 MIL.	71981/2S25 71981/2L25 COM'L.	71981/2S25 71981/2L25 MIL.	71981/2S30/35 71981/2L30/35 COM'L.	71981/2S30/35 71981/2L30/35 MIL.	71981/2S45/55(3) 71981/2L45/55(3) COM'L.	71981/2S45/55(3) 71981/2L45/55(3) MIL.	71981/2S70 71981/2L70 COM'L.	71981/2S70 71981/2L70 MIL.	71981/2S85 71981/2L85 COM'L.	71981/2S85 71981/2L85 MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(2)	S	135	–	120	140	100	125	100	110	100	110	–	110	–	110	mA
		L	115	–	105	125	85	110	85	95	85	95	–	95	–	95	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	S	175	–	150	170	135	155	125	140	125	140	–	140	–	140	mA
		L	160	–	140	155	125	145	115/105	125/115	100	110	–	110	–	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IL}, V_{CC} = Max., Outputs Open f = f_{MAX}(2)	S	75	–	60	70	55	60	50/45	55/50	45	50	–	50	–	50	mA
		L	65	–	50	60	45	50	40/35	45/40	30	35	–	35	–	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(2)	S	25	–	20	25	15	20	15	20	15	20	–	20	–	20	mA
		L	2.5	–	1.0	2.0	0.5	1.5	0.5	1.5	0.5	1.5	–	1.5	–	1.5	

NOTES:

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
3. –55°C to +125°C temperature range only.

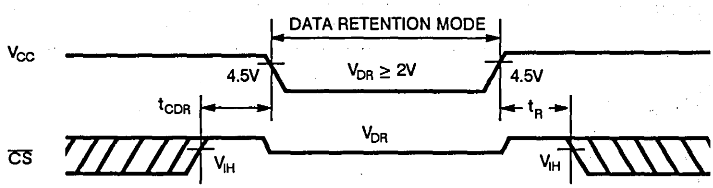
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.[1] V_{CC} @ 2.0V	TYP.[1] V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current		MIL.	–	10	15	600	900	µA
			COM'L.	–	10	15	150	225	
t_{CDR}[3]	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		0	–		–		ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–		–		ns
$\lvert I_{LI} \rvert$[3]	Input Leakage Current			–	–		2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

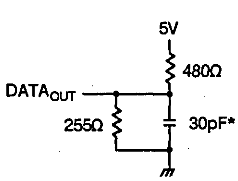


Figure 1. Output Load

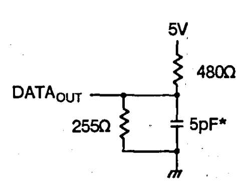


Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

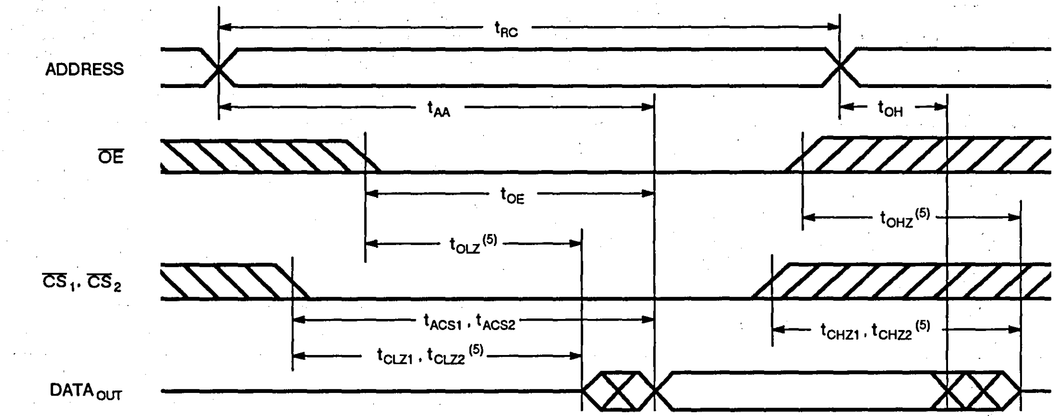
4

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

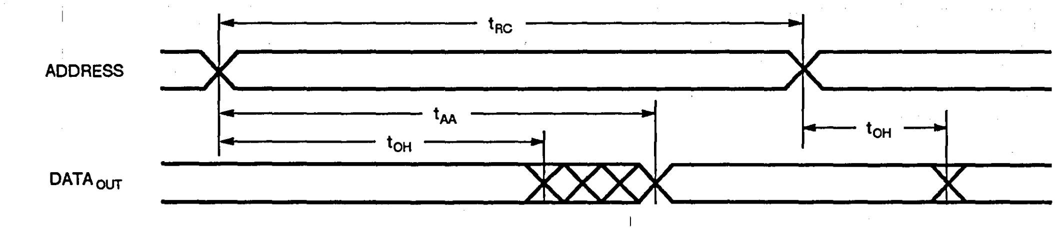
SYMBOL	PARAMETER	71981/2S15[1]/20 71981/2L15[1]/20 MIN.	MAX.	71981/2S25/30 71981/2L25/30 MIN.	MAX.	71981/2S35/45 71981/2L35/45 MIN.	MAX.	71981/2S55[2] 71981/2L55[2] MIN.	MAX.	71981/2S70[2] 71981/2L70[2] MIN.	MAX.	71981/2S85[2] 71981/2L85[2] MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	15/20	–	25/30	–	35/45	–	55	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	15/20	–	25/30	–	35/45	–	55	–	70	–	85	ns
$t_{ACS1,2}$	Chip Select-1, 2 Access Time [3]	–	15/20	–	25/30	–	35/45	–	55	–	70	–	85	ns
$t_{CLZ1,2}$	Chip Select-1, 2 to Output in Low Z [4]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	12/15	–	15/20	–	20/25	–	35	–	45	–	55	ns
t_{OLZ}	Output Enable to Output in Low Z [4]	5	–	5	–	5	–	5	–	5	–	5	–	ns
$t_{CHZ1,2}$	Chip Select-1, 2 to Output in High Z [4]	–	7/8	–	10/13	–	15	–	20	–	25	–	30	ns
t_{OHZ}	Output Disable to Output in High Z [4]	–	7/8	–	15	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time [4]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time [4]	–	15/20	–	25/30	–	35/45	–	55	–	70	–	85	ns

NOTES:
1. 0°C to +70°C temperature range only. Data for 20ns devices is preliminary for military temperature range.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.

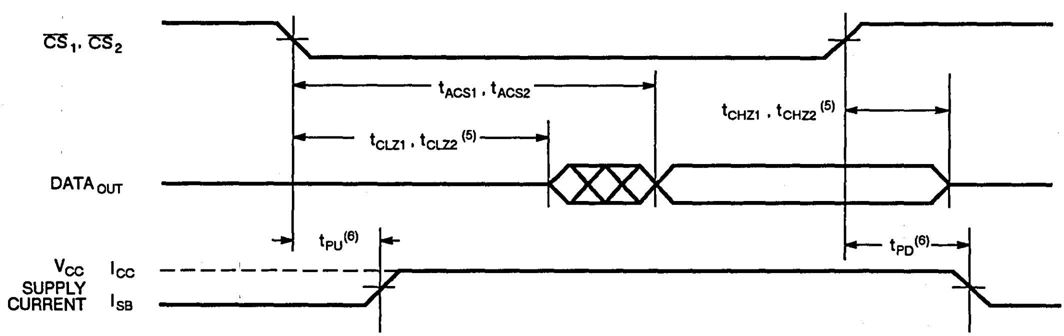
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

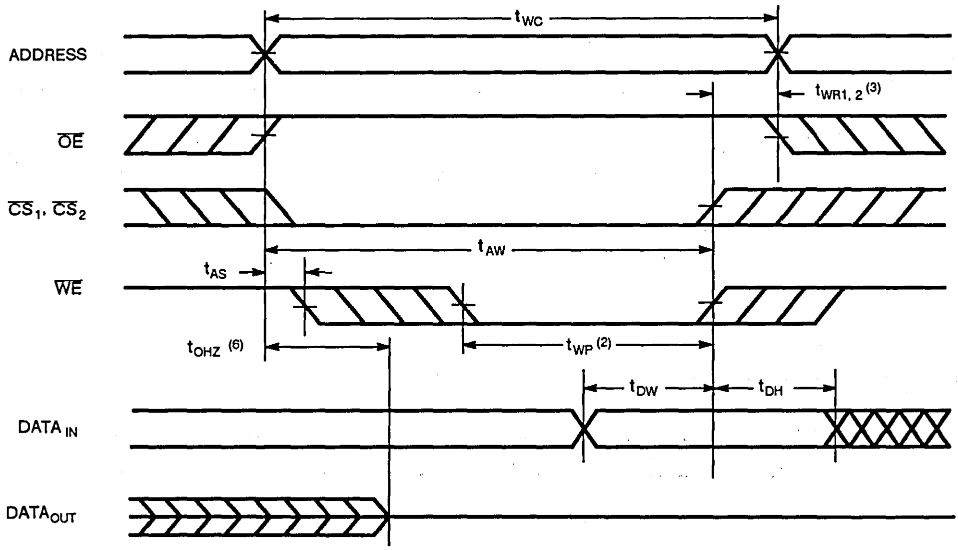
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $\overline{CS}_2 = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}_1$, and or $\overline{CS}_2$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.
6. This parameter is guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

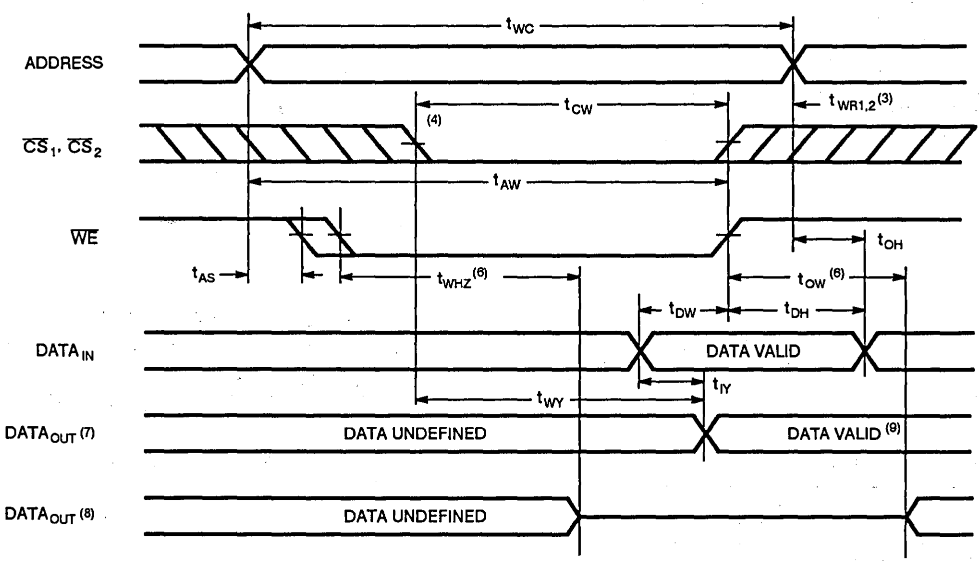
SYMBOL	PARAMETER	71981/2S15[1]/20 71981/2L15[1]/20 MIN.	MAX.	71981/2S25/30 71981/2L25/30 MIN.	MAX.	71981/2S35/45 71981/2L35/45 MIN.	MAX.	71981/2S55[2] 71981/2L55[2] MIN.	MAX.	71981/2S70[2] 71981/2L70[2] MIN.	MAX.	71981/2S85[2] 71981/2L85[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	13/17	–	20/25	–	30/40	–	50	–	60	–	75	–	ns
$t_{CW1, 2}$	Chip Select to End of Write	13/17	–	20/25	–	25/35	–	50	–	60	–	75	–	ns
t_{AW}	Address Valid to End of Write	13/17	–	20/25	–	25/35	–	50	–	60	–	75	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	13/17	–	20/25	–	25/35	–	50	–	60	–	75	–	ns
$t_{WR1, 2}$	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output High Z [3, 5]	–	6/7	–	7/10	–	10/15	–	25	–	30	–	40	ns
t_{DW}	Data Valid to End of Write	8/10	–	13/15	–	15/20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write [3, 5]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{IY}	Data Valid to Output Valid [3, 4]	–	12/15	–	20/25	–	30/35	–	40	–	45	–	50	ns
t_{WY}	Write Enable to Output Valid [3, 4]	–	12/15	–	20/25	–	30/35	–	40	–	45	–	50	ns

NOTES:
1. 0°C to +70°C temperature range only. Data for 20ns devices is preliminary for military temperature range.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. For IDT71981S/L only.
5. For IDT71982S/L only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING) (1)

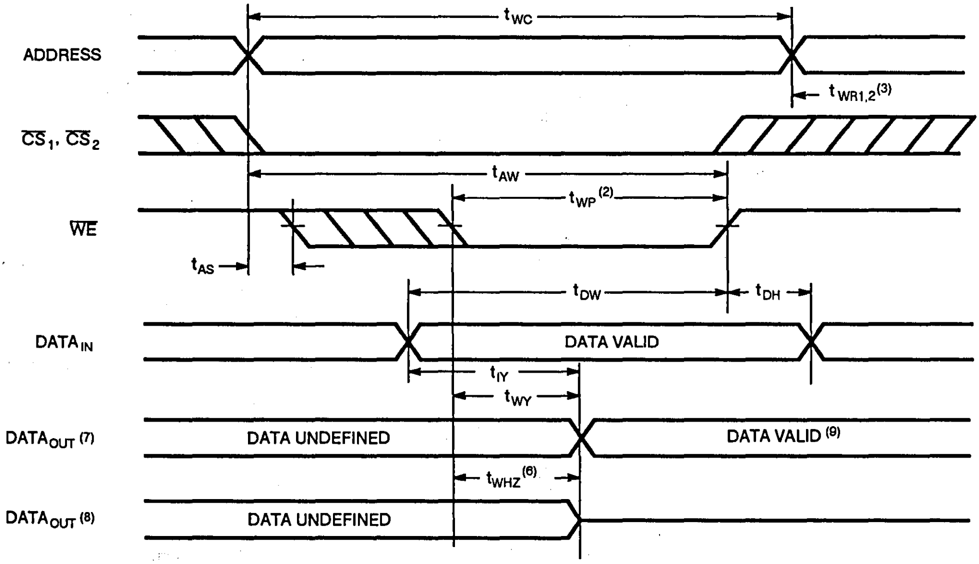


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) (1, 5)



4

TIMING WAVEFORM OF WRITE CYCLE NO. 3 ($\overline{WE}$ CONTROLLED, $\overline{OE}$ LOW) (1, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}_1$, or $\overline{CS}_2$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{WE}$, a low $\overline{CS}_1$ and a low $\overline{CS}_2$.
3. t_{WR} is measured from the earlier of $\overline{CS}_1$, $\overline{CS}_2$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}_1$ and or $\overline{CS}_2$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
6. Transition is measured ±200mV from steady state.
7. For IDT71981 only.
8. For IDT71982 only.
9. $DATA_{OUT}$ = $DATA_{IN}$

TRUTH TABLE

MODE	$\overline{CS}_1$	$\overline{CS}_2$	$\overline{WE}$	$\overline{OE}$	OUTPUT	POWER
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	D_{OUT}	Active
Write (1)	L	L	L	L	D_{IN}	Active
Write (1)	L	L	L	H	High Z	Active
Write (2)	L	L	L	X	High Z	Active
Read	L	L	H	H	High Z	Active

NOTES:
1. For IDT71981 only.
2. For IDT71982 only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

ORDERING INFORMATION

IDT XXXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range	
Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package	
P	Plastic DIP (300 mil)
C	Sidebraze DIP (400 mil)
L	Leadless Chip Carrier

Speed (Speed in Nanoseconds)	
15	Commercial Only
20	
25	
30	
35	
45	
55	Military Only
70	Military Only
85	Military Only

Power	
S	Standard Power
L	Low Power

Device Type	
71981	64K (16K x 4-Bit)
71982	64K (16K x 4-Bit) High Impedance Outputs

4

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (8K x 8-BIT)

IDT7164S
IDT7164L

FEATURES:

- High-speed address/chip select access time
  - Military: 35/45/55/70/85/100/120/150/200ns (max.)
  - Commercial: 30/35/45ns (max.)
- Low power consumption
  - IDT7164S
    Active: 300mW (typ.)
    Standby: 100μw (typ.)
  - IDT7164L
    Active: 250mW (typ.)
    Standby: 30μw (typ.)
- Battery backup operation—2V data retention voltage (L Version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Available in standard 28-pin DIP (600 mil), 28-pin THINDIP (300 mil), 28-pin LCC, 32-pin LCC and PLCC and 28-pin SOIC
- Pin-compatible with standard 64K static RAM and EPROM
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-85525 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology.

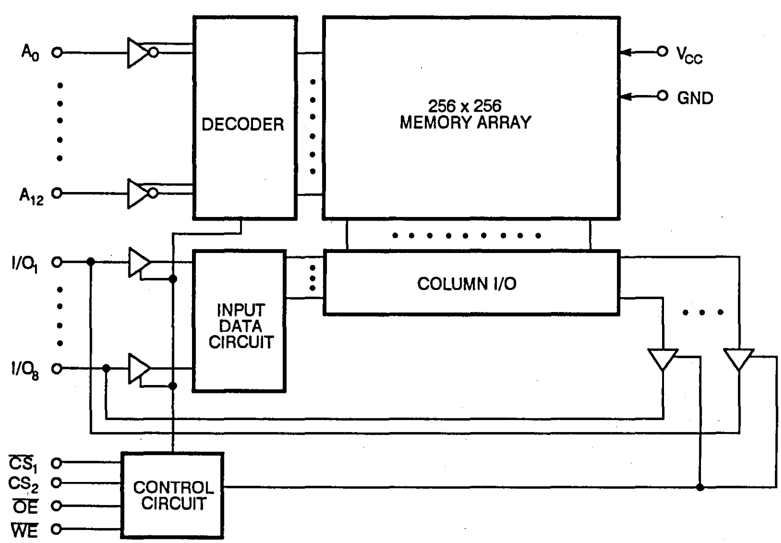
Address access times as fast as 30ns are available with typical power consumption of only 250mW. The circuit also offers a reduced power standby mode. When $\overline{CS}_1$ goes high or CS_2 goes low, the circuit will automatically go to, and remain in, a low-power standby mode. In the full standby mode, the low-power device typically consumes less than 30μW. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10μW operating off a 2V battery.

All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin, 300 mil THINDIP; 28-pin, 600 mil DIP; 32-pin LCC and PLCC and 28-pin LCC and SOIC, providing high board-level packing densities.

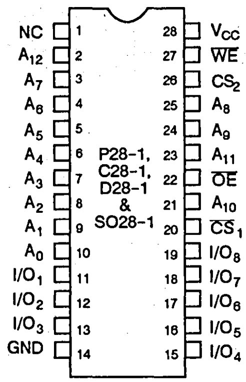
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

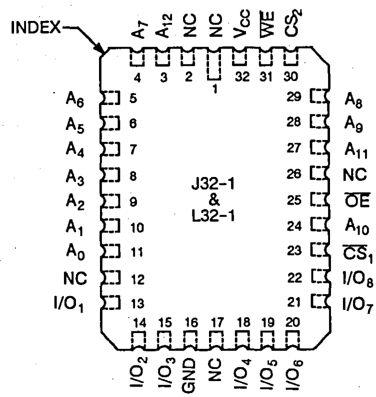


CEMOS is a trademark of Integrated Device Technology, Inc.

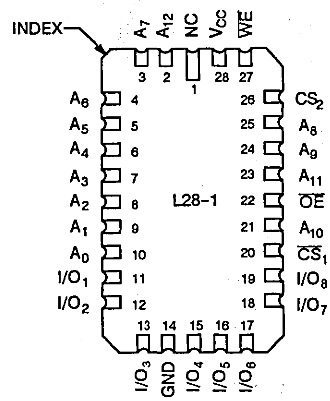
PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW

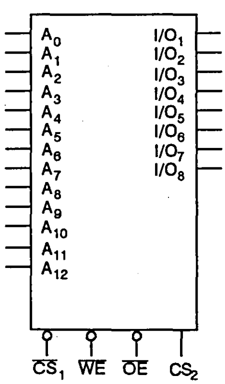


32-PIN LCC/PLCC
TOP VIEW



28-PIN LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0 - A_{12}	Address	$\overline{WE}$	Write Enable
I/O_1 - I/O_8	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}_1$	Chip Select	GND	Ground
CS_2	Chip Select	V_{CC}	Power

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7164S MIN.	IDT7164S TYP.(1)	IDT7164S MAX.	IDT7164L MIN.	IDT7164L TYP.(1)	IDT7164L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}_1 = V_{IH}$, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	IDT7164S30 IDT7164L30 COM'L.	MIL.	IDT7164S35 IDT7164L35 COM'L.	MIL.	IDT7164S45 IDT7164L45 COM'L.	MIL.	IDT7164S55 IDT7164L55 COM'L.	MIL.	IDT7164S70 IDT7164L70 COM'L.	MIL.	IDT7164S85(2) IDT7164L85(2) COM'L.	MIL.	UNIT
I_{CC1}	Operating Power Supply Current, $\overline{CS}_1 = V_{IL}$, Outputs Open, $CS_2 = V_{IH}$ V_{CC} = Max., f = 0(3)	S	90	–	90	100	90	100	–	100	–	100	–	100	mA
		L	80	–	80	90	80	90	–	90	–	90	–	90	
I_{CC2}	Dynamic Operating Current $\overline{CS}_1 = V_{IL}$, Outputs Open, $CS_2 = V_{IH}$, V_{CC} = Max., f = f_{MAX}(3)	S	160	–	150	160	150	160	–	160	–	160	–	160	mA
		L	140	–	130	140	120	130	–	125	–	120	–	120	
I_{SB}	Standby Power Supply Current (TTL Level), f = f_{MAX}(3) $\overline{CS}_1 \geq V_{IH}$, or $CS_2 \geq V_{IL}$ V_{CC} = Max., Outputs Open	S	20	–	20	20	20	20	–	20	–	20	–	20	mA
		L	3	–	3	5	3	5	–	5	–	5	–	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) f = 0(3) 1. $\overline{CS}_1 \geq V_{HC}$ and $CS_2 \geq V_{HC}$ 2. $CS_2 \leq V_{LC}$, V_{CC} = Max.	S	15	–	15	20	15	20	–	20	–	20	–	20	mA
		L	0.2	–	0.2	1.0	0.2	1.0	–	1.0	–	1.0	–	1.0	

NOTES:
1. All values are maximum guaranteed values.
2. Also available: 100, 120, 150 and 200ns military devices.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

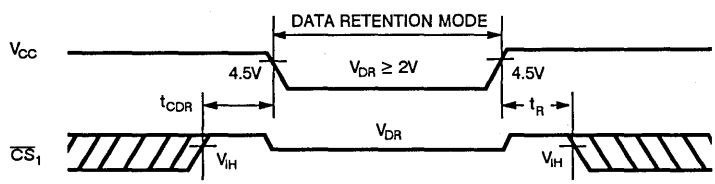
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.[1] V_{CC} @ 2.0V	TYP.[1] V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–	2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	1. $\overline{CS}_1 \geq V_{HC}$, $CS_2 \geq V_{HC}$ 2. $CS_2 \leq V_{LC}$	–	10	15	200	300	µA
			–	10	15	60	90	µA
t_{CDR}	Chip Deselect to Data Retention Time		0	–		–		ns
t_R	Operation Recovery Time		t_{RC}[2]	–		–		ns
$\lvert I_{LI}\rvert$[3]	Input Leakage Current		–	–		2		µA

NOTES:
1. $T_A = +25°C$
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

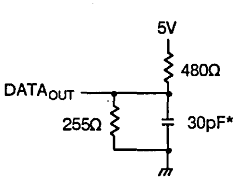


Figure 1. Output Load

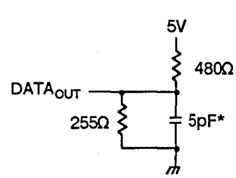


Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

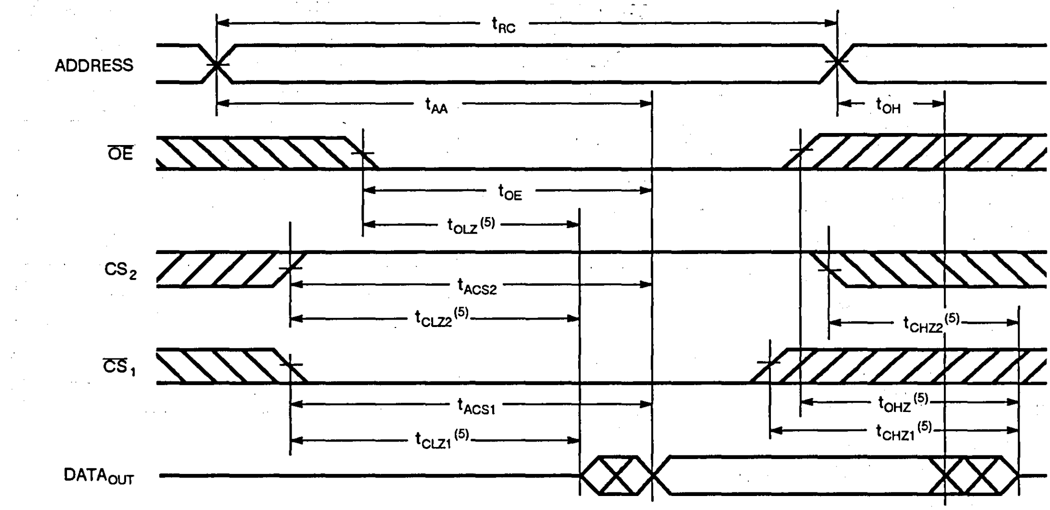
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

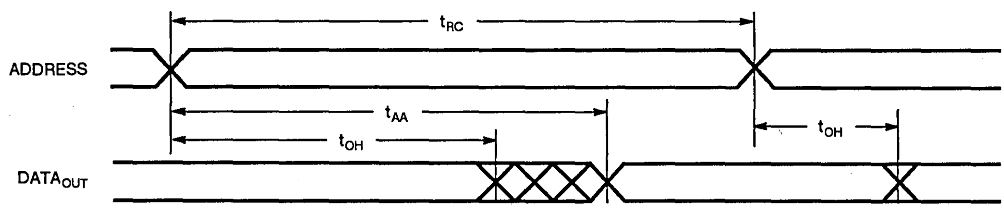
SYMBOL	PARAMETER	7164S30[1, 6] 7164L30[1, 6]		7164S35[5] 7164L35[5]		7164S45 7164L45		7164S55[2] 7164L55[2]		7164S70[2] 7164L70[2]		7164S85[2] 7164L85[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	30	–	35	–	45	–	55	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	30	–	35	–	45	–	55	–	70	–	85	ns
$t_{ACS1, 2}$	Chip Select-1, 2 Access Time [3]	–	35[6]	–	40[5]	–	45	–	55	–	70	–	85	ns
$t_{CLZ1, 2}$	Chip Select-1, 2 to Output in Low Z [4]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	15	–	20	–	25	–	30	–	35	–	40	ns
t_{OLZ}	Output Enable to Output in Low Z [4]	0	–	0	–	0	–	0	–	0	–	0	–	ns
$t_{CHZ1, 2}$	Chip Select-1, 2 to Output in High Z [4]	–	15	–	15	–	20	–	25	–	30	–	35	ns
t_{OHZ}	Output Disable to Output in High Z [4]	–	15	–	15	–	20	–	25	–	30	–	35	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time [4]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Select to Power Down Time [4]	–	30	–	35	–	45	–	55	–	70	–	85	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 100, 120, 150 and 200ns military devices.
3. Both chip selects must be active for the device to be selected.
4. This parameter guaranteed but not tested.
5. t_{ACS1} = 35ns, t_{ACS2} = 40ns
6. t_{ACS1} = 30ns, t_{ACS2} = 35ns

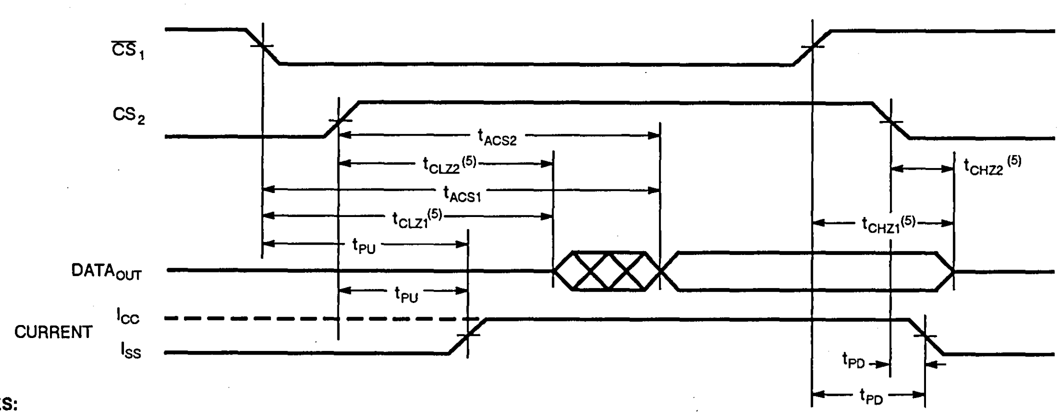
TIMING WAVEFORM OF READ CYCLE NO. 1 [1]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 3 [1, 3, 4]



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low and CS_2 transition high.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.

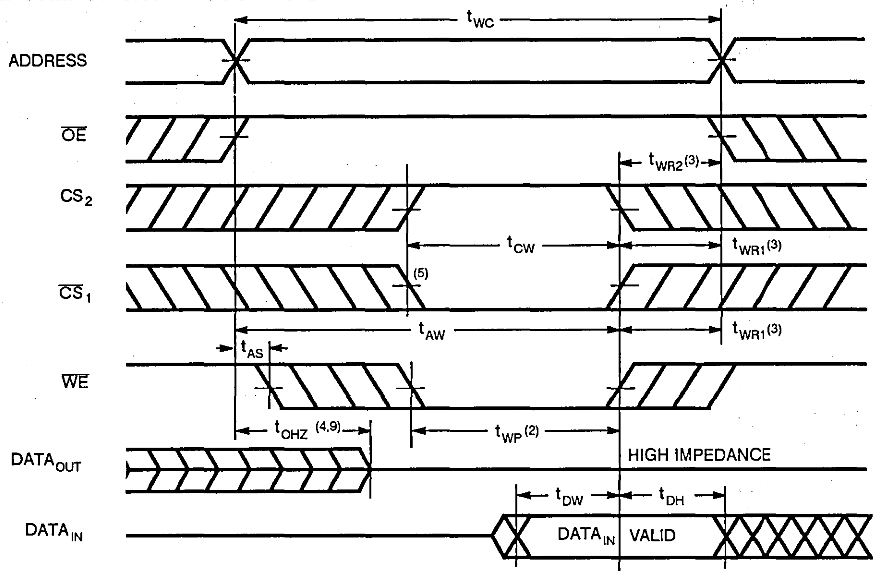
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7164S30[1] 7164L30[1] MIN.	MAX.	7164S35 7164L35 MIN.	MAX.	7164S45 7164L45 MIN.	MAX.	7164S55[2] 7164L55[2] MIN.	MAX.	7164S70[2] 7164L70[2] MIN.	MAX.	7164S85[2] 7164L85[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	30	–	35	–	45	–	55	–	70	–	85	–	ns
$t_{CW1,2}$	Chip Select to End of Write	25	–	30	–	40	–	50	–	60	–	75	–	ns
t_{AW}	Address Valid to End of Write	25	–	30	–	40	–	50	–	60	–	75	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	25	–	30	–	40	–	50	–	60	–	75	–	ns
t_{WR1}	Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$)	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WR2}	Write Recovery Time (CS_2)	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{WHZ}	Write Enable to Output High Z[3]	–	12	–	15	–	20	–	25	–	30	–	35	ns
t_{DW}	Data to Write Time Overlap	13	–	15	–	20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold from Write Time[4]	3/5	–	3/5	–	3/5	–	3/5	–	3/5	–	3/5	–	ns
t_{OW}	Output Active from End of Write[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns

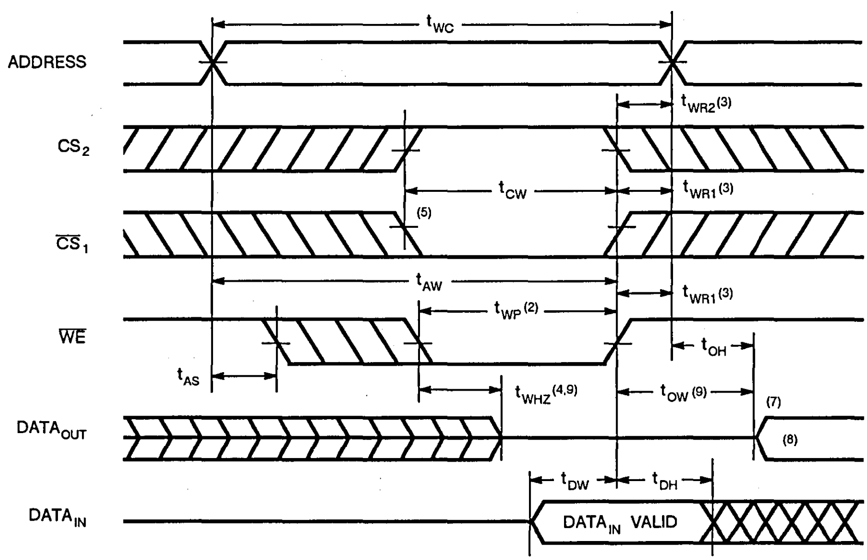
NOTES:

1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only. Also available: 100, 120, 150 and 200ns military devices.
3. This parameter guaranteed but not tested.
4. With respect to $\overline{CS}_1$, $\overline{WE}$ = 30ns, CS_2 = 5ns

TIMING WAVEFORM OF WRITE CYCLE NO. 1[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2[1, 6]



NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}_1$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}_1$ low transition or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. $DATA_{OUT}$ is the same phase of write data of this write cycle.
8. If $\overline{CS}_1$ is low and CS_2 is high during this period, I/O pins are in the output state. Data input signals must not be applied.
9. Transition is measured ±200mV from steady state.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

TRUTH TABLE

$\overline{WE}$	$\overline{CS}_1$	CS_2	$\overline{OE}$	I/O	MODE
X	H	X	X	HIGH Z	Standby (I_{SB})
X	X	L	X	HIGH Z	Standby (I_{SB})
X	V_{HC}	V_{HC} or V_{LC}	X	HIGH Z	Standby (I_{SB1})
X	X	V_{LC}	X	HIGH Z	Standby (I_{SB1})
H	L	H	H	HIGH Z	Output disable
H	L	H	L	D_{OUT}	Read
L	L	H	X	D_{IN}	Write

NOTE:
1. CS_2 will power-down $\overline{CS}_1$, but $\overline{CS}_1$ will not power-down CS_2.

ORDERING INFORMATION

IDT XXXXX Device Type — A Power — 999 Speed — A Package — A Process/Temperature Range

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	P	Plastic DIP
	TC	Sidebraze THINDIP
	D	CERDIP
	J	Plastic Leaded Chip Carrier
	L	Leadless Chip Carrier
	SO	Small Outline IC
Speed (Speed in Nanoseconds)	30	Commercial Only
	35	
	45	
	55	Military Only
	70	Military Only
	85	Military Only
Power	S	Standard Power
	L	Low Power
Device Type	7164	64K (8K x 8-Bit) CMOS Static RAM

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (4K x 16-BIT)

ADVANCE INFORMATION
IDT7186S
IDT7186L

FEATURES:

- 16-bit word width, with separate control of upper and lower bytes
- High-speed access
  - Military: 55/70/85ns (max.)
  - Commercial: 45/55ns (max.)
- Low power consumption
  - IDT7186S
    Active: 400mW (typ.)
    Standby: 100μW (typ.)
  - IDT7186L
    Active: 300mW (typ.)
    Standby: 30μW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- JEDEC compatible pinout
- Battery backup operation—2V data retention
- Available in 40-pin, 600 mil plastic and sidebraze DIP
- TTL-compatible
- Single 5V (±10%) power supply
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7186 is an extremely high-speed 4K x 16-bit static RAM designed for use in wide-word systems where high speed, low power and board density are of the utmost importance.

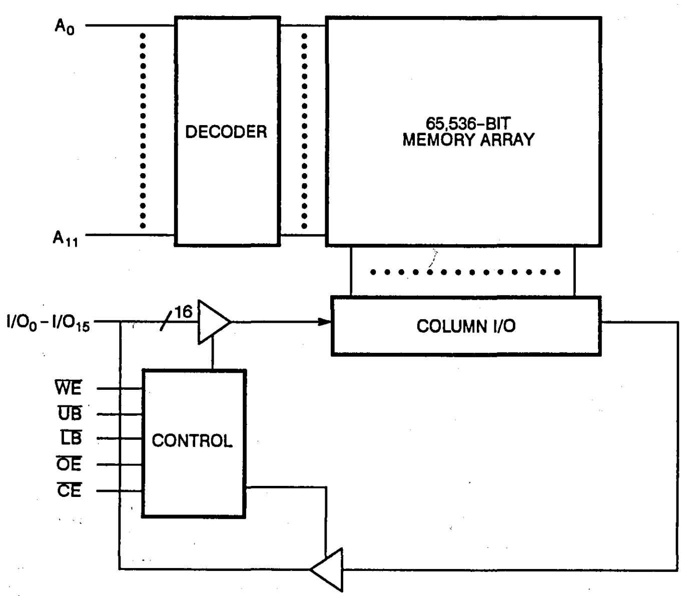
The IDT7186 uses sixteen bidirectional input/output lines to provide simultaneous access to all bits in a word and has two byte enable lines to allow the upper and lower byte of a word to be accessed either together or independently. A high-speed output enable pin allows designers to turn on the IDT7186's outputs at a speed much higher than the already fast address access time and achieve a considerable throughput advantage. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry to enter a very low standby mode.

Fabricated using IDT's CEMOS™ high-performance technology, the IDT7186 typically operates on only 300mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, typically consuming 30μW from a 2V battery.

The IDT7186 is packaged in either a sidebraze or plastic 40-pin DIP. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

4

FUNCTIONAL BLOCK DIAGRAM

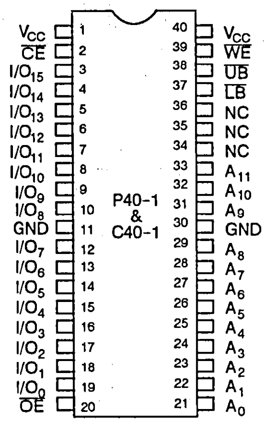


CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

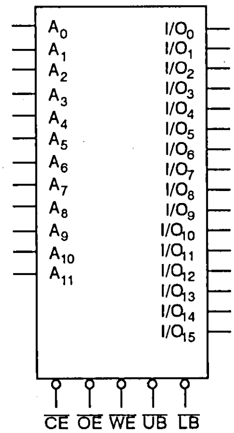
DSC-1024/-

PIN CONFIGURATIONS



DIP
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0-A_{11}	Addresses
I/O_0-I/O_{15}	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{UB}$	Upper Byte Enable
$\overline{LB}$	Lower Byte Enable
GND	Ground
V_{CC}	Power

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT7186S MIN.	IDT7186S MAX.	IDT7186L MIN.	IDT7186L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	10	–	5	μA
			COM'L.	–	10	–	5	μA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} Max. $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	10	–	5	μA
			COM'L.	–	10	–	5	μA
V_{OL}	Output Low Voltage	I_{OL} = 6mA, V_{CC} = Min.		–	0.4	–	0.4	V
		I_{OL} = 8mA, V_{CC} = Min.		–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	2.4	–	V

4

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	IDT7186S45 IDT7186L45 COM'L.	IDT7186S45 IDT7186L45 MIL.	IDT7186S55 IDT7186L55 COM'L.	IDT7186S55 IDT7186L55 MIL.	IDT7186S70 IDT7186L70 COM'L.	IDT7186S70 IDT7186L70 MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CE}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0 (2)	S	130	–	130	150	130	150	mA
		L	115	–	115	135	115	135	mA
I_{CC2}	Dynamic Operating Current $\overline{CE}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX} (2)	S	160	–	160	190	160	190	mA
		L	140	–	140	170	140	170	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CE}$ ≥ V_{IH} V_{CC} = Max., f = f_{MAX} (2) Outputs Open	S	40	–	40	40	40	40	mA
		L	6	–	6	6	6	6	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CE}$ ≥ V_{HC}, V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC} V_{CC} = Max., f = 0 (2)	S	15	–	15	20	15	20	mA
		L	0.5	–	0.5	1.5	0.5	1.5	mA

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, address and data input are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

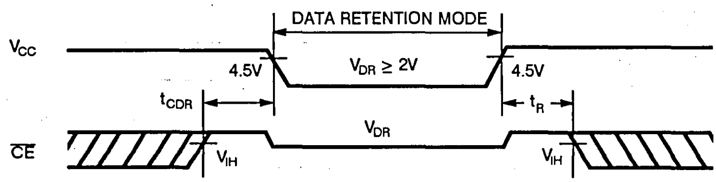
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.[1] V_{CC} @ 2.0V	TYP.[1] V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$, $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	–	–	600	900	µA
			COM'L.	–	–	–	200	300	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–	–	–	–	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–	–	–	–	ns
$\lvert I_{LI} \rvert$[3]	Input Leakage Current			–	–	–	2	2	µA

NOTES:
1. $T_A = +25°C$
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

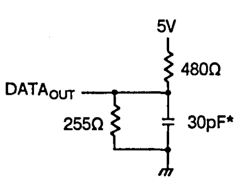


Figure 1. Output Load

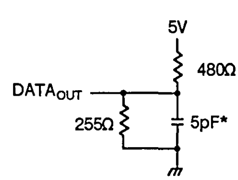


Figure 2. Output Load (for t_{OW}, t_{WHZ}, t_{CHZ}, t_{CLZ}, t_{BHZ}, t_{BLZ}, t_{OHZ}, t_{OLZ})

* Including scope and jig.

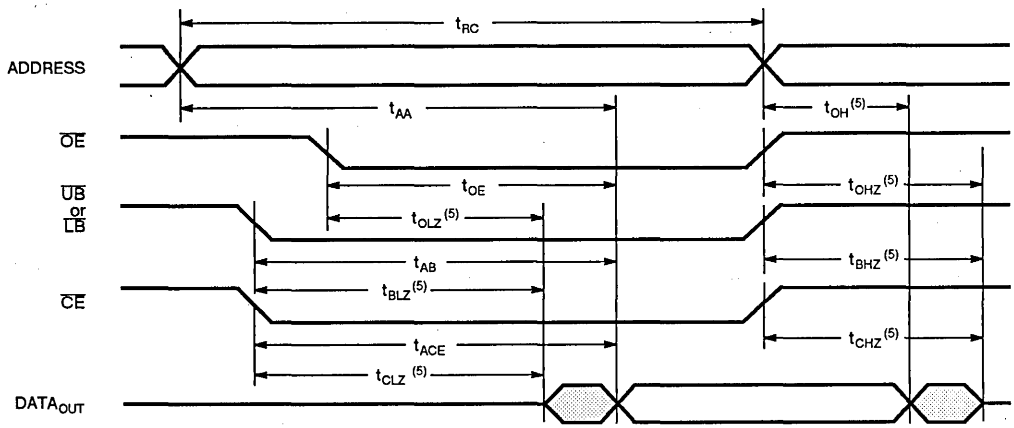
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7186S45 (1) IDT7186L45 (1)		IDT7186S55 IDT7186L55		IDT7186S70 IDT7186L70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE								
t_{RC}	Read Cycle Time	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	45	–	55	–	70	ns
t_{ACE}	Chip Enable Access Time	–	45	–	55	–	70	ns
t_{AB}	Upper/Lower Byte Enable Access Time	–	20	–	25	–	30	ns
t_{CLZ}	Chip Enable to Output in Low Z (2)	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	20	–	25	–	30	ns
t_{BLZ}	Upper/Lower Byte Enable to Output in Low Z (2)	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z (2)	5	–	5	–	5	–	ns
t_{CHZ}	Chip Disable to Output in High Z (2)	–	20	–	25	–	30	ns
t_{OHZ}	Output Disable to Output in High Z (2)	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	ns
t_{BHZ}	Upper/Lower Byte Enable to Output in High Z (2)	–	20	–	25	–	30	ns
t_{PU}	Chip Enable to Power Up Time	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time	–	45	–	55	–	70	ns

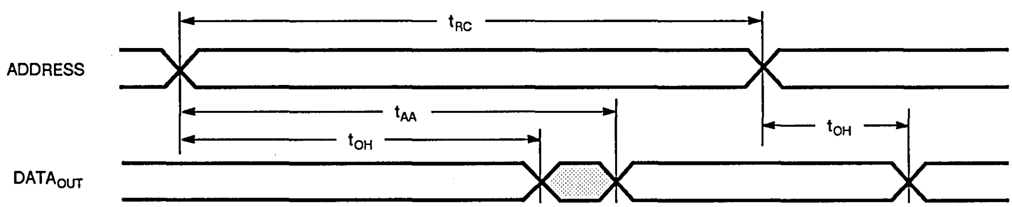
NOTES:

1. 0°C to +70°C temperature range only.
2. This parameter is guaranteed but not tested.

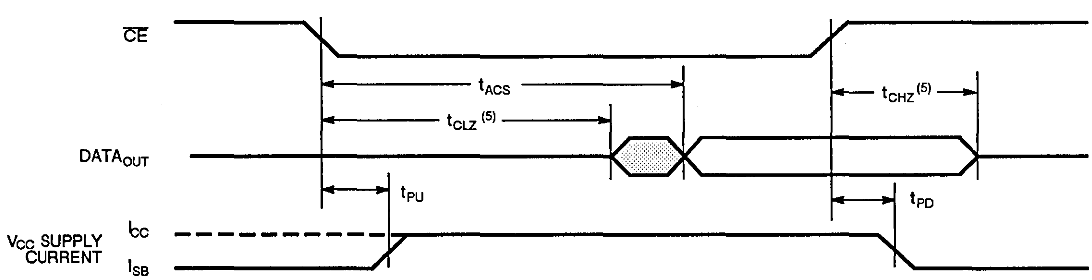
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (Continuously Enabled Read) (1, 2, 4, 6)



TIMING WAVEFORM OF READ CYCLE NO. 3 ($\overline{CE}$ Controlled Read W/Power-Up/Down Timing) (1, 3, 4, 6)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CE} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state with 5pf load (including scope and jig).
6. $\overline{UB}$ or $\overline{LB} = V_{IL}$

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

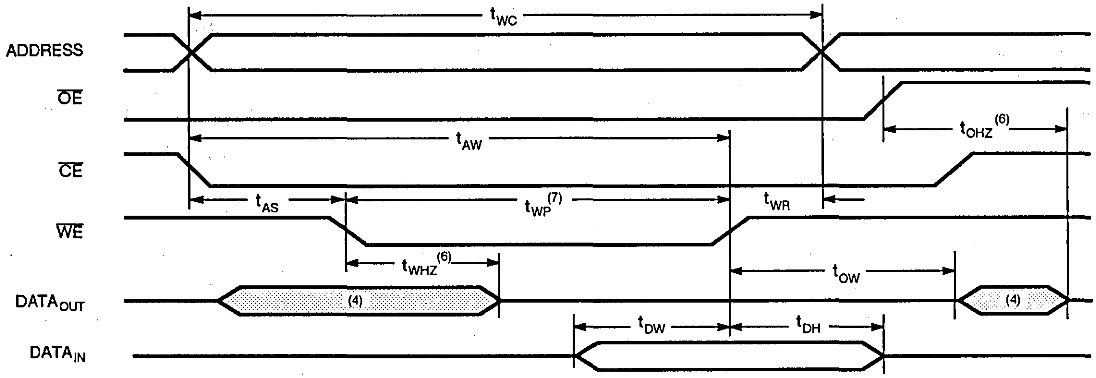
SYMBOL	PARAMETER	IDT7186S45 (1) IDT7186L45 (1)		IDT7186S55 IDT7186L55		IDT7186S70 IDT7186L70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	–	55	–	70	–	ns
t_{CW}	Chip Enable to End of Write	40	–	50	–	60	–	ns
t_{BW}	Upper/Lower Byte Enable to End of Write	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	ns
t_{WHZ}	Write to Output in High Z (2)	–	20	–	25	–	30	ns
t_{DW}	Data Set-up Time	20	–	25	–	30	–	ns
t_{DH}	Data Hold from Write Time	3	–	3	–	3	–	ns
t_{OW}	Output Active from End of Write (2)	5	–	5	–	5	–	ns

NOTES:

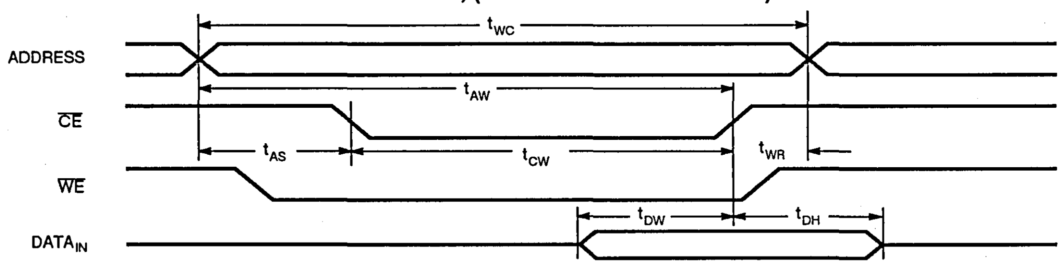
1. 0°C to +70°C temperature range only.
2. This parameter is guaranteed but not tested.

4

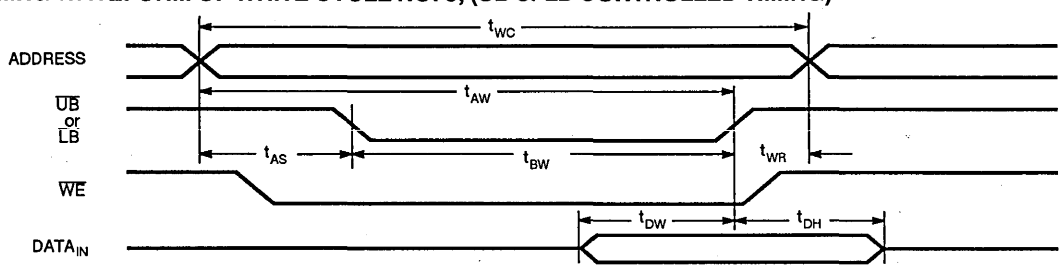
TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 7, 8)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING) (1, 2, 3, 5, 8)



TIMING WAVEFORM OF WRITE CYCLE NO. 3, ($\overline{UB}$ or $\overline{LB}$ CONTROLLED TIMING) (1, 2, 3, 5, 9)



NOTES:

1. $\overline{WE}$, $\overline{CE}$, or both $\overline{UB}$ or $\overline{LB}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{BW}, t_{CW} or t_{WP}) of a low $\overline{UB}$ or $\overline{LB}$, a low $\overline{CE}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{UB}$, $\overline{LB}$, $\overline{CE}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. $\overline{UB}$ or $\overline{LB}$ = V_{IL}
9. $\overline{CE}$ = V_{IL}

TRUTH TABLE (1)

INPUTS					OUTPUTS		MODE
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$I/O_8 - I/O_{15}$	$I/O_0 - I/O_7$	
H	X	X	X	X	Hi-Z	Hi-Z	Deselected, Powered Down
L	X	X	H	H	Hi-Z	Hi-Z	Both Bytes Deselected
L	L	X	L	H	$DATA_{IN}$	Hi-Z	Write to Upper Byte Only
L	L	X	H	L	Hi-Z	$DATA_{IN}$	Write to Lower Byte Only
L	L	X	L	L	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes (Word Write)
L	H	L	L	H	$DATA_{OUT}$	Hi-Z	Read Upper Byte Only
L	H	L	H	L	Hi-Z	$DATA_{OUT}$	Read Lower Byte Only
L	H	L	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes (Word Read)
L	H	H	X	X	Hi-Z	Hi-Z	Outputs Disabled

NOTES:
1. H = High, L = Low, X = Don't Care, Hi-Z = High Impedance

ORDERING INFORMATION

IDT XXXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/ Temperature Range)

Process/Temperature Range:
- Blank — Commercial (0°C to +70°C)
- B — Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B,

Package:
- P — Plastic DIP
- C — Sidebraze DIP

Speed:
- 45 — Commercial Only
- 55
- 70

Speed in Nanoseconds

Power:
- S — Standard Power
- L — Low Power

Device Type:
- 7186 — 64K (4K x 16-Bit)

Integrated Device Technology, Inc.

CMOS STATIC RAM PLASTIC SIP MODULE (16K x 5-BIT)

IDT7MP564

FEATURES:

- 81,920-bit CMOS static RAM module with decoupling capacitor
- High speed: 20ns max.
- Low power consumption: 1.1W typ.
- IDT7MP564 package options reduce overall height
- Utilizes IDT6167s—high-performance 16K RAMs produced with advanced CEMOS™
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

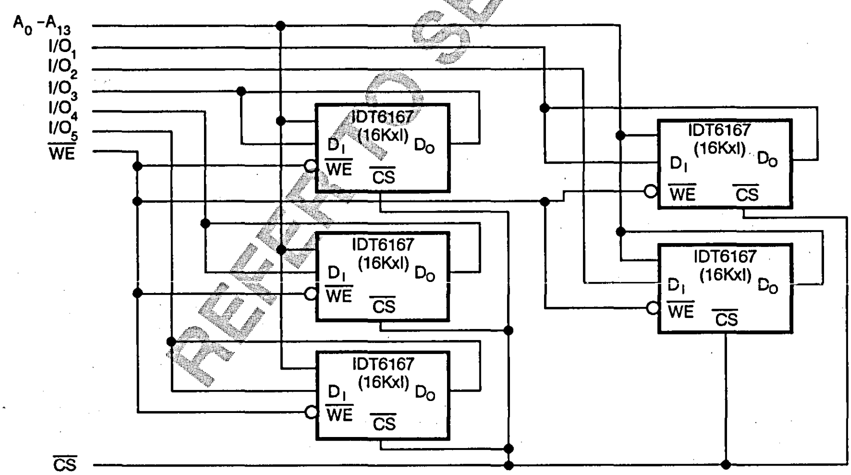
DESCRIPTION:

The IDT7MP564 is an 80K (16,384 x 5-bit) high-speed CMOS static RAM constructed on an epoxy laminate substrate using 5 IDT6167 (16,384 x 1-bit) CMOS static RAMs in plastic surface mount packages. Extremely fast speeds can be achieved with this technique due to use of the IDT6167 RAMs, fabricated in IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 16K static RAMs available.

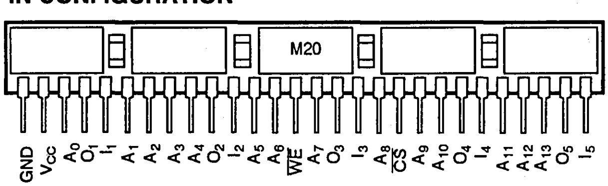
The IDT7MP564 is available with access times as fast as 20ns, with maximum power consumption of only 2.2 watts. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit automatically goes to, and remains in, a standby mode as long as $\overline{CS}$ remains high, consuming only 963mW maximum. Substantially lower power levels can be achieved in the I_{SB1} mode (less than 138mW max.).

All inputs and outputs of the IDT7MP564 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SIP SIDE VIEW

PIN NAMES

$A_0 - A_{13}$	Addresses	$\overline{WE}$	Write Enable
$I/O_1 - I/O_5$	Data Inputs/Outputs	V_{CC}	Power
$\overline{CS}$	Chip Select	GND	Ground

CEMOS is a trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE **DECEMBER 1987**

DSC-7008/-

Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (256K x 1-BIT)

PRELIMINARY
IDT71257S
IDT71257L

FEATURES:

- High-speed (equal access and cycle time)
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - IDT71257S
    Active: 400mW (typ.)
    Standby: 400µW (typ.)
  - IDT71257L
    Active: 350mW (typ.)
    Standby: 100µW (typ.)
- Battery backup operation—2V data retention (L version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in high-density industry standard 24-pin, 300 mil DIP and 24-pin SOIC
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71257 is a 262,144-bit high-speed static RAM organized as 256K x 1. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

Access times as fast as 25ns are available with typical power consumption of only 350mW. The IDT71257 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 100µW operation off a 2V battery.

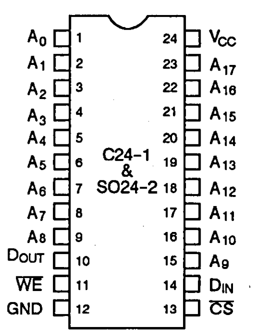
All inputs and outputs of the IDT71257 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT71257 is packaged in a 24-pin 300 mil DIP and a 24-pin SOIC, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

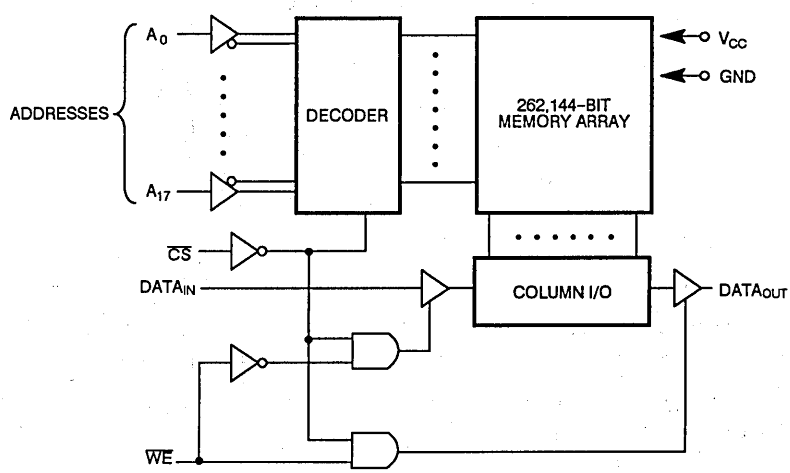
4

PIN CONFIGURATION



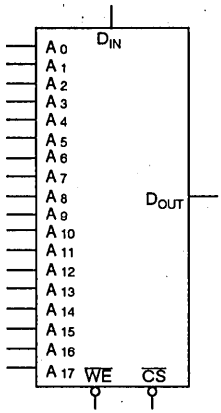
DIP/SOIC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

LOGIC SYMBOL



PIN NAMES

$A_0 - A_{17}$	Addresses
D_{IN}	Data Input
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
D_{OUT}	Data Output
GND	Ground
V_{CC}	Power

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71257S MIN.	IDT71257S MAX.	IDT71257L MIN.	IDT71257L MAX.	UNIT
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	
$\lvert I_{LO}\rvert$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		–	0.4	–	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS (1) (V_{CC} = 5V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

SYMBOL	PARAMETER	POWER	FUNCTION	IDT71257S25 IDT71257L25		IDT71257S35(4) IDT71257L35(4)		IDT71257S45 IDT71257L45		IDT71257S55 IDT71257L55		IDT71257S70 IDT71257L70		UNIT
				COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(3)	S	READ	60	–	50	60	50	60	50	60	–	60	mA
			WRITE(2)	110	–	100	110	100	110	100	110	–	110	
		L	READ	40	–	30	40	30	40	30	40	–	40	
			WRITE(2)	100	–	90	100	90	100	90	100	–	100	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	S	READ	160	–	150	160	150	160	150	160	–	160	mA
			WRITE(2)	160	–	150	160	150	160	150	160	–	160	
		L	READ	140	–	130	140	130	140	130	140	–	140	
			WRITE(2)	140	–	130	140	130	140	130	140	–	140	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(3)	S		35	–	35	35	35	35	35	35	–	35	mA
		L		20	–	20	20	20	20	20	20	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., f = 0(3)	S		30	–	30	35	30	35	30	35	–	35	mA
		L		1.5	–	1.5	4.5	1.5	4.5	1.5	4.5	–	4.5	

NOTES:
1. All values are maximum guaranteed values.
2. Write cycle current specifications are included to aid in the design of extremely sensitive applications. It should be noted that in most systems the ratio of read cycles to write cycles is extremely high. When comparing these figures to those on other data sheets, we recommend that the read cycle data is used (especially where "Average" current consumption figures are specified).
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. Preliminary data for military devices only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

TRUTH TABLE (V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

$\overline{WE}$	$\overline{CS}$	OUTPUT	MODE
X	H	Hi-Z	Standby (I_{SB})
X	V_{HC}	Hi-Z	Standby (I_{SB1})
H	L	D_{OUT}	Read
L	L	Hi-Z	Write

NOTE:
1. H = V_{IH}, L = V_{IL}, X = Don't Care

4

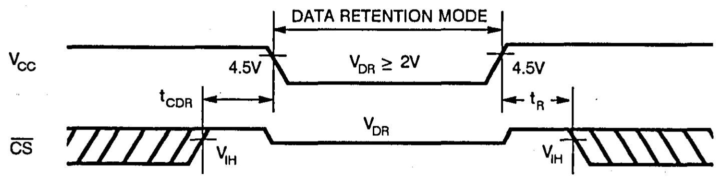
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL.	–	50	75	2000	3000	µA
			COM'L.	–	50	75	500	750	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–	–	–	–	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–	–	–	–	ns

NOTES:
1. $T_A = +25°C$
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed, but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

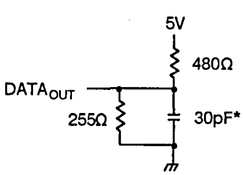


Figure 1. Output Load

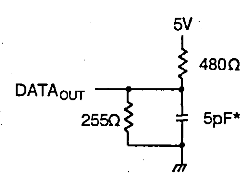


Figure 2. Output Load (for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, t_{OW})

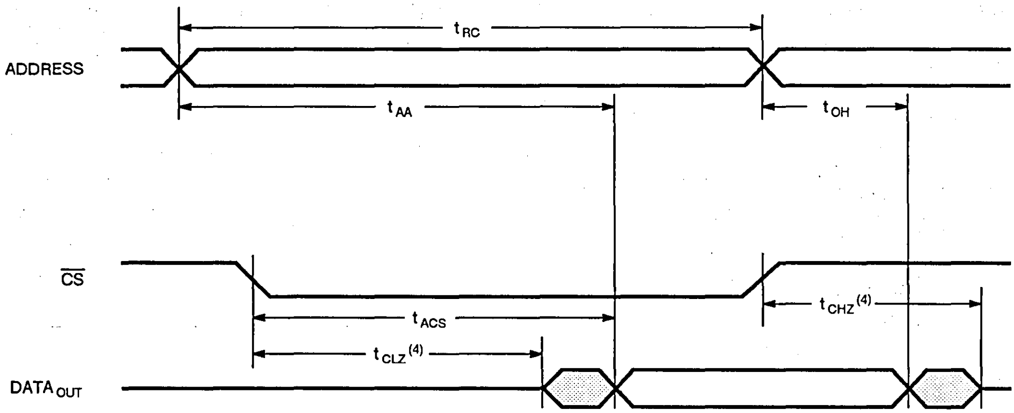
*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

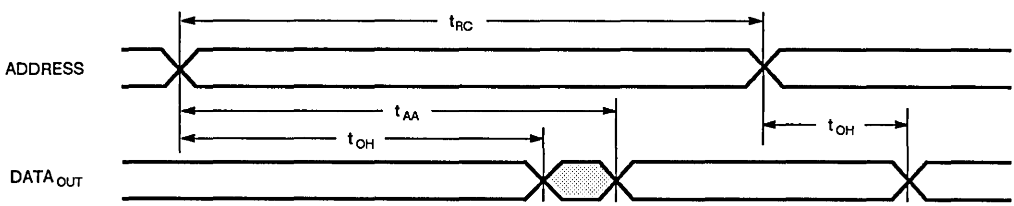
SYMBOL	PARAMETER	IDT71257S25(1) IDT71257L25(1) MIN.	MAX.	IDT71257S35 IDT71257L35 MIN.	MAX.	IDT71257S45 IDT71257L45 MIN.	MAX.	IDT71257S55 IDT71257L55 MIN.	MAX.	IDT71257S70(2) IDT71257L70(2) MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	25	–	35	–	45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time	–	30	–	35	–	45	–	55	–	70	ns
t_{CLZ}	Chip Select to Output in Low Z(3)	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time(3)	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time(3)	–	25	–	35	–	45	–	55	–	70	ns
t_{CHZ}	Chip Deselect to Output in High Z(3)	–	13	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

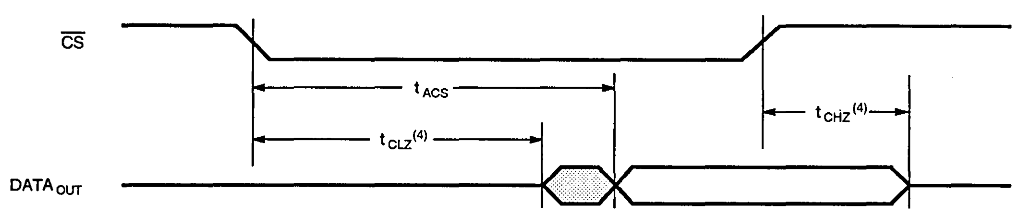
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 3 [1, 3]



NOTES:

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

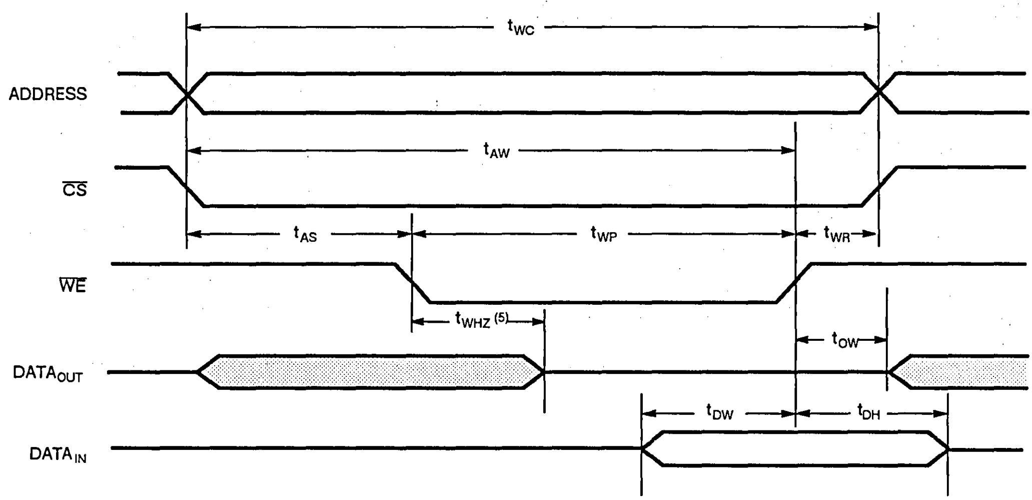
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71257S25[1] IDT71257L25[1] MIN.	MAX.	IDT71257S35 IDT71257L35 MIN.	MAX.	IDT71257S45 IDT71257L45 MIN.	MAX.	IDT71257S55 IDT71257L55 MIN.	MAX.	IDT71257S70[2] IDT71257L70[2] MIN.	MAX.	UNIT
WRITE CYCLE												
t_{WC}	Write Cycle Time	20	–	30	–	40	–	50	–	60	–	ns
t_{CW}	Chip Select to End of Write	20	–	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	20	–	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	20	–	30	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output in High Z[3]	–	13	–	15	–	20	–	25	–	30	ns
t_{DW}	Data Valid to End of Write	15	–	20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write[3]	5	–	5	–	5	–	5	–	5	–	ns

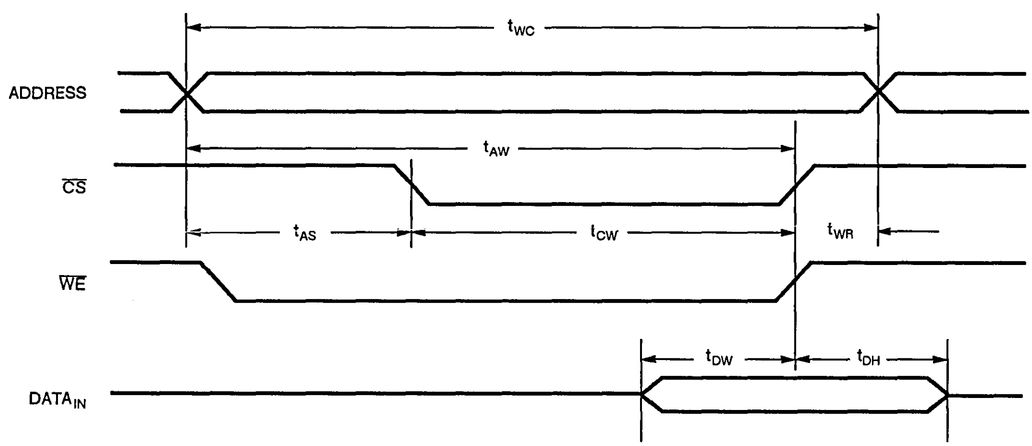
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

4

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (1, 2, 3) ($\overline{WE}$ CONTROLLED TIMING)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (1, 2, 3, 4) ($\overline{CS}$ CONTROLLED TIMING)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneous with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/ Temperature Range)

Field	Code	Description
Process/ Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (–55°C to +125°C) Compliant with MIL-STD-883, Class B
Package	C	Sidebraze DIP
	SO	Small Outline IC
Speed	25	Commercial Only
	35	
	45	
	55	
	70	Military Only
Power	L	Low Power
	S	Standard Power
Device Type	71257	256K (256K x 1-Bit) Static RAM

Speed in Nanoseconds

Integrated Device Technology, Inc.

256K (256K x 1-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

IDT7MP156

FEATURES:

- High-density 256K (256K x 1) CMOS static RAM module
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Available in 28-pin SIP (single in-line package) for maximum space saving
- Fast access times: 25ns (max.) over commercial temperature
- Low power consumption
  - Dynamic: less than 600mW (typ.)
  - Full standby: less than 30mW (typ.)
- Utilizes IDT7187 high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION

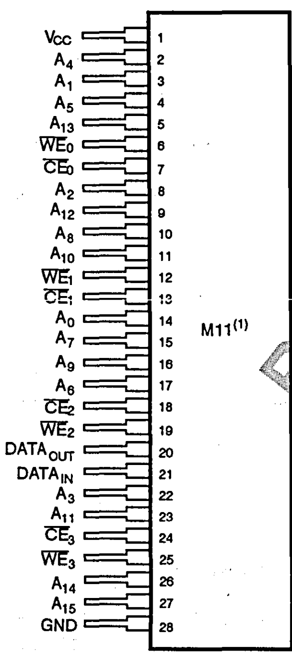
The IDT7MP156 is a 256K (256K x 1-bit) high-speed static RAM module constructed on an epoxy laminate surface using four IDT7187 64K x 1 static RAMs in surface mount packages. Extremely fast speeds can be achieved with this technique due to use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS technology.

The 7MP family of surface mounted SIP technology is a cost-effective solution allowing for very high packing density. The IDT7MP156 is offered in a 28-pin SIP (single in-line package). The IDT7MP156 can be mounted on 200 mil centers, yielding 1.25 megabits of memory in less than 3 square inches of board space.

The IDT7MP156 is available with maximum access times as fast as 25ns with maximum power consumption of 1.8 watts. The module also offers a full standby mode of 440mW (max.).

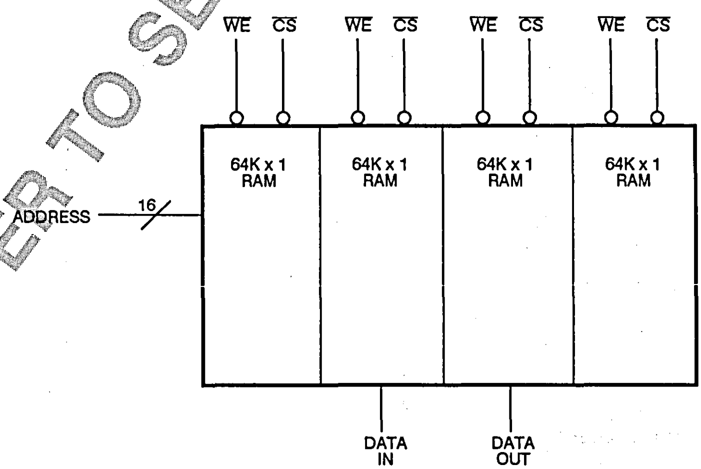
All inputs and outputs of the IDT7MP156 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

PIN CONFIGURATION



SIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0–A_{15}	Address Lines
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}_{0-3}$	Chip Enable
$\overline{WE}_{0-3}$	Write Enable
Vcc	Power
GND	Ground

NOTE:
1. For module dimensions, plese refer to module drawing M11 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

256K (256K x 1-BIT) CMOS STATIC RAM SIP MODULE

IDT7MC156

FEATURES:

- High-density 256K (256K x 1) CMOS static RAM module
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Available in low profile 28-pin ceramic SIP (single in-line package) for maximum space saving
- Fast access times: 25ns (max.) over commercial temperature
- Low power consumption
  - Dynamic: less than 600mW (typ.)
  - Full standby: less than 30mW (typ.)
- Utilizes IDT7187s high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT7MC156 is a 256K (256K x 1-bit) high-speed static RAM module constructed on a co-fired ceramic substrate using four IDT7187 64K x 1 static RAMs in surface mount packages.

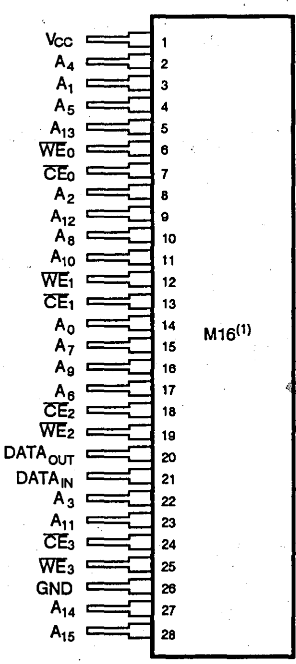
The 7MC family of ceramic SIPs offers the optimum in packing density and profile height. The IDT7MC156 is offered in a 28-pin ceramic SIP (single in-line package). At only 350 mils high, this low profile package is ideal for systems with minimal board spacing. Surface mount SIP technology also yields very high packing density, allowing greater than three IDT7MC156 modules to be stacked per inch of board space.

The IDT7MC156 is available with maximum access times as fast as 25ns and maximum power consumption of 1.8 watts. The module also offers a full standby mode of 440mW (max.).

All inputs and outputs of the IDT7MC156 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access times for ease of use.

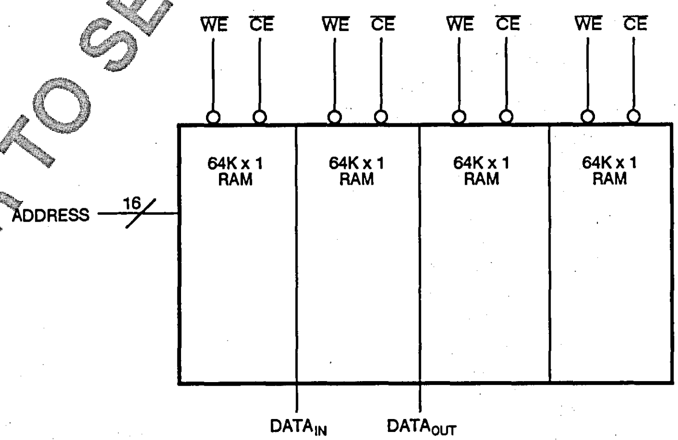
4

PIN CONFIGURATION



SIP SIDE VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{15}	Address Lines
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CS}_{0-3}$	Chip Enable
$\overline{WE}_{0-3}$	Write Enable
Vcc	Power
GND	Ground

NOTE:

1. For module dimensions, please refer to module drawing M16 in the packaging section.

Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (64K x 4-BIT)

PRELIMINARY
IDT71258S
IDT71258L

FEATURES:

- High-speed (equal access and cycle time)
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55/ns (max.)
- Low-power operation
  - IDT71258S
    Active: 400mW (typ.)
    Standby: 400μW (typ.)
  - IDT71258L
    Active: 350mW (typ.)
    Standby: 100μW (typ.)
- Battery backup operation—2V data retention (L version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in high-density industry standard 24-pin, 300 mil DIP and 24-pin SOIC
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71258 is a 262,144-bit high-speed static RAM organized as 64K x 4. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

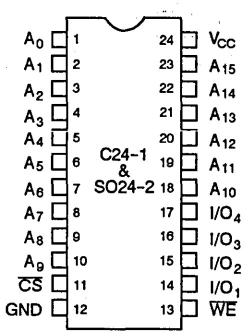
Access times as fast as 25ns are available with typical power consumption of only 350mW. The IDT71258 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements . This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 100μW operation off a 2V battery.

All inputs and outputs of the IDT71258 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT71258 is packaged in a 24-pin 300 mil DIP and a 24-pin SOIC providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

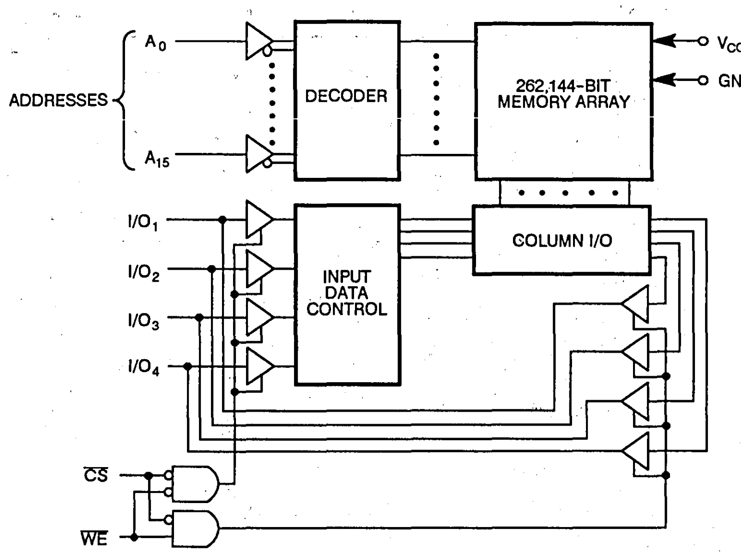


DIP/SOIC TOP VIEW

PIN NAMES

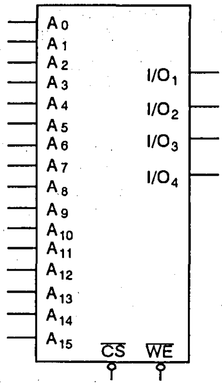
$A_0 - A_{15}$	Addresses
I/O_1 - I/O_4	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
GND	Ground
V_{CC}	Power

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

LOGIC SYMBOL



RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	$-0.5^{(1)}$	–	0.8	V

NOTE:

1. V_{IL} = –3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71258S MIN.	IDT71258S MAX.	IDT71258L MIN.	IDT71258L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		–	0.4	–	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS(1) (V_{CC} = 5V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

SYMBOL	PARAMETER	POWER	FUNCTION	IDT71258S25 IDT71258L25 COM'L.	MIL.	IDT71258S35(4) IDT71258L35(4) COM'L.	MIL.	IDT71258S45 IDT71258L45 COM'L.	MIL.	IDT71258S55 IDT71258L55 COM'L.	MIL.	IDT71258S70 IDT71258L70 COM'L.	MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(3)	S	READ	60	–	50	60	50	60	50	60	–	60	mA
			WRITE(2)	110	–	100	110	100	110	100	110	–	110	
		L	READ	40	–	30	40	30	40	30	40	–	40	
			WRITE(2)	100	–	90	100	90	100	90	100	–	100	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	S	READ	160	–	150	160	150	160	150	160	–	160	mA
			WRITE(2)	160	–	150	160	150	160	150	160	–	160	
		L	READ	140	–	130	140	130	140	130	140	–	140	
			WRITE(2)	140	–	130	140	130	140	130	140	–	140	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}(3)	S	–	35	–	35	35	35	35	35	35	–	35	mA
		L	–	20	–	20	20	20	20	20	20	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., f = 0(3)	S	–	30	–	30	35	30	35	30	35	–	35	mA
		L	–	1.5	–	1.5	4.5	1.5	4.5	1.5	4.5	–	4.5	

NOTES:
1. All values are maximum guaranteed values.
2. Write cycle current specifications are included to aid in the design of extremely sensitive applications. It should be noted that in most systems the ratio of read cycles to write cycles is extremely high. When comparing these figures to those on other data sheets, we recommend that the read cycle data is used (especially where "Average" current consumption figures are specified).
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $/t_{RC}$. f = 0 means no input lines change.
4. Preliminary data for military devices only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is but production tested.

TRUTH TABLE (V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

$\overline{WE}$	$\overline{CS}$	I/O	MODE
X	H	Hi-Z	Standby (I_{SB})
X	V_{HC}	Hi-Z	Standby (I_{SB1})
H	L	D_{OUT}	Read
L	L	D_{IN}	Write

NOTE:
1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

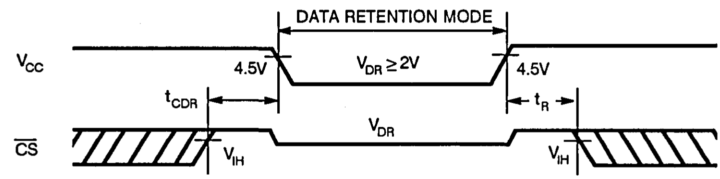
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.[1] V_{CC} @ 2.0V	TYP.[1] V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL.	—	50	75	2000	3000	µA
			COM'L.	—	50	75	500	750	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns

NOTES:
1. $T_A = +25°C$
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

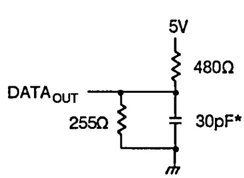


Figure 1. Output Load

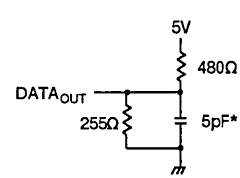


Figure 2. Output Load (for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, t_{OW})

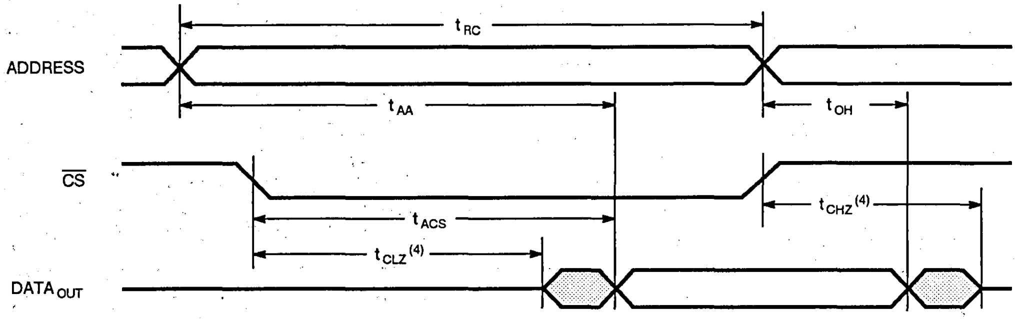
*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±10%, All Temperature Ranges

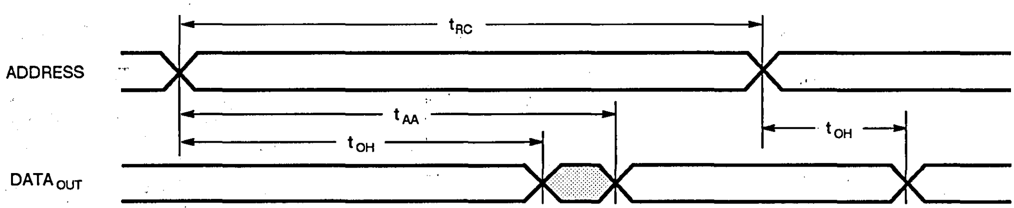
SYMBOL	PARAMETER	IDT71258S25[1] IDT71258L25[1] MIN.	MAX.	IDT71258S35 IDT71258L35 MIN.	MAX.	IDT71258S45 IDT71258L45 MIN.	MAX.	IDT71258S55 IDT71258L55 MIN.	MAX.	IDT71258S70[2] IDT71258L70[2] MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	25	–	35	–	45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time	–	30	–	35	–	45	–	55	–	70	ns
t_{CLZ}	Chip Select to Output in Low Z[3]	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	25	–	35	–	45	–	55	–	70	ns
t_{CHZ}	Chip Deselect to Output in High Z[3]	–	13	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed, but not tested.

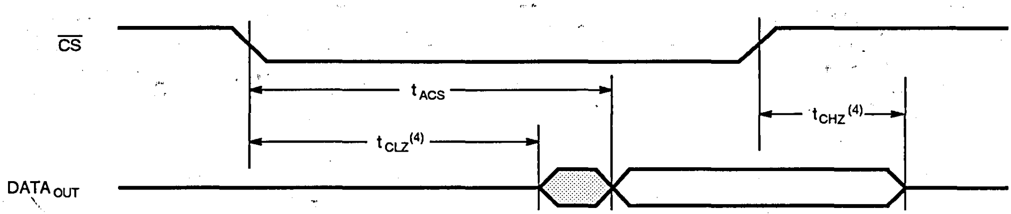
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 3 [1, 3]



NOTES:

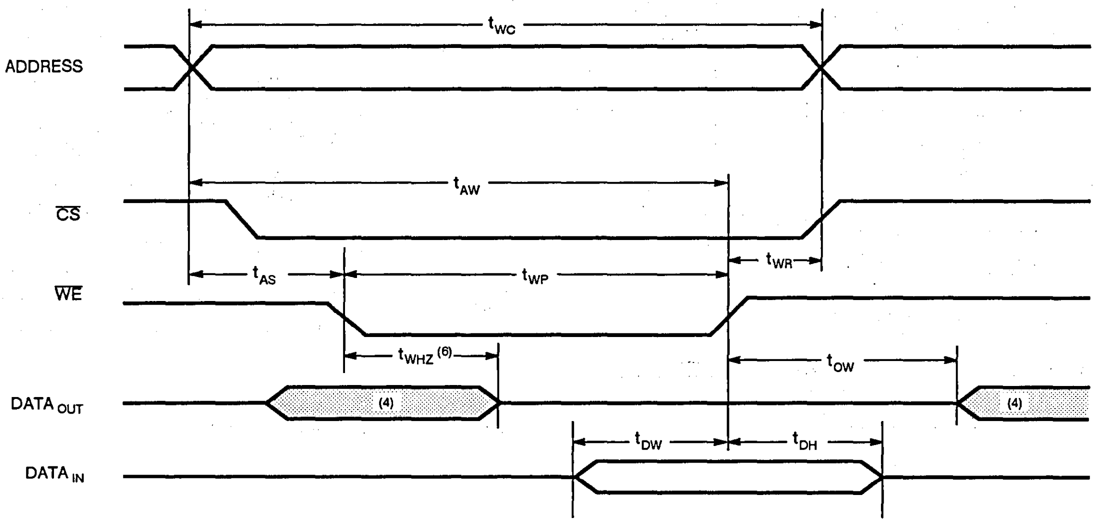
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±10%, All Temperature Ranges

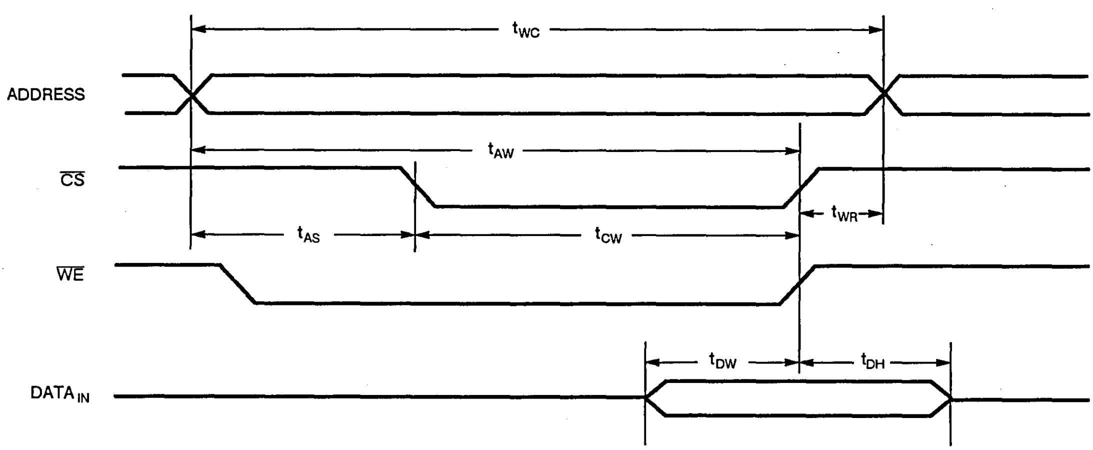
SYMBOL	PARAMETER	IDT71258S25 (1) IDT71258L25 (1) MIN.	MAX.	IDT71258S35 IDT71258L35 MIN.	MAX.	IDT71258S45 IDT71258L45 MIN.	MAX.	IDT71258S55 IDT71258L55 MIN.	MAX.	IDT71258S70 (2) IDT71258L70 (2) MIN.	MAX.	UNIT
WRITE CYCLE												
t_{WC}	Write Cycle Time	20		30	–	40	–	50	–	60	–	ns
t_{CW}	Chip Select to End of Write	20	–	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	20	–	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	20	–	30	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output in High Z (3)	–	13	–	15	–	20	–	25	–	30	ns
t_{DW}	Data Valid to End of Write	15	–	20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write (3)	5	–	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 6)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

ORDERING INFORMATION

IDT XXXX Device Type — A Power — 999 Speed — A Package — A Process/Temperature Range

Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant with MIL-STD-883, Class B
Package	C	Sidebraze DIP
	SO	Small Outline IC
Speed	25	Commercial Only (Speed in Nanoseconds)
	35	
	45	
	55	
	70	Military Only (Speed in Nanoseconds)
Power	L	Low Power
	S	Standard Power
Device Type	71258	256K (64K x 4-Bit) Static RAM

Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (64K x 4-BIT)

IDT61298S
IDT61298L

FEATURES:

- Fast Output Enable ($\overline{OE}$) pin available for added system flexibility
- High speed (equal access and cycle times)
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low power consumption
  - IDT61298S
    Active: 400mW (typ.)
    Standby: 400μw (typ.)
  - IDT61298L
    Active: 350mW (typ.)
    Standby: 100μw (typ.)
- Battery back-up operation—2V data retention (L version only)
- JEDEC standard pinout
- 28-pin sidebraze DIP
- Produced with advanced CEMOS ™ technology
- Bidirectional data inputs and outputs
- Inputs/Outputs TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT61298 is a 262,144-bit high-speed static RAM organized as 64K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

The IDT61298 features two memory control functions: Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). These two functions greatly enhance the IDT61298's overall flexibility in high-speed memory applications.

Access times as fast as 25ns are available with typical power consumption of only 350mW. The IDT61298 offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 100μW when operating from a 2V battery.

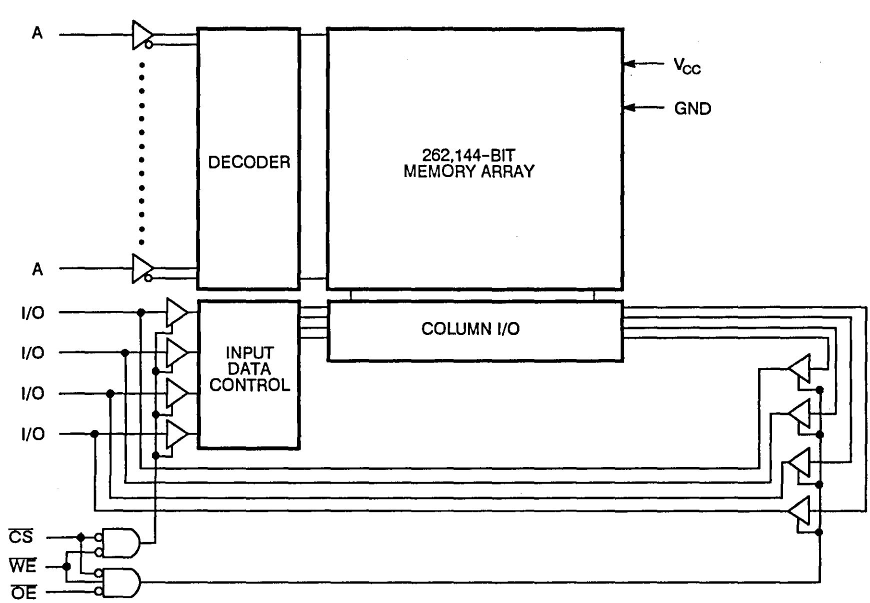
All inputs and outputs are TTL-compatible and the device operates from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT61298 is packaged in a 28-pin sidebraze THINDIP providing improved board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

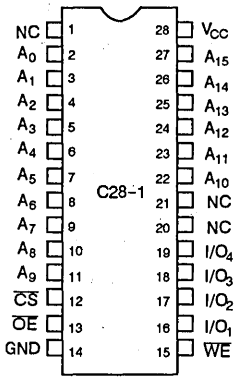
4

FUNCTIONAL BLOCK DIAGRAM



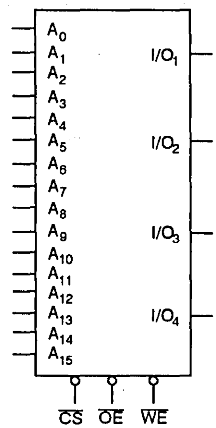
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0–A_{15}	Address Inputs	I/O1-4	Data Input/Output
$\overline{CS}$	Chip Select	V_{CC}	Power
$\overline{WE}$	Write Enable	GND	Ground
$\overline{OE}$	Output Enable		

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

4

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT61298S MIN.	IDT61298S TYP.[1]	IDT61298S MAX.	IDT61298L MIN.	IDT61298L TYP.[1]	IDT61298L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	– –	– –	10 5	– –	– –	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	– –	– –	10 5	– –	– –	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS [1] V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	FUNCTION	IDT61298S25 IDT61298L25		IDT61298S35[2] IDT61298L35[2]		IDT61298S45 IDT61298L45		IDT61298S55 IDT61298L55		IDT61298S70 IDT61298L70		UNIT
				COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[3]	S	READ	60	–	50	60	50	60	50	60	–	60	mA
			WRITE[4]	110	–	100	110	100	110	100	110	–	110	
		L	READ	40	–	30	40	30	40	30	40	–	40	
			WRITE[4]	100	–	90	100	90	100	90	100	–	100	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	S	READ	160	–	150	160	150	160	150	160	–	160	mA
			WRITE[4]	160	–	150	160	150	160	150	160	–	160	
		L	READ	140	–	130	140	130	140	130	140	–	140	
			WRITE[4]	140	–	130	140	130	140	130	140	–	140	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH} V_{CC} = Max., f = f_{MAX}[3] Outputs Open.	S		35	–	35	35	35	35	35	35	–	35	mA
		L		20	–	20	20	20	20	20	20	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC} V_{CC} = Max., f = 0[3]	S		30	–	30	35	30	35	30	35	–	35	mA
		L		1.5	–	1.5	4.5	1.5	4.5	1.5	4.5	–	4.5	

NOTES:
1. All values are maximum guaranteed values.
2. Preliminary data for military devices only.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. Write cycle current specifications are included to aid in the design of extremely sensitive applications. It should be noted that in most systems the ratio of read cycles to write cycles is extremely high. When calculating total current consumption, the designer should weight these figures by the percentage of "On" time as well as the anticipated ratio of read to write cycles (usually greater than 90%).

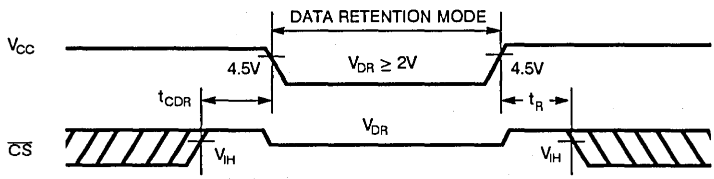
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL.	–	50	75	2000	3000	µA
			COM'L.	–	50	75	500	750	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:
1. $T_A = +25°C$
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

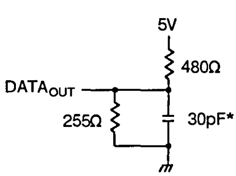


Figure 1. Output Load

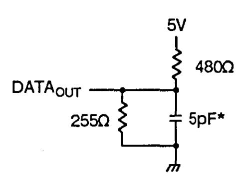


Figure 2. Output Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

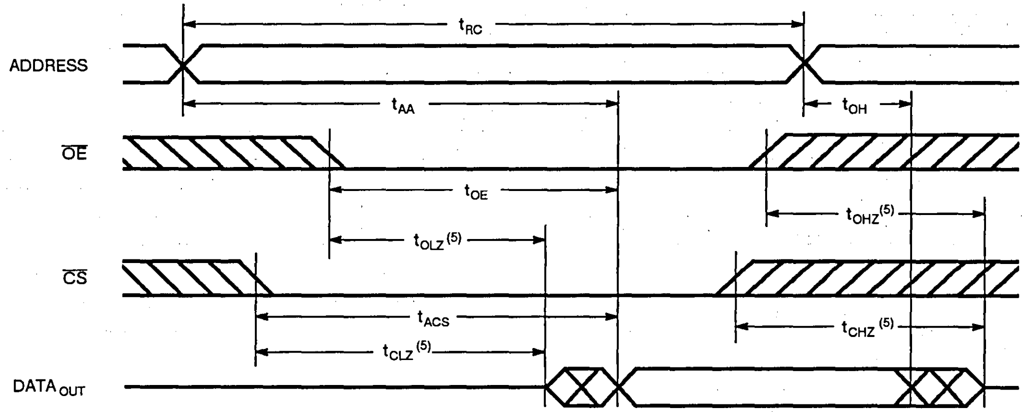
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	61298S25[1] 61298L25[1] MIN.	MAX.	61298S35[4] 61298L35[4] MIN.	MAX.	61298S45 61298L45 MIN.	MAX.	61298S55 61298L55 MIN.	MAX.	61298S70[2] 61298L70[2] MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	25	–	35	–	45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time	–	30	–	35	–	45	–	55	–	70	ns
t_{CLZ} (3)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	15	–	25	–	30	–	35	–	45	ns
t_{OLZ} (3)	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ} (3)	Chip Select to Output in High Z	–	13	–	15	–	20	–	25	–	30	ns
t_{OHZ} (3)	Output Disable to Output in High Z	–	13	–	15	–	15	–	20	–	25	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{PU} (3)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD} (3)	Chip Deselect to Power Down Time	–	25	–	35	–	45	–	55	–	70	ns

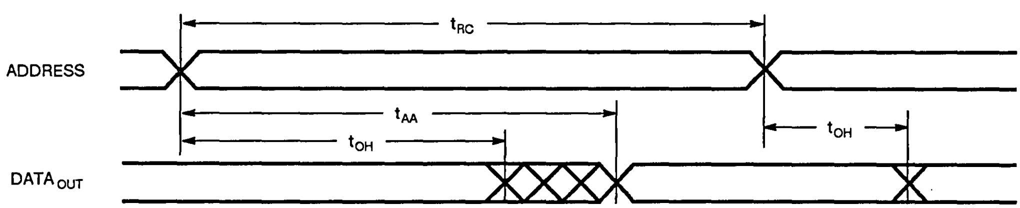
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. Preliminary data for military devices only.

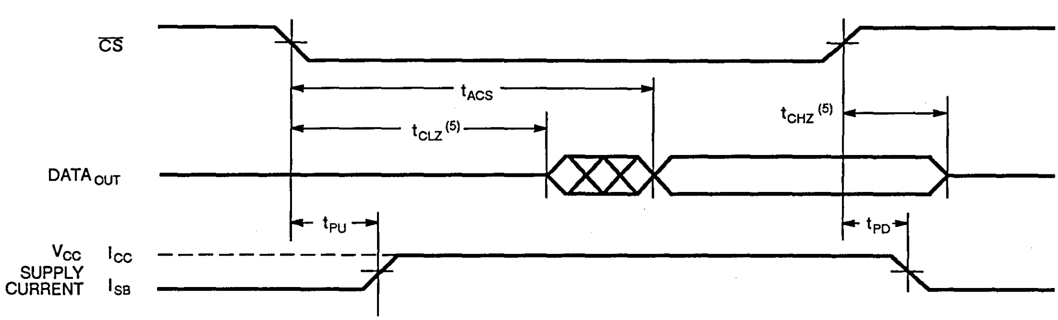
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

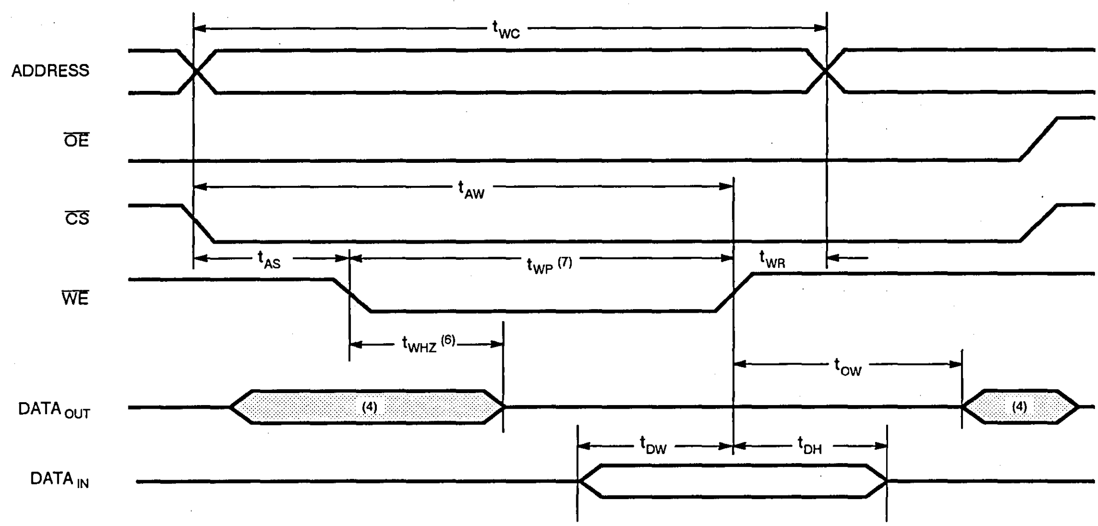
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

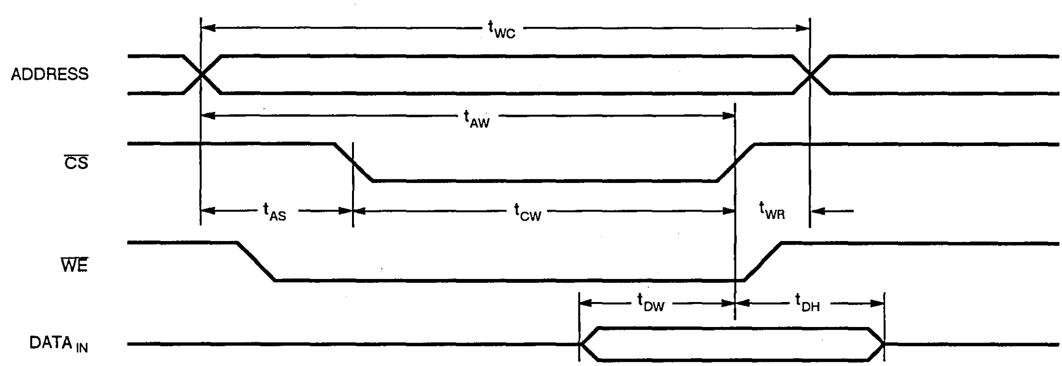
SYMBOL	PARAMETER	61298S25 (1) 61298L25 (1)		61298S35 (4) 61298L35 (4)		61298S45 61298L45		61298S55 61298L55		61298S70(2) 61298L70(2)		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE												
t_{WC}	Write Cycle Time	20	–	30	–	40	–	50	–	60	–	ns
t_{CW}	Chip Select to End of Write	20	–	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	20	–	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	20	–	30	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ} (3)	Write Enable to Output in High Z	–	13	–	15	–	20	–	25	–	30	ns
t_{DW}	Data Valid to End of Write	15	–	20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns
t_{OW} (3)	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. Preliminary data for military devices only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ}+ t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	POWER
Standby	H	X	X	High Z	Standby
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active
Read	L	H	H	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:

1. This parameter is determined by device characterization but is not production tested.

ORDERING INFORMATION

IDT 61298 (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range:
- Blank — Commercial (0°C to +70°C)
- B — Military (-55°C to +125°C) Compliant with MIL-STD-883, Class B

Package:
- C — Sidebraze DIP

Speed in Nanoseconds:
- 25 — Commercial only
- 35
- 45
- 55
- 70 — Military Only

Power:
- S — Standard Power
- L — Low Power

Device Type:
- 61298 — 64K x 4-Bit

Integrated Device Technology, Inc.

CMOS STATIC RAMS 256K (64K x 4-BIT)

Separate Data Inputs and Outputs

PRELIMINARY
IDT71281S/L
IDT71282S/L

FEATURES:

- Separate data inputs and outputs
- IDT71281S/L: outputs track inputs during write mode
- IDT71282S/L: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low power consumption
  - IDT71281/2S
    Active: 400mW (typ.)
    Standby: 400μw (typ.)
  - IDT71281/2L
    Active: 350mW (typ.)
    Standby: 100μw (typ.)
- Battery backup operation—2V data retention (L version only)
- High-density 28-pin DIP
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71281/IDT71282 are 262,144-bit high-speed static RAMs organized as 64K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

Access times as fast as 25ns are available with typical power consumption of only 350mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, this standby mode. The ultra-low-power standby mode capability provides significant system-level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 100μW operating off a 2V battery.

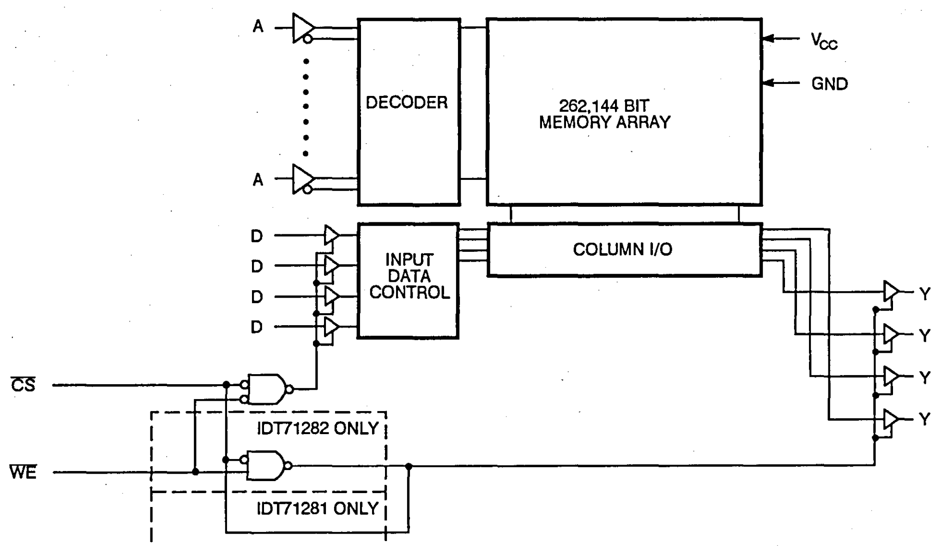
All inputs and outputs of the IDT71281/IDT71282 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT71281/IDT71282 are packaged in 28-pin sidebraze DIPs, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

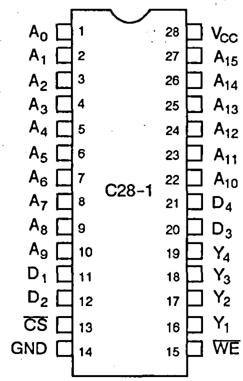
4

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

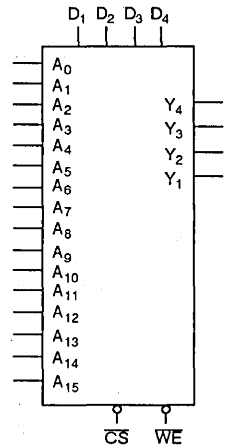


DIP
TOP VIEW

PIN NAMES

A_0-A_{15}	Address Inputs	D_1-D_4	$DATA_{IN}$
$\overline{CS}$	Chip Select	Y_1-Y_4	$DATA_{OUT}$
$\overline{WE}$	Write Enable	GND	Ground
V_{CC}	Power		

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS (for all speeds)

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT71281/2S MIN.	IDT71281/2S TYP.[1]	IDT71281/2S MAX.	IDT71281/2L MIN.	IDT71281/2L TYP.[1]	IDT71281/2L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	FUNCTION	71281/2S25 71281/2L25 COM'L.	MIL.	71281/2S35[2] 71281/2L35[2] COM'L.	MIL.	71281/2S45 71281/2L45 COM'L.	MIL.	71281/2S55 71281/2L55 COM'L.	MIL.	71281/2S70 71281/2L70 COM'L.	MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[2]	S	READ	60	–	50	60	50	60	50	60	–	60	mA
			WRITE[4]	130	–	120	130	120	130	120	130	–	130	
		L	READ	40	–	30	40	30	40	30	40	–	40	
			WRITE[4]	120	–	110	120	110	120	110	120	–	120	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	S	READ	160	–	150	160	150	160	150	160	–	160	mA
			WRITE[4]	170	–	160	170	160	170	160	170	–	170	
		L	READ	140	–	130	140	130	140	130	140	–	140	
			WRITE[4]	150	–	140	150	140	150	140	150	–	150	
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	S		35	–	35	35	35	35	35	35	–	35	mA
		L		20	–	20	20	20	20	20	20	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., f = 0[2]	S		30	–	30	35	30	35	30	35	–	35	mA
		L		1.5	–	1.5	4.5	1.5	4.5	1.5	4.5	–	4.5	

NOTES:

1. All values are maximum guaranteed values.
2. Preliminary data for military devices only.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. Write cycle current specifications are included to aid in the design of extremely sensitve applications. It should be noted that, in most systems, the ratio of read cycles to write cycles is extremely high. When calculating total current consumption, the designer should weight these figures by the percentage of "On" time as well as the anticipated ratio of read to write cycles (usually greater than 90%).

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

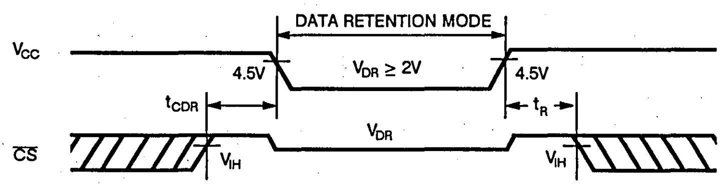
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.[1] V_{CC} @ 2.0V	TYP.[1] V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL.	–	50	75	2000	3000	µA
			COM'L.	–	50	75	500	750	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–		–		ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–		–		ns
$\|I_{LI}\|$[3]	Input Leakage Current			–	–		2		µA

NOTES:

1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

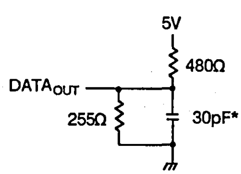


Figure 1. Output Load

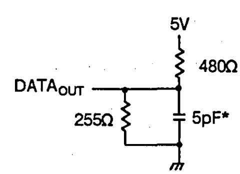


Figure 2. Output Load (for t_{CLZ}, t_{CHZ}, t_{OW} and t_{WHZ})

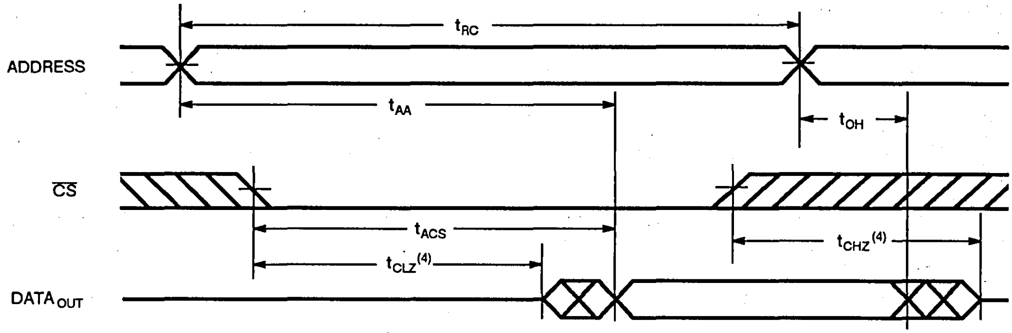
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

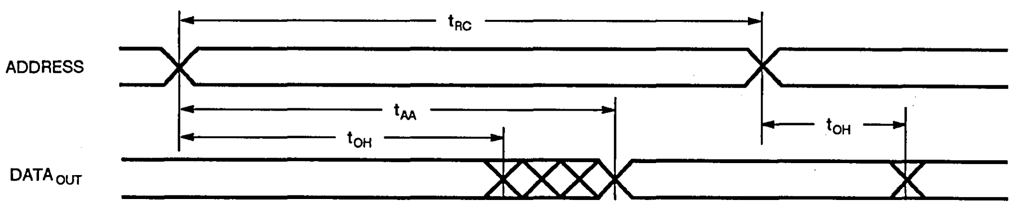
SYMBOL	PARAMETER	71281/2S25 (1) 71281/2L25 (1) MIN.	MAX.	71281/2S35 (5) 71281/2L35 (5) MIN.	MAX.	71281/2S45 71281/2L45 MIN.	MAX.	71281/2S55 71281/2L55 MIN.	MAX.	71281/2S70 (2) 71281/2L70 (2) MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	25	–	35	–	45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time (3)	–	30	–	35	–	45	–	55	–	70	ns
t_{CLZ}	Chip Select to Output in Low Z (4)	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Select to Output in High Z (4)	–	13	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time (4)	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time (4)	–	25	–	35	–	45	–	55	–	70	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.
5. Preliminary data for military devices only.

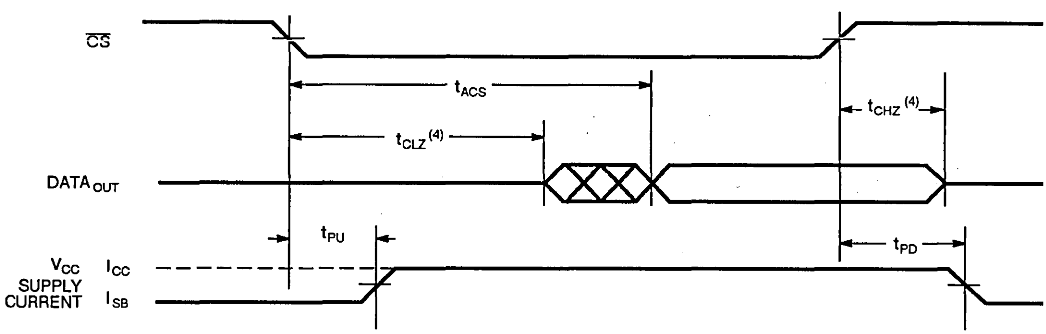
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3]



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state.

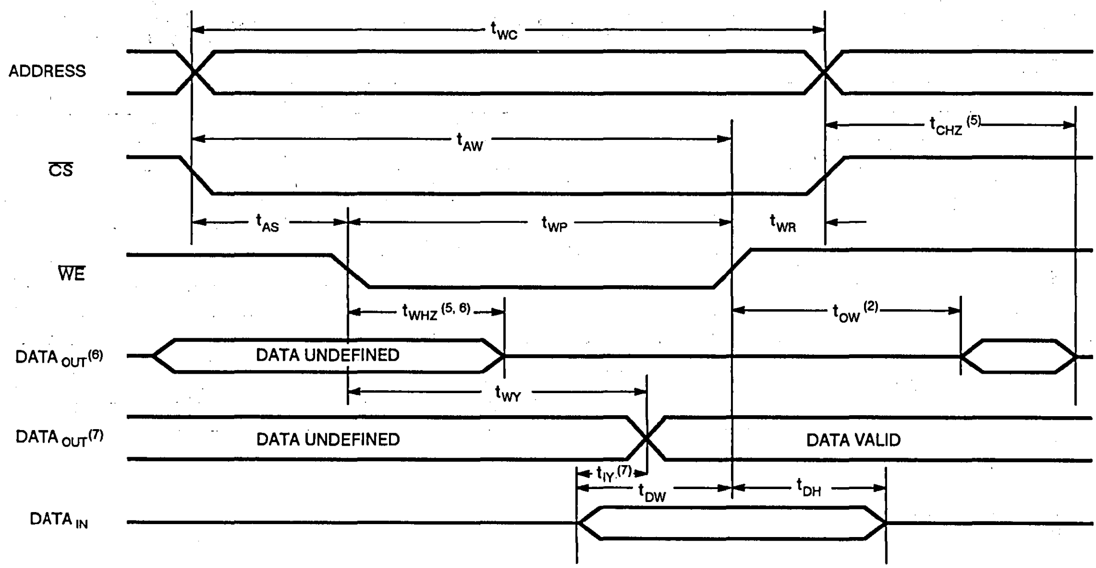
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	71281/2S25 (1) 71281/2L25 (1) MIN.	MAX.	71281/2S35(7) 71281/2L35(7) MIN.	MAX.	71281/2S45 71281/2L45 MIN.	MAX.	71281/2S55 71281/2L55 MIN.	MAX.	71281/2S70 (2) 71281/2L70 (2) MIN.	MAX.	UNIT
WRITE CYCLE												
t_{WC}	Write Cycle Time	20	–	30	–	40	–	50	–	60	–	ns
t_{CW}	Chip Select to End of Write (3)	20	–	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	20	–	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	20	–	30	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output in High Z (4, 6)	–	13	–	15	–	20	–	25	–	30	ns
t_{DW}	Data Valid to End of Write	15	–	20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write (4, 6)	5	–	5	–	5	–	5	–	5	–	ns
t_{IY}	Data Valid to Output Valid (4, 5)	–	20	–	30	–	35	–	40	–	45	ns
t_{WY}	Write Enable to Output Valid (4, 5)	–	20	–	30	–	35	–	40	–	45	ns

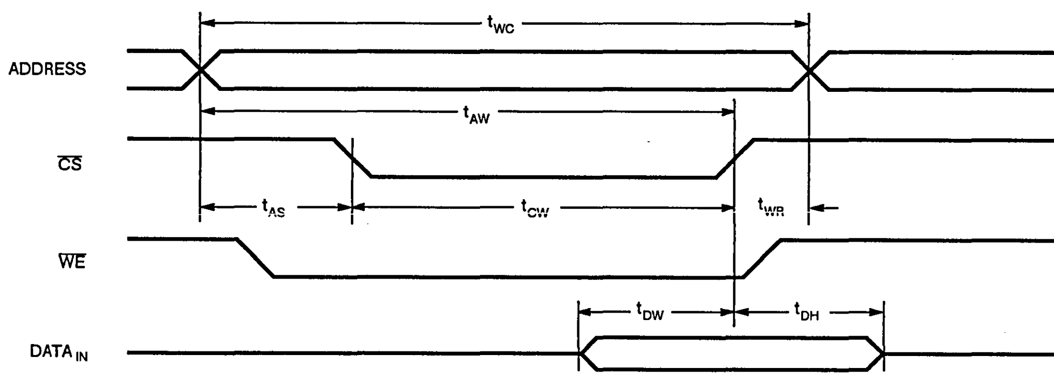
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.
5. For IDT71281S/L only.
6. For IDT71282S/L only.
7. Preliminary data for military devices only.

4

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 4]



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$, and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state (IDT71282 only).
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
6. IDT71282 only.
7. IDT71281 only.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write (1)	L	L	D_{IN}	Active
Write (2)	L	L	High Z	Active

NOTES:
1. For IDT71281 only.
2. For IDT71282 only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

ORDERING INFORMATION

IDT XXXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	C	Sidebraze DIP
Speed	25	Commercial Only
	35	
	45	Speed in Nanoseconds
	55	
	70	Military Only
Power	S	Standard Power
	L	Low Power
Device Type	71281	256K (64K x 4-Bit)
	71282	256K (64K x 4-Bit) High Impedance Outputs

Integrated Device Technology, Inc.

256K (64K x 4-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

IDT7MP456

FEATURES:

- High-density 256K (64K x 4) CMOS static RAM module
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Available in 28-pin SIP (single in-line package) for maximum space saving
- Fast access times: 25ns (max.) over commercial temperature
- Low power consumption
  - Dynamic: less than 1.2W (typ.)
  - Full standby: less than 30 mW(typ.)
- Utilizes IDT7187 high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

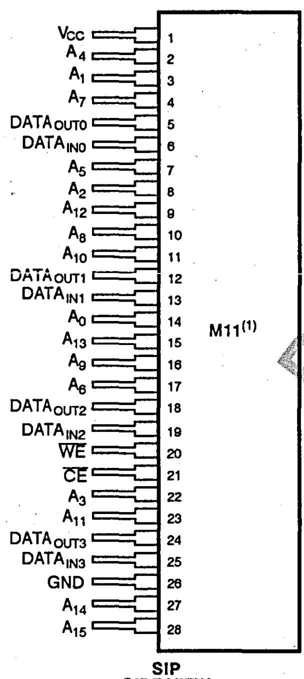
The IDT7MP456 is a 256K (64K x 4-bit) high-speed static RAM module constructed on an epoxy laminate surface using four IDT7187 64K x 1 static RAMs in plastic surface mount packages. Extremely fast speeds can be achieved with this technique due to the use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS technology .

The 7MP family of surface mounted SIP technology is a cost-effective solution allowing for very high packing density. The IDT7MP456 is offered in a 28-pin SIP. The IDT7MP456 can be mounted on 200 mil centers, yielding 1.25 megabits of memory in less than 3 square inches of board space.

The IDT7MP456 is available with maximum access times as fast as 25ns, with maximum power consumption of 3.3 watts. The module also offers a full standby mode of 440mW(max.).

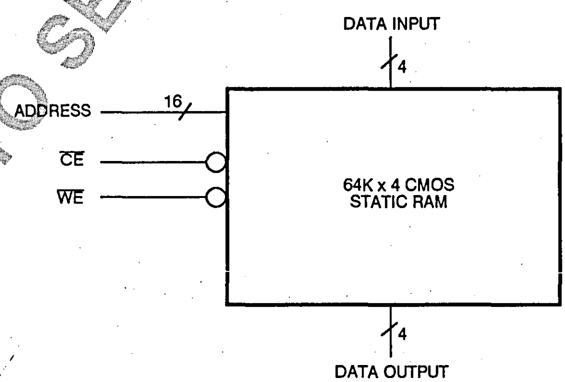
All inputs and outputs of the IDTMP456 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

PIN CONFIGURATION



SIP
SIDE VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{15}	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
D_{IN0} - D_{IN3}	Data Input
D_{OUT0} - D_{OUT3}	Data Output
V_{CC}	Power
GND	Ground

NOTE:

1. For module dimensions, please refer to module drawing M11 in the packaging section.

Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (32K x 8-BIT)

PRELIMINARY
IDT71256S
IDT71256L

FEATURES:

- High-speed address/chip select time
  - Military: 45/55/70/85ns (max.)
  - Commercial: 35/45/55/70ns (max.)
- Low-power operation
  - IDT71256S
    Active: 300mW (typ.)
    Standby: 200μW (typ.)
  - IDT71256L
    Active: 250mW (typ.)
    Standby: 15μW (typ.)
- Battery Backup operation—2V data retention
- Produced with advanced high-performance CEMOS ™ technology
- Single 5V(±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 28-pin CERDIP and plastic DIP (600 mil), 28-pin SOIC and 32-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-88552 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

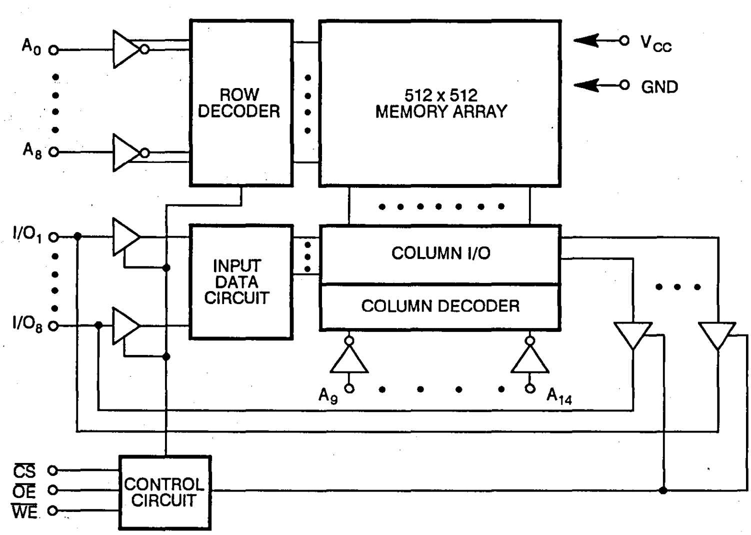
Address access times as fast as 35ns are available with power consumption of only 300mW (typ.). The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a low-power standby mode as long as $\overline{CS}$ remains high. In the full standby mode, the low-power device consumes less than 15μW, typically. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 5μW when operating off a 2V battery.

All inputs and outputs of the IDT71256 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT71256 is packaged in a 28-pin SOIC, a 28-pin 600 mil CERDIP or plastic DIP and 32-pin leadless chip carrier and PLCC, providing high board-level packing densities.

The IDT71256 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

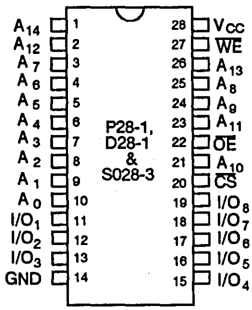
FUNCTIONAL BLOCK DIAGRAM



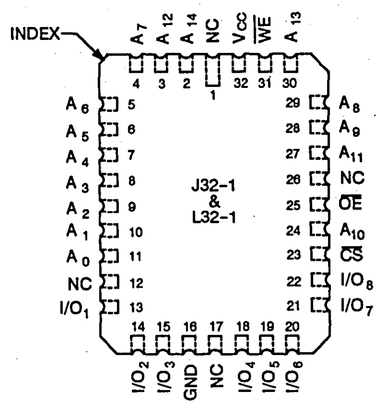
CEMOS is a trademark of Integrated Device Technology, Inc.

DSC-1015/-

PIN CONFIGURATIONS

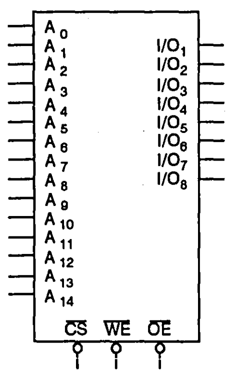


DIP/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0 - A_{14}	Addresses
I/O_1 - I/O_8	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
V_{CC}	Power

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71256S MIN.	IDT71256S MAX.	IDT71256L MIN.	IDT71256L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		–	0.4	–	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS[1, 3] V_{CC} = 5V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	FUNCTION	IDT71256x35 COM'L.	IDT71256x35 MIL.	IDT71256x45 COM'L.	IDT71256x45 MIL.	IDT71256x55 COM'L.	IDT71256x55 MIL.	IDT71256x70 COM'L.	IDT71256x70 MIL.	IDT71256x85 COM'L.	IDT71256x85 MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0	S	READ	30	–	30	40	30	40	30	40	–	40	mA
			WRITE[2]	90	–	90	100	90	100	90	100	–	100	
		L	READ	15	–	15	20	15	20	15	20	–	20	
			WRITE[2]	80	–	80	90	80	90	80	90	–	90	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[4]	S	READ	155	–	140	150	140	150	140	150	–	150	mA
			WRITE[2]	150	–	140	150	140	150	140	150	–	150	
		L	READ	135	–	110	120	90	100	75	85	–	70	
			WRITE[2]	130	–	115	125	105	115	95	105	–	90	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, f = f_{MAX}[4] V_{CC} = Max., Outputs Open.	S		20	–	20	20	20	20	20	20	–	20	mA
		L		3	–	3	3	3	3	3	3	–	3	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, f = 0 V_{CC} = Max.	S		15	–	15	20	15	20	15	20	–	20	mA
		L		0.4	–	0.4	1.5	0.4	1.5	0.4	1.5	–	1.5	

NOTES:
1. All values are maximum guaranteed values.
2. Write cycle current specifications are included to aid in the design of extremely sensitive applications. It should be noted that in most systems the ratio of Read cycles to Write cycles is extremely high. When calculating total current consumption, the designer should weight these figures by the percentage of "On" time as well as the anticipated ratio of Read to Write cycles (usually greater than 90%).
3. "x" in part numbers indicates power rating (S or L).
4. f_{MAX} = $1/t_{RC}$

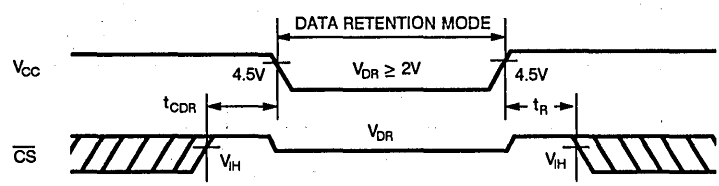
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL.	–	–	–	500	800	µA
			COM'L.	–			120	200	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–	–	–	–	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–	–	–	–	ns

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

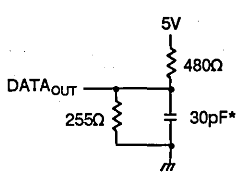


Figure 1. Output Load

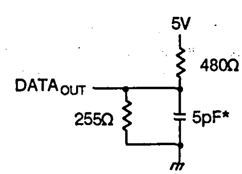


Figure 2. Output Load (for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, t_{OW})

* Including scope and jig.

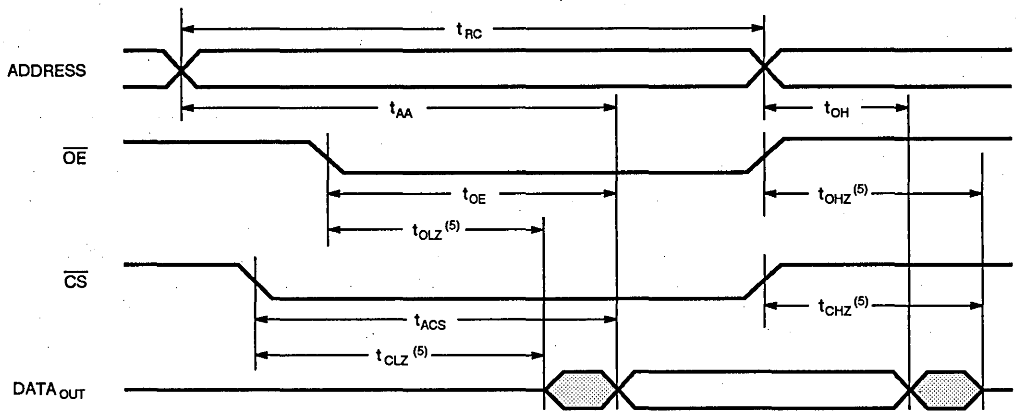
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71256S35 (1) IDT71256L35 (1) MIN.	MAX.	IDT71256S45 IDT71256L45 MIN.	MAX.	IDT71256S55 IDT71256L55 MIN.	MAX.	IDT71256S70 IDT71256L70 MIN.	MAX.	IDT71256S85 (2) IDT71256L85 (2) MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	35	–	45	–	55	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	35	–	45	–	55	–	70	–	85	ns
t_{ACS}	Chip Select Access Time	–	35	–	45	–	55	–	70	–	85	ns
t_{CLZ}	Chip Select to Output in Low Z (3)	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	15	–	20	–	25	–	30	–	35	ns
t_{OLZ}	Output Enable to Output in Low Z (3)	0	–	0	–	0	–	0	–	0	–	ns
t_{CHZ}	Chip Deselect to Output in High Z (3)	–	15	–	20	–	25	–	30	–	35	ns
t_{OHZ}	Output Disable to Output in High Z (3)	–	15	–	20	–	25	–	30	–	35	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns

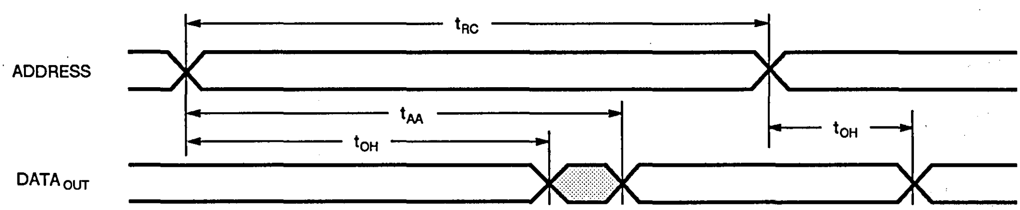
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed, but not tested.

4

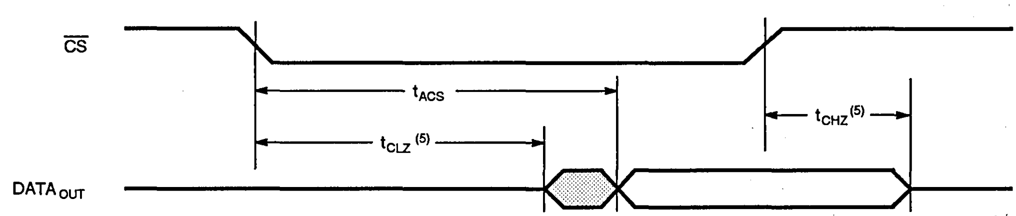
TIMING WAVEFORM OF READ CYCLE NO. 1 [1]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 3 [1, 3, 4]



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

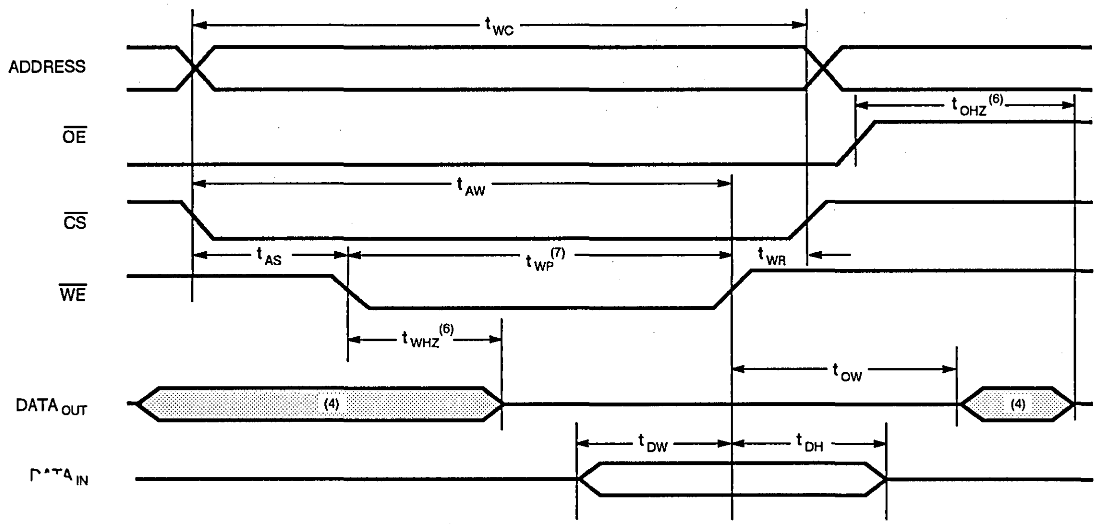
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71256S35[1] IDT71256L35[1] MIN.	MAX.	IDT71256S45 IDT71256L45 MIN.	MAX.	IDT71256S55 IDT71256L55 MIN.	MAX.	IDT71256S70 IDT71256L70 MIN.	MAX.	IDT71256S85[2] IDT71256L85[2] MIN.	MAX.	UNIT
WRITE CYCLE												
t_{WC}	Write Cycle Time	35	–	45	–	55	–	70	–	85	–	ns
t_{CW}	Chip Select to End of Write	30	–	40	–	50	–	60	–	70	–	ns
t_{AW}	Address Valid to End of Write	30	–	40	–	50	–	60	–	70	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	30	–	35	–	40	–	45	–	50	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write to Output in High Z[3]	–	15	–	20	–	25	–	30	–	35	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold from Write Time	3	–	3	–	3	–	3	–	3	–	ns
t_{OW}	Output Active from End of Write[3]	5	–	5	–	5	–	5	–	5	–	ns

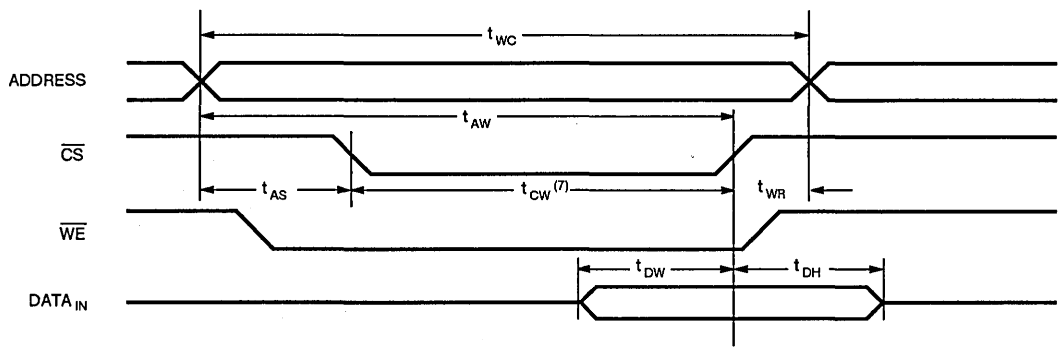
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed, but not tested.

4

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 5, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

TRUTH TABLE V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	FUNCTION
X	H	X	Hi-Z	Standby (I_{SB})
X	V_{HC}	X	Hi-Z	Standby (I_{SB1})
H	L	H	Hi-Z	Output Disable
H	L	L	$DATA_{OUT}$	Read
L	L	X	$DATA_{IN}$	Write

NOTE:
1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	SO	Small Outline IC
	J	Plastic Leaded Chip Carrier
	L	Leadless Chip Carrier
Speed	35	Commercial Only
	45	
	55	Speed in Nanoseconds
	70	
	85	Military Only
Power	L	Low Power
	S	Standard Power
Device Type	71256	256K (32K x 8-Bit) Static RAM

Integrated Device Technology, Inc.

256K (32K x 8-BIT) CMOS STATIC RAM MODULE (Low-Power Version)

IDT8M856L

FEATURES:

- High-density 256K (32K x 8-bit) CMOS static RAM module
- Equivalent to JEDEC standard for future monolithic 32K x 8 static RAMs
- High-speed—45ns (max.) commercial; 55ns (max.) military
- Low power consumption; typically less than 225mW operating, less than 500μW in full standby
- Utilizes IDT7164s—high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Pin-compatible with IDT7M864 (8K x 8 SRAM module)
- Offered in the JEDEC standard 28-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT8M856 is a 256K (32,768 x 8-bit) high-speed static RAM constructed on a co-fired ceramic substrate using four IDT7164 (8,192 x 8) static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic 256K static RAMs is achieved by utilization of an on-board decoder circuit that interprets the higher order address A_{13} and A_{14} to select one of the four 8K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 64K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

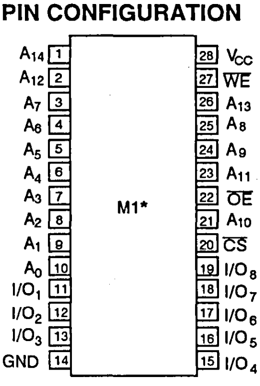
The IDT8M856 is available with maximum access times as fast as 45ns for commercial and 55ns for military temperature ranges, with maximum power consumption of only 825mW. The circuit also offers a substantially low-power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to a standby mode with power consumption of only 83mW (max.).

The IDT8M856 is offered in a 28-pin, 600 mil center sidebraze DIP. This provides four times the density of the IDT7M864 (8K x 8 module) in the same socket, with only minor pin assignment changes. In addition, the JEDEC standard for 256K monolithic pinouts has been adhered to, allowing for compatibility with 256K monolithics.

All inputs and outputs of the IDT8M856 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

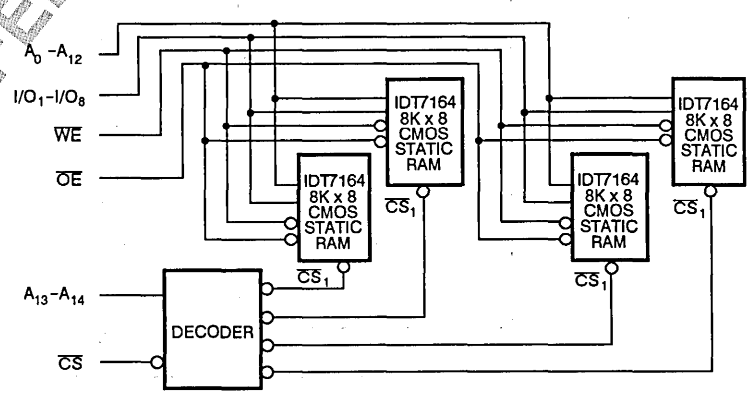
All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



NOTE:
* For module dimensions, please refer to module drawing M1 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN NAMES

$A_0 - A_{14}$	Addresses	$\overline{WE}$	Write Enable
$I/O_1 - I/O_8$	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	GND	Ground
V_{CC}	Power		

Integrated Device Technology, Inc.

256K CMOS STATIC RAM MODULE

IDT7M656L

FEATURES:

- High-density 256K-bit CMOS static RAM module
- Customer-configured to 16Kx16, 32Kx8 or 64Kx4
- Fast access times
  - Military: 20ns
  - Commercial: 15ns
- Low power consumption
  - Active: 3.2mW (typ.) (in 16K x 16 organization)
  - Standby: 0.16mW (typ.)
- Utilizes 16 IDT6167s high-performance 16K x 1 CMOS static RAMs produced with IDT's advanced CEMOS ™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Single 5V (±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Module available with semiconductor components compliant to MIL-STD-883, Class B.

DESCRIPTION:

The IDT7M656 is a 256K-bit high-speed CMOS static RAM constructed on a multilayered ceramic substrate using 16 IDT6167 (16Kx1) static RAMs in leadless chip carriers. Making 4 chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 16Kx16, 32Kx8 or 64Kx4 organization. In addition, extremely high speeds are achievable by the use of IDT6167s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides some of the fastest 16K static RAMs available.

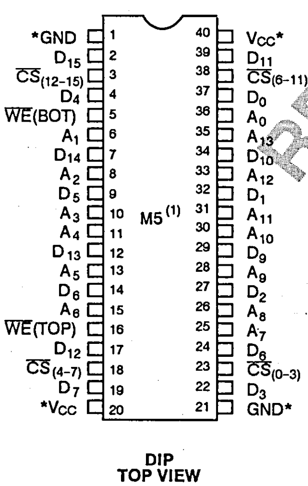
The IDT7M656 is available with access times as fast as 15ns commercial and 20ns military temperature range, with maximum operating power consumption of only 7.9W (significantly less if organized 32Kx8 or 64Kx4). The RAM module also offers a maximum standby power mode of 3.0W and a maximum full standby mode of 176mW.

The IDT7M656 is offered in a high-density 40-pin, 900 mil center sidebraze DIP to take full advantage of the compact IDT6167s in leadless chip carriers.

All inputs and outputs of the IDT7M656 are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

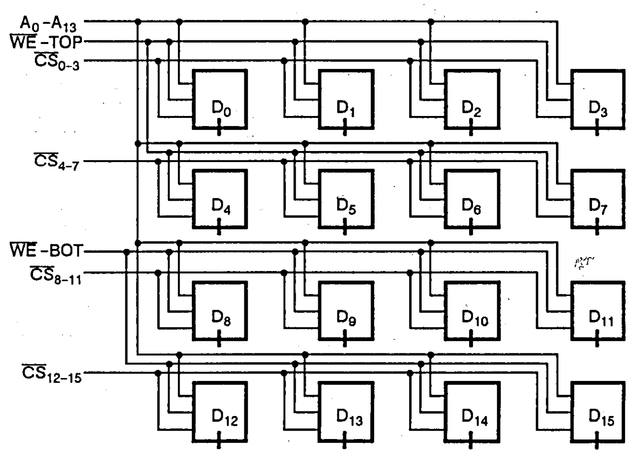
PIN CONFIGURATION



DIP
TOP VIEW

1. For module dimensions, please refer to module drawing M5 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{xx}	Addresses	D_{xx}	$DATA_{IN/OUT}$
$\overline{CS}_{xx}$	Chip Selects	V_{CC}	Power
$\overline{WE}_{xx}$	Write Enable	GND	Ground

256K (16K x 16-BIT) & 128K (8K x 16-BIT) CMOS STATIC RAM PLASTIC SIP MODULES

IDT8MP656S
IDT8MP628S

FEATURES:

- High-density 256K/128K CMOS static RAM modules
- 16K x 16 organization (IDT8MP656S) with 8K x 16 option (IDT8MP628)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  - Flexibility in application
- Fast access times
  - 40ns (max.)
- Low power consumption
  - Active: less than 825mW (typ. in 16K x 16 organization)
  - Standby: less than 20mW (typ.)
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Offered in an SIP (single in-line) package for maximum space-savings
- Utilizes IDT7164s—high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT8MP656S/IDT8MP628S are 256K/128K-bit high-speed CMOS static RAMs constructed on an epoxy laminate substrate using four IDT7164 8K x 8 static RAMs (IDT8MP656S) or two IDT7164 static RAMs (IDT8MP628S) in plastic surface mount packages.

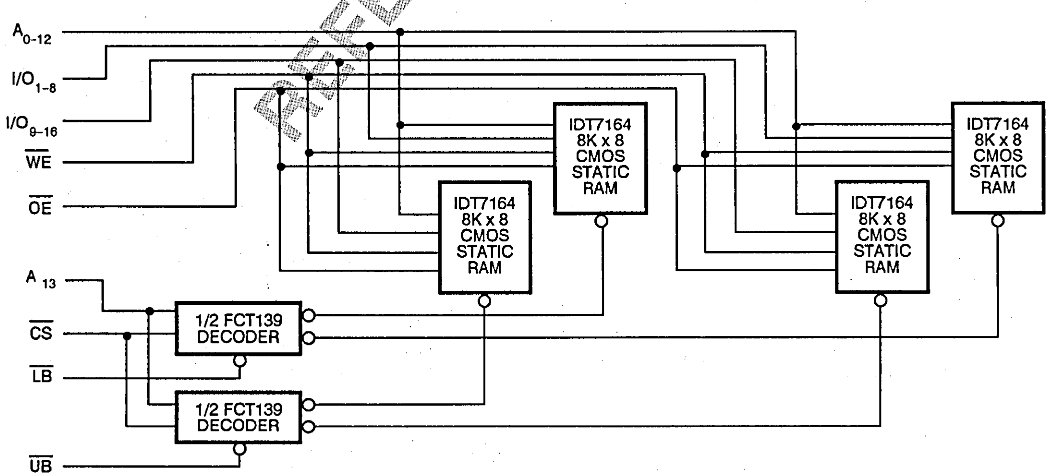
Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{13} to select one of the two 8K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On the IDT8MP628S 8K x 16 option, A_{13} needs to be externally grounded for proper operation.) Extremely high speeds are achievable by the use of IDT7164s, fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 256K/128K static RAMs available.

The IDT8MP656S/IDT8MP628S are available with maximum operating power consumption of only 1.8W (IDT8MP656S 16K x 16 option). The modules also offer a full standby mode of 330mW (max.).

The IDT8MP656S/IDT8MP628S are offered in a 40-pin plastic SIP. For the JEDEC standard 40-pin DIP, refer to the IDT8M656S/IDT8M628S.

All inputs and outputs of the IDT8MP656S/IDT8MP628S are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

DSC-7016/-

256K (16K x 16-BIT) & 128K (8K x 16-BIT) CMOS STATIC RAM MODULE

IDT8M656S
IDT8M628S

FEATURES:

- High-density 256K/128K-bit CMOS static RAM modules
- 16K x 16 organization (IDT8M656) with 8K x 16 option (IDT8M628)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  - Flexibility in application
- Equivalent to JEDEC standard for future monolithic 16K x 16/8K x 16 static RAMs
- High-speed
  - Military: 50ns (max.)
  - Commercial: 40ns (max.)
- Low power consumption: typically less than 825mW operating (IDT8M656), less than 40mW in standby
- Utilizes IDT7164s—high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 40-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT8M656S/IDT8M628S are 256K/128K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic substrate using four IDT7164 8K x 8 static RAMs (IDT8M656S) or two IDT7164 static RAMs (IDT8M628S) in leadless chip carriers.

Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{13} to select one of the two 8K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On the IDT8M628S 8K x 16 option, A_{13} needs to be externally grounded for proper operation.) Extremely high speeds are achievable by the use of IDT7164s fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 256K/128K static RAMs available.

The IDT8M656S/IDT8M628S are available with access times as fast as 40ns over the commercial temperature range, with maximum operating power consumption of only 1.98W (IDT8M656S 16K x 16 option). The module also offers a full standby mode of 440mW (max.).

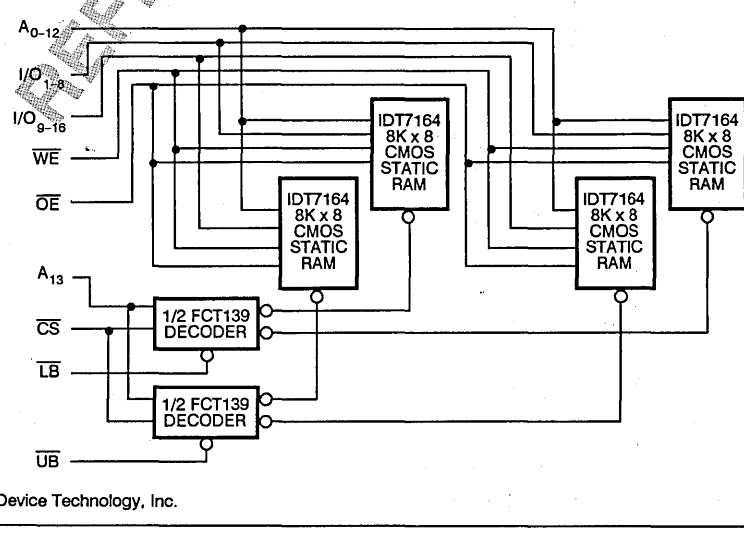
The IDT8M656S/IDT8M628S are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT7164s in leadless chip carriers.

All inputs and outputs of the IDT8M656S/IDT8M628S are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

4

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

DSC-7018/-

512K (64K x 8-BIT or 64K x 9-BIT) CMOS STATIC RAM MODULE

IDT7M812
IDT7M912

Integrated Device Technology, Inc.

FEATURES:

- High-density 512K-bit CMOS static RAM module
- 64K x 8 (IDT7M812) or 64K x 9 (IDT7M912) configuration
- Fast access times
  - Military: 35ns (max.)
  - Commercial: 25ns (max.)
- Low power consumption
  - Active: 2.4W (typ. in 64K x 8 organization)
  - Standby: 240µW (typ. in 64K x 8 organization)
- Utilizes 8 (IDT7M812) or 9 (IDT7M912) IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in 40-pin, 600 mil center sidebraze DIP, achieving very high memory density
- Single 5V(±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT7M812/IDT7M912 are 512K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic substrate using 8 IDT7187 64K x 1 static RAMs (IDT7M812) or 9 IDT7187 static RAMs (IDT7M912) in leadless chip carriers. Extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

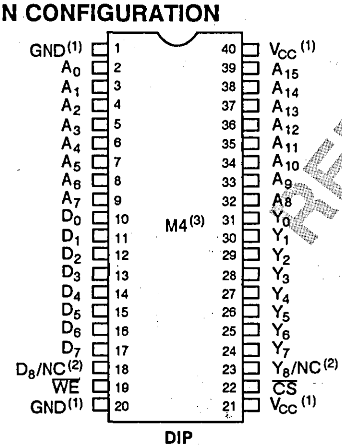
The IDT7M812/IDT7M912 are available with access times as fast as 25ns commercial and 35ns military temperature range, with maximum operating power consumption of only 6.9W (IDT7M912, 64K x 9 option). The module also offers a standby power mode of less than 3.2W (max.) and a full standby mode of 1.2W (max.).

The IDT7M812/IDT7M912 are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT7187s in leadless chip carriers. The IDT7M912 (64K x 9) option can provide more flexibility in system application for error detection, parity bit, etc.

All inputs and outputs of the IDT7M812/IDT7M912 are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing access and cycles times for ease of use.

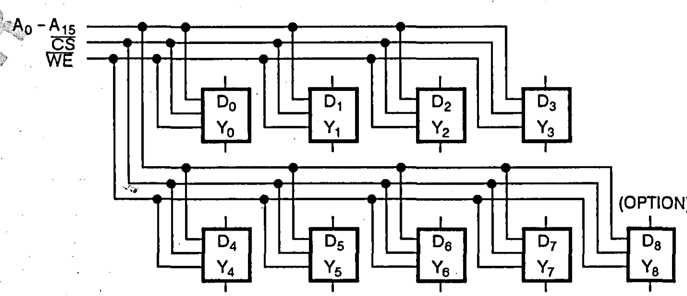
All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{15}	Address
D_0-D_8	Data Input
Y_0-Y_8	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

NOTES:

1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. Pin 18 is D_8 and pin 23 is Y_8 in 64K x 9 (IDT7M912) option and both 18 and 23 are NC in 64K x 8 (IDT7M812) option.
3. For module dimensions, please refer to module drawing M4 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

512K (16K x 32) CMOS STATIC RAM DUAL CERAMIC SIP MODULE WITH SEPARATE I/O

ADVANCE INFORMATION
IDT7MC4032

FEATURES:

- High-density 32 bit word 512K (16K x 32) static RAM module
- Available in low profile 88-pin sidebraze dual ceramic SIP (single in-line package)
- Separate I/O
- Fast access time: 30ns (max.)
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- High impedance outputs during write mode
- CEMOS ™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled in IDT's high reliability vapor phase solder reflow process
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible
- Multiple GND pins for maximum noise immunity

DESCRIPTION:

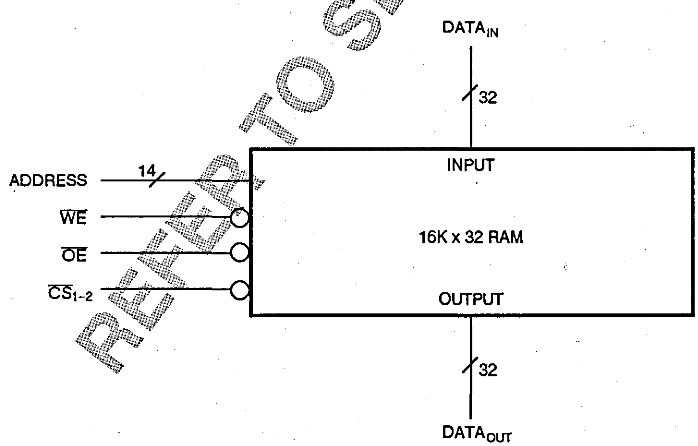
The IDT7MC4032 is a 32-bit wide 512K (16K x 32) static RAM module with separate I/O constructed on a co-fired ceramic substrate using eight IDT71982 16K x 4 static RAMs in leadless chip carriers. Extremely fast speeds can be achieved due to the use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS ™ technology. The IDT7MC4032 is available with access time as fast as 30ns, with minimal power consumption.

4

The 7MC family of ceramic SIPs offers the optimum is packing density and profile height. The IDT7MC4032 is packaged in a 88-pin dual ceramic SIP. The dual row configuration allows 88 pins to be placed on a package less than 4.5 inches long and .27 inches wide. At only 520 mils high, this profile package is ideal for systems with minimum board spacing. Extremely high packing density can also be achieved allowing four IDT7MC4032 modules to be stacked per inch of board space.

All inputs and outputs of the IDT7MC4032 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

Integrated Device Technology, Inc.

CMOS STATIC RAM 1 MEG (1,024K x 1-BIT)

ADVANCE INFORMATION
IDT71027S
IDT71027L

FEATURES:

- One full megabit of static RAM in popular 1,024K x 1 configuration
- High-speed access
  - Military: 55/70/90ns (max.)
  - Commercial: 45/55/70ns (max.)
- Low power consumption
  - IDT71027S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT71027L
    Active: 500mW (typ.)
    Standby: 200µW (typ.)
- Battery backup operation—2V data retention
- Available in 28-pin DIP
- TTL-compatible
- Single 5V (±10%) power supply
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71027 is an extremely high-density (1,024K x 1-bit) high-speed static RAM designed for use in systems where fast computation, low power and board density are of the utmost importance.

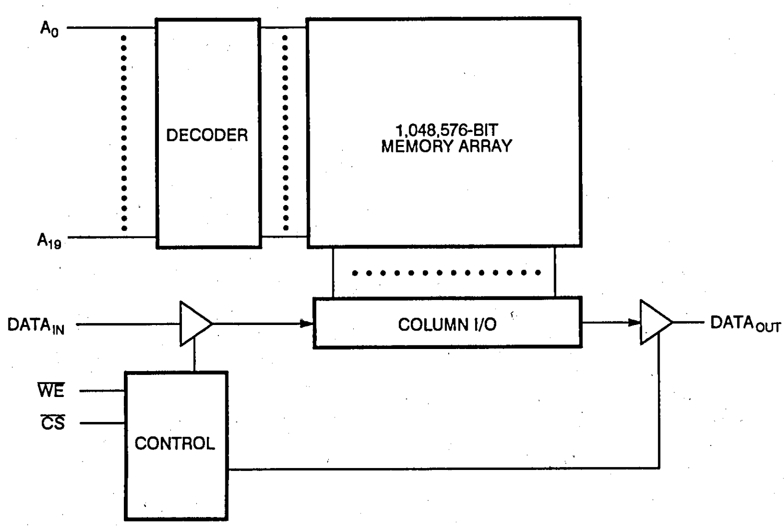
The IDT71027 uses individual input and output lines to provide fast read and write access to all memory locations. This function allows designers to fully utilize the IDT71027's already fast 45ns address access time to achieve a considerable throughput advantage. An automatic power down feature, controlled by $\overline{CS}$, permits the on-chip circuitry to enter a very low standby power mode and be brought back into operation at a speed equal to the address access time.

Fabricated using IDT's CEMOS™ high-performance technology, the IDT71027 typically operates on only 500mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, typically consuming 200µW from a 2V battery.

All inputs and outputs of the IDT71027 are TTL-compatible and the device operates from a standard 5V supply, simplifying system design. The IDT71027 is packaged in a 28-pin DIP.

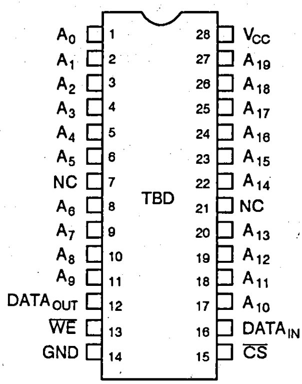
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



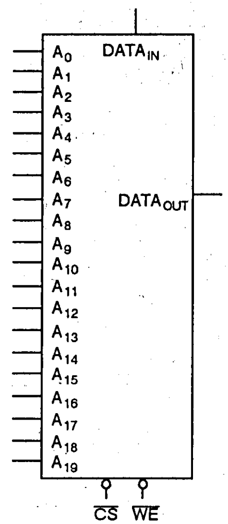
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP
TOP VIEW

LOGIC SYMBOL



TRUTH TABLE [1]

$\overline{CS}$	$\overline{WE}$	OUTPUT	MODE
H	X	Hi-Z	Deselected
L	H	D_{OUT}	Read
L	L	Hi-Z	Write

NOTE:
1. H = High, L = Low, X = Don't Care, Hi-Z = High-Impedance

1 MEGABIT (1024K x 1-BIT) CMOS STATIC RAM SIP MODULE

Integrated Device Technology, Inc.

PRELIMINARY
IDT7MC4001

FEATURES:

- High-density 1 megabit (1024K x 1) CMOS static RAM module
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Available in low profile 30-pin ceramic SIP (single in-line package) for maximum space saving
- Fast access times: 35ns (max.)
- Separate I/O lines
- Low power consumption
  - Dynamic: 1.35W (max.)
  - Full standby: 330mW (max.)
- Single 5V(±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

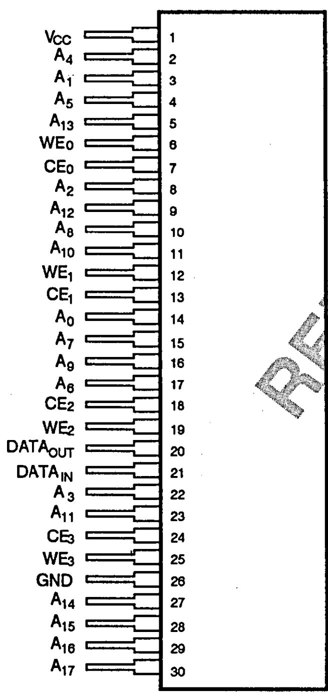
The IDT7MC4001 is a 1 megabit (1024K x 1-bit) high-speed static RAM module with separate I/O. The module is constructed on a co-fired ceramic substrate using four IDT71257 256K x 1 static RAMs in surface mount packages.

The 7MC family of ceramic SIPs offers the optimum in packing density and profile height. The IDT7MC4001 is offered in a 30-pin ceramic SIP (single in-line package). At only 420 mils high, this low profile package is ideal for systems with minimal board spacing. Surface mount SIP technology also yields very high packing density, allowing five IDT7MC4001 modules to be stacked per inch of board space.

The IDT7MC4001 is available with maximum access times as fast as 35ns, with maximum power consumption of 1.35 watts. The module also offers a full standby mode of 330mW (max.).

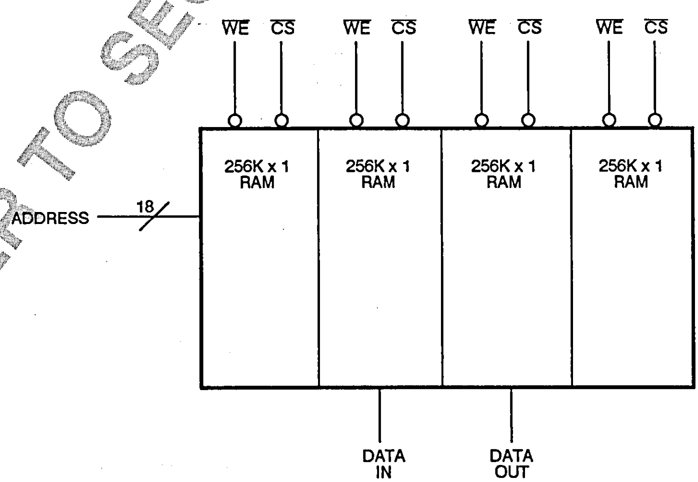
All inputs and outputs of the IDT7MC4001 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access times for ease of use.

PIN CONFIGURATION



SIP
SIDE VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{0-17}	Address
$DATA_{IN}$	Data Input
$DATA_{OUT}$	Data Output
$\overline{CS}_{0-3}$	Chip Select
$\overline{WE}_{0-3}$	Write Enable
V_{CC}	Power
GND	Ground

CEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

CMOS STATIC RAM 1 MEG (256K x 4-BIT)

ADVANCE INFORMATION
IDT71028S
IDT71028L

FEATURES:

- One full megabit of static RAM in popular 256K x 4 configuration
- High-speed access
  - Military: 55/70/90ns (max.)
  - Commercial: 45/55/70ns (max.)
- Low power consumption
  - IDT71028S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT71028L
    Active: 500mW (typ.)
    Standby: 200μW (typ.)
- Battery back-up operation—2V data retention
- Available in 28-pin DIP
- TTL-compatible
- Single 5V (±10%) power supply
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71028 is an extremely high-density (256K x 4-bit), high-speed static RAM designed for use in systems where fast computation, low power and board density are of the utmost importance.

The IDT71028 uses four bidirectional input/output lines to provide simultaneous access to all bits in a word and has a high-speed 45ns address access time to achieve a considerable throughput advantage. An automatic power down feature, controlled by $\overline{CS}$, permits the on-chip circuitry to enter a very low standby power mode and be brought back into operation at a speed equal to the address access time.

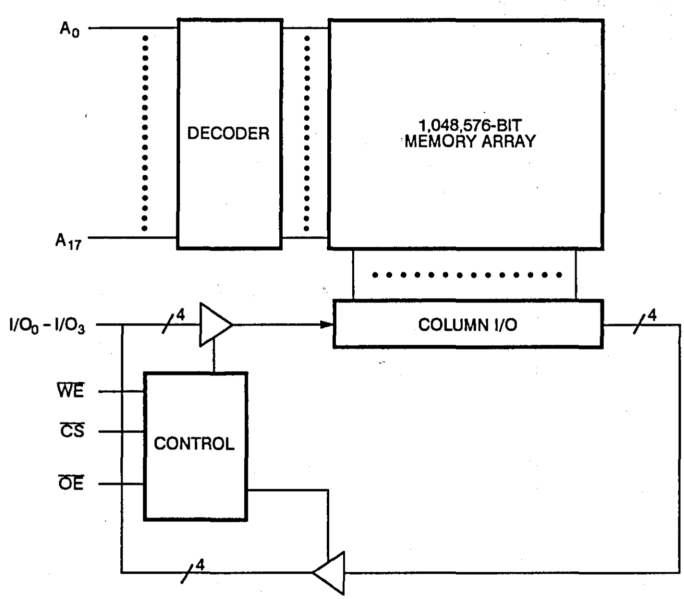
Fabricated using IDT's CEMOS™ high-performance technology, the IDT71028 typically operates on only 500mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, typically consuming 200μW from a 2V battery.

All inputs and outputs of the IDT71028 are TTL-compatible and the device operates from a standard 5V supply, simplifying system design. The IDT71028 is packaged in a 28-pin DIP.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

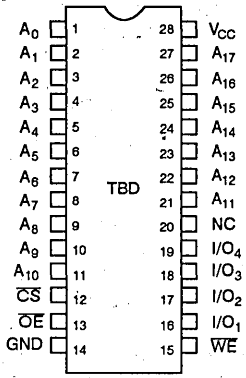
4

FUNCTIONAL BLOCK DIAGRAM



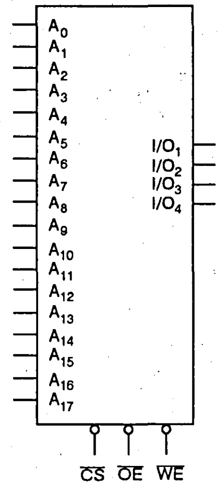
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP
TOP VIEW

LOGIC SYMBOL



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O_1 - I/O_4	FUNCTION
H	X	X	High Z	Deselected, Powered Down (I_{SB})
L	H	H	High Z	Outputs Disabled
L	L	H	D_{OUT}	Read Data from RAM
L	X	L	High Z	Write Data to RAM

NOTE:

1. H = High, L = Low, X = Don't Care, High Z = High Impedance

Integrated Device Technology, Inc.

CMOS STATIC RAM 1 MEG (128K x 8-BIT)

ADVANCE INFORMATION
IDT71024S
IDT71024L

FEATURES:

- One full megabit of static RAM in popular 128K x 8 configuration
- Two chip selects plus Output Enable pin
- High-speed access
  - Military: 55/70/90ns (max.)
  - Commercial: 45/55/70ns (max.)
- Low power consumption
  - IDT71024S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT71024L
    Active: 500mW (typ.)
    Standby: 200μW (typ.)
- Battery back-up operation—2V data retention
- Available in 32-pin, 600 mil DIP
- TTL-compatible
- Single 5V (±10%) power supply
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71024 is an extremely high-density 128K x 8-bit high-speed static RAM designed for use in systems where fast computation, low power and board density are of the utmost importance.

The IDT71024 uses eight bidirectional input/output lines to provide simultaneous access to all bits in a word and has an output enable ($\overline{OE}$) pin which operates as fast as 25ns. This function allows designers to access the IDT71024 at speeds much higher than the already fast 45ns address access time to achieve a considerable throughput advantage. An automatic power down feature permits the on-chip circuitry to enter a very low standby power mode and be brought back into operation at a speed equal to the address access time.

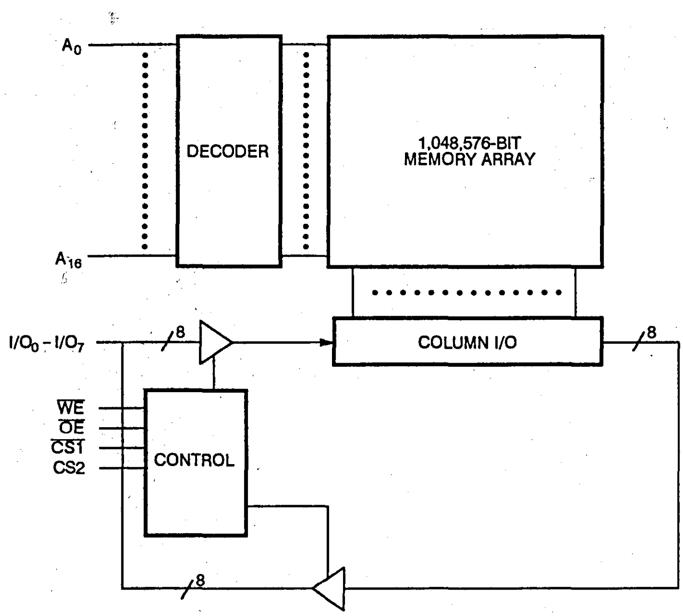
Fabricated using IDT's CEMOS™ high-performance technology, the IDT71024 typically operates on only 500mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, typically consuming 200μW from a 2V battery.

All inputs and outputs of the IDT71024 are TTL-compatible and the device operates from a standard 5V supply, simplifying system design. The IDT71024 is packaged in a 32-pin DIP.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

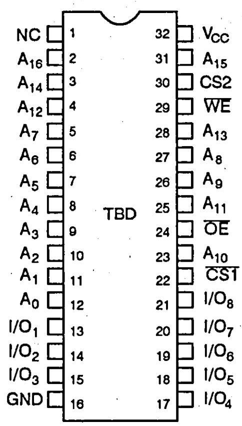
4

FUNCTIONAL BLOCK DIAGRAM



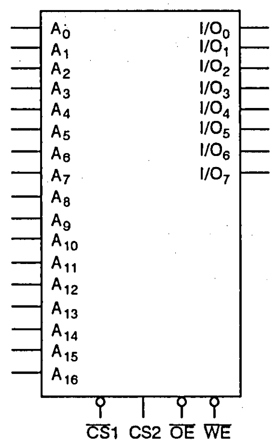
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP
TOP VIEW

LOGIC SYMBOL



TRUTH TABLE

INPUTS				OUTPUTS	FUNCTION
$\overline{WE}$	$\overline{CS}_1$	CS_2	$\overline{OE}$	I/O_0-I/O_7	
X	H	X	X	High Z	Deselected
X	X	L	X	High Z	Deselected
H	L	H	H	High Z	Outputs disabled
H	L	H	L	D_{OUT}	Read data from RAM
L	L	H	X	High Z	Write data to RAM

NOTE:
1. H = High, L = Low, X = Don't Care, High Z = High Impedance

1 MEGABIT (128K x 8-BIT) CMOS STATIC RAM MODULE

IDT8M824S

FEATURES:

- High-density 1024K (128K x 8) CMOS static RAM module
- Equivalent to JEDEC standard for future monolithic 128K x 8 static RAMs
- High-speed
  - Military: 60ns (max.)
  - Commercial: 40ns (max.)
- Low power consumption
  - Active: less than 550mW (typ.)
  - Standby: less than 20mW (typ.)
- CEMOS ™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 32-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT8M824S is a1024K (131,072 x 8-bit) high-speed static RAM constructed on a co-fired ceramic substrate using four IDT71256 32K x 8 static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic one megabit static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} and A_{16} to select one of the four 32K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

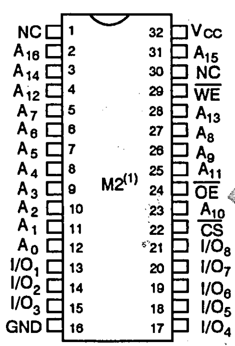
The IDT8M824S is available with maximum access times as fast as 40ns for commercial temperature range, with maximum power consumption of 1.2 watts. The module offers a full standby mode of 440mW (max.).

The IDT8M824S is offered in a 32-pin, 600 mil center sidebraze DIP, adhering to JEDEC standards for one megabit monolithic pinouts, allowing for compatibility with future monolithics.

All inputs and outputs of the IDT8M824S are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

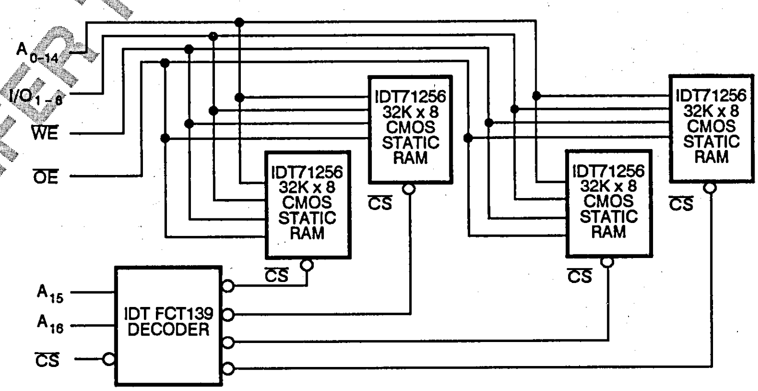
PIN CONFIGURATION



DIP
TOP VIEW

1. For module dimensions, please refer to module drawing M2 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{0-16}	Addresses
I/O_{0-8}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power

$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground

CEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

1 MEGABIT (128K x 8-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

IDT8MP824S

FEATURES:

- High-density 1024K (128K x 8) CMOS static RAM module
- Fast access time
  - 40ns (max.) over commercial temperature range
- Low power consumption
  - Active: less than 500mW (typ.)
  - Standby: less than 8mW (typ.)
- Cost-effective plastic surface-mounted RAM packages on an epoxy laminate (FR4) substrate
- Offered in a SIP (single in-line package) for maximum space-saving
- Utilizes IDT71256s—high-performance 256K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

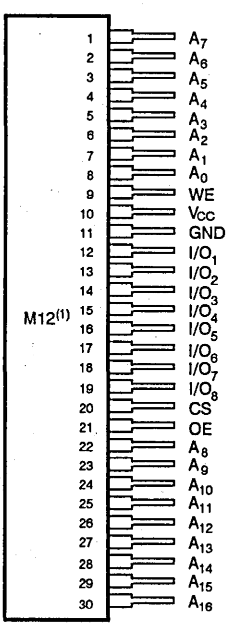
The IDT8MP824S is a1024K (131, 072 x 8-bit) high-speed static RAM constructed on an epoxy laminate substrate using four IDT71256 32K x 8 static RAMs in plastic surface mount packages. Functional equivalence to proposed monolithic one megabit static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} and A_{16} to select one of the four 32K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

The IDT8MP824S is available with maximum access times as fast as 40ns over the commercial temperature range, with maximum operating power consumption of 825mW. The module also offers a full standby mode of 330mW (max.).

The IDT8MP824S is offered in a 30-pin SIP. For the 32-pin JEDEC standard DIP, refer to the IDT8M824S.

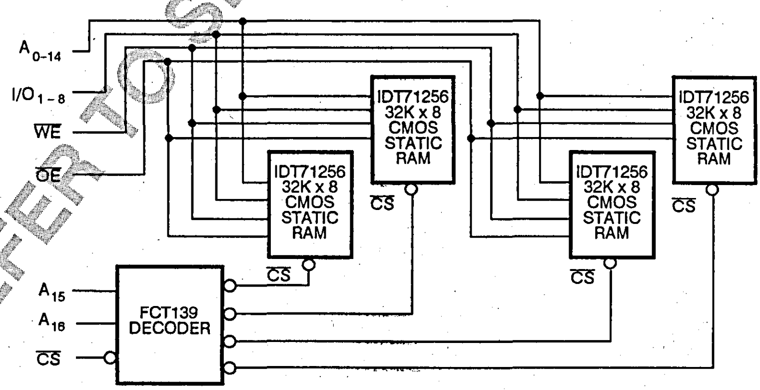
All inputs and outputs of the IDT8MP824S are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

PIN CONFIGURATION



SIP SIDE VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{0-16}	Addresses
I/O_{1-8}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground

1. For module dimensions, please refer to module drawing M12 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

1 MEGABIT CMOS STATIC RAM MODULE

IDT7M624S

FEATURES:

- High-density 1024K-bit CMOS static RAM module
- Customer-configured to 64K x 16, 128K x 8 or 256K x 4
- Fast access times
  - Military: 35ns (max.)
  - Commercial: 25ns (max.)
- Low power consumption
  - Active: 4.8W (typ. in 64K x 16 organization)
  - Standby: 1.6mW (typ.)
- Utilizes 16 IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Pin-compatible with IDT7M656 (256K RAM module)
- Single 5V(±10%) power supply
- Dual GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT7M624 is a 1024K-bit high-speed CMOS static RAM constructed on a multi-layered ceramic substrate using 16 IDT7187 64K x 1 static RAMs in leadless chip carriers. Making four chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 64K x 16, 128K x 8 or 256K x 4 organization. In addition, extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

The IDT7M624 is available with access times as fast as 25ns commercial and 35ns military temperature range, with maximum operating power consumption of only 12.3W (significantly less if organized 128K x 8 or 256K x 4). The module also offers a standby power mode of 5.7W (max.) and a full standby mode of 1.7W (max.).

The IDT7M624 is offered in a 40-pin, 900 mil center sidebraze DIP to take advantage of the compact IDT7187s in leadless chip carriers.

All inputs and outputs of the IDT7M624 are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access times for ease of use.

All IDT military module semiconductor components are compliant with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

M6[(2)]

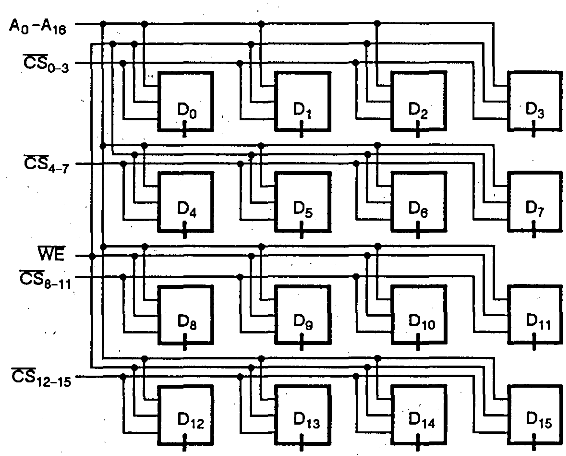
Signal	Pin	Pin	Signal
[(1)]GND	1	40	V_{CC}
D_{15}	2	39	D_{11}
$\overline{CS}_{(12-15)}$	3	38	$\overline{CS}_{(6-11)}$
D_4	4	37	D_0
$\overline{WE}$	5	36	A_0
A_1	6	35	A_{13}
D_{14}	7	34	D_{10}
A_2	8	33	A_{12}
D_5	9	32	D_1
A_3	10	31	A_{11}
A_4	11	30	A_{10}
D_{13}	12	29	D_9
A_5	13	28	A_9
D_6	14	27	D_2
A_6	15	26	A_8
A_{14}	16	25	A_7
D_{12}	17	24	D_8
$\overline{CS}_{(4-7)}$	18	23	$\overline{CS}_{(0-3)}$
D_7	19	22	D_3
A_{15}	20	21	GND[(1)]

DIP
TOP VIEW

PIN NAMES

A_{0-16}	Address
D_{0-15}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. Both GND pins need to be grounded for proper operation.
2. For module dimensions, please refer to module drawing M6 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

1 MEGABIT CMOS STATIC RAM PLASTIC MODULE

ADVANCE INFORMATION
IDT7MB624

FEATURES:

- High-density 1024K-bit CMOS static RAM module
- Customer-configured to 64K x 16, 128K x 8 or 256K x 4
- Fast access times
  - 25ns (max.)
- Low power consumption
  - Active: 4.8W (typ.) (in 64K x 16 organization)
  - Standby: 1.6mW (typ.)
- Utilizes 16 IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Offered in 40-pin, 900 mil center plastic DIP, achieving very high memory density
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate

DESCRIPTION:

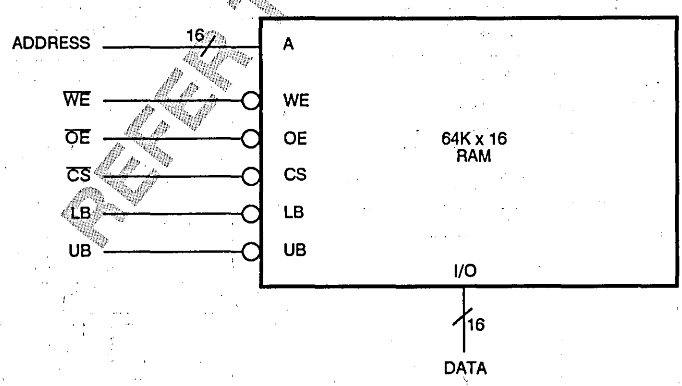
The IDT7MB624 is a 1024K-bit high-speed CMOS static RAM constructed on an epoxy laminate substrate using 16 IDT7187 (64K x 1) static RAMs in plastic surface mount packages. Making four chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 64K x 16, 128K x 8 or 256K x 4 organization. In addition, extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

The IDT7MB624 is available with access times as fast as 25ns over the commercial temperature range, with maximum operating power consumption of only 9.6W (significantly less if organized 128K x 8 or 256K x 4). The module also offers a standby power mode of 4.4W (max.) and a full standby mode of 1.7W (max.).

The IDT7MB624 is offered in a high-density 40-pin, 900 mil center plastic DIP to take full advantage of the compact IDT7187s in plastic surface mount packages.

All inputs and outputs of the IDT7MB624 are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE **DECEMBER 1987**

DSC-7001/-

Integrated Device Technology, Inc.

1 MEGABIT (64K x 16-BIT) & 512K (32K x 16-BIT) CMOS STATIC RAM MODULE

IDT8M624S
IDT8M612S

FEATURES:

- High-density 1024K/512K-bit CMOS static RAM module
- 64K x 16 organization (IDT8M624S) with 32K x 16 option (IDT8M612S)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  — Allows flexibility in application
- Equivalent to JEDEC standard for future monolithic 64K x 16/ 32K x 16 static RAMs
- High speed, 40ns (max.) over commercial temperature range
- Low power consumption
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 40-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT8M624S/IDT8M612S are 1024K/512K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic-substrate using four IDT71256 32K x 8 static RAMs (IDT8M624S) or two IDT71256 static RAMs (IDT8M612S) in leadless chip carriers. Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} to select one of the two 32K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On the IDT8M612S 32K x 16 option, A_{15} needs to be externally grounded for proper operation.) Extremely high speeds are achievable by the use of IDT71256s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 1024K/512K static RAMs available.

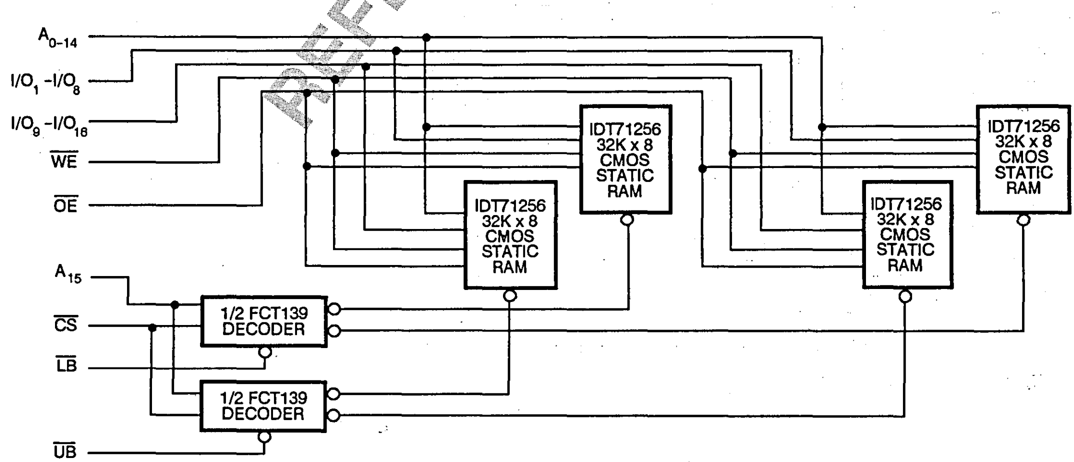
The IDT8M624S/IDT8M612S are available with access times as fast as 40ns commercial and 60ns military temperature range, with maximum operating power consumption of only 1.8W (max.—IDT8M624S 64K x 16 option). The module also offers a full standby mode of 440mW (max.).

The IDT8M624S/IDT8MP612S are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT71256s in leadless chip carriers.

All inputs and outputs of the IDT8M624S/IDT8M612S are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

1 MEGABIT (64K x 16-BIT) & 512K (32K x 16-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

IDT8MP624L
IDT8MP612L

FEATURES:

- High-density 1024K/512K-bit CMOS static RAM module
- 64K x 16 organization (IDT8MP624) with 32K x 16 option (IDT8MP612)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  - Allows flexibility in application
- Fast access time: 40ns (max.)
- Low power consumption
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Offered in a SIP (single in-line) package for maximum space-savings
- Cost-effective plastic surface-mounted RAM packages on an epoxy laminate (FR4) substrate
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

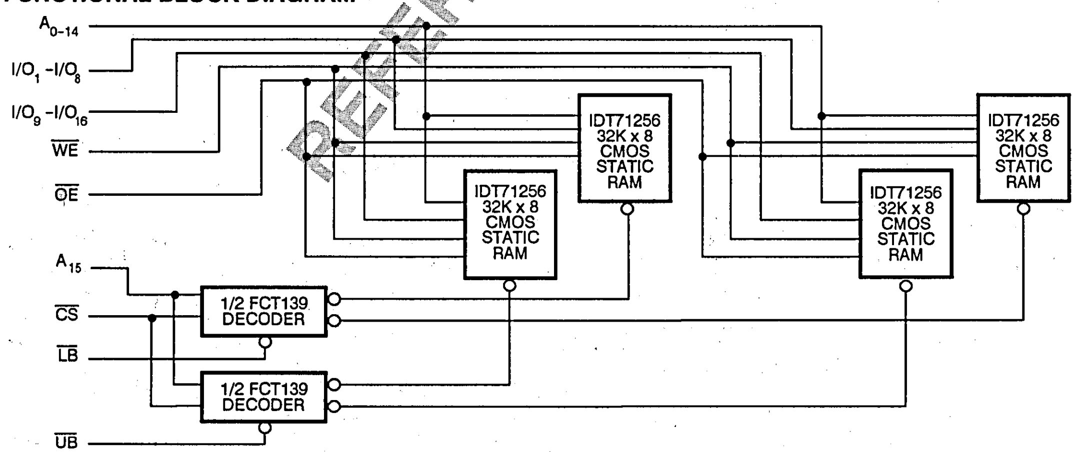
The IDT8MP624S/IDT8MP612S are 1024K/512K high-speed CMOS static RAMs constructed on an epoxy laminate substrate using four IDT71256 32K x 8 static RAMs (IDT8MP624S) or two IDT71256 static RAMs (IDT8MP612S) in plastic surface-mount packages. Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} to select one of the two 32K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On the IDT8MP612S 32K x 16 option, A_{15} needs to be externally grounded for proper operation.) Extremely high speeds are achieved by the use of IDT71256s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 1024K/512K static RAMs available.

The IDT8MP624S/IDT8MP612S are available with access times as fast as 40ns over the commercial temperature range, with maximum operating power consumption of only 1.8W (64K x 16 option). The module also offers a full standby mode of 330mW (max.)

The IDT8MP624S/IDT8MP612S are offered in a 40-pin plastic SIP package. For the 40-pin JEDEC standard DIP, refer to the IDT8M624S/IDT8M612S.

All inputs and outputs of the IDT8MP624S/IDT8MP612S are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE **DECEMBER 1987**

DSC-7014/-

Integrated Device Technology, Inc.

2 MEGABIT (64K x 32) CMOS STATIC RAM MODULE

ADVANCE INFORMATION
IDT7M4017

FEATURES:

- High-density 2 megabit (64K x 32) CMOS static RAM module
- Fast access times
  - Military: 60ns (max.)
  - Commercial: 45ns (max.)
- Individual byte selects
- Upper and lower word write enables
- CEMOS ™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in 60-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M4017 is a 2 megabit (64K x 32) high-speed static RAM module constructed on a co-fired ceramic substrate using eight IDT71256 32K x 8 static RAMs in leadless chip carriers. On-board decoders use A_{15} to select the upper or lower bank of RAMs. Four chip selects control individual byte selection. Extremely fast speeds can be achieved due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

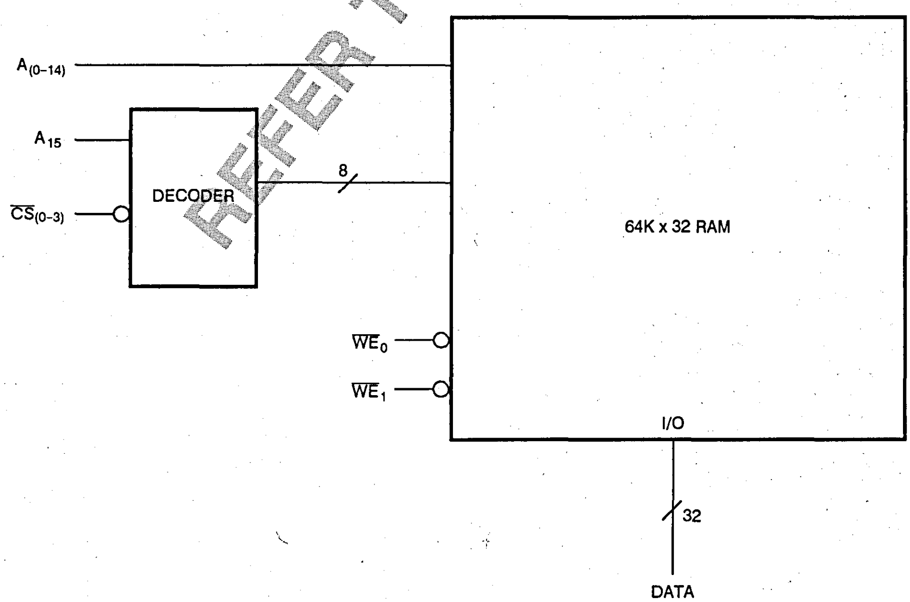
The IDT7M4017 is offered in a 60-pin, 600 mil center sidebraze DIP which enables two megabits of memory to be placed in less than 1.9 square inches of board space.

The IDT7M4017 is available with fast access times over the commercial and military temperature ranges, with minimal power consumption. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to a substantially lower power mode.

All inputs and outputs of the IDT7M4017 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

4 MEGABIT (512K x 8) CMOS STATIC RAM PLASTIC SIP MODULE

IDT7MP4008S

FEATURES:

- High-density 4 megabit (512K x 8) CMOS static RAM module
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Available in 36-pin SIP (single in-line package) for maximum space saving
- Fast access times
  - 45ns (max.)
- Low power consumption
  - Dynamic: 2.6W (max.)
  - Full standby: 1.9 (max.)
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

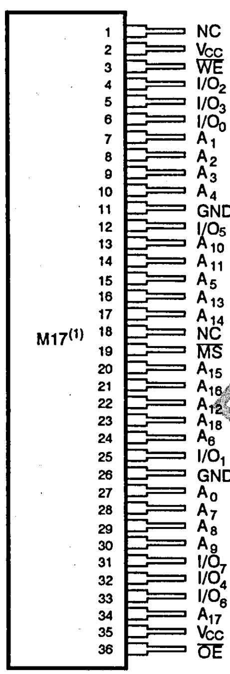
The IDT7MP4008 is a 4 megabit (512K x 8-bit) high-speed static RAM module constructed on an epoxy laminate surface using sixteen IDT71256 32K x 8 static RAMs in plastic surface mount packages. Extremely fast speeds can be achieved with this technique due to the use of 256K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS technology.

The 7MP family of surface mounted SIP technology is a cost-effective solution allowing for very high packing density. The IDT7MP4008 is offered in a 36-pin SIP. The 7MP4008 can be stacked on 300 mil centers, yielding greater than 12 megabits of RAM in less than 5 square inches of board space.

The IDT7MP4008 is available with maximum access times as fast as 45ns with maximum power consumption of 2.6 watts. The IDT7MP4008 also offers a full standby mode of 1.9W (max.).

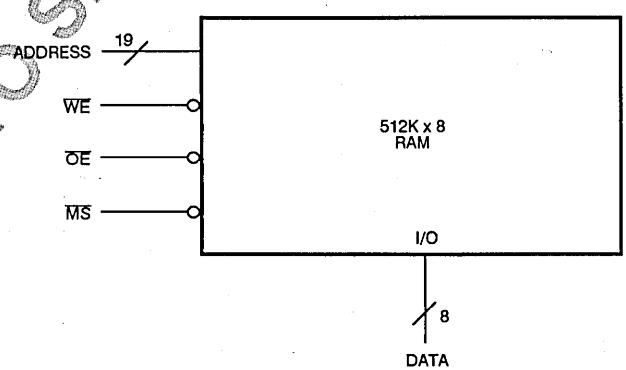
All inputs and outputs of the IDT7MP4008 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

PIN CONFIGURATION



SIP SIDE VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{0-18}	Addresses
I/O_{0-7}	Data Inputs/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{MS}$	Module Select
V_{CC}	Power
GND	Ground

NOTE:
1. For module dimensions, please refer to module drawing M17 in the packaging section.

Integrated Device Technology, Inc.

4 MEGABIT (256K x 16) CMOS STATIC RAM MODULE

ADVANCE INFORMATION
IDT7M4016

4

FEATURES:

- High-density 4 megabit (256K x 16) CMOS static RAM module
- Low power consumption
- Utilizes 16 IDT71257 high-performance 256K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in 48-pin, 900 mil wide ceramic sidebraze DIP
- 4X the density of the IDT7M624 (1024K RAM module) in the same size package
- Multiple GND pins for maximum noise immunity
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

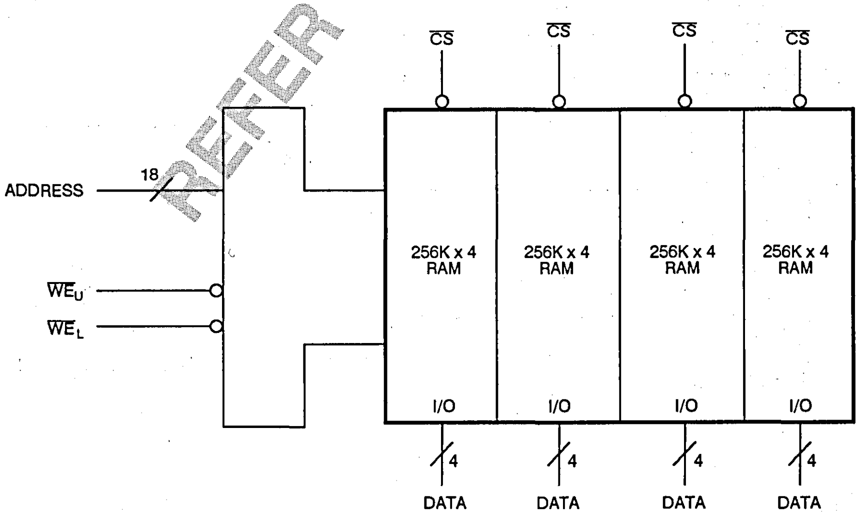
The IDT7M4016 is a 4-megabit high-speed CMOS static RAM module constructed on a multi-layered ceramic substrate using sixteen IDT71257 (256K x 1) static RAMs in leadless chip carriers. The IDT7M4016 is an upgrade from the IDT7M624 (1024K RAM module) offering four times the memory density in the same size package. Making four chip select lines available (one for each group of four RAMs) allows the user to configure the memory into a 256K x 16, 512K x 8 or 1024K x 4 organization. In addition, extremely high speeds are achievable by the use of IDT71257s, fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 256K static RAMs available.

The IDT7M4016 is packaged in a 48-pin, 900 mil center sidebraze DIP to take advantage of the compact leadless chip carriers. This enables four megabits of static RAM memory to be placed in less than 2.2 square inches of board space.

All inputs and outputs of the IDT7M4016 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-7009/-

CMOS STATIC RAM 16K (4K x 4-BIT) CACHE-TAG RAM

ADVANCE INFORMATION IDT6178S

Integrated Device Technology, Inc.

FEATURES:

- High-speed address access time
  - Military: 15ns
  - Commercial: 12ns
- High-speed comparison time
  - Military: 15ns
  - Commercial: 12ns
- Low power consumption
  - IDT6178S
    Active: 300mW (typ.)
- Produced with advanced CEMOS™ high-performance technology
- Input and output TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B.

DESCRIPTION:

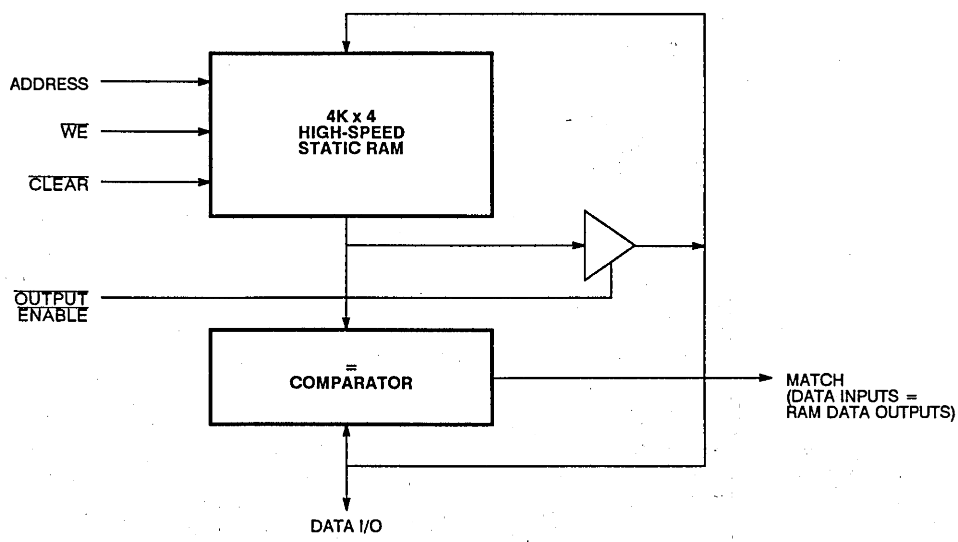
The IDT6178 is a high-speed cache address comparator subsystem consisting of a 16,384-bit static RAM organized as 4K x 4. Cycle Time and Compare Access Time are equal. The IDT6178 features an onboard 4-bit comparator that compares RAM contents and current input data. The result is an active high level on the MATCH pin. The MATCH pins of several IDT6178s can be nanded together to provide enabling acknowledging signals to the data cache or processor.

The IDT6178 is fabricated using IDT's high-performance, high-reliability technology—CEMOS™. Address-to-compare access times as fast as 12ns are available, with Tag Data-to-compare access times as fast as 12ns.

All inputs and outputs of the IDT6178 are TTL-compatible and operate from a single 5V supply. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation.

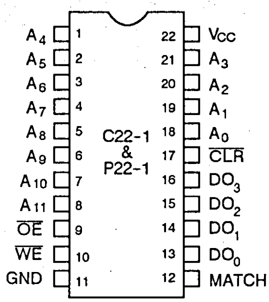
The IDT6178 is packaged in either a 22-pin, 300 mil plastic or ceramic DIP and military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



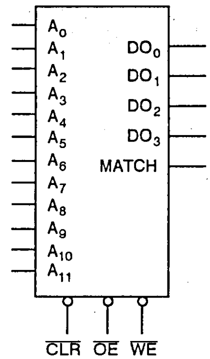
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP
TOP VIEW

LOGIC SYMBOL



TRUTH TABLE [1]

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	$DO_0 - DO_3$	FUNCTION
X	X	L	L	X	Reset
H	H	H	H	Data In	Compare, equal
H	H	H	L	Data In	Compare, not equal
L	X	H	L	Data In	Write
H	L	H	L	Data Out	Read

NOTE:
1. H = High, L = Low, X = Don't Care

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (8K x 8-BIT) CACHE-TAG RAM

IDT7174S

FEATURES:

- High-speed address to MATCH comparison time
  - Military: 45/55ns (max.)
  - Commercial: 37/45ns (max.)
- High-speed address access time
  - Military: 45/55ns (max.)
  - Commercial: 35/45ns (max.)
- High-speed chip select access time
  - Military: 25/30ns (max.)
  - Commercial: 20/25ns (max.)
- Low-power operation
  - IDT7174S
    Active: 300mW (typ.)
- High-speed asynchronous RAM Clear on Pin 1 (Reset Cycle Time = 2 x t_{AA})
- MATCH Output on Pin 26
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard 28-pin DIP (600 mil and 300 mil), 28-pin SOIC, 32-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7174 is a high-speed cache address comparator subsystem consisting of a 65,536-bit static RAM organized as 8K x 8 and an 8-bit comparator. A single IDT7174 can map 8K cache words into a 1 megabyte address space by comparing 20 bits of address organized as 13 word cache address bits and 7 upper address bits. Two IDT7174s can be combined to provide 28 bits of address comparison, etc. The IDT7174 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system-reset, a requirement for cache comparator systems. The IDT7174 can also be used as an 8K x 8 high-speed static RAM.

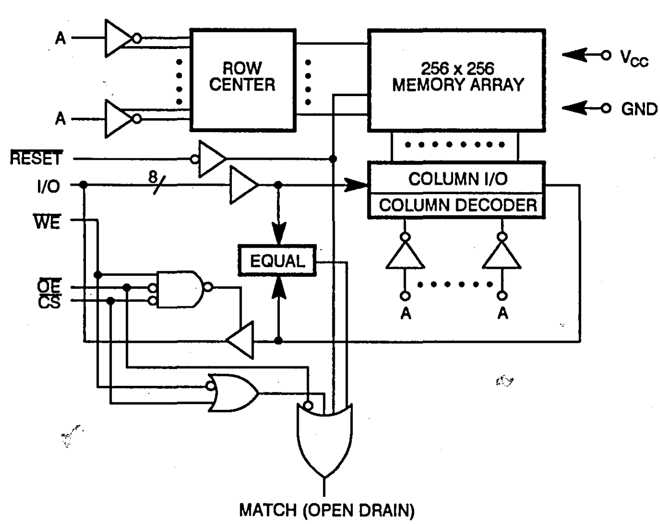
The IDT7174 is fabricated using IDT's high-performance, high-reliability technology—CEMOS. Address access times as fast as 35ns, chip select times of 20ns and address-to-comparison times of 37ns are available with maximum power consumption of 825mW.

All inputs and outputs of the IDT7174 are TTL-compatible and the device operates from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7174 is packaged in a 28-pin DIP (600 mil and 300 mil), a 28-pin SOIC and 32-pin LCC and PLCC, providing high board level packing densities.

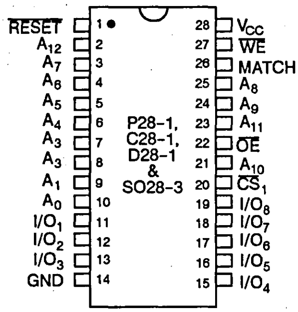
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

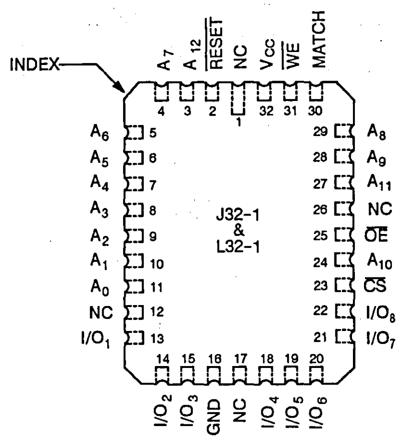


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

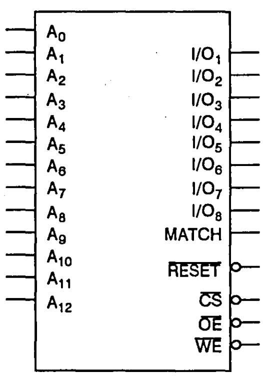


DIP/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_{0-12}	Address	$\overline{WE}$	Write Enable
I/O_{1-8}	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	GND	Ground
$\overline{RESET}$	Memory Reset	V_{CC}	Power
MATCH	Data/Memory Match (Open Drain)		

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage [1]	2.2	–	6.0	V
V_{IHR}	$\overline{RESET}$ Input High Voltage	2.5 [2]	–	6.0	V
V_{IL}	Input Low Voltage	-0.5 [3]	–	0.8	V

NOTES:

1. All inputs except $\overline{RESET}$.
2. When using bipolar devices to drive the $\overline{RESET}$ input, a pullup resistor of 1kΩ–10kΩ is usually required to assure this voltage.
3. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

4

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7174S MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	– –	– –	10 5	µA
$\|I_{LO}\|$	Output Leakage Current(2)	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	– –	– –	10 5	µA
V_{OL}	Output Low Voltage	I_{OL} = 18mA MATCH	MIL.	–	–	0.5	V
		I_{OL} = 22mA MATCH	COM'L.	–	–	0.5	V
		I_{OL} = 10mA, V_{CC} = Min. (All outputs except MATCH)		–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min. (All outputs except MATCH)		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min. (Except MATCH)		2.4	–	–	V

NOTES:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.
2. Data and MATCH

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	IDT7174S35 COM'L.	MIL.	IDT7174S45 COM'L.	MIL.	IDT7174S55 COM'L.	MIL.	UNIT
I_{CC1}	Operating Power Supply Current Outputs Open, V_{CC} = Max., f = 0	110	–	110	125	–	125	mA
I_{CC2}	Dynamic Operating Current Outputs Open, V_{CC} = Max., f = f_{Max}	150	–	140	150	–	145	mA

NOTE:
1. All values are maximum guaranteed values.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

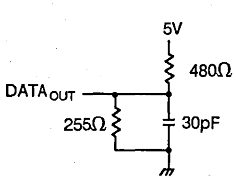


Figure 1. Output Load

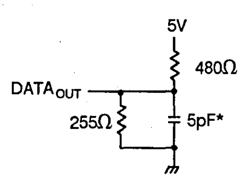
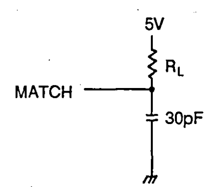


Figure 2. Output Load (for t_{CLZ} t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

* Including scope and jig



R_L = 200Ω (COM'L.)
= 270Ω (MIL.)

Figure 3. Output Load for MATCH

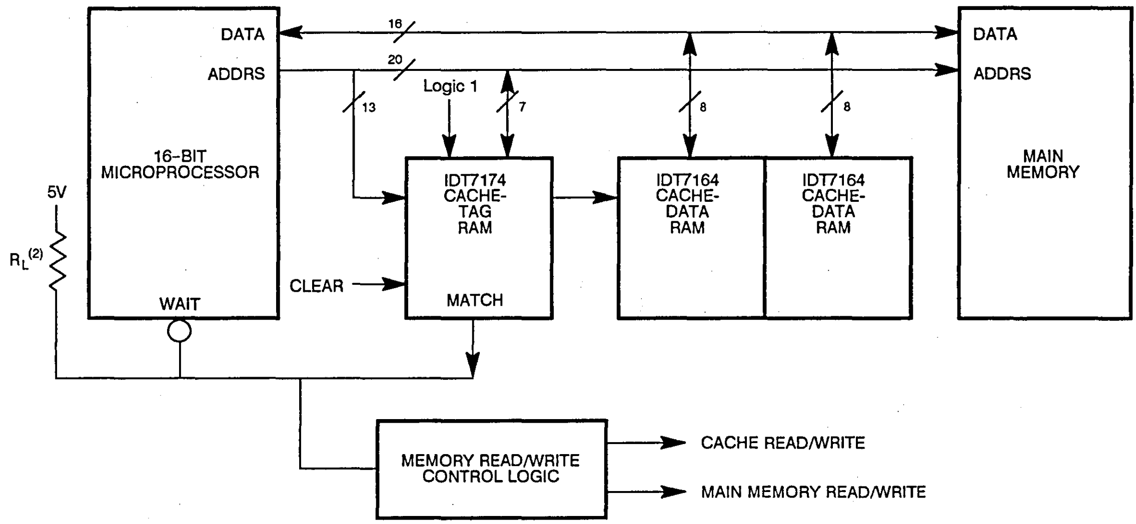


Figure 4. Example of Cache Memory System Block Diagram

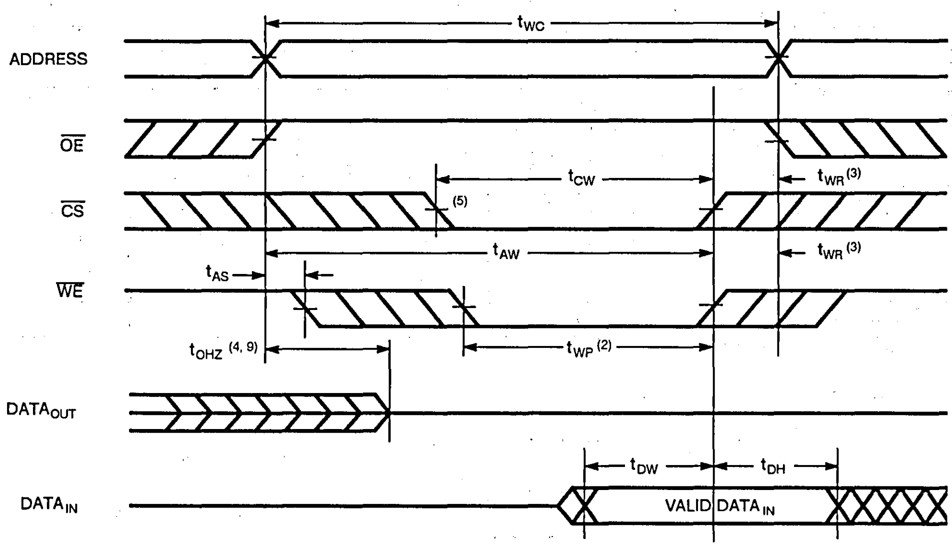
NOTES:
1. For more information, see application note AN-07 "Cache-Tag RAM Chips Simplify Cache Memory Design".
2. R_L = 200Ω (commercial) or 270Ω (military)

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

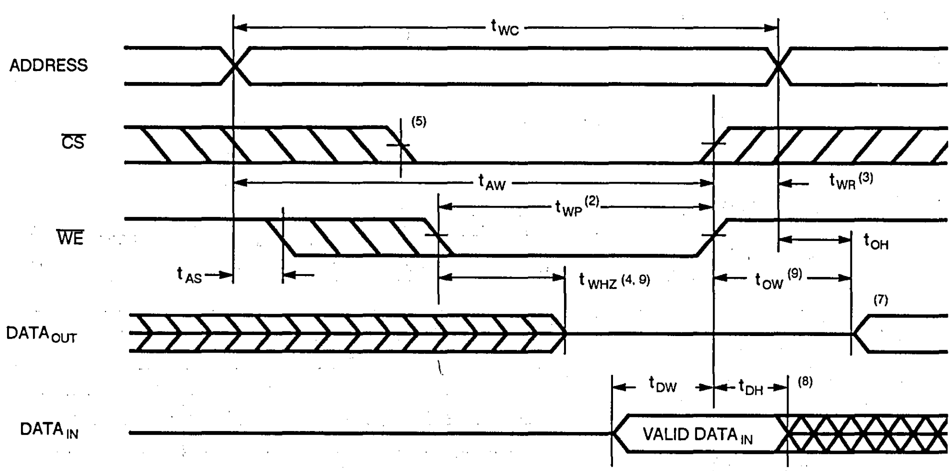
SYMBOL	PARAMETER	IDT7174S35 (1) MIN.	IDT7174S35 (1) MAX.	IDT7174S45 MIN.	IDT7174S45 MAX.	IDT7174S55 (2) MIN.	IDT7174S55 (2) MAX.	UNIT
WRITE CYCLE								
t_{WC}	Write Cycle Time	35	–	45	–	55	–	ns
t_{CW}	Chip Select to End of Write	20	–	25	–	30	–	ns
t_{AW}	Address Valid to End of Write	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	30	–	40	–	50	–	ns
t_{WR}	Write Recovery Time ($\overline{CS}$, $\overline{WE}$)	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output in High Z (3)	–	15	–	20	–	25	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	25	–	ns
t_{DH}	Data Hold From Write Time	2	–	2	–	2	–	ns
t_{OW}	Output Active from End of Write (3)	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (1, 6)



NOTES:

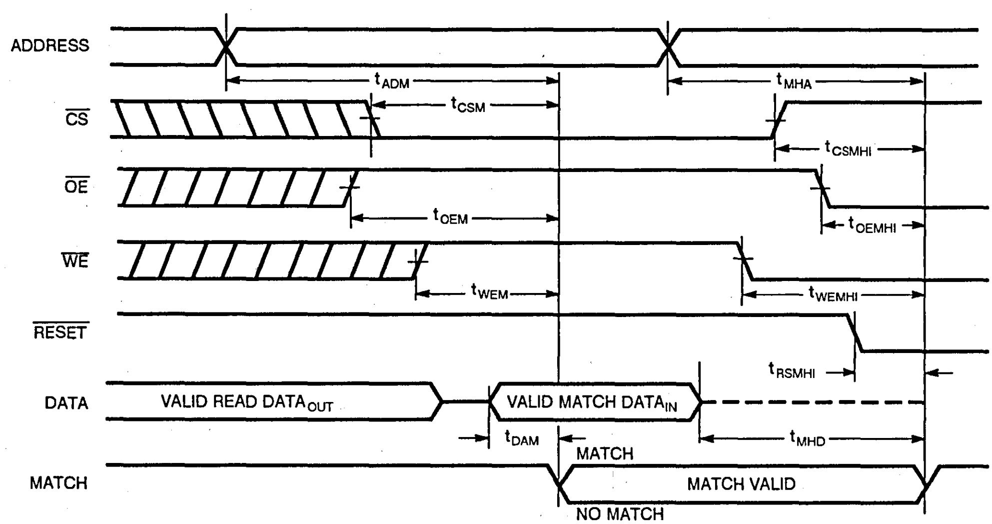
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{WE}$ and a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. $DATA_{OUT}$ is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7174S35 (1) MIN.	IDT7174S35 (1) MAX.	IDT7174S45 MIN.	IDT7174S45 MAX.	IDT7174S55 (2) MIN.	IDT7174S55 (2) MAX.	UNIT
MATCH								
t_{ADM}	Address to MATCH Valid	–	37	–	45	–	55	ns
t_{CSM}	Chip Select to MATCH Valid	–	20	–	25	–	30	ns
t_{CSMHI}	Chip Deselect to MATCH High	–	20	–	25	–	30	ns
t_{DAM}	Data Input to MATCH Valid	–	28	–	35	–	45	ns
t_{OEMHI}	$\overline{OE}$ Low to MATCH High	–	25	–	35	–	45	ns
t_{OEM}	$\overline{OE}$ High to MATCH Valid	–	25	–	35	–	45	ns
t_{WEMHI}	$\overline{WE}$ Low to MATCH High	–	25	–	35	–	45	ns
t_{WEM}	$\overline{WE}$ High to MATCH Valid	–	25	–	35	–	45	ns
t_{RSMHI}	$\overline{RESET}$ Low to MATCH High	–	25	–	35	–	45	ns
t_{MHA}	MATCH Valid Hold From Address	5	–	5	–	5	–	ns
t_{MHD}	MATCH Valid Hold From Data	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.

MATCH TIMING

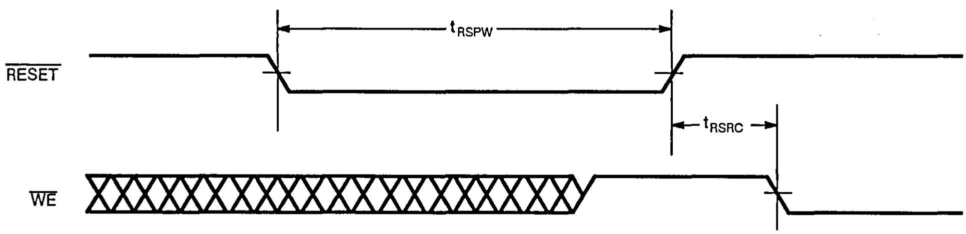


AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7174S35 (1) MIN.	IDT7174S35 (1) MAX.	IDT7174S45 MIN.	IDT7174S45 MAX.	IDT7174S55 (2) MIN.	IDT7174S55 (2) MAX.	UNIT
RESET								
t_{RSPW}	$\overline{\text{RESET}}$ Pulse Width (3)	65	–	80	–	100	–	ns
t_{RSRC}	$\overline{\text{RESET}}$ High to $\overline{\text{WE}}$ Low	5	–	10	–	10	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Recommended duty cycle 10% maximum.

RESET TIMING



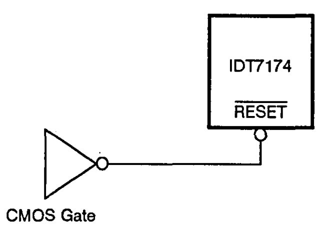
CAPACITANCE(1) (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

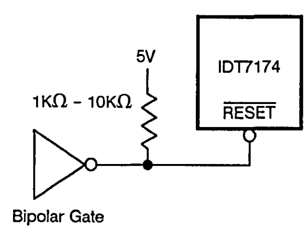
NOTE:
1. This parameter is determined by device characterization, but is not production tested.

TRUTH TABLE

$\overline{\text{WE}}$	$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{RESET}}$	MATCH	I/O	FUNCTION
X	X	X	L	H	–	Reset all bits to low
X	H	X	H	H	High Z	Deselect chip
H	L	H	H	L	D_{IN}	No MATCH
H	L	H	H	H	D_{IN}	MATCH
H	L	L	H	H	D_{OUT}	Read
L	L	X	H	H	D_{IN}	Write



Driving the $\overline{\text{RESET}}$ pin with CMOS logic.



Driving the $\overline{\text{RESET}}$ pin with bipolar logic.

Figure 4.

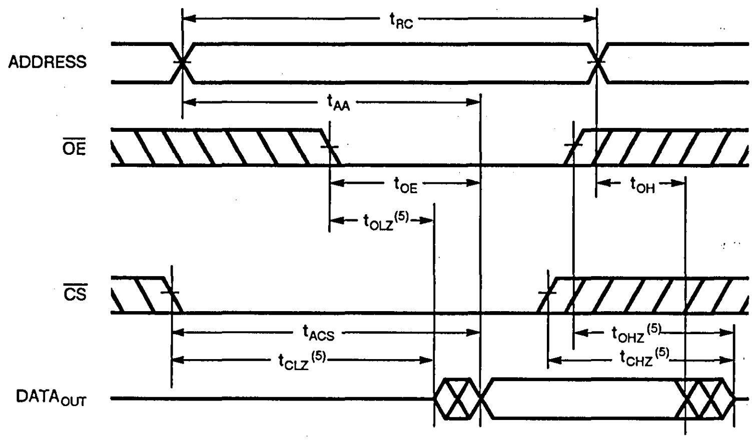
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7174S35 (1)		IDT7174S45		IDT7174S55 (2)		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE								
t_{RC}	Read Cycle Time	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	20	–	25	–	30	ns
t_{CLZ}	Chip Select to Output in Low Z	0	–	0	–	0	–	ns
t_{OE}	Output Enable to Output Valid	–	20	–	25	–	30	ns
t_{OLZ}	Output Enable to Output in Low Z (3)	0	–	0	–	0	–	ns
t_{CHZ}	Chip Select to Output in High Z (3)	–	15	–	20	–	25	ns
t_{OHZ}	Output Disable to Output in High Z (3)	–	15	–	20	–	25	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	ns

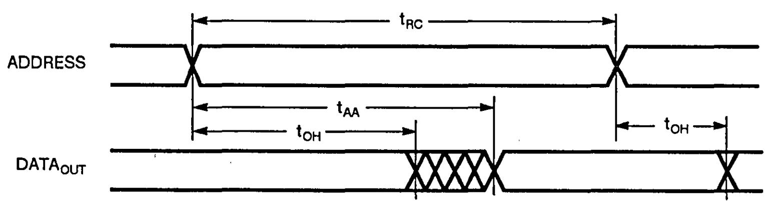
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.

4

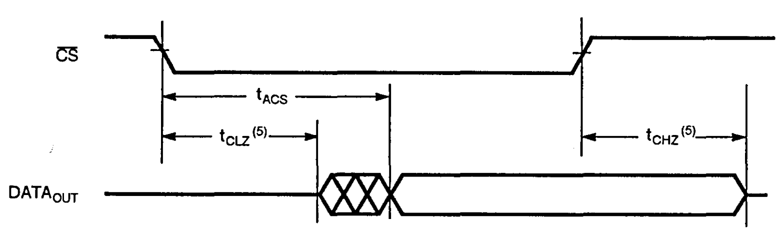
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.

ORDERING INFORMATION

IDT XXXX A 999 A A

XXXX	A	999	A	A
Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B, Method 5004

Package

P	Plastic DIP
TC	THINDIP (Sidebraze)
D	CERDIP
J	Plastic Leaded Chip Carrier
L	Leadless Chip Carrier
SO	Small Outline IC

Speed

35	Commercial Only	Speed in Nanoseconds
45		
55	Military Only	

Power

S	Standard Power

Device Type

7174	64K (8K x 8-Bit) Cache-Tag RAM

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (8K x 8-BIT) RESETTABLE RAM

IDT7165S
IDT7165L

FEATURES:

- High-speed asynchronous RAM clear on Pin 1 (clears all RAM bits to 0, reset cycle time = 2 x t_{AA})
- High-speed address access time
  - Military: 35/45/55ns (max.)
  - Commercial: 30/35/45/55ns (max.)
- High-speed chip select ($\overline{CS}_1$) time
  - Military: 20/25/30/35ns (max.)
  - Commercial: 15/20/25/30ns (max.)
- Low-power operation
  - IDT7165S
    Active: 300mW (typ.)
    Standby: 100µW (typ.)
  - IDT7165L
    Active:250mW (typ.)
    Standby: 30µW (typ.)
- Battery backup operation—2V data retention voltage (IDT7165L only)
- Produced with CEMOS™ high-performance technology
- Single 5V(±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard 28-pin, 600 mil DIP, 300 mil DIP, 28-pin SOIC, 32-pin LCC and PLCC
- Military product is compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7165 is a high-speed 65,536-bit static RAM, organized 8K x 8, with reset function. The $\overline{RESET}$ pin provides a single RAM clear control which clears all words in the internal RAM to zero when activated. This allows the memory bits for all locations to be cleared at power-on or system reset, or for a fast clear to be available to graphics, histogramming and other designs where a byte-by-byte RAM clear would cause noticeable system speed degradation.

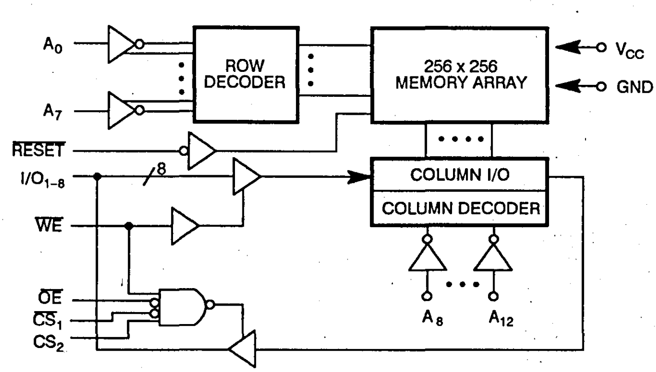
This product is fabricated using IDT's high-performance, high-reliability CEMOS technology. Address access time of 30ns and chip select ($\overline{CS}_1$) time of 15ns are available with maximum power consumption of only 770mW. This circuit also offers a reduced power standby mode. When CS_2 goes low, the circuit will automatically go to and remain in a low-power standby mode. In the full standby mode, the low-power device typically consumes less than 30µW. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10µW operating from a 2V battery.

All inputs and outputs of the IDT7165 are TTL-compatible and the device operates from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, so no clocks or refreshing operation is required.

The IDT7165 is packaged in a 28-pin 300 or 600 mil DIP, 28-pin SOIC, and 32-pin LCC and PLCC, providing high board level densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to the military temperature applications which require instant destruction of sensitive RAM data and demand the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

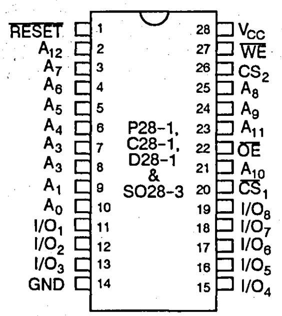


CEMOS is a trademark of Integrated Device Technology, Inc.

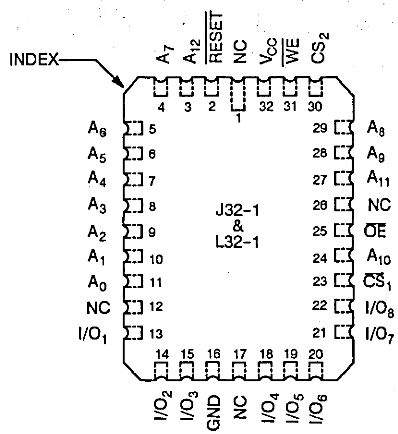
MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-1021/-

PIN CONFIGURATIONS

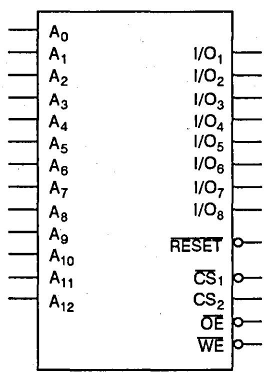


DIP/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

$A_{0\text{-}12}$	Address	$\overline{WE}$	Write Enable
$I/O_{1\text{-}8}$	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}_1$, CS_2	Chip Select	GND	Ground
$\overline{RESET}$	Memory Reset	V_{CC}	Power

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage(1)	2.2	–	6.0	V
V_{IHR}	$\overline{RESET}$ Input High Voltage	2.5(2)	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(3)	–	0.8	V

NOTES:

1. All inputs except $\overline{RESET}$.
2. When using bipolar devices to drive the $\overline{RESET}$ input, a pullup resistor of 1kΩ–10kΩ is usually required to assure this voltage.
3. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7165S MIN.	IDT7165S TYP.(1)	IDT7165S MAX.	IDT7165L MIN.	IDT7165L TYP.(1)	IDT7165L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	– –	– –	10 5	– –	– –	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	– –	– –	10 5	– –	– –	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

4

DC ELECTRICAL CHARACTERISTICS (1)

$V_{CC} = 5.0V \pm 10\%$, V_{LC} = 0.2V, V_{HC} = V_{CC} –0.2V

SYMBOL	PARAMETER	POWER	IDT7165S/L30 COM'L.	IDT7165S/L30 MIL.	IDT7165S/L35 COM'L.	IDT7165S/L35 MIL.	IDT7165S/L45 COM'L.	IDT7165S/L45 MIL.	IDT7165S/L55 COM'L.	IDT7165S/L55 MIL.	UNIT
I_{CC1} (2)	Operating Power Supply Current Outputs Open, V_{CC} = Max., f = 0	S	90	–	90	100	90	100	90	100	mA
		L	80	–	80	90	80	90	80	90	
I_{CC2} (2)	Dynamic Operating Current Outputs Open, V_{CC} = Max., f = f_{MAX}	S	160	–	150	160	150	160	150	160	mA
		L	140	–	130	140	120	130	115	125	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}_1 \geq V_{IH}$, $CS_2 \leq V_{IL}$, and $\overline{RESET} \geq V_{IH}$ V_{CC} = Max., Outputs Open	S	20	–	20	20	20	20	20	20	mA
		L	3	–	3	5	3	5	3	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $CS_2 \leq V_{LC}$ and $\overline{RESET} \geq V_{HC}$, V_{CC} = Max.	S	15	–	15	20	15	20	15	20	mA
		L	0.2	–	0.2	1	0.2	1	0.2	1	

NOTES:
1. All values are maximum guaranteed values.
2. $CS_2 = V_{IH}$

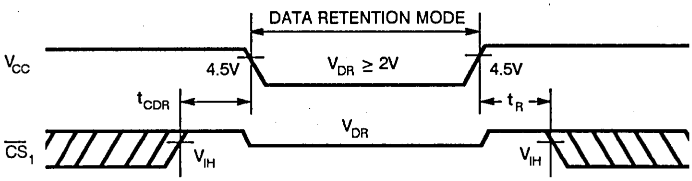
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$CS_2 \leq V_{LC}$ and $\overline{RESET} \geq V_{HC}$	MIL.	–	10	15	200	300	µA
			COM'L.	–	10	15	60	90	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

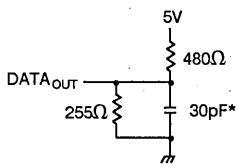


Figure 1. Output Load

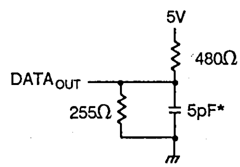


Figure 2. Output Load
(for t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{OW}, t_{WHZ})

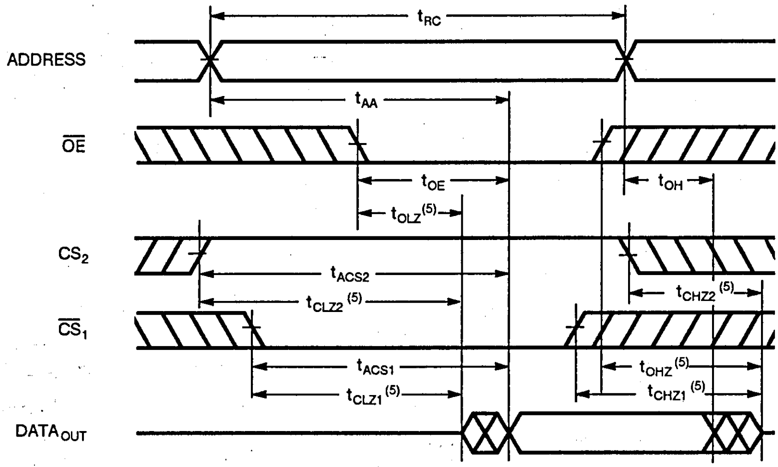
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

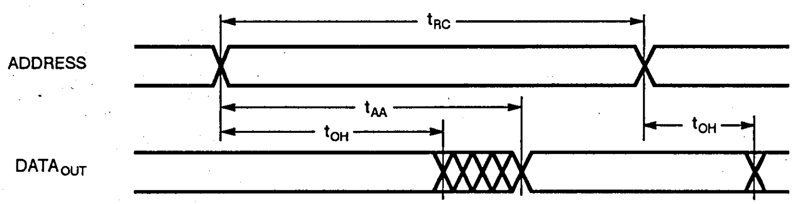
SYMBOL	PARAMETER	IDT7165S30 (1) IDT7165L30 (1) MIN.	MAX.	IDT7165S35 IDT7165L35 MIN.	MAX.	IDT7165S45 IDT7165L45 MIN.	MAX.	IDT7165S55 IDT7165L55 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	30	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	30	–	35	–	45	–	55	ns
t_{ACS1}	Chip Select-1 Access Time (2)	–	15	–	20	–	25	–	30	ns
t_{ACS2}	Chip Select-2 Access Time (2)	–	35	–	40	–	45	–	55	ns
t_{CLZ1}	Chip Select-1 to Output in Low Z (3)	0	–	0	–	0	–	0	–	ns
t_{CLZ2}	Chip Select-2 to Output in Low Z (3)	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	15	–	20	–	25	–	30	ns
t_{OLZ}	Output Enable to Output in Low Z (3)	0	–	0	–	0	–	0	–	ns
t_{CHZ1}	Chip Select-1 to Output in High Z (3)	–	15	–	15	–	20	–	25	ns
t_{CHZ2}	Chip Select-2 to Output in High Z (3)	–	15	–	15	–	20	–	25	ns
t_{OHZ}	Output Disable to Output in High Z (3)	–	15	–	15	–	20	–	25	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time (3)	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Select to Power Down Time (3)	–	30	–	35	–	45	–	55	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. Both chip selects must be active for the device to be selected.
3. This parameter is guaranteed but not tested.

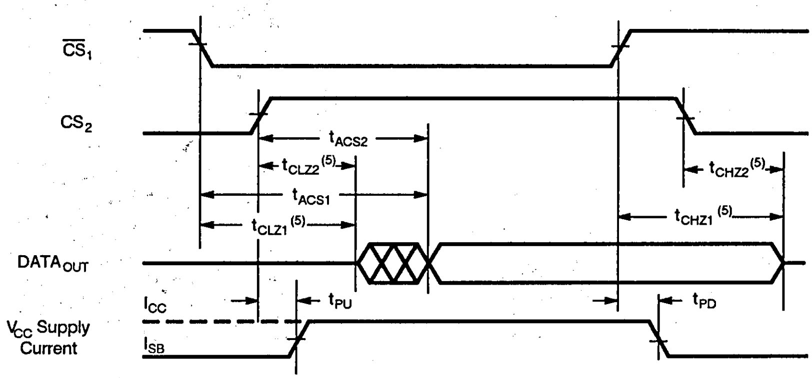
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

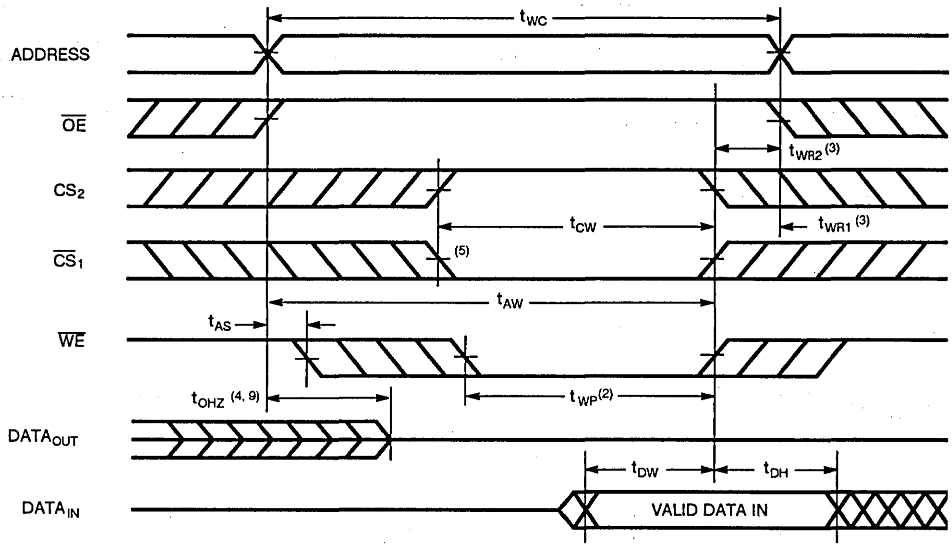
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$.
3. Addresses valid prior to or coincident with $\overline{CS}_1$ transition low and CS_2 transition high.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

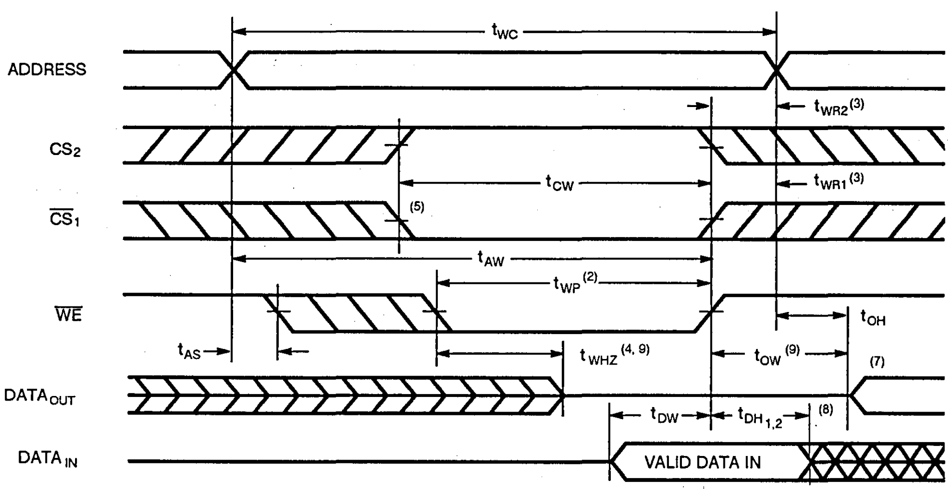
SYMBOL	PARAMETER	IDT7165S30 (1) IDT7165L30 (1) MIN.	MAX.	IDT7165S35 IDT7165L35 MIN.	MAX.	IDT7165S45 IDT7165L45 MIN.	MAX.	IDT7165S55 IDT7165L55 MIN.	MAX.	UNIT
WRITE CYCLE										
t_{WC}	Write Cycle Time	30	–	35	–	45	–	55	–	ns
t_{CW1}	Chip Select-1 to End of Write	20	–	20	–	25	–	30	–	ns
t_{CW2}	Chip Select-2 to End of Write	25	–	30	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	25	–	30	–	40	–	50	–	ns
t_{AS}	Address Setup Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	25	–	30	–	40	–	50	–	ns
t_{WR1}	Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$)	0	–	0	–	0	–	0	–	ns
t_{WR2}	Write Recovery Time (CS_2)	5	–	5	–	5	–	5	–	ns
t_{WHZ}	Write Enable to Output In High Z (2)	–	12	–	15	–	20	–	25	ns
t_{DW}	Data to Write Time Overlap	13	–	15	–	20	–	25	–	ns
t_{DH1}	Data Hold From Write Time ($\overline{CS}_1$)	3	–	3	–	3	–	3	–	ns
t_{DH2}	Data Hold From Write Time (CS_2)	5	–	5	–	5	–	5	–	ns
t_{OW}	Output Active from End of Write (2)	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 [1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 [1, 6]



NOTES:

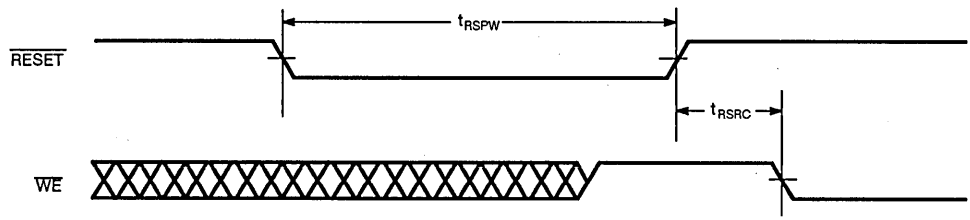
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{WE}$, a low $\overline{CS}_1$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or CS_2 going low to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}_1$ low transition or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. $DATA_{OUT}$ is the same phase of write data of this write cycle.
8. If $\overline{CS}_1$ is low and CS_2 is high during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7165S30 (1) IDT7165L30 (1) MIN.	MAX.	IDT7165S35 IDT7165L35 MIN.	MAX.	IDT7165S45 IDT7165L45 MIN.	MAX.	IDT7165S55 IDT7165L55 MIN.	MAX.	UNIT
RESET										
t_{RSPW}	Reset Pulse Width (2)	55	–	65	–	80	–	100	–	ns
t_{RSRC}	Reset High to $\overline{WE}$ Low	5	–	5	–	10	–	10	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. Recommended duty cycle = 10% maximum.

RESET TIMING



CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

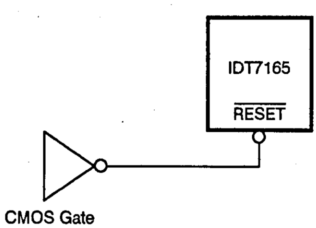
NOTE:
1. This parameter is determined by device characterization, but is not production tested.

TRUTH TABLE

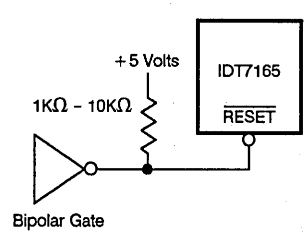
(V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

$\overline{WE}$	$\overline{CS}_1$	CS_2	$\overline{OE}$	$\overline{RESET}$	I/O	FUNCTION
X	X	X	X	L	–	Reset all bits to low
X	H	X	X	H	Z	Deselect chip
X	X	L	X	H	Z	Deselect power down(1)
X	V_{HC}	X	X	H	Z	Deselect chip
X	X	V_{LC}	X	V_{HC}	Z	CMOS deselect power down (1)
H	L	H	H	H	Z	Output disable
H	L	H	L	H	D_{OUT}	Read
L	L	H	X	H	D_{IN}	Write

NOTE:
1. CS_2 will power down $\overline{CS}_1$, but $\overline{CS}_1$ will not power down CS_2.



Driving the $\overline{RESET}$ pin with CMOS logic.



Driving the $\overline{RESET}$ pin with bipolar logic.

Figure 3.

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/ Temperature Range)

Field	Code	Description
Process/ Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B, Method 5004
Package	P	Plastic DIP
	TC	THINDIP (Sidebraze)
	D	CERDIP
	SO	Small Outline IC
	J	Plastic Leaded Chip Carrier
	L	Leadless Chip Carrier
Speed	30	Commercial Only
	35	
	45	
	55	
Power	L	Low Power
	S	Standard Power
Device Type	7165	64K (8K x 8-Bit) Static RAM

Speeds 30, 35, 45, 55: Speed in Nanoseconds

Integrated Device Technology, Inc.

CMOS RESETTABLE RAM WITH CMOS I/O LEVELS 64K (8K x 8-BIT)

IDT71C65S
IDT71C65L

FEATURES:

- Input and output directly CMOS-compatible
- High-speed (equal access and cycle time)
  - Military: 35/45/55ns (max.)
  - Commercial: 30/35/45ns (max.)
- Low-power operation
  - IDT71C65S
    Active: 300mW (typ.)
    Standby: 100µW (typ.)
  - IDT71C65L
    Active: 250mW (typ.)
    Standby: 30µW (typ.)
- Battery backup operation—2V data retention (L version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V(±10%) power supply
- Static operation: no clocks or refresh required
- Available in standard 28-pin, 300 mil THINDIP; 28-pin, 600 mil plastic DIP; 28-pin SOIC and 32-pin LCC
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71C65 is a 65,536-bit high-speed static RAM organized as 8K x 8. Inputs and outputs are compatible with industry standard CMOS input and output voltage levels.

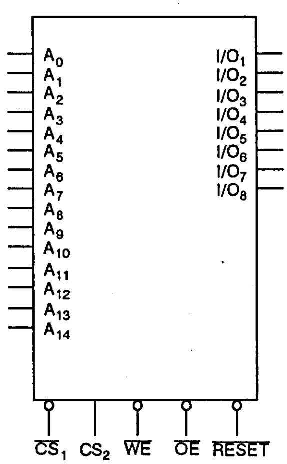
This product is fabricated using IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories. An address access time of 30ns and a chip select ($\overline{CS}_1$) time of 15ns are available with typical power consumption of only 250mW. This circuit also offers a reduced power standby mode. In the full standby mode, the low-power device consumes less than 30µW typically. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 80µW operation off a 2V battery.

All inputs and outputs of the IDT71C65 are CMOS-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

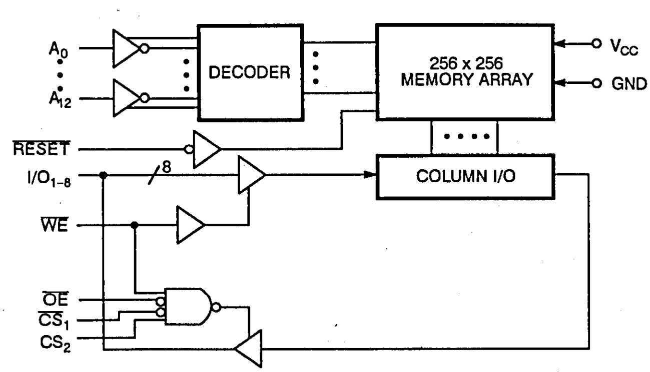
The IDT71C65 is packaged in a 28-pin, 300 mil THINDIP; 600 mil plastic DIP; a 32-pin LCC and a 28-pin SOIC, providing high board level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM

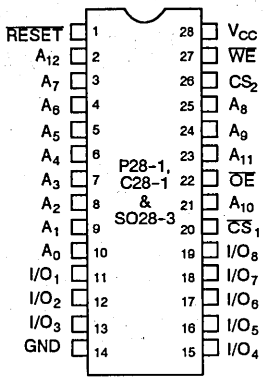


CEMOS is a trademark of Integrated Device Technology, Inc.

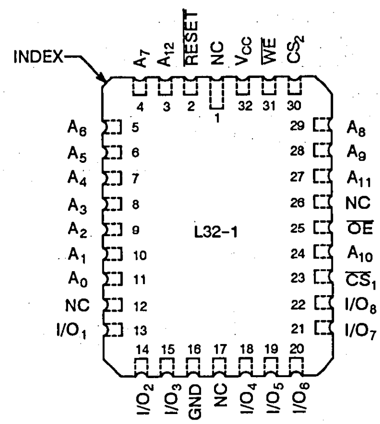
MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-1011/-

PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW



LCC
TOP VIEW

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

PIN NAMES

$A_0 - A_{12}$	Address	$\overline{OE}$	Output Enable
$I/O_1 - I/O_8$	Data Input/Output	$\overline{RESET}$ (1)	Memory Reset
$\overline{CS}_1$, CS_2	Chip Select	GND	Ground
$\overline{WE}$	Write Enable	V_{CC}	Power

NOTE:
1. A 1KΩ pull-up resistor on the $\overline{RESET}$ input is required for added noise immunity.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND(2)	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All inputs and V_{CC} pin. Data pins $I/O_1 - I/O_8$ must not be taken above V_{CC} + 1.0V.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	70% of V_{CC}	—	5.5(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	30% of V_{CC}	V

NOTES:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.
2. If V_{IH} = 5.5V, V_{CC} = 4.5V, there is risk of latch up.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71C65S MIN.	IDT71C65S MAX.	IDT71C65L MIN.	IDT71C65L MAX.	UNIT
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max. $\overline{CS}_1 = V_{IH}$, V_{OUT} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 50µA, V_{CC} = Min.		–	0.1	–	0.1	V
		I_{OL} = 8mA, V_{CC} = Min.	MIL.	–	0.44	–	0.44	V
		I_{OL} = 10mA, V_{CC} = Min.	COM'L.	–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = –50µA, V_{CC} = 4.5V		4.4	–	4.4	–	V
		I_{OH} = –8mA, V_{CC} = 4.5V	COM'L.	3.7	–	3.7	–	V
		I_{OH} = –6mA, V_{CC} = 4.5V	MIL.	3.8	–	3.8	–	V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V, V_{IH} = V_{CC}-0.8V, V_{IL} = 0.8V

SYMBOL	PARAMETER	POWER	IDT71C65S30 IDT71C65L30 COM'L.	MIL.	IDT71C65S35 IDT71C65L35 COM'L.	MIL.	IDT71C65S45 IDT71C65L45 COM'L.	MIL.	IDT71C65S55 IDT71C65L55 COM'L.	MIL.	UNIT
I_{CC1} (2)	Operating Power Supply Current V_{CC} = Max., f = 0(3)	S	95	–	95	105	95	105	–	105	mA
		L	85	–	85	95	85	95	–	95	
I_{CC2} (2)	Dynamic Operating Current Outputs Open; V_{CC} = Max., f = f_{MAX}(3)	S	160	–	160	170	160	170	–	170	mA
		L	135	–	125	135	115	125	–	120	
I_{SB}	Standby Power Supply Current 1) $CS_2 \le V_{IL}$, and $\overline{RESET} \ge V_{IH}$, f = f_{MAX}(3) 2) $\overline{CS}_1 \ge V_{IH}$, V_{CC} = Max., Outputs Open, $CS_2 \ge V_{IH}$, f = f_{MAX}(3), $\overline{RESET} \ge V_{IH}$	S	20	–	20	20	20	20	–	20	mA
		L	3	–	3	5	3	5	–	5	
I_{SB1}	Full Standby Power Supply Current 1) $CS_2 \le V_{LC}$, $\overline{RESET} \ge V_{HC}$, f = 0(3) 2) $\overline{CS}_1 \ge V_{HC}$, $CS_2 \ge V_{HC}$, $\overline{RESET} \ge V_{HC}$ f = 0(3)	S	15	–	15	20	15	20	–	20	mA
		L	0.2	–	0.2	1	0.2	1	–	1	

NOTES:
1. All values are maximum guaranteed values.
2. $CS_2 = V_{IH}$, $\overline{CS}_1 = V_{IL}$
3. At f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

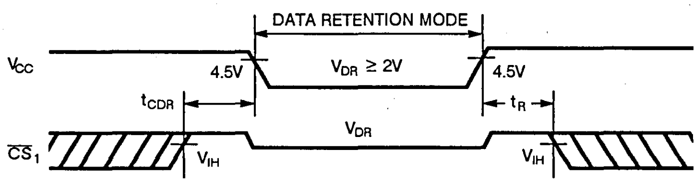
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.[1] V_{CC} @ 2.0V	TYP.[1] V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	1) $\overline{RESET} \geq V_{HC}$, $\overline{CS}_1 \geq V_{HC}$, $CS_2 \geq V_{HC}$ 2) $CS_2 \leq V_{LC}$, $\overline{RESET} \geq V_{HC}$	MIL.	–	10	15	200	300	µA
			COM'L.	–	10	15	60	90	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	–	–	–	–	ns
t_R	Operation Recovery Time			t_{RC}[2]	–	–	–	–	ns
$\lvert I_{LI} \rvert$	Input Leakage Current[3]			–	–	–	2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.
4. During data retention all I/O pins have to be $\leq V_{LC}$ or $\geq V_{HC}$ but $\leq V_{CC}$.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to V_{CC}
Input Rise/Fall Times	5ns
Input Timing Reference Levels	2.5V
Output Reference Levels	2.5V
Output Load	See Figures 1 and 2

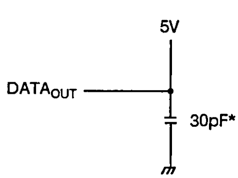


Figure 1. Output Load

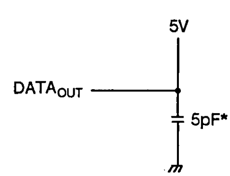


Figure 2. Output Load
(for t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{OW}, t_{WHZ})

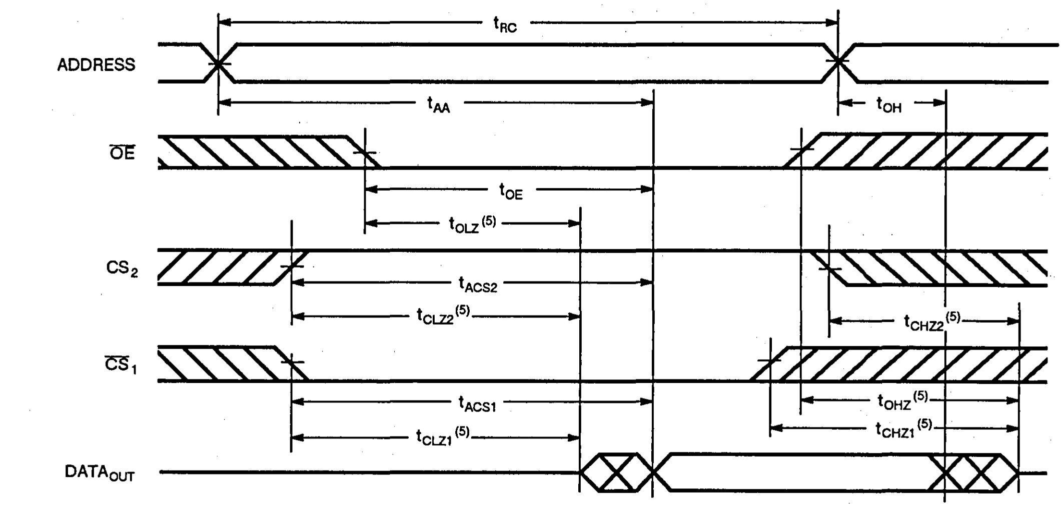
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

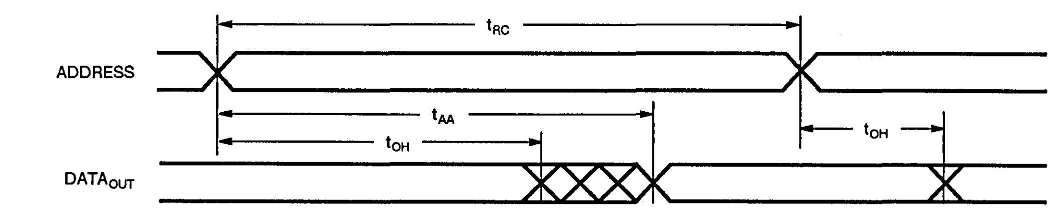
SYMBOL	PARAMETER	IDT71C65S30(1) IDT71C65L30(1) MIN.	MAX.	IDT71C65S35 IDT71C65L35 MIN.	MAX.	IDT71C65S45 IDT71C65L45 MIN.	MAX.	IDT71C65S55(4) IDT71C65L55(4) MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	30	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	30	–	35	–	45	–	55	ns
t_{ACS1}	Chip Select 1 Access Time (2)	–	20	–	25	–	35	–	40	ns
t_{ACS2}	Chip Select 2 Access Time (2)	–	35	–	40	–	45	–	55	ns
t_{CLZ1}	Chip Select 1 to Output in Low Z (3)	0	–	0	–	0	–	0	–	ns
t_{CLZ2}	Chip Select 2 to Output in Low Z (3)	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	20	–	25	–	35	–	40	ns
t_{OLZ}	Output Enable to Output in Low Z (3)	0	–	0	–	0	–	0	–	ns
t_{CHZ1}	Chip Select 1 to Output in High Z (3)	–	15	–	20	–	25	–	30	ns
t_{CHZ2}	Chip Select 2 to Output in High Z (3)	–	15	–	20	–	25	–	30	ns
t_{OHZ}	Output Disable to Output in High Z (3)	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time (3)	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time (3)	–	30	–	35	–	45	–	55	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. Both chip selects must be active for the device to be selected.
3. This parameter is guaranteed but not tested.
4. -55°C to +125°C temperature range only.

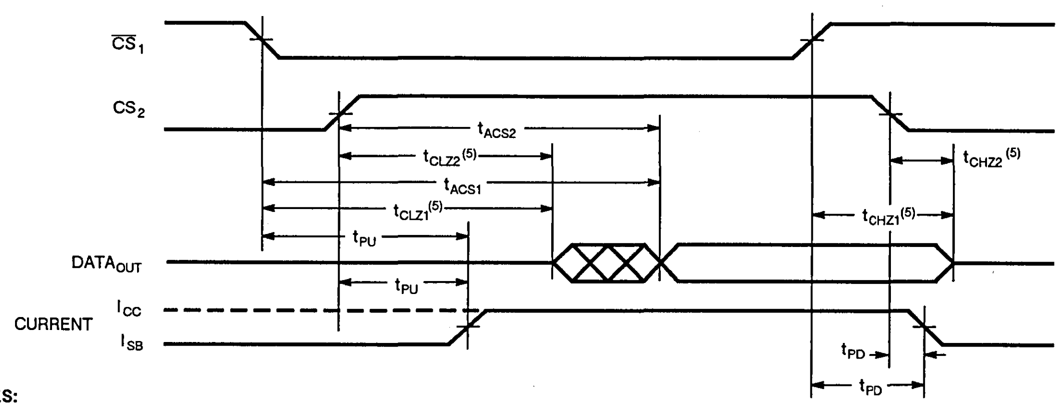
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

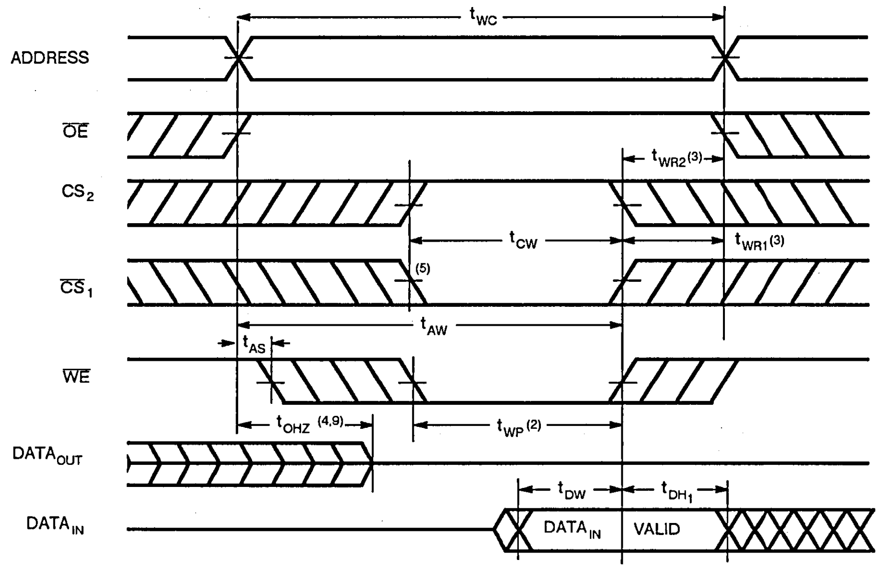
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low and CS_2 transition high.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

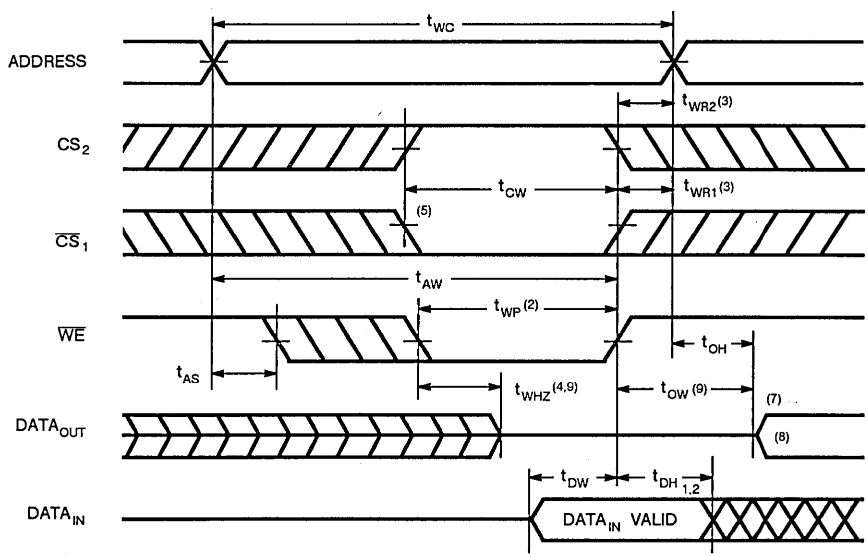
SYMBOL	PARAMETER	IDT71C65S30 (1) IDT71C65L30 (1) MIN.	MAX.	IDT71C65S35 IDT71C65L35 MIN.	MAX.	IDT71C65S45 IDT71C65L45 MIN.	MAX.	IDT71C65S55 (2) IDT71C65L55 (2) MIN.	MAX.	UNIT
WRITE CYCLE										
t_{WC}	Write Cycle Time	30	–	35	–	45	–	55	–	ns
t_{CW1}	Chip Select 1 to End of Write	20	–	20	–	25	–	30	–	ns
t_{CW2}	Chip Select 2 to End of Write	25	–	30	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	25	–	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	25	–	30	–	40	–	50	–	ns
t_{WR1}	Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$)	0	–	0	–	0	–	0	–	ns
t_{WR2}	Write Recovery Time (CS_2)	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output In High Z (3)	–	10	–	12	–	15	–	20	ns
t_{DW}	Data to Write Time Overlap	15	–	18	–	25	–	30	–	ns
t_{DH1}	Data Hold From Write Time ($\overline{CS}_1$, $\overline{WE}$)	0	–	0	–	0	–	0	–	ns
t_{DH2}	Data Hold From Write Time (CS_2)	5	–	5	–	5	–	5	–	ns
t_{OW}	Output Active from End of Write (3)	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2[1, 6]



NOTES:

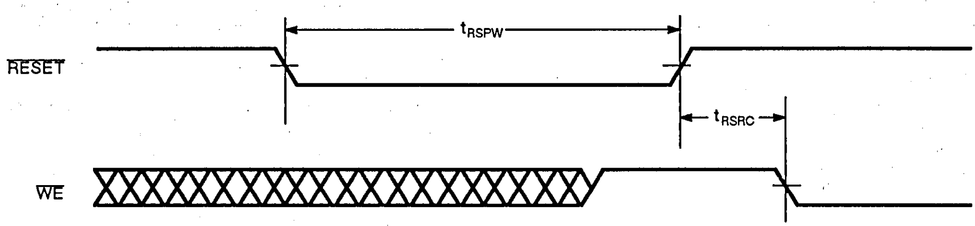
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}_1$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}_1$ low transition or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. $DATA_{OUT}$ is the same phase of write data of this write cycle.
8. If $\overline{CS}_1$ is low and CS_2 is high during this period, I/O pins are in the output state. Data input signals must not be applied.
9. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71C65S30(1) IDT71C65L30(1) MIN.	MAX.	IDT71C65S35 IDT71C65L35 MIN.	MAX.	IDT71C65S45 IDT71C65L45 MIN.	MAX.	IDT71C65S55(2) IDT71C65L55(2) MIN.	MAX.	UNIT
$\overline{\text{RESET}}$(3)										
t_{RSPW}	$\overline{\text{RESET}}$ Pulse Width(4)	55	—	65	—	80	—	100	—	ns
t_{RSR}	$\overline{\text{RESET}}$ High to $\overline{\text{WE}}$ Low	5	—	5	—	10	—	10	—	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. A 1KΩ pull-up resistor to V_{CC} on the $\overline{\text{RESET}}$ pin is required for added noise immunity.
4. Maximum 10% duty cycle applies.

$\overline{\text{RESET}}$ TIMING



ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range:
- Blank — Commercial (0°C to +70°C)
- B — Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:
- P — Plastic DIP
- TC — Sidebraze THINDIP
- L — Leadless Chip Carrier
- SO — Small Outline IC

Speed (Speed in Nanoseconds):
- 30 — Commercial Only
- 35
- 45
- 55 — Military Only

Power:
- S — Standard Power
- L — Low Power

Device Type:
- 71C65 — 64K (8K x 8-Bit) CMOS I/O Resettable RAM

Integrated Device Technology, Inc.

CMOS SYNCHRONOUS RAM 64K (64K x 1-BIT)

PRELIMINARY
IDT71501S

FEATURES:

- Internal pipeline registers on Address, Data and control lines
- Very fast write cycle time
- High-speed
  - Military: 45ns (max.)
  - Commercial: 35/45ns (max.)
- Low power consumption: 385mW (typ.)
- All inputs/outputs TTL-compatible (V_{OL} = 0.4V @ I_{OL} = 8mA)
- Separate, latched data input and output
- Three-state output
- Available in JEDEC standard 24-pin, 300 mil Sidebraze and Plastic DIP, 24-pin, 300 mil SOIC and 28-pin LCC
- Produced with advanced CEMOS™ high-performance technology
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71501 is a high-speed 64K x 1 static RAM synchronized with pipeline registers on the Address, Data, Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) pins. This product is designed to assist in the design of pipelined processing systems by removing the need for external pipeline registers. The internal registers offer speed improvements through higher integration of system functions.

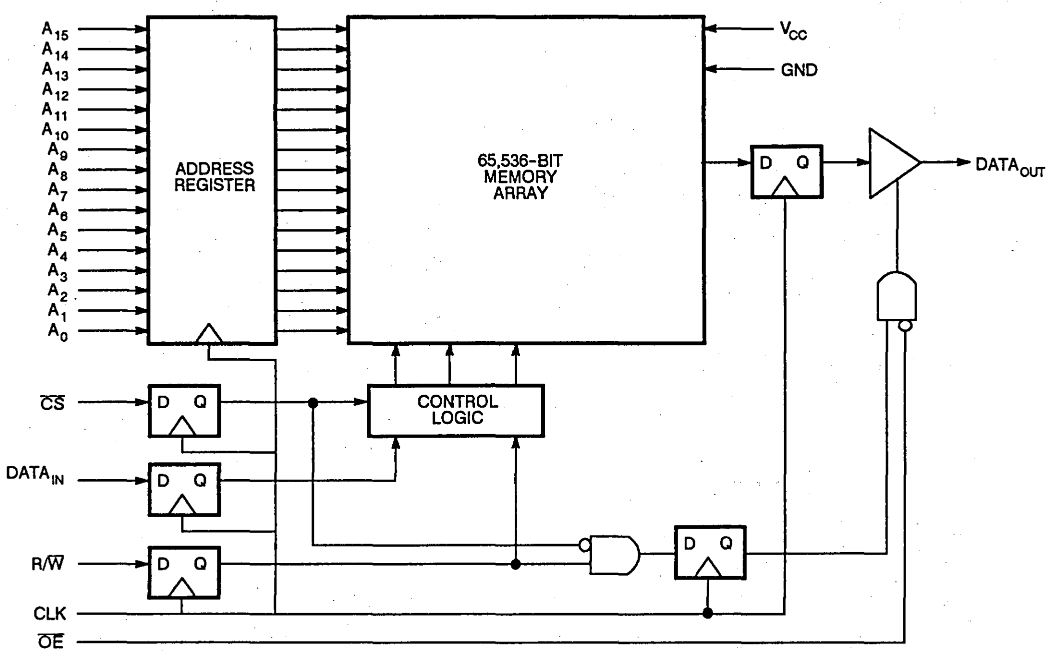
Read cycle times are as fast as 35ns, with higher speed Output Enable ($\overline{OE}$) and Clock to Valid Data Output functions to enable the high-speed system designer the maximum throughput possible in an efficient large-memory pipelined system. Write cycles are as fast as 25ns. Fabricated using IDT's CEMOS high-performance technology, these devices typically operate on 385mW of power.

The IDT71501 is packaged in industry standard 24-pin, 300 mil plastic and ceramic DIPs, as well as a 28-pin leadless chip carrier (LCC) and a 24-lead, 300 mil gullwing SOIC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

4

FUNCTIONAL BLOCK DIAGRAM

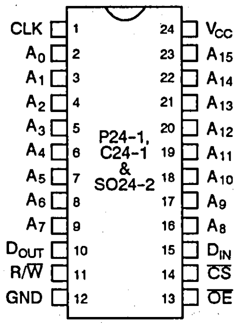


CEMOS is a trademark of Integrated Device Technology, Inc.

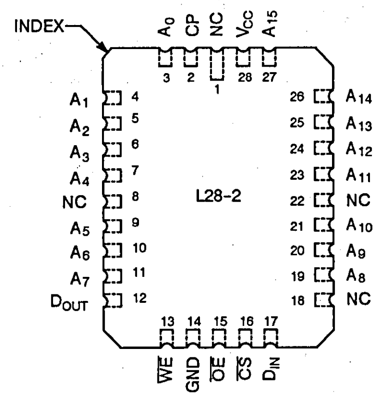
MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-1038/-

PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71501S MIN.	IDT71501S MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	MIL. COM'L.	– –	10 5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC} V_{CC} = Max.	MIL. COM'L.	– –	10 5	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open V_{CC} = Max.	MIL. COM'L.	– –	140 125	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100% V_{CC} = Max., Output Open	MIL. COM'L.	– –	140 125	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		–	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		–	0.5	
V_{OH}	Output High Voltage	I_{OL} = –4mA, V_{CC} = Min.		2.4	–	V

4

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

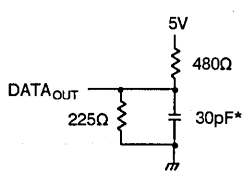


Figure 1. Output Load

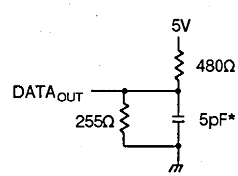


Figure 2. Output Load (for t_{OLZ}, t_{OHZ})

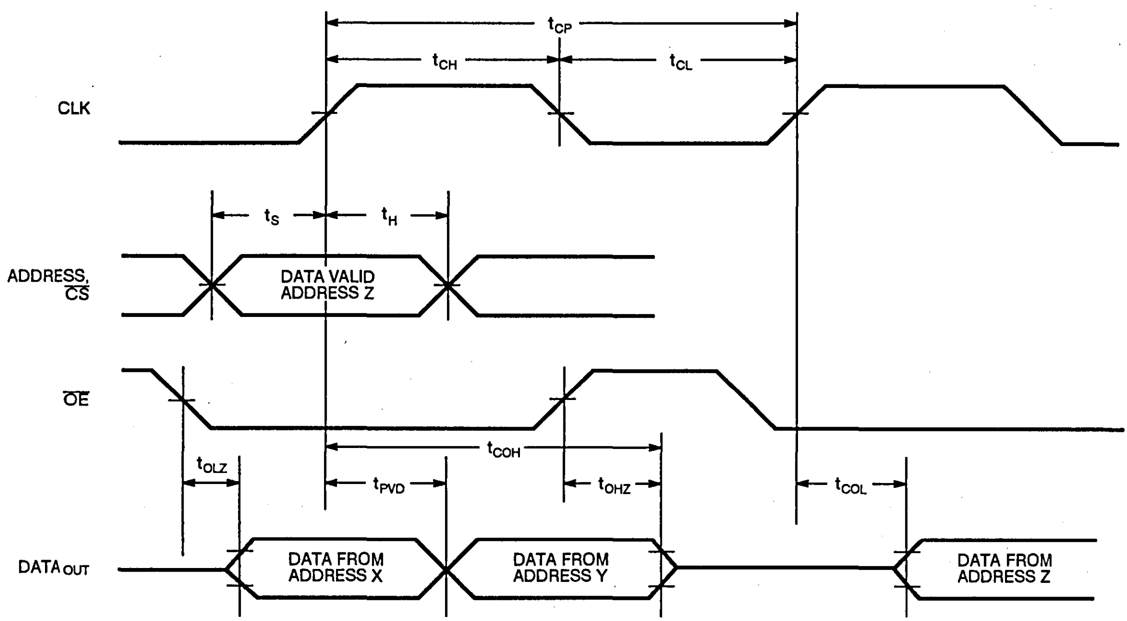
*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

SYMBOL	PARAMETER	IDT71501S35 MIN.	IDT71501S35 MAX.	IDT71501S45 MIN.	IDT71501S45 MAX.	UNIT
READ CYCLE						
t_{CP}	Clock Period (Read Cycle Time)	35	–	45	–	ns
t_{CH}	Clock High Time	7	–	7	–	ns
t_{CL}	Clock Low Time	7	–	7	–	ns
t_S	Data, Address, $\overline{WE}$, $\overline{CS}$ Set-up Time	5	–	5	–	ns
t_H	Data, Address, $\overline{WE}$, $\overline{CS}$ Hold Time	5	–	5	–	ns
t_{OLZ}	Output Low Z Time (1, 2)	0	–	0	–	ns
t_{OHZ}	Output High Z Time (1, 2)	–	15	–	20	ns
t_{PVD}	Prop. Delay, CLK to Valid Data Out	13	–	18	–	ns
t_{COL}	Clock to Output in Low Z (2)	0	–	0	–	ns
t_{COH}	Clock to Output in High Z (2)	–	20	–	25	ns

NOTES:
1. Transition is measured ±200mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE (1)



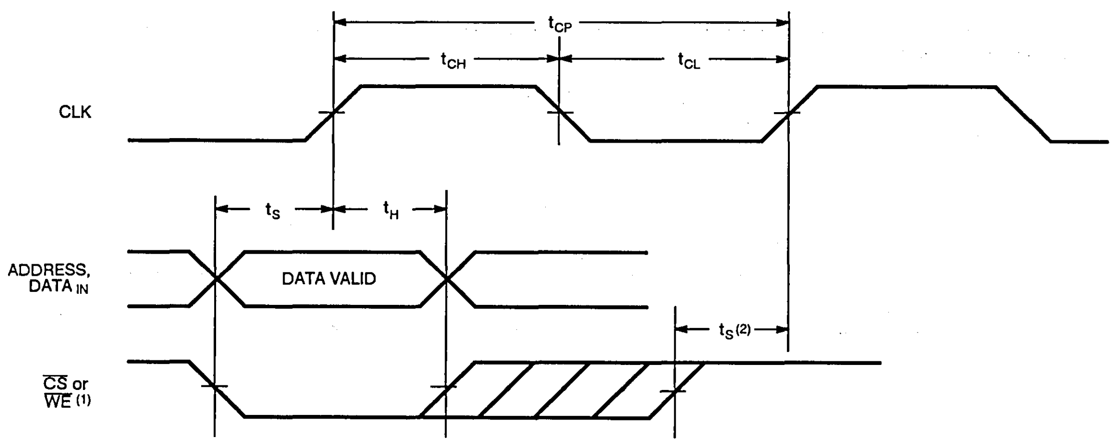
NOTE:
1. The device must be selected by a $\overline{CS}$ level for the conditions above to take place.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

SYMBOL	PARAMETER	IDT71501S35 MIN.	IDT71501S35 MAX.	IDT71501S45 MIN.	IDT71501S45 MAX.	UNIT
WRITE CYCLE						
t_{CP}	Clock Period (Write Cycle Time)	25	–	35	–	ns
t_{CH}	Clock High Time	7	–	7	–	ns
t_{CL}	Clock Low Time	7	–	7	–	ns
t_S	Data, Address, $\overline{WE}$, $\overline{CS}$ Set-up Time	5	–	5	–	ns
t_H	Data, Address, $\overline{WE}$, $\overline{CS}$ Hold Time	5	–	5	–	ns

4

TIMING WAVEFORM OF WRITE CYCLE



NOTES:
1. Either $\overline{CS}$ or $\overline{WE}$ can be used to trigger a write cycle, provided that the other signal is low at the same time.
2. When a write is terminated, either $\overline{CS}$ or $\overline{WE}$ must become high at least one t_S before the next rising edge of CLK.

TRUTH TABLE

MODE	INPUT BEFORE CLK ↑ A_{0-15}	$\overline{CS}$	D_{IN}	$\overline{WE}$	$\overline{OE}$	AFTER CLK ↑ D_{OUT}
Read	ADDR	L	X	H	L	Data
Write	ADDR	L	Data	L	X	High Z
Deselect	X	H	X	X	X	High Z
Disable	X	X	X	X	H	High Z

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	P	Plastic DIP
	C	Sidebraze DIP
	SO	Small Outline IC
	L	LCC
Speed	35	Commercial Only } Speed in Nanoseconds
	45	
Power	S	Standard Power
Device Type	71501	64K (64K x 1-Bit) CMOS Synchronous RAM

512K (64K x 8) SYNCHRONOUS STATIC RAM PLASTIC SIP MODULE

ADVANCE INFORMATION
IDT7MP6025

FEATURES:

- 64K x 8 fully synchronous memory
- High-speed—20MHz read cycle time
- 16-bit synchronous address input
- 8-bit synchronous data input
- Synchronous chip select and write enable
- Separate clock enable for each register
- Low standby power
- Onboard decoupling capacitors
- Available in 43-pin SIP (single in-line package) configuration
- 2 Ground and 2 V_{CC} pins

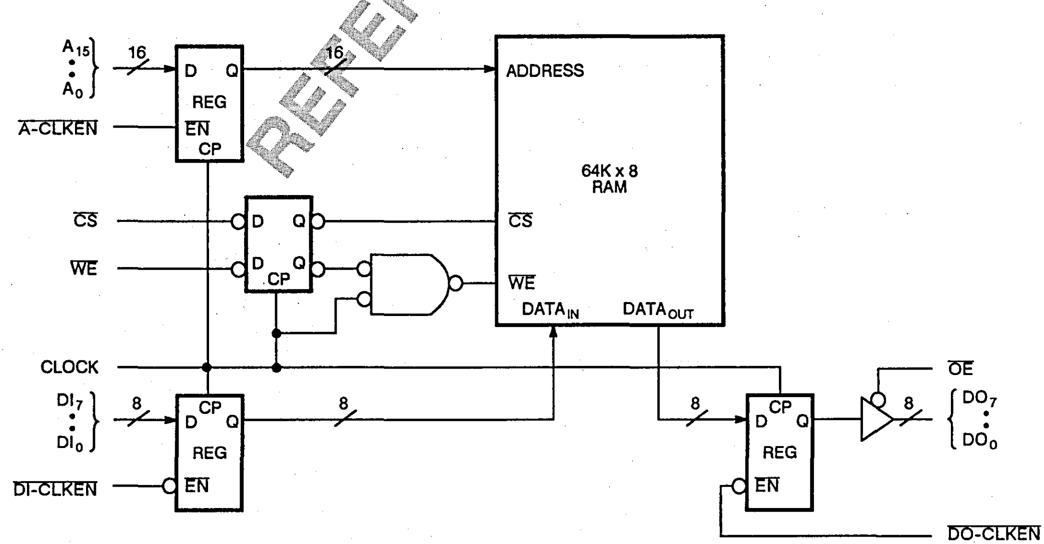
DESCRIPTION:

The IDT7MP6025 is a 64K x 8 synchronous RAM with edge triggered registers on the address lines, data-in bus, data-out bus, chip select and write enable. The edge triggered register of the 16 address lines features an independent clock enable that allows the address register to be selectively loaded. The address register will be loaded on the low-to-high transition of the clock when the clock enable line is low and will hold its current contents on the low-to-high transition of the clock when the clock enable is high. Similarly, the 8-bit data-in register will be loaded with new data on the low-to-high transition of the clock when the data-in clock enable is low and will hold its contents when the data-in clock enable is high. The data-out register will receive new data from the 64K x 8 RAM when the clock enable line is low and will hold its data when the clock enable line is high at the low-to-high transition of the clock. All clock enables, as well as address and data inputs, must meet the appropriate set-up and hold times with respect to the clock.

The eight data output bits are enabled when the output enable is low and are in the high-impedance state when the output enable is high. The chip select and write enable signals are also registered in D flip-flops. These two flip-flops are loaded with new data on each low-to-high transition of the clock. The chip select is passed directly from the Q output of the D-type flip-flop to the 64K x 8 RAM. The write enable signal is gated with the clock signal to generate a delayed write enable pulse. In essence, this gives the output of the address register time to settle and internally select the appropriate byte of RAM before the write enable goes low to write new data into the RAM. Thus, the low-to-high transition of the clock causes the chip select and write enable flip-flops to be loaded with new data and immediately deselects a previous write by means of the clock going high. The data lines to the RAM and the address lines to the RAM may indeed change to new values based on the low-to-high transition of the clock. When the clock goes from high-to-low, if the chip select is low and the write enable is low, a write cycle is begun and the data at the RAM data inputs will be written into the selected address. If the write enable is high or the chip enable is high, data will not be written into the memory.

One of the features of this configuration of memory that have registers on all of the address lines, data input lines and data output lines as well as the control lines, is to provide the highest possible clock rate in the system. All that is necessary is that the data, address, chip select, write enable and clock enables signals meet the required set-up and hold time with respect to the clock. In this manner, fully asynchronous operation is achieved. The IDT7MP6025 is offered as a compact, cost-effective 43-pin plastic SIP module.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE **DECEMBER 1987**

Integrated Device Technology, Inc.

DUAL MULTIPLEXED 16K x 20 SYNCHRONOUS STATIC RAM MODULE

ADVANCE INFORMATION
IDT7M6001

FEATURES:

- Dual 16K x 20 synchronous RAM
- Edge triggered data input and data output registers
- Edge triggered data address registers
- Two address register sources individually selectable
- Separate chip select and write enables to each memory array
- Individual clock lines to each register
- Dual high-performance 16K x 20 memories
- Unique ping-pong operation capability
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in compact 92-pin ceramic sidebraze QIP (quad in-line) package
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Military modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

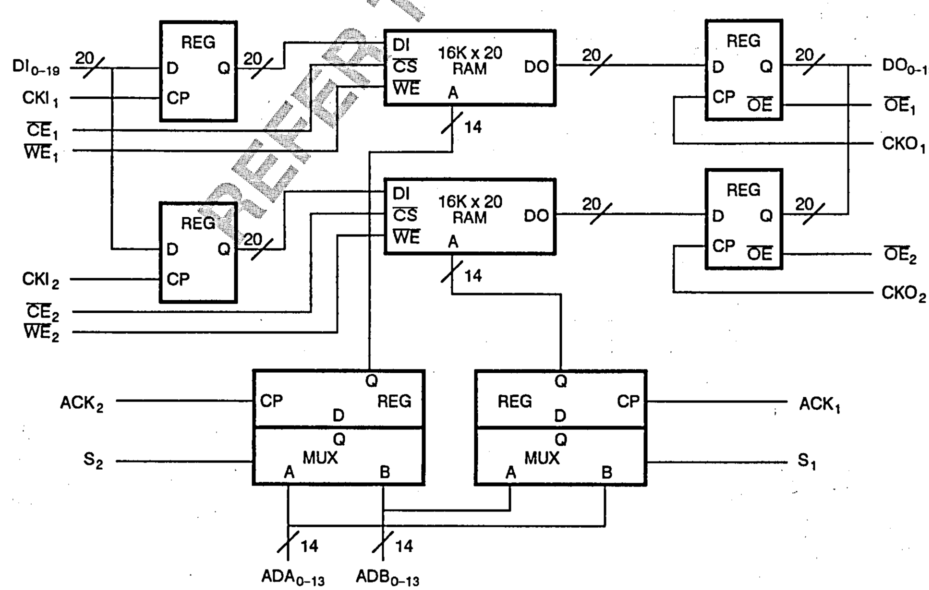
The IDT7M6001 is a dual multiplexed 16K x 20 synchronous RAM module. It utilizes ten IDT71981 high-speed synchronous memories, along with the appropriate input data, output data and address registers. The device features the ability to be used in a ping-pong mode. That is, data can be loaded into one memory array at one address and be read from the other memory array at a different address. This allows systems to be built that can perform fast Fourier Transforms in either a decimation-in-time or a decimation-in-frequency configuration. Data read from Memory 1 can be synchronously loaded into its output register, while data can be written into a different location in Memory 2. Similarly, data can be read from Memory 1 and Memory 2 in parallel from two different addresses and can be written into Memory 1 and Memory 2 at unique addresses. Registers at the data input and data output provide fully synchronous pipelined operation. The two memory systems are 20 bits wide and have multiplexed data input and data output bits from the module data pins. By taking advantage of the speed of the registers, data on the pins can run at a speed twice that of the memory. That is, both output registers can be read or both input registers can be loaded in a single memory cycle.

Two address sources are available to each address register to the RAM. Address Source A or Address Source B may be selected to load the edge triggered register for the 16K x 20-bit memory. The IDT54/74FCT399 is used for the two input multiplexer and address registers for each 16K x 20 memory. All inputs and outputs of the IDT7M4017 are TTL-compatible and operate from a single 5V supply.

The IDT7M6001 is offered as a compact 92-pin quad in-line (QIP) ceramic module. It is constructed using ceramic LCC components on a multilayer co-fired ceramic substrate and occupies only 4.2 square inches of board space.

All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

1 MEGABIT (128K x 8) REGISTERED/BUFFERED/ LATCHED CMOS STATIC RAM SUBSYSTEMS

IDT7M824 FAMILY

4

FEATURES:

- High-density 1024K-bit (128K x 8-bit) CMOS static RAM modules with registered/buffered/latched addresses and I/Os
- High-speed registered access time:
  - Military temperature range: 60ns (max.)
  - Commercial temperature range: 50ns (max.)
- 20MHz read cycle time
- Low power consumption (typ.)
  - Active: 1.5W
  - Standby: 75mW
- Low input capacitance (typ.): input 20pF; output 25pF
- High output drive (min.): I_{OL} = 48mW; I_{OH} = -15mA
- Available in 64-pin, 900 mil centre sidebraze DIP (with LCCs on both sides), achieving very high memory density
- Module select output
- Separate inputs and outputs
- Clear data and clock enables on all registers
- Address, input and outputs on separate clocks or latch enables
- Registered write enable
- Internal bypass capacitors for minimizing power supply noise
- TTL-compatible; single 5V (±10%) power supply
- Five GND pins for maximum noise immunity, five V_{CC} pins
- Military grade module available with semiconductor components compliant to the latest revision of MIL-STD-883, Class B

DESCRIPTION:

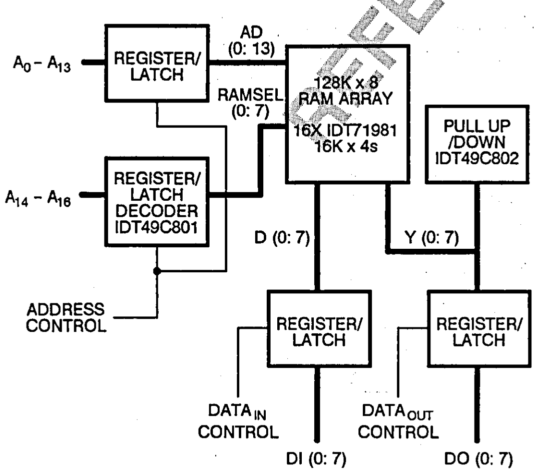
The IDT7M824 family is a set of 1024K-bit (128K x 8-bit) high-speed CMOS static RAM modules with registered/buffered/ latched addresses and I/Os. They are constructed on co-fired, multi-layered ceramic substrates with sidebrazed leads using 16 IDT71981 (16K x 4) static RAMs, IDT logic devices and decoupling capacitors. Devices in leadless chip carriers are mounted top and bottom for maximum density.

Extremely high speeds are achievable by the use of IDT71981s and logic devices fabricated in IDT's high-performance, high-reliability CEMOS ™ technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest circuits possible. The IDT7M824 has registered access times of 50ns (max.) over the commercial temperature range and can be operated with cycle times as fast as 20MHz.

Designing with this device can be very flexible because of such features as module select output and clock enables on all registers, registered write enable and 8-bit separate inputs and outputs. Because of the proprietary IDT49C801, the modules are cascadable in terms of depth with no additional external decoding. The write enable can be turned off when the module is deselected. Immunity to noise has been extended with such features as 8-bit separate inputs and outputs; addresses, inputs, and outputs on separate clocks; internal decoupling capacitors; five ground pins and five V_{CC} pins.

The semiconductor components used on all IDT military modules are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT SELECTOR GUIDE

PART NO.	I/O AND ADDRESS FEATURES		
	ADDRESS BUS	INPUT DATA BUS	OUTPUT DATA BUS
IDT7M820	L/B	L/B	L/B
IDT7M821	L/B	R	R
IDT7M822	L/B	R	L/B
IDT7M823	L/B	L/B	R
IDT7M825	R	R	R
IDT7M826	R	R	L/B
IDT7M827	R	L/B	R
IDT7M828	R	L/B	L/B

NOTES:

1. L/B = LATCHED/BUFFERED
   R = REGISTERED
2. For module dimensions, please refer to module drawing M8 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-7000/-

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (4K x 16-BIT) REGISTERED RAM w/SPC™

ADVANCE INFORMATION
IDT71502S
IDT71502L

FEATURES:

- 4K x 16-bit RAM with register at output, serial load and readback
- Designed for microprogram writable control store
- Serial Protocol Channel (SPC) allows load and readout of RAM over a 4-wire channel
- RAM address counter speeds RAM load, readout
- Outputs may be programmed to be registered or non-registered in groups of 8 bits
- Initialize register allows initial microword selection
- Synchronous and asynchronous output enables allow for depth expansion and bus driving
- Breakpoint comparator supports system diagnostics
- Parity check on outputs for high-reliability designs
- High-speed (address set-up before clock)
  - Military: 45/55ns (max.)
  - Commercial: 35/45ns (max.)
- Built in CMOS for low power consumption
- Inputs and outputs directly TTL-compatible
- Standard 48-pin DIP
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71502 Registered RAM is designed expressly for efficient use in writable control stores. This 65,536-bit high-speed static RAM is organized as 4K x 16 bits with a high-speed register at the RAM outputs and serial load and readback capability using the IDT Serial Protocol Channel (SPC). Its architecture is optimized for microprogram writable control store use. Hardware is provided for software test and debug, parity checking and serial microcode load at initialization.

The IDT71502 is available with address set-up before clock times as fast as 35ns with a maximum power consumption of only 900mW.

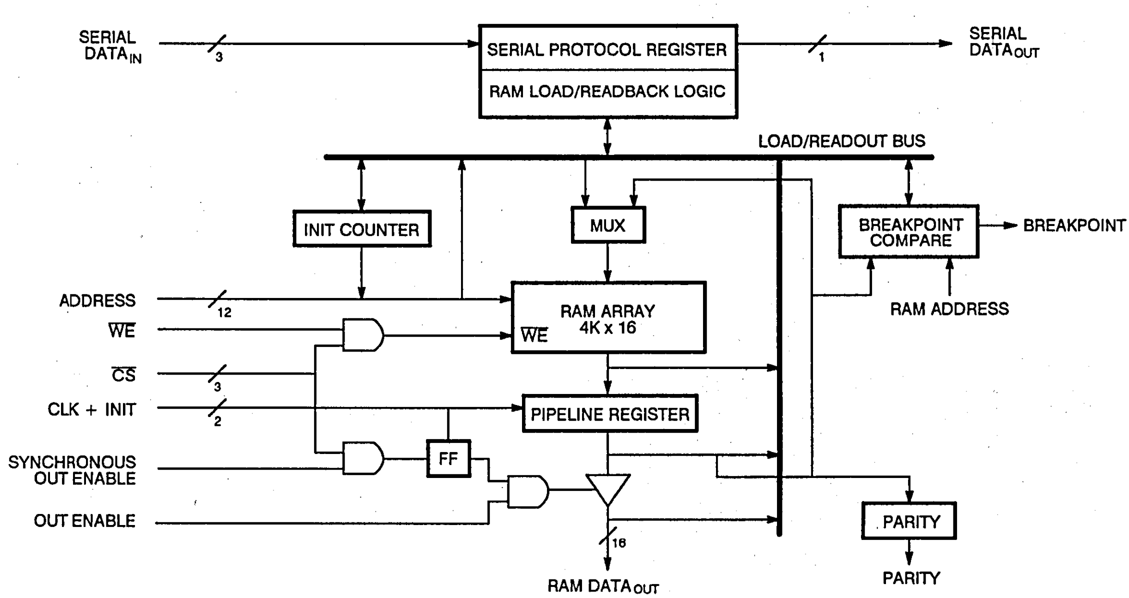
All inputs and outputs of the IDT71502 are TTL-compatible and the device operates from a single 5V supply. Fully static, asynchronous circuitry is used, requiring no clocks (with the exception of the register clock) or refreshing for operation.

The IDT71502 is fabricated using IDT's high-performance, high-reliability technology — CEMOS ™. This technology gives the IDT71502 the combination of low power, high speed and high density that makes it a cost-effective alternative to bipolar and NMOS devices such as registered PROMs.

The IDT71502 is packaged in a 48-pin, 600 mil DIP, providing high board level packing densities.

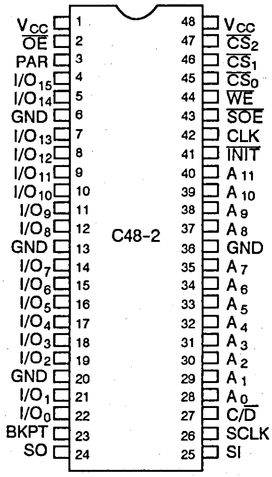
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



CEMOS and SPC are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP
TOP VIEW

PIN NAMES

NAME	FUNCTION
A_{0-11}	Address
I/O_{0-15}	Data Input/Output
$\overline{CS}_{0-2}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{SOE}$	Synchronous Output Enable
CLK	Clock (to register)
$\overline{INIT}$	Initialize
BKPT	Breakpoint Detect
PAR	Parity
SI	SPC Serial $DATA_{IN}$ (1)
SO	SPC Serial $DATA_{OUT}$ (1)
SCLK	SPC Clock (1)
$C/\overline{D}$	SPC Command/$\overline{Data}$ (1)
GND	Ground
V_{CC}	Power

NOTE:
1. The Serial Protocol Channel (SPC) is discussed at length in IDT Application Note 16.

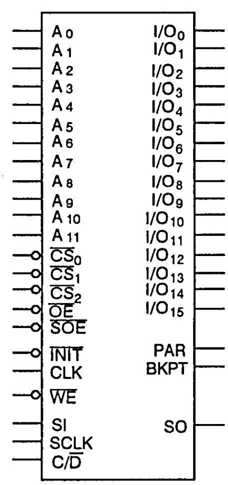
TRUTH TABLE - READ/WRITE OPERATIONS STANDARD PIPELINED MODE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{SOE}$	CLK	I/O OPERATION
Deselected	H	X	L	X	↑	High Z
Read	L	H	H	X	X	High Z
Read	L	H	L	H	↑	High Z
Read	L	H	L	L	↑	$DATA_{OUT}$ @ Address
Write	L	L	X	X	X	$DATA_{IN}$ @ Address

TRUTH TABLE - SPC OPERATIONS

MODE	$C/\overline{D}$	SCLK	FUNCTION
Command	H	↑	Shift bit into command register
Data	L	↑	Shift bit into data register
Execute	↓	↑	Execute command during time between $C/\overline{D}$ and SCLK

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1) (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71502S MIN.	IDT71502S TYP.(1)	IDT71502S MAX.	IDT71502L MIN.	IDT71502L TYP.(1)	IDT71502L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage (2)	I_{OL} = 16mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
V_{OH}	Output High Voltage (2)	I_{OH} = -8mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage, BKPT	I_{OL} = 24mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V

NOTES:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.
2. All outputs except BKPT, which is open drain.

4

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	POWER	IDT71502S35(2) IDT71502L35(2) COM'L.	MIL.	IDT71502S45 IDT71502L45 COM'L.	MIL.	IDT71502S55(3) IDT71502L55(3) COM'L.	MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0	S	–	–	–	–	–	–	mA
		L	–	–	–	–	–	–	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}	S	–	–	–	–	–	–	mA
		L	–	–	–	–	–	–	

NOTES:
1. All values are guaranteed maximums.
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71502S35[1] IDT71502L35[1] MIN.	MAX.	IDT71502S45 IDT71502L45 MIN.	MAX.	IDT71502S55[2] IDT71502L55[2] MIN.	MAX.	UNIT
READ CYCLE								
t_{RC}	Read Cycle Time	50	–	65	–	80	–	ns
t_{AS}	Address Set-up Time	35	–	45	–	55	–	ns
t_{CS}	Chip Select Set-up Time	15	–	18	–	20	–	ns
t_S	Set-up Time: $\overline{SOE}$	15	–	18	–	20	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	ns
t_{CH}	Chip Select Hold Time	5	–	5	–	5	–	ns
t_H	Hold Time: $\overline{SOE}$	5	–	5	–	5	–	ns
t_{CD}	Clock to Output Delay	–	15	–	20	–	25	ns
t_{CWH}	Clock Width, High	20	–	25	–	30	–	ns
t_{CWL}	Clock Width, Low	20	–	25	–	30	–	ns
t_{AAN}	Address Access Time, Non-Pipelined	–	50	–	65	–	80	ns
t_{OE}	Asynchronous Output Enable Time	–	20	–	25	–	30	ns
t_{OZ}	Asynchronous Output Disable Time[3]	–	20	–	25	–	30	ns
t_{SOE}	Synchronous Output Enable Time	–	25	–	30	–	35	ns
t_{SOZ}	Synchronous Output Disable Time[3]	–	25	–	30	–	35	ns
t_{INIT}	Initialize to Output Delay	–	60	–	75	–	90	ns
t_{IR}	Initialize Recovery Time	50	–	60	–	75	–	ns
t_{IW}	Initialize Pulse Width	50	–	60	–	75	–	ns
t_{BPR}	Breakpoint Delay From Register	–	40	–	50	–	60	ns
t_{BPA}	Breakpoint Delay From Address	–	40	–	50	–	60	ns
t_{PAR}	Parity Generation Time	–	50	–	60	–	75	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (4K x 16-BIT) REGISTERED RAM w/SPC™

ADVANCE INFORMATION
IDT71502S
IDT71502L

FEATURES:

- 4K x 16-bit RAM with register at output, serial load and readback
- Designed for microprogram writable control store
- Serial Protocol Channel (SPC) allows load and readout of RAM over a 4-wire channel
- RAM address counter speeds RAM load, readout
- Outputs may be programmed to be registered or non-registered in groups of 8 bits
- Initialize register allows initial microword selection
- Synchronous and asynchronous output enables allow for depth expansion and bus driving
- Breakpoint comparator supports system diagnostics
- Parity check on outputs for high-reliability designs
- High-speed (address set-up before clock)
  - Military: 45/55ns (max.)
  - Commercial: 35/45ns (max.)
- Built in CMOS for low power consumption
- Inputs and outputs directly TTL-compatible
- Standard 48-pin DIP
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71502 Registered RAM is designed expressly for efficient use in writable control stores. This 65,536-bit high-speed static RAM is organized as 4K x 16 bits with a high-speed register at the RAM outputs and serial load and readback capability using the IDT Serial Protocol Channel (SPC). Its architecture is optimized for microprogram writable control store use. Hardware is provided for software test and debug, parity checking and serial microcode load at initialization.

The IDT71502 is available with address set-up before clock times as fast as 35ns with a maximum power consumption of only 900mW.

All inputs and outputs of the IDT71502 are TTL-compatible and the device operates from a single 5V supply. Fully static, asynchronous circuitry is used, requiring no clocks (with the exception of the register clock) or refreshing for operation.

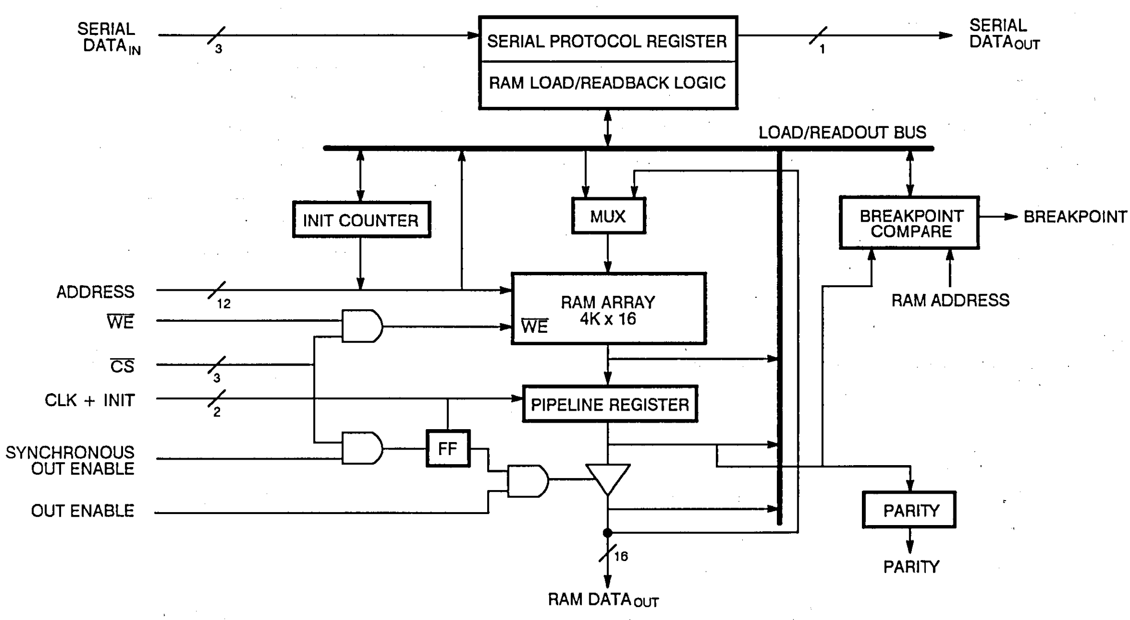
The IDT71502 is fabricated using IDT's high-performance, high-reliability technology—CEMOS™. This technology gives the IDT71502 the combination of low power, high speed and high density that makes it a cost-effective alternative to bipolar and NMOS devices such as registered PROMs.

The IDT71502 is packaged in a 48-pin, 600 mil DIP, providing high board level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

4

FUNCTIONAL BLOCK DIAGRAM



CEMOS and SPC are trademarks of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

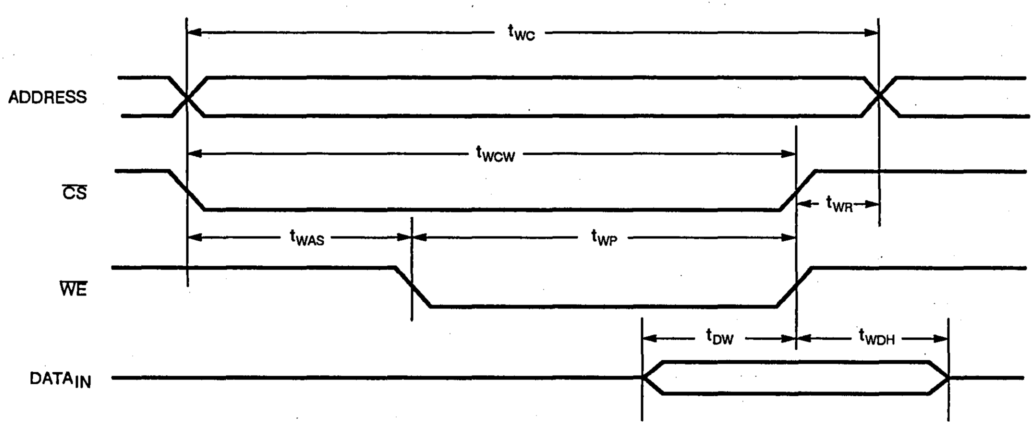
DSC-1039/-

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71502S35[1] IDT71502L35[1] MIN.	MAX.	IDT71502S45 IDT71502L45 MIN.	MAX.	IDT71502S55[2] IDT71502L55[2] MIN.	MAX.	UNIT
RAM WRITE CYCLE								
t_{WC}	RAM Write Cycle Time	50	–	65	–	80	–	ns
t_{WAS}	RAM Write Address Set-up Time	0	–	0	–	0	–	ns
t_{WP}	RAM Write Pulse Width	40	–	50	–	60	–	ns
t_{DW}	RAM Write Data Set-up Before End Of Write	20	–	25	–	30	–	ns
t_{WCW}	Chip Select To End Of Write	40	–	50	–	60	–	ns
t_{WDH}	RAM Write Data Hold Time	0	–	0	–	0	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE [1]



NOTE:
1. A write occurs during the overlap of both $\overline{CS}$ and $\overline{WE}$ low.

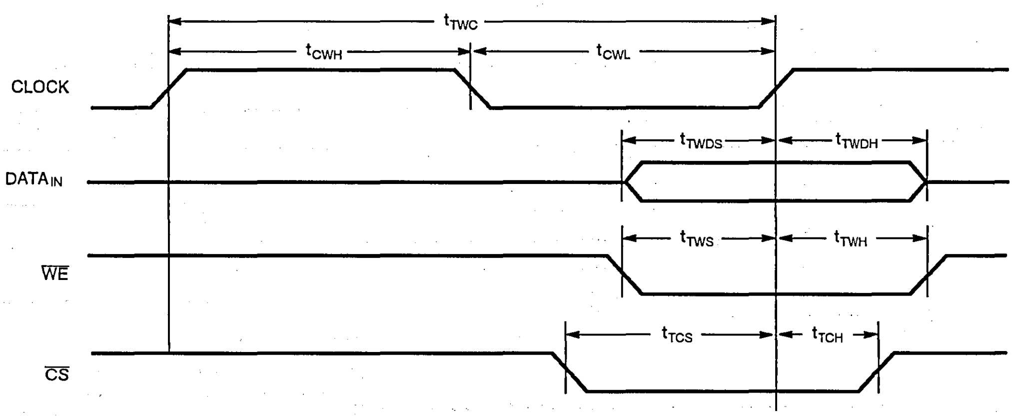
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71502S35[1] IDT71502L35[1] MIN.	MAX.	IDT71502S45 IDT71502L45 MIN.	MAX.	IDT71502S55[2] IDT71502L55[2] MIN.	MAX.	UNIT
TRACE WRITE CYCLE								
t_{TWC}	Trace Write Cycle Time	50	–	60	–	75	–	ns
t_{TWDS}	Trace Write Data Set-up Time	10	–	12	–	15	–	ns
t_{TWDH}	Trace Write Data Hold Time	0	–	0	–	0	–	ns
t_{TWS}	Trace Write Enable Set-up Time	10	–	12	–	15	–	ns
t_{TCS}	Trace Write Chip Select Set-up Time	10	–	12	–	15	–	ns
t_{TWH}	Trace Write Enable Hold Time	0	–	0	–	0	–	ns
t_{TCH}	Trace Write Chip Select Hold Time	0	–	0	–	0	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.

4

TIMING WAVEFORM OF TRACE WRITE CYCLE [1]



NOTE:
1. A write occurs if both $\overline{CS}$ and $\overline{WE}$ are low at the clock low-to-high transition

AC TEST CONDITIONS (Read and Write Cycles)

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

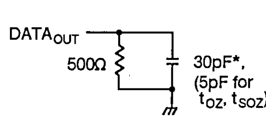


Figure 1. Output Load

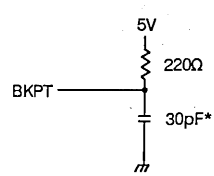


Figure 2. Output Load (for BKPT pin)

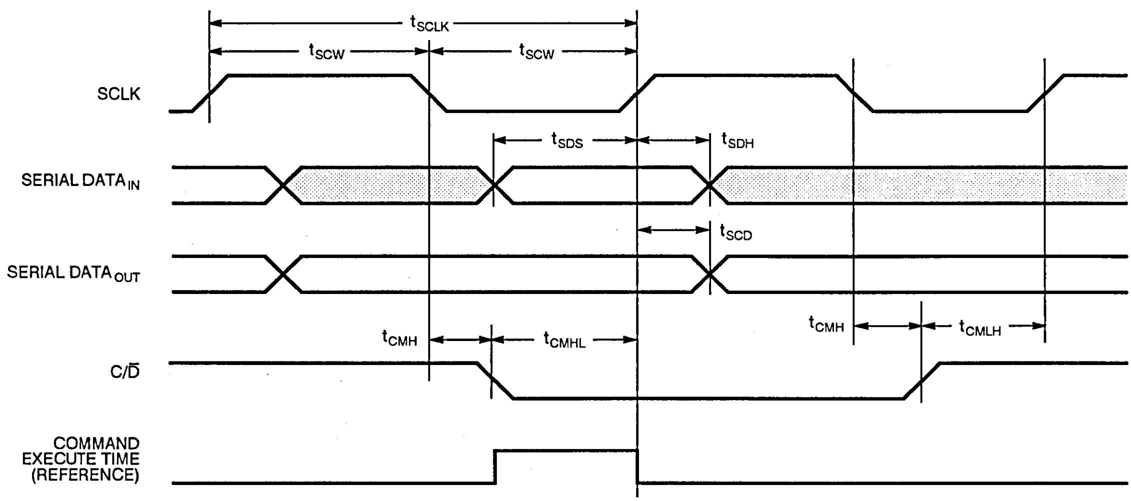
*Includes scope and jig.

SPC AC ELECTRICAL CHARACTERISTICS (1) V_{CC} = 5V ±10%, All Temperature Ranges

SYMBOL	PARAMETER	IDT71502S/L(1) MIN.	MAX.	UNIT
t_{SCLK}	SCLK Period	100	–	ns
t_{SCW}	SCLK Pulse Width	40	–	ns
t_{SDS}	Serial Data Set-up Time	20	–	ns
t_{SDH}	Serial Data Hold Time	0	–	ns
t_{SCD}	Clock to serial Data Output Delay	–	50	ns
t_{SPD}	Serial Data-In-to-Out Delay, Stub Mode	–	40	ns
t_{CMLH}	Command/Data Set-up Time, Low-to-High(2)	20	–	ns
t_{CMHL}	Command Set-up Time, High-to-Low (Execution Time)(2)	40	–	ns
t_{CMH}	Command/Data Hold Time(2)	20	–	ns

NOTES:
1. These specifications apply to all speed grades of the product.
2. C/$\overline{D}$ cannot change while CLOCK is high.

TIMING WAVEFORM OF SPC CHANNEL



AC TEST CONDITIONS (SPC)

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 3

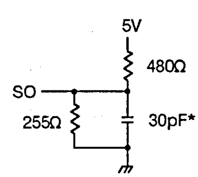
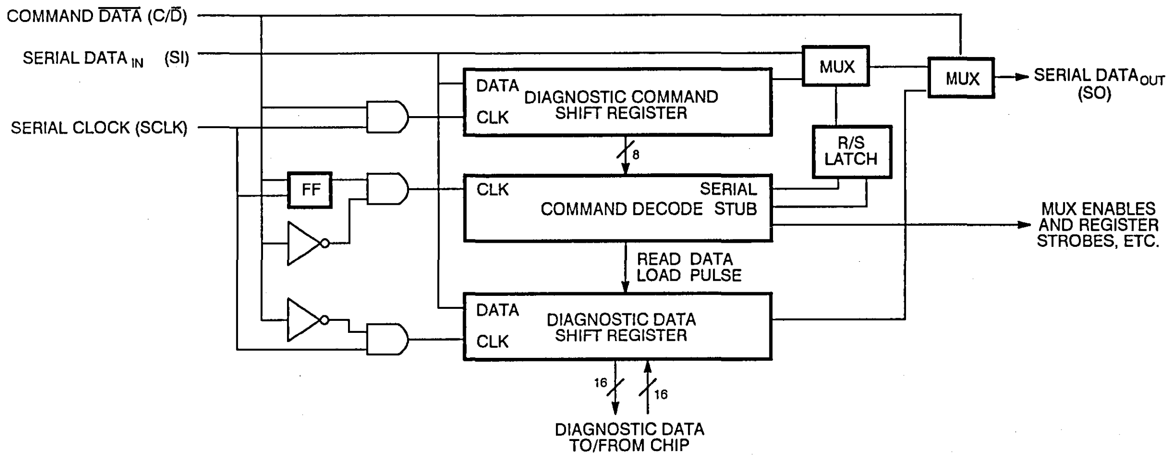


Figure 3. Output Load for Serial Output

*Includes scope and jig.

SPC FUNCTIONAL BLOCK DIAGRAM



4

SPC COMMAND FORMAT

7 — 4	3 — 0
SPC Command Code 4 bits	SPC Register Code 4 bits

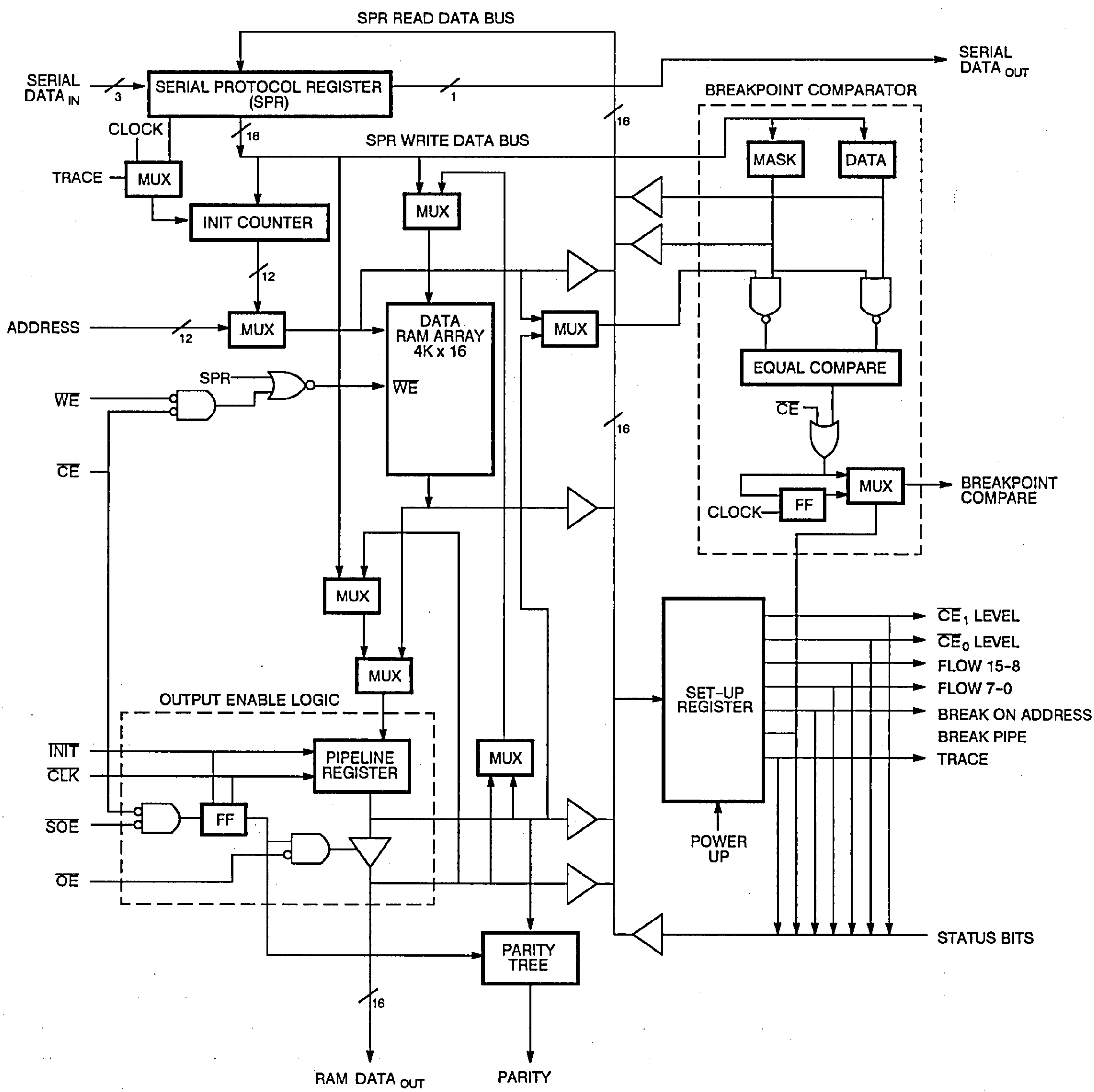
SPC COMMAND CODES

COMMAND CODE	READ/WRITE FUNCTION	ACTION	NOTES
0	Read	Read Register	Uses Register Select Field
1	Write	Write Register	Uses Register Select Field
2	Read	Read Register and Increment Initialize Counter	Serial RAM Read
3	Write	Write and Increment Initialize Counter	Serial RAM Write
4-C	–	Reserved (No-Op)	–
D	Write	Stub Diagnostic	Broadcast Commands
E	Write	Serial Diagnostic	Serial Commands
F	–	No-Op	Guaranteed No-Op

SPC REGISTER CODES

REGISTER CODE	READ/WRITE FUNCTION	REGISTER	NOTES
0	R/W	Initialize Counter	–
1	R/W	RAM Output	–
2	R/W	Pipeline Register	–
3	R/W	Break Mask Register	–
4	R/W	Break Data Register	–
5	R/W	Set-up + Status Register	Break Multiplexer, Trace Mode, etc.
6	Rd Only	Y_{15} - Y_0 (Data Pins)	Data Pins of Chip
7	Rd Only	RAM Address	Address Going into RAM
8-F	–	Reserved (unused)	–

REGISTERED RAM DATA FLOW BLOCK DIAGRAM



SET-UP REGISTER FORMAT

BIT	NAME	TYPE (1)	FUNCTION	POWER-UP VALUE
15	$\overline{CE}$	RO	Chip Enable State: NOR of All Chip Enable Pins	0
14	$\overline{SOE}$ FF	RO	$\overline{SOE}$ FF State: 1 = Output Enabled, 0 = Output Disabled	0
13	$\overline{SOE}$ Pin	RO	$\overline{SOE}$ Pin State: 1 = High, 0 = Low	0
12	$\overline{OE}$ Pin	RO	$\overline{OE}$ Pin State: 1 = High, 0 = Low	0
11	$\overline{WE}$ Pin	RO	$\overline{WE}$ Pin State: 1 = High, 0 = Low	0
10	$\overline{INIT}$ Pin	RO	$\overline{INIT}$ Pin State: 1 = High, 0 = Low	0
9	BP Compare	RO	Breakpoint Comparator Output: 1 = Compare Valid	0
8	BP Pin	RO	BP Pin State: 1 = High, 0 = Low	0
7	$\overline{CS}_1$ Level	R/W	0 = $\overline{CS}_1$ is Low Active; 1 = CS_1 is High Active	0
6	$\overline{CS}_0$ Level	R/W	0 = $\overline{CS}_0$ is Low Active; 1 = CS_0 is High Active	0
5	Non-Reg High	R/W	Set Pipeline Register Bits 15–8 to Flow-Through Mode	0
4	Non-Reg Low	R/W	Set Pipeline Register Bits 7–0 to Flow-Through Mode	0
3	–	–	(Unused)	0
2	BC Address	R/W	0 = Breakpoint on Pipeline Register Output, 1 = Breakpoint on RAM Address Inputs	0
1	BC Pipelined	R/W	Set Breakpoint Output MUX for Pipeline FF Output	0
0	Trace Mode	R/W	Set for Trace Mode: Y_{15-0} to Pipeline Register, Pipeline Register to RAM, Initialize Counter as Address, Write with Clock Pulse	0

NOTE:
1. RO means Read Only. R/W means Read/Write.

4

GENERAL DESCRIPTION

The IDT71502 Registered RAM consists of a 4K x 16-bit RAM plus a 16-bit pipeline register and is designed for microcode writable control store use. A serial shift register system, the Serial Protocol Channel (SPC), is included on-chip for serial load and read-back of the RAM data. A RAM address counter is also provided to speed up RAM load and read-back. The SPC serial shift register is also configured to be used as a diagnostic register. The shift register can read all status conditions on the chip such as the RAM output, pipeline register output, data output pin state and RAM load/read counter value. A breakpoint comparator is included to support the diagnostic function. This breakpoint comparator can be used to detect a particular bit pattern in the RAM address or pipeline register outputs.

The IDT71502 Registered RAM includes features to support control store applications. These include synchronous output enable and an initialize register for selecting the initial value of the pipeline register. A parity output is provided which indicates the parity of the contents of the pipeline register. The parity output can be used to provide parity check control for high-reliability systems.

The IDT71502 Registered RAM can also be used as a trace RAM for recording external data. In this mode, the data I/O pins are inputs and data is clocked into the RAM using the Initialize register as the address counter. The Trace mode, in combination with the breakpoint comparator, allows the IDT71502 Registered RAM to be used as a one-chip logic analyzer.

RAM Operation

After power up, and in its typical operating mode, the IDT71502 Registered RAM is set for pipelined read and direct (non-pipelined) write. Data may be directly written into the RAM by driving the address and data inputs and strobing the Write Enable input. Data is read from the RAM by driving the address lines and clocking the pipeline register.

The RAM may also be read and written by the Serial Protocol Channel (SPC). This is the typical path for loading the RAM after power up.

Serial Protocol Channel

The Serial Protocol Channel (SPC) logic consists of a 16-bit data shift register, an 8-bit command register and clock logic consisting of gates and a flip-flop. A block diagram of the command decode logic is shown for reference. The command decode logic decodes and executes the command in the command shift register using the clock from the clock logic. The command is divided into two four-bit fields. The most significant four bits of the command register define the command to be executed: read, write, etc. The least significant four bits define the register to be read or written. (NOTE: The data to the SPC is shifted in LSB first.)

The SPC is connected to the outside world through four wires. These wires consist of serial data in and out, a shift clock and a command/data line. When the command/data line is high, commands are shifted from the serial data into the command register by the clock. When the command/data line is low, data is shifted into the data shift register by the clock. When the command/data line transitions from high (command) to low (data), a clock pulse is generated internally to the command decode logic. This pulse lasts from the beginning of the high-to-low transition to the next serial clock pulse and is used to execute the command in the command register.

Two of the defined commands are Serial and Stub. These commands control a latch which determines the source of the serial data out in the command mode. The Serial command causes the data output to be taken from the last stage of the command shift register. This is the normal operating mode, where all the shift registers in a system are connected into one long shift register. The SPC logic in the IDT71502 is automatically set to the Serial mode by power up. The Stub command sets the latch and causes the serial output data to be taken from the serial input. In this mode, the serial data is passed directly from one chip to the next so that all command registers have the same data at their serial inputs. This allows a broadcast mode where all command registers in a system can be loaded with the same command at the same time.

SPC commands cause data to be written into registers or read from various points on the chip. The SPC commands for the IDT71502 Registered RAM are shown in the SPC Command Codes and SPC Register Codes tables. The 8-bit command is divided into two 4-bit fields. The four most significant bits define the read or write function and the least significant four bits select a register to be read or written.

RAM Load/Readback Logic

A detailed block diagram of the IDT71502 Registered RAM, showing the various internal registers and the load and readback paths, is shown in the Registered RAM Data Flow Block Diagram. In addition to the logic shown in the Functional Block Diagram on the first page of the data sheet, there is an Initialize Counter for loading and initializing the RAM, Break Data and Mask registers for the Breakpoint Comparator and multiplexers at the input to the Pipeline register for allowing data from the data I/O pins to be clocked into the Pipeline register in the Trace mode before being written into the RAM. The data flow block diagram also shows the various multiplexers for routing data for breakpoint and readback use.

Initialize Counter

The Initialize Counter provides the initial address to the RAM after reset of the part. A pulse applied to the Initialize pin causes the Initialize Counter to be gated to the RAM address and the RAM data to be preset into the pipeline register. This provides an initial value in the pipeline register before the first clock pulse arrives. The Initialize Counter can be reset to zero at power up of the chip and can be loaded with a value other than zero by the SPC. Once loaded with a value by the SPC, this value is used in further chip reset operations.

Set-up Register

The Set-up Register is a 16-bit register used to set the chip operating mode and to read back chip operating status conditions. A command word written into the Set-up Register sets 7 latches which control the chip operating conditions. Reading the Set-up Register provides the current status of these 7 latches and various other signals on the chip. At power up, the 7 latches are cleared to zero and the Initialize counter is cleared to zero. The format of the Set-up Register is shown in the Set-up Register Format table.

The Set-up Register has 7 latches which determine the operating mode of the chip. These are $\overline{CS}_1$, $\overline{CS}_0$, Non-Reg High, Non-Reg Low, BC RAM, Break Pipe and Trace. The $\overline{CS}_1$ and $\overline{CS}_0$ bits determine the polarity of the $\overline{CS}_1$ and $\overline{CS}_0$ chip enables. The Non-Reg High and Low bits set the upper and lower bytes of the Pipeline Register to a flow-through mode, respectively. The BC RAM bit determines the source of the data for breakpoint comparison, either the Pipeline Register or the RAM address. The Break Pipe latch switches the breakpoint pin multiplexer from the comparator to the buffer flip-flop. The trace latch sets the chip into the Trace mode.

Power Up State

Power up is defined as taking V_{CC} from below 1.0 volts to 5.0 volts nominal. This generates power up reset, an internal signal which resets several registers on the chip. After power up, the IDT71502 is in the following state:

- Set-up Register cleared to zero
- Initialize Counter cleared to zero
- Breakpoint Mask Register cleared to equal (Breakpoint output high)
- $\overline{SOE}$ Flip-Flop cleared to outputs off

Note that taking V_{CC} from 5.0 volts to 2.0 volts and back to 5.0 volts will not cause power up reset.

Set-up Register: Programmable Chip Enable

The chip enable function is programmable by bits in the Set-up Register. The logic for this is shown in Figure 1. The bits in the Set-up Register define the active state of each chip enable: high or low. This allows up to four RAMs to be cascaded in depth with no external decoders required (16K x 16 bits of RAM).

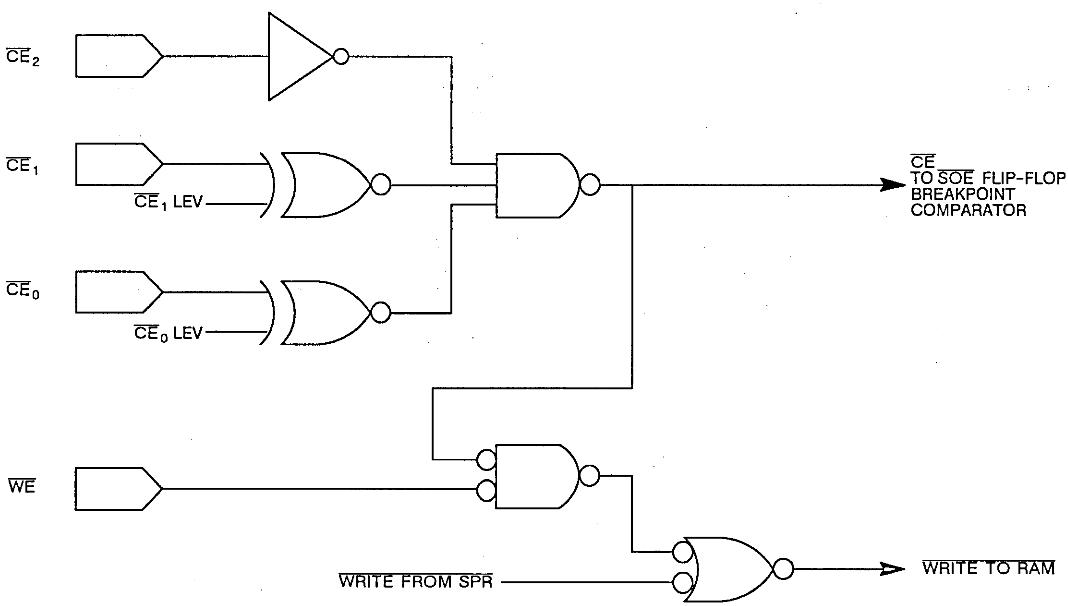


Figure 1. Chip Enable Logic Block Diagram

Set-up Register: Non-Registered Outputs

Two bits of the Set-up Register, Non-Reg Hi and Non-Reg Lo, can be set to cause the Pipeline Register bits 15-9 and 7-0, respectively, to be set to the flow-through mode. In the flow-through mode, both latches of the register are open and the register acts like a simple buffer with its output following its input. This allows the user to have some non-registered bits in microcode applications. The output circuit consisting of the Pipeline Register, the Synchronous Output Enable ($\overline{SOE}$), and the Output Enable ($\overline{OE}$), has some special logic to support this mode, as shown in Figure 2. Also, activating the Initialize pin causes the Pipeline Register to be put in the flow-through mode. Figure 2 shows the Pipeline Register as two latches operated in the MASTER/SLAVE configuration. The clock input will cause the latch pair to work as a register. If the Initialize pin is activated, both registers will be placed in the flow-through mode by the OR gates. Also, if either Non-Reg bit is set, its corresponding 8-bit portion of the register will be placed in the flow-through mode.

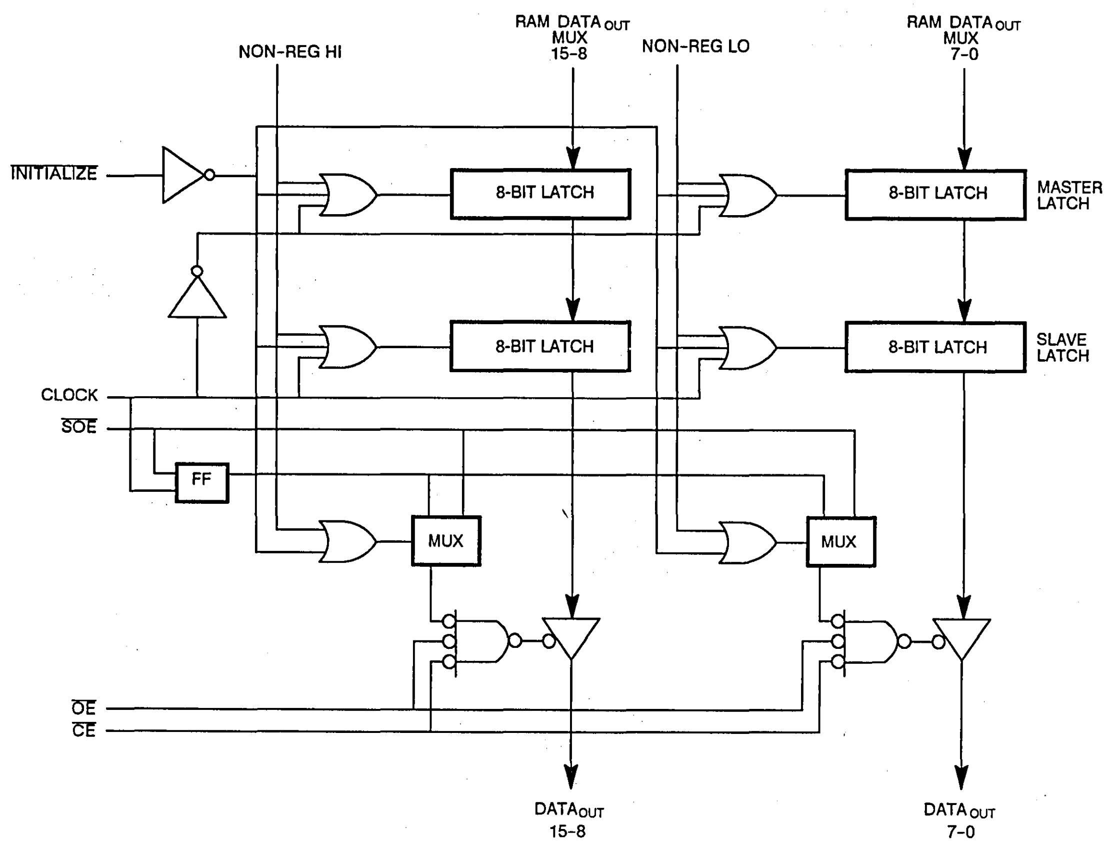
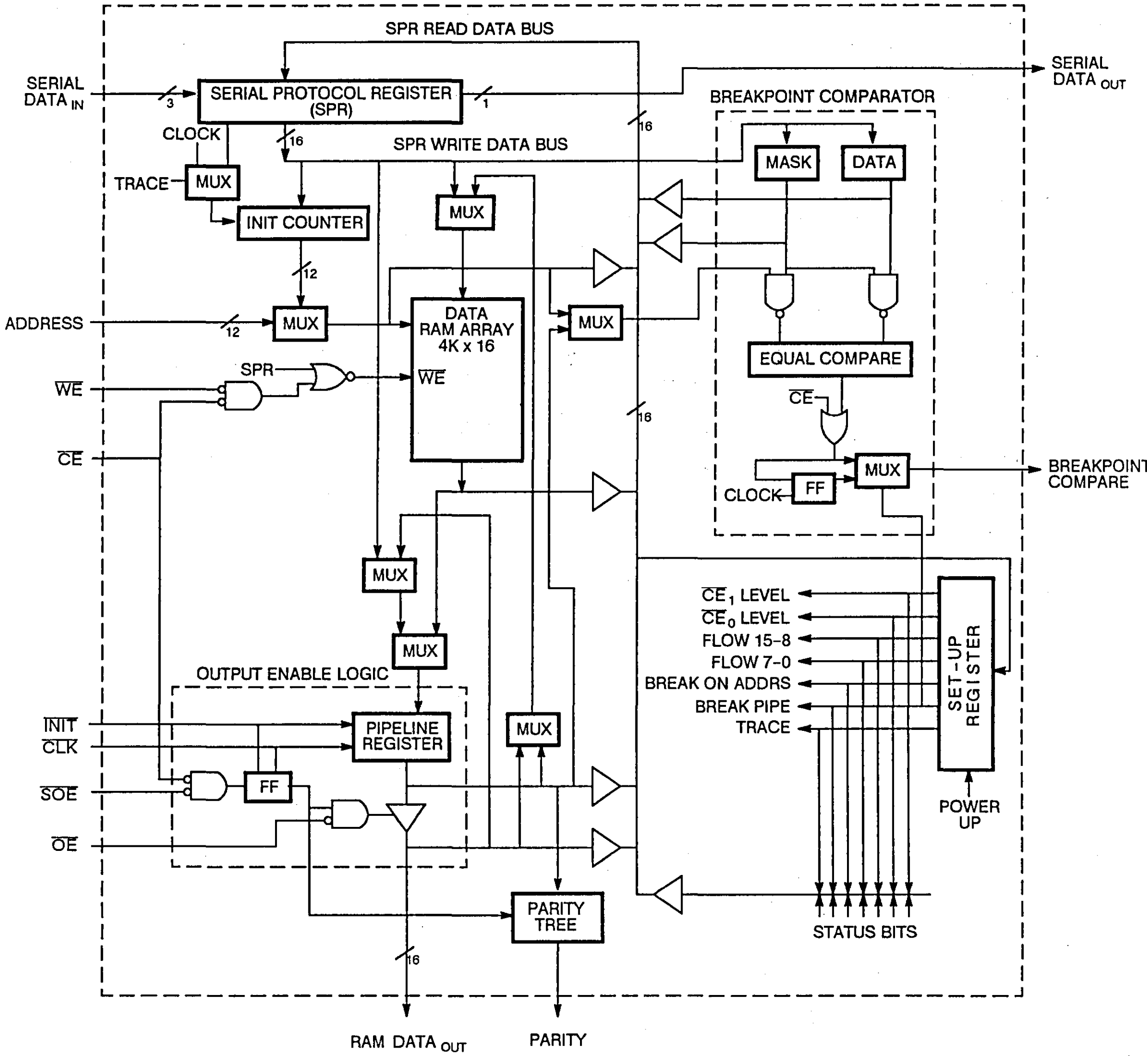


Figure 2. Output Logic Block Diagram

When in the flow-through mode, the output enable flip-flop for that half must also be in the flow-through mode for external chip expansion to work properly. A non-registered RAM bit must be enabled by a non-registered output enable, while a registered bit must be enabled by a synchronous output enable. This is done by using the non-registered bit to control a multiplexer which selects between the $\overline{SOE}$ flip-flop input and output as the source of the output enable.

REGISTERED RAM DATA FLOW BLOCK DIAGRAM



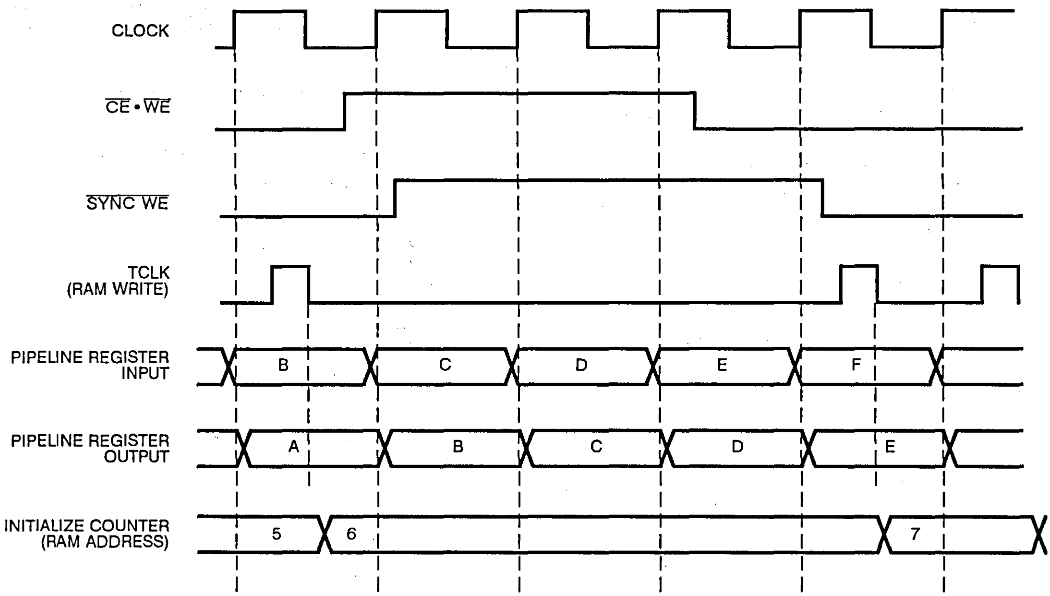


Figure 4. Trace Mode Sequence Timing Diagram

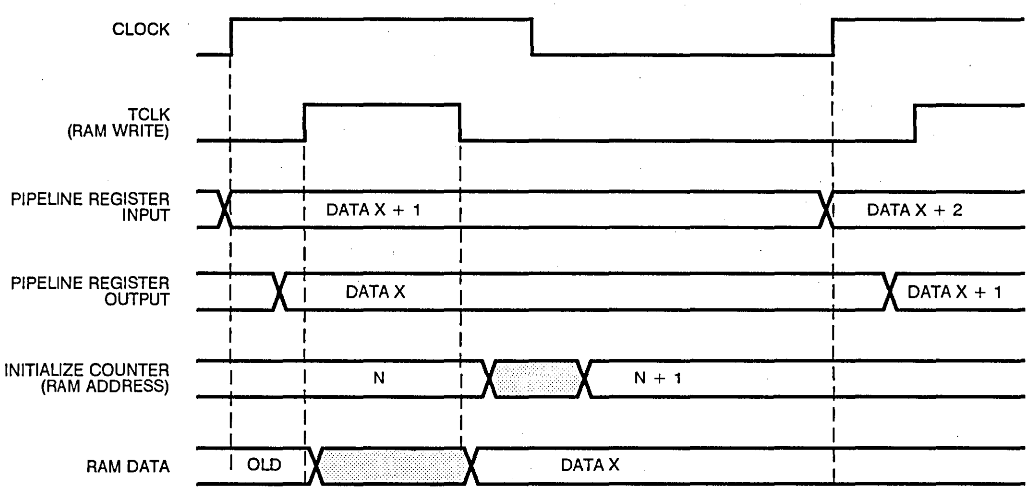


Figure 5. Trace Mode Clock Timing Diagram

Parity Output

The Parity Output pin is generated from a 16-bit parity tree, as shown in the Parity Tree Logic Block Diagram (Figure 6). Even parity is used. Parity is generated on the contents of the Pipeline Register. The parity output driver is three-state and is enabled by the $\overline{SOE}$ Flip-Flop to allow depth expansion of the parity output.

The Parity Output always reflects the parity of the registered value. Additional flip-flops and multiplexers are included in the parity tree to cover the case of non-registered outputs. If one or both bytes of the Pipeline Register are set to the Non-Registered mode, a flip-flop pipeline delay is added to the corresponding byte parity chain to make the result of that byte parity calculation the same as if the Pipeline Register was not in the Non-Pipelined mode.

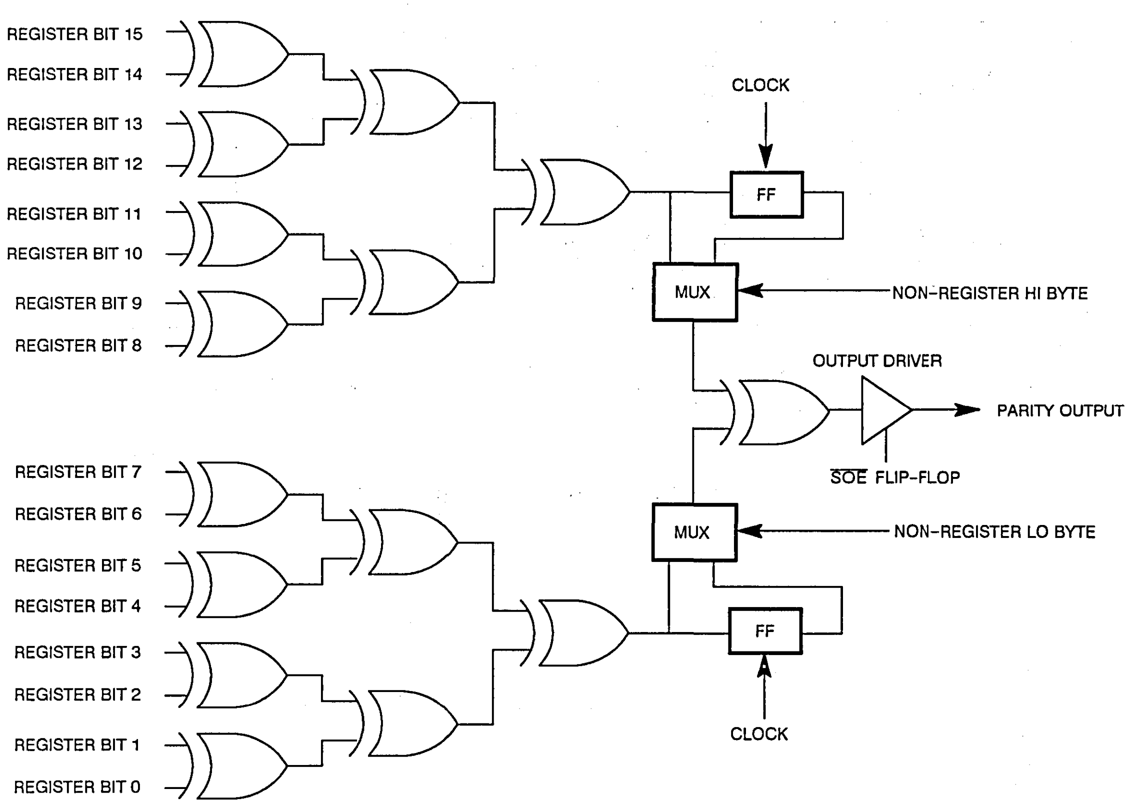


Figure 6. Parity Tree Logic Block Diagram

REGISTERED RAM APPLICATIONS

Using the Registered RAM in Writable Control Stores

The IDT71502 Registered RAM is designed expressly for efficient use in writable control stores. A simplified block diagram of a 16-bit microprogram-controlled system using the IDT71502 is shown in Writable Control Store Using Registered RAM (Figure 7). The system shown uses four IDT71502 Registered RAM chips to provide 4K x 64 bits of microcode writable control store.

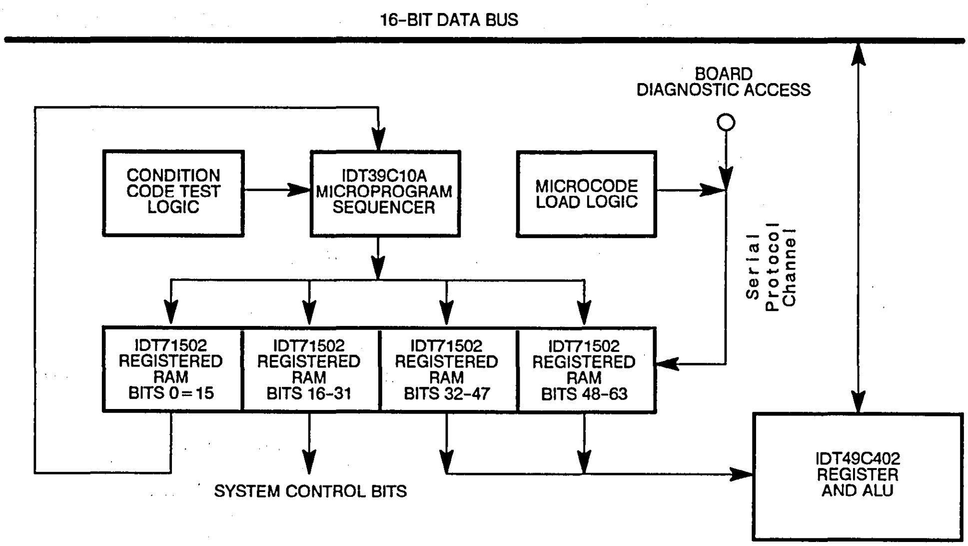


Figure 7. Writable Control Store Using Registered RAM

Using the Parity Output

The parity output can be used in conjunction with an additional IDT71502 Registered RAM to provide parity checking for control stores. This is shown in the Parity Check in a Writable Control Store System (Figure 8) block diagram. The parity output driver is gated by the $\overline{SOE}$ Flip-Flop. This allows simple depth expansion of the parity function by paralleling the parity outputs in the same manner as the data outputs, as shown in the Parity Check in a Depth Expanded Writable Control Store System (Figure 9) block diagram.

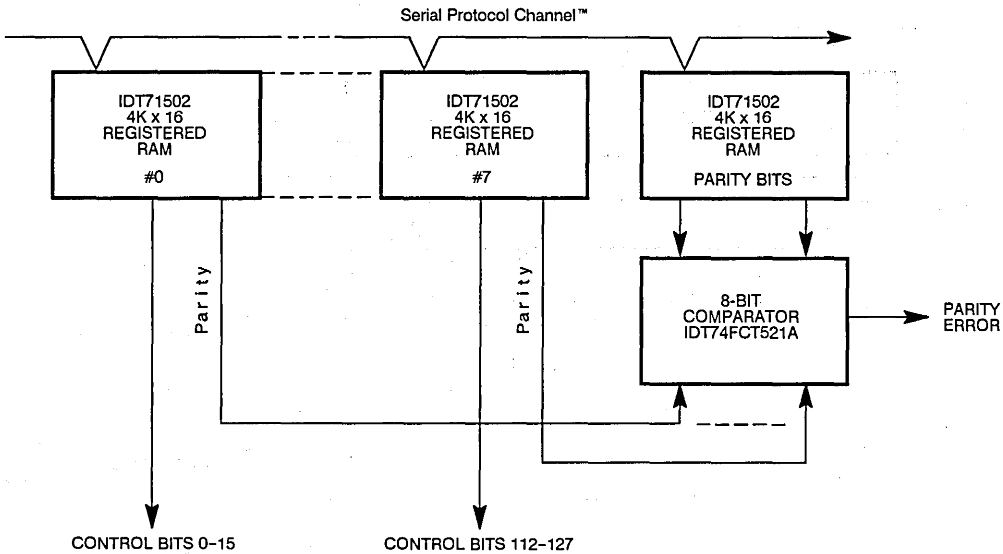


Figure 8. Parity Check in a Writable Control Store System

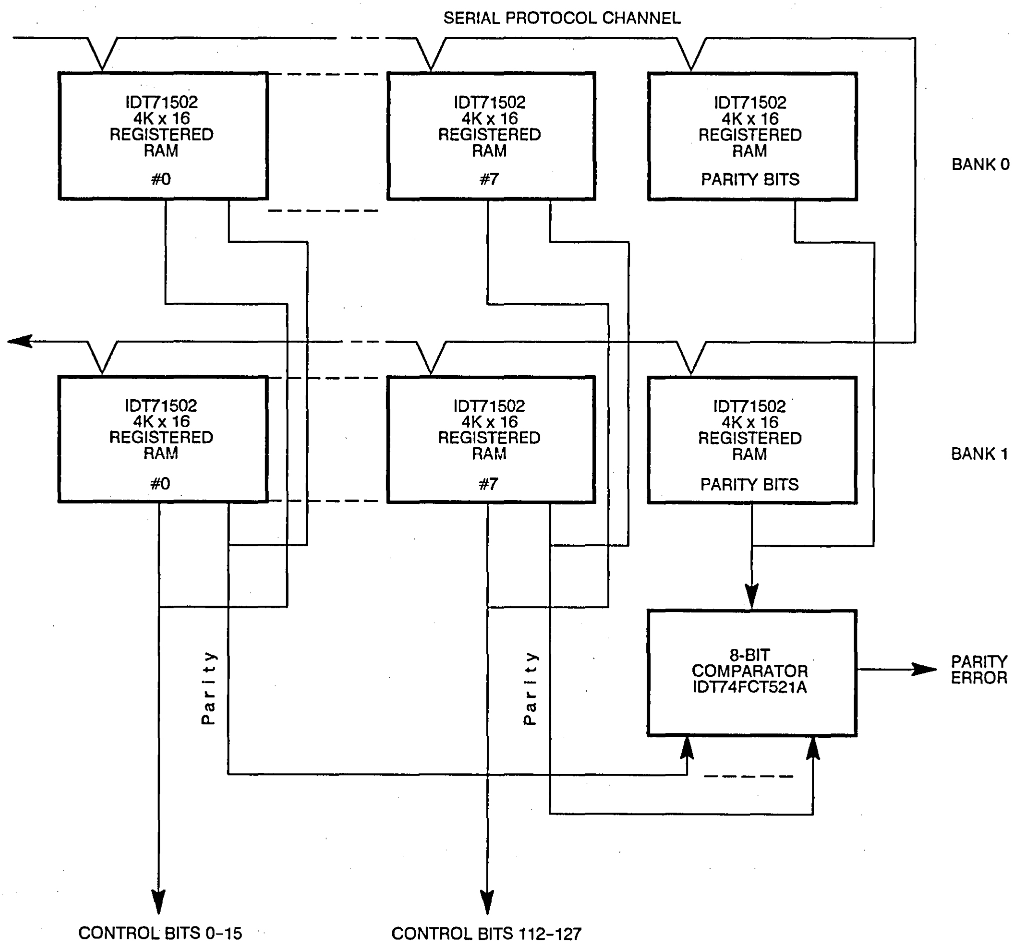


Figure 9. Parity Check in a Depth Expanded Writable Control Store System

Using Trace Mode as a Logic Analyzer

The Trace mode allows the IDT71502 to be used as an on-board logic analyzer for system diagnostics. It is particularly powerful when used in conjunction with the Breakpoint function. In the Trace mode, data is recorded in sequential locations in the RAM as controlled by the Trace Counter. Since the incoming data is clocked into the pipeline register, the set-up and hold times are short and compatible with capturing changing bus data, for example. A block diagram of a system with an IDT71502 used in the Trace mode is shown in Diagnostic Bus Monitoring Using Trace Mode (Figure 10).

The Breakpoint outputs from the IDT71502 devices in a system can be used to control the Trace mode writing. The Breakpoint outputs are open drain types which provide a wire-AND function when connected together to a single pull-up resistor. By tying the Breakpoint outputs for the writable control store RAMs and the trace RAM, a breakpoint comparison can be made over the full microcode word plus the data bus contents. This comparison can be used to enable the trace write so that only data which occurred at the Breakpoint times is recorded. This allows recording the data that was on the bus during each instance of an I/O write, for example.

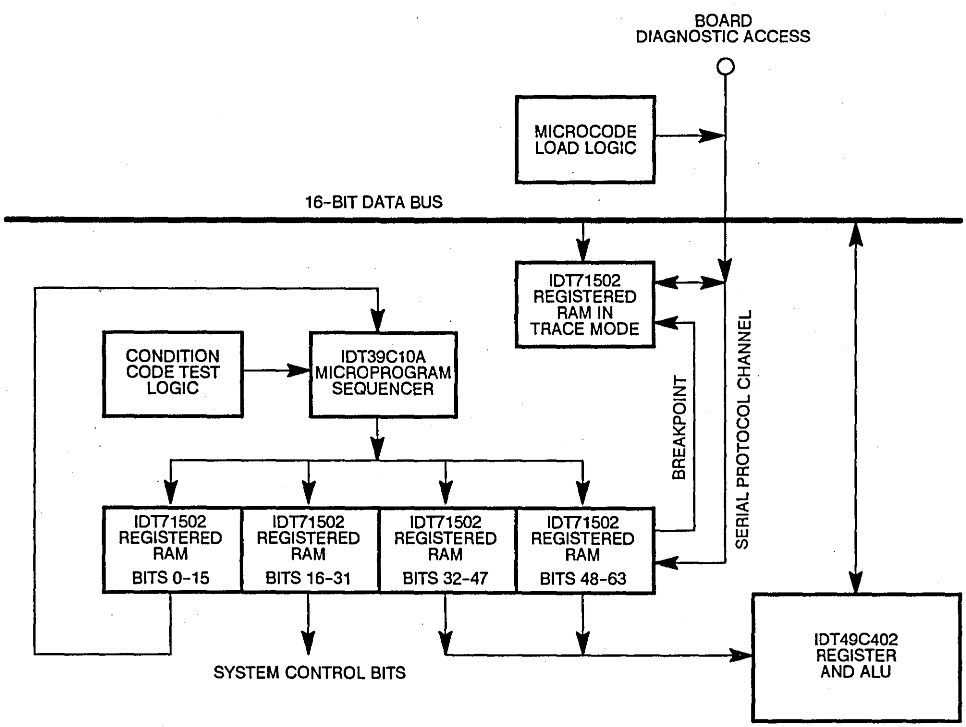


Figure 10. Diagnostic Bus Monitoring Using Trace Mode

Serial Loading of the IDT71502 Using the SPC

In order to use the IDT71502 in writable control store applications, it must be loaded with the microprogram before use. This is done using the Serial Protocol Channel (SPC). Loading the RAM over the SPC can be done in several ways. The microcode can be loaded from a central microprocessor, which can perform both microcode load and system diagnostics at power up, or it can be loaded using dedicated load logic.

An example of a design of this dedicated load logic is shown in the Microcode Load Logic Example (Figure 11). The purpose of this example is to show how one goes about designing this logic. This example shows an approach which loads the RAMs with data from a single EPROM. The load logic gets the SPC command and data information from the EPROM. It is controlled by single byte instructions from the same EPROM. The format of these instructions is shown in Microcode Load Logic Instruction Formats (Figure 12), and a map of the typical contents of the EPROM is shown in Microcode Load EPROM Memory Map (Figure 13).

The load logic consists of a 16-bit address counter, an 8-bit shift register, a 4-bit byte counter and a PAL containing a 2-bit instruction register. The logic in the PAL interprets the 2-bit load instructions to cause bytes of command or data information to be loaded into the IDT74FCT299 shift register and shifted to the SPC. The two IDT74FCT161 counters are used to count the bytes being sent and the 8 bits in each byte.

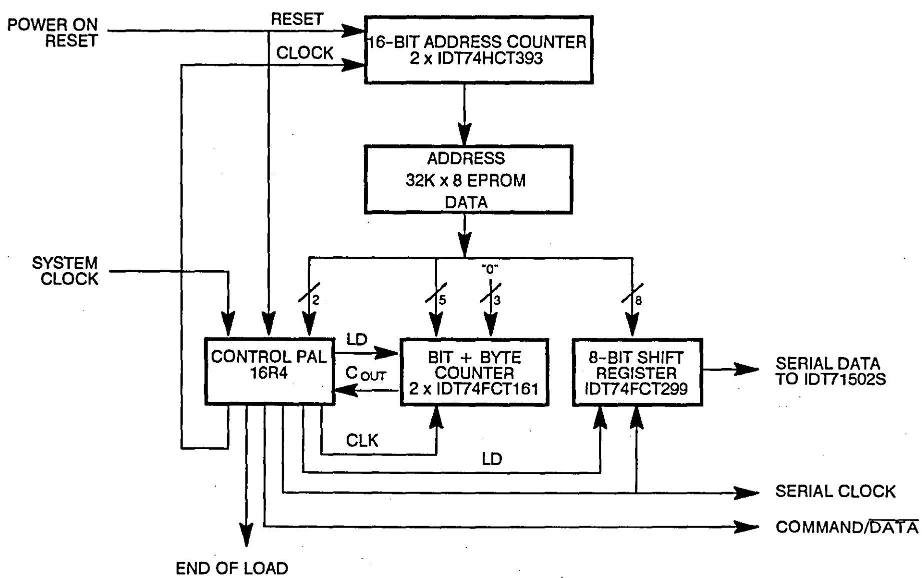


Figure 11. Microcode Load Logic Example

0	0	BYTE COUNT	LOAD COMMAND
0	1	BYTE COUNT	LOAD COMMAND USING SLOW CLOCK
1	0	BYTE COUNT	LOAD DATA
1	1	BYTE COUNT	STOP, END OF LOOP

Figure 12. Microcode Load Logic Instruction Formats

EPROM ADDRESS	EPROM Data			
0000	0	0	4	LOAD 4 COMMAND BYTES
0001	COMMAND BYTE 0			
0002	COMMAND BYTE 1			
0003	COMMAND BYTE 2			
0004	COMMAND BYTE 3			
0005	1	0	8	LOAD 8 DATA BYTES
0006	DATA BYTE 0			
0007	DATA BYTE 1			
	⋮			
000B	DATA BYTE 7			
000C	0	0	4	LOAD 4 COMMAND BYTES
000D	COMMAND BYTE 0			
	ETC.			
XXXX	1	1	0	STOP, END OF LOOP

Figure 13. Microcode Load EPROM Memory Map

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	C	Sidebraze DIP
Speed	35	Commercial only — Speed in Nanoseconds
	45	
	55	Military Only — Speed in Nanoseconds
Power	L	Low Power
	S	Standard Power
Device Type	71502	64K (4K x 16-Bit) Registered RAM

Integrated Device Technology, Inc.

16K x 32 WRITABLE CONTROL STORE STATIC RAM MODULE

ADVANCE INFORMATION
IDT7M6032

FEATURES:

- 16K x 32 high-performance Writable Control Store (WCS)
- Serial Protocol Channel (SPC™) – reading, writing and interrogation
- 4 byte/wide output enables
- Separate chip select, write enable and output enable memory controls
- High fanout pipeline register
- Fully width expandable
- Designed for high-speed writable control store applications
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Compact 64-pin ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Military modules available with semiconductor components manufactured in compliance to MIL-STD-883, Class B

DESCRIPTION:

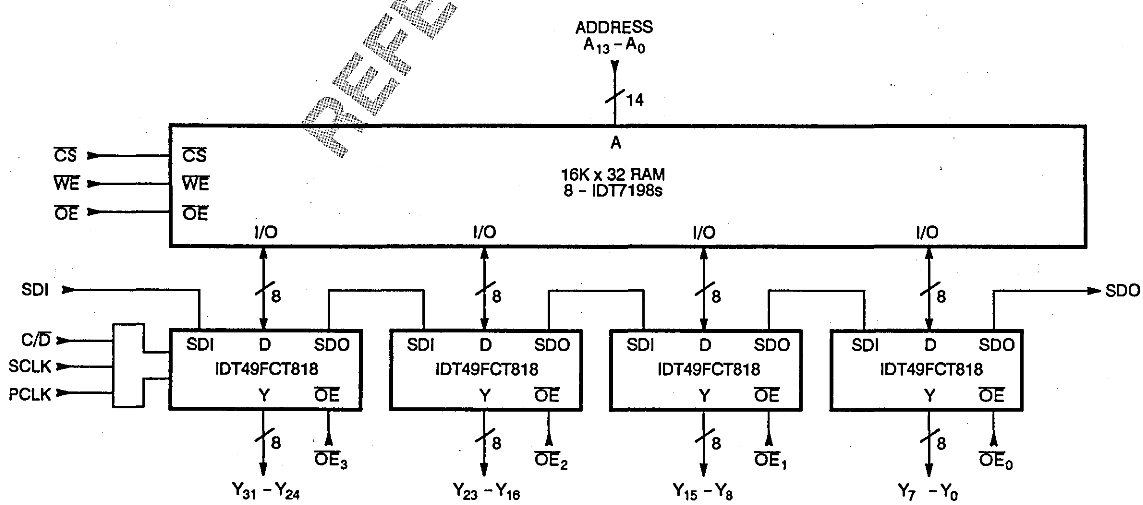
The IDT7M6032 is a 16K x 32-bit Writable Control Store (WCS) RAM and pipeline register. It features eight IDT7198 16K x 4 high-performance static RAMs and four IDT49FCT818 Serial Protocol Channel (SPC) registers. These devices are arranged to form the 16K x 32 Writable Control Store RAM with Serial Protocol Channel for loading of the memory. The address lines, chip select, write enable and output enable of the RAMs are all bused together to form one large 16K x 32 memory. Each eight outputs of the RAM are connected to the D inputs of an IDT49FCT818 in the normal fashion. The device has the serial data-in and serial data-output bits connected to form a 32-bit Serial Protocol Channel register. The module features four separate output enables, one for each of the IDT49FCT818 registers. Thus, the Y outputs from the IDT49FCT818 registers may be enabled or put into the high-impedance state on individual 8-bit boundaries. The Command/Data (C/$\overline{D}$), Serial Shift Clock (SCLK) and Parallel Clock (PCLK) are all bus organized across the four IDT49FCT818 registers. The thirty-two register output bits, eight from each device, are separately brought out to form a 32-bit wide pipeline register on the Writable Control Store.

In normal operation, data from the 32-bit wide memory is loaded into the IDT49FCT818 registers on the low-to-high transition of PCLK. Reading and writing of the memory by means of the Serial Protocol Channel is performed in the normal fashion using the IDT49FCT818. That is, the data to be loaded can be shifted in the serial data input by using the SCLK and a load command executed by shifting the proper command word in the serial data input when the C/$\overline{D}$ line is in the command mode. This command will then be executed by manipulating the C/$\overline{D}$ line and SCLK line in the desired fashion. Data is then written into the RAM by bringing the write enable line on the RAM memory from the high state to the low state and back to the high state.

The IDT7M6032 is offered in a compact 64-pin 600 mil wide ceramic dual in-line module. It is constructed using ceramic LCC components on a multilayer co-fired ceramic substrate and occupies less than 2 square inches of board space.

The semiconductor components used on all IDT military modules are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS and SPC are trademarks of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

8K x 112 WRITABLE CONTROL STORE STATIC RAM MODULE

ADVANCE INFORMATION
IDT7MB6042

FEATURES:

- 8K x 112 high-performance Writable Control Store (WCS)
- Serial Protocol Channel (SPC™)—reading, writing and interrogation
- High fanout pipeline register
- Width expandable
- Designed for high-speed writable control store applications
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Compact quad in-line module
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

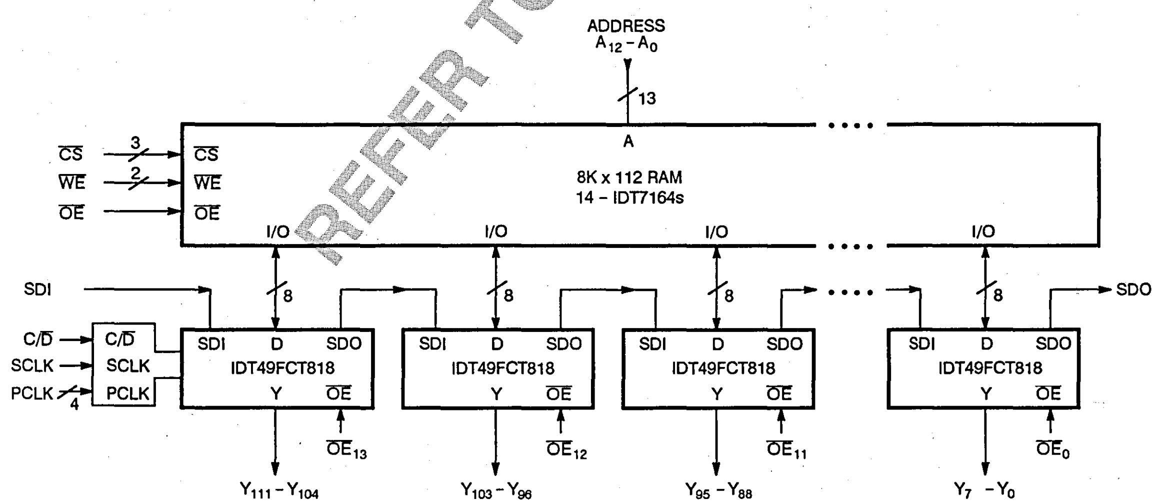
DESCRIPTION:

The IDT7MB6042 is an 8K x 112-bit Writable Control Store (WCS) RAM and pipeline register. It features fourteen 8K x 8 IDT7164 high-performance static RAMs and fourteen IDT49FCT818 Serial Protocol Channel (SPC) registers. These devices are arranged to form the 8K x 112 Writable Control Store RAM with Serial Protocol Channel for loading of the memory. Each eight outputs of the RAM are connected to the D inputs of an IDT49FCT818 in the normal fashion. The device has the serial data-in and serial data-output bits connected to form a 112-bit Serial Protocol Channel register. The command/data ($C/\overline{D}$) and Serial Shift Clock (SCLK) are all bus organized across the fourteen IDT49FCT818 registers. The 112 register output bits, 8 from each device, are separately brought out to form a 112-bit wide pipeline register on the Writable Control Store.

In normal operation, data from the 112-bit wide memory is loaded into the IDT49FCT818 registers on the low-to-high transition of PCLK. Reading and writing of the memory by means of the Serial Protocol Channel are performed using the protocol of the IDT49FCT818. (For details of this operation, please refer to the IDT49FCT818 data sheet.) The data to be loaded can be shifted in the serial data input by using the SCLK and a load command executed by shifting the proper command word in the serial data input when the $C/\overline{D}$ line is in the command mode. This command will then be executed by manipulating the $C/\overline{D}$ line and SCLK line in the desired fashion. Data is then written into the RAM by bringing the write enable line on the RAM memory from the high state to the low state and back to the high state.

The IDT7MB6042 is offered as a compact, cost-effective plastic quad in-line module and occupies less than 9 square inches of board space.

FUNCTIONAL BLOCK DIAGRAM



DSC-7021/-

5

DUAL-PORT RAMS

Integrated Device Technology has emerged as the leading Dual-Port RAM supplier by combining advanced CEMOS technology with innovative circuit design. With system performance advantages as a goal, we have brought system design expertise together with circuit and technology expertise in defining dual-port RAM products. Our dual-port memories are now industry standards.

The synergistic relationship between advanced process technology, system expertise and unique design capability add value beyond that normally achieved. As an example, our dual-port memories provide arbitration along with a completely tested solution to the metastability problem. Various arbitration techniques are available to the designer to prevent contention and system wait states. On-chip hardware arbitration, "semaphore" token passing or software arbitration allow the most efficient memory to be selected for each application. At IDT, innovation counts only when it provides system advantages to the user.

Both commercial and military versions of all IDT memories are available. Our military devices are manufactured and processed strictly in conformance with all the administrative processing and performance requirements of MIL-STD-883. Because we anticipated increased military radiation resistance requirements, all devices are also offered with special radiation resistant processing and guarantees. As the leading supplier of military specialty RAMs, IDT provides performance and quality levels second to none.

Our commercial dual-port memories, in fact, share most processing steps with military devices.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAMS 8K (1K x 8-BIT)

IDT7130SA/LA
IDT7140SA/LA

FEATURES:

- High-speed access
  - Military: 45/55/70/90/100/120ns (max.)
  - Commercial: 35/45/55/70/90/100ns (max.)
- Low-power operation
  - IDT7130/40SA
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - IDT7130/40LA
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- MASTER IDT7130 easily expands data bus width to 16-or-more-bits using SLAVE IDT7140
- On-chip port arbitration logic (IDT7130 only)
- $\overline{\text{BUSY}}$ output flag on IDT7130; $\overline{\text{BUSY}}$ input on IDT7140
- $\overline{\text{INT}}$ flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V±10% power supply
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86875 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT7130/IDT7140 are high-speed 1K x 8 dual-port static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7140 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{\text{CE}}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

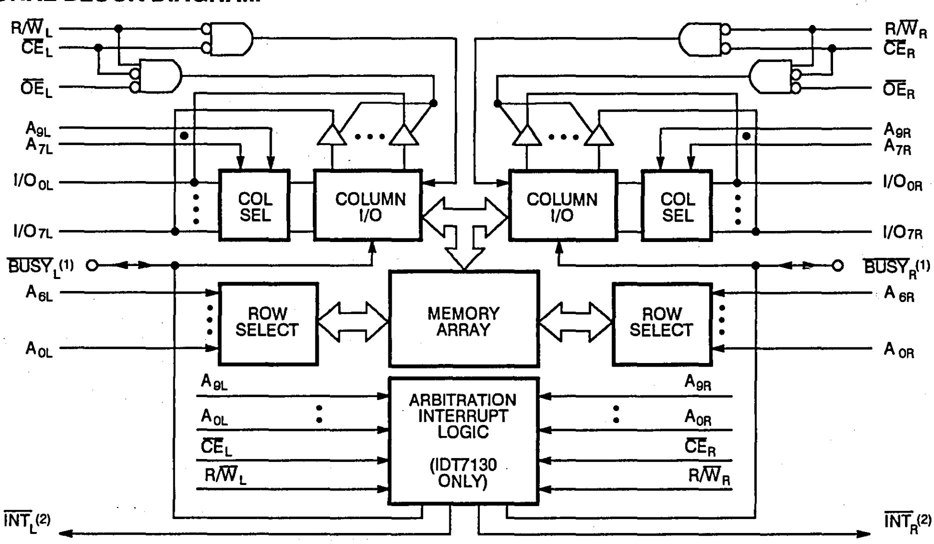
Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 35ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µW from a 2V battery.

The IDT7130/7140 devices are packaged in 48-pin sidebraze or plastic DIPs, 48- or 52-pin LCCs, 52-pin PLCCs, and 48-lead flatpacks.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

5

FUNCTIONAL BLOCK DIAGRAM

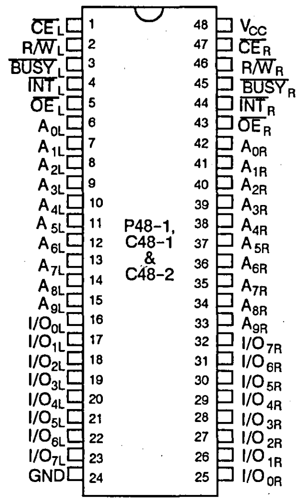


NOTES:

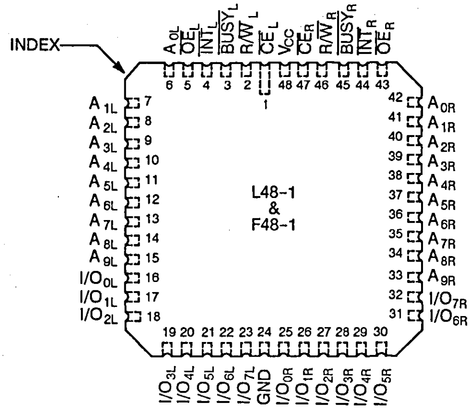
1. IDT7130 (MASTER): $\overline{\text{BUSY}}$ is open drain output and requires pullup resistor.
   IDT7140 (SLAVE): $\overline{\text{BUSY}}$ is input.
2. Open drain output: requires pullup resistor.

CEMOS is a trademark of Integrated Device Technology, Inc.

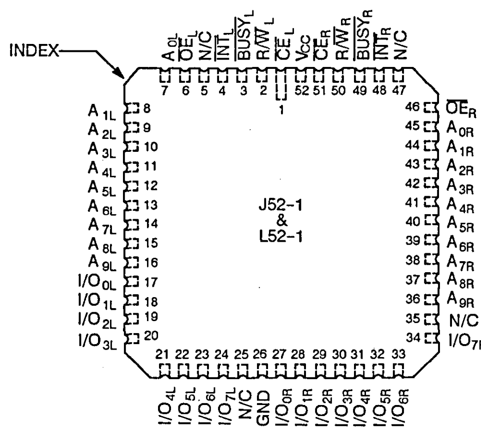
PIN CONFIGURATIONS



DIP
TOP VIEW



48-PIN LCC/FLATPACK
TOP VIEW



52-PIN LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7130SA IDT7140SA MIN.	MAX.	IDT7130LA IDT7140LA MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage (I/O_0- I/O_7)	I_{OL} = 4.0mA	–	0.4	–	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$, $\overline{INT}$)	I_{OL} = 16mA	–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (1) (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		7130 x 35(2) 7140 x 35(2) TYP.	MAX.	7130 x 45 7140 x 45 TYP.	MAX.	7130 x 55 7140 x 55 TYP.	MAX.	7130 x 70 7140 x 70 TYP.	MAX.	7130 x 90 7140 x 90 TYP.	MAX.	7130 x 100/120(3) 7140 x 100/120(3) TYP.	MAX.	UNIT
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}(4)	MIL.	SA	–	–	75	230	65	230	65	225	65	200	65	190	mA
				LA	–	–	75	185	65	185	65	180	65	160	65	155	
			COM'L.	SA	75	195	75	190	65	180	65	180	65	180	65	180	
				LA	75	155	75	145	65	140	65	135	65	130	65	130	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}(4)	MIL.	SA	–	–	25	65	25	65	25	65	25	65	25	65	mA
				LA	–	–	25	55	25	55	25	55	25	45	25	45	
			COM'L.	SA	25	65	25	65	25	65	25	60	25	55	25	55	
				LA	25	45	25	45	25	45	25	40	25	35	25	35	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}(4)	MIL.	SA	–	–	40	135	40	135	40	135	40	125	40	125	mA
				LA	–	–	40	110	40	110	40	110	40	100	40	100	
			COM'L.	SA	40	130	40	120	40	115	40	110	40	110	40	110	
				LA	40	95	40	85	40	85	40	85	40	75	40	75	
I_{SB3}	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0(4)	MIL.	SA	–	–	1.0	30	1.0	30	1.0	30	1.0	30	1.0	30	mA
				LA	–	–	0.2	10	0.2	10	0.2	10	0.2	10	0.2	10	
			COM'L.	SA	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
				LA	0.2	4	0.2	4	0.2	4	0.2	4	0.2	4	0.2	4.0	
I_{SB4}	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$-0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}(4)	MIL.	SA	–	–	40	125	40	120	40	115	40	110	40	110	mA
				LA	–	–	35	95	35	90	35	85	35	80	35	80	
			COM'L.	SA	40	115	40	105	40	100	40	100	40	95	40	95	
				LA	35	90	35	80	35	75	35	75	35	70	35	70	

NOTES:

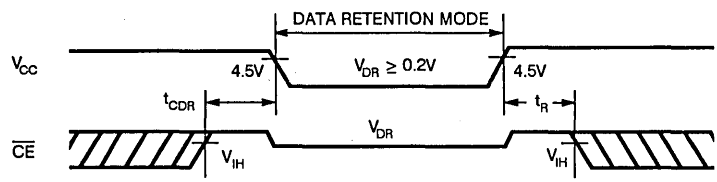
1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby, I_{SB3}.

DATA RETENTION CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7130LA/IDT7140LA MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention			2.0	–	–	V
I_{CCDR}	Data Retention Current	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V	MIL.	–	100	4000	µA
			COM'L.	–	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V		0	–	–	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–	–	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

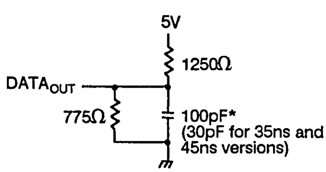


Figure 1. Output Load

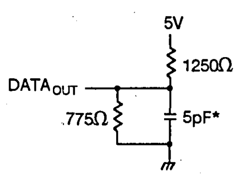


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

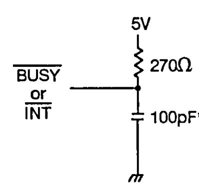


Figure 3. $\overline{BUSY}$ and $\overline{INT}$ Output Load

* Including scope and jig.

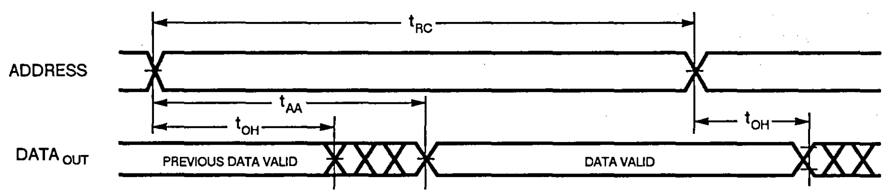
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	7130 x 35(2) 7140 x 35(2) MIN.	MAX.	7130 x 45 7140 x 45 MIN.	MAX.	7130 x 55 7140 x 55 MIN.	MAX.	7130 x 70 7140 x 70 MIN.	MAX.	7130 x 90 7140 x 90 MIN.	MAX.	7130 x 100/120(3) 7140 x 100/120(3) MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	35	–	45	–	55	–	70	–	90	–	100/120	–	ns
t_{AA}	Address Access Time	–	35	–	45	–	55	–	70	–	90	–	100/120	ns
t_{ACE}	Chip Enable Access Time	–	35	–	45	–	55	–	70	–	90	–	100/120	ns
t_{AOE}	Output Enable Access Time	–	25	–	30	–	35	–	40	–	40	–	40/60	ns
t_{OH}	Output Hold From Address Change	0	–	0	–	0	–	0	–	10	–	10	–	ns
t_{LZ}	Output Low Z Time (1, 4)	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Output High Z Time (1, 4)	–	15	–	20	–	30	–	35	–	40	–	40	ns
t_{PU}	Chip Enable to Power Up Time (4)	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time (4)	–	50	–	50	–	50	–	50	–	50	–	50	ns

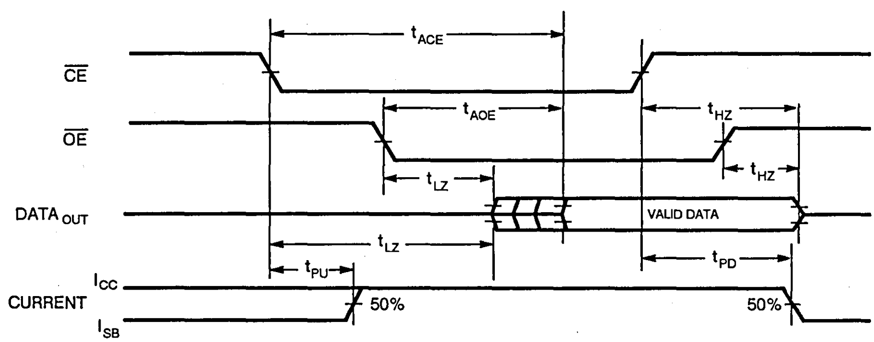
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.

5

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)



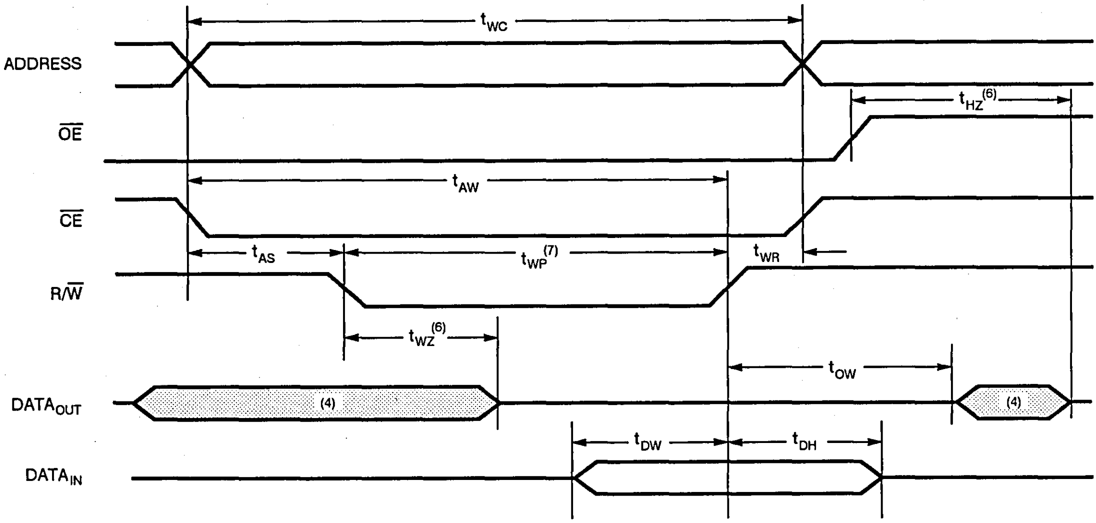
NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (6)

SYMBOL	PARAMETER	7130 x 35(2) 7140 x 35(2) MIN.	MAX.	7130 x 45 7140 x 45 MIN.	MAX.	7130 x 55 7140 x 55 MIN.	MAX.	7130 x 70 7140 x 70 MIN.	MAX.	7130 x 90 7140 x 90 MIN.	MAX.	7130 x 100/120(3) 7140 x 100/120(3) MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time (5)	35	–	45	–	55	–	70	–	90	–	100/120	–	ns
t_{EW}	Chip Enable to End of Write	30	–	35	–	40	–	50	–	85	–	90/100	–	ns
t_{AW}	Address Valid to End of Write	30	–	35	–	40	–	50	–	85	–	90/100	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	30	–	35	–	40	–	50	–	55	–	55/65	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	20	–	20	–	20	–	30	–	40	–	40	–	ns
t_{HZ}	Output High Z Time (1,4)	–	15	–	20	–	30	–	35	–	40	–	40	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enabled to Output in High Z (1,4)	–	15	–	20	–	30	–	35	–	40	–	40/50	ns
t_{OW}	Output Active From End of Write (1,4)	0	–	0	–	0	–	0	–	0	–	0	–	ns

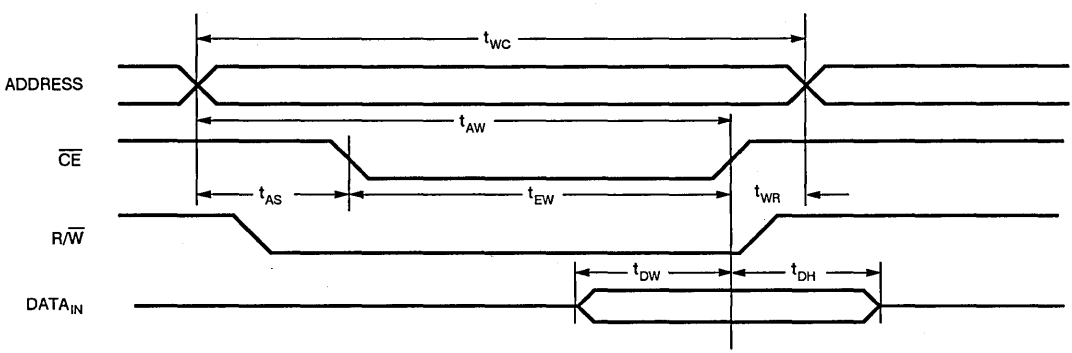
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$.
6. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING) (1, 2, 3, 7)



5

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:

1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $t_{WZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

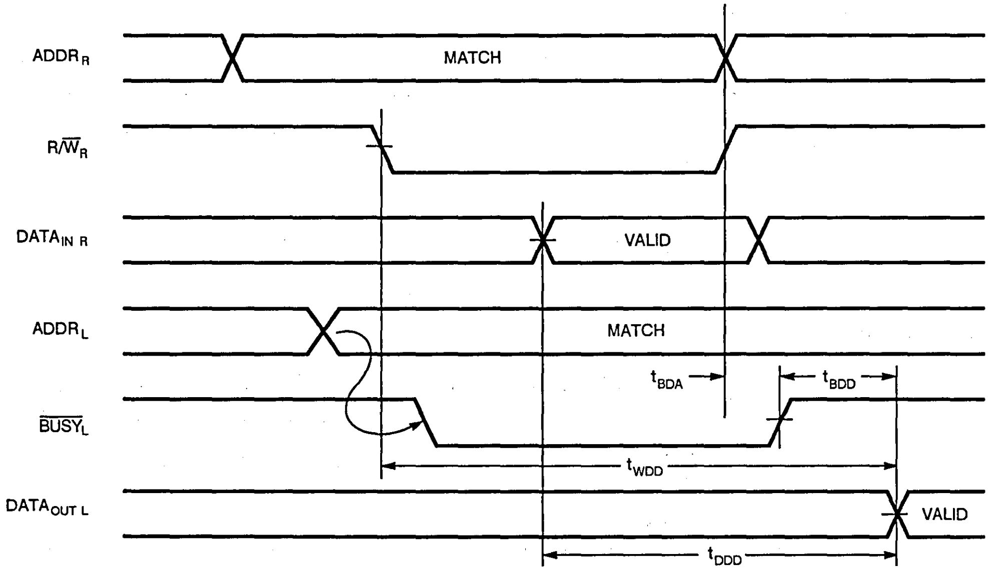
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [8]

SYMBOL	PARAMETER	7130 x 35[1] 7140 x 35[1]		7130 x 45 7140 x 45		7130 x 55 7140 x 55		7130 x 70 7140 x 70		7130 x 90 7140 x 90		7130 x 100/120[2] 7140 x 100/120[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
BUSY TIMING														
t_{WB}	Write to $\overline{BUSY}$ [3, 6]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WH}	Write Hold After $\overline{BUSY}$ [7]	20	–	20	–	20	–	20		20	–	20	–	ns
t_{BAA}	$\overline{BUSY}$ Access Time to Address	–	35	–	35	–	45	–	45	–	45	–	50/60	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	–	30	–	35	–	40	–	40	–	45	–	50/60	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	–	30	–	30	–	35	–	35	–	45	–	50/60	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	–	25	–	25	–	30	–	30	–	45	–	50/60	ns
t_{WDD}	Write Pulse to Data Delay [4]	–	60	–	70	–	80	–	90	–	100	–	120/140	ns
t_{DDD}	Write Data Valid to Read Data Delay [4]	–	35	–	45	–	55	–	70	–	90	–	100/120	ns
t_{APS}	Arbitration Priority Set-up Time	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data [5]	–	Note 5	–	Note 5	–	Note 5	–	Note 5	–	Note 5	–	Note 5	ns

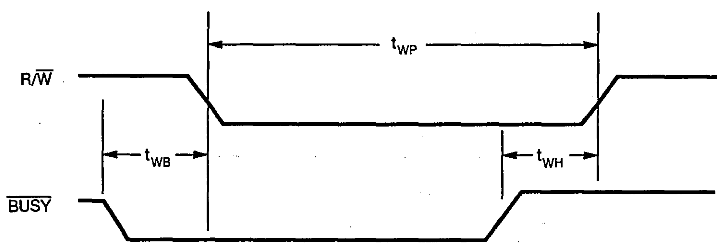
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. For SLAVE part (IDT7140) only.
4. Port-to-port delay through RAM cells from writing port to reading port.
5. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ WITH $\overline{\text{BUSY}}$



TIMING WAVEFORM OF WRITE WITH $\overline{\text{BUSY}}$



CAPACITANCE (T_A = +25°C, f = 1.0MHz)

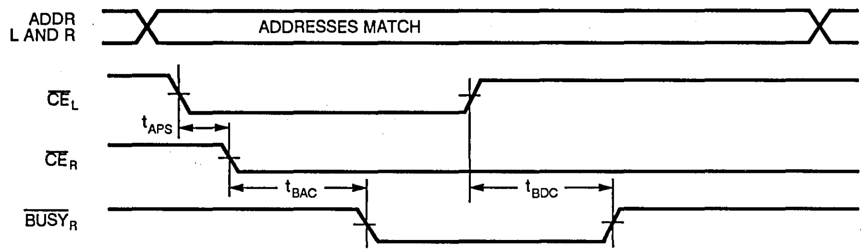
SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:

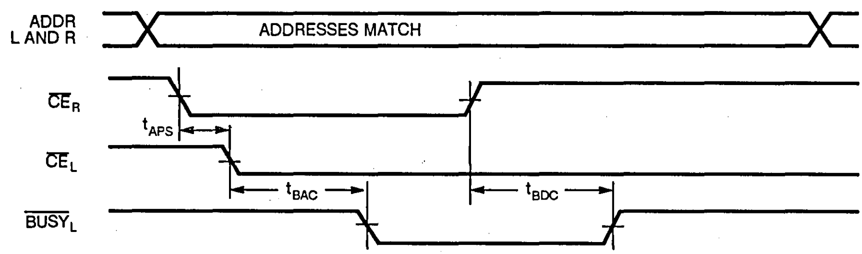
1. This parameter is determined by device characterization but is not production tested.

TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:

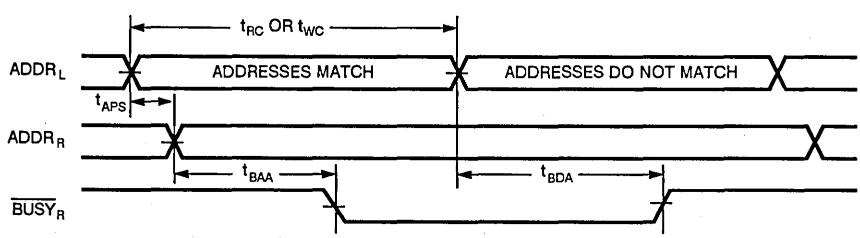


$\overline{CE}_R$ VALID FIRST:

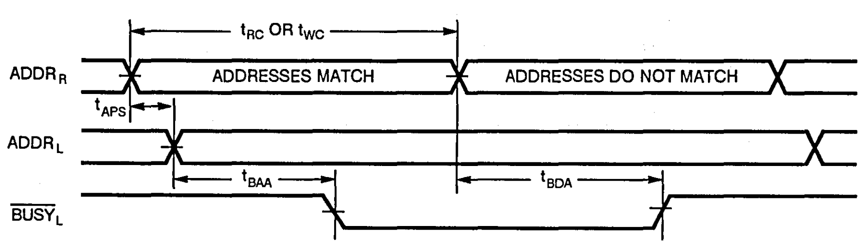


TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION [1]

LEFT ADDRESS VALID FIRST:



RIGHT ADDRESS VALID FIRST:



NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

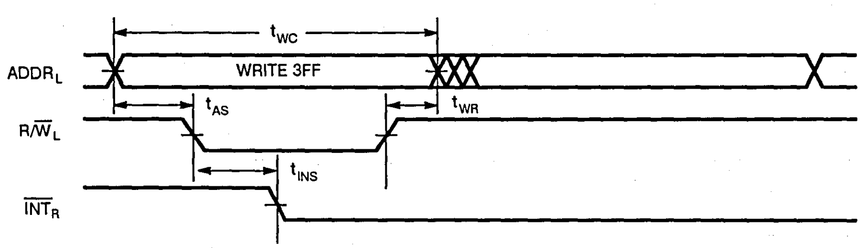
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	7130 x 35[1] 7140 x 35[1] MIN.	MAX.	7130 x 45 7140 x 45 MIN.	MAX.	7130 x 55 7140 x 55 MIN.	MAX.	7130 x 70 7140 x 70 MIN.	MAX.	7130 x 90 7140 x 90 MIN.	MAX.	7130 x 100/120[2] 7140 x 100/120[2] MIN.	MAX.	UNIT
INTERRUPT TIMING														
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{INS}	Interrupt Set Time	–	35	–	40	–	45	–	50	–	55	–	60/70	ns
t_{INR}	Interrupt Reset Time	–	35	–	40	–	45	–	50	–	55	–	60/70	ns

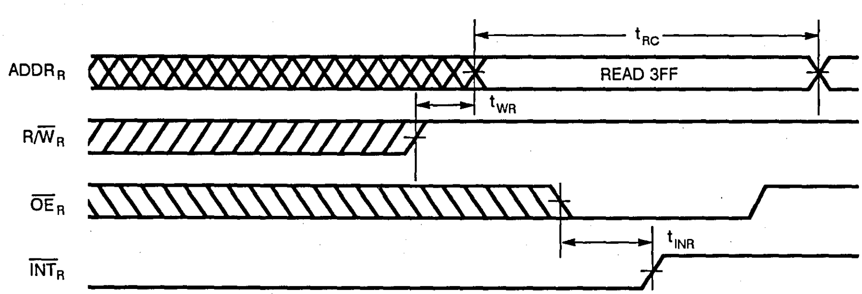
NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.

TIMING WAVEFORM OF INTERRUPT MODE (1, 2)

LEFT SIDE SETS $\overline{INT}_R$:



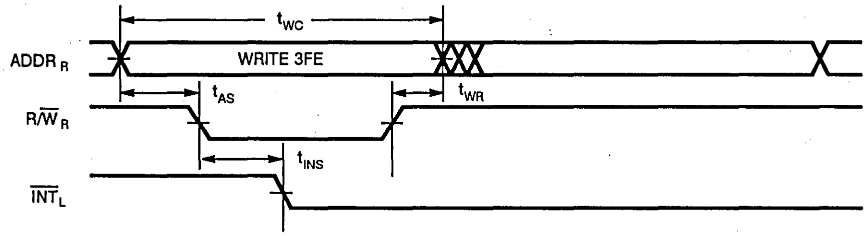
RIGHT SIDE CLEARS $\overline{INT}_R$:



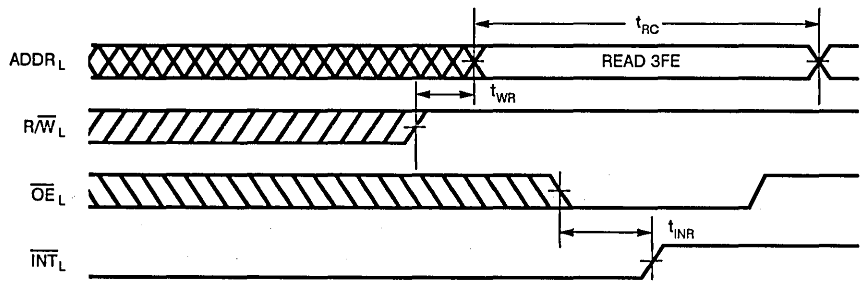
NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset to V_{OH} during power up.

TIMING WAVEFORM OF INTERRUPT MODE (1, 2)

RIGHT SIDE SETS $\overline{INT}_L$:



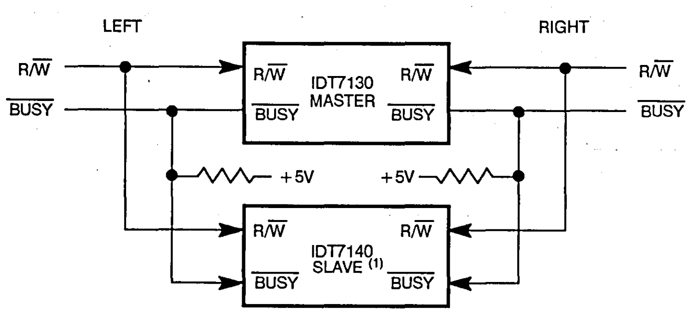
LEFT SIDE CLEARS $\overline{INT}_L$:



NOTES:

1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (high) during power up.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:

1. No arbitration in IDT7140 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7140 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT7130/40 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7130/40 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 3FF. The message (8 bits) at 3FE or 3FF is user-defined. If the interrupt function is not used, address locations 3FE and 3FF are not used as mail boxes, but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I—NON-CONTENTION READ/WRITE CONTROL (4)

LEFT OR RIGHT PORT (1)				FUNCTION
$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L =$ H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory (2)
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port (3)
H	L	H	Z	High Impedance Outputs

NOTES:
1. $A_{0L} - A_{9L} \neq A_{0R} - A_{9R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II—INTERRUPT FLAG (1, 4)

LEFT PORT					RIGHT PORT					FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L} - A_{9L}$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0L} - A_{9R}$	$\overline{INT}_R$	
L	L	X	3FF	X	X	X	X	X	L (2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FF	H (3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L (3)	L	L	X	3FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FE	H (2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH, L= LOW, X = DON'T CARE, NC= NO CHANGE

TABLE III—ARBITRATION (2)

LEFT PORT		RIGHT PORT		FLAGS (1)		FUNCTION
$\overline{CE}_L$	$A_{0L} - A_{9L}$	$\overline{CE}_R$	$A_{0L} - A_{9R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} - A_{9R}$	L	$\neq A_{0L} - A_{9L}$	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL5R	$= A_{0R} - A_{9R}$	LL5R	$= A_{0L} - A_{9L}$	H	L	L-Port Wins
RL5L	$= A_{0R} - A_{9R}$	RL5L	$= A_{0L} - A_{9L}$	L	H	R-Port Wins
LW5R	$= A_{0R} - A_{9R}$	LW5R	$= A_{0L} - A_{9L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R} - A_{9R}$	LW5R	$= A_{0L} - A_{9L}$	L	H	Arbitration Resolved

NOTE:
1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid $\geq$ 5ns before right address.
   RV5L = Right Address Valid $\geq$ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW $\geq$ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW $\geq$ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	P	Plastic DIP
	C	Sidebraze DIP
	J	Plastic Leaded Chip Carrier
	L48	48-Pin Leadless Chip Carrier
	L52	52-Pin Leadless Chip Carrier
	F	Flatpack
Speed	35	Commercial Only — Speed in Nanoseconds
	45	Speed in Nanoseconds
	55	Speed in Nanoseconds
	70	Speed in Nanoseconds
	90	Speed in Nanoseconds
	100	Speed in Nanoseconds
	120	Military Only — Speed in Nanoseconds
Power	LA	Low Power
	SA	Standard Power
Device Type	7130	8K (1K x 8-Bit) MASTER Dual-Port RAM
	7140	8K (1K x 8-Bit) SLAVE Dual-Port RAM

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT)

IDT7132SA/LA IDT7142SA/LA

FEATURES:

- High-speed access
  - Military: 45/55/70/90/100/120ns (max.)
  - Commercial: 35/45/55/70/90/100ns (max.)
- Low-power operation
  - IDT7132/42SA
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - IDT7132/42LA
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- MASTER IDT7132 easily expands data bus width to 16-or-more bits using SLAVE IDT7142
- On-chip port arbitration logic (IDT7132 only)
- $\overline{\text{BUSY}}$ output flag on IDT7132; $\overline{\text{BUSY}}$ input on IDT7142
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V ±10% power supply
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87002 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT7132/IDT7142 are high-speed 2K x 8 dual-port static RAMs. The IDT7132 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7142 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

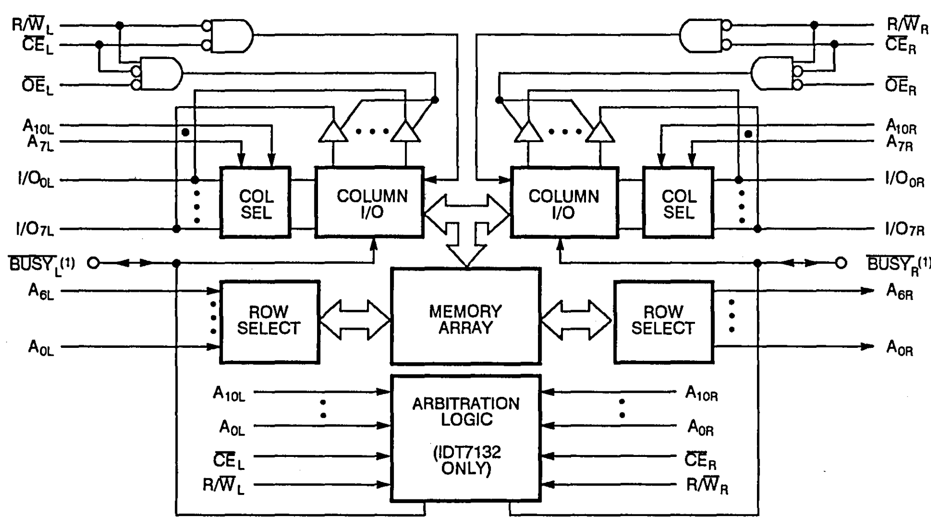
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{\text{CE}}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 35ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µW from a 2V battery.

The IDT7132/7142 devices are packaged in a 48-pin sidebraze or plastic DIP, 48- or 52-pin LCC, 52-pin PLCC, and a 48-lead flatpack.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



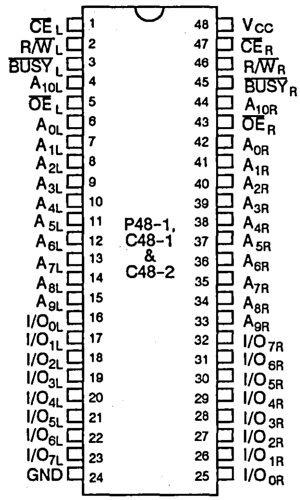
NOTES:

1. IDT7132 (MASTER): $\overline{\text{BUSY}}$ is open drain output and requires pullup resistor.
   IDT7142 (SLAVE): $\overline{\text{BUSY}}$ is input.

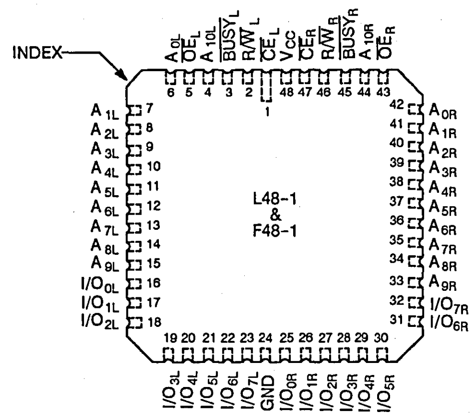
CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

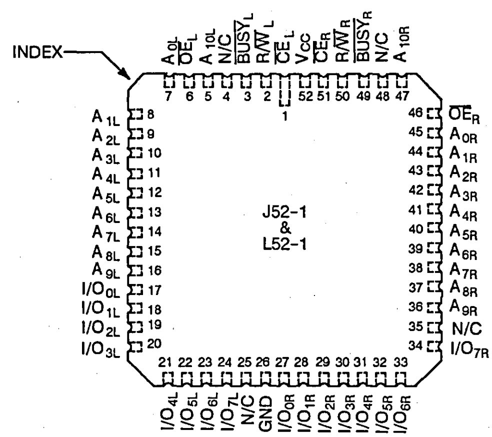
PIN CONFIGURATIONS



DIP
TOP VIEW



48-PIN LCC/FLATPACK
TOP VIEW



52-PIN LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7132SA IDT7142SA MIN.	IDT7132SA IDT7142SA MAX.	IDT7132LA IDT7142LA MIN.	IDT7132LA IDT7142LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE} = V_{IH}$, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 4mA	–	0.4	–	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (1) (V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION	7132 x 35(2) 7142 x 35(2) TYP.	MAX.	7132 x 45 7142 x 45 TYP.	MAX.	7132 x 55 7142 x 55 TYP.	MAX.	7132 x 70 7142 x 70 TYP.	MAX.	7132 x 90 7142 x 90 TYP.	MAX.	7132 x 100/120(3) 7142 x 100/120(3) TYP.	MAX.	UNIT
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$ Outputs Open f = f_{MAX}(4)	MIL. SA	–	–	75	230	65	230	65	225	65	200	65	190	mA
			MIL. LA	–	–	75	185	65	185	65	180	65	160	65	155	
			COM'L. SA	75	195	75	190	65	180	65	180	65	180	65	180	
			COM'L. LA	75	155	75	145	65	140	65	135	65	130	65	130	
I_{SB1}	Standby Current (Both Ports – TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}(4)	MIL. SA	–	–	25	65	25	65	25	65	25	65	25	65	mA
			MIL. LA	–	–	25	55	25	55	25	55	25	45	25	45	
			COM'L. SA	25	65	25	65	25	65	25	60	25	55	25	55	
			COM'L. LA	25	45	25	45	25	55	25	40	25	35	25	35	
I_{SB2}	Standby Current (One Port – TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}(4)	MIL. SA	–	–	40	135	40	135	40	135	40	125	40	125	mA
			MIL. LA	–	–	40	110	40	110	40	110	40	100	40	100	
			COM'L. SA	40	130	40	120	40	115	40	110	40	110	40	110	
			COM'L. LA	40	95	40	85	40	85	40	85	40	75	40	75	
I_{SB3}	Full Standby Current (Both Ports – All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0(4)	MIL. SA	–	–	1.0	30	1.0	30	1.0	30	1.0	30	1.0	30	mA
			MIL. LA	–	–	0.2	10	0.2	10	0.2	10	0.2	10	0.2	10	
			COM'L. SA	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
			COM'L. LA	0.2	4	0.2	4	0.2	4	0.2	4	0.2	4	0.2	4.0	
I_{SB4}	Full Standby Current (One Port – All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$-0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}(4)	MIL. SA	–	–	40	125	40	120	40	115	40	110	40	110	mA
			MIL. LA	–	–	35	95	35	90	35	85	35	80	35	80	
			COM'L. SA	40	115	40	105	40	100	40	100	40	95	40	95	
			COM'L. LA	35	90	35	80	35	75	35	75	35	70	35	70	

NOTES:
1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. f_{MAX} = All inputs cycling at f = $1/t_{RC}$ (except Output Enable). f = 0 means no address or control lines change. Applies only to input at CMOS level standby, I_{SB3}.

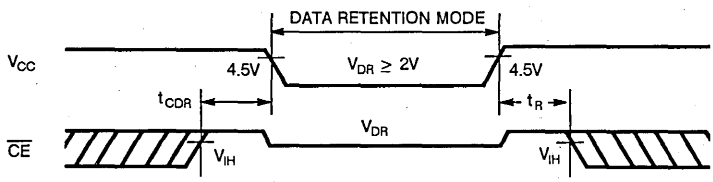
DATA RETENTION CHARACTERISTICS (LA Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7132LA/IDT7142LA MIN.	TYP.(1)	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention			2.0	–	–	V
I_{CCDR}	Data Retention Current	$V_{CC} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	MIL.	–	100	4000	µA
			COM'L.	–	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–	–	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–	–	ns

NOTES:
1. $V_{CC} = 2V$, $T_A = +25°C$
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

5

DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

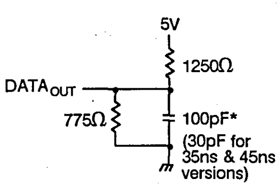


Figure 1. Output Load

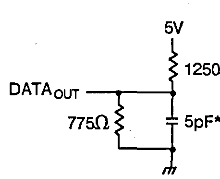


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

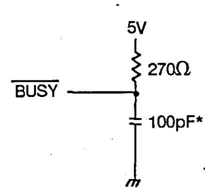


Figure 3. $\overline{BUSY}$ Output Load (IDT7132 only)

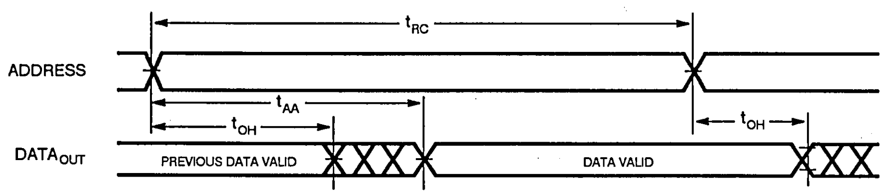
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (5)

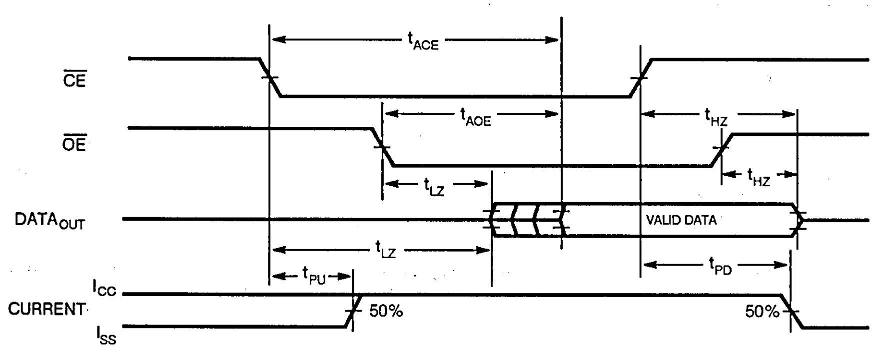
SYMBOL	PARAMETER	7132 x 35(2) 7142 x 35(2) MIN.	MAX.	7132 x 45 7142 x 45 MIN.	MAX.	7132 x 55 7142 x 55 MIN.	MAX.	7132 x 70 7142 x 70 MIN.	MAX.	7132 x 90 7142 x 90 MIN.	MAX.	7132 x 100/120(3) 7142 x 100/120(3) MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	35	–	45	–	55	–	70	–	90	–	100/120	–	ns
t_{AA}	Address Access Time	–	35	–	45	–	55	–	70	–	90	–	100/120	ns
t_{ACE}	Chip Enable Access Time	–	35	–	45	–	55	–	70	–	90	–	100/120	ns
t_{AOE}	Output Enable Access Time	–	25	–	30	–	35	–	40	–	40	–	40/60	ns
t_{OH}	Output Hold From Address Change	0	–	0	–	0	–	0	–	10	–	10	–	ns
t_{LZ}	Output Low Z Time (1, 4)	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Output High Z Time (1, 4)	–	15	–	20	–	30	–	35	–	40	–	40	ns
t_{PU}	Chip Enable to Power Up Time (4)	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time (4)	–	50	–	50	–	50	–	50	–	50	–	50	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$

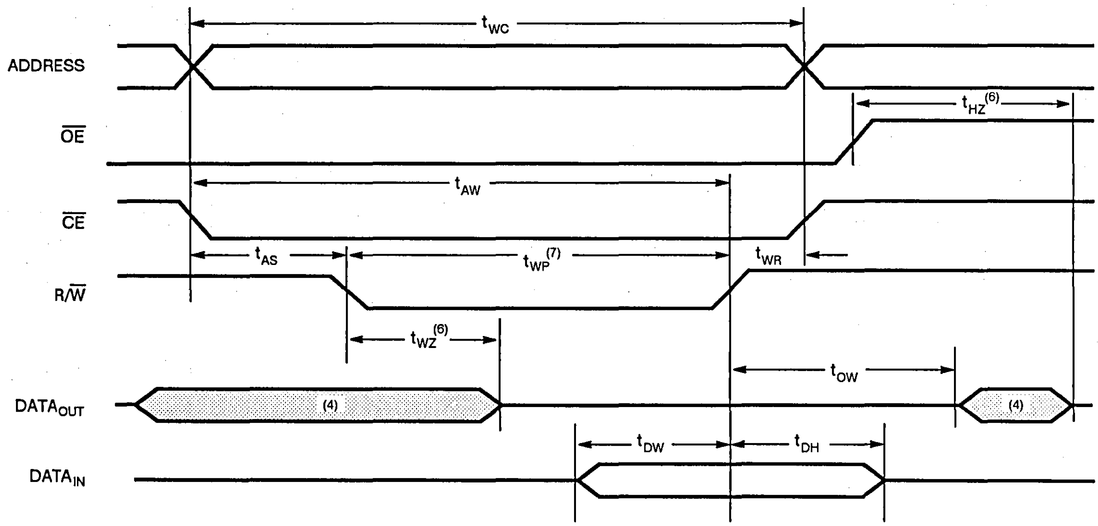
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [6]

SYMBOL	PARAMETER	7132 x 35[2] 7142 x 35[2]		7132 x 45 7142 x 45		7132 x 55 7142 x 55		7132 x 70 7142 x 70		7132 x 90 7142 x 90		7132 x 100/120[3] 7142 x 100/120[3]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE														
t_{WC}	Write Cycle Time [5]	35		45	–	55	–	70	–	90	–	100/120		ns
t_{EW}	Chip Enable to End of Write	30		35		40	–	50	–	85	–	90/100	–	ns
t_{AW}	Address Valid to End of Write	30		35	–	40	–	50	–	85	–	90/100	–	ns
t_{AS}	Address Set-up Time	0		0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	30		35	–	40	–	50	–	55	–	55/65	–	ns
t_{WR}	Write Recovery Time	0		0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	20		20	–	20	–	30	–	40	–	40	–	ns
t_{HZ}	Output High Z Time [1,4]		15	–	20	–	30	–	35	–	40	–	40	ns
t_{DH}	Data Hold Time	0		0	–	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enabled to Output in High Z [1,4]	–	15	–	20	–	30	–	35	–	40	–	40/50	ns
t_{OW}	Output Active From End of Write [1,4]	0		0	–	0	–	0	–	0	–	0	–	ns

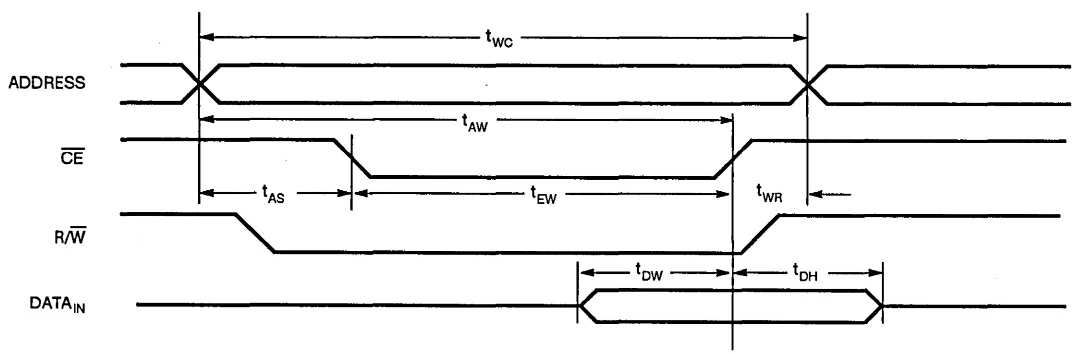
NOTES:

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$.
6. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING) (1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:

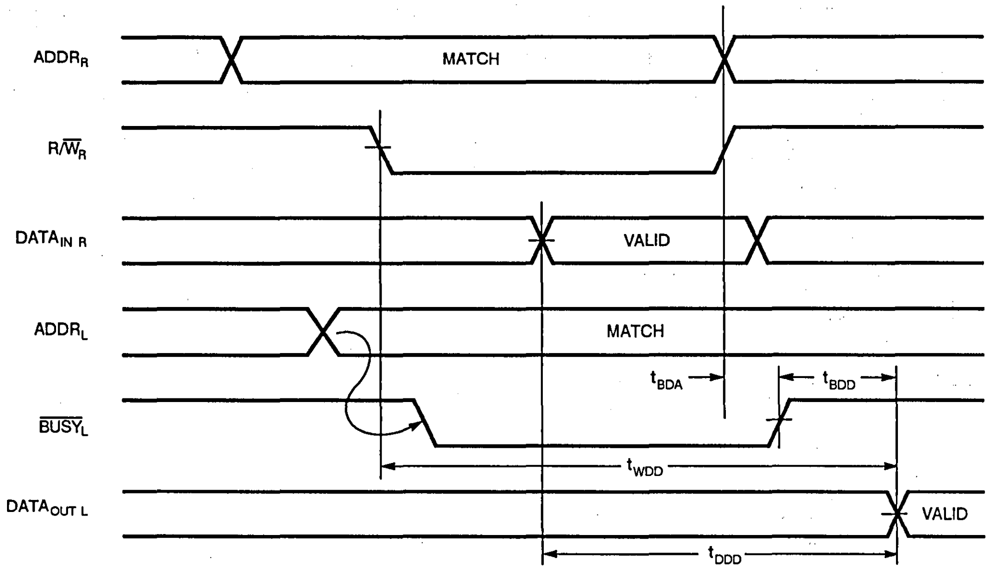
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ}+ t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

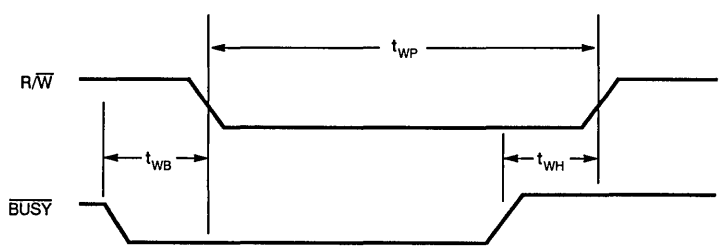
SYMBOL	PARAMETER	7132 x 35(1) 7142 x 35(1)		7132 x 45 7142 x 45		7132 x 55 7142 x 55		7132 x 70 7142 x 70		7132 x 90 7142 x 90		7132 x 100/120(2) 7142 x 100/120(2)		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
BUSY TIMING														
t_{WB}	Write to $\overline{BUSY}$ (3, 6)	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WH}	Write Hold After $\overline{BUSY}$ (7)	20	–	20	–	20		20	–	20	–	20	–	ns
t_{BAA}	$\overline{BUSY}$ Access Time to Address	–	35	–	35	–	45	–	45	–	45	–	50/60	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	–	30	–	35	–	40	–	40	–	45	–	50/60	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	–	30	–	30	–	35	–	35	–	45	–	50/60	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	–	25	–	25	–	30	–	30	–	45	–	50/60	ns
t_{WDD}	Write Pulse to Data Delay (4)	–	60	–	70	–	80	–	90	–	100	–	120/140	ns
t_{DDD}	Write Data Valid to Read Data Delay (4)	–	35	–	45	–	55	–	70	–	90	–	100/120	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data (5)	–	Note 5	–	Note 5	–	Note 5	–	Note 5	–	Note 5	–	Note 5	ns
t_{APS}	Arbitration Priority Set-up Time	5	–	5	–	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. For SLAVE part (IDT7142) only.
4. Port-to-port delay through RAM cells from writing port to reading port.
5. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$(actual).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF READ WITH $\overline{\text{BUSY}}$

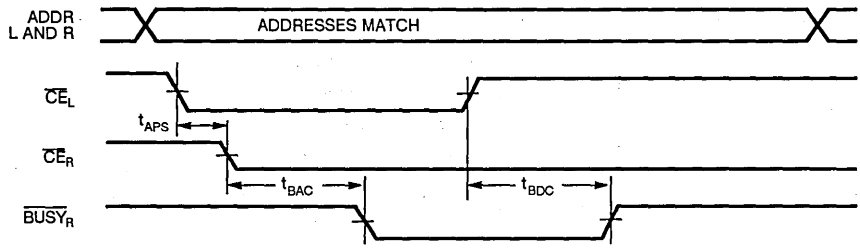


TIMING WAVEFORM OF WRITE WITH $\overline{\text{BUSY}}$

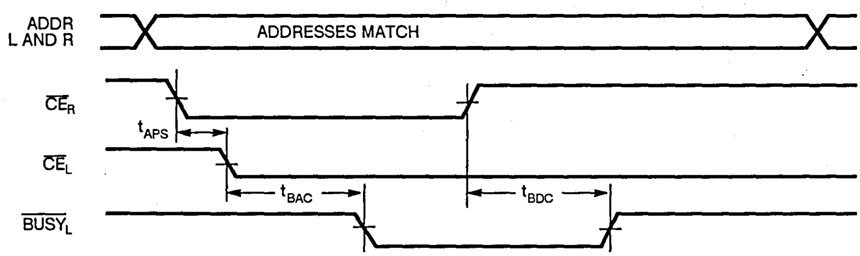


TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:

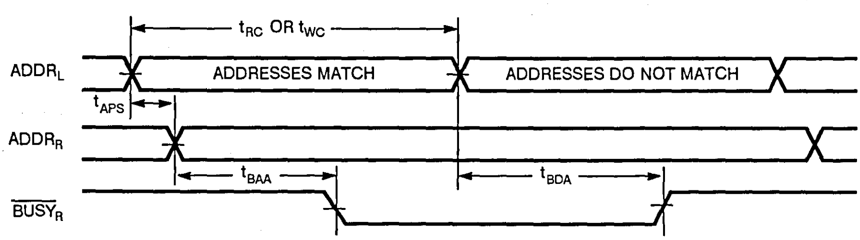


$\overline{CE}_R$ VALID FIRST:

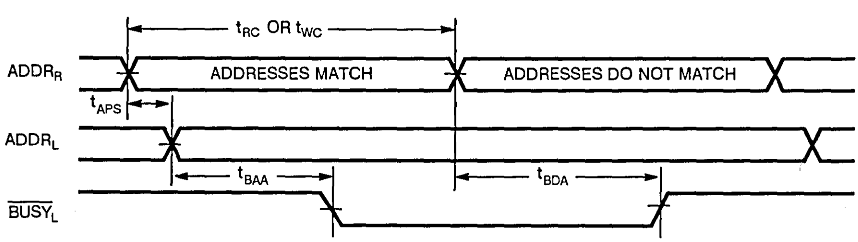


TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (1)

LEFT ADDRESS VALID FIRST:

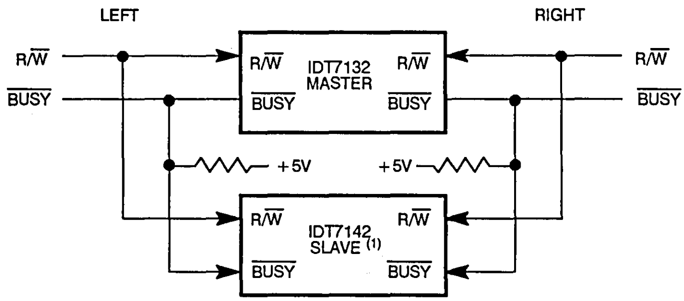


RIGHT ADDRESS VALID FIRST:



NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:

1. No arbitration in IDT7142 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7142 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT7132/42 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active BUSY flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

5

TRUTH TABLES

TABLE I—NON-CONTENTION READ/WRITE CONTROL

LEFT OR RIGHT PORT (1)				FUNCTION
$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L =$ H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory (2)
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port (3)
H	L	H	Z	High Impedance Outputs

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{BDD} timing.

H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is sampled and not 100% tested.

TABLE II – ARBITRATION [2]

LEFT PORT		RIGHT PORT		FLAGS [1]		FUNCTION
$\overline{CE}_L$	A_{0L} - A_{10L}	$\overline{CE}_R$	A_{0R} - A_{10R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R}$-A_{10R}	L	$\neq A_{0L}$-A_{10L}	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL5R	$= A_{0R}$-A_{10R}	LL5R	$= A_{0L}$-A_{10L}	H	L	L-Port Wins
RL5L	$= A_{0R}$-A_{10R}	RL5L	$= A_{0L}$-A_{10L}	L	H	R-Port Wins
LW5R	$= A_{0R}$-A_{10R}	LW5R	$= A_{0L}$-A_{10L}	H	L	Arbitration Resolved
LW5R	$= A_{0R}$-A_{10R}	LW5R	$= A_{0L}$-A_{10L}	L	H	Arbitration Resolved

NOTE:
1. X = DON'T CARE, L = LOW, H = HIGH
2. LV5R = Left Address Valid $\geq$ 5ns before right address.
   RV5L = Right Address Valid $\geq$ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW $\geq$ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW $\geq$ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range:
- Blank — Commercial (0°C to +70°C)
- B — Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:
- P — Plastic DIP
- C — Sidebraze DIP (600 mil)
- J — Plastic Leaded Chip Carrier
- L — Leadless Chip Carrier – indicate 48- or 52-pin
- F — Flatpack

Speed (Speed in Nanoseconds):
- 35 — Commercial Only
- 45
- 55
- 70
- 90
- 100
- 120 — Military Only

Power:
- LA — Low Power
- SA — Standard Power

Device Type:
- 7132 — 16K (2K x 8-Bit) MASTER Dual-Port RAM
- 7142 — 16K (2K x 8-Bit) SLAVE Dual-Port RAM

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAMS 16K (2K x 8-BIT) WITH INTERRUPTS

IDT71321SA/LA
IDT71421SA/LA

FEATURES:

- High-speed access
  - Military: 45/55/70ns (max.)
  - Commercial: 35/45/55ns (max.)
- Low-power operation
  - IDT71321/421SA
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - IDT71321/421LA
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- Two $\overline{INT}$ flags for port-to-port communications
- MASTER IDT71321 easily expands data bus width to 16-or-more-bits using SLAVE IDT71421
- On-chip port arbitration logic (IDT71321 only)
- $\overline{BUSY}$ output flag on IDT71321; $\overline{BUSY}$ input on IDT71421
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V ±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71321/IDT71421 are high-speed 2K x 8 dual-port static RAMs with internal interrupt logic for interprocessor communications. The IDT71321 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM, together with the IDT71421 "SLAVE" dual-port, in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

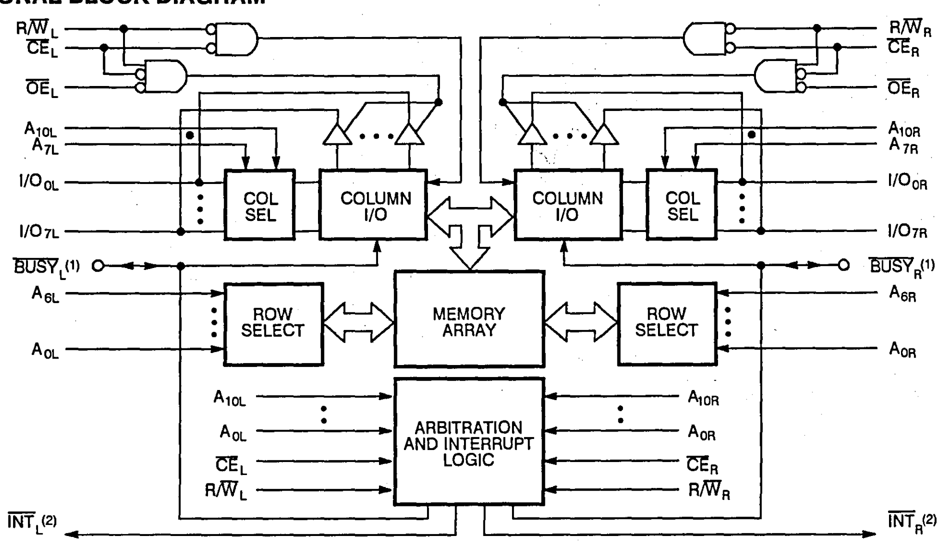
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 35ns. Low-power (LA) versions offer battery backup data retention capability with each port typically consuming 200µW from a 2V battery.

The IDT71321/71421 devices are packaged in 52-pin LCCs and PLCCs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

5

FUNCTIONAL BLOCK DIAGRAM

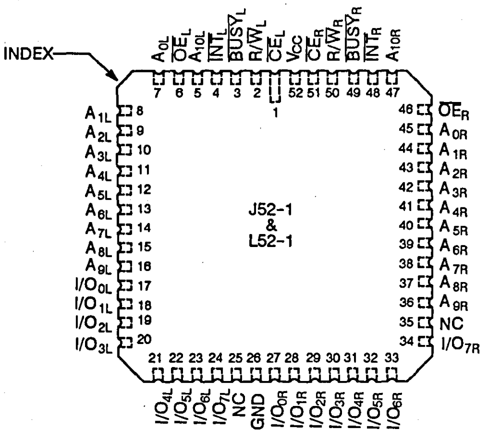


NOTES:

1. IDT71321 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor. IDT71421 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	IDT71321SA IDT71421SA MIN.	MAX.	IDT71321LA IDT71421LA MIN.	MAX.	UNIT
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 4mA	–	0.4	–	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}/\overline{INT}$)	I_{OL} = 16mA	–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (1) (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		71321x35 (2) 71421x35 (2) TYP. (4)	MAX.	71321x45 71421x45 TYP. (4)	MAX.	71321x55 71421x55 TYP. (4)	MAX.	71321x70 (3) 71421x70 (3) TYP. (4)	MAX.	UNIT
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX} (5)	MIL.	SA	–	–	75	230	65	230	65	225	mA
				LA	–	–	75	185	65	185	65	180	
			COM'L.	SA	75	195	75	190	65	180	–	–	
				LA	75	155	75	145	65	140	–	–	
I_{SB1}	Standby Current (Both Ports – TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH} f = f_{MAX} (5)	MIL.	SA	–	–	25	65	25	65	25	65	mA
				LA	–	–	25	55	25	55	25	55	
			COM'L.	SA	25	65	25	65	25	65	–	–	
				LA	25	45	25	45	25	45	–	–	
I_{SB2}	Standby Current (One Port – TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX} (5)	MIL.	SA	–	–	40	135	40	135	40	135	mA
				LA	–	–	40	110	40	110	40	110	
			COM'L.	SA	40	130	40	120	40	115	–	–	
				LA	40	95	40	85	40	85	–	–	
I_{SB3}	Full Standby Current (Both Ports – All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, f = 0 (5)	MIL.	SA	–	–	1.0	30	1.0	30	1.0	30	mA
				LA	–	–	0.2	10	0.2	10	0.2	10	
			COM'L.	SA	1.0	15	1.0	15	1.0	15	–	–	
				LA	0.2	4.0	0.2	4.0	0.2	4.0	–	–	
I_{SB4}	Full Standby Current (One Port – All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX} (5)	MIL.	SA	–	–	40	125	40	120	40	110	mA
				LA	–	–	35	95	35	90	35	80	
			COM'L.	SA	40	115	40	115	40	100	–	–	
				LA	35	90	35	80	35	75	–	–	

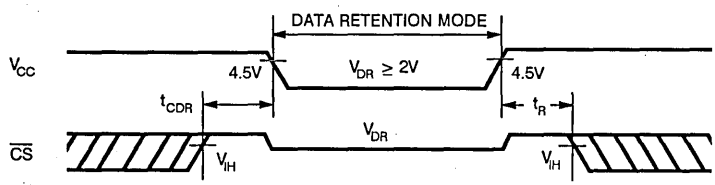
NOTES:
1. "x" in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. V_{CC} = 5V, T_A = +25°C
5. f_{MAX} = $1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby I_{SB3}.

DATA RETENTION CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITION		IDT71321LA/IDT71421LA MIN.	TYP.(1)	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention			2.0	–	–	V
I_{CCDR}	Data Retention Current	$V_{CC} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.2V$	MIL.	–	100	4000	µA
			COM'L.	–	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		0	–	–	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–	–	ns

NOTES:
1. $V_{CC} = 2V$, $T_A = +25°C$
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

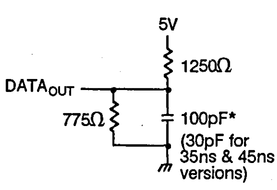


Figure 1. Output Load

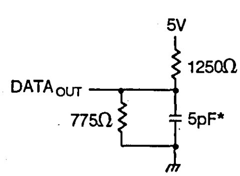


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

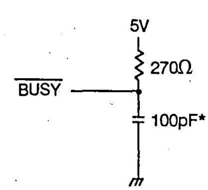


Figure 3. $\overline{BUSY}$ and $\overline{INT}$ Output Load

* Including scope and jig.

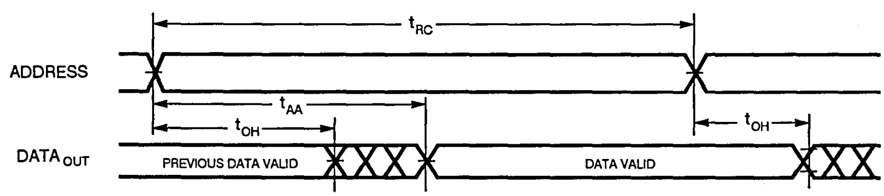
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	71321SA/LA35(2) 71421SA/LA35(2) MIN.	MAX.	71321SA/LA45 71421SA/LA45 MIN.	MAX.	71321SA/LA55 71421SA/LA55 MIN.	MAX.	71321SA/LA70(3) 71421SA/LA70(3) MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	35	–	45	–	55	–	70	ns
t_{ACE}	Chip Enable Access Time	–	35	–	45	–	55	–	70	ns
t_{AOE}	Output Enable Access Time	–	25	–	30	–	35	–	40	ns
t_{OH}	Output Hold From Address Change	0	–	0	–	0	–	0	–	ns
t_{LZ}	Output Low Z Time (1, 4)	5	–	5	–	5	–	5	–	ns
t_{HZ}	Output High Z Time (1, 4)	–	15	–	20	–	30	–	35	ns
t_{PU}	Chip Enable to Power Up Time (4)	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time (4)	–	50	–	50	–	50	–	50	ns

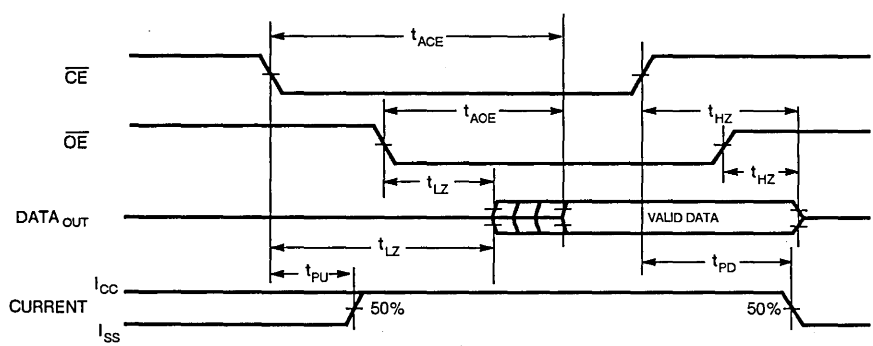
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.

5

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)



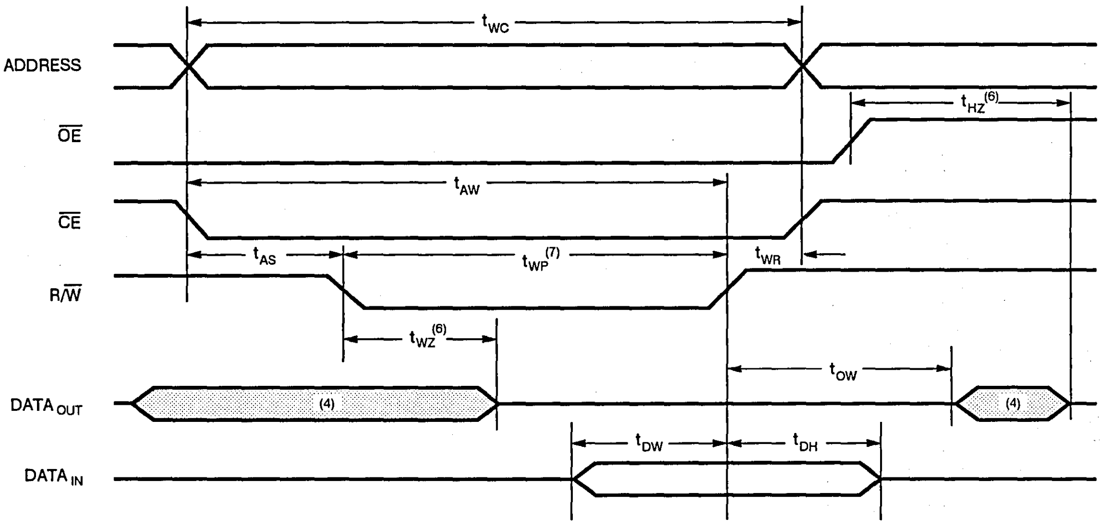
NOTES:
1. $R/\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$.
3. Addresses valid prior to, or coincident with, $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

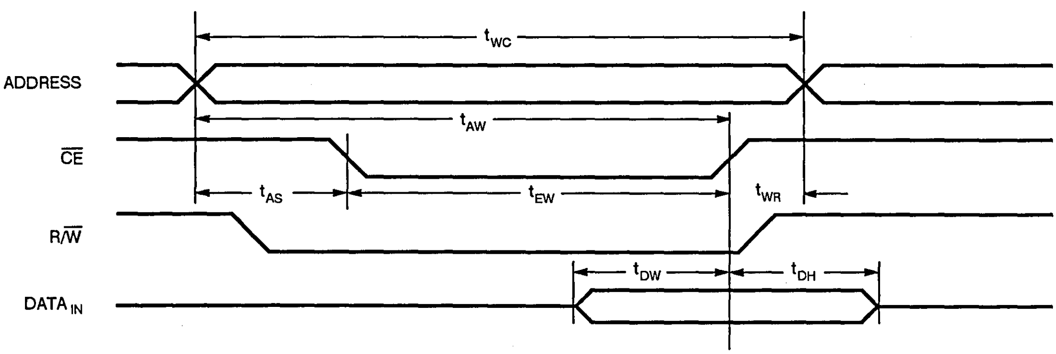
SYMBOL	PARAMETER	71321SA/LA35[2] 71421SA/LA35[2] MIN.	MAX.	71321SA/LA45 71421SA/LA45 MIN.	MAX.	71321SA/LA55 71421SA/LA55 MIN.	MAX.	71321SA/LA70[3] 71421SA/LA70[3] MIN.	MAX.	UNIT
WRITE CYCLE										
t_{WC}	Write Cycle Time [5]	35	–	45	–	55	–	70	–	ns
t_{EW}	Chip Enable to End of Write	30	–	35	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	30	–	35	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	30	–	35	–	40	–	50	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	20	–	20	–	20	–	30	–	ns
t_{HZ}	Output High Z Time [1,4]	–	15	–	20	–	30	–	35	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enabled to Output in High Z [1,4]	–	15	–	20	–	30	–	35	ns
t_{OW}	Output Active From End of Write [1,4]	0	–	0	–	0	–	0	–	ns

NOTES:
1. Transition is measured ±500mV from low or high voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING (1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING (1, 2, 3, 5)



NOTES:

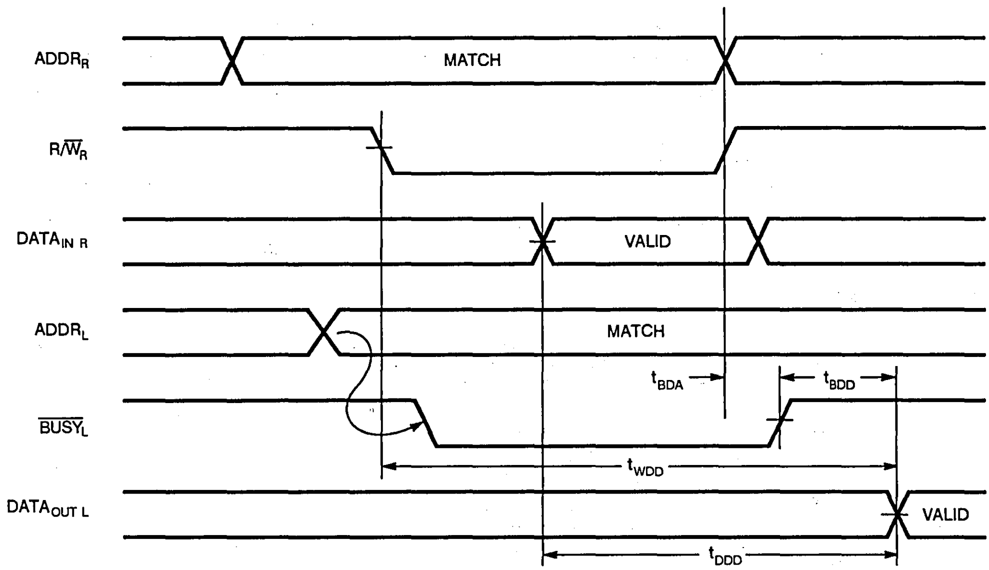
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse must be the larger of t_{WP} or ($t_{WZ} + t_{DW}$) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

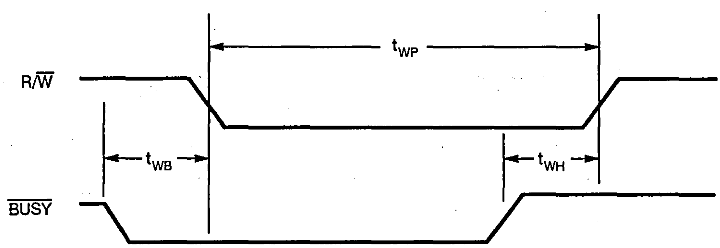
SYMBOL	PARAMETER	71321SA/LA35(1) 71421SA/LA35(1) MIN.	MAX.	71321SA/LA45 71421SA/LA45 MIN.	MAX.	71321SA/LA55 71421SA/LA55 MIN.	MAX.	71321SA/LA70(2) 71421SA/LA70(2) MIN.	MAX.	UNIT
BUSY TIMING										
t_{WB}	Write to $\overline{BUSY}$ (3, 6)	0	–	0	–	-10	–	-10	–	ns
t_{WH}	Write Hold After $\overline{BUSY}$ (7)	20	–	20	–	20		20	–	ns
t_{BAA}	$\overline{BUSY}$ Access Time to Address	–	35	–	35	–	45	–	45	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	–	30	–	35	–	40	–	40	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	–	30	–	30	–	35	–	35	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	–	25	–	25	–	30	–	30	ns
t_{WDD}	Write Pulse to Data Delay (4)	–	60	–	70	–	80	–	90	ns
t_{DDD}	Write Data Valid to Read Data Delay (4)	–	35	–	45	–	55	–	70	ns
t_{APS}	Arbitration Priority Set-up Time	5	–	5	–	5	–	5	–	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data (5)	–	Note 5	–	Note 5	–	Note 5	–	Note 5	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. For SLAVE part (IDT71421) only.
4. Port-to-port delay through RAM cells from writing port to reading port.
5. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$



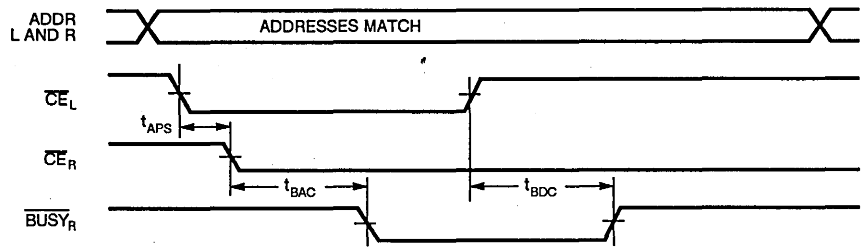
TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$



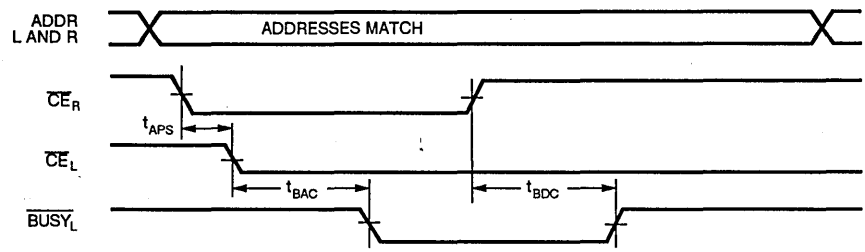
5

TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:

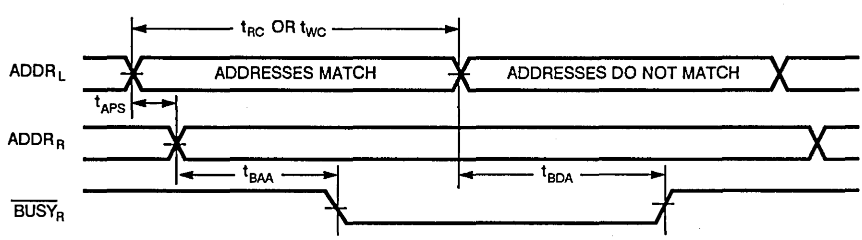


$\overline{CE}_R$ VALID FIRST:

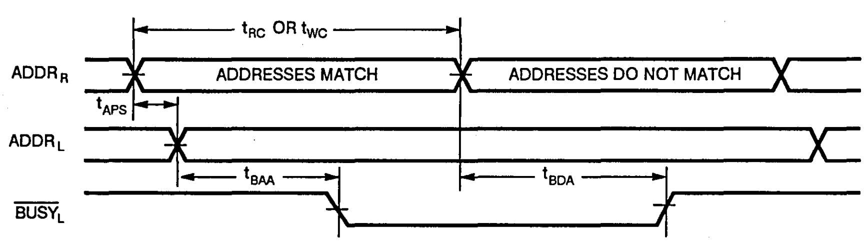


TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION [1]

LEFT ADDRESS VALID FIRST:



RIGHT ADDRESS VALID FIRST:



NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

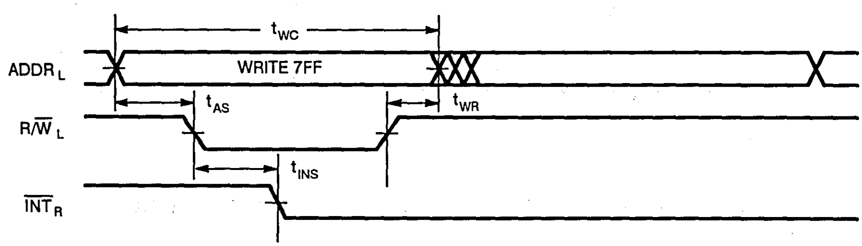
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	71321SA/LA35(1) 71421SA/LA35(1) MIN.	MAX.	71321SA/LA45 71421SA/LA45 MIN.	MAX.	71321SA/LA55 71421SA/LA55 MIN.	MAX.	71321SA/LA70(2) 71421SA/LA70(2) MIN.	MAX.	UNIT
INTERRUPT TIMING										
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{INS}	Interrupt Set Time	–	35	–	40	–	45	–	50	ns
t_{INR}	Interrupt Reset Time	–	35	–	40	–	45	–	50	ns

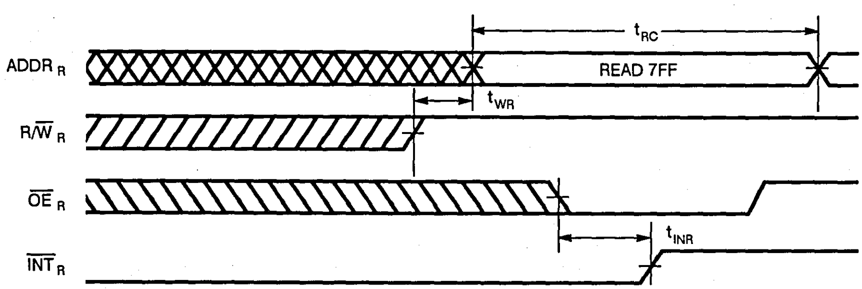
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.

TIMING WAVEFORM OF INTERRUPT MODE (1, 2)

LEFT SIDE SETS $\overline{INT}_R$:



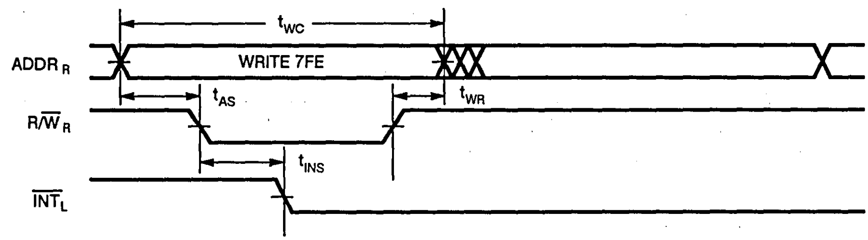
RIGHT SIDE CLEARS $\overline{INT}_R$:



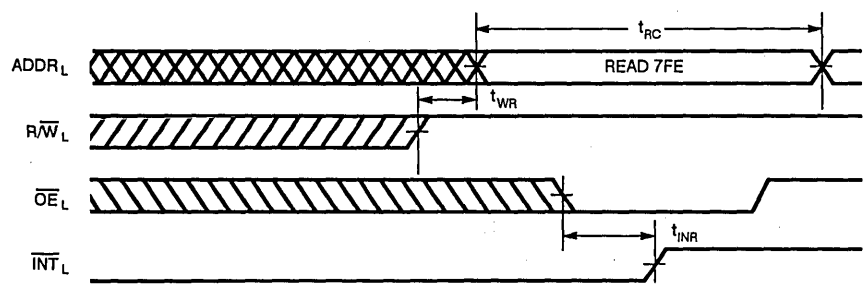
NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset to V_{OH} during power up.

TIMING WAVEFORM OF INTERRUPT MODE [1, 2]

RIGHT SIDE SETS $\overline{INT}_L$:



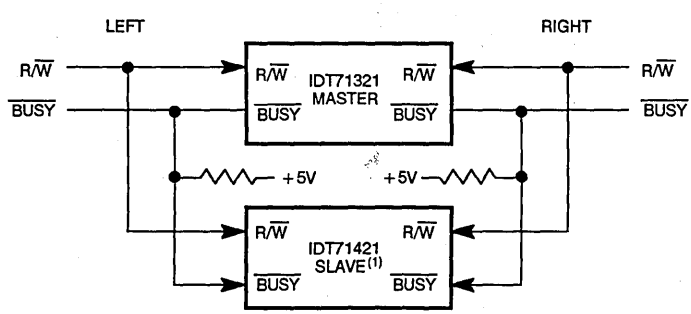
LEFT SIDE CLEARS $\overline{INT}_L$:



NOTES:

1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (high) during power up.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:

1. No arbitration in IDT71421 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT71421 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT71321/421 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 7FE (HEX). The left port clears the interrupt by reading address location 7FE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 7FF. The message (8 bits) at 7FE or 7FF is user-defined. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its L $\overline{BUSY}$ while another activates its R $\overline{BUSY}$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I — NON-CONTENTION READ/WRITE CONTROL[4]

LEFT OR RIGHT PORT [1]				FUNCTION
$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L =$ H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory [2]
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port [3]
H	L	H	Z	High Impedance Outputs

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{BDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

CAPACITANCE ($T_A = +25°C$, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNITS
C_{IN}	Input Capacitance	$V_{IN} = 0V$	11	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

TABLE II — INTERRUPT FLAG [1, 4]

LEFT PORT					RIGHT PORT					FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L}-A_{10L}$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0L}-A_{10R}$	$\overline{INT}_R$	
L	L	X	7FF	X	X	X	X	X	L [2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H [3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L [3]	L	L	X	7FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H [2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE

TABLE III — ARBITRATION [2]

LEFT PORT		RIGHT PORT		FLAGS [1]		FUNCTION
$\overline{CE}_L$	$A_{0L}-A_{10L}$	$\overline{CE}_R$	$A_{0L}-A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R}-A_{10R}$	L	$\neq A_{0L}-A_{10L}$	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL5R	$= A_{0R}-A_{10R}$	LL5R	$= A_{0L}-A_{10L}$	H	L	L-Port Wins
RL5L	$= A_{0R}-A_{10R}$	RL5L	$= A_{0L}-A_{10L}$	L	H	R-Port Wins
LW5R	$= A_{0R}-A_{10R}$	LW5R	$= A_{0L}-A_{10L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R}-A_{10R}$	LW5R	$= A_{0L}-A_{10L}$	L	H	Arbitration Resolved

NOTES:
1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

ORDERING INFORMATION

IDT	XXXX	A	999	A	A
	Device Type	Power	Speed	Package	Process/ Temperature Range

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	J	PLCC
	L	LCC
Speed	35	Commercial Only } Speed in Nanoseconds
	45	
	55	
	70	Military Only } Speed in Nanoseconds
Power	LA	Low Power
	SA	Standard Power
Device Type	71321	16K (2K x 8-Bit) MASTER Dual-Port RAM w/ Interrupt
	71421	16K (2K x 8-Bit) SLAVE Dual-Port RAM w/ Interrupt

5

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT) WITH SEMAPHORE

PRELIMINARY
IDT71322S
IDT71322L

FEATURES:

- High-speed access
  - Military: 45/55/70ns (max.)
  - Commercial: 45/55/70ns (max.)
- Low-power operation
  - IDT71322S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT71322L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation—2V data retention
- TTL-compatible, single 5V(±10%) power supply
- Available in a variety of plastic and hermetic packages for both through hole and surface mount applications
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

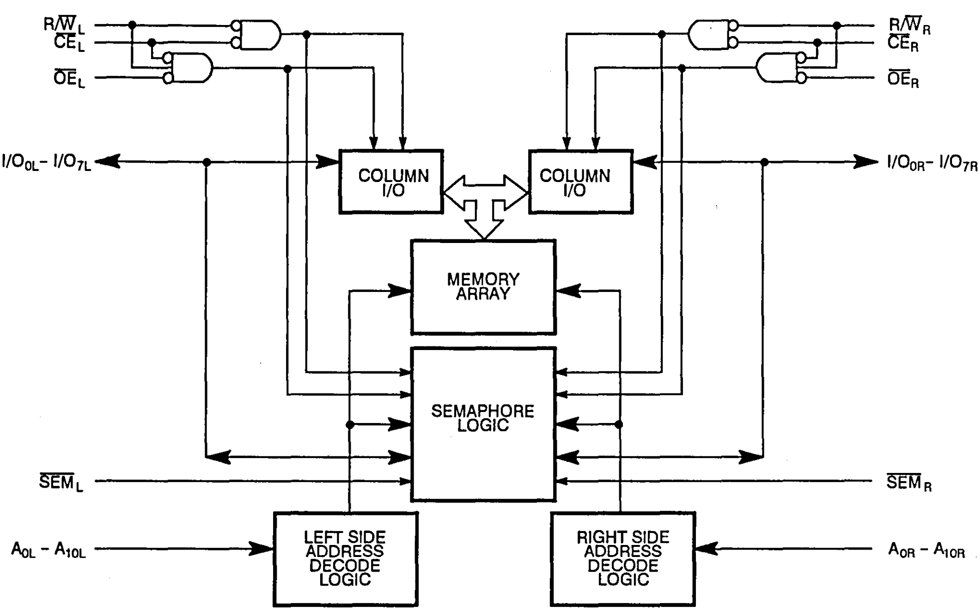
The IDT71322 is an extremely high-speed 2K x 8 dual-port static RAM with full on-chip hardware support of semaphore signalling between the two ports.

The IDT71322 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in memory. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. This block contains unassigned flags which can be accessed by either side; however, only one side can control the flag at any time. An automatic power down feature, controlled by $\overline{CE}$ and $\overline{SEM}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, this device typically operates on only 500mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery.

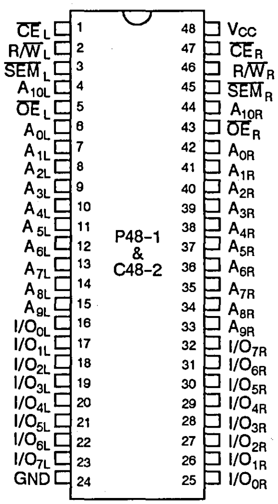
The IDT71322 is packaged in a 48-pin sidebraze or plastic DIP or 52-pin LCC and PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

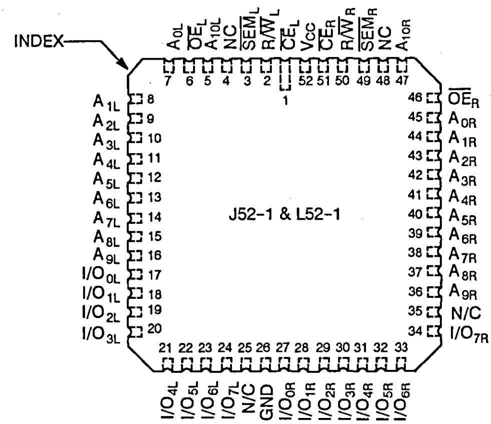


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characteristics, but is not production tested.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT71322S MIN.	IDT71322S MAX.	IDT71322L MIN.	IDT71322L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA	–	0.4	–	0.4	V
		I_{OL} = 8mA	–	0.5	–	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		IDT71322x45 TYP.[2]	IDT71322x45 MAX.	IDT71322x55 TYP.[2]	IDT71322x55 MAX.	IDT71322x70 TYP.[2]	IDT71322x70 MAX.	UNIT
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open $\overline{SEM}$ = Don't Care f = f_{MAX}[3]	MIL.	S	100	240	100	230	100	230	mA
				L	100	200	100	180	100	180	
			COM'L.	S	170	200	100	200	100	200	
				L	100	160	100	160	100	160	
I_{CC1}	Dynamic Operating Current (Semaphores Both Sides)	$\overline{CE}$ = V_{IH} $\overline{SEM}$ = V_{IL} Outputs Open f = f_{MAX}[3]	MIL.	S	85	130	85	130	85	130	mA
				L	85	110	85	110	85	110	
			COM'L.	S	85	130	85	130	85	130	
				L	85	100	85	100	85	100	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{IH} f = f_{MAX}[3]	MIL.	S	25	70	25	70	25	70	mA
				L	25	50	25	50	25	50	
			COM'L.	S	25	70	25	70	25	70	
				L	25	40	25	40	25	40	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	MIL.	S	50	160	50	150	50	150	mA
				L	50	130	50	120	50	120	
			COM'L.	S	50	130	50	130	50	130	
				L	50	100	50	100	50	100	
I_{SB3}	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{CC} -0.2V, f = 0[3]	MIL.	S	1	30	1	30	1	30	mA
				L	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1	15	1	15	1	15	
				L	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	50	130	50	120	50	120	mA
				L	45	100	45	90	45	90	
			COM'L.	S	45	110	50	110	50	110	
				L	45	90	45	90	45	90	

NOTES:
1. x in part numbers indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C
3. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby, I_{SB3}.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

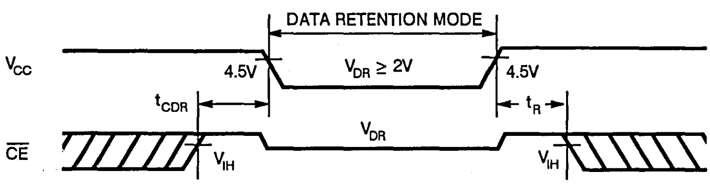
(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.[1] V_{CC} @ 2.0V	TYP.[1] V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$, $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	–	–	4000	TBD	µA
			COM'L.	–	–	–	1500	TBD	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–	–	–	–	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–	–	–	–	ns

NOTES:
1. $T_A = +25°C$
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

5

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

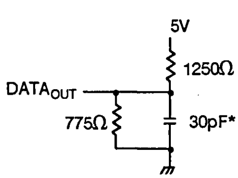


Figure 1. Output Load

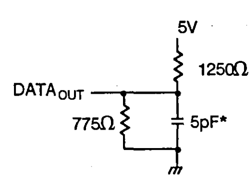


Figure 2. Output Load (for $t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}$)

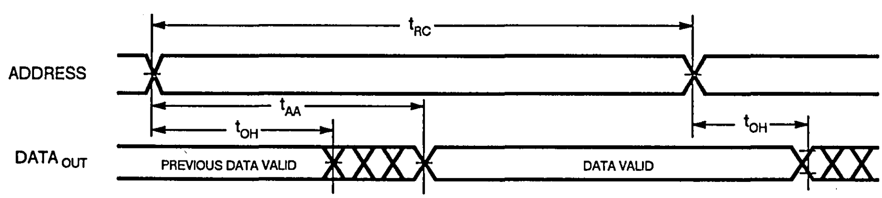
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

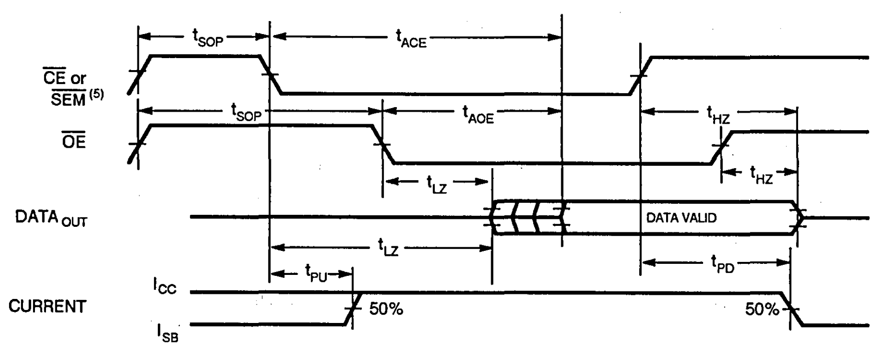
SYMBOL	PARAMETER	IDT71322S45 IDT71322L45 MIN.	MAX.	IDT71322S55 IDT71322L55 MIN.	MAX.	IDT71322S70 IDT71322L70 MIN.	MAX.	UNIT
READ CYCLE								
t_{RC}	Read Cycle Time	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	45	–	55	–	70	ns
t_{ACE}	Chip Enable Access Time (3)	–	45	–	55	–	70	ns
t_{AOE}	Output Enable Access Time	–	25	–	30	–	40	ns
t_{OH}	Output Hold From Address Change	5	–	5	–	5	–	ns
t_{LZ}	Output Low Z Time (1, 2)	5	–	5	–	5	–	ns
t_{HZ}	Output High Z Time (1, 2)	–	25	–	30	–	40	ns
t_{PU}	Chip Enable to Power Up Time (2)	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time (2)	–	50	–	50	–	50	ns
t_{SOP}	Sem Flg update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	–	20	–	20	–	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$
5. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$.

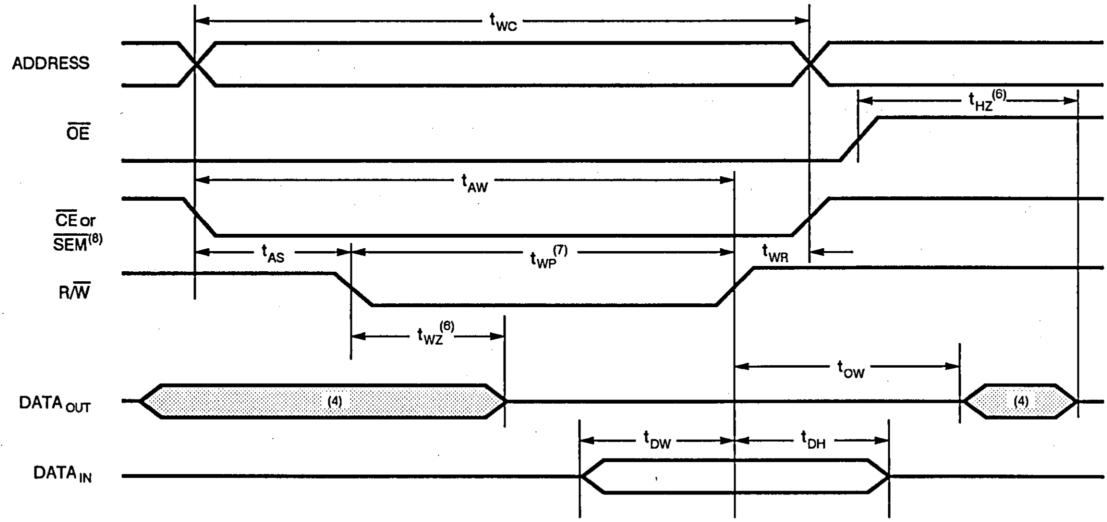
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	IDT71322S45 IDT71322L45 MIN.	MAX.	IDT71322S55 IDT71322L55 MIN.	MAX.	IDT71322S70 IDT71322L70 MIN.	MAX.	UNIT
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	–	55	–	70	–	ns
t_{EW}	Chip Enable to End of Write (3)	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	20	–	25	–	30	–	ns
t_{HZ}	Output High Z Time (1,2)	–	20	–	25	–	30	ns
t_{DH}	Data Hold Time	3	–	3	–	3	–	ns
t_{WZ}	Write Enabled to Output in High Z (1,2)	–	20	–	25	–	30	ns
t_{OW}	Output Active From End of Write (1,2)	0	–	0	–	0	–	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	–	10	–	10	–	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	–	10	–	10	–	ns

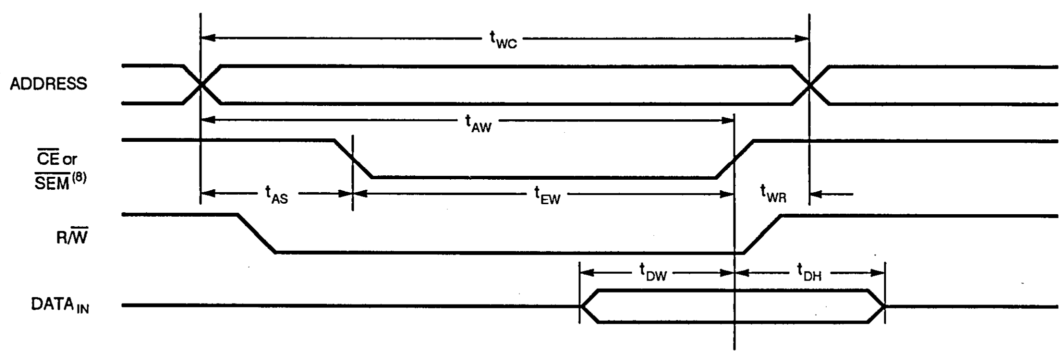
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$. Either condition must be valid for the entire t_{EW} time.

5

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING (1, 2, 3, 7)



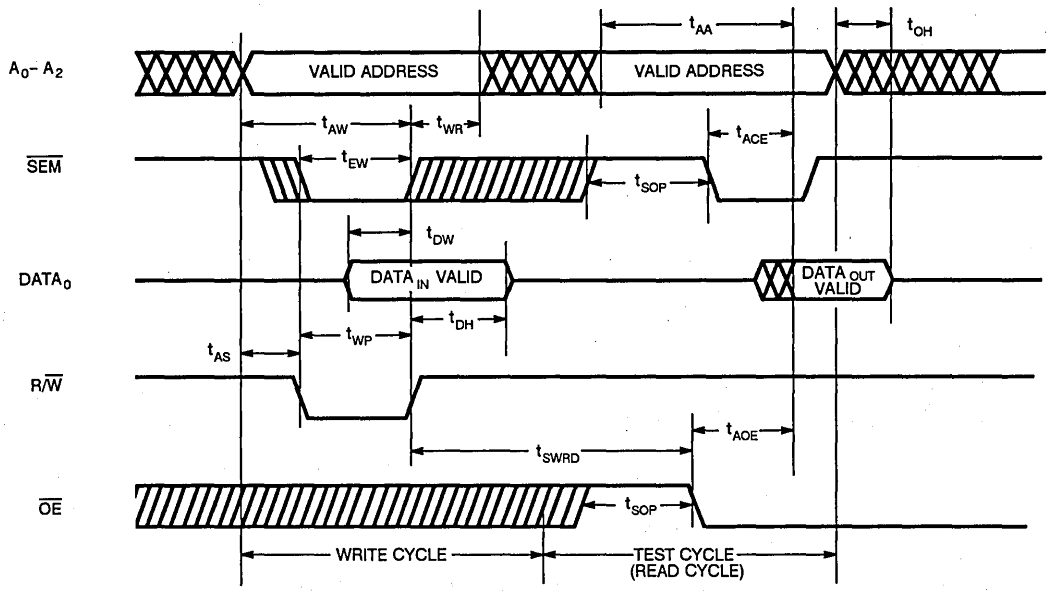
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING (1, 2, 3, 5, 9)



NOTES:

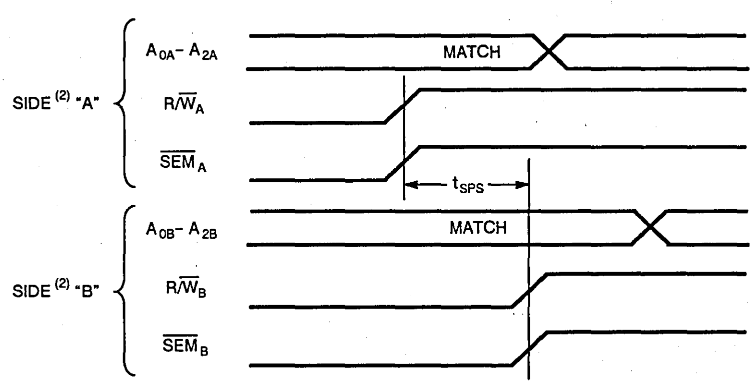
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ or $\overline{SEM}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
9. $\overline{OE}$ = V_{IL}

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE (1)



NOTE:
1. $\overline{CE} = V_{IH}$ for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE CONTENTION (1, 3, 4)



NOTES:
1. $D_{OR} = D_{OL} = V_{IL}$, $\overline{CE}_R = \overline{CE}_L = V_{IH}$. Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. Either side "A" = left and side "B" = right, or side "A" = right and side "B" = left.
3. This parameter is measured from the point where $R/\overline{W}_A$ or $\overline{SEM}_A$ goes high until $R/\overline{W}_B$ or $\overline{SEM}_B$ goes high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

5

FUNCTIONAL DESCRIPTION

The IDT71322 is an extremely fast dual-port 2K x 8 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Table I where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT71322 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT71322's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT71322 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor had set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT71322 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A_0 - A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other (see Table II). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence of WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as a one, a fact which the processor will verify by the subsequent read (see Table II). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during a subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 3. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

TABLE I—NON-CONTENTION READ/WRITE CONTROL

LEFT OR RIGHT PORT (1)					FUNCTION
$R/\overline{W}$	$\overline{CE}$	$\overline{SEM}$	$\overline{OE}$	D_{0-7}	
X	H	H	X	Z	Port Disabled and in Power Down Mode
H	H	L	L	$DATA_{OUT}$	Data in Semaphore Flag Output on Port
X	X	X	H	Z	Output Disabled
↑	H	L	X	$DATA_{IN}$	Port Data Bit D_0 Written Into Semaphore Flag
H	L	H	L	$DATA_{OUT}$	Data In Memory Output on Port
L	L	H	X	$DATA_{IN}$	Data On Port Written Into Memory
X	L	L	X	–	Not Allowed

NOTE:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
   H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE
   ↑ = Low-to-High transition

TABLE II—EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE (1)

FUNCTION	$D_0 - D_7$ LEFT	$D_0 - D_7$ RIGHT	STATUS
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT71322.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen. Code integrity is of the utmost importance when semaphores are used instead of slower, more restrictive hardware intensive schemes.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT71322's dual-port RAM. Say the 2K x 8 RAM was to be divided into two 1K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 1K of dual-port RAM, the processor on the left port could write and then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 1K. Meanwhile, the right processor would attempt to perform the same function. Since this processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 1K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 1K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices had determined which memory area was "off limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

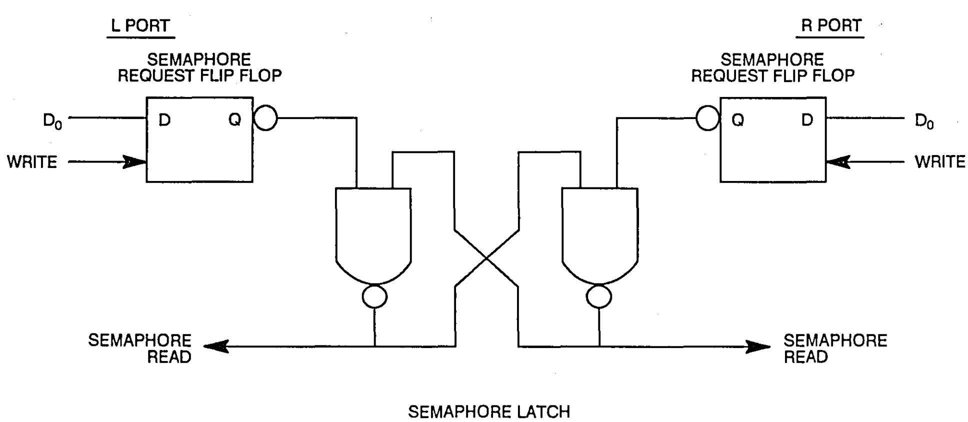


FIGURE 3. IDT71322 Semaphore Logic

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	P	Plastic DIP
	C	Sidebraze DIP
	J	Plastic Leaded Chip Carrier
	L	Leadless Chip Carrier
Speed	45 50 70	Speed in Nanoseconds
Power	L	Low Power
	S	Standard Power
Device Type	71322	16K (2K x 8-Bit) Dual-Port RAM w/Semaphore

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAMS 32K (2K x 16-BIT)

PRELIMINARY
IDT7133S/L
IDT7143S/L

FEATURES:

- High-speed access
  - Military: 70/90ns (max.)
  - Commercial: 55/70/90ns (max.)
- Low-power operation
  - IDT7133/43S
    Active: 375mW (typ.)
    Standby: 5mW (typ.)
  - IDT7133/43L
    Active: 375mW (typ.)
    Standby: 1mW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- On-chip port arbitration logic (IDT7133 only)
- $\overline{BUSY}$ output flag on IDT7133; $\overline{BUSY}$ input on IDT7143
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Available in 68-pin PGA, DIP (600 mil, 70 mil centers), LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7133/7143 are high-speed 2K x 16 dual-port static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7143 "SLAVE" dual-port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

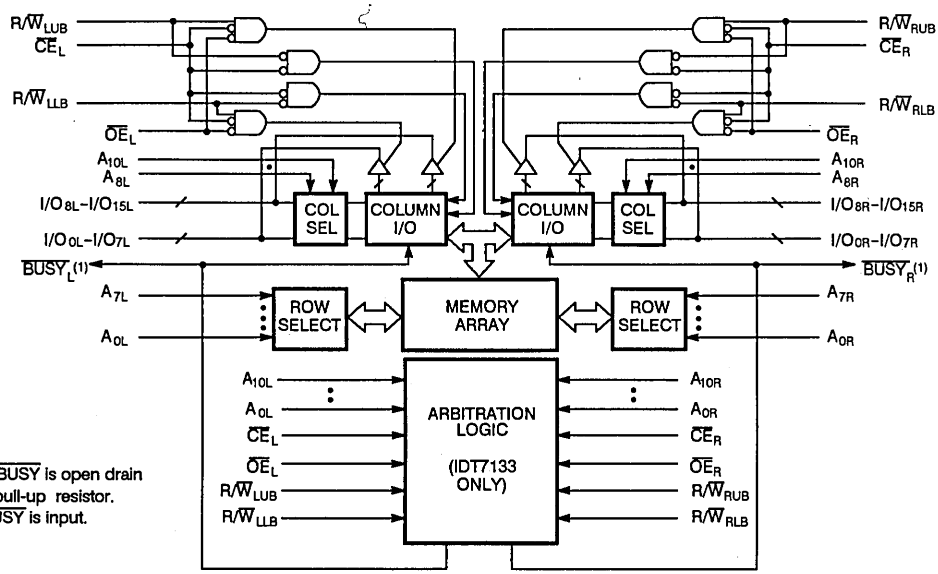
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 375mW of power at maximum access times as fast as 55ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 1mW from a 2V battery.

The IDT7133/7143 devices have identical pinouts. Each is packaged in a 68-pin PGA, 68-pin LCC, 68-pin PLCC, and 70 mil center DIPs.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

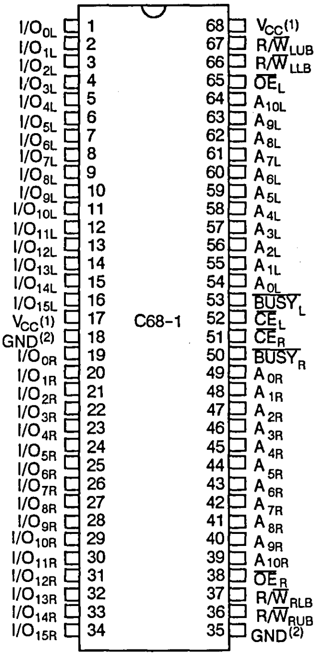


NOTES:

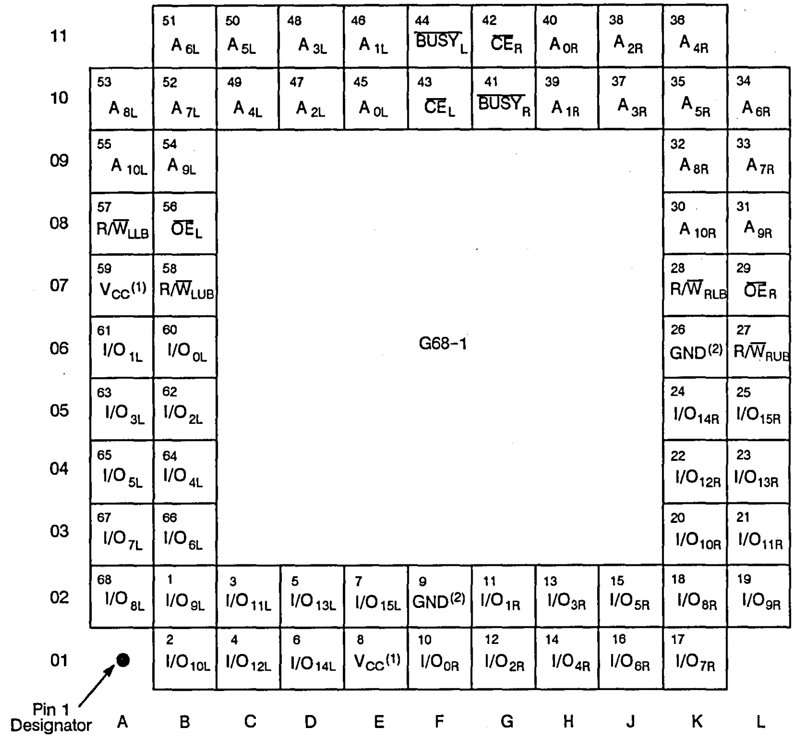
1. IDT7133 (MASTER): $\overline{BUSY}$ is open drain output and requires pull-up resistor. IDT7143 (SLAVE): $\overline{BUSY}$ is input.
2. LB = LOWER BYTE
   UB = UPPER BYTE

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



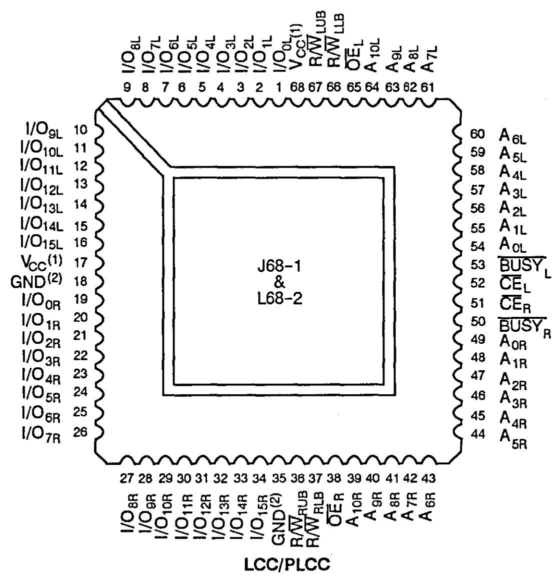
DIP
TOP VIEW



PGA TOP VIEW

NOTES:

1. Both V_{CC} pins must be connected to the supply to assure reliable operation.
2. Both GND pins must be connected to the supply to assure reliable operation.
3. UB = Upper Byte, LB = Lower Byte.



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	2.0	2.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Either port, V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7133S IDT7143S MIN.	IDT7133S IDT7143S MAX.	IDT7133L IDT7143L MIN.	IDT7133L IDT7143L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	μA
V_{OL}	Output Low Voltage (I/O_0 - I/O_{15})	I_{OL} = 4mA	–	0.4	–	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (4) (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		IDT7133x55 (1) IDT7143x55 (1) TYP.(2)	IDT7133x55 (1) IDT7143x55 (1) MAX.	IDT7133x70 IDT7143x70 TYP.(2)	IDT7133x70 IDT7143x70 MAX.	IDT7133x90 IDT7143x90 TYP.(2)	IDT7133x90 IDT7143x90 MAX.	UNIT
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX} (3)	MIL.	S	–	–	75	260	75	260	mA
				L	–	–	75	240	75	240	
			COM'L.	S	75	240	75	240	75	235	
				L	75	220	75	220	75	215	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH} f = f_{MAX} (3)	MIL.	S	–	–	25	75	25	75	mA
				L	–	–	25	65	25	65	
			COM'L.	S	25	70	25	70	25	65	
				L	25	60	25	60	25	55	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH} f = f_{MAX} (3) Active Port Outputs Open	MIL.	S	–	–	50	170	50	170	mA
				L	–	–	50	150	50	150	
			COM'L.	S	50	150	50	150	50	145	
				L	50	130	50	130	50	125	
I_{SB3}	Full Standby Current (Both Ports — CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V f = 0(3)	MIL.	S	–	–	1	30	1	30	mA
				L	–	–	0.2	10	0.2	10	
			COM'L.	S	1	15	1	15	1	15	
				L	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V f = f_{MAX} (3) Active Port Outputs Open	MIL.	S	–	–	45	160	45	155	mA
				L	–	–	40	140	40	135	
			COM'L.	S	45	140	45	140	45	135	
				L	40	120	40	120	40	115	

NOTES:
1. 0°C to +70°C temperature range only.
2. V_{CC} = 5V, T_A = +25°C
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. "x" in part numbers indicates power rating (S or L).

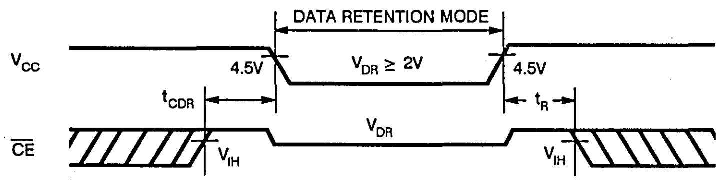
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES [1]

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		IDT7133S/L/IDT7143S/L MIN.	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V $\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		2.0	–	V
I_{CCDR}	Data Retention Current		MIL.	–	4000	µA
			COM'L.	–	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–	ns
I_{LI}[3]	Input Leakage Current			–	2	µA

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, & 3

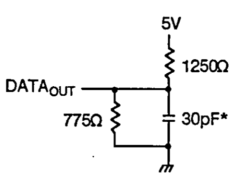


Figure 1. Output Load

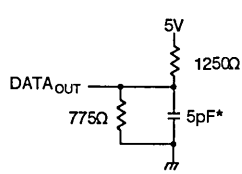


Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

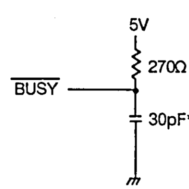


Figure 3. $\overline{BUSY}$ Output Load (IDT7133 only)

* Including scope and jig.

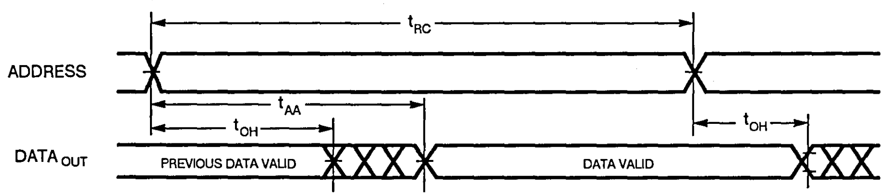
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

SYMBOL	PARAMETER	IDT7133S/L55 (2) IDT7143S/L55 (2) MIN.	MAX.	IDT7133S/L70 IDT7143S/L70 MIN.	MAX.	IDT7133S/L90 IDT7143S/L90 MIN.	MAX.	UNIT
READ CYCLE								
t_{RC}	Read Cycle Time	55	–	70	–	90	–	ns
t_{AA}	Address Access Time	–	55	–	70	–	90	ns
t_{ACE}	Chip Enable Access Time	–	55	–	70	–	90	ns
t_{AOE}	Output Enable Access Time	–	35	–	40	–	40	ns
t_{OH}	Output Hold From Address Change	0	–	0	–	10	–	ns
t_{LZ}	Output Low Z Time (1, 3)	5	–	5	–	5	–	ns
t_{HZ}	Output High Z Time (1, 3)	–	30	–	35	–	40	ns
t_{PU}	Chip Enable to Power Up Time (3)	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time (3)	–	50	–	50	–	50	ns

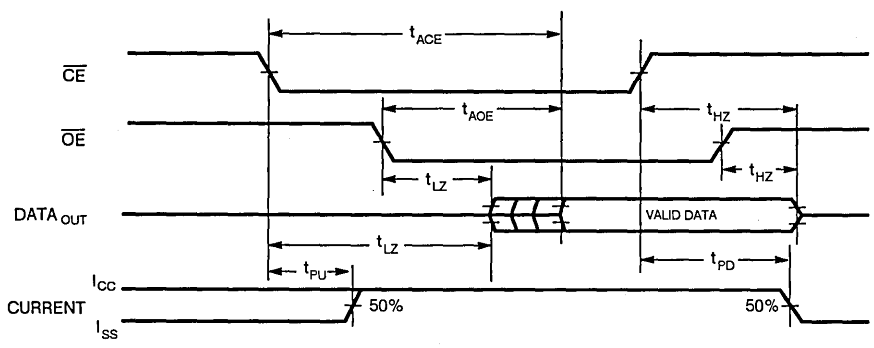
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (see Figures 1, 2 & 3).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed but not tested.

5

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)



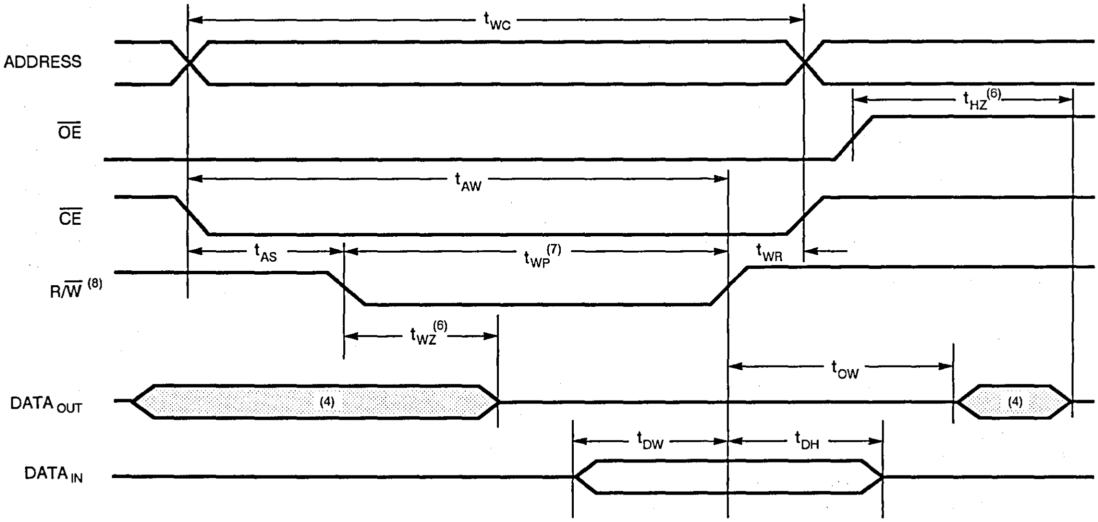
NOTES:
1. $R/\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

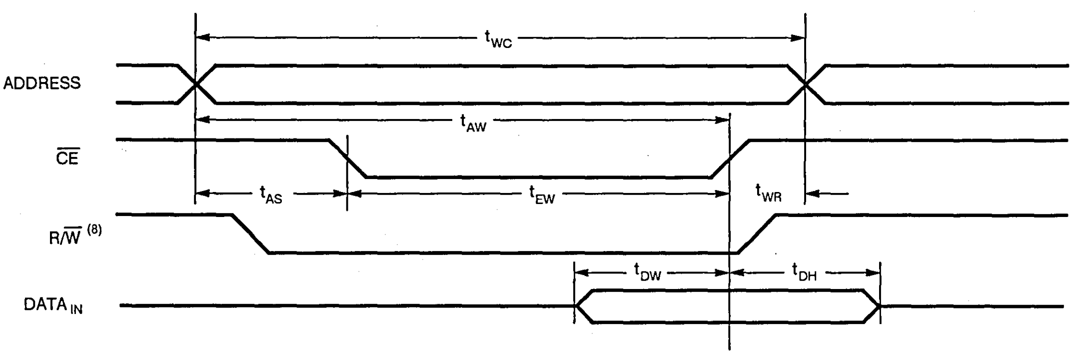
SYMBOL	PARAMETER	IDT7133S/L55 (2) IDT7143S/L55 (2) MIN.	MAX.	IDT7133S/L70 IDT7143S/L70 MIN.	MAX.	IDT7133S/L90 IDT7143S/L90 MIN.	MAX.	UNIT
WRITE CYCLE								
t_{WC}	Write Cycle Time(4)	55	–	70	–	90	–	ns
t_{EW}	Chip Enable to End of Write	40	–	50	–	85	–	ns
t_{AW}	Address Valid to End of Write	40	–	50	–	85	–	ns
t_{AS}	Address Setup Time	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	40	–	50	–	55	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	20	–	25	–	30	–	ns
t_{HZ}	Output High Z Time(1, 3)	–	20	–	25	–	25	ns
t_{DH}	Data Hold Time	5	–	5	–	5	–	ns
t_{WZ}	Write Enable to Output in High Z(1, 3)	–	20	–	25	–	25	ns
t_{OW}	Output Active From End of Write(1, 3)	0	–	0	–	0	–	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (see Figures 1, 2 & 3).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed but not tested.
4. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WR} + t_{WP}$.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($R/\overline{W}$ CONTROLLED TIMING) (1, 2, 3, 7)



WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:

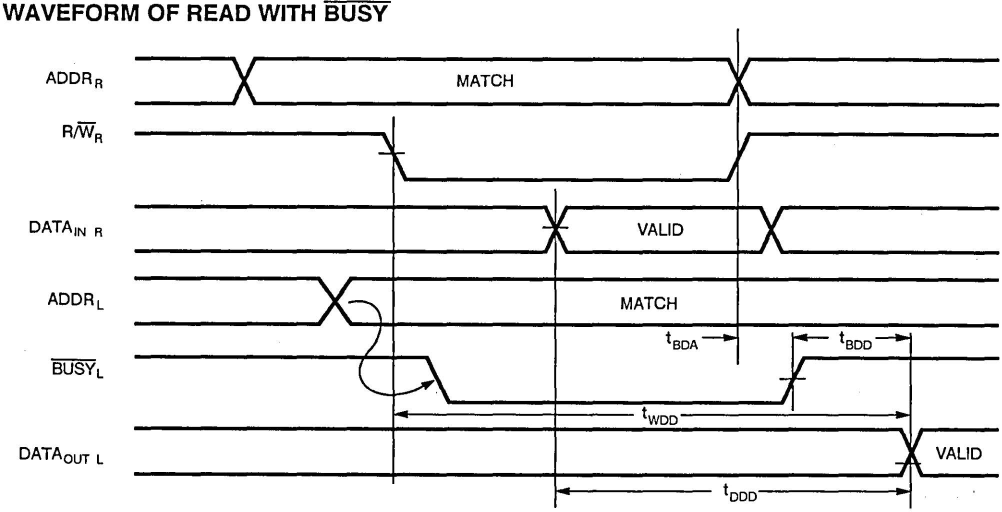
1. $R/\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low $R/\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or $R/\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the $R/\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a $R/\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an $R/\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. $R/\overline{W}$ for either upper or lower byte.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

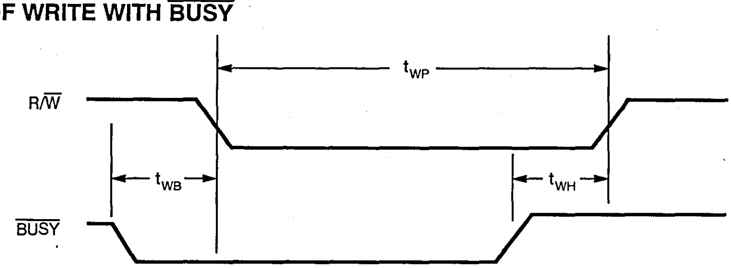
SYMBOL	PARAMETER	IDT7133S/L55 (2) IDT7143S/L55 (2) MIN.	MAX.	IDT7133S/L70 IDT7143S/L70 MIN.	MAX.	IDT7133S/L90 IDT7143S/L90 MIN.	MAX.	UNIT
BUSY TIMING								
t_{WB}	Write to $\overline{BUSY}$ (1, 5)	0	–	0	–	0	–	ns
t_{WH}	Write Hold After $\overline{BUSY}$ (1, 6)	30	–	30	–	30	–	ns
t_{BAA}	$\overline{BUSY}$ Access Time to Address	–	50	–	55	–	55	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	–	40	–	45	–	45	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	–	35	–	35	–	45	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	–	30	–	30	–	45	ns
t_{WDD}	Write Pulse to Data Delay (3)	–	80	–	90	–	100	ns
t_{DDD}	Write Data Valid to Read Data Delay (3)	–	55	–	70	–	90	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data (4)	–	Note 4	–	Note 4	–	Note 4	ns
t_{APS}	Arbitration Priority Set Up Time	5	–	5	–	10	–	ns

NOTES:
1. For SLAVE part (IDT7143) only.
2. 0°C to +70°C temperature range only.
3. Port to port delay through RAM cells from writing port to reading port.
4. t_{BDD} is calculated parameter and is greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$

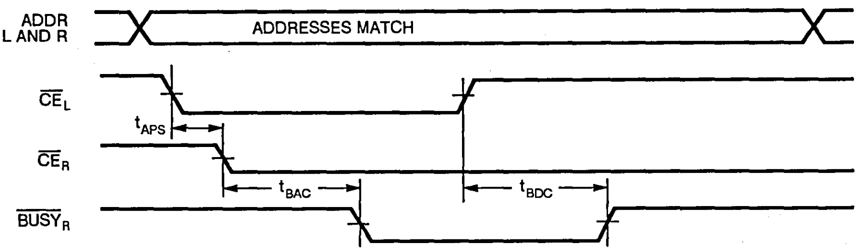


TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$

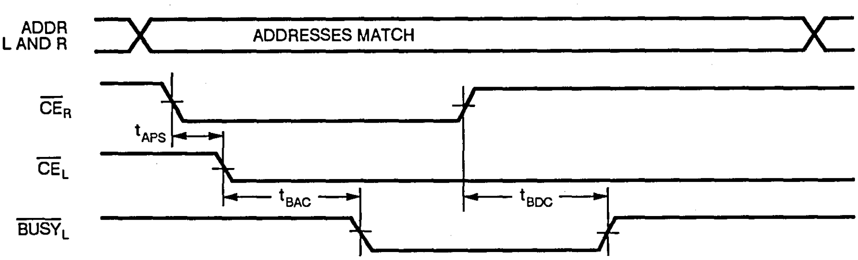


TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:



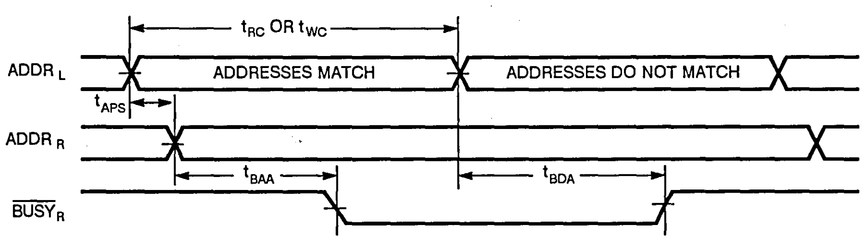
$\overline{CE}_R$ VALID FIRST:



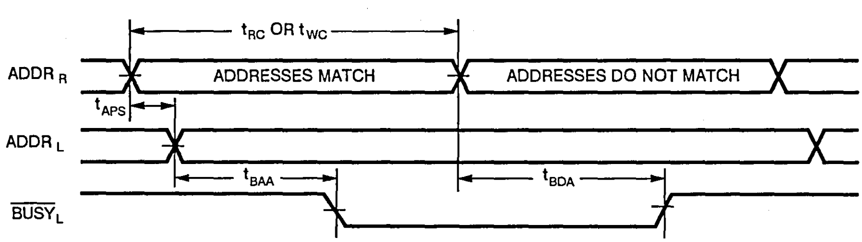
5

TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION [1]

LEFT ADDRESS VALID FIRST:



RIGHT ADDRESS VALID FIRST:



NOTE:
1. $\overline{CE}_L = CE_R = V_{IL}$

FUNCTIONAL DESCRIPTION:

The IDT7133/43 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to 32 bits or more in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TABLE I—NON-CONTENTION READ/WRITE CONTROL[4]

LEFT OR RIGHT PORT (1)						FUNCTION
$R/\overline{W}_{LB}$	$R/\overline{W}_{UB}$	$\overline{CE}$	$\overline{OE}$	I/O_{0-7}	I/O_{8-15}	
X	X	H	X	Z	Z	Port Disabled and in Power Down mode, I_{SB2} or I_{SB4}
X	X	H	X	Z	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	L	X	$DATA_{IN}$	$DATA_{IN}$	Data on Lower Byte and Upper Byte Written into Memory[2]
L	H	L	L	$DATA_{IN}$	$DATA_{OUT}$	Data on Lower Byte Written into Memory,[2] Data in Memory Output on Upper Byte[3]
H	L	L	L	$DATA_{OUT}$	$DATA_{IN}$	Data in Memory Output on Lower Byte,[3] Data on Upper Byte Written into Memory[2]
L	H	L	H	$DATA_{IN}$	Z	Data on Lower Byte Written into Memory[2]
H	L	L	H	Z	$DATA_{IN}$	Data on Upper Byte Written into Memory[2]
H	H	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Data in Memory Output on Lower Byte and Upper Byte[3]
H	H	L	H	Z	Z	High Impedance Outputs

NOTES:

1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = High, L = Low, X = Don't Care, Z = High Impedance, LB = Lower Byte, UB = Upper Byte

TABLE II — ARBITRATION

LEFT PORT		RIGHT PORT		FLAGS(1)		FUNCTION
$\overline{CE}_L$	$A_{0L}-A_{10L}$	$\overline{CE}_R$	$A_{0R}-A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R}-A_{10R}$	L	$\neq A_{0L}-A_{10L}$	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL5R	$= A_{0R}-A_{10R}$	LL5R	$= A_{0L}-A_{10L}$	H	L	L-Port Wins
RL5L	$= A_{0R}-A_{10R}$	RL5L	$= A_{0L}-A_{10L}$	L	H	R-Port Wins
LW5R	$= A_{0R}-A_{10R}$	LW5R	$= A_{0L}-A_{10L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R}-A_{10R}$	LW5R	$= A_{0L}-A_{10L}$	L	H	Arbitration Resolved

NOTE:
1. X = Don't Care, L = Low, H = High
   LV5R = Left Address Valid $\geq$ 5ns before right address
   RV5L = Right Address Valid $\geq$ 5ns before left address
   Same = Left and Right Address match within 5ns of each other
   LL5R = Left $\overline{CE}$ = LOW $\geq$ 5ns before Right $\overline{CE}$
   RL5L = Right $\overline{CE}$ = LOW $\geq$ 5ns before Left $\overline{CE}$
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other

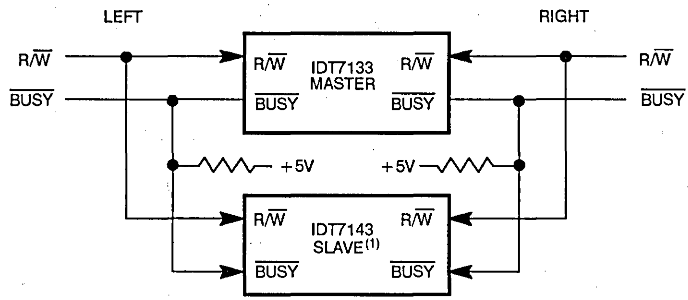
5

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Input/Output Capacitance	$V_{I/O}$ = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

32-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:

1. No arbitration in IDT7143 (SLAVE). $\overline{\text{BUSY}}$-IN inhibits write in IDT7143 (SLAVE).

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	XC	Sidebraze Shrink-DIP
	J	Plastic Leaded Chip Carrier
	L	Leadless Chip Carrier
	G	Pin Grid Array
Speed	55	Commercial Only — Speed in Nanoseconds
	70	Speed in Nanoseconds
	90	Speed in Nanoseconds
Power	L	Low Power
	S	Standard Power
Device Type	7133	32K (2K x 16-Bit) MASTER Dual-Port RAM
	7143	32K (2K x 16-Bit) SLAVE Dual-Port RAM

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT)

PRELIMINARY
IDT7134S
IDT7134L

FEATURES:

- High-speed access
  - Military: 45/55/70ns (max.)
  - Commercial: 45/55/70ns (max.)
- Low-power operation
  - IDT7134S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT7134L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

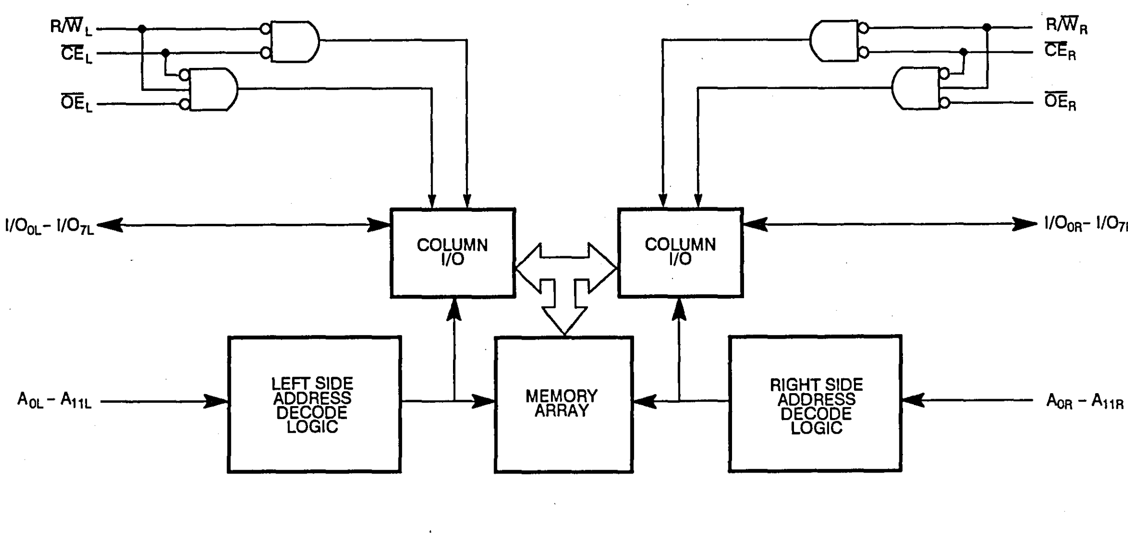
The IDT7134 is an extremely high-speed 4K x 8 dual-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same dual-port RAM location.

The IDT7134 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these dual-ports typically operate on only 500mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery.

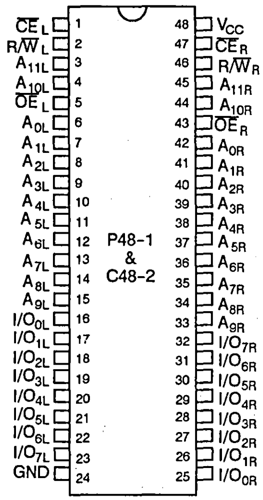
The IDT7134 is packaged in either a sidebraze or plastic 48-pin DIP and 52-pin LCC and PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

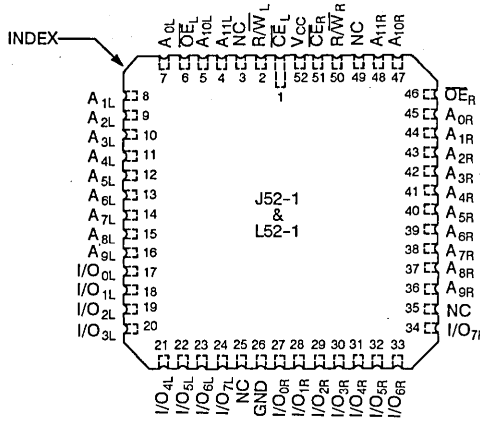


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7134S MIN.	IDT7134S MAX.	IDT7134L MIN.	IDT7134L MAX.	UNIT
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA	–	0.4	–	0.4	V
		I_{OL} = 8mA	–	0.5	–	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (1) (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		IDT7134x45 TYP.(2)	IDT7134x45 MAX.	IDT7134x55 TYP.(2)	IDT7134x55 MAX.	IDT7134x70 TYP.(2)	IDT7134x70 MAX.	UNIT
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}(3)	MIL.	S	100	240	100	230	100	230	mA
				L	100	200	100	180	100	180	
			COM'L.	S	100	200	100	200	100	200	
				L	100	160	100	160	100	160	
I_{SB1}	Standby Current (Both Ports – TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH} f = f_{MAX}(3)	MIL.	S	25	70	25	70	25	70	mA
				L	25	50	25	50	25	50	
			COM'L.	S	25	70	25	70	25	70	
				L	25	40	25	40	25	40	
I_{SB2}	Standby Current (One Port – TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}(3)	MIL.	S	50	160	50	150	50	150	mA
				L	50	130	50	120	50	120	
			COM'L.	S	50	130	50	130	50	130	
				L	50	100	50	100	50	100	
I_{SB3}	Full Standby Current (Both Ports – All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, f = 0(3)	MIL.	S	1.0	30	1.0	30	1.0	30	mA
				L	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	1.0	15	
				L	0.2	4.0	0.2	4.0	0.2	4.0	
I_{SB4}	Full Standby Current (One Port – All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC}-0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}(3)	MIL.	S	50	130	50	120	50	120	mA
				L	45	100	45	90	45	90	
			COM'L.	S	45	110	50	110	50	110	
				L	45	90	45	90	45	90	

NOTES:

1. "x" in part number indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C
3. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standy I_{SB3}.

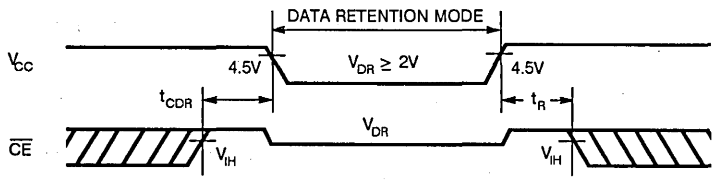
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP. V_{CC} @ 2.0V	TYP. V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention			2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	–	–	4000	TBD	μA
			COM'L.	–	–	–	1500	TBD	μA
$t_{CDR}^{(3)}$	Chip Deselect to Data Retention Time			0	–	–	–	–	ns
$t_R^{(3)}$	Operation Recovery Time			$t_{RC}^{(2)}$	–	–	–	–	ns

NOTES:
1. $V_{CC} = 2V$, $T_A = +25°C$
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

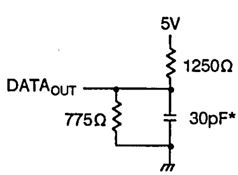


Figure 1. Output Load

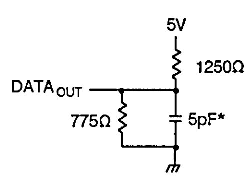


Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

*Including scope and jig.

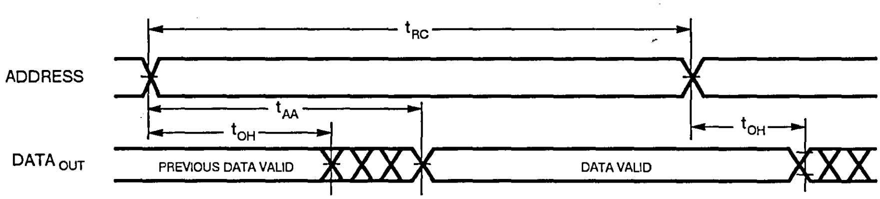
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

SYMBOL	PARAMETER	IDT7134S45 IDT7134L45 MIN.	MAX.	IDT7134S55 IDT7134L55 MIN.	MAX.	IDT7134S70 IDT7134L70 MIN.	MAX.	UNIT
READ CYCLE								
t_{RC}	Read Cycle Time	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	45	–	55	–	70	ns
t_{ACE}	Chip Enable Access Time	–	45	–	55	–	70	ns
t_{AOE}	Output Enable Access Time	–	25	–	30	–	40	ns
t_{OH}	Output Hold From Address Change	5	–	5	–	5	–	ns
t_{LZ}	Output Low Z Time(1, 2)	5	–	5	–	5	–	ns
t_{HZ}	Output High Z Time(1, 2)	–	25	–	30	–	40	ns
t_{PU}	Chip Enable to Power Up Time(2)	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time(2)	–	50	–	50	–	50	ns

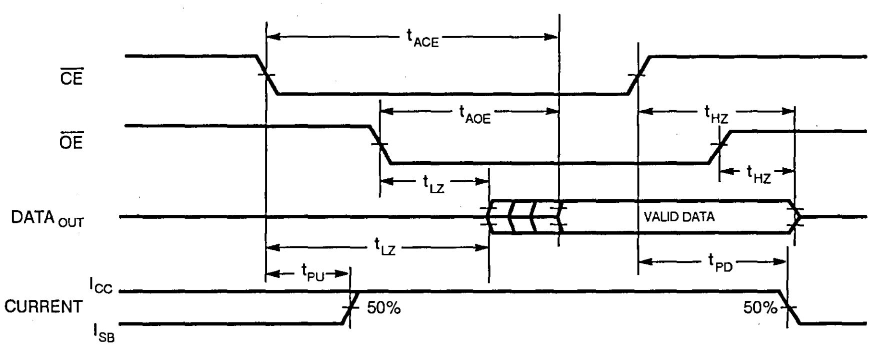
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.

5

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)



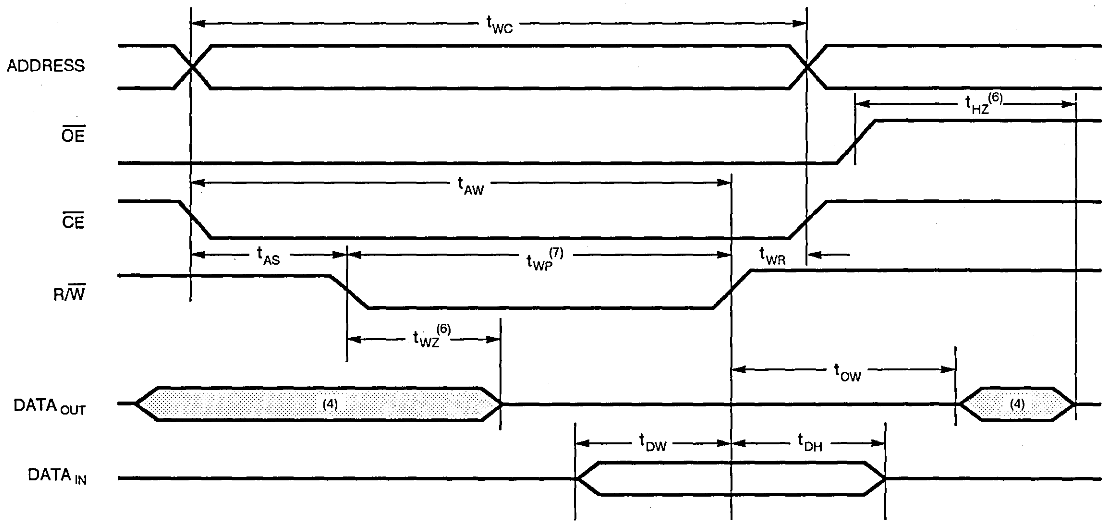
NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

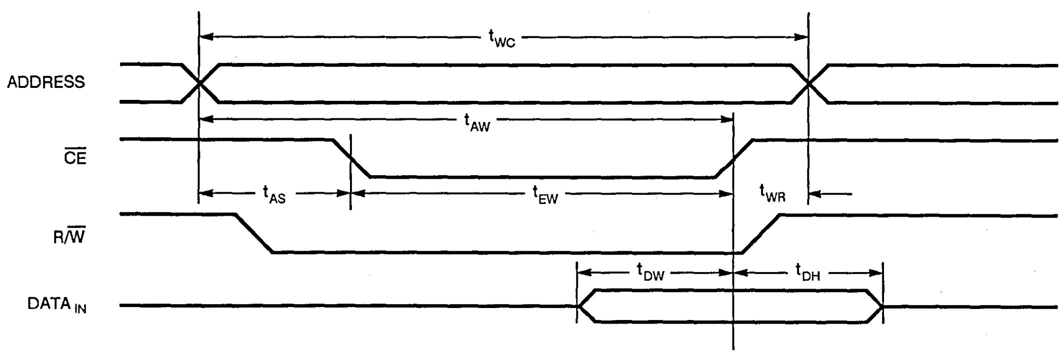
SYMBOL	PARAMETER	IDT7134S45 IDT7134L45 MIN.	MAX.	IDT7134S55 IDT7134L55 MIN.	MAX.	IDT7134S70 IDT7134L70 MIN.	MAX.	UNIT
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	–	55	–	70	–	ns
t_{EW}	Chip Enable to End of Write	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	20	–	25	–	30	–	ns
t_{HZ}	Output High Z Time(1,2)	–	20	–	25	–	30	ns
t_{DH}	Data Hold Time	3	–	3	–	3	–	ns
t_{WZ}	Write Enabled to Output in High Z (1,2)	–	20	–	25	–	30	ns
t_{OW}	Output Active From End of Write(1,2)	0	–	0	–	0	–	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{\text{W}}$ CONTROLLED TIMING (1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{\text{CE}}$ CONTROLLED TIMING (1, 2, 3, 5)



NOTES:

1. R/$\overline{\text{W}}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{\text{CE}}$ and a low R/$\overline{\text{W}}$.
3. t_{WR} is measured from the earlier of $\overline{\text{CE}}$ or R/$\overline{\text{W}}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{\text{CE}}$ low transition occurs simultaneously with or after the R/$\overline{\text{W}}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{\text{OE}}$ is low during a R/$\overline{\text{W}}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{\text{OE}}$ is high during an R/$\overline{\text{W}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

FUNCTIONAL DESCRIPTION:

The IDT7134 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in the table below.

TABLE I—NON-CONTENTION READ/WRITE CONTROL

LEFT OR RIGHT PORT [1]				FUNCTION
$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L =$ H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port
X	X	H	Z	High Impedance Outputs

NOTE:
1. $A_{0L} - A_{11L} \neq A_{0R} - A_{11R}$
H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	P	Plastic DIP
	C	Sidebraze DIP
	J	PLCC
	L	LCC
Speed	45 55 70	Speed in Nanoseconds
Power	L	Low Power
	S	Standard Power
Device Type	7134	32K (4K x 8-Bit) Dual-Port RAM

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT) WITH SEMAPHORE

IDT71342S
IDT71342L

FEATURES:

- High-speed access
  - Military: 45/55/70ns (max.)
  - Commercial: 45/55/70ns (max.)
- Low-power operation
  - IDT71342S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT71342L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation—2V data retention
- TTL-compatible; single +5V(±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71342 is an extremely high-speed 4K x 8 dual-port static RAM with full on-chip hardware support of semaphore signalling between the two ports.

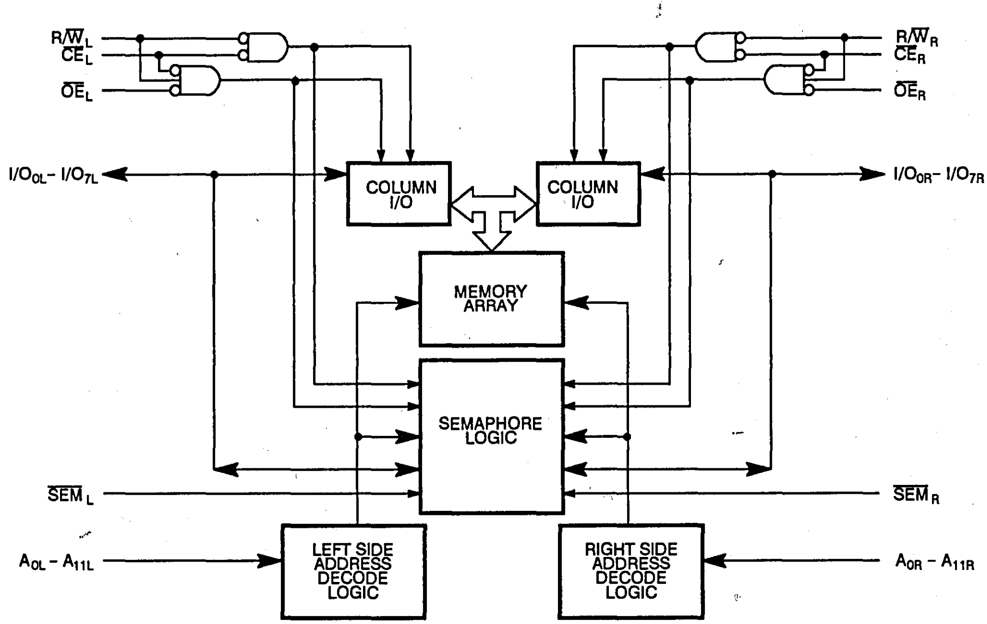
The IDT71342 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in memory. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. This block contains unassigned flags which can be accessed by either side; however, only one side can control the flag at any time. An automatic power down feature, controlled by $\overline{CE}$ and $\overline{SEM}$, permits the on-chip circuitry of each port to enter a very low standby power mode (both $\overline{CE}$ and $\overline{SEM}$ high).

Fabricated using IDT's CEMOS™ high-performance technology this device typically operates on only 500mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200μW from a 2V battery. The device is packaged in either a hermetic 52-pin leadless chip carrier or a 52-pin PLCC.

The IDT71342 military devices are manufactured in compliance with the latest revision of MIL-STD-883, Class B.

5

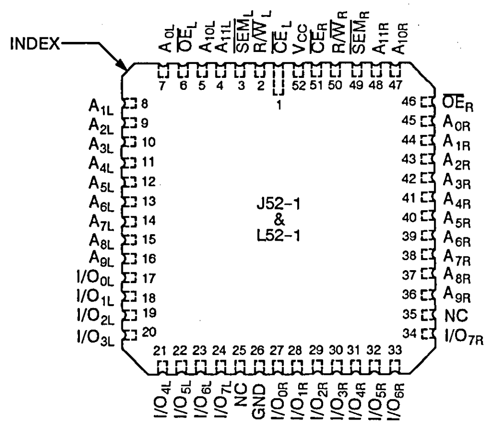
FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

PIN CONFIGURATION



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER [1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT71342S MIN.	IDT71342S MAX.	IDT71342L MIN.	IDT71342L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA	–	0.4	–	0.4	V
		I_{OL} = 8mA	–	0.5	–	0.5	
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (1) (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		IDT71342x45 TYP.(2)	IDT71342x45 MAX.	IDT71342x55 TYP.(2)	IDT71342x55 MAX.	IDT71342x70 TYP.(2)	IDT71342x70 MAX.	UNIT
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open $\overline{SEM}$ = Don't Care f = f_{MAX}(3)	MIL.	S	100	240	100	230	100	230	mA
				L	100	200	100	180	100	180	
			COM'L.	S	170	200	100	200	100	200	
				L	100	160	100	160	100	160	
I_{CC1}	Dynamic Operating Current (Semaphores Both Sides)	$\overline{CE}$ = V_{IH} $\overline{SEM}$ = V_{IL} Outputs Open f = f_{MAX}(3)	MIL.	S	85	130	85	130	85	130	mA
				L	85	110	85	110	85	110	
			COM'L.	S	85	130	85	130	85	130	
				L	85	100	85	100	85	100	
I_{SB1}	Standby Current (Both Ports–TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH} $\overline{SEM}_L$ = $\overline{SEM}_R$ ≥ V_{IH} f = f_{MAX}(3)	MIL.	S	25	70	25	70	25	70	mA
				L	25	50	25	50	25	50	
			COM'L.	S	25	70	25	70	25	70	
				L	25	40	25	40	25	40	
I_{SB2}	Standby Current (One Port–TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}(3) $\overline{SEM}_L$ = $\overline{SEM}_R$ ≥ V_{IH}	MIL.	S	50	160	50	150	50	150	mA
				L	50	130	50	120	50	120	
			COM'L.	S	50	130	50	130	50	130	
				L	50	100	50	100	50	100	
I_{SB3}	Full Standby Current (Both Ports– All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V $\overline{SEM}_L$ = $\overline{SEM}_R$ ≥ V_{CC} -0.2V, f = 0(3)	MIL.	S	1.0	30	1.0	30	1.0	30	mA
				L	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	1.0	15	
				L	0.2	4.0	0.2	4.0	0.2	4.0	
I_{SB4}	Full Standby Current (One Port–All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}(3)	MIL.	S	50	130	50	120	50	120	mA
				L	45	100	45	90	45	90	
			COM'L.	S	45	110	50	110	50	110	
				L	45	90	45	90	45	90	

NOTES:

1. "x" in part numbers indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C
3. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby, I_{SB3}.

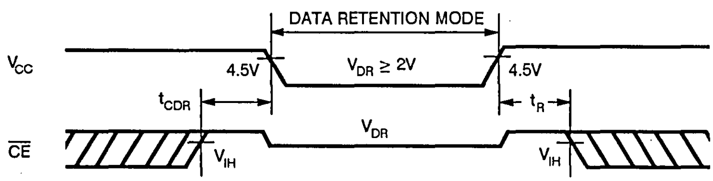
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP. V_{CC} @ 2.0V	TYP. V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$, $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	–	–	4000	TBD	µA
			COM'L.	–	–	–	4000	TBD	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–	–	–	–	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–	–	–	–	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

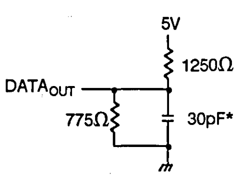


Figure 1. Output Load

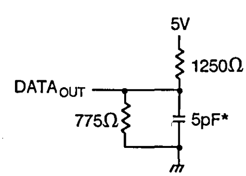


Figure 2. Output Load
(for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

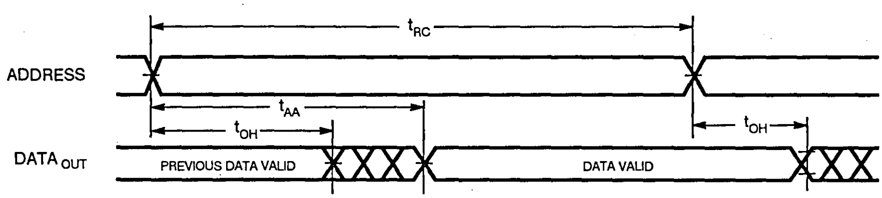
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

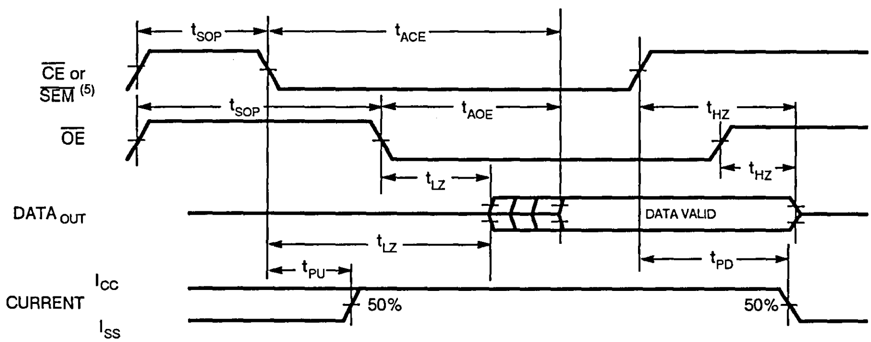
SYMBOL	PARAMETER	IDT71342S45 IDT71342L45 MIN.	MAX.	IDT71342S55 IDT71342L55 MIN.	MAX.	IDT71342S70 IDT71342L70 MIN.	MAX.	UNIT
READ CYCLE								
t_{RC}	Read Cycle Time	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	45	–	55	–	70	ns
t_{ACE}	Chip Enable Access Time (3)	–	45	–	55	–	70	ns
t_{AOE}	Output Enable Access Time	–	25	–	30	–	40	ns
t_{OH}	Output Hold From Address Change	5	–	5	–	5	–	ns
t_{LZ}	Output Low Z Time (1, 2)	5	–	5	–	5	–	ns
t_{HZ}	Output High Z Time (1, 2)	–	25	–	30	–	40	ns
t_{PU}	Chip Enable to Power Up Time (2)	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time (2)	–	50	–	50	–	50	ns
t_{SOP}	Sem Flg update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	–	20	–	20	–	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)



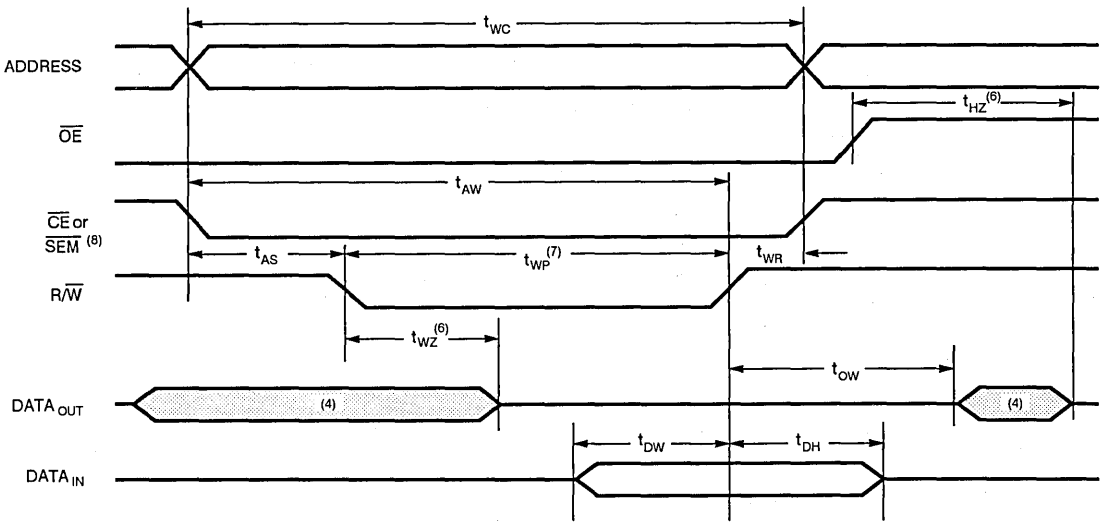
NOTES:
1. $R/\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$
5. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

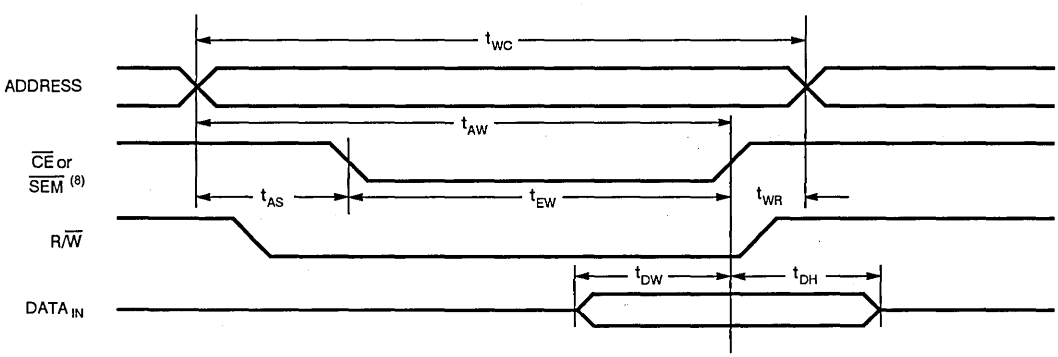
SYMBOL	PARAMETER	IDT71342S45 IDT71342L45 MIN.	MAX.	IDT71342S55 IDT71342L55 MIN.	MAX.	IDT71342S70 IDT71342L70 MIN.	MAX.	UNIT
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	–	55	–	70	–	ns
t_{EW}	Chip Enable to End of Write (3)	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	20	–	25	–	30	–	ns
t_{HZ}	Output High Z Time (1,2)	–	20	–	25	–	30	ns
t_{DH}	Data Hold Time	3	–	3	–	3	–	ns
t_{WZ}	Write Enable to Output in High Z (1,2)	–	20	–	25	–	30	ns
t_{OW}	Output Active From End of Write (1,2)	0	–	0	–	0	–	ns
t_{SWR}	$\overline{SEM}$ Flag Write to Read Time	10	–	10	–	10	–	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	–	10	–	10	–	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$. This condition must be valid for entire t_{EW} time.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, $R/\overline{W}$ CONTROLLED TIMING (1, 2, 3, 7)



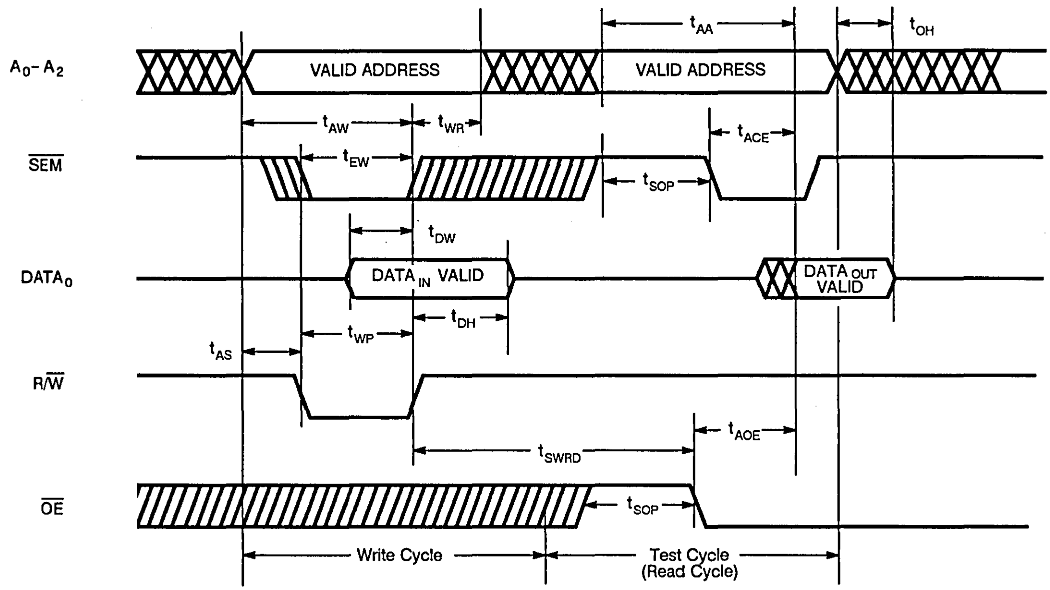
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING (1, 2, 3, 5, 9)



NOTES:

1. $R/\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ or $\overline{SEM}$ and a low $R/\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or $R/\overline{W}$ (or $\overline{SEM}$ or $R/\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the $R/\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a $R/\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an $R/\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
9. $\overline{OE}$ = V_{IL}

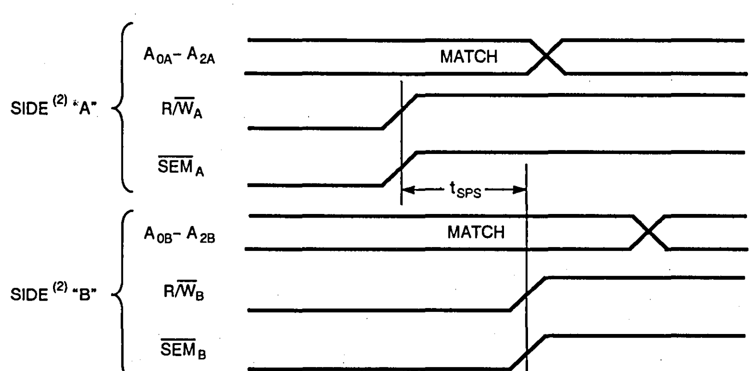
TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE (1)



NOTE:

1. $\overline{CE} = V_{IH}$ for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE CONTENTION (1, 3, 4)



NOTES:

1. $D_{OR} = D_{OL} = V_{IL}$, $\overline{CE}_R = \overline{CE}_L = V_{IH}$, semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. Either side "A" = left and side "B" = right, or side "A" = right and side "B" = left.
3. This parameter is measured from the point where $R/\overline{W}_A$ or $\overline{SEM}_A$ goes high until $R/\overline{W}_B$ or $\overline{SEM}_B$ goes high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

FUNCTIONAL DESCRIPTION

The IDT71342 is an extremely fast dual-port 4K x 8 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAMs and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Table I where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT71342 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT71342's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT71342 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor had set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT71342 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A_0 - A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other (see Table II). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence of WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as a one, a fact which the processor will verify by the subsequent read (see Table II). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during a subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 3. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

TABLE I – NON-CONTENTION READ/WRITE CONTROL

LEFT OR RIGHT PORT (1)					FUNCTION
$R/\overline{W}$	$\overline{CE}$	$\overline{SEM}$	$\overline{OE}$	D_{0-7}	
X	H	H	X	Z	Port Disabled and in Power Down Mode
H	H	L	L	$DATA_{OUT}$	Data in Semaphore Flag Output on Port
X	X	X	H	Z	Output Disabled
_⌠‾	H	L	X	$DATA_{IN}$	Port Data Bit D_0 Written Into Semaphore Flag
H	L	H	L	$DATA_{OUT}$	Data In Memory Output on Port
L	L	H	X	$DATA_{IN}$	Data On Port Written Into Memory
X	L	L	X	–	Not Allowed

NOTE:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
   H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE
   _⌠‾ = Low-to-High transition

TABLE II – EXAMPLE SEMAPHORE PROCUREMENT SEQUENCE

FUNCTION	$D_0 - D_7$ LEFT	$D_0 - D_7$ RIGHT	STATUS
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT71342.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen. Code integrity is of the utmost importance when semaphores are used instead of slower, more restrictive hardware intensive schemes.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT71342's dual-port RAM. Say the 4K x 8 RAM was to be divided into two 2K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 2K of dual-port RAM, the processor on the left port could write and then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 2K. Meanwhile, the right processor would attempt to perform the same function. Since this processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 2K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 2K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices had determined which memory area was "off limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

5

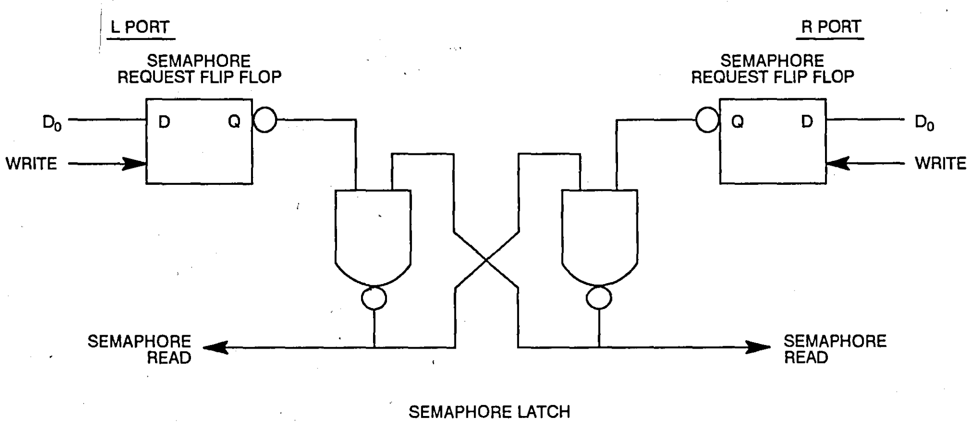


FIGURE 3. IDT71342 Semaphore Logic

ORDERING INFORMATION

IDT XXXX A 999 A A

- XXXX: Device Type
- A: Power
- 999: Speed
- A: Package
- A: Process/ Temperature Range

Field	Code	Description
Process/ Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	J	PLCC
	L	LCC
Speed	45 55 70	Speed in Nanoseconds
Power	L	Low Power
	S	Standard Power
Device Type	71342	32K (4K x 8-Bit) Dual-Port RAM w/Semaphore

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM MODULE 64K (8K x 8-BIT) & 128K (16K x 8-BIT)

IDT7M134S
IDT7M135S

FEATURES:

- High-density 64K/128K-bit CMOS dual-port RAM modules
- 16K x 8 organization (IDT7M135) with 8K x 8 option (IDT7M134)
- Low power consumption
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- On-chip port arbitration logic
- $\overline{\text{BUSY}}$ flags
- Fully asynchronous operation from either port
- Single 5V (±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- On-chip pull up resistors for open-drain $\overline{\text{BUSY}}$ flag option
- Inputs and outputs directly TTL-compatible
- Fully static operation
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT7M134/135 are 64K/128K-bit high-speed CMOS dual-port static RAM modules constructed on a multi-layered ceramic substrate using four IDT7132 2K x 8 dual-port RAMs (IDT7M134) or eight IDT7132 dual-port RAMs (IDT7M135) in leadless chip carriers. Dual-port function is achieved by utilization of the two on-board IDT54/74FCT138 decoder circuits that interpret the higher order addresses A_{L11-13} and A_{R11-13} to select one of the eight 2K x 8 dual-port RAMs. (On IDT7M134 8K x 8 option, the A_{L13} and A_{R13} need to be externally grounded and the selection becomes one of the four 2K x 8 dual-port RAMs.) Extremely high speeds are achieved in this fashion due to the use of the IDT7132 dual-port RAM, fabricated in IDT's high-performance CEMOS technology.

The IDT7M134/135 provide two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in the memory. The $\overline{\text{BUSY}}$ flags are provided for the situation when both ports simultaneously access the same memory location. The on-chip arbitration logic will determine which port has access and sets the $\overline{\text{BUSY}}$ flag of the delayed port. $\overline{\text{BUSY}}$ is set at speeds that permit the processor to hold the operation and its respective address and data. The delayed port will have access when $\overline{\text{BUSY}}$ goes high (inactive).

The IDT7M134/135 are available with access times as fast as 45ns commercial and 60ns military temperature range, with operating power consumption of only 2.1W/3.5W (max.). The module also offers a standby power mode of 1.4W/2.8W (max.) and a full standby mode of 660mW/1.3W (max.).

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

5

PIN CONFIGURATION

Signal	Pin	Pin	Signal
GND(1)	1	58	V_{CC}(1)
$\overline{CE}_L$	2	57	$\overline{CE}_R$
$R/\overline{W}_L$	3	56	$R/\overline{W}_R$
$R330_L$	4	55	$R330_R$
$\overline{BUSY}_L$	5	54	$BUSY_R$
$\overline{OE}_L$	6	53	$\overline{OE}_R$
A_{0L}	7	52	A_{0R}
A_{1L}	8	51	A_{1R}
A_{2L}	9	50	A_{2R}
A_{3L}	10	49	A_{3R}
A_{4L}	11	48	A_{4R}
A_{5L}	12	47	A_{5R}
A_{6L}	13	46	A_{6R}
A_{7L}	14	45	A_{7R}
A_{8L}	15	44	A_{8R}
A_{9L}	16	43	A_{9R}
A_{10L}	17	42	A_{10R}
A_{11L}	18	41	A_{11R}
A_{12L}	19	40	A_{12R}
A_{13L}(2)	20	39	A_{13}(2)
I/O_{0L}	21	38	I/O_{0R}
I/O_{1L}	22	37	I/O_{1R}
I/O_{2L}	23	36	I/O_{2R}
I/O_{3L}	24	35	I/O_{3R}
I/O_{4L}	25	34	I/O_{4R}
I/O_{5L}	26	33	I/O_{5R}
I/O_{6L}	27	32	I/O_{6R}
I/O_{7L}	28	31	I/O_{7R}
GND(1)	29	30	V_{CC}(1)

M7(3)

DIP
TOP VIEW

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$\overline{BUSY}_L$	$\overline{BUSY}_R$	$\overline{\text{BUSY}}$ Flag (Open Drain)
$R330_L$	$R330_R$	PULL-UP Resistors for Open-drain $\overline{\text{BUSY}}$ Flag option
A_{0L} - A_{13L}	A_{0R} - A_{13R}	Address
I/O_{0L} - IO_{7L}	I/O_{0R} - I/O_{7R}	Data Input/Output
V_{CC}		Power
GND		Ground

NOTES:
1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. On 8K x 8 IDT7M134 option A_{13L} and A_{13R} need to be externally connected to ground for proper operation.
3. For module dimensions, please refer to module drawing M7 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-7023/-

Integrated Device Technology, Inc.

256K (32K x 8-BIT) DUAL-PORT CMOS STATIC RAM MODULE

IDT7M137

FEATURES:

- High-density 256K-bit CMOS dual-port RAM module
- 32K x 8 organization
- Low power consumption
- CEMOS ™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Battery backup operation—2V data retention
- Fully asynchronous operation from either port
- Single 5V(±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Fully static operation
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M137 is a 256K-bit high-speed CMOS dual-port static RAM module constructed on a multi-layered ceramic substrate using eight IDT7134 dual-port RAMs in leadless chip carriers. The full 32K bytes of dual-port RAM are directly addressable by utilization of the two on-board IDT54/74FCT138 decoder circuits that interpret the higher order addresses A_{L12-14} and A_{R12-14} to select one of the eight 4K x 8 dual-port RAMs. Extremely high speeds are achieved in this fashion due to the use of the IDT7134 dual-port RAM, fabricated in IDT's high-performance CEMOS technology.

The IDT7M137 provides two ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in the memory. The IDT7M137 is designed to be used in systems where on-chip hardware port arbitration is not needed. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7M137 is available with access times as fast as 55ns commercial and 60ns military temperature range, with operating power consumption of only 4W (max.) The modules also offer a standby power mode of 3.6W (max.) and full standby mode of 1.3W (max.).

All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

Signal	Pin	Pin	Signal
GND(1)	1	58	V_{CC}(1)
$\overline{CE}_L$	2	57	$\overline{CE}_R$
$R/\overline{W}_L$	3	56	$R/\overline{W}_R$
NC	4	55	NC
A_{11L}	5	54	A_{11R}
$\overline{OE}_L$	6	53	$\overline{OE}_R$
A_{0L}	7	52	A_{0R}
A_{1L}	8	51	A_{1R}
A_{2L}	9	50	A_{2R}
A_{3L}	10	49	A_{3R}
A_{4L}	11	48	A_{4R}
A_{5L}	12	47	A_{5R}
A_{6L}	13	46	A_{6R}
A_{7L}	14	45	A_{7R}
A_{8L}	15	44	A_{8R}
A_{9L}	16	43	A_{9R}
A_{10L}	17	42	A_{10R}
A_{12L}	18	41	A_{12R}
A_{13L}	19	40	A_{13R}
A_{14L}(2)	20	39	A_{14R}(2)
I/O_{0L}	21	38	I/O_{0R}
I/O_{1L}	22	37	I/O_{1R}
I/O_{2L}	23	36	I/O_{2R}
I/O_{3L}	24	35	I/O_{3R}
I/O_{4L}	25	34	I/O_{4R}
I/O_{5L}	26	33	I/O_{5R}
I/O_{6L}	27	32	I/O_{6R}
I/O_{7L}	28	31	I/O_{7R}
GND(1)	29	30	V_{CC}(1)

M7(3)

DIP TOP VIEW

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L-14L}	A_{0R-14R}	Address
I/O_{0L-7L}	I/O_{0R-7R}	Data Input/Output
V_{CC}		Power
GND		Ground

NOTES:

1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. On 16K x 8 IDT7M136 option, A_{14L} and A_{14R} need to be externally connected to ground for proper operation.
3. For module dimensions, please refer to module drawing M7 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

CMOS SLAVE DUAL-PORT RAM MODULE 64K (8K x 8-BIT) & 128K (16K x 8-BIT)

IDT7M144S
IDT7M145S

FEATURES:

- High-density 64K/128K-bit CMOS SLAVE dual-port RAM modules
- Easily expands data bus width to 16-or-more-bits when used with MASTER IDT7M134 or IDT7M135
- 16K x 8 organization (IDT7M145) or 8K x 8 option (IDT7M144)
- High-speed access
  - Military: 60ns (max.)
  - Commercial: 45ns (max.)
- Low power operation
  - Active: 950mW (typ.) (IDT7M144)
  - Standby: 20mW (typ.) (IDT7M144)
- $\overline{BUSY}$ input flags
- Fully asynchronous operation from either port
- Fully static operation
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Single 5V(±10%) power supply
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M144/145 are 64K/128K-bit high-speed CEMOS™ SLAVE dual-port static RAM modules constructed on a multi-layered, co-fired, ceramic substrate using four IDT7142 2K x 8 SLAVE dual-port RAMs (IDT7M144) or eight IDT7142 SLAVE dual-port RAMs (IDT7M145) in leadless chip carriers. Dual-port function is achieved by utilization of the two on-board IDT54/74FCT138 decoder circuits that interpret the higher order addresses A_{L11-13} and A_{R11-13} to select one of the eight 2K x 8 dual-port RAMs. (On IDT7M144 8K x 8 option, the A_{L13} and A_{R13} need to be externally grounded and the selection becomes one of the four 2K x 8 dual-port RAMs.)

The IDT7M144/145 are designed as "SLAVE" dual-port RAM modules to be used together with the IDT7M135/135 "MASTER" dual-port RAM modules in 16-or-more-bit systems, whereas the IDT7M134/135 are designed to be used as stand-alone 8-bit dual-port RAM modules. Using the IDT MASTER/SLAVE dual-port RAM module approach in 16-or-more-bit memory system applications results in full speed operation without the need for additional discrete logic.

Both SLAVE IDT7M144/145 and MASTER IDT7M134/135 modules provide two ports with separate control, address and I/O pins that permit independent asynchronous access for reads or writes to any location in the memory. The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. The delayed port will have access when $\overline{BUSY}$ goes high (inactive). The $\overline{BUSY}$ pins are outputs on the MASTER and inputs on the SLAVE.

PIN CONFIGURATION

Pin name	Pin	Pin	Pin name
GND(1)	1	58	V_{CC}(1)
$\overline{CE}_L$	2	57	$\overline{CE}_R$
$R/\overline{W}_L$	3	56	$R/\overline{W}_R$
NC	4	55	NC
$\overline{BUSY}_L$(3)	5	54	$\overline{BUSY}_R$(3)
$\overline{OE}_L$	6	53	$\overline{OE}_R$
A_{0L}	7	52	A_{0R}
A_{1L}	8	51	A_{1R}
A_{2L}	9	50	A_{2R}
A_{3L}	10	49	A_{3R}
A_{4L}	11	48	A_{4R}
A_{5L}	12	47	A_{5R}
A_{6L}	13	46	A_{6R}
A_{7L}	14	45	A_{7R}
A_{8L}	15	44	A_{8R}
A_{9L}	16	43	A_{9R}
A_{10L}	17	42	A_{10R}
A_{11L}	18	41	A_{11R}
A_{12L}	19	40	A_{12R}
A_{13L}(2)	20	39	A_{13R}(2)
I/O_{0L}	21	38	I/O_{0R}
I/O_{1L}	22	37	I/O_{1R}
I/O_{2L}	23	36	I/O_{2R}
I/O_{3L}	24	35	I/O_{3R}
I/O_{4L}	25	34	I/O_{4R}
I/O_{5L}	26	33	I/O_{5R}
I/O_{6L}	27	32	I/O_{6R}
I/O_{7L}	28	31	I/O_{7R}
GND(1)	29	30	V_{CC}(1)

M7(4)

DIP TOP VIEW

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$A_{0L}-A_{13L}$	$A_{0R}-A_{13R}$	Address
$I/O_{0L}-I/O_{7L}$	$I/O_{0R}-I/O_{7R}$	Data Input/Output
V_{CC}		Power
GND		Ground

NOTES:

1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. On 8K x 8 IDT7M134 option, A_{13L} and A_{13R} need to be externally connected to ground for proper operation.
3. IDT7M134/135 (MASTER): $\overline{BUSY}$ is open drain output and requires pull up resistor. IDT7M144/145 (SLAVE): $\overline{BUSY}$ is input.
4. For module dimensions, please refer to module drawing M7 in the packaging section.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

6

FIFO MEMORIES

Integration of IDT's high-speed static RAM technology with internal support logic yields high-performance, high-density FIFO memories. A FIFO is used as a memory buffer between two asynchronous systems with simultaneous read/write access. The data rate between the two systems can be regulated by monitoring the status flags and throttling the read and write accesses. Since these FIFOs are built with an internal RAM pointer architecture, there is no fall-through time between a write to a memory location and a read from that memory location. System performance is significantly improved over the shift register-based architecture of previous FIFO designs which are handicapped with long fall-through times.

IDT offers the widest selection of monolithic FIFOs, ranging from shallow 64 x 4 and 64 x 5 to the high-density 4K x 9. Shallow FIFOs regulate data flow in tightly coupled computational engines. High density FIFOs store large data blocks in networking, telecommunication and data storage systems. The IDT7200 FIFO family (256 x 9 through the 4K x 9 FIFOs) are all pin and function compatible, making density upgrades simple. All IDT FIFOs can be cascaded to greater word depths and expanded to greater word widths with no external support logic.

A variety of packages are available: standard plastic DIP and CERDIP, surface mount ceramic LCC, PLCC and SOIC and high-reliability Flatpack. Increasing board density is the overwhelming goal of the IDT's package development efforts, as demonstrated by the introduction of the 300 mil THINDIP.

The Parallel-Serial FIFO incorporates a serial input and a serial output shifter for serial-to-parallel bus interface. The Parallel-Serial FIFO also offers six status flags for flexible data throttling.

FIFO modules, composed of four LCC devices mounted on a multi-layer co-fired ceramic substrate, increase densities to 16K x 9 which are pin-compatible with current monolithic versions.

IDT is committed to offering FIFOs of increasing density and speed and enhanced architectural innovations, such as Flexishift and the BiFIFO, for easier system interface.

TABLE OF CONTENTS

CONTENTS **PAGE**

FIFO Memories

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 256 x 9-BIT & 512 x 9-BIT

IDT7200S/L
IDT7201SA/LA

FEATURES:

- First-In/First-Out dual-port memory
- 256 X 9 organization (IDT7200)
- 512 x 9 organization (IDT7201A)
- Low power consumption
- Ultra high speed—35ns cycle time (28.5MHz)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- IDT7200 and IDT7201A are pin and functionally compatible with Mostek MK4501, but with Half-Full Flag capability in single device mode
- Master/Slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning flags
- Auto retransmit capability
- High-performance CEMOS™ technology
- Available in plastic DIP, CERDIP, 300 mil sidebraze THINDIP, LCC, PLCC and Flatpack
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87531 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT7200/7201A are dual-port memories that utilize a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The devices use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the devices through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The devices have a read/write cycle time of 35ns (28.5MHz).

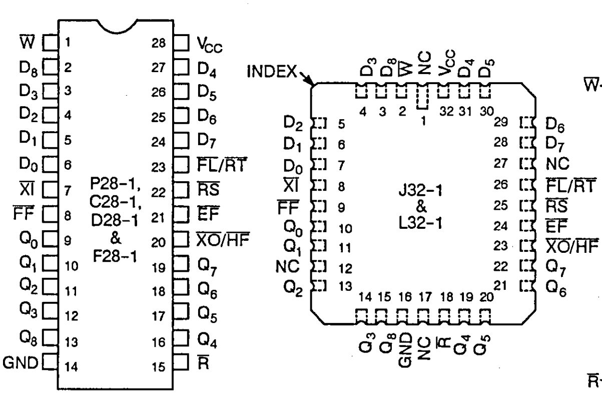
The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

The IDT7200/1A are fabricated using IDT's high-speed CEMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

6

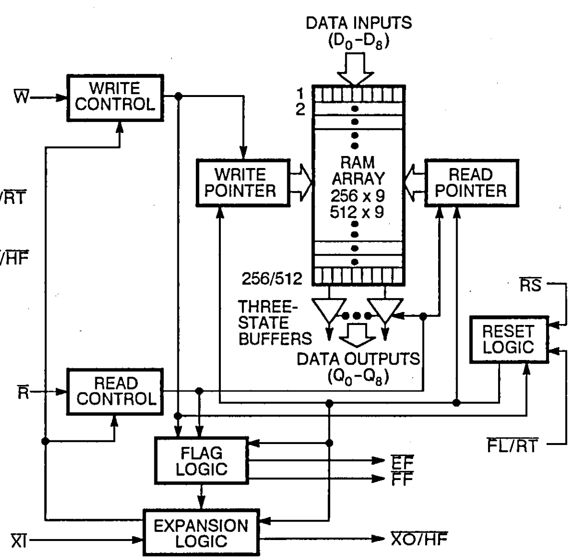
PIN CONFIGURATIONS



DIP TOP VIEW

LCC/PLCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL} (1)	Input Low Voltage Commercial and Military	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7200S/L IDT7201SA/LA COMMERCIAL t_A = 25, 35ns			IDT7200S/L IDT7201SA/LA MILITARY t_A = 30, 40ns			IDT7200S/L IDT7201SA/LA COMMERCIAL t_A = 50, 65, 80, 120ns			IDT7200S/L IDT7201SA/LA MILITARY t_A = 50, 65, 80, 120ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{LI} (1)	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	-1	–	1	-10	–	10	μA
I_{LO} (2)	Output Leakage Current	-10	–	10	-10	–	10	-10	–	10	-10	–	10	μA
V_{OH}	Output Logic "1" Voltage I_{OH} = -2mA	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
I_{CC1} (3)	Active Power Supply Current	–	–	125	–	–	140	–	50	80	–	70	100	mA
I_{CC2} (3)	Average Standby Current ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)	–	–	15	–	–	20	–	5	8	–	8	15	mA
$I_{CC3}(L)$ (3)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	500	–	–	900	–	–	500	–	–	900	μA
$I_{CC3}(S)$ (3)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	5	–	–	9	–	–	5	–	–	9	mA

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$
3. I_{CC} measurements are made with outputs open.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	COM'L.		MIL.		COM'L.		MIL.		MILITARY AND COMMERCIAL								UNIT
		7200x25 7201x25		7200x30 7201x30		7200x35 7201x35		7200x40 7201x40		7200x50 7201x50		7200x65 7201x65		7201x80		7201x120		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_S	Shift Frequency	–	28.5	–	25	–	22.2	–	20	–	15	–	12.5	–	10	–	7	MHz
t_{RC}	Read Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_A	Access Time	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RPW}	Read Pulse Width (2)	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z (3)	5	–	5	–	5	–	5	–	10	–	10	–	10	–	10	–	ns
t_{WLZ}	Write Pulse Low to Data Bus at Low Z (3, 4)	5	–	5	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z (3)	–	18	–	20	–	20	–	25	–	30	–	30	–	30	–	35	ns
t_{WC}	Write Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{WPW}	Write Pulse Width (2)	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{DS}	Data Set-up Time	15	–	18	–	18	–	20	–	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	5	–	10	–	10	–	10	–	ns
t_{RSC}	Reset Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RS}	Reset Pulse Width (2)	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSS}	Reset Set-up Time	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RTC}	Retransmit Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RT}	Retransmit Pulse Width (2)	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTS}	Retransmit Set-up Time	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{EFL}	Reset to Empty Flag Low	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{HFH}, t_{FFH}	Reset to Half-Full and Full Flag High	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{REF}	Read Low to Empty Flag Low	–	25	–	30	–	30	–	30	–	45	–	60	–	60	–	60	ns
t_{RFF}	Read High to Full Flag High	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RPE}	Read Pulse Width After $\overline{EF}$ High	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WEF}	Write High to Empty Flag High	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WFF}	Write Low to Full Flag Low	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RHF}	Read High to Half-Full Flag High	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XI}	$\overline{XI}$ Pulse Width	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	–	15	–	15	–	15	–	15	–	15	–	15	–	15	–	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.
5. "x" in part rating indicates power rating (S/SA or L/LA).

6

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is sampled and not 100% tested.

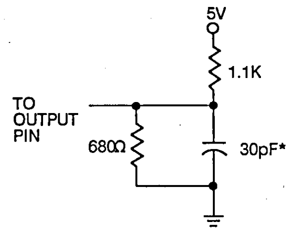


Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN (D_0-D_8)

Data inputs for 9-bit wide data.

CONTROLS

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read enable ($\overline{R}$) and Write enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2, (i.e., t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read enable ($\overline{R}$) goes high, the Data Outputs (Q_0-Q_8) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7200/7201A can be made to retransmit data when the Retransmit enable control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read enable ($\overline{R}$) and Write enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 256/512 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full-Flag ($\overline{FF}$) will go low after 256 writes for the IDT7200 and 512 writes for the IDT7201A.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is one location from the write pointer, indicating that the device is empty. If the write pointer is not moved after Reset ($\overline{RS}$), the Empty Flag ($\overline{EF}$) will go low after 256 reads for the IDT7200 and 512 reads for the IDT7201A.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

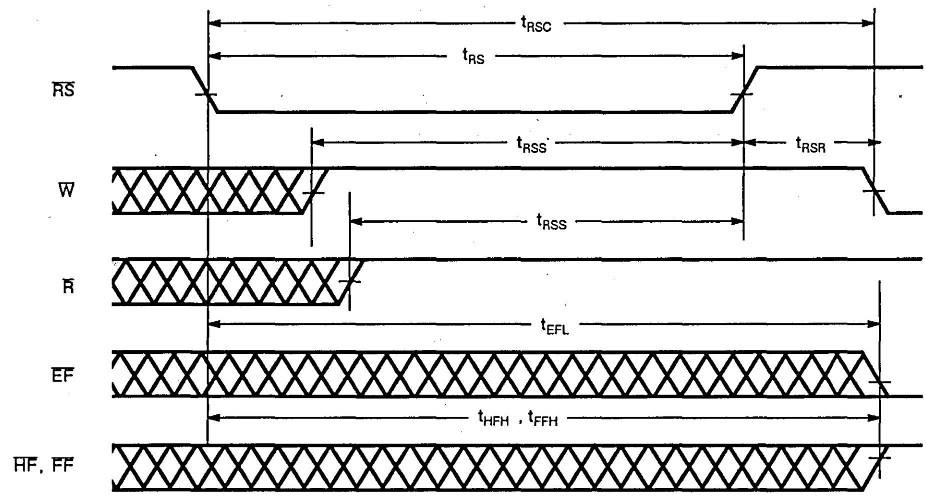
This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q_0–Q_8)

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read ($\overline{R}$) is in a high state.



NOTES:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of RS.

Figure 2. Reset

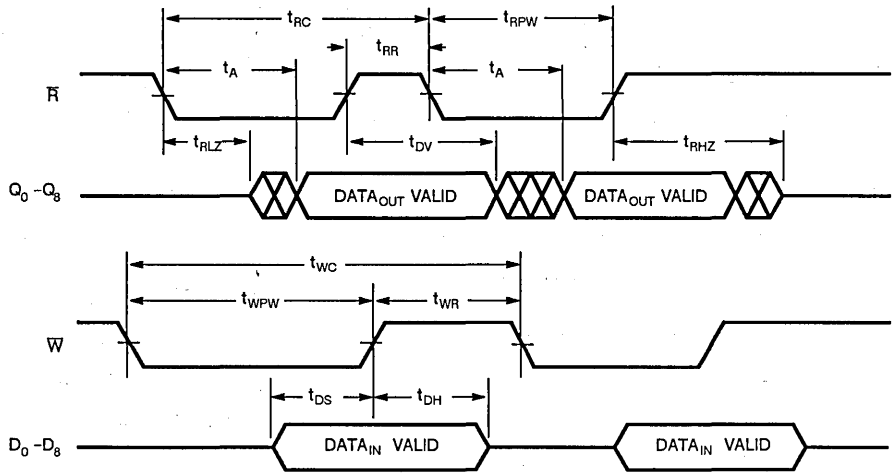


Figure 3. Asynchronous Write and Read Operation

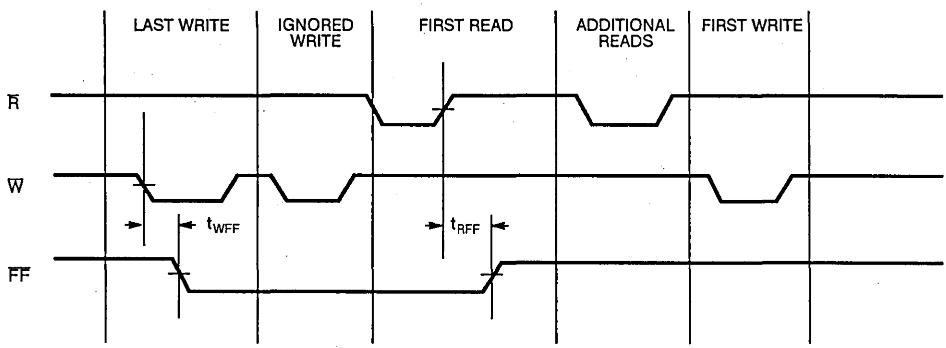


Figure 4. Full Flag From Last Write to First Read

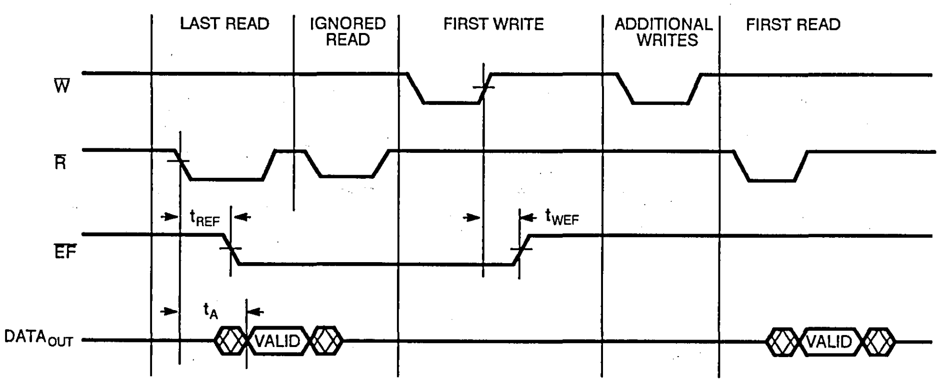
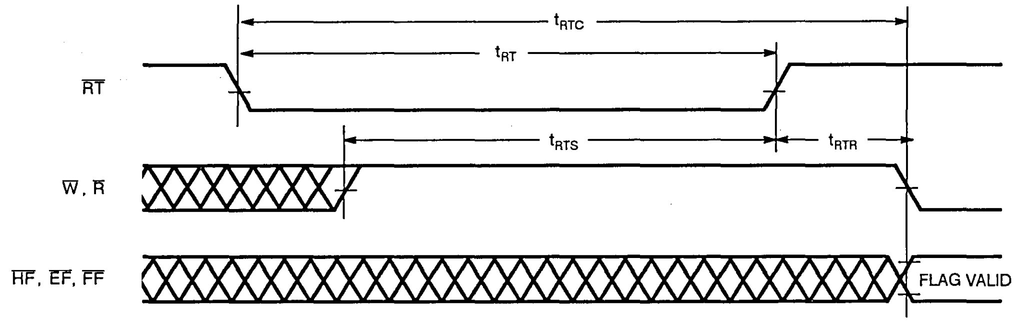


Figure 5. Empty Flag From Last Read to First Write



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

6

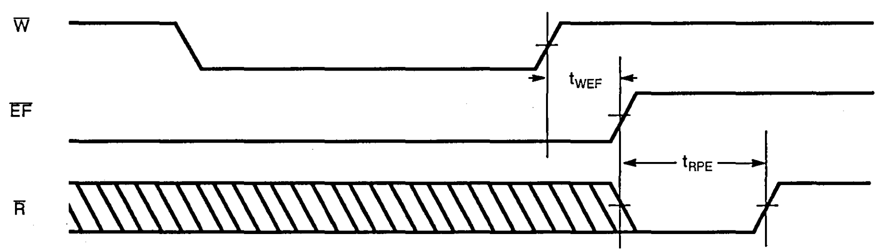


Figure 7. Empty Flag Timing

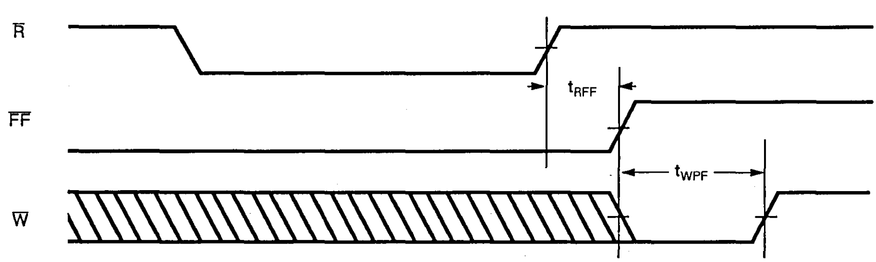


Figure 8. Full Flag Timing

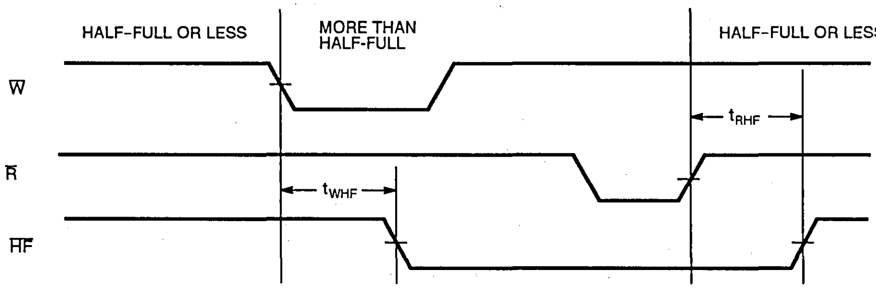


Figure 9. Half-Full Flag Timing

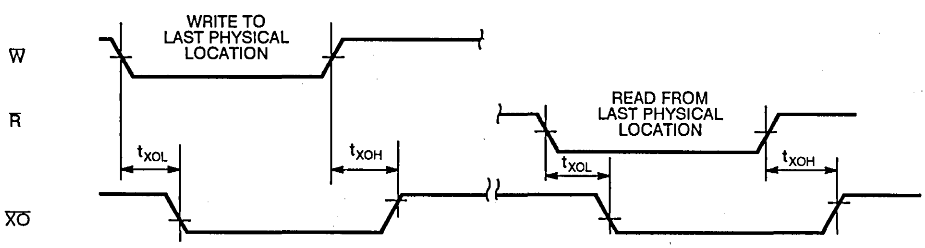


Figure 10. Expansion Out

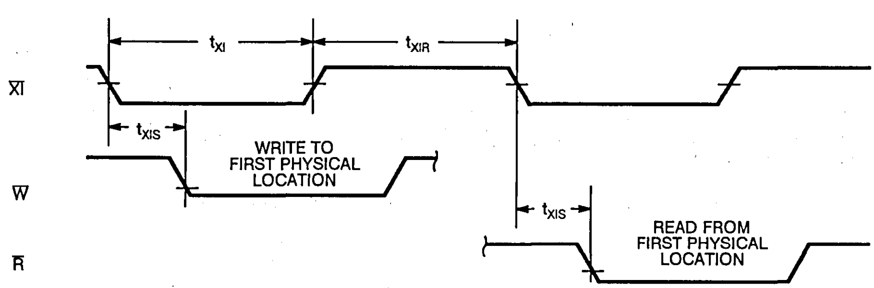


Figure 11. Expansion In

OPERATING MODES

SINGLE DEVICE MODE

A single IDT7200/7201A may be used when the application requirements are for 256/512 words or less. The IDT7200/7201A is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12). In this mode the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).

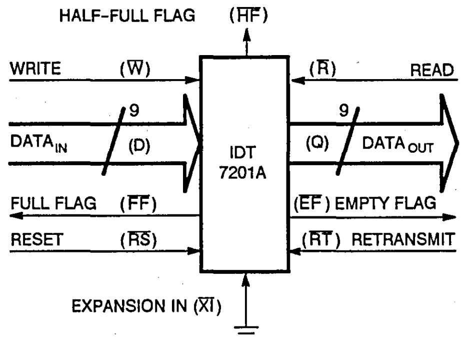
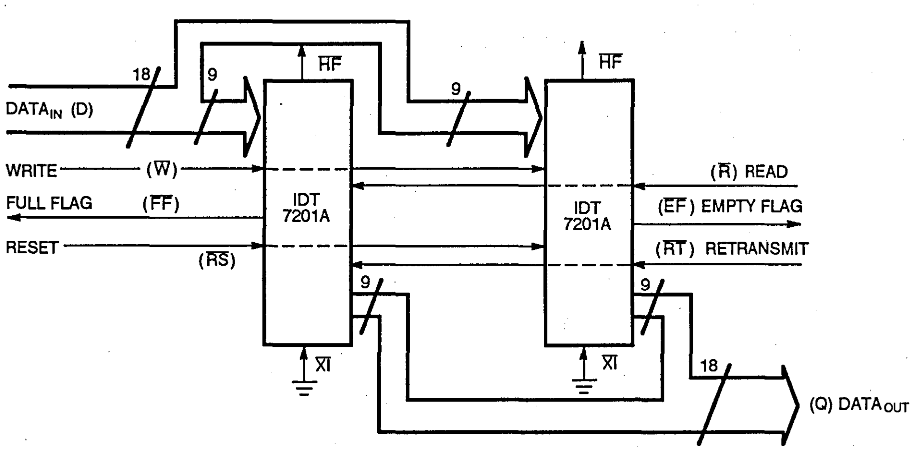


Figure 12. Block Diagram of Single 512x9 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7201As. Any word width can be attained by adding additional IDT7201As.



NOTE:

1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and the $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 13. Block Diagram of 512x18 FIFO Memory Used In Width Expansion Mode

6

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7200/7201A can easily be adapted to applications where the requirements are for greater than 256/512 words. Figure 14 demonstrates Depth Expansion using three IDT7200/7201As. Any depth can be attained by adding additional IDT7200/7201As. The IDT7200/7201A operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7200/7201As as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system, (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits the reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$)ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ is low, more words can be written to the FIFO (the subsequent writes after the first write edge will de-assert the Empty Flag); however, the same word (written on the first write edge) presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line, being low, causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs."

TABLE I—RESET AND RETRANSMIT—

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II—RESET AND FIRST LOAD TRUTH TABLE—

DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
$\overline{RS}$ = Reset Input $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

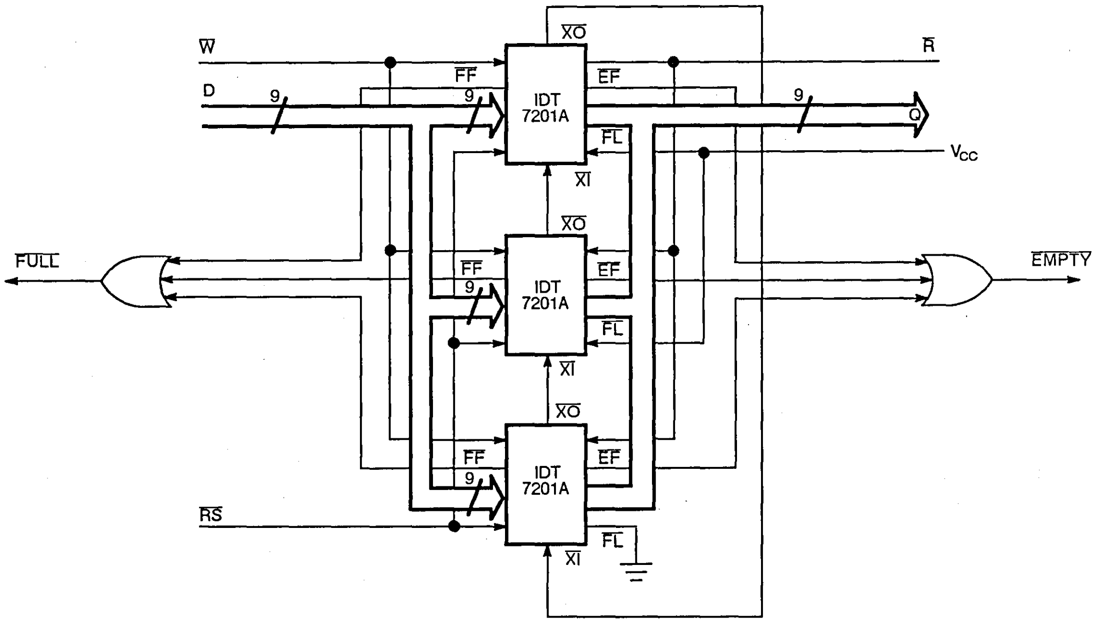
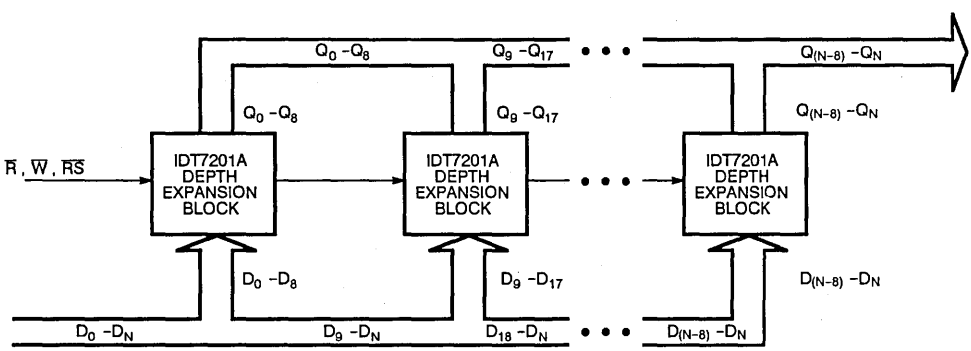


Figure 14. Block Diagram of 1536 x 9 FIFO Memory (Depth Expansion)



NOTES:

1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

6

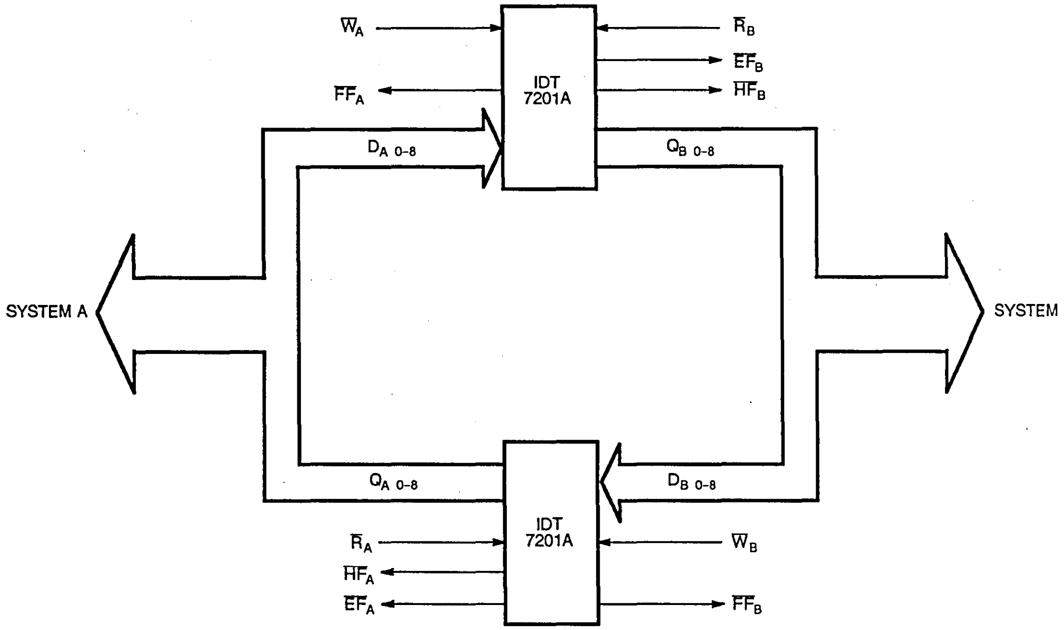


Figure 16. Bidirectional FIFO Mode

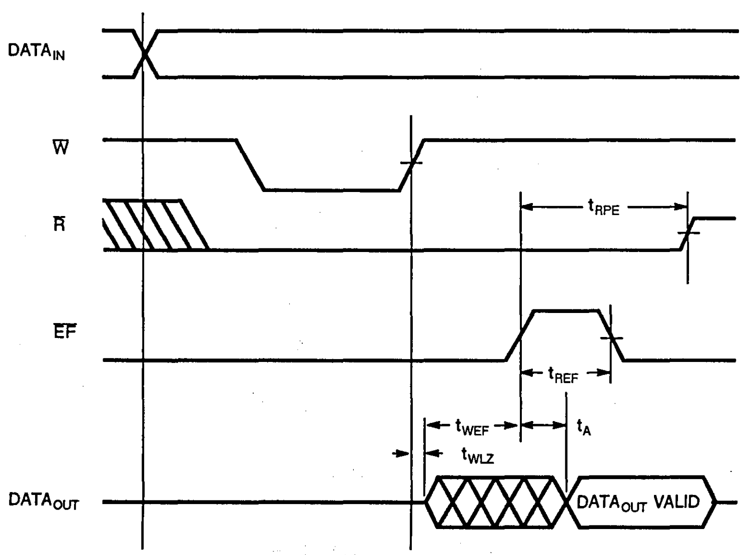


Figure 17. Read Data Flow-Through Mode

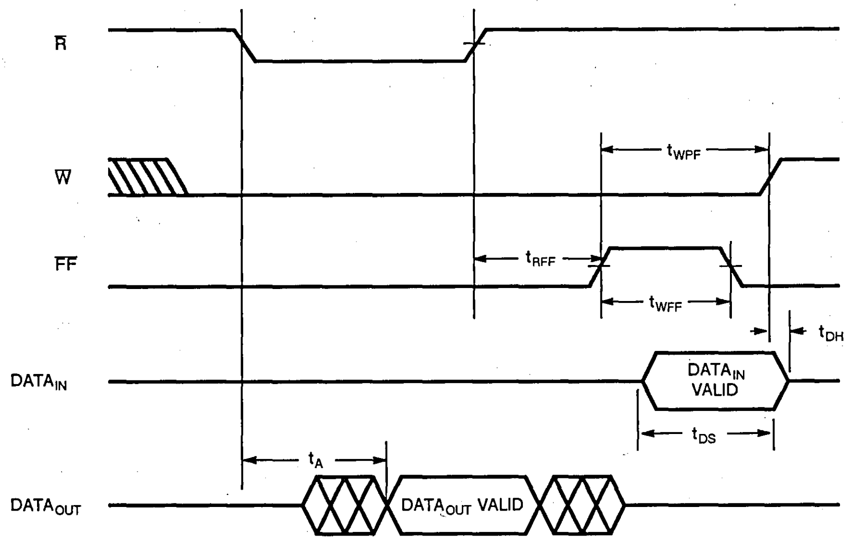


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

P	Plastic Dip
D	CERDIP
TC	Sidebraze THINDIP
J	Plastic Leaded Chip Carrier
L	Leadless Chip Carrier
F	Flatpack

Speed — Access Time (t_A) Speed in Nanoseconds

25	Commercial Only
30	Military Only
35	Commercial Only
40	Military Only
50	
65	
80	
120	

Power

SA	Standard Power*
LA	Low Power*

Device Type

7200	256 x 9-Bit FIFO
7201	512 x 9-Bit FIFO

* "A" to be included for 7201 ordering part number only.

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 1024 x 9-BIT

FEATURES:

- First-In/First-Out dual-port memory
- 1024 x 9 organization
- Low power consumption
- Ultra high speed—35ns cycle time (28.5MHz)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin compatible with Mostek MK4501, but with Half-Full Flag capability
- Allows for deep word structure (1024) without expansion
- Half-Full Flag capability in single device mode
- Master/Slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning flags
- Auto retransmit capability
- High-performance CEMOS™ technology
- Available in Plastic DIP, CERDIP, 300 mil sidebraze THINDIP, LCC, PLCC and Flatpack
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7202A is a dual-port memory that utilizes a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

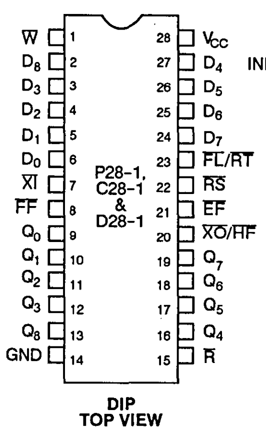
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The device has a read/write cycle time of 35ns (28.5MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

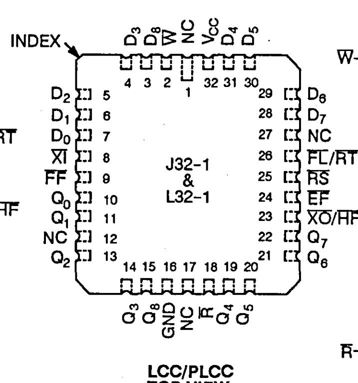
The IDT7202A is fabricated using IDT's high-speed CEMOS technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 1024 x 9 organization of the IDT7202A allows a 1024 deep word structure without the need for expansion.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

PIN CONFIGURATIONS



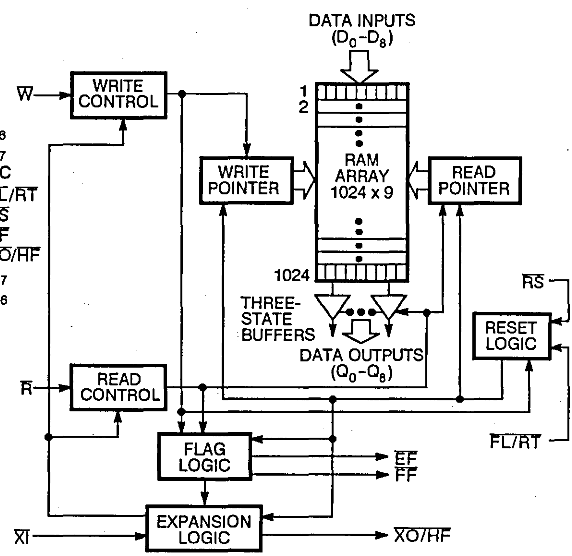
DIP TOP VIEW



LCC/PLCC TOP VIEW

CONSULT FACTORY FOR FLATPACK PINOUT

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
$V_{IL}^{(1)}$	Input Low Voltage Commercial and Military	–	–	0.8	V

NOTE:

1. 1.5V undershoots are allowed for 10ns once per cycle.

6

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7202SA/LA COMMERCIAL t_A = 25, 35ns			IDT7202SA/LA MILITARY t_A = 30, 40ns			IDT7202SA/LA COMMERCIAL t_A = 50, 65, 80, 120ns			IDT7202SA/LA MILITARY t_A = 50, 65, 80, 120ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$I_{LI}^{(1)}$	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	-1	–	1	-10	–	10	µA
$I_{LO}^{(2)}$	Output Leakage Current	-10	–	10	-10	–	10	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = -2mA	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
$I_{CC1}^{(3)}$	Active Power Supply Current	–	–	125	–	–	140	–	50	80	–	70	100	mA
$I_{CC2}^{(3)}$	Average Standby Current ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)	–	–	15	–	–	20	–	5	8	–	8	15	mA
$I_{CC3}(L)^{(3)}$	Power Down Current (All Input = V_{CC} -0.2V)	–	–	500	–	–	900	–	–	500	–	–	900	µA
$I_{CC3}(S)^{(3)}$	Power Down Current (All Input = V_{CC} -0.2V)	–	–	5	–	–	9	–	–	5	–	–	9	mA

NOTES:

1. Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$
3. I_{CC} measurements are made with outputs open.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	COM'L.		MIL.		COM'L.		MIL.		MILITARY AND COMMERCIAL								UNIT
		7202x25		7202x30		7202x35		7202x40		7202x50		7202x65		7202x80		7202x120		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_S	Shift Frequency	–	28.5	–	25	–	22.2	–	20	–	15	–	12.5	–	10	–	7	MHz
t_{RC}	Read Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_A	Access Time	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RPW}	Read Pulse Width (2)	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z (3)	5	–	5	–	5	–	5	–	10	–	10	–	10	–	10	–	ns
t_{WLZ}	Write Pulse Low to Data Bus at Low Z (3, 4)	5	–	5	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z (3)	–	18	–	20	–	20	–	25	–	30	–	30	–	30	–	35	ns
t_{WC}	Write Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{WPW}	Write Pulse Width (2)	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{DS}	Data Set-up Time	15	–	18	–	18	–	20	–	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	5	–	10	–	10	–	10	–	ns
t_{RSC}	Reset Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RS}	Reset Pulse Width (2)	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSS}	Reset Set-up Time	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RTC}	Retransmit Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RT}	Retransmit Pulse Width (2)	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTS}	Retransmit Set-up Time	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{EFL}	Reset to Empty Flag Low	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{HFH}, t_{FFH}	Reset to Half-Full and Full Flag High	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{REF}	Read Low to Empty Flag Low	–	25	–	30	–	30	–	30	–	45	–	60	–	60	–	60	ns
t_{RFF}	Read High to Full Flag High	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RPE}	Read Pulse Width After $\overline{EF}$ High	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WEF}	Write High to Empty Flag High	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WFF}	Write Low to Full Flag Low	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RHF}	Read High to Half-Full Flag High	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XI}	$\overline{XI}$ Pulse Width	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	–	15	–	15	–	15	–	15	–	15	–	15	–	15	–	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.
5. "x" in part rating indicates power rating (SA or LA).

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

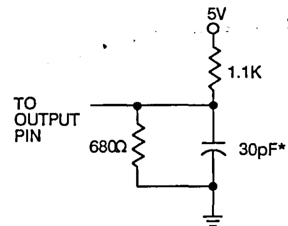


Figure 1. Output Load

*Includes jig and scope capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is sampled and not 100% tested.

SIGNAL DESCRIPTIONS

INPUTS

DATA IN (D_0-D_8)

Data inputs for 9-bit wide data.

CONTROLS

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2, (i.e., t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs (Q_0-Q_8) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7202A can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 1024 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full-flag ($\overline{FF}$) will go low after 1024 writes.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is one location from the write pointer, indicating that the device is empty. If the write pointer is not moved after Reset ($\overline{RS}$), the Empty Flag ($\overline{EF}$) will go low after 1024 reads.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

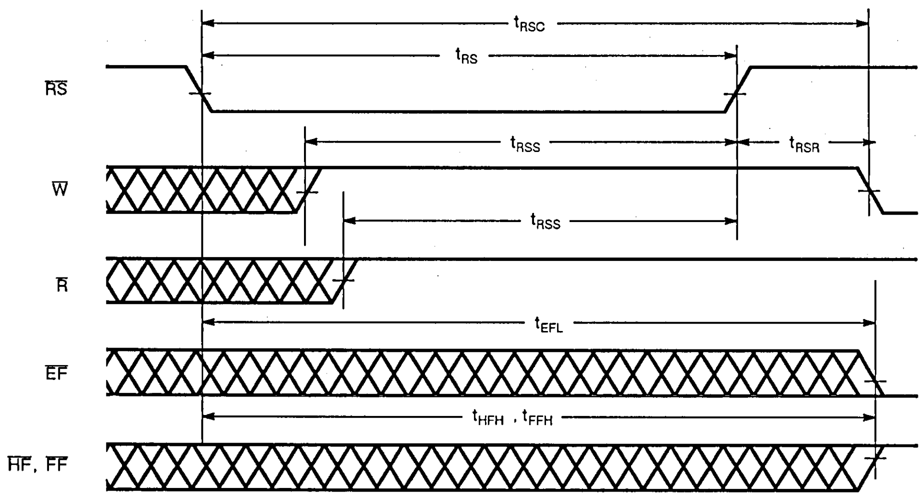
This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q_0 – Q_8)

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read ($\overline{R}$) is in a high state.



NOTES:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of RS.

Figure 2. Reset

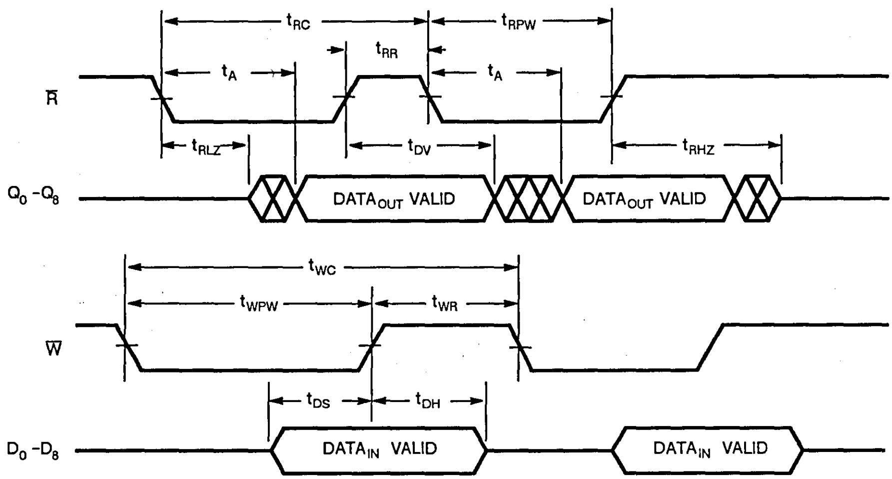


Figure 3. Asynchronous Write and Read Operation

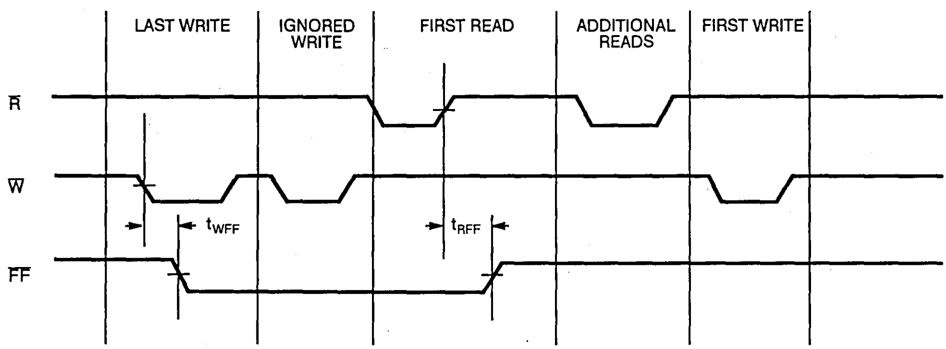


Figure 4. Full Flag From Last Write to First Read

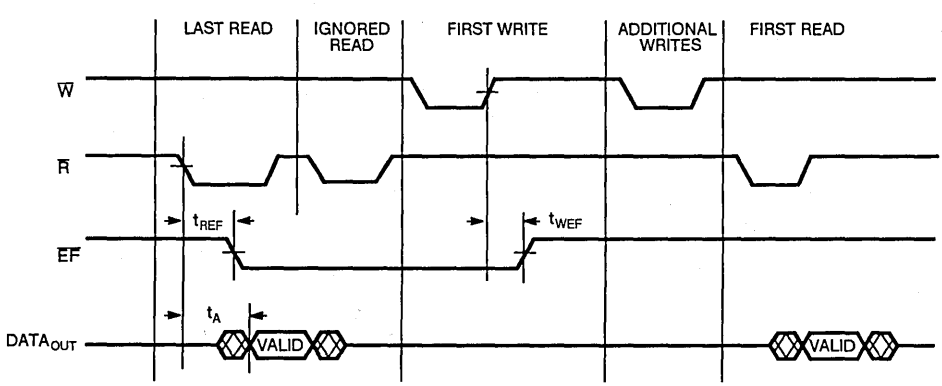
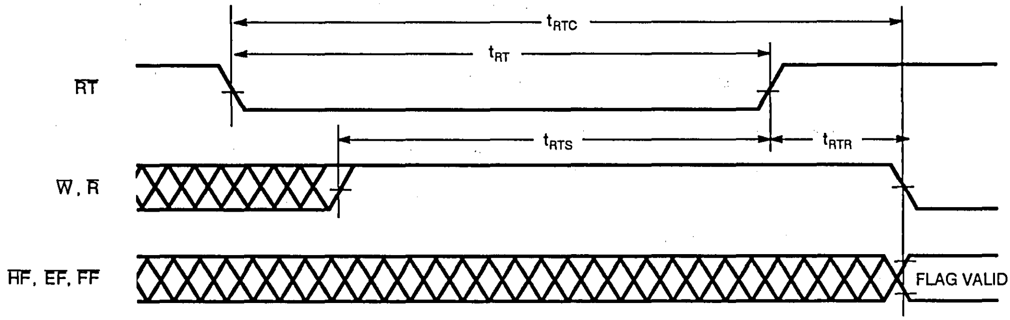


Figure 5. Empty Flag From Last Read to First Write



NOTES:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

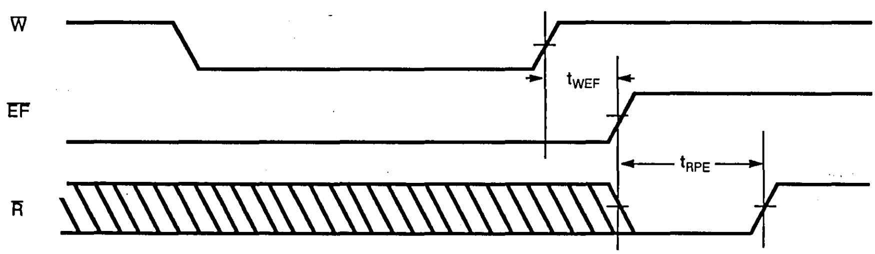


Figure 7. Empty Flag Timing

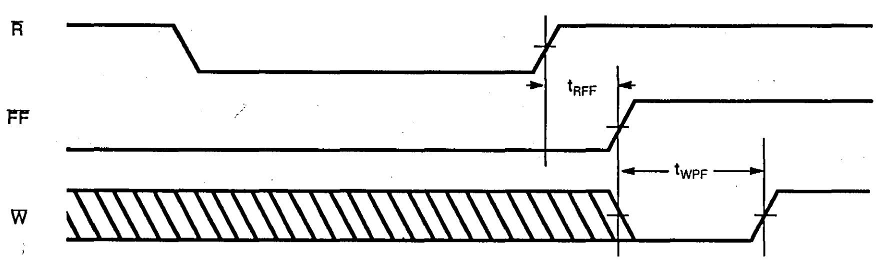


Figure 8. Full Flag Timing

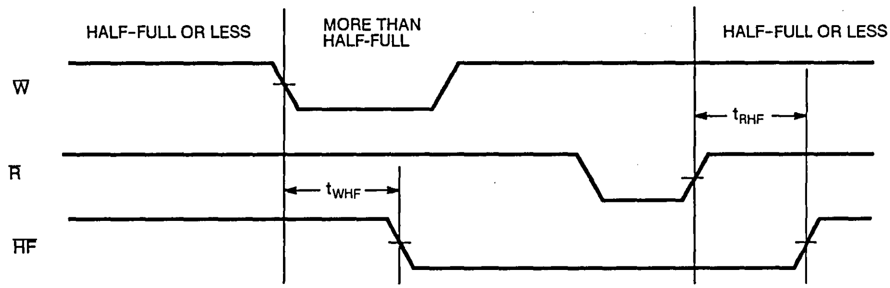


Figure 9. Half-Full Flag Timing

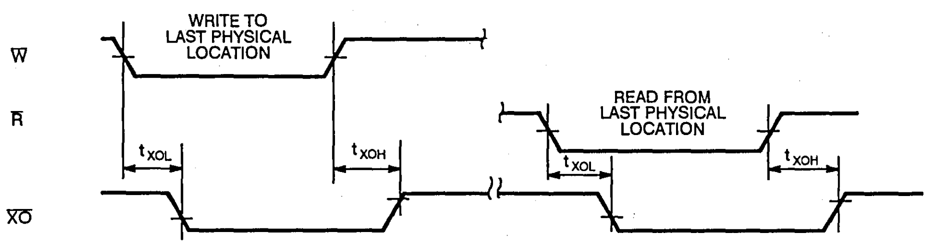


Figure 10. Expansion Out

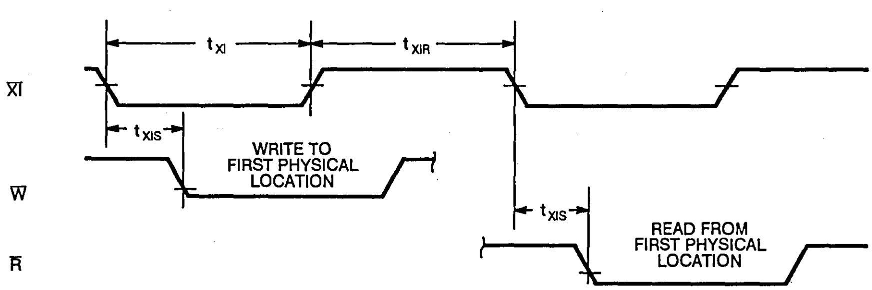


Figure 11. Expansion In

OPERATING MODES

SINGLE DEVICE MODE

A single IDT7202A may be used when the application requirements are for 1024 words or less. The IDT7202A is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12). In this mode the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).

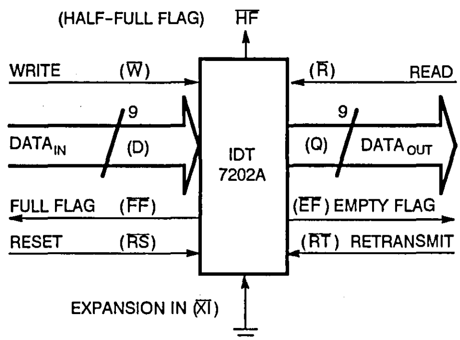
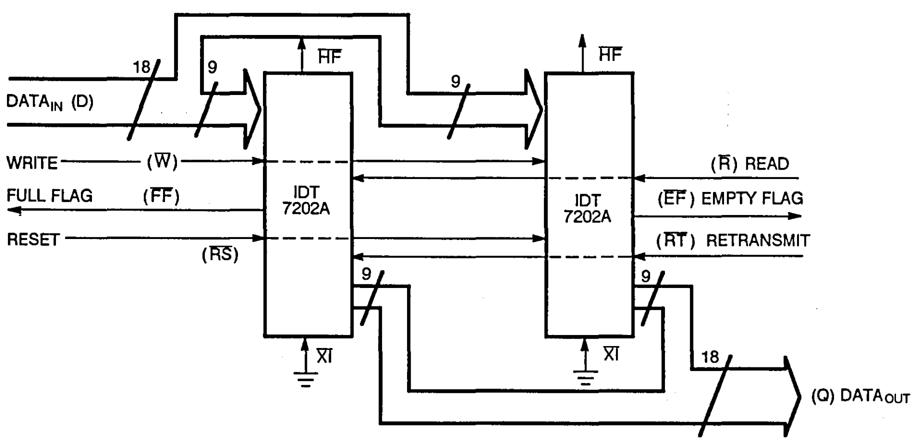


Figure 12. Block Diagram of Single 1024 x 9 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7202As. Any word width can be attained by adding additional IDT7202s.



NOTE:

1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and the $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 13. Block Diagram of 1024 x 18 FIFO Memory Used in Width Expansion Mode

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7202A can easily be adapted to applications where the requirements are for greater than 1024 words. Figure 14 demonstrates Depth Expansion using three IDT7202As. Any depth can be attained by adding additional IDT7202As. The IDT7202As operate in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7202As as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits the reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$)ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ is low, more words can be written to the FIFO (the subsequent writes after the first write edge will de-assert the Empty Flag); however, the same word (written on the first write edge) presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ was low. On toggling $\overline{R}$, the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line, being low, causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs".

TABLE I—RESET AND RETRANSMIT—

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTES:
1. Pointer will increment if flag is high.

TABLE II—RESET AND FIRST LOAD TRUTH TABLE—

DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
   $\overline{RS}$ = Reset Input $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

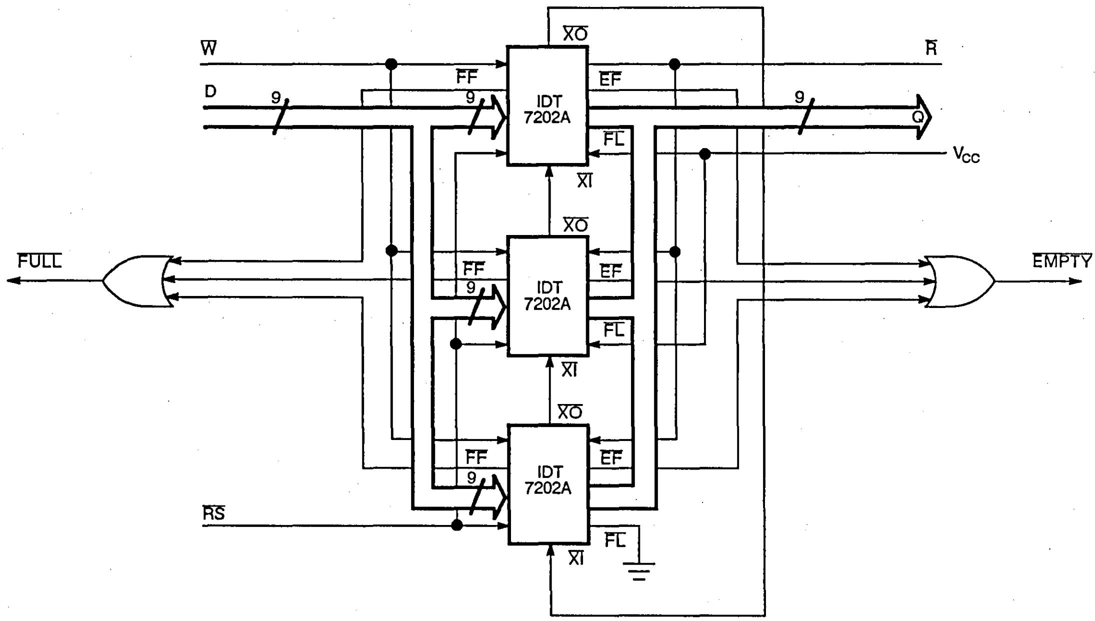
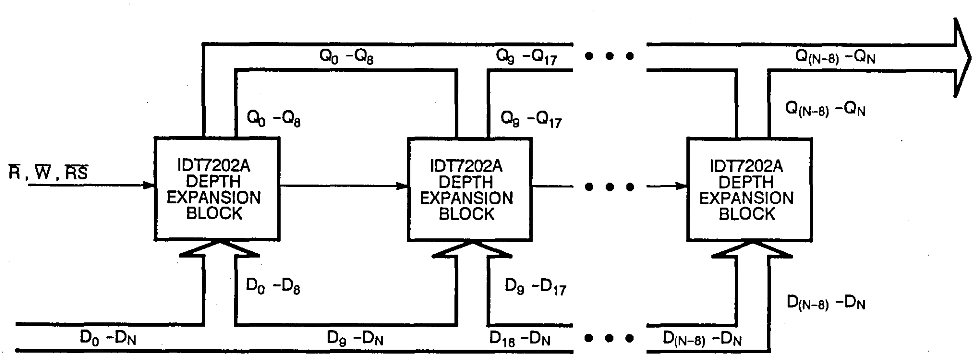


Figure 14. Block Diagram of 3072 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

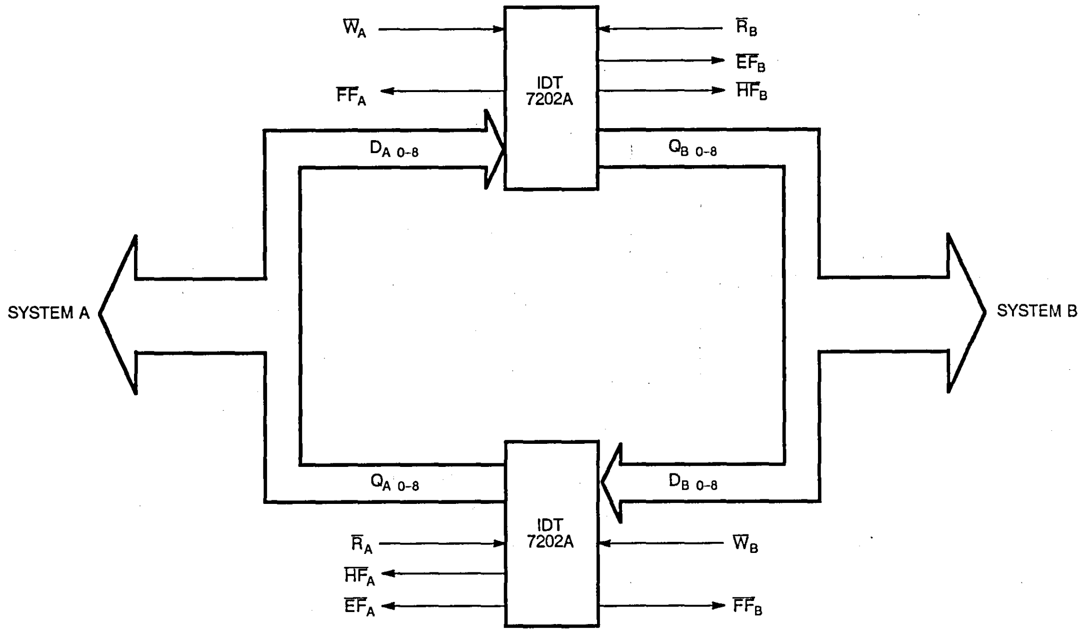


Figure 16. Bidirectional FIFO Mode

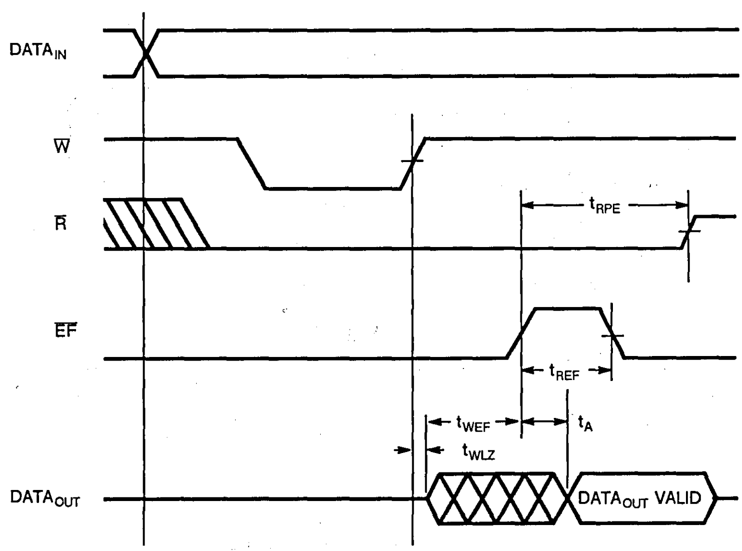


Figure 17. Read Data Flow-Through Mode

6

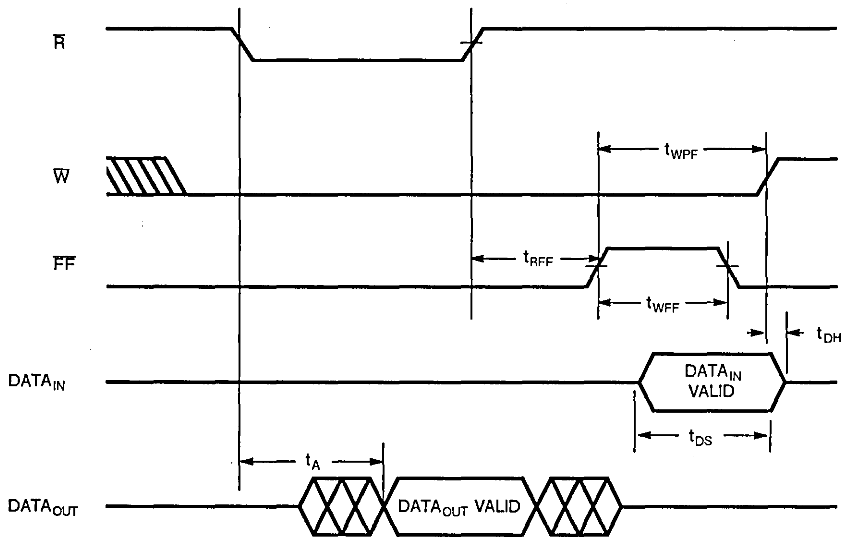


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range		
Blank	Commercial (0°C to +70°C)	
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B	
Package		
P	Plastic Dip	
D	CERDIP	
TC	Sidebraze THINDIP	
J	Plastic Leaded Chip Carrier	
L	Leadless Chip Carrier	
F	Flatpack	
Speed		
25	Commercial Only	Access Time (t_A) Speed in Nanoseconds
30	Military Only	
35	Commercial Only	
40	Military Only	
50		
65		
80		
120		
Power		
SA	Standard Power	
LA	Low Power	
Device Type		
7202	1024 x 9-Bit FIFO	

1Kx9-BIT CMOS PARALLEL FIFO WITH FLAGS

ADVANCE INFORMATION
IDT72021

FEATURES:

- First-In/First-Out (FIFO) dual-port memory
- 1Kx9-bit organization
- Ultra-high-speed: 25ns access time, 35ns cycle time (28.5MHz)
- Fully expandable in word depth and/or width
- Asynchronous and simultaneous read and write
- Functionally equivalent to the IDT7202 but with Output Enable and Almost-Empty/Full Flag
- Four status flags: Full, Empty, Half-Full (single device mode) and Almost-Empty/Full (1/8 or 7/8) signal on 0, 128, 512, 896 and 1024-byte boundaries
- Output Enable controls the data output port
- Auto-retransmit capability
- Master/Slave multiprocesssing applications
- Video frame buffer or laser printer buffer applications
- Available in 32-pin DIP and surface mount 32-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72021 is a dual-port memory that utilizes a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device has Full, Empty, Half-Full and Almost-Empty/Full flags to prevent data overflow or underflow. Expansion logic allows wider and/or deeper FIFOs to be created using multiple devices without external logic.

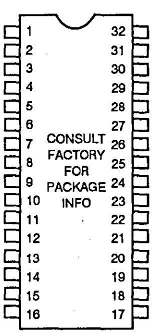
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of Write ($\overline{W}$) and Read ($\overline{R}$) pins. The device has a read/write access time of 25ns and a read/write cycle time of 35ns (28.5MHz). The IDT72021 can perform asynchronous and simultaneous read and write operations.

The IDT72021 utilizes a 9-bit wide dual-port RAM array to allow for zero fall-through time and to allow the user to store tag or parity bits. This 9-bit feature is useful in data communications applications where transmission/reception error checking is necessary. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position, when $\overline{RT}$ is pulsed low, to allow for retransmission of data from the beginning. Four status flags prevent the overflow or underflow of the FIFO and permit interrupt signals to be sent to the transmitting data source.

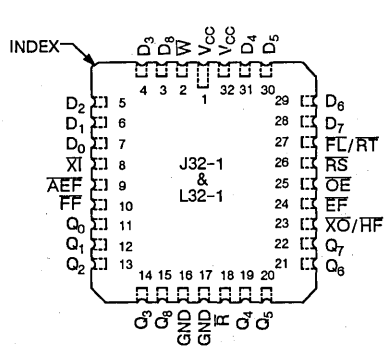
The IDT72021 is fabricated using IDT's high-performance CEMOS™ technology, which combines high speed and low power consumption. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, for high reliability systems.

6

PIN CONFIGURATIONS

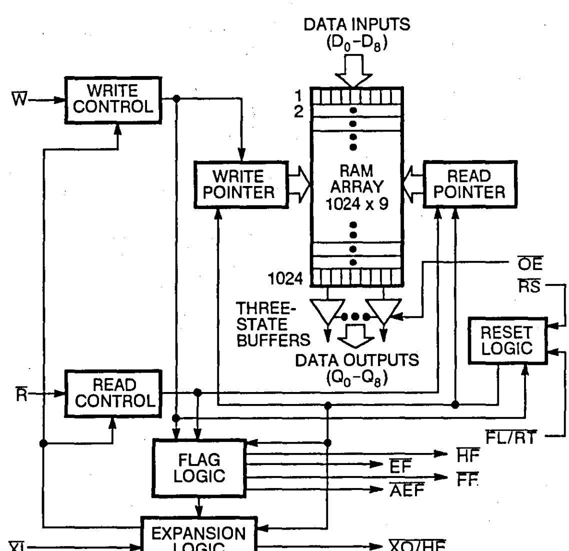


DIP
TOP VIEW



LCC/PLCC
PINOUT

FUNCTIONAL BLOCK DIAGRAM



![Integrated Device Technology, Inc.]

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 2048 x 9-BIT & 4096 x 9-BIT

IDT7203S/L
IDT7204S/L

FEATURES:

- First-In/First-Out dual-port memory
- 2048 x 9 organization (IDT7203)
- 4096 x 9 organization (IDT7204)
- Low power consumption
  - Active: 660mW (max.)
  - Power down: 66mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin and functionally compatible with IDT7201A/7202A
- IDT7204 allows 4096 word structure without expansion
- Half-Full Flag capability in single device mode
- Master/Slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- Auto retransmit capability
- High-performance CEMOS™ technology
- Available in CERDIP, Plastic DIP, PLCC and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7203/7204 are dual-port memories that utilize a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

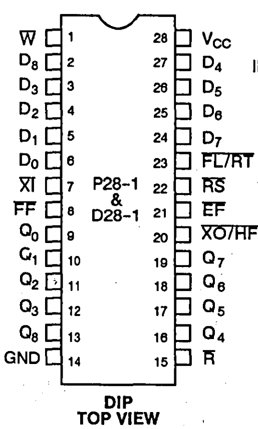
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The device has a read/write cycle time of 45ns (22.2MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

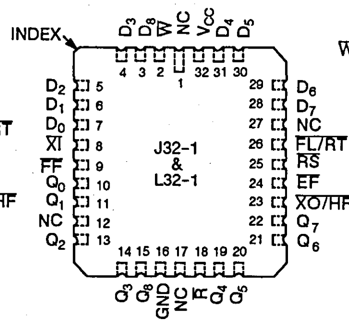
The IDT7203/7204 is fabricated using IDT's high-speed CEMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 4096 x 9 organization for the IDT7204 allows a 4096 deep word structure without the need for expansion.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

PIN CONFIGURATIONS

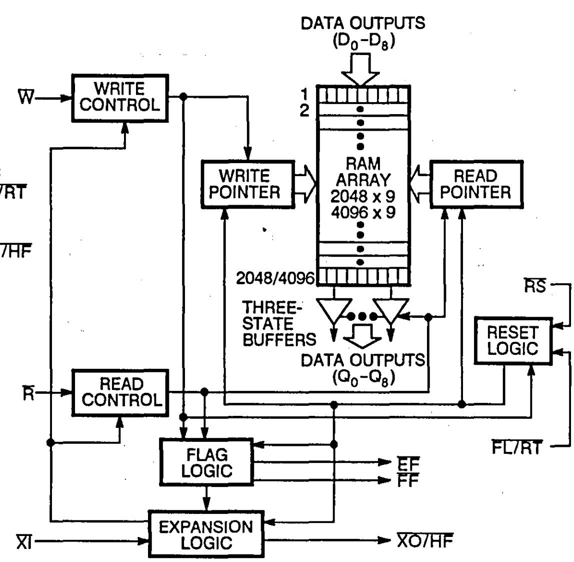


DIP TOP VIEW



PLCC/LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL} (1)	Input Low Voltage Commercial & Military	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

6

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7203S/L IDT7204S/L COMMERCIAL t_A = 50, 65, 80, 120ns			IDT7203S/L IDT7204S/L MILITARY t_A = 50, 65, 80, 120ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{IL} (1)	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	µA
I_{OL} (2)	Output Leakage Current	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -2mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	–	–	0.4	–	–	0.4	V
I_{CC1} (3)	Average V_{CC} Power Supply Current	–	75	120	–	100	150	mA
I_{CC2} (3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	–	8	12	–	12	25	mA
I_{CC3} (L) (3)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	2	–	–	4	mA
I_{CC3} (S) (3)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	8	–	–	12	mA

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{OUT}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
3. I_{CC} measurements are made with outputs open.

AC ELECTRICAL CHARACTERISTICS [1]

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

SYMBOL	PARAMETER	7203S/L50 7204S/L50 MIN.	MAX.	7203S/L65 7204S/L65 MIN.	MAX.	7203S/L80 7204S/L80 MIN.	MAX.	7203S/L120 7204S/L120 MIN.	MAX.	UNIT
f_s	Shift Frequency	–	15	–	12.5	–	10	–	7	MHz
t_{RC}	Read Cycle Time	65	–	80	–	100	–	140	–	ns
t_A	Access Time	–	50	–	65	–	80	–	120	ns
t_{RR}	Read Recovery Time	15	–	15	–	20	–	20	–	ns
t_{RPW}	Read Pulse Width [2]	50	–	65	–	80	–	120	–	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z [3]	10	–	10	–	10	–	10	–	ns
t_{WLZ}	Write Pulse Low to Data Bus at Low Z [3, 4]	15	–	15	–	20	–	20	–	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z [3]	–	30	–	30	–	30	–	35	ns
t_{WC}	Write Cycle Time	65	–	80	–	100	–	140	–	ns
t_{WPW}	Write Pulse Width [2]	50	–	65	–	80	–	120	–	ns
t_{WR}	Write Recovery Time	15	–	15	–	20	–	20	–	ns
t_{DS}	Data Set-up Time	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	5	–	10	–	10	–	10	–	ns
t_{RSC}	Reset Cycle Time	65	–	80	–	100	–	140	–	ns
t_{RS}	Reset Pulse Width [2]	50	–	65	–	80	–	120	–	ns
t_{RSS}	Reset Set-up Time	50	–	65	–	80	–	120	–	ns
t_{RSR}	Reset Recovery Time	15	–	15	–	20	–	20	–	ns
t_{RTC}	Retransmit Cycle Time	65	–	80	–	100	–	140	–	ns
t_{RT}	Retransmit Pulse Width [2]	50	–	65	–	80	–	120	–	ns
t_{RTS}	Retransmit Set-up Time	50	–	65	–	80	–	120	–	ns
t_{RTR}	Retransmit Recovery Time	15	–	15	–	20	–	20	–	ns
t_{EFL}	Reset to Empty Flag Low	–	65	–	80	–	100	–	140	ns
t_{HFH}, t_{FFH}	Reset to Half-Full and Full Flag High	–	65	–	80	–	100	–	140	ns
t_{REF}	Read Low to Empty Flag Low	–	45	–	60	–	60	–	60	ns
t_{RFF}	Read High to Full Flag High	–	45	–	60	–	60	–	60	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	50	–	65	–	80	–	120	–	ns
t_{WEF}	Write High to Empty Flag High	–	45	–	60	–	60	–	60	ns
t_{WFF}	Write Low to Full Flag Low	–	45	–	60	–	60	–	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	–	65	–	80	–	100	–	140	ns
t_{RHF}	Read High to Half-Full Flag Low	–	65	–	80	–	100	–	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	50	–	65	–	80	–	120	–	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	–	50	–	65	–	80	–	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	–	50	–	65	–	80	–	120	ns
t_{XI}	$\overline{XI}$ Pulse Width	50	–	65	–	80	–	120	–	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	–	10	–	10	–	110	–	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	–	15	–	15	–	15	–	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read dataflow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

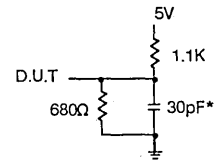


Figure 1. Output Load

*Includes jig and scope capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)(1)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN} (3)	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT} (2, 3)	Output Capacitance	V_{OUT} = 0V	12	pF

NOTES:
1. This parameter is sampled and not 100% tested.
2. With output deselected.
3. Characterized values, not currently tested.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0 – D_8)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2 (i.e. t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after master Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs (Q_0 through Q_8) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations, with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first device loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7203/7204 can be made to retransmit data when the Retransmit Enable ControL ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 2048/4096 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$) depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 2048 writes for the IDT7203 and 4096 writes for the IDT7204.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is one location from the write pointer, indicating that the device is empty. If the write pointer is not moved after reset ($\overline{RS}$), the Empty Flag ($\overline{EF}$) will go low after 2048 reads for the IDT7203 and 4096 reads for the IDT7204.

EXPANSION OUT/HALF FULL FLAG ($\overline{XO}/\overline{HF}$)

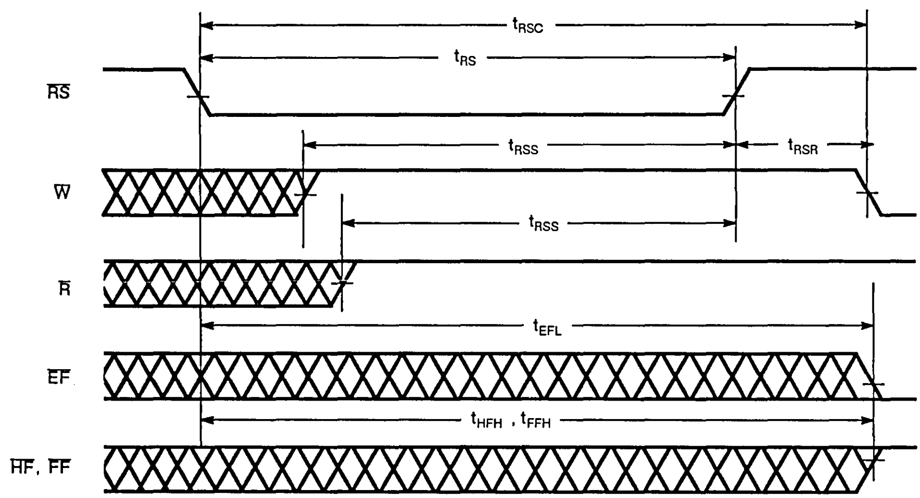
This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q_0 - Q_8)

Q_0 - Q_8 are data outputs for 9-bit wide data. These output are in a high impedance condition whenever Read ($\overline{R}$) is in a high state.



NOTES:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

Figure 2. Reset

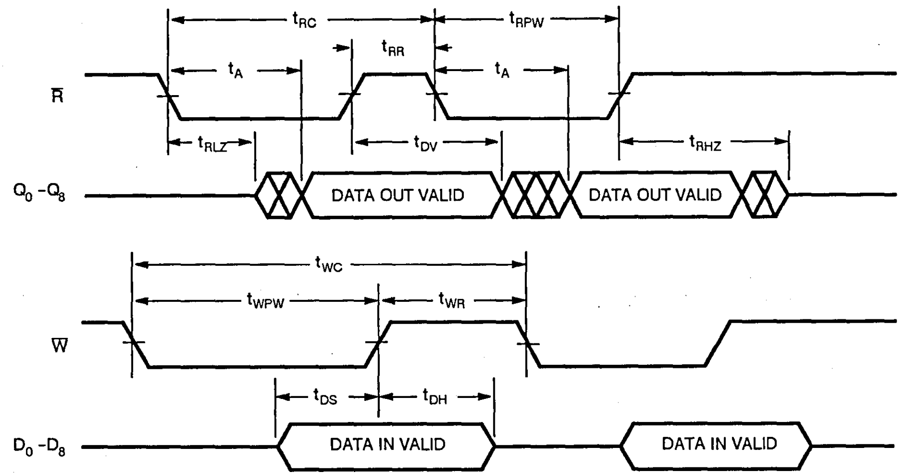


Figure 3. Asynchronous Write and Read Operation

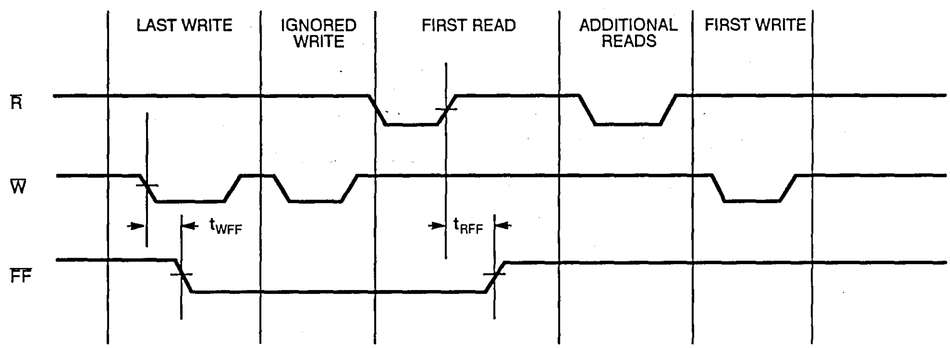


Figure 4. Full Flag From Last Write to First Read

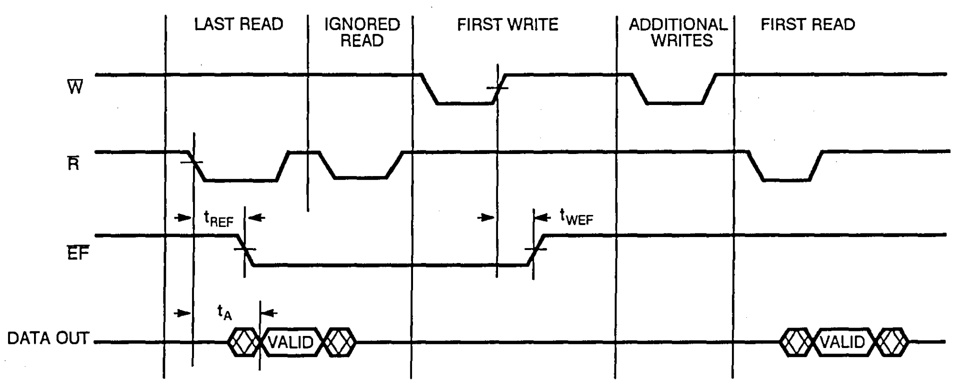
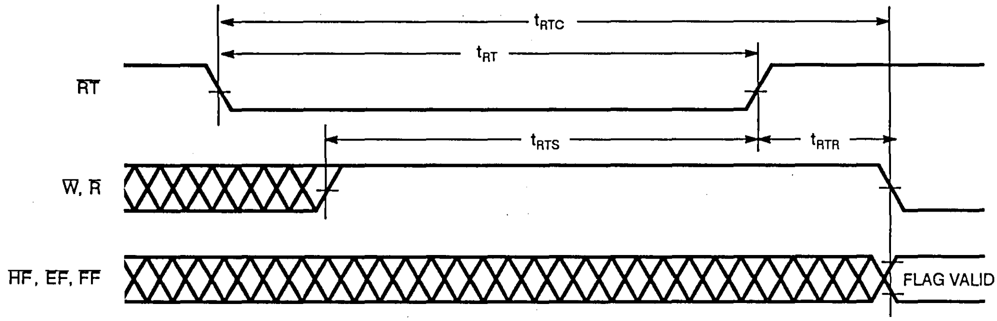


Figure 5. Empty Flag From Last Read to First Write



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

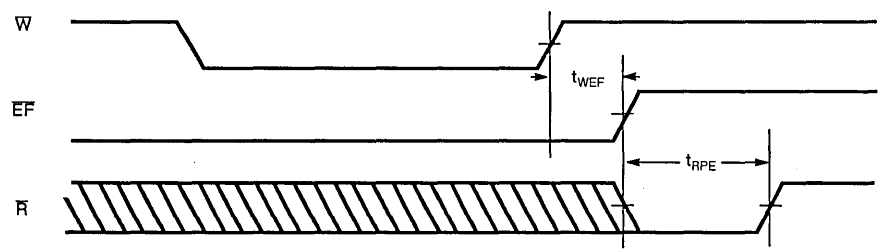


Figure 7. Empty Flag Timing

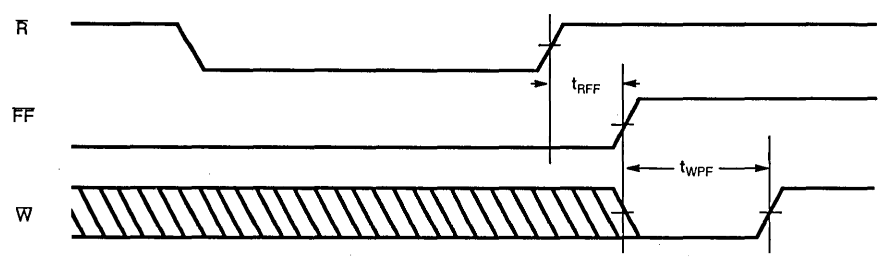


Figure 8. Full Flag Timing

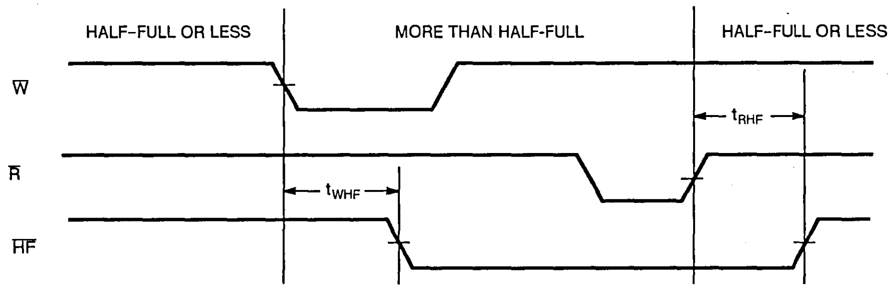


Figure 9. Half-Full Flag Timing

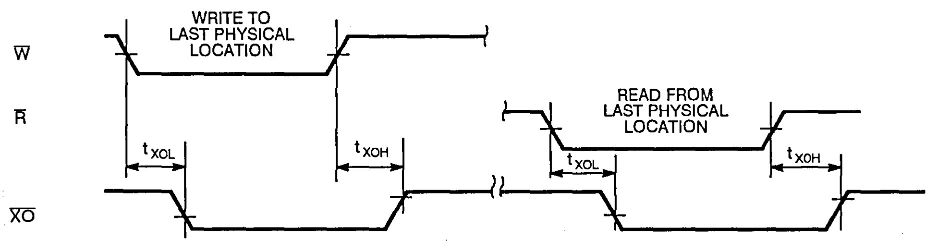


Figure 10. Expansion Out

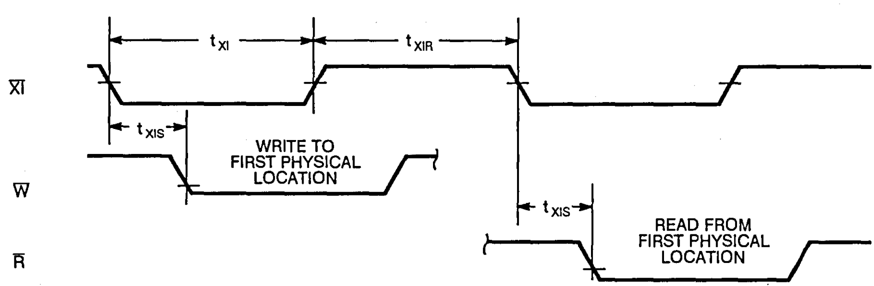


Figure 11. Expansion In

OPERATING MODES:

SINGLE DEVICE MODE

A single IDT7203/7204 may be used when the application requirements are for 2048/4096 words or less. The IDT7203/7204 are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 10). In this mode, the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).

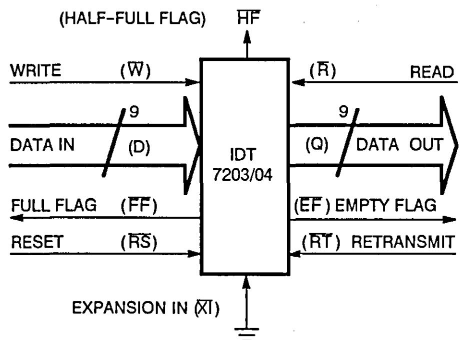
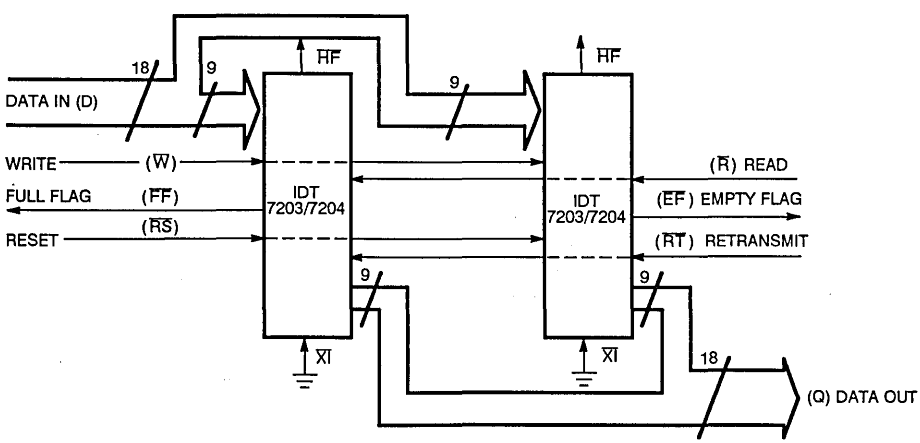


Figure 12. Block Diagram of Single 2048 x 9/4096 x 9 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7203/7204s. Any word width can be attained by adding additional IDT7203/7204s.



NOTE:

Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 13. Block Diagram of 2048 x 18/4096 x 18 FIFO Memory Used in Width Expansion Mode

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7203/7204 can easily be adapted to applications when the requirements are for greater than 2048/4906 words. Figure 14 demonstrates Depth Expansion using three IDT7203/7204s. Any depth can be attained by adding additional IDT7203/7204. The IDT7203/7204 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7203/7204s as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each systems (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge will deassert the empty flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information, refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs".

TRUTH TABLES

TABLE I—RESET AND RETRANSMIT—

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II—RESET AND FIRST LOAD TRUTH TABLE—

DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

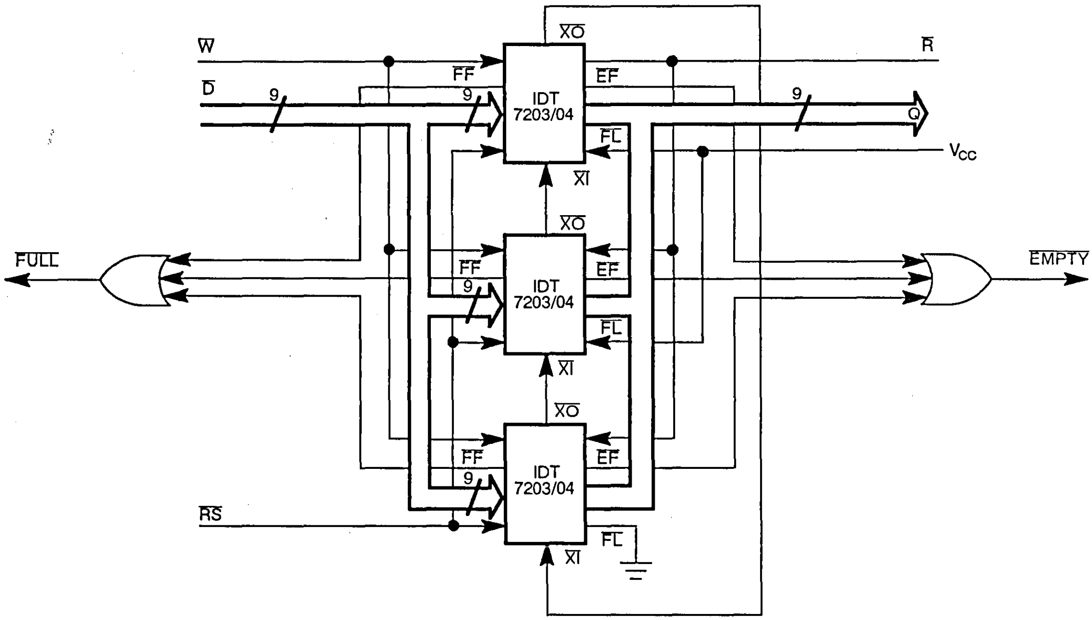
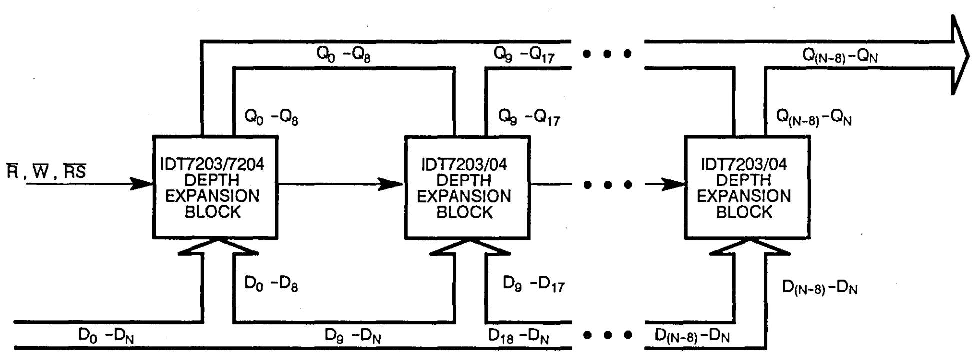


Figure 14. Block Diagram of 6,144 x 9/12,288 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

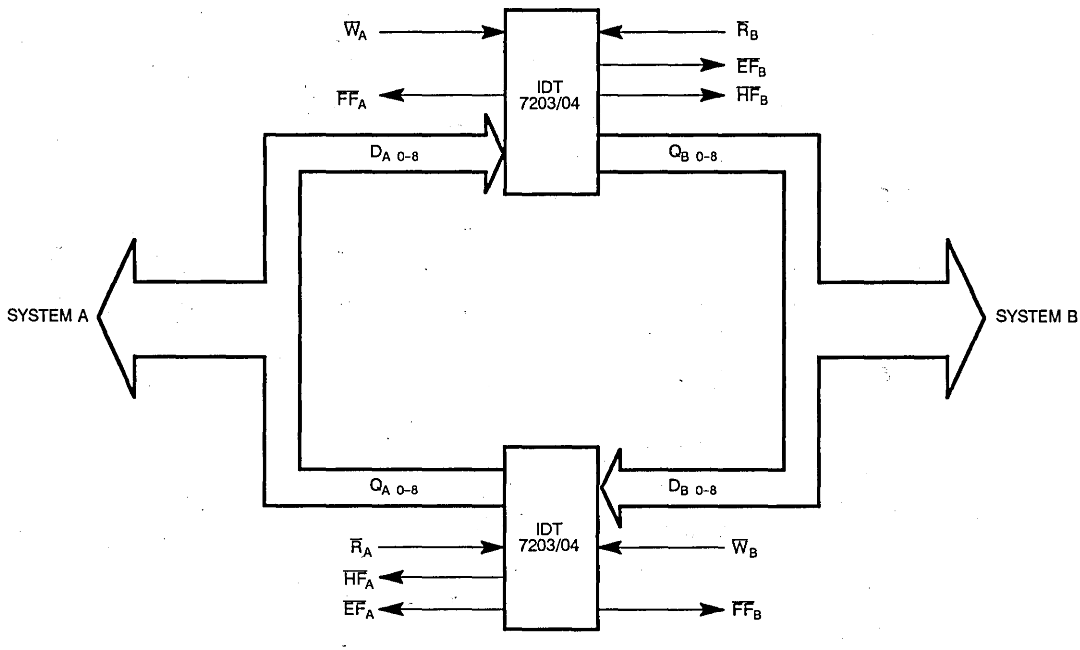


Figure 16. Bidirectional FIFO Mode

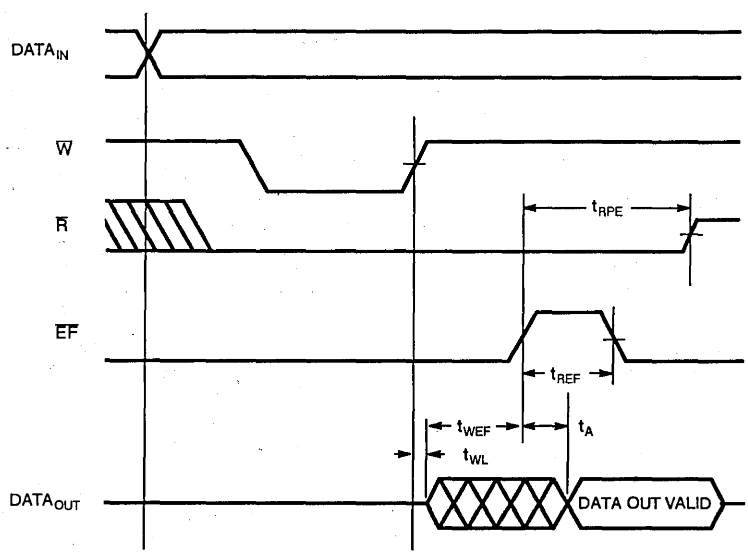


Figure 17. Read Data Flow-Through Mode

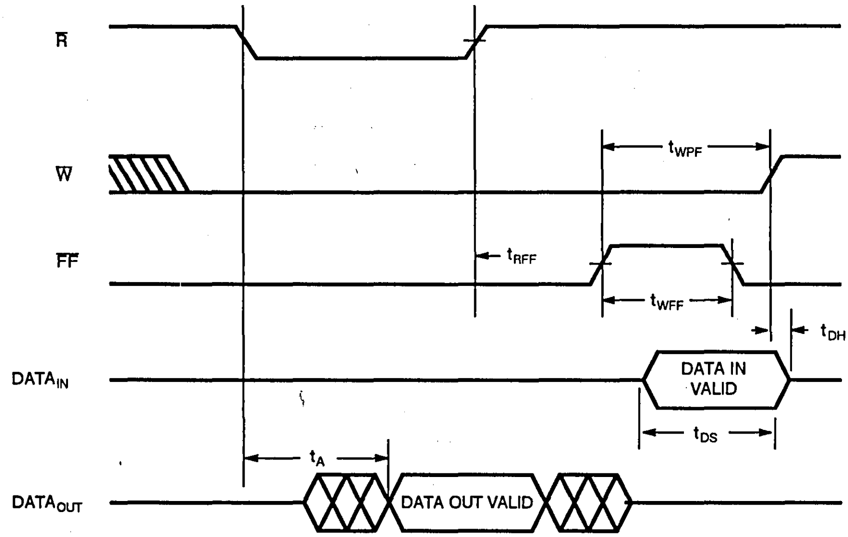


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (−55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	J	Plastic Leaded Chip Carrier
	L	Leadless Chip Carrier
Speed	50	Access Time (t_A) Speed in Nanoseconds
	65	
	80	
	120	
Power	S	Standard Power
	L	Low Power
Device Type	7203	2045 x 9-Bit FIFO
	7204	4096 x 9-Bit FIFO

Integrated Device Technology, Inc.

4K x 9-BIT CMOS PARALLEL FIFO WITH FLAGS

ADVANCE INFORMATION
IDT72041

FEATURES:

- First-In/First-Out (FIFO) dual-port memory
- 4K x 9-bit organization
- Ultra high speed: 35ns access time, 45ns cycle time (22MHz)
- Fully expandable by both word depth and/or bit width
- Asynchronous and simultaneous read and write
- Functionally equivalent to the IDT7204 but with Output Enable and Almost-Empty/Full Flag
- Four status flags: Full, Empty, Half-Full (single device mode) and Almost-Empty/Full (1/8 or 7/8) signal on 0, 512, 2048, 3584, and 4096-byte boundaries
- Output Enable controls the data output port
- Auto retransmit capability
- Master/Slave multiprocessing applications
- Video frame buffer or laser printer buffer applications
- Available in 32-pin DIP and surface mount 32-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72041 is a dual-port memory that utilizes a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device has Full, Empty, Half-Full and Almost-Empty/Full flags to prevent data overflow or underflow. Expansion logic allows wider and/or deeper FIFOs to be created using multiple devices, without external logic.

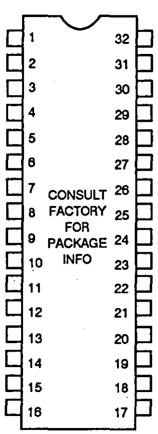
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The device has a read/write access time of 35ns and a read/write cycle time of 45ns (22MHz). The IDT72041 can perform asynchronous and simultaneous read and write operations.

The IDT72041 utilizes a 9-bit wide dual-port RAM array to allow for zero fall-through time and to allow the user to store tag or parity bits. This 9-bit feature is useful in data communications applications where transmission/reception error checking is necessary. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position, when RT is pulsed low, to allow for retransmission of data from the beginning. Four status flags prevent the overflow or underflow of the FIFO and permit interrupt signals to be sent to the transmitting data source.

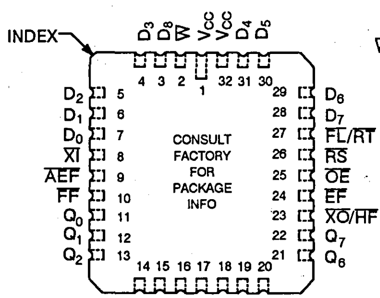
The IDT72041 is fabricated using IDT's high-performance CEMOS™ technology, which combines high speed and low power consumption. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, for high-reliability systems.

6

PIN CONFIGURATIONS

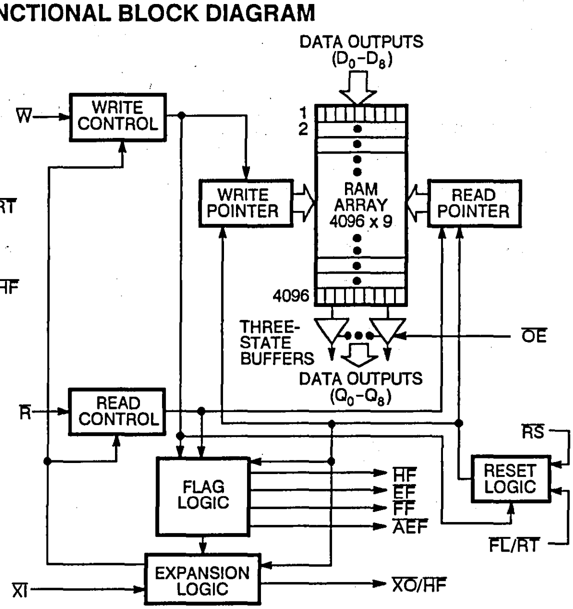


DIP
TOP VIEW



LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 8K x 9-BIT

ADVANCE INFORMATION
IDT7205

FEATURES:

- First-In/First-Out dual-port memory
- 8K x 9-bit organization
- Low power consumption
- Ultra high speed: 65ns cycle time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin-compatible with IDT7200/01/02/03/04 FIFO family
- Half-Full Flag capability in single device mode
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning flags
- Auto retransmit capability
- High-performance submicron CEMOS ™ technology
- Available in 28-pin plastic DIP, CERDIP and 32-pin surface mount LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7205 is a dual-port memory that utilizes a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

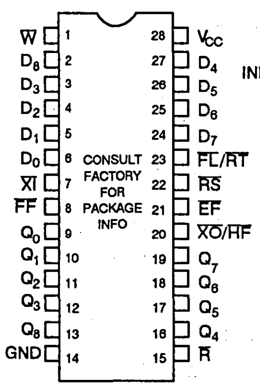
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 65ns (15MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a RETRANSMIT ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position, when $\overline{RT}$ is pulsed low, to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

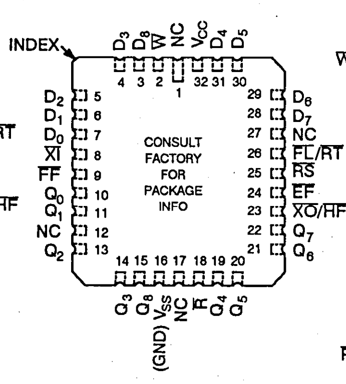
The IDT7205 is fabricated using IDT's high-speed CEMOS submicron technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 8K x 9 organization allows a 8196 deep word structure without the need for expansion.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

PIN CONFIGURATIONS

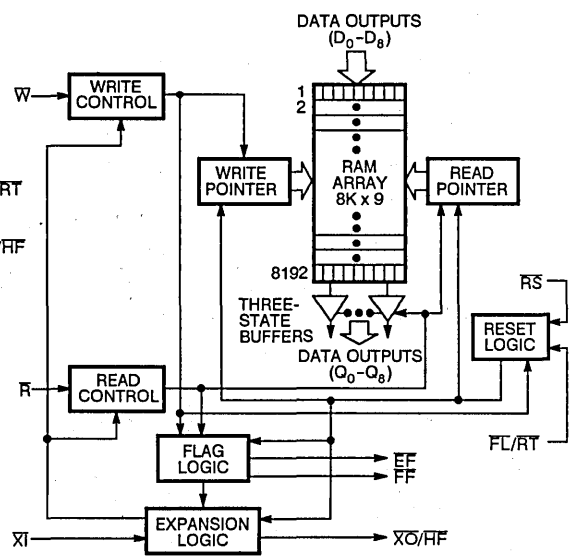


DIP
TOP VIEW



LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

Integrated Device Technology, Inc.

CMOS PARALLEL-SERIAL FIFO 2048 x 9-BIT & 4096 x 9-BIT

IDT72103
IDT72104

FEATURES:

- 50ns parallel port access time
- 40MHz serial input/output port frequency
- Serial-to-Parallel, Parallel-to-Serial, Serial-to-Serial and Parallel-to-Parallel operations
- Easily expandable in depth and width
- Programmable wordlengths from 4 bits to any bit width using Flexishift™ for serial operations without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Full-Minus-One, Empty, Almost-Empty (1/8 from empty), Empty-Plus-One and Half-Full
- Asynchronous and simultaneous read and write operations
- Dual-ported zero fall-through time architecture
- Output enable control provided for parallel output port
- Retransmit capability in single device mode
- High-performance CEMOS™ technology
- Available in 40-pin ceramic and plastic DIP, 44-pin LCC and J-Leaded PLCC
- Military product compliant to MIL-STD-883, Class B

APPLICATIONS:

- High-Speed Data Acquisition Systems
- Local Area Network Buffers
- Remote Telemetry Buffers
- Serial Link Buffers
- High-Speed Parallel Bus-to-Bus Serial Communications
- Magnetic Media Controllers
- Single Chip Video Frame Buffers
- FAX/Printer Buffers

DESCRIPTION:

The IDT72103/72104 are high-speed Parallel-Serial FIFOs that are ideally suited for serial communications, high-density media storage and local area networks.

The devices have four ports: two 9-bit parallel ports and the other two for serial input and serial output. A variety of operations can be performed: Serial-to-Parallel, Parallel-to-Serial, Serial-to-Serial and Parallel-to-Parallel. The Parallel-Serial FIFOs can expand in depth or width for any of these modes.

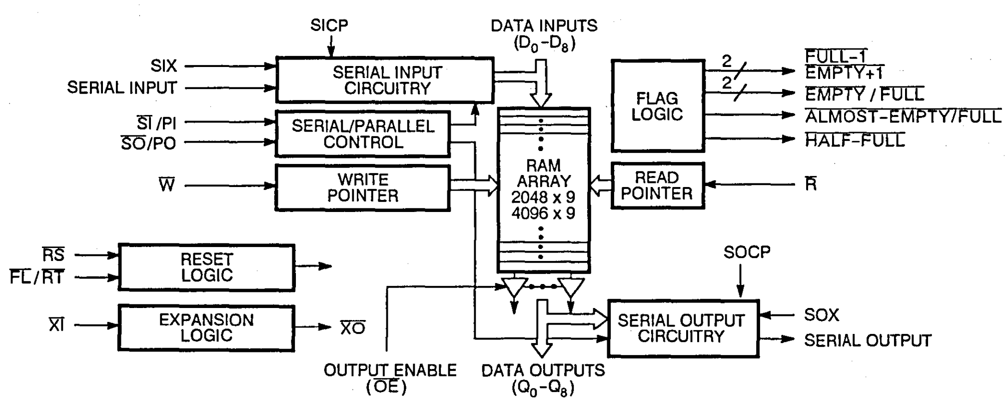
A unique feature that enhances the bandwidth is the handling of serial wordlengths that are not a multiple of 9. The IDT72103/72104 can be configured to handle serial wordlengths from 4 bits to words of any length using multiple devices. This feature is provided without using any additional ICs. For example, a user can configure a 4K x 24 FIFO by using three devices to generate internal increments to the read/write pointers every 24 cycles.

A number of flags are provided to monitor the status of the FIFO. These include Full, Almost-Full (when the FIFO is more than 7/8 full), Full-Minus-One (when the FIFO has one or zero locations left), Empty, Almost-Empty (when the FIFO is less than 1/8 full), Empty-Plus-One (when there is only one or zero samples left in the FIFO) and Half-Full.

Read and Write controls are provided to permit asynchronous and simultaneous operations. An Output Enable control is provided on the parallel output port. Expansion control pins $\overline{XO}$ and $\overline{XI}$ are provided to allow cascading for deeper FIFOs.

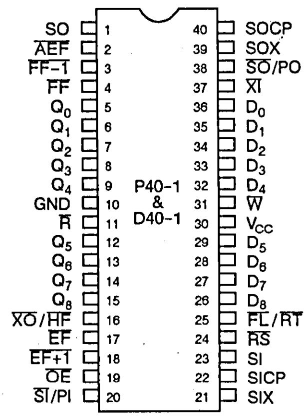
The IDT72103/72104 are manufactured using IDT's CEMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

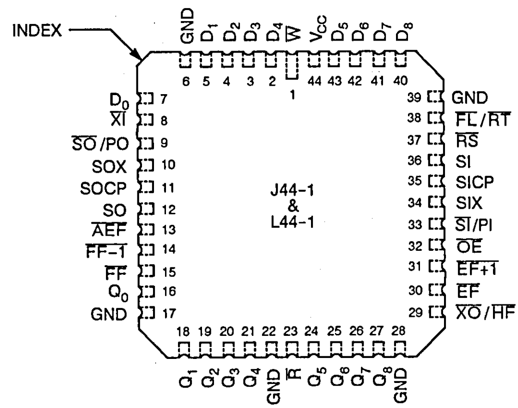


CEMOS and Flexishift are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL} (1)	Input Low Voltage Commercial & Military	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT72103/IDT72104 COMMERCIAL MIN.	TYP.	MAX.	IDT72103/IDT72104 MILITARY MIN.	TYP.	MAX.	UNIT
I_{IL} (1)	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	μA
I_{OL} (2)	Output Leakage Current	-10	–	10	-10	–	10	μA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -2mA (5)	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA (6)	–	–	0.4	–	–	0.4	V
I_{CC1} (3)	Power Supply Current	–	90	140	–	100	160	mA
I_{CC2} (3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	–	8	12	–	12	25	mA
I_{CC3} (L) (3, 4)	Power Down Current	–	–	2	–	–	4	mA
I_{CC3} (S) (3, 4)	Power Down Current	–	–	8	–	–	12	mA

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{OUT}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$
3. I_{CC} measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = $\overline{W}$ = $\overline{R}$ = V_{CC} -0.2V; all other inputs $\geq V_{CC}$ -0.2V or $\leq$ 0.2V
5. For SO, I_{OUT} = -8mA.
6. For SO, I_{OUT} = 16mA

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	FIGURE	72103x50 72104x50 MIN.	MAX.	72103x65 72104x65 MIN.	MAX.	72103x80 72104x80 MIN.	MAX.	72103x120 72104x120 MIN.	MAX.	UNIT
f_S	Parallel I/O Shift Frequency	–	–	15	–	12.5	–	10	–	7	MHz
f_{SOCP}	Serial-Out Shift Frequency	–	–	40	–	33	–	28	–	25	MHz
f_{SICP}	Serial-In Shift Frequency	–	–	40	–	33	–	28	–	25	MHz
PARALLEL-OUTPUT MODE TIMINGS											
t_A	Access Time	23	–	50	–	65	–	80	–	120	ns
t_{RR}	Read Recovery Time	23	15	–	15	–	20	–	20	–	ns
t_{RPW}	Read Pulse Width	23	50	–	65	–	80	–	120	–	ns
t_{RC}	Read Cycle Time	23	65	–	80	–	100	–	140	–	ns
t_{WLZ}	Write Pulse Low to Data Bus at Low Z [1]	1	15	–	15	–	20	–	20	–	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z [1]	23	10	–	10	–	10	–	10	–	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z [1]	23	–	30	–	30	–	35	–	35	ns
t_{DV}	Data Valid from Read Pulse High	23	5	–	5	–	5	–	5	–	ns
PARALLEL INPUT MODE TIMINGS											
t_{DS}	Data Set-up Time	24	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	24	5	–	10	–	10	–	10	–	ns
t_{WC}	Write Cycle Time	24	65	–	80	–	100	–	140	–	ns
t_{WPW}	Write Pulse Width	24	50	–	65	–	80	–	120	–	ns
t_{WR}	Write Recovery Time	24	15	–	15	–	20	–	20	–	ns
RESET TIMINGS											
t_{RSC}	Reset Cycle Time	18	65	–	80	–	100	–	140	–	ns
t_{RS}	Reset Pulse Width	18	50	–	65	–	80	–	120	–	ns
t_{RSS}	Reset Set-up Time	18	50	–	65	–	80	–	120	–	ns
t_{RSR}	Reset Recovery Time	18	15	–	15	–	20	–	20	–	ns
RESET TO FLAGS DELAYS											
t_{RSF1}	Reset to $\overline{EF}$, $\overline{AEF}$ and $\overline{EF+1}$ Low	18	–	65	–	80	–	100	–	140	ns
t_{RSF2}	Reset to $\overline{HF}$, $\overline{FF}$ and $\overline{FF-1}$ High	18	–	65	–	80	–	100	–	140	ns
RESET TO TIME DELAYED OUTPUTS—SERIAL MODE ONLY											
t_{RSQL}	Reset Going Low to Q_{0-8} Low	–	35	–	50	–	65	–	105	–	ns
t_{RSQH}	Reset Going High to Q_{0-8} High	–	35	–	50	–	65	–	105	–	ns
t_{RSDL}	Reset Going Low to D_{0-8} Low	–	35	–	50	–	65	–	105	–	ns
RETRANSMIT TIMINGS											
t_{RTC}	Retransmit Cycle Time	19	65	–	80	–	100	–	140	–	ns
t_{RT}	Retransmit Pulse Width	19	50	–	65	–	80	–	120	–	ns
t_{RTS}	Retransmit Set-up Time	19	50	–	65	–	80	–	120	–	ns
t_{RTR}	Retransmit Recovery Time	19	15	–	15	–	20	–	20	–	ns
PARALLEL MODE FLAG PROPAGATION DELAYS											
t_{REF}	Read Low to $\overline{EF}$ Low	25	–	45	–	60	–	60	–	60	ns
t_{RFF}	Read High to $\overline{FF}$ High	26	–	45	–	60	–	60	–	60	ns
t_{RF}	Read High to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	27	–	65	–	80	–	100	–	140	ns
t_{RE}	Read Low to Transitioning $\overline{AEF}$ and $\overline{EF+1}$	28	–	65	–	80	–	100	–	140	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	1	50	–	65	–	80	–	120	–	ns
t_{WEF}	Write High to $\overline{EF}$ High	25	–	45	–	60	–	60	–	60	ns
t_{WFF}	Write Low to $\overline{FF}$ Low	26	–	45	–	60	–	60	–	60	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	27	–	65	–	80	–	100	–	140	ns
t_{WE}	Write High to Transitioning $\overline{AEF}$ and $\overline{EF+1}$	28	–	65	–	80	–	100	–	140	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ High	2	50	–	65	–	80	–	120	–	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	FIGURE	72103x50 72104x50		72103x65 72104x65		72103x80 72104x80		72103x120 72104x120		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
DEPTH EXPANSION MODE DELAYS											
t_{XOL}	Read/Write to $\overline{XO}$ Low	20	–	50	–	65	–	80	–	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	20	–	50	–	65	–	80	–	120	ns
t_{XI}	$\overline{XI}$ Pulse Width	21	50	–	65	–	80	–	120	–	ns
t_{XIR}	$\overline{XI}$ Recovery Time	21	10	–	10	–	10	–	10	–	ns
t_{XIS}	$\overline{XI}$ Set-up Time	21	15	–	15	–	15	–	15	–	ns
SERIAL INPUT MODE TIMINGS											
t_{S2}	Serial Data In Set-up Time to SICP Rising Edge	30	15	–	15	–	20	–	20	–	ns
t_{H2}	Serial Data In Hold Time to SICP Rising Edge	30	0	–	0	–	5	–	5	–	ns
t_{S3}	SIX Set-up Time to SICP Rising Edge	30	5	–	5	–	5	–	5	–	ns
t_{S4}	$\overline{W}$ Set-up Time to SICP Rising Edge	30	5	–	5	–	5	–	5	–	ns
t_{H4}	$\overline{W}$ Hold Time to SICP Rising Edge	30	7	–	10	–	12	–	15	–	ns
t_{SICW}	Serial In Clock Width High/Low	30	10	–	10	–	15	–	15	–	ns
t_{S5}	$\overline{SI}$/PI Set-up Time to SICP Rising Edge	30	50	–	65	–	80	–	120	–	ns
SERIAL OUTPUT MODE TIMINGS											
t_{S6}	$\overline{SO}$/PO Set-up Time to SOCP Rising Edge	29	50	–	65	–	80	–	120	–	ns
t_{S7}	SOX Set-up Time to SOCP Rising Edge	29	5	–	5	–	5	–	5	–	ns
t_{S8}	$\overline{R}$ Set-up Time to SOCP Rising Edge	29	5	–	5	–	5	–	5	–	ns
t_{H8}	$\overline{R}$ Hold Time to SOCP Rising Edge	29	7	–	10	–	12	–	15	–	ns
t_{SOCW}	Serial In Clock Width High/Low	29	10	–	10	–	15	–	15	–	ns
SERIAL MODE RECOVERY TIMINGS											
t_{REFSO}	Recovery Time SOCP After $\overline{EF}$ Goes High	32	50	–	65	–	80	–	120	–	ns
t_{REFSI}	Recovery Time SICP After $\overline{FF}$ Goes High	32	15	–	15	–	20	–	20	–	ns
SERIAL MODE FLAG PROPAGATION DELAYS											
t_{SOCEF}	SOCP Rising Edge (Bit 0 - First Word) to $\overline{EF}$ Low	32	–	25	–	30	–	30	–	30	ns
t_{SOCFF}	SOCP Rising Edge (Bit 0 - First Word) to $\overline{FF}$ High	31	–	40	–	50	–	60	–	60	ns
t_{SOCF}	SOCP Rising Edge (Bit 0 - Second Word) to $\overline{FF-1}$, $\overline{HF}$, $\overline{AEF}$, $\overline{EF+1}$ High	31	–	40	–	50	–	60	–	60	ns
t_{SICEF}	SICP Rising Edge (Bit 0 - First Word) to $\overline{EF}$ High	34	–	65	–	80	–	80	–	80	ns
t_{SICFF}	SICP Rising Edge (Bit 0 - First Word) to $\overline{FF}$ Low	34	–	40	–	50	–	60	–	60	ns
t_{SICF}	SICP Rising Edge (Bit 0 - Second Word) to $\overline{EF+1}$, $\overline{HF}$, $\overline{AEF}$, $\overline{FF-1}$ High	33	–	65	–	80	–	80	–	80	ns
SERIAL INPUT MODE DELAYS											
t_{PD1}	SICP Rising Edge to D [1]	30	5	20	5	25	5	30	5	35	ns
SERIAL OUTPUT MODE DELAYS											
t_{PD2}	SOCP Rising Edge to Q[1]	29	5	20	5	25	5	30	5	30	ns
t_{SOHZ}	SOCP Rising Edge to SO at High-Z[1]	29	5	16	5	20	5	25	5	30	ns
t_{SOLZ}	SOCP Rising Edge to SO at Low-Z [1]	29	5	22	5	22	5	30	5	35	ns
t_{SOPD}	SOCP Rising Edge to Valid Data on SO	29	–	18	–	22	–	30	–	35	ns
OUTPUT ENABLE/DISABLE DELAYS											
t_{OEHZ}	Output Enable to High-Z (Disable)[1]	22	–	16	–	20	–	25	–	30	ns
t_{OELZ}	Output Enable to Low-Z (Enable) [1]	22	5	–	5	–	5	–	5	–	ns
t_{AOE}	Output Enable to Data Valid (Q_{0-8})	22	–	22	–	25	–	30	–	35	ns

NOTE:

1. Guaranteed by design minimum times, not tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

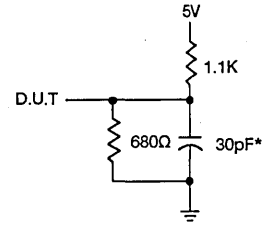


Figure A. Output Load.

*Includes jig and scope capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

GENERAL SIGNAL DESCRIPTIONS:

Inputs:

Data Inputs (D_0-D_8)

In the parallel-in mode ($\overline{SI}$/PI is connected to V_{CC}) D_0-D_8 are the data inputs.

The serial input mode is selected by grounding the $\overline{SI}$/PI pin. The D_{0-8} lines are then outputs which are used to program the width of the serial word.

Reset ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input goes high-to-low. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the Read ($\overline{R}$) and Write ($\overline{W}$) inputs must be high during reset. Half-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).

Write ($\overline{W}$)

A write cycle is initiated on the falling edge of Write if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of Write ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF} allowing a valid write to begin.

Read ($\overline{R}$)

A read cycle is initiated on the falling edge of Read ($\overline{R}$), provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis independent of any ongoing write operations. After Read ($\overline{R}$) goes high, the Data Outputs (Q_{0-8}) will return to a high-impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations with the data outputs remaining in a high-impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

This is a dual-purpose output. In the Multiple Device mode, this pin is grounded to indicate that it is the first device loaded (see Operating Modes). In the Single Device mode, this pin acts as the retransmit input. The Single Device mode is initiated by grounding Expansion In ($\overline{XI}$).

The IDT72103/4 can be made to retransmit data when the Retransmit ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read ($\overline{R}$) and Write ($\overline{W}$) must be high during retransmit. This feature is useful when less than 2048/4096 writes are performed between resets. The retransmit feature is not available in the Depth Expansion mode and will affect Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

Expansion In ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the Single Device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain mode.

Output Enable ($\overline{OE}$)

The parallel output buffers are tri-stated when $\overline{OE}$ is high.

Outputs:

Data Outputs (Q_0-Q_8)

Data outputs for 9-bit wide data. These outputs are in a high impedance condition wherever Read ($\overline{R}$) is in a high state.

Full Flag ($\overline{FF}$)

Full Flag ($\overline{FF}$) is asserted (LOW) when the FIFO is full. When the FIFO is full, the internal write pointer will not be incremented by additional write pulses.

Serial-In Mode

When the FIFO is loaded serially, the Serial-In Clock (SICP) asserts the Full Flag. On the second rising edge of SICP, for the last word in the FIFO, the Full Flag is asserted (LOW) and is only deasserted by a subsequent read operation. Note that when the $\overline{FF}$ is asserted, the last SICP for that word will have to be stretched as shown in Figure 33; otherwise, the data may be scrambled in the next write cycle after a word has been read from the FIFO.

Parallel-In Mode

When the FIFO is in Parallel-In mode, the falling edge of Write asserts the Full Flag (LOW). The Full Flag is deasserted (HIGH) by subsequent read operations—either serial or parallel.

Full-1 Flag ($\overline{FF-1}$)

This flag is asserted (LOW) when the FIFO is one word away from being full. It remains asserted when the FIFO is full.

Expansion Out/Half-Full Flag ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the Single Device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory. After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Multiple Device mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

Almost-Empty or Almost-Full Flag ($\overline{AEF}$)

This flag is asserted (LOW) if there are 0-255 bytes or 1793-2048 bytes in the IDT72103, 2K x 9 FIFO; it is asserted if there are 0-511 or 3585-4096 bytes in the IDT72104, 4K x 9 FIFO.

Empty+1 Flag ($\overline{EF+1}$)

In the parallel output mode, this flag is asserted (LOW) when there is one word or less in the FIFO. It remains LOW when the FIFO is empty.

When in the serial mode, the $\overline{EF+1}$ flag operates as an $\overline{EF+2}$ Flag. The $\overline{EF+1}$ goes LOW when the second to the last word is read from the RAM and is ready to be shifted out. The next word to be read is the next to the last word.

TABLE 1: STATUS FLAGS

NUMBER OF WORDS IN FIFO 2K	4K	$\overline{FF}$	$\overline{FF-1}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF+1}$[(1)]	$\overline{EF}$
0	0	H	H	L	H	L	L
1	1	H	H	L	H	L	H
2-255	2-511	H	H	L	H	H	H
256-1024	512-2048	H	H	H	H	H	H
1025-1792	2049-3584	H	H	H	L	H	H
1793-2046	3585-4094	H	H	L	L	H	H
2047	4095	H	L	L	L	H	H
2048	4096	L	L	L	L	H	H

NOTE:
1. $\overline{EF+1}$ acts as $\overline{EF+2}$ in the serial out mode.

Empty Flag

Parallel-Out Mode

When the FIFO is in the Parallel-Out mode and there is only one word in the FIFO, the falling edge of the $\overline{R}$ line causes the Empty Flag ($\overline{EF}$) line to be asserted (LOW). This is shown in Figure 25. The empty flag is then deasserted (HIGH) by either the rising edge of $\overline{W}$ or rising edge of SICP, as shown in Figure 25.

Serial-Out Mode

The use of the Empty Flag ($\overline{EF}$) is important for proper serial-out operation when the FIFO is almost empty. The $\overline{EF}$ flag is asserted LOW after the first bit of the last word is shifted out. The $\overline{EF}$ flag is brought HIGH at the end of the next write ($\overline{W}$ goes from LOW-to-HIGH). In order to meet internal set-up times, the $\overline{EF}$ flag must be HIGH for a minimum period of time (t_{REFSO}) before the first shift out of the next word. This is analogous to the read flow-through mode in parallel output operation.

For continuous shifting at the highest clock rates, certain considerations apply. If the $\overline{EF}$ goes LOW during the serial shift of a word, it must be HIGH at least one or two serial clocks before the first bit of the next word is started. Otherwise, the clock must be stopped until $\overline{EF}$ has gone HIGH and the minimum set-up period is met. For continuous operation, the $\overline{EF}$ must be tested two clock cycles from the end of the serial word. For slower shift rates, the $\overline{EF}$ can be tested just before starting to shift the first bit of the next word.

SERIAL SIGNAL DESCRIPTIONS:

Serial Input (SI)

Serial data is read into the serial input register via the Serial Input. In both Depth and Serial Word Width Expansion modes, the Serial Input signals of the different IDT72103/4 devices in the expansion array are connected together.

Serial Output (SO)

Serial data is output on the serial output pin. In both Depth and Serial Word Width Expansion modes the Serial Output signals of the different IDT72103/4 devices in the expansion array are connected together. Following reset, the serial output is tri-stated until the first positive edge of the serial output clock signal. Data is clocked out Least Significant Bit first. In the Serial Width Expansion mode, the serial output is tri-stated again after the ninth bit is output.

Serial Input Clock (SICP)

New serial data is read into the serial input register on the rising edge of the Serial Input Clock signal. In both Depth and Serial Word Width Expansion modes, the Serial Input Clock signals of the different IDT72103/4 devices in the expansion array are connected together.

Serial Output Clock (SOCP)

New serial data bits are read from the serial output register on the rising edge of Serial Output Clock signal. In both Depth and Serial Word Width Expansion modes, the Serial Output Clock signals of the different IDT72103/4 parts in the expansion array are connected together.

Serial Input Expansion (SIX)

The Serial Input Expansion pin is tied high for single-device serial-input operation or parallel input operation. In the Serial Input Expansion mode, the SIX pin is tied high on the device that will source the lower order bits of the serial word. The device or devices that source the next higher order serial bits have their SIX pin (or pins) tied to the D_8 pin of the device that will source the next lower order bits of the serial word.

Serial Output Expansion (SOX)

The Serial Output Expansion pin is tied high for single-device serial-output operation or parallel output operation. In the Serial Output Expansion mode, SOX is tied high on the device that will source the lower order bits of the serial word. The device or devices that source the next higher order serial bits have their SOX pin (or pins) tied to the Q_8 pin of the device that will source the next lower order bits of the serial word. Data is clocked out Least Significant Bit first.

Serial/Parallel Input ($\overline{SI}$/PI)

The Serial/Parallel Input pin programs whether the IDT72103/4 accepts parallel or serial data as input. When this pin is low, the FIFO expects serial data and the D_0-D_8 pins become outputs used to program the write signal and, therefore, program the serial input word width. For instance, connecting D_6 to $\overline{W}$ will program a serial word width of 7 bits; connecting D_7 to $\overline{W}$ will program a serial word width of 8 bits and so on.

Serial/Parallel Output ($\overline{SO}$/PO)

The Serial/Parallel Output pin programs whether the IDT72103/4 outputs parallel or serial data. When this pin is low, the FIFO expects serial data and the Q_0-Q_8 pins output signals used to program the read signal and, therefore, program the serial output word width.

Operating the IDT72103/4 FIFO Full and Empty Boundary Conditions

The design of the IDT72103/4 FIFOs gates out write pulses once the FIFO is full and gates out read pulses once the FIFO is empty. Excess writes are ignored and, thus, do not overwrite valid data. Excess reads produce invalid data since the outputs of the FIFO are tri-stated when the Empty Flag is asserted, but but do not read data bytes out of sequence.

The Full and Empty flags signal the full and empty boundary conditions. An internal read cycle cannot begin until the Empty Flag is deasserted and a write cannot begin until the Full Flag is deasserted (Figures 1 and 2).

If Read is low prior to the deassertion of the Empty Flag, or Write is low prior to the deassertion of the Full Flag, they cannot be allowed to go high again until an appropriate minimum read or write pulse time has elapsed (Figure 1—t_{RPE} and Figure 2—t_{WPF}). Failure to observe this boundary condition timing produces internal read and write pulses of excessively short duration and may result in erratic operation.

The parallel outputs are tri-stated unless the Read signal ($\overline{R}$) is low, Output Enable ($\overline{OE}$) is low and the Empty Flag ($\overline{EF}$) is deasserted (HIGH).

6

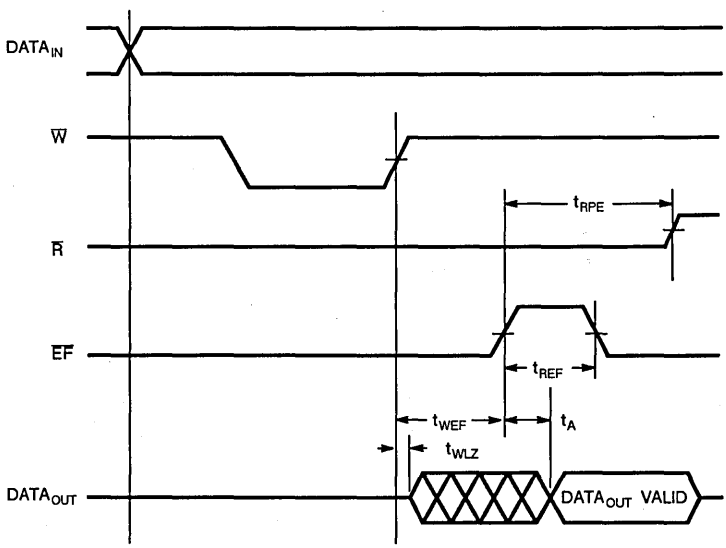


Figure 1. FIFO Empty Boundary Condition Timing

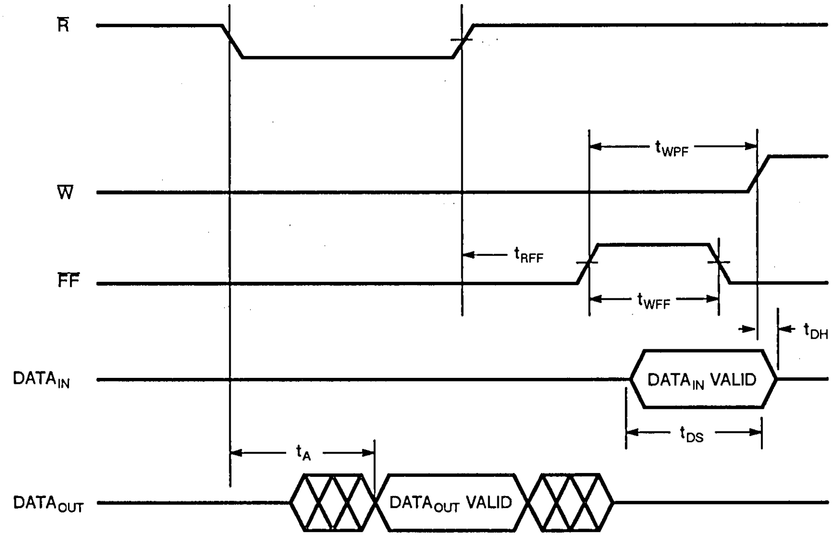


Figure 2. FIFO Full Boundary Condition Timing

Parallel Operating Modes:

Parallel Data Input

By setting S̄I/PI HIGH, the data is written into the FIFO in parallel through the D_{0-8} input data lines. A write cycle is initiated on the falling edge of the Write (W̄) signal provided the Full Flag (F̄F̄) is not asserted. If the W̄ signal changes from HIGH-to-LOW and the Full Flag (F̄F̄) is already set, the write line is inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. The data is written to the RAM at the write pointer. On the rising edge of W̄, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

Parallel Data Output

By setting S̄Ō/PO HIGH, the Parallel-Out mode is chosen. A read cycle is initiated on the falling edge of Read (R̄) provided the Empty Flag is not set. The output data is accessed on a first-in/first-out basis, independent of the ongoing write operations. In the Parallel-Out mode, as shown in Figure 23 the data is available t_A after the falling edge of R̄ and the output bus Q goes into high impedance after R̄ goes HIGH.

Alternately, the user can access the FIFO by keeping R̄ LOW and enabling data on the bus by asserting Output Enable (ŌĒ). When R̄ is LOW, the ŌĒ signal enables data on the output bus. When R̄ is LOW and ŌĒ is HIGH, the output bus is three-stated. When R̄ is HIGH, the output bus is disabled irrespective of ŌĒ. The enable and disable times for Output Enable are shown in Figure 22.

Single Device Mode

A single IDT72103/4 may be used when the application requirements are for 2048/4096 words or less. The IDT72103/4 is in the Single Device Configuration when the Expansion In (X̄Ī) control input is grounded. (See Figure 3.) In this mode the Half-Full Flag (H̄F̄), which is an active low output, is shared with Expansion Out (X̄Ō).

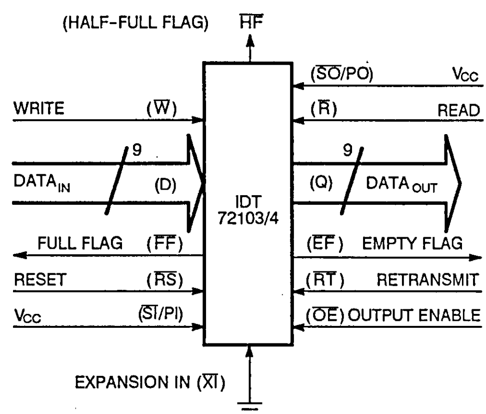
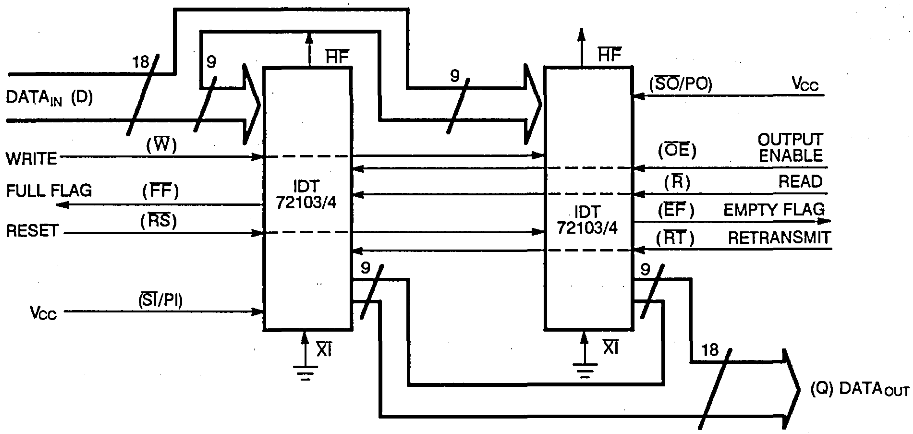


Figure 3. Block Diagram of Single 2048 x 9/4096 x 9 FIFO

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags can be detected from any one device. Figure 4 demonstrates an 18-bit word width by using two IDT72103/4s. Any word width can be attained by adding additional IDT72103/4s.



NOTE:

1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and the $\overline{HF}$ signals of either (any) device used in the width expansion configuration. Do not connect any flag signals together.

Figure 4. Block Diagram of 2048 x 18/4096 x 18 FIFO Memory Used in Width Expansion Mode

TRUTH TABLES
TABLE 2: RESET AND RETRANSMIT– SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{AEF}$, $\overline{EF}$, $\overline{EF+1}$	$\overline{FF}$, $\overline{FF-1}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE:

1. Pointer will increment if appropriate flag is HIGH.

TABLE 3: RESET AND FIRST LOAD TRUTH TABLE– DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

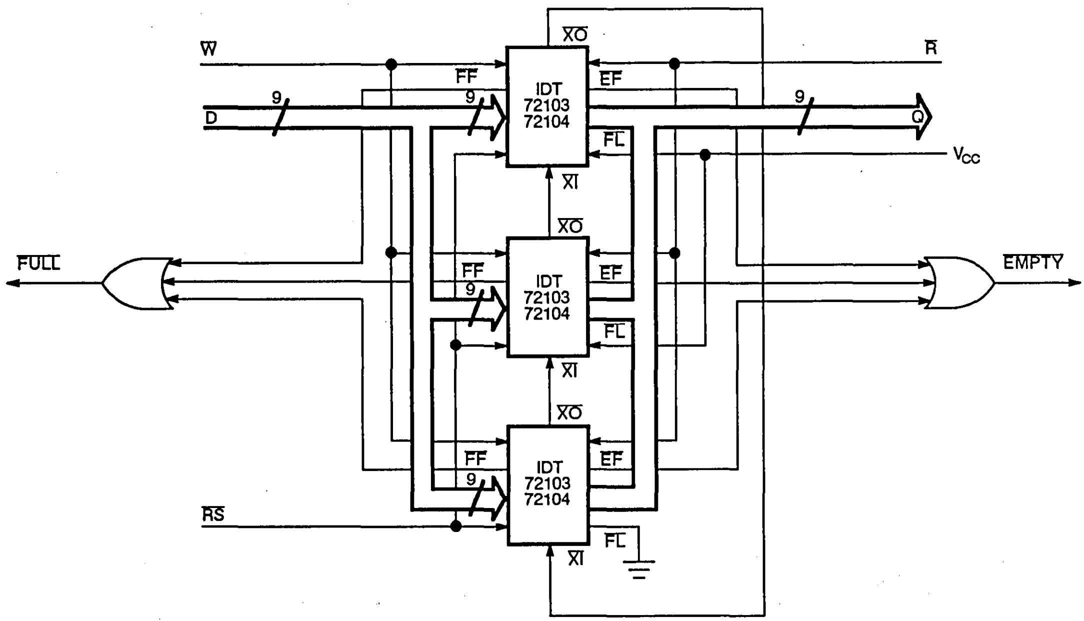
NOTES:

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input

Depth Expansion (Daisy Chain) Mode

The IDT72103/4 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 5 demonstrates Depth Expansion using three IDT72103/4s. Any depth can be attained by adding additional IDT72103/4s. The IDT72103/4 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 5.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 5.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.



NOTE:
1. $\overline{SI}$/PI and $\overline{SO}$/PO pins are tied to V_{CC}.

Figure 5. Block Diagram of 6,144 x 9/12,288 x 9-FIFO Memory, Depth Expansion

Bidirectional Mode

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72103/4 as shown in Figure 6. Both Depth Expansion and Width Expansion may be used in this mode.

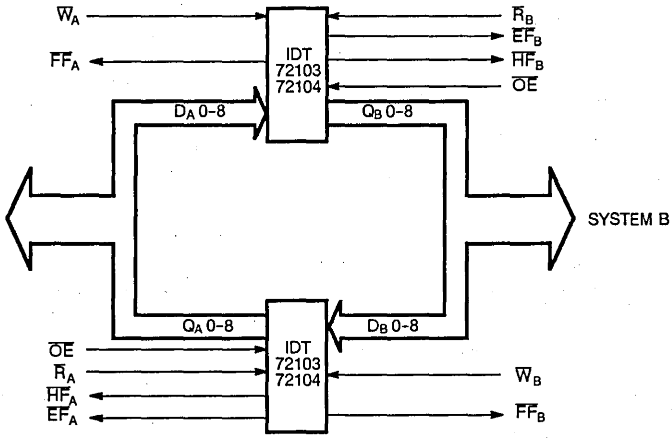
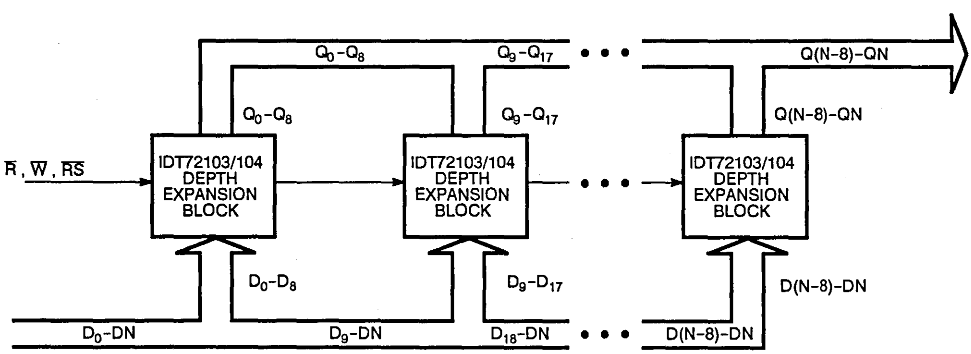


Figure 6. Bidirectional FIFO Mode

Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 7).



NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 5.
2. For Flag detection see WIDTH EXPANSION Section and Figure 4.

Figure 7. Compound FIFO Expansion

Serial Operating Modes

Serial Data Input

The Serial Input mode is selected by grounding the $\overline{SI}$/PI line. The D_{0-8} lines are then outputs which are used to program the width of the serial word. They are taps off a digital delay line which are meant for connection to the $\overline{W}$ input. For instance, connecting D_6 to $\overline{W}$ will program a serial word width of 7 bits, connecting D_7 to $\overline{W}$ will program a serial word width of 8 bits and so on.

By programming the serial word width, an economy of clock cycles is achieved. As an example, if the word width is 6 bits, then on every 6th clock cycle the serial data register is written in parallel into the FIFO RAM array. Thus, the possible clock cycles for an extra 3 bits of width in the RAM array are not required.

The SIX signal is used for Serial-In Expansion. When the serial word width is 9 or less, the SIX input must be tied HIGH. When more than 9 bits of serial word width is required, more than one device is required. The SIX input of the least significant device must be tied HIGH. The D_8 pin of the least significant device must be tied to SIX of the next significant device. In other words, the SIX input of the most significant and intermediate devices must always be connected to the D_8 of the next least significant device.

Figure 8 shows the relationship of the SIX, SICP and D_{0-8} lines. In the standalone case (Figure 8), on the first LOW-to-HIGH of SICP, the D_{1-7} lines go LOW and the D_0 line remains HIGH. On the next SICP clock edge, the D_1 goes HIGH, then D_2 and so on. This continues until the D line, which is connected to $\overline{W}$, goes HIGH. On the next clock cycle, after $\overline{W}$ is HIGH, all of the D lines go LOW again and a new serial word input starts.

In the cascaded case, the first LOW-to-HIGH SICP clock edge for a serial word will cause all timed outputs (D) to go LOW except for D_0 of the least significant device. The D outputs of the least significant device will go high on consecutive clock cycles until D_8. When D_8 goes HIGH, the SIX of the next device goes HIGH. On the next cycle after the SIX input is brought HIGH, the D_0 goes HIGH; then on the next cycle D_1 and so one. A D_i output from the most significant device is issued to create the $\overline{W}$ for all cascaded devices.

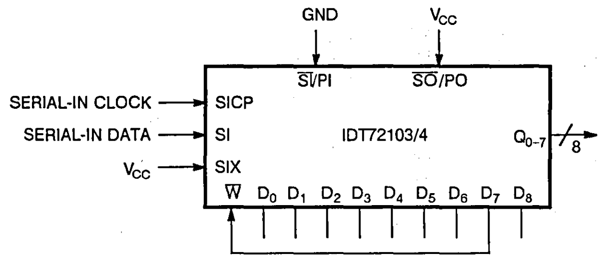
The minimum serial word width is 4 bits and the maximum is virtually unlimited.

When in the Serial mode, the Least Significant Bit of a serial stream is shifted in first. If the FIFO output is in the Parallel mode, the first serial bit will come out on Q_0. The second bit shifted in is on Q_1 and so on.

In the Serial Cascade mode, the serial input (SI) pins must be connected together. Each of the devices then receives serial information together and uses the SIX and D_{0-8} lines to determine whether to store it or not.

The example shown in Figure 10 shows the interconnections for a serializing FIFO that transfers data to the internal RAM in 16-bit quantities (i.e. every 16 SICP cycles). This corresponds to incrementing the write pointer every 16 SICP cycles.

SINGLE DEVICE SERIAL INPUT CONFIGURATION



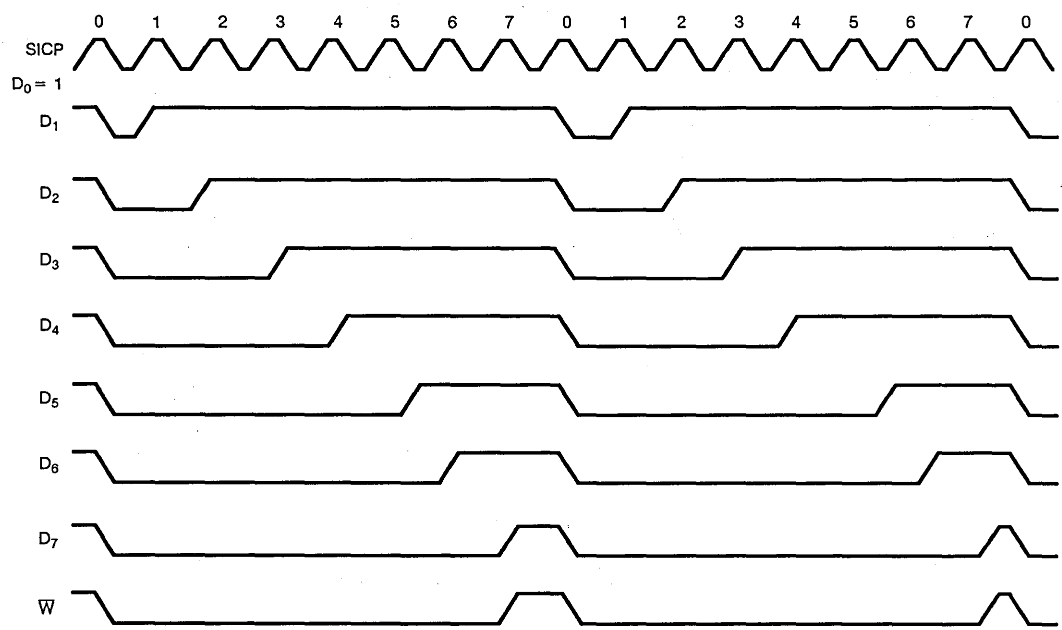


Figure 8. Serial-In Mode Where 8-Bit Parallel Output Data is Read

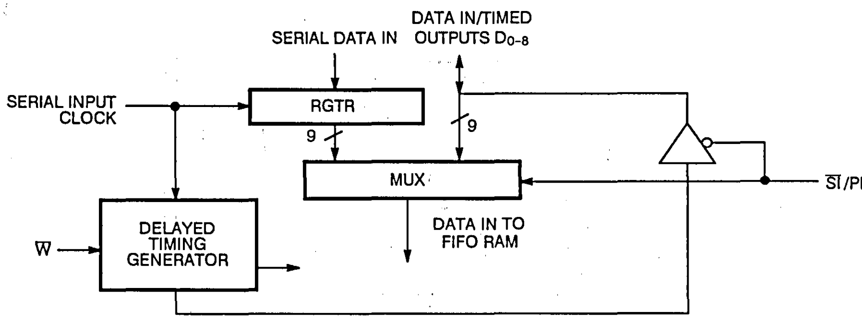


Figure 9. Serial-Input Circuitry

SERIAL INPUT WIDTH EXPANSION

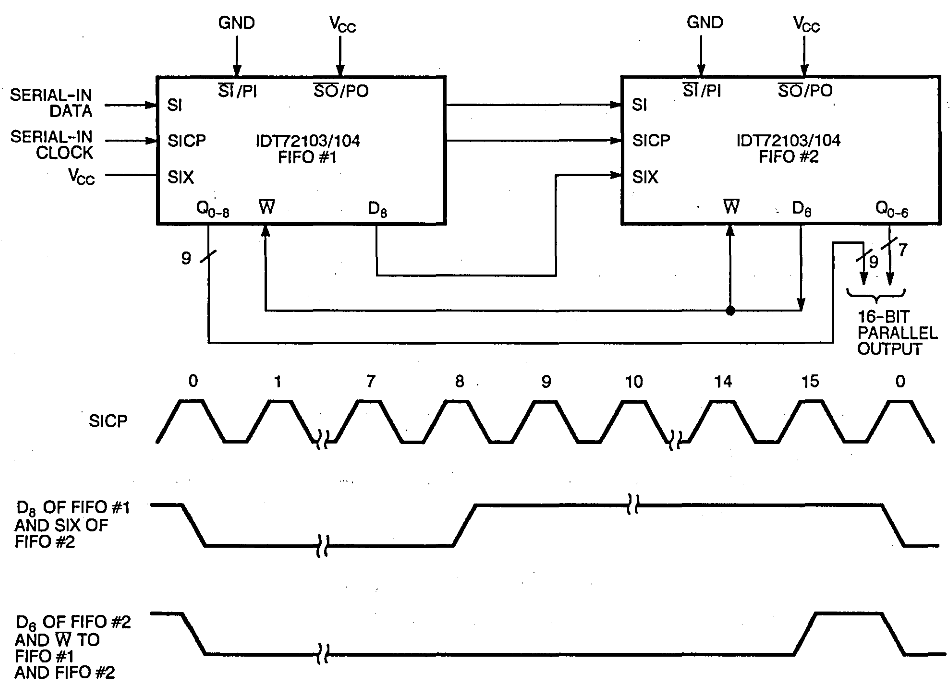
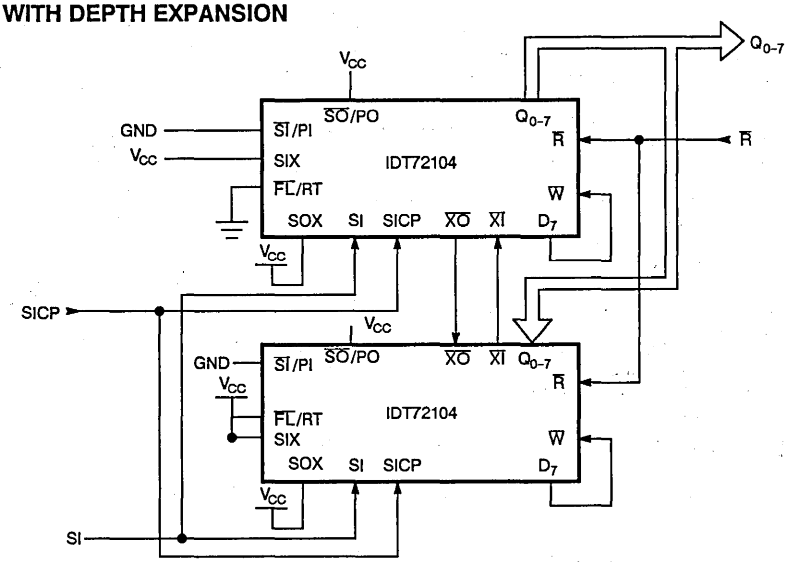


Figure 10. Serial-In Configuration for Serial-In to Parallel-Out Data of 16 bits

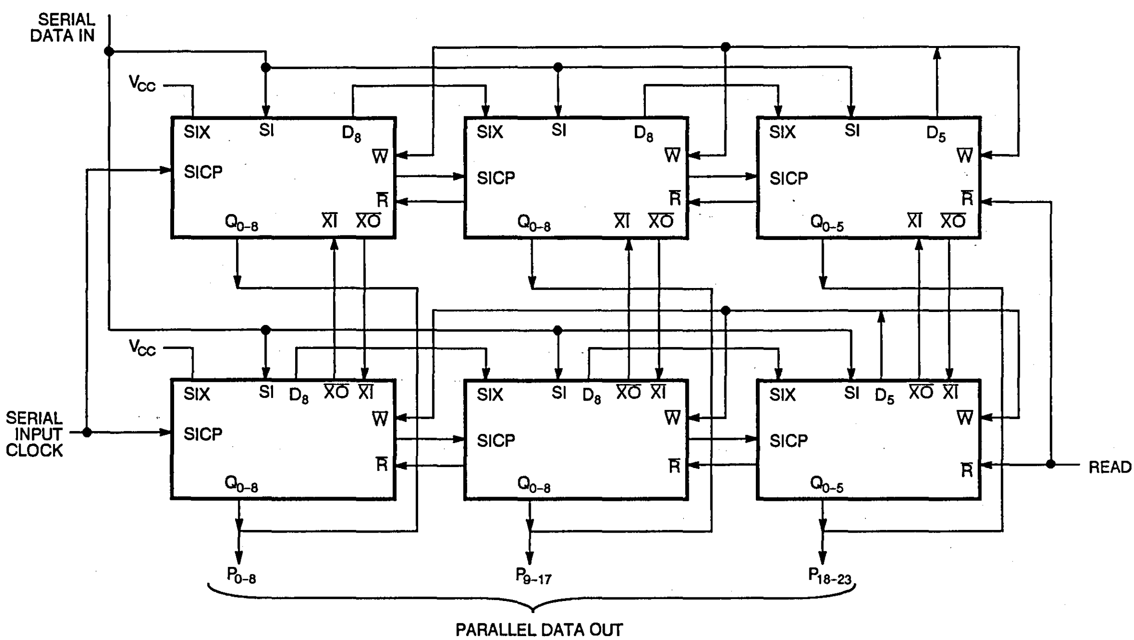
SERIAL INPUT WITH DEPTH EXPANSION



NOTE:
1. All $\overline{SI}$/PI pins are tied to V_{CC} and $\overline{SO}$/PO pins are tied to GND. $\overline{OE}$ is tied HIGH. For $\overline{FF}$ and $\overline{EF}$ connections see Figure 17.

Figure 11. An 8K x 8 Serial-In, Parallel-Out FIFO

SERIAL INPUT WITH WIDTH AND DEPTH EXPANSION



NOTE:
1. All $\overline{SI}$/PI pins is tied to GND. $\overline{SO}$/PO is tied to V_{CC}. For $\overline{FF}$ and $\overline{EF}$ connections see Figure 17.

Figure 12. An 8K x 24 Serial-In, Parallel-Out FIFO Using Six IDT72104s

Serial Data Output

The Serial Output mode is selected by setting the $\overline{SO}$/PO line low. When in the Serial-Out mode, one of the Q_{0-8} lines should be used to control the $\overline{R}$ signal. In the Serial-Out mode, the Q_{0-8} are taps off a digital delay line. By selecting one of these taps and connecting it to the $\overline{R}$ input, the width of the serial word to be read and shifted is programmed. For instance, if the Q_5 line is connected to the $\overline{R}$ input, on every sixth clock cycle a new word is read from the FIFO RAM array and begins to be shifted out. The serial word is shifted out Least Significant Bit first. If the input mode of the FIFO is parallel, the information that was written into the D_0 bit will come out as the fist bit of the serial word. The second bit of the serial stream will be the D_1 bit and so on.

In the standalone case, the SOX line is tied HIGH and not used. On the first LOW-to-HIGH of the SOCP clock, all of the Q outputs except for Q_0 go LOW and a new serial word is started. On the next clock cycle, Q_1 will go HIGH, Q_2 on the next clock and so on, as shown in Figure 13. This continues until the Q line, which is connected to $\overline{R}$, goes HIGH at which point all of the Q lines go LOW on the next clock and a new serial word is started.

In the cascaded case, word widths of more than 9 bits can be achieved by using more than one device. By tying the SOX line of the least significant device HIGH and the SOX of the subsequent devices to Q_8 of the previous devices, a cascaded serial word is achieved. On the first LOW-to-HIGH clock edge of SOCP, all the lines go LOW except for Q_0. Just as in the standalone case, on each consecutive clock cycle, each Q line goes HIGH in order of least to most significant. When Q_8 (which is connected to the SOX input of the next device) goes HIGH, the D_0 of that device goes HIGH, thus cascading from one device to the next. The Q line of the most significant device, which programs the serial word width, is connected to all $\overline{R}$ inputs.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three-statable, only the device which is currently shifting out is enabled and driving the 1-bit bus.

Figure 15 shows an example of the interconnections for a 16-bit serialized FIFO.

SINGLE DEVICE SERIAL OUTPUT CONFIGURATION

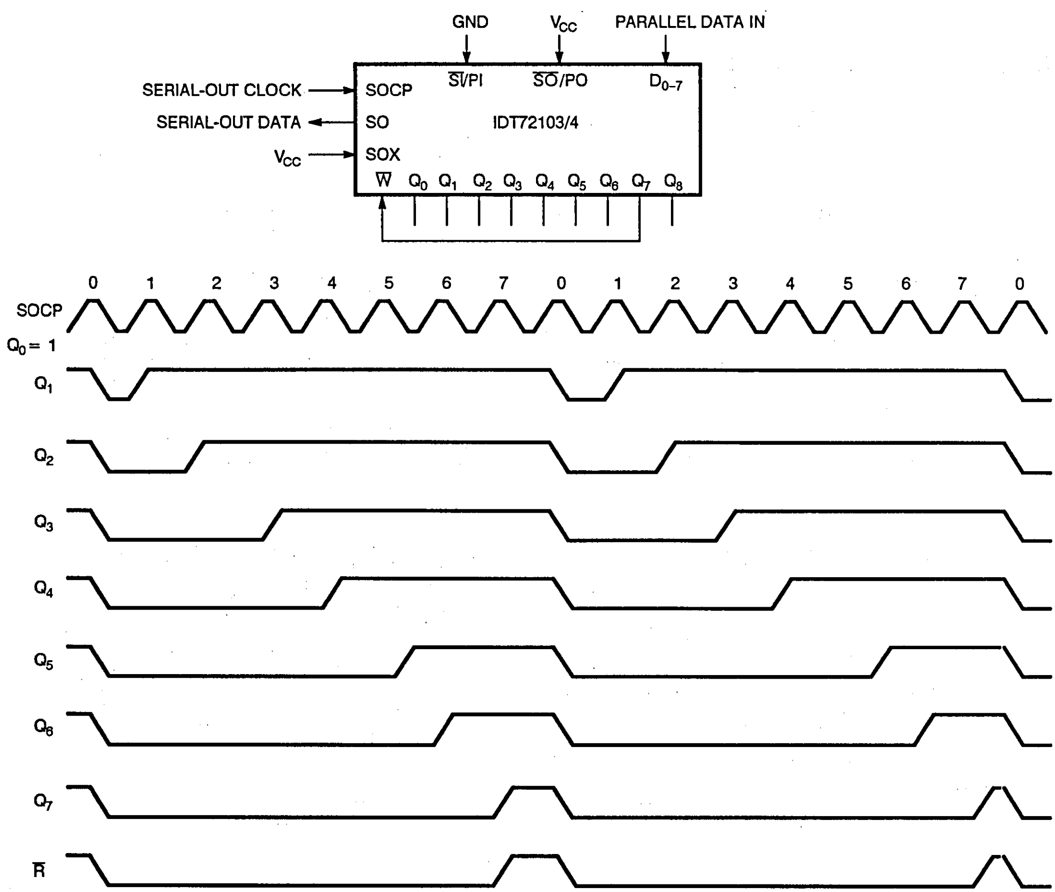


Figure 13. Serial-Out Configuration Where Input Data Is Loaded In 8-Bit Quantities and Read Out Serially

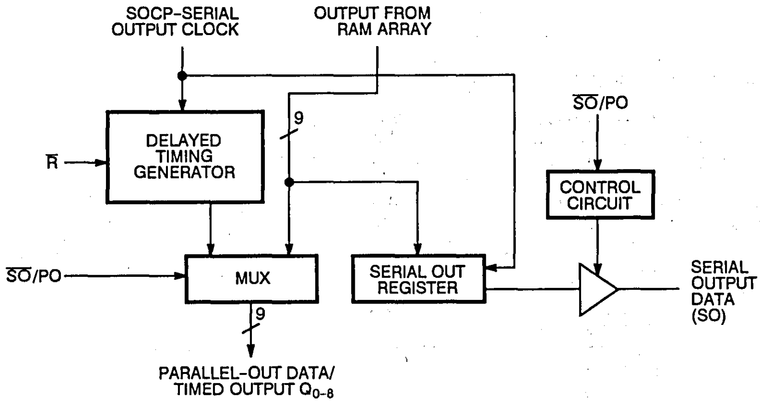


Figure 14. Serial-Output Circuitry

SERIAL-OUT WIDTH EXPANSION

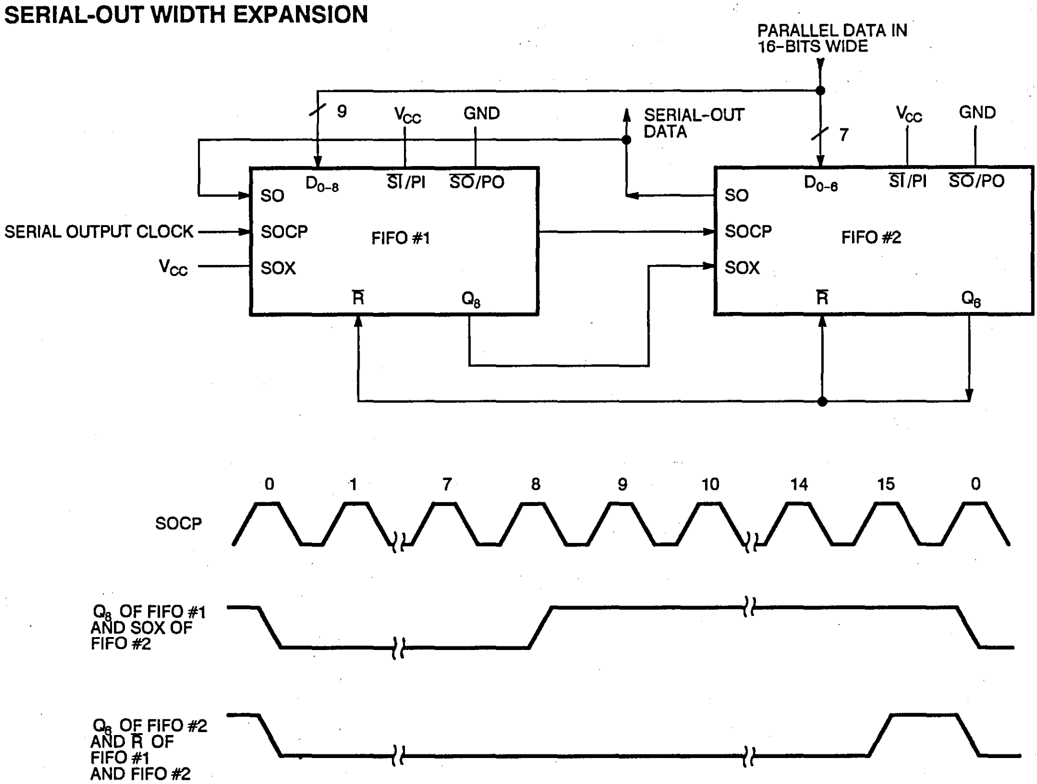
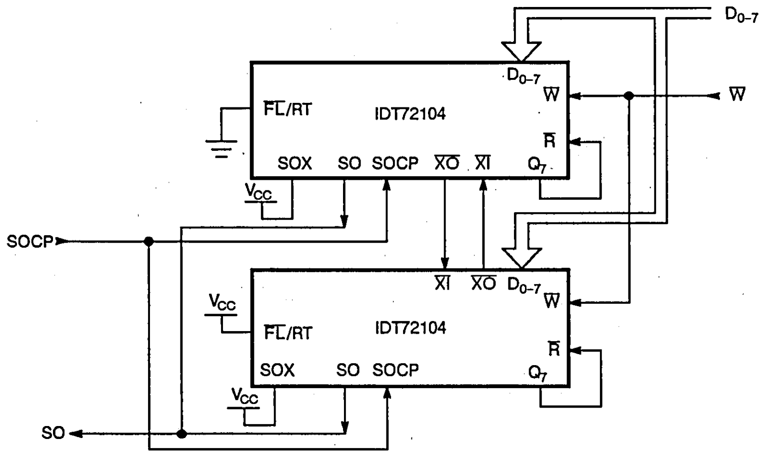


Figure 15. Serial Output for 16-Bit Parallel Data In. The Parallel Data In is tied to D_{0-8} of FIFO #1 and D_{0-6} of FIFO #2

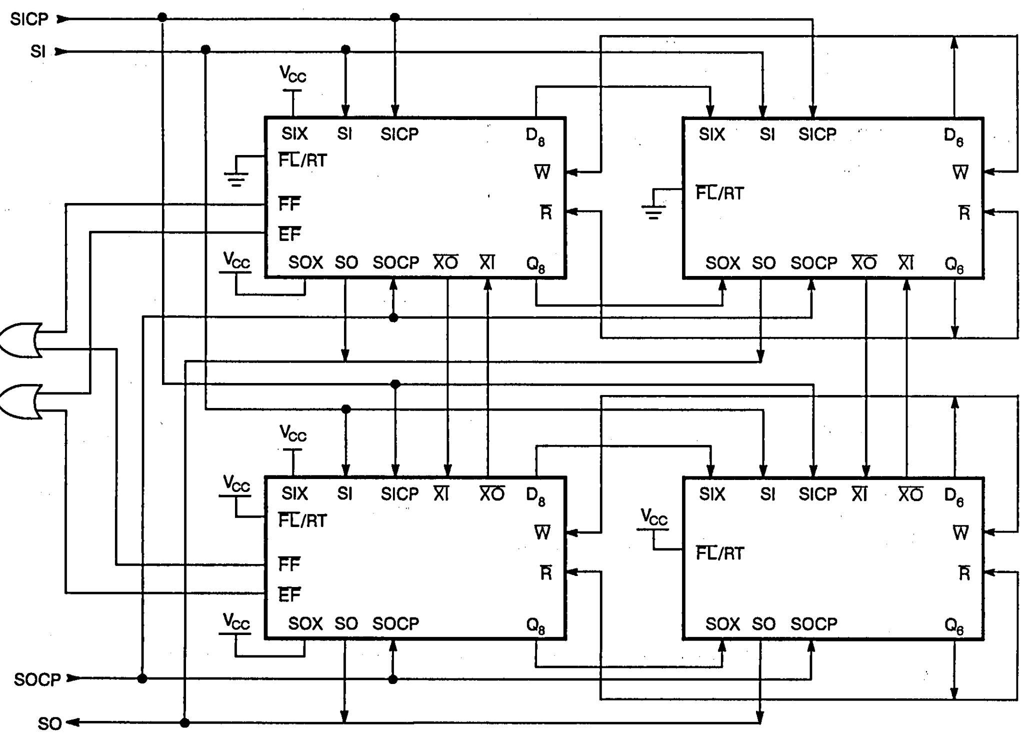
SERIAL OUTPUT WITH DEPTH EXPANSION



NOTE:
1. All SI/PI pins are tied to V_{CC} and SO/PO pins are tied to GND. OE is tied HIGH. For FF and EF connections see Figure 17.

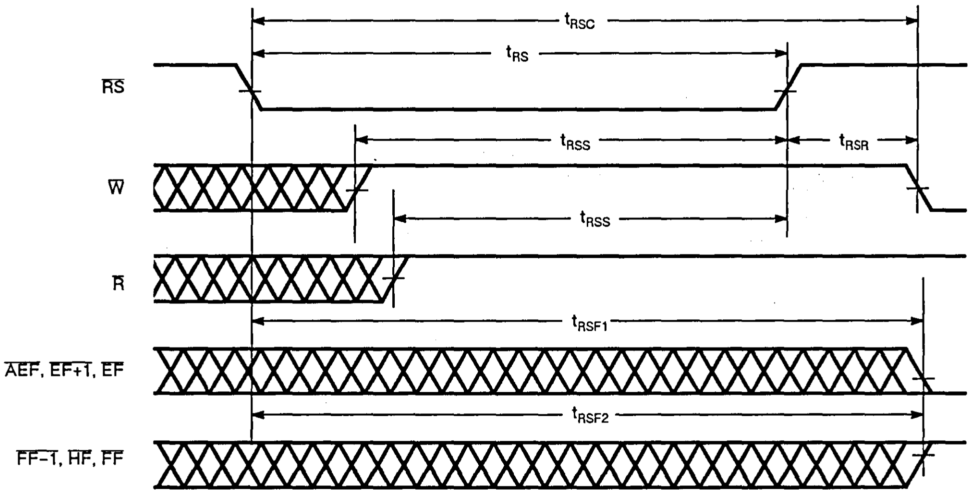
Figure 16. An 8K x 8 Parallel-In Serial-Out FIFO

SERIAL IN AND SERIAL OUT WITH WIDTH AND DEPTH EXPANSION



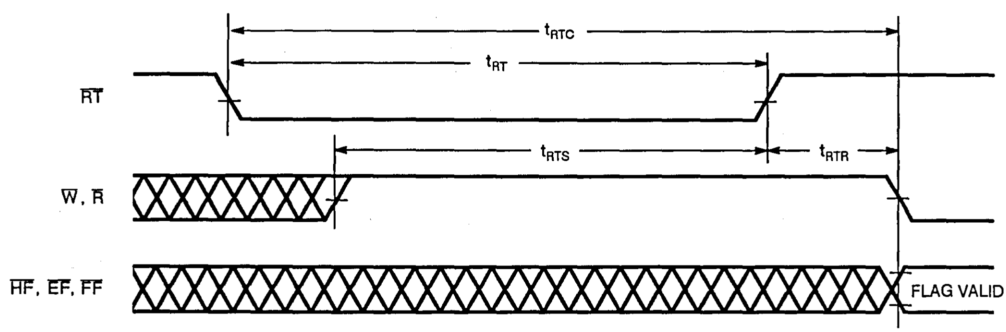
NOTE:
1. All RS pins are connected together. All OE pins are connected HIGH. All SI/PI and SO/PO pins are grounded.

Figure 17. A 128K x 1 Serial-In Serial-Out FIFO



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.

Figure 18. Reset



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$, $\overline{AEF}$, $\overline{FF-1}$ and $\overline{EF+1}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 19. Retransmit

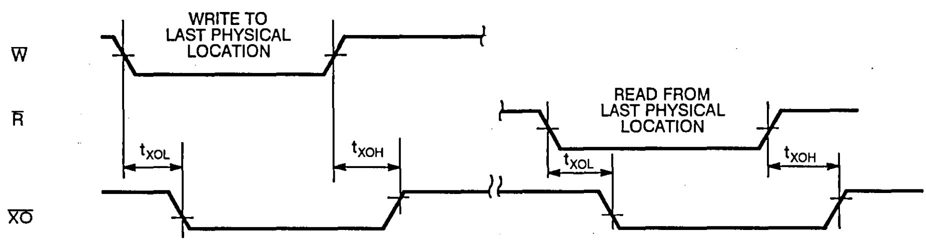


Figure 20. Expansion-Out

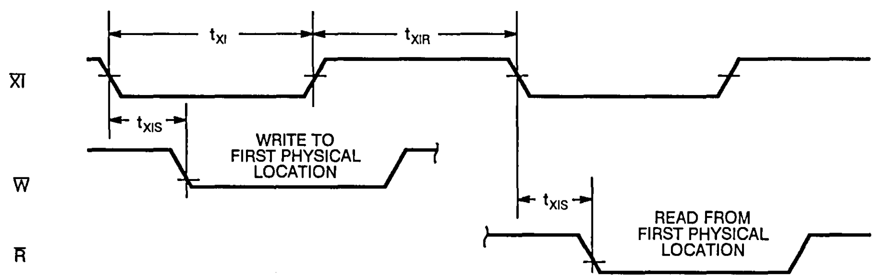


Figure 21. Expansion-In

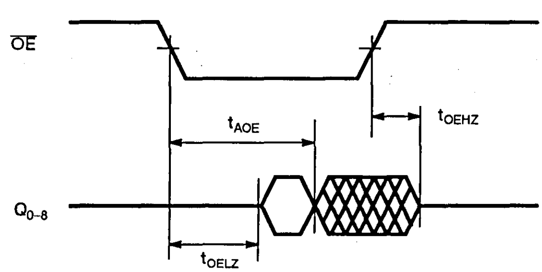


Figure 22. Output Enable Timings

PARALLEL TIMINGS – READ/WRITE

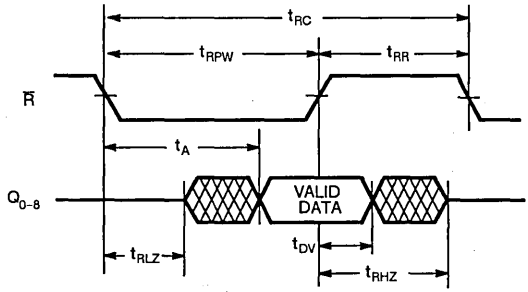


Figure 23. Read Operation in Parallel Data Out Mode

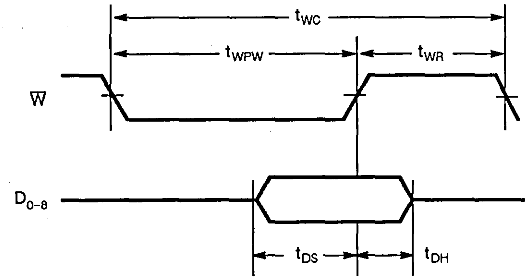
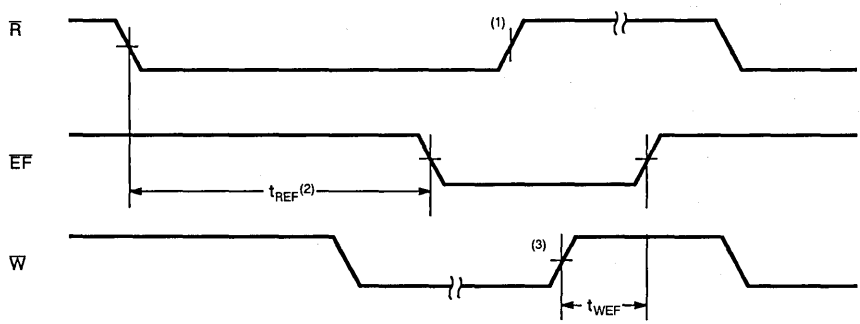


Figure 24. Write Operation in Parallel Data In Mode

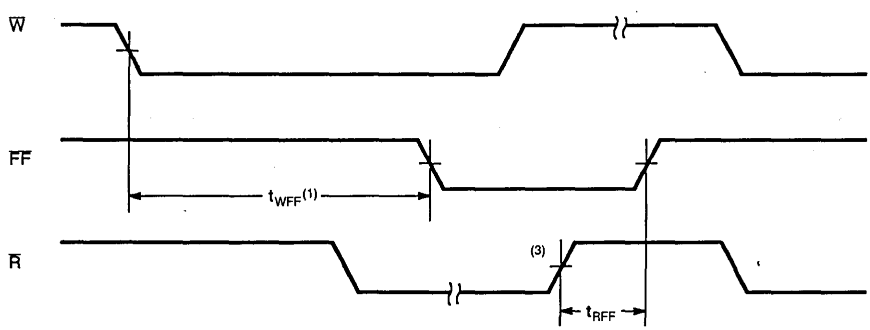
PARALLEL TIMINGS – FLAGS



NOTES:

1. Data is valid on this edge.
2. The Empty Flag is asserted by $\overline{R}$ in the Parallel-Out mode and is specified by t_{REF}. The $\overline{EF}$ flag is deasserted by the rising edge of $\overline{W}$.
3. First rising edge of Write after $\overline{EF}$ is set.

Figure 25. Empty Flag Timings in Parallel-Out Mode



NOTE:

1. For the assertion time, t_{WFF} is used when data is written in the Parallel mode. The $\overline{FF}$ is deasserted by the rising edge of $\overline{R}$.

Figure 26. Full Flag Timings in Parallel-In Mode

PARALLEL TIMINGS – FLAGS

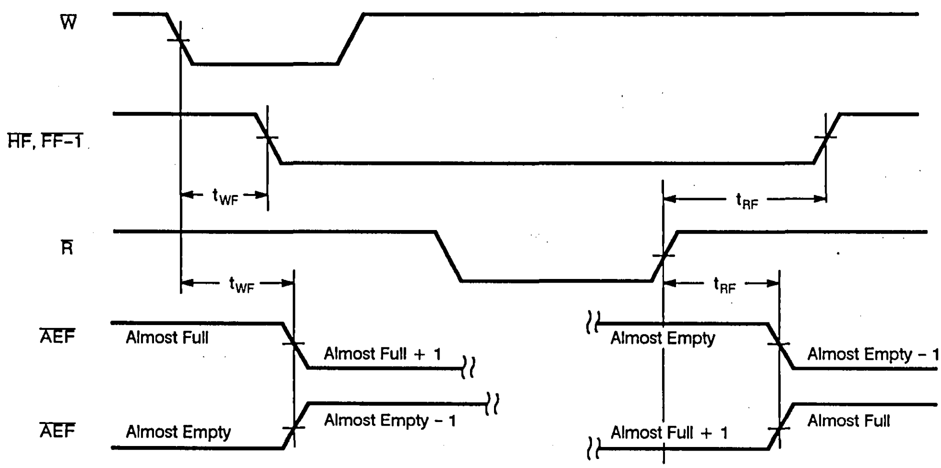


Figure 27. The Almost-Full, Half-Full and Full–1 Flag Timings

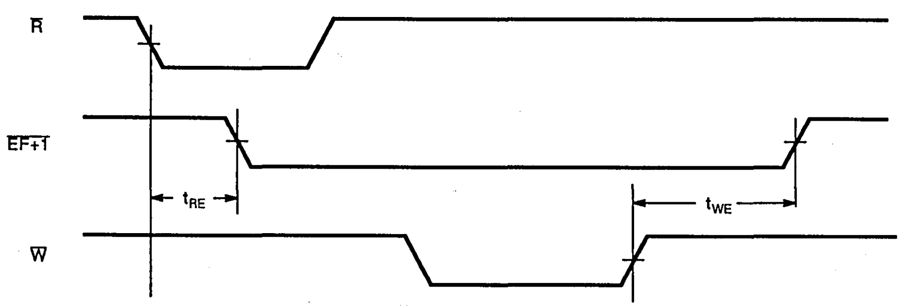
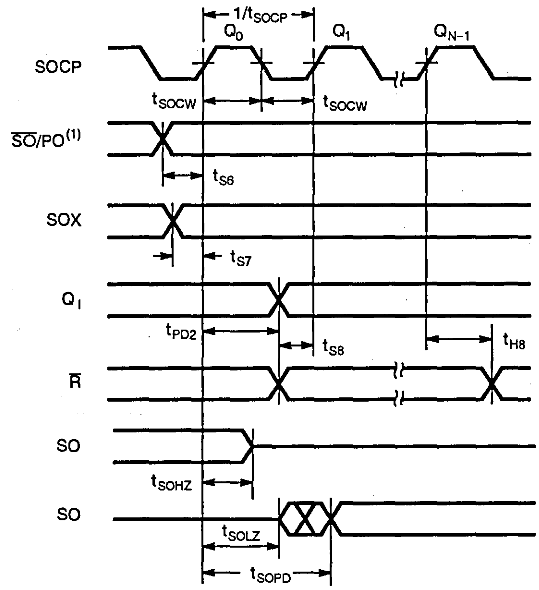


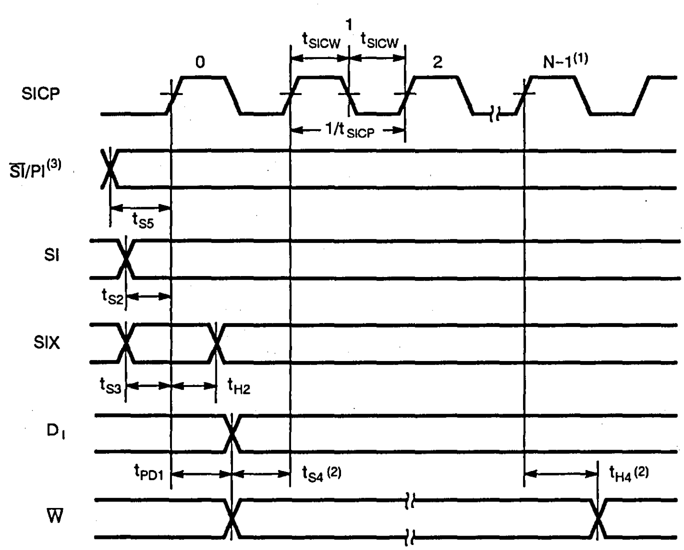
Figure 28. Empty+1 Flag Timings

SERIAL TIMINGS – READ/WRITE



NOTE:
1. After $\overline{SO}$/PO has been set up, it cannot be dynamically changed; it can only be changed after a reset operation.

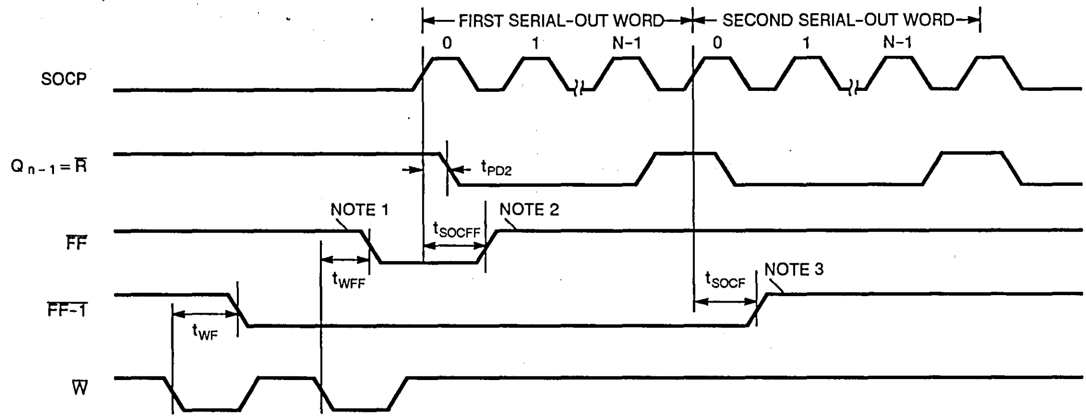
Figure 29. Read Operation In Serial-Out Mode



NOTES:
1. For the Standalone mode, $N \geq 4$ and the input bits are numbered 0 to N–1.
2. For the recommended interconnections, D_I is to be directly tied to $\overline{W}$ and the t_{S4} and t_{H4} requirements will be satisfied. For users that modify $\overline{W}$ externally, t_{S4} and t_{H4} have to be met.
3. After $\overline{SI}$/PI has been set up, it cannot be dynamically changed; it can only be changed after a reset operation.

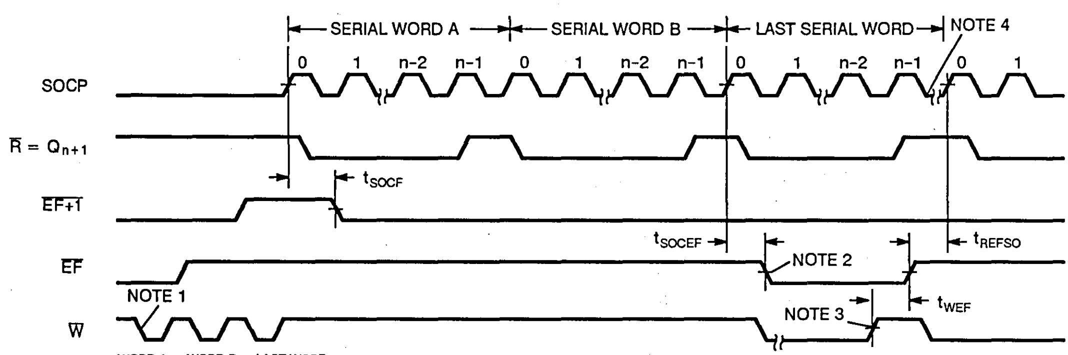
Figure 30. Write Operation In Serial-In Mode

SERIAL TIMINGS – FLAGS



NOTES:
1. The FIFO is full and a new read sequence is starting.
2. On the first rising edge of SOCP, the $\overline{FF}$ is de-asserted. In the Serial-In mode, a new write operation can begin after t_{RFFS1} after $\overline{FF}$ goes HIGH. In the Parallel-In mode, a new write operation can occur immediately after $\overline{FF}$ flag goes HIGH.
3. The $\overline{FF-1}$ Flag is deasserted after the first SOCP of the second serial word.

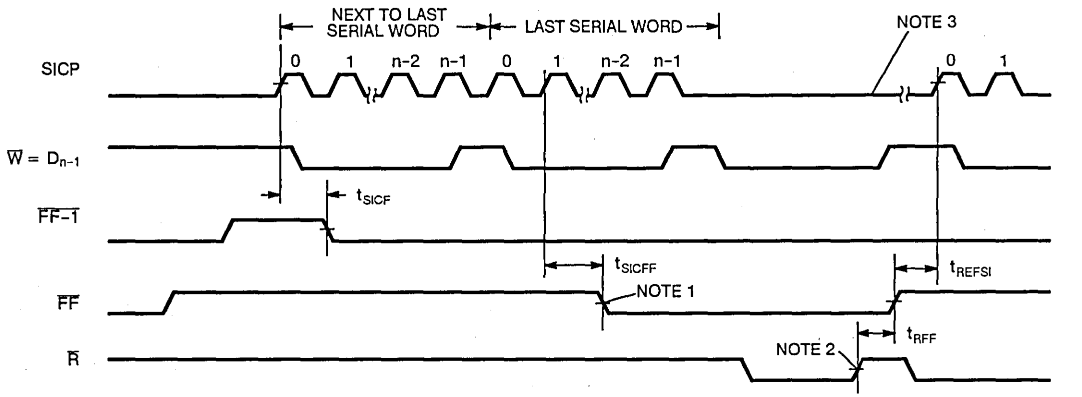
Figure 31. Full Flag and Full–1 Flag Deassertion in the Serial-Out Mode



NOTES:
1. Parallel write shown for reference only. Can also use serial input mode.
2. The Empty Flag is asserted in the Serial-Out mode by using the t_{SOCEF} parameter. This parameter is measured in the worst case from the rising edge of the SOCP used to clock data bit 0. Whenever $\overline{EF}$ goes LOW, there is only one word to be shifted out. In the Parallel-In mode, the $\overline{EF}$ flag is deasserted by the rising edge of $\overline{W}$. In the Serial-In mode, the $\overline{EF}$ flag is deasserted by the rising edge of W.
3. First Write rising edge after $\overline{EF}$ is set.
4. SOCP should not be clocked until $\overline{EF}$ goes HIGH.

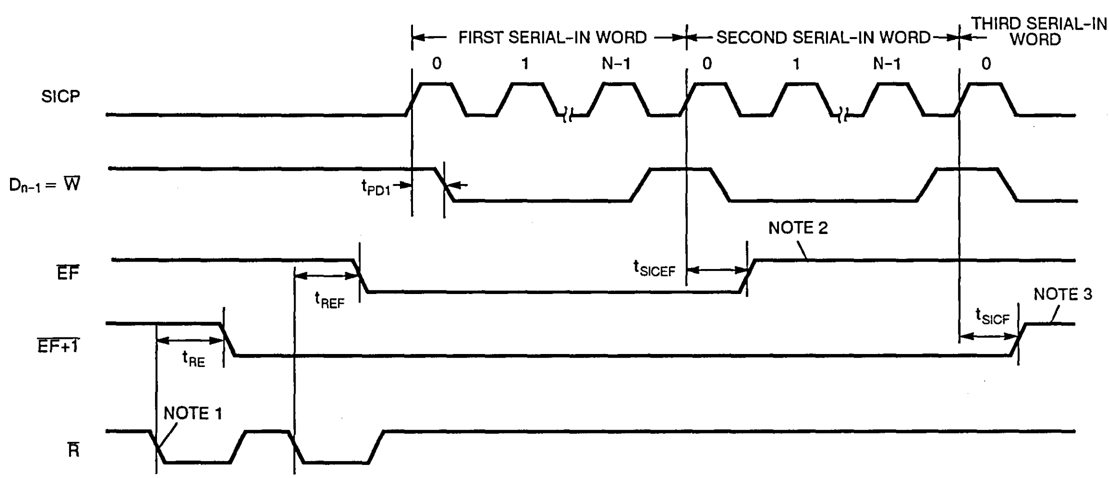
Figure 32. Empty Flag and Empty+1 Flag Assertion in the Serial-Out Mode, FIFO Being Emptied

SERIAL TIMINGS – FLAGS



NOTES:
1. The Full Flag is asserted in the Serial-In mode by using the t_{SICFF} parameter. This parameter is measured in the worst case from the rising edge of SICP followed by a (t_{PD1} + t_{WFF}) delay from the first rising edge of SICP of the last word.
2. First Read rising edge after $\overline{FF}$ is set.
3. SICP should not be clocked until $\overline{FF}$ goes HIGH.

Figure 33. Full Flag and Full–1 Flag Assertion in the Serial-In Mode, FIFO Being Filled



NOTES:
1. Parallel Read shown for reference only. Can also use serial output mode.
2. The Empty Flag is deasserted when an entire word has been loaded into the internal RAM. It can occur after the first rising edge of SICP of the second Serial-In word. In the Serial-Out mode, a new read operation can begin t_{REFSO} after $\overline{EF}$ goes HIGH. In the Parallel-Out mode, a new read operation can occur immediately after $\overline{FF}$ goes HIGH.
3. The Empty+1 Flag is deasserted after the first rising edge of SICP of the third Serial-In word.

Figure 34. Empty Flag and Empty+1 Flag Deassertion in Serial-In Mode

6

ORDERING INFORMATION

IDT XXXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B,
Package	P	Plastic DIP
	D	CERDIP
	J	Plastic Leaded Chip Carrier
	L	Leadless Chip Carrier
Speed (Parallel Access Time (t_A))	50	(40MHz serial shift rate)
	65	(33MHz serial shift rate)
	80	(28MHz serial shift rate)
	120	(25MHz serial shift rate)
Power	S	Standard Power
	L	Low Power
Device Type	72103	2048 x 9-Bit Parallel-Serial FIFO
	72104	4096 x 9-Bit Parallel-Serial FIFO

Integrated Device Technology, Inc.

CMOS PARALLEL FIFO 64 x 4-BIT AND 64 x 5-BIT

IDT72401
IDT72402
IDT72403
IDT72404

FEATURES:

- First-In/First-Out dual-port memory
- 64 x 4 organization (IDT72401/03)
- 64 x 5 organization (IDT72402/04)
- IDT72401/02 pin and functionally compatible with MMI67401/02
- RAM-based FIFO with low fall-through time
- Low power consumption
  - Active: 175mW (typ.)
- Maximum shift-rate—45MHz
- High data output drive capability
- Asynchronous and simultaneous read and write
- Fully expandable by bit width
- Fully expandable by word depth at 35MHz
- IDT72403/04 have Output Enable pin to enable output data
- High-speed data communications applications
- High-performance CEMOS™ technology
- Available in CERDIP, plastic DIP, LCC and SOIC
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86846 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT72401 and IDT72403 are asynchronous, high-performance First-In/First-Out memories organized 64 words by 4 bits. The IDT72402 and IDT72404 are asynchronous, high-performance First-In/First-Out memories organized as 64 words by 5 bits. The IDT72403 and IDT72404 also have an Output Enable ($\overline{OE}$) pin. The FIFOs accept 4-bit or 5-bit data at the data input (D_0-$D_{3,4}$). The stored data stack up on a first-in/first-out basis.

A Shift Out (SO) signal causes the data at the next to last word to be shifted to the output while all other data shifts down one location in the stack. The Input Ready (IR) signal acts like a flag to indicate when the input is ready for new data (IR = HIGH) or to signal when the FIFO is full (IR = LOW). The Input Ready signal can also be used to cascade multiple devices together. The Output Ready (OR) signal is a flag to indicate that the output contains valid data (OR = HIGH) or to indicate that the FIFO is empty (OR = LOW). The Output Ready signal can also be used to cascade multiple devices together.

Width expansion is accomplished by logically ANDing the Input Ready (IR) and Output Ready (OR) signals to form composite signals.

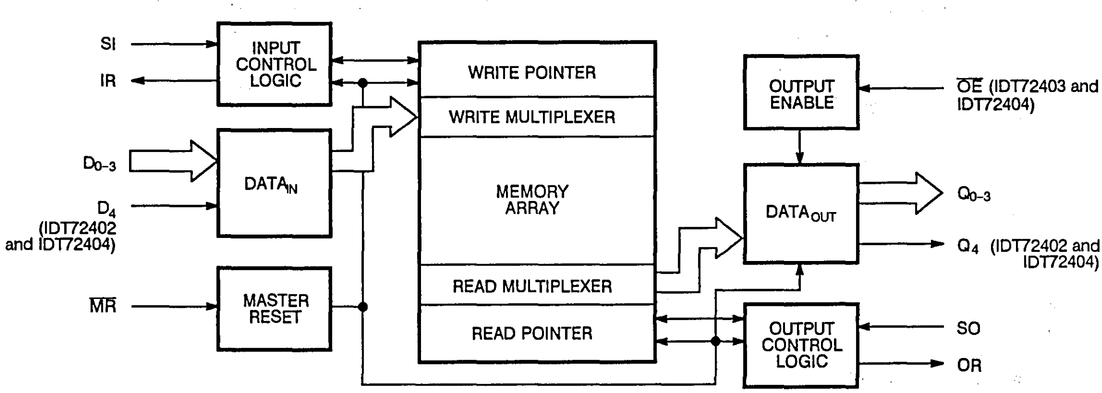
Depth expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The Input Ready pin of the receiving device is connected to the Shift Out pin of the sending device and the Output Ready pin of the sending device is connected to the Shift In pin of the receiving device.

Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely varying operating frequencies. The 45MHz speed makes these FIFOs ideal for high-speed communication and controller applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

6

FUNCTIONAL BLOCK DIAGRAM

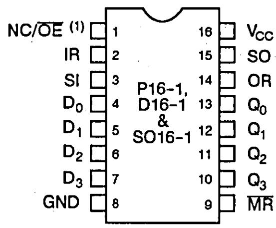


CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

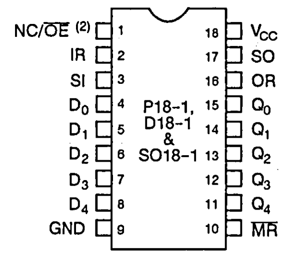
PIN CONFIGURATIONS

IDT72401
IDT72403

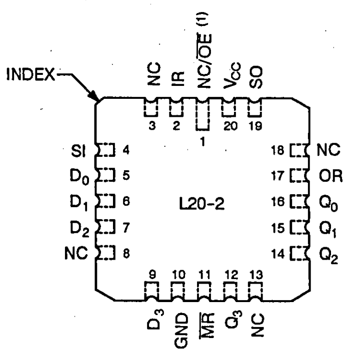


DIP/SOIC
TOP VIEW

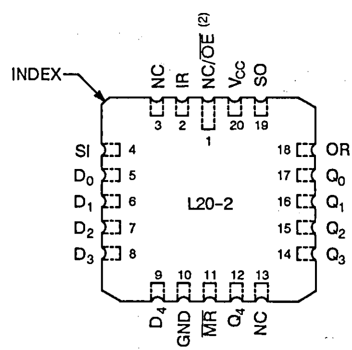
IDT72402
IDT72404



DIP/SOIC
TOP VIEW



LCC
TOP VIEW



LCC
TOP VIEW

NOTES:
1. Pin 1: NC – No Connection IDT72401
   $\overline{OE}$ – IDT72403
2. Pin 1: NC – No Connection IDT72402
   $\overline{OE}$ – IDT72404

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL} (1)	Input High Voltage	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

6

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
V_{IC} (1)	Input Clamp Voltage		–	–	–
I_{IL}	Low-Level Input Current	V_{CC} = Max., GND $\leq V_I \leq V_{CC}$	-10	–	µA
I_{IH}	High-Level Input Current	V_{CC} = Max., GND $\leq V_I \leq V_{CC}$	–	+10	µA
V_{OL}	Low-Level Output Current	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	–	V
I_{OS} (2)	Output Short-Circuit Current	V_{CC} = Max., V_O = GND	-20	-90	mA
I_{HZ}	Off-State Output Current (IDT72403 and IDT72404)	V_{CC} = Max., V_O = 2.4V	–	+20	µA
I_{LZ}		V_{CC} = Max., V_O = 0.4V	-20	–	µA
I_{CC} (3, 4)	Supply Current	V_{CC} = Max.: f = 10MHz Commercial Military	 – –	 35 45	mA

NOTES:
1. FIFO is able to withstand a -1.5V undershoot for less than 10ns.
2. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
3. I_{CC} measurements are made with outputs open.
4. For frequencies greater than 10MHz, I_{CC} = 35mA + (1.5mA x [f - 10MHz]) commercial, and I_{CC} = 40mA + (1.5mA x [f - 10MHz]) military.

OPERATING CONDITIONS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	FIGURE	COMMERCIAL		MILITARY AND COMMERCIAL								UNIT
			IDT72401L45 IDT72402L45 IDT72403L45 IDT72404L45		IDT72401L35 IDT72402L35 IDT72403L35 IDT72404L35		IDT72401L25 IDT72402L25 IDT72403L25 IDT72404L25		IDT72401L15 IDT72402L15 IDT72403L15 IDT72404L15		IDT72401L10 IDT72402L10 IDT72403L10 IDT72404L10		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{SIH} (1)	Shift In HIGH Time	2	9	–	9	–	11	–	11	–	11	–	ns
t_{SIL}	Shift In LOW Time	2	11	–	17	–	24	–	25	–	30	–	ns
t_{IDS}	Input Data Set-up	2	0	–	0	–	0	–	0	–	0	–	ns
t_{IDH}	Input Data Hold Time	2	13	–	15	–	20	–	30	–	40	–	ns
t_{SOH} (1)	Shift Out HIGH Time	5	9	–	9	–	11	–	11	–	11	–	ns
t_{SOL}	Shift Out LOW Time	5	11	–	17	–	24	–	25	–	25	–	ns
t_{MRW}	Master Reset Pulse	8	20	–	25	–	25	–	25	–	30	–	ns
t_{MRS}	Master Reset Pulse to SI	8	10	–	10	–	10	–	25	–	35	–	ns
t_{SIR}	Data Set-up to IR	4	3	–	3	–	5	–	5	–	5	–	ns
t_{HIR}	Data Hold from IR	4	13	–	15	–	20	–	30	–	30	–	ns
t_{SOR}	Data Set-up to OR HIGH	7	0	–	0	–	0	–	0	–	0	–	ns

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	FIGURE	COMMERCIAL		MILITARY AND COMMERCIAL								UNIT
			IDT72401L45 IDT72402L45 IDT72403L45 IDT72404L45		IDT72401L35 IDT72402L35 IDT72403L35 IDT72404L35		IDT72401L25 IDT72402L25 IDT72403L25 IDT72404L25		IDT72401L15 IDT72402L15 IDT72403L15 IDT72404L15		IDT72401L10 IDT72402L10 IDT72403L10 IDT72404L10		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{IN}	Shift In Rate	2	–	45	–	35	–	25	–	15	–	10	MHz
t_{IRL} (1)	Shift In to Input Ready LOW	2	–	18	–	18	–	21	–	35	–	40	ns
t_{IRH} (1)	Shift In to Input Ready HIGH	2	–	18	–	20	–	28	–	40	–	45	ns
f_{OUT}	Shift Out Rate	5	–	45	–	35	–	25	–	15	–	10	MHz
t_{ORL} (1)	Shift Out to Output Ready LOW	5	–	18	–	18	–	19	–	35	–	40	ns
t_{ORH} (1)	Shift Out to Output Ready HIGH	5	–	18	–	20	–	34	–	40	–	55	ns
t_{ODH}	Output Data Hold (Previous Word)	5	5	–	5	–	5	–	5	–	5	–	ns
t_{ODS}	Output Data Shift (Next Word)	5	–	20	–	25	–	35	–	55	–	55	ns
t_{PT}	Data Throughput or "Fall-Through"	4, 7	–	25	–	28	–	40	–	65	–	65	ns
t_{MRORL}	Master Reset to OR LOW	8	–	25	–	28	–	35	–	35	–	40	ns
t_{MRIRH}	Master Reset to IR HIGH	8	–	25	–	28	–	35	–	35	–	40	ns
t_{MRQ}	Master Reset to Data Output LOW	8	–	20	–	20	–	25	–	35	–	40	ns
t_{OOE} (3)	Output Valid from $\overline{OE}$ LOW	9	–	12	–	15	–	20	–	30	–	35	ns
t_{HZOE} (3)	Output HIGH-Z from $\overline{OE}$ HIGH	9	–	12	–	12	–	15	–	25	–	30	ns
t_{IPH} (2)	Input Ready Pulse HIGH	4	9	–	9	–	11	–	11	–	11	–	ns
t_{OPH} (2)	Output Ready Pulse HIGH	7	9	–	9	–	11	–	11	–	11	–	ns

NOTES:

1. Since the FIFO is a very high-speed device, care must be exercised in the design of the hardware and timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between V_{CC} and GND with very short lead length is recommended.
2. This parameter applies to FIFOs communicating with each other in a cascaded mode. IDT FIFOs are guaranteed to cascade with other IDT FIFOs of like speed grades.
3. IDT72403 and IDT72404 only.

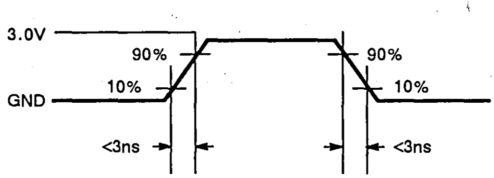
AC TEST CONDITIONS

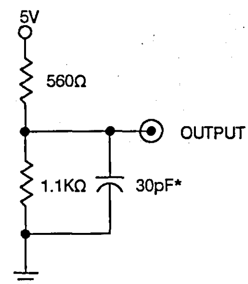
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.





*Includes jig and scope capacitances.

Figure 1. AC Test Load

6

SIGNAL DESCRIPTIONS

INPUTS:

DATA INPUT ($D_{0-3,4}$)

Data input lines. The IDT72401 and IDT72403 have a 4-bit data input. The IDT72402 and IDT72404 have a 5-bit data input.

CONTROLS

SHIFT IN (SI)

Shift In controls the input of the data into the FIFO. When SI is HIGH, data can be written to the FIFO via the $D_{0-3,4}$ lines.

SHIFT OUT (SO)

Shift Out controls the output of data out of the FIFO. When SO is HIGH, data can be read from the FIFO via the Data Output ($Q_{0-3,4}$) lines.

MASTER RESET ($\overline{MR}$)

Master Reset clears the FIFO of any data stored within. Upon power up, the FIFO should be cleared with a Master Reset. Master Reset is active LOW.

INPUT READY (IR)

When Input Ready is HIGH, the FIFO is ready for new input data to be written to it. When IR is LOW the FIFO is unavailable for new input data. Input Ready is also used to cascade many FIFOs together, as shown in Figures 10 and 11 in the Applications section.

OUTPUT READY (OR)

When Output Ready is HIGH, the output ($Q_{0-3,4}$) contains valid data. When OR is LOW, the FIFO is unavailable for new output data. Output Ready is also used to cascade many FIFOs together, as shown in Figures 10 and 11.

OUTPUT ENABLE ($\overline{OE}$) (IDT72403 AND IDT72404 ONLY)

Output Enable is used to read FIFO data onto a bus. Output Enable is active LOW.

OUTPUTS

DATA OUTPUT ($Q_{0-3,4}$)

Data Output lines. The IDT72401 and IDT72403 have a 4-bit data output. The IDT72402 and IDT72404 have a 5-bit data output.

FUNCTIONAL DESCRIPTION

These 64 x 4 and 64 x 5 FIFOs are designed using a dual-port RAM architecture as opposed to the traditional shift register approach. This FIFO architecture has a write pointer, a read pointer and control logic, which allow simultaneous read and write operations. The write pointer is incremented by the falling edge of the Shift In (SI) control; the read pointer is incremented by the falling edge of the Shift Out (SO). The Input Ready (IR) signals when the FIFO has an available memory location; Output Ready (OR) signals when there is valid data on the output. Output Enable ($\overline{OE}$) provides the capability of three-stating the FIFO outputs.

FIFO Reset

The FIFO must be reset upon power up using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state, signified by Output Ready (OR) being LOW and Input Ready (IR) being HIGH. In this state, the data outputs ($Q_{0-3,4}$) will be LOW.

Data Input

Data is shifted in on the LOW-to-HIGH transition of Shift In (SI). This loads input data into the first word location of the FIFO and causes Input Ready to go LOW. On the HIGH-to-LOW transition of Shift In, the write pointer is moved to the next word position and Input Ready (IR) goes HIGH, indicating the readiness to accept new data. If the FIFO is full, Input Ready will remain LOW until a word of data is shifted out.

Data Output

Data is shifted out on the HIGH-to-LOW transition of Shift Out (SO). This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and Output Ready (OR) will go HIGH. If data is not present, Output Ready will stay LOW indicating the FIFO is empty. The last valid word read from the FIFO will remain at the FIFO's output when it is empty. When the FIFO is not empty, Output Ready (OR) goes LOW on the LOW-to-HIGH transition of Shift Out. Previous data remains on the output until the HIGH-to-LOW transition of Shift Out (SO).

Fall-Through Mode

The FIFO operates in a fall-through mode when data gets shifted into an empty FIFO. After a fall-through delay the data propagates to the output. When the data reaches the output, the Output Ready (OR) goes HIGH. Fall-through mode also occurs when the FIFO is completely full. When data is shifted out of the full FIFO, a location is available for new data. After a fall-through delay, the Input Ready goes HIGH. If Shift In is HIGH, the new data can be written to the FIFO.

Since these FIFOs are based on an internal dual-port RAM architecture with separate read and write pointers, the fall-through time (t_{PT}) is one cycle long. A word may be written into the FIFO on a clock cycle and can be accessed on the next clock cycle.

TIMING DIAGRAMS

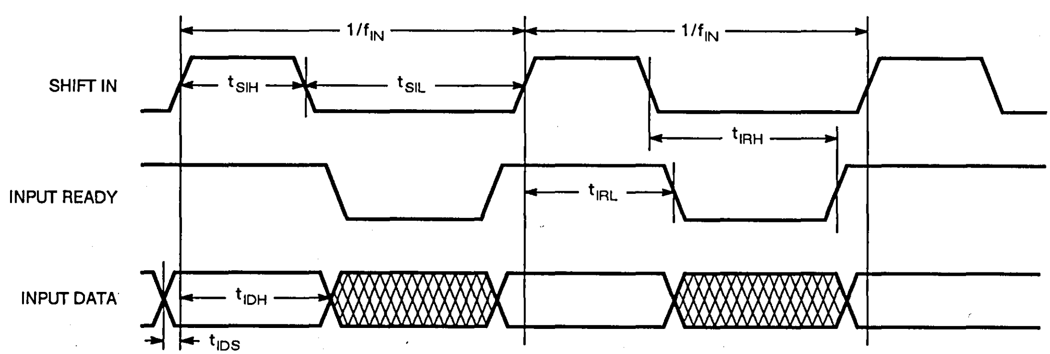
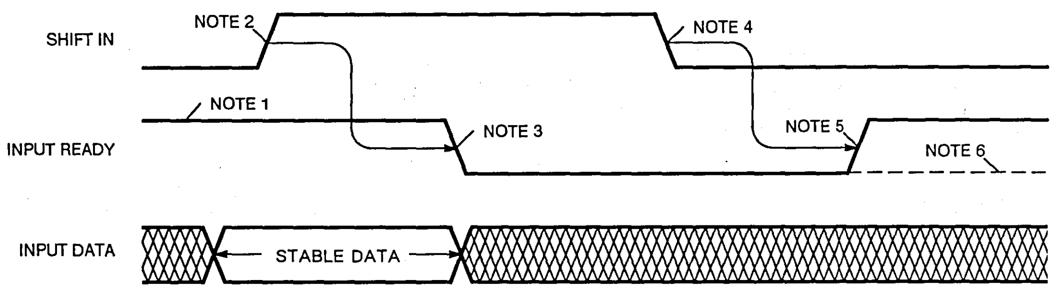


Figure 2. Input Timing

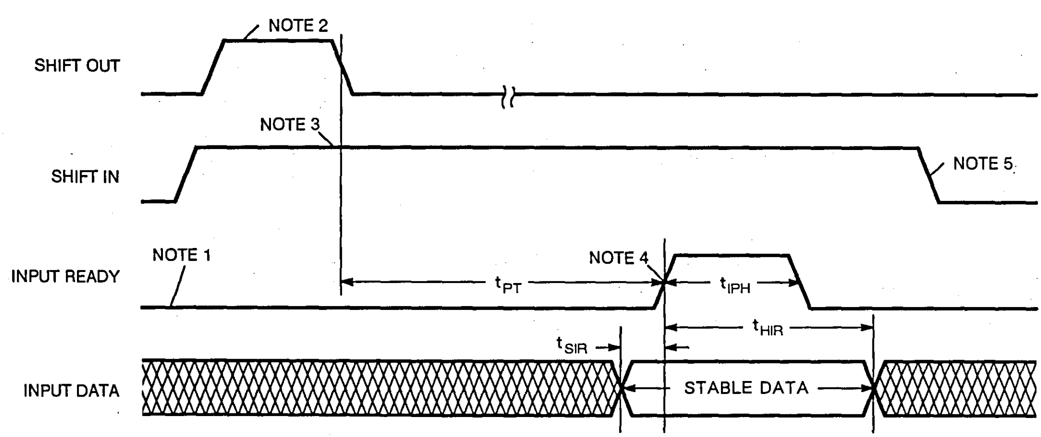
TIMING DIAGRAMS (Continued)



NOTES:
1. Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
2. Input Data is loaded into the first word.
3. Input Ready goes LOW indicating the first word is full.
4. The write pointer is incremented.
5. The FIFO is ready for the next word.
6. If the FIFO is full then the Input Ready remains LOW.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (see Figure 4).

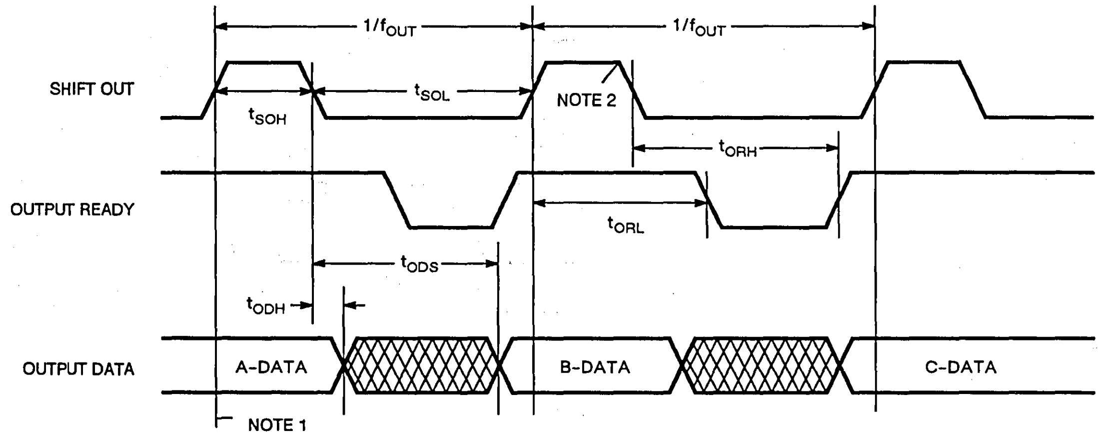
Figure 3. The Mechanism of Shifting Data Into the FIFO



NOTES:
1. FIFO is initially full.
2. Shift Out pulse is applied.
3. Shift In is held HIGH.
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the FIFO.
5. The write pointer is incremented.

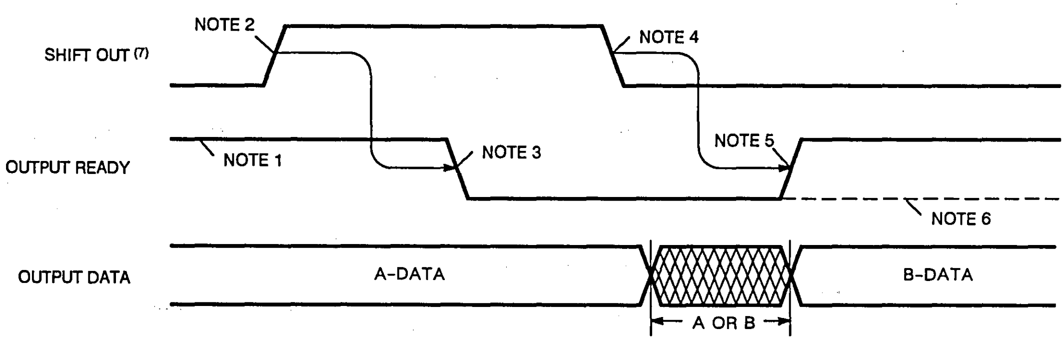
Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH

TIMING DIAGRAMS (Continued)



NOTES:
1. This data is loaded consecutively A, B, C.
2. Data is shifted out when Shift Out makes a HIGH to LOW transition.

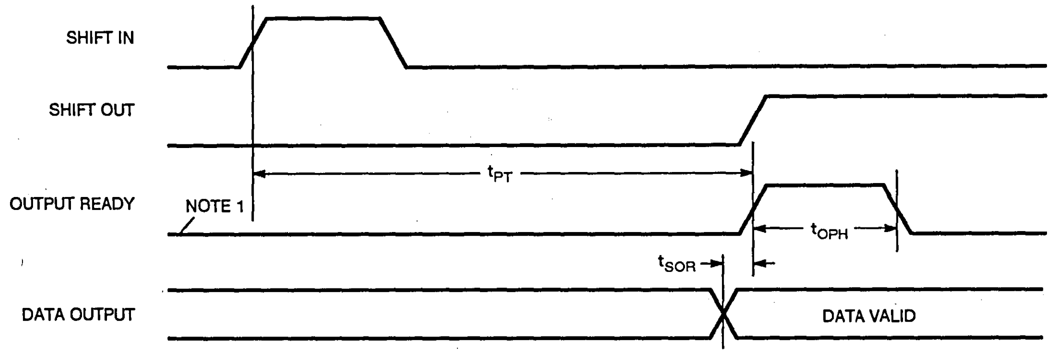
Figure 5. Output Timing



NOTES:
1. Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
2. Shift Out goes HIGH causing the next step.
3. Output Ready goes LOW.
4. Read pointer is incremented.
5. Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
6. If the FIFO has only one word loaded (A DATA) then Output Ready stays LOW and the A DATA remains unchanged at the outputs.
7. Shift Out pulses applied when Output Ready is LOW will be ignored.

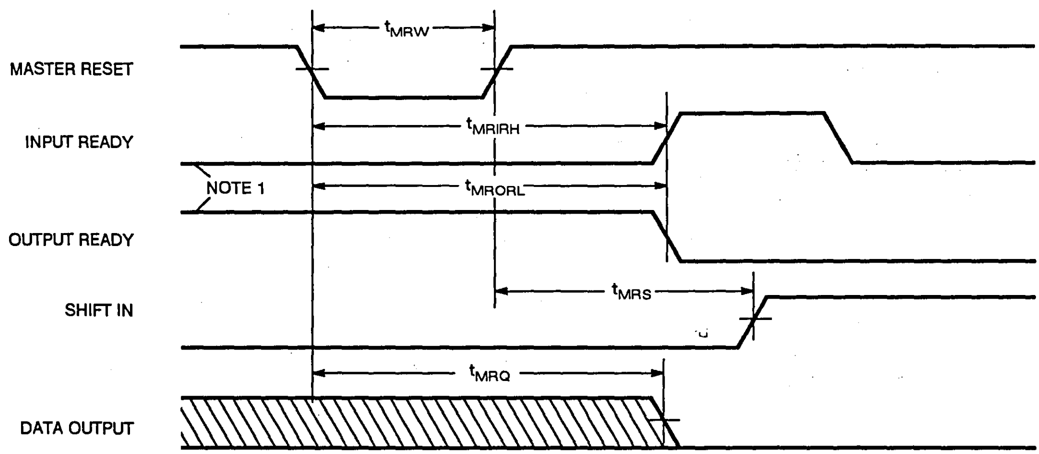
Figure 6. The Mechanism of Shifting Data Out of the FIFO

TIMING DIAGRAMS (Continued)



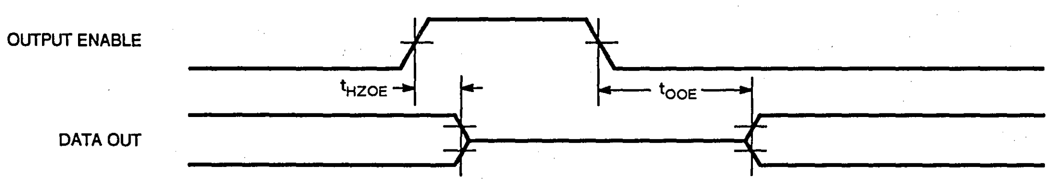
NOTE:
1. FIFO initially empty.

Figure 7. t_{PT} and t_{OPH} Specification



NOTE:
1. Worst case, FIFO initially full.

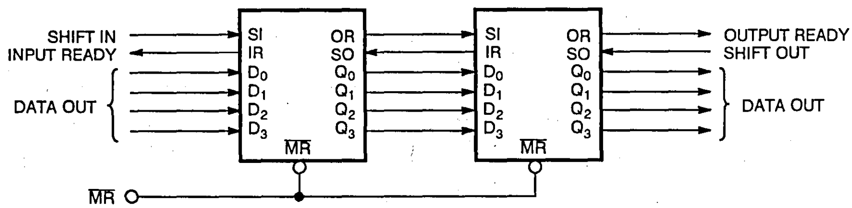
Figure 8. Master Reset Timing



NOTE:
1. High-Z transitions are referenced to the steady-state V_{OH} - 500mV and V_{OL} + 500mV levels on the output. t_{HZOE} is tested with 5pF load capacitance instead of 30pF as shown in Figure 1.

Figure 9. Output Enable Timing, IDT72403 and IDT72404 Only

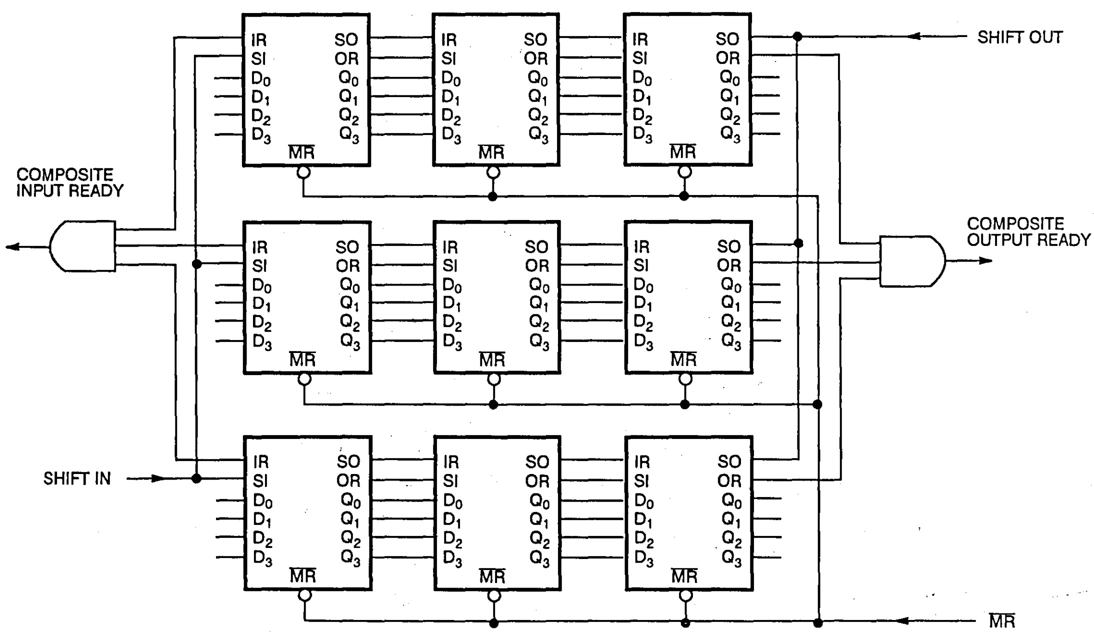
APPLICATIONS



NOTE:

1. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

Figure 10. 128 x 4 Depth Expansion



NOTES:

1. When the memory is empty, the last word read will remain on the outputs until the Master Reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will appear at the output after a fall-through time. OR will go HIGH for one internal cycle (at least t_{ORL}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the Master Reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the Master Reset goes HIGH, the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the Master Reset is ended, IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
5. FIFOs are expandable in depth and width. However, in forming wider words, two external gates are required to generate composite Input and Output Ready flags. This is due to the variation of delays of the FIFOs.

Figure 11. 192 x 12 Depth and Width Expansion

ORDERING INFORMATION

IDT XXXX XX XXX XX X

IDT	XXXX	XX	XXX	XX	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range

Code	Description
Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

Code	Description
D	CERDIP
L	Leadless Chip Carrier
P	Plastic Dip
SO	Small Outline IC

Speed — Shift Frequency (MHz)

Code	Description
45	Commercial Only
35	
25	
15	
10	

Power

Code	Description
L	Low Power

Device Type

Code	Description
72401	64 x 4 FIFO
72402	64 x 5 FIFO
72403	64 x 4 FIFO with Output Enable
72404	64 x 5 FIFO with Output Enable

6

Integrated Device Technology, Inc.

CMOS PARALLEL 64 x 5-BIT FIFO WITH FLAGS

IDT72413

FEATURES:

- First-In/First-Out dual-port memory—45MHz
- 64 x 5 organization
- Low power consumption
  - Active: 200mW (typical)
- RAM-based internal structure allows for fast fall-through time
- Asynchronous and simultaneous read and write
- Expandable by bit width
- Cascadable by word depth at 25MHz and 35MHz
- Half-Full and Almost-Full/Empty status flags
- IDT72413 is pin and functionally compatible with the MMI67413
- High-speed data communications applications
- Bidirectional and rate buffer applications
- High-performance CEMOS ™ technology
- Available in plastic DIP, CERDIP, LCC and SOIC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72413 is a 64 x 5, high-speed First-In/First-Out (FIFO) that loads and empties data on a first-in/first-out basis. It is expandable in bit width. The IDT72413 25MHz and 35MHz versions are cascadable in depth.

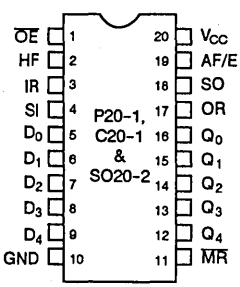
The FIFO has a Half-Full Flag, which signals when it has 32 or more words in memory. The Almost-Full/Empty Flag is active when there are 56 or more words in memory or when there are 8 or less words in memory.

The IDT72413 is pin and functionally compatible to the MMI 67413. It operates at a shift rate of 45MHz. This makes it ideal for use in high-speed data buffering applications. The IDT72413 can be used as a rate buffer, between two digital systems of varying data rates, in high-speed tape drivers, hard disk controllers, data communications controllers and graphics controllers

The IDT72413 is fabricated using IDT's high-performance CEMOS process. This process maintains the speed and high output drive capability of TTL circuits in low-power CMOS.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

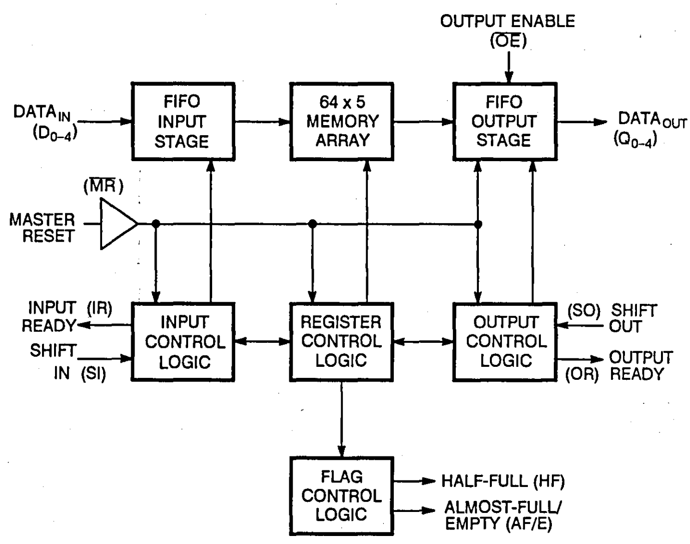
PIN CONFIGURATION



DIP/SOIC TOP VIEW

LCC (CONSULT FACTORY) L20-2

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-2015/-

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL}[1]	Input Low Voltage	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C, Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS				MIN.	MAX.	UNIT
V_{IC}[1]	Input Clamp Voltage					–	–	
I_{IL}	Low-Level Input Current	V_{CC} = Max.; GND ≤ V_I ≤ V_{CC}				-10	–	µA
I_{IH}	High-Level Input Current	V_{CC} = Max.; GND ≤ V_I ≤ V_{CC}				–	10	µA
V_{OL}	Low-Level Output Voltage	V_{CC} = Min.	I_{OL} (Q_{0-4})	MIL.	12mA	–	0.4	V
				COM'L.	24mA			
			I_{OL} (IR, OR)[2]		8mA			
			I_{OL} (HF, AF/E)		8mA			
V_{OH}	High-Level Output Voltage	V_{CC} = Min.	I_{OH} (Q_{0-4})		-4mA	2.4	–	V
			I_{OH} (IR, OR)		-4mA			
			I_{OH} (HF, AF/E)		-4mA			
I_{OS}[3]	Output Short-Circuit Current	V_{CC} = Max.	V_O = 0V			-20	-90	mA
I_{HZ}	Off-State Output Current	V_{CC} = Max.	V_O = 2.4V			–	+20	µA
I_{LZ}	Off-State Output Current	V_{CC} = Max.	V_O = 0.4V			-20	–	µA
I_{CC}[4]	Supply Current	V_{CC} = Max. Inputs LOW, Outputs Open, f = 25MHz			MIL.	–	70	mA
					COM'L.	–	60	mA

NOTES:
1. FIFO is able to withstand a -1.5V undershoot for less than 10ns.
2. Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25MHz.
3. Not more than one output should be shorted at a time and duration of the short circuit test should not exceed one second.
4. Frequencies greater than 25MHz, I_{CC} = 60mA + (1.5mA x [f - 25MHz]) commercial and I_{CC} = 70mA + (1.5mA x [f - 25MHz]) military.

OPERATING CONDITIONS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C, Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	FIGURE	MILITARY AND COMMERCIAL				COMMERCIAL		UNIT
			IDT72413L45		IDT72413L35		IDT72413L25		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{SIH}[1]	Shift In HIGH Time	2	9	–	9	–	16	–	ns
t_{SIL}[1]	Shift In LOW Time	2	11	–	17	–	20	–	ns
t_{IDS}	Input Data Set-Up	2	0	–	0	–	0	–	ns
t_{IDH}	Input Data Hold Time	2	13	–	15	–	25	–	ns
t_{SOH}[1]	Shift Out HIGH Time	5	9	–	9	–	16	–	ns
t_{SOL}	Shift Out LOW Time	5	11	–	17	–	20	–	ns
t_{MRW}	Master Reset Pulse	8	20	–	30	–	35	–	ns
t_{MRS}	Master Reset to SI	8	20	–	35	–	35	–	ns

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C, Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	FIGURE	MILITARY AND COMMERCIAL				COMMERCIAL		UNIT
			IDT72413L45		IDT72413L35		IDT72413L25		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{IN}	Shift In Rate	2	–	45	–	35	–	25	MHz
t_{IRL}[1]	Shift In ↑ to Input Ready LOW	2	–	18	–	18	–	28	ns
t_{IRH}[1]	Shift In ↓ to Input Ready HIGH	2	–	18	–	20	–	25	ns
f_{OUT}	Shift Out Rate	5	–	45	–	35	–	25	MHz
t_{ORL}[1]	Shift Out ↓ to Output Ready LOW	5	–	18	–	18	–	28	ns
t_{ORH}[1]	Shift Out ↓ to Output Ready HIGH	5	–	18	–	20	–	25	ns
t_{ODH}[1]	Output Data Hold Previous Word	5	5	–	5	–	5	–	ns
t_{ODS}	Output Data Shift Next Word	5	–	20	–	20	–	20	ns
t_{PT}	Data Throughput or "Fall-Through"	4, 7	–	25	–	28	–	40	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8	–	25	–	28	–	30	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH	8	–	25	–	28	–	30	ns
t_{MRIRL}[2]	Master Reset ↓ Input Ready LOW	8	–	25	–	28	–	30	ns
t_{MRQ}	Master Reset ↓ to Outputs LOW	8	–	20	–	25	–	35	ns
t_{MRHF}	Master Reset ↓ to Half-Full Flag	8	–	25	–	28	–	40	ns
t_{MRAFE}	Master Reset ↓ to AF/E Flag	8	–	25	–	28	–	40	ns
t_{IPH}	Input Ready Pulse HIGH	4	5	–	5	–	5	–	ns
t_{OPH}	Output Ready Pulse HIGH	7	5	–	5	–	5	–	ns
t_{ORD}	Output Ready ↑ HIGH to Valid Data	5	–	5	–	5	–	7	ns
t_{AEH}	Shift Out ↑ to AF/E HIGH	9	–	28	–	28	–	40	ns
t_{AEL}	Shift In ↑ to AF/E	9	–	28	–	28	–	40	ns
t_{AFL}	Shift Out ↑ to AF/E LOW	10	–	28	–	28	–	40	ns
t_{AFH}	Shift In ↑ to AF/E HIGH	10	–	28	–	28	–	40	ns
t_{HFH}	Shift In ↑ to HF HIGH	11	–	28	–	28	–	40	ns
t_{HFL}	Shift Out ↑ to HF LOW	11	–	28	–	28	–	40	ns
t_{PHZ}	Output Disable Delay	12	–	12	–	12	–	15	ns
t_{PLZ}		12	–	12	–	12	–	15	ns
t_{PZL}	Output Enable Delay	12	–	15	–	15	–	20	ns
t_{PZH}		12	–	15	–	15	–	20	ns

NOTES:

1. Since the FIFO is a very high-speed device, care must be taken in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between V_{CC} and GND with very short lead length is recommended.
2. If the FIFO is not full, (IR = HIGH), $\overline{MR}$↓ forces IR to go LOW, and $\overline{MR}$↑ causes IR to go HIGH.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

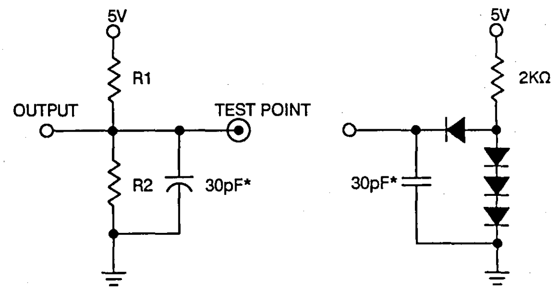
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.
2. Characterized values, not currently tested.

STANDARD TEST LOAD

DESIGN TEST LOAD



*Includes jig and scope capacitances.

RESISTOR VALUES FOR STANDARD TEST LOAD

I_{OL}	R1	R2
24mA	200Ω	300Ω
12mA	390Ω	760Ω
8mA	600Ω	1200Ω

Figure 1. Output Load

6

FUNCTIONAL DESCRIPTION:

The IDT72413, 65 x 5 FIFO is designed using a dual-port RAM architecture as opposed to the traditional shift register approach. This FIFO architecture has a write pointer, a read pointer and control logic, which allow simultaneous read and write operations. The write pointer is incremented by the falling edge of the Shift In (SI) control; the read pointer is incremented by the falling edge of the Shift Out (SO). The Input Ready (IR) signals when the FIFO has an available memory location; Output Ready (OR) signals when there is valid data on the output. Output Enable ($\overline{OE}$) provides the capability of three-stating the FIFO outputs.

FIFO RESET

The FIFO must be reset upon power up using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state signified by Output Ready (OR) being LOW and Input Ready (IR) being HIGH. In this state, the data outputs (Q_{0-4}) will be LOW.

DATA INPUT

Data is shifted in on the LOW-to-HIGH transition of Shift In (SI). This loads input data into the first word location of the FIFO and causes the Input Ready to go LOW. On the HIGH-to-LOW transition of Shift In, the write pointer is moved to the next word position and Input Ready (IR) goes HIGH indicating the readiness to accept new data. If the FIFO is full, Input Ready will remain LOW until a word of data is shifted out.

DATA OUTPUT

Data is shifted out on the HIGH-to-LOW transition of Shift Out (SO). This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and Output Ready (OR) will go HIGH. If data is not present, Output Ready will stay LOW indicating the FIFO is empty. The last valid word read from the FIFO will remain at the FIFO's output when it is empty. When the FIFO is not empty, Output Ready (OR) goes LOW on the LOW-to-HIGH transition of Shift Out.

FALL-THROUGH MODE

The FIFO operates in a Fall-Through Mode when data gets shifted into an empty FIFO. After the fall-through delay the data propagates to the output. When the data reaches the output, the Output Ready (OR) goes HIGH.

A Fall-Through Mode also occurs when the FIFO is completely full. When data is shifted out of the full FIFO, a location is available for new data. After a fall-through delay, the Input Ready goes HIGH. If Shift In is HIGH, the new data can be written to the FIFO. The fall-through delay of a RAM-based FIFO (one clock cycle) is far less than the delay of a shift register-based FIFO.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA INPUT (D_{0-4})

Data input lines. The IDT72413 has a 5-bit data input.

CONTROLS:

SHIFT IN (SI)

Shift In controls the input of the data into the FIFO. When SI is HIGH, data can be written to the FIFO via the D_{0-4} lines. The data has to meet set-up and hold time requirements with respect to the rising edge of SI.

SHIFT OUT (SO)

Shift Out controls the output data from the FIFO.

MASTER RESET ($\overline{MR}$)

Master Reset clears the FIFO of any data stored within. Upon power up, the FIFO should be cleared with a Master Reset. Master Reset is active LOW.

HALF-FULL FLAG (HF)

Half-Full Flag signals when the FIFO has 32 or more words in it.

INPUT READY (IR)

When Input Ready is HIGH, the FIFO is ready for new input data to be written to it. When IR is LOW, the FIFO is unavailable for new input data. Input Ready is also used to cascade many FIFOs together, as shown in Figure 13 in the Applications section.

OUTPUT READY (OR)

When Output Ready is HIGH, the output (Q_{0-4}) contains valid data. When OR is LOW, the FIFO is unavailable for new output data. Output Ready is also used to cascade many FIFOs together, as shown in Figure 13 in the Applications section.

OUTPUT ENABLE ($\overline{OE}$)

Output Enable is used to enable the FIFO outputs onto a bus. Output Enable is active LOW.

ALMOST-FULL/EMPTY FLAG (AFE)

Almost-Full/Empty Flag signals when the FIFO is 7/8 full (56 or more words) or 1/8 from empty (8 or less words).

OUTPUTS:

DATA OUTPUT (Q_{0-4})

Data output lines, three-state. The IDT72413 has a 5-bit output.

TIMING DIAGRAMS

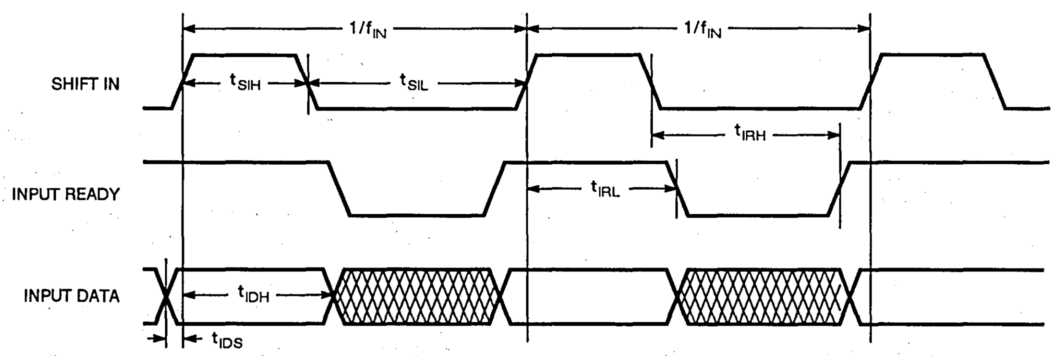
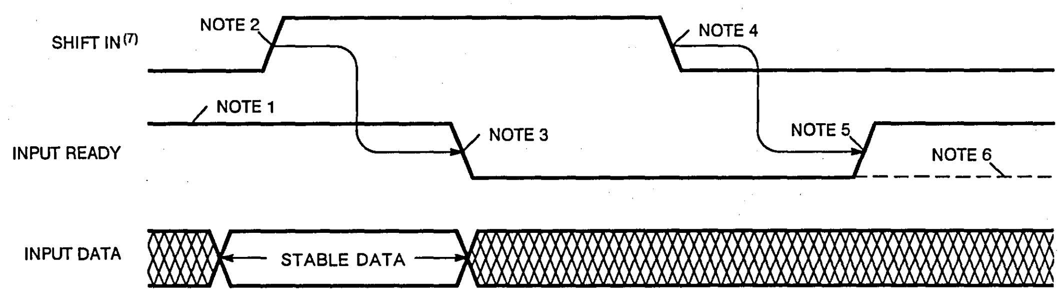


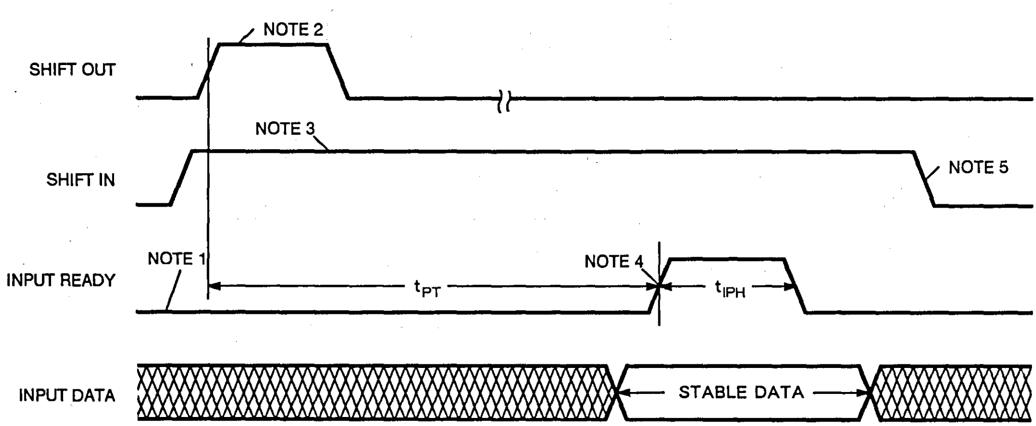
Figure 2. Input Timing

TIMING DIAGRAMS (Continued)



NOTES:
1. Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
2. Input Data is loaded into the FIFO.
3. Input Ready goes LOW indicating the FIFO is unavailable for new data.
4. The write pointer is incremented.
5. The FIFO is ready for the next word.
6. If the FIFO is full, then the Input Ready remains LOW.
7. Shift In pulses applied while Input Ready is LOW will be ignored (see Figure 4).

Figure 3. The Mechanism of Shifting Data Into the FIFO

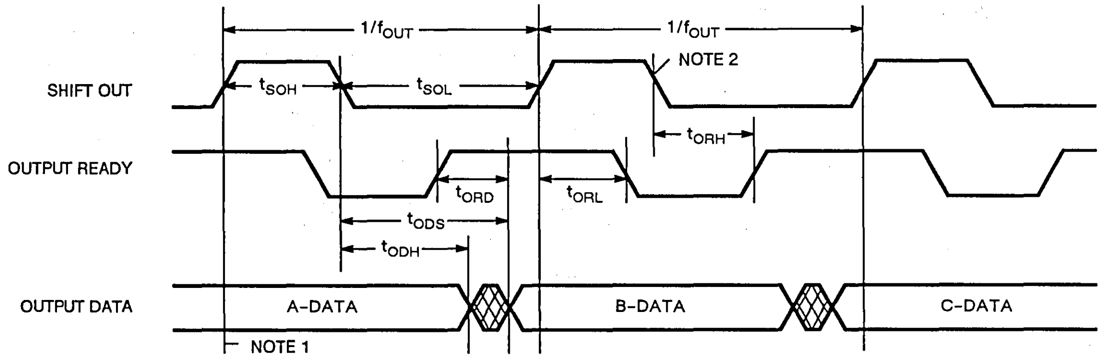


NOTES:
1. FIFO is initially full.
2. Shift Out pulse is applied.
3. Shift In is held HIGH.
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the FIFO.
5. The write pointer is incremented. Shift In should not go LOW until ($t_{PT} + t_{IPH}$).

Figure 4. Data Is Shifted In Whenever Shift In and Input Ready are Both HIGH

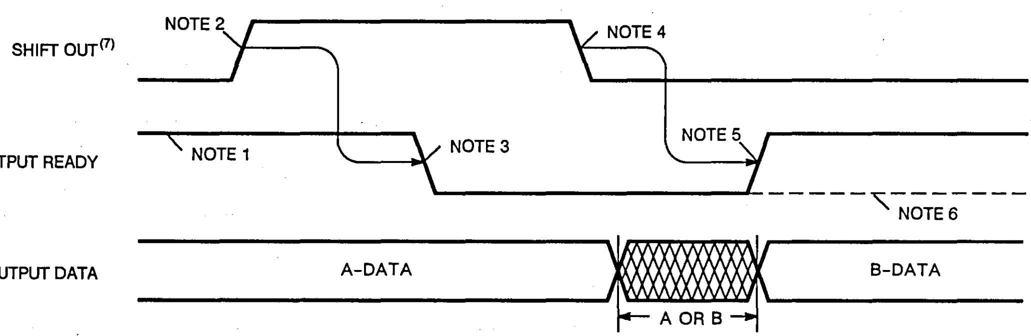
6

TIMING DIAGRAMS (Continued)



NOTES:
1. This diagram is loaded consecutively, A, B, C.
2. Output data changes on the falling edge of SO after a valid Shift Out sequence, i.e., OR and SO are both high together.

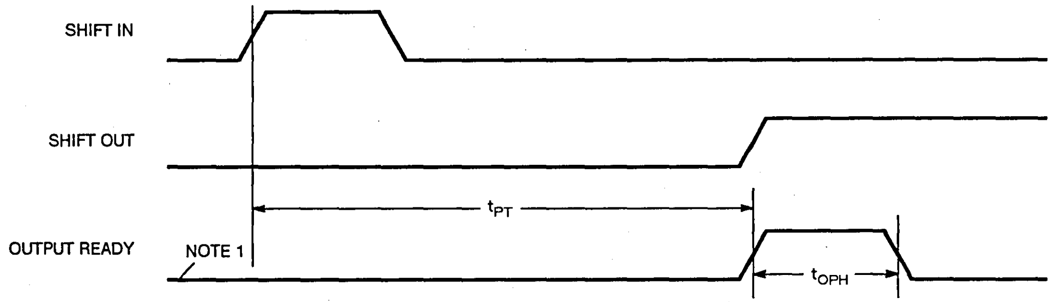
Figure 5. Output Timing



NOTES:
1. Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
2. Shift Out goes HIGH causing the next step.
3. Output Ready goes LOW.
4. Read pointer is incremented.
5. Output Ready goes HIGH indicating that new data (B) will be available at the FIFO outputs after t_{ORD} ns.
6. If the FIFO has only one word loaded (A-DATA), Output Ready stays LOW and the A-DATA remains unchanged at the outputs.
7. Shift Out pulses applied when Output Ready is LOW will be ignored.

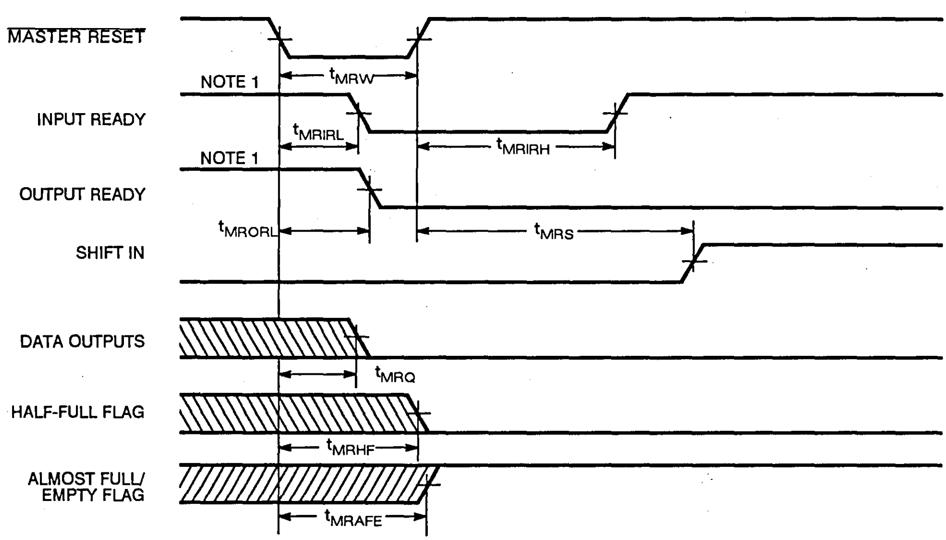
Figure 6. The Mechanism of Shifting Data Out of the FIFO

TIMING DIAGRAMS (Continued)



NOTE:
1. FIFO initially empty.

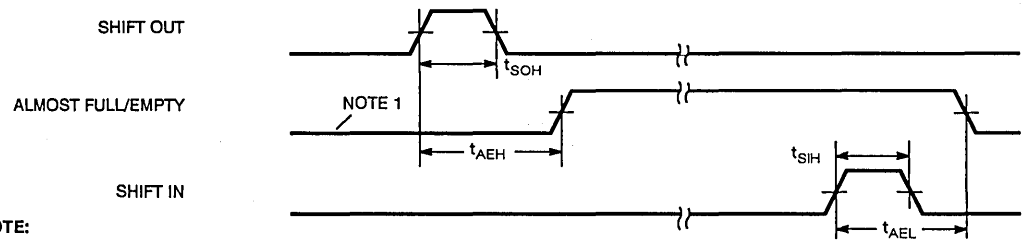
Figure 7. t_{PT} and t_{OPH} Specification



NOTE:
1. FIFO is partially full.

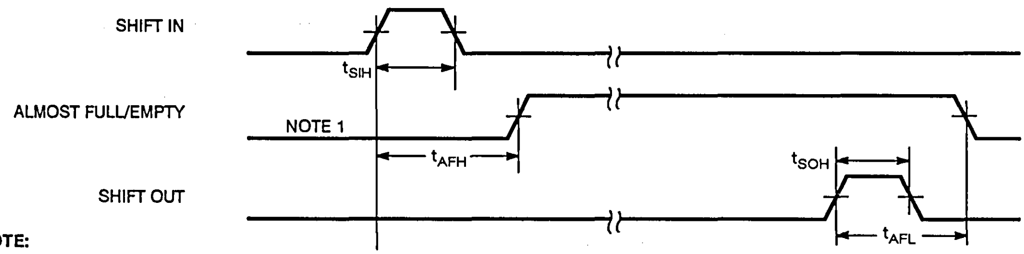
Figure 8. Master Reset Timing

TIMING DIAGRAMS (Continued)



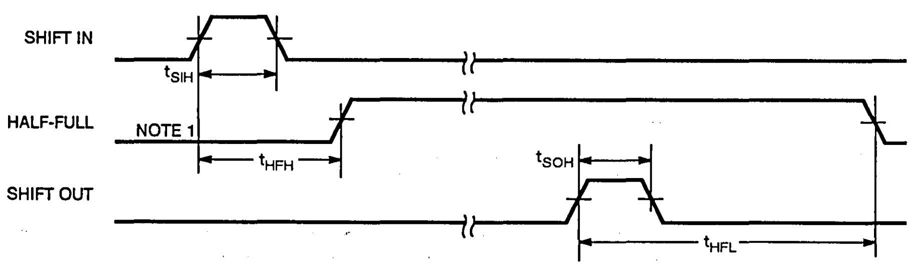
NOTE:
1. FIFO contains 9 words (one more than Almost-Empty).

Figure 9. t_{AEH} and t_{AEL} Specifications



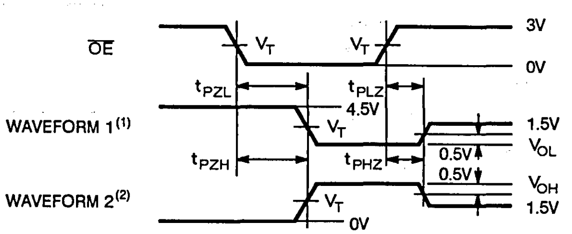
NOTE:
1. FIFO contains 55 words (one short of Almost-Full).

Figure 10. t_{AFH} and t_{AFL} Specifications



NOTE:
1. FIFO contains 31 words (one short of Half-Full).

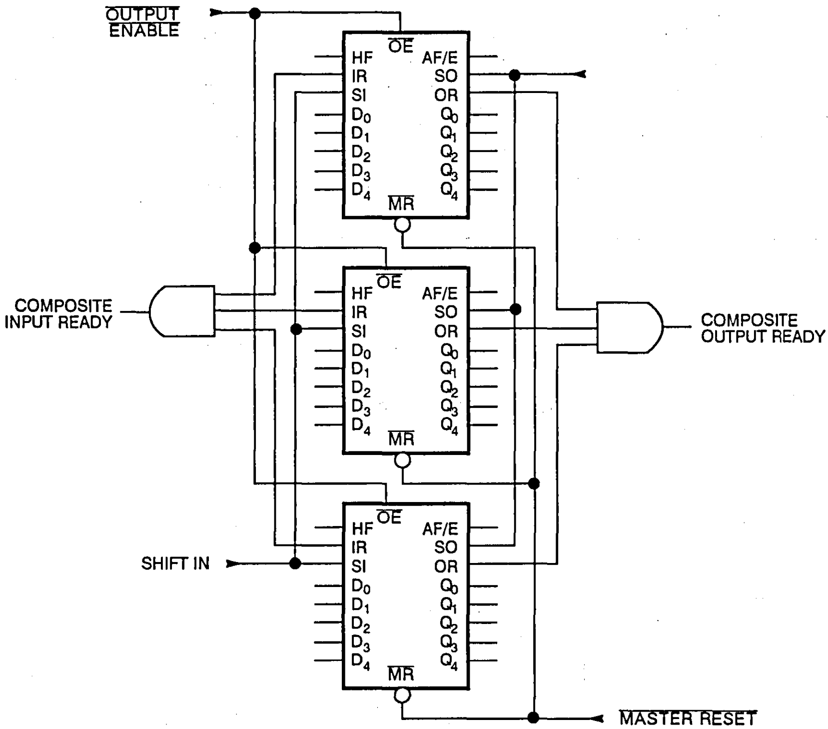
Figure 11. t_{HFL} and t_{HFH} Specifications



NOTES:
1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

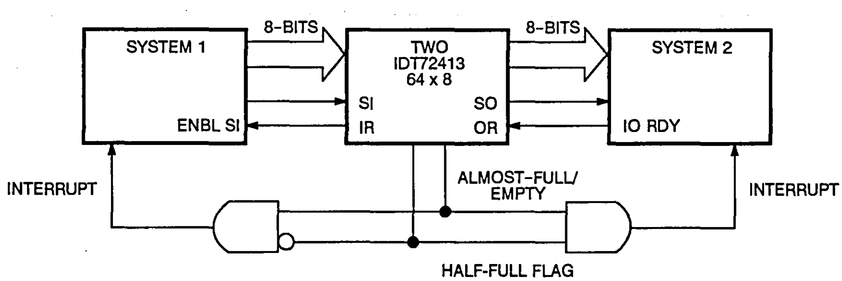
Figure 12. Enable and Disable

APPLICATIONS



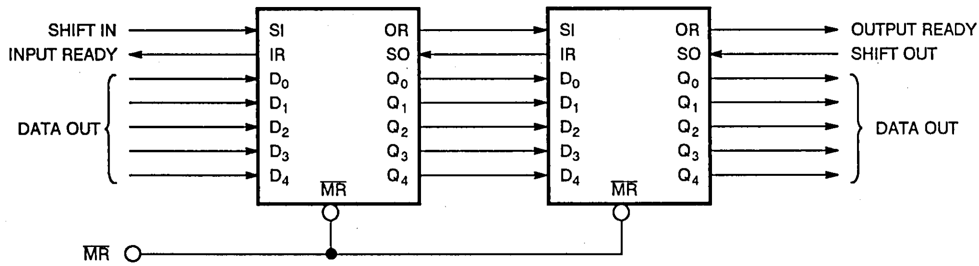
NOTE:
1. FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This requirement is due to the different fall-through times of the FIFOs.

Figure 13. 64x15 FIFO with IDT72413



NOTE:
1. Cascading the FIFOs in word width is done by ANDing the IR and OR as shown in Figure 13.

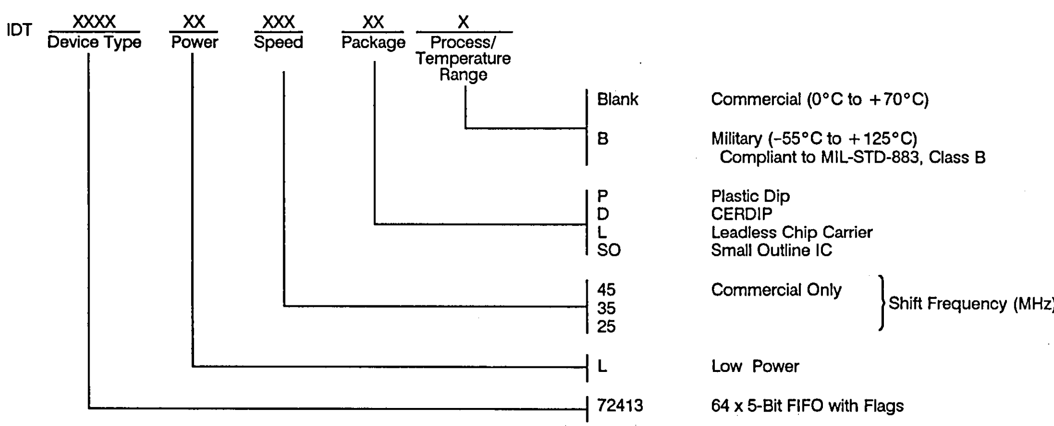
Figure 14. Application for IDT72413 for Two Asynchronous Systems



NOTE:
1. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

Figure 15. 128 x 5 Depth Expansion

ORDERING INFORMATION



Integrated Device Technology, Inc.

1K x 18-BIT – 2K x 9-BIT CMOS BiFIFO

ADVANCE INFORMATION
IDT7252

FEATURES:

- Bidirectional First-In/First-Out (FIFO) memory
- Back-to-back 1Kx18-bit and 2Kx9-bit FIFO organization
- Facilitates processor-to-peripheral and processor-to-processor communication
- Matches mixed bus widths: 16-bit to 8-bit buses and 32-bit to 8-bit buses
- Easy interface to microprocessor bus
- Asynchronous and simultaneous read and write operations
- Parity check and generate
- Convenient request/acknowledge interface program option for interface to peripherals
- Eight software programmable status Empty/Full Flags (offset and polarity) selectable onto four output pins
- Typical interface applications include microprocessor to floppy/hard disk controllers, microprocessor to SCSI bus, microprocessor to Local Area Network (LAN) controllers and microprocessor to 8-bit microcontroller
- Available in 48-pin DIP, and 70 mil center SHRINK-DIP and surface mount 52-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

FIFOs are used to link microprocessors and peripherals together asynchronously for sending and receiving data and commands. Often the data or commands must be sent in both directions. The IDT7252 BiFIFO is a compact, highly integrated solution to simplifying data transfer between two processors or a processor and peripheral of different bus bandwidths. Using the BiFIFO can quadruple system throughput performance of the peripheral interface by eliminating inefficiencies associated with widely varying, mismatched bus widths. The BiFIFO can handle data transfers between 16-bit to 8-bit buses and 32-bit to 8-bit buses.

The BiFIFO can be accessed on either side by a microprocessor or bit-slice machine. It contains a 1Kx18-bit FIFO in both directions. The 8-bit port views a 2Kx9-bit FIFO instead of a 1Kx18-bit FIFO. The ninth bit of this FIFO is available for control or parity and can be stored in the FIFO array or parity can be checked or generated. A unique data bypass mode allows for synchronous communication between two devices for initialization. Later asynchronous communications can occur via the FIFOs.

To ease connection to peripherals and reduce parts count, a request/acknowledge-type handshake is included that utilizes Request (REQ) and Acknowledge (ACK) signals. A microprocessor-type interface generates read and write strobes and accesses the internal read and write pointers.

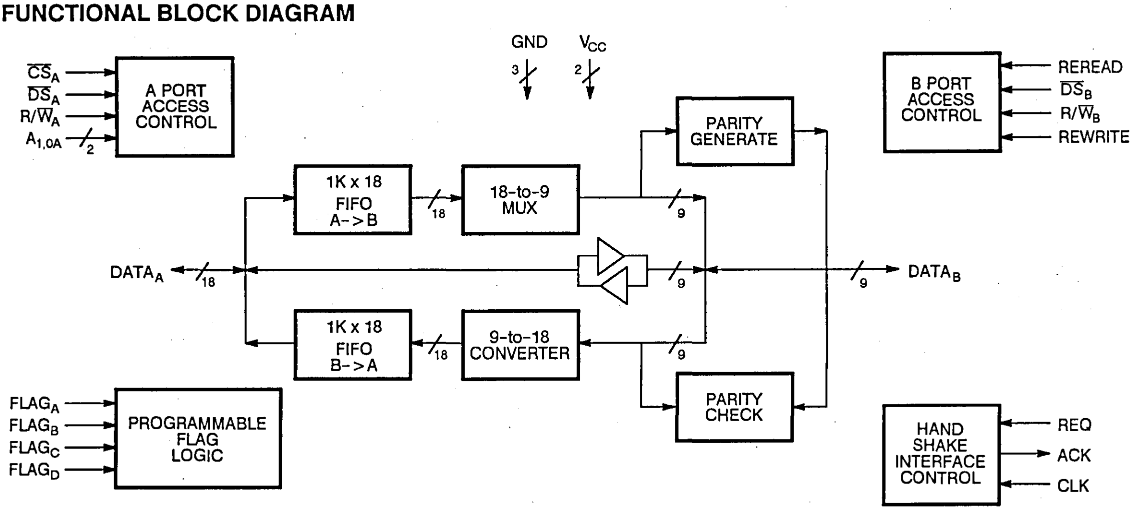
Four status flags can be programmed to access any one of eight internal flags. Four Full/Empty Flags can be chosen, as well as four Full + Offset or Empty + Offset Flags. The offset value can be determined by the user. The polarity of the flags can also be set by the user.

The BiFIFO has an innovative Reread (RER) and Rewrite (REW) capability. The internal read and write pointers can be set to a position determined by the user through a control register. Then, upon signalling the RER input, the read pointer is reset to the initial position and data is read again. With signalling REW, the write pointer is reset to the initial position and data is written again.

The BiFIFO is available in a 48-pin DIP, 48-pin 70 mil center SHRINK-DIP and surface mount 52-pin LCC and PLCC packages. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

6

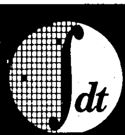
FUNCTIONAL BLOCK DIAGRAM



CEMOS and BiFIFO are trademarks of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-2016/–



CMOS PARALLEL IN-OUT FIFO MODULE 2K x 9-BIT & 4K x 9-BIT

IDT7M203S
IDT7M204S

FEATURES:

- First-In, First-Out memory module
- 2K x 9 organization (IDT7M203S)
- 4K x 9 organization (IDT7M204S)
- Low-power consumption
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Single 5V (±10%) power supply
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- High-performance CEMOS™ technology
- Pin compatible with IDT7201 and Mostek MK4501, but with four times word depth (IDT7M203S) or eight times (IDT7M204S)
- Module available with semiconductor components 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M203/204 are FIFO memory modules that utilize a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

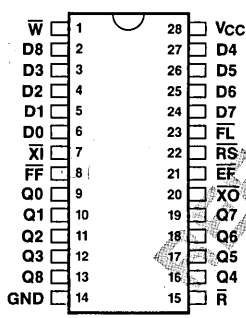
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 65ns (15MHz) for commercial and 70ns (14MHz) for military temperature ranges.

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

The IDT7M203/204 are constructed on a multi-layered ceramic substrate using four IDT7201 (512x9) or four IDT7202 (1Kx9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7201s and IDT7202s fabricated in IDT's high-performance CEMOS technology.

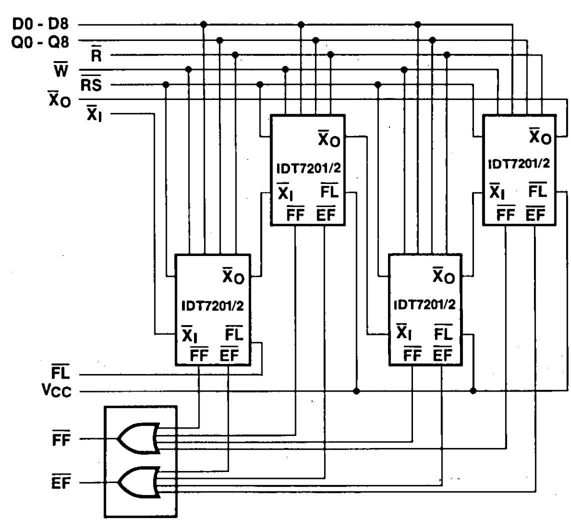
IDT's military FIFO modules have semiconductor components 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



DUAL 4-INPUT OR GATE

PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = DATA IN	$\overline{XO}$ = EXPANSION OUT	V_{CC} = 5V
$\overline{RS}$ = RESET	Q = DATA OUT	$\overline{FF}$ = FULL FLAG	GND = GROUND

CEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

CMOS PARALLEL IN-OUT FIFO MODULE 8K x 9-BIT & 16K x 9-BIT

IDT7M205S
IDT7M206S

FEATURES:

- First-In/First-Out memory module
- 8K x 9 organization (IDT7M205S)
- 16K x 9 organization (IDT7M206S)
- Low power consumption
  - Active: 840mW (typ. Com'l.)
  - Power Down: 176mW (max. Com'l)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Single 5V (±10%) power supply
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning flags
- High-performance CEMOS™ technology
- Pin-compatible with IDT7201 and Mostek MK4501, but with 16 times word depth (IDT7M205S) or 32 times (IDT7M206S)
- Module available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

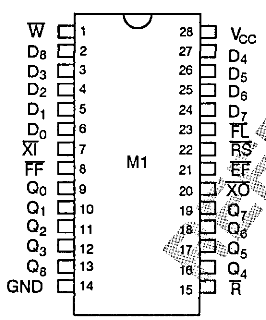
The IDT7M205S/206S are FIFO memory modules constructed on a multi-layered ceramic substrate using four IDT7203 (2K x 9) or four IDT7204 (4K x 9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7203s and IDT7204s fabricated in IDT's high-performance CEMOS technology. These devices utilize a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The devices have a read/write cycle time of 50ns (25MHz) for commercial and 65ns (15MHz) for military temperature ranges.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

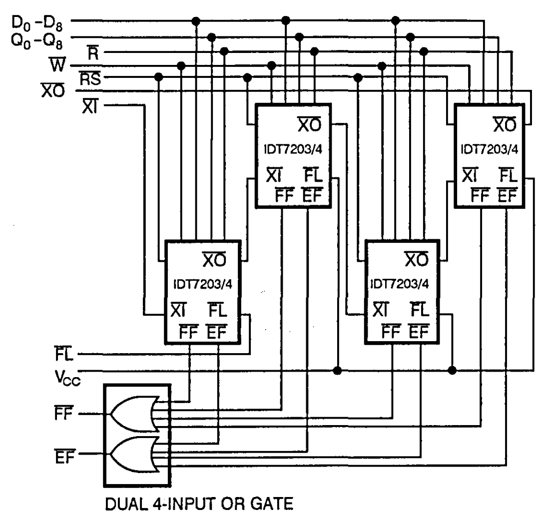
IDT's Military FIFO modules have semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = $DATA_{IN}$	$\overline{XO}$ = EXPANSION OUT	V_{CC} = 5V
$\overline{RS}$ = RESET	Q = $DATA_{OUT}$	$\overline{FF}$ = FULL FLAG	GND = GROUND

CEMOS is a trademark of Integrated Device Technology, Inc.

7

DIGITAL SIGNAL PROCESSING

Digital Signal Processing (DSP) building block components ease the high bandwidth digital processing of analog signals using complex algorithms. Integrated Device Technology's advances in VLSI design and CMOS technology have accelerated development of high-speed DSP building block components which address similar advances in DSP algorithms. All IDT DSP components are designed with a three-bus architecture, ideal for high bus bandwidth systems. These components can be divided into two categories: fixed-point components and floating-point components.

Fixed-point multipliers, multiplier-accumulators, multi-level pipeline register files and DSP arithmetic-logic units offer high-performance functions for 12-bit and 16-bit data. IDT offers the fastest fixed-point building blocks in the industry for the most demanding DSP system requirements.

Floating-point multipliers and ALUs operate in 32-bit and 64-bit IEEE Standard 754 floating-point format required in systems of the highest performance and precision. The floating-point format eliminates the shifting and scaling of data frequently performed in fixed-point. The IDT floating-point multiplier and ALU perform in the pipeline mode for systems needing the highest throughput and in the flow-through mode for systems needing maximum flexibility.

IDT's goal is to provide the highest level of integration and highest performance components for the most demanding DSP systems.

TABLE OF CONTENTS

CONTENTS **PAGE**

Digital Signal Processing

12 x 12-BIT PARALLEL CMOS MULTIPLIER-ACCUMULATOR

IDT7209L

Integrated Device Technology, Inc.

FEATURES:

- 12 x 12-bit parallel multiplier-accumulator with selectable accumulation and subtraction
- High-speed: 45ns maximum multiply-accumulate time
- Selectable accumulation, subtraction, rounding and preloading with 27-bit result
- Pin and functionally compatible with the TRW TDC1009J
- Performs subtraction and double precision addition and multiplication
- Produced using advanced CEMOS™ high-performance technology
- Low power consumption (less than 150mW typical)—less than 1/10 the power of compatible bipolar
- Inputs and outputs directly TTL-compatible
- Single 5V supply
- Available in topbraze DIP, LCC and Pin Grid Array
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7209 is a high-speed, low-power 12 x 12 parallel multiplier-accumulator that is ideally suited for real-time digital signal processing applications. Fabricated using IDT's CEMOS silicon gate technology, this device offers a very low-power alternative to existing bipolar and NMOS counterparts, with only 1/10 the power dissipation and exceptional speed (45ns maximum) performance.

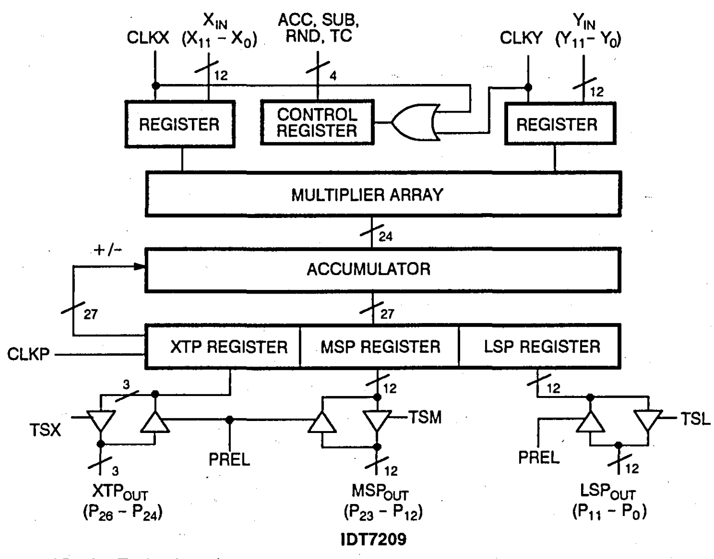
A pin and functional replacement for TRW's TDC1009J, the IDT7209 operates from a single 5 volt supply and is compatible with standard TTL logic levels. The architecture of the IDT7209 is fairly straightforward, featuring individual input and output registers with clocked D-type flip-flops, a preload capability which enables input data to be preloaded into the output registers, individual three-state output ports for the Extended Product (XTP) and Most Significant Product (MSP) and a Least Significant Product (LSP) output.

The X_{IN} and Y_{IN} data input registers may be specified through the use of the Two's Complement input (TC) as either two's complement or an unsigned magnitude, yielding a full-precision 24-bit result that may be accumulated to a full 27-bit result. The three output registers—Extended Product (XTP), Most Significant Product (MSP) and Least Significant Product (LSP)—are controlled by the respective TSX, TSM and TSL input lines.

The Accumulate input (ACC) enables the device to perform either a multiply or a multiply-accumulate function. In the multiply-accumulate mode, output data can be added to or subtracted from subsequent results. When the Subtraction (SUB) input is active simultaneously with an active ACC, a subtraction can be performed. The double precision accumulated result is rounded down to either a single precision or single precision plus 3-bit extended result. In the multiply mode, the Extended Product output (XTP) is sign extended in the two's complement mode or set to zero in the unsigned mode. The Round (RND) control rounds up the Most Significant Product (MSP) and the 3-bit Extended Product (XTP) outputs. When Preload input (PREL) is active, all the output buffers are forced into a high-impedance state (see Preload truth table) and external data can be loaded into the output register by using the TSX, TSL and TSM signals as input controls.

7

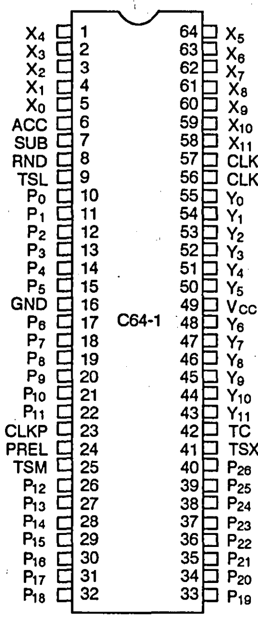
FUNCTIONAL BLOCK DIAGRAM



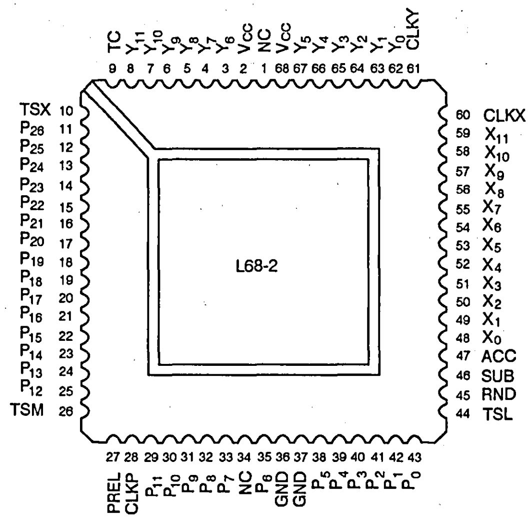
IDT7209

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

G68-2

	A	B	C	D	E	F	G	H	J	K	L
11		NC	CLKY	Y_1	Y_3	Y_5	Y_6	Y_8	Y_{10}	TC	
10	X_{11}	CLKX	Y_0	Y_2	Y_4	V_{CC}	Y_7	Y_9	Y_{11}	TSX	NC
09	X_9	X_{10}								P_{25}	P_{26}
08	X_7	X_8								P_{23}	P_{24}
07	X_5	X_6								P_{21}	P_{22}
06	X_3	X_4								P_{19}	P_{20}
05	X_1	X_2								P_{17}	P_{18}
04	ACC	X_0								P_{15}	P_{16}
03	RND	SUB								P_{13}	P_{14}
02	NC	TSL	P_1	P_3	P_5	P_6	P_8	P_{10}	CLKP	TSM	P_{12}
01	●	P_0	P_2	P_4	GND	P_7	P_9	P_{11}	PREL	NC	

Pin 1 Designator

PGA
TOP VIEW

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL}	Input Low Voltage	–	–	0.8	V

7

DC ELECTRICAL CHARACTERISTICS—FAST

(Commercial V_{CC}= 5V ±10%, T_A = 0°C to +70°C, Military V_{CC}= 5V ±10%, T_A = -55°C to +125°C
for Commercial clocked multiply times of 45, 55,65ns or Military, 55, 65, 75ns)

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.[1]	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.[1]	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	–	–	10	–	–	20	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	–	10	–	–	20	µA
I_{CC}[2]	Operating Power Supply Current	Outputs Open Measured at 10MHz[2]	–	40	80	–	40	100	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	–	20	50	–	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ -0.2V, $V_{IN} \leq$ 0.2V	–	4	20	–	4	25	mA
I_{CC}/f[2, 3]	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	–	–	6	–	–	8	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	–	0.4	–	–	0.4	V

NOTE:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN}= 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 80 + 6(f - 10)mA, where f = operating frequency in MHz. For the military range, I_{CC} = 100 + 8(f - 10) where f = operating frequency in MHz, f = $1/t_{MA}$.
3. For frequencies greater than 10MHz.

DC ELECTRICAL CHARACTERISTICS – SLOW

(Commercial V_{CC}= 5V ±10%, T_A = 0°C to +70°C, Military V_{CC}= 5V ±10%, T_A = -55°C to +125°C for Commercial clocked multiply times of 100, 135ns or Military, 120, 170ns)

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.[1]	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.[1]	MILITARY MAX.	UNIT
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	–	–	2	–	–	10	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	–	2	–	–	10	µA
I_{CC}[2]	Operating Power Supply Current	Outputs Open Measured at 10MHz[2]	–	30	60	–	30	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	–	10	30	–	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ -0.2V, $V_{IN} \leq$ 0.2V	–	0.1	1.0	–	0.1	2.0	mA
I_{CC}/f[2, 3]	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	–	–	5	–	–	7	mA/ MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	–	0.4	–	–	0.4	V

NOTE:
1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN}= 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 60 + 5(f - 10)mA, where f = operating frequency in MHz. For the military range, I_{CC} = 80 + 7(f - 10) where f = operating frequency in MHz, f = $1/t_{MA}$.
3. For frequencies greater than 10MHz.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7209L45 MIN.	IDT7209L45 MAX.	IDT7209L65 MIN.	IDT7209L65 MAX.	IDT7209L100 MIN.	IDT7209L100 MAX.	IDT7209L135 MIN.	IDT7209L135 MAX.	UNIT	TEST LOAD FIGURE
t_{MA}	Multiply-Accumulate Time	–	45	–	65	–	100	–	135	ns	1
t_D	Output Delay	–	25	–	35	–	35	–	40	ns	1
t_{ENA}	3 State Enable Time[1]	–	25	–	30	–	35	–	40	ns	2
t_{DIS}	3 State Disable Time[1]	–	25	–	30	–	35	–	40	ns	2
t_S	Input Register Set-up Time	15	–	25	–	25	–	25	–	ns	–
t_H	Input Register Hold Time	3	–	3	–	0	–	0	–	ns	–
t_{PW}	Clock Pulse Width	15	–	25	–	25	–	25	–	ns	–

NOTE:
1. Transition is measured ±500mV from steady state voltage with loading specified in Figure 2.

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7209L55 MIN.	IDT7209L55 MAX.	IDT7209L75 MIN.	IDT7209L75 MAX.	IDT7209L120 MIN.	IDT7209L120 MAX.	IDT7209L170 MIN.	IDT7209L170 MAX.	UNIT	TEST LOAD FIGURE
t_{MA}	Multiply-Accumulate Time	–	55	–	75	–	120	–	170	ns	1
t_D	Output Delay	–	30	–	35	–	40	–	45	ns	1
t_{ENA}	3 State Enable Time[1]	–	30	–	35	–	40	–	45	ns	2
t_{DIS}	3 State Disable Time[1]	–	30	–	35	–	40	–	45	ns	2
t_S	Input Register Set-up Time	20	–	25	–	30	–	30	–	ns	–
t_H	Input Register Hold Time	3	–	3	–	0	–	0	–	ns	–
t_{PW}	Clock Pulse Width	20	–	30	–	30	–	30	–	ns	–

NOTE:
1. Transition is measured ±500mV from steady state voltage with loading specified in Figure 2.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

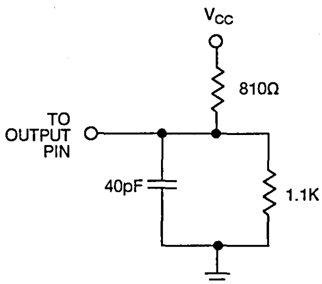


Figure 1. AC Output Test Load

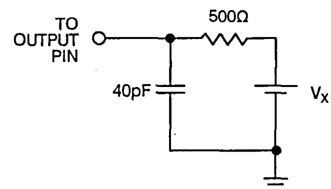


Figure 2. Output Three-State Delay Load (V_X = 0V or 2.6V)

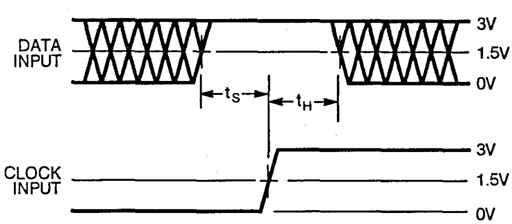


Figure 3. Set-Up And Hold Time

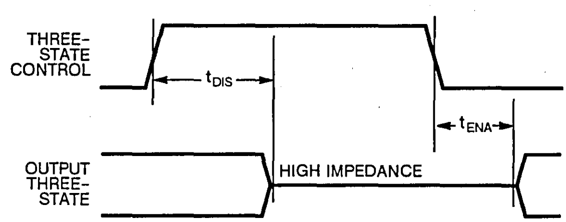


Figure 4. Three-State Control Timing Diagram

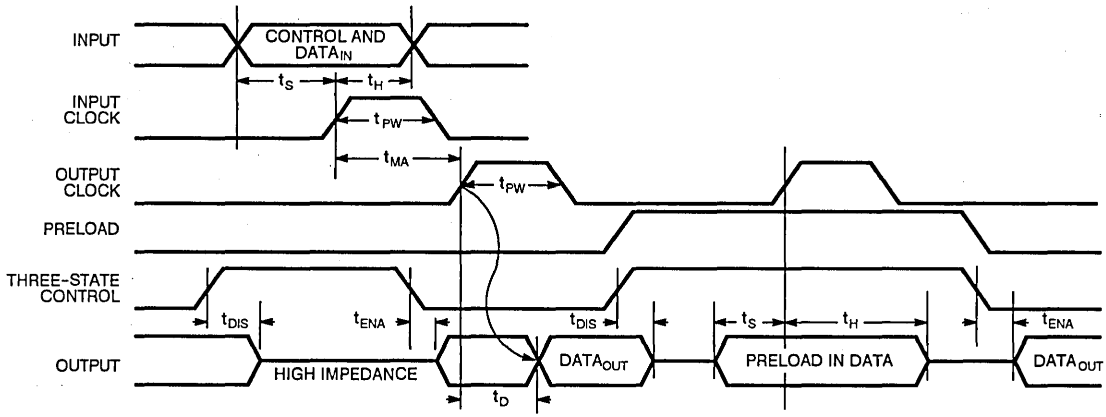


Figure 5. Timing Diagram

SIGNAL DESCRIPTIONS:

INPUTS:

X_{IN} (X_{11} - X_0)

Multiplicand Data Inputs

Y_{IN} (Y_{11} - Y_0)

Multiplier Data Inputs

INPUT CLOCKS:

CLKX, CLKY

Input data is loaded on the rising edge of these clocks.

CONTROLS:

ACC (Accumulate)

When ACC is high, the contents of the XTP, MSP and LSP registers are added to or subtracted from the multiplier output. When ACC is low, the device acts as a simple multiplier with no accumulation being performed and the next product generated will be stored directly into the output registers. The ACC signal is loaded on the rising edge of the CLKX or CLKY and must be valid for the duration of the data input.

SUB (Subtract)

When the ACC and SUB signals are both high, the contents of the output register are subtracted from the next product generated and the difference is stored back into the output registers at the rising edge of the next CLKP. When ACC is high and SUB is low, an addition instead of a subtraction is performed. Like the ACC signal, the SUB signal is loaded into the SUB register at the rising edge of either CLKX or CLKY and must be valid over the same period as the input data is valid. When the ACC is low, SUB acts as a "don't care" input.

TC (Two's Complement)

When the TC Control is high, it makes both the X and Y input two's complement inputs. When the TC Control is low, it makes both inputs, X and Y, unsigned magnitude inputs.

RND (Round)

A high level at this input adds a "1" to the most significant bit of the LSP to round up the XTP and MSP data. RND, like ACC and SUB, is loaded on the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

PREL (Preload)

When the PREL input is high, the output is driven to a high impedance state. When the TSX, TSL and TSM inputs are also high, the contents of the output register can be preset to the preload data applied to the output pins at the rising edge of CLKP. The PREL, TSM, TSL and TSX inputs must be valid over the same period that the preload input is valid.

TSX, TSL, TSM (Three State Output Controls)

The XTP, MSP and LSP registers are controlled by direct non-registered control signals. These output drivers are at high impedance (disabled) when control signals TSX, TSM and TSL are high and are enabled when TSX, TSM and TSL are low.

OUTPUT CLOCK:

CLKP

Output data is loaded into the output register on the rising edge of this clock.

OUTPUTS:

XTP (P_{26} - P_{24})

Extended Product Output (3-bits)

MSP (P_{23} - P_{12})

Most Significant Product

LSP (P_{11} - P_0)

Least Significant Product

PRELOAD TRUTH TABLE

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Hi Z
0	0	1	0	Q	Hi Z	Q
0	0	1	1	Q	Hi Z	Hi Z
0	1	0	0	Hi Z	Q	Q
0	1	0	1	Hi Z	Q	Hi Z
0	1	1	0	Hi Z	Hi Z	Q
0	1	1	1	Hi Z	Hi Z	Hi Z
1	0	0	0	Hi Z	Hi Z	Hi Z
1	0	0	1	Hi Z	Hi Z	PL
1	0	1	0	Hi Z	PL	Hi Z
1	0	1	1	Hi Z	PL	PL
1	1	0	0	PL	Hi Z	Hi Z
1	1	0	1	PL	Hi Z	PL
1	1	1	0	PL	PL	Hi Z
1	1	1	1	PL	PL	PL

NOTES:

Hi Z = Output buffers at high impedance (output disabled).

Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.

PL = Output buffers at high impedance or output disabled. Preload data supplied externally at output pins will be loaded into the output register at the rising edge of CLKP.

NOTES ON TWO'S COMPLEMENT FORMATS:

1. In two's complement notation, the location of the binary point that signifies the separation of the fractional and integer fields is just after the sign, between the sign bit (-2^0) and the next significant bit for the multiplier inputs. This same format is carried over to the output format, except that the extended significance of the integer field is provided to extend the utility of the accumulator. In the case of the output notation, the output binary point is located between the 2^0 and 2^{-1} bit positions. The location of the binary point is arbitrary, as long as there is consistency with both the input and output formats. The number field can be considered entirely integer with the binary point just to the right of the least significant bit for the input, product and the accumulated sum.

2. When in the non-accumulating mode, the first four bits (P_{26} through P_{23}) will all indicate the sign of the product. Additionally, the P_{22} term will also indicate the sign with one exception, when multiplying -1×-1. With the additional bits that are available in this multiplier, the -1×-1 is a valid operation that yields a $+1$ product.

3. In operations that require the accumulation of single products or sum of products, there is no change in format. To allow for a valid summation beyond that available for a single multiplication product, three additional significant bits (guard bits) are provided. This is the same as if the product was accumulated off-chip in a separate 27-bit wide adder. Taking the sign at the most significant bit position will guarantee that the largest number field will be used. When the accumulated sum only occupies the right hand portion of the accumulator, the sign will be extended into the lesser significant bit positions.

7

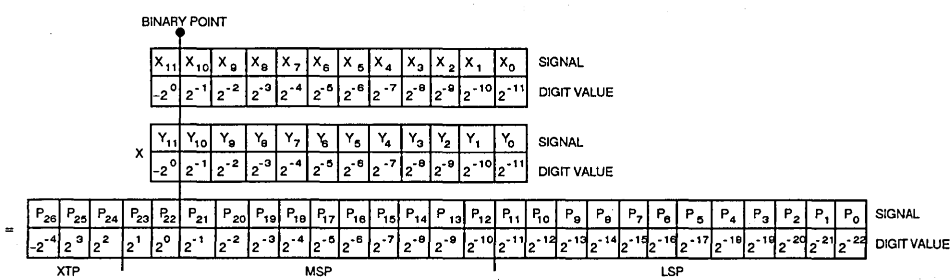


Figure 6. Fractional Two's Complement Notation

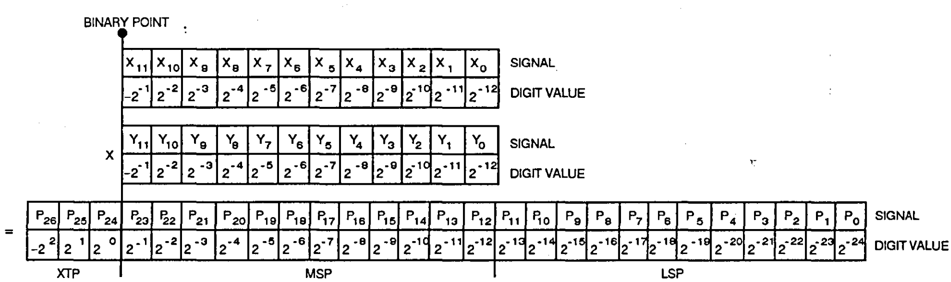


Figure 7. Fractional Unsigned Magnitude Notation

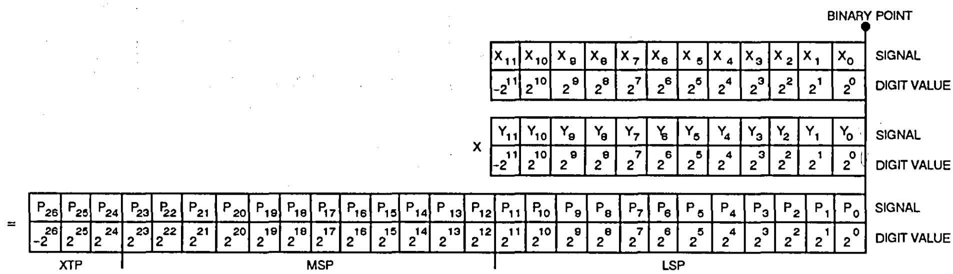


Figure 8. Integer Two's Complement Notation

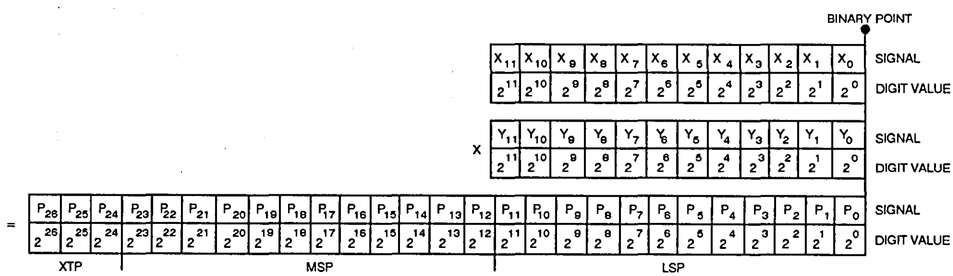


Figure 9. Integer Unsigned Magnitude Notation

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range:
- Blank — Commercial (0°C to +70°C)
- B — Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:
- C — Topbraze DIP
- L — Leadless Chip Carrier
- G — Pin Grid Array

Speed in Nanoseconds:

COM'L.	MIL.
45	55
65	75
100	120
135	170

Power:
- L — Low Power

Device Type:
- 7209 — 12 x 12 Parallel CMOS Multiplier-Accumulator

Integrated Device Technology, Inc.

16 x 16-BIT PARALLEL CMOS MULTIPLIER-ACCUMULATOR

IDT7210L IDT7243L

FEATURES:

- 16 x 16-bit parallel multiplier-accumulator with selectable accumulation and subtraction
- High-speed: 35ns multiply-accumulate time
- IDT7210 features selectable accumulation, subtraction, rounding and preloading with 35-bit result
- IDT7243 features selectable accumulation, subtraction and rounding with 19-bit result
- IDT7210 is pin and functionally compatible with the TRW TDC1010J
- IDT7243 is pin and functionally compatible with the TRW TDC1043
- Both devices perform subtraction and double precision addition and multiplication
- Produced using advanced CEMOS ™ high-performance technology
- Low power consumption (less than 250mW typical) – less than 1/10 the power of compatible bipolar and 1/7 the power of NMOS designs
- Input and output directly TTL-compatible
- Single 5V supply
- Available in plastic and topbraze DIP, SHRINK-DIP, LCC, Fine-Pitch LCC, PLCC, Flatpack and Pin Grid Array
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7210/7243 are high-speed, low-power 16 x 16-bit parallel multiplier-accumulators that are ideally suited for real-time digital signal processing applications. Fabricated using CEMOS silicon gate technology, these devices offer a very low-power alternative to existing bipolar and NMOS counterparts, with only 1/7 to 1/10 the power dissipation and exceptional speed (35ns maximum) performance.

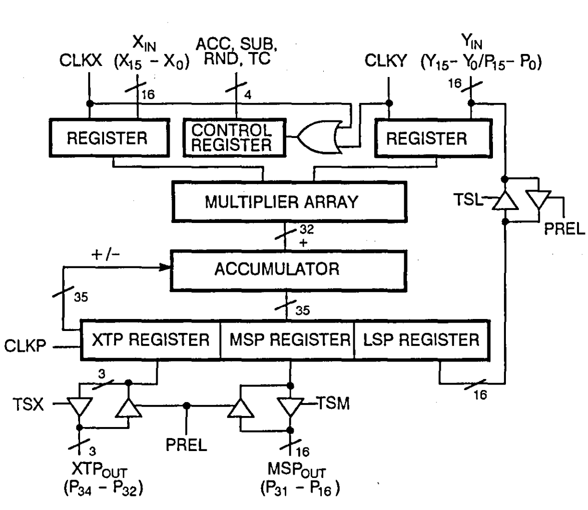
Pin and functional replacements for TRW's TDC1010J/TDC1043, the IDT7210/7243 operate from a single 5 volt supply and are compatible with standard TTL logic levels. The architecture of the IDT7210/7243 is fairly straightforward, featuring individual input and output registers with clocked D-type flip-flops, a preload capability (IDT7210 only) which enables input data to be preloaded into the output registers, individual three-state output ports for the Extended Product (XTP) and Most Significant Product (MSP) and a Least Significant Product output (LSP) which is multiplexed with the Y input. Unlike the IDT7210, the IDT7243 does not have either a preload capability or a Least Significant Product (LSP) output accessible externally.

The X_{IN} and Y_{IN} data input registers may be specified through the use of the Two's Complement input (TC) as either a two's complement or an unsigned magnitude, yielding a full-precision 32-bit result that may be accumulated to a full 35-bit result. The three output registers – Extended Product (XTP), Most Significant Product (MSP) and Least Significant Product (LSP) – are controlled by the respective TSX, TSM and TSL input lines. The LSP output can be routed through Y_{IN} ports in the IDT7210.

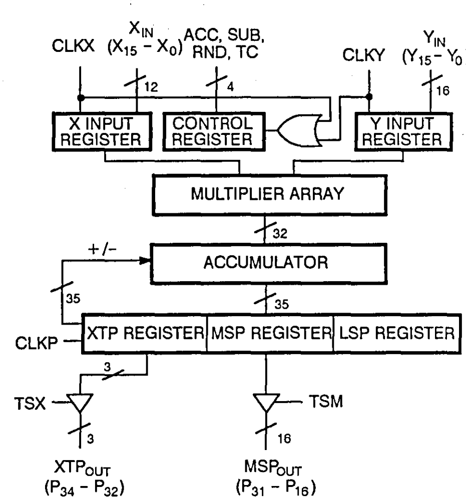
Continued on Page 2

7

FUNCTIONAL BLOCK DIAGRAM



IDT7210



IDT7243

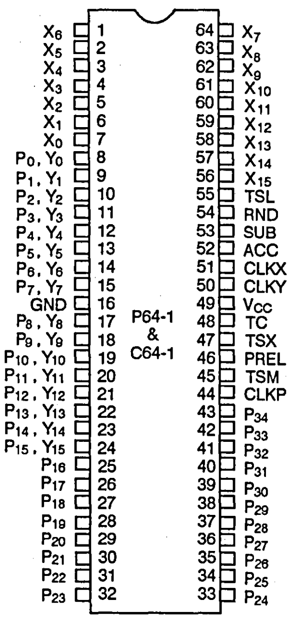
CEMOS is a trademark of Integrated Device Technology, Inc.

DESCRIPTION (Continued)

The Accumulate input (ACC) enables the device to perform either a multiply or a multiply-accumulate function. In the multiply-accumulate mode, output data can be added to or subtracted from subsequent results. When the Subtraction (SUB) input is active simultaneously with an active ACC, a subtraction can be performed. The double precision accumulated result is rounded down to either a single precision or single precision plus 3-bit extended result. In the multiply mode, the Extended Product output (XTP) is sign extended in the two's complement mode or set to zero in the unsigned mode. The Round (RND) control rounds up the Most Significant Product (MSP) and the 3-bit Extended Product (XTP) outputs. When Preload input (PREL) is active, all the output buffers are forced into a high-impedance state (see Preload truth table) and external data can be loaded into the output register by using the TSX, TSL and TSM signals as input controls.

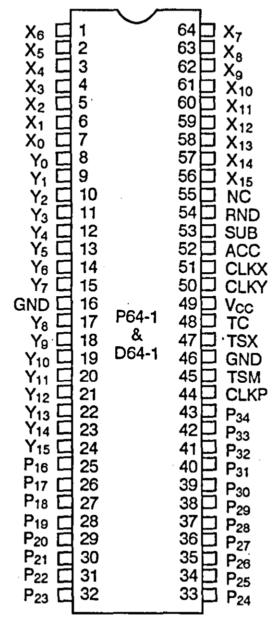
PIN CONFIGURATIONS

IDT7210



DIP
TOP VIEW

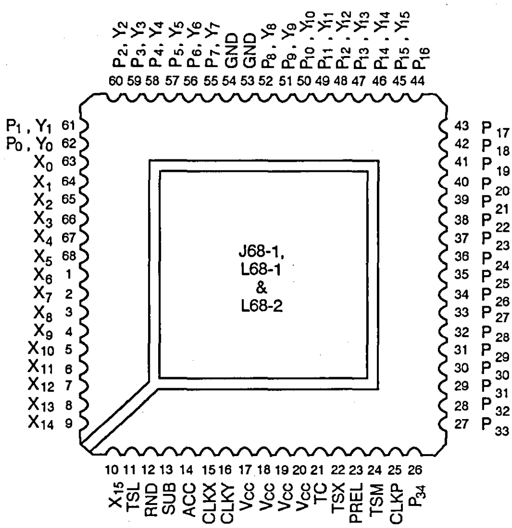
IDT7243



DIP
TOP VIEW

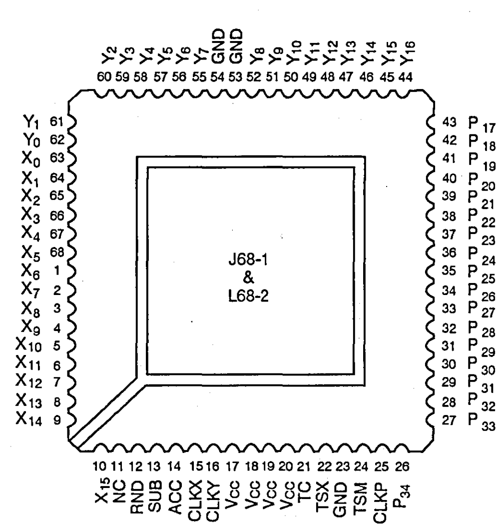
PIN CONFIGURATIONS

IDT7210



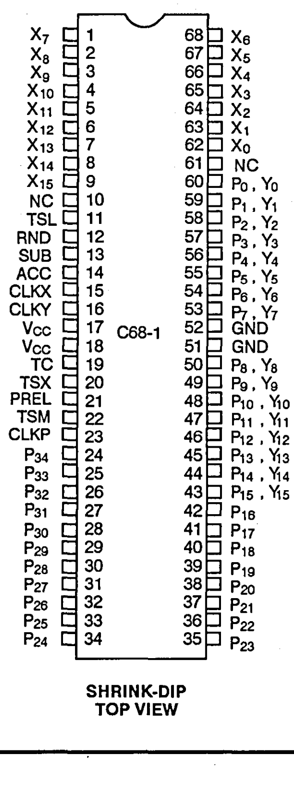
LCC/PLCC/FINE-PITCH LCC
TOP VIEW

IDT7243



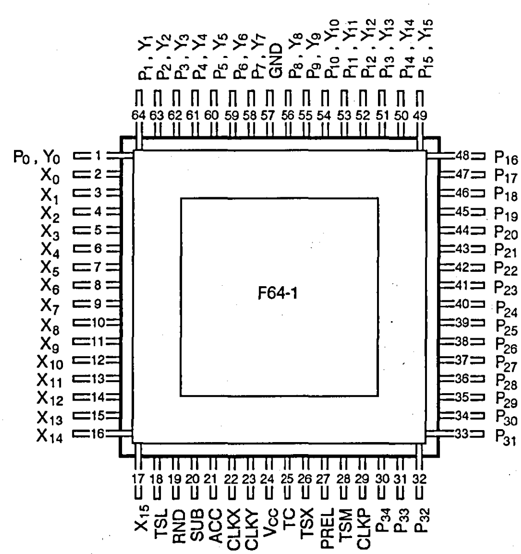
LCC/PLCC
TOP VIEW

IDT7210



SHRINK-DIP
TOP VIEW

IDT7210



FLATPACK
TOP VIEW

PIN CONFIGURATIONS (Continued)

IDT7210

	A	B	C	D	E	F	G	H	J	K	L
11		NC	X_{15}	RND	ACC	CLK_Y	TC	PREL	CLK_P	P_{33}	
10	X_{13}	X_{14}	TSL	SUB	CLK_X	V_{CC}	TSX	TSM	P_{34}	P_{32}	NC
09	X_{11}	X_{12}								P_{30}	P_{31}
08	X_9	X_{10}								P_{28}	P_{29}
07	X_7	X_8								P_{26}	P_{27}
06	X_5	X_6				G68-2				P_{24}	P_{25}
05	X_3	X_4								P_{22}	P_{23}
04	X_1	X_2								P_{20}	P_{21}
03	Y_0, P_0	X_0								P_{18}	P_{19}
02	NC	Y_1, P_1	Y_3, P_3	Y_5, P_5	Y_7, P_7	Y_8, P_8	Y_{10}, P_{10}	Y_{12}, P_{12}	Y_{14}, P_{14}	P_{16}	P_{17}
01	●	Y_2, P_2	Y_4, P_4	Y_6, P_6	GND	Y_9, P_9	Y_{11}, P_{11}	Y_{13}, P_{13}	Y_{15}, P_{15}	NC	

Pin 1 Designator

PGA
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL}	Input Low Voltage	–	–	0.8	V

DC ELECTRICAL CHARACTERISTICS – FAST

(Commercial V_{CC}= 5V ±10%, T_A = 0°C to +70°C, Military V_{CC}= 5V ±10%, T_A = -55°C to +125°C
for Commercial clocked multiply times of 20, 25, 35, 45, 55, 65, 75ns or Military 25, 30, 40, 55, 65, 75, 85ns)

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	–	–	10	–	–	20	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	–	10	–	–	20	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	–	45	90	–	45	110	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	–	20	50	–	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ -0.2V, $V_{IN} \leq$ 0.2V	–	4	10	–	4	12	mA
I_{CC}/f (2, 3)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	–	–	6	–	–	8	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	–	–	2.4	–	–	V
V_{OL}(4)	Output Low Voltage	V_{CC} = Min., I_{OL} = 4mA	–	–	0.4	–	–	0.4	V

NOTES:
1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 90 + 6(f – 10)mA, where f = operating frequency in MHz. For the military range, I_{CC} = 110 + 8(f – 10) where f = operating frequency in MHz, f = 1/t_{MA}.
3. For frequencies greater than 10MHz.
4. I_{OL} = 8mA for t_{MA} = 20ns to 55ns.

7

DC ELECTRICAL CHARACTERISTICS – SLOW

(Commercial V_{CC}= 5V ±10%, T_A = 0°C to +70°C, Military V_{CC}= 5V ±10%, T_A = -55°C to +125°C
for Commercial clocked multiply times of 100, 165ns or Military, 120, 200ns)

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	–	–	2	–	–	10	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	–	2	–	–	10	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	–	35	70	–	35	90	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	–	10	30	–	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ -0.2V, $V_{IN} \leq$ 0.2V	–	0.1	1.0	–	0.1	2.0	mA
I_{CC}/f (2, 3)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	–	–	5	–	–	7	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4mA	–	–	0.4	–	–	0.4	V

NOTES:
1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN}= 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 70 + 5(f – 10)mA, where f = operating frequency in MHz. For the military range, I_{CC} = 90 + 7(f – 10) where f = operating frequency in MHz, f = 1/t_{MA}.
3. For frequencies greater than 10MHz.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	7210L35		7210L45 7243L45		7210L55 7243L55		7210L65 7243L65		7210L75 7243L75		7210L100 7243L100		7210L160 7243L160		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{MA} (2)	Multiply-Accumulate Time	–	35	–	45	–	55	–	65	–	75	–	100	–	165	ns
t_D(2)	Output Delay	–	25	–	25	–	30	–	35	–	35	–	35	–	40	ns
t_{ENA} (3)	3-State Enable Time (1)	–	25	–	25	–	30	–	30	–	35	–	35	–	40	ns
t_{DIS}(3)	3-State Disable Time(1)	–	25	–	25	–	30	–	30	–	35	–	35	–	40	ns
t_S	Input Register Set-up Time	12	–	15	–	20	–	25	–	25	–	25	–	30	–	ns
t_H	Input Register Hold Time	3	–	3	–	3	–	3	–	3	–	0	–	0	–	ns
t_{PW}	Clock Pulse Width	10	–	15	–	20	–	25	–	25	–	25	–	25	–	ns

NOTES:
1. Transition is measured ±500mV from steady state voltage with loading specified in Figure 2.
2. See Test Load Figure 1.
3. See Test Load Figure 2.

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ±10%, T_A = –55°C to +125°C)

SYMBOL	PARAMETER	7210L40		7210L55 7243L55		7210L65 7243L65		7210L75 7243L75		7210L85 7243L85		7210L120 7243L120		7210L200 7243L200		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{MA} (2)	Multiply-Accumulate Time	–	40	–	55	–	65	–	75	–	85	–	120	–	200	ns
t_D(2)	Output Delay	–	25	–	30	–	35	–	35	–	35	–	40	–	45	ns
t_{ENA} (3)	3 State Enable Time(1)	–	25	–	30	–	30	–	35	–	35	–	40	–	45	ns
t_{DIS} (3)	3 State Disable Time(1)	–	25	–	30	–	30	–	30	–	35	–	40	–	45	ns
t_S	Input Register Set-up Time	15	–	20	–	25	–	25	–	25	–	30	–	30	–	ns
t_H	Input Register Hold Time	3	–	3	–	3	–	3	–	3	–	0	–	0	–	ns
t_{PW}	Clock Pulse Width	15	–	20	–	25	–	25	–	30	–	30	–	30	–	ns

NOTES:
1. Transition is measured ±500mV from steady state voltage with loading specified in Figure 2.
2. See Test Load Figure 1.
3. See Test Load Figure 2.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

CAPACITANCE (T_A= +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

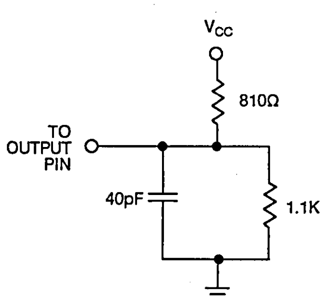


Figure 1. AC Output Test Load

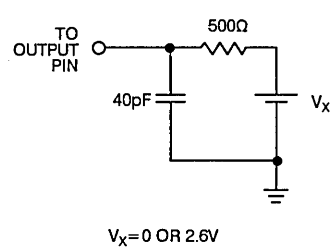


Figure 2. Output Three-State Delay Load

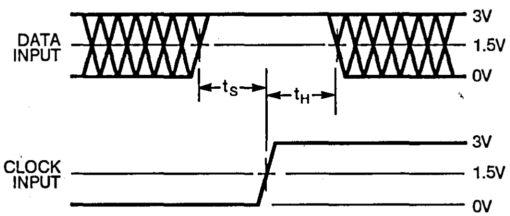


Figure 3. Set-Up and Hold Time

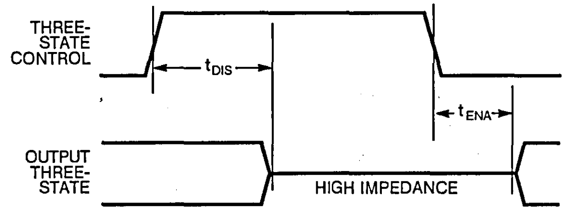


Figure 4. Three-State Control Timing Diagram

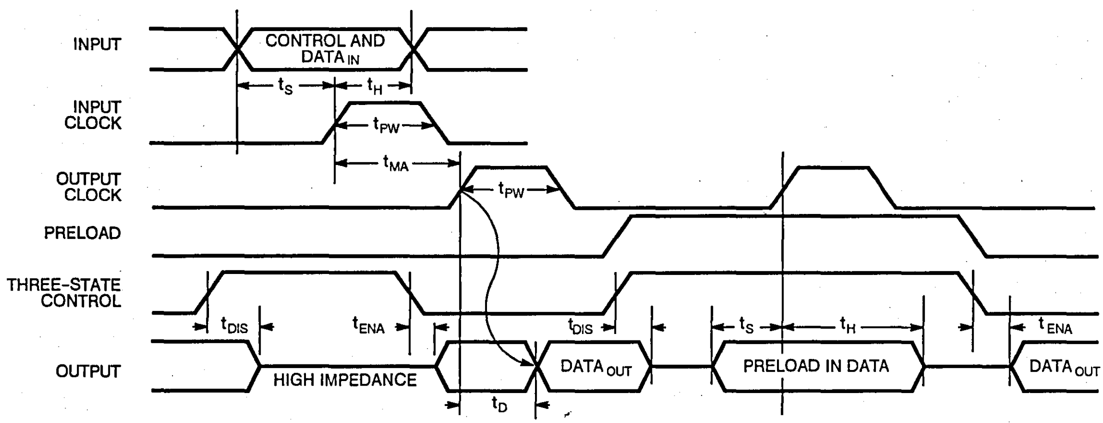


Figure 5. Timing Diagram

SIGNAL DESCRIPTIONS:

INPUTS:

X_{IN} (X_{15} - X_0)

Multiplicand Data Inputs

Y_{IN} (Y_{15} - Y_0)

Multiplier Data Inputs

INPUT CLOCKS:

CLKX, CLKY

Input data is loaded on the rising edge of these clocks.

CONTROLS:

ACC (Accumulate)

When ACC is high, the contents of the XTP, MSP and LSP registers are added to or subtracted from the multiplier output. When ACC is low, the device acts as a simple multiplier with no accumulation being performed and the next product generated will be stored directly into the output registers. The ACC signal is loaded on the rising edge of the CLKX or CLKY and must be valid for the duration of the data input.

SUB (Subtract)

When the ACC and SUB signals are both high, the contents of the output register are subtracted from the next product generated and the difference is stored back into the output registers at the rising edge of the next CLKP. When ACC is high and SUB is low, an addition instead of a subtraction is performed. Like the ACC signal, the SUB signal is loaded into the SUB register at the rising edge of either CLKX or CLKY and must be valid over the same period as the input data is valid. When the ACC is low, SUB acts as a "don't care" input.

TC (Two's Complement)

When the TC Control is high, it makes both the X and Y input two's complement inputs. When the TC Control is low, it makes both inputs, X and Y, unsigned magnitude inputs.

RND (Round)

A high level at this input adds a "1" to the most significant bit of the LSP to round up the XTP and MSP data. RND, like ACC and SUB, is loaded on the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

PREL (Preload) (IDT7210 only)

When the PREL input is high, the output is driven to a high impedance state. When the TSX, TSL and TSM inputs are also high, the contents of the output register can be preset to the preload data applied to the output pins at the rising edge of CLKP. The PREL, TSM, TSL and TSX inputs must be valid over the same period that the preload input is valid.

Y_{IN}/LSP Output—(LSP output, IDT7210 only)

Shares functions between 16-bit data input (Y_{IN}) and the least significant product output (LSP).

TSX, TSL, TSM (Three-State Output Controls)

The XTP, MSP and LSP registers are controlled by direct non-registered control signals. These output drivers are at high impedance (disabled) when control signals TSX, TSM and TSL are high and are enabled when TSX, TSM and TSL are low.

OUTPUT CLOCK:

CLKP

Output data is loaded into the output register on the rising edge of this clock.

OUTPUTS:

XTP (P_{34} - P_{32})

Extended Product Output (3-bits)

MSP (P_{31} - P_{16})

Most Significant Product

LSP (P_{15} - P_0)

Least Significant Product (IDT7210 only), shared with Y_{IN} input.

NOTES ON TWO'S COMPLEMENT FORMATS:

1. In two's complement notation, the location of the binary point that signifies the separation of the fractional and integer fields is just after the sign, between the sign bit (-2^0) and the next significant bit for the multiplier inputs. This same format is carried over to the output format, except that the extended significance of the integer field is provided to extend the utility of the accumulator. In the case of the output notation, the output binary point is located between the 2^0 and 2^{-1} bit positions. The location of the binary point is arbitrary, as long as there is consistency with both the input and output formats. The number field can be considered entirely integer with the binary point just to the right of the least significant bit for the input, product and the accumulated sum.
2. When in the non-accumulating mode, the first four bits (P_{34} to P_{31}) will all indicate the sign of the product. Additionally, the P_{30} term will also indicate the sign with one exception, when multiplying -1×-1. With the additional bits that are available in this multiplier, the -1×-1 is a valid operation that yields a $+1$ product.
3. In operations that require the accumulation of single products or sum of products, there is no change in format. To allow for a valid summation beyond that available for a single multiplication product, three additional significant bits (guard bits) are provided. This is the same as if the product was accumulated off-chip in a separate 35-bit wide adder. Taking the sign at the most significant bit position will guarantee that the largest number field will be used. When the accumulated sum only occupies the right hand portion of the accumulator, the sign will be extended into the lesser significant bit positions.

PRELOAD TRUTH TABLE (IDT7210 only)

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Hi Z
0	0	1	0	Q	Hi Z	Q
0	0	1	1	Q	Hi Z	Hi Z
0	1	0	0	Hi Z	Q	Q
0	1	0	1	Hi Z	Q	Hi Z
0	1	1	0	Hi Z	Hi Z	Q
0	1	1	1	Hi Z	Hi Z	Hi Z
1	0	0	0	Hi Z	Hi Z	Hi Z
1	0	0	1	Hi Z	Hi Z	PL
1	0	1	0	Hi Z	PL	Hi Z
1	0	1	1	Hi Z	PL	PL
1	1	0	0	PL	Hi Z	Hi Z
1	1	0	1	PL	Hi Z	PL
1	1	1	0	PL	PL	Hi Z
1	1	1	1	PL	PL	PL

NOTES:

Hi Z = Output buffers at high impedance (output disabled).

Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.

PL = Output buffers at high impedance or output disabled. Preload data supplied externally at output pins will be loaded into the output register at the rising edge of CLKP.

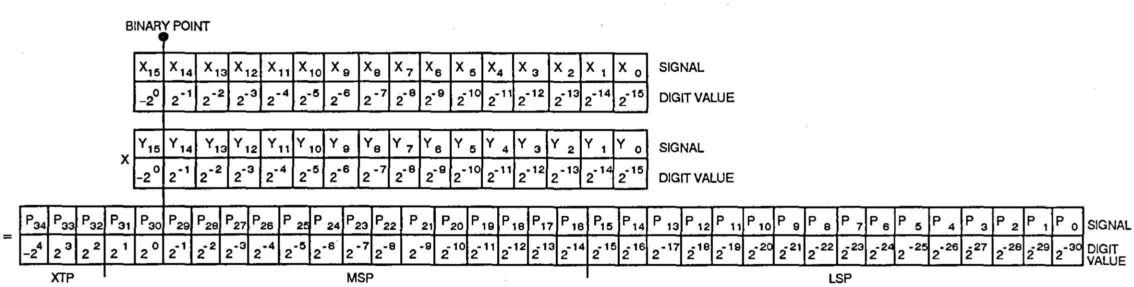


Figure 6. Fractional Two's Complement Notation

BINARY POINT

X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	SIGNAL
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	DIGIT VALUE

X

Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	SIGNAL
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	DIGIT VALUE

=

P_{34}	P_{33}	P_{32}	P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0	SIGNAL
2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}	2^{-32}	DIGIT VALUE

XTP MSP LSP

Figure 7. Fractional Unsigned Magnitude Notation

BINARY POINT

X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	SIGNAL
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

X

Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	SIGNAL
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

=

P_{34}	P_{33}	P_{32}	P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0	SIGNAL
-2^{34}	2^{33}	2^{32}	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

XTP MSP LSP

Figure 8. Integer Two's Complement Notation

BINARY POINT

X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	SIGNAL
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

X

Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	SIGNAL
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

=

P_{34}	P_{33}	P_{32}	P_{31}	P_{30}	P_{29}	P_{28}	P_{27}	P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0	SIGNAL
2^{34}	2^{33}	2^{32}	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

XTP MSP LSP

Figure 9. Integer Unsigned Magnitude Notation

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

P	Plastic DIP
XC	Sidebraze SHRINK-DIP*
C	Topbraze DIP
J	Plastic Leaded Chip Carrier
XL	Leadless Chip Carrier (25 MIL Center)*
L	Leadless Chip Carrier
F	Flatpack*
G	Pin Grid Array*

Speed (Speed in Nanoseconds)

COM'L.	MIL.
35*	40*
45	55
55	65
65	75
100	85
165	120
	200

Power

L	Low Power

Device Type

7210 7243	16 x 16 Parallel CMOS Multiplier-Accumulator

* IDT7210 only.

7

12 x 12-BIT PARALLEL CMOS MULTIPLIER

IDT7212L IDT7213L

FEATURES:

- 12 x 12-bit parallel multiplier with double precision product
- High-speed: 35ns maximum clock to multiply time
- Low power consumption: 150mW typical, less than 1/10 the power of compatible bipolar parts
- Produced with advanced CEMOS ™ high-performance technology
- IDT7212L is pin and functionally compatible with TRW MPY012H
- IDT7213L requires only a single clock with register enables
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Single 5V power supply
- Input and output directly TTL-compatible
- Three-state output
- Available in topbraze DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7212/IDT7213 are high-speed, low-power 12 x 12-bit multipliers ideal for fast, real-time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, high-reliability technology, CEMOS, has achieved speeds (35ns max.) exceeding bipolar at 1/10 the power consumption.

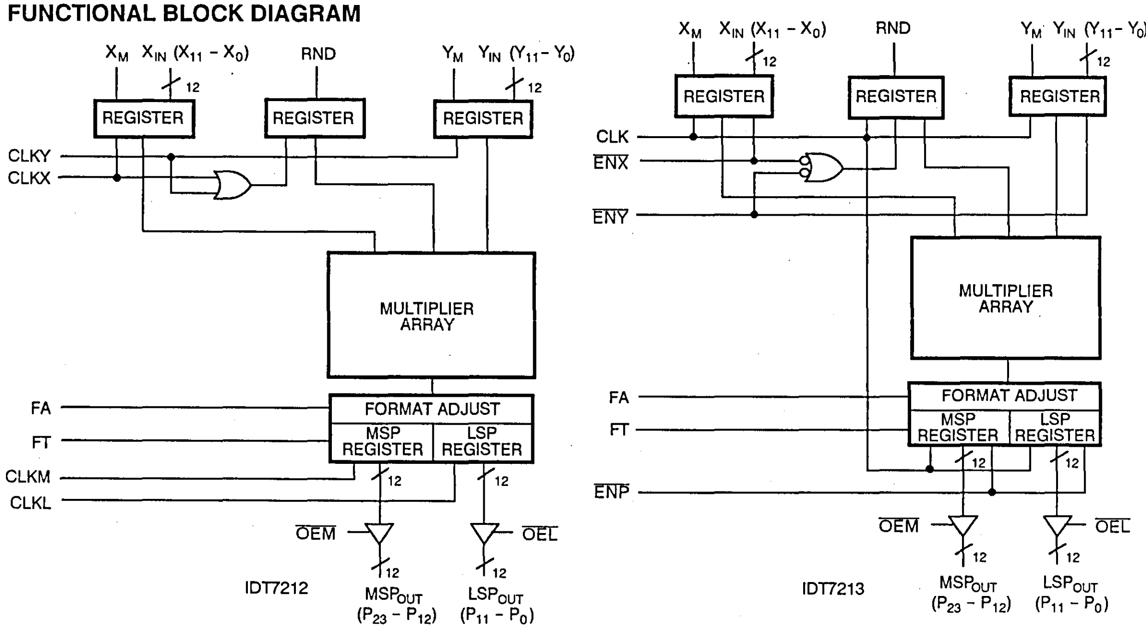
The IDT7212/IDT7213 are ideal for applications requiring high-speed multiplications such as fast Fourier transform analysis digital filtering, graphic display systems, speech synthesis and recognition and in any system requirement where multiplication speeds of a mini/micro computer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge triggered D-type flip-flop. With the IDT7212, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The IDT7213 has only a single clock input (CLK) and three register enables. $\overline{ENX}$ and $\overline{ENY}$ control the two input registers, while $\overline{ENP}$ controls the entire product.

The IDT7212/IDT7213 offer additional flexibility with the FA control. The FA control formats the output for 2's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

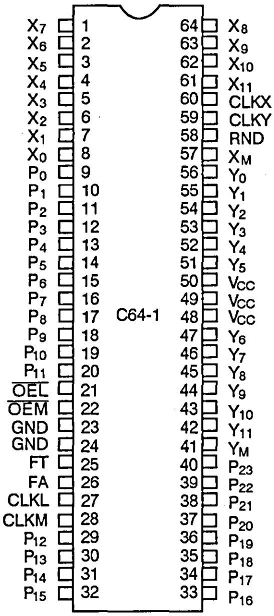
FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

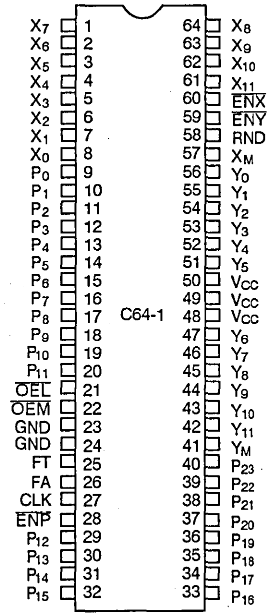
PIN CONFIGURATIONS

IDT7212



DIP
TOP VIEW

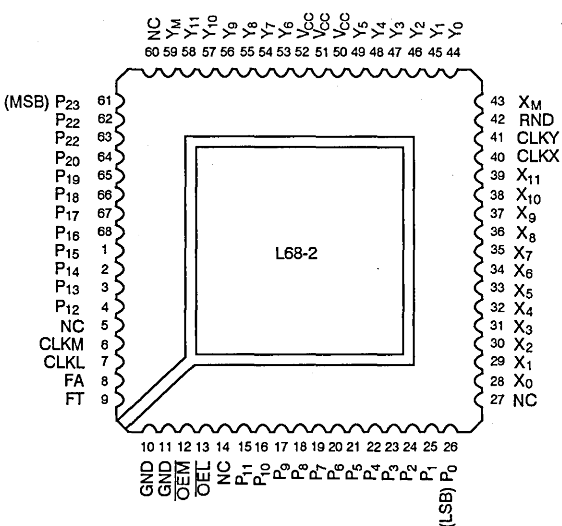
IDT7213



DIP
TOP VIEW

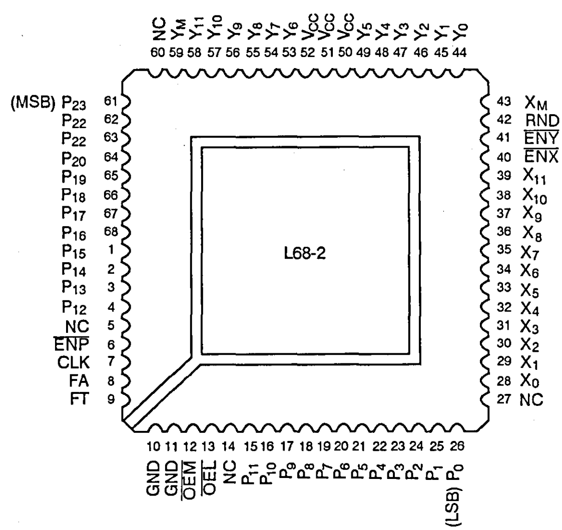
7

IDT7212



LCC
TOP VIEW

IDT7213



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.4	1.4	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL}	Input Low Voltage	–	–	0.8	V

DC ELECTRICAL CHARACTERISTICS – FAST

(Commercial V_{CC} = 5V ±10%, T_A = 0°C to +70°C, Military V_{CC} = 5V ±10%, T_A = -55°C to +125°C)
for Commercial clocked multiply times of 30, 35, 45, 70ns or Military, 40, 55, 90ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.[1]	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.[1]	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	–	–	10	–	–	20	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	–	10	–	–	20	µA
I_{CC}[2]	Operating Power Supply Current	Outputs Open Measured at 10MHz[2]	–	30	65	–	30	85	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	–	20	50	–	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq$ 0.2V	–	4	20	–	4	25	mA
I_{CC} /f[2, 3]	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	–	–	6	–	–	8	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	–	0.4	–	–	0.4	V

NOTES:
1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 65 + 6(f - 10)mA, where f= operating frequency in MHz. For the military range, I_{CC} = 85 + 8(f - 10) where f = operating frequency in MHz, f = 1/t_{MUC}(IDT7212), f = 1/t_{MC} (IDT7213).
3. For frequencies greater than 10MHz.

DC ELECTRICAL CHARACTERISTICS—SLOW

(Commercial V_{CC} = 5V ±10%, T_A = 0°C to +70°C, Military V_{CC} = 5V ±10%, T_A = -55°C to +125°C) for Commercial clocked multiply times of 115ns or Military, 140ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	–	–	2	–	–	10	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	–	2	–	–	10	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	–	25	55	–	25	75	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	–	10	30	–	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq$ 0.2V	–	0.1	1.0	–	0.1	2.0	mA
I_{CC} /f(2, 3)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	–	–	5	–	–	7	mA/ MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	–	0.4	–	–	0.4	V

NOTES:
1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 55 + 5(f - 10)mA, where f= operating frequency in MHz. For the military range, I_{CC} = 75 + 7(f - 10) where f = operating frequency in MHz, f = 1/t_{MUC}(IDT7212), f = 1/t_{MC} (IDT7213).
3. For frequencies greater than 10MHz.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7212L35 IDT7213L35 MIN.	MAX.	IDT7212L45 IDT7213L45 MIN.	MAX.	IDT7212L70 IDT7213L70 MIN.	MAX.	IDT7212L115 IDT7213L115 MIN.	MAX.	UNIT	TEST LOAD FIGURE
t_{MUC}	Unclocked Multiply Time	–	55	–	65	–	105	–	155	ns	1
t_{MC}	Clocked Multiply Time	–	35	–	45	–	70	–	115	ns	1
t_S	X, Y, RND Set-up Time	15	–	20	–	20	–	25	–	ns	1
t_H	X, Y, RND Hold Time	3	–	3	–	2	–	0	–	ns	1
t_{PWH}	Clock Pulse Width High	15	–	20	–	20	–	25	–	ns	1
t_{PWL}	Clock Pulse Width Low	15	–	20	–	20	–	25	–	ns	1
t_{PDP}	Output Clock to P	–	25	–	25	–	30	–	40	ns	1
t_{ENA}	3 State Enable Time(2)	–	25	–	30	–	35	–	40	ns	2
t_{DIS}	3 State Disable Time(2)	–	25	–	25	–	30	–	35	ns	2
t_S	Clock Enable Set-up Time (IDT7213 only)	15	–	20	–	25	–	25	–	ns	1
t_H	Clock Enable Hold Time (IDT7213 only)	3	–	3	–	3	–	0	–	ns	1
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML(1) (IDT7212 only)	0	–	0	–	0	–	0	–	ns	

NOTES:
1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage with loading specified in Figure 2.

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7212L40 IDT7213L40		IDT7212L55 IDT7213L55		IDT7212L90 IDT7213L90		IDT7212L140 IDT7213L140		UNIT	TEST LOAD FIGURE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{MUC}	Unclocked Multiply Time	–	60	–	75	–	130	–	185	ns	1
t_{MC}	Clocked Multiply Time	–	40	–	55	–	90	–	140	ns	1
t_S	X, Y, RND Set-up Time	20	–	20	–	25	–	30	–	ns	1
t_H	X, Y, RND Hold Time	3	–	3	–	2	–	0	–	ns	1
t_{PWH}	Clock Pulse Width High	20	–	25	–	30	–	30	–	ns	1
t_{PWL}	Clock Pulse Width Low	20	–	25	–	30	–	30	–	ns	1
t_{PDP}	Output Clock to P	–	25	–	30	–	35	–	45	ns	1
t_{ENA}	3 State Enable time(2)	–	25	–	30	–	40	–	45	ns	2
t_{DIS}	3 State Disable Time(2)	–	25	–	25	–	40	–	45	ns	2
t_S	Clock Enable Set-up Time (IDT7213 only)	20	–	25	–	30	–	30	–	ns	1
t_H	Clock Enable Hold Time (IDT7213 only)	3	–	3	–	2	–	0	–	ns	1
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML(1) (IDT7212 only)	0	–	0	–	0	–	0	–	ns	1

NOTES:
1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage with loading specified in Figure 2.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

CAPACITANCE (T_A= +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

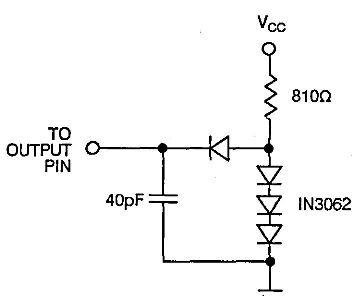


Figure 1. AC Output Test Load

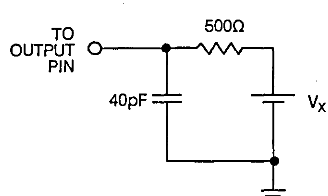
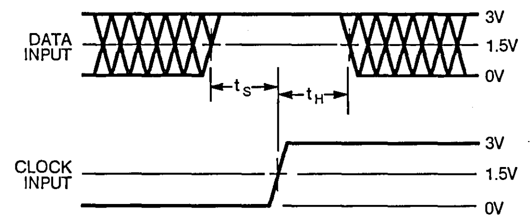


Figure 2. Output Three-State Delay Load (V_x = 0V or 2.6V)



NOTE:
Diagram shown for HIGH data only. Output transition may be opposite sense.

Figure 3. Set-Up And Hold Time

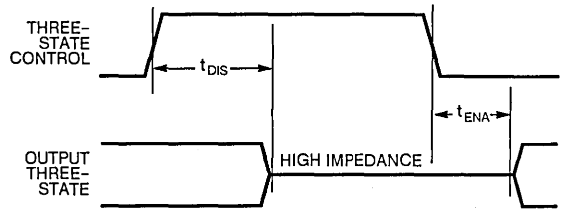


Figure 4. Three-State Control Timing Diagram

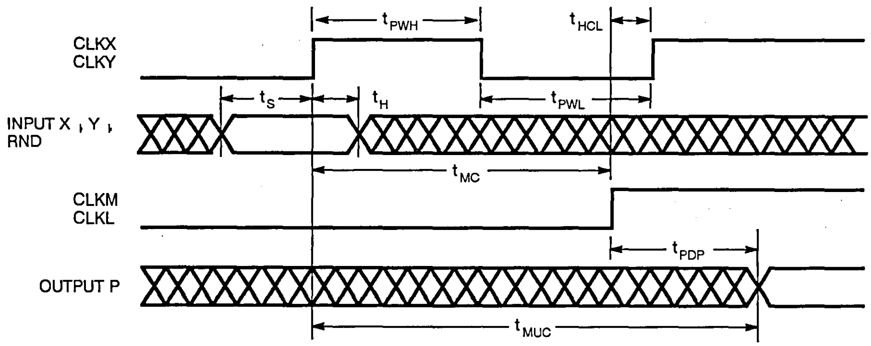


Figure 5. IDT7212 Timing Diagram

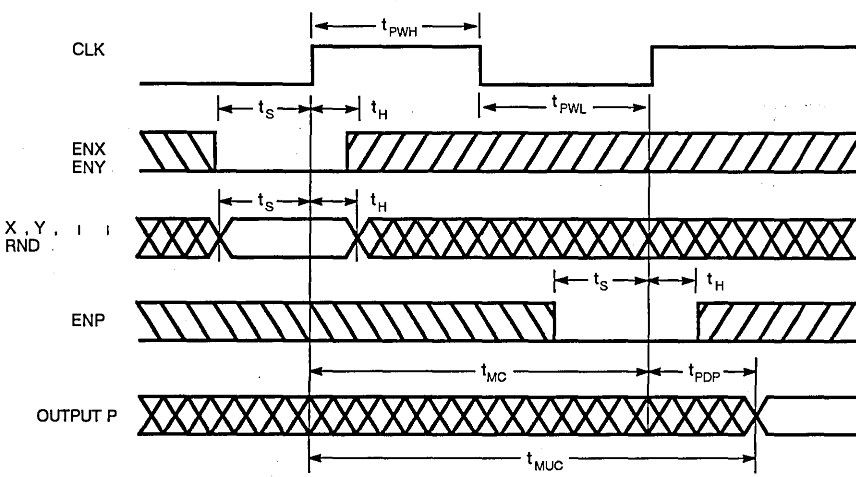


Figure 6. IDT7213 Timing Diagram

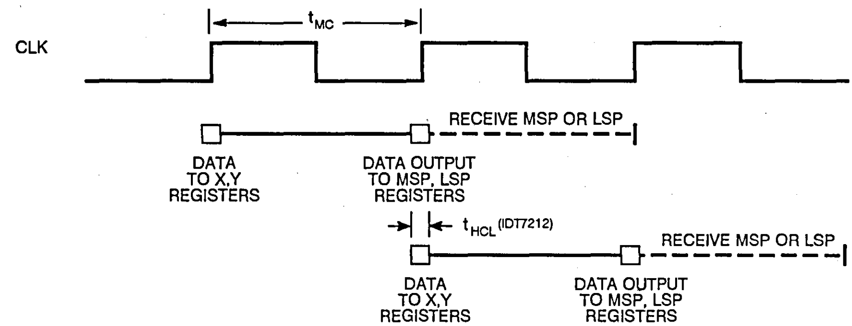


Figure 7. Simplified Timing Diagram-Typical Application

SIGNAL DESCRIPTIONS:

INPUTS:

X_{IN} (X_{11} through X_0)

Twelve Multiplicand Data Inputs

Y_{IN} (Y_{11} through Y_0)

Twelve Multiplier Data Inputs

INPUT CLOCKS (IDT7212 ONLY):

CLKX

The rising edge of this clock loads the X_{11} - X_0 data input register along with the two's complement and round registers.

CLKY

The rising edge of this clock loads the Y_{11} - Y_0 data input register along with the two's complement and round registers.

CLKM

The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKL

The rising edge of this clock loads the Least Significant Product (LSP) register.

INPUT CLOCKS (IDT7213 ONLY):

CLK

The rising edge of this clock loads all registers.

$\overline{ENX}$

Register enable for the X_{11} - X_0 data input register along with the two's complement and round registers.

$\overline{ENY}$

Register enable for the Y_{11} - Y_0 data input register along with the two's complement and round registers.

$\overline{ENP}$

Register enable the Most Significant Product (MSP) and Least Significant Product (LSP).

NOTE:
1. TRW MPY012H/K pin designation.

CONTROLS:

X_M, Y_M(TCX, TCY)[1]

Mode control inputs for each data word. A low input designates unsigned data input with a high input used for two's complement.

FA (RS)[1]

When the format adjust control is HIGH, a full 24-bit product is selected. When this control is LOW, a left-shifted 23-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional two's complement applications (see Multiplier Input/Output Formats).

FT

When this control is HIGH, both the Most Significant Product (MSP) and Least Significant Product (LSP) registers are bypassed.

$\overline{OEL}$

Three-state enable for LSP output.

$\overline{OEP}$

Three-state enable for MSP output.

RND

Round control for the rounding of the Most Significant Product (MSP). When this control is HIGH, a one is added to the Most Significant Bit (MSB) of the Least Significant Product (LSP). Note that this bit depends on the state of the Format Adjust (FA) control. If FA is LOW when RND is HIGH, a one will be added to the P_{10}. If FA is HIGH when RND is HIGH, a one will be added to the P_{11}. In either case, the LSP output will reflect this addition when RND is HIGH. Note also the rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

OUTPUTS:

MSP (P_{23} through P_{12})

Most Significant Product Output

LSP (P_{11} through P_0)

Least Significant Product Output

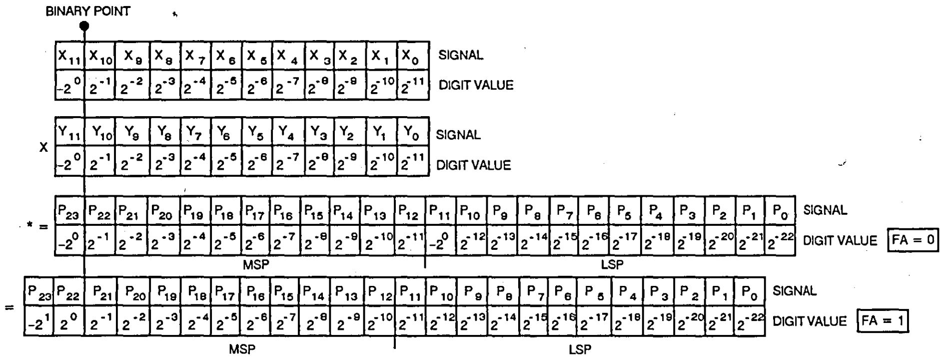


Figure 8. Fractional Two's Complement Notation

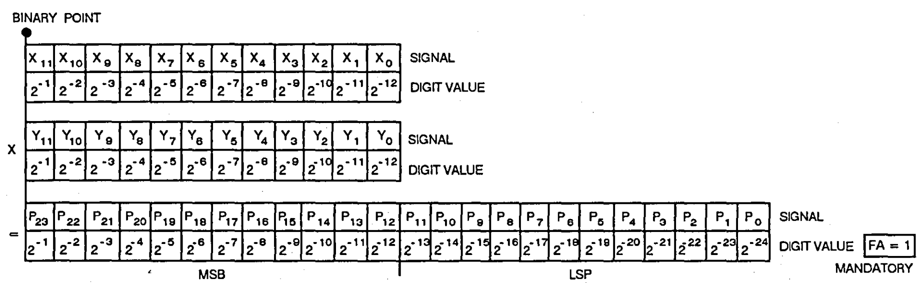


Figure 9. Fractional Unsigned Magnitude Notation

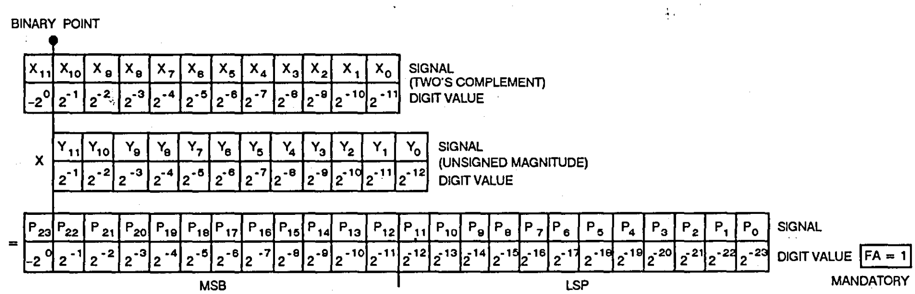


Figure 10. Fractional Mixed Mode Notation

*In this format an overflow occurs in the attempted multiplication of the two's complement number 10000 . . . 0 with 1000. . . 00 yielding an erroneous product of -1 in the fraction case and -2^{22} in the integer case.

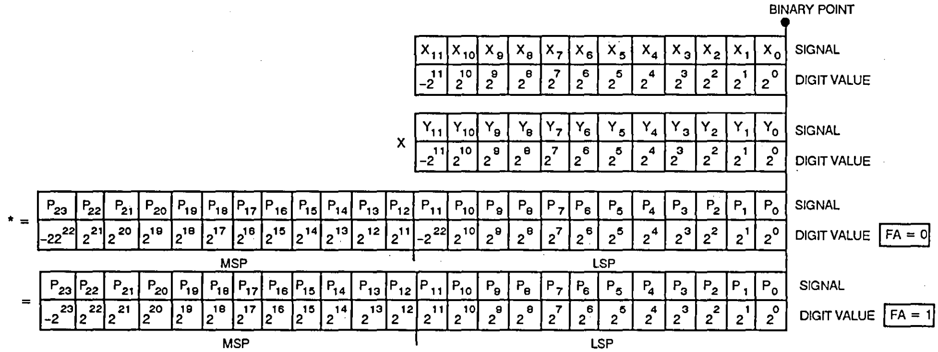


Figure 11. Integer Two's Complement Notation

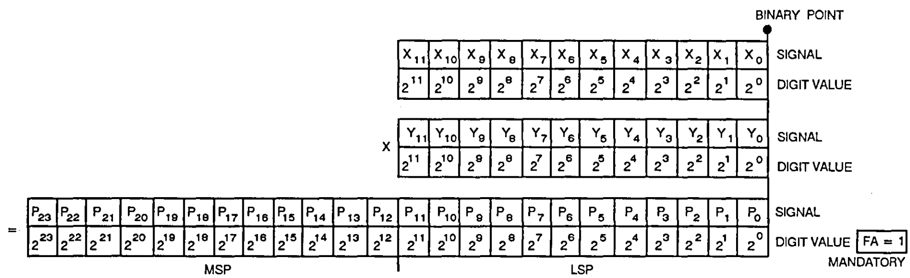


Figure 12. Integer Unsigned Magnitude Notation

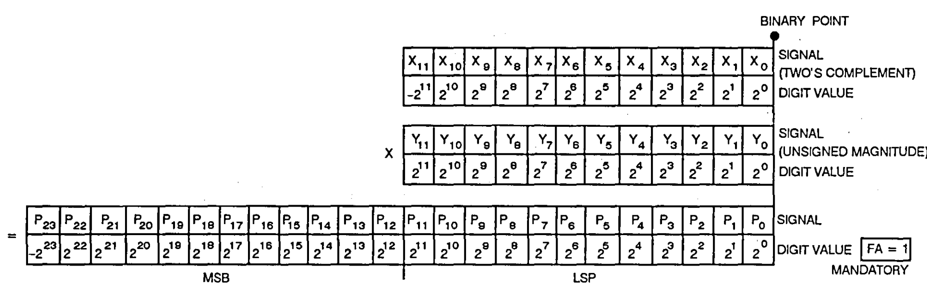


Figure 13. Integer Mixed Mode Notation

*In this format an overflow occurs in the attempted multiplication of the two's complement number 10000 . . . 0 with 1000. . . 00 yielding an erroneous product of -1 in the fraction case and -2^{22} in the integer case.

ORDERING INFORMATION

IDT XXXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range	
BLANK	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	
C	Topbraze DIP
L	Leadless Chip Carrier
Power	
L	Low Power
Device Type	
7212	12 x 12-Bit Parallel CMOS Multiplier
7213	12 x 12-Bit Parallel CMOS Multiplier with Single Clock

Speed (Speed in Nanoseconds)

COM'L.	MIL.
35	40
45	55
70	90
115	140

Integrated Device Technology, Inc.

32-BIT AND 64-BIT IEEE FLOATING-POINT MULTIPLIER AND ALU

IDT721264
IDT721265

FEATURES:

- Conforms to the requirements of IEEE Standard 754, 1985 version, for full 32-bit and 64-bit multiply and arithmetic operations
- Very high-speed operation
  - 16.7 megaflops (60ns) pipelined ALU operation (Add/Subtract/Convert/Compare)
  - 16.7 megaflops (60ns) pipelined 32-bit (single precision) multiplications
  - 8.0 megaflops (120ns) pipelined 64-bit (double precision) multiplications
- Full floating-point function arithmetic logic unit including:
  - Add
  - Subtract
  - Absolute Value
  - Compare
  - Conversion to and from two's complement integer
  - Performs 2-A to support Newton-Raphson division
- Low-power (500mW typical per device) operation
- Single 5 volt supply—no need for two supplies
- Advanced CEMOS™ technology
- Flexible system design
  - Three 32-bit ports allow two data inputs and one result output every clock cycle
  - One, two or three port architectures supported
  - Single phase, edge-triggered clock interface, with fully registered TTL-compatible inputs and outputs
- Full commercial and military ranges available
- Standard 144-pin grid array package
  - Pin and functionally compatible with Weitek 1264/1265

DESCRIPTION:

The IDT721264 floating-point multiplier and the IDT721265 floating-point ALU provide high-speed 32-bit and 64-bit floating-point processing capability.

The IDT721264/65 are fabricated using IDT's advanced CEMOS technology and are capable of a total flow-through multiply latency (time required from the input of the operand until the result can be used by another device) of 180ns for single precision and 270ns for double precision multiplications. This ultra-high-speed performance is achieved by combining both state-of-the-art CEMOS technology and advanced circuit design techniques.

For signal processing applications, where higher throughput speeds are required, operations including the function specification can be pipelined. For single precision multiplications, new operands can be loaded and a product unloaded every 60ns, while double precision multiplies can be accomplished at a 120ns rating. The IDT721265 ALU executes all operations at a 60ns pipelined throughput. All operations, including the function specification, are pipelined so there is no penalty for interleaving various functions. The on-chip pipeline is automatically advanced, using internal timers, so explicit pipeline flushing is not required.

This flexible two-chip set operates in full conformance with the requirements of IEEE standard 754, 1985 version. It performs operations on single (32-bit) and double (64-bit) precision operands, as well as conversion to 32-bit two's complement integers (IDT721265 only). The IDT721264/65 accommodates all rounding modes, infinity and reserved operand representations and the treatment of exceptions such as overflow, underflow, invalid and inexact operations. Exact conformance to the standards ensures complete software portability between prototype development and final application. A "FAST" mode eliminates the time penalty for denormalized numbers by substituting zero for a denormalized number.

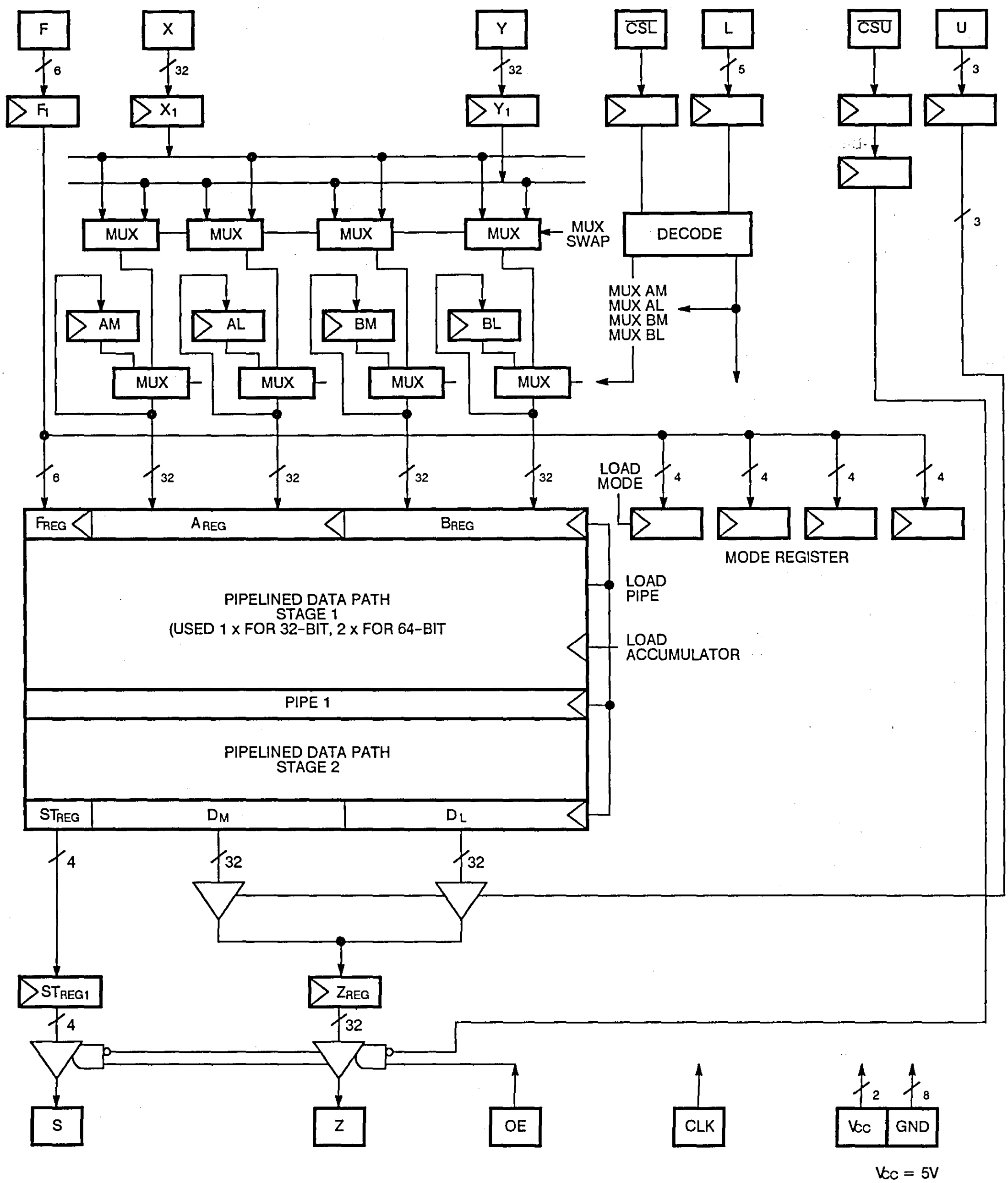
The flexible input/output architecture of these devices allows them to be used in systems with one, two or three 32-bit buses, or one 64-bit bus. Fully registered inputs and outputs, separately controlled, are loaded on each rising edge of the clock.

A 64-bit function control determines the arithmetic function to be performed while a 4-bit status output flags arithmetic exceptions and conditions. Both the function inputs and status outputs propagate along with the data to ease system design timing.

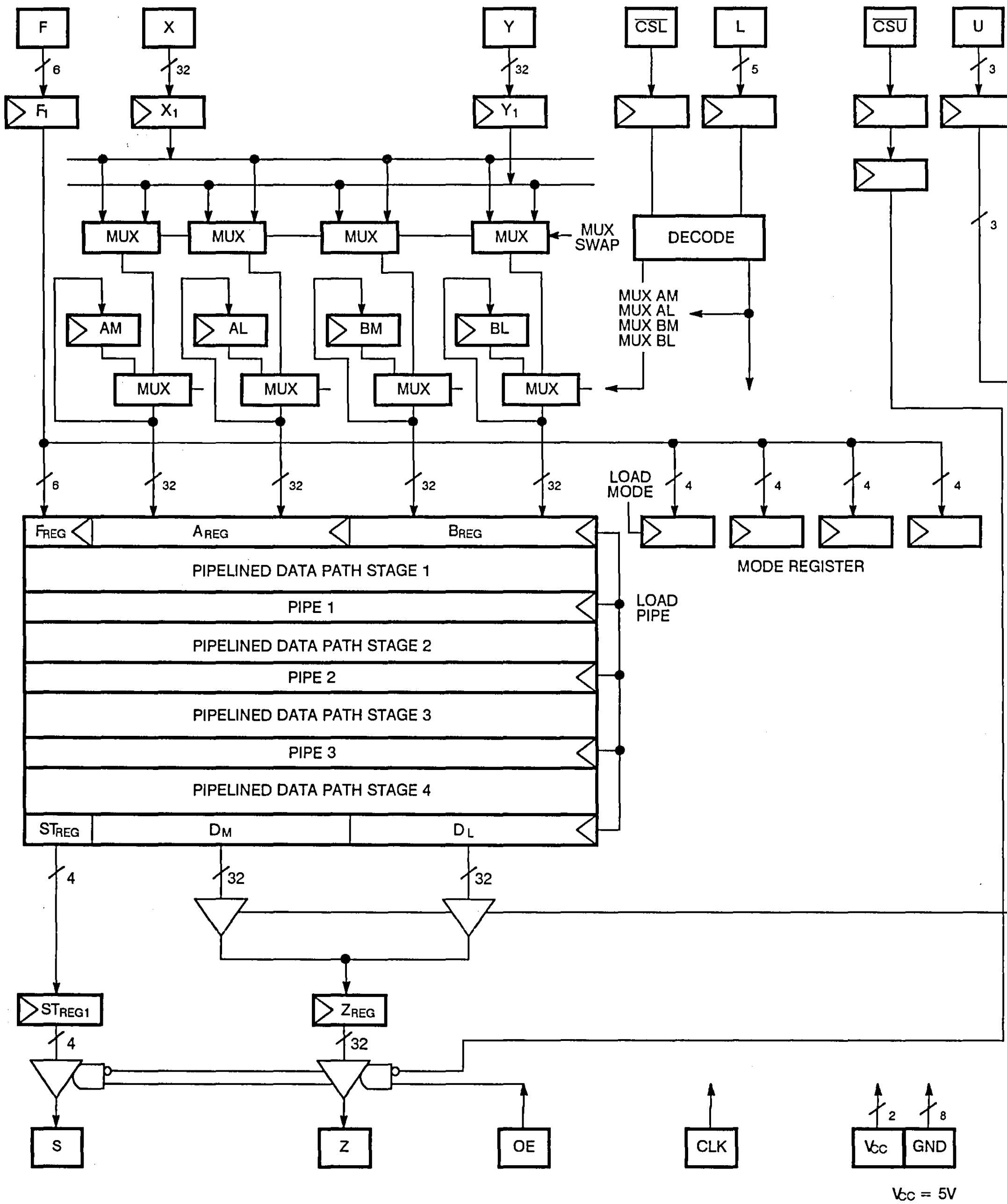
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883C, Class B.

CEMOS is a trademark of Integrated Device Technology, Inc.

FUNCTIONAL BLOCK DIAGRAM
IDT721264 FLOATING-POINT MULTIPLIER



FUNCTIONAL BLOCK DIAGRAM
IDT721265 FLOATING-POINT ALU



PIN CONFIGURATION

15	GND	Y_0	Y_{17}	Y_{18}	Y_4	Y_{21}	Y_6	Y_7	Y_{24}	Y_9	Y_{11}	Y_{12}	Y_{28}	Y_{30}	GND
14	Z_1	V_{CC}	GND	Y_{16}	Y_2	Y_{19}	Y_{20}	Y_{22}	Y_{25}	Y_{10}	Y_{27}	Y_{13}	Y_{14}	NC	X_0
13	Z_3	Z_{17}	Z_0	NC	Y_1	Y_3	Y_5	Y_{23}	Y_8	Y_{26}	Y_{29}	Y_{15}	Y_{31}	NC	X_{17}
12	Z_{19}	Z_{18}	Z_{16}										NC	X_{16}	X_{18}
11	Z_{20}	Z_4	Z_2										X_1	X_2	X_4
10	Z_{22}	Z_{21}	Z_5										X_3	X_{19}	X_{21}
9	Z_7	Z_6	Z_{23}										X_5	X_{20}	X_6
8	Z_{24}	Z_9	Z_8					G144-1					X_{23}	X_{22}	X_7
7	Z_{25}	Z_{11}	Z_{26}										X_8	X_{25}	X_{24}
6	Z_{10}	Z_{12}	Z_{28}										X_{26}	X_{10}	X_9
5	Z_{27}	Z_{29}	Z_{30}										X_{29}	X_{27}	X_{11}
4	Z_{13}	Z_{15}	NC										X_{15}	X_{13}	X_{12}
3	Z_{14}	V_{CC}	NC	NC	S_1	U_1	NC	GND	F_1	L_4	L_0	NC	X_{31}	X_{14}	X_{28}
2	Z_{31}	NC	S_2	S_0	$\overline{CSU}$	U_0	CLK	F_4	F_0	NC	L_2	NC	GND	NC	X_{30}
1	GND	S_3	GND	OE	U_2	NC	NC	F_5	F_3	F_2	NC	L_3	L_1	$\overline{CSL}$	GND
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R

PIN 1 DESIGNATOR

PIN GRID ARRAY
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL}	Input Low Voltage	–	–	0.8	V

NOTE:
1. 1.5V under shoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

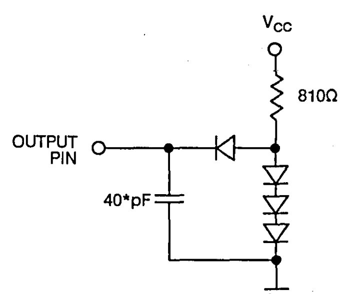
(Commercial V_{CC} = 5V ± 5%, T_A = 0°C to 70°C, Military V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL MAX.	MILITARY MIN.	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	–	10	–	20	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	10	–	20	µA
I_{CC}(1)	Operating Power Supply Current	Outputs Open, V_{CC} = Max.	–	100	–	120	mA
I_{CCQ}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq$0.2V, V_{CC} = Max.	–	5	–	5	mA
I_{CC}/f (1,2)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	–	4	–	6	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	–	2.4	–	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	–	0.4	V

NOTES:
1. I_{CC} is measured at 10MHz and V_{IN} = TTL voltages. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 100 + 4(f–10)mA, where f = operating frequency in MHz. For the military range, I_{CC} = 120 + 6(f–10) where f = operating frequency in MHz.
2. For frequencies greater than 10MHz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



*Includes scope and jig.

Figure 1. Output Load

OPERATING CONDITIONS

(Commercial V_{CC} = 5V ± 5%, T_A = 0°C to 70°C, Military V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	t_{CY} = 30ns MIN.	MAX.	t_{CY} = 40ns MIN.	MAX.	t_{CY} = 50ns MIN.	MAX.	t_{CY} = 60ns MIN.	MAX.	UNIT
t_{CY}	Clock Cycle Time	30	–	40	–	50	–	60	–	ns
t_{CH}	Clock HIGH Time	12	–	15	–	20	–	25	–	ns
t_{CL}	Clock LOW Time	12	–	15	–	20	–	25	–	ns
t_S	Input Set-up Time	11	–	13	–	15	–	15	–	ns
t_H	Input Hold Time	2	–	3	–	3	–	3	–	ns

AC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 5V ± 5%, T_A = 0°C to 70°C, Military V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	t_{CY} = 30ns MIN.	MAX.	t_{CY} = 40ns MIN.	MAX.	t_{CY} = 50ns MIN.	MAX.	t_{CY} = 60ns MIN.	MAX.	UNIT
t_{DO}	Output Delay Time	–	28	–	30	–	35	–	35	ns
t_{VO}	Output Data Valid	5	–	5	–	5	–	5	–	ns
t_{OZ}	Output Disable Time	–	25	–	30	–	35	–	35	ns
t_{ZO}	Output Enable Time	–	25	–	30	–	35	–	35	ns
t_{LA}	Total Latency Time IDT721265 ALU All Functions IDT721264 MPY 32-Bit Functions IDT721264 MPY 64-Bit Functions	 – – –	 270 180 270	 – – –	 360 240 360	 – – –	 450 300 450	 – – –	 540 360 540	 ns ns ns
t_{OP}	Pipelined Time per Stage IDT721265 ALU All Functions IDT721264 MPY 32-Bit Functions IDT721264 MPY 64-Bit Functions	 – – –	 60 60 120	 – – –	 80 80 160	 – – –	 100 100 200	 – – –	 120 120 240	 ns ns ns
t_{LAP}	Pipelined Total Latency IDT721265 ALU All Functions IDT721264 MPY 32-Bit Functions IDT721264 MPY 64-Bit Functions	 – – –	 360 210 300	 – – –	 480 280 400	 – – –	 600 350 500	 – – –	 720 420 600	 ns ns ns
Array Time (IDT721265)	A, B register to Z register, pipeline registers transparent	–	100	–	120	–	150	–	180	ns
Array Time (IDT721264)	Time to Make One Pass Through Multiplier Array for 64-Bit or 32-Bit	–	60	–	80	–	100	–	120	ns
t_{P64}	Time for a 64-Bit Result to go from the Pipeline Register to the Input Register of the Z-Reg (DM, DL Transparent)	–	90	–	120	–	150	–	180	ns
t_{P32}	Time for a 32-Bit Result to go from the Pipeline Register to the Input of the DM, DL	–	60	–	80	–	100	–	120	ns
t_{FLOW64}	Time Required for 64-Bit Data to Make One Pass Through the Array and the Transparent Pipeline Registers and Transparent DM, DL to the Input of the Z-Reg	–	120	–	160	–	200	–	240	ns
t_{FLOW32}	Time Required for 32-Bit Data to Make One Pass Through the Array and the Transparent Pipeline Registers and Transparent DM, DL to the Input of the Z-Reg	–	120	–	160	–	200	–	240	ns

7

SIGNAL DESCRIPTIONS:

INPUTS:

X_{0-31} (Input Operand)
X operand inputs, 32-bit.

Y_{0-31} (Input Operand)
Y operand inputs, 32-bit.

CONTROL:

L_{0-4} (Load Control)
The input configuration of the IDT721264 and IDT721265 can be configured through the use of the 5-bit load control to specify the destination of the data from the X and Y inputs to the AM, AL, BM, BL registers or the arithmetic array.

F_{0-5} (Function Control)
The function configuration of the IDT721264 and IDT721265 can be configured through the use of the 6-bit function control to specify the operation to be performed. See Tables 3 and 4 for the specific function controls for the multiplier and ALU.

U_{0-2} (Unload Control)
The unload control (U_{0-2}) chooses the source of the output.

$\overline{CSL}$ (Input Enable)
When $\overline{CSL}$ is low, input ports X and Y are enabled. Input data buses may be shared with the ALU and multiplier with $\overline{CSL}$.

$\overline{CSU}$ (Synchronous Output Enable)
When $\overline{CSU}$ is low, output port Z is enabled. Therefore, microcode can control the three-stating of the Z output. Since $\overline{CSL}$ is pipelined, it takes effect 2 clock cycles after it is asserted.

$\overline{OE}$ (Asynchronous Output Enable)
When $\overline{OE}$ is high, output port Z is enabled. When $\overline{OE}$ is high, the Z output is enabled if $\overline{CSU}$ is low.

CLK (Clock)
The clock input.

OUTPUTS:

Z_{0-31} (Result)
The Z result output, 32-bit, three-state.

S_{0-3} (Status)
The 4-bit status output indicates any exceptions which resulted from multiplier or ALU operations.

POWER SUPPLY:

V_{CC} (Power Supply)
Two power supply pins, 5V.

GND (Ground)
Eight ground pins, 0V.

GENERAL OPERATING MODES

Both the Multiplier and the ALU are architected identically with two input ports and one output port that surround the pipelined arithmetic array. The function control (6-bits) controls the selection of the arithmetic operations with the input and output ports controlled by a total of 8 bits of the load and unload control registers.

INPUT PORTS

The IDT721264 multiplier and the IDT721265 ALU have identical input and control structures that handle data on two 32-bit buses (X and Y). The on-chip registers (AL, AM, BL, BM) can be written from either of the buses or data can be passed from the inputs directly into the arithmetic unit.

Both devices can be used in a range of bus configurations for operations in both 32-bit and 64-bit by configuring the input data in combination with the high bandwidth output. Transfers of data input and output can be made at twice the pipeline rate. The input buses are fully registered and can be configured for one or two 32-bit inputs or one 64-bit output. These registers are loaded on each LOW-to-HIGH transition of the clock provided $\overline{CSL}$ is held LOW.

LOAD CONTROL

The Load Control (L_{0-4}) is used to transfer data from the input ports to the internal registers or the arithmetic array. L_0 controls the initiation of an operation. When this input is LOW only a data transfer occurs while, when it is held HIGH, data is transferred and an operation is begun. The sequence of events is as follows: two registers (AREG and BREG) are loaded from the specified AL, AM, BL, BM register and the X and Y ports and the FREG is loaded from port F while, on the next cycle, the specified operation in the FREG begins with the data already loaded into the AREG and BREG. The X and Y ports can be used as single operand operations and must be loaded into the AREG. The configuration of these ports can be accomplished by using the Mode bits M_{15} and M_{14} for 16-, 32- and 64-bit data. The most significant halves of the AREG and BREG must be loaded with any 32-bit operands.

UNLOAD CONTROL

The Unload Control (U_{0-2}) chooses whether the DM or DL register is sent to the Z register. The DM register stores the result of 32-bit floating-point operations. With 64-bit operations, the most significant 32 bits are stored in the DM register; the least significant half is stored in the DL register. A 32-bit result is sent from the Z register to the Z output port on each clock cycle.

TABLE 1. LOAD CONTROL TRUTH TABLE

L_4	L_3	L_2	L_1	L_0		LOAD OPERATION
0	0	0	0	0	(0)	(NOP)
0	0	0	0	1	(1)	AM, AL → AREG; BM, BL → BREG; F1 → FREG
0	0	0	1	0	(2)	Load Mode
0	0	0	1	1	(3)	– Reserved
0	0	1	0	0	(4)	Y1 → AL; X1 → BL
0	0	1	0	1	(5)	Y1 → AL; X1 → BL; AM, Y1 → AREG; BM, X1 → BREG; F1 → FREG
0	0	1	1	0	(6)	Y1 → AM; X1 → BM
0	0	1	1	1	(7)	Y1 → AM; X1 → BM; Y1, AL → AREG; X1, BL → BREG; F1 → FREG
0	1	0	0	0	(8)	X1 → BM; Y1 → BL
0	1	0	0	1	(9)	X1 → BM; Y1 → BL; AM, AL → AREG; X1, Y1 → BREG; F1 → FREG
0	1	0	1	0	(10)	X1 → AM; Y1 → AL
0	1	0	1	1	(11)	X1 → AM; Y1 → AL; X1, Y1 → AREG; BM, BL → BREG; F1 → FREG
0	1	1	0	0	(12)	X1 → AL; Y1 → BL
0	1	1	0	1	(13)	X1 → AL; Y1 → BL; AM, X1 → AREG; BM, Y1 → BREG; F1 → FREG
0	1	1	1	0	(14)	X1 → AM; Y1 → BM
0	1	1	1	1	(15)	X1 → AM; Y1 → BM; X1, AL → AREG; Y1, BL → BREG; F1 → FREG
1	0	0	0	0	(16)	Y1 → BM
1	0	0	0	1	(17)	Y1 → BM; AM, AL → AREG; Y1, BL → BREG; F1 → FREG
1	0	0	1	0	(18)	Y1 → BL
1	0	0	1	1	(19)	Y1 → BL; AM, AL → AREG; BM, Y1 → BREG; F1 → FREG
1	0	1	0	0	(20)	Y1 → AL
1	0	1	0	1	(21)	Y1 → AL; AM, Y1 → AREG; BM, BL → BREG; F1 → FREG
1	0	1	1	0	(22)	Y1 → AM
1	0	1	1	1	(23)	Y1 → AM; Y1, AL → AREG; BM, BL → BREG; F1 → FREG
1	1	0	0	0	(24)	X1 → BM
1	1	0	0	1	(25)	X1 → BM; AM, AL → AREG; X1, BL → BREG; F1 → FREG
1	1	0	1	0	(26)	X1 → BL
1	1	0	1	1	(27)	X1 → BL; AM, AL → AREG; BM, X1 → BREG; F1 → FREG
1	1	1	0	0	(28)	X1 → AL
1	1	1	0	1	(29)	X1 → AL; AM, X1 → AREG; BM, BL → BREG; F1 → FREG
1	1	1	1	0	(30)	X1 → AM
1	1	1	1	1	(31)	X1 → AM; X1, AL → AREG; BM, BL → BREG; F1 → FREG

LOAD SEQUENCES

32-BIT OPERATIONS WITH TWO 32-BIT PORTS

OPERATION	L_4	L_3	L_2	L_1	L_0	INST#
LOAD MODE [1]	0	0	0	1	0	(2)
Y1, AL → AREG; X1, BL → BREG; F1 → FREG; Y1 → AM; X1 → BM	0	0	1	1	1	(7)

NOTE:
1. If the mode does not change between operations, it does not need to be reloaded.

64-BIT OPERATIONS USING THE X AND Y PORTS AS A SINGLE 64-BIT PORT

OPERATION	L_4	L_3	L_2	L_1	L_0	INST#
LOAD MODE	0	0	0	1	0	(2)
X1 → AM; Y1 → AL	0	1	0	1	0	(10)
AM, AL → AREG; X1, Y1 → BREG; F1 → FREG; X1 → BM; Y1 → BL	0	1	0	0	1	(9)

TABLE 2. UNLOAD CONTROL TRUTH TABLE

CSU	U_2	U_1	U_0	EDGE #1	EDGE #2
0	0	0	0	$DM_{31-0} \rightarrow$ ZREG	STREG1 $\rightarrow S^+$, ZREG $\rightarrow Z^+$
0	0	1	0	DM_{31-16}, $DL_{31-16} \rightarrow$ ZREG	STREG1 $\rightarrow S^+$, ZREG $\rightarrow Z^+$
0	1	0	0	$DL_{31-0} \rightarrow$ ZREG	STREG1 $\rightarrow S^+$, ZREG $\rightarrow Z^+$
0	1	1	0	DM_{15-0}, $DL_{15-0} \rightarrow$ ZREG	STREG1 $\rightarrow S^+$, ZREG $\rightarrow Z^+$
1	X	X	X		S^+ and Z^+ Tri-Stated

TABLE 3. FUNCTION CONTROLS FOR FLOATING-POINT MULTIPLIER

F_2	F_1	F_0		OPERATION	MNEMONIC	DESCRIPTION
0	0	0	(0)	F32 x F32	MUL32	Single Multiply
0	0	1	(1)	F64 x F64	MUL64	Double Multiply
0	1	0	(2)	W32 x F32	MULAW32	Single Multiply, A Wrapped
0	1	1	(3)	W64 x F64	MULAW64	Double Multiply, A Wrapped
1	0	0	(4)	F32 x W32	MULBW32	Single Multiply, B Wrapped
1	0	1	(5)	F64 x W64	MULBW64	Double Multiply, B Wrapped
1	1	0	(6)	W32 x W32	MULABW32	Single Multiply, A & B Wrapped
1	1	1	(7)	W64 x W64	MULABW64	Double Multiply, A & B Wrapped
F_5	F_4	F_3		OPERATION	MNEMONIC	DESCRIPTION
0	0	0	(0)	A x B	MUL	Multiply
0	0	1	(1)	$\|A\|$ x B	MULABSA	B Times Magnitude of A
0	1	0	(2)	A x $\|B\|$	MULABSB	A Times Magnitude of B
0	1	1	(3)	$\|A\|$ x $\|B\|$	MULABSAB	Magnitude of A Times B
1	0	0	(4)	-(A x B)	MULNEG	Multiply and Negate
1	0	1	(5)	(-$\|A\|$) x B	MULNEGA	B Times Negative Value of A
1	1	0	(6)	A x (-$\|B\|$)	MULNEGB	A Times Negative Value of B
1	1	1	(7)	-($\|A\|$ x $\|B\|$)	MULNEGAB	Negative Value of A Times B

MULTIPLIER OPERATION: IDT721264

The IDT721264 has exception detection handling circuitry, a 56 x 28-bit multiplier array, an exponent adder circuit, a normalizing shifter and a rounding circuit for IEEE format adjustment.

The exception detection circuit is at the beginning of the multiplier. Exceptions can be Not-a-Number (NaN) or a denormalized input and timings are handled like normal numbers.

A clocked 54 x 28-bit multiplier array multiplies the mantissa portion of the floating-point number. A single precision multiply takes one pass through the array; a double precision multiply takes two passes. Each pass through the array takes two clock cycles.

Partial results are stored in the accumulator (an adder and a transparent latch). The cycle time determines the number of clock cycles required to complete a multiplication. A long cycle time requires fewer clock cycles to complete the operation. A clock time of 30ns calls for four cycles to perform a double precision multiply. In the first two clock cycles, the operands are multiplied in the array. On the second cycle, the accumulator register must be latched to retain the results. On the fourth cycle the accumulator register must be transparent so that the results are passed to the pipeline register. An accumulator timer can be set to latch or pass results one to four clock cycles after the beginning of the operation. The timer is reset at the beginning of each operation.

MULTIPLIER FUNCTION CONTROL

The multiplier controls are given in Table 3. The multiplier functions can be considered briefly in the following manner:

F_5	F_4	F_3	F_2	F_1	F_0
CS	MB	MA	WB	BA	SD

CS: 1-> Complement sign of result
MB: 1-> Magnitude of B
MA: 1-> Magnitude of A
WB: 1-> Operand B is wrapped
WA: 1-> Operand A is wrapped
SD: 0-> Single precision operation
SD: 1-> Double precision operation

The Mode Control bits are loaded from the F_{0-3} function control bits. The F_{5-4} function control bits determine which of the four 4-bit mode control subsets is loaded.

F_5	F_4	EDGE 0	EDGE 1
0	0	F → F1	F → M_{3-0}
0	1	F → F1	F → M_{7-4}
1	0	F → F1	F → M_{11-8}
1	1	F → F1	F → M_{15-12}

MULTIPLIER MODE CONTROL

IEEE OR FAST MODE

Mode bit M_0 controls the way denormalized numbers are handled. If M_0 is 0, the IEEE format is used. The multiplier generates denormalized operand exceptions and produces UNRM values on underflow exceptions. The denormalized operands are sent to the ALU to be wrapped; the wrapped numbers (WNRMs) can then be multiplied. The IEEE Compatibility section discusses this in detail.

If M_0 is 1, the Fast mode is used in order to achieve the maximum performance, by eliminating the direct handling of denormalized numbers. The multiplier flushes denormalized operands (DNRMs) to zero and rounds underflow or unnormalized results (UNRMs) to zero. Mode bit M_2 must be set to zero in the Fast mode.

M_0	DESCRIPTION
0	IEEE Mode
1	Fast Mode

ROUNDING MODE

Mode bits M_1, M_2 and M_3 select the Rounding mode. Renormalization and IEEE rounding functions are performed between the pipeline register and the DM and DL registers.

M_3	M_2	DESCRIPTION
0	0	Round to nearest value or if a tie, round to even significand
0	1	Round to zero
1	0	Round towards positive infinity
1	1	Round towards negative infinity

PIPELINE CONFIGURATION

Mode bit M_4 controls whether the DM and DL registers are transparent. Mode bit M_5 controls whether the pipeline register is transparent.

M_4	DESCRIPTION
0	Transparent DM, DL
1	Latched DM, DL

M_5	DESCRIPTION
0	Transparent pipeline register
1	Latched pipeline register

ACCUMULATOR ADVANCE CONTROL

Mode bits M_{7-6} control the timing of the partial product accumulator. The accumulator is alternately latched and made transparent every N + 1 cycles, where N is the value of M_{7-6}. The accumulator timer is reset at the beginning of each operation. The accumulator timer is used to achieve maximum throughput.

M_7	M_6	DESCRIPTION
0	0	N = 1, Clock/1
0	1	N = 2, Clock/2
1	0	N = 3, Clock/3
1	1	N = 4, Clock/4

PIPELINE ADVANCE CONTROL

Mode bits M_{11-8} control the pipeline advance control of the pipeline registers. If M_{11-8} are all zeros, the pipeline registers will only be latched at the beginning of an operation. If M_{11-8} are non-zero values, N, the pipeline registers will be clocked at the beginning of every operation and every N cycles after the beginning of every operation. The internal pipeline advance timer is reset at the beginning of every operation.

For example, if N = 4 and operations are started on cycles 0, 6 and 10, pipeline advances will occur on cycles 0, 4, 6, 10, 14, 18 and so on. The pipeline advance control is used to achieve maximum throughput.

7

M_{11}	M_{10}	M_9	M_8	DESCRIPTION
0	0	0	0	N = 0, pipeline registers are latched
0	0	0	1	N = 1, pipeline registers are clocked 1 cycle after first operation
0	0	1	0	N = 2, pipeline registers are clocked 2 cycles after first operation
0	0	1	1	N = 3, pipeline registers are clocked 3 cycles after first operation
.	.	.	.	.
.	.	.	.	.
1	1	1	1	N = 15, pipeline registers are clocked 15 cycles after first operation

BUS BANDWIDTH CONTROL

Mode bits M_{13-12} are not used. Mode bits M_{15-14} control the input bus bandwidth of the X and Y input ports. When M_{15-14} are set to zero, the X1 and Y1 registers are loaded every clock cycle from the X and Y ports.

M_{15}	M_{14}	DESCRIPTION	DATA PATH
0	0	N = 1, 32-but bus	X-> X1; Y-> Y1
0	1	N = 2, Reserved	
1	0	N = 3, Unused	
1	1	N = 4, Unused	

ALU OPERATION: IDT721265

The IDT721265 ALU has five basic components: exception detection circuitry, a shifter to normalize the smaller of the two input operands, a 57-bit adder, a shifter to renormalize the result and IEEE rounding circuitry. The IDT721265 is easily considered as an ALU with multiple internal pipeline registers. The internal pipeline registers and the DM and DL registers can be made transparent by mode bits M_{7-4}.

The pipeline registers are clocked at the beginning of each operation and every N cycles thereafter, when N is given a value by mode bits M_{11-8}.

ALU FUNCTION CONTROL

The IDT721265's function controls are shown in Table 4. The IDT superset functions are highlighted in Table 5.

The Mode Control bits are loaded from the F_{3-0} function control bits. The F_{5-4} function control bits determine which of the four 4-bit mode control subsets is loaded.

F_5	F_4	EDGE 0	EDGE 1
0	0	F → F1	F1 → M_{3-0}
0	1	F → F1	F1 → M_{7-4}
1	0	F → F1	F1 → M_{11-8}
1	1	F → F1	F1 → M_{15-12}

ALU MODE CONTROL

IEEE OR FAST MODE

Mode bit M_0 controls the way denormalized numbers are handled. If M_0 is 0, the IEEE format is used. The ALU generates denormalized operand exceptions and produces UNRM values on underflow exceptions. The IEEE Compatibility section discusses this in detail.

If M_0 is 1, the Fast mode is used in order to achieve the maximum performance by eliminating the direct handling of denormalized numbers. The ALU flushes denormalized operands (UNRMs) to zero and rounds underflow or unnormalized results (UNRMs) to zero. Mode bit M_2 must be set to zero in the Fast mode.

M_0	DESCRIPTION
0	IEEE Mode
1	Fast Mode

ROUNDING MODE

Mode bits M_1, M_2 and M_3 select the Rounding mode. Renormalization and IEEE rounding functions are performed between the pipeline register and the DM and DL registers.

M_3	M_2	M_1	DESCRIPTION
0	0	0	Round to nearest value or if a tie, round to even significand
0	1	0	Round to zero
1	0	0	Round towards positive infinity
1	1	0	Round towards negative infinity
X	X	1	Round to zero, all cases

PIPELINE CONFIGURATION

Mode bits M_{7-4} determine which of the pipeline registers and DM and DL registers are made transparent. If the mode bit is low, the corresponding register is made transparent. If the mode bit is high, the register is latched by the rising edge of the clock. If the pipeline registers are made transparent, the latency time is reduced at the expense of slower overall throughput. The highest system throughput results from enabling all the pipeline registers.

Mode bit M_4 controls whether the DM and DL registers are transparent. Mode bits M_{7-5} control which of the pipeline registers are transparent.

M_7	M_6	M_5	M_4
PIPE1	PIPE2	PIPE3	STREG, DM, DL

PIPELINE ADVANCE CONTROL

Mode bits M_{11-8} control the pipeline advance control of the pipeline registers. If M_{11-8} are all zeros, the pipeline registers will only be latched at the beginning of an operation. If M_{11-8} are non-zero values, N, the pipeline registers will be clocked at the beginning of every operation and every N cycles after the beginning of every operation. The internal pipeline advance timer is reset at the beginning of every operation.

For example, if N = 4 and operations are started on cycles 0, 6 and 10, pipeline advances will occur on cycles 0, 4, 6, 10, 14, 18 and so on. The pipeline advance control is used to achieve maximum throughput.

M_{11}	M_{10}	M_9	M_8	DESCRIPTION
0	0	0	0	N = 0, pipeline registers are latched
0	0	0	1	N = 1, pipeline registers are clocked 1 cycle after first operation
0	0	1	0	N = 2, pipeline registers are clocked 2 cycles after first operation
0	0	1	1	N = 3, pipeline registers are clocked 3 cycles after first operation
.	.	.	.	.
.	.	.	.	.
1	1	1	1	N = 15, pipeline registers are clocked 15 cycles after first operation

BUS BANDWIDTH CONTROL

Mode bits M_{13-12} are not used. Mode bits M_{15-14} control the input bus bandwidth of the X and Y input ports. When M_{15-14} are set to zero, the X1 and Y1 registers are loaded every clock cycle from the X and Y ports.

M_{15}	M_{14}	DESCRIPTION	DATA PATH
0	0	N = 1, 32-but bus	X→ X1; Y →Y1
0	1	N = 2, Reserved	
1	0	N = 3, Unused	
1	1	N = 4, Unused	

7

TABLE 4. FUNCTION CONTROLS FOR ALU – IDT721265

F_5	F_4	F_3	F_2	F_1	F_0		OPERATION	DESCRIPTION
0	0	0	0	0	0	(0)	F32 - F32	Single Subtract
0	0	0	0	0	1	(1)	F64 - F64	Double Subtract
0	0	0	0	1	0	(2)	$\lvert F32 - F32 \rvert$	Single ABS Subtract
0	0	0	0	1	1	(3)	$\lvert F64 - F64 \rvert$	Double ABS Subtract
0	0	0	1	0	0	(4)	$\lvert F32 \rvert - \lvert F32 \rvert$	Single Subtract ABS (1)
0	0	0	1	0	1	(5)	$\lvert F64 \rvert - \lvert F64 \rvert$	Double Subtract ABS (1)
0	0	0	1	1	0	(6)		RESERVED
0	0	0	1	1	1	(7)		RESERVED
0	0	1	0	0	0	(8)	-F32 + 0	Single Negate
0	0	1	0	0	1	(9)	-F64 + 0	Double Subtract
0	0	1	0	1	0	(10)	2 - F32	Single 2-A (1)
0	0	1	0	1	1	(11)	2 - F64	Double 2-A (1)
0	0	1	1	0	0	(12)	-F32 - F32	Single 2's Complement of Addition (1)
0	0	1	1	0	1	(13)	-F64 - F64	Double 2's Complement of Addition (1)
0	0	1	1	1	0	(14)		RESERVED
0	0	1	1	1	1	(15)		RESERVED
0	1	0	0	0	0	(16)	F32 + F32	Single Addition
0	1	0	0	0	1	(17)	F64 + F64	Double Addition
0	1	0	0	1	0	(18)	$\lvert F32 + F32 \rvert$	Single ABS Addition
0	1	0	0	1	1	(19)	$\lvert F64 + F64 \rvert$	Double ABS Addition
0	1	0	1	0	0	(20)	$\lvert F32 \rvert + \lvert F32 \rvert$	Single Add ABS
0	1	0	1	0	1	(21)	$\lvert F64 \rvert + \lvert F64 \rvert$	Double Add ABS
0	1	0	1	1	0	(22)		RESERVED
0	1	0	1	1	1	(23)		RESERVED
0	1	1	0	0	0	(24)	F32 + 0	Single Pass
0	1	1	0	0	1	(25)	F64 + 0	Double Pass
0	1	1	0	1	0	(26)	F32 + $\lvert F32 \rvert$	Single Mixed Addition (1)
0	1	1	0	1	1	(27)	F64 + $\lvert F64 \rvert$	Double Mixed Addition (1)
0	1	1	1	0	0	(28)	$\lvert F32 \rvert$ + 0	Single Pass ABS
0	1	1	1	0	1	(29)	$\lvert F64 \rvert$ + 0	Double Pass ABS
0	1	1	1	1	0	(30)		RESERVED
0	1	1	1	1	1	(31)		RESERVED
1	0	0	0	0	0	(32)	COMP F32 - F32	Single Compare
1	0	0	0	0	1	(33)	COMP F64 - F64	Double Compare
1	0	0	0	1	0	(34)	F32 - $\lvert F32 \rvert$	Single Mixed Subtract (1)
1	0	0	0	1	1	(35)	F64 - $\lvert F64 \rvert$	Double Mixed Subtract (1)
1	0	0	1	0	0	(36)	COMP $\lvert F32 \rvert - \lvert F32 \rvert$	Single Compare ABS
1	0	0	1	0	1	(37)	COMP $\lvert F64 \rvert - \lvert F64 \rvert$	Double Compare ABS
1	0	0	1	1	0	(38)		RESERVED
1	0	0	1	1	1	(39)		RESERVED
1	0	1	0	0	0	(40)	COMP F32 - 0	Single Compare with Zero
1	0	1	0	0	1	(41)	COMP F64 - 0	Double Compare with Zero
1	0	1	0	1	0	(42)	$-\lvert F32 \rvert + 0$	Single Negate of ABS (1)
1	0	1	0	1	0	(43)	$-\lvert F64 \rvert + 0$	Double Negate of ABS (1)
1	0	1	1	0	0	(44)	$-\lvert F32 \rvert - \lvert F32 \rvert$	Single 2's Complement of Add ABS (1)
1	0	1	1	0	1	(45)	$-\lvert F64 \rvert - \lvert F64 \rvert$	Double 2's Complement of Add ABS (1)
1	0	1	1	1	0	(46)		RESERVED
1	0	1	1	1	1	(47)		RESERVED
1	1	0	0	0	0	(48)	U32 → D32 EX	Single Unwrap Exact
1	1	0	0	0	1	(49)	U64 → D64 EX	Double Unwrap Exact
1	1	0	0	1	0	(50)	D32 → W32	Single Wrap
1	1	0	0	1	0	(51)	D64 → W64	Double Wrap
1	1	0	1	0	0	(52)	U32 → D32 INX	Single Unwrap Inexact
1	1	0	1	0	1	(53)	U64 → D64 INX	Double Unwrap Inexact
1	1	0	1	1	0	(54)		RESERVED
1	1	0	1	1	1	(55)		RESERVED
1	1	1	0	0	0	(56)	F32 → I32	Single Fix
1	1	1	0	0	1	(57)	F64 → I64	Double Fix
1	1	1	0	1	0	(58)	I32 → F32	Single Float
1	1	1	0	1	0	(59)	I64 → F64	Double Float
1	1	1	1	0	0	(60)	F32 → F64	Single Convert to Double
1	1	1	1	0	1	(61)	F64 → F32	Double Convert to Single
1	1	1	1	1	0	(62)		RESERVED
1	1	1	1	1	1	(63)		RESERVED

NOTE:
1. IDT proprietary functions. Reserved functions in Weitek-Compatible mode.

TABLE 5. IDT721265 ALU SUPERSET FUNCTION CONTROLS

F_5	F_4	F_3	F_2	F_1	F_0		OPERATION	DESCRIPTION
0	0	0	1	0	0	(4)	|F32| - |F32|	Single Subtract Absolute Value
0	0	0	1	0	1	(5)	|F64| - |F64|	Double Subtract Absolute Value
0	0	1	0	1	0	(10)	2 - F32	Single 2 - A
0	0	1	0	1	1	(11)	2 - F64	Double 2 - A
0	0	1	1	0	0	(12)	-F32 - F32	Single 2's Complement of Addition
0	0	1	1	0	1	(13)	-F64 - F64	Double 2's Complement of Addition
0	1	1	0	1	0	(26)	F32 + |F32|	Single Mixed Addition
0	1	1	0	1	1	(27)	F64 + |F64|	Double Mixed Addition
1	0	0	0	1	0	(34)	F32 - |F32|	Single Mixed Subtract
1	0	0	0	1	1	(35)	F64 - |F64|	Double Mixed Subtract
1	0	1	0	1	0	(42)	-|F32| + 0	Single Negate of Absolute Value
1	0	1	0	1	1	(43)	-|F64| + 0	Double Negate of Absolute Value
1	0	1	1	0	0	(44)	-|F32| - |F32|	Single 2's Complement of Add Absolute Value
1	0	1	1	0	1	(45)	-|F64| - |F64|	Double 2's Complement of Add Absolute Value

RESULTS STATUS

The 4-bit Result Status (S_{3-0}) indicates any exceptions or conditions of the results of a floating-point operation. Comparison conditions are shown on S_{3-0} when comparison operations are performed. Exception status is shown on S_{3-0} when exceptions occur on an operation. Table 6 details the results status indicators.

TABLE 6. STATUS TRUTH TABLE

S_3^+	S_2^+	S_1^+	S_0^+		COMPARISON CONDITION	EXCEPTION STATUS
0	0	0	0	(0)	Equal	Result = +0 or -0, exact
0	0	0	1	(1)	Less than	Result = +infinity or -infinity, exact
0	0	1	0	(2)	Greater than	Result finite and < > 0, exact
0	0	1	1	(3)		Result finite and < > 0, inexact
0	1	0	0	(4)		—Not used
0	1	0	1	(5)		Overflow & inexact
0	1	1	0	(6)		Underflow
0	1	1	1	(7)		Underflow & inexact
1	0	0	0	(8)		Operand A is denormalized
1	0	0	1	(9)		Operand B is denormalized
1	0	1	0	(10)		Operands A & B are denormalized
1	0	1	1	(11)		—Not used
1	1	0	0	(12)		Operand A is NAN
1	1	0	1	(13)		Operand B is NAN
1	1	1	0	(14)		Operands A & B are NAN
1	1	1	1	(15)	Unordered	Invalid Operation

During certain operations, more than one exception may occur. The higher priority exception will be indicated on the result status output.

PRIORITY	EXCEPTION
Highest	Operands A & B are NAN
	Operand A is NAN
	Operand B is NAN
	Invalid Operation
	Operands A & B are Denormalized
	Operand A is Denormalized
	Operand B is Denormalized
	Underflow & Inexact
	Underflow
	Overflow & Inexact
Lowest	Result is Finite < > 0, Inexact

7

TIMING

The IDT721264 and IDT721265 are designed to be able to operate as pipelined processors, to maximize systems throughput or to be able to operate as flow-through processors to minimize the latency period from input to output result. The following figures explain the various timing constraints for pipelined and flow-through modes in both single and double precision operations.

MULTIPLIER TIMINGS

64-BIT MAXIMUM PIPELINED THROUGHPUT

For maximum throughput for 64-bit multiplications, the accumulator timer should be set to clock/2 (M_{7-6} = 1), the pipeline advance control should be set to four (M_{11-8} = 4), the pipeline registers should be latched (M_5 = 1) and the DM and DL registers should be transparent (M_4 = 0). The timing is shown in Figure 3.

The first cycle after the inputs and function code are loaded, the 64-bit multiplication begins. Two cycles later, the accumulator stores the partial product of the first pass through the array. Two cycles later, the unrounded results are latched into the pipeline register. Three cycles later (t_{P64}), the result is available on the output port.

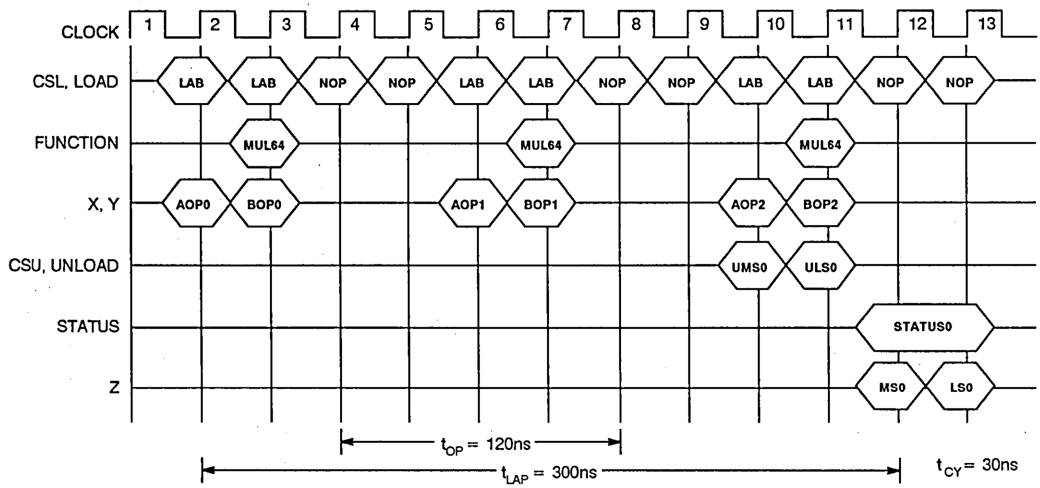


Figure 3. IDT721264 64-bit Pipelined Operation Timing

32-BIT MAXIMUM PIPELINED THROUGHPUT

For maximum throughput for 32-bit multiplications, the accumulator timer should be set to clock/1 (M_{7-6} = 0), the pipeline advance control should be set to two (M_{11-8} = 2), the pipeline registers and the DM and DL register should be latched (M_5 = M_4 = 1). The result of the multiplication will be stored on the most significant half of the DM register. The timing is shown is Figure 4.

The first cycle after the inputs and function code are loaded, the 32-bit multiplication begins. Two cycles later, the unrounded results are latched into the pipeline register. Two cycles later, the results are at the input of the DM register. One cycle later (t_{P32}), the result is available at the input of the ZREG and can be output on the following cycle.

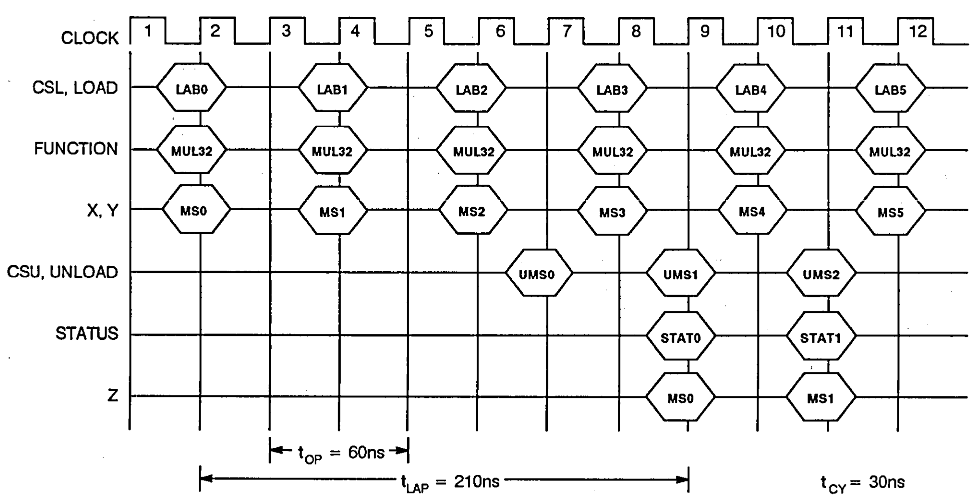


Figure 4. IDT721264 32-bit Pipelined Operation Timing

64-BIT MINIMUM LATENCY FLOW-THROUGH

For minimum latency for 64-bit multiplications, the accumulator timer should be set to clock/2 (M_{7-6} = 1), the pipeline advance control should be set to zero (M_{11-8} = 0) and the pipeline registers and DM and DL registers should be transparent (M_5 = M_4 = 0). The timing is shown is Figure 5.

The first cycle after the inputs and function code are loaded, the 64-bit multiplication begins. Two cycles later, the accumulator stores the partial product of the first pass through the array. Four cycles later (t_{FLOW64}), the result is available at the input of the ZREG and can be output on the following cycle.

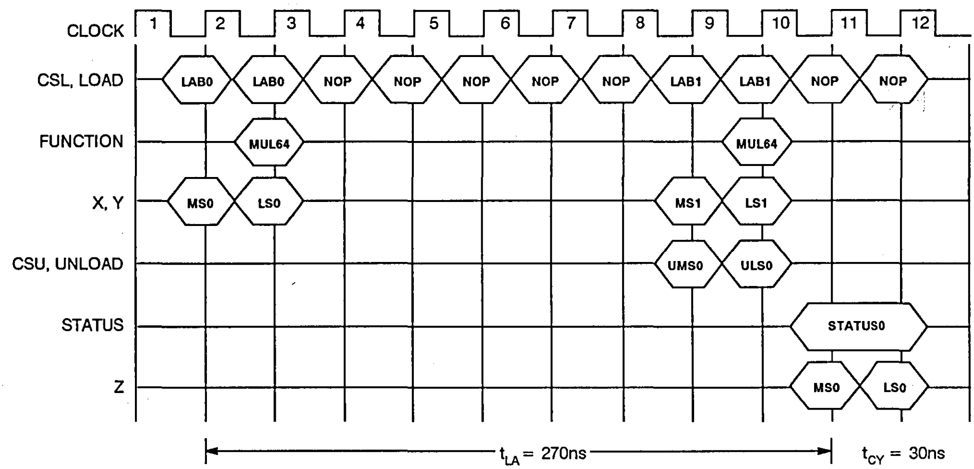


Figure 5. IDT721264 64-bit Flow-through Operation Timing

32-BIT MINIMUM LATENCY FLOW-THROUGH

For minimum latency for 32-bit multiplications, the accumulator timer should be set to clock/2 (M_{7-6} = 1), the pipeline advance control should be set to zero (M_{11-8} = 0) and the pipeline registers and DM and DL registers should be transparent (M_5 = M_4 = 0).

The result of the multiplication will be stored on the most significant half of the DM register. The timing is shown is Figure 6.

The first cycle after the inputs and function code are loaded, the 32-bit multiplication begins. Four cycles later (t_{FLOW32}), the result is available at the input of the ZREG and can be output on the following cycle.

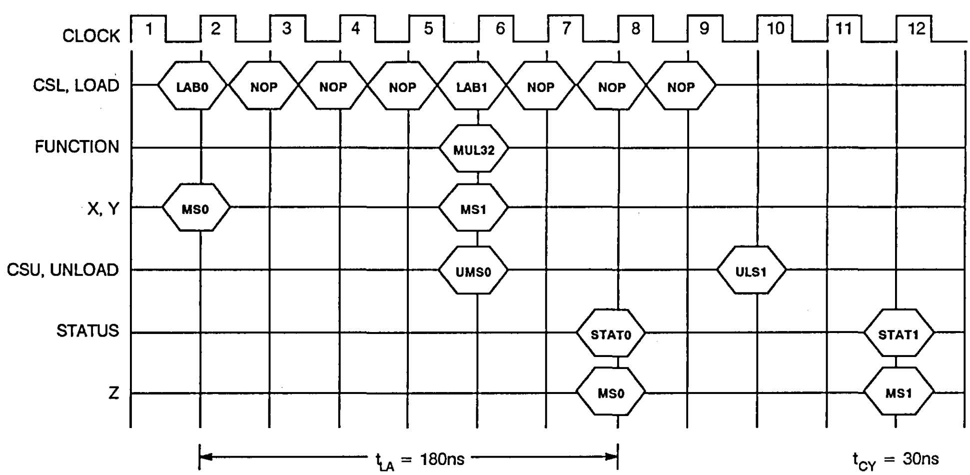


Figure 6. IDT721264 32-bit Flow-through Operation Timing

ALU TIMINGS

32-BIT AND 64-BIT MAXIMUM PIPELINED THROUGHPUT

The ALU has the same throughput for 32-bit and 64-bit operations. For maximum throughput, the pipeline advance control should be set to two ($M_{11-8} = 2$) and all pipeline registers should be enabled ($M_7 = M_6 = M_5 = M_4 = 1$). The timing is shown in Figure 7.

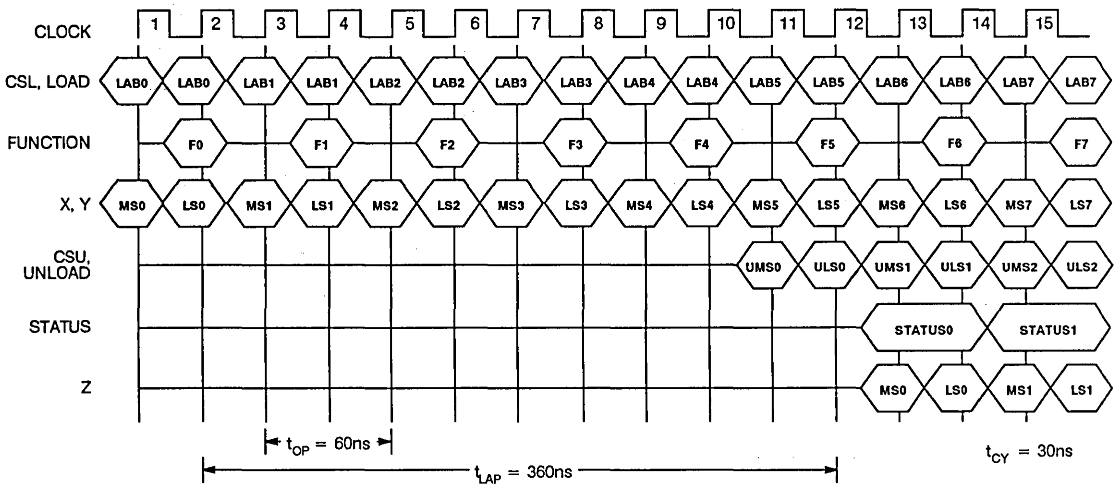


Figure 7. IDT721265 32-bit and 64-bit Pipelined Timing

32-BIT AND 64-BIT MINIMUM LATENCY FLOW-THROUGH

For minimum latency for ALU operations, the pipeline advance control should be set to zero ($M_{11-8} = 0$) and all pipeline registers should be disabled ($M_7 = M_6 = M_5 = M_4 = 0$). The timing is shown in Figure 8.

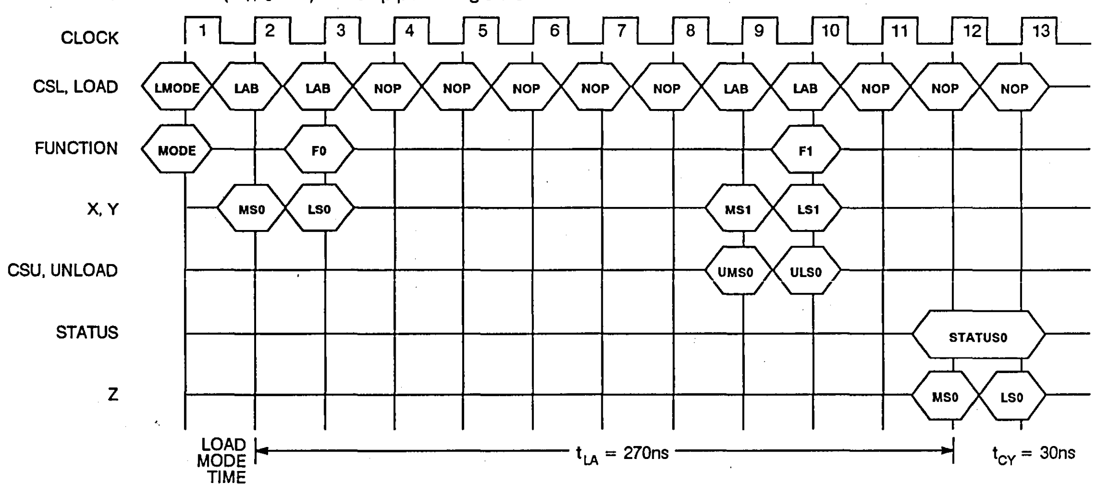
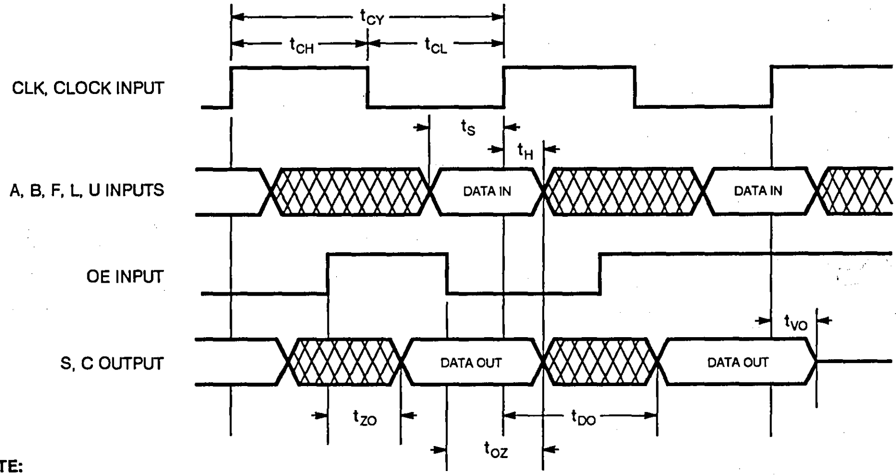


Figure 8. IDT721265 32-bit and 64-bit Flow-through Timing



NOTE:
1. CSU is LOW.

Figure 9. Input/Output Timing (1)

IEEE COMPATIBILITY

The IDT721264 and IDT721265 conform to the IEEE Standard 754, 1895 Version, which specifies floating-point processor data formats, rounding modes and exception handling. Many data formats are specified in the IEEE Standard 754: single precision, double precision, normalized numbers, denormalized numbers, wrapped numbers, zero and infinity. See Table 7. The Gradual Underflow section discusses how denormalized numbers (DNRMs) are handled.

DATA FORMATS

SINGLE PRECISION

The chip set performs 32-bit and 64-bit IEEE standard floating-point operations. The 32-bit data format has a single sign bit, a 23-bit magnitude fraction field and an 8-bit exponent field in the following format:

31	30 23	22 0
Sign bit	8-bit Exponent	23-bit Fraction

Exponents for normalized single precision numbers range from 1 to 254. Exponents of zero and 255 are reserved for special operands. The exponent bias is + 127, which means that the exponent value is e-127. The fraction value is 1.f, where 1 is the hidden bit and f is the fraction. The single precision number can be represented as $(1)^S \times 2^{e-127} \times 1.f$.

DOUBLE PRECISION

The 64-bit data format has a single sign bit, a 52-bit magnitude fraction field and an 11-bit exponent field in the following format:

63	62 52	51 0
Sign bit	11-bit Exponent	52-bit Fraction

Exponents for normalized double precision numbers range from 1 to 2046. Exponents of zero and 2047 are reserved for special operands. The exponent bias is +1023, which means that the exponent value is e-1023. The fraction value is 1.f, where 1 is the hidden bit and f is the fraction. The double precision number can be represented as $(1)^S \times 2^{e-1023} \times 1.f$.

NORMALIZED NUMBERS (NORM)

Most operations are performed on normalized numbers. In normalized single precision numbers where the exponent ranges from 1 (00000001) to 254 (11111110), the fraction is normalized and the hidden bit equals 1. This translates to a decimal number range from 10^{+38} to 10^{-38} for both positive and negative numbers and a precision of 7 decimal places.

In normalized double precision numbers where the exponent ranges from 1 to 2046, the fraction is normalized and the hidden bit equals 1. This translates to a decimal number range from 10^{+307} to 10^{-308} for both positive and negative numbers and a precision of 15 decimal places.

INFINITY

Infinity is defined as an exponent of 1 and a fraction of 0. IEEE Standard 754 defines both positive and negative infinity.

ZERO

Zero is defined as an exponent of 0, the hidden bit of 0 and a fraction of 0. IEEE Standard 754 defines both +0 and -0.

DENORMALIZED NUMBERS (DNRM)

A denormalized number is defined with an exponent of 0, the hidden bit of 0 and a non-zero fraction. Only the ALU can directly handle denormalized numbers. To multiply two denormalized numbers, the operands must first be wrapped by the ALU, then sent to the multiplier for the multiplication of two wrapped (and normalized) numbers.

WRAPPED NUMBERS (WNRM)

A wrapped number is created by normalizing a denormalized number's fraction and subtracting the number of shifts from the exponent. The fraction is shifted left until the hidden bit is 1. The exponent equals one minus the number of shifts and is in two's complement format. Only the ALU can wrap denormalized numbers and the multiplier can operate on one or two wrapped numbers.

UN-NORMALIZED NUMBERS (UNRM)

An un-normalized number results from an addition or multiplication which is smaller than the minimum representable normalized number. An un-normalized number has a wrapped exponent, a hidden bit of 1 and a normalized fraction. The smallest un-normalized number (UNRM.MIN) is the result of multiplying the two smallest denormalized numbers (DNRM.MIN).

NOT-a-NUMBER (NaN)

Not-a-Number is a special data format to flag data overflow or underflow, uninitialized operands and invalid operations (i.e., 0 x ∞). Not-a-Number has an exponent of all 1s and a non-zero fraction.

TABLE 7. IEEE SINGLE PRECISION FORMATS SUPPORTED BY THE IDT721264 AND IDT721265

OPERAND	EXPONENT	FRACTION	HIDDEN BIT	VALUE
NAN	255	ANY	N/A	NONE
INFINITY	255	ALL 0's	1	$(-1)^S \infty$
NORM.MAX	254	ALL 1's	1	$(-1)^S \times 2^{127} \times (2)$
NORM	1 to 254	ANY	1	$(-1)^S \times 2^{e-127} \times (1.f)$
NORM.MIN	1	ALL 0's	1	$(-1)^S \times 2^{-126} \times (1)$
DNRM.MAX	0	ALL 1's	0	$(-1)^S \times 2^{-126}$
DNRM	0	ANY	0	$(-1)^S \times 2^{-126} \times (0.f)$
DNRM.MIN	0	000...01	0	$(-1)^S \times 2^{-126} 2^{-23}$
WNRM.MAX	0	ALL 1's	1	$(-1)^S \times 2^{-126}$
WNRM	0 to (-22)	ANY	1	$(-1)^S \times 2^{e-127} \times (1.f)$
WNRM.MIN	-22	ALL 0's	1	$(-1)^S \times 2^{-149}$
UNRM.MAX	0	ALL 1's	1	$(-1)^S \times 2^{-126}$
UNRM. MIN	-171	ALL 0's	1	$(-1)^S \times 2^{-298}$
ZERO	0	ALL 0's	1	$(-1)^S$ 0

ROUNDING MODES

The chip set supports the four IEEE Standard 754 rounding modes: round to nearest, round toward zero, round toward plus infinity and round toward minus infinity. Biased rounding or unbiased rounding may occur. Biased rounding introduces a small offset in the direction of the bias. IEEE Standard 754 specifies positive bias, negative bias and bias toward zero. Unbiased rounding rounds toward the nearest representable number. If a number is halfway between two representable numbers, the number is rounded towards the nearest even number which averages the rounding up and down.

ROUND TO NEAREST (RN)

The result is rounded to the nearest representable number. If a number is halfway between two representable numbers, the number is rounded towards the nearest even number.

ROUND TOWARDS ZERO (RZ)

The result is rounded to the nearest representable number not greater in magnitude than the number.

ROUND TOWARD PLUS INFINITY (RP)

The result is rounded to the nearest representable number not less than the number.

ROUND TOWARD MINUS INFINITY (RM)

The result is rounded to the nearest representable number not greater than the number.

If the result of an operation is less than the minimum representable number, the underflow condition exists and is handled differently in the multiplier and ALU. In the Fast mode the underflow result is set to zero for both the multiplier and ALU. In the IEEE mode, the multiplier will not round the underflow result but will wrap it. The inexact status bit, S_0, is one if any of the truncated bits contains a one. The ALU can unwrap the result, using the "UNWRAP EXACT" or "UNWRAP INEXACT" depending on the value of S_0. The ALU status register will show whether the result is exact or inexact.

EXCEPTION HANDLING

The chip set performs exception handling according to the IEEE Standard 754. The status bits are pipelined synchronously with the operands and partial results. The status bits are stored in the STREG1 when the result is clocked into the output register until the rising edge of the next clock cycle.

The result of an ALU Compare operation is shown on the status output. A Compare result supersedes an exception status.

INEXACT (INX)

When the result of an ALU or multiplier operation losses accuracy, an Inexact status is shown. The ALU computes more that 23 fraction bits in a single precision and 53 bits in double precision. If any of the lesser significant bits equals 1, then an INX is signaled. In floating-point to fixed-point conversions, any loss of accuracy will signal INX. For normalized number operations, INX will not be signaled.

UNDERFLOW (UNF)

Underflow is asserted if a rounded result is less than the minimum normalized number. If the result is exactly zero, UNF will not be asserted.

OVERFLOW (OVF)

Overflow is asserted if a rounded result is greater than the maximum normalized number. The result is either infinity or the largest representable number and is a factor of the Round mode.

RESULT	ROUNDING MODE
+NORM.MAX (positive)	RM or RZ
-NORM.MAX (negative)	RP or RZ
+∞ (positive)	RN or RP
-∞ (negative)	RN or RM

Overflow is also asserted if the result of a floating-to-fixed operation overflows the 32-bit format.

INVALID OPERATION (INV)

The following are Invalid Operations (INV):

- One of the operands is a NaN
- 0 x ∞
- +∞ - +∞
- -∞ + +∞
- +∞ + -∞
- -∞ - -∞

OPERATIONS

The following tables represent different results obtained from different operand formats and rounding modes. Tables for both IEEE and Fast modes are shown. All results are in the "Result-Exception Status" format.

7

TABLE 8. FLOATING-POINT ADD/SUBTRACT ("FAST" MODE)

A/B	ZERO	DNRM	NRM	INF	NAN
ZERO	OK-ZERO(3)	OK-ZERO(3)	OK-NRM	OK-INF	INV-NAN
DNRM	OK-ZERO(3)	OK-ZERO(3)	OK-NRM	OK-INF	INV-NAN
NRM	OK-NRM	OK-NRM	OK-ZERO UNF-ZERO OK-NRM OK-INF(4)	OK-INF	INV-NAN
INF	OK-INF	OK-INF	OK-INF	OK-INF(1) INV-NAN(2)	INV-NAN
NAN	INV-NAN	INV-NAN	INV-NAN	INV-NAN	INV-NAN

NOTES:

1. +INF+INF → +INF
   -INF-INF → -INF
2. +INF-INF → NAN
   -INF+INF → NAN
3. +ZERO+ZERO → +ZERO (RN, RZ, RP, RM)
   -ZERO-ZERO → -ZERO (RN, RZ, RP, RM)
   +ZERO-ZERO → +ZERO (RN, RZ, RP)
   +ZERO-ZERO → -ZERO (RM)
   -ZERO+ZERO → +ZERO (RN, RZ, RP)
   -ZERO+ZERO → -ZERO (RM)
4. OVF will produce INF or MAX.NRM, depending upon the rounding mode
   +NRM.MAX if [(RM, RZ) AND (TRESULTS is +)]
   +NRM.MAX if [(RM, RZ) AND (TRESULTS is -)]
   +INF if [(RN, RP) AND (TRESULT is +)]
   -INF if [(RN, RM) AND (TRESULT is +)]

TABLE 9. FLOATING-POINT MULTIPLICATION ("FAST" MODE)

A/B	ZERO	DNRM	NRM	INF	NAN
ZERO	OK-ZERO	OK-ZERO	OK-NRM	INF-NAN	INV-NAN
DNRM	OK-ZERO	OK-ZERO	OK-NRM	OK-INF	INV-NAN
NRM	OK-ZERO	OK-ZERO	UNF-ZERO OK-NRM OK-INF(1)	OK-INF	INV-NAN
INF	INF-NAN	OK-INF	OK-INF	OK-INF INV-NAN	INV-NAN
NAN	INV-NAN	INV-NAN	INV-NAN	INV-NAN	INV-NAN

NOTES:
1. OVF will produce INF or MAX.NRM, depending upon the rounding mode
 +NRM.MAX if [(RM, RZ) AND (TRESULTS is +)]
 +NRM.MAX if [(RM, RZ) AND (TRESULTS is -)]
 +INF if [(RN, RP) AND (TRESULT is +)]
 -INF if [(RN, RM) AND (TRESULT is -)]

TABLE 10. FLOATING-POINT ADD/SUBTRACT (IEEE MODE)

A/B	ZERO	DNRM	NRM	INF	NAN
ZERO	OK-ZERO(3)	UNF-WNRM	OK-NRM	OK-INF	INV-NAN
DNRM	UNF-WNRM	UNF-WNRM OK-ZERO(3) OK-NRM	OK-NRM UNF-WNRM	OK-INF	INV-NAN
NRM	OK-NRM	UNF-WNRM OK-NRM OK-INF (4)	OK-ZERO UNF-WNRM OK-NRM OK-INF (4)	OK-INF	INV-NAN
INF	OK-INF	OK-INF	OK-INF	OK-INF(1) INV-NAN(2)	INV-NAN
NAN	INV-NAN	INV-NAN	INV-NAN	INV-NAN	INV-NAN

NOTES:
1. +INF+INF → +INF
 -INF-INF → -INF
2. +INF-INF → NAN
 -INF+INF → NAN
3. +ZERO+ZERO → +ZERO (RN, RZ, RP, RM)
 -ZERO-ZERO → -ZERO (RN, RZ, RP, RM)
 +ZERO-ZERO → +ZERO (RN, RZ, RP)
 +ZERO-ZERO → -ZERO (RM)
 -ZERO+ZERO → +ZERO (RN, RZ, RP)
 -ZERO+ZERO → -ZERO (RM)
4. OVF will produce INF or MAX.NRM, depending upon the rounding mode
 +NRM.MAX if [(RM, RZ) AND (TRESULTS is +)]
 +NRM.MAX if [(RM, RZ) AND (TRESULTS is -)]
 +INF if [(RN, RP) AND (TRESULT is +)]
 -INF if [(RN, RM) AND (TRESULT is +)]

TABLE 11. FLOATING-POINT MULTIPLICATION (IEEE MODE)

A/B	ZERO	DNRM	NRM	INF	NAN
ZERO	OK-ZERO	OK-ZERO	OK-ZERO	INF-NAN	INV-NAN
DNRM	OK-ZERO	OK-ZERO	DIN-ZERO	OK-INF	INV-NAN
NRM	OK-ZERO	OK-ZERO	UNF-ZERO OK-NRM OK-INF(1)	OK-INF	INV-NAN
INF	INF-NAN	OK-INF	OK-INF	OK-INF	INV-NAN
NAN	INV-NAN	INV-NAN	INV-NAN	INV-NAN	INV-NAN

NOTES:
1. OVF will produce INF or MAX.NRM, depending upon the rounding mode
 +NRM.MAX if [(RM, RZ) AND (TRESULTS is +)]
 +NRM.MAX if [(RM, RZ) AND (TRESULTS is -)]
 +INF if [(RN, RP) AND (TRESULT is +)]
 -INF if [(RN, RM) AND (TRESULT is +)]

TABLE 12. FLOATING-POINT COMPARE STATUS

						INPUT B					
	U	U	U	U	U	NAN	U	U	U	U	U
	U	L	L	L	L	+INF	L	L	L	E	U
	U	L	L	L	L	+NRM	L	L	Note 1	G	U
	U	L	L	L	L	+DNRM	L	Note 1	G	G	U
	U	L	L	L	E	+ZERO	E	G	G	G	U
INPUT A	NAN	-INF	-NRM	-DNRM	-ZERO		+ZERO	+DNRM	+NRM	+INF	NAN
	U	L	L	L	E	-ZERO	E	G	G	G	U
	U	L	L	Note 1	G	-DNRM	G	G	G	G	U
	U	L	Note 1	G	G	-NRM	G	G	G	G	U
	U	E	G	G	G	-INF	G	G	G	G	U
	U	U	U	U	U	NAN	U	U	U	U	U

NOTE:
1. Equal, less than or greater than
   E–A = B
   L–A < B
   G–A > B
   U–Unordered

TABLE 13. CONVERT SINGLE TO DOUBLE

F32 → F64					
F32 OPERAND		F64 RESULT		STATUS	COMMENTS
077777	177777	077777 177777	177777 177777	12	NaN
077600	000000	077760 000000	000000 000000	1	+INF
077577	000000	043757 160000	177777 000000	2	+MAX.NRM
037600	000000	037760 000000	000000 000000	2	+1
000200	000000	034020 000000	000000 000000	2	+MIN.NRM
000177	177777	033757 140000	177777 000000	2	+MAX.DNRM
000000	000001	033240 000000	000000 000000	2	+MIN.DNRM
000000	000000	000000 000000	000000 000000	0	+ZERO
177600	000000	177760 000000	000000 000000	1	-INF
177577	177777	143757 160000	177777 000000	2	-MAX.NRM
140000	000000	140000 000000	000000 000000	2	-2
100200	000000	134020 000000	000000 000000	2	-MIN.NRM
100177	177777	133757 140000	177777 000000	2	-MAX.DNRM
100000	000001	133200 000000	000000 000000	2	-MIN.DNRM
100000	000000	100000 000000	000000 000000	0	-ZERO

TABLE 14. CONVERT DOUBLE TO SINGLE (1)

F64 → F32					
F64 OPERAND		F32 RESULT		STATUS	COMMENTS
077777 177777	177777 177777	077777	177777	12	NaN
077760 000000	000000 000000	077600	000000	1	+INF
077757 000000	177777 000000	077600	000000	5	+MAX.NRM OPERAND
043757 170000	177777 000000	077600	000000	5	+OVF RESULT
043757 160000	177777 000000	077577	177777	2	+MAX.NRM RESULT
043757 177777	177777 177777	077400	000000	3	+INEXACT
037760 000000	000000 000000	037600	000000	2	+1
034020 000000	000000 000000	000200	000000	2	+MIN.NRM RESULT
034017 160005	177777 000000	000200	000000	3	+MIN.NRM RESULT
033757 140000	177777 000000	000177	177777	6	+MAX.DNRM RESULT
033240 000000	000000 000000	000000	000001	6	+MIN.DNRM RESULT
033230 000000	000000 000000	000000	000001	7	+MIN.DNRM RESULT
033220 000000	000000 000000	000000	000000	7	+ZERO RESULT
000020 000000	000000 000000	000000	000000	7	+MIN.NRM OPERAND
000017 177777	177777 177777	000000	000000	7	+MAX.DNRM OPERAND
000000 000000	000000 000000	000000	000000	0	+ZERO
177760 000000	000000 000000	177600	000000	1	-INF
177757 177777	177777 177777	177600	000000	5	-MAX.NRM OPERAND
100000 000000	000000 000000	100000	000000	0	-ZERO

NOTE:
1. Round Mode = RN

TABLE 15. DOUBLE FLOAT

I32 → F64					
I32 OPERAND		F64 RESULT		STATUS	COMMENTS
077777	177777	040737 177700	177777 000000	2	+MAX OPERAND
077777	177776	040737 177600	177777 000000	2	–
000000	000002	040000 000000	000000 000000	2	+2
000000	000001	037760 000000	000000 000000	2	+1
000000	000000	000000 000000	000000 000000	0	ZERO
177777	177777	137760 000000	000000 000000	2	-1
177777	177776	140000 000000	000000 000000	2	-2
100000	000002	140737 177600	177777 000000	2	–
100000	000001	140737 177700	177777 000000	2	–
100000	000000	140740 000000	000000 000000	2	-MAX OPERAND

TABLE 16. SINGLE FLOAT [1]

I32 → F32					
I32 OPERAND		F32 RESULT		STATUS	COMMENTS
077777	177777	047400	000000	3	+MAX OPERAND
077777	177700	047400	000000	3	–
077777	177600	047377	177777	2	–
000000	000002	040000	000000	2	+2
000000	000001	037600	000000	2	+1
000000	000000	000000	000000	0	ZERO
177777	177777	137600	000000	2	-1
177777	177776	140000	000000	2	-2
100000	000000	147400	000000	2	-MAX OPERAND

NOTE:
1. Round Mode = RN

TABLE 17. DOUBLE FIX [1]

F64 → I32					
F64 OPERAND		I32 RESULT		STATUS	COMMENTS
077777 177777	177777 177777	077777	177777	12	NAN
077760 000000	000000 000000	077777	177777	5	+INF
077757 177777	177777 177777	077777	177777	5	+MAX.NRM OPERAND
040737 177740	177777 000000	077777	177777	5	+OVF
040737 177700	177777 000000	077777	177777	2	+MAX RESULT
040000 000000	000000 000000	000000	000002	2	+2
377760 000000	000000 000000	000000	000001	2	+1
037750 000000	000000 000000	000000	000001	3	+1
037740 000000	000000 000000	000000	000000	3	ZERO
000020 000000	000000 000000	000000	000000	3	+MIN.NRM
000000 000000	000000 000001	000000	000000	3	+MIN.NRM
000000 000000	000000 000000	000000	000000	0	+ZERO
177760 000000	000000 000000	100000	000000	5	-INF
177757 177777	177777 000000	100000	000000	5	-MAX.NRM OPERAND
140740 000100	000000 000000	100000	000000	5	-OVF
140740 000000	000000 000000	100000	000000	2	-MAX RESULT
140000 000000	000000 000000	177777	177776	2	-2
137760 000000	000000 000000	177777	177777	2	-1
137750 000000	000000 000000	177777	177777	3	-1
137740 000000	000000 000000	000000	000000	3	ZERO
100200 000000	000000 000000	000000	000000	3	-MIN.NRM
100000 000000	000000 000001	000000	000000	3	-MIN.DNRM
100000 000000	000000 000000	000000	000000	0	-ZERO

NOTE:
1. Round Mode = RN

TABLE 18. SINGLE FIX (1)

F32 → I32					
F32 OPERAND		I32 RESULT		STATUS	COMMENTS
077777	177777	077777	177777	12	NAN
077600	000000	077777	177777	5	+INF
077577	177777	077777	177777	5	+MAX.NRM
047400	000000	077777	177777	5	+OVF
047377	177777	077777	177600	2	+MAX RESULT
040000	000000	000000	000002	2	+2
037600	000000	000000	000001	2	+1
037500	000000	000000	000001	3	+1
000200	000000	000000	000000	3	+MIN.NRM
000000	000001	000000	000000	3	+MIN.DNRM
000000	000000	000000	000000	2	+ZERO
177600	000000	100000	000000	5	-INF
177577	177777	100000	000000	5	-MAX.NRM
147400	000001	100000	000000	5	-OVF
147400	000000	100000	000000	2	-MAX RESULT
140000	000000	177777	177776	2	-2
137600	000000	177777	177777	2	-1
137500	000000	177777	177777	3	-1
137400	000000	000000	000000	3	-ZERO
100200	000000	000000	000000	3	-MIN.NRM
100000	000001	000000	000000	3	-MIN.DNRM
100000	000000	000000	000000	0	-ZERO

NOTE:
1. Round Mode = RN

TABLE 19. DOUBLE WRAP DENORMALIZED VALUE

D64 → W64					
D64 OPERAND		W64 RESULT		STATUS	COMMENTS
000000 000000	000000 000001	076320 000000	000000 000000	2	+MIN.DNRM
000010 000000	000000 000000	000000 000000	000000 000000	2	–
000017 177777	177777 177777	000017 177777	177777 177776	2	+MAX.DNRM

TABLE 20. SINGLE WRAP DENORMALIZED VALUE

D32 → W32					
D32 OPERAND		W32 RESULT		STATUS	COMMENTS
100000	000001	172400	000000	2	-MIN.DNRM
100100	000000	100000	000000	2	–
100177	177777	100177	177776	2	-MAX.DNRM

TABLE 21. DOUBLE UNWRAP EXACT VALUE (1)

U64 → D64					
U64 OPERAND		D64 RESULT		STATUS	COMMENTS
000017 177777	177777 177777	000020 000000	000000 000000	3	+MIN.NRM RESULT
000000 000000	000000 000000	000010 000000	000000 000000	6	+UNF
077777 177777	177777 177777	000010 000000	000000 000000	7	–
076320 000000	000000 000000	000000 000000	000000 000001	6	+MIN.DNRM RESULT
076317 177777	177777 177777	000000 000000	000000 000001	7	–

NOTE:
1. Round Mode = RN

TABLE 22. SINGLE UNWRAP EXACT VALUE (1)

U32 → D32					
U32 OPERAND		D32 RESULT		STATUS	COMMENTS
100177	177777	100200	000000	3	–
100000	000000	100100	000000	6	–
177777	177777	100100	000000	7	–
172400	000000	100000	000001	6	–
172577	177777	100000	000002	7	–

NOTE:
1. Round Mode = RN

7

GRADUAL UNDERFLOW

The minimum normalized number has an exponent of one and a fraction field of zero. Zero has an exponent of zero and a fraction field of all zeros. This gives users the ability to deal with numbers between NORM.MIN and ZERO. These numbers are known as denormals. Their format is given in the number format section. The IEEE standard has specified gradual underflow as the way to handle denormals. Many of the features of the IDT721264 and IDT721265 are included to deal with denormals in a manner consistent with IEEE Standard 754. Since denormals are very close to zero, many applications can substitute zero for a denormal without a significant loss of accuracy. For these applications, a "FAST" mode is included which substitutes zero for all denormalized inputs to the IDT721264 and IDT721265. Zero is also inserted for all UNRM outputs in "FAST" mode.

For all arithmetic operations, the IDT721265 handles denormalized inputs directly as it would handle and other number.

Unfortunately, a floating-point multiplier must either operate exclusively on normalized numbers or suffer large cost and performance penalties in dealing directly with denormals. A normalized format that yields an equivalent to a given denormalized number is the wrapped format. The number format table shows the equivalence of wrapped and denormalized numbers. To translate a denormalized number to a wrapped number, the fraction is normalized (shifted up so that a one is in the hidden bit) and one is subtracted from the exponent for every position shifted. The IDT721264 can multiply correctly either two wrapped numbers or a wrapped and a normalized number. To understand the full procedure, consider the following case.

Assume one of the two input operands to the IDT721264 is a denormalized number. Four cycles after the input, the denorm exception is flagged. The denormalized operand must then be sent to the IDT721265 to be wrapped. Once wrapped, the operand can be sent back to the IDT721264 for multiplication. The result o the multiplication will either be a normalized number or a UNRM.

If the result is a UNRM, status bit S_0 indicates either UNF (if all the truncated bits are equal to zero) or UNF-INX (if any of the truncated bits is equal to one).

No rounding will occur regardless of the rounding mode specified.

The underflowed number may then be sent to the IDT721265 for "unwrapping". To unwrap a number, the fraction field is shifted right and the exponent incremented by one for each shift position. Status bit S_0 must be used to conditionally execute the "UNWRAP INEXACT" or "UNWRAP EXACT" instruction. The rounding must be performed in the ALU. The unwrapping may have three possible results:

RESULT	EXCEPTION	COMMENT
DNRM	UNF	When the denormalized result is exact. Note that this result is possible only if the UNWRAP EXACT instruction is possible (i.e., both the input and the result must be exact).
DNRM	UNF-INX	If either the "UNWRAP INEXACT" instruction is executed or if the result of the "UNWRAP INEXACT" instruction is inexact.
ZERO	INX	The result is zero, but the unwrapping has resulted in the loss of precision.

ORDERING INFORMATION

IDT XXXXXX– (Device Type) A (Power) 99 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range:
- BLANK — Commercial (0°C to +70°C
- B — Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:
- G — Pin Grid Array

Speed:
- 30 — (Commercial only)
- 40
- 50 — Clock Cycle Time (ns)
- 60

Power:
- L — Low Power

Device Type:
- 721264 — 32-/64-Bit Floating-Point Multiplier
- 721265 — 32-/64-Bit Floating-Point ALU

Integrated Device Technology, Inc.

16 x 16-BIT PARALLEL CMOS MULTIPLIERS

IDT7216L
IDT7217L

FEATURES:

- 16 x 16 parallel multiplier with double precision product
- 20ns clocked multiply time
- Low power consumption: 120mA
- Produced with advanced submicron CEMOS™ high-performance technology
- IDT7216L is pin- and functionally-compatible with TRW MPY016H/K and AMD Am29516
- IDT7217L requires only single clock with register enables making it pin- and functionally-compatible with AMD Am29517
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Single 5V power supply
- Input and output directly TTL- compatible
- Three-state output
- Available in plastic DIP, Shrink-DIP, Fine-Pitch LCC, LCC, PLCC, Flatpack and Pin Grid Array
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87531 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT7216/IDT7217 are high-speed, low-power 16 x 16-bit multipliers ideal for fast, real time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, submicron CEMOS technology, has achieved speeds comparable to bipolar (20ns max.), at 1/10th the power consumption.

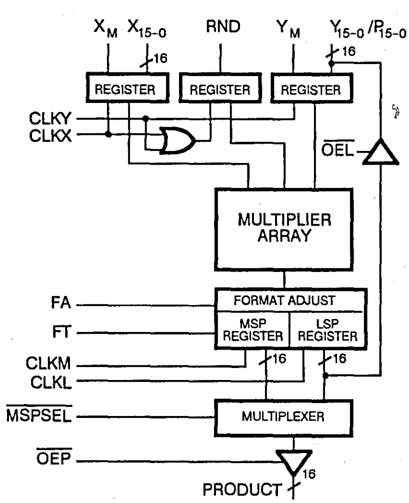
The IDT7216/IDT7217 are ideal for applications requiring high-speed multiplication such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition and in any system requirement where multiplication speeds of a mini/microcomputer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge-triggered D-type flip-flop. In the IDT7216, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The IDT7217 has only a single clock input (CLK) and three register enables. $\overline{ENX}$ and $\overline{ENY}$ control the two input registers, while $\overline{ENP}$ controls the entire product.

The IDT7216/IDT7217 offer additional flexibility with the FA control and $\overline{MSPSEL}$ functions. The FA control formats the output for two's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. The $\overline{MSPSEL}$ low selects the MSP to be available at the product output port, while a high selects the LSP to be available. Keeping this pin low will ensure compatibility with the TRW MPY016H.

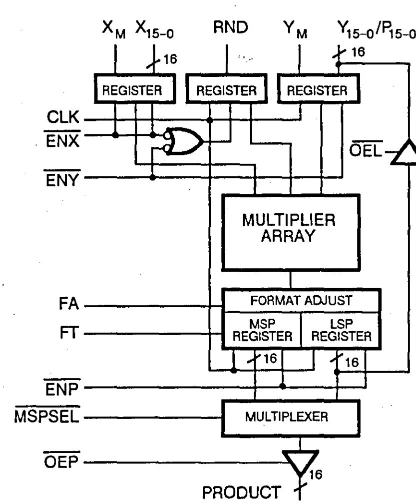
The IDT7216/IDT7217 multipliers are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAMS



MSP $_{OUT}$ (P_{31} – P_{16})

IDT7216



MSP $_{OUT}$ (P_{31} – P_{16})

IDT7217

CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-2023/-

PIN CONFIGURATIONS

IDT7216

P64-1 & C64-1

Pin	Signal	Pin	Signal
1	X_4	64	X_5
2	X_3	63	X_6
3	X_2	62	X_7
4	X_1	61	X_8
5	X_0	60	X_9
6	$\overline{OEL}$	59	X_{10}
7	CLKL	58	X_{11}
8	CLKY	57	X_{12}
9	P_0, Y_0	56	X_{13}
10	P_1, Y_1	55	X_{14}
11	P_2, Y_2	54	X_{15}
12	P_3, Y_3	53	CLKX
13	P_4, Y_4	52	RND
14	P_5, Y_5	51	X_M
15	P_6, Y_6	50	Y_M
16	P_7, Y_7	49	V_{CC}
17	P_8, Y_8	48	V_{CC}
18	P_9, Y_9	47	GND
19	P_{10}, Y_{10}	46	GND
20	P_{11}, Y_{11}	45	$\overline{MSPSEL}$
21	P_{12}, Y_{12}	44	FT
22	P_{13}, Y_{13}	43	FA
23	P_{14}, Y_{14}	42	$\overline{OEP}$
24	P_{15}, Y_{15}	41	CLKM
25	P_0, P_{16}	40	P_{15}, P_{31}
26	P_1, P_{17}	39	P_{14}, P_{30}
27	P_2, P_{18}	38	P_{13}, P_{29}
28	P_3, P_{19}	37	P_{12}, P_{28}
29	P_4, P_{20}	36	P_{11}, P_{27}
30	P_5, P_{21}	35	P_{10}, P_{26}
31	P_6, P_{22}	34	P_9, P_{25}
32	P_7, P_{23}	33	P_8, P_{24}

64-PIN DIP TOP VIEW

IDT7217

P64-1 & C64-1

Pin	Signal	Pin	Signal
1	X_4	64	X_5
2	X_3	63	X_6
3	X_2	62	X_7
4	X_1	61	X_8
5	X_0	60	X_9
6	$\overline{OEL}$	59	X_{10}
7	CLK	58	X_{11}
8	$\overline{ENY}$	57	X_{12}
9	P_0, Y_0	56	X_{13}
10	P_1, Y_1	55	X_{14}
11	P_2, Y_2	54	X_{15}
12	P_3, Y_3	53	$\overline{ENX}$
13	P_4, Y_4	52	RND
14	P_5, Y_5	51	X_M
15	P_6, Y_6	50	Y_M
16	P_7, Y_7	49	V_{CC}
17	P_8, Y_8	48	V_{CC}
18	P_9, Y_9	47	GND
19	P_{10}, Y_{10}	46	GND
20	P_{11}, Y_{11}	45	$\overline{MSPSEL}$
21	P_{12}, Y_{12}	44	FT
22	P_{13}, Y_{13}	43	FA
23	P_{14}, Y_{14}	42	$\overline{OEP}$
24	P_{15}, Y_{15}	41	$\overline{ENP}$
25	P_0, P_{16}	40	P_{15}, P_{31}
26	P_1, P_{17}	39	P_{14}, P_{30}
27	P_2, P_{18}	38	P_{13}, P_{29}
28	P_3, P_{19}	37	P_{12}, P_{28}
29	P_4, P_{20}	36	P_{11}, P_{27}
30	P_5, P_{21}	35	P_{10}, P_{26}
31	P_6, P_{22}	34	P_9, P_{25}
32	P_7, P_{23}	33	P_8, P_{24}

64-PIN DIP TOP VIEW

IDT7216/IDT7217

C68-1

Pin	Signal	Pin	Signal
1	X_5	68	X_4
2	X_6	67	X_3
3	X_7	66	X_2
4	X_8	65	X_1
5	X_9	64	X_0
6	X_{10}	63	$\overline{OEL}$
7	X_{11}	62	CLKL/(CLK)*
8	X_{12}	61	CLKY/($\overline{ENY}$)*
9	N/C	60	N/C
10	X_{13}	59	P_0, Y_0
11	X_{14}	58	P_1, Y_1
12	X_{15}	57	P_2, Y_2
13	*($\overline{ENX}$)/CLKX	56	P_3, Y_3
14	RND	55	P_4, Y_4
15	X_M	54	P_5, Y_5
16	Y_M	53	P_6, Y_6
17	V_{CC}	52	P_7, Y_7
18	V_{CC}	51	P_8, Y_8
19	GND	50	P_9, Y_9
20	GND	49	P_{10}, Y_{10}
21	GND	48	P_{11}, Y_{11}
22	$\overline{MSPSEL}$	47	P_{12}, Y_{12}
23	FT	46	P_{13}, Y_{13}
24	FA	45	P_{14}, Y_{14}
25	$\overline{OEP}$	44	P_{15}, Y_{15}
26	*($\overline{ENP}$)/CLKM	43	P_0, P_{16}
27	N/C	42	P_1, P_{17}
28	P_{15}, P_{31}	41	P_2, P_{18}
29	P_{14}, P_{30}	40	P_3, P_{19}
30	P_{13}, P_{29}	39	P_4, P_{20}
31	P_{12}, P_{28}	38	P_5, P_{21}
32	P_{11}, P_{27}	37	P_6, P_{22}
33	P_{10}, P_{26}	36	P_7, P_{23}
34	P_9, P_{25}	35	P_8, P_{24}

68-PIN SHRINK-DIP TOP VIEW

* (IDT7217 Pin Designation)

PIN CONFIGURATIONS (CONTINUED)

IDT7216/IDT7217

	A	B	C	D	E	F	G	H	J	K	L
11		NC	X_{13}	X_{15}	RND	Y_M	V_{CC}	GND	FT	$\overline{OEP}$	
10	X_{11}	X_{12}	X_{14}	CLKX or $\overline{ENX}$*	X_M	V_{CC}	GND	$\overline{MSPSEL}$	FA	CLKM or $\overline{ENP}$*	NC
09	X_9	X_{10}								P_{30}, P_{14}	P_{31}, P_{15}
08	X_7	X_8								P_{28}, P_{12}	P_{29}, P_{13}
07	X_5	X_6								P_{26}, P_{10}	P_{27}, P_{11}
06	X_3	X_4				G68-2				P_{24}, P_8	P_{25}, P_9
05	X_1	X_2								P_{22}, P_6	P_{23}, P_7
04	$\overline{OEL}$	X_0								P_{20}, P_4	P_{21}, P_5
03	CLKY or $\overline{ENY}$*	CLKL or CLK*								P_{18}, P_2	P_{19}, P_3
02	NC	Y_0, P_0	Y_2, P_2	Y_4, P_4	Y_6, P_6	Y_8, P_8	Y_{10}, P_{10}	Y_{12}, P_{12}	Y_{14}, P_{14}	P_{16}, P_0	P_{17}, P_1
01	●	Y_1, P_1	Y_3, P_3	Y_5, P_5	Y_7, P_7	Y_9, P_9	Y_{11}, P_{11}	Y_{13}, P_{13}	Y_{15}, P_{15}	NC	

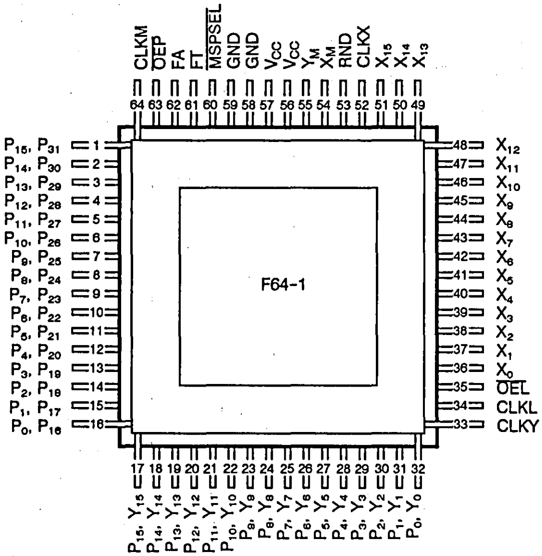
Pin 1 Designator

*Pin designation for IDT7217

PGA TOP VIEW

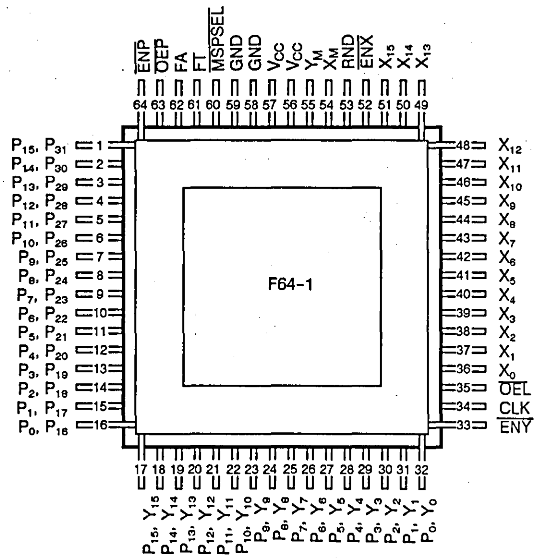
7

IDT7216



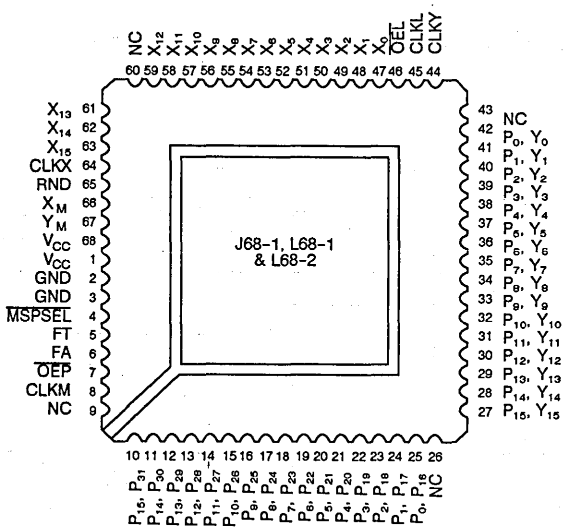
**64-LEAD FLATPACK
TOP VIEW**

IDT7217



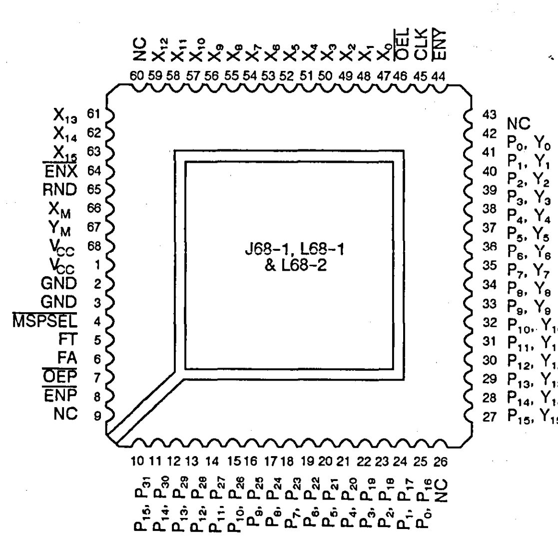
**64-LEAD FLATPACK
TOP VIEW**

IDT7216



**LCC/PLCC/
FINE-PITCH LCC
TOP VIEW**

IDT7217



**LCC/PLCC/
FINE-PITCH LCC
TOP VIEW**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL}	Input Low Voltage	–	–	0.8	V

DC ELECTRICAL CHARACTERISTICS-FAST

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to +70°C, Military V_{CC} = 5V ±10%, T_A = -55°C to +125°C) for Commercial clocked multiply times of 20, 25, 35, 45, 55, 65ns or Military, 25, 30, 40, 55, 65, 75ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.[1]	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.[1]	MILITARY MAX.	UNIT
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	–	–	10	–	–	20	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	–	10	–	–	20	µA
I_{CC}[2]	Operating Power Supply Current	Outputs Open Measured at 10MHz[2]	–	40	80	–	40	100	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	–	20	40	–	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ -0.2V, $V_{IN} \leq$ 0.2V	–	4	20	–	4	25	mA
I_{CC}/f [2,3]	Increase in Power Supply Current MHz	V_{CC} = Max., f > 10MHz	–	–	4	–	–	6	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	–	–	2.4	–	–	V
V_{OL}[4]	Output Low Voltage	V_{CC} = Min., I_{OL} = 4mA	–	–	0.4	–	–	0.4	V

NOTES:
1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 80 + 4(f-10)mA; for the military range, I_{CC} = 100 + 6(f-10). f = operating frequency in MHz, f = 1/t_{MUC} for IDT7216 and f = 1/t_{MC} for IDT7217.
3. For frequencies greater than 10MHz.
4. I_{OL} = 8mA for t_{MC} = 20 to 55ns

DC ELECTRICAL CHARACTERISTICS-SLOW

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to +70°C, Military V_{CC} = 5V ±10%, T_A = -55°C to +125°C) for Commercial clocked multiply times of 75, 95, 140ns or Military, 90, 120, 185ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.[1]	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.[1]	MILITARY MAX.	UNIT
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	–	–	2	–	–	10	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	–	2	–	–	10	µA
I_{CC}[2]	Operating Power Supply Current	Outputs Open Measured at 10MHz[2]	–	30	60	–	30	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	–	10	30	–	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ -0.2V, $V_{IN} \leq$ 0.2V	–	0.1	1.0	–	1.0	2.0	mA
I_{CC}/f [2,3]	Increase in Power Supply Current MHz	V_{CC} = Max., f > 10MHz	–	–	4	–	–	6	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4mA	–	–	0.4	–	–	0.4	V

NOTES:
1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 60 + 4(f-10)mA, where f = operating frequency in MHz; for the military range, I_{CC} = 80 + 6(f-10) where f = operating frequency in MHz.
3. For frequencies greater than 10MHz.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

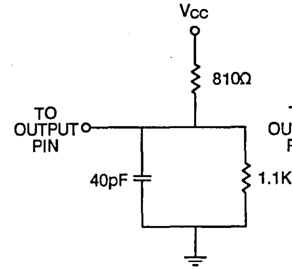


Figure 1. AC Output Test Load

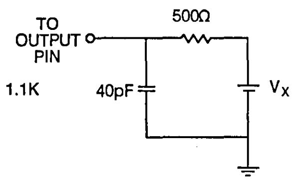
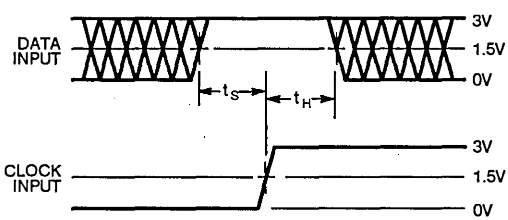


Figure 2. Output Three-State Delay Load (V_X = 0V or 2.6V)



NOTE:
1. Diagram shown for HIGH data only.Output transition may be opposite sense.

Figure 3. Set-Up And Hold Time

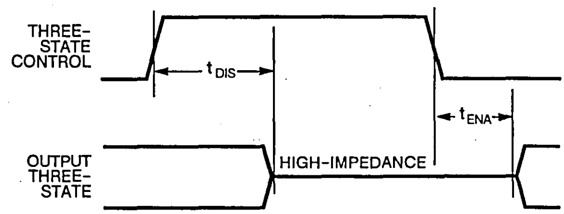


Figure 4. Three-State Control Timing Diagram

AC ELECTRICAL CHARACTERISTICS COMMERCIAL(3) (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	7216L20/25 7217L20/25 MIN.	MAX.	7216L35/45 7217L35/45 MIN.	MAX.	7216L55/65 7217L55/65 MIN.	MAX.	7216L75/90 7217L75/90 MIN.	MAX.	7216L140 7217L140 MIN.	MAX.	UNIT
t_{MUC}	Unclocked Multiply Time	–	30/38	–	55/65	–	75/85	–	100/125	–	180	ns
t_{MC}	Clocked Multiply Time	–	20/25	–	35/45	–	55/65	–	75/90	–	140	ns
t_S	X, Y, RND Set-up Time	10/12	–	12/15	–	20	–	25	–	25	–	ns
t_H	X, Y, RND Hold Time	0/2	–	3	–	3	–	2/0	–	0	–	ns
t_{PWH}	Clock Pulse Width High	9/10	–	10/15	–	15	–	20	–	25	–	ns
t_{PWL}	Clock Pulse Width Low	9/10	–	10/15	–	20	–	20	–	25	–	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out	–	18/20	–	25	–	25/30	–	30/35	–	40	ns
t_{PDP}	Output Clock to P	–	18/20	–	25	–	30	–	35	–	40	ns
t_{PDY}	Output Clock to Y	–	18/20	–	25	–	30	–	35	–	40	ns
t_{ENA}	3-State Enable Time(2)	–	18/20	–	25	–	30/35	–	35	–	40	ns
t_{DIS}	3-State Disable Time(2)	–	15/18	–	22	–	25	–	30	–	40	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	10	–	10	–	10	–	25	–	25	–	ns
t_H	Clock Enable Hold Time (IDT7217 only)	0/2	–	3	–	3	–	3	–	3	–	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)(1)	0	–	0	–	0	–	0	–	0	–	ns

NOTES:
1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured +500mV from steady state voltage with loading specified in Figure 2.
3. For test load, see Figure 1.

AC ELECTRICAL CHARACTERISTICS MILITARY [3] (V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	7216L25/30 7217L25/30		7216L40/55 7217L40/55		7216L65/75 7217L65/75		7216L90/120 7217L90/120		7216L185 7217L185		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{MUC}	Unclocked Multiply Time	–	38/43	–	60/75	–	85/95	–	125/160	–	230	ns
t_{MC}	Clocked Multiply Time	–	25/30	–	40/55	–	65/75	–	90/120	–	185	ns
t_S	X, Y, RND Set-up Time	12	–	15/20	–	25	–	30	–	30	–	ns
t_H	X, Y, RND Hold Time	2	–	3	–	3	–	2/0	–	0	–	ns
t_{PWH}	Clock Pulse Width High	10	–	15	–	15	–	25/30	–	30	–	ns
t_{PWL}	Clock Pulse Width Low	10	–	15	–	15	–	25/30	–	30	–	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out	–	20	–	25/30	–	35	–	40	–	45	ns
t_{PDP}	Output Clock to P	–	20	–	25/30	–	30/35	–	40	–	45	ns
t_{PDY}	Output Clock to Y	–	20	–	25/30	–	30/35	–	40	–	45	ns
t_{ENA}	3-State Enable Time [2]	–	20	–	25	–	35/40	–	40	–	45	ns
t_{DIS}	3-State Disable Time [2]	–	18	–	25	–	25	–	40	–	45	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	10	–	12/15	–	15	–	30	–	30	–	ns
t_H	Clock Enable Hold Time (IDT7217 only)	2	–	3	–	3	–	3	–	3	–	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only) [1]	0	–	0	–	0	–	0	–	0	–	ns

NOTES:
1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured +500mV from steady state voltage with loading specified in Figure 2.
3. For test load, see Figure 1.

7

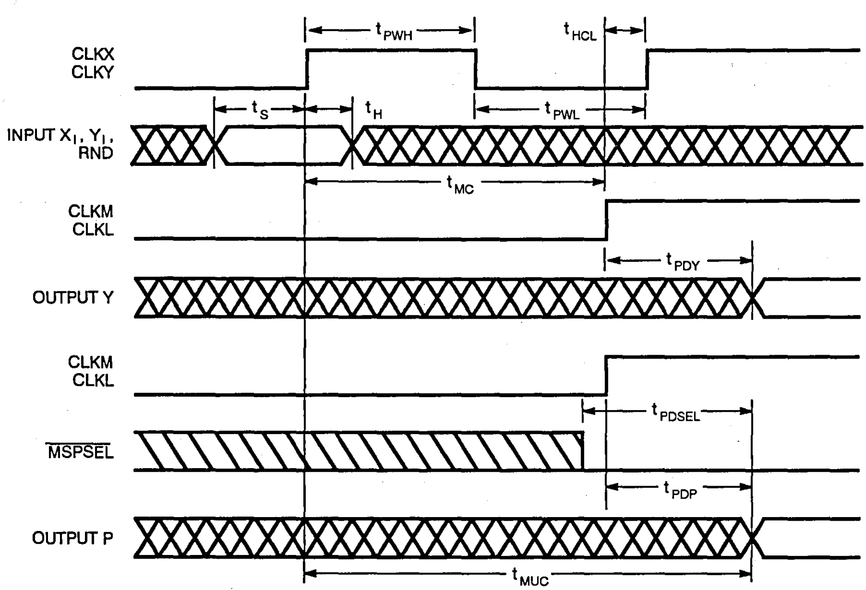


Figure 5. IDT7216 Timing Diagram

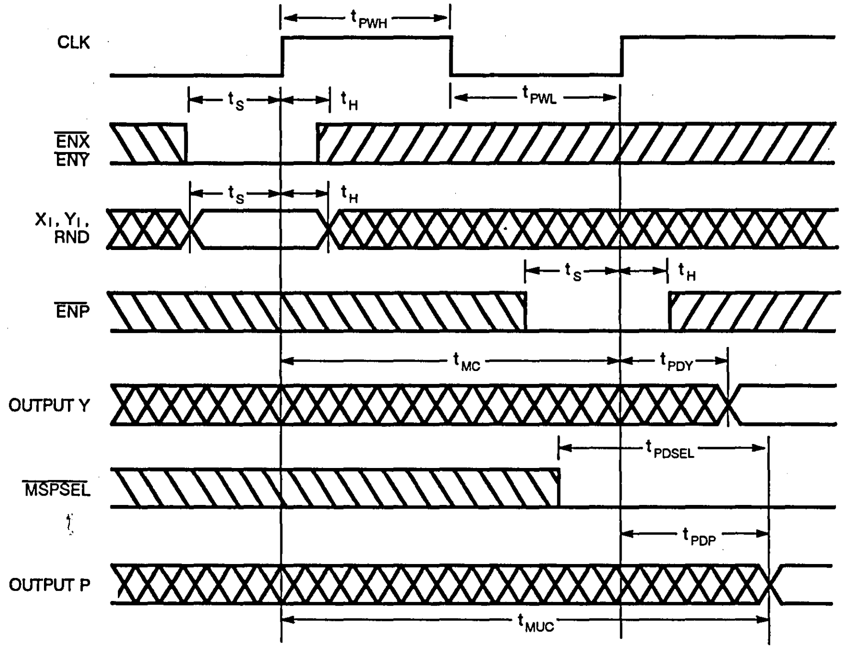


Figure 6. IDT7217 Timing Diagram

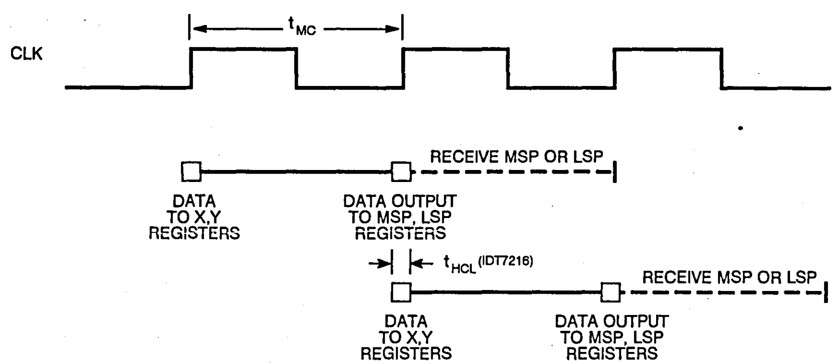


Figure 7. Simplified Timing Diagram–Typical Application

SIGNAL DESCRIPTIONS

INPUTS:

X_{IN} (X_{15} through X_0)

Sixteen Multiplicand Data Inputs.

Y_{IN} (Y_{15} through Y_0)

Sixteen Multiplier Data Inputs. (This is also an output port for $P_{15\text{-}0}$.)

INPUT CLOCKS (IDT7216 ONLY)

CLKX

The rising edge of this clock loads the $X_{15\text{-}0}$ data input register along with the X mode and round registers.

CLKY

The rising edge of this clock loads the $Y_{15\text{-}0}$ data input register along with the Y mode and round registers.

CLKM

The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKL

The rising edge of this clock loads the Least Significant Product (LSP) register.

INPUT CLOCKS (IDT7217 ONLY)

CLK

The rising edge of this clock loads all registers.

$\overline{\text{ENX}}$

Register enable for the $X_{15\text{-}0}$ data input register along with the X mode and round registers.

$\overline{\text{ENY}}$

Register enable for the $Y_{15\text{-}0}$ data input register along with the Y mode and round registers.

$\overline{\text{ENP}}$

Register enable for the Most Significant Product (MSP) and Least Significant Product (LSP).

CONTROLS

X_M, Y_M (TCX, TCY)[1]

Mode control inputs for each data word. A LOW input designates unsigned data input and a HIGH input designates two's complement.

FA (RS)[1]

When the format adjust control is HIGH, a full 32-bit product is selected. When this control is LOW, a left-shifted 31-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional two's complement applications (see Multiplier Input/Output Formats).

FT

When this control is HIGH, both the Most Significant Product (MSP) and Least Significant Product (LSP) registers are transparent.

$\overline{\text{OEL}}$

Three-state enable for routing LSP through Y_{IN} /LSP_{OUT} port.

$\overline{\text{OEP}}$

Three-state enable for the product output port.

RND

Round control for the rounding of the Most Significant Product (MSP). When this control is HIGH, a one is added to the Most Significant Bit (MSB) of the Least Significant Product (LSP). Note that this bit depends on the state of the format adjust (FA) control. If FA is LOW when RND is HIGH, a one will be added to the 2^{-16} bit (P_{14}). If FA is HIGH when RND is HIGH, a one will be added to the 2^{-15} bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

MSPSEL

When the $\overline{\text{MSPSEL}}$ is LOW, the Most Significant Product (MSP) is selected. When HIGH, the Least Significant Product (LSP) is available at the product output port.

OUTPUTS

MSP (P_{31} through P_{16})

Most Significant Product output.

LSP (P_{15} through P_0)

Least Significant Product output.

$Y_{15\text{-}0}$ /LSP_{OUT} (Y_{15} through Y_0 or P_{15} through P_0)

Least Significant Product (LSP) Output available when $\overline{\text{OEL}}$ is LOW. This is also an output port for $Y_{15\text{-}0}$.

NOTE:
1. TRW MPY016H/K pin designation.

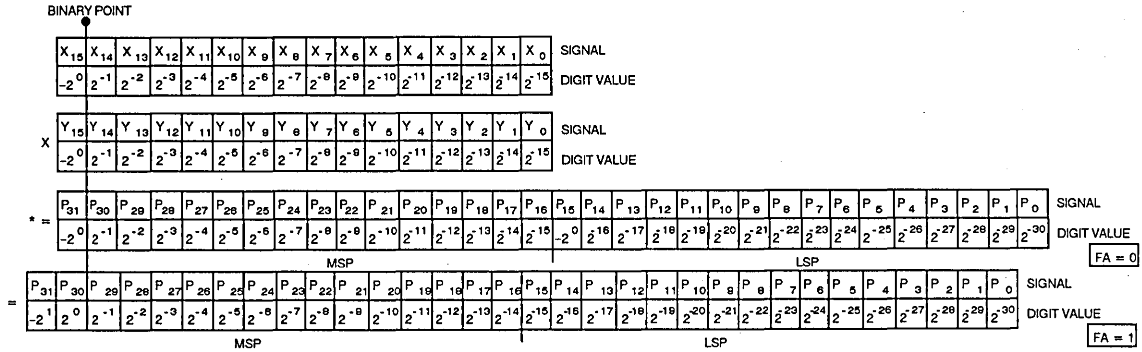


Figure 8. Fractional Two's Complement Notation

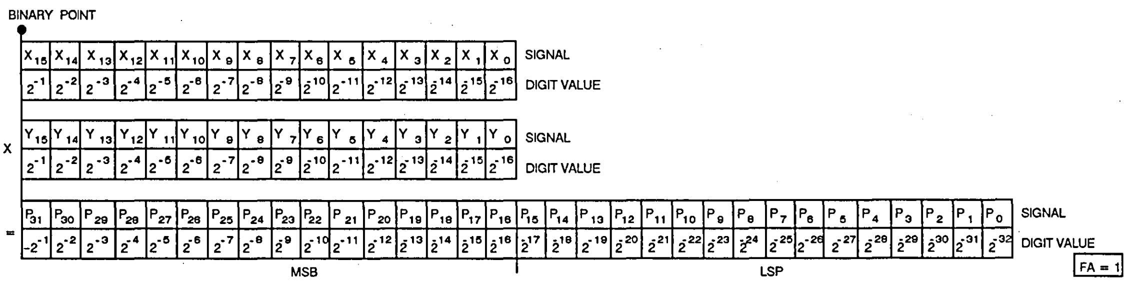


Figure 9. Fractional Unsigned Magnitude Notation

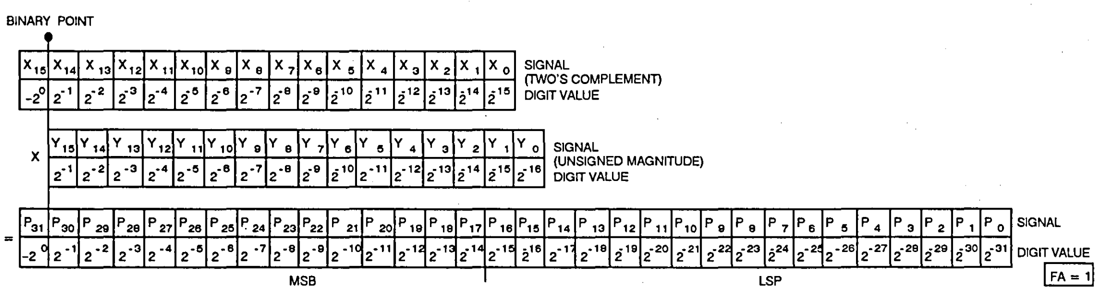


Figure 10. Fractional Mixed Mode Notation

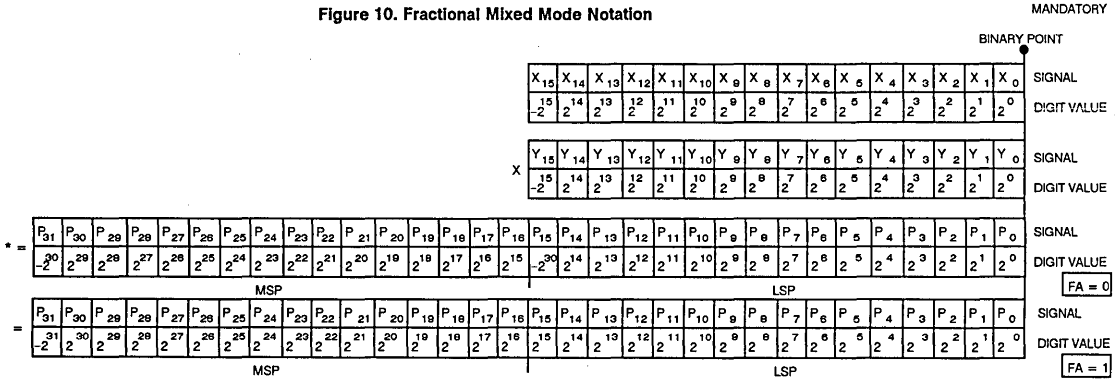


Figure 11. Integer Two's Complement Notation

*In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000 . . . 0 with 1,000.0 yielding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

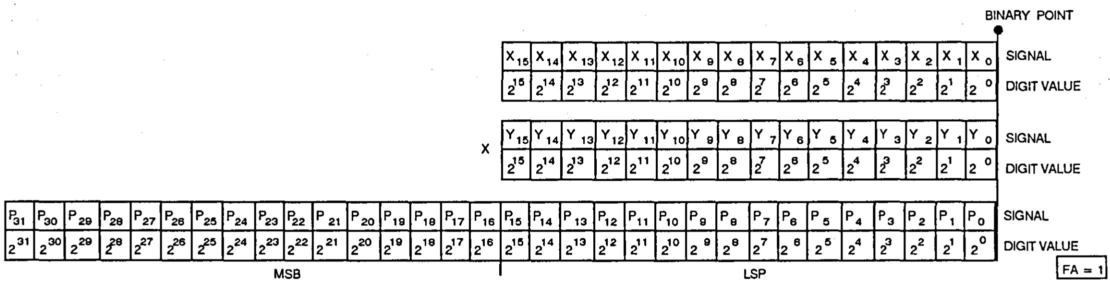


Figure 12. Integer Unsigned Magnitude Notation

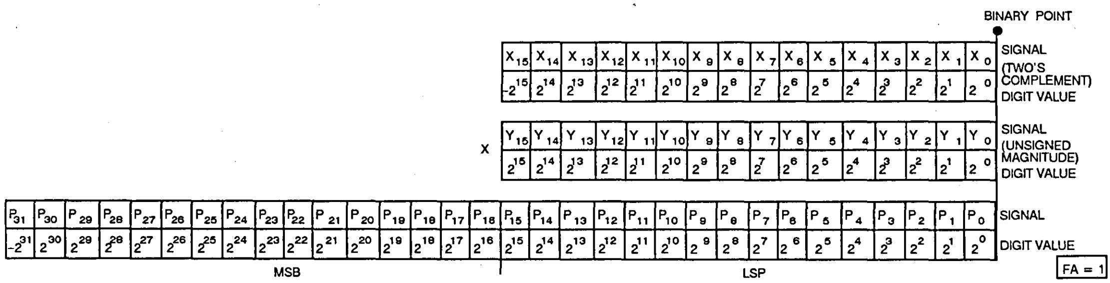


Figure 13. Integer Mixed Mode Notation

ORDERING INFORMATION

IDT XXXX (Device Type) XX (Power) XXX (Speed) XX (Package) X (Process/Temperature Range)

Process/Temperature Range
- BLANK — Commercial (0°C to +70°C)
- B — Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package
- P — Plastic DIP
- XC — Shrink-DIP
- C — Topbraze DIP
- J — Plastic Leaded Chip Carrier
- XL — Fine-Pitch LCC (.025 Centers)
- L — Leadless Chip Carrier
- F — Flatpack
- G — Pin Grid Array

Speed
- 20, 25, 35, 45, 55, 65, 75, 90, 140 — Commercial (t_{MC})
- 25, 30, 40, 55, 65, 75, 90, 120, 185 — Military (t_{MC})

Power
- L — Low Power

Device Type
- 7216, 7217 — 16 x 16 Multiplier

Integrated Device Technology, Inc.

16 x 16-BIT PARALLEL CMOS MULTIPLIER WITH 32-BIT OUTPUT

ADVANCE INFORMATION
IDT7317

FEATURES

- 16 x 16-bit parallel multiplier with 32-bit output available immediately
- 20ns clocked multiply time
- Low power consumption: 80mA (worst case)
- One clock and three register enables
- Unsigned, Two's Complement or Mixed mode operations
- Flexible output scaling shifter
- Pipeline or Flow-through modes
- TTL-compatible input/output
- Three-state outputs
- Produced with advanced submicron CEMOS ™ high-performance technology
- Available in 84-lead Pin Grid Array
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

The IDT7317 is a high-speed, low-power 16 x 16-bit multiplier which halves the processing time of previously available devices by virtue of the whole 32-bit product being accessible on the output bus. This feature eliminates the need for multiplexing the Most Significant Product (MSP) and Least Significant Product (LSP) on the same 16-bit output bus. IDT's high-performance submicron CEMOS technology yields very fast (20ns) clocked multiply times.

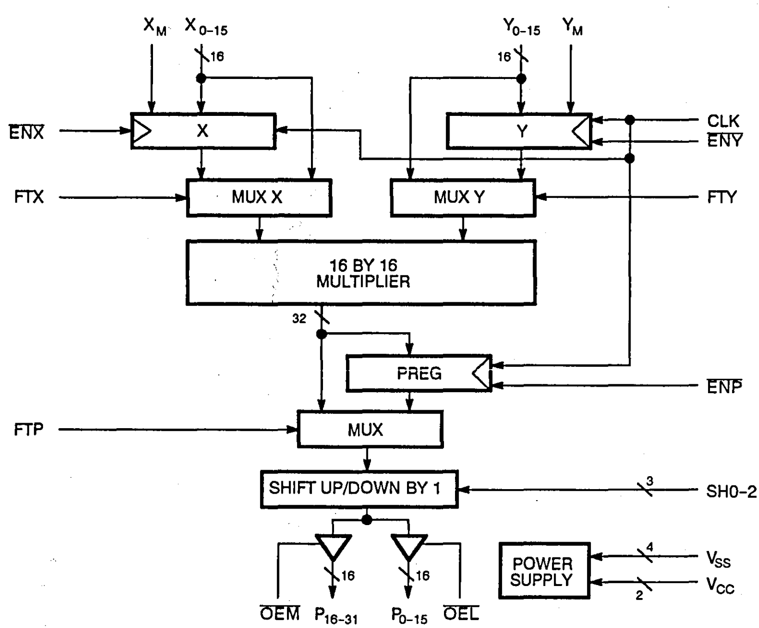
The IDT7317 is ideal for Digital Signal Processing (DSP) applications requiring high-speed integer multiplications and requires the double precision 32-bit product available on the output in one clock cycle. Typical applications include Fast Fourier Transforms (FFT), digital filtering and graphic display systems.

All input registers and MSP and LSP output registers are designed with positive edge triggered D-type flip-flops. The IDT7317 has one clock and three register enables – $\overline{ENX}$ and $\overline{ENY}$ control the input registers; $\overline{ENP}$ controls the 32-bit output register.

An output scaling shifter can shift the 32-bit result up or down by one position for sign extension or for greater result accuracy.

Military versions of the IDT7317 are manufactured in compliance with the latest revision of MIL-STD-883, Class B for high-reliability systems.

FUNCTIONAL BLOCK DIAGRAMS



CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

PIN CONFIGURATIONS

(CONSULT FACTORY)

PIN DESCRIPTION

INPUTS

DATA INPUT (X_{0-15})

Sixteen-bit multiplicand data inputs.

DATA INPUT (Y_{0-15})

Sixteen-bit multiplier data inputs.

OUTPUTS

DATA OUTPUT (P_{0-31})

Thirty-two-bit product outputs, P_{0-15} is the LSP and P_{16-31} is the MSP.

CONTROLS

CLOCK (CLK)

Clock input, the low-to-high transition loads all registers.

ENABLE X REGISTER ($\overline{ENX}$)

Register enable for the X_{0-15} data input register and X mode.

ENABLE Y REGISTER ($\overline{ENY}$)

Register enable for the Y_{0-15} data input register and Y mode.

ENABLE P REGISTER ($\overline{ENP}$)

Register enable for the P_{0-31} data output register.

X_M

Mode control for input X_{0-15}. A low input designates unsigned data input; a high input designates two's complement.

Y_M

Mode control for input Y_{0-15}. A low input designates unsigned data input; a high input designates two's complement.

FLOW-THROUGH-X (FTX)

Flow-through control input. When FTX is high, the input register X is transparent.

FLOW-THROUGH-Y (FTY)

Flow-through control input. When FTY is high, the input register Y is transparent.

FLOW-THROUGH-P (FTP)

Flow-through control input. When FTP is high, the output register P is transparent.

SHIFT CONTROL (SH0-2)

Shift control input pins which are used to normalize or scale the output as follows:

SH2	SH1	SH0	CONTROL
0	X	X	No shift
1	0	0	Shift up by 1 position arithmetic and fill 0
1	0	1	Shift up logical by 1 position and fill 0
1	1	0	Shift down by 1 position arithmetic and sign extension
1	1	1	Shift down logical by 1 position and fill 0

OUTPUT ENABLE, P_{0-15} ($\overline{OEL}$)

Three-state enable for the LSP, P_{0-15}.

OUTPUT ENABLE, P_{16-31} ($\overline{OEM}$)

Three-state enable for the MSP, P_{16-31}.

POWER SUPPLY

V_{CC0-1}

Two power supply pins, 5V.

V_{SS0-3}

Four ground pins, 0V.

Integrated Device Technology, Inc.

16-BIT CMOS EIGHT-LEVEL PIPELINE REGISTER

ADVANCE INFORMATION
IDT7320

FEATURES:

- Eight 16-bit high-speed pipeline registers
- Configurable to four two-level, two four-level or eight single-level registers
- Powerful instruction set: Transfer, Hold, Load Directly
- Fast 10ns access time
- Serial Protocol Channel (SPC™) for diagnostics
- Functionally replaces four Am29520s
- Used for temporary address storage or programmable pipeline registers for DSP and Array Processing systems
- Synchronous FIFO applications
- Coefficient storage for FIR filters
- Video delay line or temporary data storage applications
- High-performance, low-power, submicron CEMOS™ technology
- Available in 48-pin plastic and ceramic DIP and 52-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7320 contains eight 16-bit registers which can be configured to be four two-level, two four-level or eight single-level pipeline registers. Under control of four instruction bits (I_{0-3}), input data (D_{0-15}) can be loaded directly into any of the individual registers or entered into the multi-level pipeline registers with a Load and Shift instruction. Two other instructions allow contents to be shifted or held.

An eight-to-one multiplexer allows data to be read from any one of eight registers (REGA-REGH). A 3-bit multiplexer select (SEL_{0-2}) control selects which of the eight registers is available at the output (Y_{0-15}). An Output Enable ($\overline{OE}$), when low, latches output data on the output pins.

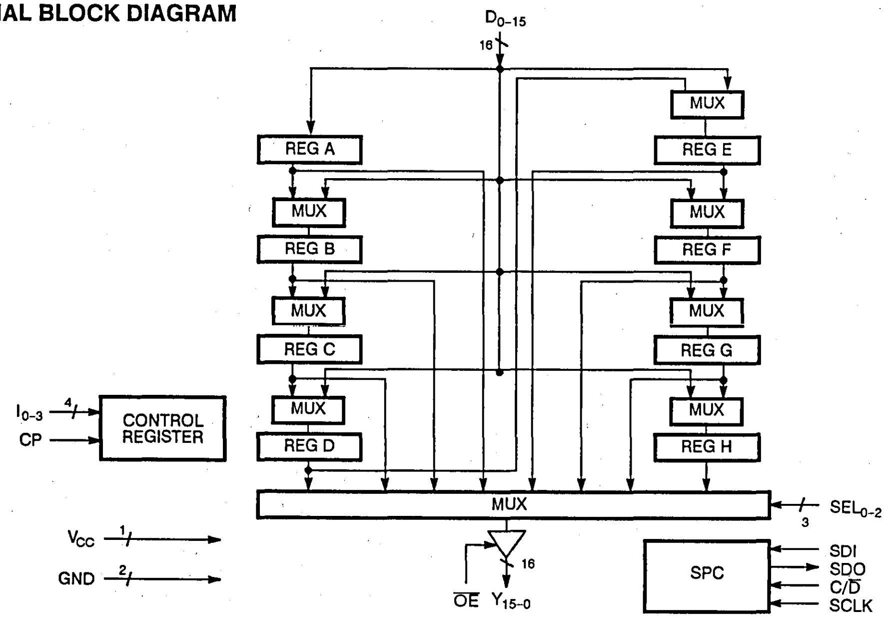
Manufactured in high-speed, submicron CEMOS technology, the register access time is 10ns, making the IDT7320 ideal for very high-speed Digital Signal Processing (DSP) and Array Processing applications.

The IDT7320 includes the innovative Serial Protocol Channel (SPC) used for system diagnostics. This on-chip feature greatly simplifies the task of writing and debugging microcode, field maintenance debug and test and system test during manufacture.

The IDT7320 is ideal for high-speed DSP applications which require an easily accessible scratch pad register for coefficients or data. It can be used as a synchronous FIFO or for video delay lines.

Available packages include 48-pin plastic and ceramic DIP and surface mount 52-pin LCC and PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

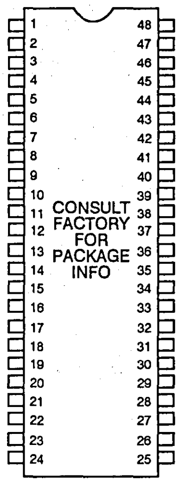


CEMOS and SPC are trademarks of Integrated Device Technology, Inc.

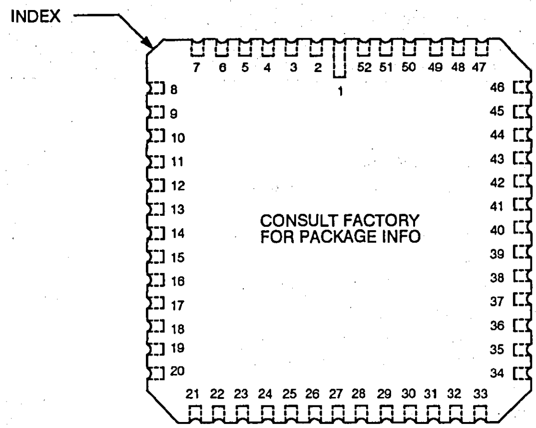
MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-2027/-

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTION

INPUTS

DATA IN (D_{0-15})

Data input port, 16 bits wide.

CONTROL

MULTIPLEXER SELECT (SEL_{0-2})

Three-bit load control lines select the one of eight registers appearing on the output Y_{0-15}.

INSTRUCTION CONTROL (I_{0-3})

Four-bit instruction control lines which determine the operation to be performed on the registers.

CLOCK (CP)

Input clock pin.

OUTPUT ENABLE ($\overline{OE}$)

Output Enable latches data onto the output pins (Y_{0-15}) when low.

SERIAL PROTOCOL CHANNEL (SPC)

SERIAL DATA INPUT (SDI)

Serial data input pin used for receiving diagnostic data and commands from a host system or from the SDO pin of a cascaded multi-level pipeline register.

SERIAL DATA OUTPUT (SDO)

Serial data output pin used for transmitting diagnostic data and commands to a host system or a cascaded multi-level pipeline register via its SDI pin.

SERIAL CLOCK (SCLK)

Input pin used for clocking in diagnostic data and command information at the SDI pin. This pin should be tied low when the diagnostic function is not being used.

COMMAND/DATA (C/D)

Command/Data input pin, when tied low, defines the bit pattern being received at the SDI pin as Data and, when high, defines the incoming pattern as a command for executing diagnostic function. This pin should be tied high when the diagnostics feature is not being used.

OUTPUTS

DATA OUT (Y_{0-15})

Data output port, 16 bits wide.

POWER SUPPLY

V_{CC}

One power supply pin, 5V.

V_{SS0-1}

Two GND pins, 0V.

Integrated Device Technology, Inc.

16-BIT CASCADABLE ALU

ADVANCE INFORMATION
IDT7381

FEATURES:

- High-performance 16-bit cascadable Arithmetic Logic Unit (ALU)
- Fast 30ns ALU operations (33MHz)
- 54/74S381 instruction set
- Pipeline or Flow-through modes
- Input and output registers can be made transparent
- Cascadable with or without carry lookahead
- Internal feedback path for accumulation
- Pin and functionally compatible with Gould S614381 and Logic Devices L4C381
- High-speed, low-power submicron CEMOS™ technology
- Available in 68-pin surface mount PLCC and LCC and 68-pin PGA
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7381 is a high-speed 16-bit cascadable Arithmetic Logic Unit (ALU). This three-bus device consists of two input registers, an ultra-fast 16-bit ALU and a 16-bit output register. With high-performance CEMOS technology, the IDT7381 can perform an ALU operation in 30ns. It functionally replaces four 54/74S381 four-bit ALUs in a compact, low-power CMOS 68-pin package.

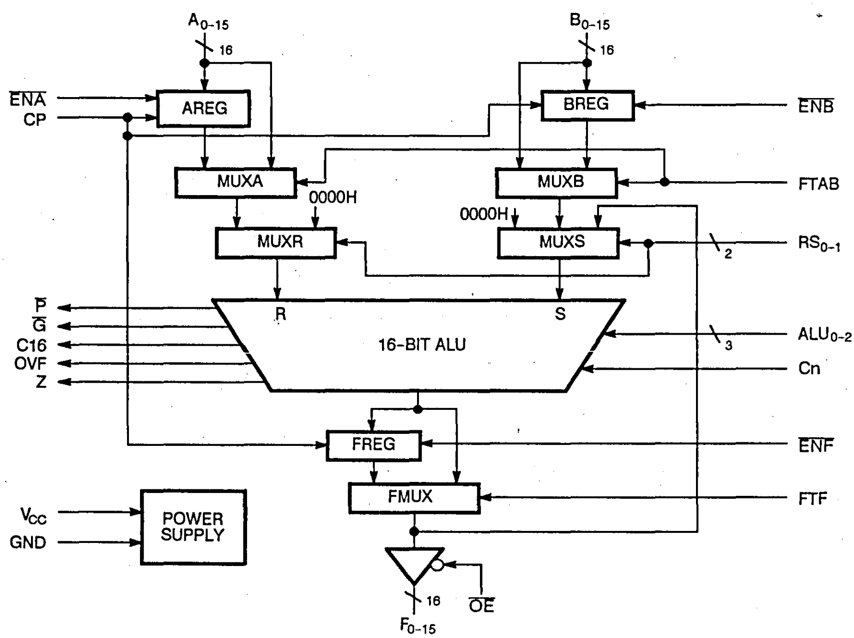
The arithmetic logic unit is a 16-bit ALU with full carry lookahead. It operates on two 16-bit operands (A_{0-15} and B_{0-15}). The two-bit operand select (RS_{0-1}) selects the R and S operands for the ALU. The three-bit ALU function (ALU_{0-2}) selects the operation to be performed. The IDT7381 can perform 3 arithmetic functions: Not(R) + S, R + Not(S) and R + S; 3 logical functions: R XOR S, R OR S and R AND S and 2 initialization functions: Set F to 0 and Preset F to 1. The 16-bit ALU result (F) is available on the output bus (Y_{0-15}).

The input and output registers are enabled under control of external pins: $\overline{ENA}$, $\overline{ENB}$ and $\overline{ENF}$, when low. The input and output registers can be made transparent under control of FTAB and FTF pins. When Output Enable ($\overline{OE}$) is low, the result is latched on the output bus.

Two status flags, Overflow (OVF) and Zero, are available as outputs. Also, Propagate ($\overline{P}$), Generate ($\overline{G}$), Carry Out (C_{n+16}) and Carry In (C_n) are provided to cascade the IDT7381 for 32-bit or wider data.

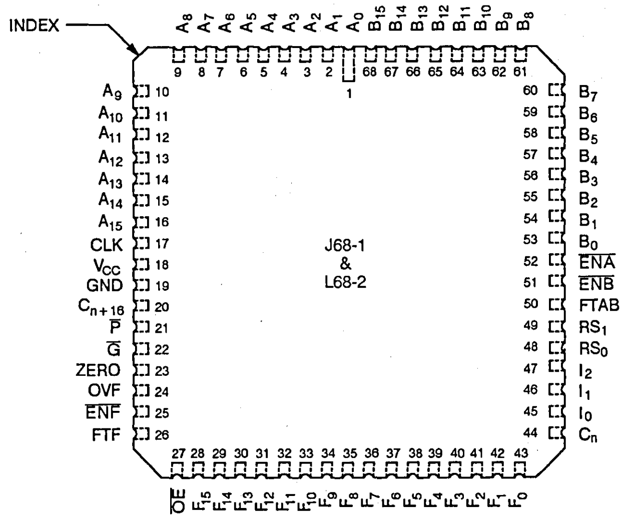
The IDT7381 is available in 68-pin surface mount, LCC and PLCC and Pin Grid Array. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, for high-reliability systems.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



LCC/PLCC TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L
11		B_7	B_6	B_4	B_2	B_0	$\overline{ENB}$	RS_1	I_2	I_0	
10	B_9	B_8	B_5	B_3	B_1	$\overline{ENA}$	FTAB	RS_0	I_1	C_n	F_0
09	B_{11}	B_{10}								F_2	F_1
08	B_{13}	B_{12}								F_4	F_3
07	B_{15}	B_{14}								F_6	F_5
06	A_1	A_0				CONSULT FACTORY FOR PACKAGE INFO				F_8	F_7
05	A_3	A_2								F_{10}	F_9
04	A_5	A_4								F_{12}	F_{11}
03	A_7	A_6								F_{14}	F_{13}
02	A_8	A_9	A_{11}	A_{13}	A_{15}	V_{CC}	C_{n+16}	$\overline{G}$	OVF	$\overline{OE}$	F_{15}
01	●	A_{10}	A_{12}	A_{14}	CLK	GND	$\overline{P}$	ZERO	$\overline{ENF}$	FTF	

Pin 1 Designator

PGA TOP VIEW

7

PIN DESCRIPTION

INPUTS

DATA A INPUT (A_{0-15})

Sixteen-bit data input port.

DATA B INPUT (B_{0-15})

Sixteen-bit data input port

CONTROLS

ENABLE REG A ($\overline{ENA}$)

Register enable for the A Register, active low.

ENABLE REG B ($\overline{ENB}$)

Register enable for the B Register, active low.

FLOW-THROUGH REG A/B (FTAB)

Flow-through control input. When this control is high, both register A and register B are transparent.

OPERAND SELECT (RS_{0-1})

Two-bit inputs are used to select the R-operand for ALU:

$RSEL_1$	$RSEL_0$	MUXR	MUXS
0	0	A	F
0	1	A	0
1	0	0	B
1	1	A	B

CLOCK (CP)

Clock Input.

ALU INSTRUCTION (ALU_{0-2})

Three-bit instruction control lines determines the ALU operation to be performed.

ALU_2	ALU_1	ALU_0	FUNCTION
0	0	0	FORCE F TO LOW
0	0	1	$F = \overline{R} + S$
0	1	0	$F = S + \overline{R}$
0	1	1	$F = R + S$
1	0	0	F = EXOR S
1	0	1	F = R OR S
1	1	0	F = R AND S
1	1	1	FORCE F TO HIGH

ENABLE REG F ($\overline{ENF}$)

Register enable for output F register, active low.

FLOW-THROUGH REG F (FT)

Flow-through control input. When this control signal is high, the F register is transparent.

OUTPUT ENABLE ($\overline{OE}$)

A control input pin which, when low, enables the three-state output buffer of Y_{0-15}. When high, it disables the three-state output buffer.

CARRY IN (C_n)

Carry In signals a carry input from the lesser significant word in the cascaded mode.

OUTPUTS

DATA OUTPUT (Y_{0-15})

Sixteen-bit output port.

PROPAGATE($\overline{P}$)

Propagate, when low, indicates the carry propagate output of the ALU.

OVERFLOW (OVF)

Overflow indicates the two's complement overflow.

GENERATE($\overline{G}$)

Generate, when low, indicates the carry generate output of the ALU.

CARRY OUT (C_{n+16})

Carry Out indicates the carry output.

ZERO DETECT (ZERO)

Zero detection output is open-drain and requires a pull-up resistor.

POWER SUPPLY

V_{CC}

One power supply pin, 5V.

GND

One ground pin, 0V.

BIT-SLICE MICROPROCESSOR DEVICES (MICROSLICE) AND EDC

Today, as for the past decade, the bit-slice processor offers the ultimate in microprocessor flexibility and performance. Through architectural enhancements and a powerful CEMOS technology, IDT has extended bit-slice performance levels far ahead of rival products.

The IDT49C400 building block family exemplifies this performance leadership. Our new architectures enable the user to obtain magnitudes of increased system speed while maintaining low CMOS power. Featured in this standard product family are the world's fastest microprogram microprocessors (including our new 32-bit IDT49C404), sequencers and register files. Additionally, IDT manufactures pin-compatible CMOS 2900 products which offer speed upgrades of up to 50% faster than bipolar equivalents.

IDT's streamlined, bit-slice architectures now enable high-speed system designers to develop ultra-fast, innovative systems which use the most powerful building block product available.

Error detection and correction play a major role in maintaining the integrity of data in large, high-speed memory boards. IDT's new family of EDC products not only boost the reliability of memory systems but do it utilizing ultra-fast CEMOS technology.

In March 1986, IDT introduced its first EDC product, the 16-bit IDT39C60. It was the first CMOS EDC device ever available and was also the world's fastest at 20ns maximum detect time. This new performance plateau set the stage for IDT's next new device, the industry-leading 32-bit IDT49C460. Available in April 1986, it too sported the industry's fastest speeds while consuming ultra-low CMOS power. It was also the only 32-bit EDC cascadable to 64 bits, ideal for today's large, high-speed systems.

Additionally, both 16- and 32-bit versions are available in space-saving surface mount and dual in-line packages, aimed at satisfying the most stringent commercial and military product needs.

IDT will continue to introduce performance upgrades to its existing product family, while offering many new architectural enhancements to the world of error detection and correction products.

TABLE OF CONTENTS

CONTENTS **PAGE**

Integrated Device Technology, Inc.

FOUR-BIT CMOS MICROPROCESSOR SLICE

IDT39C01C
IDT39C01D
IDT39C01E

MICROSLICE ™ PRODUCT

FEATURES:

- Low-power CEMOS ™
  - I_{CC} (max.)
    Military: 35mA
    Commercial: 30mA
  Fast
  - IDT39C01C—meets 2901C speeds
  - IDT39C01D—20% speed upgrade
  - IDT39C01E—40% speed upgrade
- Eight-function ALU
  - Performs addition, two subtraction operations and five logic functions on two source operands
- Expandable
  - Longer word lengths achieved through cascading any number of IDT39C01s
- Four status flags
  - Carry, overflow, negative and zero
- Pin-compatible and functionally equivalent to all versions of the 2901
- Available in 40-pin DIP and 44-pin LCC
- Military product available compliant to MIL-STD-883,

DESCRIPTION:

The IDT39C01s are high-speed, cascadable ALUs which can be used to implement CPUs, peripheral controllers and programmable microprocessors. The IDT39C01's microinstruction flexibility allows for easy emulation of most digital computers.

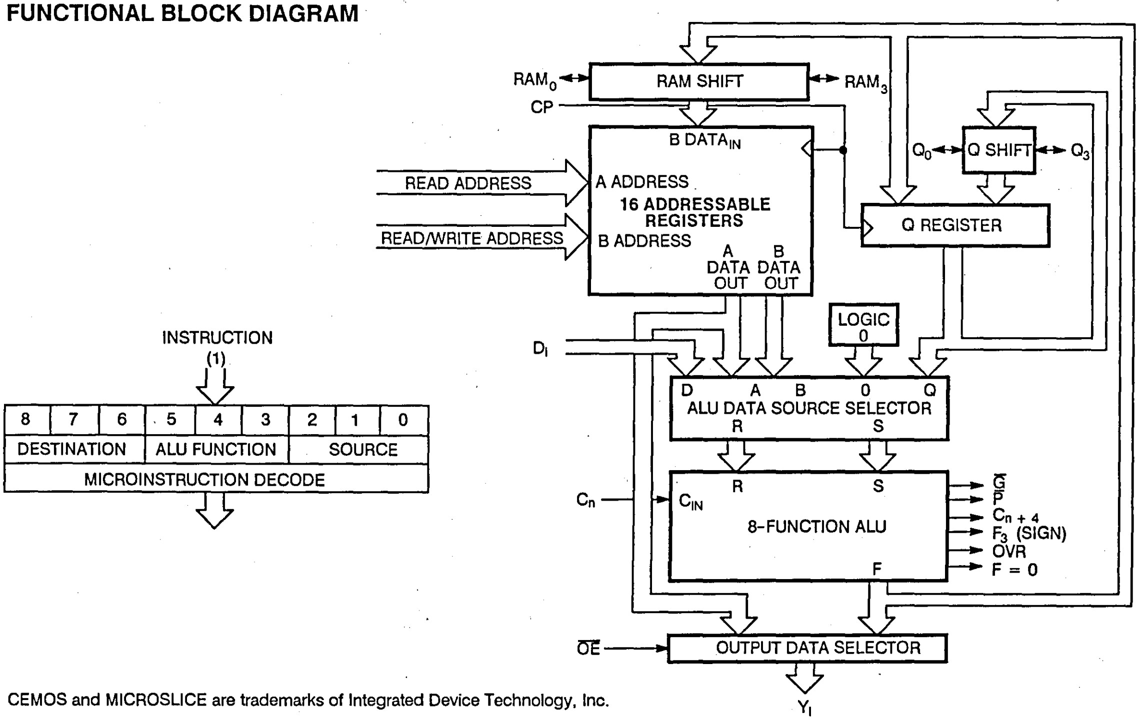
This extremely low-power yet high-speed ALU consists of a 16-word by 4-bit dual-port RAM, a high-speed ALU and the required shifting, decoding and multiplexing logic. It is expandable in 4-bit increments, contains a flag output along with three-state data outputs and can easily use either a ripple carry or full lookahead carry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU destination register, ALU source operands and the ALU function.

The IDT39C01 is fabricated using CEMOS, a CMOS technology designed for high-performance and high-reliability. It is a pin-compatible, performance-enhanced, functional replacement for all versions of the 2901.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

8

FUNCTIONAL BLOCK DIAGRAM

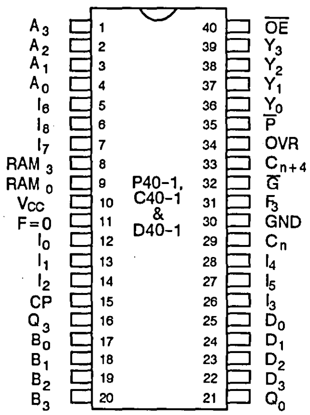


CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.

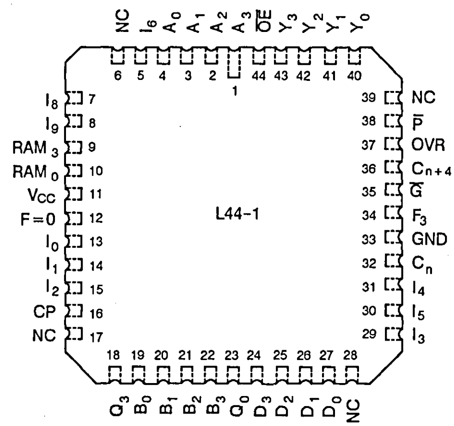
MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-9000/-

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

FLATPACK
(Consult Factory)

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_0-A_3	I	Four address inputs to the register file which selects one register and displays its contents through the A port.
B_0-B_3	I	Four address inputs to the register file which selects one of the registers in the file, the contents of which is displayed through the B port. It also selects the location into which new data can be written when the clock goes LOW.
I_0-I_8	I	Nine instruction control lines which determine what data source will be applied to the ALU $I_{0,1,2}$, what function the ALU will perform $I_{3,4,5}$ and what data is to be deposited in the Q Register or the register file $I_{6,7,8}$.
D_0-D_3	I	Four-bit direct data inputs which are the ALU data source for entering external data into the device. D_0 is the LSB.
Y_0-Y_3	O	Four three-state output lines which, when enabled, display either the four outputs of the ALU or the data on the A port of the register stack. This is determined by the destination code $I_{6,7,8}$.
F_3	O	Most significant ALU output bit (sign-bit).
F = 0	O	Open drain output which goes HIGH if the F_0 -F_3 ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C_n	I	Carry-in to the internal ALU.
C_{n+4}	O	Carry-out of the internal ALU.
Q_3 RAM_3	I/O	Bidirectional lines controlled by $I_{6,7,8}$. Both are three-state output drivers connected to the TTL-compatible CMOS inputs. When the destination code on $I_{6,7,8}$ indicates an up shift, the three-state outputs are enabled, the MSB of the Q Register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q_0 RAM_0	I/O	Both bidirectional lines function identically to Q_3 and RAM_3 lines except they are the LSB of the Q Register and RAM.
$\overline{OE}$	I	Output enable on which, when pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
$\overline{G}$, $\overline{P}$	O	Carry generate and carry propagate output of the ALU. These are used to perform a carry-lookahead operation.
OVR	O	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sigh-bit.
CP	I	Clock input. LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 16 x 4 RAM which compromises the master latches of the register file. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.

DEVICE ARCHITECTURE:

The IDT39C01 CMOS bit-slice microprocessor is configured four bits wide and is cascadable to any number of bits (4, 8, 12, 16, etc.). Key elements which make up this four-bit microprocessor slice are: (1) the register file (16 x 4 dual-port RAM) with shifter, (2) ALU and (3) Q Register and shifter.

REGISTER FILE—RAM data is read from the A port as controlled by the 4-bit A address field input. Data, as defined by the B address field input, can be simultaneously read from the B port of the RAM. This same code can be applied to the A select and B select field with the identical data appearing at both the RAM A port and B port outputs simultaneously. New data is written into the file (word) defined by the B address field of the RAM when activated by the RAM write enable. The RAM data input field is driven by a 3-input multiplexer that is used to shift the ALU output data (F). It is capable of shifting the data up one position, down one position or not shifting at all. The other inputs to the multiplexer are from the RAM_3 and RAM_0 I/O pins. For a shift up operation, the RAM_3 output buffer is enabled and the RAM_0 multiplexer input is enabled. During a shift down operation the RAM_0 output buffer is enabled and the RAM_3 multiplexer input is enabled. Four-bit latches hold the RAM data while the clock is LOW with the A port output and B port output each driving separate latches. The data to be written into the RAM is applied from the ALU F output.

ALU—The ALU can perform three binary arithmetic and five logic operations on the two 4-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer with both having an inhibit capability. Both multiplexers are controlled by the I_0, I_1, I_2 inputs. This multiplexer configuration enables the user to select various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. Microinstruction inputs (I_3, I_4, I_5) are used to select the ALU function. This high-speed ALU also incorporates a carry-in (C_n) input, carry propagate ($\overline{P}$) output, carry generate ($\overline{G}$) output and carry-out (C_{n+4}) all aimed at accelerating arithmetic operations by the use of carry-lookahead logic. The overflow output pin (OVR) will be HIGH when arithmetic operations exceed the two's complement number range. The ALU data outputs (F_0, F_1, F_2, F_3) are routed to the RAM Q Register inputs and the Y outputs under control of the I_6, I_7, I_8 control signal inputs. The MSB of the ALU is output as F_3 so the user can examine the sign-bit without enabling the three-state outputs. An open drain output, F = 0, is HIGH when $F_0 = F_1 = F_2 = F_3 = 0$ so that the user can determine when the ALU output is zero by wire-ORing these outputs together.

Q REGISTER—The Q Register is a separate 4-bit file intended for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. It is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q Register. In either the shift-up or shift-down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q_0 and Q_3, which operate comparably to the RAM shifter. They are controlled by the I_6, I_7, I_8 inputs.

The clock input of the IDT39C01 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW-to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and RAM EN is enabled, new data will be written into the RAM file defined by the B address field.

8

ALU SOURCE OPERAND CONTROL

MNEMONIC	MICROCODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	OCTAL CODE	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

ALU FUNCTION CONTROL

MNEMONIC	MICROCODE				ALU FUNCTION	SYMBOL
	I_5	I_4	I_3	OCTAL CODE		
ADD	L	L	L	0	R Plus S	$R + S$
SUBR	L	L	H	1	S Minus R	$S - R$
SUBS	L	H	L	2	R Minus S	$R - S$
OR	L	H	H	3	R OR S	$R \vee S$
AND	H	L	L	4	R AND S	$R \wedge S$
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \veebar S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

ALU DESTINATION CONTROL

MNEMONIC	MICROCODE				RAM FUNCTION		Q REGISTER FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	OCTAL CODE	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_3	X	Q_3

X = DON'T CARE. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
UP is toward MSB; DOWN is toward LSB.

SOURCE OPERAND AND ALU FUNCTION MATRIX

OCTAL $I_{5,4,3}$	ALU FUNCTION	$I_{2,1,0}$ OCTAL							
		0	1	2	3	4	5	6	7
		ALU SOURCE							
		A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S C_n = H	A + B A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q - A - 1 Q - A	B - A - 1 B - A	Q - 1 Q	B - 1 B	A - 1 A	A - D - 1 A - D	Q - D - 1 Q - D	-D - 1 -D
2	C_n = L R Minus S C_n = H	A - Q - 1 A - Q	A - B - 1 A - B	-Q - 1 -Q	-B - 1 -B	-A - 1 -A	D - A - 1 D - A	D - Q - 1 D - Q	D - 1 D
3	R OR S	A V Q	A V B	Q	B	A	D V A	D V Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ⊽ Q	A ⊽ B	Q	B	A	D ⊽ A	D ⊽ Q	D
7	R EX-NOR S	$\overline{A ⊽ Q}$	$\overline{A ⊽ B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D ⊽ A}$	$\overline{D ⊽ Q}$	$\overline{D}$

+ = PLUS; - = MINUS; ∧ = AND; ⊽ = EX-OR; V = OR

ALU LOGIC MODE FUNCTIONS

OCTAL $I_{5,4,3}$	OCTAL $I_{2,1,0}$	GROUP	FUNCTION
4	0	AND	$A \wedge Q$
4	1		$A \wedge B$
4	5		$D \wedge A$
4	6		$D \wedge Q$
3	0	OR	$A \vee Q$
3	1		$A \vee B$
3	5		$D \vee A$
3	6		$D \vee Q$
6	0	EX-OR	$A \forall Q$
6	1		$A \forall B$
6	5		$D \forall A$
6	6		$D \forall Q$
7	0	EX-NOR	$\overline{A \forall Q}$
7	1		$\overline{A \forall B}$
7	5		$\overline{D \forall A}$
7	6		$\overline{D \forall Q}$
7	2	INVERT	$\overline{Q}$
7	3		$\overline{B}$
7	4		$\overline{A}$
7	7		$\overline{D}$
6	2	PASS	Q
6	3		B
6	4		A
6	7		D
3	2	PASS	Q
3	3		B
3	4		A
3	7		D
4	2	"ZERO"	0
4	3		0
4	4		0
4	7		0
5	0	MASK	$\overline{A} \wedge Q$
5	1		$\overline{A} \wedge B$
5	5		$\overline{D} \wedge A$
5	6		$\overline{D} \wedge Q$

ALU ARITHMETIC MODE FUNCTIONS

OCTAL $I_{5,4,3}$	OCTAL $I_{2,1,0}$	C_n = L GROUP	C_n = L FUNCTION	C_n = H GROUP	C_n = H FUNCTION
0	0	ADD	A + Q	ADD plus one	A + Q + 1
0	1		A + B		A + B + 1
0	5		D + A		D + A + 1
0	6		D + Q		D + Q + 1
0	2	PASS	Q	Increment	Q + 1
0	3		B		B + 1
0	4		A		A + 1
0	7		D		D + 1
1	2	Decrement	Q - 1	PASS	Q
1	3		B - 1		B
1	4		A - 1		A
2	7		D - 1		D
2	2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2	3		-B - 1		-B
2	4		-A - 1		-A
1	7		-D - 1		-D
1	0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1	1		B - A - 1		B - A
1	5		A - D - 1		A - D
1	6		Q - D - 1		Q - D
2	0		A - Q - 1		A - Q
2	1		A - B - 1		A - B
2	5		D - A - 1		D - A
2	6		D - Q - 1		D - Q

DEFINITIONS

$P_0 = R_0 + S_0$
$P_1 = R_1 + S_1$
$P_2 = R_2 + S_2$
$P_3 = R_3 + S_3$
$G_0 = R_0 S_0$
$G_1 = R_1 S_1$
$G_2 = R_2 S_2$
$G_3 = R_3 S_3$
$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_n$
$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$

+ = OR

LOGIC FUNCTIONS FOR $\overline{G}$, $\overline{P}$, C_{n+4} AND OVR

$I_{5,4,3}$	FUNCTION	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3 P_2 P_1 P_0}$	$\overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0}$	C_4	$C_3 \forall C_4$
1	S - R	← Same as R + S equations, but substitute $\overline{R}_I$ for R_I in definitions →			
2	R - S	← Same as R + S equations, but substitute $\overline{S}_I$ for S_I in definitions →			
3	R V S	LOW	$P_3 P_2 P_1 P_0$	$\overline{P_3 P_2 P_1 P_0} + C_n$	$\overline{P_3 P_2 P_1 P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R}$ ∧ S	LOW	← Same as R V S equation, but substitute $\overline{R}_I$ for R_I in definitions →		
6	$R \forall S$	← Same as $\overline{R \vee S}$ equation, but substitute $\overline{R}_I$ for R_I in definitions →			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 P_0$	$\overline{G_3 + P_3 G_2 + P_3 P_2 G_1}$ $+ P_3 P_2 P_1 P_0 (G_0 + \overline{C}_n)$	See Note 2

NOTES:
1. + = OR
2. $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$

8

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.[2]	MAX.	UNIT
I_{IH}	Input HIGH Current (All Inputs)	V_{CC} = Max. V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current (All Inputs)	V_{CC} = Max. V_{IN} = GND		–	-0.1	-5	µA
V_{OH}	Output High Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -1.0mA (MIL.)	2.4	4.3	–	V
			I_{OH} = -1.6mA (COM'L.)	2.4	4.3	–	
V_{OL}	Output Low Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA (MIL.)	–	0.3	0.5	V
			I_{OL} = 20mA (COM'L.)	–	0.3	0.5	
V_{IH}	Input High Voltage	Guaranteed Logic HIGH Level [1]		2.0	–	–	V
V_{IL}	Input Low Voltage	Guaranteed Logic LOW Level [1]		–	–	0.8	V
I_{OZ}	Output Leakage Current	V_{CC} = Max.	V_{OUT} = 0	–	-0.1	-10	µA
			V_{OUT} = V_{CC}(Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min. V_{OUT} = 0V[2]		-30	–	–	mA

NOTES:

1. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
2. Not more than one output should be shorted at a time. Duration of the short circuit test shall not exceed one second.
3. V_{CC} = 5.0V @ T_A +25°C

DC ELECTRICAL CHARACTERISTICS (Cont'd)

$T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (Commercial)
$T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (Military)
$V_{LC} = 0.2V$
$V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)			MIN.	TYP.(3)	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = H			–	0.5	5.0	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = L			–	0.5	5.0	mA
I_{CCT}	Quiescent Input Power Supply (4) Current (per Input @ TTL High)	V_{CC} = Max., V_{IH} = 3.4V, f_{CP} = 0			–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L		MIL.	–	1.5	2.5	mA/ MHz
				COM'L.	–	1.0	2.0	
I_{CC}	Total Power Supply Current(5)	V_{CC} = Max., Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ 50% Data Duty Cycle	IDT39C01C	MIL.	–	–	30	mA
			f_{CP} = 10MHz	COM'L.	–	–	25	
			IDT39C01D	MIL.	–	–	35	
			f_{CP} = 15MHz	COM'L.	–	–	30	
			IDT39C01E	MIL.	–	–	40	
			f_{CP} = 17.5MHz	COM'L.	–	–	35	
		V_{CC} = Max., Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V 50% Data Duty Cycle	IDT39C01C	MIL.	–	–	35	
			f_{CP} = 10MHz	COM'L.	–	–	30	
			IDT39C01D	MIL.	–	–	40	
			f_{CP} = 15MHz	COM'L.	–	–	35	
			IDT39C01E	MIL.	–	–	45	
			f_{CP} = 17.5MHz	COM'L.	–	–	40	

NOTES:

4. I_{CCQT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
5. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock Input Frequency

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large V_{CC} current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

IDT39C01C
AC ELECTRICAL CHARACTERISTICS
(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01C over the -55°C to +125°C and 0°C to +70°C temperature range. V_{CC} is specified at 5V ±10% for military temperature range and 5V ±5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

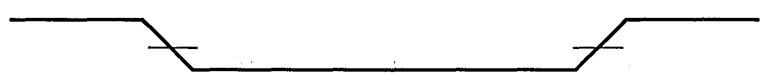
	MIL.	COM'L.	UNIT
Read-Modify-Write Cycle (from selection of A, B, registers to end of cycle)	32	31	ns
Maximum Clock Frequency to to shift Q (50% duty cycle, I = 432 or 632)	31	32	MHz
Minimum Clock LOW Time	15	15	ns
Minimum Clock HIGH Time	15	15	ns
Minimum Clock Period	32	31	ns

COMBINATIONAL PROPAGATION DELAYS[1] C_L = 50pF

	TO OUTPUT																
FROM INPUT	Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	48	40	48	40	48	40	44	37	48	40	48	40	48	40	–	–	ns
D	37	30	37	30	37	30	34	30	40	38	37	30	37	30	–	–	ns
C_n	25	22	25	22	21	20	–	–	28	25	25	22	28	25	–	–	ns
$I_{0,1,2}$	40	35	40	35	40	35	44	37	44	37	40	35	40	35	–	–	ns
$I_{3,4,5}$	40	35	40	35	40	35	40	35	40	38	40	35	40	35	–	–	ns
$I_{6,7,8}$	29	25	–	–	–	–	–	–	–	–	–	–	29	26	29	26	ns
A Bypass ALU (I = 2XX)	40	35	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock	40	35	40	35	40	35	40	35	40	35	40	35	40	35	33	28	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP:



INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Source Address	15	15	2	1[3]	30, 15 + TPWL[4]		2	1	ns
B Destination Address	15	15	Do not change [2]				2	1	ns
D	– [1]	–	–	–	25	25	0	0	ns
C_n	–	–	–	–	20	20	0	0	ns
$I_{0,1,2}$	–	–	–	–	30	30	0	0	ns
$I_{3,4,5}$	–	–	–	–	30	30	0	0	ns
$I_{6,7,8}$	10	10	Do not change [2]				0	0	ns
$RAM_{0,3}$, $Q_{0,3}$	–	–	–	–	12	12	0	0	ns

OUTPUT ENABLE/DISABLE TIMES
(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
$\overline{OE}$	Y	25	23	25	23

NOTES:
1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.

IDT39C01D
AC ELECTRICAL CHARACTERISTICS
(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01D over the -55°C to +125°C and 0°C to +70°C temperature range. V_{CC} is specified at 5V ±10% for military temperature range and 5V ±5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNIT
Read-Modify-Write Cycle (from selection of A, B, registers to end of cycle)	27	23	ns
Maximum Clock Frequency to to shift Q (50% duty cycle, I = 432 or 632)	37	43	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period	27	23	ns

COMBINATIONAL PROPAGATION DELAYS[1] C_L = 50pF

FROM INPUT	TO OUTPUT: Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	33	30	33	30	33	30	33	28	33	30	33	30	33	30	–	–	ns
D	24	21	23	20	23	20	21	20	25	24	24	21	25	22	–	–	ns
C_n	18	17	17	16	14	14	–	–	19	18	17	16	19	18	–	–	ns
$I_{0,1,2}$	28	26	27	25	26	24	28	24	29	25	27	24	27	25	–	–	ns
$I_{3,4,5}$	27	26	27	24	26	24	26	24	27	26	26	24	27	26	–	–	ns
$I_{6,7,8}$	18	16	–	–	–	–	–	–	–	–	–	–	21	21	21	21	ns
A Bypass ALU (I = 2XX)	26	24	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ⟋	27	24	26	23	26	23	25	23	27	24	26	24	27	24	20	19	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP:


INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Source Address	11	10	0	0[3]	24, 11 + TPWL[4]	21, 10 + TPWL[4]	2	1	ns
B Destination Address	11	10	Do not change[2]				2	1	ns
D	–[1]	–	–	–	16	16	0	0	ns
C_n	–	–	–	–	13	13	0	0	ns
$I_{0,1,2}$	–	–	–	–	19	19	0	0	ns
$I_{3,4,5}$	–	–	–	–	19	19	0	0	ns
$I_{6,7,8}$	7	7	Do not change[2]				0	0	ns
$RAM_{0,3}$, $Q_{0,3}$	–	–	–	–	9	9	0	0	ns

OUTPUT ENABLE/DISABLE TIMES
(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
$\overline{OE}$	Y	16	14	18	16

NOTES:
1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.

IDT39C01E
AC ELECTRICAL CHARACTERISTICS
(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01E over the -55°C to +125°C and 0°C to +70°C temperature range. V_{CC} is specified at 5V ±10% for military temperature range and 5V ±5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNIT
Read-Modify-Write Cycle (from selection of A, B, registers to end of cycle)	21	20	ns
Maximum Clock Frequency to to shift Q (50% duty cycle, I = 432 or 632)	46	50	MHz
Minimum Clock LOW Time	10	8	ns
Minimum Clock HIGH Time	10	8	ns
Minimum Clock Period	21	20	ns

COMBINATIONAL PROPAGATION DELAYS(1) C_L = 50pF

	TO OUTPUT																
FROM INPUT	Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	26	22	26	22	26	22	26	21	26	22	26	22	26	22	–	–	ns
D	18	16	17	15	17	15	16	15	19	18	18	16	19	16	–	–	ns
C_n	13	13	13	12	10	10	–	–	14	13	13	12	14	13	–	–	ns
$I_{0,1,2}$	21	20	20	19	19	18	21	18	22	19	20	18	20	19	–	–	ns
$I_{3,4,5}$	20	20	20	18	19	18	19	18	20	20	19	18	20	20	–	–	ns
$I_{6,7,8}$	13	12	–	–	–	–	–	–	–	–	–	–	16	16	16	16	ns
A Bypass ALU (I = 2XX)	19	18	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ⎍	20	18	19	17	19	17	19	17	20	18	19	18	20	18	15	15	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Source Address	8	7	0	0(3)	18, 8 + TPWL (4)	15, 7 + TPWL (4)	2	1	ns
B Destination Address	8	7	Do not change (2)				2	1	ns
D	– (1)	–	–	–	12	12	0	0	ns
C_n	–	–	–	–	10	10	0	0	ns
$I_{0,1,2}$	–	–	–	–	14	14	0	0	ns
$I_{3,4,5}$	–	–	–	–	14	14	0	0	ns
$I_{6,7,8}$	5	5	Do not change (2)				0	0	ns
$RAM_{0,3}$, $Q_{0,3}$	–	–	–	–	9	9	0	0	ns

OUTPUT ENABLE/DISABLE TIMES
(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
$\overline{OE}$	Y	14	10	12	12

NOTES:
1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 4

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

INPUT/OUTPUT INTERFACE CIRCUIT

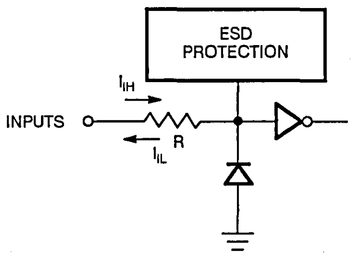


Figure 1. Input Structure (All Inputs)

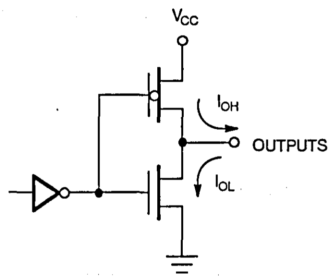


Figure 2. Output Structure (All Outputs Except F = 0)

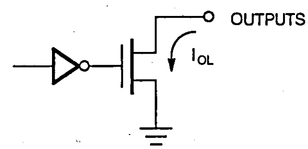
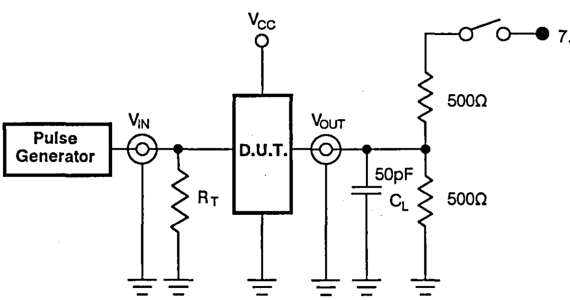


Figure 3. Output Structure (F = 0 Only)

TEST LOAD CIRCUIT



TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All other Outputs	Open

DEFINITIONS
C_L = Load capacitance: includes jig and probe capacitance
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 4. Switching Test Circuits

ORDERING INFORMATION

IDT 39C01 (Device Type) X (Speed) X (Package) X (Process/Temperature Range)

Process/Temperature Range:
- BLANK — Commercial (0°C to +70°C)
- B — Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:
- P — Plastic DIP
- C — Sidebraze DIP
- D — CERDIP
- L — LCC

Speed:
- C — Four-Bit Microprocessor Slice
- D — High-Speed Four-Bit Microprocessor Slice
- E — Ultra-High-Speed Four-Bit CMOS Microprocessor Slice

Integrated Device Technology, Inc.

CMOS CARRY LOOKAHEAD GENERATOR

IDT39C02A

MICROSLICE ™ PRODUCT

FEATURES:

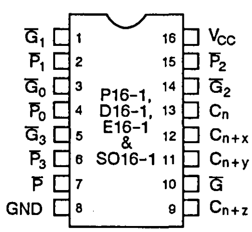
- Provides lookahead carries across any number of 4-bit microprocessor ALUs
- Very high speed and output drive over full temperature and voltage supply extremes
- 6ns typical propagation delay
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5µW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than bipolar (5µW max.)
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

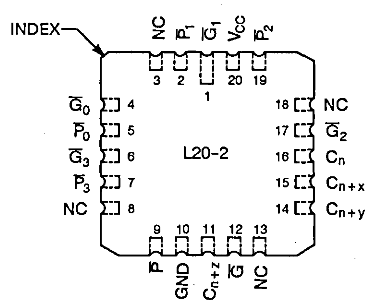
The IDT39C02A is a high-speed carry lookahead generator built using advanced CEMOS ™, a dual metal CMOS technology. The IDT39C02A is generally used with an arithmetic logic unit to provide high-speed lookahead over larger word lengths.

The IDT39C02A is a pin-compatible, performance enhanced, functional replacement for all versions of the 2902.

PIN CONFIGURATIONS

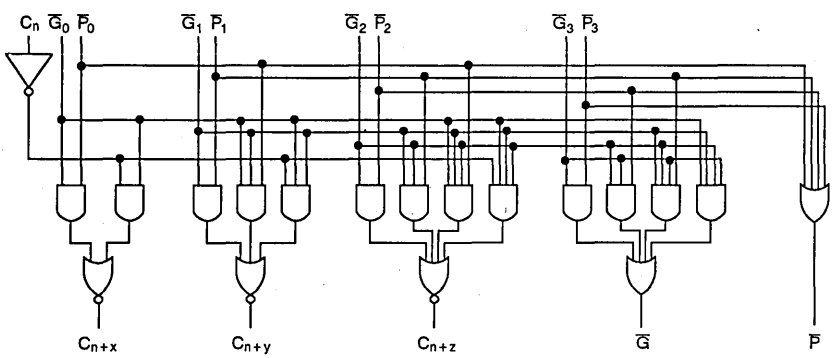


DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



MICROSLICE and CEMOS are trademarks of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	μA
I_{SC}	Short Circuit Current	V_{CC} = Max. [3]		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300μA	V_{HC}	V_{CC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	V
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		–	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4V [4]		–	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	–	0.15	–	mA/MHz
I_{CC}	Total Power Supply Current [5]	V_{CC} = Max. f = 10MHz Outputs Open 50% Duty Cycle One Input Toggling	$V_{HC} \leq V_{IN} \leq V_{LC}$	–	1.5	–	mA
			V_{IN} = 3.4V [4]	–	2.0	–	
		All Inputs	V_{IN} = 3.4V [4]	–	16.0	–	

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f \times N) + D \times N_D)$
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
C_n	Carry Input
$\overline{G}_0, \overline{G}_1, \overline{G}_2, \overline{G}_3$	Carry Generate Inputs (Active LOW)
$\overline{P}_0, \overline{P}_1, \overline{P}_2, \overline{P}_3$	Carry Propagate Inputs (Active LOW)
C_{n+x}-C_{n+z}	Carry Outputs
G	Carry Generate Output (Active LOW)
P	Carry Propagate Output (Active LOW)

TRUTH TABLE [1]

C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	G	P
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

NOTE:
1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	TYPICAL	COMMERCIAL		MILITARY		UNIT
				MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+x} C_{n+y}, C_{n+z}		6.0	3.0	14.0	3.0	16.5	ns
t_{PLH} t_{PHL}	Propagation Delay P_0, P_1, or P_2, to C_{n+x}, C_{n+y}, C_{n+z}		6.0	2.0	9.0	2.0	11.5	ns
t_{PLH} t_{PHL}	Propagation Delay G_0, G_1, or G_2 to C_{n+x}, C_{n+y}, C_{n+z}	C_L = 50pF R_L = 500Ω	6.0	2.0	9.5	2.0	11.5	ns
t_{PLH} t_{PHL}	Propagation Delay P_1, P_2 or P_3, to G		7.0	3.0	12.0	3.0	16.5	ns
t_{PLH} t_{PHL}	Propagation Delay G_n to G		7.5	3.0	12.0	3.0	16.5	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to P		6.0	2.5	11.0	2.5	12.5	ns

ORDERING INFORMATION

IDT XXXXX (Device Type) XX (Package) X (Process/Temperature Range)

Process/Temperature Range:
- BLANK — Commercial (0°C to +70°C)
- B — Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:
- P — Plastic DIP
- D — CERDIP
- SO — Small Outline IC
- E — CERPACK
- L — Leadless Chip Carrier

Device Type:
- 39C02A — Carry Lookahead Generator

Integrated Device Technology, Inc.

4-BIT CMOS MICROPROCESSOR SLICE

IDT39C03A
IDT39C03B

MICROSLICE™ PRODUCT

FEATURES:

- Fast
  - IDT39C03A matches 2903A speeds
  - IDT39C03B 20% speed upgrade
- Low-power CMOS
  - Commercial: 50mA (max.)
  - Military: 55mA (max.)
- Pin-compatible, performance enhanced functional replacement for the 2903A
- Cascadable to 8, 12, 16, etc. bits
- Expandable Register File
- On-chip Parity Generation and Sign Extension Logic
  - Provide parity across the entire ALU output and sign extension at any slice boundary
- On-chip Normalized Logic
  - Floating-point mantissa and exponent easily developed using single microcycle per shift
- On-chip multiplication and division logic
  - Executes unsigned and two's complement multiplication along with last cycle of two's complement multiplication
- Packaged in 48-pin plastic and ceramic DIPs and 52-pin LCC
- Military product available compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT39C03s are four-bit expandable CMOS microprocessor slices. While executing the identical functions associated with the high-speed IDT39C01 series of 4-bit slices, the IDT39C03s also provide additional enhancements for use in arithmetic-oriented processors.

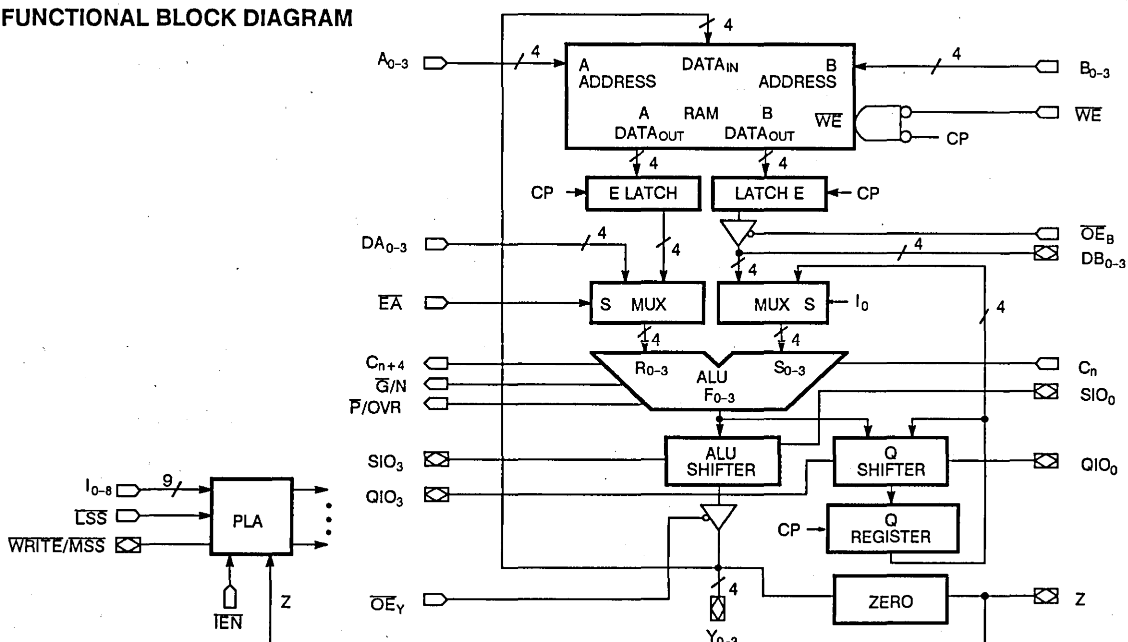
These extremely low-power yet high-speed microprocessors consist of a 16-word by 4-bit dual-port RAM, a multidirectional three-port architecture, 16 logic operation ALU and the necessary shifting, decoding and multiplexing logic. Compatible 2903A arithmetic and logic instructions, including the special multiplication, division and normalized instructions, are available on the IDT39C03s. Both are easily expandable in 4-bit increments.

Both devices are pin-compatible, functional-replacements for the 2903A. The fastest version, the IDT39C03B, is a 20% speed upgrade from the normal 2903A device. The IDT39C03A meets the 2903A speeds.

The IDT39C03s are fabricated using CEMOS™, a CMOS technology designed for high-performance and high-reliability.

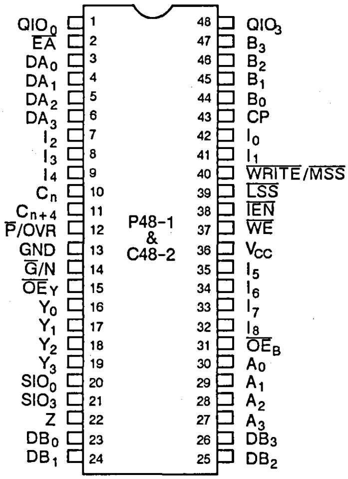
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications.

FUNCTIONAL BLOCK DIAGRAM

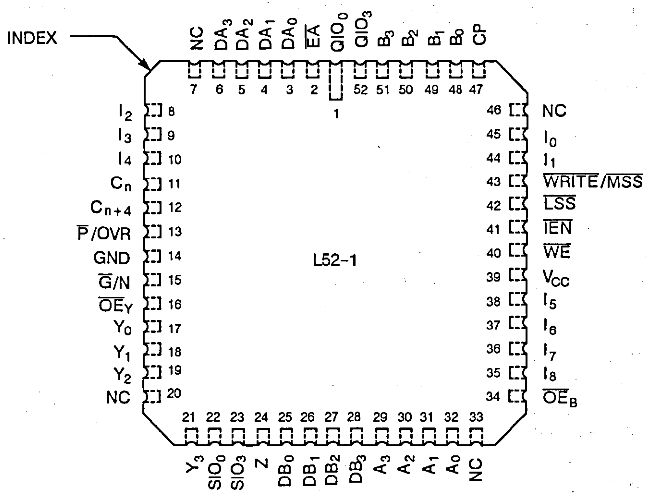


CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_{0-3}	I	RAM A Address Inputs (TTL Input) — Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.
B_{0-3}	I	RAM B Address Inputs (TTL Input) — Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are LOW.
$\overline{WE}$	I	Write Enable Input (TTL Input) — The RAM write enable input. If $\overline{WE}$ is LOW, data at the Y I/O port is written into the RAM when the CP input is LOW. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.
DA_{0-3}	I	External Data Inputs (TTL Input) — A 4-bit external data input which can be selected as one of the IDT39C03 ALU operand sources; DA_0 is the least significant bit.
$\overline{EA}$	I	Control Input (TTL Input) — A control input which, when HIGH, selects DA_{0-3} as the ALU R operand and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-3} output data.
DB_{0-3}	I/O	External Data Inputs/Outputs (Three-State Input/Output) — A four-bit external data input/output. Under control of the $\overline{OE}_B$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.
$\overline{OE}_B$	I	Control Input (TTL Input) — A control input which, when LOW, enables RAM output B onto the DB_{0-3} lines and, when HIGH, disables the RAM output B tri-state buffers.
C_n	I	Carry-in Input (TTL Input) — The carry-in input to the IDT39C03 ALU.
I_{0-8}	I	Instruction Inputs (TTL Input) — The nine instruction inputs used to select the IDT39C03 operation to be performed.
$\overline{IEN}$	I	Instruction Enable Input (TTL Input) — The instruction enable input which, when LOW, allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is HIGH, the Q Register and Sign Compare flip-flop are in the hold mode. On the IDT39C03, $\overline{IEN}$ also controls $\overline{WRITE}$.
C_{n+4}	O	Carry-Out Output (TTL Input) — This output generally indicates the carry-out of the IDT39C03 ALU. Refer to Table 5 for an exact definition of this pin.
$\overline{G}$/N	O	Carry-Generate Output (TTL Output) — A multi-purpose pin which indicates the carry generate, $\overline{G}$ function, at the least significant and intermediate slices and generally indicates the sign N of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.
$\overline{P}$/OVR	O	Carry Propagate Output (TTL Output) — A multi-purpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.
Z	I/O	Open-Drain I/O Pin (Open-Drain Input/Output) — An open-drain input/output pin which, when HIGH, generally indicates the outputs are all LOW. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.
SIO_0, SIO_3	I/O	Bidirectional Serial Shift I/Os for the ALU (Three-State Input/Output) — Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO_0 is an input and SIO_3 an output. During a shift-down operation, SIO_3 is an input and SIO_0 is an output. Refer to Tables 3 and 4 for an exact definition of these pins.
QIO_0, QIO_3	I/O	Bidirectional Serial Shift I/Os for the Q Shifter (Three-State Input/Output) — Bidirectional serial shift inputs/outputs for the Q Shifter shifter which operate line SIO_0 and SIO_3. Refer to Tables 3 and 4 for an exact definition of these pins.
$\overline{LSS}$	I	Control Input (TTL Input) — An input pin which, when tied LOW, programs the chip to act as the least significant slice (LSS) of an IDT39C03 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE}/\overline{MSS}$ pin. When $\overline{LSS}$ is tied HIGH, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{WRITE}$ output buffer is disabled.
$\overline{WRITE}/\overline{MSS}$	I/O	Control Input (Three-State Input/Output) — When $\overline{LSS}$ is tied LOW, the $\overline{WRITE}$ output signal appears at this pin; the $\overline{WRITE}$ signal is LOW when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied HIGH, $\overline{WRITE}/\overline{MSS}$ is an input pin; tying it HIGH programs the chip to operate as an intermediate slice (IS) and tying it LOW programs the chip to operate as the most significant slice (MSS).
Y_{0-3}	I/O	Data Inputs/Outputs (Three-State Input/Output) — Four data inputs/outputs of the IDT39C03. Under control of the $\overline{OE}_Y$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.
$\overline{OE}_Y$	I	Control Input (TTL Input) — A control input which, when LOW, enables the ALU shifter output data onto the Y_{0-3} lines and, when HIGH, disables the Y_{0-3} three-state output buffers.
CP	I	Clock Input (TTL Input) — The clock input to the IDT39C03. The Q Register and Sign Compare flip-flop are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$, data is written in the RAM when CP is LOW.

ARCHITECTURE OF THE IDT39C03

The IDT39C03s are high-performance, cascadable, 4-bit microprocessor slices used in CPUs, peripheral controllers, microprogrammable machines and in a number of other applications. The functional blocks consist of the following:

- 16-word-by-4-bit dual-port RAM
- high-speed ALU and shifter
- Q register with shifter input
- 9-bit instruction decoder

DUAL-PORT RAM

Both the A and B ports of the dual-port RAM can be addressed and read simultaneously at the respective RAM A and B output ports. If both ports address the same memory location, identical data will be read from both the A and B port. The latches at the RAM output ports are transparent when the clock input, CP, is HIGH and holds the RAM output data when CP is LOW. RAM data is read at the DB (I/O) port under control of the $\overline{OE}_B$ three-state output enable.

External data can be written directly into the RAM from the Y I/O port, or the ALU shifter output data can be enabled onto the Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is LOW and the clock input, CP, is LOW.

ALU

The IDT39C03s perform seven arithmetic operations and nine logic operations on two 4-bit operands. Various pairs of ALU source operands are easily selected via the ALU multiplexer inputs. The $\overline{EA}$ input selects either the DA external data input or RAM output port A for use as one ALU operand. The $\overline{OE}_B$ and I_0 inputs select RAM output port B, DB external data input or the Q register content for use as the second ALU source operand. During certain ALU operations, zeros are forced at the ALU operand inputs. Thus, the IDT39C03s are capable of operating on data from two external sources, from an internal and external source, or from two internal sources. Table 1 indicates all the possible pairs of ALU source operands as a function of the $\overline{EA}$, $\overline{OE}_B$ and I_0 inputs.

With instruction bits I_4, I_3, I_2, I_1 and I_0 LOW, the IDT39C03s execute special functions which have been defined in Table 4. When the IDT39C03s execute instructions other than the nine special instructions, the ALU operation is defined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the ALU operation as a function of these four instruction bits.

Cascading the IDT39C03s, in either the carry lookahead or ripple carry approach, is very simple. In a cascaded configuration, each slice must be properly programmed to Most Significant Slice (MSS), Intermediate Slice (IS) or Least Significant Slice (LSS). The IDT39C03s incorporate the carry generate ($\overline{G}$) and carry propagate ($\overline{P}$) signals necessary for cascading.

TABLE 1.
ALU OPERAND SOURCES[1]

$\overline{EA}$	I_0	$\overline{OE}$	ALU OPERAND R	ALU OPERAND S
L	L	L	RAM Output A	RAM Output B
L	L	H	RAM Output A	DB_{0-3}
L	H	X	RAM Output A	Q Register
H	L	L	DA_{0-3}	RAM Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

NOTE:
1. L = LOW, H = HIGH, X = Don't Care

TABLE 2.
IDT39C03 ALU FUNCTIONS[1]

I_4	I_3	I_2	I_1	HEX CODE	ALU FUNCTIONS	
L	L	L	L	0	I_0 = L	Special Functions
					I_0 = H	F_i = HIGH
L	L	L	H	1	F = S Minus R Minus 1 Plus C_n	
L	L	H	L	2	F = R Minus S Minus 1 Plus C_n	
L	L	H	H	3	F = R Plus S Plus C_n	
L	H	L	L	4	F = S Plus C_n	
L	H	L	H	5	F = $\overline{S}$ Plus C_n	
L	H	H	L	6	F = R Plus C_n	
L	H	H	H	7	F = $\overline{R}$ Plus C_n	
H	L	L	L	8	F_i = LOW	
H	L	L	H	9	F_i = $\overline{R}_i$ AND S_i	
H	L	H	L	A	F_i = R_i EXCLUSIVE NOR S_i	
H	L	H	H	B	F_i = R_i EXCLUSIVE OR S_i	
H	H	L	L	C	F_i = R_i AND S_i	
H	H	L	H	D	F_i = R_i NOR S_i	
H	H	H	L	E	F_i = R_i NAND S_i	
H	H	H	H	F	F_i = R_i OR S_i	

NOTE:
1. L = LOW, H = HIGH, i = 0 to 3

Also generated is a carry-out signal, C_{n+4}, which is generally available as an output of each slice. Both the carry-in (C_n) and carry-out (C_{n+4}) signals are active HIGH. The ALU generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multipurpose $\overline{G}$/N and $\overline{P}$/OVR outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. Refer to Table 5 for the exact definition of these four signals.

ALU SHIFTER

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F) or shifts it down one position (F/2). Both arithmetic and logical shift operations are possible. The arithmetic shift operation shifts data around the most significant (sign) bit position of the MSS and a logical shift operation shifts data through this bit position (see Figure 1). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation SIO_3 is generally a serial shift input and SIO_0 a serial shift output. For exact definition of the SIO_0 and SIO_3 operation, refer to Tables 3 and 4.

Also provided in the ALU shifter is sign extension at the slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, Y_3, and propagated to the SIO_3 output.

Providing ALU error detection, the IDT39C03s ALU shifter contains a cascadable, five-bit parity generator/checker. Parity for the F_0, F_1, F_2, F_3, ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output.

The operation of the ALU shifter is defined by the instruction inputs. Specified in Table 4 are the special functions and the operations the ALU shifter performs. When the IDT39C03s execute instructions other than special functions,the ALU shifter operation is determined by instruction bits I_8, I_7, I_6 and I_5. How these four bits operate with the ALU shifter is defined in Table 3.

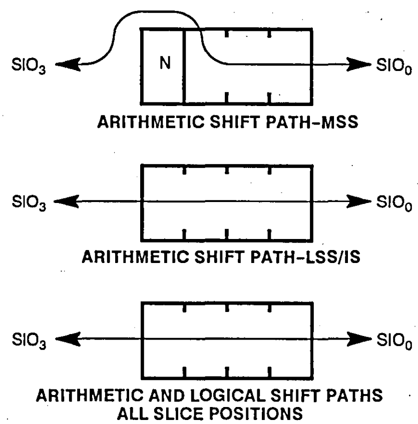


Figure 1.

Q REGISTER

The Q Register is an auxiliary 4-bit register which is clocked on the LOW-to-HIGH transition of the CP input. It is intended primarily for use in multiplication and division operations; however, it can also be used as an accumulator or holding register for some applications. The F output of the ALU can be loaded into the Q Register and/or the Q Register can be selected as the source for the ALU S operand. The shifter at the input to the Q Register can shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. Both QIO_0 and QIO_3 are bidirectional shift serial inputs/outputs. During a Q Register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift input and QIO_0 is a serial shift output.

The IDT39C03s provide the capability of double-length arithmetic and logical shifting. To perform the double-length shift, QIO_3 of the MSS is connected to SIO_0 of the LSB and executing an instruction which shifts both the ALU output and the Q Register.

The instruction inputs also control the Q Register and shifter, as shown in Table 4. When executing instructions other than the special functions, the Q Register and shifter operation is controlled by instruction bits I_8, I_7, I_6 and I_5, as shown in Table 3.

OUTPUT BUFFERS

Both the DB and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls. The Y output buffers are enabled when the $\overline{OE}_Y$ is LOW and are in the High Z state when $\overline{OE}_Y$ is HIGH. The DB output buffers are enabled when the $\overline{OE}_B$ input is LOW. The zero, Z pin, is an open drain I/O that can be wire-Ored between slices. As an output it can be used as a zero detect status flag and generally indicates that the Y_{0-3} pins are all LOW. Table 5 defines the exact signal functions.

INSTRUCTION DECODER

The Instruction Decoder generates the required internal control signals relative to the nine instruction inputs, I_{0-8}, the Instruction Enable input, $\overline{\text{IEN}}$, the $\overline{\text{LSS}}$ input and the $\overline{\text{WRITE}}$/MSS input/output.

When an instruction which writes data into the RAM is being performed, the $\overline{\text{WRITE}}$ output is LOW. Reference Tables 3 and 4 for proper pin operation. When $\overline{\text{IEN}}$ is HIGH, the $\overline{\text{WRITE}}$ output is forced HIGH and the Q Register and Sign Compare Flip-Flop contents are preserved. When $\overline{\text{IEN}}$ is LOW, the $\overline{\text{WRITE}}$ output is enabled and the Q Register and Sign Compare Flip-Flop can be written according to the IDT39C03s instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during a divide operation. See Figure 2.

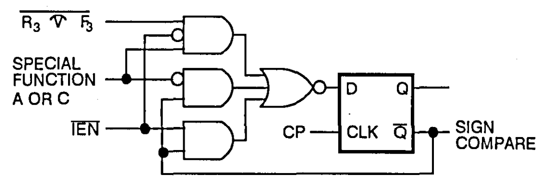


Figure 2. Sign Compare Flip-Flop

SLICE POSITION PROGRAMMING

When the $\overline{\text{LSS}}$ input is LOW, the device becomes the Least Significant Slice and enables the $\overline{\text{WRITE}}$ output signal onto the $\overline{\text{WRITE}}$/MSS bidirectional I/O pin. When the $\overline{\text{LSS}}$ input is HIGH, the $\overline{\text{WRITE}}$/MSS pin becomes an input which when HIGH programs the slice to operate as an Intermediate Slice (IS). Connecting it LOW programs the slice to operate as a Most Significant Slice (MSS). The $\overline{\text{WRITE}}$/MSS pin must be tied HIGH via a pull-up resistor. $\overline{\text{WRITE}}$/MSS and $\overline{\text{LSS}}$ should not be connected together.

SPECIAL FUNCTIONS

Nine special functions are provided on the IDT39C03s which make possible the implementation of the following operations:

- Single and Double Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation by One or Two

Adjusting a single-precision or double-precision floating-point number in order to bring its mantissa within a specified range can be performed using the single-length and double-length normalization operations. These special functions can be used to perform a two's complement, non-restoring divide operation. They provide single and double-precision divide operations and can be performed in "n" clock cycles (where "n" is the number of bits in the quotient). The unsigned multiply special function and the two two's complement multiply special functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in "n" clock cycles. During the last cycle of the two's complement multiplication, a conditional subtraction (rather than addition) is performed due to the fact that the sign bit of the multiplier carries negative weight.

The sign/magnitude-two's complement special function can be used to convert number representation systems. A number expressed in sign/magnitude representation can be converted to the two's complement representation, and vice-versa, in one clock cycle.

Incrementing an unsigned or two's complement number by one or two is easily accomplished using the increment by one or two special function.

TABLE 3. ALU DESTINATION CONTROL FOR I_0 OR I_1 OR I_2 OR I_3 = HIGH, $\overline{IEN}$ = LOW

I_8	I_7	I_6	I_5	HEX CODE	ALU SHIFTER FUNCTION	SIO_3		Y_3		Y_2		Y_1	Y_0	SIO_0	$\overline{WRITE}$	Q REG & SHIFTER FUNCTION	QIO_3	QIO_0
						MOST SIG. SLICE	OTHER SLICES	MOST SIG. SLICE	OTHER SLICES	MOST SIG. SLICE	OTHER SLICES							
L	L	L	L	0	Arith. F/2 → Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Z	Z
L	L	L	H	1	Log. F/2 → Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Z	Z
L	L	H	L	2	Arith. F/2 → Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log. Q/2 → Q	Input	Q_0
L	L	H	H	3	Log. F/2 → Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log. Q/2 → Q	Input	Q_0
L	H	L	L	4	F → Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	Hold	Z	Z
L	H	L	H	5	F → Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	Log. Q/2 → Q	Input	Q_0
L	H	H	L	6	F → Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	F → Q	Z	Z
L	H	H	H	7	F → Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	F → Q	Z	Z
H	L	L	L	8	Arith. 2F → Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Z	Z
H	L	L	H	9	Log. 2F → Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Z	Z
H	L	H	L	A	Arith. 2F → Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q → Q	Q_3	Input
H	L	H	H	B	Log. 2F → Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q → Q	Q_3	Input
H	H	L	L	C	F → Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	H	Hold	Z	Z
H	H	L	H	D	F → Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	H	Log. 2Q → Q	Q_3	Input
H	H	H	L	E	SIO_0 → Y_0, Y_1, Y_2, Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Z	Z
H	H	H	H	F	F → Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	L	Hold	Z	Z

NOTE:
1. Parity = $F_3 \forall F_2 \forall F_1 \forall F_0 \forall SIO_3$, L = LOW Z = High Impedance $\forall$ = Exclusive OR, H = HIGH

8

TABLE 4. SPECIAL FUNCTIONS FOR $I_4 = I_3 = I_2 = I_1 = I_0$ LOW [(4)]

(HEX) $I_8 I_7 I_6 I_5$	SPECIAL FUNCTION	ALU FUNCTION	ALU SHIFTER FUNCTION	SIO_3		SIO_0	Q REGISTER & SHIFTER FUNCTION	QIO_3	QIO_0	$\overline{WRITE}$
				MSS	OTHER SLICES					
0	Unsigned Multiply	$F=S+C_n$ if $Z=L$ $F=R+S+C_n$ if $Z=H$	Log $F/2 \rightarrow Y$ (1)	Z	Input	F_0	Log $Q/2 \rightarrow Q$	Input	Q_0	L
1	(5)									
2	Two's Complement Multiply	$F=S+C_n$ if $Z=L$ $F=R+S+C_n$ if $Z=H$	Log $F/2 \rightarrow Y$ (2)	Z	Input	F_0	Log $Q/2 \rightarrow Q$	Input	Q_0	L
3	(5)									
4	Increment by One or Two	$F=S+1+C_n$	$F \rightarrow Y$	Input	Input	Parity	Hold	Z	Z	L
5	Sign/Magnitude Two's Complement	$F=S+C_n$ if $Z=L$ $F=\overline{S}+C_n$ if $Z=H$	$F \rightarrow Y$(3)	Input	Input	Parity	Hold	Z	Z	L
6	Two's Complement Multiply Last Cycle	$F=S+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	Log $F/2 \rightarrow Y$ (2)	Z	Input	F_0	Log $Q/2 \rightarrow Q$	Input	Q_0	L
7	(5)									
8	Single Length Normalize	$F=S+C_n$	$F \rightarrow Y$	F_3	F_3	Z	Log $2Q \rightarrow Q$	Q_3	Input	L
9	(5)									
A	Double Length Normalize and First Divide Op	$F=S+C_n$	Log $2F \rightarrow Y$	$R_3 \forall F_3$	F_3	Input	Log $2Q \rightarrow Q$	Q_3	Input	L
B	(5)									
C	Two's Complement Divide	$F=S+R+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	Log $2F \rightarrow Y$	$\overline{R_3 \forall F_3}$	F_3	Input	Log $2Q \rightarrow Q$	Q_3	Input	L
D	(5)									
E	Two's Complement Divide Correction and Remainder	$F=S+R+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	$F \rightarrow Y$	F_3	F_3	Z	Log $2Q \rightarrow Q$	Q_3	Input	L
F	(5)									

NOTES:
1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the most significant slice only, $F_3 \forall$ OVR is internally gated to the Y_3 output.
3. At the most significant slice only, $S_3 \forall F_3$ is generated the Y_3 output.
4. The Q Register cannot be used explicitly as an operand for any Special Functions. It is defined implicitly within the functions.
5. Not Valid
6. L = LOW, H = HIGH, X = Don't Care, Z = High Impedance, $\forall$ = Exclusive OR, PARITY = $SIO_3 \forall F_3 \forall F_2 \forall F_1 \forall F_0$

TABLE 5. IDT39C03A STATUS OUTPUTS

(HEX) I_{8-5}	(HEX) I_{4-1}	I_0	G_I (I=0 to 3)	P_I (I=0 to 3)	C_{n+4}	$\overline{P}$/OVR MOST SIG. SLICE	$\overline{P}$/OVR OTHER SLICES	$\overline{G}$/N MOST SIG. SLICE	$\overline{G}$/N OTHER SLICES	Z ($\overline{OEY}$ = L) MOST SIG. SLICE	Z ($\overline{OEY}$ = L) INTER-MEDIATE SLICE	Z ($\overline{OEY}$ = L) LEAST SIG. SLICE
X	0	H	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	1	X	$\overline{R}_I \wedge S_I$	$\overline{R}_I \vee S_I$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	2	X	$R_I \wedge \overline{S}_I$	$R_I \vee \overline{S}_I$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	3	X	$R_I \wedge S_I$	$R_I \vee S_I$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	4	X	0	S_I	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	5	X	0	$\overline{S}_I$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	6	X	0	R_I	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	7	X	0	$\overline{R}_I$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	8	X	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	9	X	$\overline{R}_I \wedge S_I$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	A	X	$R_I \wedge S_I$	$R_I \vee S_I$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	B	X	$\overline{R}_I \wedge S_I$	$R_I \vee S_I$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	C	X	$R_I \wedge S_I$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	D	X	$\overline{R}_I \wedge \overline{S}_I$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	E	X	$R_I \wedge S_I$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	F	X	$\overline{R}_I \wedge \overline{S}_I$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
0	0	L	0 if Z=L $R_I \wedge S_I$ if Z=H	S_I if Z=L $R_I \vee S_I$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
1	0	L	(Note 6)	–	–	–	–	–	–	–	–	–
1	8	L	(Note 6)	–	–	–	–	–	–	–	–	–
2	0	L	0 if Z=L $R_I \wedge S_I$ if Z=H	S_I if Z=L $R_I \vee S_I$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
3	0	L	(Note 6)	–	–	–	–	–	–	–	–	–
4	0	L	(Note 1)	(Note 2)	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
5	0	L	0	S_I if Z=L S_I if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3 if Z=L $F_3 \forall S_3$ if Z=H	$\overline{G}$	S_3	Input	Input
6	0	L	0 if Z=L $\overline{R}_I \wedge S_I$ if Z=H	S_I if Z=L $\overline{R}_I \vee S_I$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
7	0	L	(Note 6)	–	–	–	–	–	–	–	–	–
8	0	L	0	S_I	(Note 3)	$Q_2 \forall Q_1$	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
9	0	L	(Note 6)	–	–	–	–	–	–	–	–	–
9	8	L	(Note 6)	–	–	–	–	–	–	–	–	–
A	0	L	0	S_I	(Note 4)	$F_2 \forall F_1$	$\overline{P}$	F_3	$\overline{G}$	(Note 5)	(Note 5)	(Note 5)
B	0	L	(Note 6)	–	–	–	–	–	–	–	–	–
C	0	L	$R_I \wedge S_I$ if Z=L $\overline{R}_I \wedge S_I$ if Z=H	$R_I \vee S_I$ if Z=L $\overline{R}_I \vee S_I$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
D	0	L	(Note 6)	–	–	–	–	–	–	–	–	–
E	0	L	$R_I \wedge S_I$ if Z=L $\overline{R}_I \wedge S_I$ Z=H	$R_I \vee S_I$ if Z=L $\overline{R}_I \vee S_I$ Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
F	0	L	(Note 6)	–	–	–	–	–	–	–	–	–

Continued next page

NOTES:
1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$.
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $P_I = S_I$.
3. At the most significant slice, $C_{n+4} = Q_3 \forall Q_2$. At other slices $C_{n+4} = G \vee PC_n$.
4. At the most significant slice, $C_{n+4}' = F_3 \forall F_2$. At other slices $C_{n+4} = G \vee PC_n$.
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\,\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$.

8

NOTES (Cont'd.):

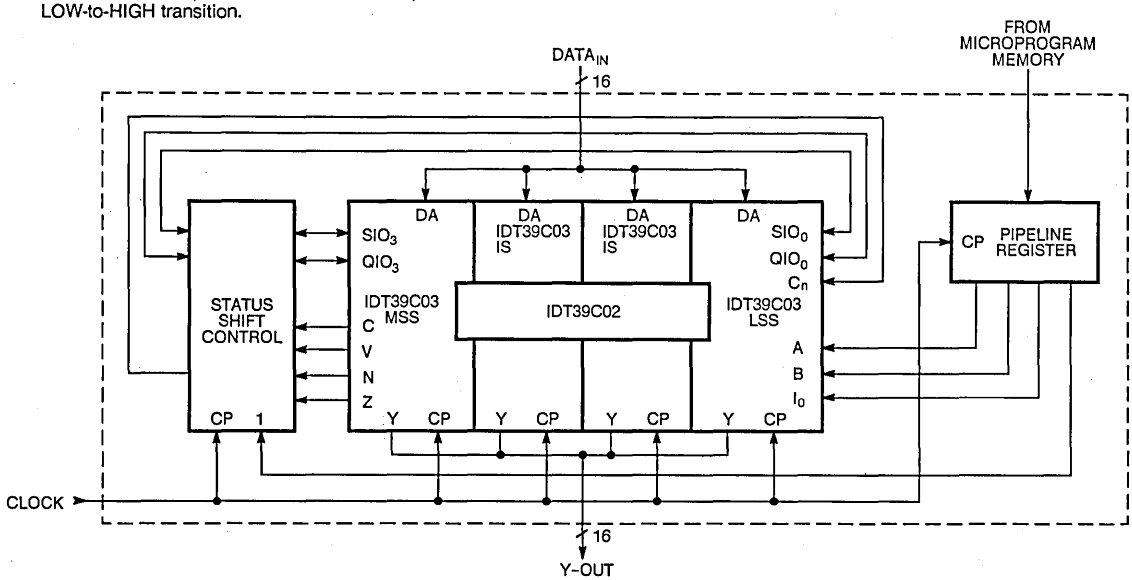
6. Not Valid.
7. L = LOW = 0, H = HIGH = 1, V = OR, Λ = AND, $\forall$= EXCLUSIVE OR, $P = P_3P_2P_1P_0$,
$G = G_3 \vee G_2P_3 \vee G_1P_2P_3 \vee G_0P_1P_2P_3$, $C_{n+3} = G_2 \vee G_1 P_2 \vee G_0P_1P_2 \vee C_nP_0P_1P_2$

Shown below is a circuit diagram for a 16-bit application using four IDT39C03s, one IDT39C02 and a status shift control device. This application has four key speed paths which are defined below:

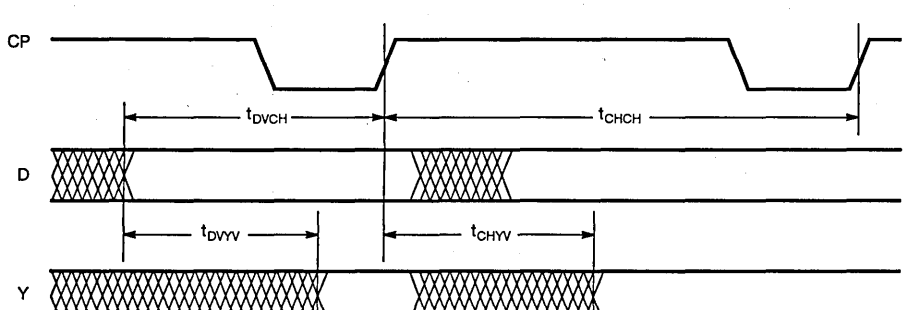
1. **Microcycle Time (t_{CHCH})**
 Minimum elapsed time between a LOW-to-HIGH clock transition and the next LOW-to-HIGH clock transition.
2. **Data Set-up Time (t_{DVCH})**
 Minimum allowable time between valid data on the D inputs and the clock LOW-to-HIGH transition.
3. **D to Y (t_{TDVYV})**
 Maximum time needed to receive valid Y output data after the D inputs are valid.
4. **CP to Y (t_{TCHYV})**
 Maximum time required to obtain valid Y outputs after a clock LOW-to-HIGH transition.

TIME IN NANOSECONDS OVER COMMERCIAL OPERATING RANGE

CYCLE	t_{CHYV}		t_{DVCH}		t_{DVYV}		t_{CHYV}	
	A	B	A	B	A	B	A	B
Logic	99	79	79	63	59	47	81	65
Logic Rotate	118	94	99	79	79	63	98	78
Arithmetic	130	104	109	87	91	73	112	90
Multiply	152	122	113	90	95	76	135	108
Divide	139	111	113	90	95	76	121	97



TIMING WAVEFORM FOR DATA$_{IN}$, CLOCK AND Y OUTPUT



ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER [1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C — V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C — V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level [4]		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level [4]		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	μA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300μA	V_{HC}	V_{CC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10	μA
			V_O = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V [3]		-30	–	–	mA

NOTES:
1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

$T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (Commercial)
$T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (Military)
$V_{LC} = 0.2V$
$V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = H		–	5	15	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = L		–	5	15	mA
I_{CCT}	Quiescent Input Power Supply(5) Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		–	0.25	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	0.5	2.0	mA/ MHz
			COM'L.	–	0.5	1.5	
I_{CC}	Total Power Supply Current(6)	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	MIL.	–	10	35	mA
			COM'L.	–	10	30	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	20	55	
			COM'L.	–	20	50	

NOTES:
5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock Input frequency

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.

IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C03A over the commercial operating range of 0°C to +70°C with V_{CC} from 4.75 to 5.25V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE 6. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

Minimum Clock Low Time	30ns
Minimum Clock High Time	30ns
Minimum Time CP and $\overline{WE}$ both Low to Write	15ns

TABLE 7. ENABLE/DISABLE TIMES ALL FUNCTIONS[1]

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	25	21
$\overline{OE}_B$	DB	25	21
I_8	SIO	25	21
I_8	QIO	38	38
$I_{8,7,6,5}$	QIO	38	38
$I_{4,3,2,1,0}$	QIO	38	35
$\overline{LSS}$	$\overline{WRITE}$	25	21

NOTE:
1. C_L = 5pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE 8. SET-UP AND HOLD TIMES ALL FUNCTIONS

		HIGH-TO-LOW		LOW-TO-HIGH		
FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q [1]
$\overline{WE}$ HIGH	CP	15	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	17	3	Shift Q
$I_{8,7,6,5}$	CP	12	–	20	0	Write into Q[2]
$\overline{IEN}$ HIGH	CP	24	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	21	0	Write into Q
$I_{4,3,2,1,0}$	CP	18	–	32	0	Write into Q[2]

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. IEN controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L → H and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	67	55	52	74	61	67	28	–	–	41	62	78
DA, DB	58	50	40	65	54	58	–	–	–	35	59	65
C_n	33	18	–	35	28	26	–	–	–	23	30	38
I_{8-0}	64	64	50	72	61	62	–	34	26*	50*	62*	74*
CP	58	42	43	61	54	58	22	–	22	37	54	60
SIO_0, SIO_3	23	–	–	29	–	–	–	–	–	–	29	19
$\overline{MSS}$	44	–	44	44	44	44	–	–	–	–	44	–
Y	–	–	–	17	–	–	–	–	–	–	–	–
$\overline{IEN}$	–	–	–	–	–	–	–	20	–	–	–	–
$\overline{EA}$	58	50	40	65	54	58	–	–	–	35	59	65

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. Standard Functions: See Table 2, Increment SF4: $F = S + 1 + C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	(67)	(55)	–	–	(61)	(67)	(28)	–	–	(41)
	IS	(67)	(55)	(52)	–	–	–	(28)	–	–	(41)
	LSS	(67)	(55)	(52)	–	–	–	(28)	–	–	(41)
DA, DB	MSS	(58)	(50)	–	–	(54)	(58)	–	–	–	(35)
	IS	(58)	(50)	(40)	–	–	–	–	–	–	(35)
	LSS	(58)	(50)	(40)	–	–	–	–	–	–	(35)
C_n	MSS	35	(18)	–	–	(28)	(26)	–	–	–	(23)
	IS	(33)	(18)	–	–	–	–	–	–	–	(23)
	LSS	(33)	(18)	–	–	–	–	–	–	–	(23)
I_{8-0}	MSS	94	75	–	–	88	88	–	–	(26)	73*
	IS	94	75	71	–	–	–	–	–	(26)	73*
	LSS	94	75	71	30	–	–	–	(34)	(26)	73*
CP	MSS	(58)	(42)	–	–	(54)	(58)	(22)	–	(22)	(37)
	IS	(58)	(42)	(43)	–	–	–	(22)	–	(22)	(37)
	LSS	90	71	67	26	–	–	(22)	–	(22)	69
Z	MSS	64	45	–	–	58	58	–	–	–	43
	IS	64	45	41	–	–	–	–	–	–	43
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. Unsigned Multiply
   SF0: $F = S + C_n$ if $Z = 0$
   $F = S + R + C_n$ if $Z = 1$
   $Y = \text{Log. } F/2$
   $Q = \text{Log. } Q/2$
   $Y_3 = C_{n+4}$ (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply
   SF2: $F = S + C_n$ if $Z = 0$
   $F = R + S + C_n$ if $Z = 1$
   $Y = \text{Log. } F/2$
   $Q = \text{Log. } Q/2$
   $Y_3 = F_3 \oplus OVR$ (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply Last Cycle
   SF6: $F = S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = \text{Log. } F/2$
   $Q = \text{Log. } Q/2$
   $Y_3 = OVR \oplus F_3$ (MSS)
   $Z = Q_0$ (LSS)

IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(67)	61/(55)	–	(74)/–	(61)	(67)	(28)	–	–	62
	IS	(67)	(55)	(52)	(74)/–	–	–	(28)	–	–	(41)
	LSS	(67)	(55)	(52)	(74)/–	–	–	(28)	–	–	(41)
DA, DB	MSS	(58)	55/(50)	–	(65)/–	(54)	(58)	–	–	–	59
	IS	(58)	(50)	(40)	(65)/–	–	–	–	–	–	(35)
	LSS	(58)	(50)	(40)	(65)/–	–	–	–	–	–	(35)
C_n	MSS	(33)	33/(18)	–	(35)/–	(28)	27	–	–	–	32
	IS	(33)	(18)	–	(35)/–	–	–	–	–	–	(23)
	LSS	(33)	(18)	–	(35)/–	–	–	–	–	–	(23)
I_{8-0}	MSS	(64)/84	75/68	–	(72)/29	(61)/77	(62)/77	–	–	(26)	63/83*
	IS	(64)/84	(64)/68	(50)/70	(72)	–	–	–	–	(26)	(62)/83*
	LSS	(64)/84	(64)/68	(50)/70	(72)	–	–	–	(34)	(26)	(62)/83*
CP	MSS	(58)/80	46/64	–	(61)/25	(54)/66	(58)/66	(22)	–	(22)	(54)/79
	IS	(58)	(42)	(43)	(61)/–	–	–	(22)	–	(22)	(54)
	LSS	(58)	(42)	(43)	(61)/–	–	–	(22)	–	(22)	(54)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/55	–/39	–/41	–	–	–	–	–	–	–/54
	LSS	–/55	–/39	–/41	–	–	–	–	–	–	–/54
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. If two delays are given, the first is for first divide and normalization; the second is for two's complement divide and two's complement divide correction.
5. Double Length Normalize and First Divide Op
   SFA: $F = S + C_n$
   $Y = $ Log. 2F
   $Q = $ Log. 2Q
   $SIO_3 = F_3 \oplus R_3$(MSS)
   $C_{n+4} = F_3 \oplus F_2$ (MSS)
   $OVR = F_2 \oplus F_1$ (MSS)
   $Z = \overline{Q}_0 \overline{Q}_1 \overline{Q}_2 \overline{Q}_3 \overline{F}_0 \overline{F}_1 \overline{F}_2 \overline{F}_3$

   Two's Complement Divide
   SFC: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = $ Log. 2F
   $Q = $ Log. 2Q
   $SIO_3 = F_3 \oplus R_3$(MSS)
   $Z = \overline{F}_3 \oplus R_3$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = F$
   $Q = $ Log. 2Q
   $Z = \overline{F}_3 \oplus R_3$ (MSS) from previous cycle
6. This specification is not tested but is guranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

8

IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	97	81	–	42	89	89	(28)	–	–	102
	IS	(67)	(55)	(52)	–	–	–	(28)	–	–	(62)
	LSS	(67)	(55)	(52)	–	–	–	(28)	–	–	(62)
DA, DB	MSS	94	76	–	37	84	84	–	–	–	97
	IS	(58)	(50)	(40)	–	–	–	–	–	–	(59)
	LSS	(58)	(50)	(40)	–	–	–	–	–	–	(59)
C_n	MSS	(33)	(18)	–	–	32	27	–	–	–	(30)
	IS	(33)	(18)	–	–	–	–	–	–	–	(30)
	LSS	(33)	(18)	–	–	–	–	–	–	–	(30)
I_{8-0}	MSS	85	67	–	28	82	73	–	–	(26)	88*
	IS	85	67	63	–	–	–	–	–	(26)	88*
	LSS	85	67	63	–	–	–	–	(34)	(26)	88*
CP	MSS	94	76	–	37	84	84	(22)	–	(22)	97
	IS	(58)	(42)	(43)	–	–	–	(22)	–	(22)	(54)
	LSS	(58)	(42)	(43)	–	–	–	(22)	–	(22)	(54)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	57	39	35	–	–	–	–	–	–	60
	LSS	57	39	35	–	–	–	–	–	–	60
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF5: $F = S + C_n$ if $Z = 0$ $\quad Y_3 = S_3 \oplus F_3$ (MSS) $\quad Q = Q$
   $F = \overline{S} + C_n$ if $Z = 1$ $\quad Z = S_3$ (MSS) $\quad N = F_3$ if $Z = 0$
   $N = F_3 \oplus S_3$ if $Z = 1$
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{\text{WRITE}}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(67)	–	–	–	–	–	(28)	–	–	(62)
	IS	(67)	(55)	(52)	–	–	–	(28)	–	–	(62)
	LSS	(67)	(55)	(52)	–	–	–	(28)	–	–	(62)
DA, DB	MSS	(58)	–	–	–	–	–	–	–	–	(59)
	IS	(58)	(50)	(40)	–	–	–	–	–	–	(59)
	LSS	(58)	(50)	(40)	–	–	–	–	–	–	(59)
C_n	MSS	(33)	–	–	–	–	–	–	–	–	(30)
	IS	(33)	(18)	–	–	–	–	–	–	–	(30)
	LSS	(33)	(18)	–	–	–	–	–	–	–	(30)
I_{8-0}	MSS	(64)	37	–	29	24	24	–	–	(26)	(62)*
	IS	(64)	(64)	(50)	29	–	–	–	–	(26)	(62)*
	LSS	(64)	(64)	(50)	29	–	–	–	(34)	(26)	(62)*
CP	MSS	(58)	29	–	26	26	29	(22)	–	(22)	(54)
	IS	(58)	(42)	(43)	26	–	–	(22)	–	(22)	(54)
	LSS	(58)	(42)	(43)	26	–	–	(22)	–	(22)	(54)
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF8: $F = S + C_n$ $\quad C_{n+4} = Q_3 \oplus Q_2$ (MSS) $\quad OVR = Q_2 \oplus Q_1$ (MSS)
   $N = Q_3$ (MSS) $\quad Z = \overline{Q_0}\overline{Q_1}\overline{Q_2}\overline{Q_3}$
   $Y = F$
   $Q = \text{LOG. } 2Q$
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

8

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C03A over the military operating range of -55°C to +125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE 9. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

Minimum Clock Low Time	30ns
Minimum Clock High Time	30ns
Minimum Time CP and $\overline{WE}$ both Low to Write	30ns

TABLE 10. ENABLE/DISABLE TIMES ALL FUNCTIONS[1]

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	25	21
$\overline{OE}_B$	DB	25	21
I_8	SIO	25	21
I_8	QIO	38	38
$I_{8,7,6,5}$	QIO	38	38
$I_{4,3,2,1,0}$	QIO	38	35
$\overline{LSS}$	$\overline{WRITE}$	30	25

NOTE:
1. C_L = 5pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE 11. SET-UP AND HOLD TIMES ALL FUNCTIONS

		HIGH-TO-LOW		LOW-TO-HIGH		
						
FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q[1]
$\overline{WE}$ HIGH	CP	15	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	17	3	Shift Q
$I_{8,7,6,5}$	CP	12	–	20	0	Write into Q[2]
$\overline{IEN}$ HIGH	CP	24	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	21	0	Write into Q
$I_{4,3,2,1,0}$	CP	18	–	32	0	Write into Q[2]

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$= L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L → H and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	70	58	52	78	68	67	28	–	–	47	71	84
DA, DB	60	52	40	66	55	58	–	–	–	35	61	74
C_n	35	19	–	41	31	29	–	–	–	23	33	40
I_{8-0}	72	69	56	80	71	69	–	36	26*	58*	75*	89*
CP	60	42	43	67	55	58	22	–	22	41	61	66
SIO_0, SIO_3	26	–	–	29	–	–	–	–	–	–	29	19
$\overline{MSS}$	44	–	44	44	44	44	–	–	–	–	44	–
Y	–	–	–	17	–	–	–	–	–	–	–	–
$\overline{IEN}$	–	–	–	–	–	–	–	20	–	–	–	–
$\overline{EA}$	60	52	40	66	55	58	–	–	–	35	61	74

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. Standard Functions: See Table 2, Increment SF4: $F=S+1+C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	72	(58)	–	–	(68)	(67)	(28)	–	–	(47)
	IS	(70)	(58)	(52)	–	–	–	(28)	–	–	(47)
	LSS	(70)	(58)	(52)	–	–	–	(28)	–	–	(47)
DA, DB	MSS	62	(52)	–	–	(55)	(58)	–	–	–	(35)
	IS	(60)	(52)	(40)	–	–	–	–	–	–	(35)
	LSS	(60)	(52)	(40)	–	–	–	–	–	–	(35)
C_n	MSS	40	(19)	–	–	(31)	(29)	–	–	–	(23)
	IS	(35)	(19)	–	–	–	–	–	–	–	(23)
	LSS	(35)	(19)	–	–	–	–	–	–	–	(23)
I_{8-0}	MSS	108	84	–	–	98	98	–	–	(26)	81*
	IS	108	84	80	–	–	–	–	–	(26)	81*
	LSS	108	84	80	33	–	–	–	(36)	(26)	81*
CP	MSS	62	(42)	–	–	(55)	(58)	(22)	–	(22)	(41)
	IS	(60)	(42)	(43)	–	–	–	(22)	–	(22)	(41)
	LSS	104	80	74	29	–	–	(22)	–	(22)	77
Z	MSS	75	51	–	–	65	65	–	–	–	48
	IS	75	51	47	–	–	–	–	–	–	48
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. Unsigned Multiply
SF0: $F=S+C_n$ if $Z=0$
$F=S+R+C_n$ if $Z=1$
$Y=$ Log. $F/2$
$Q=$ Log. $Q/2$
$Y_3=C_{n+4}$ (MSS)
$Z=Q_0$ (LSS)

Two's Complement Multiply
SF2: $F=S+C_n$ if $Z=0$
$F=R+S+C_n$ if $Z=1$
$Y=$ Log. $F/2$
$Q=$ Log. $Q/2$
$Y_3=F_3 \oplus OVR$ (MSS)
$Z=Q_0$ (LSS)

Two's Complement Multiply Last Cycle
SF6: $F=S+C_n$ if $Z=0$
$F=S-R-1+C_n$ if $Z=1$
$Y=$ Log. $F/2$
$Q=$ Log. $Q/2$
$Y_3= OVR \oplus F_3$ (MSS)
$Z=Q_0$ (LSS)
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(70)	72/(58)	–	(78)/–	(68)	(67)	(28)	–	–	(71)
	IS	(70)	(58)	(52)	(78)/–	–	–	(28)	–	–	(71)
	LSS	(70)	(58)	(52)	(78)/–	–	–	(28)	–	–	(71)
DA, DB	MSS	(60)	66/(52)	–	(66)/–	(55)	(58)	–	–	–	(61)
	IS	(60)	(52)	(40)	(66)/–	–	–	–	–	–	(61)
	LSS	(60)	(52)	(40)	(66)/–	–	–	–	–	–	(61)
C_n	MSS	(35)	37/(19)	–	(41)/–	(31)	(29)	–	–	–	36
	IS	(35)	(19)	–	(41)/–	–	–	–	–	–	(33)
	LSS	(35)	(19)	–	(41)/–	–	–	–	–	–	(33)
I_{8-0}	MSS	(72)/96	89/79	–	(80)/33	(71)/91	(69)/91	–	–	(26)	76/98*
	IS	(72)/96	(69)/79	(56)/79	(80)/–	–	–	–	–	(26)	(75)/98*
	LSS	(72)/96	(69)/79	(56)/79	(80)/–	–	–	–	(36)	(26)	(75)/98*
CP	MSS	(60)/91	51/74	–	(67)/28	(55)/74	(58)/74	(22)	–	(22)	(61)/93
	IS	(60)	(42)	(43)	(67)/–	–	–	(22)	–	(22)	(61)
	LSS	(60)	(42)	(43)	(67)/–	–	–	(22)	–	(22)	(61)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/63	–/46	–/46	–	–	–	–	–	–	–/65
	LSS	–/63	–/46	–/46	–	–	–	–	–	–	–/65
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.
5. Double Length Normalize and First Divide Op
   SFA: $F = S + C_n$
   $Y = \text{Log. } 2F$
   $Q = \text{Log. } 2Q$
   $SIO_3 = F_3 \oplus R_3$(MSS)
   $C_{n+4} = F_3 \oplus F_2$ (MSS)
   $OVR = F_2 \oplus F_1$ (MSS)
   $Z = \overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}\,\overline{Q_3}\,\overline{F_0}\,\overline{F_1}\,\overline{F_2}\,\overline{F_3}$

   Two's Complement Divide
   SFC: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = \text{Log. } 2F$
   $Q = \text{Log. } 2Q$
   $SIO_3 = \overline{F_3 \oplus R_3}$(MSS)
   $Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = F$
   $Q = \text{Log. } 2Q$
   $Z = F_3 \oplus R_3$(MSS) from previous cycle
6. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	114	95	–	49	106	106	(28)	–	–	125
	IS	(70)	(58)	(52)	–	–	–	(28)	–	–	(71)
	LSS	(70)	(58)	(52)	–	–	–	(28)	–	–	(71)
DA, DB	MSS	108	89	–	43	101	101	–	–	–	119
	IS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
	LSS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
C_n	MSS	36	(19)	–	–	35	(29)	–	–	–	(33)
	IS	(35)	(19)	–	–	–	–	–	–	–	(33)
	LSS	(35)	(19)	–	–	–	–	–	–	–	(33)
I_{8-0}	MSS	98	79	–	33	97	88	–	–	(26)	109*
	IS	98	79	73	–	–	–	–	–	(26)	109*
	LSS	98	79	73	–	–	–	–	(36)	(26)	109*
CP	MSS	108	89	–	43	101	101	(22)	–	(22)	119
	IS	(60)	(42)	(43)	–	–	–	(22)	–	(22)	(61)
	LSS	(60)	(42)	(43)	–	–	–	(22)	–	(22)	(61)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	65	46	40	–	–	–	–	–	–	76
	LSS	65	46	40	–	–	–	–	–	–	76
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF5: $F = S + C_n$ if $Z = 0$; $F = \overline{S} + C_n$ if $Z = 1$; $Y_3 = S_3 \oplus F_3$ (MSS); $Z = S_3$ (MSS); $Y = F$; $Q = Q$; $N = F_3$ if $Z = 0$; $N = F_3 \oplus S_3$ if $Z = 1$
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(70)	–	–	–	–	–	(28)	–	–	(71)
	IS	(70)	(58)	(52)	–	–	–	(28)	–	–	(71)
	LSS	(70)	(58)	(52)	–	–	–	(28)	–	–	(71)
DA, DB	MSS	(60)	–	–	–	–	–	–	–	–	(61)
	IS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
	LSS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
C_n	MSS	(35)	–	–	–	–	–	–	–	–	(33)
	IS	(35)	(19)	–	–	–	–	–	–	–	(33)
	LSS	(35)	(19)	–	–	–	–	–	–	–	(33)
I_{8-0}	MSS	(72)	47	–	33	27	27	–	–	(26)	(75)*
	IS	(72)	(69)	(56)	33	–	–	–	–	(26)	(75)*
	LSS	(72)	(69)	(56)	33	–	–	–	(36)	(26)	(75)*
CP	MSS	(60)	31	–	28	26	31	(22)	–	(22)	(61)
	IS	(60)	(42)	(43)	28	–	–	(22)	–	(22)	(61)
	LSS	(60)	(42)	(43)	28	–	–	(22)	–	(22)	(61)
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF8: $F = S + C_n$ $\quad C_{n+4} = Q_3 \oplus Q_2$ (MSS) $\quad OVR = Q_2 \oplus Q_1$ (MSS)
   $N = Q_3$ (MSS) $\quad Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
   $Y = F$
   Q = LOG. 2Q
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C03B over the commercial operating range of 0°C to +70°C with V_{CC} from 4.75 to 5.25V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE 12. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

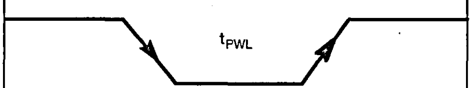
Minimum Clock Low Time	24ns
Minimum Clock High Time	24ns
Minimum Time CP and $\overline{WE}$ both Low to Write	12ns

TABLE 13. ENABLE/DISABLE TIMES ALL FUNCTIONS[1]

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	20	17
$\overline{OE}_B$	DB	20	17
I_8	SIO	20	17
I_8	QIO	30	30
$I_{8,7,6,5}$	QIO	30	30
$I_{4,3,2,1,0}$	QIO	30	30
$\overline{LSS}$	$\overline{WRITE}$	20	17

NOTE:
1. C_L = 5pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE 14. SET-UP AND HOLD TIMES ALL FUNCTIONS



FROM	WITH RESPECT TO	HIGH-TO-LOW SET-UP	HIGH-TO-LOW HOLD	LOW-TO-HIGH SET-UP	LOW-TO-HIGH HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	11	3	Store Y in RAM/Q[1]
$\overline{WE}$ HIGH	CP	12	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	12	0	Write into RAM
A, B Source	CP	16	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	5	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	14	3	Shift Q
$I_{8,7,6,5}$	CP	10	–	16	0	Write into Q[2]
$\overline{IEN}$ HIGH	CP	19	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	17	0	Write into Q
$I_{4,3,2,1,0}$	CP	14	–	25	0	Write into Q[2]

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$= L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L → H and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	54	44	41	60	49	54	23	–	–	33	50	62
DA, DB	46	40	32	52	43	47	–	–	–	28	47	52
C_n	26	15	–	28	22	20	–	–	–	19	24	30
I_{8-0}	51	51	40	58	49	50	–	27	21*	40*	50*	59*
CP	46	34	35	49	43	47	18	–	18	30	43	48
SIO_0, SIO_3	19	–	–	23	–	–	–	–	–	–	23	15
$\overline{MSS}$	35	–	35	35	35	35	–	–	–	–	35	–
Y	–	–	–	14	–	–	–	–	–	–	–	–
$\overline{IEN}$	–	–	–	–	–	–	–	16	–	–	–	–
$\overline{EA}$	46	40	32	52	43	47	–	–	–	28	47	52

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. Standard Functions: See Table 2, Increment SF4: $F=S+1+C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	(54)	(44)	–	–	(49)	(54)	(23)	–	–	(33)
	IS	(54)	(44)	(41)	–	–	–	(23)	–	–	(33)
	LSS	(54)	(44)	(41)	–	–	–	(23)	–	–	(33)
DA, DB	MSS	(46)	(40)	–	–	(43)	(47)	–	–	–	(28)
	IS	(46)	(40)	(32)	–	–	–	–	–	–	(28)
	LSS	(46)	(40)	(32)	–	–	–	–	–	–	(28)
C_n	MSS	28	(15)	–	–	(22)	(20)	–	–	–	(19)
	IS	(26)	(15)	–	–	–	–	–	–	–	(19)
	LSS	(26)	(15)	–	–	–	–	–	–	–	(19)
I_{8-0}	MSS	75	60	–	–	70	70	–	–	(21)	58*
	IS	75	60	57	–	–	–	–	–	(21)	58*
	LSS	75	60	57	24	–	–	–	(27)	(21)	58*
CP	MSS	(46)	(34)	–	–	(43)	(47)	(18)	–	(18)	(30)
	IS	(46)	(34)	(35)	–	–	–	(18)	–	(18)	(30)
	LSS	72	57	54	21	–	–	(18)	–	(18)	55
Z	MSS	51	36	–	–	46	46	–	–	–	34
	IS	51	36	33	–	–	–	–	–	–	34
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(19)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. Unsigned Multiply
   SF0: $F=S+C_n$ if $Z=0$
   $F=S+R+C_n$ if $Z=1$
   $Y=$ Log. F/2
   $Q=$ Log. Q/2
   $Y_3=C_{n+4}$ (MSS)
   $Z=Q_0$ (LSS)

   Two's Complement Multiply
   SF2: $F=S+C_n$ if $Z=0$
   $F=R+S+C_n$ if $Z=1$
   $Y=$ Log. F/2
   $Q=$ Log. Q/2
   $Y_3=F_3 \oplus$ OVR (MSS)
   $Z=Q_0$ (LSS)

   Two's Complement Multiply Last Cycle
   SF6: $F=S+C_n$ if $Z=0$
   $F=S-R-1+C_n$ if $Z=1$
   $Y=$ Log. F/2
   $Q=$ Log. Q/2
   $Y_3=$ OVR $\oplus$ (MSS)
   $Z=Q_0$ (LSS)
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{\text{WRITE}}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(54)	48/(44)	–	(60)/–	(49)	(54)	(23)	–	–	50
	IS	(54)	(44)	(41)	(60)/–	–	–	(23)	–	–	(33)
	LSS	(54)	(44)	(41)	(60)/–	–	–	(23)	–	–	(33)
DA, DB	MSS	(46)	44/(40)	–	(52)/–	(43)	(47)	–	–	–	47
	IS	(46)	(40)	(32)	(52)/–	–	–	–	–	–	(28)
	LSS	(46)	(40)	(32)	(52)/–	–	–	–	–	–	(28)
C_n	MSS	(26)	26/(15)	–	(28)/–	(22)	23	–	–	–	26
	IS	(26)	(15)	–	(28)/–	–	–	–	–	–	(19)
	LSS	(26)	(15)	–	(28)/–	–	–	–	–	–	(19)
I_{8-0}	MSS	(51)/67	(51)/54	–	57/23	(49)/62	(50)/73	–	–	(21)	(50)/66*
	IS	(51)/67	(51)/54	(40)/56	57/–	–	–	–	–	(21)	(50)/66*
	LSS	(51)/67	(51)/54	(40)/56	57/–	–	–	–	(27)	(21)	(50)/66*
CP	MSS	(46)/64	37/51	–	(49)/20	(43)/53	(47)53	(18)	–	(18)	(43)/63
	IS	(46)	(34)	(35)	(49)/–	–	–	(18)	–	(18)	(43)
	LSS	(46)	(34)	(35)	(49)/–	–	–	(18)	–	(18)	(43)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/44	–/31	–/33	–	–	–	–	–	–	–/43
	LSS	–/44	–/31	–/33	–	–	–	–	–	–	–/43
SIO_0, SIO_3	Any	(19)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.
5. Double Length Normalize and First Divide Op
   SFA: $F=S+C_n$
   $Y=$ Log. 2F
   $Q=$ Log. 2Q
   $SIO_3 = F_3 \oplus R_3$(MSS)
   $C_{n+4} = F_3 \oplus F_2$ (MSS)
   $OVR = F_2 \oplus F_1$ (MSS)
   $Z = \overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}\,\overline{Q_3}\,\overline{F_0}\,\overline{F_1}\,\overline{F_2}\,\overline{F_3}$

   Two's Complement Divide
   SFC: $F=R+S+C_n$ if $Z=0$
   $F=S-R-1+C_n$ if $Z=1$
   $Y=$ Log. 2F
   $Q=$ Log. 2Q
   $SIO_3 = \overline{F_3 \oplus R_3}$(MSS)
   $Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F=R+S+C_n$ if $Z=0$
   $F=S-R-1+C_n$ if $Z=1$
   $Y=F$
   $Q=$ Log. 2Q
   $Z=F_3 \oplus R_3$(MSS) from previous cycle
6. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	77	65	–	34	72	72	(23)	–	–	82
	IS	(54)	(44)	(41)	–	–	–	(23)	–	–	(50)
	LSS	(54)	(44)	(41)	–	–	–	(23)	–	–	(50)
DA, DB	MSS	75	60	–	30	67	67	–	–	–	78
	IS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
	LSS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
C_n	MSS	(26)	(15)	–	–	26	22	–	–	–	(24)
	IS	(26)	(15)	–	–	–	–	–	–	–	(24)
	LSS	(26)	(15)	–	–	–	–	–	–	–	(24)
I_{8-0}	MSS	68	54	–	23	66	58	–	–	(21)	70*
	IS	68	54	50	–	–	–	–	–	(21)	70*
	LSS	68	54	50	–	–	–	–	(27)	(21)	70*
CP	MSS	75	60	–	30	67	67	(18)	–	(18)	77
	IS	(46)	(34)	(35)	–	–	–	(18)	–	(18)	(43)
	LSS	(46)	(34)	(35)	–	–	–	(18)	–	(18)	(43)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	46	32	28	–	–	–	–	–	–	48
	LSS	(19)	32	28	–	–	–	–	–	–	48

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF5: $F = S + C_n$ if $Z = 0$; $F = \overline{S} + C_n$ if $Z = 1$; $Y_3 = S_3 \oplus F_3$ (MSS); $Z = S_3$ (MSS); $Q = Q$; $N = F_3$ if $Z = 0$; $N = F_3 \oplus S_3$ if $Z = 1$
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(54)	–	–	–	–	–	(23)	–	–	(50)
	IS	(54)	(44)	(41)	–	–	–	(23)	–	–	(50)
	LSS	(54)	(44)	(41)	–	–	–	(23)	–	–	(50)
DA, DB	MSS	(46)	–	–	–	–	–	–	–	–	(47)
	IS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
	LSS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
C_n	MSS	(26)	–	–	–	–	–	–	–	–	(24)
	IS	(26)	(15)	–	–	–	–	–	–	–	(24)
	LSS	(26)	(15)	–	–	–	–	–	–	–	(24)
I_{8-0}	MSS	(51)	30	–	23	19	19	–	–	(21)	(50)*
	IS	(51)	52	(40)	23	–	–	–	–	(21)	(50)*
	LSS	(51)	52	(40)	23	–	–	–	(27)	(21)	(50)*
CP	MSS	(46)	23	–	21	21	21	(18)	–	(18)	(43)
	IS	(46)	(34)	(35)	21	–	–	(18)	–	(18)	(43)
	LSS	(46)	(34)	(35)	21	–	–	(18)	–	(18)	(43)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–	–	–	–	–	–	–	–	–	–
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(19)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF8: $F = S + C_n$ $\quad C_{n+4} = Q_3 \oplus Q_2$ (MSS) $\quad OVR = Q_2 \oplus Q_1$ (MSS)
   $N = Q_3$ (MSS) $\quad Z = \overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}\,\overline{Q_3}$
   $Y = F$
   $Q = LOG.\ 2Q$
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03B GUARANTEED MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C03B over the military operating range of -55°C to +125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE 15. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

Minimum Clock Low Time	24ns
Minimum Clock High Time	24ns
Minimum Time CP and $\overline{WE}$ both Low to Write	24ns

TABLE 16. ENABLE/DISABLE TIMES ALL FUNCTIONS[1]

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	20	17
$\overline{OE}_B$	DB	20	17
I_8	SIO	20	17
I_8	QIO	30	30
$I_{8,7,6,5}$	QIO	30	30
$I_{4,3,2,1,0}$	QIO	30	28
$\overline{LSS}$	$\overline{WRITE}$	24	20

NOTE:
1. C_L = 5pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE 17. SET-UP AND HOLD TIMES ALL FUNCTIONS

		HIGH-TO-LOW		LOW-TO-HIGH		
FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	11	3	Store Y in RAM/Q[1]
$\overline{WE}$ HIGH	CP	12	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	12	0	Write into RAM
A, B Source	CP	16	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	5	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	14	3	Shift Q
$I_{8,7,6,5}$	CP	10	–	16	0	Write into Q[2]
$\overline{IEN}$ HIGH	CP	19	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	17	0	Write into Q
$I_{4,3,2,1,0}$	CP	14	–	25	0	Write into Q[2]

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L → H and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

IDT39C03B GUARANTEED MILITARY RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	56	46	42	62	55	54	23	–	–	38	57	67
DA, DB	48	42	32	53	44	46	–	–	–	28	49	59
C_n	28	15	–	33	25	23	–	–	–	19	26	32
I_{8-0}	57	55	45	64	57	55	–	29	21	46	60	72
CP	48	33	34	54	44	46	18	–	18	33	49	53
SIO_0, SIO_3	20	–	–	23	–	–	–	–	–	–	23	15
$\overline{MSS}$	35	–	35	35	35	35	–	–	–	–	35	–
Y	–	–	–	14	–	–	–	–	–	–	–	–
$\overline{IEN}$	–	–	–	–	–	–	–	16	–	–	–	–
$\overline{EA}$	48	42	32	53	44	46	–	–	–	28	49	59

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. Standard Functions: See Table 2, Increment SF4: $F=S+1+C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	58	(46)	–	–	(55)	(54)	(23)	–	–	(38)
	IS	(56)	(46)	(42)	–	–	–	(23)	–	–	(38)
	LSS	(56)	(46)	(42)	–	–	–	(23)	–	–	(38)
DA, DB	MSS	50	(42)	–	–	(44)	(46)	–	–	–	(28)
	IS	(48)	(42)	(32)	–	–	–	–	–	–	(28)
	LSS	(48)	(42)	(32)	–	–	–	–	–	–	(28)
C_n	MSS	32	(15)	–	–	(25)	(23)	–	–	–	(19)
	IS	(28)	(15)	–	–	–	–	–	–	–	(19)
	LSS	(28)	(15)	–	–	–	–	–	–	–	(19)
I_{8-0}	MSS	86	67	–	–	78	78	–	–	(21)	65*
	IS	86	67	64	–	–	–	–	–	(21)	65*
	LSS	86	67	64	27	–	–	–	(29)	(21)	65*
CP	MSS	50	(33)	–	–	(44)	(46)	(18)	–	(18)	(33)
	IS	(48)	(33)	(34)	–	–	–	(18)	–	(18)	(33)
	LSS	83	64	59	23	–	–	(18)	–	(18)	62
Z	MSS	60	40	–	–	52	52	–	–	–	38
	IS	60	40	38	–	–	–	–	–	–	38
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(20)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. Unsigned Multiply
   SF0: $F=S+C_n$ if $Z=0$
   $F=S+R+C_n$ if $Z=1$
   $Y=\text{Log. } F/2$
   $Q=\text{Log. } Q/2$
   $Y_3=C_{n+4}$ (MSS)
   $Z=Q_0$ (LSS)

   Two's Complement Multiply
   SF2: $F=S+C_n$ if $Z=0$
   $F=R+S+C_n$ if $Z=1$
   $Y=\text{Log. } F/2$
   $Q=\text{Log. } Q/2$
   $Y_3=F_3 \oplus OVR$ (MSS)
   $Z=Q_0$ (LSS)

   Two's Complement Multiply Last Cycle
   SF6: $F=S+C_n$ if $Z=0$
   $F=S-R-1+C_n$ if $Z=1$
   $Y=\text{Log. } F/2$
   $Q=\text{Log. } Q/2$
   $Y_3=$ OVR $\oplus$ (MSS)
   $Z=Q_0$ (LSS)
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03B GUARANTEED MILITARY RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{\text{WRITE}}$	$QIO_{0,3}$	SIO
A, B Addr	MSS	(56)	58/(46)	–	(62)/–	(55)	(54)	(23)	–	–	(57)
	IS	(56)	(46)	(42)	(62)/–	–	–	(23)	–	–	(57)
	LSS	(56)	(46)	(42)	(62)/–	–	–	(23)	–	–	(57)
DA, DB	MSS	(48)	(42)	–	(53)/–	(44)	(46)	–	–	–	(49)
	IS	(48)	(42)	(32)	(53)/–	–	–	–	–	–	(49)
	LSS	(48)	(42)	(32)	(53)/–	–	–	–	–	–	(49)
C_n	MSS	(28)	30/(15)	–	(33)/–	(25)	(23)	–	–	–	29
	IS	(28)	(15)	–	(33)/–	–	–	–	–	–	(19)
	LSS	(28)	(15)	–	(33)/–	–	–	–	–	–	(19)
I_{8-0}	MSS	(57)/77	72/63	–	(64)/–	(57)/73	(55)/73	–	–	(21)	(60)/78*
	IS	(57)/77	(55)/63	(45)/63	(64)/–	–	–	–	–	(21)	(60)/78*
	LSS	(57)/77	(55)/63	(45)/63	(64)/–	–	–	–	(29)	(21)	(60)/78*
CP	MSS	(48)/73	40/59	–	(54)/22	(44)/59	(46)/59	(18)	–	(18)	(49)/74
	IS	(48)	(33)	(34)	(54)/–	–	–	(18)	–	(18)	(49)
	LSS	(48)	(33)	(34)	(54)/–	–	–	(18)	–	(18)	(49)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/50	–/37	–/37	–	–	–	–	–	–	–/52
	LSS	–/50	–/37	–/37	–	–	–	–	–	–	–/52
SIO_0, SIO_3	Any	(20)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. If two delays are given, the first is for first divide and normalization; the second is for two's complement divide and two's complement divide correction.
5. Double Length Normalize and First Divide Op
   SFA: $F=S+C_n$
   $Y=$ Log. 2F
   $Q=$ Log. 2Q
   $SIO_3=F_3 \oplus R_3$(MSS)
   $C_{n+4}=F_3 \oplus F_2$ (MSS)
   $OVR=F_2 \oplus F_1$ (MSS)
   $Z=\overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}\,\overline{Q_3}\,\overline{F_0}\,\overline{F_1}\,\overline{F_2}\,\overline{F_3}$

   Two's Complement Divide
   SFC: $F=R+S+C_n$ if $Z=0$
   $F=S-R-1+C_n$ if $Z=1$
   $Y=$ Log. 2F
   $Q=$ Log. 2Q
   $SIO_3=\overline{F_3 \oplus R_3}$(MSS)
   $Z=\overline{F_3 \oplus R_3}$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F=R+S+C_n$ if $Z=0$
   $F=S-R-1+C_n$ if $Z=1$
   $Y=F$
   $Q=$ Log. 2Q
   $Z=\overline{F_3 \oplus R_3}$(MSS) from previous cycle
6. This specification is not tested but is guranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03B GUARANTEED MILITARY RANGE PERFORMANCE
SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	92	76	–	39	85	85	(23)	–	–	100
	IS	(56)	(46)	(42)	–	–	–	(23)	–	–	(57)
	LSS	(56)	(46)	(42)	–	–	–	(23)	–	–	(57)
DA, DB	MSS	86	72	–	35	80	80	–	–	–	95
	IS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
	LSS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
C_n	MSS	29	(15)	–	–	28	(23)	–	–	–	(26)
	IS	(28)	(15)	–	–	–	–	–	–	–	(26)
	LSS	(28)	(15)	–	–	–	–	–	–	–	(26)
I_{8-0}	MSS	78	64	–	26	78	78	–	–	(21)	87*
	IS	78	64	58	–	–	–	–	–	(21)	87*
	LSS	78	64	58	–	–	–	–	(29)	(21)	87*
CP	MSS	86	72	–	34	80	80	(18)	–	(18)	95
	IS	(48)	(33)	(34)	–	–	–	(18)	–	(18)	(49)
	LSS	(48)	(33)	(34)	–	–	–	(18)	–	(18)	(49)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	52	37	32	–	–	–	–	–	–	60
	LSS	52	37	32	–	–	–	–	–	–	60
SIO_0, SIO_3	Any	(20)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF5: $F = S + C_n$ if $Z = 0$; $F = \overline{S} + C_n$ if $Z = 1$; $Y_3 = S_3 \oplus F_3$ (MSS); $Z = S_3$ (MSS); $Y = F$; $Q = Q$; $N = F_3$ if $Z = 0$; $N = F_3 \oplus S_3$ if $Z = 1$
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

8

IDT39C03B GUARANTEED MILITARY RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(56)	–	–	–	–	–	(23)	–	–	(57)
	IS	(56)	(46)	(42)	–	–	–	(23)	–	–	(57)
	LSS	(56)	(46)	(42)	–	–	–	(23)	–	–	(57)
DA, DB	MSS	(48)	–	–	–	–	–	–	–	–	(49)
	IS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
	LSS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
C_n	MSS	(28)	–	–	–	–	–	–	–	–	(26)
	IS	(28)	(15)	–	–	–	–	–	–	–	(26)
	LSS	(28)	(15)	–	–	–	–	–	–	–	(26)
I_{8-0}	MSS	(57)	38	–	26	22	22	–	–	(21)	(60)*
	IS	(57)	(55)	(45)	26	–	–	–	–	(21)	(60)*
	LSS	(57)	(55)	(45)	26	–	–	–	(29)	(21)	(60)*
CP	MSS	(48)	25	–	23	20	25	(18)	–	(18)	(49)
	IS	(48)	(33)	(34)	23	–	–	(18)	–	(18)	(49)
	LSS	(48)	(33)	(34)	23	–	–	(18)	–	(18)	(49)
SIO_0, SIO_3	Any	(20)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF8: $F = S + C_n$ $C_{n+4} = Q_3 \oplus Q_2$ (MSS) $OVR = Q_2 \oplus Q_1$ (MSS)
   $N = Q_3$ (MSS) $Z = \overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}\,\overline{Q_3}$
   $Y = F$
   $Q = LOG.\ 2Q$

IDT39C03 INPUT/OUTPUT INTERFACE CIRCUITRY

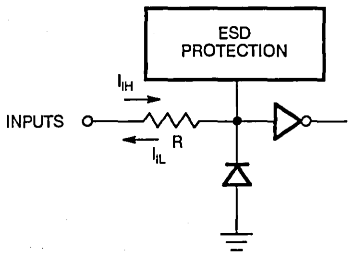


Figure 1. Input Structure (All Inputs)

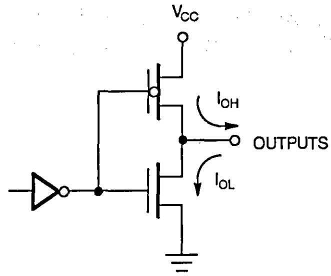


Figure 2. Output Structure (All Outputs)

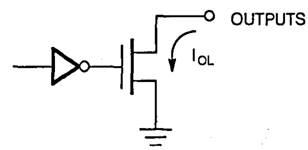
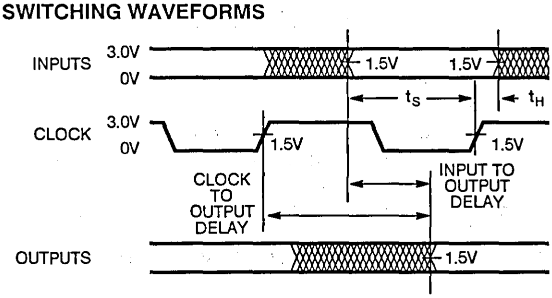


Figure 3. Open Drain Structure

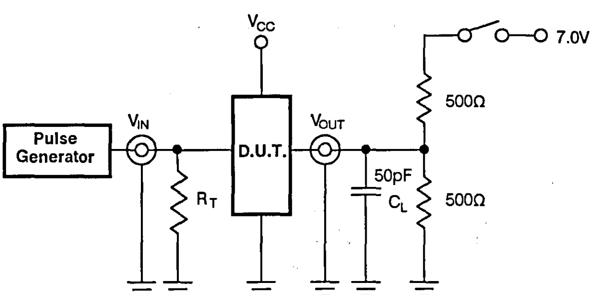
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 4

SWITCHING WAVEFORMS



TEST LOAD CIRCUIT



TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All other Outputs	Open

DEFINITIONS

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 4. Switching Test Circuits

ORDERING INFORMATION

XXXXX — Device Type; X — Package; X — Process Temperature Range

Process Temperature Range:
- Blank — Commercial (0°C to +70°C)
- B — Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:
- P — Plastic DIP
- C — Sidebraze DIP
- L — Leadless Chip Carrier

Device Type:
- 39C03A — 4-Bit CMOS µP Slice
- 39C03B — High-Speed 4-Bit CMOS µP Slice

Integrated Device Technology, Inc.

4-BIT CMOS MICROPROGRAM SEQUENCER

IDT39C09A/B
IDT39C11A/B

MICROSLICE™ PRODUCT

FEATURES:

- Low-power CMOS
  - Commercial: 45mA (max.)
  - Military: 55mA (max.)
- Fast
  - A version meets standard speed
  - B version is 20%-50% speed upgrade
- 9-Deep stack
  - Accommodates nested loops and subroutines
- Cascadable
  - Infinitely expandable in 4-bit increments
- Available in 28-pin DIP and LCC (IDT39C09) and 20-pin DIP, LCC and SOIC (IDT39C11)
- Pin-compatible, functional enhancement for all versions of the 2909/2911
- Military product compliant to MIL-STD-883, Class B

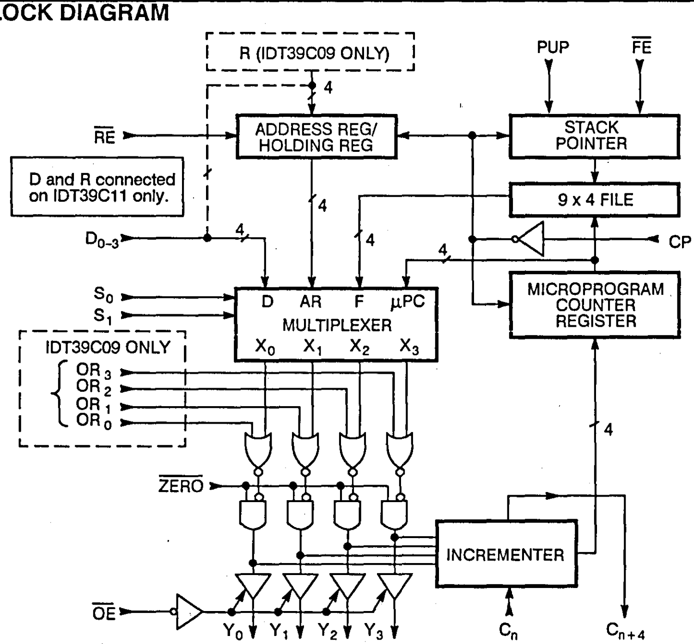
DESCRIPTION:

The IDT39C09/11 devices are high-speed, 4-bit address sequencers intended for controlling the sequence of microinstructions located in the microprogram memory. They are fully cascadable and can be expanded to any increment of 4 bits.

The IDT39C09s can select an address from any four sources: 1) external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a 9-word deep push-pop stack; or 4) a program counter register. Also included in the stack are additional control functions which efficiently execute nested subroutine linkage. Each output can be ORed with an external input for conditional skip or branch instructions. A $\overline{ZERO}$ input line forces the outputs to all zeroes. All outputs are three-state and are controlled by the $\overline{OE}$ (Output Enable) pin.

The IDT39C11s operate identically to the IDT39C09s, except the four OR inputs are removed and the D and R inputs are tied together. They are fabricated using CEMOS™, CMOS technology designed for high-performance and high-reliability. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

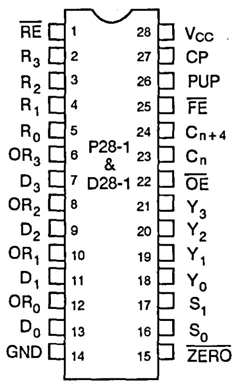
FUNCTIONAL BLOCK DIAGRAM



CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.

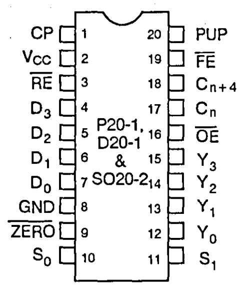
PIN CONFIGURATIONS

IDT39C09



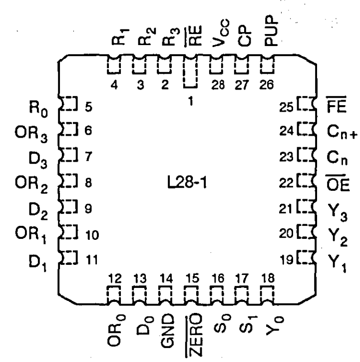
DIP
TOP VIEW

IDT39C11



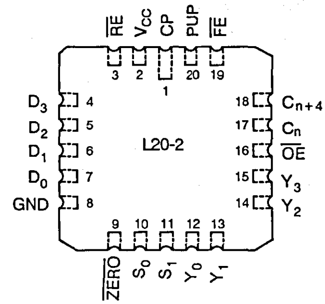
DIP/SOIC
TOP VIEW

IDT39C09



LCC
TOP VIEW

IDT39C11



LCC
TOP VIEW

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
S_1, S_0	I	Control lines for address source selection.
$\overline{FE}$, PUP	I	Control lines for push/pop stack.
$\overline{RE}$	I	Enable line for internal address register.
OR_i	I	Logic OR inputs on each address output line. (IDT39C09 ONLY.)
$\overline{ZERO}$	I	When LOW, forces output lines to zero.
$\overline{OE}$	I	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance).
C_n	I	Carry-in to the incrementer.
R_i	I	Inputs to the internal address register. (IDT39C09 ONLY.)
D_i	I	Direct inputs to the multiplexer.
CP	I	Clock input to the AR, µPC register and Push-Pop stack.
Y_i	O	Address outputs from IDT39C09/11. (Address inputs to control memory.)
C_{n+4}	O	Carry out from the incrementer.

8

MICROPROGRAM SEQUENCER ARCHITECTURE

The IDT39C09/11's architecture consists of the following segments:

- Multiplexer
- Direct Inputs
- Address Register
- Microprogram Counter
- Stack

MULTIPLEXER

The multiplexer is controlled by the S_0 and S_1 inputs to select the address source. The two inputs control the selection of the address register, direct inputs, microprogram counter or stack as the source of the next microinstruction address.

DIRECT INPUTS

This 4-bit field of inputs (D_I) allows addresses from an external source to be output on the Y outputs. On the IDT39C11s, these inputs are also used as inputs to the register.

ADDRESS REGISTER

The Address Register (AR) consists of 4 D-type, edge-triggered flip-flops which are controlled by the Register Enable ($\overline{RE}$) input. With the address register enable LOW, new data will be entered into the register on the clock LOW-to-HIGH transition. The address register is also available as the next microinstruction address to the multiplexer.

MICROPROGRAM COUNTER

Both devices contain a microprogram counter (μPC), which consists of a 4-bit incrementer followed by a 4-bit register. The incrementer has Carry-In (C_n) and Carry-Out (C_{n+4}) for easy and simple cascading.

When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one ($Y + 1 \rightarrow \mu PC$). If the least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle ($Y \rightarrow \mu PC$).

STACK

The 9-deep stack, which stores return addresses when executing microinstructions, is an input to the multiplexer. It contains a stack pointer which always points to the last word written. The added stack depth of 9 on the IDT39C09/11 allows for additional microinstruction nesting.

The stack pointer is an up/down counter controlled by File End ($\overline{FE}$) and Push/POP (PUP) inputs. When the $\overline{FE}$ input is LOW and the PUP input is HIGH, the PUSH operation is enabled. The stack pointer will then increment and the memory array is written with the microinstruction address following the subroutine jump that initiated the PUSH. A POP operation is initiated at the end of a microsubroutine to obtain the return address. A POP will occur when $\overline{FE}$ and PUP are both LOW, implying a return from a subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the $\overline{FE}$ input is HIGH, no action is taken by the stack pointer regardless of any other input.

The $\overline{ZERO}$ is used to force the four outputs to the binary zero state. When LOW, all Y outputs are LOW regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output (IDT39C09 only). This allows jumping to different microinstructions on programmed conditions.

The Output Enable ($\overline{OE}$) input controls the Y outputs. When HIGH, the outputs are programmed to a high impedance condition.

OPERATION OF THE IDT39C09/11

Figure 1 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Also in Figure 1 is the truth table for the output control and the push/pop stack control. S_0, S_1, $\overline{FE}$ and PUP operation is explained in Figure 2. All four define the address appearing on the Y outputs and the state of the internal registers following a clock LOW-to-HIGH transition.

The columns on the left explain the sequence of microinstructions to be executed. At address J + 2, the sequence control portion of the microinstruction contains the command "Jump to Subroutine at A". At the time T2, this instruction is in the μWR and the IDT39C09 inputs are set up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I (A), is accessed and is at the inputs of the μWR. On the next clock transition, I (A) is loaded into the μWR for execution and the return address J + 3 is pushed onto the stack. The return instruction is executed at T5. Figure 4 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

Figures 3 and 4 are examples of subroutine execution. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls the four signals S_0, S_1, $\overline{FE}$ and PUP. The starting address of the subroutine is applied to the D inputs of the IDT39C09 at the correct time.

ADDRESS SELECTION

S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
L	L	Microprogram Counter	µPC
L	H	Address/Holding Register	AR
H	L	Push-Pop Stack	STK0
H	H	Direct Inputs	D_I

OUTPUT CONTROL

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

SYNCHRONOUS STACK CONTROL

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 1.

CYCLE	S_0, S_1, $\overline{FE}$, PUP	µPC	REG	Y_{OUT}	COMMENT	PRINCIPAL USE
N N + 1	L L L L –	J J + 1	K K	J –	Pop Stack	End Loop
N N + 1	L L L H –	J J + 1	K K	J –	Push µPC	Set-up Loop
N N + 1	L L H X –	J J + 1	K K	J –	Continue	Continue
N N + 1	L H L L –	J K + 1	K K	K –	Pop Stack; Use AR for Address	End Loop
N N + 1	L H L H –	J K + 1	K K	K –	Push µPC; Jump to Address in AR	JSR AR
N N + 1	L H H X –	J K + 1	K K	K –	Jump to Address in AR	JMP AR
N N + 1	H L L L –	J Ra + J	K K	Ra –	Jump to Address in STK0; Pop Stack	RTS
N N + 1	H L L H –	J Ra + 1	K K	Ra –	Jump to Address in STK0; Push µPC	
N N + 1	H L H X –	J Ra + 1	K K	Ra –	Jump to Address in STK0	Stack Ref (Loop)
N N + 1	H H L L –	J D + 1	K K	D –	Pop Stack; Jump to Address on D	End Loop
N N + 1	H H L H –	J D + 1	K K	D –	Jump to Address on D; Push µPC	JSR D
N N + 1	H H H X –	J D + 1	K K	D –	Jump to Address on D	JMP D

X = Don't Care, 0 = LOW, 1 = HIGH, Assume C_N = HIGH

Figure 2. Output and Internal Next-Cycle Register States for IDT39C09/11

CONTROL MEMORY

EXECUTE CYCLE	MICROPROGRAM ADDRESS	MICROPROGRAM SEQUENCER INSTRUCTION
	J - 1	–
T_0	J	–
T_1	J + 1	–
T_2	J + 2	JSR A
T_6	J + 3	–
T_7	J + 4	–
	–	–
	–	–
	–	–
	–	–
T_3	A	I (A)
T_4	A + 1	–
T_5	A + 2	RTS
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–

In the columns in figures 3 and 4, the sequence of microinstructions to be executed are shown. At address J + 2, the command "Jump to Subroutine at A" is contained in the sequence control portion of the microinstruction. At time T_2, this instruction is in the μWR and the IDT39C09 inputs are set up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I (A), is accessed and is at the inputs of the μWR. On the next clock transition, I (A) is loaded into the μWR for execution and the return address J + 3 is pushed onto the stack. The return instruction is executed at T_5. Figure 4 shows a similar timing chart of one subroutine linking to a second, the latter consisting of only one microinstruction.

EXECUTE CYCLE		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
CLOCK SIGNALS											
IDT39C09/11 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	J + 4	J + 5		
	STK0	–	–	–	J + 3	J + 3	J + 3	–	–		
	STK1	–	–	–	–	–	–	–	–		
	STK2	–	–	–	–	–	–	–	–		
	STK3	–	–	–	–	–	–	–	–		
IDT39C09/11 Output	Y	J + 1	J + 2	A	A + 1	A + 2	J + 3	J + 4	J + 5		
ROM Output	(Y)	I (J + 1)	JSR A	I (A)	I (A + 1)	RTS	I (J + 3)	I (J + 4)	I (J + 5)		
Contents of μWR (Instruction being executed)	μWR	I (J)	I (J + 1)	JSR A	I (A)	I (A + 1)	RTS	I (J + 3)	I (J + 4)		

C_n = High

Figure 3. Subroutine Execution

CONTROL MEMORY

EXECUTE CYCLE	MICROPROGRAM ADDRESS	MICROPROGRAM SEQUENCER INSTRUCTION
	J – 1	–
T_0	J	–
T_1	J + 1	–
T_2	J + 2	JSR A
T_9	J + 3	–
	–	–
	–	–
	–	–
	–	–
T_3	A	–
T_4	A + 1	–
T_5	A + 2	JSR B
T_7	A + 3	–
T_8	A + 4	RTS
	–	–
	–	–
	–	–
	–	–
T_6	B	RTS
	–	–
	–	–

EXECUTE CYCLE		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
CLOCK SIGNALS											
IDT39C09/11 Inputs (from µWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	µPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	B + 1	A + 4	A + 5	J + 4
	STK0	–	–	–	J + 3	J + 3	J + 3	A + 3	J + 3	J + 3	–
	STK1	–	–	–	–	–	–	J + 3	–	–	–
	STK2	–	–	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–	–	–
IDT39C09/11 Output	Y	J + 1	J + 2	A	A + 1	A + 2	B	A + 3	A + 4	J + 3	J + 4
ROM Output	(Y)	I(J + 1)	JSR A	I(A)	I(A + 1)	JSR B	RTS	I(A + 3)	RTS	I(J + 3)	I(J + 4)
Contents of µWR (Instruction being executed)	µWR	I(J)	I(J + 1)	JSR A	I (A)	I(A + 1)	JSR B	RTS	I(A + 3)	RTS	I(J + 3)

C_n = High

Figure 4. Two Nested Subroutines. Routine B is Only One Instruction

IDT39C09/11 APPLICATIONS

The IDT39C09 and IDT39C11 are four-bit-slice sequencers which are cascaded to form a microprogram memory address generator. Both products make available to the user several lines which are used to directly control the internal holding register, multiplexer and stack. By appropriate control of these lines, the user can implement any desired set of sequence control functions; by cascading parts he can generate any desired address length. These two qualities set the IDT39C09 and IDT39C11 apart from the IDT39C10, which is architecturally similar, but is fixed at 12 bits in length and has a fixed set of 16 sequence control instructions. The IDT39C09 or IDT39C11 should be selected instead of the IDT39C10 under the following conditions: (1) address less than 8 bits and not likely to be expanded; (2) address longer than 12 bits; (3) more complex instruction set needed than is available on IDT39C10.

CONTROL UNIT ARCHITECTURE

The recommended architecture using the IDT39C09 or IDT39C11 is shown in Figure 5. The path from the pipeline register output through the next address logic, multiplexer and microprogram memory is all combinational. The pipeline register contains the current microinstruction being executed. A portion of that microinstruction consists of a sequence control command such as "continue", "loop", "return from subroutine", etc. The bits representing this sequence command are logically combined with bits representing such things as test conditions and system state to generate the required control signals to the IDT39C09 or IDT39C11.

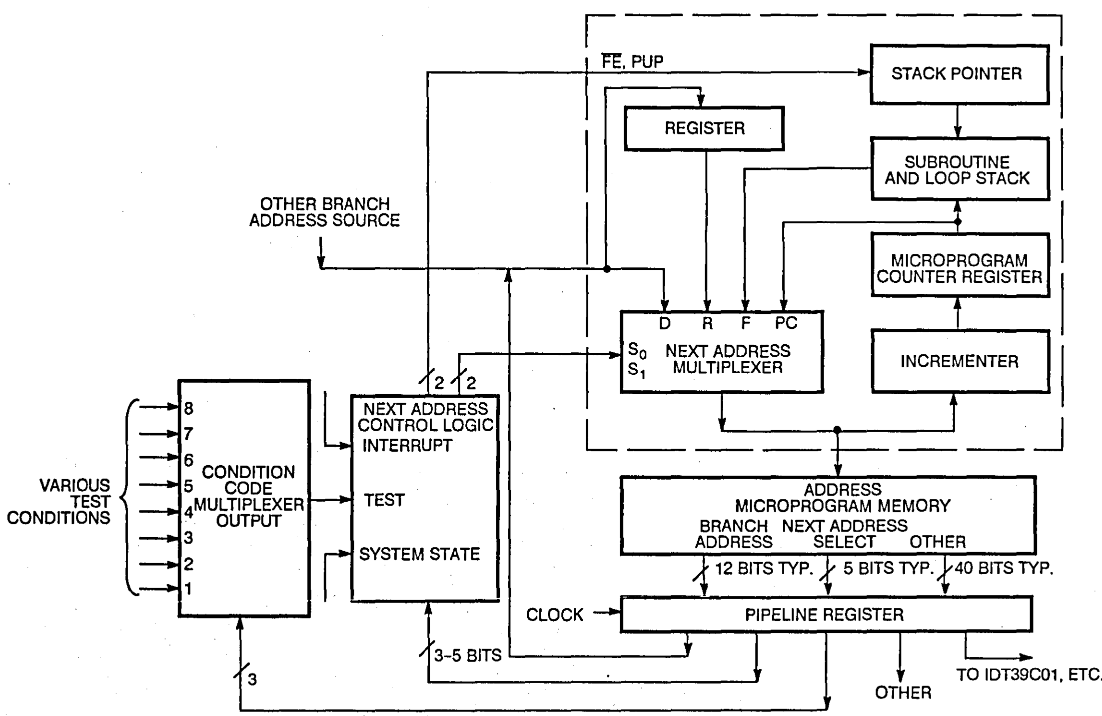


Figure 5. Recommended Computer Control Unit Architecture Using the IDT39C09A/B and IDT39C11A/B

IDT39C09/11 EXPANSION

Figure 6 shows the interconnection of three IDT39C11s to form a 12-bit sequencer. Note that the only interconnection between packages, other than the common clock and control lines, is the ripple carry between μPC incrementors. This carry path is not in the critical speed path if the IDT39C11 Y outputs drive the microprogram memory, because the ripple carry occurs in parallel with the memory access time. If, on the other hand, a microaddress register is placed at the IDT39C11 output, then the carry may lie in the critical speed path since the last carry-in must be stable for a set-up time prior to the clock.

SELECTING BETWEEN THE IDT39C09 AND IDT39C11

The difference between the IDT39C09 and the IDT39C11 involves two signals: the data inputs to the holding register and the OR inputs. In the IDT39C09, separate four-bit fields are provided for the holding register and the direct branch inputs to the multiplexer. In the IDT39C11, these fields are internally tied together. This may affect the design of the branch address system, as shown in Figure 7. Using the IDT39C09, the register inputs may be connected directly to the microprogram memory; the internal register replaces part of the pipeline register. The direct (D) inputs may be tied to the mapping logic which translates instruction op codes into microprogram addresses. While the same technique might be used with the IDT39C11, it is more common to connect the IDT39C11's D inputs to a branch address bus onto which various sources may be enabled. Shown in Figure 7 is a pipeline register and a mapping ROM. Other sources might also be applied to the same bus. The internal register is used only for temporary storage of some previous branch address.

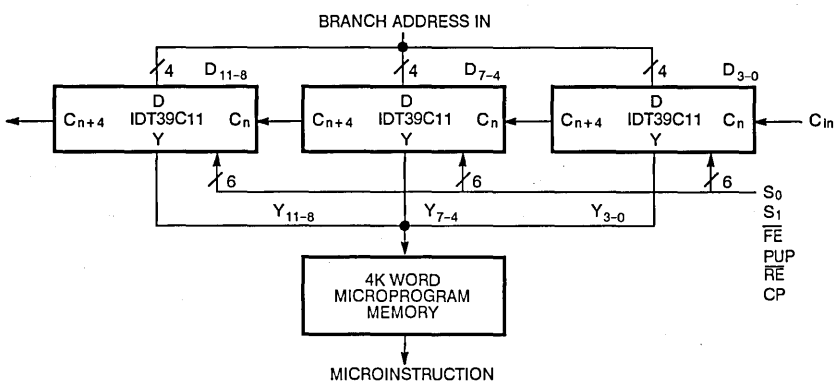


Figure 6. Twelve Bit Sequencer

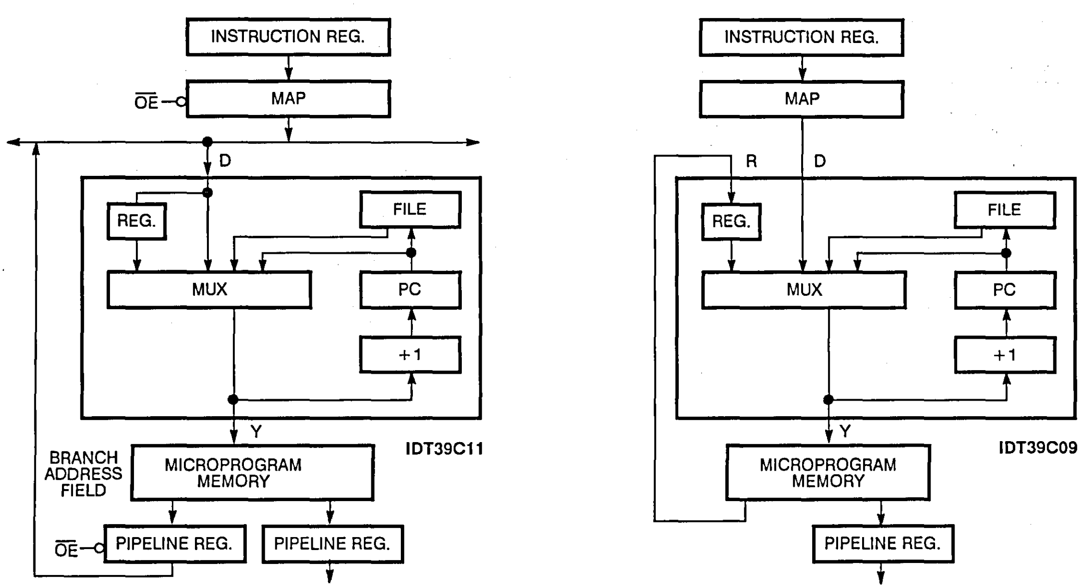


Figure 7. Branch Address Structure

The second difference between the IDT39C09 and IDT39C11 is that the IDT39C09 has OR inputs available on each address output line. These pins can be used to generate multi-way single-cycle branches by simply typing several test conditions into the OR lines (see Figure 8). Typically, a branch is taken to an address with zeros in the least significant bits. These bits are replaced with 1s or 0s by test conditions applied to the OR lines. In Figure 8, the states of the two test conditions X and Y result in a branch to 1100, 1101, 1110 or 1111.

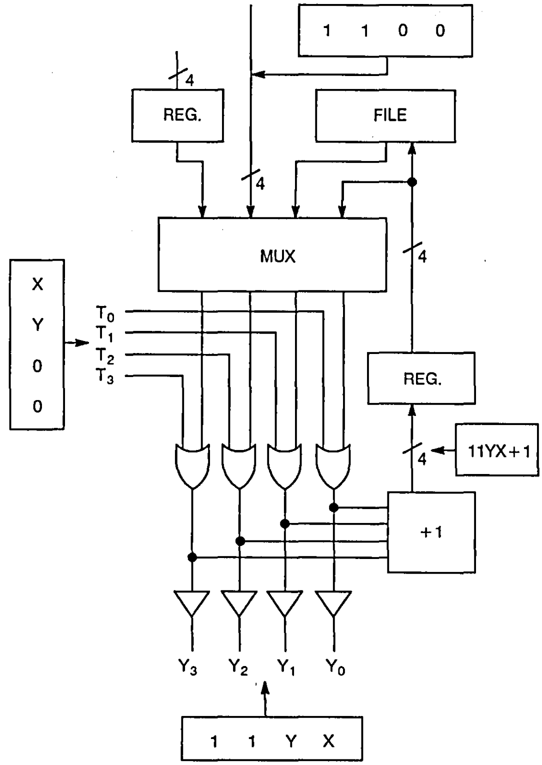


Figure 8. Use of OR Inputs to Obtain 4-Way Branch

HOW TO PERFORM COMMON FUNCTIONS WITH THE IDT39C09/11

1. CONTINUE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
PC	HOLD	H	L	L	H	X

Contents of PC placed on Y outputs; PC incremented.

2. BRANCH

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	HOLD	H	H	H	H	X

Feed data on D inputs straight through to memory address lines.
Increment address and place in PC.

3. JUMP TO SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	PUSH	H	H	H	L	H

Subroutine address fed from D inputs to memory address.
Current PC is pushed onto stack where it is saved for the return.

4. RETURN FROM SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
STACK	POP	H	H	L	L	L

The address at the top of the stack is applied to the microprogram memory and is incremented for PC on the next cycle. The stack is popped to remove the return address.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ±10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level (4)		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level (4)		–	–	0.8	V
I_{IH}	Input High Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10	µA
			V_O = V_{CC} (max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V (3)		-30	-50	–	mA

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (CONT'D)

T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ±10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = H		–	2.5	5	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = L		–	2.5	5	mA
I_{CCT}	Quiescent Input Power Supply(5) Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	2.0	4.0	mA/ MHz
			COM'L.	–	2.0	3.0	
I_{CC}	Total Power Supply Current(6)	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	MIL.	–	25	45	mA
			COM'L.	–	25	35	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	35	55	
			COM'L.	–	35	45	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

   $I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$
   CD_H = Clock duty cycle high period
   D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
   N_T = Number of dynamic inputs driven at TTL levels
   f_{CP} = Clock Input frequency

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large V_{CC} current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels are very important. Since many inputs may change coincidently, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

IDT39C09B/IDT39C11B SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Table I, II and III below define the timing characteristics of the IDT39C09B/11B over the operating voltage and temperature ranges. The tables are divided into three types of parameters: clock characteristics, combinational delays from inputs to outputs and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading.

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	COMMERCIAL	MILITARY
Minimum Clock LOW Time	12	12
Minimum Clock HIGH Time	12	12

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF (except output disable test)

FROM INPUT	COMMERCIAL		MILITARY		UNIT
	Y	C_{n+4}	Y	C_{n+4}	
D_I	14	15	16	17	ns
S_0, S_1	13	15	15	17	ns
OR_I	14	14	15	15	ns
C_n	–	11	–	12	ns
$\overline{ZERO}$	14	14	15	15	ns
$\overline{OE}$ LOW (enable)	14	–	15	–	ns
$\overline{OE}$ HIGH (disable)[1]	14	–	15	–	ns
Clock ↑ S_1S_0 = LH	17	17	19	19	ns
Clock ↑ S_1S_0 = LL	17	17	19	19	ns
Clock ↑ S_1S_0 = HL	17	17	19	19	ns

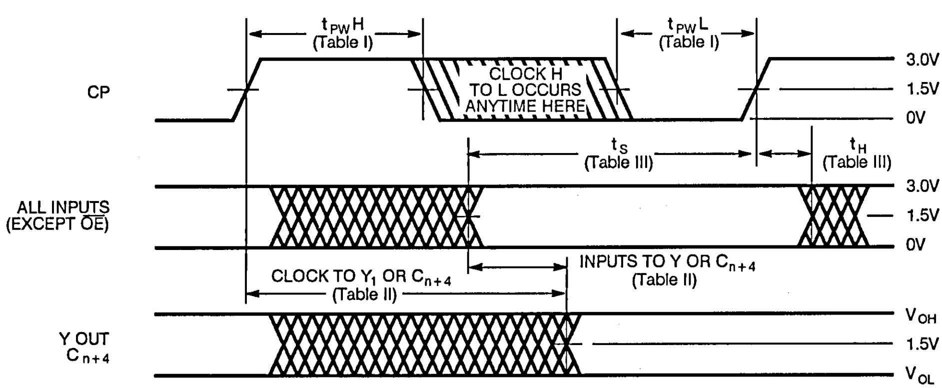
NOTE:
1. C_L = 5pF

TABLE III
GUARANTEED SET-UP AND HOLD TIMES [1]

FROM INPUT	COMMERCIAL		MILITARY		UNIT
	SET-UP TIME	HOLD TIME	SET-UP TIME	HOLD TIME	
$\overline{RE}$	6	2	7	3	ns
R_I [2]	6	2	7	3	ns
PUP	9	2	10	3	ns
$\overline{FE}$	9	2	10	3	ns
C_n	6	2	7	3	ns
D_I	8	0	9	0	ns
OR_I	8	0	9	0	ns
S_0,S_1	11	0	12	0	ns
$\overline{ZERO}$	7	0	8	0	ns

NOTES:
1. All times relative to clock LOW-to-HIGH transition.
2. On IDT39C11, R_I and D_I are internally connected together and labeled D_I. Use R_I set-up and hold times when D inputs are used to load register.

8



IDT39C09A/IDT39C11A SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Table I, II and III below define the timing characteristics of the IDT39C09A/11A over the operating voltage and temperature ranges. The tables are divided into three types of parameters: clock characteristics, combinational delays from inputs to outputs and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading.

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	COMMERCIAL	MILITARY
Minimum Clock LOW Time	20	20
Minimum Clock HIGH Time	20	20

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF (except output disable test)

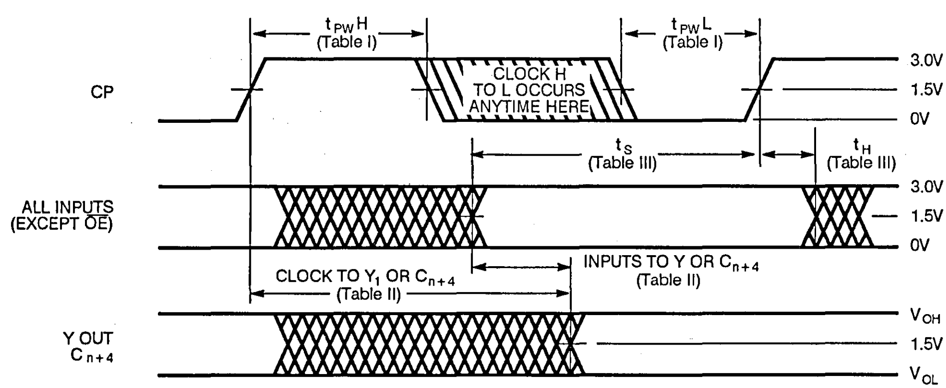
FROM INPUT	COMMERCIAL		MILITARY		UNIT
	Y	C_{n+4}	Y	C_{n+4}	
D_I	17	22	20	25	ns
S_0, S_1	29	34	29	34	ns
OR_I	17	22	20	25	ns
C_n	–	14	–	16	ns
$\overline{ZERO}$	29	34	30	35	ns
$\overline{OE}$ LOW (enable)	25	–	25	–	ns
$\overline{OE}$ HIGH (disable)[1]	25	–	25	–	ns
Clock ↑ S_1S_0 = LH	39	44	45	50	ns
Clock ↑ S_1S_0 = LL	39	44	45	50	ns
Clock ↑ S_1S_0 = HL	44	49	53	58	ns

NOTE:
1. C_L = 5pF

TABLE III
GUARANTEED SET-UP AND HOLD TIMES [1]

FROM INPUT	COMMERCIAL		MILITARY		UNIT
	SET-UP TIME	HOLD TIME	SET-UP TIME	HOLD TIME	
$\overline{RE}$	19	4	19	5	ns
R_I [2]	10	4	12	5	ns
PUP	25	4	27	5	ns
$\overline{FE}$	25	4	27	5	ns
C_n	18	4	18	5	ns
D_I	25	0	25	0	ns
OR_I	25	0	25	0	ns
S_0,S_1	25	0	29	0	ns
$\overline{ZERO}$	25	0	29	0	ns

NOTES:
1. All times relative to clock LOW-to-HIGH transition.
2. On IDT39C11, R_I and D_I are internally connected together and labeled D_I. Use R_I set-up and hold times when D inputs are used to load register.



TEST LOAD CIRCUIT

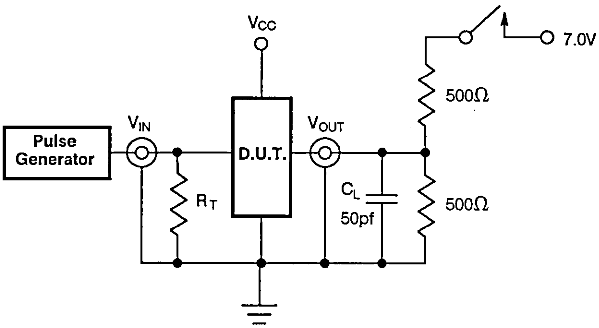
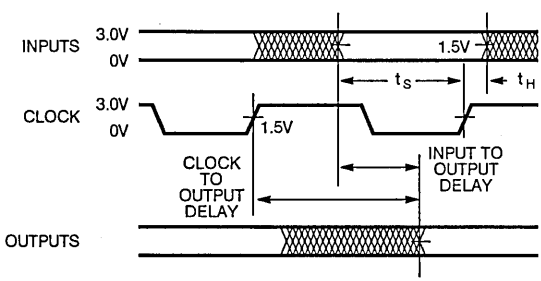


Figure 9. Switching Test Circuit (all outputs)

TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All other Outputs	Open

DEFINITIONS
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SWITCHING WAVEFORMS



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 9

8

INPUT/OUTPUT INTERFACE CIRCUITRY

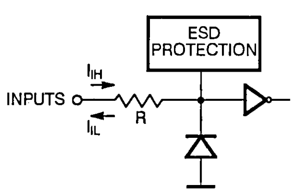


Figure 10. Input Structure

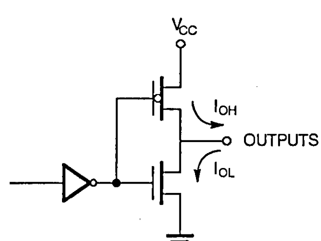


Figure 11. Output Structure

ORDERING INFORMATION

IDT XXXXX (Device Type) X (Speed) X (Package) X (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	D	CERDIP
	P	Plastic DIP
	L	LCC
	SO	Small Outline IC (IDT39C11 only)
Speed	A	Standard-Speed Sequencer
	B	High-Speed Sequencer
Device Type	39C09	4-Bit CMOS Microprogram Sequencer
	39C11	4-Bit CMOS Microprogram Sequencer

Integrated Device Technology, Inc.

12-BIT CMOS MICROPROGRAM SEQUENCER

IDT39C10B
IDT39C10C

MICROSLICE™ PRODUCT

FEATURES:

- Low-power CEMOS™
  - I_{CC} (max.)
    Military: 90mA
    Commercial: 75mA
- Fast
  - IDT39C10B matches 2910A speeds
  - IDT39C10C 30% speed upgrade
- 33-Deep stack
  - Accommodates highly nested loops and subroutines
- 12-bit address width
- 12-bit internal loop counter
- 16 powerful microinstructions
- Three output enables control 3-way branch
- Available in 40-pin DIP and 44-pin LCC/PLCC
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87708 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

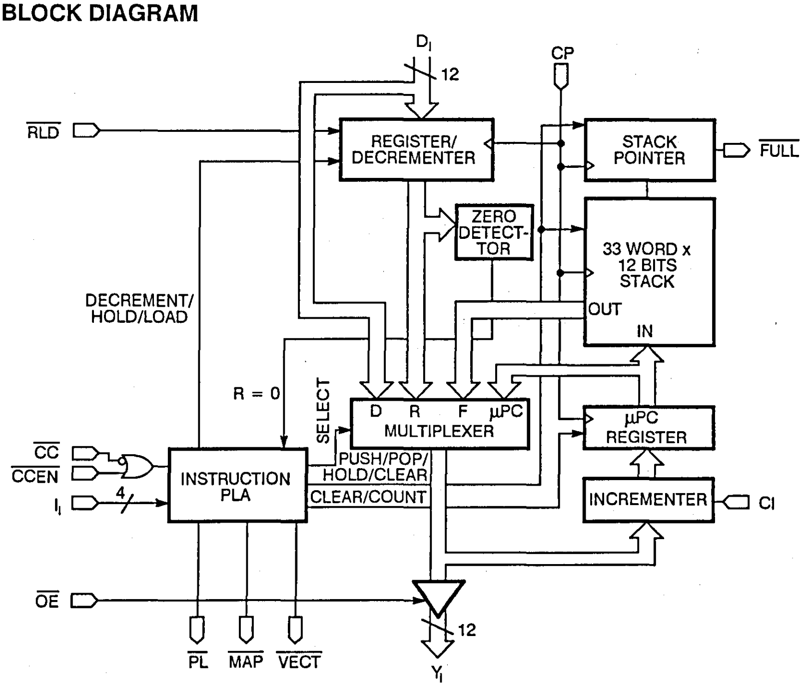
The IDT39C10 microprogram sequencers are designed for use in high-performance microprogram state machines. These microprogram sequencers are intended for use in controlling the sequence of microinstructions executed in the microprogram memory. The IDT39C10s provide several conditional branch instructions that allow branching to any microinstruction within the 4K microword address space. A 33-deep last-in/first-out stack provides for a very powerful microprogram subroutine return linkage and looping capability. With this depth of a microprogram return stack, the microprogrammer has maximum flexibility in nesting subroutines and loops. The counter contained in the IDT39C10s provides for microinstruction loop counts of up to 4096, in terms of total count length.

The IDT39C10s provide a 12-bit address to the microprogram memory. This microprogram sequencer selects one of four sources for the address. These are (1) the microprogram address register, (2) external direct input, (3) internal register counter and (4) the 33-deep LIFO stack. The microprogram counter usually contains an address that is one greater than the microinstruction currently being executed in the microprogram pipeline register.

The IDT39C10s are fabricated using CEMOS, a CMOS technology designed for high-performance and high-reliability. The devices are pin-compatible, performance-enhanced, functional replacements for the 2910A.

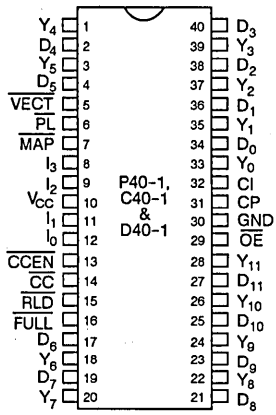
8

FUNCTIONAL BLOCK DIAGRAM

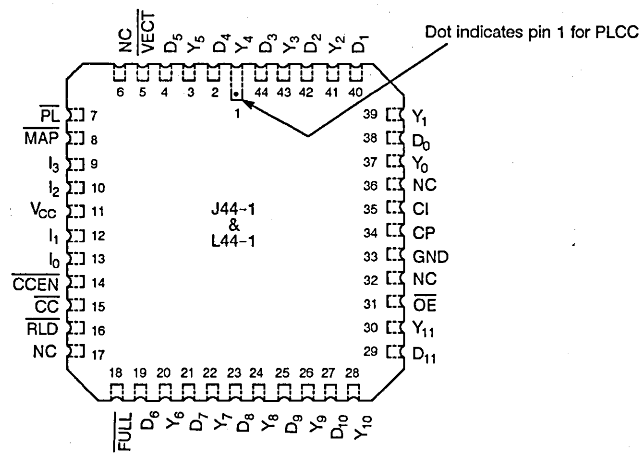


MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

PIN CONFIGURATIONS



DIP
TOP VIEW



PLCC/LCC
TOP VIEW

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
D_i	I	Direct input to register/counter and multiplexer D_0 is LSB.
I_i	I	Selects one-of-sixteen instructions.
$\overline{CC}$	I	Used as test criterion. Pass test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	I	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the part operates as though $\overline{CC}$ were true (LOW).
CI	I	Low order carry input to incrementer for microprogram counter.
$\overline{RLD}$	I	When LOW forces loading of register/counter regardless of instruction or condition.
$\overline{OE}$	I	Three-state control of Y_i outputs.
CP	I	Triggers all internal state changes at LOW-to-HIGH edge.
Y_i	O	Address to microprogram memory. Y_0 is LSB, Y_{11} is MSB.
$\overline{FULL}$	O	Indicates that 33 items are on the stack.
$\overline{PL}$	O	Can select #1 source (usually Pipeline Register) as direct input source.
$\overline{MAP}$	O	Can select #2 source (usually Mapping PROM or PLA) as direct input source.
$\overline{VECT}$	O	Can select #3 source (for example, Interrupt Starting Address) as direct input source.

PRODUCT DESCRIPTION

The IDT39C10s are high-performance CMOS microprogram sequencers that are intended for use in very high-speed microprogrammable microprocessor applications. The sequencers allow for direct control of up to 4K words of microprogram.

The heart of the microprogram sequencers is a 4-input multiplexer that is used to select one of four address sources to select the next microprogram address. These address sources include the register/counter, the direct input, the microprogram counter or the stack as the source for the address of the next microinstruction.

The register/counter consists of twelve D-type flip-flops which can contain either an address or a count. These edge-triggered flip-flops are under the control of a common clock enable, as well as the four microinstruction control inputs. When the load control (RLD) is LOW, the data at the D inputs is loaded into this register on the LOW-to-HIGH transition of the clock. The output of the register/counter is available at the multiplexer as a possible next address source for the microcode. Also, the terminal count output associated with the register/counter is available at the internal instruction PLA to be used as a condition code input for some of the microinstructions. The IDT39C10s contain a microprogram counter that usually contains the address of the next microinstruction compared to that currently being executed. The microprogram counter actually consists of a 12-bit incrementer followed by a 12-bit register. The microprogram counter will increment the address coming out of the sequencer going to the microprogram memory if the carry-in input to this counter is HIGH; otherwise, this address will be loaded into the microprogram counter. Normally, this carry-in input is set to the logic HIGH state so that the incrementer will be active. Should the carry-in input be set LOW, the same address is loaded into the microprogram counter. This is a technique that can be used to allow execution of the same microinstruction several times.

There are twelve D-inputs on the IDT39C10s that go directly to the address multiplexer. These inputs are used to provide a branch address that can come directly from the microcode or some other external source. The fourth input available to the multiplexer for next address control is the 33-deep, 12-bit wide LIFO stack. The LIFO stack provides return address linkage for subroutines and loops. The IDT39C10s contain a built-in stack pointer that always points to the last stack location written. This allows for stack reference operations, usually called loops, to be performed without popping the stack.

The stack pointer internal to the IDT39C10s is actually an up/down counter. During the execution of microinstructions one, four and five, the PUSH operation may occur depending on the state of the condition code input. This causes the stack pointer to be incremented by one and the stack to be written with the required return linkage (the value contained in the microprogram counter). On the microprogram cycle following the PUSH, this new return linkage data that was in the microprogram counter is now at the new location pointed to by the stack pointer. Thus, any time the multiplexer looks at the stack, it will see this data on the top of the stack.

During five different microinstructions, a pop operation associated with the stack may occur. If the pop occurs, the stack pointer is decremented at the next LOW-to-HIGH transition of the clock. A pop decrements the stack pointer which is the equivalent of removing the old information from the top of the stack.

The IDT39C10s are designed so that the stack pointer linkage allows any sequence of pushes, pops or stack references to be used. The depth of the stack can grow to a full 33 locations. After a depth of 33 is reached, the $\overline{\text{FULL}}$ output goes LOW. If further PUSHes are attempted when the stack is full, the stack information at the top of the stack will be destroyed but the stack pointer will not end around. It is necessary to initialize the stack pointer when power is first turned on. This is performed by executing a RESET instruction (Instruction 0). This sets the stack pointer to the stack empty position—the equivalent depth of zero. Similary, a pop from an empty stack may place unknown data on the Y outputs, but the stack pointer is designed not to end around. Thus, the stack pointer will remain at the 0 or stack empty location if a pop is executed while the stack is already empty.

The IDT39C10s' internal 12-bit register/counter is used during microinstructions eight, nine and fifteen. During these instructions, the 12-bit counter acts as a down counter and the terminal count (count = 0) is used by the internal instruction PLA as an input to control the microinstruction branch test capability. The design of the internal counter is such that, if it is preloaded with a number N and then this counter is used in a microprogram loop, the actual sequence in the loop will be executed N + 1 times. Thus, it is possible to load the counter with a count of 0 and this will result in the microcode being executed one time. The 3-way branch microinstruction, Instruction 15, uses both the loop counter and the external condition code input to control the final source address from the Y outputs of the microprogram sequencer. This 3-way branch may result in the next address coming from the D inputs, the stack or the microprogram counter.

The IDT39C10s provide a 12-bit address at the Y outputs that are under control of the $\overline{\text{OE}}$ input. Thus, the outputs can be put in the three-state mode, allowing the writable control store to be loaded or certain types of external diagnostics to be executed.

In summary, the IDT39C10s are the most powerful microprogram sequencers currently available. They provide the deepest stack, the highest performance and the lowest power dissipation for today's microprogrammed machine design.

IDT39C10 OPERATION

The IDT39C10s are CMOS pin-compatible implementations of the Am2910 & 2910A microprogram sequencers. The IDT39C10's microprogram is functionally identical except that it provides a 33-deep stack to give the microprogrammer more capability in terms of microprogram subroutines and microprogram loops. The definition of each microprogram instruction is shown in the table of instructions. This table shows the results of each instruction in terms of controlling the multiplexer, which determines the Y outputs, and in controlling the signals that can be used to enable various branch address sources ($\overline{\text{PL}}$, $\overline{\text{MAP}}$, $\overline{\text{VECT}}$). The operation of the register/counter and the 33-deep stack after the next LOW-to-HIGH transition of the clock are also shown. The internal multiplexer is used to select which of the internal sources is used to drive the Y outputs. The actual value loaded into the microprogram counter is either identical to the Y output or the Y output value is incremented by 1 and placed in the microprogram counter. This function is under the control of the carry input. For each of the microinstruction inputs only one of the three outputs ($\overline{\text{PL}}$, $\overline{\text{MAP}}$, $\overline{\text{VECT}}$) will be LOW. Note that this function is not determined by any of the possible condition code inputs. These outputs can be used to control the three-state selection of one of the sources for the microprogram branches.

Two inputs, $\overline{\text{CC}}$ and $\overline{\text{CCEN}}$, can be used to control the conditional instructions. These are fully defined in the table of instructions. The $\overline{\text{RLD}}$ input can be used to load the internal register/counter at any time. When this input is LOW, the data at the D inputs will be loaded into this register/counter on the LOW-to-HIGH transition of the clock. Thus, the $\overline{\text{RLD}}$ input overrides the internal hold or decrement operations specified by the various microinstructions. The $\overline{\text{OE}}$ input is normally LOW and is used as the three-state enable for the Y outputs. The internal stack in the IDT39C10s is a last-in/first-out memory that is 12-bits in width and 33 words deep. It has a stack pointer that addresses the stack and always points to the value currently on the top of the stack. When instruction 0 (RESET) is executed, the stack pointer is initialized to the top of the stack which is, by definition, the stack empty condition. Thus, the contents of the top of the stack are undefined until the forced PUSH occurs. A pop performed while the stack is empty will not change the stack pointer in any way; however, it will result in unknown data at the Y outputs.

By definition, the stack is full any time 33 more pushes than pops have occurred since the stack was last empty. When this happens, the Full Flag will go LOW. This signal first goes LOW on the microcycle after the 33 pushes occur. When this signal is LOW, no additional pushes should be attempted or the information on the top of the stack will be lost.

THE IDT39C10 INSTRUCTION SET

This data sheet contains a block diagram of the IDT39C10 microprogram sequencers. As can be seen, the devices are controlled by a 4-bit microinstruction word ($I_3 - I_0$). Normally, this word is supplied from one 4-bit field of the microinstruction word associated with the entire state machine system. These four bits provide for the selection of one of the sixteen powerful instructions associated with selecting the address of the next microinstruction. Unused Y outputs can be left open; however, the corresponding most significant D inputs should be tied to ground for smaller microwords. This is necessary to make sure the internal operation of the counter is proper should less than 4K of microcode be implemented. As shown in the block diagram, the internal instruction PLA uses the four instruction inputs as well as the $\overline{CC}$, $\overline{CCEN}$ and the internal counter = 0 line for controlling the sequencer. This internal instruction PLA provides all of the necessary internal control signals to control each particular part of the microprogram sequencer. The next address at the Y outputs of the IDT39C10s can be from one of four sources. These include the internal microprogram counter, the last-in/first-out stack, the register/counter and the direct inputs.

The following paragraphs will describe each instruction associated with the IDT39C10s. As a part of the discussion, an example of each instruction is shown in Figure 1. The purpose of the examples is to show microprogram flow. Thus, in each example the microinstruction currently being executed has a circle around it. That is, this microinstruction is assumed to be the contents of the pipeline register at the output of the microprogram memory. In these drawings, each of the dots refers to the time that the contents of the microprogram memory word would be in the pipeline register and is currently being executed.

INSTRUCTION 0 – JUMP 0 (JZ)

This instruction is used at power up time or at any restart sequence when the need is to reset the stack pointer and jump to the very first address in microprogram memory. The Jump 0 instruction does not change the contents of the register/counter.

INSTRUCTION 1 – CONDITIONAL JUMP TO SUBROUTINE (CJS)

The Conditional Jump to Subroutine instruction is the one used to call microprogram subroutines. The subroutine address will be contained in the pipeline register and presented at the D inputs. If the condition code test is passed, a branch is taken to the subroutine. Referring to the flow diagram for the IDT39C10s shown in Figure 1, we see that the content of the microprogram counter is 68. This value is pushed onto the stack and the top of stack pointer is incremented. If the test is failed, this Conditional Jump to Subroutine instruction behaves as a simple continue. That is, the content of microinstruction address 68 is executed next.

INSTRUCTION 2 – JUMP MAP (JMAP)

This sequencer instruction can be used to start different microprogram routines based on the machine instruction opcode. This is typically accomplished by using a mapping PROM as an input to the D inputs on the microprogram sequencer. The JMAP instruction branches to the address appearing on the D inputs. In the flow diagram shown in Figure 1, we see that the branch actually will be to the contents of microinstruction 85 and this instruction will be executed next.

INSTRUCTION 3 – CONDITIONAL JUMP PIPELINE (CJP)

The simplest branching control available in the IDT39C10 microprogram sequencers is that of conditional jump to address. In this instruction, the jump address is usually contained in the microinstruction pipeline register and presented to the D inputs. If the test is passed, the jump is taken while, if the test fails, this instruction executes as a simple continue. In the example shown in the flow diagram of Figure 1, we see that if the test is passed, the next microinstruction to be executed is the content of address 25. If the test is failed, the microcode simply continues to the contents of the next instruction.

INSTRUCTION 4 – PUSH/CONDITIONAL LOAD COUNTER (PUSH)

With this instruction, the counter can be conditionally loaded during the same instruction that pushes the current value of the microprogram counter on to the stack. Under any condition independent of the conditional testing, the microprogram counter is pushed on to the stack. If the conditional test is passed, the counter will be loaded with the value on the D inputs to the sequencer. If the test fails, the contents of the counter will not change. The PUSH/Conditional Load Counter instruction is used in conjunction with the loop instruction (Instruction 13), the repeat file based on the counter instruction (Instruction 9) or the 3-way branch instruction (Instruction 15).

INSTRUCTION 5 – CONDITIONAL JUMP TO SUBROUTINE R/PL (JSRP)

Subroutines may be called by a Conditional Jump Subroutine from the internal register or from the external pipeline register. In this instruction the contents of the microprogram counter are pushed on the stack and the branch address for the subroutine call will be taken from either the internal register/counter or the external pipeline register presented to the D inputs. If the conditional test is passed, the subroutine address will be taken from the pipeline register. If the conditional test fails, the branch address is taken from the internal register/counter. An example of this is shown in the flow diagram of Figure 1.

INSTRUCTION 6 – CONDITIONAL JUMP VECTOR (CJV)

The Conditional Jump Vector instruction is similar to the Jump Map instruction in that it allows a branch operation to a microinstruction as defined from some external source, except that it is conditional. The Jump Map instruction is unconditional. If the conditional test is passed, the branch is taken to the new address on the D inputs. If the conditional test is failed, no branch is taken but rather the microcode simply continues to the next sequential microinstruction. When this instruction is executed, the $\overline{VECT}$ output is LOW unconditionally. Thus, an external 12-bit field can be enabled on to the D inputs of the microprogram sequencer.

INSTRUCTION 7 – CONDITIONAL JUMP R/PL (JRP)

The Conditional Jump register/counter or external pipeline register always causes a branch in microcode. This jump will be to one of two different locations in the microcode address space. If the test is passed, the jump will be to the address presented on the D inputs to the microprogram sequencer. If the conditional test fails, the branch will be to the address contained in the internal register/counter.

INSTRUCTION 8 – REPEAT LOOP COUNTER NOT EQUAL TO 0 (RFCT)

This instruction utilizes the loop counter and the stack to implement microprogrammed loops. The start address for the loop would be initialized by using the PUSH/Conditional Load Counter instruction. Then, when the repeat loop instruction is executed, if the counter is not equal to 0, the next microword address will be taken from the stack. This will cause a loop to be executed as shown in the Figure 1 flow diagram. Each time the microcode sequence goes around the loop, the counter is decremented. When the counter reaches 0, the stack will be popped and the microinstruction address will be taken from the microprogram counter. This instruction performs a timed wait or allows a single sequence to be executed the desired number of times. Remember, the actual number of loops performed is equal to the value in the counter plus 1.

INSTRUCTION 9 – REPEAT PIPELINE COUNTER NOT EQUAL TO 0 (RPCT)

This instruction is another technique for implementing a loop using the counter. Here, the branch address for the loop is contained in the pipeline register. This instruction does not use the stack in any way as a part of its implementation. As long as the counter is not equal to 0, the next microword address will be taken from the D inputs of the microprogram sequencer. When the counter reaches 0, the internal multiplexer will select the address source from the microprogram counter, thus causing the microcode to continue on and leave the loop.

INSTRUCTION 10 – CONDITIONAL RETURN (CRTN)

The Conditional Return instruction is used for terminating subroutines. The fact that it is conditional allows the subroutine either to be ended or to continue. If the conditional test is passed, the address of the next microinstruction will be taken from the stack and it will be popped. If the conditional test fails, the next microinstruction address will come from the internal microprogram counter. This is depicted in the flow diagram of Figure 1. It is important to remember that every subroutine call must somewhere be followed by a return from subroutine call in order to have an equal number of pushes and pops on the stack.

INSTRUCTION 11 – CONDITIONAL JUMP PIPELINE AND POP (CJPP)

The Conditional Jump Pipeline and Pop instruction is a technique for exiting a loop from within the middle of the loop. This is depicted fully in the flow diagram for the IDT39C10s as shown in Figure 1. The conditional test input for this instruction results in a branch being taken if the test is passed. The address selected will be that on the D inputs to the microprogram sequencer and, since the loop is being terminated, the stack will be popped. Should the test be failed on the conditional test inputs,the microprogram will simply continue to the next address as taken from the microprogram counter. The stack will not be affected if the conditional test input is failed.

INSTRUCTION 12 – LOAD COUNTER AND CONTINUE (LDCT)

The Load Counter and Continue instruction is used to place a value on the D inputs in the register/counter and continue to the next microinstruction.

INSTRUCTION 13 – TEST END OF LOOP (LOOP)

The Test End of Loop instruction is used as a last instruction in a loop associated with the stack. During this instruction, if the conditional test input is failed, the loop branch address will be that on the stack. Since we may go around the loop a number of times, the stack is not popped. If the conditional test input is passed, then the loop is terminated and the stack is popped. Notice that the loop instruction requires a PUSH to be performed at the instruction immediately prior to the loop return address. This is necessary so as to have the correct address on the stack before the loop operation. It is for this reason that the stack pointer always points to the last thing written on the stack.

INSTRUCTION 14 – CONTINUE (CONT)

Continue is a simple instruction where the address for the microinstruction is taken from the microprogram counter. This instruction simply causes sequential program flow to the next microinstruction in microcode memory.

INSTRUCTION 15 – THREE WAY BRANCH (TWB)

The Three-Way Branch instruction is used for looping while waiting for a conditional event to come true. If the event does not come true after some number of microinstructions, then a branch is taken to another microprogram sequence. This is depicted in Figure 1 showing the IDT39C10's flow diagram and is also described in full detail in the IDT39C10's instruction operational summary. Operation of the instruction is such that any time the external conditional test input is passed, the next microinstruction will be that associated with the program counter and the loop will be left. The stack is also popped. Thus, the external test input overrides the other possibilities. Should the external conditional test input not be true, the rest of the operation is controlled by the internal counter. If the counter is not equal to 0, the loop is taken by selecting the address on the top of the stack as the address out of the Y outputs of the IDT39C10s. In addition, the counter is decremented. Should the external conditional test input be failed and the counter also have counted to 0, this instruction "times out". The result is that the stack is popped and a branch is taken to the address presented to the D inputs of the IDT39C10 microprogram sequencers. This address is usually provided by the external pipeline register.

CONDITIONAL TEST

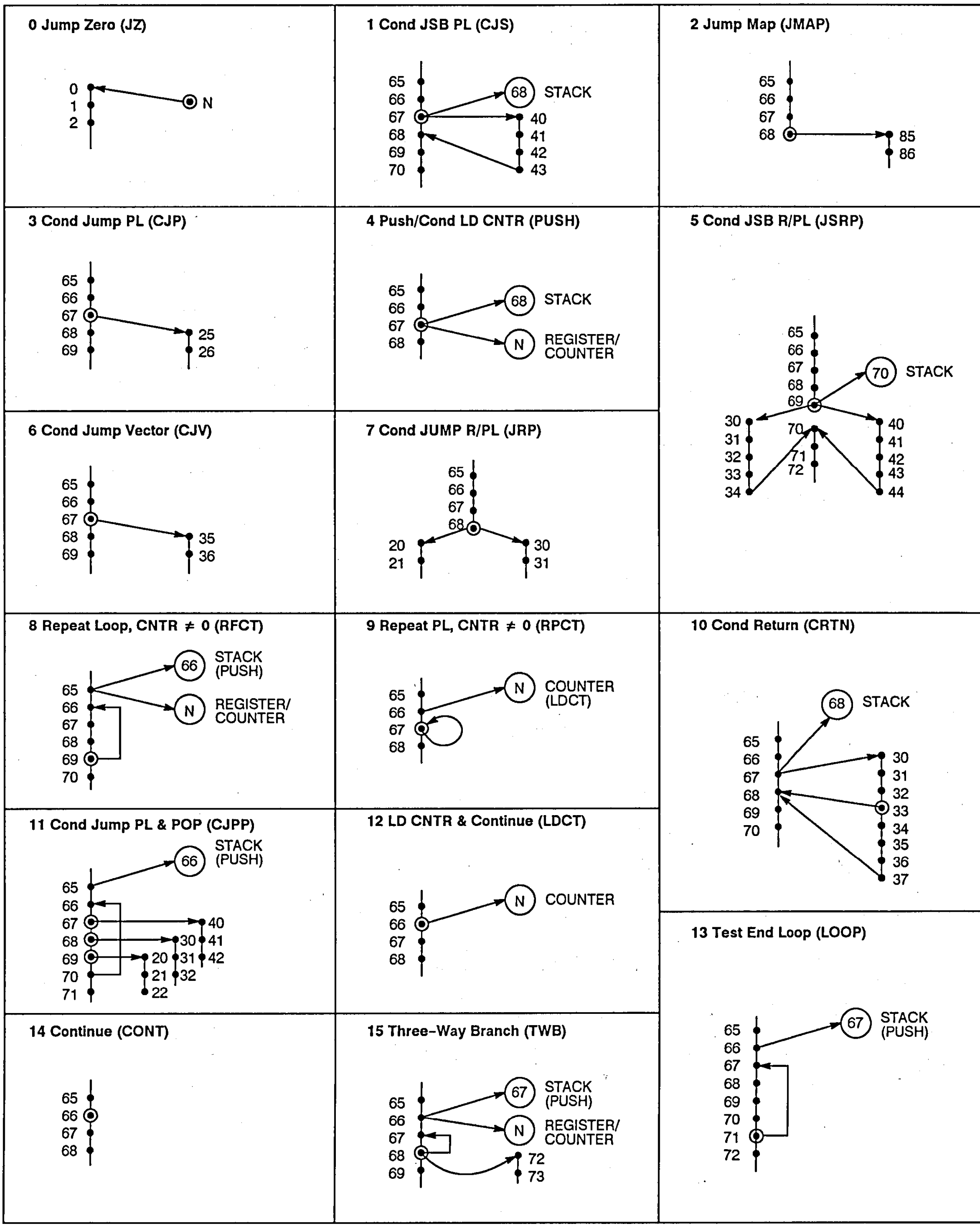
Throughout this discussion we have talked about microcode passing the conditional test. There are actually two inputs associated with the conditional test input. These include the $\overline{CCEN}$ and the $\overline{CC}$ inputs. The $\overline{CCEN}$ input is a condition code enable. Whenever the $\overline{CCEN}$ input is HIGH, the $\overline{CC}$ input is ignored and the device operates as though the $\overline{CC}$ input were true (LOW). Thus, a fail of the external test condition can be defined as $\overline{CCEN}$ equals LOW and $\overline{CC}$ equals HIGH. A pass condition is defined as a $\overline{CCEN}$ equal to HIGH or a $\overline{CC}$ equal to LOW. It is important to recognize the full function of the condition code enable and the condition code inputs in order to understand when the test is passed or failed.

IDT39C10 INSTRUCTION OPERATIONAL SUMMARY

$I_3 - I_0$	MNEMONIC	CC	COUNTER TEST	STACK	ADDRESS SOURCE	REGISTER/ COUNTER	ENABLE SELECT
0	JZ	X	X	CLEAR	0	NC	$\overline{PL}$
1	CJS	PASS FAIL	X X	PUSH NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
2	JMAP	X	X	NC	D	NC	$\overline{MAP}$
3	CJP	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
4	PUSH	PASS FAIL	X X	PUSH PUSH	PC PC	LOAD NC	$\overline{PL}$ $\overline{PL}$
5	JSRP	PASS FAIL	X X	PUSH PUSH	D R	NC NC	$\overline{PL}$ $\overline{PL}$
6	CJV	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{VECT}$ $\overline{VECT}$
7	JRP	PASS FAIL	X X	NC NC	D R	NC NC	$\overline{PL}$ $\overline{PL}$
8	RFCT	X X	= 0 NOT = 0	POP NC	PC STACK	NC DEC	$\overline{PL}$ $\overline{PL}$
9	RPCT	X X	= 0 NOT = 0	NC NC	PC D	NC DEC	$\overline{PL}$ $\overline{PL}$
10	CRTN	PASS FAIL	X X	POP NC	STACK PC	NC NC	$\overline{PL}$ $\overline{PL}$
11	CJPP	PASS FAIL	X X	POP NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
12	LDCT	X	X	NC	PC	LOAD	$\overline{PL}$
13	LOOP	PASS FAIL	X X	POP NC	PC STACK	NC NC	$\overline{PL}$ $\overline{PL}$
14	CONT	X	X	NC	PC	NC	$\overline{PL}$
15	TWB	PASS PASS FAIL FAIL	= 0 NOT = 0 = 0 NOT = 0	POP POP POP NC	PC PC D STACK	NC DEC NC DEC	$\overline{PL}$ $\overline{PL}$ $\overline{PL}$ $\overline{PL}$

NC = No Change; DEC = Decrement

FIGURE 1. IDT39C10B FLOW DIAGRAMS



8

IDT39C10 INSTRUCTIONS

$I_3 - I_0$	MNEMONIC	NAME	REG/ CNTR CON-TENTS	FAIL $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH		PASS $\overline{CCEN}$ = HIGH or $\overline{CC}$ = LOW		REG/ CNTR	ENABLE
				Y	STACK	Y	STACK		
0	JZ	Jump Zero	X	0	CLEAR	0	CLEAR	HOLD	$\overline{PL}$
1	CJS	Cond JSB PL	X	PC	HOLD	D	PUSH	HOLD	$\overline{PL}$
2	JMAP	Jump Map	X	D	HOLD	D	HOLD	HOLD	$\overline{MAP}$
3	CJP	Cond Jump PL	X	PC	HOLD	D	HOLD	HOLD	$\overline{PL}$
4	PUSH	PUSH/Cond Ld Cntr	X	PC	PUSH	PC	PUSH	Note 1	$\overline{PL}$
5	JSRP	Cond JSB R/PL	X	R	PUSH	D	PUSH	HOLD	$\overline{PL}$
6	CJV	Cond Jump Vector	X	PC	HOLD	D	HOLD	HOLD	$\overline{VECT}$
7	JRP	Cond Jump R/PL	X	R	HOLD	F	HOLD	DEC	$\overline{PL}$
8	RFCT	Repeat Loop, CNTR ≠ 0	≠ 0	F	HOLD	F	HOLD	DEC	$\overline{PL}$
			= 0	PC	POP	PC	POP	HOLD	$\overline{PL}$
9	RPCT	Repeat PL, CNTR ≠ 0	≠ 0	D	HOLD	D	HOLD	DEC	$\overline{PL}$
			= 0	PC	HOLD	PC	HOLD	HOLD	$\overline{PL}$
10	CRTN	Cond RTN	X	PC	HOLD	F	POP	HOLD	$\overline{PL}$
11	CJPP	Cond Jump PL & POP	X	PC	HOLD	D	POP	HOLD	$\overline{PL}$
12	LDCT	LD Contr & Continue	X	PC	HOLD	PC	HOLD	LOAD	$\overline{PL}$
13	LOOP	Test End Loop	X	F	HOLD	PC	POP	HOLD	$\overline{PL}$
14	CONT	Continue	X	PC	HOLD	PC	HOLD	HOLD	$\overline{PL}$
15	TWB	Three-Way Branch	≠ 0	F	HOLD	PC	POP	DEC	$\overline{PL}$
			= 0	D	POP	PC	POP	HOLD	$\overline{PL}$

NOTE:

1. If $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH, hold; else load. X = Don't Care

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER (1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ±10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level [4]		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level [4]		–	–	0.8	V
I_{IH}	Input High Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10	µA
			V_O = V_{CC} (max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V [3]		-30	–	–	mA
I_{CCQH}	Quiescent Power Supply Current CP = H	V_{CC} = Max. $V_{HC} \leq V_{IH}$, $V_{IL} \leq V_{LC}$ f_{CP} = 0, CP = H		–	35	50	mA
I_{CCQL}	Quiescent Power Supply Current CP = L	V_{CC} = Max. $V_{HC} \leq V_{IH}$, $V_{IL} \leq V_{LC}$ f_{CP} = 0, CP = L		–	35	50	mA
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IH} = 3.4V, f_{CP} = 0		–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IH}$, $V_{IL} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	1.0	3.0	mA/ MHz
			COM'L.	–	1.0	1.5	
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \leq V_{IH}$, $V_{IL} \leq V_{LC}$	MIL.	–	45	80	mA
			COM'L.	–	45	65	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	50	90	
			COM'L.	–	50	75	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock Input frequency

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large V_{CC} current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

IDT39C10C AC ELECTRICAL CHARACTERISTICS

I. SET-UP AND HOLD TIMES

INPUTS	$t_{(s)}$		$t_{(h)}$		UNIT
	COM'L.	MIL.	COM'L.	MIL.	
$D_I \rightarrow R$	6	7	0	0	ns
$D_I \rightarrow PC$	13	15	0	0	ns
I_{0-3}	23	25	0	0	ns
$\overline{CC}$	15	18	0	0	ns
$\overline{CCEN}$	15	18	0	0	ns
CI	6	7	0	0	ns
$\overline{RLD}$	11	12	0	0	ns

II. COMBINATIONAL DELAYS

INPUTS	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		UNIT
	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
D_{0-11}	12	15	–	–	–	–	ns
I_{0-3}	20	25	13	15	–	–	ns
$\overline{CC}$	16	20	–	–	–	–	ns
$\overline{CCEN}$	16	20	–	–	–	–	ns
CP	28	33	–	–	22	25	ns
$\overline{OE}$ [1]	10/10	13/13	–	–	–	–	ns

NOTE:
1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF.

III. CLOCK REQUIREMENTS

	COM'L.	MIL.	UNIT
Minimum clock LOW time	18	20	ns
Minimum clock HIGH time	17	20	ns
Minimum clock period	35	40	ns

IDT39C10B AC ELECTRICAL CHARACTERISTICS

I. SET-UP AND HOLD TIMES

INPUTS	$t_{(s)}$		$t_{(h)}$		UNIT
	COM'L.	MIL.	COM'L.	MIL.	
$D_I \rightarrow R$	16	16	0	0	ns
$D_I \rightarrow PC$	30	30	0	0	ns
I_{0-3}	35	38	0	0	ns
$\overline{CC}$	24	35	0	0	ns
$\overline{CCEN}$	24	35	0	0	ns
CI	18	18	0	0	ns
$\overline{RLD}$	19	20	0	0	ns

II. COMBINATIONAL DELAYS

INPUTS	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		UNIT
	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
D_{0-11}	20	25	–	–	–	–	ns
I_{0-3}	35	40	30	35	–	–	ns
$\overline{CC}$	30	36	–	–	–	–	ns
$\overline{CCEN}$	30	36	–	–	–	–	ns
CP	40	46	–	–	31	35	ns
$\overline{OE}$ [1]	25/27	25/30	–	–	–	–	ns

NOTE:
1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF.

III. CLOCK REQUIREMENTS

	COM'L.	MIL.	UNIT
Minimum clock LOW time	20	25	ns
Minimum clock HIGH time	20	25	ns
Minimum clock period	50	51	ns

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 3

IDT39C10B INPUT/OUTPUT INTERFACE CIRCUIT

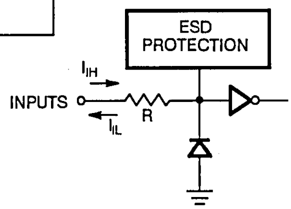


Figure 1. Input Structure

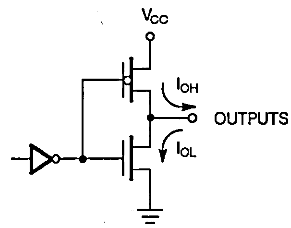
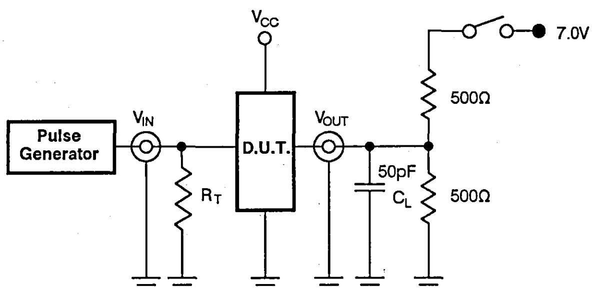


Figure 2. Output Structure

TEST LOAD CIRCUIT



TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All other Outputs	Open

DEFINITIONS

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 3. Switching Test Circuits

ORDERING INFORMATION

IDT 39C10 (Device Type) X (Speed) X (Package) X (Process/ Temperature Range)

Process/Temperature Range:
- Blank — Commercial (0°C to +70°C)
- B — Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:
- P — Plastic DIP
- C — Sidebraze DIP
- D — CERDIP
- J — PLCC
- L — LCC

Speed:
- B — Fast 12-Bit Microprogram Sequencer
- C — Ultra-fast 12-Bit Microprogram Sequencer

8

Integrated Device Technology, Inc.

4-BIT CMOS MICROPROCESSOR SLICE

IDT39C203
IDT39C203A

MICROSLICE™ PRODUCT

FEATURES:

- Fast
  - IDT39C203 matches 29203 speeds
  - IDT39C203A 20% speed upgrade
- Low-power CMOS
  - Military: 55mA (max.)
  - Commercial: 50mA (max.)
- Pin-compatible, performance-enhanced functional replacement for the 29203
- Cascadable to 8, 12, 16, etc. bits
- Infinitely expandable register file
- Improved I/O capability
  - DA, DB and Y ports are bidirectional
- Performs BCD arithmetic
  - Features automatic BCD add, subtract and conversion between binary and BCD
- On-chip parity generation and sign extension logic
- On-chip normalization logic
- On-chip multiplication division logic
- Packaged in 48-pin plastic and sidebraze DIP, 52-pin LCC
- Military product available compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT39C203s are four-bit expandable, high-performance CMOS microprocessor slices. Along with the standard features associated with the IDT39C01s and IDT39C03s, the IDT 39C203s also incorporate additional enhancements for arithmetic-oriented processors.

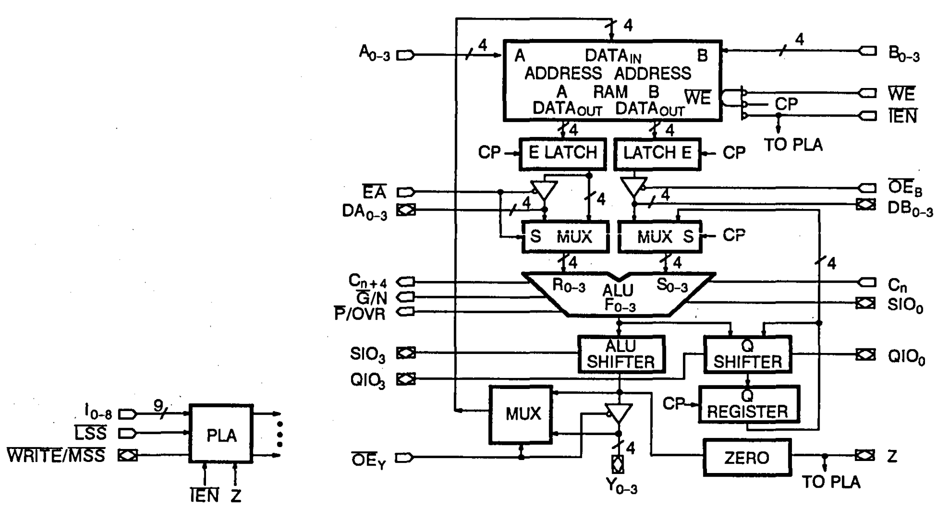
These extremely low-power yet high-speed three-port three-address architectured microprocessors consist of a 16-word by 4-bit dual-port RAM with latches on both outputs, high-performance ALU and shifter, a flexible Q register with shifter input, and nine-bit instruction decoder. Additionally, special instructions which allow the easy implementation of multiplication, division, normalization, BCD arithmetic and conversion are standard on the IDT39C203s. Both devices are easily expandable in 4-bit increments.

They are pin-compatible, functional replacements for all versions of the 29203. The fastest version, the IDT 39C203A, is a 20% speed upgrade from the normal 29203 device. The IDT39C203 meets the 29203 speeds.

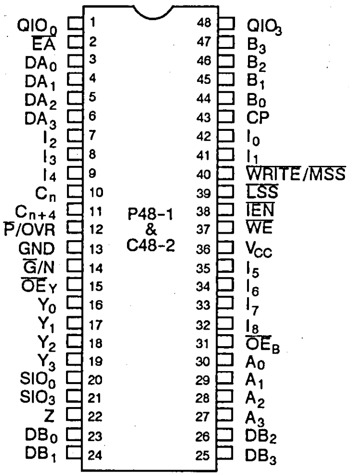
The IDT39C203s are fabricated using CEMOS™, CMOS technology designed for high-performance and high-reliability.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

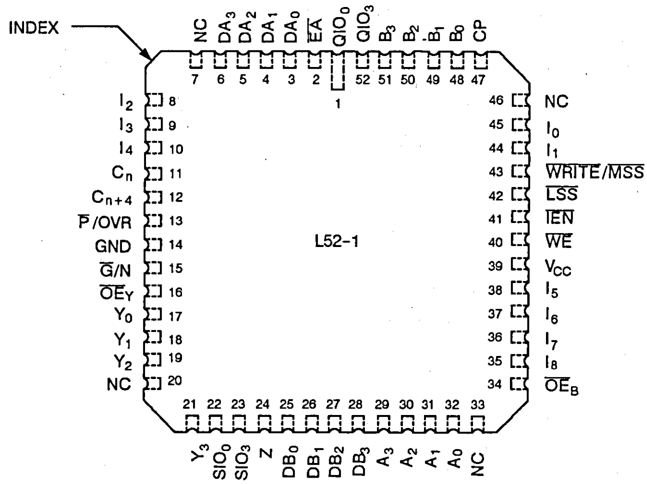
FUNCTIONAL BLOCK DIAGRAM



CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.



DIP
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
$A_0 - A_3$	I	Four address inputs to the RAM containing the address of the RAM word appearing at output port A.
$B_0 - B_3$	I	Four address inputs to the RAM which selects one of the words in the RAM, the contents of which is displayed through the B port. It also selects the location into which new data can be written when the $\overline{WE}$ input and CP input are low.
DA_{0-3}	I/O	Four-bit bidirectional data pins for entering external data into the ALU. The DA lines act as either RAM port A output data or as input operand R to the ALU.
DB_{0-3}	I/O	Four-bit bidirectional data pins for entering external data into the ALU. The DB lines act as either RAM port B output data or as input operand S to the ALU.
$\overline{WE}$	I	The RAM write enable input which, when LOW, causes the Y I/O port data to be written into the RAM when the CP input is low. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.
$\overline{EA}$	I	Enable input which, when HIGH, selects DA_{0-3} as the ALU R operand and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-3} output data.
$\overline{OE}_B$	I	Output enable, which, when HIGH selects DB_{0-3} as the ALU S operand, and, when LOW, selects RAM output B as the ALU S operand and the DB_{0-3} output data.
$SIO_0 - SIO_3$	I/O	Bidirectional serial shift inputs/outputs for the ALU shifter. SIO_0 is an input SIO_3 an output during a shift-up operation. SIO_3 is an input and SIO_0 an output during a shift-down operation. Refer to Tables 3 and 4 for an exact definition of of these pins.
$QIO_0 - QIO_3$	I/O	Bidirectional serial shift inputs/outputs for the ALU shifter. They operate like the SIO_0 and SIO_3 pins. Refer to Tables 3 and 4 for an exact definition of these pins.
C_n	I	Carry-in input to the ALU.
$\overline{IEN}$	I	Instruction enable input. When LOW, it enables writing into the Q register and the Sign Compare flip-flop and RAM. When HIGH, the Q register and the Sign Compare flip-flop are in hold mode. On the IDT39C203, $\overline{EIN}$ does not affect WRITE but internally disables the RAM write enable.
$\overline{LSS}$	I	Input pin, when held LOW, causes the chip to act as the Least Significant Slice ($\overline{LSS}$) of an IDT39C203 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE/MSS}$ pin. When $\overline{LSS}$ is held HIGH, the chip acts as either an Intermediate or Most Significant Slice ($\overline{MSS}$) and the $\overline{WRITE}$ output buffer is disabled.
$\overline{WRITE/MSS}$	I/O	The write output signal appears at this pin when $\overline{LSS}$ is held LOW. When an instruction which causes data to be written into the RAM is being executed, the $\overline{WRITE}$ signal is LOW. When $\overline{LSS}$ is HIGH, $\overline{WRITE/MSS}$ is an input pin; holding it HIGH programs the chip to operate as an Intermediate Slice (IS) and holding it LOW programs the chip to operate as the Most Significant Slice (MSS).
C_{n+4}	O	This output indicates the carry-out of the ALU. Refer to Table 5 for an exact definition of this pin.
Z	I/O	An open collector input/out pin. When HIGH, it indicates that all outputs are LOW. Z is used as an input pin for some special functions. Refer to Table 5 for an exact definition of this pin.
$\overline{G}$/N	O	$\overline{G}$ indicates the carry generate function at the Least Significant and Intermediate slices and indicates the sign (N) of the ALU result at the Most Significant Slice. Refer to Table 5 for an exact definition of this pin.
$\overline{OE}_Y$	I	A control input pin. When LOW the ALU shifter output data is enabled onto the Y_{0-3} lines. When HIGH the Y_{0-3} three-state output buffers are disabled.
CP	I	Clock input to the IDT39C203. The Sign Compare flip-flop and the Q register are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$ and CP is LOW, data is written in the RAM.
$\overline{P}$/OVR	O	$\overline{P}$ indicates the carry propagate function at the Least Significant and Intermediate slices and indicates the conventional two's complement overflow (OVR) signal at the Most Significant Slice. Refer to Table 5 for an exact definition of this pin.
Y_{0-3}	I/O	Four data inputs/outputs of the IDT39C203. Controlled by the $\overline{OE}_Y$ input, the ALU shifter output data can be enabled onto these lines or external data is written directly into the RAM using these lines as data inputs.
I_{0-8}	I	The nine instruction inputs used to select the IDT39C203 operation to be performed.

DEVICE ARCHITECTURE

The IDT39C203 is a CMOS high-performance 4-bit microprocessor slice cascadable to any number of bits (8, 12, 16, etc.). Its versatile microinstructions allow emulation of virtually any digital computer. The ALU sources, function and destination can be selected by the 9-bit microinstruction set. Key elements which make up this 4-bit microprocessor slice are: (1) the RAM file (a 16x4 dual-port RAM) with latches on both outputs, (2) high-performance ALU with shifter, (3) a flexible Q register with shifter input and (4) a nine-bit instruction decoder.

RAM FILE

RAM data is read from the A port as controlled by the 4-bit A address field input. Simultaneously, data can be read from the B port as defined by the 4-bit B address field input. If the same address is applied at both the A input field and the B input field, identical data will appear at the two respective output ports. Data is written into the RAM when $\overline{WE}$ and $\overline{IEN}$ are both LOW and the clock CP is LOW. Both the RAM output data latches are transparent, while the clock pulse CP is HIGH and latches the data when CP is low.

New data is written into the RAM word defined by the B address field. External data at the Y I/O port can be written directly into the RAM or ALU shifter output data can be enabled onto the Y I/O port and written into the RAM. The three-state output enable $\overline{OE}_B$ allows RAM B port data to be read at the DB I/O port, while $\overline{EA}$ performs the same function for the A port data the DA I/O port.

ALU

The ALU can perform seven arithmetic and nine logic operations on the two 4-bit input words S and R. Multiplexers at the ALU inputs allow selection of various pairs of ALU source operands. The $\overline{EA}$ input selects either external DA data or RAM A-port output data as the 4-bit R source operand. The $\overline{OE}_B$ and I_0 inputs provide selection of either RAM B port output or external DB data or the Q register output as the 4-bit S source operand. Also, during certain ALU operations, zeros are forced at the ALU operand inputs. Thus, the ALU can operate on data from two external sources, from an external and an internal source or from two internal sources. Table 1 shows all possible pairs of source operands as selected by $\overline{EA}$, $\overline{OE}_B$ and I_0 inputs.

Table 1. ALU Operand Sources[1]

$\overline{EA}$	I_0	$\overline{OE}_B$	ALU OPERAND R	ALU OPERAND S
L	L	L	Ram Output A	Ram Output B
L	L	H	Ram Output A	DB_{0-3}
L	H	X	Ram Output A	Q Register
H	L	L	DA_{0-3}	Ram Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

Note:
1. L= LOW, H=HIGH, X=DON'T CARE

The ALU performs special functions when instruction bits I_3, I_2, I_1 and I_0 are LOW. Table 4 defines these special functions and the operation which the ALU performs for each. When the ALU executes instructions other than the special functions, the operation is defined by instruction bits I_4, I_3, I_2 and I_1. Table 2 defines the operation as a function of these four instruction bits.

The IDT 39C203 may be cascaded in either a ripple carry or lookahead carry fashion. When configured as cascaded ALUs, the IDT39C203s must be programmed to be a Most Significant Slice (MSS), an Intermediate Slice (IS) or a Least Significant Slice (LSS) of the array. The carry generate ($\overline{G}$) and carry propagate ($\overline{P}$) signals that are necessary in a cascaded system are available as outputs on the IDT39C203 Least Significant and Intermediate slices.

The IDT39C203 provides a carry-out signal (C_{n+4}) which is available as an output of each slice. The carry-in (C_n) and carry-out (C_{n+4}) are both active HIGH. Two other status outputs are generated by the ALU. These are the negative (N) and the overflow (OVR). The N output indicates positive or negative results, while the OVR output indicates that the arithmetic operation performed exceeded the available two's complement range. Thus, the pins $\overline{G}$/N and $\overline{P}$/OVR indicate carry generate or propagate on the Least Significant and Intermediate slices and sign and overflow on the Most Significant Slice. Refer to Table 5 for an exact definition of these four signals.

Table 2. IDT39C203 ALU Functions[1]

I_4	I_3	I_2	I_1	I_0	ALU FUNCTIONS
L	L	L	L	L	Special Functions
L	L	L	L	H	F_i = HIGH
L	L	L	H	X	$F=S-R-1+C_n$
L	L	H	L	X	$F=R-S-1+C_n$
L	L	H	H	X	$F=R+S+C_n$
L	H	L	L	X	$F=S+C_n$
L	H	L	H	X	$F=\overline{S}+C_n$
L	H	H	L	L	Reserved Special Functions
L	H	H	L	H	$F=R+C_n$
L	H	H	H	L	Reserved Special Functions
L	H	H	H	H	$F=\overline{R}+C_n$
L	H	H	H	L	Special Functions
H	L	L	L	H	F_i = LOW
H	L	L	H	X	$F_i = \overline{R_i}$ AND S_i
H	L	H	L	X	F_i = Ri EXCLUSIVE NOR S_i
H	L	H	H	X	F_i = Ri EXCLUSIVE OR S_i
H	H	L	L	X	F_i = Ri AND S_i
H	H	L	H	X	F_i = Ri NOR S_i
H	H	H	L	X	F_i = Ri NAND S_i
H	H	H	H	X	F_i = Ri OR S_i

Note:
1. L= LOW, H=HIGH, i = 0 to 3, X = DON'T CARE

ALU SHIFTER

The ALU shifter shifts the ALU output data under instruction control. It can shift up one bit position (2F), shift down one bit position (F/2) or pass the ALU output non-shifted (F). An arithmetic shift operation shifts the data around the Most Significant (sign) Bit of the Most Significant Slice and a logical shift operation shifts the data through the Most Significant Bit. Figure 1 shows these shift patterns. The SIO_0 and SIO_3 are bidirectional serial shift input/output pins. During a shift-up operation, SIO_0 is generally an input while SIO_3 is an output; whereas, during a shift-down operation, SIO_0 is generally an output while SIO_3 acts as an input. Refer to Tables 3 and 4 for an exact definition of these pins.

The ALU shifter also provides sign extension and parity generating/checking capabilities. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, and Y_3 and be propagated to the SIO_3 output. A cascadable, five-bit parity generator/checker generates parity for the F_0, F_1, F_2 and F_3 ALU outputs, the SIO_3 input and, under instruction control, is made available at the SIO_0 output. Table 4 defines the special functions and the operation the ALU shifter performs for each instruction. For instructions other than the special functions, the ALU shifter operation is determined by instruction bits I_8, I_7, I_6 and I_5. Table 3 defines the ALU shifter operation as a function of these four bits.

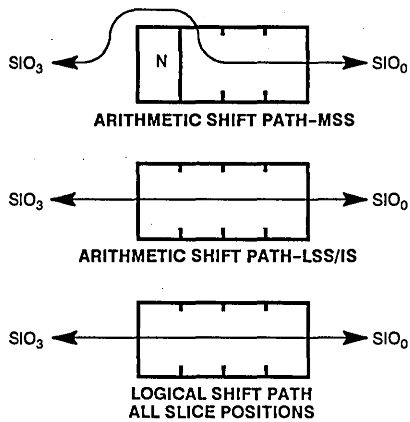


Figure 1.

Q REGISTER FILE

The Q register is a separate 4-bit file intended primarily for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. The ALU output (F) can be loaded into the Q register and/or the Q register can be selected as one of the ALU S operands. The shifter at the input to the Q register performs only logical shifts. It can shift-up the data one bit position (2Q) or down one bit position (Q/2). For a shift-up operation, QIO_0 acts as an input while QIO_3 acts as an output; whereas for a shift-down operation QIO_0 is an output and QIO_3 is an input. By connecting QIO_3 of the Most Significant Slice to SIO_0 of the Least Significant Slice, double-length arithmetic and logical shifting is possible with cascaded IDT39C203s.

Table 4 defines the special functions and the operations which the Q register and the shifter performs for selected instruction inputs. While executing instructions other than the special functions, the Q register and the shifter operation is controlled by instruction bits I_8, I_7, I_6 and I_5. Table 3 defines the Q register and shifter operation as a function of these four bits.

Table 3. ALU Destination Control for I_0 or I_1 or I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW[1]

						SIO_3		Y_3		Y_2								
I_8	I_7	I_6	I_5	HEX CODE	ALU SHIFTER FUNCTION	MOST SIG. SLICE	OTHER SLICES	MOST SIG. SLICE	OTHER SLICES	MOST SIG. SLICE	OTHER SLICES	Y_1	Y_0	SIO_0	$\overline{WRITE}$ /MSS	Q REG & SHIFTER FUNCTION	QIO_3	QIO_0
L	L	L	L	0	Arith F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Z	Z
L	L	L	H	1	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Z	Z
L	L	H	L	2	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log. Q/2 →Q	Input	Q_0
L	L	H	H	3	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log. Q/2 →Q	Input	Q_0
L	H	L	L	4	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	Hold	Z	Z
L	H	L	H	5	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	Log. Q/2 →Q	Input	Q_0
L	H	H	L	6	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	F→Q	Z	Z
L	H	H	H	7	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	F→Q	Z	Z
H	L	L	L	8	Arith . 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Z	Z
H	L	L	H	9	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Z	Z
H	L	H	L	A	Arith. F/2→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q →Q	Q_3	Input
H	L	H	H	B	Log. F/2→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q →Q	Q_3	Input
H	H	L	L	C	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	H	Hold	Z	Z
H	H	L	H	D	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	H	Log. 2Q →Q	Q_3	Input
H	H	H	L	E	SIO_0→Y_0, Y_1, Y_2, Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Z	Z
H	H	H	H	F	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	L	Hold	Z	Z

NOTE:
1. Parity = $F_3 \forall F_2 \forall F_1 \forall F_0 \forall SIO_3$, L = LOW Z = High Impedance $\forall$ = Exclusive OR, H = HIGH

INSTRUCTION DECODER

The internal control signals necessary for the operation of the IDT39C203 are generated by the instruction decoder as a function of the nine instruction inputs, I_{0-8}; the instruction enable input, $\overline{IEN}$; the $\overline{LSS}$ input; and the $\overline{MSS/WRITE}$ input/output.

The $\overline{WRITE}$ output is LOW when an instruction which writes data into the RAM is executed. Refer to Tables 3 and 4 for a definition of the $\overline{WRITE}$ output as a function of the instruction inputs. When $\overline{IEN}$ is HIGH, the $\overline{WRITE}$ output is forced HIGH and the Q register and Sign Compare flip-flop contents are preserved. When $\overline{IEN}$ is LOW, the $\overline{WRITE}$ output is enabled and the Q register and Sign Compare flip-flop can be written according to the IDT39C203s instruction. The Sign Compare flip-flop shown in Figure 2 is an on-chip flip-flop which is used during a divide operation.

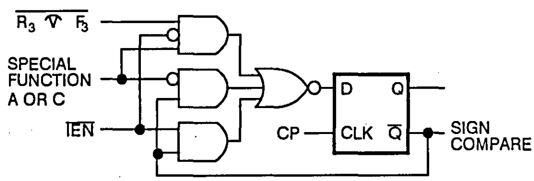


Figure 2. Sign Compare Flip-Flop

SLICE POSITION PROGRAMMING

Holding the $\overline{LSS}$ pin LOW programs the IDT39C203 slice (LSS) and enables the $\overline{WRITE}$ output signal onto the $\overline{MSS/WRITE}$ I/O pin. When $\overline{LSS}$ is tied HIGH, the $\overline{MSS/WRITE}$ pin becomes an input tying $\overline{MSS/WRITE}$ LOW programs the slice to operate as the Most Significant Slice (MSS); tying it HIGH causes the slice to operate as an Intermediate Slice. The $\overline{MSS/WRITE}$ pin should be tied HIGH through a resistor, independent of the LSS pin.

SPECIAL FUNCTIONS

Sixteen special functions are provided on the IDT39C203 which permit the implementation of the following operations:

- Single and double length normalization
- Two's complement division
- Unsigned and two's complement multiplication
- Conversion between two's complement and sign/magnitude representation
- Incrementation and decrementation by one or two
- BCD add, subtract, and divide by two
- Single and double-precision BCD-to binary and binary-to-BCD conversion

Adjusting a single-precision or double-precision floating-point number in order to bring its mantissa within a specified range can be performed using the single-length and double-length normalization operations. Three special functions can be used to perform a two's complement, non-restoring divide operation. They provide single and double-precision divide operations and can be performed in "n" clock cycles (where "n" is the number of bits in the quotient).

The unsigned multiply special function and the two two's complement multiply special functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in "n" clock cycles. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed due to the fact that the sign bit of the multiplier carries negative weight.

The sign/magnitude two's complement special function can be used to convert number representation systems. A number expressed in sign/magnitude representation can be converted to the two's complement representation, and vice-versa, in one clock cycle. Incrementing an unsigned or two's complement number by one or two is easily accomplished using the increment by one or two special functions.

In addition to BCD arithmetic special functions to add or subtract two BCD numbers, a BCD divide by two adjust instructions can be used to obtain a valid BCD representation after shifting a number down by one bit. The BCD/binary conversion special function instructions permit single and double-precision algorithms to convert from BCD-to-binary and from binary-to-BCD.

8

Table 4. Special Functions (7,8)

HEX $I_8I_7I_6I_5$	I_4	HEX $I_3I_2I_1I_0$	SPECIAL FUNCTION	ALU FUNCTION	ALU SHIFTER FUNCTION	SIO_3 MSS	SIO_3 OTHER SLICES	SIO_0	Q REGISTER & SHIFTER FUNCTION	QIO_3	QIO_0	$\overline{WRITE}$ /MSS
0	L	0	Unsigned Multiply	$F=S+C_n$ if $Z=L$ $F=R+S+C_n$ if $Z=H$	Log F/2→Y (1)	X	Input	F_0	Log Q/2 →Q	Input	Q_0	L
1	L	0	BCD to Binary Conversion	Note 4	Log F/2→Y	Input	Input	F_0	Log Q/2 →Q	Input	Q_0	L
1	H	0	Multiprecision BCD to Binary	Note 4	Log F/2→Y	Input	Input	F_0	Hold	X	Q_0	L
2	L	0	Two's Complement Multiply	$F=S+C_n$ if $Z=L$ $F=R+S+C_n$ if $Z=H$	Log F/2→Y (2)	X	Input	F_0	Log Q/2 →Q	Input	Q_0	L
3	L	0	Decrement by One or Two	$F=S-2+C_n$	F→Y	Input	Input	Parity	Hold	X	X	L
4	L	0	Increment by One or Two	$F=S+1+C_n$	F→Y	Input	Input	Parity	Hold	X	X	L
5	L	0	Sign/Magnitude Two's Complement	$F=S+C_n$ if $Z=L$ $F=S+C_n$ if $Z=H$	F→Y (3)	Input	Input	Parity	Hold	X	X	L
6	L	0	Two's Complement Multiply, Last Cycle	$F=S+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	L F/2→Y (2)	X	Input	F_0	Log Q/2 →Q	Input	Q_0	L
7	L	0	BCD Divide by Two	Note 4	F→Y	Input	Input	Parity	Hold	X	X	L
8	L	0	Single Length Normalize	$F=S+C_n$	F→Y	F_3	F_3	X	Log 2Q →Q	Q_3	Input	L
9	L	0	Binary to BCD Conversion	Note 5	Log 2F→Y	F_3	F_3	Input	Log 2Q →Q	Q_3	Input	L
9	H	0	Multiprecision Binary to BCD	Note 5	Log 2F→Y	F_3	F_3	Input	Hold	X	Input	L
A	L	0	Double Length Normalize and First Divide Op	$F=S+C_n$	Log 2F→Y	$R_3 \forall F_3$	F_3	Input	Log 2Q →Q	Q_3	Input	L
B	L	0	BCD Add	$F=R+S+C_n$ BCD (6)	F→Y	0	0	X	Hold	X	X	L
C	L	0	Two's Complement Divide	$F=S+R+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	Log 2F→Y	$R_3 \forall F$	F_3	Input	Log 2Q →Q	Q_3	Input	L
D	L	0	BCD Subtract	$F=R-S-1+C_n$ BCD (6)	F→Y	0	0	X	Hold	X	X	L
E	L	0	Two's Complement Divide Correction and Remainder	$F=S+R+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	F→Y	F_3	F_3	X	Log 2Q →Q	Q_3	Input	L
F	L	0	BCD Subtract	$F=S-R-1+C_n$ BCD (6)	F→Y	0	0	X	Hold	X	X	L

NOTES:
1. At the Most Significant Slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the Most Significant Slice only, $F_3 \forall$ OVR is internally gated to the Y_3 output.
3. At the Most Significant Slice only, $S_3 \forall F_3$ is generated the Y_3 output.
4. On each slice, F = S if magnitude of S_{0-3} is less than 8, and F = S minus three if magnitude of S_{0-3} is 8 or greater.
5. On each slice, F = S if magnitude of S_{0-3} is less than 5, and F = S plus three if magnitude of S_{0-3} is 5 or greater. Addition is modulo 16.
6. Additions and Subtractions are BCD adds and subtracts. Results are undefined if R or S are not in valid BCD format.
7. The Q register cannot be used explicitly as an operand for any special functions. It is defined implicitly within the functions.
8. L = LOW, H = HIGH, X = Don't Care, $\forall$ = Exclusive OR, PARITY = $SIO_3 \forall F_3 \forall F_2 \forall F_1 \forall F_0$

Table 5. IDT39C203 Status Outputs

(HEX) I_{8-5}	(HEX) I_{4-1}	I_0	Gi (i=0 to 3)	Pi (i=0 to 3)	C_{n+4}	$\overline{P}$/OVR MOST SIG. SLICE	$\overline{P}$/OVR OTHER SLICES	$\overline{G}$/N MOST SIG. SLICE	$\overline{G}$/N OTHER SLICES	Z ($\overline{OE}_Y$ = L) MOST SIG. SLICE	Z ($\overline{OE}_Y$ = L) INTER-MEDIATE SLICE	Z ($\overline{OE}_Y$ = L) LEAST SIG. SLICE
X	0	H	0	1	0	0	0	F_3	G	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	1	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	2	X	$R_i \wedge \overline{S}_i$	$R_i \vee \overline{S}_i$	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	4	X	0	S_i	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	5	X	0	$\overline{S}_i$	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	6	H	0	R_i	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	7	H	0	$\overline{R}_i$	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	8	H	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	9	X	$\overline{R}_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	B	X	$\overline{R}_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	D	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	E	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	F	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
0	0	L	0 if Z=L $R_i \wedge S_i$ if Z=H	S_i if Z=L $R_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
1	0	L	0	S_i	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
1	8	L	0	S_i	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
2	0	L	0 if Z=L $R_i \wedge S_i$ if Z=H	S_i if Z=L $R_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
3	0	L	Note 6	Note 7	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
4	0	L	Note 1	Note 2	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
5	0	L	0	S_i if Z=L S_i if Z=H	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3 if Z=L $F_3 \veebar S_3$ if Z=H	$\overline{G}$	S_3	Input	Input
6	0	L	0 if Z=L $\overline{R}_i \wedge S_i$ if Z=H	S_i if Z=L $R_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
7	0	L	0	S_i	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
8	0	L	0	S_i	Note 3	$Q_2 \veebar Q_1$	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
9	0	L	0	S_i	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
9	8	L	0	S_i	0	0	0	F_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$Q_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
A	0	L	0	S_i	Note 4	$F_2 \veebar F_1$	$\overline{P}$	F_3	$\overline{G}$	Note 5	Note 5	Note 5
B	0	L	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	Note 8	Note 8	Note 9	Note 9	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
C	0	L	$R_i \wedge S_i$ if Z=L $\overline{R}_i \wedge S_i$ if Z=H	$R_i \vee S_i$ if Z=L $\overline{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
D	0	L	$R_i \wedge \overline{S}_i$	$R_i \vee \overline{S}_i$	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
E	0	L	$R_i \wedge S_i$ if Z=L $\overline{R}_i \wedge S_i$ Z=H	$R_i \vee S_i$ if Z=L $\overline{R}_i \vee S_i$ Z=H	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
F	0	L	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$

Notes on next page

8

NOTES:
1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$.
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $P_I = S_I$.
3. At the most significant slice, $C_{n+4} = Q_3 \veebar Q_2$. At other slices $C_{n+4} = G \vee PC_n$.
4. At the most significant slice, $C_{n+4} = F_3 \veebar F_2$. At other slices $C_{n+4} = G \vee PC_n$.
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3 \overline{F}_0 \overline{F}_1 \overline{F}_2 \overline{F}_3$.
6. If $\overline{LSS}$ is LOW, $G_0 = 0$ and $G_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = S_{0,1,2,3}$.
7. If $\overline{LSS}$ is LOW, $P_0 = S$ and $P_{1,2,3} = S$. If $\overline{LSS}$ is HIGH, $P_{0,1,2,3} = 1$.
8. On all slices $\overline{P} = (\overline{P}_0 + \overline{P}_3)(\overline{P}_0 + \overline{P}_2)(\overline{P}_0 + \overline{G}_1 + \overline{P}_2)$.
9. On all slices $\overline{G} = \overline{G}_3 (\overline{G}_0 + \overline{G}_1 + \overline{P}_2)(\overline{G}_0 + \overline{G}_1)(\overline{P}_1 + \overline{G}_2)(\overline{P}_3 + \overline{P}_1 \bullet \overline{P}_2 \bullet \overline{G}_0)$.
10. L = LOW = 0, H = HIGH = 1, V = OR, $\wedge$ = AND, $\veebar$ = EXCLUSIVE OR, $P = P_3P_2P_1P_0$, $G = G_3 \vee G_2P_3 \vee G_1P_2P_3 \vee G_1P_1P_2P_3$, $C_{n+3} = G_2 \vee G_1P_2 \vee G_0P_1P_2 \vee C_nP_0P_1P_2 \vee C_nP_0P_1P_2$

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (Commercial)
$T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (Military)
$V_{LC} = 0.2V$
$V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level [4]		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level [4]		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., $V_{IN} = V_{CC}$		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -300µA$	V_{HC}	V_{CC}	–	V
			$I_{OH} = -12mA$ MIL.	2.4	4.3	–	
			$I_{OH} = -15mA$ COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 300µA$	–	GND	V_{LC}	V
			$I_{OL} = 20mA$ MIL.	–	0.3	0.5	
			$I_{OL} = 24mA$ COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	$V_O = 0V$	–	-0.1	-10	µA
			$V_O = V_{CC}$	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V [3]		-30	–	–	mA
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = H		–	5	15	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = L		–	5	15	mA
I_{CCT}	Quiescent Input Power Supply [5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		–	0.25	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	0.5	2.0	mA/ MHZ
			COM'L.	–	0.5	1.5	
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	MIL.	–	10	35	mA
			COM'L.	–	10	30	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	20	55	
			COM'L.	–	20	50	

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{CP} = Clock input frequency.

8

IDT39C203A GUARANTEED COMMERCIAL RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C203A over the commercial operating range of 0 to +70°C with V_{CC} from 4.75 to 5.25V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Table 12. Clock and Write Pulse Characteristics All Functions

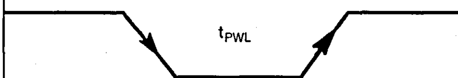
Minimum Clock Low Time	24ns
Minimum Clock High Time	24ns
Minimum Time CP and $\overline{WE}$ both Low to Write	12ns

Table 13. Enable/Disable Times All Functions[1]

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	20	17
$\overline{OE}_B$	DB	20	17
$\overline{EA}$	DA	20	17
I_8	SIO	20	17
I_8	QIO	30	30
$I_{8,7,6,5}$	QIO	30	30
$I_{4,3,2,1,0}$	QIO	30	28
$\overline{LSS}$	$\overline{WRITE}$	20	17

NOTE:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Table 14. Set-up and Hold Times All Functions



		HIGH-TO-LOW		LOW-TO-HIGH		
FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	11	3	Store Y in RAM/Q[1]
$\overline{WE}$ HIGH	CP	12	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	12	0	Write into RAM
A, B Source	CP	16	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	5	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	14	3	Shift Q
$I_{8,7,6,5}$	CP	10	–	16	0	Write into Q[2]
$\overline{IEN}$ HIGH	CP	19	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	17	0	Write into Q
$I_{4,3,2,1,0}$	CP	14	–	26	0	Write into Q[2]

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. IEN controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L → H and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

IDT39C203A GUARANTEED COMMERCIAL RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT/DECREMENT BY ONE OR TWO INSTRUCTIONS (SF3, SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	54	44	42	59	49	54	22	–	–	33	50	62
DA, DB	46	40	32	52	43	46	–	–	–	28	47	52
C_n	26	14	–	28	22	22	–	–	–	18	24	30
I_{8-0}	51	51	40	58	49	50	–	27	21	40	50	59
CP	46	34	34	49	43	46	18	–	18	30	43	48
SIO_0, SIO_3	18	–	–	23	–	–	–	–	–	–	23	15
$\overline{MSS}$	35	–	35	35	35	35	–	–	–	–	35	–
$\overline{EA}$	46	40	32	52	43	46	–	–	–	28	47	52

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output..
3. Standard Functions: See Table 2, Increment SF4: $F=S+1+C_n$ and Decrement SFD: $F=S-2+C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	(54)	(44)	–	–	(49)	(54)	(22)	–	–	(33)
	IS	(54)	(44)	(42)	–	–	–	(22)	–	–	(33)
	LSS	(54)	(44)	(42)	–	–	–	(22)	–	–	(33)
DA, DB	MSS	(46)	(40)	–	–	(43)	(46)	–	–	–	(28)
	IS	(46)	(40)	(32)	–	–	–	–	–	–	(28)
	LSS	(46)	(40)	(32)	–	–	–	–	–	–	(28)
C_n	MSS	28	(14)	–	–	(22)	(22)	–	–	–	(18)
	IS	(26)	(14)	–	–	–	–	–	–	–	(18)
	LSS	(26)	(14)	–	–	–	–	–	–	–	(18)
I_{8-0}	MSS	75	60	–	–	70	70	–	–	(21)	58
	IS	75	60	57	–	–	–	–	–	(21)	58
	LSS	75	60	57	24	–	–	–	(27)	(21)	58
CP	MSS	(46)	(34)	–	–	(43)	(46)	(18)	–	(18)	(30)
	IS	(46)	(34)	(34)	–	–	–	(18)	–	(18)	(30)
	LSS	75	60	57	24	–	–	(18)	–	(18)	58
Z	MSS	51	36	–	–	46	46	–	–	–	34
	IS	51	36	33	–	–	–	–	–	–	34
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(18)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. Unsigned Multiply
   SF0: $F=S+C_n$ if $Z=0$
   $F=S+R+C_n$ if $Z=1$
   $Y=\text{Log. } F/2$
   $Q=\text{Log. } Q/2$
   $Y_3=C_{n+4}$ (MSS)
   $Z=Q_0$ (LSS)

   Two's Complement Multiply
   SF2: $F=S+C_n$ if $Z=0$
   $F=R+S+C_n$ if $Z=1$
   $Y=\text{Log. } F/2$
   $Q=\text{Log. } Q/2$
   $Y_3=F_3 \oplus OVR$ (MSS)
   $Z=Q_0$ (LSS)

   Two's Complement Multiply Last Cycle
   SF6: $F=S+C_n$ if $Z=0$
   $F=S-R-1+C_n$ if $Z=1$
   $Y=\text{Log. } F/2$
   $Q=\text{Log. } Q/2$
   $Y_3=OVR \oplus F_3$ (MSS)
   $Z=Q_0$ (LSS)

IDT39C203A GUARANTEED COMMERCIAL RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(54)	49/(44)	–	(59)/–	(49)	(54)	(22)	–	–	(50)
	IS	(54)	(44)	(42)	(59)/–	–	–	(22)	–	–	(50)
	LSS	(54)	(44)	(42)	(59)/–	–	–	(22)	–	–	(50)
DA, DB	MSS	(46)	44/40	–	(52)/–	(43)	(46)	–	–	–	(47)
	IS	(46)	(40)	(32)	(52)/–	–	–	–	–	–	(47)
	LSS	(46)	(40)	(32)	(52)/–	–	–	–	–	–	(47)
C_n	MSS	(26)	26/(14)	–	(28)/–	(22)	(22)	–	–	–	26
	IS	(26)	(14)	–	(28)/–	–	–	–	–	–	(24)
	LSS	(26)	(14)	–	(28)/–	–	–	–	–	–	(24)
I_{8-0}	MSS	(51)/67	60/54	–	(58)/23	(49)/62	(50)/62	–	–	(21)	(50)/66
	IS	(51)/67	(51)/54	(40)/(56)	(58)/–	–	–	–	–	(21)	(50)/66
	LSS	(51)/67	(51)/54	(40)/(56)	(58)/–	–	–	–	(27)	(21)	(50)/66
CP	MSS	(46)/68	37/55	–	(49)/24	(43)/53	(46)/53	(18)	–	(18)	(43)/63
	IS	(46)	(34)	(34)	(49)/–	–	–	(18)	–	(18)	(43)
	LSS	(46)	(34)	(34)	(49)/–	–	–	(18)	–	(18)	(43)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/44	–/31	–/33	–	–	–	–	–	–	–/43
	LSS	–/44	–/31	–/33	–	–	–	–	–	–	–/43
SIO_0, SIO_3	Any	(18)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.
5. Double Length Normalize and First Divide Op
   SFA: $F = S + C_n$
   $Y = \text{Log. } 2F$
   $Q = \text{Log. } 2Q$
   $SIO_3 = F_3 \oplus R_3$ (MSS)
   $C_{n+4} = F_3 \oplus F_2$ (MSS)
   $OVR = F_2 \oplus F_1$ (MSS)
   $Z = \overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}\,\overline{Q_3}\,\overline{F_0}\,\overline{F_1}\,\overline{F_2}\,\overline{F_3}$

   Two's Complement Divide
   SFC: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = \text{Log. } 2F$
   $Q = \text{Log. } 2Q$
   $SIO_3 = \overline{F_3 \oplus R_3}$ (MSS)
   $Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = F$
   $Q = \text{Log. } 2Q$
   $Z = F_3 \oplus R_3$ (MSS) from previous cycle

IDT39C203A GUARANTEED COMMERCIAL RANGE PERFORMANCE BCD INSTRUCTIONS (SF1, SF7, SF9, SFB, SFD, SFF)

FROM	TO												
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{\text{WRITE}}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	MSS	58	48	–	(59)	54	54	(22)	–	–	44	(50)	(62)
	IS	58	48	44	(59)	–	–	(22)	–	–	44	(50)	(62)
	LSS	58	48	44	(59)	–	–	(22)	–	–	44	(50)	(62)
DA, DB	MSS	49	42	–	(52)	47	47	–	–	–	36	(47)	(52)
	IS	49	42	38	(52)	–	–	–	–	–	36	(47)	(52)
	LSS	49	42	38	(52)	–	–	–	–	–	36	(47)	(52)
C_n	MSS	29	18	–	30	26	26	–	–	–	24	29	35
	IS	29	18	–	30	–	–	–	–	–	24	29	35
	LSS	29	18	–	30	–	–	–	–	–	24	29	35
I_{8-0}	MSS	58	(51)	–	(58)/36	50	(50)	–	–	(21)	(40)	(50)	(59)
	IS	58	(51)	50	(58)/36	–	–	–	–	(21)	(40)	(50)	(59)
	LSS	58	(51)	50	(58)/36	–	–	–	(27)	(21)	(40)	(50)	(59)
CP	MSS	50	42	–	54/24	50	50	(18)	–	(18)	31	48	52
	IS	50	42	40	54/24	–	–	(18)	–	(18)	31	48	52
	LSS	50	42	40	54/24	–	–	(18)	–	(18)	31	48	52
SIO_{0-3}	Any	(18)	–	–	–	–	–	–	–	–	–	–	–

NOTES:

1. Binary-to-BCD and multiprecision Binary-to-BCD instructions only.
2. BCD-to-binary conversion (SF1), Binary-to-BCD conversion (SF9), BCD subtract (SFD, SFF), BCD divide by two (SF7), BCD add (SFB)
3. A "–" means the delay path does not exist.
4. A number in parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
5. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's divide correction.

IDT39C203A GUARANTEED COMMERCIAL RANGE PERFORMANCE SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	78	67	–	36	71	71	(22)	–	–	84
	IS	(54)	(44)	(42)	–	–	–	(22)	–	–	(50)
	LSS	(54)	(44)	(42)	–	–	–	(22)	–	–	(50)
DA, DB	MSS	75	63	–	32	67	67	–	–	–	80
	IS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
	LSS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
C_n	MSS	(26)	(14)	–	–	26	(21)	–	–	–	(24)
	IS	(26)	(14)	–	–	–	–	–	–	–	(24)
	LSS	(26)	(14)	–	–	–	–	–	–	–	(24)
I_{8-0}	MSS	68	54	–	22	66	58	–	–	(21)	70*
	IS	68	54	50	–	–	–	–	–	(21)	70*
	LSS	68	54	50	–	–	–	–	(27)	(21)	70*
CP	MSS	75	63	–	32	67	67	(18)	–	(18)	80
	IS	(46)	(34)	(34)	–	–	–	(18)	–	(18)	(43)
	LSS	(46)	(34)	(34)	–	–	–	(18)	–	(18)	(43)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	46	31	28	–	–	–	–	–	–	48
	LSS	46	31	28	–	–	–	–	–	–	48
SIO_0, SIO_3	Any	(18)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. SF5: $F = S + C_n$ if $Z = 0$, $Y_3 = S_3 \oplus F_3$ (MSS), $Q = Q$
   $F = \overline{S} + C_n$ if $Z = 1$, $Z = S_3$ (MSS), $N = F_3$ if $Z = 0$
   $N = F_3 \oplus S_3$ if $Z = 1$

IDT39C203A GUARANTEED COMMERCIAL RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(54)	–	–	–	–	–	(22)	–	–	(50)
	IS	(54)	(44)	(42)	–	–	–	(22)	–	–	(50)
	LSS	(54)	(44)	(42)	–	–	–	(22)	–	–	(50)
DA, DB	MSS	(46)	–	–	–	–	–	–	–	–	(47)
	IS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
	LSS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
C_n	MSS	(26)	–	–	–	–	–	–	–	–	(24)
	IS	(26)	(14)	–	–	–	–	–	–	–	(24)
	LSS	(26)	(14)	–	–	–	–	–	–	–	(24)
I_{8-0}	MSS	(51)	30	–	23	19	19	–	–	(21)	(50)*
	IS	(51)	(51)	(40)	23	–	–	–	–	(21)	(50)*
	LSS	(51)	(51)	(40)	23	–	–	–	(27)	(21)	(50)*
CP	MSS	(46)	23	–	24	21	21	(18)	–	(18)	(43)
	IS	(46)	(34)	(34)	24	–	–	(18)	–	(18)	(43)
	LSS	(46)	(34)	(34)	24	–	–	(18)	–	(18)	(43)
SIO_0, SIO_3	Any	(18)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. SF8: $F = S + C_n$ $\quad C_{n+4} = Q_3 \oplus Q_2$ (MSS) $\quad OVR = Q_2 \oplus Q_1$ (MSS)
   $N = Q_3$ (MSS) $\quad Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
   $Y = F$
   $Q = \text{Log. } 2Q$

IDT39C203A GUARANTEED MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C203A over the military operating range of -55 °C to +125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Table 15. Clock and Write Pulse Characteristics All Functions

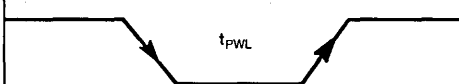
Minimum Clock Low Time	24ns
Minimum Clock High Time	24ns
Minimum Time CP and $\overline{WE}$ both Low to Write	24ns

Table 16. Enable/Disable Times All Functions[1]

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	20	17
$\overline{OE}_B$	DB	20	17
$\overline{EA}$	DA	20	17
I_8	SIO	20	17
I_8	QIO	30	30
$I_{8,7,6,5}$	QIO	30	30
$I_{4,3,2,1,0}$	QIO	30	28
$\overline{LSS}$	$\overline{WRITE}$	24	20

NOTE:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Table 17. Set-up and Hold Times All Functions



FROM	WITH RESPECT TO	HIGH-TO-LOW SET-UP	HIGH-TO-LOW HOLD	LOW-TO-HIGH SET-UP	LOW-TO-HIGH HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	11	3	Store Y in RAM/Q[1]
$\overline{WE}$ HIGH	CP	12	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	12	0	Write into RAM
A, B Source	CP	16	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	5	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	14	3	Shift Q
$I_{8,7,6,5}$	CP	10	–	16	0	Write into Q[2]
$\overline{IEN}$ HIGH	CP	19	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	17	0	Write into Q
$I_{4,3,2,1,0}$	CP	14	–	26	0	Write into Q[2]

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. IEN controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L → H and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

IDT39C203A GUARANTEED MILITARY RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT/DECREMENT BY ONE OR TWO INSTRUCTIONS (SF3, SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	56	46	42	62	54	54	22	–	–	38	57	67
DA, DB	48	42	32	53	44	46	–	–	–	28	49	59
C_n	28	15	–	33	25	23	–	–	–	18	26	32
I_{8-0}	58	55	45	64	57	55	–	29	21	46	60	71
CP	48	34	34	54	44	46	18	–	18	33	49	53
SIO_0, SIO_3	21	–	–	23	–	–	–	–	–	–	23	15
$\overline{MSS}$	35	–	35	35	35	35	–	–	–	–	35	–
$\overline{EA}$	48	42	32	53	44	46	–	–	–	28	49	59

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output..
3. Standard Functions: See Table 2, Increment SF4: $F = S + 1 + C_n$ and Decrement SF3: $F = S - 2 + C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	(56)	(46)	–	–	(54)	(54)	(22)	–	–	(38)
	IS	(56)	(46)	(42)	–	–	–	(22)	–	–	(38)
	LSS	(56)	(46)	(42)	–	–	–	(22)	–	–	(38)
DA, DB	MSS	(48)	(42)	–	–	(44)	(46)	–	–	–	(28)
	IS	(48)	(42)	(32)	–	–	–	–	–	–	(28)
	LSS	(48)	(42)	(32)	–	–	–	–	–	–	(28)
C_n	MSS	32	(15)	–	–	(25)	(23)	–	–	–	(18)
	IS	(28)	(15)	–	–	–	–	–	–	–	(18)
	LSS	(28)	(15)	–	–	–	–	–	–	–	(18)
I_{8-0}	MSS	86	67	–	–	78	78	–	–	(21)	65*
	IS	86	67	64	–	–	–	–	–	(21)	65*
	LSS	86	67	64	26	–	–	–	(29)	(21)	65*
CP	MSS	(48)	(34)	–	–	(44)	(46)	(18)	–	(18)	(33)
	IS	(48)	(34)	(34)	–	–	–	(18)	–	(18)	(33)
	LSS	87	68	63	27	–	–	(18)	–	(18)	66
Z	MSS	60	41	–	–	52	52	–	–	–	38
	IS	60	41	38	–	–	–	–	–	–	38
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(21)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number in parenthesis means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Tests.
4. Unsigned Multiply
   SF0: $F = S + C_n$ if $Z = 0$
   $F = S + R + C_n$ if $Z = 1$
   $Y_3 = C_{n+4}$ (MSS)
   $Z = Q_0$ (LSS)
   $Y = $ Log. F/2
   $Q = $ Log. Q/2

   Two's Complement Multiply
   SF2: $F = S + C_n$ if $Z = 0$
   $F = R + S + C_n$ if $Z = 1$
   $Y_3 = F_3 \oplus OVR$ (MSS)
   $Z = Q_0$ (LSS)
   $Y = $ Log. F/2
   $Q = $ Log. Q/2

   Two's Complement Multiply Last Cycle
   SF6: $F = S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y_3 = OVR \oplus F_3$ (MSS)
   $Z = Q_0$ (LSS)
   $Y = $ Log. F/2
   $Q = $ Log. Q/2

IDT39C203A GUARANTEED MILITARY RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(56)	58/(46)	–	(62)/–	(54)	(54)	(22)	–	–	(57)
	IS	(56)	(46)	(42)	(62)/–	–	–	(22)	–	–	(57)
	LSS	(56)	(46)	(42)	(62)/–	–	–	(22)	–	–	(57)
DA, DB	MSS	(48)	53/(42)	–	(53)/–	(44)	(46)	–	–	–	(49)
	IS	(48)	(42)	(32)	(53)/–	–	–	–	–	–	(49)
	LSS	(48)	(42)	(32)	(53)/–	–	–	–	–	–	(49)
C_n	MSS	(28)	30/(15)	–	(33)/–	(25)	(23)	–	–	–	29
	IS	(28)	(15)	–	(33)/–	–	–	–	–	–	(26)
	LSS	(28)	(15)	–	(33)/–	–	–	–	–	–	(26)
I_{8-0}	MSS	(58)/77	71/63	–	(64)/26	(57)/73	(55)/73	–	–	(21)	61/78*
	IS	(58)/77	(55)/63	(45)/63	(64)	–	–	–	–	(21)	(60)/78*
	LSS	(58)/77	(55)/63	(45)/63	(64)	–	–	–	(29)	(21)	(60)/78*
CP	MSS	(48)/78	41/64	–	(54)/27	(44)/59	(46)/59	(18)	–	(18)	(49)/74
	IS	(48)	(34)	(34)	(54)	–	–	(18)	–	(18)	(49)
	LSS	(48)	(34)	(34)	(54)	–	–	(18)	–	(18)	(49)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/50	–/37	–/37	–	–	–	–	–	–	–/52
	LSS	–/50	–/37	–/37	–	–	–	–	–	–	–/52
SIO_0, SIO_3	Any	(21)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.
5. Double Length Normalize and First Divide Op
   SFA: $F=S+C_n$
   $SIO_3 = F_3 \oplus R_3$ (MSS)
   $C_{n+4} = F_3 \oplus F_2$ (MSS)
   $OVR = F_2 \oplus F_1$ (MSS)
   $Z = \overline{Q}_0 \overline{Q}_1 \overline{Q}_2 \overline{Q}_3 \overline{F}_0 \overline{F}_1 \overline{F}_2 \overline{F}_3$
   Y = Log. 2F
   Q = Log. 2Q

   Two's Complement Divide
   SFC: $F=R+S+C_n$ if $Z=0$
   $F=S-R-1+C_n$ if $Z=1$
   Y = Log. 2F
   Q = Log. 2Q
   $SIO_3 = \overline{F_3 \oplus R_3}$ (MSS)
   $Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F=R+S+C_n$ if $Z=0$
   $F=S-R-1+C_n$ if $Z=1$
   Y = F
   Q = Log. 2Q
   $Z = F_3 \oplus R_3$ (MSS) from previous cycle

IDT39C203A GUARANTEED MILITARY RANGE PERFORMANCE BCD INSTRUCTIONS (SF1, SF7, SF9, SFB, SFD, SFF)

FROM	TO												
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	MSS	60	52	–	(62)	56	56	(22)	–	–	48	(57)	(67)
	IS	60	52	46	(62)	–	–	(22)	–	–	48	(57)	(67)
	LSS	60	52	46	(62)	–	–	(22)	–	–	48	(57)	(67)
DA, DB	MSS	50	43	–	(53)	51	51	–	–	–	40	(49)	(59)
	IS	50	43	40	(53)	–	–	–	–	–	40	(49)	(59)
	LSS	50	43	40	(53)	–	–	–	–	–	40	(49)	(59)
C_n	MSS	31	21	–	35	30	30	–	–	–	27	31	38
	IS	31	21	–	35	–	–	–	–	–	27	31	38
	LSS	31	21	–	35	–	–	–	–	–	27	31	38
I_{8-0}	MSS	61	(55)	–	(64)/40(1)	58	58	–	–	(21)	(46)	(60)	(71)
	IS	61	(55)	56	(64)/40(1)	–	–	–	–	(21)	(46)	(60)	(71)
	LSS	61	(55)	56	(64)/40(1)	–	–	–	(29)	(21)	(46)	(60)	(71)
CP	MSS	54	43	–	56/27(1)	53	53	(18)	–	(18)	34	50	59
	IS	54	43	42	56/27(1)	–	–	(18)	–	(18)	34	50	59
	LSS	54	43	42	56/27(1)	–	–	(18)	–	(18)	34	50	59
SIO_{0-3}	Any	(21)	–	–	–	–	–	–	–	–	–	–	–

NOTES:
1. Binary-to-BCD and multiprecision Binary-to-BCD instructions only.
2. BCD-to-binary conversion (SF1), Binary-to-BCD conversion (SF9), BCD subtract (SFD, SFF), BCD divide by two (SF7), BCD add (SFB)
3. A "–" means the delay path does not exist.
4. A number in parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
5. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide cor rection.

IDT39C203A GUARANTEED MILITARY RANGE PERFORMANCE SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	91	78	–	42	85	85	(22)	–	–	102
	IS	(56)	(46)	(42)	–	–	–	(22)	–	–	(57)
	LSS	(56)	(46)	(42)	–	–	–	(22)	–	–	(57)
DA, DB	MSS	86	74	–	37	81	81	–	–	–	90
	IS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
	LSS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
C_n	MSS	29	(15)	–	–	28	(23)	–	–	–	(26)
	IS	(28)	(15)	–	–	–	–	–	–	–	(26)
	LSS	(28)	(15)	–	–	–	–	–	–	–	(26)
I_{8-0}	MSS	78	63	–	26	78	70	–	–	(21)	87*
	IS	78	63	58	–	–	–	–	–	(21)	87*
	LSS	78	63	58	–	–	–	–	(29)	(21)	87*
CP	MSS	85	74	–	37	81	81	(18)	–	(18)	98
	IS	(48)	(34)	(34)	–	–	–	(18)	–	(18)	(49)
	LSS	(48)	(34)	(34)	–	–	–	(18)	–	(18)	(49)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	52	37	32	–	–	–	–	–	–	61
	LSS	52	37	32	–	–	–	–	–	–	61
SIO_0, SIO_3	Any	(21)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. SF5: $F=S+C_n$ if $Z=0$, $F=\overline{S}+C_n$ if $Z=1$, $Y_3=S_3 \oplus F_3$ (MSS), $Z=S_3$ (MSS), $Y=F$, $Q=Q$, $N=F_3$ if $Z=0$, $N=F_3 \oplus S_3$ if $Z=1$

IDT39C203A GUARANTEED MILITARY RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(56)	–	–	–	–	–	(22)	–	–	(57)
	IS	(56)	(46)	(42)	–	–	–	(22)	–	–	(57)
	LSS	(56)	(46)	(42)	–	–	–	(22)	–	–	(57)
DA, DB	MSS	(48)	–	–	–	–	–	–	–	–	(49)
	IS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
	LSS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
C_n	MSS	(28)	–	–	–	–	–	–	–	–	(26)
	IS	(28)	(15)	–	–	–	–	–	–	–	(26)
	LSS	(28)	(15)	–	–	–	–	–	–	–	(26)
I_{8-0}	MSS	(58)	38	–	26	22	22	–	–	(21)	60*
	IS	(58)	(55)	(45)	26	–	–	–	–	(21)	60*
	LSS	(58)	(55)	(45)	26	–	–	–	(29)	(21)	60*
CP	MSS	(48)	25	–	27	21	25	(18)	–	(18)	(49)
	IS	(48)	(34)	(34)	27	–	–	(18)	–	(18)	(49)
	LSS	(48)	(34)	(34)	27	–	–	(18)	–	(18)	(49)
SIO_0, SIO_3	Any	(21)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. SF8: $F = S + C_n$ $\quad C_{n+4} = Q_3 \oplus Q_2$ (MSS) $\quad OVR = Q_2 \oplus Q_1$ (MSS)
   $N = Q_3$ (MSS) $\quad Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
   $Y = F$
   $Q = $ Log. 2Q

8

IDT39C203 GUARANTEED COMMERCIAL RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C203 over the commercial operating range of 0 to 70°C with V_{CC} from 4.75 to 5.25V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Table 6. Clock and Write Pulse Characteristics All Functions

Minimum Clock Low Time	30ns
Minimum Clock High Time	30ns
Minimum Time CP and $\overline{WE}$ both Low to Write	15ns

Table 7. Enable/Disable Times All Functions [1]

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	25	21
$\overline{OE}_B$	DB	25	21
$\overline{EA}$	DA	25	21
I_8	SIO	25	21
I_8	QIO	38	38
$I_{8,7,6,5}$	QIO	38	38
$I_{4,3,2,1,0}$	QIO	38	35
$\overline{LSS}$	$\overline{WRITE}$	25	21

NOTE:
1. C_L = 5pF for output disable tests. Measurement is made to a 0.5V change on the output.

Table 8. Set-up and Hold Times All Functions

		HIGH-TO-LOW		LOW-TO-HIGH		
						
FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q [1]
$\overline{WE}$ HIGH	CP	15	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	17	3	Shift Q
$I_{8,7,6,5}$	CP	12	–	20	0	Write into Q [2]
$\overline{IEN}$ HIGH	CP	24	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	21	0	Write into Q
$I_{4,3,2,1,0}$	CP	18	–	32	0	Write into Q [2]

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$= L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. IEN controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L→ H and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

IDT39C203 GUARANTEED COMMERCIAL RANGE PERFORMANCE STANDARD FUNCTIONS AND INCREMENT/DECREMENT BY ONE OR TWO INSTRUCTIONS (SF3, SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	67	55	52	74	61	67	28	–	–	41	62	78
DA, DB	58	50	40	65	54	58	–	–	–	35	59	65
C_n	33	18	–	35	28	27	–	–	–	23	30	38
I_{8-0}	64	64	50	72	61	62	–	34	26*	50*	62*	74*
CP	58	42	43	61	54	58	22	–	22	37	54	60
SIO_0, SIO_3	23	–	–	29	–	–	–	–	–	–	29	19
$\overline{MSS}$	44	–	44	44	44	44	–	–	–	–	44	–
$\overline{EA}$	58	50	40	65	54	58	–	–	–	35	59	65

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. Standard Functions: See Table 2, Increment SF4: $F = S + 1 + C_n$ and Decrement SF3: $F = S - 2 + C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	(67)	(55)	–	–	(61)	(67)	(28)	–	–	(41)
	IS	(67)	(55)	(52)	–	–	–	(28)	–	–	(41)
	LSS	(67)	(55)	(52)	–	–	–	(28)	–	–	(41)
DA, DB	MSS	(58)	(50)	–	–	(54)	(58)	–	–	–	(35)
	IS	(58)	(50)	(40)	–	–	–	–	–	–	(35)
	LSS	(58)	(50)	(40)	–	–	–	–	–	–	(35)
C_n	MSS	35	(18)	–	–	(28)	(27)	–	–	–	(23)
	IS	(33)	(18)	–	–	–	–	–	–	–	(23)
	LSS	(33)	(18)	–	–	–	–	–	–	–	(23)
I_{8-0}	MSS	94	75	–	–	88	88	–	–	(26)*	73*
	IS	94	75	71	–	–	–	–	–	(26)*	73*
	LSS	94	75	71	30	–	–	–	(34)	(26)*	73*
CP	MSS	(58)	(42)	–	–	(54)	(58)	(22)	–	(22)	(37)
	IS	(58)	(42)	(43)	–	–	–	(22)	–	(22)	(37)
	LSS	94	75	71	30	–	–	(22)	–	(22)	73
Z	MSS	64	45	–	–	58	58	–	–	–	43
	IS	64	45	41	–	–	–	–	–	–	43
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. A number in parentheses means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instructions Test.
4. Unsigned Multiply
   SF0: $F = S + C_n$ if $Z = 0$
   $F = S + R + C_n$ if $Z = 1$
   $Y =$ Log. F/2
   $Q =$ Log. Q/2
   $Y_3 = C_{n+4}$ (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply
   SF2: $F = S + C_n$ if $Z = 0$
   $F = R + S + C_n$ if $Z = 1$
   $Y =$ Log. F/2
   $Q =$ Log. Q/2
   $Y_3 = F_3 \oplus OVR$ (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply Last Cycle
   SF6: $F = S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y =$ Log. F/2
   $Q =$ Log. Q/2
   $Y_3 =$ OVR $\oplus$ (MSS)
   $Z = Q_0$ (LSS)

IDT39C203 GUARANTEED COMMERCIAL RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$/MSS	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(67)	61/(55)	–	(74)/–	(61)	(67)	(28)	–	–	62
	IS	(67)	(55)	(52)	(74)/–	–	–	(28)	–	–	62
	LSS	(67)	(55)	(52)	(74)/–	–	–	(28)	–	–	62
DA, DB	MSS	(58)	55/(50)	–	(65)/–	(54)	(58)	–	–	–	59
	IS	(58)	(50)	(40)	(65)/–	–	–	–	–	–	59
	LSS	(58)	(50)	(40)	(65)/–	–	–	–	–	–	59
C_n	MSS	(33)	33/(18)	–	(35)/–	(28)	(27)	–	–	–	32
	IS	(33)	(18)	–	(35)/–	–	–	–	–	–	30
	LSS	(33)	(18)	–	(35)/–	–	–	–	–	–	30
I_{8-0}	MSS	(64)/84	75/68	–	(72)/29	(61)/77	(62)/77	–	–	(26)*	63/83*
	IS	(64)/84	(64)/68	(50)/70	(72)/–	–	–	–	–	(26)*	(62)/83*
	LSS	(64)/84	(64)/68	(50)70	(72)/–	–	–	–	(34)	(26)*	(62)/83*
CP	MSS	(58)/85	46/69	–	(61)/30	(54)/66	(58)/66	(22)	–	(22)	(54)/79*
	IS	(58)	(42)	(43)	(61)/–	–	–	(22)	–	(22)	(54)
	LSS	(58)	(42)	(43)	(61)/–	–	–	(22)	–	(22)	(54)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/55	–/39	–/41	–	–	–	–	–	–	–/54
	LSS	–/55	–/39	–/41	–	–	–	–	–	–	–/54
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.
5. Double Length Normalize and First Divide Op
   SFA: $F=S+C_n$
   $Y=$ Log. 2F
   $Q=$ Log. 2Q
   $SIO_3=F_3 \oplus R$ (MSS)
   $C_{n+4}=F_3 \oplus F_2$ (MSS)
   $OVR=F_2 \oplus F_1$ (MSS)
   $Z=\overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}\,\overline{Q_3}\,\overline{F_0}\,\overline{F_1}\,\overline{F_2}\,\overline{F_3}$

   Two's Complement Divide
   SFC: $F=R+S+C_n$ if $Z=0$
   $F=S-R-1+C_n$ if $Z=1$
   $Y=$ Log. 2F
   $Q=$ Log. 2Q
   $SIO_3=\overline{F_3 \oplus R_3}$ (MSS)
   $Z=\overline{F_3 \oplus R_3}$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F=R+S+C_n$ if $Z=0$
   $F=S-R-1+C_n$ if $Z=1$
   $Y=F$
   $Q=$ Log. 2Q
   $Z=F_3 \oplus R_3$ (MSS) from previous cycle

IDT39C203 GUARANTEED COMMERCIAL RANGE PERFORMANCE BCD INSTRUCTIONS (SF1, SF7, SF9, SFB, SFD, SFF)

FROM	TO												
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	MSS	72	60	–	(74)	68	68	(28)	–	–	55	(62)	(78)
	IS	72	60	55	(74)	–	–	(28)	–	–	55	(62)	(78)
	LSS	72	60	55	(74)	–	–	(28)	–	–	55	(62)	(78)
DA, DB	MSS	61	52	–	(65)	59	59	–	–	–	45	(59)	(65)
	IS	61	52	48	(65)	–	–	–	–	–	45	(59)	(65)
	LSS	61	52	48	(65)	–	–	–	–	–	45	(59)	(65)
C_n	MSS	36	23	–	37	33	33	–	–	–	30	36	44
	IS	36	23	–	37	–	–	–	–	–	30	36	44
	LSS	36	23	–	37	–	–	–	–	–	30	36	44
I_{8-0}	MSS	72	(64)	–	(72)/45[1]	62	(62)	–	–	(26)	(50)	(62)	(74)
	IS	72	(64)	63	(72)/45[1]	–	–	–	–	(26)	(50)	(62)	(74)
	LSS	72	(64)	63	(72)/45[1]	–	–	–	(34)	(26)	(50)	(62)	(74)
CP	MSS	62	53	–	68/30[1]	62	62	(22)	–	(22)	39	60	65
	IS	62	53	50	68/30[1]	–	–	(22)	–	(22)	39	60	65
	LSS	62	53	50	68/30[1]	–	–	(22)	–	(22)	39	60	65
SIO_{0-3}	Any	(23)	–	–	–	–	–	–	–	–	–	–	–

NOTES:
1. Binary-to-BCD and multiprecision Binary-to-BCD instructions only.
2. BCD-to-binary conversion (SF1), Binary-to-BCD conversion (SF9), BCD subtract (SFD, SFF), BCD divide by two (SF7), BCD add (SFB)
3. A number in parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C203 GUARANTEED COMMERCIAL RANGE PERFORMANCE SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	97	84	–	45	89	89	(28)	–	–	105
	IS	(67)	(55)	(52)	–	–	–	(28)	–		(62)
	LSS	(67)	(55)	(52)	–	–	–	(28)	–		(62)
DA, DB	MSS	94	79	–	40	84	84	–	–		100
	IS	(58)	(50)	(40)	–	–	–	–	–		(59)
	LSS	(58)	(50)	(40)	–	–	–	–	–		(59)
C_n	MSS	(33)	(18)	–	–	32	(27)	–	–		(30)
	IS	(33)	(18)	–	–	–	–	–	–		(30)
	LSS	(33)	(18)	–	–	–	–	–	–		(30)
I_{8-0}	MSS	85	67	–	28	82	73	–	–	(26)	88*
	IS	85	67	63	–	–	–	–	–	(26)	88*
	LSS	85	67	63	–	–	–	–	(34)	(26)	88*
CP	MSS	94	79	–	40	84	84	(22)	–	(22)	100
	IS	(58)	(42)	(43)	–	–	–	(22)	–	(22)	(54)
	LSS	(58)	(42)	(43)	–	–	–	(22)	–	(22)	(54)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	57	39	35	–	–	–	–	–	–	60
	LSS	57	39	35	–	–	–	–	–	–	60
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. A number in parentheses means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. SF5: $F = S + C_n$ if $Z = 0$, $Y_3 = S_3 \oplus F_3$ (MSS), $Q = Q$
   $F = \overline{S} + C_n$ if $Z = 1$, $Z = S_3$ (MSS), $N = F_3$ if $Z = 0$
   $N = F_3 \oplus S_3$ if $Z = 1$

IDT39C203 COMMERCIAL RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(67)	–	–	–	–	–	(28)	–	–	(62)
	IS	(67)	(55)	(52)	–	–	–	(28)	–	–	(62)
	LSS	(67)	(55)	(52)	–	–	–	(28)	–	–	(62)
DA, DB	MSS	(58)	–	–	–	–	–	–	–	–	(59)
	IS	(58)	(50)	(40)	–	–	–	–	–	–	(59)
	LSS	(58)	(50)	(40)	–	–	–	–	–	–	(59)
C_n	MSS	(33)	–	–	–	–	–	–	–	–	(30)
	IS	(33)	(18)	–	–	–	–	–	–	–	(30)
	LSS	(33)	(18)	–	–	–	–	–	–	–	(30)
I_{8-0}	MSS	(64)	37	–	29	24	24	–	–	(26)	(62)*
	IS	(64)	(64)	(50)	29	–	–	–	–	(26)	(62)*
	LSS	(64)	(64)	(50)	29	–	–	–	(34)	(26)	(62)*
CP	MSS	(58)	29	–	30	26	29	(22)	–	(22)	(54)
	IS	(58)	(42)	(43)	30	–	–	(22)	–	(22)	(54)
	LSS	(58)	(42)	(43)	30	–	–	(22)	–	(22)	(54)
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. A number is parantheses means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. SF8: $F = S + C_n$ $\quad C_{n+4} = Q_3 \oplus Q_2$ (MSS) $\quad OVR = Q_2 \oplus Q_1$ (MSS)
   $N = Q_3$ (MSS) $\quad Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
   $Y = F$
   $Q = \text{LOG } 2Q$

8

IDT39C203 GUARANTEED MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C203 over the military operating range of -55°C to +125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Table 9. Clock and Write Pulse Characteristics All Functions

Minimum Clock Low Time	30ns
Minimum Clock High Time	30ns
Minimum Time CP and $\overline{WE}$ both Low to Write	30ns

Table 10. Enable/Disable Times All Functions[1]

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	25	21
$\overline{OE}_B$	DB	25	21
$\overline{EA}$	DA	25	21
I_8	SIO	25	21
I_8	QIO	38	38
$I_{8,7,6,5}$	QIO	38	38
$I_{4,3,2,1,0}$	QIO	38	35
$\overline{LSS}$	$\overline{WRITE}$	30	25

NOTE:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Table 11. Set-up and Hold Times All Functions

		HIGH-TO-LOW		LOW-TO-HIGH		
						
FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q[1]
$\overline{WE}$ HIGH	CP	15	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	17	3	Shift Q
$I_{8,7,6,5}$	CP	12	–	20	0	Write into Q[2]
$\overline{IEN}$ HIGH	CP	24	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	21	0	Write into Q
$I_{4,3,2,1,0}$	CP	18	–	32	0	Write into Q[2]

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$= L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. IEN controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L → H and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

IDT39C203 GUARANTEED MILITARY RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT/DECREMENT BY ONE OR TWO INSTRUCTIONS (SF3, SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	70	58	52	78	68	67	28	–	–	47	71	84
DA, DB	60	52	40	66	55	58	–	–	–	35	61	74
C_n	35	19	–	41	31	29	–	–	–	23	33	40
I_{8-0}	72	69	56	80	71	69	–	36	26*	58*	75*	89*
CP	60	42	43	67	55	58	22	–	22	41	61	66
SIO_0, SIO_3	26	–	–	29	–	–	–	–	–	–	29	19
$\overline{MSS}$	44	–	44	44	44	44	–	–	–	–	44	–
$\overline{EA}$	60	52	40	66	55	58	–	–	–	35	61	74

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. Standard Functions: See Table 2, Increment SF4: $F = S + 1 + C_n$ and Decrement SF3: $F = S - 2 + C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	(70)	(58)	–	–	(68)	(67)	(28)	–	–	(47)
	IS	(70)	(58)	(52)	–	–	–	(28)	–	–	(47)
	LSS	(70)	(58)	(52)	–	–	–	(28)	–	–	(47)
DA, DB	MSS	(60)	(52)	–	–	(55)	(58)	–	–	–	(35)
	IS	(60)	(52)	(40)	–	–	–	–	–	–	(35)
	LSS	(60)	(52)	(40)	–	–	–	–	–	–	(35)
C_n	MSS	40	(19)	–	–	(31)	(29)	–	–	–	(23)
	IS	(35)	(19)	–	–	–	–	–	–	–	(23)
	LSS	(35)	(19)	–	–	–	–	–	–	–	(23)
I_{8-0}	MSS	108	84	–	–	98	98	–	–	(26)	81*
	IS	108	84	80	–	–	–	–	–	(26)	81*
	LSS	108	84	80	33	–	–	–	(36)	(26)	81*
CP	MSS	62	(42)	–	–	(55)	(58)	(22)	–	(22)	(41)
	IS	(60)	(42)	(43)	–	–	–	(22)	–	(22)	(41)
	LSS	109	85	79	34	–	–	(22)	–	(22)	82
Z	MSS	75	51	–	–	65	65	–	–	–	48
	IS	75	51	47	–	–	–	–	–	–	48
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. A number in parentheses means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. Unsigned Multiply
   SF0: $F = S + C_n$ if $Z = 0$
   $F = S + R + C_n$ if $Z = 1$
   $Y = $ Log. F/2
   $Q = $ Log. Q/2
   $Y_3 = C_{n+4}$ (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply
   SF2: $F = S + C_n$ if $Z = 0$
   $F = R + S + C_n$ if $Z = 1$
   $Y = $ Log. F/2
   $Q = $ Log. Q/2
   $Y_3 = F_3 \oplus OVR$ (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply Last Cycle
   SF6: $F = S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = $ Log. F/2
   $Q = $ Log. Q/2
   $Y_3 = OVR \oplus F_3$ (MSS)
   $Z = Q_0$ (LSS)

IDT39C203 GUARANTEED MILITARY RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(70)	72/(58)	–	(78)/–	(68)	(67)	(28)	–	–	(71)
	IS	(70)	(58)	(52)	(78)/–	–	–	(28)	–	–	(71)
	LSS	(70)	(58)	(52)	(78)/–	–	–	(28)	–	–	(71)
DA, DB	MSS	(60)	66/(52)	–	(66)/–	(55)	(58)	–	–	–	(61)
	IS	(60)	(52)	(40)	(66)/–	–	–	–	–	–	(61)
	LSS	(60)	(52)	(40)	(66)/–	–	–	–	–	–	(61)
C_n	MSS	(35)	37/(19)	–	(41)/–	(31)	(29)	–	–	–	36
	IS	(35)	(19)	–	(41)/–	–	–	–	–	–	(33)
	LSS	(35)	(19)	–	(41)/–	–	–	–	–	–	(33)
I_{8-0}	MSS	(72)/96	89/79	–	(80)/33	(71)/91	(69)/91	–	–	(26)	76/98
	IS	(72)/96	(69)/79	(56)/79	(80)/–	–	–	–	–	(26)	(75)/98*
	LSS	(72)/96	(69)/79	(56)/79	(80)/–	–	–	–	(36)	(26)	(75)/98*
CP	MSS	(60)/97	51/80	–	(67)/34	(55)/74	(58)/74	(22)	–	(22)	(61)/93
	IS	(60)	(42)	(43)	(67)/–	–	–	(22)	–	(22)	(61)
	LSS	(60)	(42)	(43)	(67)/–	–	–	(22)	–	(22)	(61)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/63	–/46	–/46	–	–	–	–	–	–	–/65
	LSS	–/63	–/46	–/46	–	–	–	–	–	–	–/65
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. A number in parentheses means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. Double Length Normalize and First Divide Op
   SFA: $F = S + C_n$
   $Y = $ Log. 2F
   $Q = $ Log. 2Q
   $SIO_3 = F_3 \oplus R_3$ (MSS)
   $C_{n+4} = F_3 \oplus F_2$ (MSS)
   $OVR = F_2 \oplus F_1$ (MSS)
   $Z = \overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}\,\overline{Q_3}\,\overline{F_0}\,\overline{F_1}\,\overline{F_2}\,\overline{F_3}$

   Two's Complement Divide
   SFC: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = $ Log. 2F
   $Q = $ Log. 2Q
   $SIO_3 = \overline{F_3 \oplus R_3}$ (MSS)
   $Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = F$
   $Q = $ Log. 2Q
   $Z = F_3 \oplus R_3$ (MSS) from previous cycle

IDT39C203 GUARANTEED MILITARY RANGE PERFORMANCE BCD INSTRUCTIONS (SF1, SF7, SF9, SFB, SFD, SFF)

FROM	TO												
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	MSS	75	65	–	(78)	70	70	(28)	–	–	60	(71)	(84)
	IS	75	65	57	(78)	–	–	(28)	–	–	60	(71)	(84)
	LSS	75	65	57	(78)	–	–	(28)	–	–	60	(71)	(84)
DA, DB	MSS	62	54	–	70	64	64	–	–	–	50	(61)	(74)
	IS	62	54	50	70	–	–	–	–	–	50	(61)	(74)
	LSS	62	54	50	70	–	–	–	–	–	50	(61)	(74)
C_n	MSS	39	26	–	(41)	37	37	–	–	–	34	39	48
	IS	39	26	–	(41)	–	–	–	–	–	34	39	48
	LSS	39	26	–	(41)	–	–	–	–	–	34	39	48
I_{8-0}	MSS	76	72	–	(80)/50[1]	73	73	–	–	(26)	(58)	(75)	(89)
	IS	76	72	70	(80)/50[1]	–	–	–	–	(26)	(58)	(75)	(89)
	LSS	76	72	70	(80)/50[1]	–	–	–	(36)	(26)	(58)	(75)	(89)
CP	MSS	67	54	–	70/34[1]	66	66	(22)	–	(22)	43	63	74
	IS	67	54	52	70/34[1]	–	–	(22)	–	(22)	43	63	74
	LSS	67	54	52	70/34[1]	–	–	(22)	–	(22)	43	63	74
SIO_{0-3}	Any	(26)	–	–	–	–	–	–	–	–	–	–	–

NOTES:

1. Binary-to-BCD and multiprecision Binary-to-BCD instructions only.
2. BCD-to-binary conversion (SF1), Binary-to-BCD conversion (SF9), BCD subtract (SFD, SFF), BCD divide by two (SF7), BCD add (SFB)
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

8

IDT39C203 GUARANTEED MILITARY RANGE PERFORMANCE SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{\text{WRITE}}$/MSS	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	114	98	–	52	106	106	(28)	–	–	128
	IS	(70)	(58)	(52)	–	–	–	(28)	–		(71)
	LSS	(70)	(58)	(52)	–	–	–	(28)	–		(71)
DA, DB	MSS	108	92	–	46	101	101	–	–	–	112
	IS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
	LSS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
C_n	MSS	36	(19)	–	–	35	(29)	–	–	–	(33)
	IS	(35)	(19)	–	–	–	–	–	–	–	(33)
	LSS	(35)	(19)	–	–	–	–	–	–	–	(33)
I_{8-0}	MSS	98	79	–	33	97	88	–	–	(26)	109*
	IS	98	79	73	–	–	–	–	–	(26)	109*
	LSS	98	79	73	–	–	–	–	(36)	(26)	109*
CP	MSS	108	92	–	46	101	101	(22)	–	(22)	122
	IS	(60)	(42)	(43)	–	–	–	(22)	–	(22)	(61)
	LSS	(60)	(42)	(43)	–	–	–	(22)	–	(22)	(61)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	65	46	40	–	–	–	–	–	–	76
	LSS	65	46	40	–	–	–	–	–	–	76
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. A number is parentheses means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF5: $F=S+C_n$ if $Z=0$, $F=\overline{S}+C_n$ if $Z=1$, $Y_3=S_3 \oplus F_3$(MSS), $Z=S_3$(MSS), $Y=F$, $Q=Q$, $N=F_3$ if $Z=0$, $N=F_3 \oplus S_3$ if $Z=1$

IDT39C203 GUARANTEED MILITARY RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(70)	–	–	–	–	–	(28)	–	–	(71)
	IS	(70)	(58)	(52)	–	–	–	(28)	–	–	(71)
	LSS	(70)	(58)	(52)	–	–	–	(28)	–	–	(71)
DA, DB	MSS	(60)	–	–	–	–	–	–	–	–	(61)
	IS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
	LSS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
C_n	MSS	(35)	–	–	–	–	–	–	–	–	(33)
	IS	(35)	(19)	–	–	–	–	–	–	–	(33)
	LSS	(35)	(19)	–	–	–	–	–	–	–	(33)
I_{8-0}	MSS	(72)	47	–	33	27	27	–	–	(26)	(75)*
	IS	(72)	(69)	(56)	33	–	–	–	–	(26)	(75)*
	LSS	(72)	(69)	(56)	33	–	–	–	(36)	(26)	(75)*
CP	MSS	(60)	31	–	34	26	31	(22)	–	(22)	(61)
	IS	(60)	(42)	(43)	34	–	–	(22)	–	(22)	(61)
	LSS	(60)	(42)	(43)	34	–	–	(22)	–	(22)	(61)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–	–	–	–	–	–	–	–	–	–
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. A number in parentheses means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF8: $F=S+C_n$ $\quad C_{n+4} = Q_3 \oplus Q_2$ (MSS) $\quad OVR=Q_2 \oplus Q_1$(MSS)
   $N=Q_3$ (MSS) $\quad Z=\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
   $Y=F$
   $Q=$Log. 2Q

8

IDT39C203 INPUT/OUTPUT INTERFACE CIRCUITRY

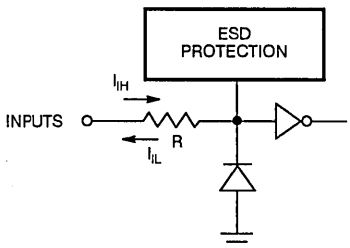


Figure 3. Input Structure (All Inputs)

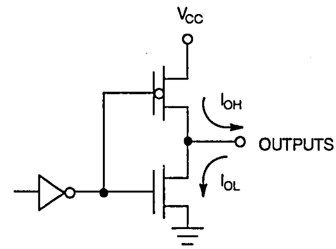


Figure 4. Output Structure (All Outputs)

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 6

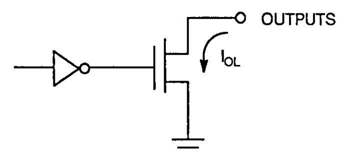


Figure 5. Open Drain Structure

TEST LOAD CIRCUIT

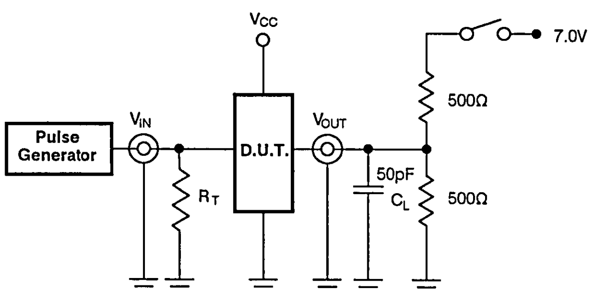


Figure 6. Switching Test Circuits (All Outputs)

SWITCH POSITION

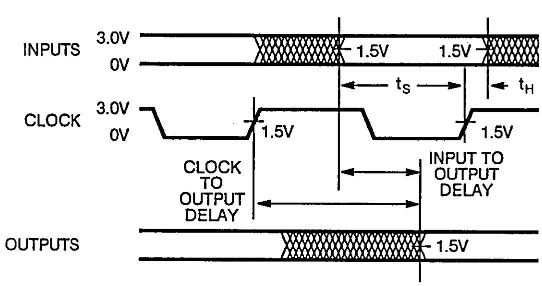
TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

SWITCHING WAVEFORMS



ORDERING INFORMATION

IDT 39C203 (Device Type) X (Speed) X (Package) X (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	P	Plastic DIP
	C	Sidebraze DIP
	L	Leadless Chip Carrier
Speed	Blank	Standard Speed 4-Bit Slice
	A	High-Speed 4-Bit Slice

16-WORD-BY-4-BIT DUAL-PORT RAM

IDT39C705A/B IDT39C707/A

Integrated Device Technology, Inc.

MICROSLICE ™ PRODUCT

FEATURES:

- Fast
  - Available in either industry-standard speed or 20% speed upgraded versions
- Low-power CEMOS ™
  - Military: 50mA (max.)
  - Commercial: 40mA (max.)
- 16-word x 4-bit dual-port CMOS RAM
- Non-inverting data output with respect to data input
- Easily cascadable with separate Write Enables
- Separate 4-bit latches with enables for each output port (IDT39C707/A has separate output control)
- IDT39C705A/B pin-compatible to all versions of the 29705
- IDT39C707/A pin-compatible to all versions of the 29707
- Available in CERDIP, Plastic DIP, LCC and SOIC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT39C705s are high-performance 16-word-by-4-bit dual-port RAMs. Addressing any of the 16 words is performed via the 4-bit A address field with the data appearing on the A output port. The same respective operation holds true for the B address input/output port and can happen simultaneously with the A port operation. New incoming data is written into the 4-bit RAM word selected by the B address. The D inputs are used to load new data into the device.

Featured are two separate output ports which allow any two 4-bit words to be read from these outputs simultaneously. Also featured is a 4-bit latch for each of the two output ports with a common Latch Enable ($\overline{LE}$) input being used to control all eight latches. Two Write Enable ($\overline{WE}$) inputs are designed such that Write Enable 1 ($\overline{WE}_1$) and Latch Enable (LE) inputs can be connected to the RAM to operate in an edge-triggered mode. The Write Enable inputs control the writing of new data into the RAM. Data is written into the B address field when both Write Enables are LOW. If either of the Write Enables are HIGH, no data is written into the RAM.

Three-state outputs allow several devices to be easily cascaded for increased memory size. When $\overline{OE}_A$ input is HIGH, the A output port is in the high impedance mode. The same respective operation occurs for the $\overline{OE}_B$ input.

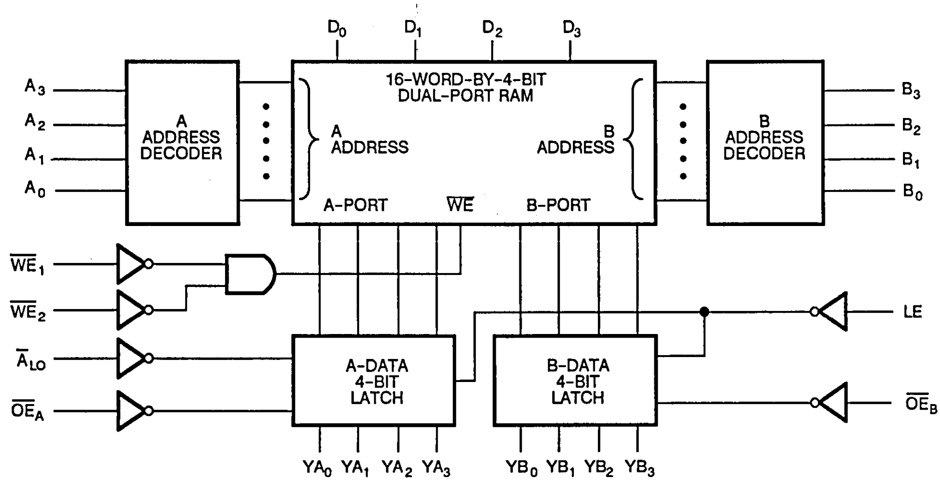
The IDT39C707s function identically to the IDT39C705s, except each output port has a separate Latch Enable (LE) input. Also, an extra Write Enable ($\overline{WE}$) may be connected directly to the IEN of the IDT39C203/A for improved cycle times when compared to the IDT39C705s. The $\overline{WE}$/BLE input can then be connected directly to the system clock.

These performance-enhanced, pin-compatible replacements for all respective versions of the 29705s and 29707s are fabricated using IDT's high-speed, high-reliability CEMOS technology.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

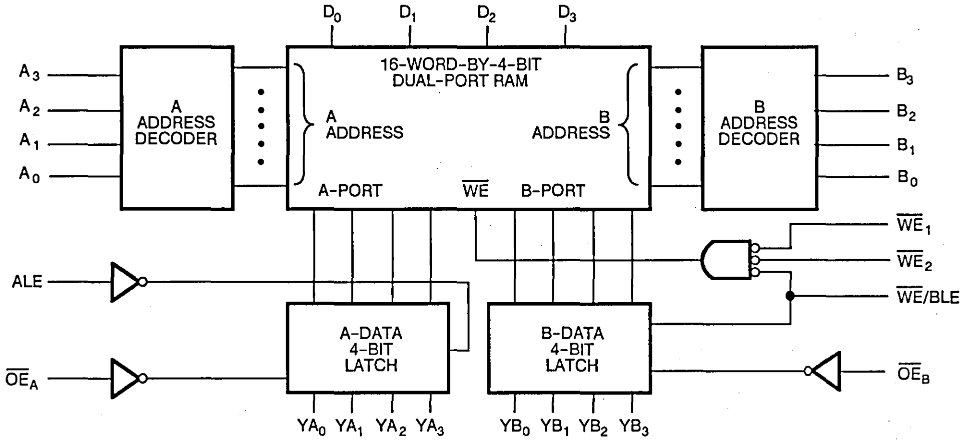
IDT39C705A/B



CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.

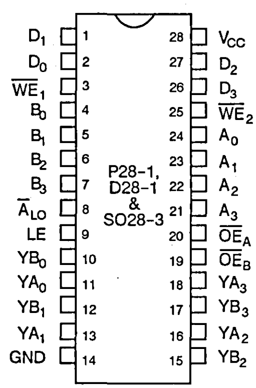
FUNCTIONAL BLOCK DIAGRAM

IDT39C707/A



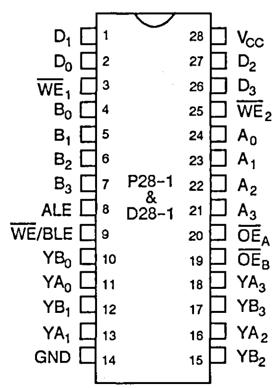
PIN CONFIGURATIONS

IDT39C705A/B

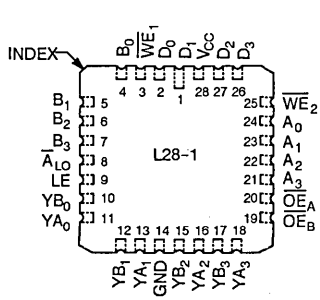


DIP/SOIC
TOP VIEW

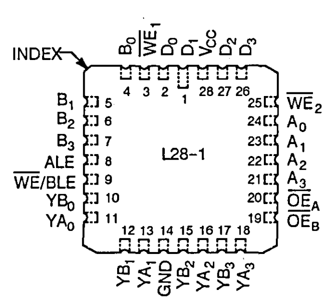
IDT39C707/A



DIP
TOP VIEW



LCC
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_0-A_3	I	Four address inputs at the A address decoder which select one of the 16 memory words for output through the A port.
B_0-B_3	I	Four address inputs at the B address decoder which select one of the 16 memory words for output through the B port. The B address field also selects the word into which new data is written.
D_0-D_3	I	Four inputs for writing new data into the RAM.
YA_0-YA_3	O	Four three-state A Data Latch outputs which display A port data and also allow several devices to be easily cascaded.
YB_0-YB_3	O	Four three-state B Data Latch outputs which display B port data and also allow several devices to be easily cascaded.
LE	I	The LE input controls the RAM A Data Latch and B Data Latch. When the LE input is HIGH, the latches are open (transparent) and the output data from the RAM is selected by the A and B address fields. When LE is LOW, the latches are closed and they retain the last data read from the RAM independent of changes in the A and B address fields (IDT39C705A/B only).
$\overline{A}_{LO}$	I	This input is used to force the A Data Latch. When $\overline{A}_{LO}$ input is HIGH, the A Latches operate in their normal fashion. Once the A Latches are forced LOW they remain LOW independent of the $\overline{A}_{LO}$ input if the latches are closed (IDT39C705A/B only).
ALE	I	This input controls the A Data Latch. When ALE is HIGH, the latch is open (transparent) and the data from the RAM, as selected by the A address field, is present at the A output. When ALE is LOW, the latch is closed and retains the last data read from the RAM independent of changes in the A address field (IDT39C707/A only).
$\overline{WE}_1$, $\overline{WE}_2$	I	When both Write Enables are LOW, new data can be written into the word selected by the B address fields. If either Write Enable input is HIGH, no new data can be written into the memory.
$\overline{WE}$/BLE	I	This input controls the writing of new data into the RAM and display of data at the B Data Latch output. When $\overline{WE}$/BLE is LOW together with $\overline{WE}_1$ and $\overline{WE}_2$, new data is written into the word selected by the B address fields. When $\overline{WE}$/BLE or any other Write Enable input is HIGH, no data is written into the RAM. When $\overline{WE}$/BLE is HIGH, the B Latch is open (transparent) and, when this input is LOW, the B Data Latch is closed (IDT39C707/A only).
$\overline{OE}_A$	I	When the A port output enable is LOW, data at the A Data Latch inputs in presented at the YA_I outputs. When $\overline{OE}_A$ is HIGH, the YA_I outputs are in the high-impedance (off) state.
$\overline{OE}_B$	I	When the B port output enable is LOW, data at the B Data Latch inputs is presented at the YB_I outputs. When $\overline{OE}_B$ is HIGH, the YB_I outputs are in the high-impedance (off) state.

IDT39C705A/B FUNCTION TABLES

WRITE CONTROL

$\overline{WE}_1$	$\overline{WE}_2$	FUNCTION	RAM OUTPUTS AT DATA-LATCH INPUTS	
			A-PORT	B-PORT
L	L	Write D into B	A Data (A ≠ B)	Input Data
L	L	Write D into B	Input Data (A = B)	Input Data
X	H	No Write	A-Data	B-Data
H	X	No Write	A-Data	B-Data

H = HIGH
L = LOW
X = Don't Care

YA READ CONTROL

INPUTS			YA OUTPUT	FUNCTION
$\overline{OE}_A$	$\overline{A}_{LO}$	LE		
H	X	X	Z	High Impedance
L	L	X	L	Force YA LOW
L	H	H	A Port RAM Data	Latches Transparent (Open)
L	H	L	NC	Latches Retain Data (Closed)

H = HIGH Z = High Impedance
L = LOW NC = No Change
X = Don't Care

YB READ CONTROL

INPUTS		YB OUTPUT	FUNCTION
$\overline{OE}_B$	LE		
H	X	Z	High Impedance
L	H	B Port RAM Data	Latches Transparent (Open)
L	L	NC	Latches Retain Data (Closed)

H = HIGH Z = High Impedance
L = LOW NC = No Change
X = Don't Care

IDT39C707/A FUNCTION TABLES

WRITE CONTROL

$\overline{WE_1}$	$\overline{WE_2}$	$\overline{WE}$/BLE	FUNCTION	RAM OUTPUTS AT LATCH INPUTS	
				A PORT	B PORT
L	L	L	Write D into B	A Data (A ≠ B)	Input Data
X	X	H	No Write	A-Data	B-Data
X	H	X	No Write	A-Data	B-Data
H	X	X	No Write	A-Data	B-Data

H = HIGH
L = LOW
X = Don't Care

YA READ CONTROL

INPUTS		YA OUTPUT	FUNCTION
$\overline{OE_A}$	ALE		
H	X	Z	High Impedance
L	H	A Port RAM Data	Latches Transparent (Open)
L	L	NC	Latches Retain Data (Closed)

H = HIGH Z = High Impedance
L = LOW NC = No Change
X = Don't Care

YB READ CONTROL

INPUTS		YB OUTPUT	FUNCTION
$\overline{OE_B}$	$\overline{WE}$/BLE		
H	X	Z	High Impedance
L	H	B Port RAM Data	Latches Transparent (Open)
L	L	NC	Latches Retain Data (Closed)

H = HIGH Z = High Impedance
L = LOW NC = No Change
X = Don't Care

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER [1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:

$T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (Commercial)
$T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (Military)
$V_{LC} = 0.2V$
$V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level (4)		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level (4)		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., $V_{IN} = V_{CC}$		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}	–	V
			I_{OH} = –12mA MIL.	2.4	4.3	–	
			I_{OH} = –15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 300\mu A$	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max. $\overline{OE} = V_{IH}$	V_O = 0V	–	-0.1	-10	µA
			$V_O = V_{CC}$ Max.	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V (3)		-15	–	–	mA
I_{CCQH}	Quiescent Power Supply Current $\overline{WE}$ = H	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{WE} = 0, $\overline{WE}$ = H		–	3	5	mA
I_{CCQL}	Quiescent Power Supply Current $\overline{WE}$ = L	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{WE} = 0, $\overline{WE}$ = L		–	3	5	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High) (5)	V_{CC} = Max., V_{IN} = 3.4V, f_{WE} = 0		–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	1.7	3.5	mA/ MHz
			COM'L.	–	1.7	2.5	
I_{CC}	Total Power Supply Current (6)	V_{CC} = Max., f_{WE} = 10MHz Outputs Open, $\overline{OE}$ = L $\overline{WE}$ = 50% Duty cycle $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	MIL.	–	20	40	mA
			COM'L.	–	20	30	
		V_{CC} = Max., f_{WE} = 10MHz Outputs Open, $\overline{OE}$ = L $\overline{WE}$ = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	25	50	
			COM'L.	–	25	40	

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, + 25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(WE_H) + I_{CCQL}(1 - WE_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{WE})$$

WE_H = Write duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{WE} = Write frequency.

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large V_{CC} current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

AC ELECTRICAL CHARACTERISTICS

PARAMETERS	FROM	TO	TEST CONDITIONS	IDT39C705A IDT39C707		IDT39C705B IDT39C707A		UNIT
				COM'L.	MIL.	COM'L.	MIL.	
Access Time	A or B Address Stable	YA Stable or YB Stable	LE = HIGH	25	30	20	24	ns
Turn-on Time	$\overline{OE}_A$ or $\overline{OE}_B$ LOW	YA or YB Stable		20	20	16	16	ns
Turn-off Time	$\overline{OE}_A$ or $\overline{OE}_B$ HIGH	YA or YB Off	C_L = 5pF	20	20	16	16	ns
Reset Time	$\overline{A}_{LO}$ LOW	YA LOW		20	20	16	16	ns
Latch Enable Time	LE HIGH	YA and YB Stable		20	22	16	16	ns
Transparency	$\overline{WE}_1$ and $\overline{WE}_2$ LOW	YA or YB	LE = HIGH	30	35	22	24	ns
	D	YA or YB	LE = HIGH	30	35	22	24	ns

MINIMUM SETUP AND HOLD TIME

PARAMETERS	FROM	TO	TEST CONDITIONS	IDT39C705A IDT39C707		IDT39C705B IDT39C707A		UNIT
				COM'L.	MIL.	COM'L.	MIL.	
Data Set-up Time	D Stable	Either $\overline{WE}$ HIGH		12	15	9	12	ns
Data Hold Time	Either $\overline{WE}$	D Changing		0	0	0	0	ns
Address Set-up Time	B Stable	Both $\overline{WE}$ LOW		6	8	4	6	ns
Address Hold Time	Either $\overline{WE}$ HIGH	B Changing		0	0	0	0	ns
Latch Close Before Write Begins	LE LOW	$\overline{WE}_1$ LOW	$\overline{WE}_2$ LOW	0	0	0	0	ns
	LE LOW	$\overline{WE}_2$ LOW	$\overline{WE}_1$ LOW	0	0	0	0	ns
Address Set-up Before Latch Closes	A or B Stable	LE LOW		12	15	9	12	ns

MINIMUM PULSE WIDTHS

PARAMETERS	INPUT	PULSE	TEST CONDITIONS	IDT39C705A IDT39C707		IDT39C705B IDT39C707A		UNIT
				COM'L.	MIL.	COM'L.	MIL.	
Write Pulse Width	$\overline{WE}_1$	HIGH-LOW-HIGH	$\overline{WE}_2$ LOW	15	15	12	12	ns
	$\overline{WE}_2$	HIGH-LOW-HIGH	$\overline{WE}_1$ LOW	15	15	12	12	ns
A Latch Reset Pulse	$\overline{A}_{LO}$	HIGH-LOW-HIGH		15	15	12	12	ns
Latch Data Capture	LE	LOW-HIGH-LOW		15	18	12	12	ns

NOTE:
The IDT39C705B/707A meet or exceed all the specifications of the IDT39C705A/707.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All other Outputs	Open

DEFINITIONS
C_L = Load capacitance: includes jig and probe capacitance
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

TEST LOAD CIRCUITS

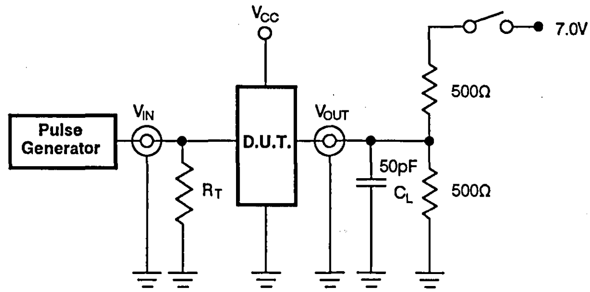


Figure 1. Switching Test Circuit

INPUT/OUTPUT INTERFACE CIRCUIT

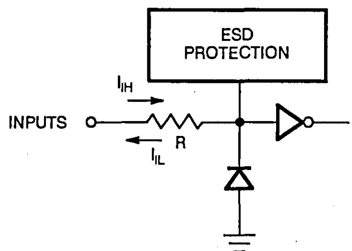


Figure 2. Input Structure

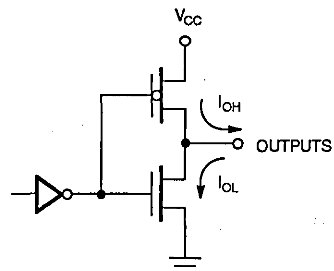


Figure 3. Output Structure

ORDERING INFORMATION

IDT XXXXXXX (Device Type/Speed) XX (Package) X (Process/Temperature Range)

Process/Temperature Range:

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

P	Plastic DIP
D	CERDIP
L	Leadless Chip Carrier
SO	Small Outline IC (IDT39C705 only)

Device Type/Speed:

39C705A	Standard Speed Dual-Port RAM
39C705B	High-Speed Dual-Port RAM
39C707	Standard Speed Dual-Port RAM
39C707A	High-Speed Dual-Port RAM

Integrated Device Technology, Inc.

HIGH PERFORMANCE CMOS MICROCYCLE LENGTH CONTROLLER

PRELIMINARY
IDT49C25
IDT49C25A

MICROSLICE™ PRODUCT

FEATURES:

- Similar function to AMD's Am2925 bipolar controller with improved speeds and output drive over full temperature and voltage supply extremes
- Four microcode-controlled clock outputs allow clock cycle length control for 15 to 30% increase in system throughput. Microcode selects one of eight clock patterns from 3 to 10 oscillator cycles in length
- System controls for $\overline{\text{RUN}}$/$\overline{\text{HALT}}$ and Single Step
  - Switch-debounced inputs provide flexible halt controls
- Low input/output capacitance
  - 6pF inputs (typ.)
  - 8pF outputs (typ.)
- CMOS power levels (5μW typ. static)
- Available in 300 mil 24-pin plastic and ceramic THINDIP, 28-pin LCC and PLCC packages and CERPACK
- Both CMOS and TTL output compatible
- Substantially lower input current levels than AMD's bipolar Am2900 series (5μA max.)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C25/A are single-chip general purpose clock generator/drivers built using IDT's advanced CEMOS™, a dual metal CMOS technology. It has microprogrammable clock cycle length to provide significant speed-up over fixed clock cycle approaches and meets a variety of system speed requirements.

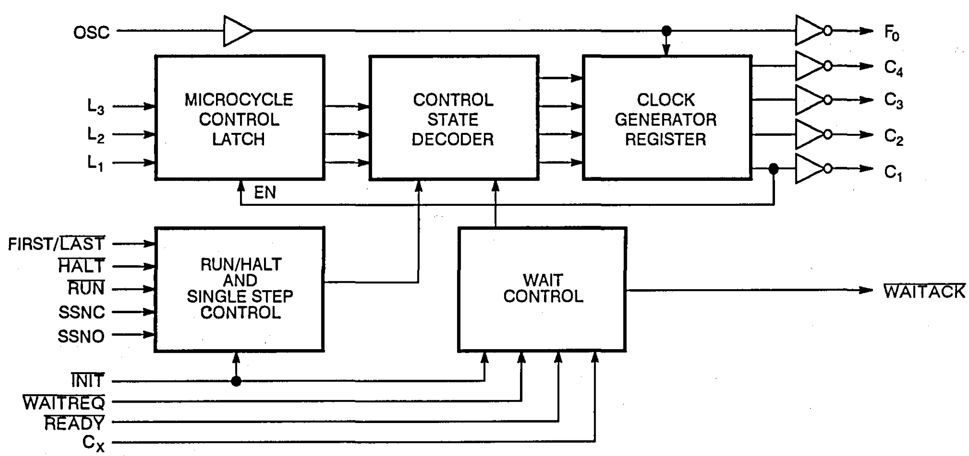
The IDT49C25/A generate four different simultaneous clock output waveforms tailored to meet the needs of the IDT3900 CMOS family and other MOS and bipolar microprocessor-based systems. One of eight cycle lengths may be generated under microprogram control using the cycle length inputs, L_1, L_2 and L_3.

A buffered oscillator output, F_0, is provided for external system timing in addition to the four microcode controlled clock outputs, C_1, C_2, C_3 and C_4.

System control functions include $\overline{\text{RUN}}$, $\overline{\text{HALT}}$, Single-Step, Initialize and Ready/Wait controls. In addition, the FIRST/$\overline{\text{LAST}}$ input determines where a halt occurs and the C_X input determines the end point timing of wait cycles. $\overline{\text{WAITACK}}$ indicates that the IDT49C25/A are in a wait state.

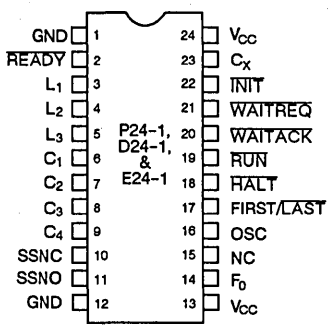
8

FUNCTIONAL BLOCK DIAGRAM

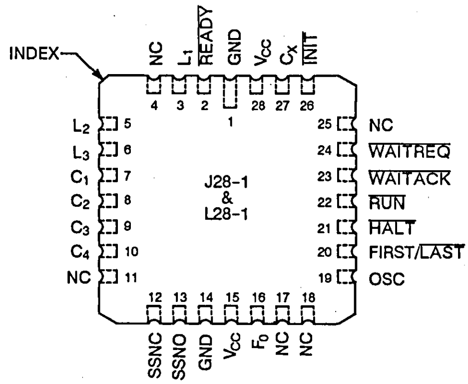


CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/CERPACK
TOP VIEW

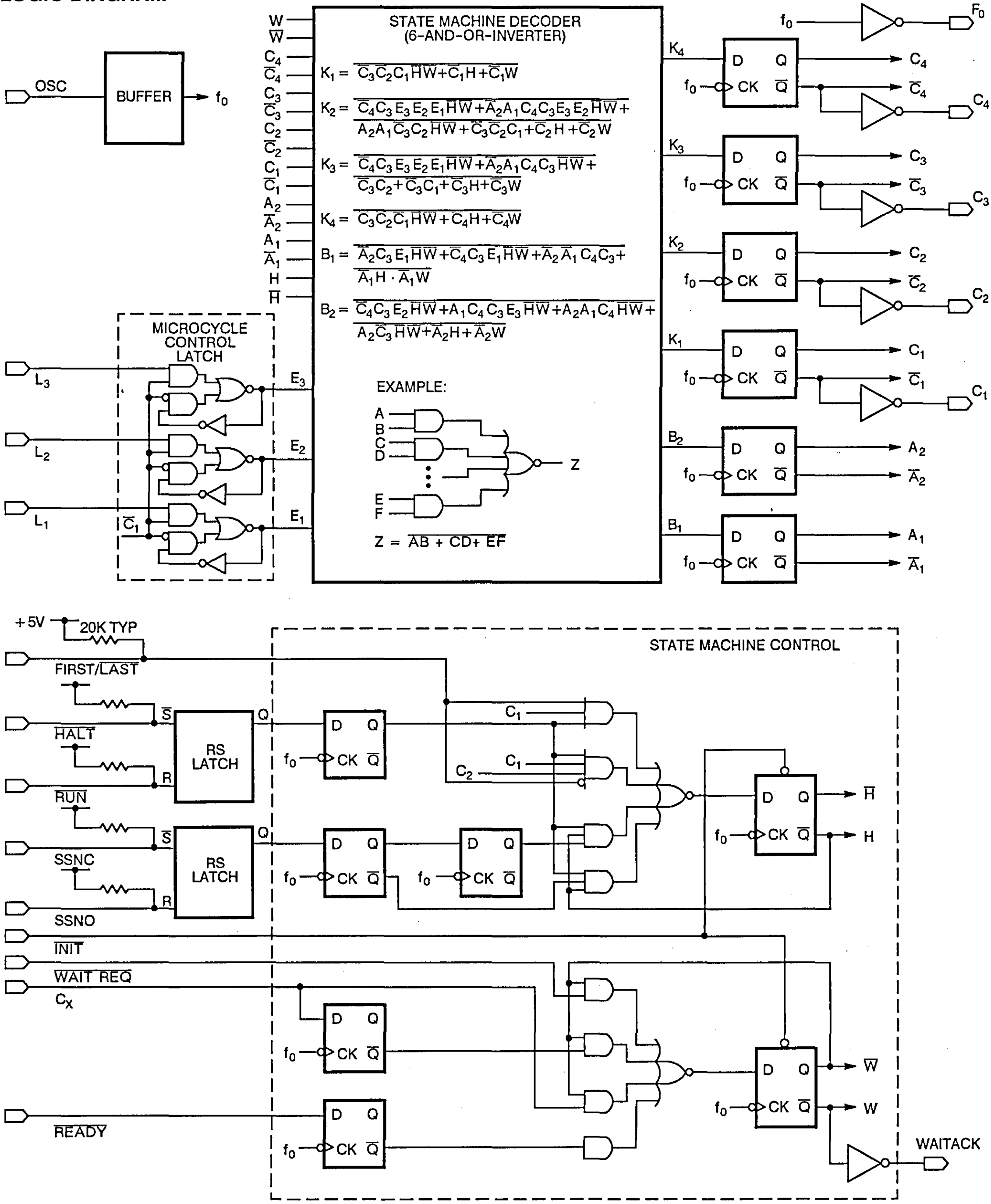


LCC/PLCC
TOP VIEW

PIN DESCRIPTIONS

PIN NO.	NAME	I/O	DESCRIPTION
6, 7, 8, 9	C_1, C_2, C_3, C_4	O	System clock outputs. These outputs are all active during every system clock cycle. Their timing is determined by clock cycle length controls, L_1, L_2 and L_3.
3, 4, 5	L_1, L_2, L_3	I	Clock cycle length control inputs. These inputs receive the microcode bits that select the microcycle lengths. They form a control word which selects one of the eight microcycle waveform patterns F_3 through F_{10}.
14	F_0	O	The buffered oscillator output. F_0 internally generates all of the timing edges for outputs C_1, C_2, C_3, C_4 and $\overline{\mathrm{WAITACK}}$. F_0 rises just prior to all of the C_1, C_2, C_3, C_4 transitions.
18, 19	$\overline{\mathrm{HALT}}$ and $\overline{\mathrm{RUN}}$	I	Debounced inputs to provide $\overline{\mathrm{HALT}}$ control. These inputs determine whether the output clocks run or not. A LOW input on $\overline{\mathrm{HALT}}$ ($\overline{\mathrm{RUN}}$ = HIGH) will stop all clock outputs.
17	FIRST/$\overline{\mathrm{LAST}}$	I	$\overline{\mathrm{HALT}}$ time control input. A HIGH input in conjunction with a $\overline{\mathrm{HALT}}$ command will cause a halt to occur when C_4 = LOW and C_1 = C_2 = C_3 = HIGH (see clock waveforms). A LOW input causes a $\overline{\mathrm{HALT}}$ to occur when C_1 = C_2 = C_3 = LOW and C_4 = HIGH.
11, 10	SSNO and SSNC	I	Single Step control inputs. These debounced inputs allow system clock cycle single stepping while $\overline{\mathrm{HALT}}$ is activated LOW.
21	$\overline{\mathrm{WAITREQ}}$	I	The Wait Request active LOW input. When LOW, this input will cause the outputs to halt during the next oscillator cycle after the C_X input goes LOW.
23	C_X	I	Wait cycle control input. The clock outputs respond to a wait request one oscillator clock cycle after C_X goes LOW. C_X is normally tied to any one of C_1, C_2, C_3 or C_4.
20	$\overline{\mathrm{WAITACK}}$	O	The Wait Acknowledge active LOW output. When LOW, this output indicates that all clock outputs are in the "WAIT" state.
2	$\overline{\mathrm{READY}}$	I	The $\overline{\mathrm{READY}}$ active LOW input is used to continue normal clock output patterns after a wait stage.
22	$\overline{\mathrm{INIT}}$	I	The Initialize active LOW input. This input is intended for use during power up initialization of the system. When LOW, all clock outputs run free regardless of the state of the Halt, Single Step, Wait Request and Ready inputs.
16	OSC	I	External oscillator input. (TTL level inputs.)

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	25	µA
I_{IL}		V_{CC} = Max. V_{IN} = 0.4V	SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$	–	–	-1.0	mA
			FIRST/$\overline{LAST}$	–	–	-1.5	
			Other Inputs	–	–	-5	µA
V_I	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		–	-0.7	-1.2	mA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = −32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300µA	V_{HC}	V_{CC}	–	
			I_{OH} = −3.0mA MIL.	2.4	4.0	–	
			I_{OH} = −5.0mA COM'L.	2.4	4.0	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 16mA MIL.	–	–	0.5	
			I_{OL} = 24mA COM'L.	–	–	0.5	

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS [1]	MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$	–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]	–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open — $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current [4]	V_{CC} = Max. Outputs Open f_I = 5MHz $\overline{READY}$, SSN0, $\overline{WAIT\ REQ}$, $\overline{HALT}$, $\overline{INIT}$ = V_{CC} L_1, L_2, L_3, SSNC, FIRST/$\overline{LAST}$, $\overline{RUN}$, C_X = GND	–	6.4	2.25	mA
		V_{CC} = Max. Outputs Open f_I = 5MHz SSN0, $\overline{HALT}$ = V_{CC} $\overline{READY}$, $\overline{WAIT\ REQ}$, $\overline{INIT}$ = 3.4V (98% duty cycle) L_1, L_2, L_3, SSNC, FIRST/$\overline{LAST}$, $\overline{RUN}$, C_X = GND	–	2.25	9.25	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}\ D_H\ N_T + I_{CCD}\ (f_{CP}/2)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input Transition pair (HLH or LHL)
   f_{CP} = ClockFrequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL		PARAMETER	CONDITION	IDT49C25					IDT49C25A[7]					UNIT
				TYP.[1]	COM'L.		MIL.		TYP.[6]	COM'L.		MIL.		
					MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
1	f_{MAX1}	F_0 Frequency (C_X Connected)[1]		–	31	–	31	–	–	40	–	40	–	ns
2	f_{MAX2}	F_0 Frequency (C_X = HIGH)		42	–	–	–	–	50	–	–	–	–	ns
3	t_{OFFSET}	F_0 (↑) to C_1, C_2, C_3, C_4 or $\overline{\text{WAITACK}}$ (↑)		–	–	8.5	–	8.5	–	–	6.0	–	6.0	ns
4	t_{OFFSET}	F_0 (↑) to C_1, C_2, C_3, C_4 or $\overline{\text{WAITACK}}$ (↓)		–	–	17	–	18	–	–	11.5	–	12	ns
5	t_{SKEW}	C_1 (↑) to C_2 (↑)		–	–	2	–	2	–	–	1.5	–	1.5	ns
6	t_{SKEW}	C_1 (↑) to C_3 (↑)		–	–	2	–	2	–	–	1.5	–	1.5	ns
7	t_{SKEW}	C_1 (↑) to C_4 (↓) Opposite Transition		–	–	11	–	11	–	–	8.0	–	8.0	ns
8	t_{SU}	L_1, L_2, L_3 to C_1 (↑)		–	4	–	4	–	–	–	3.0	–	3.0	ns
9	t_H	L_1, L_2, L_3 to C_1 (↑)	C_L = 50pF	–	8	–	8	–	–	–	6	–	6	ns
10	t_{SU}	C_X to F_0 (↑)[2]	R_L = 500Ω	–	18	–	18	–	–	12	–	12	–	ns
11	t_H	C_X to F_0 (↑)[2]		–	0	–	0	–	–	0	–	0	–	ns
12	t_{SU}	$\overline{\text{WAITREQ}}$ to F_0 (↑)[3]		–	18	–	18	–	–	12	–	12	–	ns
13	t_H	$\overline{\text{WAITREQ}}$ to F_0 (↑)[3]		–	0	–	0	–	–	0	–	0	–	ns
14	t_{SU}	$\overline{\text{READY}}$ to F_0 (↑)[3]		–	18	–	18	–	–	12	–	12	–	ns
15	t_H	$\overline{\text{READY}}$ to F_0 (↑)[3]		–	0	–	0	–	–	0	–	0	–	ns
16	t_{SU}	$\overline{\text{RUN}}$, $\overline{\text{HALT}}$ (↑) to F_0 (↑)[3, 4]		–	18	–	18	–	–	12	–	12	–	ns
17	t_{SU}	SSNC, SSNO to F_0 (↑)[3, 4]		–	18	–	18	–	–	12	–	12	–	ns
18	t_{SU}	FIRST/$\overline{\text{LAST}}$ to F_0 (↑)[5]		–	18	–	18	–	–	12	–	12	–	ns
19	t_{SU}	$\overline{\text{INIT}}$ (↑) to F_0 (↑)[3]		–	18	–	18	–	–	12	–	–	–	ns
20	t_{PWL}	$\overline{\text{INIT}}$ LOW Pulse Width		–	20	–	25	–	–	18	–	2.3	–	ns
21	t_{PLH}	$\overline{\text{INIT}}$ to $\overline{\text{WAITACK}}$		–	–	25	–	27	–	–	16	–	18	ns
22	t_{PLH}	OSC to F_0		–	–	13	–	16	–	–	8.5	–	10.5	ns
23	t_{PHL}			–	–	13	–	16	–	–	8.5	–	10.5	ns

NOTES:

1. The frequency guarantees apply with C_X connected to C_1, C_2, C_3, C_4, or HIGH. The C_X input load must be considered part of the 50pf/500Ω clock output loading.
2. These set-up and hold times apply to the F_0 LOW-to-HIGH transition of the period in which C_X goes LOW.
3. These inputs are synchronized internally. Failure to meet t_S may cause a $1/F_0$ delay but will not cause incorrect operation.
4. These inputs are "debounced" by an internal R-S flip-flop and are intended to be connected to manual break-before-sake switches.
5. FIRST/$\overline{\text{LAST}}$ normally wired HIGH or LOW.
6. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
7. These values are preliminary only.

SWITCHING WAVEFORMS

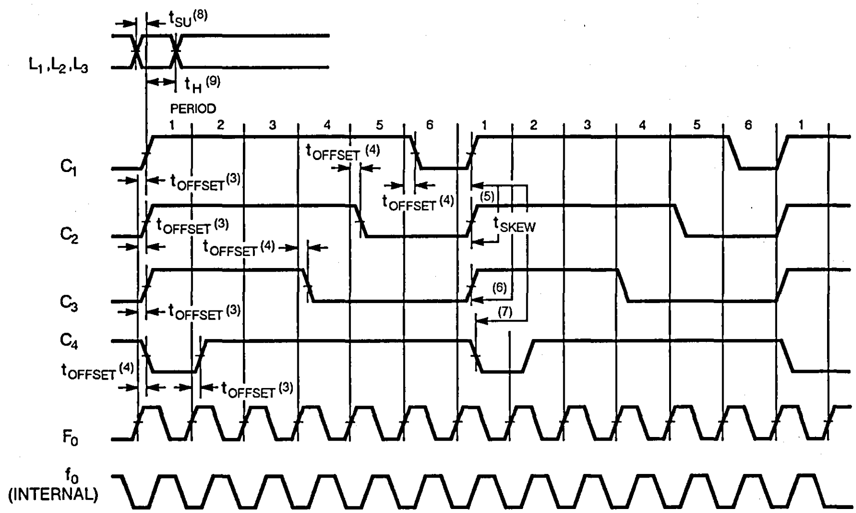


Figure 2. Normal Cycle Without Wait States (Pattern F_6 Shown)

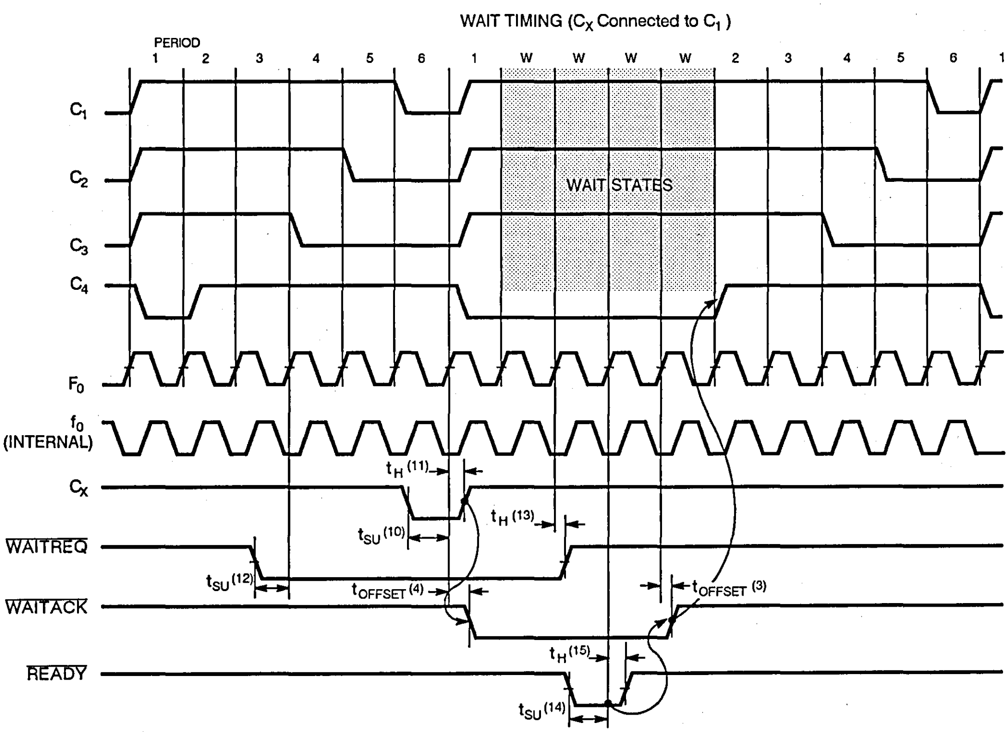


Figure 3. Wait Timing (C_X Connected to C_1)

DETAILED DESCRIPTION

The IDT49C25/A are dynamically programmable general-purpose clock controllers. They can be logically separated into two parts—a state machine decoder and a state machine control section.

The state machine takes microcode information from the Microcycle Length (L) inputs L_1, L_2 and L_3 and counts the fundamental frequency of the oscillator (OSC) to create the clock outputs F_0, C_1, C_2, C_3 and C_4.

The clock outputs have a characteristic wave shape relationship for each microcycle length. For example, C_1 is always LOW only on the last F_0 clock period of a microcycle and C_4 is always LOW on the first. C_3 has an approximate duty cycle of 50% and C_2 is HIGH for all but the last two periods (see Figure 4).

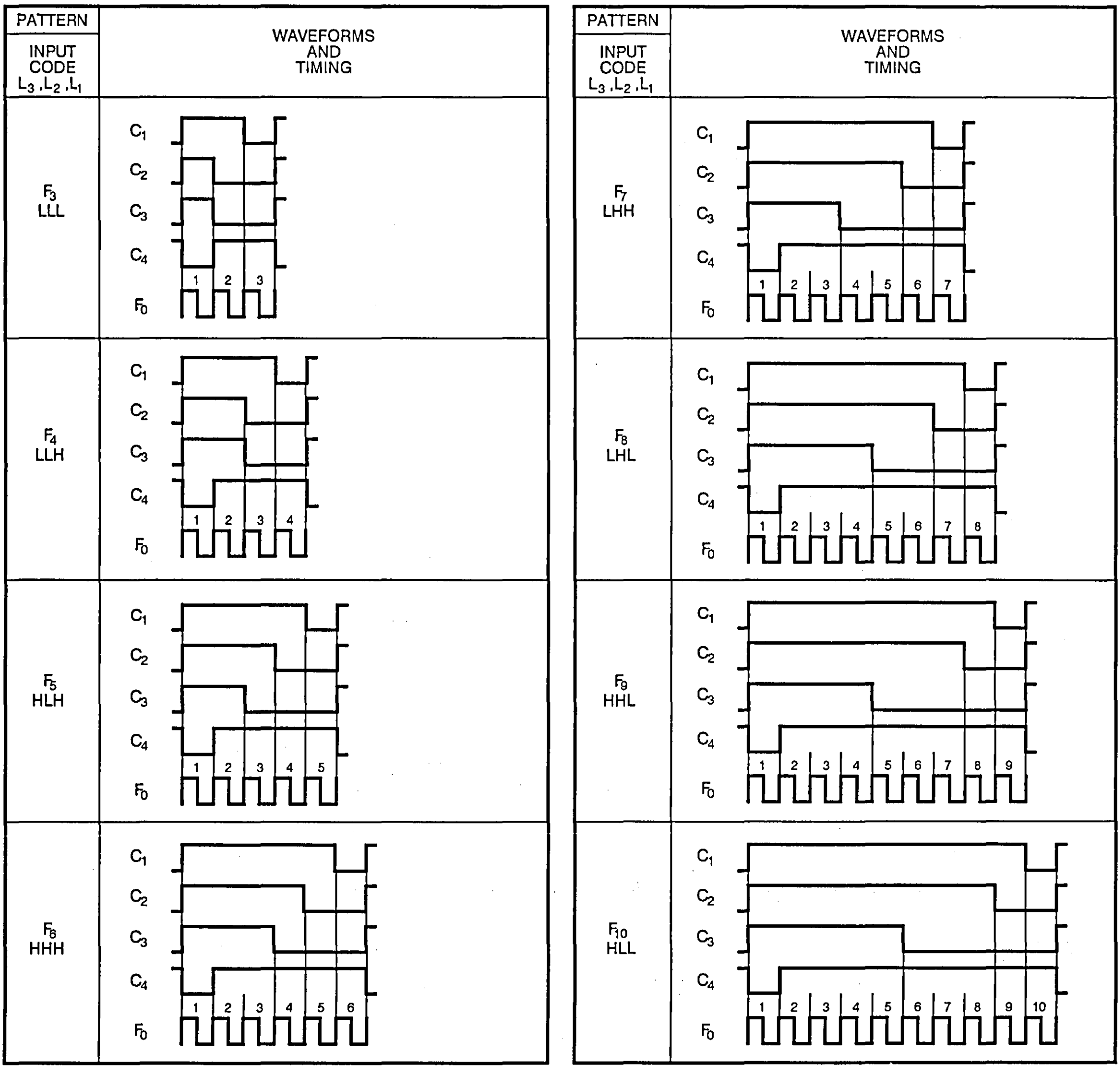


Figure 4. IDT49C25/A Clock Waveforms

The current state of the machine is contained in a register, part of which is the Clock Generator Register. C_1, C_2, C_3 and C_4 are the outputs of this register. These outputs and the outputs of the Microcycle Control Latch are fed into combinatorial logic to generate the next state. On each falling edge of the internal clock, the next state is entered into the current state register. The Microcycle Control Latch is latched when C_1 is HIGH. This means that it will be loaded during the last state of each microcycle (C_1 = C_2 = C_3 = LOW, C_4 = HIGH). This internal latch selects one of eight possible microcycle lengths, F_3 to F_{10}.

The state machine control logic, which determines the mode of operation of the state machine, is intended to be connected to a front panel. There are four basic modes of operation of the IDT49C25/A comprised of $\overline{\text{RUN}}$, $\overline{\text{HALT}}$, $\overline{\text{WAIT}}$ and SINGLE STEP.

System Timing

In the typical computer, the time required to execute different instructions varies. However, the time allotted to each instruction is the time that it takes to execute the longest instruction. The IDT49C25/A allow the user to dynamically vary the time allotted for each instruction, thereby allowing the user to realize a higher throughput.

IDT49C25/A Control Inputs

The control inputs fall into two categories, microcycle length control and clock control. Microcycle length control is provided via the "L" inputs which are intended to be connected to the microprogram memory. The "L" inputs are used to select one of eight cycle lengths ranging from three oscillator cycles for pattern F_3 to ten oscillator cycles for pattern F_{10}. This information is always loaded at the end of the microcycle into the Microcycle Control Latch which performs the function of a pipeline register for the microcycle length microcode bits. Therefore, the cycle length goes in the same microword as the instruction that it is associated with.

The clock control inputs are used to synchronize the microprogram machine with the external world and I/O devices. Inputs like $\overline{\text{RUN}}$, $\overline{\text{HALT}}$, SSNO and SSNC, which start and stop execution, are meant to be connected to switches on the front panel of the microprogrammed machine (see Figure 5). These inputs have internal pull-up resistors and are connected to an R-S flip-flop in order to provide switch debouncing. The FIRST/$\overline{\text{LAST}}$ input is used to determine at what point of the microcycle the IDT49C25/A will halt when $\overline{\text{HALT}}$ or a SINGLE STEP is initiated. In most applications, the user wires this input HIGH or LOW, depending on his design.

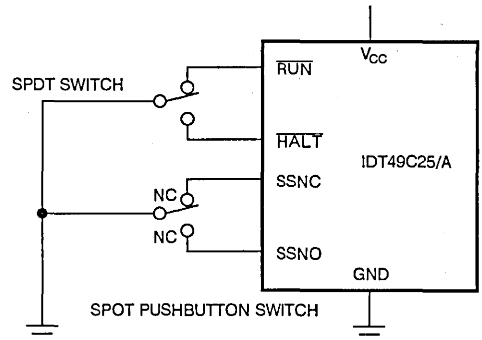


Figure 5. Switch Connection for $\overline{\text{RUN}}$/$\overline{\text{HALT}}$ and Single Step

When $\overline{\text{HALT}}$ is held low ($\overline{\text{RUN}}$ = HIGH), the state machine will start the halt mode on the last (C_1 = LOW) or the first (C_4 = LOW) state of the microcycle as determined by the FIRST/$\overline{\text{LAST}}$ input. When $\overline{\text{RUN}}$ goes low ($\overline{\text{HALT}}$ = HIGH), the state machine will resume the run mode.

The $\overline{\text{WAITREQ}}$, C_X, $\overline{\text{READY}}$ and $\overline{\text{WAITACK}}$ signals are used to synchronize other parts of a computer system (memory, I/O devices) to the CPU by dynamically stretching the microcycle. For example, the CPU may access a slow peripheral that requires the data remain on the data bus for several microseconds. In this case, the peripheral pulls the $\overline{\text{WAITREQ}}$ line LOW. The C_X input lets the design specify when the $\overline{\text{WAITREQ}}$ line is sampled in the microcycle. This has a direct impact on how much time the peripheral has to respond in order to request a wait cycle (see Figure 6). The $\overline{\text{READY}}$ line is used by the peripheral to signal when it is ready to resume execution of the rest of the microcycle. The $\overline{\text{WAITACK}}$ line goes LOW on the next oscillator cycle after the C_X input goes LOW and remains LOW until the second oscillator cycle after $\overline{\text{READY}}$ goes LOW.

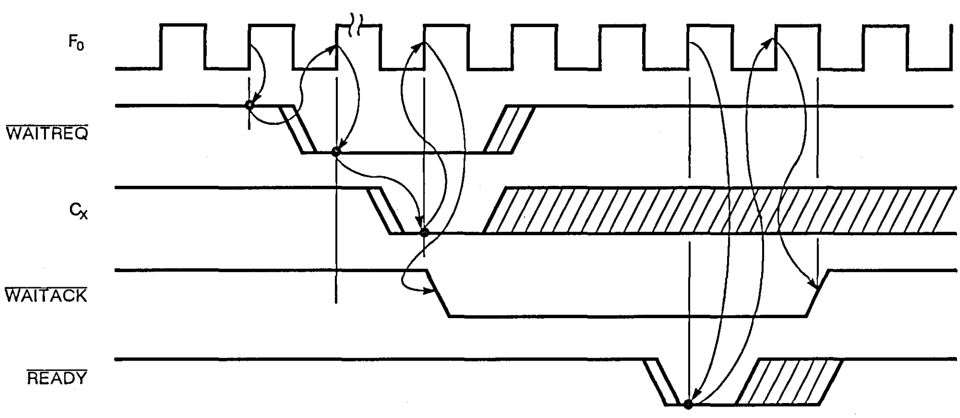


Figure 6. $\overline{\text{WAIT}}$/$\overline{\text{READY}}$ Timing

The SSNO and SSNC inputs are used to initiate the SINGLE STEP mode. These debounced inputs allow a single microcycle to occur while in the halt mode. SSNO (normally open) and SSNC (normally closed) are intended to be connected to a momentary SPDT switch. After SSNO has been low for one clock edge, the state machine will change to the next run mode. The microcycle will end on the first or last state of the microcycle, depending on the state of the FIRST/$\overline{\text{LAST}}$.

AC Timing Signal References

Set-up and hold times in registers and latches are measured relative to the clock signals that drive them. In the IDT49C25/A, the external oscillator provides a free running clock signal that drives all the registers on the devices. This clock is provided for the user through the buffered output of F_0. Therefore, F_0 is used as the reference of set-up, hold and clock-to-output times. However, for the Microcycle Control Latch, the set-up and hold times are referenced to the C_1 output which is the buffered version of the latch enable. This reference is appropriate for the Microcycle Control Latch because, in a typical application, this latch is considered part of the pipeline registered which is also driven by one of the "C" outputs.

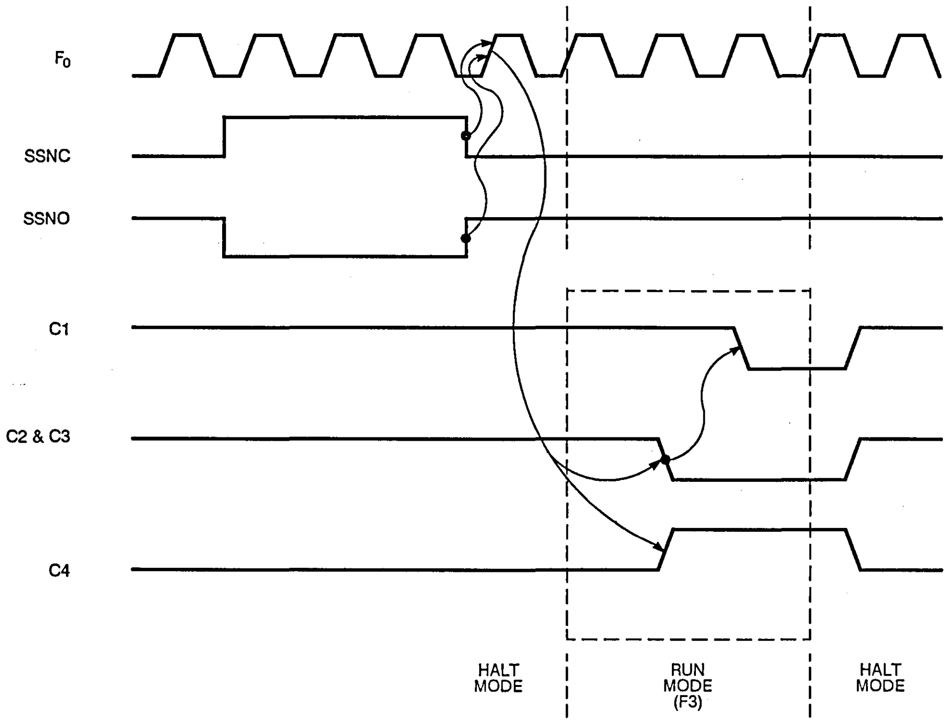
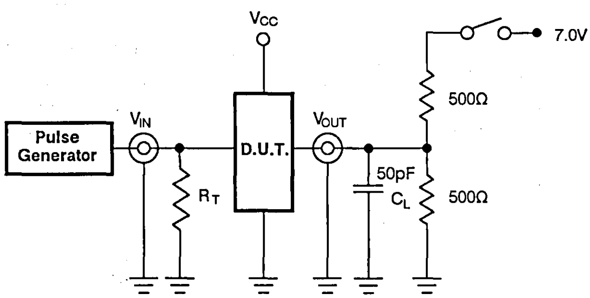


Figure 7. Single Step Timing Sequence

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR THREE-STATE OUTPUTS



SWITCH POSITION

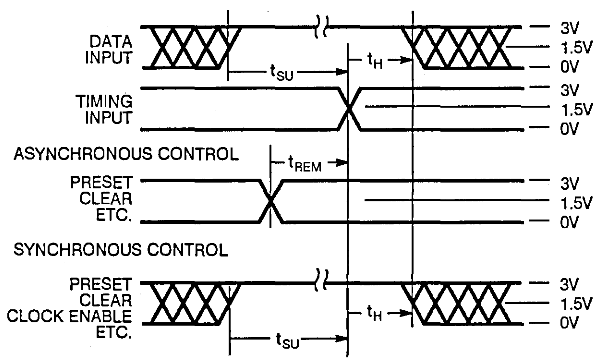
TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS

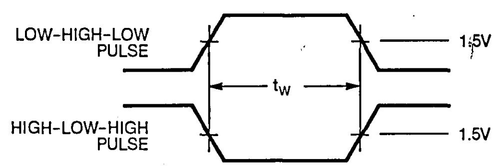
C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

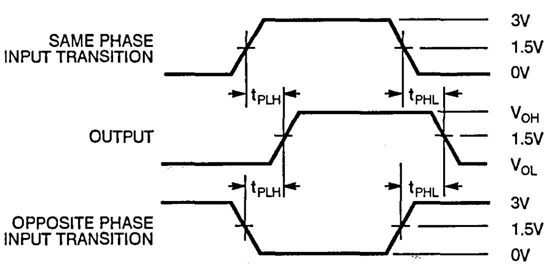
SET-UP, HOLD AND RELEASE TIMES



PULSE WIDTH



PROPAGATION DELAY



ORDERING INFORMATION

IDT49C25/A XX (Device Type) X (Package) X (Process/Temperature)

Field	Code	Description
Process/Temperature	BLANK	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	J	Plastic Leaded Chip Carrier
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	25	Microcycle Length Controller
	25A	Fast Microcycle Length Controller

Integrated Device Technology, Inc.

16-BIT CMOS MICROPROCESSOR SLICE

IDT49C401
IDT49C401A

MICROSLICE ™ PRODUCT

FEATURES:

- Fast
  - 30% faster than four 2901Cs and one 2902A
- Low Power CEMOS ™
  - Military: 225mA (max.)
  - Commercial: 180mA (max.)
- Functionally equivalent to four 2901s and one 2902
- Pin-compatible, performance-enhanced replacement for IMI4X2901B
- Independent, simultaneous access to two 16-word x 16-bit register files
- Expanded destination functions with eight new operations allowing Direct Data to be loaded directly into the dual-port RAM and Q Register
- Cascadable
- Available in 64-pin DIP
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

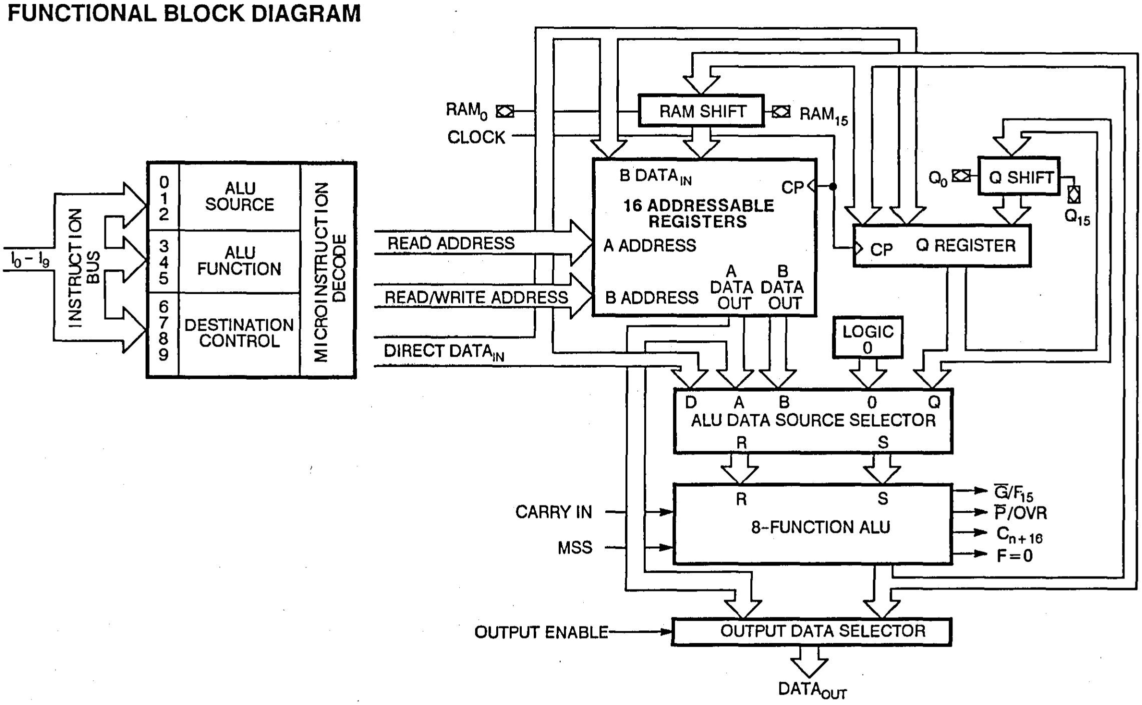
The IDT49C401s are high-speed, fully cascadable 16-bit CMOS microprocessor slice units which combine the standard functions of four 2901s and a 2902 with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

The IDT49C401s include all of the normal functions associated with standard 2901 bit-slice operation: (a) a 3-bit instruction field (I_0, I_1, I_2) which controls the source operand selection for the ALU, (b) a 3-bit microinstruction field (I_3, I_4, I_5) used to control the eight possible functions of the ALU and (c) sixteen destination control functions which are selected by the microcode inputs (I_6, I_7, I_8, I_9). Eight of the sixteen destination control functions reflect the standard 2901 operation, while the other eight additional destination control functions allow for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU and new combinations of destination functions with the RAM A port output available at the Y output pins of the device. Also featured is an on-chip dual-port RAM that contains 16 words by 16 bits.

The IDT49C401s are fabricated using CEMOS, a CMOS technology designed for high performance and high reliability. These performance enhanced devices feature both bipolar speed and bipolar output drive capabilities, while maintaining exceptional microinstruction speeds at greatly reduced CMOS power levels.

8

FUNCTIONAL BLOCK DIAGRAM

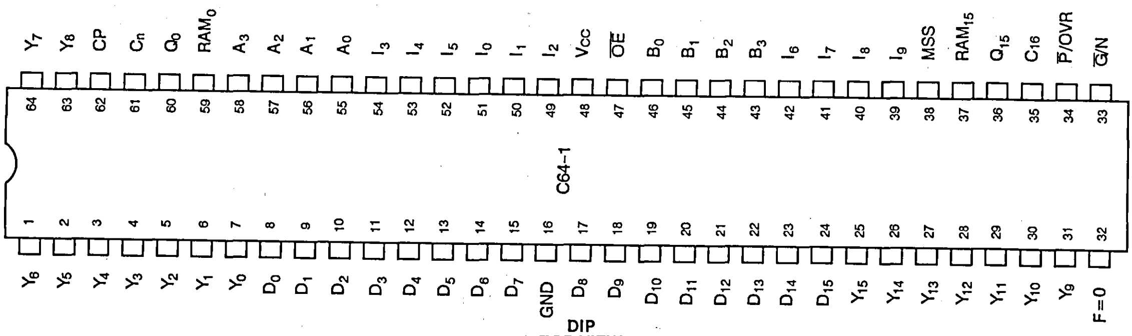


CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-9010/-

PIN CONFIGURATION



DIP
TOP VIEW

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_0-A_3	I	Four address inputs to the register file which selects one register and displays its contents through the A port.
B_0-B_3	I	Four address inputs to the register file which selects one of the registers in the file, the contents of which is displayed through the B port. It also selects the location into which new data can be written when the clock goes LOW.
I_0-I_9	I	Ten instruction control lines which determine what data source will be applied to the ALU $I_{(0, 1, 2)}$, what function the ALU will perform $I_{(3, 4, 5)}$ and what data is to be deposited in the Q Register or the register file $I_{(6, 7, 8, 9)}$. Original 2901 destinations are selected if I_9 is disconnected. In this mode, proper I_9 bias is controlled by an internal pullup resistor to V_{CC}.
D_0-D_{15}	I	Sixteen-bit direct data inputs which are the data source for entering external data into the device ALU, Q Register or RAM. D_0 is the LSB.
Y_0-Y_{15}	O	Sixteen three-state output lines which, when enabled, display either the sixteen outputs of the ALU or the data on the A port of the register stack. This is determined by the destination code $I_{(6, 7, 8, 9)}$.
$\overline{G}/F_{15}$	O	A multipurpose pin which indicates the carry generate ($\overline{G}$) function at the least significant and intermediate slices or as F_{15}, the most significant ALU output (sign bit). $\overline{G}/F_{15}$ selection is controlled by the MSS pin. If MSS = HIGH, F_{15} is enabled. If MSS = LOW, $\overline{G}$ is enabled.
F = 0	O	Open drain output which goes HIGH if the F_0-F_{15} ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C_n	I	Carry-in to the internal ALU.
C_{n+16}	O	Carry-out of the internal ALU.
Q_{15} RAM_{15}	I/O	Bidirectional lines controlled by $I_{(6, 7, 8, 9)}$. Both are three-state output drivers connected to the TTL-compatible inputs. When the destination code on $I_{(6, 7, 8, 9)}$ indicates an up shift, the three-state outputs are enabled, the MSB of the Q Register is available on the Q_{15} pin and the MSB of the ALU output is available on the RAM_{15} pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q_0 RAM_0	I/O	Both bidirectional lines function identically to Q_{15} and RAM_{15} lines, except they are the LSB of the Q Register and RAM.
$\overline{OE}$	I	Output enable. When pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
$\overline{P}$/OVR	O	A multipurpose pin which indicates the carry propagate ($\overline{P}$) output for performing a carry lookahead operation or overflow (OVR) the Exclusive-OR of the carry-in and carry-out of the ALU MSB. OVR, at the most significant end of the word, indicates that the result of an arithmetic two's complement operation has overflowed into the sign bit. $\overline{P}$/OVR selection is controlled by the MSS pin. If MSS = HIGH, OVR is enabled. If MSS = LOW, $\overline{P}$ is enabled.
CP	I	The clock input. LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 64 x 16 RAM which compromises the master latches of the register file. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.
MSS	I	When HIGH, enables OVR and F_{15} on the $\overline{P}$/OVR and $\overline{G}/F_{15}$ pins. When LOW, enables $\overline{G}$ and $\overline{P}$ on these pins. If left open, internal pullup resistor to V_{CC} provides declaration that the device is the most significant slice and will define pins as OVR and F_{15}.

DEVICE ARCHITECTURE:

The IDT49C401 CMOS bit-slice microprocessor is configured sixteen bits wide and is cascadable to any number of bits (16, 32, 48, 64). Key elements which make up these 16-bit microprocessor slices are the (1) register file (16 x 16 dual-port RAM) with shifter, (2) ALU and (3) Q Register and shifter.

REGISTER FILE—A 16-bit data word from one of the 16 RAM registers can be read from the A port as selected by the 4-bit A address field. Simultaneously, the same data word or any other word from the 16 RAM registers can be read from the B port as selected by the 4-bit B address field. New data is written into the RAM register location selected by the B address field during the clock (CP) LOW time. Two 16-bit latches hold the RAM A port and B port during the clock (CP) LOW time, eliminating any data races. During clock HIGH, these latches are transparent, reading the data selected by the A and B addresses. The RAM data input field is driven from a four-input multiplexer that selects the ALU output or the D inputs. The ALU output can be shifted up one position, down one position or not shifted. Shifting data operations involves the RAM_{15} and RAM_0 I/O pins. For a shift up operation, the RAM shifter MSB is connected to an enabled RAM_{15} I/O output while the RAM_0 I/O input is selected as the input to the LSB. During a shift down operation, the RAM shifter LSB is connected to an enabled RAM_0 I/O output, while the RAM_{15} I/O input is selected as the input to the MSB.

ALU—The ALU can perform three binary arithmetic and five logic operations on the two 16-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer, with both having a zero source operand. Both multiplexers are controlled by the $I_{(0,1,2)}$ inputs. This multiplexer configuration enables the user to select various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. Microinstruction inputs $I_{(3,4,5)}$ are used to select the ALU function. This high-speed ALU cascades to any word length, providing carry-in (C_n), carry-out (C_{n+16}) and an open-drain (F = 0) output. When all bits of the ALU are zero, the pull-down device of F = 0 is off, allowing a wire-OR of this pin over all cascaded devices. Multipurpose pins $\overline{G}/F_{15}$ and $\overline{P}$/OVR are aimed at accelerating arithmetic operations. For intermediate and least significant slices, the MSS pin is programmed LOW, selecting the carry-generate ($\overline{G}$) and carry-propagate ($\overline{P}$) output functions to be used by carry lookahead logic. For the most significant slice, MSS is programmed high, selecting the sign-bit (F_{15}) and the two's complement overflow (OVR) output functions. The sign bit (F_{15}) allows the ALU sign bit to be monitored without enabling the three-state ALU outputs. The overflow (OVR) output is high when the two's complement arithmetic operation has overflowed into the sign bit as logically determined from the Exclusive-OR of the carry-in and carry-out of the most significant bit of the ALU. For all 16-bit applications, the MSS pin on the IDT49C401s is tied high or not connected since only one device is needed. With MSS open or tied high, internal circuitry will direct pins 33 and 34 to function as F_{15} and OVR, respectively. It is in this 16-bit operating mode that the IDT49C401s function identically to the IMI4X2901B. The ALU data outputs are available at the three-state outputs $Y_{(0-15)}$ or as inputs to the RAM register file and Q Register under control of the $I_{(6,7,8,9)}$ instruction inputs.

Q REGISTER—The Q Register is a separate 16-bit register intended for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. It is driven from a 4-input multiplexer. In the no-shift mode, the multiplexer enters the ALU F output or Direct Data into the Q Register. In either the shift up or shift down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q_0 and Q_{15}, which operate comparably to the RAM shifter. They are controlled by the $I_{(6,7,8,9)}$ inputs.

The clock input of the IDT49C401 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW-to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and $I_{(6,7,8,9)}$ define the RAM as the destination, new data will be written into the RAM file defined by the B address field.

8

ALU SOURCE OPERAND CONTROL

MNEMONIC	MICROCODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	OCTAL CODE	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

ALU FUNCTION CONTROL

MNEMONIC	MICROCODE				ALU FUNCTION	SYMBOL
	I_5	I_4	I_3	OCTAL CODE		
ADD	L	L	L	0	R Plus S	$R + S$
SUBR	L	L	H	1	S Minus R	$S - R$
SUBS	L	H	L	2	R Minus S	$R - S$
OR	L	H	H	3	R OR S	$R \vee S$
AND	H	L	L	4	R AND S	$R \wedge S$
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \veebar S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

ALU ARITHMETIC MODE FUNCTIONS

OCTAL		C_n = L		C_n = H	
$I_{5,4,3}$	$I_{2,1,0}$	GROUP	FUNCTION	GROUP	FUNCTION
0	0	ADD	A + Q	ADD plus one	A + Q + 1
0	1		A + B		A + B + 1
0	5		D + A		D + A + 1
0	6		D + Q		D + Q + 1
0	2	PASS	Q	Increment	Q + 1
0	3		B		B + 1
0	4		A		A + 1
0	7		D		D + 1
1	2	Decrement	Q - 1	PASS	Q
1	3		B - 1		B
1	4		A - 1		A
2	7		D - 1		D
2	2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2	3		-B - 1		-B
2	4		-A - 1		-A
1	7		-D - 1		-D
1	0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1	1		B - A - 1		B - A
1	5		A - D - 1		A - D
1	6		Q - D - 1		Q - D
2	0		A - Q - 1		A - Q
2	1		A - B - 1		A - B
2	5		D - A - 1		D - A
2	6		D - Q - 1		D - Q

ALU LOGIC MODE FUNCTIONS

OCTAL		GROUP	FUNCTION
$I_{5,4,3}$	$I_{2,1,0}$		
4	0	AND	$A \wedge Q$
4	1		$A \wedge B$
4	5		$D \wedge A$
4	6		$D \wedge Q$
3	0	OR	$A \vee Q$
3	1		$A \vee B$
3	5		$D \vee A$
3	6		$D \vee Q$
6	0	EX-OR	$A \veebar Q$
6	1		$A \veebar B$
6	5		$D \veebar A$
6	6		$D \veebar Q$
7	0	EX-NOR	$\overline{A \veebar Q}$
7	1		$\overline{A \veebar B}$
7	5		$\overline{D \veebar A}$
7	6		$\overline{D \veebar Q}$
7	2	INVERT	$\overline{Q}$
7	3		$\overline{B}$
7	4		$\overline{A}$
7	7		$\overline{D}$
6	2	PASS	Q
6	3		B
6	4		A
6	7		D
3	2	PASS	Q
3	3		B
3	4		A
3	7		D
4	2	"ZERO"	0
4	3		0
4	4		0
4	7		0
5	0	MASK	$\overline{A} \wedge Q$
5	1		$\overline{A} \wedge B$
5	5		$\overline{D} \wedge A$
5	6		$\overline{D} \wedge Q$

SOURCE OPERAND AND ALU FUNCTION MATRIX [1]

OCTAL $I_{5,4,3}$	ALU FUNCTION	$I_{2,1,0}$ OCTAL							
		0	1	2	3	4	5	6	7
		ALU SOURCE							
		A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q - A - 1 Q - A	B - A - 1 B - A	Q - 1 Q	B - 1 B	A - 1 A	A - D - 1 A - D	Q - D - 1 Q - D	-D - 1 -D
2	C_n = L R Minus S C_n = H	A - Q - 1 A - Q	A - B - 1 A - B	-Q - 1 -Q	-B - 1 -B	-A - 1 -A	D - A - 1 D - A	D - Q - 1 D - Q	D - 1 D
3	R OR S	A V Q	A V B	Q	B	A	D V A	D V Q	D
4	R AND S	$A \wedge Q$	$A \wedge B$	0	0	0	$D \wedge A$	$D \wedge Q$	0
5	$\bar{R}$ AND S	$\bar{A} \wedge Q$	$\bar{A} \wedge B$	Q	B	A	$\bar{D} \wedge A$	$\bar{D} \wedge Q$	0
6	R EX-OR S	$A \veebar Q$	$A \veebar B$	Q	B	A	$D \veebar A$	$D \veebar Q$	D
7	R EX-NOR S	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\bar{Q}$	$\bar{B}$	$\bar{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\bar{D}$

NOTE:
1. + = Plus; - = Minus; $\wedge$ = AND; $\veebar$ = EX-OR; V = OR

ALU DESTINATION CONTROL [1]

MNEMONIC	MICROCODE					RAM FUNCTION		Q REGISTER FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER		
	I_9	I_8	I_7	I_6	HEX CODE	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_{15}	Q_0	Q_{15}	
OREG	H	L	L	L	8	X	NONE	NONE	F→Q	F	X	X	X	X	Existing 2901 Functions
NOP	H	L	L	H	9	X	NONE	X	NONE	F	X	X	X	X	
RAMA	H	L	H	L	A	NONE	F→B	X	NONE	A	X	X	X	X	
RAMF	H	L	H	H	B	NONE	F→B	X	NONE	F	X	X	X	X	
RAMQD	H	H	L	L	C	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_{15}	Q_0	IN_{15}	
RAMD	H	H	L	H	D	DOWN	F/2→B	X	NONE	F	F_0	IN_{15}	Q_0	X	
RAMQU	H	H	H	L	E	UP	2F→B	UP	2Q→Q	F	IN_0	F_{15}	IN_0	Q_{15}	
RAMU	H	H	H	H	F	UP	2F→B	X	NONE	F	IN_0	F_{15}	X	Q_{15}	
DFF	L	L	L	L	0	NONE	D→B	NONE	F→Q	F	X	X	X	X	New Added IDT49C401 Functions
DFA	L	L	L	H	1	NONE	D→B	NONE	F→Q	A	X	X	X	X	
FDF	L	L	H	L	2	NONE	F→B	NONE	D→Q	F	X	X	X	X	
FDA	L	L	H	H	3	NONE	F→B	NONE	D→Q	A	X	X	X	X	
XQDF	L	H	L	L	4	X	NONE	DOWN	Q/2→Q	F	X	X	Q_0	IN_{15}	
DXF	L	H	L	H	5	NONE	D→B	X	NONE	F	X	X	Q_0	X	
XQUF	L	H	H	L	6	X	NONE	UP	2Q→Q	F	X	X	IN_0	Q_{15}	
XDF	L	H	H	H	7	X	NONE	NONE	D→Q	F	X	X	X	Q_{15}	

NOTE:
1. X = Don't Care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs
UP is toward MSB; DOWN is toward LSB

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC}-0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level [4]		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level [4]		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10	µA
			V_O = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V [3]		-15	-30	–	mA

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd.)

$T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (Commercial)
$T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (Military)
$V_{LC} = 0.2V$
$V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = H	MIL.		150	245	mA
			COM'L.		150	195	
I_{CCQL}	Quiescent Power Supply Current CP = L	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = L	MIL.		80	125	mA
			COM'L.		80	98	
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	2.0	3.0	mA/ MHz
			COM'L.	–	2.0	2.5	
I_{CC}	Total Power Supply Current [6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	MIL.	–	135	210	mA
			COM'L.	–	135	170	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	145	225	
			COM'L.	–	145	180	

NOTES:
5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock Input frequency

8

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.

IDT49C401A AC ELECTRICAL CHARACTERISTICS (Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C401A over the -55°C to +125°C and 0°C to +70°C temperature ranges. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNIT
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	28	24	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)	35	41	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period	36	31	ns

COMBINATIONAL PROPAGATION DELAYS (1) C_L = 50pF

FROM INPUT	TO OUTPUT																UNIT
	Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15}		(MSS = H) OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	41	37	39	35	41	37	41	37	37	34	41	37	40	36	–	–	ns
D	32	29	29	26	29	26	31	28	27	25	32	29	28	26	–	–	ns
C_n	29	25	–	–	26	24	25	23	20	18	29	26	23	21	–	–	ns
$I_{0,1,2}$	35	32	30	27	35	32	34	31	29	26	35	32	30	27	–	–	ns
$I_{3,4,5}$	35	32	28	26	34	31	34	31	27	25	35	32	28	26	–	–	ns
$I_{6,7,8,9}$	25	23	–	–	–	–	–	–	–	–	–	–	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock –	34	31	31	28	33	30	34	31	30	27	34	31	34	31	25	23	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP:

INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Source Address	11	10	0 (3)	0 (3)	24 (4)	21 (4)	2	1	ns
B Destination Address	11	10	Do not change (2)				2	1	ns
D	– (1)	–	–	–	12/22 (5)	10/20 (5)	2	1	ns
C_n	–	–	–	–	17	15	0	0	ns
$I_{0,1,2}$	–	–	–	–	28	25	0	0	ns
$I_{3,4,5}$	–	–	–	–	28	25	0	0	ns
$I_{6,7,8,9}$	11	10	Do not change (2)				0	0	ns
$RAM_{0,15}$, $Q_{0,15}$	–	–	–	–	12	11	0	0	ns

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).

IDT49C401
AC ELECTRICAL CHARACTERISTICS
(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C401 over the -55°C to +125°C and 0°C to +70°C temperature ranges. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNIT
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	50	48	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)	20	21	MHz
Minimum Clock LOW Time	30	30	ns
Minimum Clock HIGH Time	20	20	ns
Minimum Clock Period	50	48	ns

COMBINATIONAL PROPAGATION DELAYS (1) C_L = 50pF

FROM INPUT	TO OUTPUT																UNIT
	Y		(MSS = L) $\overline{G}, \overline{P}$		(MSS = H) F_{15}		(MSS = H) OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	52	47	47	42	52	47	47	42	38	34	52	47	44	40	–	–	ns
D	35	32	34	31	35	32	34	31	27	25	35	32	28	26	–	–	ns
C_n	29	26	–	–	29	26	27	25	20	18	29	26	23	21	–	–	ns
$I_{0,1,2}$	41	37	30	27	41	37	38	35	29	26	41	37	30	27	–	–	ns
$I_{3,4,5}$	40	36	28	26	40	36	37	34	27	25	40	36	28	26	–	–	ns
$I_{6,7,8,9}$	26	24	–	–	–	–	–	–	–	–	–	–	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock —	42	38	41	37	42	38	41	37	30	27	42	38	41	37	25	23	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Source Address	20	18	0 (3)	0 (3)	50 (4)	48 (4)	2	1	ns
B Destination Address	20	18	Do not change (2)				2	1	ns
D	– (1)	–	–	–	30/40 (5)	26/36 (5)	2	1	ns
C_n	–	–	–	–	35	32	0	0	ns
$I_{0,1,2}$	–	–	–	–	45	41	0	0	ns
$I_{3,4,5}$	–	–	–	–	45	41	0	0	ns
$I_{6,7,8,9}$	12	11	Do not change (2)				0	0	ns
$RAM_{0,15}, Q_{0,15}$	–	–	–	–	12	11	0	0	ns

NOTES:
1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).

IDT49C401A
OUTPUT ENABLE/DISABLE TIMES
(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
$\overline{OE}$	Y	25	23	25	23

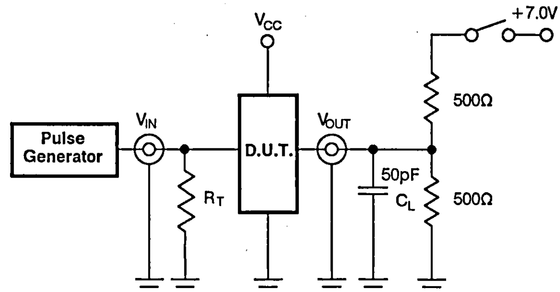
IDT49C401
OUTPUT ENABLE/DISABLE TIMES
(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
$\overline{OE}$	Y	22	20	20	18

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

TEST LOAD CIRCUIT



INPUT/OUTPUT INTERFACE CIRCUIT

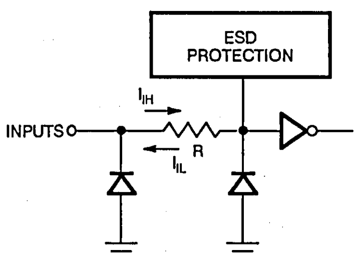


Figure 2. Input Structure (All Inputs)

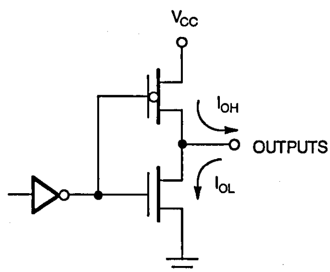


Figure 3. Output Structure (All Outputs Except F = 0)

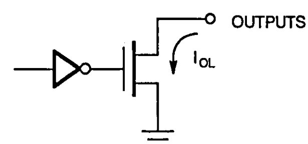


Figure 4. Output Structure (F = 0)

ORDERING INFORMATION

IDT 49C401 (Device Type) XXX (Speed) XX (Package) X (Process/Temperature Range)

Process/Temperature Range:
- Blank — Commercial (0°C to +70°C)
- B — Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:
- C — Sidebraze DIP

Speed:
- Blank — 16-Bit µP Slice
- A — High-Speed 16-Bit µP Slice

16-BIT CMOS MICROPROCESSOR SLICE

IDT49C402
IDT49C402A

Integrated Device Technology, Inc.

MICROSLICE™ PRODUCT

FEATURES:

- Functionally equivalent to four 2901s and one 2902
- IDT49C402A 45% faster than four 2901s and one 2902A
- Expanded two-address architecture with independent, simultaneous access to two 64 x 16 register files
- Expanded destination functions with 8 new operations allowing Direct Data to be loaded directly into the dual-port RAM and Q Register
- Clamp diodes on all inputs provide noise suppression
- Fully cascadable
- 68-pin PGA, Shrink-DIP (600 mil, 70 mil centers) and LCC (25 and 50 mil centers)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C402s are high-speed, fully cascadable 16-bit CMOS microprocessor slice units which combine the standard functions of four 2901s and a 2902 with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

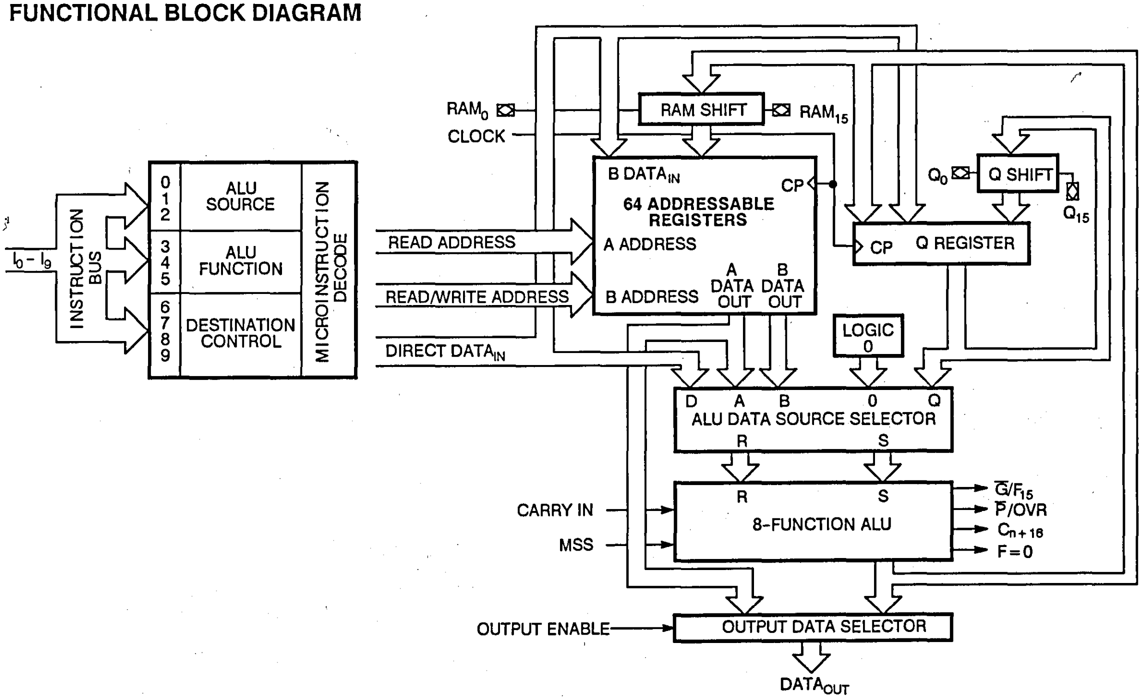
The IDT49C402s include all of the normal functions associated with standard 2901 bit-slice operation: (a) a 3-bit instruction field (I_0, I_1, I_2) which controls the source operand selection for the ALU; (b) a 3-bit microinstruction field (I_3, I_4, I_5) used to control the eight possible functions of the ALU; (c) eight destination control functions which are selected by the microcode inputs (I_6, I_7, I_8); and (d) a tenth microinstruction input, I_9, offering eight additional destination control functions. This I_9 input, in conjunction with I_6, I_7 and I_8, allows for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU and new combinations of destination functions with the RAM A port output available at the Y output pins of the device.

Also featured is an on-chip dual-port RAM that contains 64 words by 16 bits—four times the number of working registers in a 2901.

The IDT49C402s are fabricated using CEMOS, a CMOS technology designed for high performance and high reliability. These performance enhanced devices feature both bipolar speed and bipolar output drive capabilities while maintaining exceptional microinstruction speeds at greatly reduced CMOS power levels.

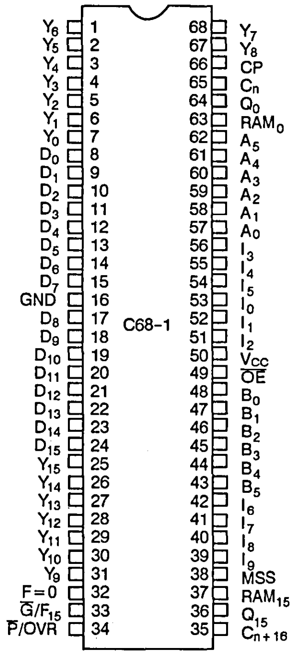
8

FUNCTIONAL BLOCK DIAGRAM

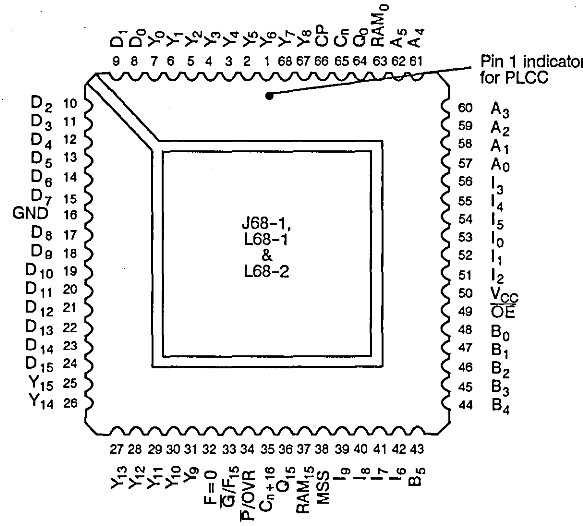


CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.

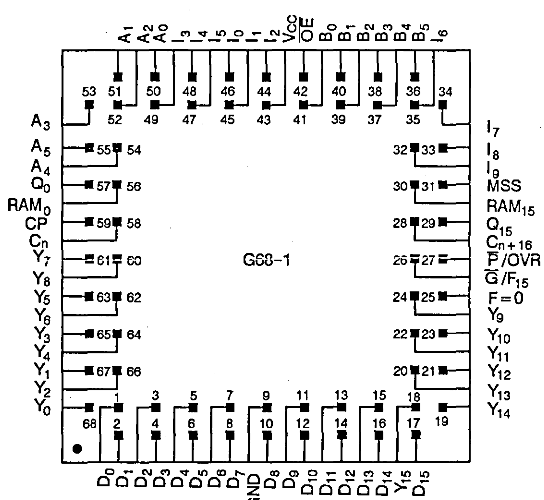
PIN CONFIGURATIONS



DIP TOP VIEW



LCC/PLCC TOP VIEW



PGA TOP VIEW

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_0–A_5	I	Six address inputs to the register file which selects one register and displays its contents through the A port.
B_0–B_5	I	Six address inputs to the register file which selects one of the registers in the file, the contents of which is displayed through the B port. It also selects the location into which new data can be written when the clock goes LOW.
I_0–I_9	I	Ten instruction control lines which determine what data source will be applied to the ALU $I_{(0, 1, 2)}$, what function the ALU will perform $I_{(3, 4, 5)}$ and what data is to be deposited in the Q Register or the register file $I_{(6, 7, 8, 9)}$. Original 2901 destinations are selected if I_9 is disconnected. In this mode, proper I_9 bias is controlled by an internal pullup resistor to V_{CC}.
D_0–D_{15}	I	Sixteen-bit direct data inputs which are the data source for entering external data into the device ALU, Q Register or RAM. D_0 is the LSB.
Y_0–Y_{15}	O	Sixteen three-state output lines which, when enabled, display either the sixteen outputs of the ALU or the data on the A port of the register stack. This is determined by the destination code $I_{(6, 7, 8, 9)}$.
$\overline{G}/F_{15}$	O	A multipurpose pin which indicates the carry generate ($\overline{G}$) function at the least significant and intermediate slices or as F_{15} the most significant ALU output (sign bit). $\overline{G}/F_{15}$ selection is controlled by the MSS pin. If MSS = HIGH, F_{15} is enabled. If MSS = LOW, $\overline{G}$ is enabled.
F = 0	O	Open drain output which goes HIGH if the F_0–F_{15} ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C_n	I	Carry-in to the internal ALU.
C_{n+16}	O	Carry-out of the internal ALU.
Q_{15} RAM_{15}	I/O	Bidirectional lines controlled by $I_{(6, 7, 8, 9)}$. Both are three-state output drivers connected to the TTL-compatible inputs. When the destination code on $I_{(6, 7, 8, 9)}$ indicates an up shift, the three-state outputs are enabled, the MSB of the Q Register is available on the Q_{15} pin and the MSB of the ALU output is available on the RAM_{15} pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q_0 RAM_0	I/O	Both bidirectional lines function identically to Q_{15} and RAM_{15} lines except they are the LSB of the Q Register and RAM.
$\overline{OE}$	I	Output enable. When pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
$\overline{P}$/OVR	O	A multipurpose pin which indicates the carry propagate ($\overline{P}$) output for performing a carry lookahead operation or overflow (OVR) the Exclusive-OR of the carry-in and carry-out of the ALU MSB. OVR, at the most significant end of the word, indicates that the result of an arithmetic two's complement operation has overflowed into the sign bit. $\overline{P}$/OVR selection is controlled by the MSS pin. If MSS = HIGH, OVR is enabled. If MSS = LOW, $\overline{P}$ is enabled.
CP	I	The clock input. LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 64 x 16 RAM which compromises the master latches of the register file. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.
MSS	I	When HIGH, enables OVR and F_{15} on the $\overline{P}$/OVR and $\overline{G}/F_{15}$ pins. When LOW, enables $\overline{G}$ and $\overline{P}$ on these pins. If left open, internal pullup resistor to V_{CC} provides declaration that the device is the most significant slice.

DEVICE ARCHITECTURE:

The IDT49C402 CMOS bit-slice microprocessor is configured sixteen bits wide and is cascadable to any number of bits (16, 32, 48, 64). Key elements which make up this 16-bit microprocessor slice are the (1) register file (64 x 16 dual-port RAM) with shifter, (2) ALU and (3) Q Register and shifter.

REGISTER FILE—A 16-bit data word from one of the 64 RAM registers can be read from the A port as selected by the 6-bit A address field. Simultaneously, the same data word, or any other word from the 64 RAM registers, can be read from the B port as selected by the 6-bit B address field. New data is written into the RAM register location selected by the B address field during the clock (CP) LOW time. Two sixteen-bit latches hold the RAM A port and B port during the clock (CP) LOW time, eliminating any data races. During clock HIGH these latches are transparent, reading the data selected by the A and B addresses. The RAM data input field is driven from a four-input multiplexer that selects the ALU output or the D inputs. The ALU output can be shifted up one position, down one position or not shifted. Shifting data operations involve the RAM_{15} and RAM_0 I/O pins. For a shift up operation, the RAM shifter MSB is connected to an enabled RAM_{15} I/O output while the RAM_0 I/O input is selected as the input to the LSB. During a shift down operation, the RAM shifter LSB is connected to an enabled RAM_0 I/O output while the RAM_{15} I/O input is selected as the input to the MSB.

ALU—The ALU can perform three binary arithmetic and five logic operations on the two 16-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer with both having a zero source operand. Both multiplexers are controlled by the $I_{(0, 1, 2)}$ inputs. This multiplexer configuration enables the user to select various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. Microinstruction inputs $I_{(3, 4, 5)}$ are used to select the ALU function. This high-speed ALU cascades to any word length, providing carry-in (C_n), carry-out (C_{n+16}) and an open-drain (F = 0) output. When all bits of the ALU are zero, the pull-down device of F = 0 is off, allowing a wire-OR of this pin over all cascaded devices. Multipurpose pins $\overline{G}/F_{15}$ and $\overline{P}$/OVR are aimed at accelerating arithmetic operations. For intermediate and least significant slices, the MSS pin is programmed LOW, selecting the carry-generate ($\overline{G}$) and carry-propagate ($\overline{P}$) output functions to be used by carry lookahead logic. For the most significant slice, MSS is programmed high, selecting the sign-bit (F_{15}) and the two's complement overflow (OVR) output functions. The sign bit (F_{15}) allows the ALU sign bit to be monitored without enabling the three-state ALU outputs. The overflow (OVR) output is high when the two's complement arithmetic operation has overflowed into the sign bit as logically determined from the Exclusive-OR of the carry-in and carry-out of the most significant bit of the ALU. The ALU data outputs are available at the three-state outputs $Y_{(0-15)}$ or as inputs to the RAM register file and Q Register under control of the $I_{(6,7,8,9)}$ instruction inputs.

Q REGISTER—The Q Register is a separate 16-bit file intended for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. It is driven from a 4-input multiplexer. In the no-shift mode, the multiplexer enters the ALU F output or Direct Data into the Q Register. In either the shift up or shift down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q_0 and Q_{15}, which operate comparably to the RAM shifter. They are controlled by the $I_{(6,7,8,9)}$ inputs.

The clock input of the IDT49C402 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW-to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and $I_{(6,7,8,9)}$ define the RAM as the destination, new data will be written into the RAM file defined by the B address field.

ALU SOURCE OPERAND CONTROL

MNEMONIC	MICROCODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	OCTAL CODE	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

ALU FUNCTION CONTROL

MNEMONIC	MICROCODE				ALU FUNCTION	SYMBOL
	I_5	I_4	I_3	OCTAL CODE		
ADD	L	L	L	0	R Plus S	$R + S$
SUBR	L	L	H	1	S Minus R	$S - R$
SUBS	L	H	L	2	R Minus S	$R - S$
OR	L	H	H	3	R OR S	$R \vee S$
AND	H	L	L	4	R AND S	$R \wedge S$
NOTRS	H	L	H	5	$\bar{R}$ AND S	$\bar{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \nabla S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \nabla S}$

ALU ARITHMETIC MODE FUNCTIONS

OCTAL $I_{5,4,3}$	OCTAL $I_{2,1,0}$	$C_n = L$ GROUP	$C_n = L$ FUNCTION	$C_n = H$ GROUP	$C_n = H$ FUNCTION
0	0	ADD	A + Q	ADD plus one	A + Q + 1
0	1		A + B		A + B + 1
0	5		D + A		D + A + 1
0	6		D + Q		D + Q + 1
0	2	PASS	Q	Increment	Q + 1
0	3		B		B + 1
0	4		A		A + 1
0	7		D		D + 1
1	2	Decrement	Q - 1	PASS	Q
1	3		B - 1		B
1	4		A - 1		A
2	7		D - 1		D
2	2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2	3		-B - 1		-B
2	4		-A - 1		-A
1	7		-D - 1		-D
1	0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1	1		B - A - 1		B - A
1	5		A - D - 1		A - D
1	6		Q - D - 1		Q - D
2	0		A - Q - 1		A - Q
2	1		A - B - 1		A - B
2	5		D - A - 1		D - A
2	6		D - Q - 1		D - Q

ALU LOGIC MODE FUNCTIONS

OCTAL $I_{5,4,3}$	OCTAL $I_{2,1,0}$	GROUP	FUNCTION
4	0	AND	$A \wedge Q$
4	1		$A \wedge B$
4	5		$D \wedge A$
4	6		$D \wedge Q$
3	0	OR	$A \vee Q$
3	1		$A \vee B$
3	5		$D \vee A$
3	6		$D \vee Q$
6	0	EX-OR	$A \nabla Q$
6	1		$A \nabla B$
6	5		$D \nabla A$
6	6		$D \nabla Q$
7	0	EX-NOR	$\overline{A \nabla Q}$
7	1		$\overline{A \nabla B}$
7	5		$\overline{D \nabla A}$
7	6		$\overline{D \nabla Q}$
7	2	INVERT	$\bar{Q}$
7	3		$\bar{B}$
7	4		$\bar{A}$
7	7		$\bar{D}$
6	2	PASS	Q
6	3		B
6	4		A
6	7		D
3	2	PASS	Q
3	3		B
3	4		A
3	7		D
4	2	"ZERO"	0
4	3		0
4	4		0
4	7		0
5	0	MASK	$\bar{A} \wedge Q$
5	1		$\bar{A} \wedge B$
5	5		$\bar{D} \wedge A$
5	6		$\bar{D} \wedge Q$

SOURCE OPERAND AND ALU FUNCTION MATRIX (1)

OCTAL $I_{5,4,3}$	ALU FUNCTION	$I_{2,1,0}$ OCTAL 0	1	2	3	4	5	6	7
		ALU SOURCE							
		A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S	A + Q	A + B	Q	B	A	D + A	D + Q	D
	C_n = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	C_n = L S Minus R	Q - A - 1	B - A - 1	Q - 1	B - 1	A - 1	A - D - 1	Q - D - 1	-D - 1
	C_n = H	Q - A	B - A	Q	B	A	A - D	Q - D	-D
2	C_n = L R Minus S	A - Q - 1	A - B - 1	-Q - 1	-B - 1	-A - 1	D - A - 1	D - Q - 1	D - 1
	C_n = H	A - Q	A - B	-Q	-B	-A	D - A	D - Q	D
3	R OR S	$A \vee Q$	$A \vee B$	Q	B	A	$D \vee A$	$D \vee Q$	D
4	R AND S	$A \wedge Q$	$A \wedge B$	0	0	0	$D \wedge A$	$D \wedge Q$	0
5	$\bar{R}$ AND S	$\bar{A} \wedge Q$	$\bar{A} \wedge B$	Q	B	A	$\bar{D} \wedge A$	$\bar{D} \wedge Q$	0
6	R EX-OR S	$A \veebar Q$	$A \veebar B$	Q	B	A	$D \veebar A$	$D \veebar Q$	D
7	R EX-NOR S	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\bar{Q}$	$\bar{B}$	$\bar{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\bar{D}$

NOTE:
1. + = Plus; - = Minus; $\wedge$ = AND; $\veebar$ = EX-OR; V = OR

ALU DESTINATION CONTROL(1)

MNEMONIC	MICROCODE I_9	I_8	I_7	I_6	HEX CODE	RAM FUNCTION SHIFT	RAM FUNCTION LOAD	Q REGISTER FUNCTION SHIFT	Q REGISTER FUNCTION LOAD	Y OUTPUT	RAM SHIFTER RAM_0	RAM SHIFTER RAM_{15}	Q SHIFTER Q_0	Q SHIFTER Q_{15}	
OREG	H	L	L	L	8	X	NONE	NONE	F→Q	F	X	X	X	X	Existing 2901 Functions
NOP	H	L	L	H	9	X	NONE	X	NONE	F	X	X	X	X	
RAMA	H	L	H	L	A	NONE	F→B	X	NONE	A	X	X	X	X	
RAMF	H	L	H	H	B	NONE	F→B	X	NONE	F	X	X	X	X	
RAMQD	H	H	L	L	C	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_{15}	Q_0	IN_{15}	
RAMD	H	H	L	H	D	DOWN	F/2→B	X	NONE	F	F_0	IN_{15}	Q_0	X	
RAMQU	H	H	H	L	E	UP	2F→B	UP	2Q→Q	F	IN_0	F_{15}	IN_0	Q_{15}	
RAMU	H	H	H	H	F	UP	2F→B	X	NONE	F	IN_0	F_{15}	X	Q_{15}	
DFF	L	L	L	L	0	NONE	D→B	NONE	F→Q	F	X	X	X	X	New Added IDT49C402 Functions
DFA	L	L	L	H	1	NONE	D→B	NONE	F→Q	A	X	X	X	X	
FDF	L	L	H	L	2	NONE	F→B	NONE	D→Q	F	X	X	X	X	
FDA	L	L	H	H	3	NONE	F→B	NONE	D→Q	A	X	X	X	X	
XQDF	L	H	L	L	4	X	NONE	DOWN	Q/2→Q	F	X	X	Q_0	IN_{15}	
DXF	L	H	L	H	5	NONE	D→B	X	NONE	F	X	X	Q_0	X	
XQUF	L	H	H	L	6	X	NONE	UP	2Q→Q	F	X	X	IN_0	Q_{15}	
XDF	L	H	H	H	7	X	NONE	NONE	D→Q	F	X	X	X	Q_{15}	

NOTE:
1. X = Don't Care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
UP is toward MSB; DOWN is toward LSB.

8

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level (4)		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level (4)		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10	µA
			V_O = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V (3)		-15	-30	–	mA

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ±10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IH}$, $V_{IL} \leq V_{LC}$ f_{CP} = 0, CP = H	MIL.	–	150	245	mA
			COM'L.	–	150	215	
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IH}$, $V_{IL} \leq V_{LC}$ f_{CP} = 0, CP = L	MIL.	–	80	125	mA
			COM'L.	–	80	110	
I_{CCT}	Quiescent Input Power Supply(5) Current (per Input @ TTL High)	V_{CC} = Max. V_{IH} = 3.4V, f_{CP} = 0	MIL.	–	0.3	0.6	mA/ Input
			COM'L.	–	0.3	0.5	
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IH}$, $V_{IL} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	2.0	3.0	mA/ MHz
			COM'L.	–	2.0	2.5	
I_{CC}	Total Power Supply Current (6)	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \leq V_{IH}$, $V_{IL} \leq V_{LC}$	MIL.	–	135	210	mA
			COM'L.	–	135	190	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	145	225	
			COM'L.	–	145	200	

NOTES:
5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock Input frequency

8

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \leq$ 0V and $V_{IH} \geq$ 3V for AC tests.

IDT49C402A AC ELECTRICAL CHARACTERISTICS (Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402A over the -55°C to +125°C and 0°C to +70°C temperature ranges. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNIT
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	28	24	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)	35	41	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period	36	31	ns

COMBINATIONAL PROPAGATION DELAYS[1] C_L = 50pF

FROM INPUT	TO OUTPUT																UNIT
	Y		(MSS = L) $\overline{G}, \overline{P}$		(MSS = H) F_{15}		(MSS = H) OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	41	37	39	35	41	37	41	37	37	34	41	37	40	36	–	–	ns
D	32	29	29	26	29	26	31	28	27	25	32	29	28	26	–	–	ns
C_n	28	25	–	–	26	24	25	23	20	18	29	26	23	21	–	–	ns
$I_{0,1,2}$	35	32	30	27	35	32	34	31	29	26	35	32	30	27	–	–	ns
$I_{3,4,5}$	35	32	28	26	34	31	34	31	27	25	35	32	28	26	–	–	ns
$I_{6,7,8,9}$	25	23	–	–	–	–	–	–	–	–	–	–	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ↑	34	31	31	28	33	30	34	31	30	27	34	31	34	31	25	23	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP:

INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Source Address	11	10	0[3]	0[3]	21, 10 + TPWL[4]		2	1	ns
B Destination Address	11	10	Do not change [2]				2	1	ns
D	–[1]	–	–	–	12/22[5]	10/20[5]	2	1	ns
C_n	–	–	–	–	17	15	0	0	ns
$I_{0,1,2}$	–	–	–	–	28	25	0	0	ns
$I_{3,4,5}$	–	–	–	–	28	25	0	0	ns
$I_{6,7,8,9}$	11	10	Do not change [2]				0	0	ns
$RAM_{0,15}, Q_{0,15}$	–	–	–	–	12	11	0	0	ns

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→ H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→ H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).

IDT49C402
AC ELECTRICAL CHARACTERISTICS
(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402 over the -55°C to +125°C and 0°C to +70°C temperature ranges. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNIT
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	50	48	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)	20	21	MHz
Minimum Clock LOW Time	30	30	ns
Minimum Clock HIGH Time	20	20	ns
Minimum Clock Period	50	48	ns

COMBINATIONAL PROPAGATION DELAYS (1) C_L = 50pF

FROM INPUT	TO OUTPUT																UNIT
	Y		(MSS = L) $\overline{G}, \overline{P}$		(MSS = H) F_{15}		(MSS = H) OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	52	47	47	42	52	47	47	42	38	34	52	47	44	40	–	–	ns
D	35	32	34	31	35	32	34	31	27	25	35	32	28	26	–	–	ns
C_n	29	26	–	–	29	26	27	25	20	18	29	26	23	21	–	–	ns
$I_{0,1,2}$	41	37	30	27	41	37	38	35	29	26	41	37	30	27	–	–	ns
$I_{3,4,5}$	40	36	28	26	40	36	37	34	27	25	40	36	28	26	–	–	ns
$I_{6,7,8,9}$	26	24	–	–	–	–	–	–	–	–	–	–	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ⟋	42	38	41	37	42	38	41	37	30	27	42	38	41	37	25	23	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP:

INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Source Address	20	18	0(3)	0(3)	50, 20 + TPWL(4)		2	1	ns
B Destination Address	20	18	Do not change (2)				2	1	ns
D	– (1)	–	–	–	30/40 (5)	26/36 (5)	2	1	ns
C_n	–	–	–	–	35	32	0	0	ns
$I_{0,1,2}$	–	–	–	–	45	41	0	0	ns
$I_{3,4,5}$	–	–	–	–	45	41	0	0	ns
$I_{6,7,8,9}$	12	11	Do not change (2)				0	0	ns
$RAM_{0,15}, Q_{0,15}$	–	–	–	–	12	11	0	0	ns

NOTES:
1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→ H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→ H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).

IDT49C402A
OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
$\overline{OE}$	Y	22	20	20	18

IDT49C402
OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
$\overline{OE}$	Y	25	23	25	23

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

TEST LOAD CIRCUIT

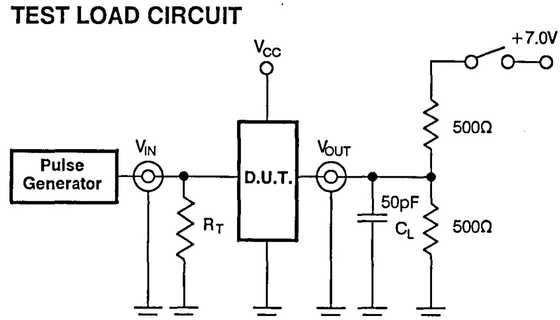


Figure 1. Switching Test Circuit (All Outputs)

INPUT/OUTPUT INTERFACE CIRCUIT

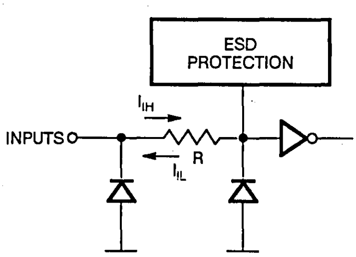


Figure 2. Input Structure (All Inputs)

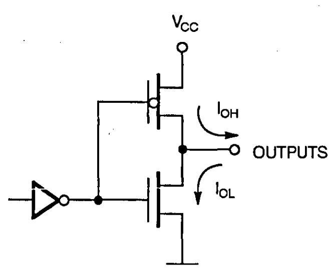


Figure 3. Output Structure (All Outputs Except F = 0)

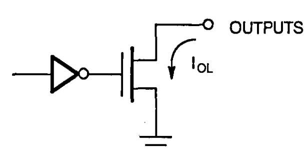


Figure 4. Output Structure (F = 0)

CRITICAL SPEED PATH ANALYSIS

Critical speed paths are for the IDT49C402A versus the equivalent bipolar circuit implementation using four 2901Cs and one 2902A is shown below.

The IDT49C402A operates faster than the theoretically achievable values of the discrete bipolar implementation. Actual speed values for the discrete bipolar circuit will increase due to on-chip/off-chip circuit board delays.

TIMING COMPARISON: IDT49C402A vs 2901C w/2902A

16-BIT µP SYSTEM	DATA PATH (COM'L.)		DATA PATH (MIL.)		UNIT
	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	
Four 2901Cs + 2902A	≥71	≥71	≥83.5	≥83.5	ns
IDT49C402A	37	36	41	40	ns
Speed Savings	34	35	42.5	43.5	ns

TIMING COMPARISON: IDT49C402 vs 2901C w/2902A

16-BIT µP SYSTEM	DATA PATH (COM'L.)		DATA PATH (MIL.)		UNIT
	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	
Four 2901Cs + 2902A	≥71	≥71	≥83.5	≥83.5	ns
IDT49C402	47	40	52	44	ns
Speed Savings	24	31	31.5	39.5	ns

ORDERING INFORMATION

IDT XXXXXX (Device Type) X (Speed) X (Package) X (Process/Temperature)

Process/Temperature:
- BLANK — Commercial (0°C to +70°C)
- B — Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:
- XC — SHRINK-DIP Sidebraze
- J — PLCC
- L — Leadless Chip Carrier (50 mil centers)
- XL — Leadless Chip Carrier (25 mil centers)
- G — Pin Grid Array
- PG — Plastic Pin Grid Array

Speed:
- BLANK — Standard Speed
- A — High-Speed

Device Type:
- 49C402 — 16-Bit Microprocessor Slice

Integrated Device Technology, Inc.

16-BIT CMOS MICROPROCESSOR SLICE

PRELIMINARY
IDT49C403
IDT49C403A

FEATURES:

- Monolithic 16-bit CMOS µP Slice
- Replaces four 2903As/29203s and a 2902A
- Fast
  - 50% faster than four 2903As/29203s and a 2902
- Low power CMOS
  - Commercial: 250mA (max.)
  - Military: 275mA (max.)
- Performs binary and BCD Arithmetic
- Expanded two-address architecture with independent, simultaneous access to two, expandable 64 x 16 register files
- Word/Byte Control
- Expanded 4 x 16 Q Register
- Performs Byte Swap and Word/Byte Operation
- Fully cascadable without the need for additional carry lookahead
- Incorporates three 16-bit Bidirectional Busses
- Includes Serial Protocol Channel (SPC™)
  - Flexible on-chip diagnostics
  - Serially monitors all pin states
  - Reads and Writes to Register File
- High Output Drive
  - Commercial: 16mA (max.)
  - Military: 12mA (max.)
- Available in 108-pin PGA
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C403 is a high-speed, fully cascadable 16-bit CMOS microprocessor slice. It combines the standard function of four 2903s/29203s and one 2902 with additional control features aimed at enhancing the performance of all bit-slice microprocessor designs.

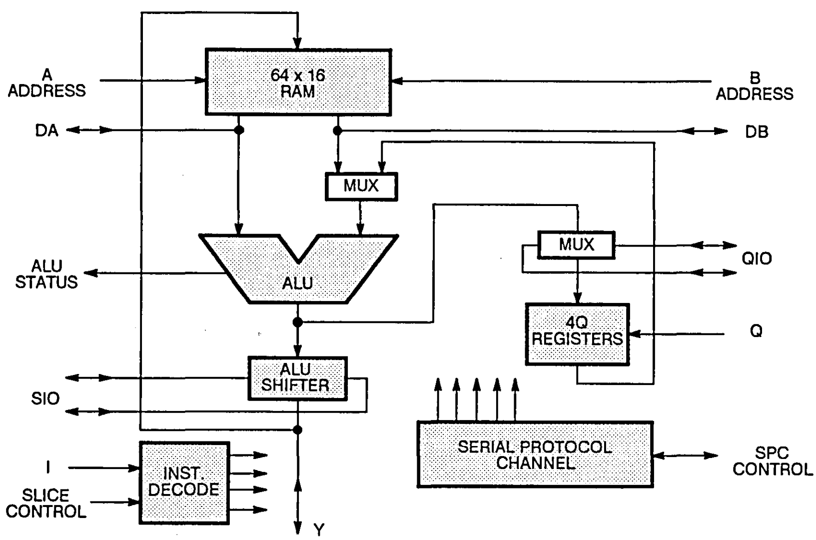
Included in this extremely low power, yet fast IDT49C403 device are 3 bidirectional data buses, 64 word x 16-bit two-port expandable RAM, 4 word x 16-bit Q Register, parity generation, sign extension, multiplication/division and normalization logic. Additionally, the IDT49C403 offers the special feature of enhanced byte support through both word/byte control and byte swap control.

The IDT49C403 easily supports fast 100ns microcycles and will enhance the speed of all existing quad 2903A/29203 systems by 50%. Being specified at an extremely low 225mA, the IDT device offers an immediate system power savings and improved reliability.

Also featured on the IDT49C403 is an innovative diagnostics capability known as Serial Protocol Channel (SPC). This on-chip feature greatly simplifies the task of writing and debugging microcode, field maintenance debug and test, along with system testing during manufacturing.

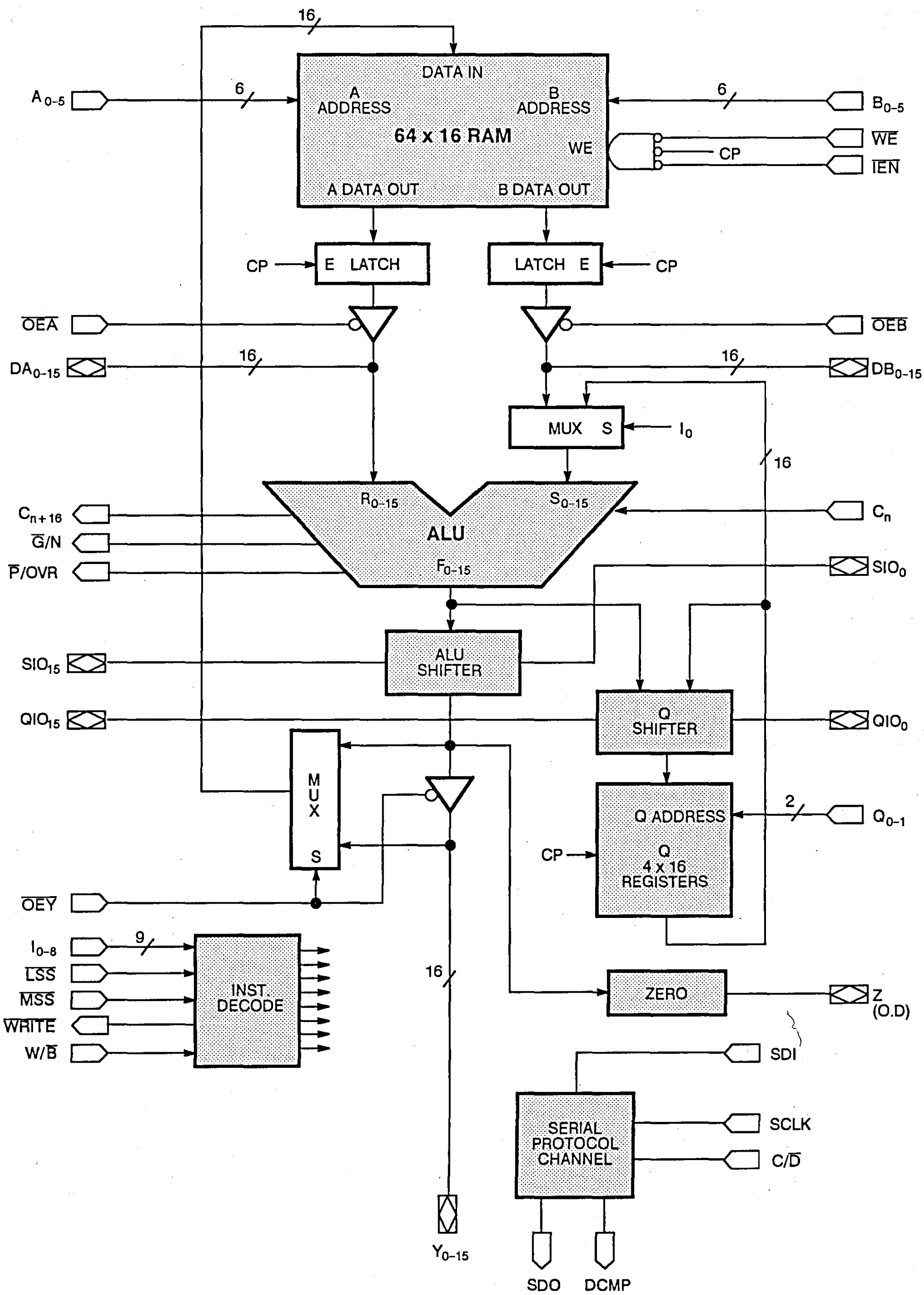
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



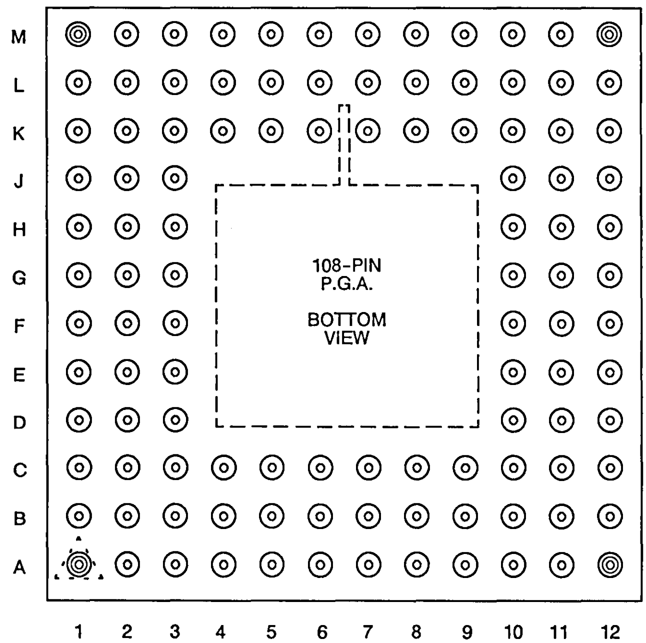
CEMOS, SPC and MICROSLICE are trademarks of Integrated Device Technology, Inc.

DETAILED BLOCK DIAGRAM



8

PIN CONFIGURATION



PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
A1	N/C	B4	DB7	C7	DCMP	E10	$W/\overline{B}$	H1	DA2	K4	DA8	L7	$\overline{WE}$	M10	Q_0
A2	V_{CC}	B5	DB4	C8	I_5	E11	$\overline{OEY}$	H2	DA3	K5	DA12	L8	B_2	M11	V_{CC}
A3	$\overline{OEB}$	B6	DB1	C9	$\overline{IEN}$	E12	SIO_0	H3	DA5	K6	N/C	L9	B_5	M12	N/C
A4	DB5	B7	$\overline{MSS}$	C10	Y_2	F1	GND	H10	Y_{13}	K7	B_0	L10	Q_1		
A5	DB3	B8	I_7	C11	Y_5	F2	DB15	H11	Y_{11}	K8	B_4	L11	SCLK		
A6	DB0	B9	C_{n+16}	C12	Y_6	F3	DB14	H12	Y_{10}	K9	$\overline{WRITE}$	L12	$C/\overline{D}$		
A7	GND	B10	$\overline{P}$/OVR	D1	DB11	F10	QIO_0	J1	DA4	K10	GND	M1	V_{CC}		
A8	I_8	B11	Y_1	D2	DB9	F11	SIO_{15}	J2	DA6	K11	SDO	M2	A_5		
A9	I_6	B12	Y_3	D3	I_3	F12	QIO_{15}	J3	A_1	K12	Y_{15}	M3	DA10		
A10	$\overline{G}$/N	C1	DB8	D10	Y_4	G1	$\overline{OEA}$	J10	SDI	L1	A_2	M4	DA13		
A11	Y_0	C2	I_4	D11	Y_7	G2	DA0	J11	Y_{14}	L2	A_4	M5	DA15		
A12	V_{CC}	C3	GND	D12	Z	G3	DA1	J12	Y_{12}	L3	DA9	M6	GND		
B1	I_2	C4	I_0	E1	DB13	G10	Y_9	K1	DA7	L4	DA11	M7	CP		
B2	I_1	C5	DB6	E2	DB12	G11	Y_8	K2	A_0	L5	DA14	M8	B_1		
B3	C_n	C6	DB2	E3	DB10	G12	GND	K3	A_3	L6	$\overline{LSS}$	M9	B_3		

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A_{0-5}	I	Six address inputs to the RAM containing the address of the RAM word appearing at output port A.
B_{0-5}	I	Six address inputs to the RAM which selects one of the words in the RAM, the contents of which is displayed through the B port. It also selects the location into which new data can be written when the $\overline{WE}$ input and CP input are low.
DA_{0-15}	I/O	Sixteen bi-directional data pins acting as operands R for entering external data into the ALU. DA_0 is the LSB. The DA lines also function as an external output for RAM port A.
DB_{0-15}	I/O	Sixteen bi-directional data pins for entering external data into the ALU. The DB lines act as either RAM port B output data, or as input operands S to the ALU.
$\overline{WE}$	I	The RAM write enable input, which when LOW causes the Y I/O port data to be written into the RAM when the CP input is low. When $\overline{WE}$ is HIGH writing data into the RAM is inhibited.
$\overline{OEA}$	I	Output enable, which, when HIGH selects DA_{0-15} as the ALU R operand, and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-15} output data.
$\overline{OEB}$	I	Output enable, which, when HIGH selects DB_{0-15} as the ALU S operand, and, when LOW, selects RAM output B as the ALU S operand and the DB_{0-15} output data.
SIO_0 SIO_{15}	I/O	Bidirectional serial shift inputs/outputs for the ALU shifter. SIO_0 is an input and SIO_{15} is an output during a shift-up operation. SIO_{15} is an input and SIO_0 is an output during a shift-down operation. Refer to Tables 4 (a, b, c, d) and 5 for an exact definition of these pins.
QIO_0 QIO_{15}	I/O	Bidirectional serial shift inputs/outputs for the Q registers shifter. They operate like SIO_0 and SIO_{15} pins. Refer to Tables 4 (a, b, c, d) and 5 for an exact definition of these pins.
C_n	I	Carry-in input to the ALU.
$\overline{IEN}$	I	Instruction enable input. When LOW, it enables writing into the Q register and the Sign Compare flip-flop. When HIGH, the Q register and the Sign Compare flip-flop are in hold mode. $\overline{IEN}$ does not affect $\overline{WRITE}$, but internally disables the RAM write enable.
$\overline{LSS}$	I	Input pin, when held LOW, causes the chip to act as either stand alone slice (SA) or the least significant slice (LSS). When $\overline{LSS}$ is held HIGH, the chip acts as either an intermediate slice or most significant slice.
$\overline{MSS}$	I	Input pin, when held LOW, programs the chip to act as either stand alone slice (SA) or the most significant slice (MSS), and holding it HIGH programs the chip to act either as an intermediate slice (IS) or the least significant slice (LSS).
$\overline{WRITE}$	O	The $\overline{WRITE}$ signal is LOW when an instruction which causes data to be written into the RAM is being executed. This pin is normally connected to the $\overline{WE}$ pin.
C_{n+16}	O	This output indicates the carry out of the ALU. Refer to Tables 6a and 6b for an exact definition of this pin.
Z	I/O	An open drain bidirectional pin. When HIGH it indicates that all outputs are LOW. Z is used as an input pin for some special functions. Refer to Tables 6a and 6b for an exact definition of this pin.
$\overline{G}$/N	O	$\overline{G}$ indicates the carry generate function at the least significant and intermediate slices, and indicates the sign, N, of the ALU result at the most significant slice. Refer to Tables 6a and 6b for an exact definition of this pin.
$\overline{OEY}$	I	A control input pin. When LOW the ALU shifter output data is enabled onto the Y_{0-15} lines. When HIGH the Y_{0-15} three-state output buffers are disabled.
CP	I	Clock input. The Sign Compare flip-flop and the Q register are clocked on the LOW-to-HIGH transition of the CP signal. When $\overline{WE}$ and CP are LOW, data is written into the RAM.
$\overline{P}$/OVR	O	$\overline{P}$ indicates the carry propagate function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Tables 6a and 6b for an exact definition of this pin.
Y_{0-15}	I/O	Sixteen bi-directional data pins. Controlled by $\overline{OEY}$ input, the ALU shifter output data can be enabled onto these lines, or external data is written directly into the RAM using these lines as data inputs.
I_{0-8}	I	The nine instruction inputs used to select the IDT49C403 operation to be performed.
Q_{0-1}	I	Two address pins to select one of the four Q registers.
W/$\overline{B}$	I	Word/$\overline{Byte}$ control pin. Used only in the standard function mode, it selects Word mode when held HIGH and Byte mode when held LOW. Must be tied HIGH when the special functions are being used.
SDI	I	Serial Data Input pin, used for receiving diagnostic data and commands from a host system or from the SDO pin of a cascaded processor.
SDO	O	Serial Data Output pin, used for transmitting diagnostic data and commands to a host system or a cascaded processor via its SDI pin.
C/$\overline{D}$	I	Input pin, when LOW defines the bit pattern being received at the SDI pin as Data, and when HIGH defines the incoming pattern as a Command for executing diagnostic functions. This pin should be tied HIGH when the diagnostics feature is not being used.
SCLK	I	Input pin used for clocking in diagnostic data and command information at the SDI pin. This pin should be tied LOW when the diagnostics function is not being used.
DCMP	O	Output pin, which, when HIGH indicates that the internal comparison between the Y or Q bus data and the data from the diagnostics data register resulted in a TRUE (they were equal). This feature is used for breakpoint detection. It is an open-drain pin and can be wire AND with other DCMP pins.

DEVICE ARCHITECTURE

The IDT49C403 CMOS microprocessor slice is configured sixteen bits wide and is cascadable to any number of bits (32, 48, 64, etc.). Key elements which make up this sixteen-bit microprocessor slice are: (1) the RAM file (a 64 x 16 dual-port RAM) with latches on both outputs. (2) a high-performance ALU with shifter, (3) a flexible Q register file (4 x 16 bits) with shifter input, (4) a nine-bit instruction decoder, and (5) Serial Protocol Channel.

The IDT49C403 incorporates Serial Protocol Channel (SPC™). For system testing and debugging purposes SPC is a method by which data can be entered into and extracted from a device through a serial data input output, thus providing access to all internal registers.

REGISTER FILE

The Register File is composed of 64 x 16 bit RAM locations. The RAM data is read from the A-port as controlled by the 6-bit A address field input. Simultaneously, data can be read from the B port as defined by the 6-bit B address field input. If the same address is applied at both the A input field and the B input field, identical data will appear at the two respective output ports. Data is written into the RAM when $\overline{WE}$, $\overline{IEN}$ and the clock CP are LOW. Both the RAM output data latches are transparent while CP is HIGH and latch the data when CP is LOW. The three-state output enable $\overline{OEB}$ allows RAM B port data to be read at the DB I/O port, while $\overline{OEA}$ performs the same function for the A port data at the DA I/O port.

New data is written into the RAM word defined by the B address field. External data at the Y I/O port can be written directly into the RAM, or the ALU shifter output data can be enabled onto the Y I/O port and written into the RAM.

ALU

The ALU can perform seven arithmetic and nine logic operations on the two 16-bit input words S and R. Multiplexers at the ALU inputs allow selection of various pairs of ALU source operands. The $\overline{OEA}$ input selects either external DA data or RAM A port output data as the 16-bit R source operand. The $\overline{OEB}$ and I_0 inputs provide selection of either RAM B port output, external DB data or the Q register file output as the 16-bit S source operand. Also, during certain ALU operations, zeroes are forced at the ALU operand inputs. Thus, the ALU can operate on data from two external sources, from an external and an internal source, or from two internal sources. Table 1 shows all possible pairs of source operands as selected by $\overline{OEA}$, $\overline{OEB}$, and I_0 inputs.

Table 1. ALU Operand Sources[1]

$\overline{OEA}$	I_0	$\overline{OEB}$	ALU OPERAND R	ALU OPERAND S
L	L	L	Ram Output A	Ram Output B
L	L	H	Ram Output A	DB_{0-15}
L	H	X	Ram Output A	Q Register
H	L	L	DA_{0-15}	Ram Output B
H	L	H	DA_{0-15}	DB_{0-15}
H	H	X	DA_{0-15}	Q Register

NOTE:
1. L = LOW, H = HIGH, X = DON'T CARE

The ALU performs special functions when instruction bits I_3, I_2, I_1, and I_0 are LOW. Table 5 defines these special functions and the operation which the ALU performs for each. When the ALU executes instructions other than the special functions, the operation is defined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the operation as a function of these four instruction bits.

Table 2. IDT49C403 ALU Functions[1]

I_4	I_3	I_2	I_1	I_0	ALU FUNCTIONS
L	L	L	L	L	Special Functions
L	L	L	L	H	F_i = HIGH
L	L	L	H	X	$F=S-R-1+C_n$
L	L	H	L	X	$F=R-S-1+C_n$
L	L	H	H	X	$F=R+S+C_n$
L	H	L	L	X	$F=S+C_n$
L	H	L	H	X	$F=\overline{S}+C_n$
L	H	H	L	L	Reserved Special Functions
L	H	H	L	H	$F=R+C_n$
L	H	H	H	L	Reserved Special Functions
L	H	H	H	H	$F=\overline{R}+C_n$
H	L	L	L	L	Special Functions
H	L	L	L	H	F_i = LOW
H	L	L	H	X	$F_i=\overline{R}$ AND S
H	L	H	L	X	$F_i=R_i$ EXCLUSIVE NOR S_i
H	L	H	H	X	$F_i=R_i$ EXCLUSIVE OR S_i
H	H	L	L	X	$F_i=R_i$ AND S_i
H	H	L	H	X	$F_i=R_i$ NOR S_i
H	H	H	L	X	$F_i=R_i$ NAND S_i
H	H	H	H	X	$F_i=R_i$ OR S_i

NOTE:
1. L=LOW, H=HIGH, i=0 to 15, X=Don't Care

The IDT49C403 may be cascaded in either a ripple carry or carry lookahead fashion. When configured as cascaded ALUs, the IDT49C403s must be programmed to be a most significant slice (MSS), an intermediate slice (IS), or a least significant slice (LSS) of the array. The carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, signals that are necessary in a cascaded system are available as outputs on the IDT49C403 least significant and intermediate slices.

The IDT49C403 provides a carry-out signal C_{n+16} which is available as an output of each slice. The carry-in, C_n, and carry-out, C_{n+16}, are both active HIGH. Two other status outputs are generated by the ALU. These are the negative, N, and the overflow, OVR. The N output indicates positive or negative results, while the OVR output indicates that the arithmetic operation performed exceeded the available two's complement range. Thus the pins $\overline{G}$/N and $\overline{P}$/OVR indicate carry generate or propagate on the least significant and intermediate slice, and sign and overflow on the most significant slice.

Refer to Tables 6a and 6b for an exact definition of these four signals.

ALU DESTINATION CONTROL

The following tables show how the shifter at the output of the ALU should function for non-special instructions. The main addition with respect to the IDT39C203 is the built in byte capability.

The 49C403 has two write enables internally. One for the upper byte and one for the lower byte. The enables are controlled by the instruction decode, external $\overline{WE}$ and the W/$\overline{B}$ input. For convenience to the user, the unused bits on the Y bus (MSB, ..., 8) are zero during byte operation. The $\overline{WE}$ input must be directly connected to the WRITE output, or indirectly through some amount of gating (i.e., expansion RAM decoding gates).

The sign extend function is an exception to the rule with regard to the internal byte write enables. When executed, all of the write enables are active, irrespective of W/$\overline{B}$. In the SA and LSS slices, the contents of bit 7 is replicated on bits 8 to 15 and SIO_{15} in the byte mode. In the word mode bit 15 is placed on SIO_{15}. In this way an 8-bit word (byte) or a 16-bit word can be extended to the entire width of the native data path. Extends of larger words than these, such as 24 and 32 bits, can be achieved by steering the $\overline{MSS}$ and $\overline{LSS}$ inputs of the IS slices to inform which device has the sign bit to extend. As Sign Extend requires internal gating of the write enables to the upper and lower portions of RAM, the instruction will not work with locations in memory expansion RAM.

ALU SHIFTER

The ALU shifter shifts the ALU output data under instruction control. It can shift up one bit position (2F), shift down one bit position (F/2), or pass the ALU output non-shifted (F). An arithmetic shift operation shifts the data around the most significant (Sign) bit of the most significant slice and a logical shift operation shifts the data through the most significant bit. Figure 1 shows these shift patterns. The SIO_0 and SIO_{15} are bidirectional serial shift input/output pins. During a shift-up operation, SIO_0 is generally an input while SIO_{15} is an output, whereas during a shift-down operation SIO_0 is generally an output while SIO_{15} acts as an input. Refer to Tables 4 (a, b, c, d) and 5 for an exact definition of these pins.

The ALU shifter also provides sign extension and parity generating/checking capabilities. Under instruction control, the SIO_0 (Sign) input can be extended through $Y_0, Y_1, Y_2, \ldots Y_{15}$ and propagated to the SIO_{15} output. A cascadable, five-bit parity generator/checking generates parity for the $F_0, F_1, F_2, \ldots F_{15}$ ALU outputs and SIO_{15} input and, under instruction control, is made available at the SIO_0 output.

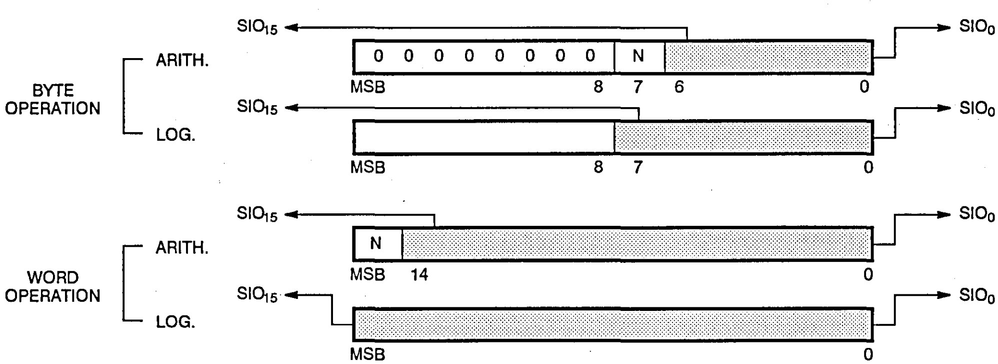


Figure 1. IDT49C403 Arithmetic and Logical Shift Operations

Table 5 defines the special functions and the operation the ALU shifter performs for each instruction. For instructions other than the special functions, the ALU shifter operation is determined by instruction bits I_8, I_7, I_6, and I_5. Table 4 (a, b, c, d) defines the ALU shifter operation as a function of these four bits.

WORD/BYTE CONTROL AND BYTE SWAP

In addition to the special ALU functions, the IDT49C403 also provides a Word and Byte control and Byte Swap features.

The W/$\overline{B}$ pin at the Instruction Decoder input selects ALU operation on either a Word or a Byte. When W/$\overline{B}$ is HIGH, the ALU operates on a Word and, when W/$\overline{B}$ is LOW, the ALU operates on a Byte. Table 4 (a, b, c, d) shows the ALU Destination Controls for Word and Byte operations for each instruction mode.

The Byte Swap special function allows the positions of the Upper and Lower bytes to be swapped before entering them as the ALU S operand. The ALU function then adds C_n to this swapped word as its F output. Table 5 shows the instruction set that allows the ALU to operate the Byte Swap feature.

Q REGISTER FILE

The Q register is a separate 4-word by 16-bit file intended primarily for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. The ALU output, F, can be loaded into the Q register and/or the Q register output can be selected as one of the ALU S operands. The shifter at the input to the Q register performs only logical shifts. It can shift-up the data one bit position (2Q) or down one bit position (Q/2). For a shift-up operation, QIO_0 acts as an input while QIO_{15} acts as an output; whereas, for a shift-down operation, QIO_0 is an output and QIO_{15} is an input. By connecting QIO_{15} of the most significant slice to SIO_0 of the least significant slice, double-length arithmetic and logical shifting is possible with cascaded IDT49C403s.

The Q_0 and Q_1 inputs enable selection of any one of the four 16-bit Q register files. Once a specific Q register has been selected, access to the other three Q registers is disabled and can be gained only after changing Q_0 and Q_1 levels to enable a different Q register.

Table 5 defines the special functions and the operations which the Q register and shifter perform for selected instruction inputs. While executing instructions other than the special functions, the Q register and shifter operation is controlled by instruction bits I_8, I_7, I_6 and I_5. Table 4 (a, b, c, d) defines the Q register and shifter operation as a function of these four bits.

INSTRUCTION DECODER

The internal control signals necessary for the operation of the IDT49C403 are generated by the instruction decoder as a function of the nine instruction inputs, I_{0-8}; the instruction enable input, $\overline{IEN}$; the $\overline{LSS}$ input; the $\overline{MSS}$ input; the W/$\overline{B}$ input and the $\overline{WRITE}$ output.

The $\overline{WRITE}$ output is LOW when an instruction which writes data into the RAM is executed. Refer to Tables 4 (a, b, c, d) and 5 for a definition of the $\overline{\text{WRITE}}$ output as a function of the instruction inputs.

When $\overline{\text{IEN}}$ is HIGH, the $\overline{\text{WRITE}}$ output is forced HIGH and the Q register and Sign Compare Flip-Flop contents are preserved. When $\overline{\text{IEN}}$ is LOW, the $\overline{\text{WRITE}}$ output is enabled and the Q register and Sign Compare Flip-Flop can be written according to the IDT49C403 instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during a divide operation. See Figure 2.

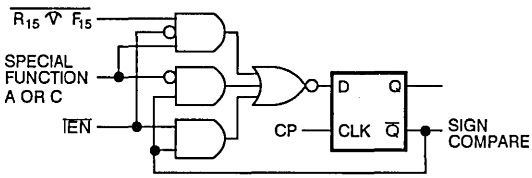


Figure 2. Sign Compare Flip-Flop

SLICE POSITION PROGRAMMING

The IDT49C403 can be programmed to operate in either a cascaded application or in the standalone mode. Table 3 shows its four programmed modes.

Table 3. SLICE Programming

SLICE PROGRAM INPUTS		MODE OF OPERATION
$\overline{\text{MSS}}$	$\overline{\text{LSS}}$	
LOW	LOW	Stand Alone Slice (SA)
LOW	HIGH	Most Significant Slice (MSS)
HIGH	HIGH	Intermediate Slice (IS)
HIGH	LOW	Least Significant Slice (LSS)

SPECIAL FUNCTIONS

Seventeen special functions are provided on the IDT49C403 which permit the implementation of the following operations:

- Single and Double Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation and Decrementation by One or Two
- BCD Add, Subtract, and Divide by Two
- Single and Double-precision BCD-to Binary and Binary-to-BCD Conversion
- Byte Swap

Adjusting a single-precision or double-precision floating-point number in order to bring its mantissa within a specified range can be performed using the single-length and double-length normalization operations.

Three special functions can be used to perform a two's complement, non-restoring divide operation. They provide single and double-precision divide operations and can be performed in "n" clock cycles (where "n" is the number of bits in the quotient).

The unsigned multiply special function and the two two's complement multiply special functions can be used to multiply two n-bit, unsigned or two's complement numbers respectively, in 'n' clock cycles. During the last cycle of the two's complement multiplication, a conditional subtraction rather than addition is performed due to the fact that the sign bit of the multiplier carries negative weight.

The sign/magnitude—two's complement special function can be used to convert number representation systems. A number expressed in sign/magnitude representation can be converted to the two's complement representation, and vice-versa, in one clock cycle.

Incrementing an unsigned or two's complement number by one or two is easily accomplished using the increment by one or two special function.

In addition to BCD arithmetic special functions to add or subtract two BCD numbers, a BCD divide by two adjust instruction can be used to obtain a valid BCD representation after shifting a number down by one bit.

The BCD/Binary conversion special function instructions permit single and double-precision algorithms to convert from BCD-to-Binary and from Binary-to-BCD.

The Byte Swap feature allows the swapping of Lower and Upper bytes of a word before presenting them as the ALU S operand. The ALU then adds the carry C_n to this swapped word to form its F output. This feature functions only for the ALU S operand.

SERIAL DIAGNOSTICS

The Serial Protocol Channel ™ (SPC) is a flexible on-chip feature of the IDT49C403 and is a set of pins by which data can be entered into and extracted from a device through a serial data input and output port.

SPC can be used at many points in the life of a product for diagnostic purposes such as system level design debug and development; system test during manufacturing and field maintenance debug and test. It allows for observation of critical signals deep within the system. During system test, when an error is observed, these signals may be modified in order to zero in on the fault in the system. Serial diagnostics is primarily a scheme utilizing only four pins to examine and alter the internal state of a system for the purpose of monitoring and diagnosing system faults.

Detailed SPC Architecture of the IDT49C403 Bit-Slice Microprocessor

The IDT49C403, a quad Am2903/29203 16-bit microprocessor slice, which includes an ALU and register file, is one of the devices on which IDT has incorporated the Serial Protocol Channel. The implementation of SPC on the IDT49C403 is shown in Figure 3.

Only four SPC pins (SDI, SDO, SCLK and C/$\overline{\text{D}}$) are used to serially access the I/O pad cells, as well as the internal ALU registers and buses. To control or monitor a section (such as the ALU), the appropriate command is loaded into the SPC command register. The desired function is then executed and the status information captured in the data register. The status information can then be serially shifted out and observed to verify proper system functionality.

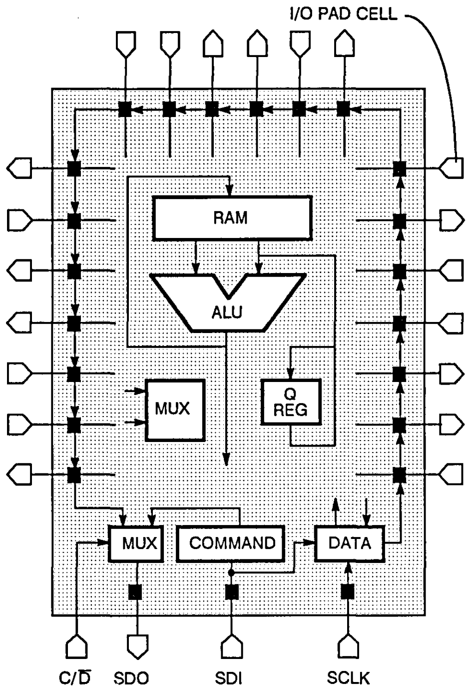


Figure 3. Conceptual Diagram of IDT49C403 Die Incorporating SPC Scan Path

The block diagram in Figure 4 shows the detailed SPC architecture for the IDT49C403. It primarily consists of serial registers for command, data, addresses and decode/control logic. The SPC command register consists of a four-bit field (signals 4-7) and four discrete control lines (signals 3, 2, 1, 0). The four-bit field coordinates the transfer of data between RAM and the SPC data register, as well as controls an on-chip break detect mechanism. The other discrete signals control the serial scan path through the I/O cells.

The SPC data register is in series with a RAM address register and I/O pad scan. The SPC data register is connected to the internal bus to gain access to the RAM register file as well as a data break point feature. The point of connection is the Y bus from the ALU back into the RAM.

8

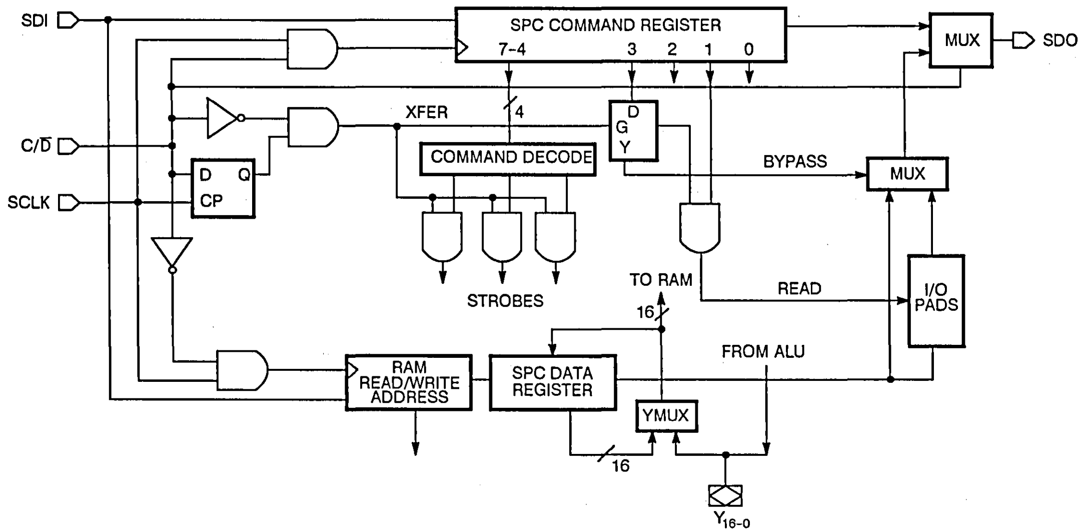


Figure 4. Internal Organization of the SPC

The multiplexer at the output transmits information via the SDO pin selecting data from either the SPC data register and the I/O pads or the command string from the SPC command register.

IDT49C403 SPC Command Opcodes

The SPC command register consists of an 8-bit field, as shown in Figure 5. Bit 1 enables the READ function of the I/O pad cells. Bit 3 enables the BYPASS function to bypass the I/O pad cells and scan out only the RAM address and data registers. Bits 0 and 2 are reserved. Bits 4 through 7 form the opcode field for reading and writing into the device.

The 4-bit command opcode field gives 16 possible command opcodes. The first 8 are reserved for writing data from the SPC data register into the registers and RAM on the device. The second 8 opcodes are reserved for reading data from registers and RAM into the 16-bit SPC data register.

COMMAND OPCODES	
OPCODE	FUNCTION
0	Write RAM
1	Write Q Registers
2	Write Break Control
3	Write Break Data
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Read RAM
9	Read Q Registers
10	Read Break Control
11	Read Break Data
12	View Y
13	Reserved
14	Reserved
15	NOP

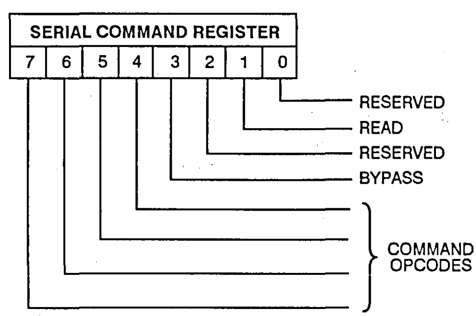


Figure 5. SPC Command Register and Opcodes for the IDT49C403

The command with opcode 0 causes a write to the internal device RAM. Opcode 1 is used to write to the Q registers. Opcodes 2 and 3 are used to write data from SPC data register into the break data register and break control registers, respectively. Opcodes 4 through 7 are reserved opcodes.

Opcode 8 is used for reading RAM data into the SPC data register. Opcode 9 is used to read a value out of the Q registers. (Here, also, the address register supplies the address of the Q register to be accessed). Opcodes 10 and 11 are used for reading the break control register and the break data register, respectively. Opcode 12 is used to strobe data from the Z bus into the 16-bit diagnostics data register. Opcodes 13 and 14 are reserved opcodes. The last opcode, 15, is a no-operation opcode. This opcode can be used to scan the data in and out of the I/O pad cells and use the device in a pass-through mode (in a cascaded application) without affecting normal device operation.

All the reserved opcodes, if executed, perform a no-operation; however, they should not be relied upon to always perform NOPs as future upgrades may make use of reserved opcodes.

Accessing the Contents of the IDT49C403 Register File

To read data from the device's internal RAM or other logic circuitry into the SPC data register, the address and don't care bits (for the SPC data register) are shifted in. The command is shifted into the SPC command register. The command register must be decoded to determine what data paths are to be steered in order to get data into the SPC data register. The read strobe, generated by the strobe logic, must then strobe this data (in parallel) into the SPC data register. The data can now be shifted out via the SDO pin and its contents disassembled and observed.

To perform the write operation, address and data must first be shifted into the SPC data register. The command is then shifted into the SPC command register via the command mode. This register provides information as to what data paths are to be steered. The address is supplied by the address register in the data scan path. The write strobe is then generated between the time the C/$\overline{D}$ line is lowered and the SCLK line is raised. This is the strobe which actually clocks the data into the RAM or register in the device.

Pad Cell Scan Path

Each I/O cell on the IDT49C403 contains a flip-flop which can be used to store the state of that cell and then be scanned out. Figure 6 shows the logic configuration. The READ line is enabled by a bit in the SPC command register and gated by the XFER signal, thus loading the scan flip-flops in parallel. The SCLK is then used to scan the data out of the SDO pin in series with the address and SPC data registers.

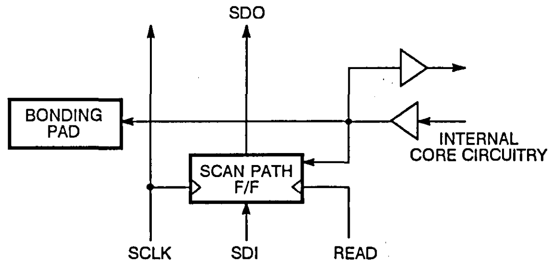


Figure 6. Serial Scan in the I/O Cell

The BYPASS bit in the SPC command register selects whether the shifting of the I/O cells will be bypassed such that only the RAM address and data registers are scanned out. When the READ bit is HIGH, data is transferred from the pins to the scan register when SCLK transitions HIGH after C/D has transitioned LOW. The BYPASS bit in the command register is active HIGH so that a HIGH level bypasses scanning the I/O cells.

Figure 7 shows the order in which the I/O pad cells are scanned. The clocking will shift out the data on the Y_{15} pin first and continue in series until the WRITE pin is shifted out last.

8

0	Y15	25	$\overline{G}$/N	50	DB10	75	DA12
1	Y14	26	CN16	51	DB11	76	DA13
2	Y13	27	15	52	DB12	77	DA14
3	Y12	28	16	53	DB13	78	DA15
4	Y11	29	17	54	DB14	79	$\overline{LSS}$
5	Y10	30	18	55	DB15	80	CP
6	Y9	31	DCMP	56	$\overline{OEA}$	81	$\overline{WE}$
7	Y8	32	$\overline{MSS}$	57	DA0	82	B0
8	QIO15	33	DB0	58	DA1	83	B1
9	SIO15	34	DB1	59	DA2	84	B2
10	QIO0	35	DB2	60	DA3	85	B3
11	SIO0	36	DB3	61	DA4	86	B4
12	$\overline{OEY}$	37	DB4	62	DA5	87	B5
13	Z	38	DB5	63	DA6	88	Q0
14	W/$\overline{B}$	39	DB6	64	DA7	89	Q1
15	Y7	40	DB7	65	A0	90	$\overline{WRITE}$
16	Y6	41	$\overline{OEB}$	66	A1		
17	Y5	42	CN	67	A2		
18	Y4	43	I0	68	A3		
19	Y3	44	I1	69	A4		
20	Y2	45	I2	70	A5		
21	Y1	46	I3	71	DA8		
22	Y0	47	I4	72	DA9		
23	$\overline{IEN}$	48	DB8	73	DA10		
24	$\overline{P}$/N	49	DB9	74	DA11		

Figure 7. Shift Order of I/O Pad Cells

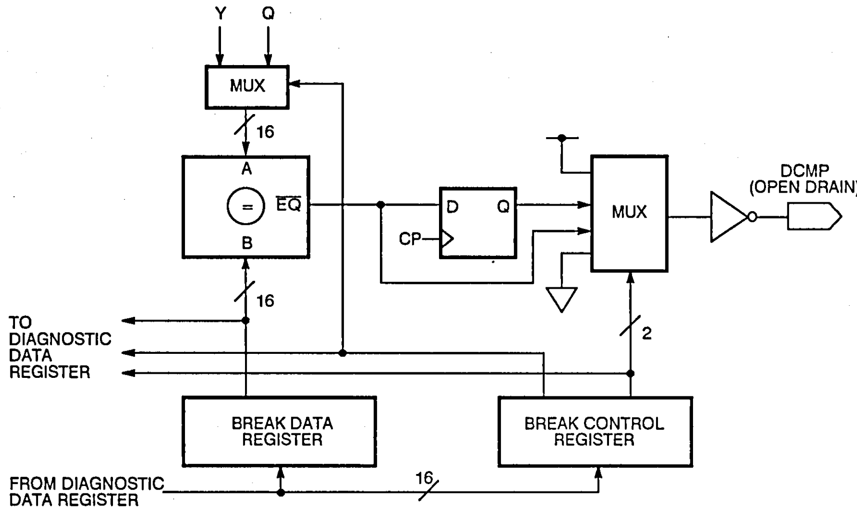


Figure 8. Breakpoint Detect Circuitry

Breakpoint Detection on the IDT49C403

Figure 8 shows the diagnostics breakpoint detection circuit on the IDT49C403. This circuit is designed to allow the user to monitor certain key data buses and detect the data patterns on the Y and Q buses. When a data pattern is detected, a breakpoint compare signal is generated on the DCMP pin and is used to halt the system operation. The DCMP is an open drain signal and should be wire-ORed with DCMP lines of other similar devices and monitored by the main sequencer in the system. The breakpoint detection mechanism thus allows for an easier debug of microcode with regard to the data path.

At the heart of the breakpoint detection circuit is a comparator which compares data from the break data register with data from either the Y bus or the Q bus. The break control register determines which of the two buses is selected for a comparison. The break control register also steers a multiplexer at the output of the comparator. This multiplexer selects between the equal-to signal, latched equal-to, V_{CC} or GND. The latched equal-to input into the multiplexer gives the user the ability to pipeline the match signal, thus shortening the system cycle time in the diagnostics mode. The V_{CC} and GND inputs to the multiplexer allow the programmer to disable the break compare feature by forcing the DCMP pin either LOW or HIGH, respectively.

When a match is made, the DCMP line goes HIGH. Thus, if any one slice in a cascade application does not match, the wire-ANDed DCMP will be low. Selecting V_{CC} via the multiplexer will disable matches altogether. To select GND, disable any one slice from the comparison.

Figure 9 shows the format of the break data and break control register. The break data pattern is 16 bits wide, with bit 16 being the most significant bit and last to be shifted in. The Break Control register contains three fields. Bits 0 and 1 control the DCMP output and bit 2 selects between the Y and the Q bus to be compared with the break data register. Bits 3 to 15 are reserved for future expansion.

BREAK DATA REGISTER FORMAT

15 … 0
BREAK DATA PATTERN

BREAK CONTROL REGISTER FORMAT

15 ••• 3	2	1 0
•••	BUS SEL	DCMP CONTROL

BREAK POINT CONTROL ACCESS

BUS SEL	BUS
0	Y
1	Q

DCMP CONTROL		DCMP STATUS
0	0	LOW
0	1	PIPELINED
1	0	NON-PIPELINED
1	1	HIGH

Figure 9. Breakpoint Control Registers and Opcodes

The SPC version allows data to be transferred into and out of a device and can also accommodate addresses and commands using the same number of pins. This is accomplished with a reconfiguration of the function of the diagnostic pins and internal logic. With this vastly expanded capability, SPC can conveniently be used in RAMs, peripherals an complex logic functions. These new capabilities allow the user to monitor and modify all of the storage elements and pins of a device. With a simple hardware interface and appropriate software, any type personal or mini computer can be turned into a development system for IDT parts with serial diagnostics.

Figure 10 shows the Serial Protocol Channel being used with a writable control store in a microprogrammed design. The control store can be initialized through the SPC path. A register with SPC is used for the instruction register going into the IDT49C410 (16-bit microprogram sequencer) as well as data registers around the IDT49C403. In this way, the designer may use the Serial Protocol Channel to observe and modify the microcode coming out of the writable control store, as well as observing and being able to modify data and instructions in the overall machine.

The block diagram of the diagnostics ring shows how the devices with diagnostics are hooked together in a serial ring via the SDI and SDO signals. The diagnostics signals may be generated through registers which are hooked up to a microprocessor. This microprocessor could conceivably be an IBM PC.

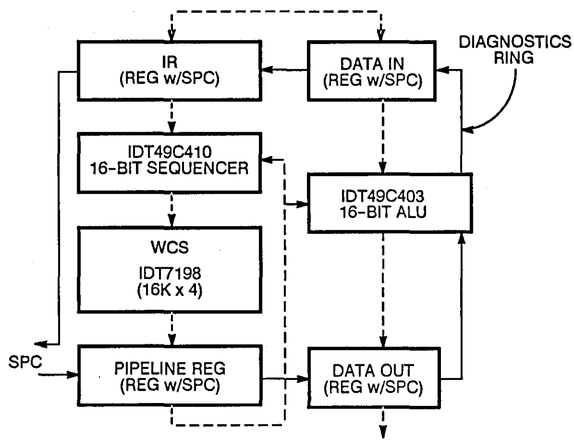


Figure 10. Typical Microprogram Application with SPC

Table 4a. ALU Destination Control (Word Mode) for I_0 or I_1 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	SIO_{15} SA	SIO_{15} MSS	SIO_{15} IS	SIO_{15} LSS	SIO_0	$\overline{WRITE}$	Q REGISTER AND SHIFTER FUNCTION	QIO_{15}	QIO_0
L L L L	Arith. F/2 → Y	0	Input →			→	F_0	L	Hold	Z	Z
L L L H	Log. F/2 → Y	1	↓				↓	L	Hold	Z	Z
L L H L	Arith. F/2 → Y	2	↓				↓	L	Log. Q/2 → Q	Input	Q_0
L L H H	Log. F/2 → Y	3	↓				↓	L	Log. Q/2 → Q	Input	Q_0
L H L L	F → Y	4	↓				Parity	L	Hold	Z	Z
L H L H	F → Y	5	↓				↓	H	Log. Q/2 → Q	Input	Q_0
L H H L	F → Y	6	↓				↓	H	F → Q	Z	Z
L H H H	F → Y	7	↓				↓	L	F → Q	Z	Z
H L L L	Arith. 2F → Y	8	F_{14}	F_{14}	F_{15}	F_{15}	Input	L	Hold	Z	Z
H L L H	Log. 2F → Y	9	F_{15}	F_{15}	↓	↓	↓	L	Hold	Z	Z
H L H L	Arith. 2F → Y	A	F_{14}	F_{14}	↓	↓	↓	L	Log. 2Q → Q	Q_{15}	Input
H L H H	Log. 2F → Y	B	F_{15}	F_{15}	↓	↓	↓	L	Log. 2Q → Q	Q_{15}	Input
H H L L	F → Y	C	↓	↓	↓	↓	↓	H	Hold	Z	Z
H H L H	F → Y	D	↓	↓	↓	↓	↓	H	Log. 2Q → Q	Q_{15}	Input
H H H L	Sign Extend	E	↓	SIO_0	SIO_0	↓	↓	L	Hold	Z	Z
H H H H	F → Y	F	↓	F_{15}	F_{15}	↓	↓	L	Hold	Z	Z

Table 4b. ALU Destination Control (Byte Mode) for I_0 or I_1 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	SIO_{15} SA	SIO_{15} MSS	SIO_{15} IS	SIO_{15} LSS	SIO_0 SA	SIO_0 MSS	SIO_0 IS	SIO_0 LSS	$\overline{WRITE}$	Q REGISTER AND SHIFTER FUNCTION	QIO_{15} MSS/IS	QIO_{15} SA/LSS	QIO_0 MSS/IS	QIO_0 SA/LSS
L L L L	Arith. F/2→Y	0	Input →			→	F_0	SIO_{15}	SIO_{15}	F_0	L	Hold	Z →			→
L L L H	Log. F/2→Y	1	↓				↓	↓	↓	↓	L	Hold	Z →			→
L L H L	Arith. F/2→Y	2	↓				↓	↓	↓	↓	L	Log. Q/2→Q	Input →	→	QIO_{15}	Q_0
L L H H	Log. F/2→Y	3	↓				↓	↓	↓	↓	L	Log. Q/2→Q	Input →	→	QIO_{15}	Q_0
L H L L	F→Y	4	↓				Parity	↓	↓	Parity	L	Hold	Z →			→
L H L H	F→Y	5	↓				↓	↓	↓	↓	H	Log. Q/2→Q	Input →	→	QIO_{15}	Q_0
L H H L	F→Y	6	↓				↓	↓	↓	↓	H	F→Q	Z →			→
L H H H	F→Y	7	↓				↓	↓	↓	↓	L	F→Q	↓			
H L L L	Arith. 2F→Y	8	F_6	SIO_0	SIO_0	F_6	Input →			→	L	Hold	↓			
H L L H	Log. 2F→Y	9	F_7	↓	↓	F_7	↓				L	Hold	↓			
H L H L	Arith. 2F→Y	A	F_6	↓	↓	F_6	↓				L	Log. 2Q →Q	QIO_0	Q_7	Input →	→
H L H H	Log. 2F→Y	B	F_7	↓	↓	F_7	↓				L	Log. 2Q →Q	QIO_0	Q_7	Input →	→
H H L L	F→Y	C	↓	↓	↓	↓	↓				H	Hold	Z →			→
H H L H	F→Y	D	↓	↓	↓	↓	↓				H	Log. 2Q →Q	QIO_0	Q_7	Input →	→
H H H L	Sign Extend	E	↓	↓	↓	↓	↓				L	Hold	Z →			→
H H H H	F→Y	F	↓	↓	↓	↓	↓				L	Hold	Z →			→

Parity = $F_{15} \oplus F_{14}$ ...... $\oplus F_3 \oplus F_2 \oplus F_1 \oplus F_0 \oplus SIO_{15}$
$\oplus$ = Exclusive OR

L = LOW
H = HIGH
Z = High Impedance

SA = Stand Alone
MSS = Most Significant Slice
IS = Intermediate Slice
LSS = Least Significant Slice

Table 4c. ALU Destination Control for I_0 or I_1 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	SIO_{15}								Y_{15}								Y_{14}							
			SA		MSS		IS		LSS		SA		MSS		IS		LSS		SA		MSS		IS		LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Arith. F/2→Y	0	Input →	→	→	→	→	→	→	→	0	F_{15}	0	F_{15}	0	SIO_{15}	0	SIO_{15}	0	SIO_{15}	0	SIO_{15}	0	F_{15}	0	F_{15}
L L L H	Log. F/2→Y	1	↓								↓	SIO_{15}	↓	SIO_{15}	↓	↓	↓	↓	↓	F_{15}	↓	F_{15}	↓	↓	↓	↓
L L H L	Arith. F/2→Y	2	↓								↓	F_{15}	↓	F_{15}	↓	↓	↓	↓	↓	SIO_{15}	↓	SIO_{15}	↓	↓	↓	↓
L L H H	Log. F/2→Y	3	↓								↓	SIO_{15}	↓	SIO_{15}	↓	↓	↓	↓	↓	F_{15}	↓	F_{15}	↓	↓	↓	↓
L H L L	F→Y	4	↓								↓	F_{15}	↓	F_{15}	↓	F_{15}	↓	F_{15}	↓	F_{14}	↓	F_{14}	↓	F_{14}	↓	F_{14}
L H L H	F→Y	5	↓								↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
L H H L	F→Y	6	↓								↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
L H H H	F→Y	7	↓								↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
H L L L	Arith. 2F→Y	8	F_6	F_{14}	SIO_0	F_{14}	SIO_0	F_{15}	F_6	F_{15}	↓	↓	↓	↓	↓	F_{14}	↓	F_{14}	↓	F_{13}	↓	F_{13}	↓	F_{13}	↓	F_{13}
H L L H	Log. 2F→Y	9	F_7	F_{15}	↓	F_{15}	↓	↓	F_7	↓	↓	F_{14}	↓	F_{14}	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
H L H L	Arith. 2F→Y	A	F_6	F_{14}	↓	F_{14}	↓	↓	F_6	↓	↓	F_{15}	↓	F_{15}	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
H L H H	Log. 2F→Y	B	F_7	F_{15}	↓	F_{15}	↓	↓	F_7	↓	↓	F_{14}	↓	F_{14}	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
H H L L	F→Y	C	↓	↓	↓	↓	↓	↓	↓	↓	↓	F_{15}	↓	F_{15}	↓	F_{15}	↓	F_{15}	↓	F_{14}	↓	F_{14}	↓	F_{14}	↓	F_{14}
H H L H	F→Y	D	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	F_{15}	↓	F_{15}	↓	↓	↓	↓	↓	F_{14}	↓	F_{14}	↓	↓
H H H L	Sign Extend	E	↓	↓	↓	SIO_0	↓	SIO_0	↓	↓	F_7	↓	SIO_0	SIO_0	SIO_0	SIO_0	F_7	↓	F_7	↓	SIO_0	SIO_0	SIO_0	SIO_0	F_7	↓
H H H H	F→Y	F	↓	↓	↓	F_{15}	↓	F_{15}	↓	↓	0	↓	0	F_{15}	0	F_{15}	0	↓	0	↓	0	F_{14}	0	F_{14}	0	↓

Table 4c. ALU Destination Control for I_0 or I_1 or I_3 = HIGH, $\overline{IEN}$ = LOW (cont'd.)

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	Y_{13-9}								Y_8								Y_7							
			SA		MSS		IS		LSS		SA		MSS		IS		LSS		SA		MSS		IS		LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Arith. F/2→Y	0	0	F_{i+1}	0	F_{i+1}	0	F_{i+1}	0	F_{i+1}	0	F_9	0	F_9	0	F_9	0	F_9	F_7	F_8	0	F_8	0	F_8	F_7	F_8
L L L H	Log. F/2→Y	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	SIO_{15}	↓	↓	↓	↓	↓	SIO_{15}	↓
L L H L	Arith. F/2→Y	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	F_7	↓	↓	↓	↓	↓	F_7	↓
L L H H	Log. F/2→Y	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	SIO_{15}	↓	↓	↓	↓	↓	SIO_{15}	↓
L H L L	F→Y	4	↓	F_i	↓	F_i	↓	F_i	↓	F_i	↓	F_8	↓	F_8	↓	F_8	↓	F_8	F_7	F_7	↓	F_7	↓	F_7	F_7	F_7
L H L H	F→Y	5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
L H H L	F→Y	6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
L H H H	F→Y	7	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
H L L L	Arith. 2F→Y	8	↓	F_{i-1}	↓	F_{i-1}	↓	F_{i-1}	↓	F_{i-1}	↓	F_7	↓	F_7	↓	F_7	↓	F_7	↓	F_6	↓	F_6	↓	F_6	↓	F_6
H L L H	Log. 2F→Y	9	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	F_6	↓	↓	↓	↓	↓	F_6	↓
H L H L	Arith. 2F→Y	A	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	F_7	↓	↓	↓	↓	↓	F_7	↓
H L H H	Log. 2F→Y	B	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	F_6	↓	↓	↓	↓	↓	F_6	↓
H H L L	F→Y	C	↓	F_i	↓	F_i	↓	F_i	↓	F_i	↓	F_8	↓	F_8	↓	F_8	↓	F_8	F_7	F_7	↓	F_7	↓	F_7	F_7	F_7
H H L H	F→Y	D	↓	↓	↓	F_i	↓	F_i	↓	↓	↓	↓	↓	F_8	↓	F_8	↓	↓	↓	↓	↓	F_7	↓	F_7	↓	↓
H H H L	Sign Extend	E	F_7	↓	SIO_0	SIO_0	SIO_0	SIO_0	F_7	↓	F_7	↓	SIO_0	SIO_0	SIO_0	SIO_0	F_7	↓	↓	↓	SIO_0	SIO_0	SIO_0	SIO_0	↓	↓
H H H H	F→Y	F	0	↓	0	F_i	0	F_i	0	↓	0	↓	0	F_8	0	F_8	0	↓	↓	↓	0	F_7	0	F_7	↓	↓

8

Table 4c. ALU Destination Control (cont'd.) for I_0 or I_1 or I_3 = HIGH, $\overline{IEN}$ = LOW

$I_8\ I_7\ I_6\ I_5$	ALU SHIFTER FUNCTION	HEX	Y_6								Y_{5-1}								Y_0							
			SA		MSS		IS		LSS		SA		MSS		IS		LSS		SA		MSS		IS		LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Arith. F/2→Y	0	SIO_{15}	F_7	0	F_7	0	F_7	SIO_{15}	F_7	F_{i+1}	F_{i+1}	0	F_{i+1}	0	F_{i+1}	F_{i+1}	F_{i+1}	F_1	F_1	0	F_1	0	F_1	F_1	F_1
L L L H	Log. F/2→Y	1	F_7						F_7																	
L L H L	Arith. F/2→Y	2	SIO_{15}						SIO_{15}																	
L L H H	Log. F/2→Y	3	F_7	↓		↓		↓	F_7	↓	↓	↓		↓		↓	↓	↓	↓	↓		↓		↓	↓	↓
L H L L	F→Y	4	F_6	F_6		F_6		F_6	F_6	F_6	F_i	F_i		F_i		F_i	F_i	F_i	F_0	F_0		F_0		F_0	F_0	F_0
L H L H	F→Y	5																								
L H H L	F→Y	6																								
L H H H	F→Y	7	↓	↓		↓		↓	↓	↓	↓	↓		↓		↓	↓	↓	↓	↓		↓		↓	↓	↓
H L L L	Arith. 2F→Y	8	F_5	F_5		F_5		F_5	F_5	F_5	F_{i-1}	F_{i-1}		F_{i-1}		F_{i-1}	F_{i-1}	F_{i-1}	SIO_0	SIO_0		SIO_0		SIO_0	SIO_0	SIO_0
H L L H	Log. 2F→Y	9																								
H L H L	Arith. 2F→Y	A																								
H L H H	Log. 2F→Y	B	↓	↓		↓		↓	↓	↓	↓	↓		↓		↓	↓	↓	↓	↓		↓		↓	↓	↓
H H L L	F→Y	C	F_6	F_6		F_6		F_6	F_6	F_6	F_i	F_i		F_i		F_i	F_i	F_i	F_0	F_0		F_0		F_0	F_0	F_0
H H L H	F→Y	D			↓	F_6	↓	F_6					↓	F_i	↓	F_i					↓	F_0	↓	F_0		
H H H L	Sign Extend	E			SIO_0	SIO_0	SIO_0	SIO_0					SIO_0	SIO_0	SIO_0	SIO_0					SIO_0	SIO_0	SIO_0	SIO_0		
H H H H	F→Y	F	↓	↓	0	F_6	0	F_6	↓	↓	↓	↓	0	F_i	0	F_i	↓	↓	↓	↓	0	F_0	0	F_0	↓	↓

i = 1 to 6 (for Q_{5-1})
i = 9 to 14 (for Q_{13-9})

SA = Stand Alone
MSS = Most Significant Slice
IS = Intermediate Slice
LSS = Least Significant Slice

$I_8\ I_7\ I_6\ I_5$	ALU SHIFTER FUNCTION	HEX	SIO_0							
			SA		MSS		IS		LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Arith. F/2→Y	0	F_0	F_0	SIO_{15}	F_0	SIO_{15}	F_0	F_0	F_0
L L L H	Log. F/2→Y	1								
L L H L	Arith. F/2→Y	2								
L L H H	Log. F/2→Y	3	↓	↓		↓		↓	↓	↓
L H L L	F→Y	4	Parity	Parity		Parity		Parity	Parity	Parity
L H L H	F→Y	5								
L H H L	F→Y	6								
L H H H	F→Y	7	↓	↓	↓	↓	↓	↓	↓	↓
H L L L	Arith. 2F→Y	8	Input →							
H L L H	Log. 2F→Y	9								
H L H L	Arith. 2F→Y	A								
H L H H	Log. 2F→Y	B								
H H L L	F→Y	C								
H H L H	F→Y	D								
H H H L	Sign Extend	E								
H H H H	F→Y	F	↓							

Table 4d. ALU Destination Control for I_0 or I_1 or I_3 = HIGH, $\overline{IEN}$ = LOW

$I_8\ I_7\ I_6\ I_5$	Q REGISTER AND SHIFTER FUNCTION	HEX	QIO_{15}				Q_{15}				Q_{14-9}				Q_8			
			MSS/IS		SA/LSS		MSS/IS		SA/LSS		MSS/IS		SA/LSS		MSS/IS		SA/LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Hold	0	Z →				Hold →				Hold →				Hold →			
L L L H	Hold	1	Z →				→				→				→			
L L H L	Log. Q/2→Q	2	Input →				↓	QIO_{15}	↓	QIO_{15}	↓	Q_{i+1}	↓	Q_{i+1}	↓	Q_9	↓	Q_9
L L H H	Log. Q/2→Q	3	Input →				↓	QIO_{15}	↓	QIO_{15}	↓	Q_{i+1}	↓	Q_{i+1}	↓	Q_9	↓	Q_9
L H L L	Hold	4	Z →				↓	Hold	↓	Hold	↓	Hold	↓	Hold	↓	Hold	↓	Hold
L H L H	Log. Q/2→Q	5	Input →				↓	QIO_{15}	↓	QIO_{15}	↓	Q_{i+1}	↓	Q_{i+1}	↓	Q_9	↓	Q_9
L H H L	F→Q	6	Z →				↓	F_{15}	↓	F_{15}	↓	F_i	↓	F_i	↓	F_8	↓	F_8
L H H H	F→Q	7	↓				↓	F_{15}	↓	F_{15}	↓	F_i	↓	F_i	↓	F_8	↓	F_8
H L L L	Hold	8	↓				↓	Hold	↓	Hold	↓	Hold	↓	Hold	↓	Hold	↓	Hold
H L L H	Hold	9	↓				↓	Hold	↓	Hold	↓	Hold	↓	Hold	↓	Hold	↓	Hold
H L H L	Log. 2Q→Q	A	QIO_0	Q_{15}	Q_7	Q_{15}	↓	Q_{14}	↓	Q_{14}	↓	Q_{i-1}	↓	Q_{i-1}	↓	Q_7	↓	Q_7
H L H H	Log. 2Q→Q	B	QIO_0	Q_{15}	Q_7	Q_{15}	↓	Q_{14}	↓	Q_{14}	↓	Q_{i-1}	↓	Q_{i-1}	↓	Q_7	↓	Q_7
H H L L	Hold	C	Z →				↓	Hold	↓	Hold	↓	Hold	↓	Hold	↓	Hold	↓	Hold
H H L H	Log. 2Q→Q	D	QIO_0	Q_{15}	Q_7	Q_{15}	↓	Q_{14}	↓	Q_{14}	↓	Q_{i-1}	↓	Q_{i-1}	↓	Q_7	↓	Q_7
H H H L	Hold	E	Z →				↓	Hold	↓	Hold	↓	Hold	↓	Hold	↓	Hold	↓	Hold
H H H H	Hold	F	Z →				↓	Hold	↓	Hold	↓	Hold	↓	Hold	↓	Hold	↓	Hold

Table 4d. ALU Destination Control for I_0 or I_1 or I_3 = HIGH, $\overline{IEN}$ = LOW (cont'd.)

$I_8\ I_7\ I_6\ I_5$	Q REGISTER AND SHIFTER FUNCTION	HEX	Q_7				Q_{6-1}				Q_0				QIO_0			
			MSS/IS		SA/LSS		MSS/IS		SA/LSS		MSS/IS		SA/LSS		MSS/IS		SA/LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Hold	0	Hold →				Hold →				Hold →				Z →			
L L L H	Hold	1	→				→				→				Z →			
L L H L	Log. Q/2→Q	2	↓	Q_8	QIO_{15}	Q_8	↓	Q_{i+1} →			↓	Q_1 →			QIO_{15}	Q_0 →		
L L H H	Log. Q/2→Q	3	↓	Q_8	QIO_{15}	Q_8	↓	Q_{i+1} →			↓	Q_1 →			QIO_{15}	Q_0 →		
L H L L	Hold	4	↓	Hold →			↓	Hold →			↓	Hold →			Z →			
L H L H	Log. Q/2→Q	5	↓	Q_8	QIO_{15}	Q_8	↓	Q_{i+1} →			↓	Q_1 →			QIO_{15}	Q_0 →		
L H H L	F→Q	6	↓	F_7 →			↓	F_i →			↓	F_0 →			Z →			
L H H H	F→Q	7	↓	F_7 →			↓	F_i →			↓	F_0 →			↓			
H L L L	Hold	8	↓	Hold →			↓	Hold →			↓	Hold →			↓			
H L L H	Hold	9	↓	Hold →			↓	Hold →			↓	Hold →			↓			
H L H L	Log. 2Q→Q	A	↓	Q_6 →			↓	Q_{i-1} →			↓	QIO_0 →			Input →			
H L H H	Log. 2Q→Q	B	↓	Q_6 →			↓	Q_{i-1} →			↓	QIO_0 →			Input →			
H H L L	Hold	C	↓	Hold →			↓	Hold →			↓	Hold →			Z →			
H H L H	Log. 2Q→Q	D	↓	Q_6 →			↓	Q_{i-1} →			↓	QIO_0 →			Input →			
H H H L	Hold	E	↓	Hold →			↓	Hold →			↓	Hold →			Z →			
H H H H	Hold	F	↓	Hold →			↓	Hold →			↓	Hold →			Z →			

Parity = $F_{15} \forall F_{14} \ldots\ldots \forall F_3 \forall F_2 \forall F_1 \forall F_0 \forall SIO_{15}$

$\forall$ = Exclusive OR

i = 1 to 6 (for Q_{6-1})
i = 9 to 14 (for Q_{14-9})

Z = High Impedance
SA = Stand Alone
MSS = Most Significant Slice
IS = Intermediate Slice
LSS = Least Significant Slice

Table 5. Special Functions (7)

HEX $I_8\ I_7\ I_6\ I_5$	I_4	HEX $I_3\ I_2\ I_1\ I_0$	SPECIAL FUNCTION	ALU FUNCTION	ALU SHIFTER FUNCTION	SIO_{15} MSS	SIO_{15} OTHER SLICES	SIO_0	Q REGISTER & SHIFTER FUNCTION	QIO_{15}	QIO_0	$\overline{WRITE}$
0	L	0	Unsigned Multiply	$F=S+C_n$ if $Z=L$ $F=R+S+C_n$ if $Z=H$	Log F/2→Y (1)	Z	Input	F_0	Log Q/2→Q	Input	Q_0	L
1	L	0	BCD-to-Binary Conversion	(4)	Log F/2→Y	Input	Input	F_0	Log Q/2→Q	Input	Q_0	L
1	H	0	Multiprecision BCD-to-Binary	(4)	Log F/2→Y	Input	Input	F_0	Hold	Z	Q_0	L
2	L	0	Two's Complement Multiply	$F=S+C_n$ if $Z=L$ $F=R+S+C_n$ if $Z=H$	Log F/2→Y (2)	Z	Input	F_0	Log Q/2→Q	Input	Q_0	L
3	L	0	Decrement by One or Two	$F=S-2+C_n$	F→Y	Input	Input	Parity	Hold	Z	Z	L
4	L	0	Increment by One or Two	$F=S+1+C_n$	F→Y	Input	Input	Parity	Hold	Z	Z	L
4	H	0	Byte Swap + C_n	$F=(LB, UB)+C_n$	F→Y	Input	Input	Parity	Hold	Z	Z	L
5	L	0	Sign/Magnitude Two's Complement	$F=S+C_n$ if $Z=L$ $F=\overline{S}+C_n$ if $Z=H$	F/2→Y (3)	Input	Input	Parity	Hold	Z	Z	L
6	L	0	Two's Complement Multiply, Last Cycle	$F=S+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	Log F/2→Y (2)	Z	Input	F_0	Log Q/2→Q	Input	Q_0	L
7	L	0	BCD Divide by Two	(4)	F→Y	Input	Input	Parity	Hold	Z	Z	L
8	L	0	Single Length Normalize	$F=S+C_n$	F→Y	F_{15}	F_{15}	Z	Log 2Q→Q	Q_{15}	Input	L
9	L	0	Binary-to-BCD Conversion	(5)	Log 2F→Y	F_{15}	F_{15}	Input	Log 2Q→Q	Q_{15}	Input	L
9	H	0	Multiprecision Binary-to-BCD	(5)	Log 2F→Y	F_{15}	F_{15}	Input	Hold	Z	Input	L
A	L	0	Double Length Normalize and First Divide Op	$F=S+C_n$	Log 2F→Y	R_{15} V F_{15}	F_{15}	Input	Log 2Q→Q	Q_{15}	Input	L
B	L	0	BCD Add	$F=R+S+C_n$ BCD (6)	F→Y	0	0	Z	Hold	Z	Z	L
C	L	0	Two's Complement Divide	$F=S+R+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	Log 2F→Y	R_{15} V F	F_{15}	Input	Log 2Q→Q	Q_{15}	Input	L
D	L	0	BCD Subtract	$F=R-S-1+C_n$ BCD (6)	F→Y	0	0	Z	Hold	Z	Z	L
E	L	0	Two's Complement Divide Correction and Remainder	$F=S+R+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	F→Y	F_{15}	F_{15}	Z	Log 2Q→Q	Q_{15}	Input	L
F	L	0	BCD Subtract	$F=R-S-1+C_n$BCD (6)	F→Y	0	0	Z	Hold	Z	Z	L

NOTES:

1. At the most significant slice only, the C_{n+16} signal is internally gated to the Y output.
2. At the most significant slice only, $F_{15} \oplus$ OVR is internally gated to the Y output.
3. At the most significant slice only, $S_{15} \oplus F_{15}$ is generated the Y output.
4. On each nibble, F = S if magnitude of S is less than 8, and F = S minus three if magnitude of S is 8 or greater.
5. On each nibble, F = S if magnitude of S is less than 5, and F = S plus three if magnitude of S is 5 or greater. Addition is modulo 16.
6. Additions and Subtractions are BCD adds and subtracts. Results are undefined if R or S are not in valid BCD format.
7. The Q register cannot be used explicitly as an operand for any Special Functions. It is defined implicitly within the functions.
8. BCD Nibble propagate: $\overline{PN}_I = (\overline{P}_{4I+0} + \overline{P}_{4I+3})(\overline{P}_{4I+0} + \overline{G}_{4I+2})(\overline{P}_{4I+0} + \overline{G}_{4I+1} + \overline{P}_{4I+2})$
   BCD Slice propage: $P = PN_3\ PN_2\ PN_1\ PN_0$
9. BCD Nibble generate: $\overline{GN}_I = \overline{G}_{4I+3}(\overline{G}_{4I+0} + \overline{G}_{4I+1} + \overline{P}_{4I+2})(\overline{G}_{4I+0} + \overline{G}_{4I+1})(\overline{P}_{4I+1} + \overline{G}_{4I+2})(\overline{P}_{4I+3} + \overline{P}_{4I+1} \cdot \overline{P}_{4I+2} \cdot \overline{G}_{4I+0})$
   BCD Slice generate: $G = GN_3 \vee GN_2\,PN_3 \vee GN_1\,PN_2\,PN_3 \vee GN_0\,PN_1\,PN_2\,PN_3$

L = LOW LB = Lower Byte $\oplus$ = Exclusive OR
H = HIGH UB = Upper Byte Parity = $SIO_{15} \oplus F_{15} \oplus F_{14} \oplus F_{13} \oplus \ldots\ldots \oplus F_0$
Z = High Impedance

Table 6a. IDT49C403 Status Outputs (Word Mode)

HEX $I_8\ I_7\ I_6\ I_5$	HEX $I_4\ I_3\ I_2\ I_1$	I_0	G_I (I=0 to 15)	P_I (I=0 to 15)	C_{n+15}	$\overline{P}$/OVR MSS/SA	$\overline{P}$/OVR OTHER SLICES	$\overline{G}$/N MSS/SA	$\overline{G}$/N OTHER SLICES	Z ($\overline{OEY}$ = L) MSS	Z ($\overline{OEY}$ = L) ISS	Z ($\overline{OEY}$ = L) LSS	Z ($\overline{OEY}$ = L) SA
X	0	H	0	1	0	0	0	F_{15}	$\overline{G}$	f (Y)	f (Y)	f (Y)	f (Y)
X	1	X	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee Si$	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	2	X	$\overline{Ri} \wedge Si$	$Ri \vee Si$	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	3	X	$\overline{Ri} \wedge Si$	$Ri \vee Si$	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	4	X	0	Si	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	5	X	0	$\overline{Si}$	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	6	X	0	Ri	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	7	X	0	$\overline{Ri}$	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	8	H	0	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	9	X	$\overline{Ri} \wedge Si$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	A	X	$Ri \wedge Si$	$Ri \vee Si$	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	B	X	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee Si$	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	C	X	$Ri \wedge Si$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	D	X	$\overline{Ri} \wedge \overline{Si}$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	E	X	$Ri \wedge Si$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	F	X	$\overline{Ri} \wedge \overline{Si}$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
0	0	L	0 if Z=L $Ri \wedge Si$ if Z=H	Si if Z=L $Ri \vee Si$ if Z=H	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Input	Input	Q_0	Q_0
1	0	L	0	Si	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
1	8	L	0	Si	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
2	0	L	0 if Z=L $Ri \wedge Si$ if Z=H	Si if Z=L $Ri \vee Si$ if Z=H	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Input	Input	Q_0	Q_0
3	0	L	(6)	(7)	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
4	0	L	(1)	(2)	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
4	8	L	(1)	(2)	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f(Y)	f(Y)	f(Y)
5	0	L	0	Si if Z=L $\overline{Si}$ if Z=H	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15} if Z=L $F_{15} \forall S_{15}$ if Z=H	$\overline{G}$	S_{15}	Input	Input	S_{15}
6	0	L	0 if Z=L $\overline{Ri} \wedge Si$ if Z=H	Si if Z=L $\overline{Ri} \vee Si$ if Z=H	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Input	Input	Q_0	Q_0
7	0	L	0	Si	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
8	0	L	0	Si	(4)	$Q_2 \forall Q_1$	$\overline{P}$	Q_{15}	$\overline{G}$	f (Q)	f (Q)	f (Q)	f (Q)
9	0	L	0	Si	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f (Q)	f (Q)	f (Q)	f (Q)
9	8	L	0	Si	0	0	0	F_{15}	$\overline{G}$	f (Q)	f (Q)	f (Q)	f (Q)
A	0	L	0	Si	(3)	$F_2 \forall F_1$	$\overline{P}$	F_{15}	$\overline{G}$	(5)	(5)	(5)	(5)
B	0	L	$Ri \wedge Si$	$Ri \vee Si$	$G \vee PC_n$	(8)	(8)	F_{15}	(9)	f(Y)	f (Y)	f (Y)	f (Y)
C	0	L	$Ri \wedge Si$ if Z=L $\overline{Ri} \wedge Si$ if Z=H	$Ri \vee Si$ if Z=L $\overline{Ri} \vee Si$ if Z=H	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Sign Compare FF Output	Input	Input	Sign Compare FF Output
D	0	L	$Ri \wedge \overline{Si}$	$Ri \vee \overline{Si}$	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	(8)	F_{15}	(9)	f(Y)	f (Y)	f (Y)	f (Y)
E	0	L	$Ri \wedge Si$ if Z=L $\overline{Ri} \wedge Si$ if Z=H	$Ri \vee Si$ if Z=L $\overline{Ri} \vee Si$ if Z=H	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Sign Compare FF Output	Input	Input	Sign Compare FF Output
F	0	L	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee Si$	$G \vee PC_n$	$C_{n+15} \forall C_{n+16}$	(8)	F_{15}	(9)	f(Y)	f (Y)	f (Y)	f (Y)

Continued next page

8

NOTES:
1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3,\ldots}, 15 = 0$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3,\ldots,15} = 0$
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3,\ldots}, 15 = S_{1,2,3,\ldots,15}$. If $\overline{LSS}$ is HIGH, $P_I = S_I$
3. At the most significant slice, $C_{n+16} = Q_{15} \veebar Q_{14}$. At other slices $C_{n+16} = G \vee PC_n$
4. At the most significant slice, $C_{n+16} = F_{15} \veebar F_{14}$. At other slices $C_{n+16} = G \vee PC_n$
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3 \ldots \overline{Q}_{15}\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3 \ldots \overline{F}_{15}$
6. If $\overline{LSS}$ is LOW, $G_0 = {}_0$ and $G_{1,2,3,\ldots,15} = S_{1,2,3,\ldots,15}$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3,\ldots,15} = S_{0,1,2,3,\ldots,15}$
7. If $\overline{LSS}$ is LOW, $P_0 = S_0$ and $P_{1,2,3,\ldots,15} = 1$. If $\overline{LSS}$ is HIGH, $P_{0,1,2,3,\ldots,15} = 1$
8. BCD Nibble propagate: $\overline{PN}_I = (\overline{P}_{4I+0} + \overline{P}_{4I+3})(\overline{P}_{4I+0} + \overline{G}_{4I+2})(\overline{P}_{4I+0} + \overline{G}_{4I+1} + \overline{P}_{4I+2})$
   BCD Slice propage: $P = PN_3\ PN_2\ PN_1\ PN_0$
9. BCD Nibble generate: $\overline{GN}_I = \overline{G}_{4I+3}(\overline{G}_{4I+0} + \overline{G}_{4I+1} + \overline{P}_{4I+2})(\overline{G}_{4I+0} + \overline{G}_{4I+1})(\overline{P}_{4I+1} + \overline{G}_{4I+2})(\overline{P}_{4I+3} + \overline{P}_{4I+1} \cdot \overline{P}_{4I+2} \cdot \overline{G}_{4I+0})$
   BCD Slice generate: $G = GN_3 \vee GN_2\ PN_3 \vee GN_1\ PN_2\ PN_3 \vee GN_0\ PN_1\ PN_2\ PN_3$

$\vee$ = OR
$\wedge$ = AND
$\veebar$ = Exclusive-OR
$P = P_{15}P_{14} \ldots\ldots P_3P_2P_1P_0$
$G = G_{15} \vee G_{14}P_{15} \vee G_{13}P_{14}P_{15} \vee G_{12}P_{13}P_{14}P_{15}$
$\vee G_{11}P_{12}P_{13}P_{14}P_{15} \vee \ldots\ldots \vee G_1P_2P_3P_4 \ldots P_{15}$

$f(Y) = \overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3 \ldots\ldots \overline{Y}_{15}$
$f(Q) = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3 \ldots\ldots \overline{Q}_{15}$
L = LOW = 0
H = HIGH = 1

Table 6b. IDT49C403 Status Outputs (Byte Mode)

HEX $I_8\ I_7\ I_6\ I_5$	HEX $I_4\ I_3\ I_2\ I_1$	I	Q_I (I=0 to 7)	P_I (I=0 to 7)	C_{n+7}	$\overline{P}$/OVR		$\overline{G}$/N		Z ($\overline{OEY}$ = L)			
						MSS/SA	OTHER SLICES	MSS/SA	OTHER SLICES	MS	ISS	LSS	SA
X	0	H	0	1	0	0	0	F_7	$\overline{G}$	f (Y)	f (Y)	f (Y)	f (Y)
X	1	X	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee Si$	$G \vee PC_n$	$C_{n+7} \veebar C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	2	X	$\overline{Ri} \wedge Si$	$Ri \vee SI$	$G \vee PC_n$	$C_{n+7} \veebar C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	3	X	$\overline{Ri} \wedge Si$	$Ri \vee Si$	$G \vee PC_n$	$C_{n+7} \veebar C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	4	X	0	Si	$G \vee PC_n$	$C_{n+7} \veebar C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	5	X	0	$\overline{Si}$	$G \vee PC_n$	$C_{n+7} \veebar C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	6	X	0	Ri	$G \vee PC_n$	$C_{n+7} \veebar C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	7	X	0	$\overline{Ri}$	$G \vee PC_n$	$C_{n+7} \veebar C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	8	H	0	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	9	X	$\overline{Ri} \wedge Si$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	A	X	$Ri \wedge Si$	$Ri \vee Si$	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	B	X	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee Si$	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	C	X	$Ri \wedge Si$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	D	X	$\overline{Ri} \wedge \overline{Si}$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	E	X	$Ri \wedge Si$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	F	X	$\overline{Ri} \wedge \overline{Si}$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)

NOTES:
$f(Y) = \overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3 \ldots\ldots \overline{Y}_7$
$f(Q) = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3 \ldots\ldots \overline{Q}_7$
L = LOW = 0
H = HIGH = 1

$\vee$ = OR
$\wedge$ = AND
$\veebar$ = Exclusive OR
$P = P_7P_6 \ldots\ldots P_3P_2P_1P_0$
$G = G_7 \vee G_6P_7 \vee G_5P_6P_7 \vee G_4P_5P_6P_7$
$\vee G_3P_4P_5P_6P_7 \vee \ldots\ldots \vee G_1P_2P_3P_4 \ldots P_7$

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level			2.0	–	–	V
V_{IL}	Input LOW Level			–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0V		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -6mA MIL.	2.4	4.3	–	
			I_{OH} = -8mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 12mA MIL.	–	0.3	0.5	
			I_{OL} = 16mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	–	-10	µA
			V_O = V_{CC} (max.)	–	–	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V (3)		-15	–	–	mA

NOTES:
1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = H		–	150	250	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = L		–	50	100	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		–	0.3	0.5	mA/Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	3.6	7.7	mA/MHz
			COM'L.	–	3.6	5.2	
I_{CC}	Total Power Supply Current (6)	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$	MIL.	–	136	252	mA
			COM'L.	–	136	227	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	150	275	
			COM'L.	–	150	250	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{CP} = Clock input frequency.

IDT49C403A GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT49C403A over the commercial operating range of 0 to +70°C with V_{CC} from 4.75 to 5.25V, and over the military operating range of -55 to +125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with input switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Table 7. Clock and Write Pulse Characteristics All Functions

	COM'L.	MIL.	UNIT
Minimum Clock Low Time	10	11	ns
Minimum Clock High Time	10	11	ns
Minimum Time CP and WE both Low to Write	10	11	ns

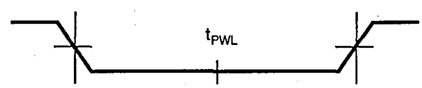
Table 8. Enable/Disable Times All Functions

FROM	TO	ENABLE COM'L.	ENABLE MIL.	DISABLE COM'L.	DISABLE MIL.	UNIT
$\overline{OE}_Y$	Y	12	13	10	11	ns
$\overline{OE}_B$	DB	14	15	12	13	ns
$\overline{EA}$	DA	15	16	13	14	ns
I_8	SIO	23	25	12	13	ns
I_8	QIO	16	17	21	22	ns
$I_{8,7,6,5}$	QIO	17	18	19	20	ns
$I_{4,3,2,1,0}$	QIO	21	22	19	20	ns

NOTE:

C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Table 9. Set-up and Hold Times All Functions



FROM	WITH RESPECT TO	SET-UP COM'L.	SET-UP MIL.	HOLD COM'L.	HOLD MIL.	SET-UP COM'L.	SET-UP MIL.	HOLD COM'L.	HOLD MIL.	UNIT	COMMENTS
Y	CP	–	–	–	–	8	9	2	2	ns	Store Y in RAM/Q (1)
$\overline{WE}$ HIGH	CP	7	8	2	2	–	–	2	2	ns	Prevent Writing
$\overline{WE}$ LOW	CP	–	–	–	–	10	11	0	0	ns	Write into RAM
A, B Source	CP	11	12	2	2	–	–	–	–	ns	Latch Data from RAM Out
B Destination (3)	CP	6	7	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
B Destination (3)	$\overline{IEN}$	6	7	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
B Destination (3)	$\overline{WE}$	6	7	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
$QIO_{0,15}$	CP	–	–	–	–	5	6			ns	Shift Q
$I_{8,7,6,5}$	CP	–	–	–	–	23	25	0	0	ns	Write into Q and RAM (2)
$\overline{IEN}$ HIGH (3)	CP	7	8	(3)		–	–			ns	Prevent Writing into Q and RAM (2)
$\overline{IEN}$ LOW (3)	CP	–	–	–	–	10	11			ns	Write into Q and RAM
$I_{4,3,2,1,0}$	CP	–	–	–	–	16	18			ns	Write into Q and RAM (2)
Q_0, Q_1	CP	–	–	–	–	8	9	2	2	ns	Write into Q
C_n	CP	–	–	–	–	28	30	0	0	ns	ALU Carry In to RAM

NOTES:

1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = 0)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. The writing of data is controlled by CP, $\overline{IEN}$, and $\overline{WE}$; all must be LOW in order to write. The set-up time of B destination address is with respect to the last of these three inputs to go LOW, and the hold time is with respect to the first to go HIGH.
4. A "–" implies this path does not exist.

IDT49C403A GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE STANDARD AND INCREMENT/DECREMENT BY ONE OR TWO INSTRUCTIONS (SF3, SF4)

FROM	SLICE	TO: Y		C_{n+16}		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0, 15}$		SIO_0		SIO_{15}		SIO_0 PARITY		UNIT
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	MSS	41	44	44	47	—	—	42	45	47	50	47	50	26	28	—	—	—	—	41	44	40	43	52	56	ns
	IS					44	47			—	—	—	—													
	LSS					44	47			—	—	—	—													
	SA					—	—			47	50	47	50													
DA, DB	MSS	34	36	28	30	—	—	29	31	36	38	34	36	—	—	—	—	—	—	24	26	27	29	46	49	ns
	IS					28	30			—	—	—	—													
	LSS					28	30			—	—	—	—													
	SA					—	—			36	38	34	36													
C_n	MSS	27	29	15	16	—	—	22	24	26	28	23	25	—	—	—	—	—	—	24	26	26	28	26	28	ns
	IS					—	—			—	—	—	—													
	LSS					—	—			—	—	—	—													
	SA					—	—			26	28	23	25													
I_{8-0}	MSS	38	41	32	34	—	—	48	51	36	38	42	45	—	—	18	19	24	26	28	30	37	39	41	44	ns
	IS					23	34			—	—	—	—													
	LSS					23	34			—	—	—	—													
	SA					—	—			36	38	42	45													
CP	MSS	43	46	44	47	—	—	39	42	51	55	54	58	20	22	—	—	26	28	36	39	37	39	41	44	ns
	IS					39	42			—	—	—	—													
	LSS					39	42			—	—	—	—													
	SA					—	—			51	55	54	58													
$\overline{MSS}$	Any	21	23	—	—	21	23	38	41	21	23	20	22	—	—	—	—	—	—	—	—	20	22	—	—	ns
SIO_{0-15}	Any	21	23	—	—	—	—	17	18	—	—	—	—	—	—	—	—	—	—			19	20	16	17	ns

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	SLICE	TO: Y		C_{n+16}		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0, 15}$		SIO_0		UNIT
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	MSS					—	—	—	—							—	—	—	—			ns
	IS									—	—	—	—									
	LSS									—	—	—	—									
	SA					—	—															
DA, DB	MSS					—	—	—	—					—	—	—	—	—	—			ns
	IS									—	—	—	—									
	LSS									—	—	—	—									
	SA					—	—															
C_n	MSS					—	—	—	—					—	—	—	—	—	—			ns
	IS					—	—			—	—	—	—									
	LSS					—	—			—	—	—	—									
	SA					—	—															
I_{8-0}	MSS					—	—	—	—					—	—							ns
	IS							—	—	—	—	—	—									
	LSS									—	—	—	—									
	SA					—	—	—	—													
CP	MSS					—	—	—	—							—	—					ns
	IS							—	—	—	—	—	—									
	LSS									—	—	—	—									
	SA					—	—															
Z ($\overline{OE}_Y$ = low)	MSS	47	48			—	—							—	—	—	—	—	—			ns
	IS									—	—	—	—									
	LSS	—	—	—	—	—	—			—	—	—	—							—	—	
	SA	—	—	—	—	—	—													—	—	
SIO_{0-15}	Any			—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ns

Unsigned Multiply

SF 0: $F=S+C_n$ if $Z=L$
$F=S+R+C_n$ if $Z=H$
$Y15=C_n+16$ (MSS)
$Z=Q0$ (LSS)
$Y=Log\ F/2$
$Q=Log\ Q/2$

Two's Complement Multiply

SF 2: $F=S+C_n$ if $Z=L$
$F=S+R+C_n$ if $Z=H$
$Y15=F15 \vee OVR$ (MSS)
$Z=Q0$ (LSS)
$Y=Log\ F/2$
$Q=Log\ Q/2$

Two's Complement Multiply Last Cycle

SF 2: $F=S+C_n$ if $Z=L$
$F=S-R-1+C_n$ if $Z=H$
$Y15=OVR \vee F15$ (MSS)
$Z=Q0$ (LSS)
$Y=Log\ F/2$
$Q=Log\ Q/2$

A '—' implies that particular data path is not valid.

IDT49C403A GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE BCD INSTRUCTIONS (SF1, SF7, SF9, SFB, SFD, SFF)

		TO																										
FROM	SLICE	Y		C_{n+16}		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0, 15}$		SIO_0		SIO_{15}		SIO_0 PARITY		UNIT
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	MSS IS LSS SA																									ns
DA, DB	MSS IS LSS SA																									ns
C_n	MSS IS LSS SA																									ns
I_{8-0}	MSS IS LSS SA																									ns
CP	MSS IS LSS SA																									ns
Z ($\overline{OE}_Y$ = low)	MSS IS LSS SA																									ns
SIO_{0-15}	Any																									ns

NOTE:
1. Binary to BCD and multiprecision Binary to BCD instructions only

BCD to Binary conversion (SF 1) Binary to BCD conversion (SF 9) BCD substract (SF F)
BCD divide by two (SF 7) BCD add (SF B)

SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

		TO																				
FROM	SLICE	Y		C_{n+16}		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0, 15}$		SIO_0		UNIT
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	MSS IS LSS SA																					ns
DA, DB	MSS IS LSS SA																					ns
C_n	MSS IS LSS SA																					ns
I_{8-0}	MSS IS LSS SA																					ns
CP	MSS IS LSS SA																					ns
Z ($\overline{OE}_Y$ = low)	MSS IS LSS SA																					ns
SIO_{0-15}	Any																					ns

SF 5: $F = S + C_n$ if $Z = L$ $Y = F$
$F = S + C_n$ if $Z = H$ $Q = Q$
$Y15 = S15 \forall F15$ (MSS) $N = F15$; $Z = L$
$Z = S15$ (MSS) $N = F15 \forall S15$; $Z = H$

IDT49C403A GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SFA, SFC, SFE) AND SINGLE LENGTH NORMALIZATION (SFB)

FROM	SLICE	TO: Y		C_{n+16}		$\overline{G}, \overline{P}$		Z		N		OVR		SIO_0		DA, DB		$QIO_{0,15}$		$\overline{WRITE}$		UNIT
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	MSS IS LSS SA																					ns
DA, DB	MSS IS LSS SA																					ns
C_n	MSS IS LSS SA																					ns
I_{8-0}	MSS IS LSS SA																					ns
CP	MSS IS LSS SA																					ns
Z ($\overline{OE}_Y$ = low)	MSS IS LSS SA																					ns
SIO_{0-15}	Any																					ns

NOTES:
1. Only 1st divide and normalization
2. Only two's complement divide and two's complement divide correction

Double Length Normalize and First Divide Op

SFA: $F = S + C_n$
$N = F15$ (MSS)
$SIO15 = F15 \veebar R15$ (MSS)
$C_n + 16 = F15 \veebar F14$ (MSS)
$OVR = F2 \veebar F1$ (MSS)
$Z = Q0\ Q1\ Q2\ Q3 \ldots Q15\ F0\ F1\ F2\ F3 \ldots F15$
$Y = \text{Log } 2F$
$Q = \text{Log } 2Q$

Two's Complement Divide

SFC: $F = S + R + C_n$ if $Z = L$
$F = S - R - 1 + C_n$ if $Z = H$
$SIO15 = F15 \veebar R15$ (MSS)
$Z = F15 \veebar R15$ (MSS) from previous cycle
$Y = \text{Log } 2F$
$Q = \text{Log } 2Q$

Two's Complement Divide Correction and Remainder

SF2: $S = C_n$ if $Z = L$
$S - R - 1 + C_n$ if $Z = H$
$Z = F15 \veebar R15$ (MSS) from previous cycle
$Y = F$
$Q = \text{Log } 2Q$

IDT49C403 GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT49C403 over the commercial operating range of 0 to 70°C with V_{CC} from 4.75 to 5.25V, and over the military operating range of -55 to +125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with input switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Table 10. Clock and Write Pulse Characteristics All Functions

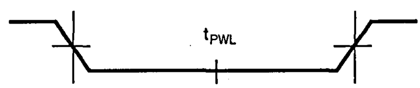
	COM'L.	MIL.	UNIT
Minimum Clock Low Time	12	13	ns
Minimum Clock High Time	12	13	ns
Minimum Time CP and WE both Low to Write	12	13	ns

Table 11. Enable/Disable Times All Functions

FROM	TO	ENABLE COM'L.	MIL.	DISABLE COM'L.	MIL.	UNIT
$\overline{OE}_Y$	Y	15	16	12	13	ns
$\overline{OE}_B$	DB	17	18	15	16	ns
$\overline{EA}$	DA	18	19	16	17	ns
I_8	SIO	28	30	15	16	ns
I_8	QIO	20	21	25	27	ns
$I_{8,7,6,5}$	QIO	21	22	22	24	ns
$I_{4,3,2,1,0}$	QIO	25	27	22	24	ns

NOTE:
C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Table 12. Set-up and Hold Times All Functions



FROM	WITH RESPECT TO	SET-UP COM'L.	MIL.	HOLD COM'L.	MIL.	SET-UP COM'L.	MIL.	HOLD COM'L.	MIL.	UNIT	COMMENTS
Y	CP	–	–	–	–	10	11	2	2	ns	Store Y in RAM/Q (1)
$\overline{WE}$ HIGH	CP	8	9	2	2	–	–	2	2	ns	Prevent Writing
$\overline{WE}$ LOW	CP	–	–	–	–	12	13	0	0	ns	Write into RAM
A, B Source	CP	14	15	2	2	–	–	–	–	ns	Latch Data from RAM Out
B Destination (3)	CP	7	8	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
B Destination (3)	$\overline{IEN}$	7	8	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
B Destination (3)	$\overline{WE}$	7	8	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
$QIO_{0,15}$	CP	–	–	–	–	6	7			ns	Shift Q
$I_{8,7,6,5}$	CP	–	–	–	–	27	30	0	0	ns	Write into Q and RAM (2)
$\overline{IEN}$ HIGH (3)	CP	8	9	(3)	(3)	(3)	(3)			ns	Prevent Writing into Q and RAM (2)
$\overline{IEN}$ LOW (3)	CP	–	–	–	–	10	11			ns	Write into Q and RAM
$I_{4,3,2,1,0}$	CP	–	–	–	–	19	21			ns	Write into Q and RAM (2)
Q_0, Q_1	CP	–	–	–	–	10	11	2	2	ns	Write into Q
C_n	CP	–	–	–	–	34	36	0	0	ns	ALU Carry In to RAM

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$= 0)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. The writing of data is controlled by CP, $\overline{IEN}$, and $\overline{WE}$; all must be LOW in order to write. The set-up time of B destination address is with respect to the last of these three inputs to go LOW, and the hold time is with respect to the first to go HIGH.
4. A "–" implies this path does not exist.

IDT49C403A GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE STANDARD AND INCREMENT/DECREMENT BY ONE OR TWO INSTRUCTIONS (SF3, SF4)

FROM	SLICE	TO: Y Com'l.	Y Mil.	C_{n+16} Com'l.	C_{n+16} Mil.	$\overline{G}, \overline{P}$ Com'l.	$\overline{G}, \overline{P}$ Mil.	Z Com'l.	Z Mil.	N Com'l.	N Mil.	OVR Com'l.	OVR Mil.	DA, DB Com'l.	DA, DB Mil.	$\overline{WRITE}$ Com'l.	$\overline{WRITE}$ Mil.	$QIO_{0, 15}$ Com'l.	$QIO_{0, 15}$ Mil.	SIO_0 Com'l.	SIO_0 Mil.	SIO_{15} Com'l.	SIO_{15} Mil.	SIO_0 PARITY Com'l.	SIO_0 PARITY Mil.	UNIT
A, B Addr	MSS	49	53	53	57	–	–	50	54	56	60	56	60	32	34	–	–	–	–	50	53	48	52	63	67	ns
	IS					53	57			–	–	–	–													
	LSS					53	57			–	–	–	–													
	SA					–	–			56	60	56	60													
DA, DB	MSS	40	43	34	36	–	–	35	37	43	46	40	43	–	–	–	–	–	–	29	31	33	35	55	59	ns
	IS					34	36			–	–	–	–													
	LSS					34	36			–	–	–	–													
	SA					–	–			43	46	40	43													
C_n	MSS	33	35	18	19	–	–	27	29	32	34	28	30	–	–	–	–	–	–	29	31	32	34	32	34	ns
	IS					–	–			–	–	–	–													
	LSS					–	–			–	–	–	–													
	SA					–	–			32	34	28	30													
I_{8-0}	MSS	46	49	39	41	–	–	56	59	43	46	51	54	–	–	21	23	29	32	34	36	45	47	49	53	ns
	IS					39	41			–	–	–	–													
	LSS					39	41			–	–	–	–													
	SA					–	–			43	46	51	54													
CP	MSS	51	55	53	56	–	–	47	51	62	66	65	70	24	26	–	–	32	34	43	46	45	47	49	53	ns
	IS					47	51			–	–	–	–													
	LSS					47	51			–	–	–	–													
	SA					–	–			62	66	65	70													
$\overline{MSS}$	Any	26	28	–	–	26	28	46	50	26	28	24	26	–	–	–	–	–	–	–	–	24	26	–	–	ns
SIO_{0-15}	Any	25	27	–	–	–	–	20	21	–	–	–	–	–	–	–	–	–	–			23	24	19	20	ns

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	SLICE	TO: Y Com'l.	Y Mil.	C_{n+16} Com'l.	C_{n+16} Mil.	$\overline{G}, \overline{P}$ Com'l.	$\overline{G}, \overline{P}$ Mil.	Z Com'l.	Z Mil.	N Com'l.	N Mil.	OVR Com'l.	OVR Mil.	DA, DB Com'l.	DA, DB Mil.	$\overline{WRITE}$ Com'l.	$\overline{WRITE}$ Mil.	$QIO_{0, 15}$ Com'l.	$QIO_{0, 15}$ Mil.	SIO_0 Com'l.	SIO_0 Mil.	UNIT
A, B Addr	MSS					–	–	–	–							–	–	–	–			ns
	IS									–	–	–	–									
	LSS									–	–	–	–									
	SA					–	–															
DA, DB	MSS					–	–	–	–					–	–	–	–	–	–			ns
	IS									–	–	–	–									
	LSS									–	–	–	–									
	SA					–	–															
C_n	MSS					–	–	–	–					–	–	–	–	–	–			ns
	IS					–	–			–	–	–	–									
	LSS					–	–			–	–	–	–									
	SA					–	–															
I_{8-0}	MSS					–	–	–	–					–	–							ns
	IS							–	–	–	–	–	–									
	LSS									–	–	–	–									
	SA					–	–	–	–													
CP	MSS					–	–	–	–							–	–					ns
	IS							–	–	–	–	–	–									
	LSS									–	–	–	–									
	SA					–	–															
Z ($\overline{OE}_Y$ = low)	MSS	65	70			–	–							–	–	–	–	–	–			ns
	IS									–	–	–	–									
	LSS	–	–	–	–	–	–			–	–	–	–							–	–	
	SA	–	–	–	–	–	–													–	–	
SIO_{0-15}	Any			–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

Unsigned Multiply
SF 0: $F=S+C_n$ If $Z=L$
$F=S+R+C_n$ If $Z=H$
$Y15=C_n+16$ (MSS)
$Z=Q0$ (LSS)
$Y=\text{Log } F/2$
$Q=\text{Log } Q/2$

Two's Complement Multiply
SF 2: $F=S+C_n$ If $Z=L$
$F=S+R+C_n$ If $Z=H$
$Y15=F15 \text{ V } OVR$ (MSS)
$Z=Q0$ (LSS)
$Y=\text{Log } F/2$
$Q=\text{Log } Q/2$

Two's Complement Multiply Last Cycle
SF 2: $F= S+C_n$ If $Z=L$
$F=S-R-1+C_n$ If $Z=H$
$Y15=OVR \text{ V } F15$ (MSS)
$Z=Q0$ (LSS)
$Y=\text{Log } F/2$
$Q=\text{Log } Q/2$

A '–' implies that particular data path is not valid.

IDT49C403 GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE BCD INSTRUCTIONS (SF1, SF7, SF9, SFB, SFD, SFF)

FROM	SLICE	TO																								UNIT
		Y		C_{n+16}		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		SIO_{15}		SIO_0 PARITY		
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	MSS IS LSS SA																									ns
DA, DB	MSS IS LSS SA																									ns
C_n	MSS IS LSS SA																									ns
I_{8-0}	MSS IS LSS SA																									ns
CP	MSS IS LSS SA																									ns
Z ($\overline{OE}_Y$ = low)	MSS IS LSS SA																									ns
SIO_{0-15}	Any																									ns

NOTE:
1. Binary to BCD and multiprecision Binary to BCD instructions only

BCD to Binary conversion (SF1)
BCD divide by two (SF7)
Binary to BCD conversion (SF9)
BCD add (SFB)
BCD substract (SFF)

SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	SLICE	TO																				UNIT
		Y		C_{n+16}		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	MSS IS LSS SA																					ns
DA, DB	MSS IS LSS SA																					ns
C_n	MSS IS LSS SA																					ns
I_{8-0}	MSS IS LSS SA																					ns
CP	MSS IS LSS SA																					ns
Z ($\overline{OE}_Y$ = low)	MSS IS LSS SA																					ns
SIO_{0-15}	Any																					ns

SF 5: $F = S + C_n$ if $Z = L$
$F = S + C_n$ if $Z = H$
$Y15 = S15 \forall F15$ (MSS)
$Z = S15$ (MSS)
$Y = F$
$Q = Q$
$N = F15$; $Z = L$
$N = F15 \forall S15$; $Z = H$

IDT49C403 GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SFA, SFC, SFE) AND SINGLE LENGTH NORMALIZATION (SFB)

		TO																				
FROM	SLICE	Y		C_{n+16}		$\overline{G}, \overline{P}$		Z		N		OVR		SIO_0		DA, DB		$QIO_{0,15}$		$\overline{WRITE}$		UNIT
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	MSS IS LSS SA																					ns
DA, DB	MSS IS LSS SA																					ns
C_n	MSS IS LSS SA																					ns
I_{8-0}	MSS IS LSS SA																					ns
CP	MSS IS LSS SA																					ns
Z ($\overline{OE}_Y$ = low)	MSS IS LSS SA																					ns
SIO_{0-15}	Any																					ns

NOTES:

1. Only 1st divide and normalization
2. Only two's complement divide and two's complement divide correction

Double Length Normalize and First Divide Op

SFA: F = S + Cn
N = F15 (MSS)
SIO15 = F15 $\forall$ R15 (MSS)
Cn+16 = F15 $\forall$ F14 (MSS)
OVR = F2 $\forall$ F1 (MSS)
Z = Q0 Q1 Q2 Q3 . . . Q15 F0 F1 F2 F3 . . . F15
Y = Log 2F
Q = Log 2Q

Two's Complement Divide

SFC: F = S + R + Cn If Z = L
F = S - R - 1 + Cn If Z = H
SIO15 = F15 $\forall$ R15 (MSS)
Z = F15 $\forall$ R15 (MSS) from previous cycle
Y = Log 2F
Q = Log 2Q

Two's Complement Divide Correction and Remainder

SF2: S = Cn If Z = L
S - R - 1 + Cn If Z = H
Z = F15 $\forall$ R15 (MSS) from previous cycle
Y = F
Q = Log 2Q

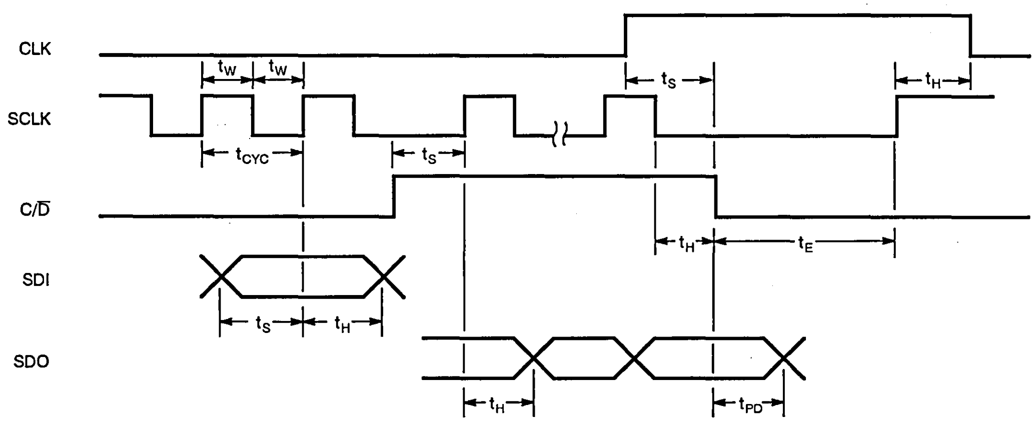


Figure 11. IDT49C403 SPC Timing Waveforms

IDT49C403/A SPC AC TIMING

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
t_{PD}	SCLK TO SDO		3	15	ns
t_{PD}	C/D̄ to SDO		3	50	ns
t_S	C/D̄ to SCLK		5	–	ns
t_S	CLK to C/D̄		20	–	ns
t_S	SDI to SCLK	R_L = 500Ω	10	–	ns
t_H	C/D̄ to SCLK	C_L = 50pF	5	–	ns
t_H	CLK to SCLK		5	–	ns
t_H	SDI to SCLK		5	–	ns
t_W	Pulse Width SCLK		20	–	ns
t_{CYC}	SCLK Period		50	–	ns
t_E	Execution, C/D̄ to SCLK		50	–	ns

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large V_{CC} current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

IDT49C403 INPUT/OUTPUT INTERFACE CIRCUITRY

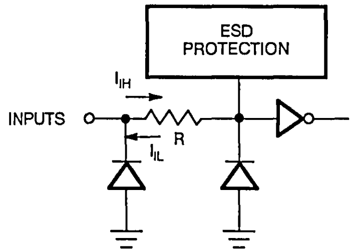


Figure 12. Input Structure (All Inputs)

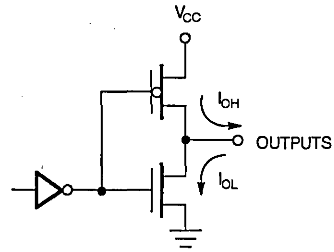


Figure 13. Output Structure (All Outputs)

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 15

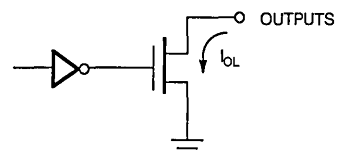
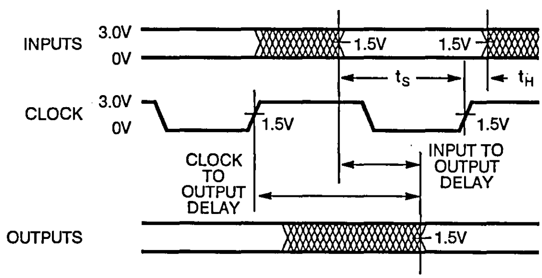


Figure 14. Open Drain Structure

SWITCHING WAVEFORMS



TEST LOAD CIRCUIT

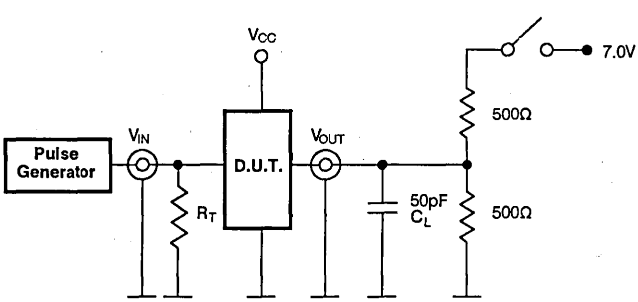


Figure 15. Test Load Circuit

TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the pulse generator

ORDERING INFORMATION

IDT 49C403 (Device Type) X (Speed) X (Package) X (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	G	Pin Grid Array
Speed	Blank	Standard Speed
	A	High Speed

Integrated Device Technology, Inc.

32-BIT CMOS MICROPROGRAM MICROPROCESSOR

ADVANCE INFORMATION
IDT49C404
IDT49C404A

MICROSLICE™ PRODUCT

FEATURES:

- High speed CMOS
  - Microcycle Time: 80ns
- Three bi-directional 32-bit data I/O ports
  - DA, DB, Y
- 64-word x 32-bit expandable 7-port register file
  - 3 input ports and 4 output ports
  - Writes 3 operands and reads 4 operands in one cycle
- 64-bit in, 32-bit out cascadable funnel shifter
  - Fast alignment to any bit boundary
- 32-bit high-speed ALU cascadable to 64 bits
  - Selects status flags from any bit boundary
- Flexible mask generator and merge logic
  - Selects bit-fields on any width, on any boundary
- Priority encoder
- Powerful orthogonal instruction set
- Built-in multiplication/division support
- Counter function
- Includes Serial Protocol Channel (SPC™)
  - Flexible on-chip diagnostics
  - Serially monitors all pin states
  - Reads and writes to Register File
- Single 5V supply
- Available in 208-pin PGA
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C404 is a cascadable, microprogrammable, high-speed CMOS 32-bit microprocessor slice. This monolithic, highly parallel, 3-port device consists of a 7-port 64-word by 32-bit working RAM, 64 bits in/32 bits out cascadable funnel shifter, high-speed multi-function 32-bit ALU and 32-bit mask generation and merge logic.

The IDT49C404 uniquely incorporates shift, ALU and merge functions into a single cycle and utilizes an orthogonal instruction set to create a highly parallel architecture that achieves added performance.

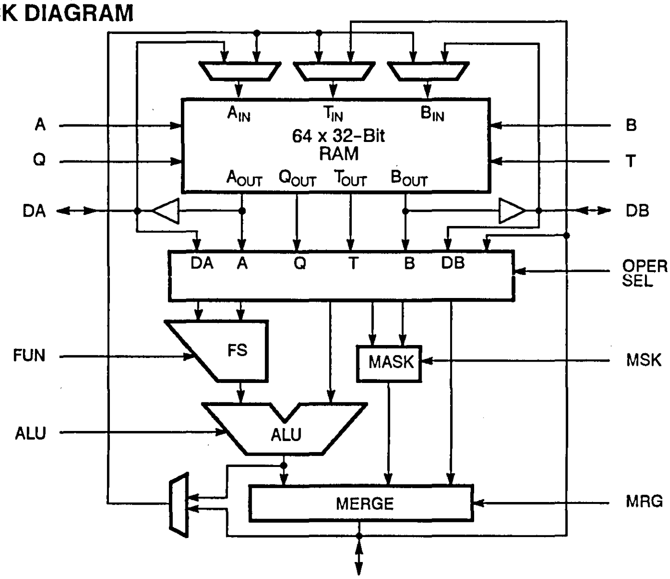
Supporting ultra-fast cycle times, the IDT49C404 offers a very-low-power CMOS alternative to existing bipolar counterparts.

This 32-bit device has been optimized, both architecturally and instruction set-wise, for use in all types of dedicated intelligent controllers such as high-speed graphics engines, array processors, fast disk and communication controllers, robotics, data base manipulation, design automation and AI.

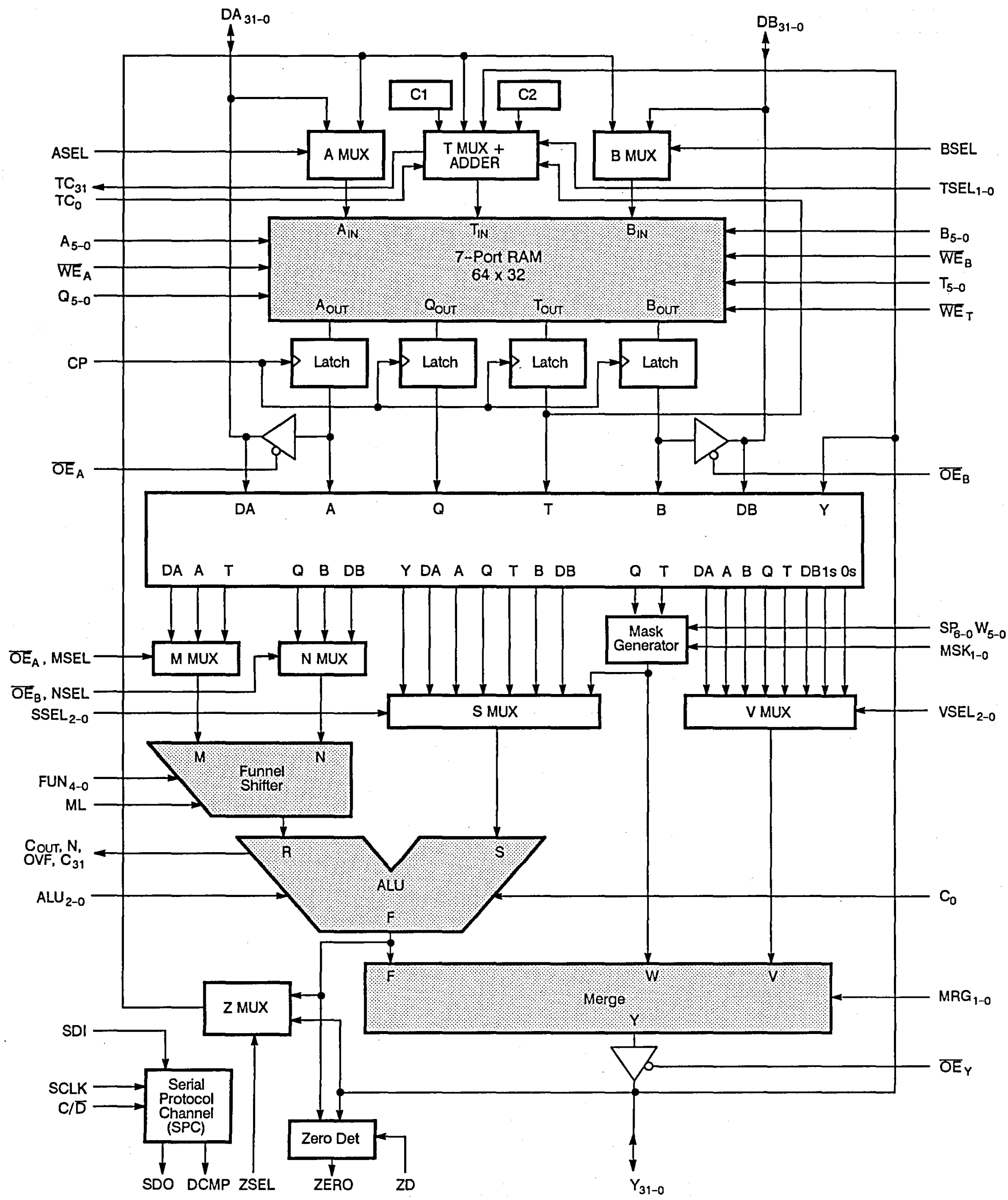
Also featured on the IDT49C404 is an innovative diagnostics capability known as Serial Protocol Channel (SPC). This on-chip feature greatly simplifies the task of writing and debugging microcode, field maintenance debug and test, along with system testing during manufacturing.

The IDT49C404 is fabricated using CEMOS™, IDT's advanced CMOS technology designed for high-performance and high-reliability. The device is packaged in a 208-lead pin grid array. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

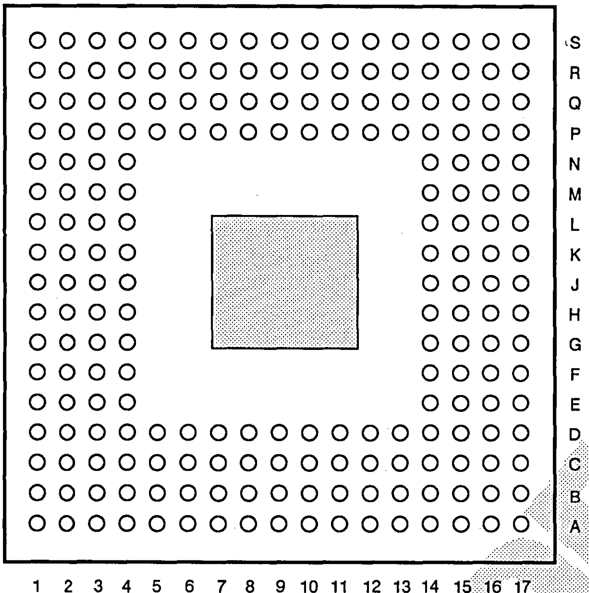
SIMPLIFIED BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



IDT49C404 PIN CONFIGURATION



PGA
BOTTOM
VIEW

TO BE DEFINED

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
A1		B1		C1		D1		E1	
A2		B2		C2		D2		E2	
A3		B3		C3		D3		E3	
A4		B4		C4		D4		E4	
A5		B5		C5		D5		E14	
A6		B6		C6		D6		E15	
A7		B7		C7		D7		E16	
A8		B8		C8		D8		E17	
A9		B9		C9		D9		F1	
A10		B10		C10		D10		F2	
A11		B11		C11		D11		F3	
A12		B12		C12		D12		F4	
A13		B13		C13		D13		F14	
A14		B14		C14		D14		F15	
A15		B15		C15		D15		F16	
A16		B16		C16		D16		F17	
A17		B17		C17		D17		G1	

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
G2		M3		Q11	
G3		M4		Q12	
G4		M14		Q13	
G14		M15		Q14	
G15		M16		Q15	
G16		M17		Q16	
G17		N1		Q17	
H1		N2		R1	
H2		N3		R2	
H3		N4		R3	
H4		N14		R4	
H14		N15		R5	
H15		N16		R6	
H16		N17		R7	
H17		P1		R8	
J1		P2		R9	
J2		P3		R10	
J3		P4		R11	
J4		P5		R12	
J14		P6		R13	
J15		P7		R14	
J16		P8		R15	
J17		P9		R16	
K1		P10		R17	
K2		P11		S1	
K3		P12		S2	
K4		P13		S3	
K14		P14		S4	
K15		P15		S5	
K16		P16		S6	
K17		P17		S7	
L1		Q1		S8	
L2		Q2		S9	
L3		Q3		S10	
L4		Q4		S11	
L14		Q5		S12	
L15		Q6		S13	
L16		Q7		S14	
L17		Q8		S15	
M1		Q9		S16	
M2		Q10		S17	

PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
DA_{31-0}	Thirty-two-bit data input/output port is under control of the signal $\overline{OE}_A$. When the $\overline{OE}_A$ is low, RAM output port A can be directly read on these lines. Data on these lines can be selected as the source for the ALU, funnel-shifter or loaded into port A of the working RAM.
DB_{31-0}	Thirty-two-bit data input/output port is under control of the signal $\overline{OE}_B$. When the $\overline{OE}_B$ is low, RAM output port B can be directly read on these lines. Data on these lines can be selected as the source for the ALU, funnel-shifter or loaded into port B of the working RAM.
Y_{31-0}	Thirty-two-bit data input/output port is under control of the signal $\overline{OE}_Y$. When $\overline{OE}_Y$ is low, the merge output can be directly read on these lines. Data on the lines can be loaded into port T of the working RAM or selected as the source for the ALU when $\overline{OE}_Y$ is high.
$\overline{OE}_Y$	A control input pin which, when low, enables the output of merge-logics on the lines Y_{31-0} and, when high, disables the Y_{31-0} three-state output buffers.
$\overline{WE}_A$	The write control signal for RAM input port A. If the signal $\overline{WE}_A$ is low, the data on the DA lines or Z bus is written into the RAM (input port A) when the clock signal is low.
$\overline{WE}_B$	The write control signal for RAM input port B. If the signal $\overline{WE}_B$ is low, the data on the DB lines or Z bus is written into the RAM (input port B) when the clock signal is low.
$\overline{WE}_T$	The write control signal for RAM input port T. If the signal $\overline{WE}_T$ is low, the data on the Z lines, Y lines, T + C1 or T + C2 is written into the RAM (input port T) when clock signal is low.
$\overline{OE}_A$	A control input for data input/output port DA. When $\overline{OE}_A$ is low, RAM output port A is read on the DA line. When $\overline{OE}_A$ is high, the data on the data lines can be selected as the source for the ALU or loaded into port A of the working RAM.
$\overline{OE}_B$	A control input for data input/output port DB. When $\overline{OE}_B$ is low, RAM output port B can be read on these lines. When is $\overline{OE}_B$ high, the data on the DB lines can be selected as the source for the ALU or loaded into port T of the working RAM.
CP	The clock input to the IDT49C404. When clock is low, data is written in the seven-port RAM.
TC_0	Used as carry input for the T counter.
TC_{31}	Used as carry output for the T counter.
ML	The input pin which can be used to load the external bit in order to fill in the vacant positions of a word in shift-linkage.
C_0	The carry input to the least significant bit of the ALU.
C_{OUT}	Indicates the carry-output.
N	Indicates the sign N of the ALU operation.
OVF	Indicates the conventional two's complement overflow.
C_{31}	The carry output pin which is used to ripple the carry in the expansion mode (64-bit).
ZERO	The open drain input/output pin which, when high, generally indicates that all outputs are low.
ALU_{2-0}	Instruction inputs are used to select the operations for the ALU.
A_{5-0}	Six RAM address inputs which contains the address of the RAM word appearing at RAM output port A and into which new data is written when $\overline{WE}_A$ is low.
B_{5-0}	Six RAM address inputs which contains the address of the RAM word appearing at RAM output port B and into which new data is written when $\overline{WE}_B$ is low.
T_{5-0}	Six RAM address inputs which contains the address of the RAM word appearing at output port T and into which new data is written under control of TSEL.
ASEL	Defines what data RAM port A receives, either DA or Z bus.
BSEL	Defines what data RAM port B receives, either DB or Z bus.
Q_{5-0}	Six RAM address inputs which contain the address of the RAM word appearing at output port Q.
SP_{6-0}	The seven pins are used to specify the start positions or the number of shift positions.
W_{5-0}	The six pins are used to specify the word width.
ZSEL	Selects the source of the Z bus between the output of the ALU (F) or the Y bus.
MSEL	Taken together with $\overline{OE}_A$, selects the source of the M input into the funnel shifter.
NSEL	Taken together with $\overline{OE}_B$, selects the source of the N input into the funnel shifter.
$VSEL_{2-0}$	Selects the source of the V bus used for merging with the output of the ALU.
ZD	Chooses zero detect of the ALU output (F) or the Y bus.
$SSEL_{2-0}$	Selects the source of the S operand input to the ALU.
FUN_{4-0}	Controls the operation of the funnel shifter.
MSK_{1-0}	Selects the function of the mask generator.
MRG_{1-0}	Controls the merge function.

PIN DESCRIPTIONS (Cont'd)

PIN NAME	DESCRIPTION
$TSEL_{1-0}$	Selects the source of the data to be written into the T port of the RAM.
SDI	Serial data input to the SPC command and data registers for diagnostics.
SDO	Serial data output from SPC command and data registers for diagnostics.
SCLK	SHIFT clock for loading the SPC command and data registers for diagnostics.
$C/\overline{D}$	Command/data control input for SPC operation.
DCMP	The open drain compare output for SPC diagnostics.
VCC_{7-0}	Eight pins for power supply 5 volt, all of which must be connected to 5 volts.
GND_{16-0}	Sixteen pins for ground, all of which must be connected to ground.

DEVICE ARCHITECTURE

The IDT49C404 is a high-speed 32-bit microprogrammable CMOS microprocessor slice which can be cascaded to 64-bits. It allows simple, yet high-speed, arithmetic and logic operations on subfields, shift, rotate, mask and merge.

In general, the IDT49C404 can be viewed as a 7-port working RAM feeding into a funnel shifter, then into an ALU and then into merge logic. The control of each of these blocks is orthogonal, allowing the user to select data from registers, shift it, operate on it with the ALU and then merge it in only one cycle. Optionally, the funnel shifter or ALU can be bypassed, allowing the user additional flexibility. In this way, the designer may avoid paying a performance penalty when a particular algorithm requires only one or the other. Thus, the cycle time can be tailored to match the processing requirements.

The IDT49C404 can be divided into the following functional segments:

- Three 32-bit bidirectional I/O ports
- Seven-port 64-word x 32-bit RAM
- 64 bits in/32 bits out cascadable funnel shifter
- 32-bit ALU
- Mask generator
- Merge logic
- Diagnostics circuitry

THREE BUS ARCHITECTURE

The IDT49C404's 3-bus architecture consists of three bi-directional 32-bit ports (DA, DB and Y). The DA and DB bi-directional buses connect respectively to the A and B RAM outputs and A and B RAM inputs. Thus, data can be read out of the RAM on DA and DB or data can be brought in independently on DA and DB. This special feature allows for easy RAM expansion. Since data can be brought out on the DA and DB buses, other ALU elements can be connected externally which extend the overall ALU, funnel shifter, mask and merge capabilities.

The third 32-bit bus, Y, is the output of the merge logic and also the input back into the RAM ports A, B and T via the Z bus or internal Y bus.The Z MUX multiplexes between the ALU or the Y bus. By selecting the output of the ALU, the results of the ALU operation can be stored back into the RAM while data may be brought out through the merge path onto the Y bus. This results in an ALU operation in parallel with the extraction of data out of the register file. Additionally, there is an alternate data path which allows the Y bus to connect directly into the T MUX such that data can be written from the ALU back into the RAM while data is being brought in, at the same time, through the Y bus to the RAM.

This three bus approach allows for the easy data accessibility necessary when designing high-performance microprocessor-based systems.

SEVEN-PORT RAM

The IDT49C404 incorporates a 64-word by 32-bit RAM which has seven ports—four read ports and three write ports. The four read ports are A, B, Q and T. The A and B ports are considered the data path ports and can be used interchangeably. During most cycles, they supply data to the funnel shifter, ALU and merge logic. These ports can be considered to be similar to the A and B ports of the IDT39C203. The Q and T output ports are used mainly for controlling such things as start and width for the funnel shifter and mask generation for merge operations. Since the Q and T ports are outputs of the RAM, the start positions may be computed on previous cycles using the ALU, thus providing extensive programmer flexibility.

There are three write ports; A, B and T. The A and B ports are typically used for results from the current cycle and the T port is used for incrementing counter values in the RAM, as well as loading data from the Y bus in parallel with ALU operations. There are four address buses controlling A, B, Q and T. In one cycle, the seven-port RAM is capable of writing to three locations while reading from four locations. This feature highlights the IDT49C404's highly parallel architecture.

64-BIT FUNNEL SHIFTER

The funnel shifter accepts two 32-bit operands (A, B, Q, DA, DB or T) which are operated on as a 64-bit word. The output of the funnel shifter is the result of selecting any consecutive 32-bit word within the 64-bit operand. The 32-bit word can start on any bit boundary between 0 and 31. The M and N input muxes allow the user to swap the data as well as duplicate it, allowing for barrel shifting. The funnel shifter also has the capability of taking any 32-bit word as an input and extending the sign, as well as providing zero fill. Through special hooks in the architecture, the funnel shifter can be expanded along with the ALU/merge logic to perform 64-bit operations in a single cycle.

ALU

The output of the funnel shifter feeds the 32-bit ALU. The ALU can perform conventional binary operations such as logic, addition, subtraction, as well as multiplication and division. Also, the sum of the start and the width information can be used to select the bit boundary from which the carry, sign and overflow flags will output as status. This allows for true arbitrary subfield operations. The other ALU inputs are selected from A, B, Q, T or mask generator.

MASK GENERATION AND MERGE LOGIC

The mask generation and merge logic allows for field manipulation within the 32-bit resulting word. The mask generator, which determines how the bits will be merged between V and F, is controlled by start and width input pins. The start and width can also come from Q or T. T is used for start and Q is used for width, thus start/width can be calculated, stored in the register file and used in the mask generator. An alternate to the mask generator is a mask which comes directly from the Q or T outputs of the RAM, allowing for totally arbitrary masks.

The V input of the merge logic comes from a multiplexer which can select any output of the RAM, DA, DB, all 1s or all 0s. The F input is connected to the output of the ALU. The mask is used to merge the V and F input on a bit-by-bit basis, which results in the Y output.

Included in the merge logic is a priority detect circuit. It is used to produce a binary weighted code to indicate the location of the highest order one on its input.

SERIAL DIAGNOSTICS

The Serial Protocol Channel (SPC) is a set of pins by which data can be entered into and extracted from a device (such as the IDT49C404) through a serial data input and output port. SPC can be used at many points in the life of a product for diagnostic purposes such as: system level design debug and development, system test during manufacturing and field maintenance debug and test. SPC is of significant benefit as board level packing densities increase. This is because access to test and debug points becomes difficult. This is particularly true in double-sided surface mount technologies.

As companies like IDT continue to integrate more onto each device and put each device into smaller and smaller packages such as surface mount devices, the board level testing becomes more complex for the designer and the manufacturing divisions of companies. To help this situation, a serial diagnostics scheme was developed. It allows for observation of critical signals deep within the system. During system test, when an error is observed, these signals may be modified in order to zero in on the fault in the system.

SPC is primarily a scheme utilizing only four pins SDI, SDO, SCLK, C/$\overline{D}$ to examine and alter the internal state of a system, for the purpose of monitoring and diagnosing system faults. The SPC has been defined in such a way that it can be implemented with a small number of gates. In many cases, SPC can be added by utilizing less than 5% of the total logic gates. As more gates are added to each device and the number of pins increase, the overhead for diagnostics decreases.

In the following block diagram of a typical application, the Serial Protocol Channel is shown being used with a writable control store in a microprogrammed design. The control store can be initialized through the SPC path. A register with SPC is used for the instruction register going into the IDT49C410 (16-bit microprogram sequencer), as well as data registers around the IDT49C404. In this way, the designer may use the Serial Protocol Channel to observe and modify the microcode coming out of the writable control store, as well as observing and being able to modify data and instructions in the overall machine.

The block diagram of the diagnostics ring in Figure 1 shows how the devices with diagnostics are hooked together in a serial ring via the SDI and SDO signals. The diagnostics signals may be generated through registers which are hooked up to a microprocessor. This microprocessor could conceivably be an IBM PC.

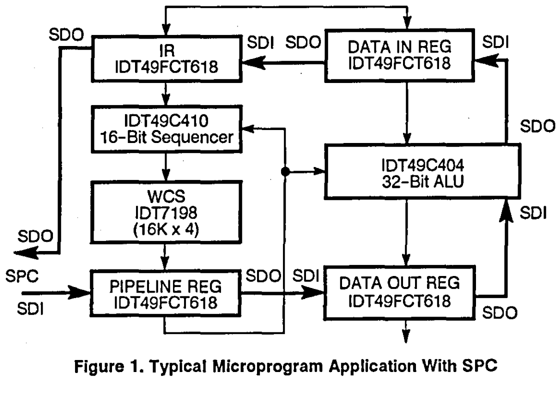


Figure 1. Typical Microprogram Application With SPC

The IDT49C404 accommodates a variety of diagnostics operations. It not only includes the standard Serial Protocol Channel but also the ability to scan data out of the I/O pad cells (as shown in Figure 2) which are connected to the pins of the device. In this way, the state of external connections can be observed, thus telling a lot about the system surrounding the IDT49C404. The scan path through the I/O pad cells is in series with the serial data register.

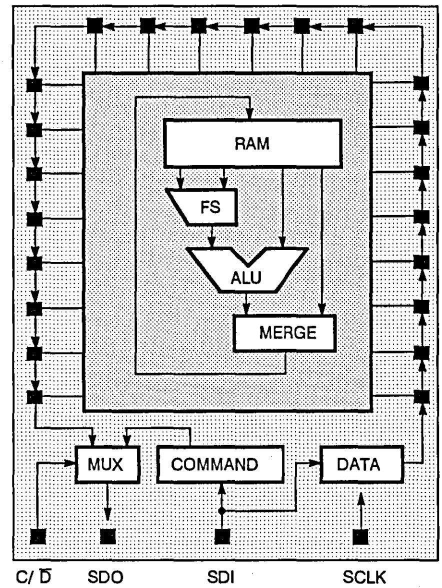


Figure 2. Conceptual Diagram of IDT49C404 Die Incorporating SPC Scan Path

CONTROL INPUTS

The control inputs of the IDT49C404 which make up the instruction set are highly orthogonal and provide the user with the highest degree of control over each individual functional unit. Each major unit in the IDT49C404 has its own set of control lines. The following diagrams show the microprogram word layout of the individual fields, as well as the opcodes and functions for each of the fields.

In order to maintain simplicity and orthogonality, the instruction combinations which are used infrequently and require special extended control (divide, multiply, etc.) are grouped together and labled as special instructions. To use these instructions, a special instruction trap door mechanism was employed in the ALU control field (opcode = 101). In the case of special instructions, the T source select and merge control define the particular instructions to be performed. Some special instructions require immediate operands which are provided by other fields such as start, width, funnel shift control, etc.

8

IDT49C404 INSTRUCTION FIELDS

44	43 42	41 40	39 38	37 36	35	34 30	29 24	23 17	16 14	13 12	11 10	9 7	6 5	4 3	2 0
$\overline{OE}_Y$	$\overline{OE}_A$ $\overline{OE}_B$	MSEL NSEL	SSEL	MASK GEN	ML	FUNNEL SHIFTER	WIDTH	START	TSEL	ALU	MRG	VSEL	ZSEL ZD	ASEL BSEL	$\overline{WE}_A$ $\overline{WE}_B$ $\overline{WE}_T$
						16-BIT IMMEDIATE FIELD				SPECIAL INSTRUCTION FIELD					
								7-BIT IMMEDIATE FIELD							

INSTRUCTION SET SUMMARY

M SOURCE SELECTION			
MNEMONIC	$\overline{OE}_A$	MSEL	M SOURCE
AOE	0	0	A
T	0	1	T
A	1	0	A
DA	1	1	DA

MASK SOURCE			
MNEMONIC	MSK		SOURCE
EXT	0	0	Start and Width from Instruction
INT	0	1	T & Q Supply Start and Width
T32	1	0	T as a 32-Bit Mask
Q32	1	1	Q as a 32-Bit Mask

ALU				
MNEMONIC	ALU			FUNCTION
ADD	0	0	0	$R + S + C_0$
SUBR	0	0	1	$S - R - 1 + C_0$
SUBS	0	1	0	$R - S - 1 + C_0$
OR	0	1	1	R or S
AND	1	0	0	R and S
–	1	0	1	Special Instruction
EXOR	1	1	0	R exor S
EXNOR	1	1	1	R exnor S

V SOURCE				
MNEMONIC	VSEL			SOURCE
DA	0	0	0	DA
A	0	0	1	A
Q	0	1	0	Q
T	0	1	1	T
B	1	0	0	B
DB	1	0	1	DB
ZEROS	1	1	0	0's
ONEs	1	1	1	1's

N SOURCE SELECTION			
MNEMONIC	$\overline{OE}_B$	NSEL	N SOURCE
BOE	0	0	B
Q	0	1	Q
B	1	0	B
DB	1	1	DB

S SOURCE				
MNEMONIC	SSEL			SOURCE
DA	0	0	0	DA
A	0	0	1	A
Q	0	1	0	Q
T	0	1	1	T
B	1	0	0	B
DB	1	0	1	DB
Y	1	1	0	Y
MASK	1	1	1	MASK

MERGE CONTROL			
MNEMONIC	MRG		FUNCTION
F	0	0	Pass F
V	0	1	Pass V
F to V	1	0	Merge F/V
V to F	1	1	Merge V/F

SPECIAL INSTRUCTIONS (ALU = 101)							
MNEMONIC	MRG		VSEL			FUNCTION	OPERANDS
UMLT	0	0	0	0	0	Unsigned Multiply	A, B, T
TMLT	0	0	0	0	1	Two's Complement Multiply	A, B, T
TMLTL	0	0	0	1	0	Two's Complement Multiply Last Cycle	A, B, T
DIVF	0	0	0	1	1	First Divide	A, B, T
DIV	0	0	1	0	0	Second Divide	A, B, T
DIVL	0	0	1	0	1	Last Divide	A, B, T
PRF	0	0	1	1	0	Prioritize First Cycle (32 Bits)	S, Mask
PRS	0	0	1	1	1	Prioritize Second Cycle (64 Bits)	S
INC	0	1	0	0	0	S + Imm (7-Bit) + C_0	S, Imm
DEC	0	1	0	0	1	S − Imm (7-Bit) − 1 + C_0	S, Imm
LDI	0	1	0	1	0	Load T with Imm (16-Bit)	16-Bit Imm
LDC1	0	1	0	1	1	Load C1 from Z bus	S
LDC2	0	1	1	0	0	Load C2 from Z bus	S
EXCHG	0	1	1	0	1	Exchange RAM Locations	DA, DB
LDAB	0	1	1	1	0	Load DA into B address	DA
LDBA	0	1	1	1	1	Load DB into A address	DB
SMAGT	1	0	0	0	0	Sign Magnitude/Two's Complement Conversion	S
PROGS	1	0	0	0	1	Program Slice	–

T SOURCE			
MNEMONIC	TSEL		SOURCE
Z	0	0	Z Bus
Y	0	1	Y Bus
TC1	1	0	T + C1 + TC_0
TC2	1	1	T + C2 + TC_0

A RAM DEST		
MNEMONIC	ASEL	SOURCE
DA	0	DA Bus
Z	1	Z Bus

B RAM DEST		
MNEMONIC	BSEL	SOURCE
Z	0	Z Bus
DB	1	DB Bus

Z BUS CONTROL

Z BUS SOURCE		
MNEMONIC	ZSEL	SOURCE
F	0	F Bus
Y	1	Y Bus

ZERO DETECT SOURCE		
MNEMONIC	ZD	SOURCE
F	0	F Bus
Y	1	Y Bus

8

FUNNEL SHIFT OPERATIONS							
MNEMONIC	FUN					FUNCTION	OPERANDS
SMLZ	0	0	0	0	0	Shift M and fill with 0	0, M
SNLZ	0	0	0	0	1	Shift N and fill with 0	0, N
SMLM	0	0	0	1	0	Shift M and fill with ML	ML, M
SNLM	0	0	0	1	1	Shift N and fill with ML	ML, N
XNM	0	0	1	0	0	Extract field from	N, M
XMN	0	0	1	0	1	Extract field from	M, N
SMAZ	0	0	1	1	0	Shift M arithmetic and fill 0	Sign, M, 0
SNAZ	0	0	1	1	1	Shift N arithmetic and fill 0	Sign, N, 0
SMAM	0	1	0	0	0	Shift M arithmetic and fill ML	Sign, M, ML
SNAM	0	1	0	0	1	Shift N arithmetic and fill ML	Sign, N, ML
BM	0	1	0	1	0	Barrel shift M	M
BN	0	1	0	1	1	Barrel shift N	N
PM	0	1	1	0	0	Pass M	M
PN	0	1	1	0	1	Pass N	N
PZ	0	1	1	1	0	Pass all 0s	0
PO	0	1	1	1	1	Pass all 1s	1
SMLZBA	1	0	0	0	0	Shift M and fill with 0, Bypass ALU	0, M
SNLZBA	1	0	0	0	1	Shift N and fill with 0, Bypass ALU	0, N
SMLMBA	1	0	0	1	0	Shift M and fill with ML, Bypass ALU	ML, M
SNLMBA	1	0	0	1	1	Shift N and fill with ML, Bypass ALU	ML, N
XNMBA	1	0	1	0	0	Extract field from N & M, Bypass ALU	N, M
XMNBA	1	0	1	0	1	Extract field from M & N, Bypass ALU	M, N
SMAZBA	1	0	1	1	0	Shift M arith. and fill 0, Bypass ALU	Sign, M, 0
SNAZBA	1	0	1	1	1	Shift N arith. and fill 0, Bypass ALU	Sign, N, 0
SMAMBA	1	1	0	0	0	Shift M arith. and fill ML, Bypass ALU	Sign, M, ML
SNAMBA	1	1	0	0	1	Shift N arith. and fill ML, Bypass ALU	Sign, N, ML
BMBA	1	1	0	1	0	Barrel shift M, Bypass ALU	M
BNBA	1	1	0	1	1	Barrel shift N, Bypass ALU	N
POCM	1	1	1	0	0	Pass 1s Complement of M	M
POCN	1	1	1	0	1	Pass 1s Complement of N	N
PMFM	1	1	1	1	0	Pass M and fill ML bit from Bit0 to SP	M
PNFM	1	1	1	1	1	Pass N and fill ML from Bit0 to SP	N

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.8	1.8	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
$C_{I/O}$(2)	I/O Capacitance	V_{OUT} = 0V	15	pF

NOTE:
1. This parameter is sampled and not 100% tested.
2. Includes only output pins.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level (4)	V_{CC} = Max.		2.0	–	–	V
V_{IL}	Input LOW Level (4)	V_{CC} = Min.		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0V		–	–	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -6mA MIL.	2.4	4.3	–	
			I_{OH} = -8mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 12mA MIL.	–	0.3	0.5	
			I_{OL} = 15mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10	µA
			V_O = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V (3)		-15	–	–	mA

NOTES:
1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

8

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ±10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H	V_{CC} = Max. $V_{IH} \geq V_{HC}$, $V_{IL} \leq V_{LC}$ f_{CP} = 0, CP = V_{CC}		–	–	–	mA
I_{CCQL}	Quiescent Power Supply Current CP = L	V_{CC} = Max. $V_{IH} \geq V_{HC}$, $V_{IL} \leq V_{LC}$ f_{CP} = 0, CP = 0V		–	–	–	mA
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IL} = 3.4V, f_{CP} = 0		–	–	–	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IH}$, $V_{IL} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = 0V	MIL.	–	–	–	mA/MHz
			COM'L.	–	–	–	
I_{CC}	Total Power Supply Current [6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = 0V 50% Duty cycle $V_{HC} \leq V_{IH}$, $V_{IL} \leq V_{LC}$	MIL.	–	–	–	mA
			COM'L.	–	–	–	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = 0V 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	300	400	
			COM'L.	–	250	350	

NOTES:
5. I_{CCQT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQCH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock Input frequency

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.

2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.

3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.

4) To guarantee data sheet compliance, the input thresholds should be tested per input pin, in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.

IDT49C404 PROPAGATION DELAYS (1)

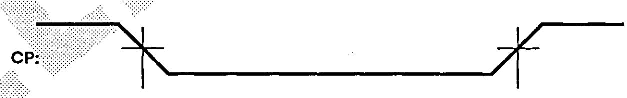
T_A = 0°C to +70°C, V_{CC} = +5V ±5%

FROM INPUT	TO OUTPUT: Y			ZERO			DCMP			STATUS FLAGS		UNIT
	ALU only	FS only	ALU & FS	ALU only	FS only	ALU & FS	ALU only	FS only	ALU & FS	ALU only	ALU & FS	
A, B, Q, T	55	55	75	58	58	78	–	–	–	40	54	ns
DA, DB	37	37	56	40	40	60	–	–	–	40	34	ns
NSEL, MSEL, MS, NS, $\overline{OEA}$, $\overline{OEB}$	–	–	–	–	–	–	–	–	–	–	–	ns
MSK, FS, STR, W	–	–	–	–	–	–	–	–	–	–	–	ns
ALU	–	–	–	–	–	–	–	–	–	–	–	ns
C_0	–	–	36	–	–	–	–	–	–	–	–	ns
MRG, ZD	–	–	–	–	–	–	–	–	–	–	–	ns
Y	–	–	–	–	–	–	–	–	–	–	–	ns

NOTE:

1. On any given cycle, an arithmetic operation without a shift operation can be performed (ALU only) or a shift operation without an arithmetic operation can be performed (FS only) or, finally, both operations in series in one single cycle (ALU + FS).

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)



INPUT	SET-UP TIME BEFORE H-L	HOLD TIME AFTER H-L	SET-UP TIME BEFORE L-H	HOLD TIME AFTER L-H	UNIT
A, B, T, Q Address (Source or Destination)	18	0	–	1	ns
DA, DB	–	–	–	0	ns
C_0, M_L	–	–	–	1	ns
I_{LINES}	–	–	–	0	ns
Y	–	–	–	0	ns

IDT49C404A PROPAGATION DELAYS [1]

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

FROM INPUT	TO OUTPUT											UNIT
	Y			ZERO			DCMP			STATUS FLAGS		
	ALU only	FS only	ALU & FS	ALU only	FS only	ALU & FS	ALU only	FS only	ALU & FS	ALU only	ALU & FS	
A, B, Q, T	–	–	–	–	–	–	–	–	–	–	–	ns
DA, DB	–	–	–	–	–	–	–	–	–	–	–	ns
NSEL, MSEL, MS, NS, $\overline{OEA}$, $\overline{OEB}$	–	–	–	–	–	–	–	–	–	–	–	ns
MSK, FS, STR, W	–	–	–	–	–	–	–	–	–	–	–	ns
ALU	–	–	–	–	–	–	–	–	–	–	–	ns
C_0	–	–	–	–	–	–	–	–	–	–	–	ns
MRG, ZD	–	–	–	–	–	–	–	–	–	–	–	ns
Y	–	–	–	–	–	–	–	–	–	–	–	ns

NOTE:

1. On any given cycle, an arithmetic operation without a shift operation can be performed (ALU only) or a shift operation without an arithmetic operation can be performed (FS only) or, finally, both operations in series in one single cycle (ALU + FS).

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

INPUT	SET-UP TIME BEFORE H-L	HOLD TIME AFTER H-L	SET-UP TIME BEFORE L-H	HOLD TIME AFTER L-H	UNIT
A, B, T, Q Address (Source or Destination)	–	–	–	–	ns
DA, DB	–	–	–	–	ns
C_0, M_L	–	–	–	–	ns
I_{LINES}	–	–	–	–	ns
Y	–	–	–	–	ns

TEST LOAD CIRCUIT

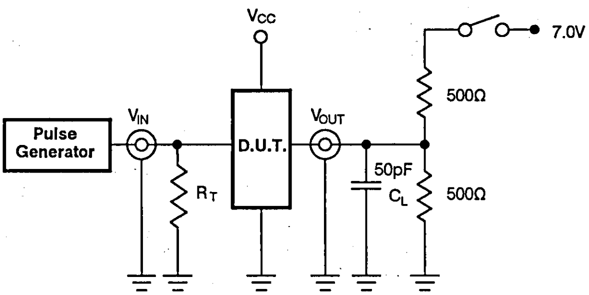


Figure 1. Switching Test Circuits (All Outputs)

SWITCH POSITION

TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

ORDERING INFORMATION

IDT XXXXXXX (Device Type) XX (Package) X (Process/Temperature)

Process/Temperature:

BLANK	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

PG	208-pin Plastic Pin Grid Array
G	208-pin Pin Grid Array

Device Type:

49C404	32-Bit CMOS Microprogram Microprocessor
49C404A	High-Speed 32-Bit CMOS Microprogram Microprocessor

16-BIT CMOS MICROPROGRAM SEQUENCER

IDT49C410
IDT49C410A

MICROSLICE ™ PRODUCT

FEATURES:

- 16-bit wide address path
  - Address up to 65,536 words of microprogram memory
- 16-bit loop counter
  - Pre-settable down-counter for counting loop iterations and repeating instructions
- Low-power CEMOS ™
  - I_{CC} (max.)
    Military: 90mA
    Commercial: 75mA
- Fast
  - IDT49C410 meets 2910A speeds
  - IDT49C410A 30% speed upgrade
- 33-deep stack
  - Accommodates highly nested microcode
- 16 powerful microinstructions
  - Executes 16 sequence control instructions
- Available in 48-pin 600 mil plastic and sidebraze, 48-pin 400 mil SHRINK-DIP, 48-pin LCC, 52-pin PLCC and 48-pin Flatpack
- Three enables control branch address sources
- Four address sources
- 2901A instruction compatibility
- Military product available compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C410s are architecture and function code compatible to the 2901A with an expanded 16-bit address path, thus allowing for programs up to 65,536 words in length. They are microprogram address sequencers intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the capability of sequential access, they provide conditional branching to any microinstruction within their 65,536 microword range.

The 33-deep stack provides microsubroutine return linkage and looping capability. The deep stack can be used for highly nested microcode applications. Microinstruction loop count control is provided with a count capacity of 65,536.

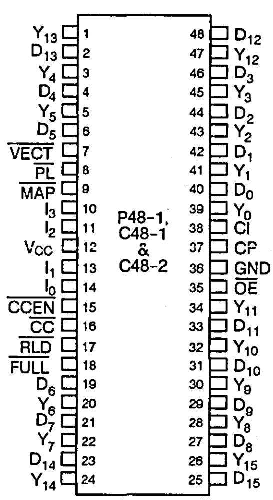
During each microinstruction, the microprogram controller provides a 16-bit address from one of four sources: 1) the microprogram address register (μPC), which usually contains an address one greater than the previous address; 2) an external (direct) input (D); 3) a register/counter (R) retaining data loaded during a previous microinstruction; or 4) a last-in/first-out stack (F).

The IDT49C410s are fabricated using CEMOS, a CMOS technology designed for high performance and high reliability.

The IDT49C410s are pin-compatible, performance-enhanced, easily upgradable versions of the 2901A.

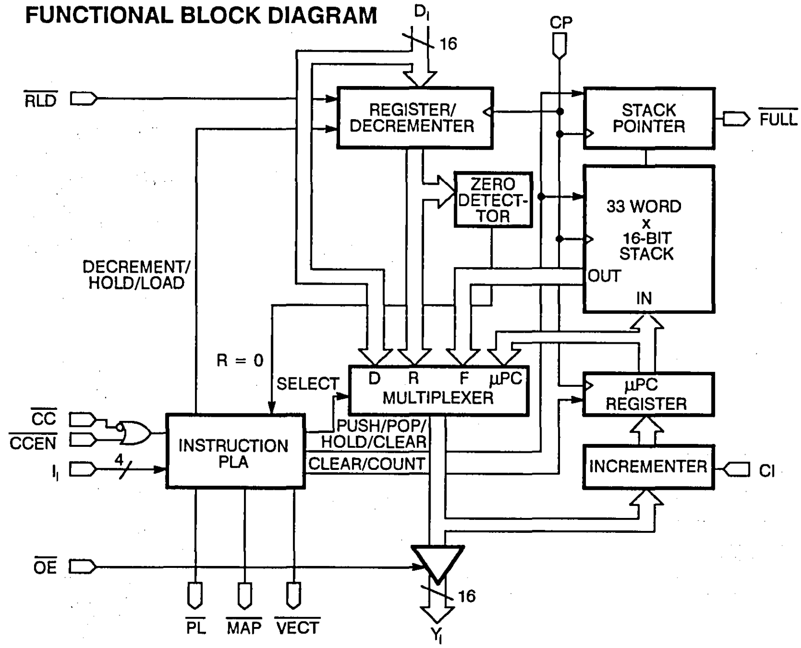
The IDT49C410s are available in 48-pin DIPs (600 mil x 100 mil centers or space-saving 400 mil x 70 mil centers), 48-pin LCC, 52-pin PLCC and 48-pin flatpacks.

PIN CONFIGURATION



DIP
TOP VIEW

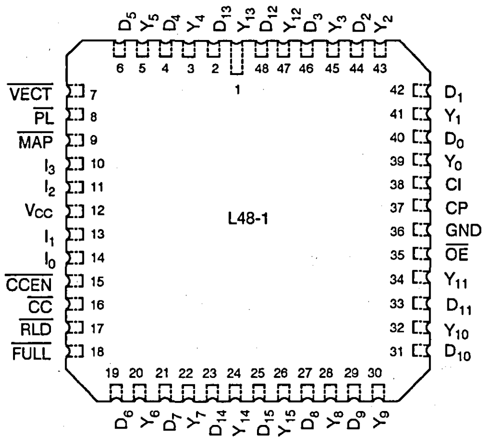
FUNCTIONAL BLOCK DIAGRAM



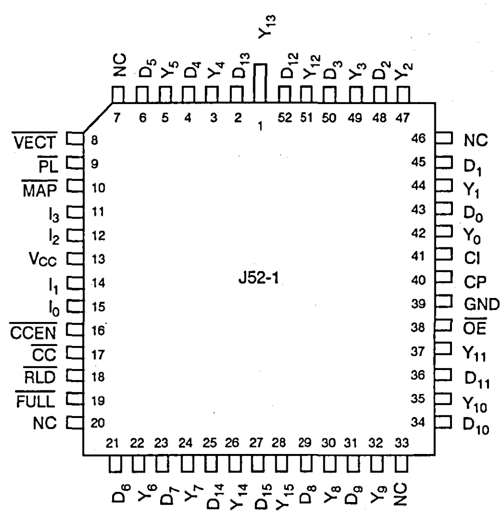
CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

PIN CONFIGURATIONS



LCC
TOP VIEW

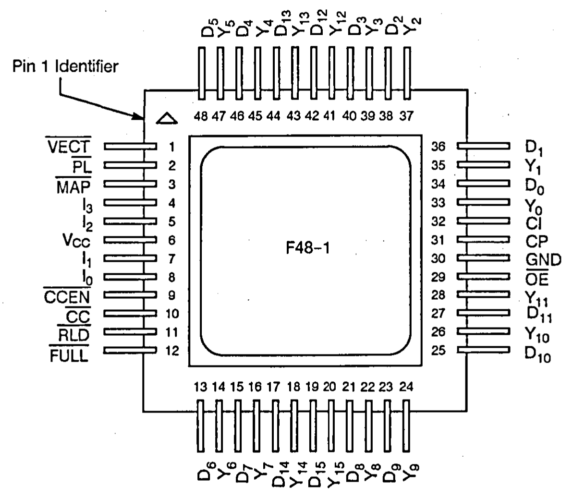


PLCC
TOP VIEW

IDT49C410 PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
D_I	I	Direct input to register/counter and multiplexer, D_0 is LSB.
I_I	I	Selects one of sixteen instructions.
$\overline{CC}$	I	Used as test criterion. Pass test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	I	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the part operates as though $\overline{CC}$ were true (LOW).
CI	I	Low order carry input to incrementer for microprogram counter.
$\overline{RLD}$	I	When LOW forces loading of register/counter regardless of instruction or condition.
$\overline{OE}$	I	Three-state control of Y_I outputs.
CP	I	Triggers all internal state changes at LOW-to-HIGH edge.
Y_I	O	Address to microprogram memory. Y_0 is LSB, Y_{15} is MSB.
$\overline{FULL}$	O	Indicates that 33 items are on the stack.
$\overline{PL}$	O	Can select #1 source (usually Pipeline Register) as direct input source.
$\overline{MAP}$	O	Can select #2 source (usually Mapping PROM or PLA) as direct input source.
$\overline{VECT}$	O	Can select #3 source (for example, Interrupt Starting Address) as direct input source.

8



FLATPACK
TOP VIEW

PRODUCT DESCRIPTION

The IDT49C410s are high-performance CMOS microprogram sequencers that are intended for use in very high-speed microprogrammable microprocessor applications. The sequencers allow for direct control of up to 64K words of microprogram.

The heart of the microprogram sequencer is a 4-input multiplexer that is used to select one of four address sources to select the next microprogram address. These address sources include the register/counter, the direct input, the microprogram counter or the stack as the source for the address of the next microinstruction.

The register/counter consists of sixteen D-type flip-flops which can contain either an address or a count. These edge-triggered flip-flops are under the control of a common clock enable as well as the four microinstruction control inputs. When the load control ($\overline{RDL}$) is LOW, the data at the D-inputs is loaded into this register on the LOW-to-HIGH transition of the clock. The output of the register/counter is available at the multiplexer as a possible next address source for the microcode. Also, the terminal count output associated with the register/counter is available at the internal instruction PLA to be used as a condition code input for some of the microinstructions. The IDT49C410s contain a microprogram counter that usually contains the address of the next microinstruction compared to that currently being executed. The microprogram counter actually consists of a 16-bit incrementer followed by a 16-bit register. The microprogram counter will increment the address coming out of the sequencer going to the microprogram memory if the carry-in input to this counter is HIGH; otherwise, this address will be loaded into the microprogram counter. Normally, this carry-in input is set to the logic HIGH state so that the incrementer will be active. Should the carry input be set LOW, the same address is loaded into the microprogram counter. This is a technique that can be used to allow execution of the same microinstruction several times.

There are sixteen D-inputs on the IDT49C410s that go directly to the address multiplexer. These inputs are used to provide a branch address that can come directly from the microcode or some other external source. The fourth input available to the multiplexer for next address control is the 33-deep, 16-bit wide LIFO stack. The LIFO stack provides return address linkage for subroutines and loops. The IDT49C410s contain a built-in stack pointer that always points to the last stack location written. This allows for stack reference operations, usually called loops, to be performed without popping the stack.

The stack pointer internal to the IDT49C410s is actually an up/down counter. During the execution of microinstructions one, four and five, the PUSH operation may occur depending on the state of the condition code input. This causes the stack pointer to be incremented by one and the stack to be written with the required return linkage (the value contained in the microprogram counter). On the microprogram cycle following the PUSH, this new return linkage data that was in the microprogram counter is now at the new location pointed to by the stack pointer. Thus, any time the multiplexer looks at the stack, it will see this data on top of the stack.

During five different microinstructions, a pop operation associated with the stack may occur. If the pop occurs, the stack pointer is decremented at the next LOW-to-HIGH transition of the clock. A pop decrements the stack pointer which is the equivalent of removing the old information from the top of the stack.

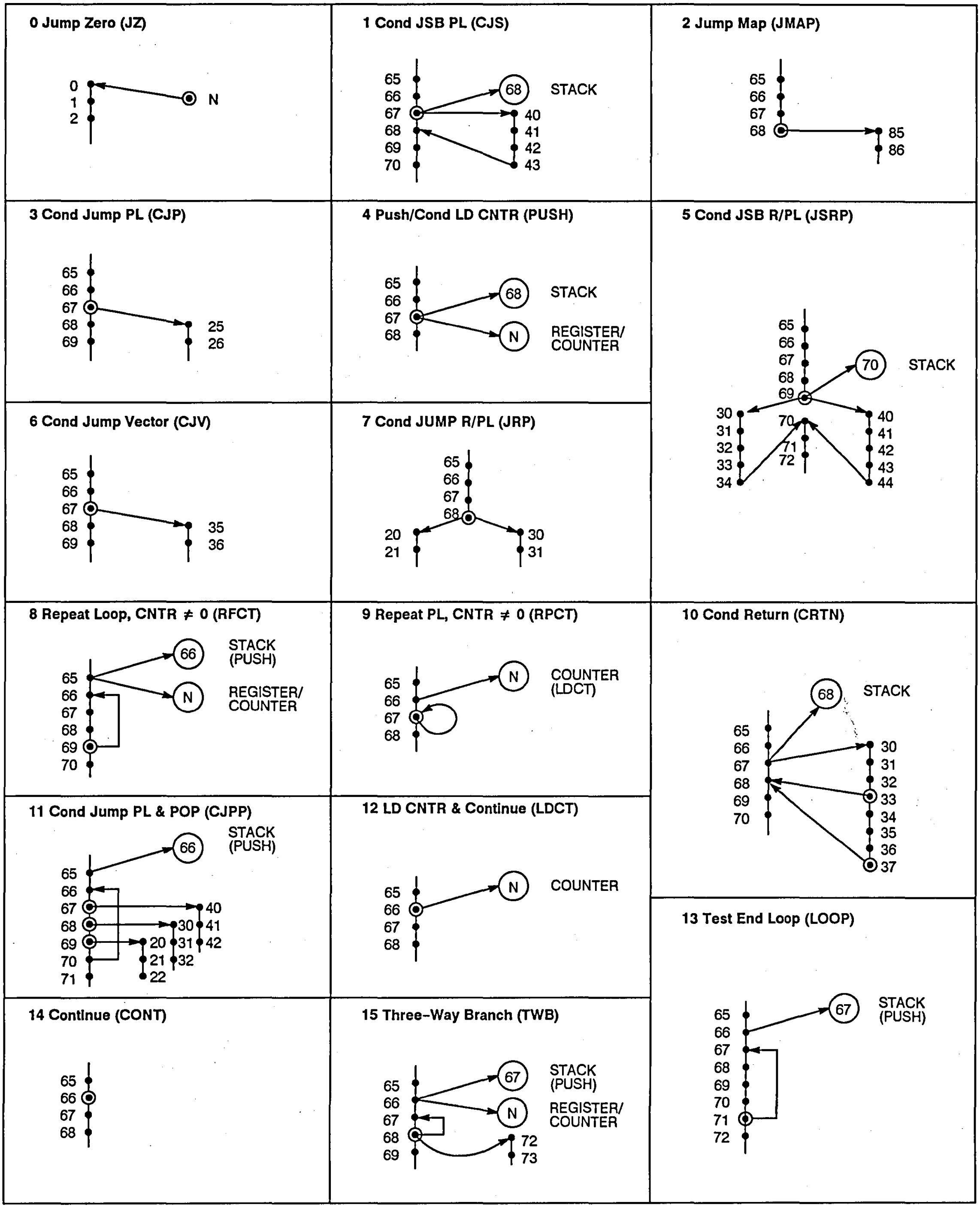
The IDT49C410s are designed so that the stack pointer linkage allows any sequence of pushes, pops or stack references to be used. The depth of the stack can grow to a full 33 locations. After a depth of 33 is reached, the $\overline{FULL}$ output goes LOW. If further PUSHes are attempted when the stack is full, the stack information at the top of the stack will be destroyed but the stack pointer will not end around. It is necessary to initialize the stack pointer when power is first turned on. This is performed by executing a RESET instruction (instruction 0). This sets the stack pointer to the stack empty position—the equivalent depth of 0. Similarly, a pop from an empty stack may place unknown data on the Y outputs, but the stack pointer is designed so as not to end around. Thus, the stack pointer will remain at the 0 or stack empty location if a pop is executed while the stack is already empty.

The IDT49C410s' internal 16-bit register/counter is used during microinstructions eight, nine and fifteen. During these instructions, the 16-bit counter acts as a down counter and the terminal count (count = 0) is used by the internal instruction PLA as an input to control the microinstruction branch test capability. The design of the internal counter is such that, if it is preloaded with a number N and then this counter is used in a microprogram loop, the actual sequence in the loop will be executed N + 1 times. Thus, it is possible to load the counter with a count of 0 and this will result in the microcode being executed one time. The 3-way branch microinstruction, instruction 15, uses both the loop counter and the external condition code input to control the final source address from the Y outputs of the microprogram sequencer. This 3-way branch may result in the next address coming from the D inputs, the stack or the microprogram counter.

The IDT49C410s provide a 16-bit address at the Y outputs that are under control of the $\overline{OE}$ input. Thus, the outputs can be put in the three-state mode, allowing the writable control store to be loaded or certain types of external diagnostics to be executed.

In summary, the IDT49C410s are the most powerful microprogram sequencers currently available. They provide the deepest stack, the highest performance and the lowest power dissipation for today's microprogrammed machine design.

FIGURE 1. IDT49410 FLOW DIAGRAMS



IDT49C410 OPERATION

The IDT49C410s are CMOS pin-compatible implementations of the Am2910 and Am2910A microprogram sequencers. The IDT49C410 sequencers are functionally identical except that they are 16 bits wide and provide a 33-deep stack to give the microprogrammer more capability in terms of microprogram subroutines and microprogram loops. The definition of each microprogram instruction is shown in the table of instructions. This table shows the results of each instruction in terms of controlling the multiplexer which determines the Y outputs and in controlling the signals that can be used to enable various branch address sources. ($\overline{PL}$,$\overline{MAP}$, $\overline{VECT}$). The operation of the register/counter and the 33-deep stack after the next LOW-to-HIGH transition of the clock are also shown. The internal multiplexer is used to select which of the internal sources is used to drive the Y outputs. The actual value loaded into the microprogram counter is either identical to the Y output or the Y output value is incremented by 1 and placed in the microprogram counter. This function is under the control of the carry input. For each of the microinstruction inputs, only one of the three outputs ($\overline{PL}$, $\overline{MAP}$ or $\overline{VECT}$) will be LOW. Note that this function is not determined by any of the possible condition code inputs. These outputs can be used to control the three-state selection of one of the sources for the microprogram branches.

Two inputs, $\overline{CC}$ and $\overline{CCEN}$, can be used to control the conditional instructions. These are fully defined in the table of instructions. The $\overline{RLD}$ input can be used to load the internal register/counter at any time. When this input is LOW, the data at the D inputs will be loaded into this register/counter on the LOW-to-HIGH transition of the clock.Thus, the $\overline{RLD}$ input overrides the internal hold or decrement operations specified by the various microinstructions. The $\overline{OE}$ input is normally LOW and is used as the three-state enable for the Y outputs. The internal stack in the IDT49C410s is a last-in/first-out memory that is 16 bits in width and 33 words deep. It has a stack pointer that addresses the stack and always points to the value currently on the top of the stack. When instruction 0 (RESET) is executed, the stack pointer is initialized to the top of the stack which is, by definition, the stack empty condition. Thus, the contents of the top of the stack are undefined until the forced PUSH occurs. A pop performed while the stack is empty will not change the stack pointer in any way; however, it will result in unknown data at the Y outputs.

By definition, the stack is full any time 33 more PUSHes than pops have occurred since the stack was last empty. When this happens, the $\overline{FULL}$ flag will go LOW. This signal first goes LOW on the microcycle after the 33 pushes occur. When this signal is LOW, no additional pushes should be attempted or the information on the top of the stack will be lost.

THE IDT49C410 INSTRUCTION SET

This data sheet contains a block diagram of the IDT49C410 microprogram sequencers. As can be seen, the devices are controlled by a 4-bit microinstruction word (I_3-I_0). Normally, this word is supplied from one 4-bit field of the microinstruction word associated with the entire state machine system. These four bits provide for the selection of one of the sixteen powerful instructions associated with selecting the address of the next microinstruction. Unused Y outputs can be left open; however, the corresponding most significant D inputs should be tied to ground for smaller microwords. This is necessary to make sure the internal operation of the counter is proper should less than 64K of microcode be implemented. As shown in the block diagram, the internal instruction PLA uses the four instruction inputs, as well as the $\overline{CC}$, $\overline{CCEN}$ and the internal counter = 0 line for controlling the sequencer. This internal instruction PLA provides all of the necessary internal control signals to control each particular part of the microprogram sequencer. The next address at the Y outputs of the IDT49C410s can be from one of four sources. These include the internal microprogram counter; the last-in/first-out stack; the register/counter and the direct inputs.

The following paragraphs will describe each instruction associated with the IDT49C410s. As a part of the discussion, an example of each instruction is shown in Figure 1. The purpose of the examples is to show microprogram flow. Thus, in each example the microinstruction currently being executed has a circle around it. That is, this microinstruction is assumed to be the contents of the pipeline register at the output of the microprogram memory. In these drawings, each of the dots refers to the time that the contents of the microprogram memory word would be in the pipeline register and is currently being executed.

INSTRUCTION 0 – JUMP 0 (JZ)

This instruction is used at power-up time or at any restart sequence when the need is to reset the stack pointer and jump to the very first address in microprogram memory. The Jump 0 instruction does not change the contents of the register/counter.

INSTRUCTION 1 – CONDITIONAL JUMP TO SUBROUTINE (CJS)

The Conditional Jump to Subroutine instruction is the one used to call microprogram subroutines. The subroutine address will be contained in the pipeline register and presented at the D inputs. If the condition code test is passed, a branch is taken to the subroutine. Referring to the flow diagram for the IDT49C410s shown in figure 1, we see that the content of the microprogram counter is 68. This value is pushed onto the stack and the top of the stack pointer is incremented. If the test is failed, then this conditional Jump to Subroutine instruction behaves as a simple continue. That is, the contents of microinstruction address 68 are executed next.

INSTRUCTION 2 – JUMP MAP (JMAP)

This sequencer instruction can be used to start different microprogram routines based on the machine instruction opcode. This is typically accomplished by using a mapping PROM as an input to the D inputs on the microprogram sequencer. The JMAP instruction branches to the address appearing on the D inputs. In the flow diagram shown in Figure 1, we see that the branch actually will be to the contents of microinstruction 85 and this instruction will be executed next.

INSTRUCTION 3 – CONDITIONAL JUMP PIPELINE (CJP)

The simplest branching control available in the IDT49C410 microprogram sequencers is that of Conditional Jump to Address. In this instruction, the jump address is usually contained in the microinstruction pipeline register and presented to the D inputs. If the test is passed, the jump is taken. If the test fails, this instruction executes as a simple continue. In the example shown in the flow diagram of Figure 1, we see that, if the test is passed, the next microinstruction to be executed is the contents of address 25. If the test is failed, the microcode simply continues to the contents of the next instruction.

INSTRUCTION 4 – PUSH/CONDITIONAL LOAD COUNTER (PUSH)

With this instruction, the counter can be conditionally loaded during the same instruction that pushes the current value of the microprogram counter on to the stack. Under any condition independent of the conditional testing, the microprogram counter is pushed on to the stack. If the conditional test is passed, the counter will be loaded with the value on the D inputs to the sequencer. If the test fails, the contents of the counter will not change. The PUSH/Conditional Load Counter instruction is used in conjunction with the loop instruction (Instruction 13), the repeat file based on the counter instruction (Instruction 9) or the 3-way branch instruction (Instruction 15).

IDT49C410 INSTRUCTION OPERATIONAL SUMMARY

I_3-I_0	MNEMONIC	CC	COUNTER TEST	STACK	ADDRESS SOURCE	REGISTER/ COUNTER	ENABLE SELECT
0	JZ	X	X	CLEAR	0	NC	$\overline{PL}$
1	CJS	PASS FAIL	X X	PUSH NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
2	JMAP	X	X	NC	D	NC	$\overline{MAP}$
3	CJP	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
4	PUSH	PASS FAIL	X X	PUSH PUSH	PC PC	LOAD NC	$\overline{PL}$ $\overline{PL}$
5	JSRP	PASS FAIL	X X	PUSH PUSH	D R	NC NC	$\overline{PL}$ $\overline{PL}$
6	CJV	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{VECT}$ $\overline{VECT}$
7	JRP	PASS FAIL	X X	NC NC	D R	NC NC	$\overline{PL}$ $\overline{PL}$
8	RFCT	X X	= 0 NOT = 0	POP NC	PC STACK	NC DEC	$\overline{PL}$ $\overline{PL}$
9	RPCT	X X	= 0 NOT = 0	NC NC	PC D	NC DEC	$\overline{PL}$ $\overline{PL}$
10	CRTN	PASS FAIL	X X	POP NC	STACK PC	NC NC	$\overline{PL}$ $\overline{PL}$
11	CJPP	PASS FAIL	X X	POP NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
12	LDCT	X	X	NC	PC	LOAD	$\overline{PL}$
13	LOOP	PASS FAIL	X X	POP NC	PC STACK	NC NC	$\overline{PL}$ $\overline{PL}$
14	CONT	X	X	NC	PC	NC	$\overline{PL}$
15	TWB	PASS PASS FAIL FAIL	= 0 NOT = 0 = 0 NOT = 0	POP POP POP NC	PC PC D STACK	NC DEC NC DEC	$\overline{PL}$ $\overline{PL}$ $\overline{PL}$ $\overline{PL}$

NC = No Change; DEC = Decrement

INSTRUCTION 5 — CONDITIONAL JUMP TO SUBROUTINE R/PL (JSRP)

Subroutines may be called by a Conditional Jump Subroutine from the internal register or from the external pipeline register. In this instruction, the contents of the microprogram counter are pushed on the stack and the branch address for the subroutine call will be taken from either the internal register/counter or the external pipeline register presented to the D inputs. If the conditional test is passed, the subroutine address will be taken from the pipeline register. If the conditional test fails, the branch address is taken from the internal register/counter. An example of this is shown in the flow diagram of Figure 1.

INSTRUCTION 6 — CONDITIONAL JUMP VECTOR (CJV)

The Conditional Jump Vector instruction is similar to the Jump Map instruction in that it allows a branch operation to a microinstruction, as defined from some external source. This instruction is similar to the Jump Map instruction except that it is conditional. The Jump Map instruction is unconditional. If the conditional test is passed, the branch is taken to the new address on the D inputs. If the conditional test is failed, no branch is taken but rather the microcode simply continues to the next sequential microinstruction. When this instruction is executed, the $\overline{VECT}$ output is LOW unconditionally. Thus, an external 16-bit field can be enabled on to the D inputs of the microprogram sequencer.

INSTRUCTION 7 — CONDITIONAL JUMP R/PL (JRP)

The Conditional Jump register/counter or external pipeline register always causes a branch in microcode. This jump will be to one of two different locations in the microcode address space. If the test is passed, the jump will be to the address presented on the D inputs to the microprogram sequencer. If the conditional test fails, the branch will be to the address contained in the internal register/counter.

INSTRUCTION 8 — REPEAT LOOP COUNTER NOT EQUAL TO 0 (RFCT)

This instruction utilizes the loop counter and the stack to implement microprogrammed loops. The start address for the loop would be initialized by using the PUSH/conditional load counter instruction. Then, when the repeat loop instruction is executed, if the counter is not equal to 0, the next microword address will be taken from the stack. This will cause a loop to be executed as shown in the Figure 1 flow diagram. Each time the microcode sequence goes around the loop, the counter is decremented. When the counter reaches 0, the stack will be popped and the microinstruction address will be taken from the microprogram counter. This instruction performs a timed wait or allows a single sequence to be executed to the desired number of times. Remember, the actual number of loops performed is equal to the value in the counter plus 1.

INSTRUCTION 9– REPEAT PIPELINE, COUNTER NOT EQUAL TO 0 (RPCT)

This instruction is another technique for implementing a loop using the counter. Here, the branch address for the loop is contained in the pipeline register. This instruction does not use the stack in any way as a part of its implementation. As long as the counter is not equal to 0, the next microword address will be taken from the D inputs of the microprogram sequencer. When the counter reaches 0, the internal multiplexer will select the address source from the microprogram counter, thus causing the microcode to continue on and leave the loop.

INSTRUCTION 10– CONDITIONAL RETURN (CRTN)

The Conditional Return instruction is used for terminating subroutines. The fact that it is conditional allows the subroutine either to be ended or continue. If the conditional test is passed, the address of the next microinstruction will be taken from the stack and it will be popped. If the conditional test fails, the next microinstruction address will come from the internal microprogram counter. This is depicted in the flow diagram of Figure 1. It is important to remember that every subroutine call must somewhere be followed by a return from subroutine call in order to have an equal number of pushes and pops on the stack.

INSTRUCTION 11– CONDITIONAL JUMP PIPELINE AND POP (CJPP)

The Conditional Jump Pipeline and Pop instruction is a technique for exiting a loop from within the middle of the loop. This is depicted fully in the flow diagrams for the IDT49C410s as shown in Figure 1. The conditional test input for this instruction results in a branch being taken if the test is passed. The address selected will be that on the D inputs to the microprogram sequencer and since the loop in being terminated, the stack will be popped. Should the test be failed on the conditional test inputs, the microprogram will simply continue to the next address as taken from the microprogram counter. The stack will not be affected if the conditional test input is failed.

INSTRUCTION 12– LOAD COUNTER AND CONTINUE (LDCT)

The Load Counter and Continue instruction is used to place a value of the D inputs in the register/counter and continue to the next microinstruction.

INSTRUCTION 13– TEST END OF LOOP (LOOP)

The Test End of Loop instruction is used as a last instruction in a loop associated with the stack. During this instruction, if the conditional test input is failed, the loop branch address will be that on the stack. Since we may go around the loop a number if times, the stack is not popped. If the conditional test input is passed, the loop is terminated and the stack is popped. Notice that the loop instruction requires a PUSH to be performed at the instruction immediately prior to the loop return address. This is necessary in order to have the correct address on the stack before the loop operation. For this reason, the stack pointer always points to the last thing written on the stack.

INSTRUCTION 14– CONTINUE (CONT)

The Continue instruction is a simple instruction whereby the address for the microinstruction is taken from the microprogram counter. This instruction simply causes sequential program flow to the next microinstruction in microcode memory.

INSTRUCTION 15– THREE WAY BRANCH (TWB)

The Three Way Branch instruction is used for looping while waiting for a conditional event to come true. If the event does not come true after some number of microinstructions, a branch is taken to another microprogram sequence. This is depicted in Figure 1 showing the IDT49C410 flow diagrams and is also described in full detail in the IDT49C410s' instruction operational summary. Operation of the instruction is such that, any time the external conditional test input is passed, the next microinstruction will be that associated with the program counter and the loop will be left; the stack is also popped. Thus, the external test input overrides the other possibilities. Should the external conditional test input not be true, then the rest of the operation is controlled by the internal counter. If the counter is not equal to 0, the loop is taken by selecting the address on the top of the stack as the address out of the Y outputs of the IDT49C410s. In addition, the counter is decremented. Should the external conditional test input be failed and the counter also have counted to 0, then this instruction "times out". The result is that the stack is popped and a branch is taken to the address presented to the D inputs of the IDT49C410 microprogram sequencers. This address is usually provided by the external pipeline register.

CONDITIONAL TEST

Throughout this discussion we have talked about microcode passing the conditional test. There are actually two inputs associated with the conditional test input. These include the $\overline{CCEN}$ and the $\overline{CC}$ inputs. The $\overline{CCEN}$ input is a condition code enable. Whenever the $\overline{CCEN}$ input is HIGH, the $\overline{CC}$ input is ignored and the device operates as though the $\overline{CC}$ input were true (LOW). Thus, a fail of the external test condition can be defined as $\overline{CCEN}$ equals LOW and $\overline{CC}$ equals HIGH. A pass condition is defined as a $\overline{CCEN}$ equal to HIGH or a $\overline{CC}$ equal to LOW. It is important to recognize the full function of the condition code enable and the condition code inputs in order to understand when the test is passed or failed.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C $\quad$ V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C $\quad$ V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Output HIGH Level	Guaranteed Logic High Level [4]		2.0	–	–	V
V_{IL}	Output LOW Level	Guaranteed Logic Low Level [4]		–	–	0.8	V
I_{IL}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	μA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300μA	V_{HC}	V_{HC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0	–	-0.1	-10	μA
			V_O = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V [3]		-30	–	–	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

8

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_C = 0, CP = H		–	35	50	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = L		–	35	50	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High)(5)	V_{CC} = Max., V_{IN} = 3.4V, f_{CP} = 0		–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	1.0	3.0	mA/ MHz
			COM'L.	–	1.0	1.5	
I_{CC}	Total Power Supply Current(6)	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	MIL.	–	45	80	mA
			COM'L.	–	45	65	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	MIL.	–	50	90	
			COM'L.	–	50	75	

NOTES:
5. I_{CCQT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}\ (CD_H) + I_{CCQL}\ (1 - CD_H) + I_{CCT}\ (N_T \times D_H) + I_{CCD}\ (f_{CP})$$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock Input Frequency

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large V_{CC} current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \le$ 0V and $V_{IH} \ge$ 3V for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

IDT49C410A
AC ELECTRICAL CHARACTERISTICS
I. SET-UP AND HOLD TIMES

INPUTS	$t_{(s)}$		$t_{(h)}$		UNIT
	COM'L.	MIL.	COM'L.	MIL.	
$D_I \rightarrow R$	6	7	0	0	ns
$D_I \rightarrow PC$	13	15	0	0	ns
I_{0-3}	23	25	0	0	ns
$\overline{CC}$	15	18	0	0	ns
$\overline{CCEN}$	15	18	0	0	ns
CI	6	7	0	0	ns
$\overline{RLD}$	11	12	0	0	ns

II. COMBINATIONAL DELAYS

INPUTS	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		UNIT
	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
D_{0-11}	12	15	–	–	–	–	ns
I_{0-3}	20	25	13	15	–	–	ns
$\overline{CC}$	16	20	–	–	–	–	ns
$\overline{CCEN}$	16	20	–	–	–	–	ns
CP	28	33	–	–	22	25	ns
$\overline{OE}$ [1]	10/10	13/13	–	–	–	–	ns

NOTE:
1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF.

III. CLOCK REQUIREMENTS

	COM'L.	MIL.	UNIT
Minimum Clock LOW Time	18	20	ns
Minimum Clock HIGH Time	17	20	ns
Minimum Clock Period	35	40	ns

IDT49C410
AC ELECTRICAL CHARACTERISTICS
1. SET-UP AND HOLD TIMES

INPUTS	$t_{(s)}$		$t_{(h)}$		UNIT
	COM'L.	MIL.	COM'L.	MIL.	
$D_I \rightarrow R$	16	16	0	0	ns
$D_I \rightarrow PC$	30	30	0	0	ns
I_{0-3}	35	38	0	0	ns
$\overline{CC}$	24	35	0	0	ns
$\overline{CCEN}$	24	35	0	0	ns
CI	18	18	0	0	ns
$\overline{RLD}$	19	20	0	0	ns

II. COMBINATIONAL DELAYS

INPUTS	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		UNIT
	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
D_{0-11}	20	25	–	–	–	–	ns
I_{0-3}	35	40	30	35	–	–	ns
$\overline{CC}$	30	36	–	–	–	–	ns
$\overline{CCEN}$	30	36	–	–	–	–	ns
CP	40	46	–	–	31	35	ns
$\overline{OE}$ [1]	25/27	25/30	–	–	–	–	ns

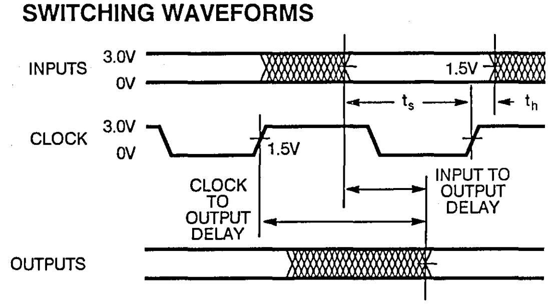
NOTE:
1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF.

III. CLOCK REQUIREMENTS

	COM'L.	MIL.	UNIT
Minimum Clock LOW Time	20	25	ns
Minimum Clock HIGH Time	20	25	ns
Minimum Clock Period	50	51	ns

8

SWITCHING WAVEFORMS



IDT49C410 INPUT/OUTPUT INTERFACE CIRCUITRY

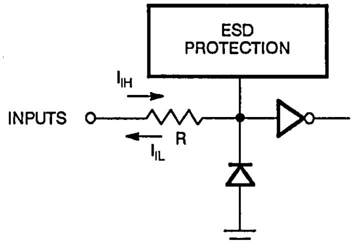


Figure 1. Input Structure

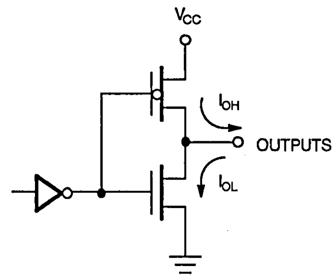


Figure 2. Output Structure

TEST LOAD CIRCUIT

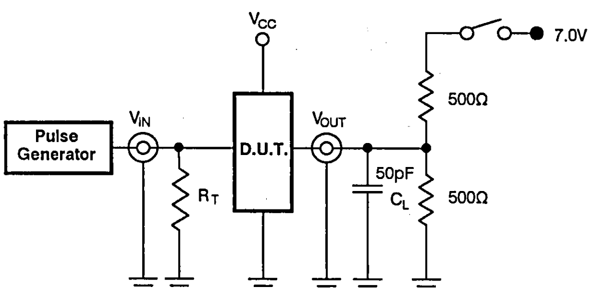


Figure 3. Switching Test Circuits

TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All other Outputs	Open

DEFINITIONS

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 3

ORDERING INFORMATION

IDT	49C410	X	X	X
	Device Type	Speed	Package	Process/ Temperature Range

Process/Temperature Range:

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

P	Plastic DIP
XC	Sidebraze SHRINK-DIP
C	Sidebraze DIP
J	PLCC
L	LCC
F	Flatpack

Speed:

Blank	16-Bit Microprogram Sequencer
A	Fast 16-Bit Microprogram Sequencer

Integrated Device Technology, Inc.

20-BIT CMOS INTERRUPTABLE MICROPROGRAM SEQUENCER

ADVANCE INFORMATION
IDT49C411

FEATURES:

- Interrupt priority handler
  - Handles up to 8 interrupts
  - Throughput of one interrupt/cycle
  - Maximum latency of 2 cycles
- 20-bit wide address path
  - Addresses up to 1Mbyte words of microprogram memory
- Two input address buses (D, A)
  - Bidirectional D bus provides access to internal stacks and ALU data path
  - Bus A provides convenient input from pipelined register
- 20-bit loop counter
  - Presettable down counter for counting loop interations and repeating instructions
  - Nested looping using loop stack
- Three independent 64-deep stacks
  - Allow for nested subroutines, interrupts and loop counters
  - Fast interrupt context switch on every clock cycle
- Multiple condition code inputs
  - Eliminates external condition code multiplexer
  - Includes ALU status flag inputs
  - Provides test and branch on <, >, =, etc.
- Multiway branch inputs
  - Allows for parallel test and branch on multiple inputs
- Incorporates Serial Protocol Channel (SPC ™)
  - On-chip diagnostics
  - Easy access to internal stacks and registers
  - Incorporates address break point detect
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C411 is a 20-bit high-performance CMOS interruptable microprogram sequencer. This flexible, yet fast sequencer is used for controlling the sequence of execution of microinstructions stored in the microprogram memory. It has been optimized for use in microprogram designs of very high-speed dedicated applications such as graphics, disk controllers, communications and DSP engines.

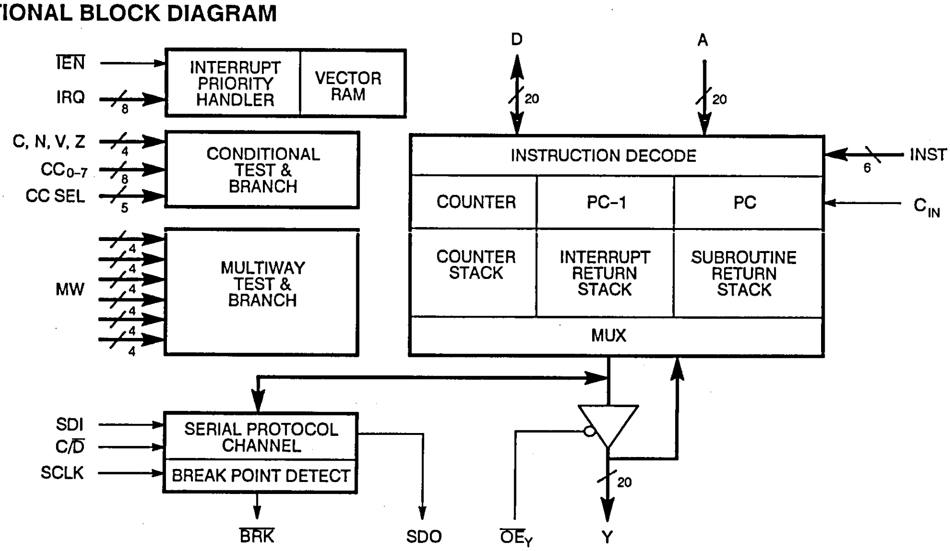
Its three bus architecture provides direct address access of up to 1 megaword of microprogram memory. The IDT49C411 includes such powerful features as a 20-bit counter/register, multiway branching, flexible condition code testing via an internal multiplexer and three independent 64-deep stacks. All three stacks enable the user to perform fast context switches every clock cycle with a maximum throughput latency of two clock cycles.

The IDT49C411 incorporates Serial Protocol Channel (SPC), an on-chip diagnostics feature which allows access to the internal stacks and registers. Also included is the provision for breakpoint detection. SPC simply and easily provides for system board and system level design verification, manufacturing test and field maintenance support.

The IDT 49C411 is fabricated using CEMOS ™, IDT's advanced CMOS technology designed for high-performance and high-reliability.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



CEMOS and SPC are registered trademarks of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

16-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT39C60A
IDT39C60-1
IDT39C60

MICROSLICE™ PRODUCT

FEATURES:

- Low power CEMOS™
  - Military: 100mA (max.)
  - Commercial: 85mA (max.)
- Fast
  - Data in to error detect
    IDT39C60A: 20ns (max.), IDT39C60-1: 25ns (max.)
    IDT39C60: 32ns (max.)
  - Data in to corrected data out
    IDT39C60A: 30ns (max.), IDT39C60-1: 52ns (max.)
    IDT39C60: 65ns (max.)
- Improves system memory reliability
  - Corrects all single-bit errors, detects all double and some triple-bit errors
- Cascadable
  - Data words up to 64 bits
- Built-in diagnostics
  - Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - Fast byte writes possible with separate byte enables
- Available in 48-pin DIP, 52-pin PLCC and LCC, as well as space-efficient 48-pin Shrink-DIP (70 mil pin centers) and 48-pin LCC
- Pin-compatible to all versions of the 2960
- Military product available compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT39C60 family are high-speed, low-power, 16-bit Error Detection and Correction Units which generate check bits on a 16-bit data field according to a modified Hamming Code and correct the data word when check bits are supplied. When performing a read operation from memory, the IDT39C60s will correct 100% of all single bit errors, will detect all double bit errors and some triple bit errors.

The IDT39C60s are easily cascadable from 16 bits up to 64 bits. Sixteen-bit systems use 6 check bits, 32-bit systems use 7 check bits and 64-bit systems use 8 check bits. For all three configurations, the error syndrome is made available.

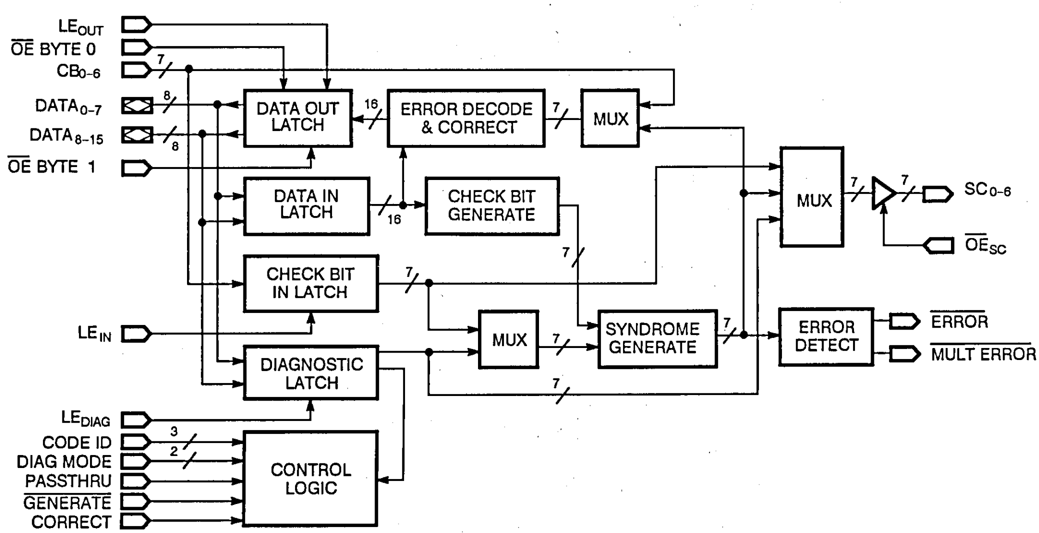
All incorporate 2 built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostic functions.

The IDT39C60s are pin-compatible, performance-enhanced functional replacements for all versions of the 2960. They are fabricated using CEMOS, a CMOS technology designed for high-performance and high-reliability. The devices are packaged in either 48-pin DIPs, or 48-pin LCC and 52-pin PLCC and LCCs.

Military grade product is manufactured in compliance to the latest revision of MIL-STD-883, Class B.

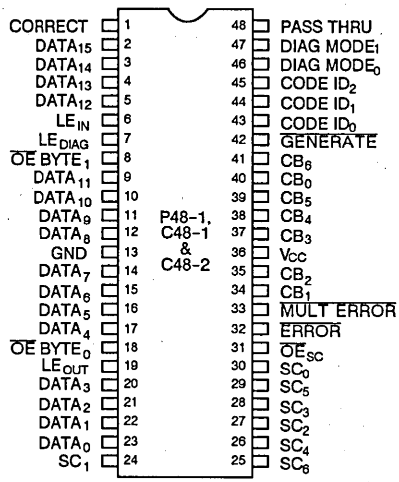
8

FUNCTIONAL BLOCK DIAGRAM

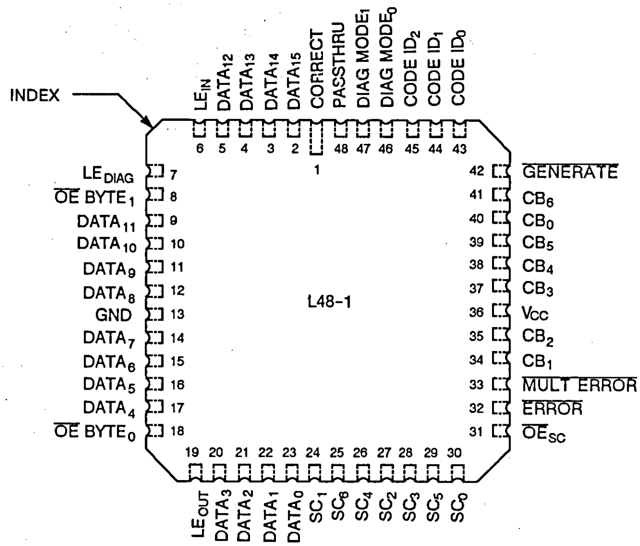


CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.

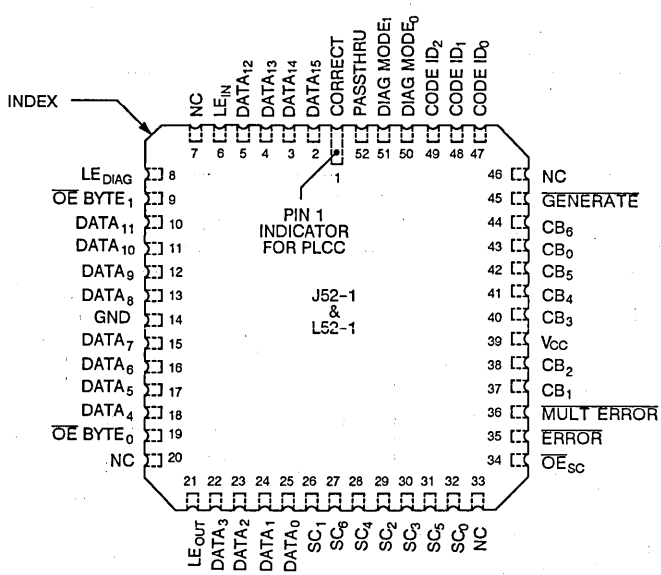
PIN CONFIGURATION



DIP
TOP VIEW
(600 mil x 100 mil CENTERS)
(400 mil x 70 mil CENTERS)



LCC
TOP VIEW
(560 mil x 650 mil)



PLCC/LCC
TOP VIEW
(750 mil x 750 mil)

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
$DATA_{0-15}$	I/O	16 bidirectional data lines. They provide input to the Data Input Latch and receive output from the Data Output Latch. $DATA_0$ is the least significant bit; $DATA_{15}$ the most significant.
CB_{0-6}	I	Seven check bit input lines. The check bit lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32- and 64-bit configurations.
LE_{IN}	I	Latch Enable – Data Input Latch. Controls latching of the input data. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.
$\overline{GENERATE}$	I	Generate Check Bits input. When this input is LOW, the EDC is in the Check Bit Generate mode. When HIGH, the EDC is in the Detect mode or Correct mode. In the Generate mode, the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. In the Detect or Correct modes the EDC detects single and multiple errors and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct mode, single-bit errors are also automatically corrected – corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates, in a coded form, the number of errors and the bit-in-error.
SC_{0-6}	O	Syndrome/Check Bit outputs. These seven lines hold the check/partial check bits when the EDC is in Generate mode and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct modes. These are 3-state outputs.
$\overline{OE}_{SC}$	I	Output Enable – Syndrome/Check Bits. When LOW, the 3-state output lines SC_{0-6} are enabled. When HIGH, the SC outputs are in the high impedance state.
$\overline{ERROR}$	O	Error Detected output. When the EDC is in Detect or Correct mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate mode, $\overline{ERROR}$ is forced HIGH. (In a 64-bit configuration, $\overline{ERROR}$ must be implemented externally.)
$\overline{MULT\ ERROR}$	O	Multiple Errors Detected output. When the EDC is in Detect or Correct mode this output, if LOW, indicates that there are two or more bit errors that have been detected. If HIGH, this indicates that either one or no errors have been detected. In Generate mode, $\overline{MULT\ ERROR}$ is forced HIGH. (In a 64-bit configuration, $\overline{MULT\ ERROR}$ must be implemented externally.)
CORRECT	I	Correct input. When HIGH, this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the EDC will drive data directly from the Data Input Latch to the Data Output Latch without correction.
LE_{OUT}	I	Latch Enable – Data Output Latch. Controls the latching of the Data Output Latch. When LOW, the Data Output Latch is latched to its previous state. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are disabled with its contents unchanged if the EDC is in Generate mode.
$\overline{OE}$ $BYTE_0$ $\overline{OE}$ $BYTE_1$	I	Output Enable – Bytes 0 and 1, Data Output Latch. These lines control the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW, these lines enable the Data Output Latch and, when HIGH, these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output Latch at a time.
PASS THRU	I	Pass Thru input. This line, when HIGH, forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SC_{0-6}) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.
DIAG $MODE_{0-1}$	I	Diagnostic Mode Select. These two lines control the initialization and diagnostic operation of the EDC.
CODE ID_{0-2}	I	Code Identification inputs. These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16, 32, and 64 bits and their respective modified Hamming codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID_2, ID_1, ID_0) is also used to instruct the EDC that the signals CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASSTHRU are to be taken from the diagnostic latch rather than the control lines.
LE DIAG	I	Latch Enable – Diagnostic Latch. The Diagnostic Latch follows the 16-bit data on the input lines when HIGH. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASSTHRU.

PRODUCT DESCRIPTION

The IDT39C60 EDC Unit is a powerful 16-bit cascadable slice used for check bit generation, error detection, error correction and diagnostics. As shown in the Functional Block Diagram, the device consists of the following:

- Data Input Latch
- Data Output Latch
- Diagnostic Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Control Logic

DATA INPUT/OUTPUT/DIAGNOSTIC LATCHES

The LE_{IN}, Latch Enable input, controls the Data Input Latch which can load 16 bits of data from the bidirectional DATA lines. The input data is used for either check bit generation or error detection/correction.

The 16 bits of data from the DATA lines can be loaded into the Diagnostic Latch under control of the Diagnostic Latch Enable, LE_{DIAG}, giving check bit information in one byte and control information in the other byte. The Diagnostic Latch is used when in Internal Control mode or in one of the Diagnostic modes.

The Data Output Latch is split into 2 bytes and enabled onto the DATA lines through separate byte control lines. The Data Output Latch stores the result of an error correction operation or is loaded directly from the Data Input Latch under control of the Latch Enable Out (LE_{OUT}). The PASSTHRU control input determines which data is loaded.

CHECK BIT GENERATION LOGIC

This block of combinational logic generates 7 check bits using a modified Hamming code from the 16 bits of data input from the Data Input Latch.

SYNDROME GENERATION LOGIC

This logic compares the check bits generated through the Check Bit Generator with either the check bits in the Check Bit Input Latch or 7 bits assigned in the Diagnostic Latch.

Syndrome bits are produced by an exclusive-OR of the two sets of bits. A match indicates no errors. If errors occur, the syndrome bits can be decoded to indicate the bit in error, whether 2 errors were detected or 3 or more errors.

ERROR DETECTION/CORRECTION LOGIC

The syndrome bits generated by the Syndrome Logic are decoded and used to control the $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ outputs. If one or more errors are detected, $\overline{\text{ERROR}}$ goes low. If two or more errors are detected, both $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ go low. Both outputs remain high when there are no errors detected.

For single bit errors, the correction logic will complement (correct) the bit in error, which can then be loaded into the Data Out Latches under the LE_{OUT} control. If check bit errors need to be corrected, then the device must be operated in the Generate mode.

CONTROL LOGIC

The control logic determines the specific mode of operation, usually from external control signals. However, the Internal Control mode allows these signals to be provided from the Diagnostic Latch.

DETAILED PRODUCT DESCRIPTION

The IDT39C60 EDC Unit contains the logic necessary to generate check bits on a 16-bit data input according to a modified Hamming code. The EDC can compare internally generated check bits against those read with the 16-bit data to allow correction of any single bit data error and detection of all double and some triple bit errors. The IDT39C60 can be used for 16-bit data words (6 check bits), 32-bit data words (7 check bits) or 64-bit data words (8 check bits).

CODE AND BYTE SELECTION

The 3 code identification pins, ID_{2-0}, are used to determine the data word size from 16, 32 or 64 bits and the byte position of each 16-bit IDT39C60 EDC device.

Code 16/22 refers to a 16-bit data field with 6 check bits.
Code 32/39 refers to a 32-bit data field with 7 check bits.
Code 64/72 refers to a 64-bit data field with 8 check bits.

The ID_{2-0} of 001 is used to place the device in the Internal Control mode as described later in this section.

Table 1 defines all possible identification codes.

CHECK AND SYNDROME BITS

The IDT39C60 provides either check bits or syndrome bits on the three-state output pins SC_{0-6}. Check bits are generated from a combination of the Data Input bits, while syndrome bits are an Exclusive-OR of the check bits generated from read data with the read check bits stored with the data. Syndrome bits can be decoded to determine the single bit in error or that a double error was detected. Some triple bit errors are also detected. The check bits are labeled:

CX, C0, C1, C2, C4	for the 8-bit configuration
CX, C0, C1, C2, C4, C8	for the 16-bit configuration
CX, C0, C1, C2, C4, C8, C16	for the 32-bit configuration
CX, C0, C1, C2, C4, C8, C16, C32	for the 64-bit configuration

Syndrome bits are similarly labeled SX through S32.

CONTROL MODE SELECTION

Tables 2 and 3 describe the 9 operating modes of the IDT39C60. The Diagnostic mode pins, DIAG $MODE_{1-0}$, define 4 basic areas of operation, with $\overline{\text{GENERATE}}$, CORRECT and PASSTHRU, further dividing operation into 8 functions with the ID_{2-0} defining the ninth mode as the Internal mode.

Generate mode is used to display the check bits on the outputs SC_{0-6}. The Diagnostic Generate mode displays check bits as stored in the Diagnostic Latch.

Detect mode provides an indication of errors or multiple errors on the outputs $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$. Single bit errors are not corrected in this mode. The syndrome bits are provided on the outputs SC_{0-6}. For the Diagnostic Detect mode, the syndrome bits are generated by comparing the internally generated check bits from the Data In Latch with check bits stored in the diagnostic latch rather than with the check bit latch contents.

Correct mode is similar to the Detect mode except that single bit errors will be complemented (corrected) and made available as input to the Data Out Latch. Again, the Diagnostic Correct mode will correct single bit errors as determined by syndrome bits generated from the Data Input and contents of the Diagnostic Latch.

The Initialize mode provides check bits for all zero bit data. Data In Latch is set and latched to a logic zero and made available as input to the Data Out Latch.

The Internal mode disables the external control pins DIAG $MODE_{1-0}$, CORRECT, PASSTHRU and CODE ID to be defined by the Diagnostic Latch. When in the internal mode, the diagnostic latch should have the CODE ID different from 001 as this would represent an invalid operation.

TABLE 1. HAMMING CODE AND SLICE IDENTIFICATION

CODE ID_2	CODE ID_1	CODE ID_0	HAMMING CODE AND SLICE SELECTED
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Bytes 0 and 1
0	1	1	Code 32/39, Bytes 2 and 3
1	0	0	Code 64/72, Bytes 0 and 1
1	0	1	Code 64/72, Bytes 2 and 3
1	1	0	Code 64/72, Bytes 4 and 5
1	1	1	Code 64/72, Bytes 6 and 7

TABLE 2. DIAGNOSTIC MODE CONTROL

DIAG $MODE_1$	DIAG $MODE_0$	DIAGNOSTIC MODE SELECTED
0	0	**Non-diagnostic mode.** The EDC functions normally in all modes.
0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate mode. The EDC functions normally in the Detect or Correct modes.
1	0	**Diagnostic Detect/Correct.** In the Detect or Correct mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate mode.
1	1	**Initialize.** The outputs of the Data Input Latch are forced to zeroes and the check bits generated correspond to the all zero data. The latch is not reset, a functional difference from the Am2960.

TABLE 3. IDT39C60 OPERATING MODES

OPERATING MODE	DM1	DM0	$\overline{\text{GENERATE}}$	CORRECT	PASS-THRU	DATA OUT LATCH (LE_{OUT} = HIGH)	SC_{0-6} ($\overline{OE}_{SC}$ = LOW)	$\overline{\text{ERROR}}$ $\overline{\text{MULT ERROR}}$
Generate	0 1	0 0	0	X	0	–	Check Bits Generated from Data In Latch	–
Detect	0 0	0 1	1	0	0	Data In Latch	Syndrome Bits Data In/Check Bit Latch	Error Dep[1]
Correct	0 0	0 1	1	1	0	Data In Latch with Single Bit Correction	Syndrome Bits Data In/Check Bit Latch	Error Dep
PASSTHRU	0 0 1	0 1 0	X	X	1	Data In Latch	Check Bit Latch	High
Diagnostic Generate	0	1	0	X	0	–	Check Bits from Diagnostic Latch	–
Diagnostic Detect	1	0	1	0	0	Data In Latch	Syndrome Bits Data In/Diagnostic Latch	Error Dep
Diagnostic Correct	1	0	1	1	0	Data In Latch with Single Bit Correction	Syndrome Bits Data In/Diagnostic Latch	Error Dep
Initialization Mode	1	1	X	X	X	Data In Latch Set to 0000	Check Bits Generated from Data In Latch (0000)	–
Internal Mode	ID_{2-0} = 001 Control Signals ID_{2-0}, DIAG $MODE_{1-0}$, CORRECT and PASSTHRU are taken from the Diagnostic Latch							

NOTE:
1. ERROR DEP (Error Dependent): $\overline{\text{ERROR}}$ will be low for single or multiple errors, with $\overline{\text{MULT ERROR}}$ low for double or multiple errors. Both signals are high for no errors.

16-BIT DATA WORD CONFIGURATION

Figure 1 indicates the 22-bit data format for two bytes of data and 6 check bits.

A single IDT39C60 EDC Unit, connected as shown in Figure 2, provides all logic needed for single bit error correction and double bit error detection of a 16-bit data field. The identification code 16/22 indicated 6 check bits are required. The CB_6 pin is, therefore, a "Don't Care" and ID_2, ID_1, ID_0 = 000.

DATA		CHECK BITS					
$BYTE_1$	$BYTE_0$	CX	C0	C1	C2	C4	C8
15 8	7 0						

USES MODIFIED HAMMING CODE 16/22
16 DATA BITS WITH 6 CHECK BITS

Figure 1. 16-Bit Data Format

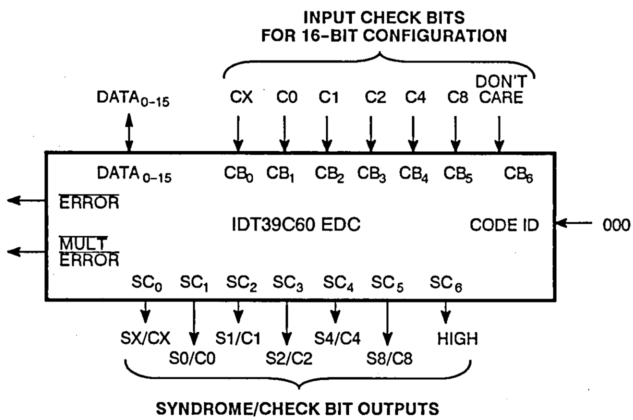


Figure 2. 16-Bit Configuration

Table 3 describes the operating modes available. The output pin SC_6, is forced high for either syndrome or check bits since only 6 check bits are used for the 16/22 code.

Table 4 indicates the data bits participating in the check bit generation. For example, check bit C0 is the Exclusive-OR function or the 8 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization mode. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate mode.

TABLE 4. 16-BIT MODIFIED HAMMING CODE—CHECK BIT ENCODE CHART [1]

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X

NOTE:
1. The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 5 indicates the decoding of the six syndrome bits to indicate the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 6 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-5} outputs. The Internal mode substitutes the indicated bit position for the external control signals.

TABLE 5.
SYNDROME DECODE TO BIT-IN-ERROR (1)

SYNDROME BITS S8 / S4 / S2 — SX S0 S1	0 0 0	1 0 0	0 1 0	1 1 0	0 0 1	1 0 1	0 1 1	1 1 1
0 0 0	*	C8	C4	T	C2	T	T	M
0 0 1	C1	T	T	15	T	13	7	T
0 1 0	C0	T	T	M	T	12	6	T
0 1 1	T	10	4	T	0	T	T	M
1 0 0	CX	T	T	14	T	11	5	T
1 0 1	T	9	3	T	M	T	T	M
1 1 0	T	8	2	T	1	T	T	M
1 1 1	M	T	T	M	T	M	M	T

NOTE:
1. * = No errors detected
Number = Number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

TABLE 6.
DIAGNOSTIC LATCH LOADING—16-BIT FORMAT

DATA BIT	INTERNAL FUNCTION
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	CODE ID_0
9	CODE ID_1
10	CODE ID_2
11	DIAG $MODE_0$
12	DIAG $MODE_1$
13	CORRECT
14	PASS THRU
15	Don't Care

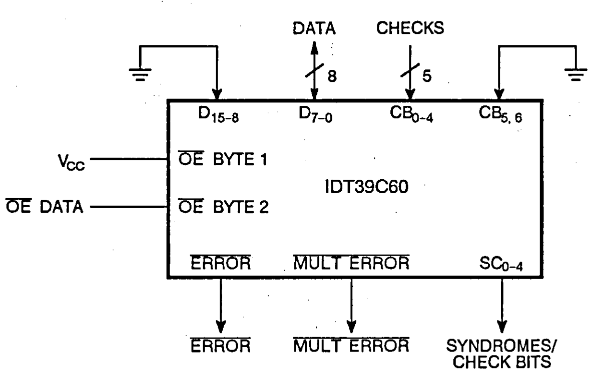


Figure 3. 8-Bit Configuration

32-BIT DATA WORD CONFIGURATION

Two IDT39C60 EDC Units, connected as shown in Figure 5, provide all logic needed for single bit error correction and double bit error detection of a 32-bit data field. The Identification code 32/39 indicates 7 check bits are required. Table 1 gives the ID_2, ID_1, ID_0 values needed for distinguishing the byte 0/1 from byte 2/3. Valid syndrome, check bits and the $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ signal come from the byte 2/3 unit. Control signals not indicated are connected to both units in parallel. The $\overline{OE}_{SC}$ always enables the SC_{0-6} outputs of byte 0/1, but must be used to select data check bits or syndrome bits fed back from the byte 2/3 for data correction modes.

Data In bits 0 through 15 are connected to the same numbered inputs of the byte 0/1 EDC unit, while Data In bits 16 through 31 are connected to byte 2/3 Data Inputs 0 to 15, respectively.

Figure 4 indicates the 39-bit data format of 4 bytes of data and 7 check bits. Check bits are input to the byte 0/1 unit through a tri-state buffer unit such as the IDT74FCT244. Correction of single bit errors of the 32-bit configuration requires a feedback of syndrome bits from byte 2/3 into the byte 1/0 unit. The MUX shown on the functional block diagram is used to select the CB_{0-6} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating modes available for the 32/39 configuration.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 7 indicates the decoding of the 7 syndrome bits to determine the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Performance data is provided in Table 8 in relating a single IDT39C60 EDC with the two cascaded units of Figure 5. As indicated, a summation of propagation delays is required from the cascading arrangement of EDC units.

Table 9 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-6} outputs. The Internal mode substitutes the indicated bit position for the external control signals.

Table 10 indicates the Data Bits participating in the check bit generation. For example, check bit C0 is the Exclusive-OR function of the 16 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization mode. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate mode.

TABLE 7.
SYNDROME DECODE TO BIT-IN-ERROR FOR 32 BITS (1)

SYNDROME BITS S16 / S8 / S4 → SX S0 S1 S2 ↓	0 0 0	1 0 0	0 1 0	1 1 0	0 0 1	1 0 1	0 1 1	1 1 1
0 0 0 0	*	C16	C8	T	C4	T	T	30
0 0 0 1	C2	T	T	27	T	5	M	T
0 0 1 0	C1	T	T	25	T	3	15	T
0 0 1 1	T	M	13	T	23	T	T	M
0 1 0 0	C0	T	T	24	T	2	M	T
0 1 0 1	T	1	12	T	22	T	T	M
0 1 1 0	T	M	10	T	20	T	T	M
0 1 1 1	16	T	T	M	T	M	M	T
1 0 0 0	CX	T	T	M	T	M	14	T
1 0 0 1	T	M	11	T	21	T	T	M
1 0 1 0	T	M	9	T	19	T	T	31
1 0 1 1	M	T	T	29	T	7	M	T
1 1 0 0	T	M	8	T	18	T	T	M
1 1 0 1	17	T	T	28	T	6	M	T
1 1 1 0	M	T	T	26	T	4	M	T
1 1 1 1	T	0	M	T	M	T	T	M

NOTE:
1. * = No errors detected
Number = Number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

TABLE 8.
KEY AC CALCULATIONS FOR THE 32-BIT CONFIGURATION

32-BIT PROPAGATION DELAY FROM	TO	COMPONENT DELAY FROM IDT39C60 AC SPECIFICATIONS
DATA	Check Bits Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	Corrected DATA Out	(DATA to SC) + (CB to SC, Code ID 011) + (CB to DATA, CODE ID 010)
DATA	Syndromes Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	$\overline{\text{ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{ERROR}}$, CODE ID 011)
DATA	$\overline{\text{MULT ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 011)

DATA				CHECK BITS						
$BYTE_3$	$BYTE_2$	$BYTE_1$	$BYTE_0$	CX	C0	C1	C2	C4	C8	C16
31 24	23 16	15 8	7 0							

USES MODIFIED HAMMING CODE 32/39
32 DATA BITS WITH 7 CHECK BITS

Figure 4. 32-Bit Data Format

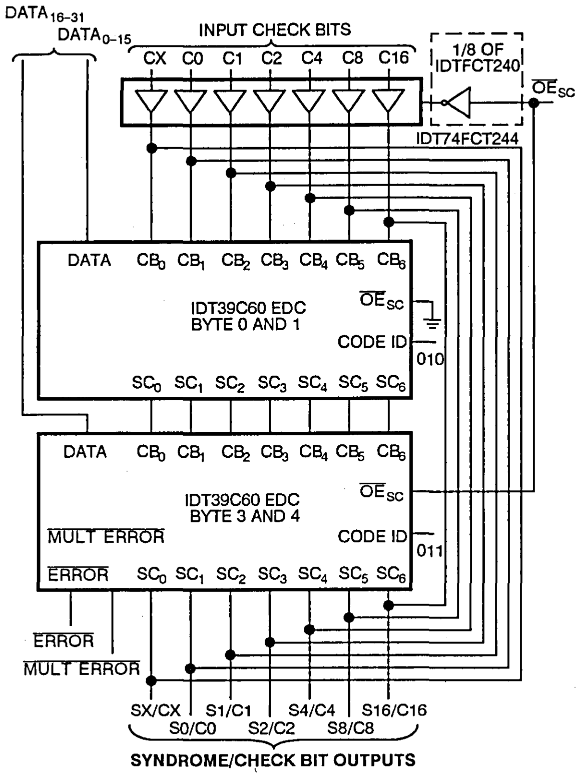


Figure 5. 32-Bit Configuration

TABLE 9. DIAGNOSTIC LATCH LOADING – 32-BIT FORMAT

DATA BIT	INTERNAL FUNCTION
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6	Diagnostic Check Bit 16
7	Don't Care
8	Slice 0/1 – CODE ID_0
9	Slice 0/1 – CODE ID_1
10	Slice 0/1 – CODE ID_2
11	Slice 0/1 – DIAG $MODE_0$
12	Slice 0/1 – DIAG $MODE_1$
13	Slice 0/1 – CORRECT
14	Slice 0/1 – PASSTHRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 – CODE ID_0
25	Slice 2/3 – CODE ID_1
26	Slice 2/3 – CODE ID_2
27	Slice 2/3 – DIAG $MODE_0$
28	Slice 2/3 – DIAG $MODE_1$
29	Slice 2/3 – CORRECT
30	Slice 2/3 – PASS THRU
31	Don't Care

TABLE 10. 32-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)	X				X		X	X	X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X					X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X

8

64-BIT DATA WORD CONFIGURATION

The IDT39C60 EDC Units connected with the MSI gates, as shown in Figure 6, provide the logic needed for single bit error correction and double bit error detection of a 64-bit data field. The Identification code 64/72 is used, indicating 8 check bits are required. Check bits and Syndrome bits are generated external to the IDT39C60 EDC using Exclusive-OR gates. For error correction, the syndrome bits must be fed back to the CB_{0-6} inputs. Thus, external tri-state buffers are used to select between the check bits read in from memory and the syndrome bits being fed back.

The $\overline{\text{ERROR}}$ signal is low for one or more errors detected. From any of the 4 devices, $\overline{\text{MULT ERROR}}$ is low for some double bit errors and for all three bit errors. Both are high otherwise. The DOUBLE ERROR signal is high only when a double bit error is detected.

Figure 6 indicates the 72-bit data format of eight bytes of data and 8 check bits. Check bits are input to the various units through a tri-state buffer such as the IDT74FCT244. Correction of single bit errors of the 64-bit configuration requires a feedback of syndrome bits as generated external to the IDT39C60 EDC. The MUX shown on the functional block diagram is used to select the CB_{0-6} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating modes available for the 64/72 configuration.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 11 indicates the decoding of the 8 syndrome bits to determine the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Performance data is provided in Table 12 in relating a single IDT39C60 EDC with the four units of Figure 7. Delay through the exclusive, or MSI, gates and the 3-state buffer must be included.

Table 13 indicates the Data Bits participating in the check bit generation. For example, check bit C0 is the Exclusive-OR function or the 32 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization mode. In the PASSTHRU mode, the contents of the check bit latch are passed through the external Exclusive-OR gates and appear inverted at the outputs labeled CX to C32.

Table 14 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-6} outputs. The Internal mode substitutes the indicated bit position for the external control signals.

DATA								CHECK BITS							
$BYTE_7$	$BYTE_6$	$BYTE_5$	$BYTE_4$	$BYTE_3$	$BYTE_2$	$BYTE_1$	$BYTE_0$	CX	C0	C1	C2	C4	C8	C16	C32
63 56	55 48	47 40	39 32	31 24	23 16	15 8	7 0								

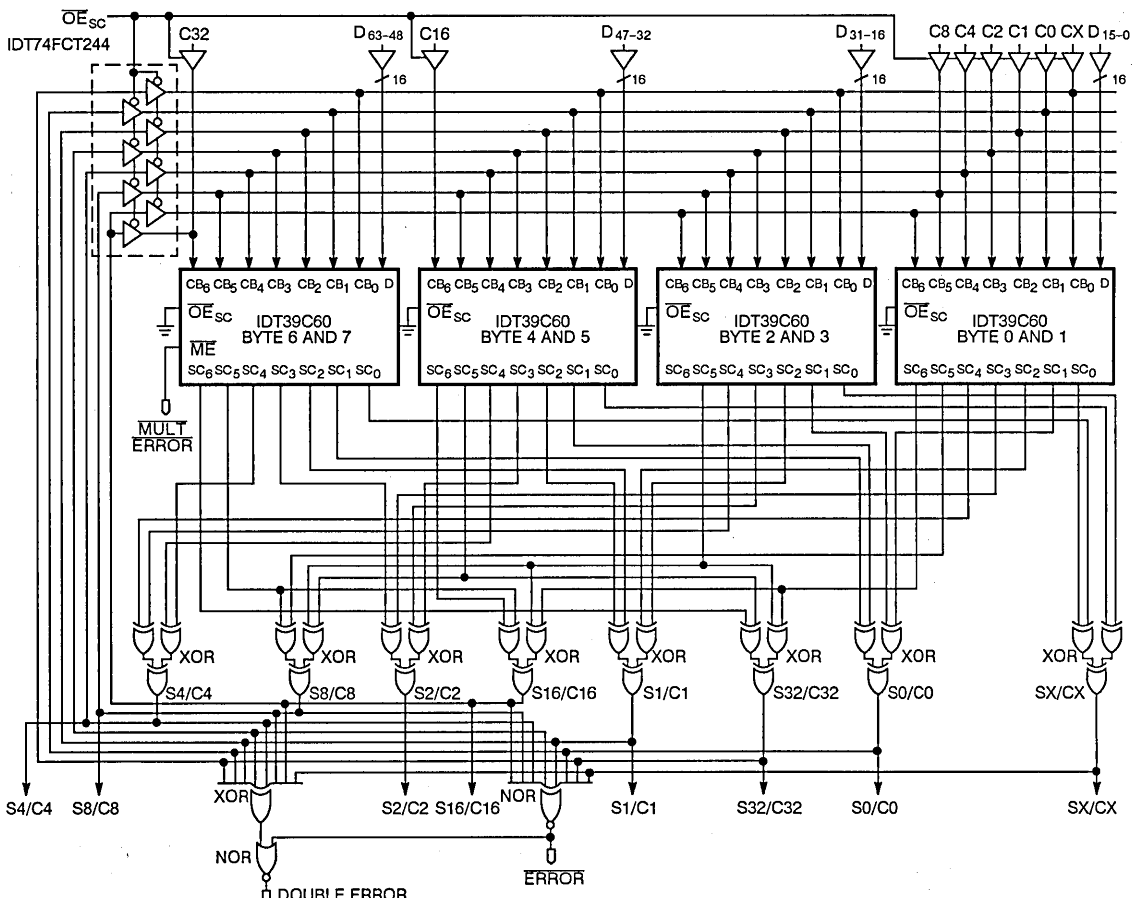
USES MODIFIED HAMMING CODE 64/72
64 DATA BITS WITH 8 CHECK BITS

Figure 6. 64-Bit Data Format

TABLE 11. SYNDROME DECODE TO BIT-IN-ERROR [1]

SYNDROME BITS																
S32	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
S16	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
S8	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
SX S0 S1 S2																
0 0 0 0	*	C32	C16	T	C8	T	T	M	C4	T	T	M	T	46	62	T
0 0 0 1	C2	T	T	M	T	43	59	T	T	53	37	T	M	T	T	M
0 0 1 0	C1	T	T	M	T	41	57	T	T	51	35	T	15	T	T	31
0 0 1 1	T	M	M	T	13	T	T	29	23	T	T	7	T	M	M	T
0 1 0 0	C0	T	T	M	T	40	56	T	T	50	34	T	M	T	T	M
0 1 0 1	T	49	33	T	12	T	T	28	22	T	T	6	T	M	M	T
0 1 1 0	T	M	M	T	10	T	T	26	20	T	T	4	T	M	M	T
0 1 1 1	16	T	T	0	T	M	M	T	T	M	M	T	M	T	T	M
1 0 0 0	CX	T	T	M	T	M	M	T	T	M	M	T	14	T	T	30
1 0 0 1	T	M	M	T	11	T	T	27	21	T	T	5	T	M	M	T
1 0 1 0	T	M	M	T	9	T	T	25	19	T	T	3	T	47	63	T
1 0 1 1	M	T	T	M	T	45	61	T	T	55	39	T	M	T	T	M
1 1 0 0	T	M	M	T	8	T	T	24	18	T	T	2	T	M	M	T
1 1 0 1	17	T	T	1	T	44	60	T	T	54	38	T	M	T	T	M
1 1 1 0	M	T	T	M	T	42	58	T	T	52	36	T	M	T	T	M
1 1 1 1	T	48	32	T	M	T	T	M	M	T	T	M	T	M	M	T

NOTE:
1. * = No errors detected, T = Two errors detected, Number = The number of the single bit-in-error, M = More than two errors detected.



NOTES:

1. In PASSTHRU mode the contents of the Check Latch appear on the XOR outputs inverted.
2. In Diagnostic Generate mode the contents of the Diagnostic Latch appear on the XOR outputs inverted.

Figure 7. 64-Bit Configuration

TABLE 12. KEY AC CALCULATIONS FOR THE 64-BIT CONFIGURATION

64-BIT PROPAGATION DELAY		COMPONENT DELAY FROM IDT39C60 AC SPECIFICATIONS
FROM	TO	
DATA	Check Bits Out	(DATA to SC) + (XOR Delay)
DATA	Corrected DATA Out	(DATA to SC) + (XOR Delay) + (Buffer DELAY) + (CB to DATA, CODE ID 1xx)
DATA	Syndromes	(DATA to SC) + (XOR Delay)
DATA	ERROR for 64-Bits	(DATA to SC) + (XOR Delay) + (NOR Delay)
DATA	MULT ERROR for 64-Bits	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to MULT ERROR, CODE ID 1xx)
DATA	DOUBLE ERROR for 64-Bits	(DATA to SC) + (XOR Delay) + (XOR/NOR Delay)

TABLE 13. 64-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART [1]

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)									X	X	X	X	X	X	X	X

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)									X	X	X	X	X	X	X	X

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)	X	X	X	X	X	X	X	X								

NOTE:

1. The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

TABLE 14.
DIAGNOSTIC LATCH LOADING – 64-BIT FORMAT

DATA BIT	INTERNAL FUNCTION
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	Slice 0/1 – CODE ID_0
9	Slice 0/1 – CODE ID_1
10	Slice 0/1 – CODE ID_2
11	Slice 0/1 – DIAG $MODE_0$
12	Slice 0/1 – DIAG $MODE_1$
13	Slice 0/1 – CORRECT
14	Slice 0/1 – PASSTHRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 – CODE ID_0
25	Slice 2/3 – CODE ID_1
26	Slice 2/3 – CODE ID_2
27	Slice 2/3 – DIAG $MODE_0$
28	Slice 2/3 – DIAG $MODE_1$
29	Slice 2/3 – CORRECT
30	Slice 2/3 – PASSTHRU
31	Don't Care
32-37	Don't Care
38	Diagnostic Check Bit 16
39	Don't Care
40	Slice 4/5 – CODE ID_0
41	Slice 4/5 – CODE ID_1
42	Slice 4/5 – CODE ID_2
43	Slice 4/5 – DIAG $MODE_0$
44	Slice 4/5 – DIAG $MODE_1$
45	Slice 4/5 – CORRECT
46	Slice 4/5 – PASSTHRU
47	Don't Care
48-54	Don't Care
55	Diagnostic Check Bit 32
56	Slice 6/7 – CODE ID_0
57	Slice 6/7 – CODE ID_1
58	Slice 6/7 – CODE ID_2
59	Slice 6/7 – DIAG $MODE_0$
60	Slice 6/7 – DIAG $MODE_1$
61	Slice 6/7 – CORRECT
62	Slice 6/7 – PASSTHRU
63	Don't Care

Some multiple errors will cause a data bit to be inverted. For example, in the 16-bit mode where bits 8 and 13 are in error, the syndrome 1111000 (SC, S0, S1, S2, S4, S8) is produced. The bit-in-error decoder receives the syndrome 11100 (S0, S1, S2, S4, S8) which it decodes as a single error in data bit 0 and inverts that bit. Figure 8 indicates a method for inhibition correction when a multiple error occurs.

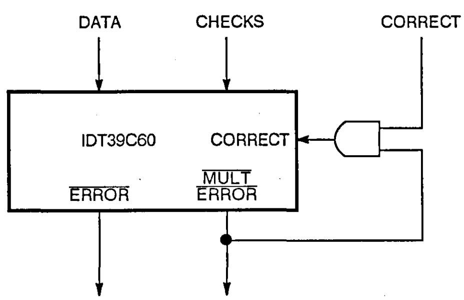


Figure 8. Inhibition of Data Modification

FUNCTIONAL EQUATIONS

The following equations and tables describe in detail how the output values of the IDT39C60 EDC are determined as a function of the value of the inputs and the internal states. Be sure to carefully read the following definitions of symbols before examining the tables.

DEFINITIONS

D_i ← $DATA_i$ if LE_{IN} is HIGH or the output of bit i of the Data Input Latch if LE_{IN} is LOW
C_i ← CB_i if LE_{IN} is HIGH or the output of bit i of the Check Bit Latch if LE_{IN} is LOW
DL_i ← Output of bit i of the Diagnostic Latch
S_i ← Internally generated syndromes (same as outputs of SC_i if outputs enabled)
PA ← $D_0 \oplus D_1 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \oplus D_{12}$
PB ← $D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7$
PC ← $D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14}$
PD ← $D_0 \oplus D_3 \oplus D_4 \oplus D_7 \oplus D_9 \oplus D_{10} \oplus D_{13} \oplus D_{15}$
PE ← $D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{11} \oplus D_{12} \oplus D_{13}$
PF ← $D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_{14} \oplus D_{15}$
PG_1 ← $D_1 \oplus D_4 \oplus D_6 \oplus D_7$
PG_2 ← $D_1 \oplus D_2 \oplus D_3 \oplus D_5$
PG_3 ← $D_8 \oplus D_9 \oplus D_{11} \oplus D_{14}$
PG_4 ← $D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15}$

Error Signals

$\overline{ERROR}$: ← $(\overline{S6} \cdot \overline{(ID_1 + ID_2)}) \cdot \overline{S5} \cdot \overline{S4} \cdot \overline{S3} \cdot \overline{S2} \cdot \overline{S1} \cdot \overline{S0}$ + GENERATE + INITIALIZE + PASSTHRU

$\overline{MULT\ ERROR}$:
(16 and 32-Bit Modes) ← $\overline{((\overline{S6 \cdot ID_1}) \oplus S5 \oplus S4 \oplus S3 \oplus S2 \oplus S1 \oplus S0)\ (ERROR) + TOME}$ + GENERATE + PASSTHRU + INITIALIZE

$\overline{MULT\ ERROR}$: (64-Bit Modes) ← $\overline{TOME}$ + GENERATE + PASSTHRU + INITIALIZE

TABLE 15. TOME (Three or More Errors) [1]

		S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
		[2]S6	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
		S5	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
		S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
S1	S2	S3																
0	0	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0
0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

NOTES:

1. S6, S5, . . . S0 are internal syndromes except in Modes 010, 100, 101, 110, 111 (CODE ID_2, ID_1, ID_0). In these modes, the syndromes are input over the check bit lines. S6 ← C6, S5 ← C5, . . . S1 ← C1, S0 ← C0.
2. The S6 internal syndrome is always forced to 0 in CODE ID 000.

SC OUTPUTS

Tables 16, 17, 18, 19, 20 show how outputs SC_{0-6} are generated in each control mode for various CODE IDs (internal control mode not applicable).

TABLE 16. GENERATE MODE (Check Bits)

GENERATE MODE (CHECK BITS)	CODE ID_{2-0}						
	000	010	011	100	101	110	111
SC_0 ←	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_3$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
SC_1 ←	PA	PA	$PA \oplus CB_1$	PA	PA	PA	PA
SC_2 ←	$\overline{PD}$	$\overline{PD}$	$PD \oplus CB_2$	$\overline{PD}$	PD	PD	PD
SC_3 ←	$\overline{PE}$	$\overline{PE}$	$PE \oplus CB_3$	$\overline{PE}$	PE	PE	PE
SC_4 ←	PF	PF	$PF \oplus CB_4$	PF	PF	PF	PF
SC_5 ←	PC	PC	$PC \oplus CB_5$	PC	PC	PC	PC
SC_6 ←	1	PB	$PC \oplus CB_6$	PB	PB	PB	PB

TABLE 17. DETECT AND CORRECT MODES (Syndromes)

DETECT AND CORRECT MODES (SYNDROMES)	CODE ID_{2-0}						
	000	010	011 [1]	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus C0$	$PG_1 \oplus PG_3 \oplus C0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus C0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus C1$	$PA \oplus C1$	$PA \oplus CB_1$	$PA \oplus C1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus C2$	$\overline{PD} \oplus C2$	$PD \oplus CB_2$	$\overline{PD} \oplus C2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus C3$	$\overline{PE} \oplus C3$	$PE \oplus CB_3$	$\overline{PE} \oplus C3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus C4$	$PF \oplus C4$	$PF \oplus CB_4$	$PF \oplus C4$	PF	PF	PF
$SC_5 \leftarrow$	$PC \oplus C5$	$PC \oplus C5$	$PC \oplus CB_5$	$PC \oplus C5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus C6$	$PC \oplus CB_6$	PB	PB	$PB \oplus C6$	$PB \oplus C6$

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

TABLE 18. DIAGNOSTIC READ MODE

DIAGNOSTIC READ MODE	CODE ID_{2-0}						
	000	010	011 [1]	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_1 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus DL_1$	$PA \oplus DL_1$	$PA \oplus CB_1$	$PA \oplus DL_1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus DL_2$	$\overline{PD} \oplus DL_2$	$PD \oplus CB_2$	$\overline{PD} \oplus DL_2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus DL_3$	$\overline{PE} \oplus DL_3$	$PE \oplus CB_3$	$\overline{PE} \oplus DL_3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus DL_4$	$PF \oplus DL_4$	$PF \oplus CB_4$	$PF \oplus DL_4$	PF	PF	PF
$SC_5 \leftarrow$	$PC \oplus DL_5$	$PC \oplus DL_5$	$PC \oplus CB_5$	$PC \oplus DL_5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus DL_6$	$PC \oplus CB_6$	PB	PB	$PB \oplus DL_6$	$PB \oplus DL_7$

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

TABLE 19. DIAGNOSTIC WRITE MODE

DIAGNOSTIC WRITE MODE	CODE ID_{2-0}						
	000	010	011 [1]	100	101	110	111
$SC_0 \leftarrow$	DL_0	DL_0	CB_0	DL_0	1	1	1
$SC_1 \leftarrow$	DL_1	DL_1	CB_1	DL_1	1	1	1
$SC_2 \leftarrow$	DL_2	DL_2	CB_2	DL_2	1	1	1
$SC_3 \leftarrow$	DL_3	DL_3	CB_3	DL_3	1	1	1
$SC_4 \leftarrow$	DL_4	DL_4	CB_4	DL_4	1	1	1
$SC_5 \leftarrow$	DL_5	DL_5	CB_5	DL_5	1	1	1
$SC_6 \leftarrow$	1	DL_6	CB_6	1	1	DL_6	DL_7

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

TABLE 20. PASSTHRU MODE

PASSTHRU MODE	CODE ID_{2-0}						
	000	010	011 [1]	100	101	110	111
$SC_0 \leftarrow$	C_0	C_0	CB_0	C_0	1	1	1
$SC_1 \leftarrow$	C_1	C_1	CB_1	C_1	1	1	1
$SC_2 \leftarrow$	C_2	C_2	CB_2	C_2	1	1	1
$SC_3 \leftarrow$	C_3	C_3	CB_3	C_3	1	1	1
$SC_4 \leftarrow$	C_4	C_4	CB_4	C_4	1	1	1
$SC_5 \leftarrow$	C_5	C_5	CB_5	C_5	1	1	1
$SC_6 \leftarrow$	1	C_6	CB_6	1	1	C_6	C_6

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

TABLE 21. CODE ID_{2-0} = 000 (1)

		S5	0	0	0	0	1	1	1	1
		S4	0	0	1	1	0	0	1	1
S2	S1	S3	0	1	0	1	0	1	0	1
0	0		–	–	–	5	–	11	14	–
0	1		–	1	2	6	8	12	–	–
1	0		–	–	3	7	9	13	15	–
1	1		–	0	4	–	10	–	–	–

NOTE:
1. Unlisted S combinations are no correction.

TABLE 22. CODE ID_{2-0} = 010 (1)

		CB6	0	0	0	0	1	1	1	1
		CB5	1	1	1	1	0	0	0	0
		CB4	0	0	1	1	0	0	1	1
CB2	CB1	CB3	0	1	0	1	0	1	0	1
0	0		–	11	14	–	–	–	–	5
0	1		8	12	–	–	–	1	2	6
1	0		9	13	15	–	–	–	3	7
1	1		10	–	–	–	–	0	4	–

NOTE:
1. Unlisted CB combinations are no correction.

TABLE 23. CODE ID_{2-0} = 011 (1)

		S6	0	0	0	0	1	1	1	1
		S5	0	0	0	0	1	1	1	1
		S4	0	0	1	1	0	0	1	1
S2	S1	S3	0	1	0	1	0	1	0	1
0	0		–	–	–	5	–	11	14	–
0	1		–	1	2	6	8	12	–	–
1	0		–	–	3	7	9	13	15	–
1	1		–	0	4	–	10	–	–	–

NOTE:
1. Unlisted S combinations are no correction.

TABLE 24. CODE ID_{2-0} = 100 (1)

		CB0	0	0	0	0	1	1	1	1
		CB6	0	0	0	0	1	1	1	1
		CB5	1	1	1	1	0	0	0	0
		CB4	0	0	1	1	0	0	1	1
CB2	CB1	CB3	0	1	0	1	0	1	0	1
0	0		–	11	14	–	–	–	–	5
0	1		8	12	–	–	–	1	2	6
1	0		9	13	15	–	–	–	3	7
1	1		10	–	–	–	–	0	4	–

NOTE:
1. Unlisted CB combinations are no correction.

TABLE 25. CODE ID_{2-0} = 101 (1)

		CB0	0	0	0	0	1	1	1	1
		CB6	0	0	0	0	1	1	1	1
		CB5	0	0	0	0	1	1	1	1
		CB4	0	0	1	1	0	0	1	1
CB2	CB1	CB3	0	1	0	1	0	1	0	1
0	0		–	–	–	5	–	11	14	–
0	1		–	1	2	6	8	12	–	–
1	0		–	–	3	7	9	13	15	–
1	1		–	0	4	–	10	–	–	–

NOTE:
1. Unlisted CB combinations are no correction.

TABLE 26. CODE ID_{2-0} = 110 (1)

		CB0	0	0	0	0	1	1	1	1
		CB6	1	1	1	1	0	0	0	0
		CB5	0	0	0	0	1	1	1	1
		CB4	0	0	1	1	0	0	1	1
CB2	CB1	CB3	0	1	0	1	0	1	0	1
0	0		–	–	–	5	–	11	14	–
0	1		–	1	2	6	8	12	–	–
1	0		–	–	3	7	9	13	15	–
1	1		–	0	4	–	10	–	–	–

NOTE:
1. Unlisted CB combinations are no correction.

TABLE 27. CODE ID_{2-0} = 111 (1)

		CB0	0	0	0	0	1	1	1	1
		CB6	1	1	1	1	0	0	0	0
		CB5	1	1	1	1	0	0	0	0
		CB4	0	0	1	1	0	0	1	1
CB2	CB1	CB3	0	1	0	1	0	1	0	1
0	0		–	11	14	–	–	–	–	5
0	1		8	12	–	–	–	1	2	6
1	0		9	13	15	–	–	–	3	7
1	1		10	–	–	–	–	0	4	–

NOTE:
1. Unlisted CB combinations are no correction.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	30	30	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level [4]		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level [4]		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10	µA
			V_O = V_{CC} (max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V [3]		-30	–	–	mA

NOTES:
1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

$T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (Commercial)
$T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (Military)
$V_{LC} = 0.2V$
$V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ $f_{OP} = 0$		–	3.0	5.0	mA
I_{CCT}	Quiescent Input Power Supply (5) Current (per Input @ TTL High)	V_{CC} = Max. $V_{IN} = 3.4V$, $f_{OP} = 0$		–	0.3	0.5	mA/Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open. $\overline{OE}$ = L	MIL.	–	5.0	8.5	mA/MHz
			COM'L.	–	5.0	7.0	mA/MHz
I_{CC}	Total Power Supply Current (6)	V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty Cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	MIL.	–	53	90	mA
			COM'L.	–	53	75	
		V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty Cycle $V_{IN} = 3.4V$, $V_{IN} = 0.4V$	MIL.	–	60	100	
			COM'L.	–	60	85	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQ}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$I_{CC} = I_{CCQ} + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{OP})$

D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{OP} = Operating frequency

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.

IDT39C60 INPUT/OUTPUT INTERFACE CIRCUITRY

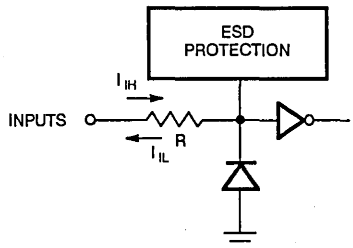


Figure 10. Input Structure (All Inputs)

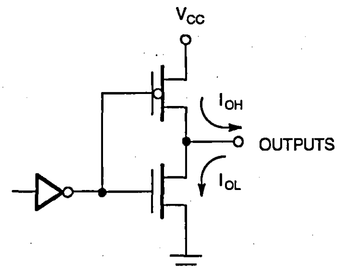
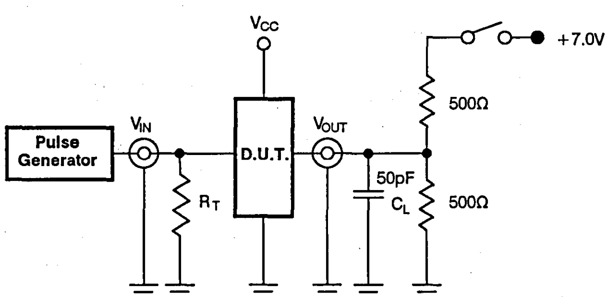


Figure 11. Output Structure

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 12

TEST LOAD CIRCUITS



TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

8

IDT39C60A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60A over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	20	30	20	23
CB_{0-6} (CODE ID_{2-0} 000, 011)	14	25	20	23
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	14	18	20	23
$\overline{GENERATE}$	15	25	14	17
CORRECT (Not Internal Control Mode)	–	20	–	–
DIAG MODE (Not Internal Control Mode)	22	25	18	21
PASSTHRU (Not Internal Control Mode)	22	25	18	21
CODE ID_{2-0}	23	28	25	28
LE_{IN} (From latched to transparent)	22	32(1)	22	25
LE_{OUT} (From latched to transparent)	–	13	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	22	32	22	25
Internal Control Mode: LE_{DIAG} (From latched to transparent)	28	38	28	31
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	28	38	28	31

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 13 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	5	3
CB_{0-6}	LE_{IN}	5	3
$DATA_{0-15}$	LE_{OUT}	24	2
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	21	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111))	LE_{OUT}	21	0
$\overline{GENERATE}$	LE_{OUT}	26	0
CORRECT	LE_{OUT}	22	0
DIAG MODE	LE_{OUT}	22	0
PASSTHRU	LE_{OUT}	22	0
CODE ID_{2-0}	LE_{OUT}	25	0
LE_{IN}	LE_{OUT}	28	0
$DATA_{0-15}$	LE_{DIAG}	5	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	24	21
$\overline{OE}_{SC}$	SC_{0-6}	24	21

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12

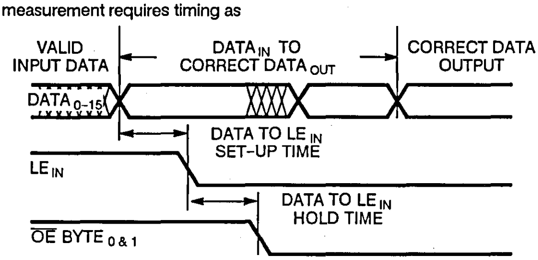


Figure 13.

IDT39C60A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60A over the military operating range of -55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	22	35	24	27
CB_{0-6} (CODE ID_{2-0} 000, 011)	17	28	24	27
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	17	20	24	27
$\overline{GENERATE}$	20	28	18	21
CORRECT (Not Internal Control Mode)	–	25	–	–
DIAG MODE (Not Internal Control Mode)	25	28	21	24
PASSTHRU (Not Internal Control Mode)	25	28	21	24
CODE ID_{2-0}	26	31	28	31
LE_{IN} (From latched to transparent)	24	37(1)	26	29
LE_{OUT} (From latched to transparent)	–	16	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	24	37	26	29
Internal Control Mode: LE_{DIAG} (From latched to transparent)	30	43	32	35
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	30	43	32	35

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 14 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	5	3
CB_{0-6}	LE_{IN}	5	3
$DATA_{0-15}$	LE_{OUT}	27	2
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	24	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111))	LE_{OUT}	24	0
$\overline{GENERATE}$	LE_{OUT}	29	0
CORRECT	LE_{OUT}	25	0
DIAG MODE	LE_{OUT}	25	0
PASSTHRU	LE_{OUT}	25	0
CODE ID_{2-0}	LE_{OUT}	28	0
LE_{IN}	LE_{OUT}	30	0
$DATA_{0-15}$	LE_{DIAG}	5	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	28	25
$\overline{OE}_{SC}$	SC_{0-6}	28	25

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12

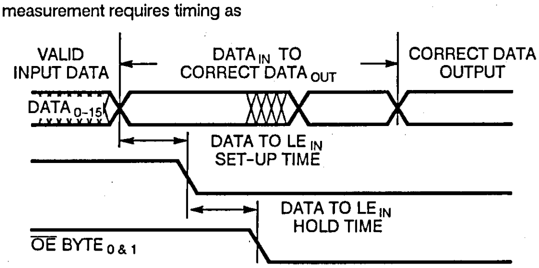


Figure 14.

8

IDT39C60-1 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60-1 over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load.

COMBINATIONAL PROPAGATION DELAYS

$C_L = 50pF$

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	28	52	25	50
CB_{0-6} (CODE ID_{2-0} 000, 011)	23	50	23	47
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	28	34	29	34
$\overline{GENERATE}$	35	63	36	55
CORRECT (Not Internal Control Mode)	–	45	–	–
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASSTHRU (Not Internal Control Mode)	36	44	29	46
CODE ID_{2-0}	61	90	60	80
LE_{IN} (From latched to transparent)	39	72(1)	39	59
LE_{OUT} (From latched to transparent)	–	31	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE_{DIAG} (From latched to transparent)	67	96	66	86
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 15 below.

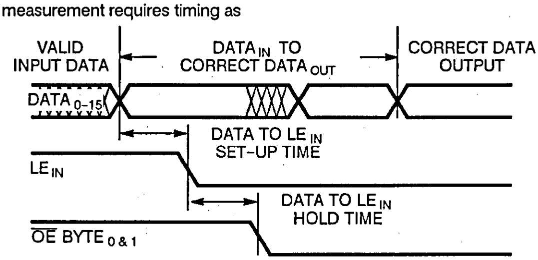


Figure 15.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	6	7
CB_{0-6}	LE_{IN}	5	6
$DATA_{0-15}$	LE_{OUT}	34	5
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	35	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111))	LE_{OUT}	27	0
$\overline{GENERATE}$	LE_{OUT}	42	0
CORRECT	LE_{OUT}	26	1
DIAG MODE	LE_{OUT}	69	0
PASSTHRU	LE_{OUT}	26	0
CODE ID_{2-0}	LE_{OUT}	81	0
LE_{IN}	LE_{OUT}	51	5
$DATA_{0-15}$	LE_{DIAG}	6	8

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with $C_L = 5pF$ and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	30	30
$\overline{OE}_{SC}$	SC_{0-6}	30	30

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

IDT39C60-1 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60-1 over the military operating range of -55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load.

COMBINATIONAL PROPAGATION DELAYS

$C_L = 50pF$

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{\text{ERROR}}$	$\overline{\text{MULT ERROR}}$
$DATA_{0-15}$	31	59	28	56
CB_{0-6} (CODE ID_{2-0} 000, 011)	25	55	25	50
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	30	38	31	37
$\overline{\text{GENERATE}}$	38	69	41	62
CORRECT (Not Internal Control Mode)	–	49	–	–
DIAG MODE (Not Internal Control Mode)	58	89	65	90
PASSTHRU (Not Internal Control Mode)	39	51	34	54
CODE ID_{2-0}	69	100	68	90
LE_{IN} (From latched to transparent)	39	82(1)	43	66
LE_{OUT} (From latched to transparent)	–	33	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	50	88	49	72
Internal Control Mode: LE_{DIAG} (From latched to transparent)	75	106	74	96
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	75	106	74	96

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 16 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	7	7
CB_{0-6}	LE_{IN}	5	7
$DATA_{0-15}$	LE_{OUT}	39	5
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	38	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111))	LE_{OUT}	30	0
$\overline{\text{GENERATE}}$	LE_{OUT}	46	0
CORRECT	LE_{OUT}	28	1
DIAG MODE	LE_{OUT}	84	0
PASSTHRU	LE_{OUT}	30	0
CODE ID_{2-0}	LE_{OUT}	89	0
LE_{IN}	LE_{OUT}	59	5
$DATA_{0-15}$	LE_{DIAG}	7	9

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with $C_L = 5pF$ and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE	DISABLE
$\overline{\text{OE}}$ $BYTE_0$, $\overline{\text{OE}}$ $BYTE_1$	$DATA_{0-15}$	35	35
$\overline{\text{OE}}_{SC}$	SC_{0-6}	35	35

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

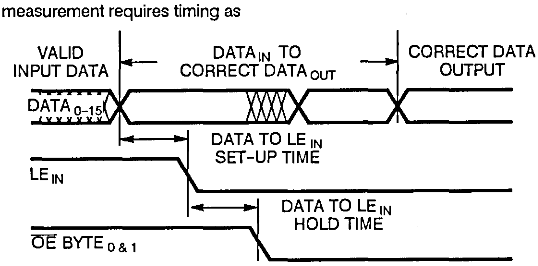


Figure 16.

IDT39C60 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60 over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	32	65(1)	32	50
CB_{0-6} (CODE ID_{2-0} 000, 011)	28	56	29	47
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	28	45	29	34
$\overline{GENERATE}$	35	63	36	55
CORRECT (Not Internal Control Mode)	–	45	–	–
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASSTHRU (Not Internal Control Mode)	36	44	29	46
CODE ID_{2-0}	61	90	60	80
LE_{IN} (From latched to transparent)	39	72(1)	39	59
LE_{OUT} (From latched to transparent)	–	31	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE_{DIAG} (From latched to transparent)	67	96	66	86
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 17 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	6	7
CB_{0-6}	LE_{IN}	5	6
$DATA_{0-15}$	LE_{OUT}	44	5
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	35	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111))	LE_{OUT}	27	0
$\overline{GENERATE}$	LE_{OUT}	42	0
CORRECT	LE_{OUT}	26	1
DIAG MODE	LE_{OUT}	69	0
PASSTHRU	LE_{OUT}	26	0
CODE ID_{2-0}	LE_{OUT}	81	0
LE_{IN}	LE_{OUT}	51	5
$DATA_{0-15}$	LE_{DIAG}	6	8

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	30	30
$\overline{OE}_{SC}$	SC_{0-6}	30	30

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

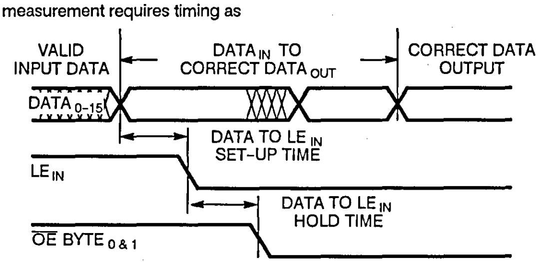


Figure 17.

IDT39C60 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60 over the military operating range of -55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	35	73(1)	36	56
CB_{0-6} (CODE ID_{2-0} 000, 011)	30	61	31	50
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	30	50	31	37
$\overline{GENERATE}$	38	69	41	62
CORRECT (Not Internal Control Mode)	–	49	–	–
DIAG MODE (Not Internal Control Mode)	58	89	65	90
PASSTHRU (Not Internal Control Mode)	39	51	34	54
CODE ID_{2-0}	69	100	68	90
LE_{IN} (From latched to transparent)	44	82(1)	43	66
LE_{OUT} (From latched to transparent)	–	33	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	50	88	49	72
Internal Control Mode: LE_{DIAG} (From latched to transparent)	75	106	74	96
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	75	106	74	96

NOTE:
1. $DATA_{IN}$ (or LE_{IN}) to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 18 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	7	7
CB_{0-6}	LE_{IN}	5	7
$DATA_{0-15}$	LE_{OUT}	50	5
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	38	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111))	LE_{OUT}	30	0
$\overline{GENERATE}$	LE_{OUT}	46	0
CORRECT	LE_{OUT}	28	1
DIAG MODE	LE_{OUT}	84	0
PASSTHRU	LE_{OUT}	30	0
CODE ID_{2-0}	LE_{OUT}	89	0
LE_{IN}	LE_{OUT}	59	5
$DATA_{0-15}$	LE_{DIAG}	7	9

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	35	35
$\overline{OE}_{SC}$	SC_{0-6}	35	35

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

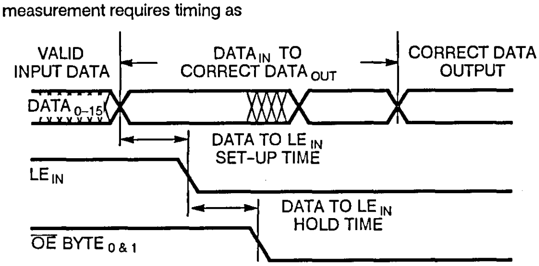


Figure 18.

ORDERING INFORMATION

IDT XXXXX (Device Type) X (Package) X (Process/ Temperature Range)

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
P	Plastic DIP
XC	Sidebraze Shrink-DIP
C	Sidebraze DIP
J	Plastic Leaded Chip Carrier
L	Leadless Chip Carrier
39C60	16-Bit EDC Unit
39C60-1	Fast 16-Bit EDC Unit
39C60A	Ultra-fast 16-Bit EDC Unit

32-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT49C460
IDT49C460A
IDT49C460B

Integrated Device Technology, Inc.

FEATURES:

- Fast

	Detect	Correct
– IDT49C460B	25ns (max.)	30ns (max.)
– IDT49C460A	30ns (max.)	36ns (max.)
– IDT49C460	40ns (max.)	49ns (max.)

- Low-power CMOS
  - Commercial: 95mA (max.)
  - Military: 125mA (max.)
- Improves system memory reliability
  - Corrects all single bit errors, detects all double and some triple-bit errors
- Cascadable
  - Data words up to 64-bits
- Built-in diagnostics
  - Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - Fast byte writes possible with separate byte enables
- Functional replacement for 32- and 64-bit configurations of the 2960
- Available in PGA, Sidebraze Shrink-DIP, LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C460s are high-speed, low-power, 32-bit Error Detection and Correction Units which generate check bits on a 32-bit data field according to a modified Hamming Code and correct the data word when check bits are supplied. The IDT49C460s are performance-enhanced functional replacements for 32-bit versions of the 2960. When performing a read operation from memory, the IDT49C460s will correct 100% of all single bit errors and will detect all double bit errors and some triple bit errors.

The IDT49C460s are easily cascadable to 64-bits. Thirty-two-bit systems use 7 check bits and 64-bit systems use 8 check bits. For both configurations, the error syndrome is made available.

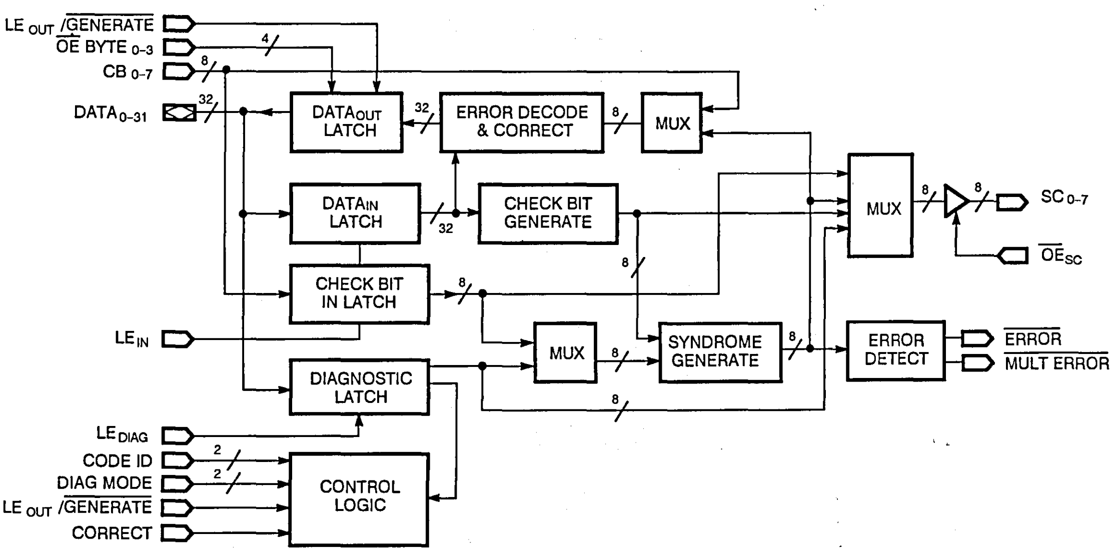
The IDT49C460s incorporate two built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostic functions.

They are fabricated using CEMOS™, a CMOS technology designed for high-performance and high-reliability. The devices are packaged in a 68-pin PGA, sidebraze Shrink-DIP (600 mil, 70 mil centers), LCC (25 mil and 50 mil centers) and PLCC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

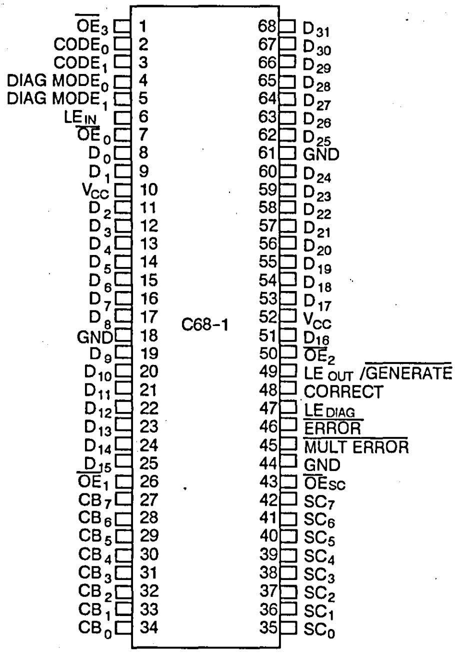
8

FUNCTIONAL BLOCK DIAGRAM

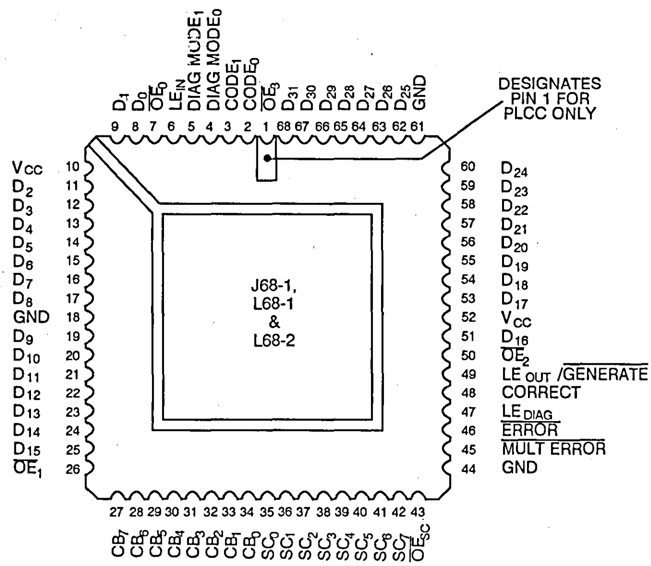


CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.

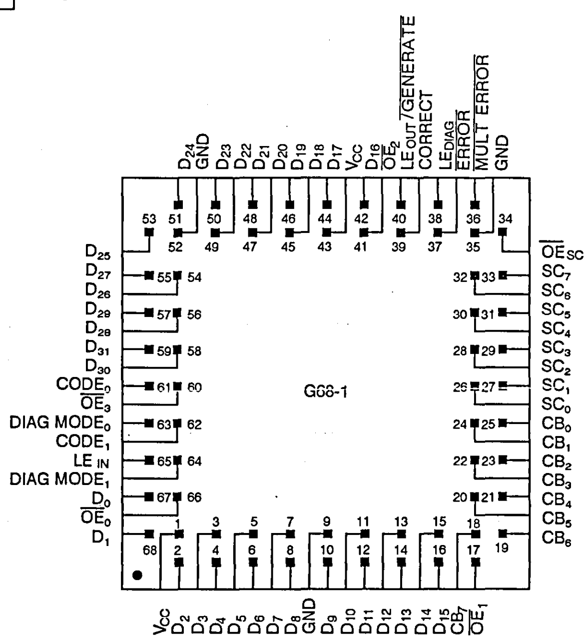
PIN CONFIGURATION



SHRINK-DIP
TOP VIEW



PLCC/LCC
TOP VIEW



PGA
TOP VIEW

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
$DATA_{0-31}$	I/O	32 bidirectional data lines. They provide input to the Data Input Latch and Diagnostic Latch and also receive output from the Data Output Latch. $DATA_0$ is the LSB; $DATA_{31}$ is the MSB.
CB_{0-7}	I	Eight check bit input lines. Used to input check bits for error detection and also used to input syndrome bits for error correction in 64-bit applications.
LE_{IN}	I	Latch Enable is for the Data Input Latch. Controls latching of the input data. Data Input Latch and Check Bit Input Latch are latched to their previous state when LOW. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits.
$LE_{OUT}/\overline{GENERATE}$	I	A multifunction pin which, when LOW, is in the Check Bit Generate Mode. In this mode, the device generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. Also, when LOW, the Data Out Latch is latched to its previous state. When HIGH, the device is in the Detect or Correct Mode. In this mode, the device detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In the Correct Mode, single bit errors are also automatically corrected and the corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the specific bit-in-error. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single bit errors are corrected by the network before being loaded into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The Data Output Latch is disabled, with its contents unchanged, if the EDC is in the Generate Mode.
SC_{0-7}	O	Syndrome Check Bit outputs. Eight outputs which hold the check bits and partial check bits when the EDC is in the Generate Mode and will hold the syndrome/partial syndrome bits when the device is in the Detect or Correct modes. All are 3-state outputs.
$\overline{OE}_{SC}$	I	Output Enable – Syndrome Check Bits. In the HIGH condition, the SC outputs are in the high impedance state. When LOW, all SC output lines are enabled.
$\overline{ERROR}$	O	In the Detect or Correct Mode, this output will go LOW if one or more data or check bits contain an error. When HIGH, no errors have been detected. This pin is forced HIGH in the Generate Mode.
$\overline{MULT\ ERROR}$	O	In the Detect or Correct Mode, this output will go LOW if two or more bit errors have been detected. A HIGH level indicates that either one or no errors have been detected. This pin is forced HIGH in the Generate Mode.
CORRECT	I	The correct input which, when HIGH, allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the device will drive data directly from the Data Input Latch to the Data Output Latch without correction.
$\overline{OE}\ BYTE_{0-3}$	I	Output Enable – Bytes 0, 1, 2, 3. Data Output Latch. Control the three-state output buffers for each of the four bytes of the Data Output Latch. When LOW, they enable the output buffer of the Data Output Latch. When HIGH, they force the Data Output Latch buffer into the high impedance mode. One byte of the Data Output Latch is easily activated by separately selecting the four enable lines.
DIAG $MODE_{0,1}$	I	Select the proper diagnostic mode. They control the initialization, diagnostic and normal operation of the EDC.
CODE $ID_{0,1}$	I	These two code identification inputs identify the size of the total data word to be processed. The two allowable data word sizes are 32 and 64 bits and their respective modified Hamming Codes are designated 32/39 and 64/72. Special CODE ID input 01 is also used to instruct the EDC that the signals CODE $ID_{0,1}$, DIAG $MODE_{0,1}$ and CORRECT are to be taken from the Diagnostic Latch rather than from the input control lines.
LE_{DIAG}	I	This is the Latch Enable for the Diagnostic Latch. When HIGH, the Diagnostic Latch follows the 32-bit data on the input lines. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for CODE $ID_{0,1}$, DIAG $MODE_{0,1}$ and CORRECT.

8

EDC ARCHITECTURE SUMMARY

The IDT49C460s are high-performance cascadable EDCs used for check bit generation, error detection, error correction and diagnostics. The function blocks for this 32-bit device consist of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch
- Diagnostic Latch
- Control Logic

DATA INPUT/OUTPUT LATCH:

The Latch Enable Input, LE_{IN}, controls the loading of 32 bits of data to the Data In Latch. The 32 bits of data from the DATA lines can be loaded in the Diagnostic Latch under control of the Diagnostic Latch Enable, LE_{DIAG}, giving check bit information in one byte and control information in the other byte. The Diagnostic Latch is used in the Internal Control Mode or in one of the diagnostic modes. The Data Output Latch has buffers that place data on the DATA lines. These buffers are split into four 8-bit buffers, each having their own output enable controls. This feature facilitates byte read and byte modify operations.

CHECK BIT INPUT LATCH:

Eight check bits are loaded under control of LE_{IN}. Check bits are used in the Error Detection and Error Correction modes.

CHECK BIT GENERATION LOGIC:

This generates the appropriate check bits for the 32 bits of data in the Data Input Latch. The modified Hamming Code is the basis for generating the proper check bits.

SYNDROME GENERATION LOGIC:

In both the Detect and Correct modes, this logic does a comparison on the check bits read from memory against the newly generated set of check bits produced for the data read in from memory. Matching sets of check bits mean no error was detected. If there is a mismatch, one or more of the data or check bits is in error. Syndrome bits are produced by an exclusive-OR of the two sets of check bits. Identical sets of check bits means the syndrome bits will be all zeros. If an error results, the syndrome bits can be decoded to determine the number of errors and the specific bit-in-error.

ERROR DETECTION LOGIC:

This part of the device decodes the syndrome bits generated by the Syndrome Generation Logic. With no errors in either the input data or check bits, both the $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ outputs are HIGH. $\overline{\text{ERROR}}$ will go low if one error is detected. $\overline{\text{MULT ERROR}}$ and $\overline{\text{ERROR}}$ will both go low if two or more errors are detected.

ERROR CORRECTION LOGIC:

In single error cases, this logic complements (corrects) the single data bit-in-error. This corrected data is loaded into the Data Output Latch, which can then be read onto the bidirectional data lines. If the error is resulting from one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed, the EDC must be switched to the Generate Mode.

DATA OUTPUT LATCH AND OUTPUT BUFFERS:

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE_{OUT}. The Data Output Latch may also be directly loaded from the Data Input Latch under control of the PASSTHRU control input. The Data Output Latch buffer is split into 4 individual buffers which can be enabled by $\overline{OE}_{0-3}$ separately for reading onto the bidirectional data lines.

DIAGNOSTIC LATCH:

A 32-bit latch is loadable, under control of the Diagnostic Latch Enable, LE_{DIAG}, from the bidirectional data lines. Check bit information is contained in one byte while the other byte contains the control information. The Diagnostic Latch is used for driving the device when in the Internal Control Mode, or for supplying check bits when in one of the diagnostic modes.

CONTROL LOGIC:

Specifies what mode the device will be operating in. Normal operation is when the control logic is driven by external control inputs. In the Internal Control Mode, the control signals are read from the Diagnostic Latch. Since LE_{OUT} and $\overline{\text{GENERATE}}$ are controlled by the same pin, the latching action (LE_{OUT} from high to low) of the Data Output Latch causes the EDC to go into the Generate Mode.

DETAILED PRODUCT DESCRIPTION

The IDT49C460 EDC units contain the logic necessary to generate check bits on 32 bits of data input according to a modified Hamming Code. The EDC can compare internally generated check bits against those read with the 32-bit data to allow correction of any single bit data error and detection of all double (and some triple) bit errors. The IDT49C460s can be used for 32-bit data words (7 check bits) and 64-bit (8 check bits) data words.

CODE AND BYTE SELECTION:

The 2 code identification pins, $ID_{0,1}$, are used to determine the data word size that is 32 or 64 bits. Table 4 defines all possible slice identification codes.

CHECK AND SYNDROME BITS:

The IDT49C460s provide either check bits or syndrome bits on the three-state output pins, SC_{0-7}. Check bits are generated from a combination of the Data Input bits, while syndrome bits are an exclusive-OR of the check bits generated from read data with the read check bit sorted with the data. Syndrome bits can be decoded to determine the single bit in error or that a double (some triple) error was detected. The check bits are labeled:

CX, C0, C1, C2, C4, C8, C16 for the 32-bit configuration
CX, C0, C1, C2, C4, C8, C16, C32 for the 64-bit configuration

Syndrome bits are similarly labeled SX through S32.

TABLE 2.
DIAGNOSTIC MODE CONTROL

CORRECT	DIAG $MODE_1$	DIAG $MODE_0$	DIAGNOSTIC MODE SELECTED
X	0	0	**Non-diagnostic Mode.** Normal EDC function in this mode.
X	0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate Mode. The EDC functions normally in the Detect or Correct modes.
X	1	0	**Diagnostic Detect/Correct.** In either mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate Mode.
1	1	1	**Initialize.** The Data Input Latch outputs are forced to zeros and latched upon removal of Initialize Mode.
0	1	1	**PASSTHRU.**

TABLE 3.
IDT49C460 OPERATING MODES

OPERATING MODE	DM_1	DM_0	$\overline{GENERATE}$	CORRECT	DATA OUT LATCH	SC_{0-7} ($\overline{OE}_{SC}$ = LOW)	$\overline{ERROR}$ $\overline{MULT\ ERROR}$
Generate	0 1	0 0	0	X	LE_{OUT} = LOW(1)	Check Bits Generated from Data In Latch	–
Detect	0 0	0 1	1	0	Data In Latch	Syndrome Bits Data In/ Check Bit Latch	Error Dep(2)
Correct	0 0	0 1	1	1	Data In Latch w/ Single Bit Correction	Syndrome Bits Data In/ Check Bit Latch	Error Dep
PASSTHRU	1	1	1	0	Data In Latch	Check Bit Latch	HIGH
Diagnostic Generate	0	1	0	X	–	Check Bits from Diagnostic Latch	–
Diagnostic Detect	1	0	1	0	Data In Latch	Syndrome Bits Data In/ Diagnostic Latch	Error Dep
Diagnostic Correct	1	0	1	1	Data In Latch w/ Single Bit Correction	Syndrome Bits Data In/ Diagnostic Latch	Error Dep
Initialization Mode	1	1	1	1	Data In Latch set to 0000	–	–
Internal Mode	CODE $ID_{0,1}$ = 01 Control Signals $ID_{0,1}$, DIAG $MODE_{0,1}$, and CORRECT are taken from Diagnostic Latch.						

NOTES:
1. In Generate Mode, data is read into the EDC unit and the check bits are generated. The same data is written to memory along with the check bits. Since the Data Out Latch is not used in the Generate Mode, LE_{OUT} (being LOW since it is tied to Generate), does not affect the writing of check bits.
2. Error Dep (Error Dependent): $\overline{ERROR}$ will be low for single or multiple errors, with $\overline{MULT\ ERROR}$ low for double or multiple errors. Both signals are high for no errors.

CONTROL MODE SELECTION:

Tables 2 and 3 describe the 9 operating modes of the IDT49C460s. The Diagnostic Mode pins—DIAG $MODE_{0,1}$—define four basic areas of operation. $\overline{GENERATE}$ and $\overline{CORRECT}$ further divide operation into 8 functions, with $ID_{0,1}$ defining the ninth mode as the Internal Mode.

Generate Mode is used to display the check bits on the outputs SC_{0-7}. The Diagnostic Generate Mode displays check bits as stored in the Diagnostic Latch.

Detect Mode provides an indication of errors or multiple errors on the outputs $\overline{ERROR}$ and $\overline{MULT\ ERROR}$. Single bit errors are not corrected in this mode. The syndrome bits are provided on the outputs SC_{0-7}. For the Diagnostic Detect Mode, the syndrome bits are generated by comparing the internally generated check bits from the Data In Latch with check bits stored in the diagnostic latch rather than with the check bit latch contents.

Correct Mode is similar to the Detect Mode except that single bit errors will be complemented (corrected) and made available as input to the Data Out Latches. Again, the Diagnostic Correct Mode will correct single bit errors as determined by syndrome bits generated from the data input and contents of the diagnostic latches.

The Initialize Mode provides check bits for all zero bit data. Data Input Latches are set, latched to a logic zero and made available as input to the Data Out Latches.

The Internal Mode disables the external control pins DIAG $MODE_{0,1}$ and CORRECT to be defined by the Diagnostic Latch. Even $ID_{1,0}$, although externally set to the 01 code, can be redefined from the Diagnostic Latch data.

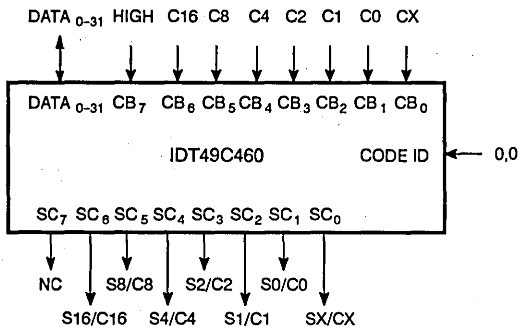


Figure 1. 32-Bit Configuration

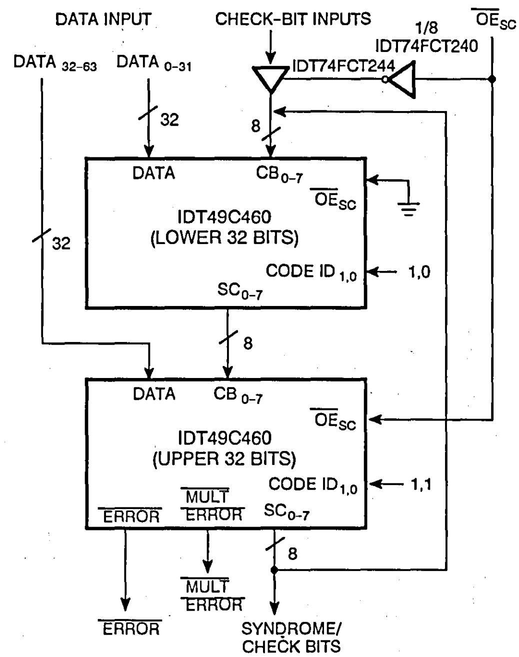


Figure 2. 64-Bit Configuration

DATA				CHECK BITS						
$BYTE_3$	$BYTE_2$	$BYTE_1$	$BYTE_0$	CX	C0	C1	C2	C4	C8	C16
31 24	23 16	15 8	7 0							

Figure 3. 32-Bit Data Format

DATA								CHECK BITS							
$BYTE_7$	$BYTE_6$	$BYTE_5$	$BYTE_4$	$BYTE_3$	$BYTE_2$	$BYTE_1$	$BYTE_0$	CX	C0	C1	C2	C4	C8	C16	C32
63 56	55 48	47 40	39 32	31 24	23 16	15 8	7 0								

Figure 4. 64-Bit Data Format

32-BIT DATA WORD CONFIGURATION:

A single IDT49C460 EDC unit, connected as shown in Figure 1, provides all the logic needed for single bit error correction and double bit error detection of a 32-bit data field. The identification code indicates 7 check bits are required. The CB_7 pin should be HIGH.

Figure 3 indicates the 39-bit data format for two bytes of data and 7 check bits. Table 3 describes the operating mode available.

Table 6 indicates the data bits participating in the check bit generation. For example, check bit C0 is the exclusive-OR function of the 16 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits from the respective latch are passed, unchanged, in the Pass Thru or Diagnostic Generate Mode.

Syndrome bits are generated by an exclusive-OR or the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 7 indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 4 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-7} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

TABLE 4. 32-BIT DIAGNOSTIC LATCH CODING FORMAT

BIT 0	CB_0 DIAGNOSTIC
BIT 1	CB_1 DIAGNOSTIC
BIT 2	CB_2 DIAGNOSTIC
BIT 3	CB_3 DIAGNOSTIC
BIT 4	CB_4 DIAGNOSTIC
BIT 5	CB_5 DIAGNOSTIC
BIT 6	CB_6 DIAGNOSTIC
BIT 7	CB_7 DIAGNOSTIC
BIT 8	CODE ID_0
BIT 9	CODE ID_1
BIT 10	DIAG $MODE_0$
BIT 11	DIAG $MODE_1$
BIT 12	CORRECT
BIT 13-31	DON'T CARE

TABLE 5. SLICE IDENTIFICATION

CODE ID_1	CODE ID_0	SLICE SELECTED
0	0	32-Bit
0	1	Internal Control Mode
1	0	64-Bit, Lower 32-Bit (0-31)
1	1	64-Bit, Upper 32-Bit (32-63)

TABLE 6. 32-BIT MODIFIED HAMMING CODE—CHECK BIT ENCODE CHART

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)	X				X		X	X	X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X					X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X

TABLE 7.
SYNDROME DECODE TO BIT-IN-ERROR

SYNDROME BITS			S16	0	1	0	1	0	1	0	1
			S8	0	0	1	1	0	0	1	1
			S4	0	0	0	0	1	1	1	1
SX	S0	S1	S2								
0	0	0	0	*	C16	C8	T	C4	T	T	30
0	0	0	1	C2	T	T	27	T	5	M	T
0	0	1	0	C1	T	T	25	T	3	15	T
0	0	1	1	T	M	13	T	23	T	T	M
0	1	0	0	C0	T	T	24	T	2	M	T
0	1	0	1	T	1	12	T	22	T	T	M
0	1	1	0	T	M	10	T	20	T	T	M
0	1	1	1	16	T	T	M	T	M	M	T
1	0	0	0	CX	T	T	M	T	M	14	T
1	0	0	1	T	M	11	T	21	T	T	M
1	0	1	0	T	M	9	T	19	T	T	31
1	0	1	1	M	T	T	29	T	7	M	T
1	1	0	0	T	M	8	T	18	T	T	M
1	1	0	1	17	T	T	28	T	6	M	T
1	1	1	0	M	T	T	26	T	4	M	T
1	1	1	1	T	0	M	T	M	T	T	M

NOTES:
* – no errors detected
Number – number of the single bit-in-error
T – two errors detected
M – three or more errors detected

64-BIT DATA WORD CONFIGURATION:

Two IDT49C460 EDC units, connected as shown in Figure 2, provide all the logic needed for single bit error correction and double bit error detection of a 64-bit data field. Table 5 gives the $ID_{1,0}$ values needed for distinguishing the upper 32 bits from the lower 32 bits. Valid syndrome, check bits and the $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ signals come from the IC with the CODE ID = 11. Control signals not indicated are connected to both units in parallel. The EDC with the CODE ID = 10 has the $\overline{\text{OE}}_{SC}$ grounded. The $\overline{\text{OE}}_{SC}$ selects the syndrome bits from the EDC with CODE ID = 11 and also controls the check bit buffers from memory.

Data In bits 0 through 31 are connected to the same numbered inputs of the EDC unit with CODE ID = 10, while Data In bits 32 through 63 are connected to Data Inputs 0 to 31, respectively, for the EDC unit with CODE ID = 11.

Figure 4 indicates the 72-bit data format of 8 bytes of data and 8 check bits. Check bits are input to the EDC unit with CODE ID = 10 through a three-state buffer unit such as the IDT74FCT244. Correction of single bit errors of the 64-bit configuration requires a feedback of syndrome bits from the lower EDC unit to the upper EDC units. The MUX shown on the functional block diagram is used to select the CB_{0-7} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating mode available for the 64/72 configuration.

Table 11 indicates the data bits participating in the check bit generation. For example, check bit C0 is the exclusive-OR function or the 32 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization modes. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate modes.

Syndrome bits are generated by an exclusive-OR of the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 9 indicates the decoding of the 8 syndrome bits to determine the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Tables 8A and 8B define the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic Check Bits to determine syndrome bits or to pass as check bits to the SC_{0-7} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Performance data is provided in Table 10, relating a single IDT49C460 EDC with the two cascaded units of Figure 2. As indicated, a summation of propagation delays is required from the cascading arrangement of EDC units.

TABLE 8A.
64-BIT DIAGNOSTIC LATCH – CODING FORMAT (EXCEPT DIAGNOSTIC WRITE MODE)

BIT	INTERNAL FUNCTION
0	CB_0 DIAGNOSTIC
1	CB_1 DIAGNOSTIC
2	CB_2 DIAGNOSTIC
3	CB_3 DIAGNOSTIC
4	CB_4 DIAGNOSTIC
5	CB_5 DIAGNOSTIC
6	CB_6 DIAGNOSTIC
7	CB_7 DIAGNOSTIC
8	$CODE_0$ LOWER 32-BIT
9	$CODE_1$ LOWER 32-BIT
10	DIAG $MODE_0$ LOWER 32-BIT
11	DIAG $MODE_1$ LOWER 32-BIT
12	CORRECT LOWER 32-BIT
13-31	DON'T CARE
32-39	DON'T CARE
40	CODE ID_0 UPPER 32-BIT
41	CODE ID_1 UPPER 32-BIT
42	DIAG $MODE_0$ UPPER 32-BIT
43	DIAG $MODE_1$ UPPER 32-BIT
44	CORRECT UPPER 32-BIT
45-63	DON'T CARE

TABLE 8B.
64-BIT DIAGNOSTIC LATCH – CODING FORMAT (DIAGNOSTIC WRITE MODE ONLY)

BIT	INTERNAL FUNCTION
0-7	DON'T CARE
8	$CODE_0$ LOWER 32-BIT
9	$CODE_1$ LOWER 32-BIT
10	DIAG $MODE_0$ LOWER 32-BIT
11	DIAG $MODE_1$ LOWER 32-BIT
12	CORRECT LOWER 32-BIT
13-31	DON'T CARE
32	CB_0 DIAGNOSTIC
33	CB_1 DIAGNOSTIC
34	CB_2 DIAGNOSTIC
35	CB_3 DIAGNOSTIC
36	CB_4 DIAGNOSTIC
37	CB_5 DIAGNOSTIC
38	CB_6 DIAGNOSTIC
39	CB_7 DIAGNOSTIC
40	CODE ID_0 UPPER 32-BIT
41	CODE ID_1 UPPER 32-BIT
42	DIAG $MODE_0$ UPPER 32-BIT
43	DIAG $MODE_1$ UPPER 32-BIT
44	CORRECT UPPER 32-BIT
45-63	DON'T CARE

TABLE 9. SYNDROME DECODE TO BIT-IN-ERROR

SYNDROME BITS			S32	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
			S16	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			S8	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
SX	S0	S1	S2																
0	0	0	0	*	C32	C16	T	C8	T	T	M	C4	T	T	M	T	46	62	T
0	0	0	1	C2	T	T	M	T	43	59	T	T	53	37	T	M	T	T	M
0	0	1	0	C1	T	T	M	T	41	57	T	T	51	35	T	15	T	T	31
0	0	1	1	T	M	M	T	13	T	T	29	23	T	T	7	T	M	M	T
0	1	0	0	C0	T	T	M	T	40	56	T	T	50	34	T	M	T	T	M
0	1	0	1	T	49	33	T	12	T	T	28	22	T	T	6	T	M	M	T
0	1	1	0	T	M	M	T	10	T	T	26	20	T	T	4	T	M	M	T
0	1	1	1	16	T	T	0	T	M	M	T	T	M	M	T	M	T	T	M
1	0	0	0	CX	T	T	M	T	M	M	T	T	M	M	T	14	T	T	30
1	0	0	1	T	M	M	T	11	T	T	27	21	T	T	5	T	M	M	T
1	0	1	0	T	M	M	T	9	T	T	25	19	T	T	3	T	47	63	T
1	0	1	1	M	T	T	M	T	45	61	T	T	55	39	T	M	T	T	M
1	1	0	0	T	M	M	T	8	T	T	24	18	T	T	2	T	M	M	T
1	1	0	1	17	T	T	1	T	44	60	T	T	54	38	T	M	T	T	M
1	1	1	0	M	T	T	M	T	42	58	T	T	52	36	T	M	T	T	M
1	1	1	1	T	48	32	T	M	T	T	M	M	T	T	M	T	M	M	T

NOTES:

* = No errors detected

Number = The number of the single bit-in-error

T = Two errors detected

M = Three or more errors detected

TABLE 10.
KEY AC CALCULATIONS FOR THE 64-BIT CONFIGURATION

64-BIT PROPAGATION DELAY		COMPONENT DELAY FOR IDT49C460 AC SPECIFICATIONS
FROM	TO	
DATA	Check Bits Out	(DATA TO SC) + (CB TO SC, CODE ID 11)
DATA	Corrected DATA Out	(DATA TO SC) + (CB TO SC, CODE ID 11) + (CB TO DATA, CODE ID 10)
DATA	Syndromes Out	(DATA TO SC) + (CB TO SC, CODE ID 11)
DATA	$\overline{\text{ERROR}}$ for 64 Bits	(DATA TO SC) + (CB TO $\overline{\text{ERROR}}$, CODE ID 11)
DATA	$\overline{\text{MULT ERROR}}$ for 64 Bits	(DATA TO SC) + (CB TO $\overline{\text{MULT ERROR}}$, CODE ID 11)

TABLE 11. 64-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODING

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)									X	X	X	X	X	X	X	X

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)									X	X	X	X	X	X	X	X

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)	X	X	X	X	X	X	X	X								

NOTE:
The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

SC OUTPUTS

The tables below indicate how the SC_{0-7} outputs are generated in each control mode for various CODE IDs (Internal Control Mode not applicable).

GENERATE	CODE ID_{1-0}		
	00	10	11
$SC_0 \leftarrow$	PH0	PH1	PH2 $\oplus$ CB_0
$SC_1 \leftarrow$	PA	PA	PA $\oplus$ CB_1
$SC_2 \leftarrow$	PB	PB	PB $\oplus$ CB_2
$SC_3 \leftarrow$	PC	PC	PC $\oplus$ CB_3
$SC_4 \leftarrow$	PD	PD	PD $\oplus$ CB_4
$SC_5 \leftarrow$	PE	PE	PE $\oplus$ CB_5
$SC_6 \leftarrow$	PF	PF	PF $\oplus$ CB_6
$SC_7 \leftarrow$	–	PF	PG $\oplus$ CB_7

CORRECT/ DETECT	CODE ID_{1-0}		
	00	10	11
$SC_0 \leftarrow$	PH0 $\oplus$ C0	PH1 $\oplus$ C0	PH2 $\oplus$ CB_0
$SC_1 \leftarrow$	PA $\oplus$ C1	PA $\oplus$ C1	PA $\oplus$ CB_1
$SC_2 \leftarrow$	PB $\oplus$ C2	PB $\oplus$ C2	PB $\oplus$ CB_2
$SC_3 \leftarrow$	PC $\oplus$ C3	PC $\oplus$ C3	PC $\oplus$ CB_3
$SC_4 \leftarrow$	PD $\oplus$ C4	PD $\oplus$ C4	PC $\oplus$ CB_4
$SC_5 \leftarrow$	PE $\oplus$ C5	PE $\oplus$ C5	PE $\oplus$ CB_5
$SC_6 \leftarrow$	PF $\oplus$ C6	PF $\oplus$ C6	PF $\oplus$ CB_6
$SC_7 \leftarrow$	–	PF $\oplus$ C7	PG $\oplus$ CB_7

DIAGNOSTIC READ	CODE ID_{1-0}		
	00	10	11
$SC_0 \leftarrow$	PH0 $\oplus$ DL0	PH1 $\oplus$ DL0	PH2 $\oplus$ CB_0
$SC_1 \leftarrow$	PA $\oplus$ DL1	PA $\oplus$ DL1	PA $\oplus$ CB_1
$SC_2 \leftarrow$	PB $\oplus$ DL2	PB $\oplus$ DL2	PB $\oplus$ CB_2
$SC_3 \leftarrow$	PC $\oplus$ DL3	PC $\oplus$ DL3	PC $\oplus$ CB_3
$SC_4 \leftarrow$	PD $\oplus$ DL4	PD $\oplus$ DL4	PD $\oplus$ CB_4
$SC_5 \leftarrow$	PE $\oplus$ DL5	PE $\oplus$ DL5	PE $\oplus$ CB_5
$SC_6 \leftarrow$	PF $\oplus$ DL6	PF $\oplus$ DL6	PF $\oplus$ CB_6
$SC_7 \leftarrow$	–	PF $\oplus$ DL7	PG $\oplus$ CB_7

DIAGNOSTIC WRITE	CODE ID_{1-0}		
	00	10	11
$SC_0 \leftarrow$	DL0	DL0	DL32
$SC_1 \leftarrow$	DL1	DL1	DL33
$SC_2 \leftarrow$	DL2	DL2	DL34
$SC_3 \leftarrow$	DL3	DL3	DL35
$SC_4 \leftarrow$	DL4	DL4	DL36
$SC_5 \leftarrow$	DL5	DL5	DL37
$SC_6 \leftarrow$	DL6	DL6	DL38
$SC_7 \leftarrow$	–	DL7	DL39

PASSTHRU	CODE ID_{1-0}		
	00	10	11
$SC_0 \leftarrow$	C0	C0	CB_0
$SC_1 \leftarrow$	C1	C1	CB_1
$SC_2 \leftarrow$	C2	C2	CB_2
$SC_3 \leftarrow$	C3	C3	CB_3
$SC_4 \leftarrow$	C4	C4	CB_4
$SC_5 \leftarrow$	C5	C5	CB_5
$SC_6 \leftarrow$	C6	C6	CB_6
$SC_7 \leftarrow$	–	C7	CB_7

DATA CORRECTION

The tables below indicate which data output bits are corrected depending upon the syndromes and the CODE ID position. The syndromes that determine data correction are, in some cases, syndromes input externally via the CB inputs and, in some cases, syndromes input externally by that EDC (S_i are the internal syndromes and are the same as the value of the SC_i output of that EDC if enabled).

32-BIT CONFIGURATION CODE ID$_{1-0}$ = 00

SYNDROME BITS SB16 / SB8 / SB4 — SBX SB0 SB1 SB2	0 0 0	1 0 0	0 1 0	1 1 0	0 0 1	1 0 1	0 1 1	1 1 1
0 0 0 0	–	–	–	–	–	–	–	30
0 0 0 1	–	–	–	27	–	5	–	–
0 0 1 0	–	–	–	25	–	3	15	–
0 0 1 1	–	–	13	–	23	–	–	–
0 1 0 0	–	–	–	24	–	2	–	–
0 1 0 1	–	1	12	–	22	–	–	–
0 1 1 0	–	–	10	–	20	–	–	–
0 1 1 1	16	–	–	–	–	–	–	–
1 0 0 0	–	–	–	–	–	–	14	–
1 0 0 1	–	–	11	–	21	–	–	–
1 0 1 0	–	–	9	–	19	–	–	31
1 0 1 1	–	–	–	29	–	7	–	–
1 1 0 0	–	–	8	–	18	–	–	–
1 1 0 1	17	–	–	28	–	6	–	–
1 1 1 0	–	–	–	26	–	4	–	–
1 1 1 1	–	0	–	–	–	–	–	–

FUNCTIONAL EQUATIONS

The equations below describe the IDT49C460 output values as defined by the value of the inputs and internal states.

DEFINITIONS

PA = D0 ⊕ D1 ⊕ D2 ⊕ D4 ⊕ D6 ⊕ D8 ⊕ D10 ⊕ D12 ⊕ D16 ⊕ D17 ⊕ D18 ⊕ D20 ⊕ D22 ⊕ D24 ⊕ D26 ⊕ D28

PB = D0 ⊕ D3 ⊕ D4 ⊕ D7 ⊕ D9 ⊕ D10 ⊕ D13 ⊕ D15 ⊕ D16 ⊕ D19 ⊕ D20 ⊕ D23 ⊕ D25 ⊕ D26 ⊕ D29 ⊕ D31

PC = D0 ⊕ D1 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D16 ⊕ D17 ⊕ D21 ⊕ D22 ⊕ D23 ⊕ D27 ⊕ D28 ⊕ D29

PD = D2 ⊕ D3 ⊕ D4 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D14 ⊕ D15 ⊕ D18 ⊕ D19 ⊕ D20 ⊕ D21 ⊕ D22 ⊕ D23 ⊕ D30 ⊕ D31

PE = D8 ⊕ D9 ⊕ D10 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D14 ⊕ D15 ⊕ D24 ⊕ D25 ⊕ D26 ⊕ D27 ⊕ D28 ⊕ D29 ⊕ D30 ⊕ D31

PF = D0 ⊕ D1 ⊕ D2 ⊕ D3 ⊕ D4 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D24 ⊕ D25 ⊕ D26 ⊕ D27 ⊕ D28 ⊕ D29 ⊕ D30 ⊕ D31

PG = D8 ⊕ D9 ⊕ D10 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D14 ⊕ D15 ⊕ D16 ⊕ D17 ⊕ D18 ⊕ D19 ⊕ D20 ⊕ D21 ⊕ D22 ⊕ D23

PH0 = D0 ⊕ D4 ⊕ D6 ⊕ D7 ⊕ D8 ⊕ D9 ⊕ D11 ⊕ D14 ⊕ D17 ⊕ D18 ⊕ D19 ⊕ D21 ⊕ D26 ⊕ D28 ⊕ D29 ⊕ D31

PH1 = D1 ⊕ D2 ⊕ D3 ⊕ D5 ⊕ D8 ⊕ D9 ⊕ D11 ⊕ D14 ⊕ D17 ⊕ D18 ⊕ D19 ⊕ D21 ⊕ D24 ⊕ D25 ⊕ D27 ⊕ D30

PH2 = D0 ⊕ D4 ⊕ D6 ⊕ D7 ⊕ D10 ⊕ D12 ⊕ D13 ⊕ D15 ⊕ D16 ⊕ D20 ⊕ D22 ⊕ D23 ⊕ D26 ⊕ D28 ⊕ D29 ⊕ D31

64-BIT CONFIGURATION (LOWER 32-BIT) CODE ID$_{1-0}$ = 10

SYNDROME BITS CB32 / CB16 / CB8 / CB4 — CBX CB0 CB1 CB2	0 0 0 0	1 1 0 0	0 0 1 0	1 1 1 0	0 0 0 1	1 1 0 1	0 0 1 1	1 1 1 1
0 0 0 0	–	–	–	–	–	–	–	–
0 0 0 1	–	–	–	–	–	–	–	
0 0 1 0	–	–	–	–	–	–	15	31
0 0 1 1	–	–	13	29	23	7	–	–
0 1 0 0	–	–	–	–	–	–	–	–
0 1 0 1	–	–	12	28	22	6	–	–
0 1 1 0	–	–	10	26	20	4	–	–
0 1 1 1	16	0	–	–	–	–	–	–
1 0 0 0	–	–	–	–	–	–	14	30
1 0 0 1	–	–	11	27	21	5	–	–
1 0 1 0	–	–	9	25	19	3	–	–
1 0 1 1	–	–	–	–	–	–	–	–
1 1 0 0	–	–	8	24	18	2	–	–
1 1 0 1	17	1	–	–	–	–	–	–
1 1 1 0	–	–	–	–	–	–	–	–
1 1 1 1	–	–	–	–	–	–	–	–

64-BIT CONFIGURATION (UPPER-BIT) CODE ID$_{1-0}$ = 11(1)

SYNDROME BITS SB32 / SB16 / SB8 / SB4 — SBX SB0 SB1 SB2	1 0 0 0	0 1 0 0	1 0 1 0	0 1 1 0	1 0 0 1	0 1 0 1	1 0 1 1	0 1 1 1
0 0 0 0	–	–	–	–	–	–	46	62
0 0 0 1	–	–	43	59	53	37	–	–
0 0 1 0	–	–	41	57	51	35	–	–
0 0 1 1	–	–	–	–	–	–	–	–
0 1 0 0	–	–	40	56	50	34	–	–
0 1 0 1	49	33	–	–	–	–	–	–
0 1 1 0	–	–	–	–	–	–	–	–
0 1 1 1	–	–	–	–	–	–	–	–
1 0 0 0	–	–	–	–	–	–	–	–
1 0 0 1	–	–	–	–	–	–	–	–
1 0 1 0	–	–	–	–	–	–	47	63
1 0 1 1	–	–	45	61	55	39		
1 1 0 0	–	–	–	–	–	–	–	–
1 1 0 1	–	–	44	60	54	38	–	–
1 1 1 0	–	–	42	58	52	36	–	–
1 1 1 1	48	32	–	–	–	–	–	–

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	30	30	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C $\quad$ V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C $\quad$ V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level[4]		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level[4]		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5.0	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5.0	μA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300μA	V_{HC}	V_{CC}	–	V
			I_{OH} = −12mA MIL.	2.4	4.3	–	
			I_{OH} = −15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10.0	μA
			V_O = V_{CC} (Max.)	–	0.1	10.0	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V[3]		-30.0	–	–	mA

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

$T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (Commercial)
$T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (Military)
$V_{LC} = 0.2V$
$V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ $f_{OP} = 0$		–	3.0	5	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High)(5)	V_{CC} = Max., V_{IN} = 3.4V, $f_{OP} = 0$		–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	6	10	mA/ MHz
			COM'L.	–	6	7	
I_{CC}	Total Power Supply Current (6)	V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	MIL.	–	60	110	mA
			COM'L.	–	60	80	
		V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	70	125	
			COM'L.	–	70	95	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQ}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQ} + I_{CCT}\,(N_T \times D_H) + I_{CCD}\,(f_{OP})$$

D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{OP} = Operating frequency in Megahertz.

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \le$ 0V and $V_{IH} \ge$ 3V for AC tests.

IDT49C460B AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT49C460B over the 0°C to +70°C commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 5%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-7}	$DATA_{0-31}$	ERROR	MULT ERROR
$DATA_{0-31}$	25	30(1)	25	27
CB_{0-7} (CODE ID 00, 11)	14	30	17	20
CB_{0-7} (CODE ID 10)	16	18	19	21
$\overline{GENERATE}$	21	23	23	23
CORRECT (Not Internal Control Mode)	–	23	–	–
DIAG MODE (Not Internal Control Mode)	17	26	20	24
CODE $ID_{0,1}$	18	26	21	26
LE_{IN} (From latched to transparent)	27	38(2)	30	33
LE_{OUT} (From latched to transparent)	–	12	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	15	29	19	22
Internal Control Mode: LE_{DIAG} (From latched to transparent)	16	32	19	24
Internal Control Mode: $DATA_{0-31}$ (Via Diagnostic Latch)	16	32	20	25

NOTES:
1. $DATA_{IN}$ to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 5A below.
2. LE_{IN} to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 5B.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-31}$	LE_{IN}	4	4
CB_{0-7}	LE_{IN}	4	4
$DATA_{0-31}$	LE_{OUT}	19	0
CB_{0-7} (CODE ID 00, 11)	LE_{OUT}	15	0
CB_{0-7} (CODE ID 10)	LE_{OUT}	15	0
CORRECT	LE_{OUT}	11	0
DIAG MODE	LE_{OUT}	17	0
CODE $ID_{0,1}$	LE_{OUT}	17	0
LE_{IN}	LE_{OUT}	20	0
$DATA_{0-31}$	LE_{DIAG}	4	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE		DISABLE	
		MIN.	MAX.	MIN.	MAX.
$\overline{OE}$ $BYTE_{0-3}$	$DATA_{0-31}$	10	23	10	19
$\overline{OE}_{SC}$	SC_{0-7}	10	24	10	20

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	9

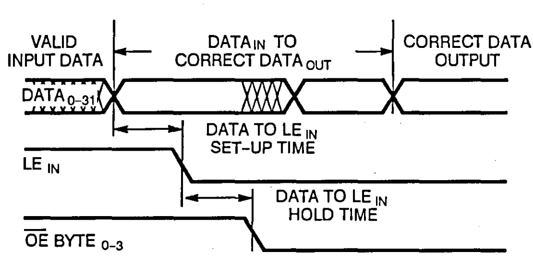


Figure 5A.

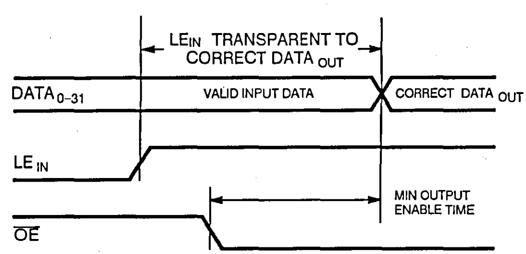


Figure 5B.

IDT49C460B AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT49C460B over the -55°C to +125°C military temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 10%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-7}	$DATA_{0-31}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-31}$	28	33(1)	28	30
CB_{0-7} (CODE ID 00, 11)	17	33	20	23
CB_{0-7} (CODE ID 10)	19	23	22	24
$\overline{GENERATE}$	24	26	26	26
CORRECT (Not Internal Control Mode)	–	26	–	–
DIAG MODE (Not Internal Control Mode)	20	29	23	27
CODE $ID_{0,1}$	21	29	24	29
LE_{IN} (From latched to transparent)	30	41(2)	33	36
LE_{OUT} (From latched to transparent)	–	15	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	18	32	22	25
Internal Control Mode: LE_{DIAG} (From latched to transparent)	19	35	22	27
Internal Control Mode: $DATA_{0-31}$ (Via Diagnostic Latch)	19	35	23	28

NOTES:

1. $DATA_{IN}$ to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 6A below.
2. LE_{IN} to correct $DATA_{OUT}$ measurement requires timing as shown in Figure 6B below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-31}$	LE_{IN}	4	4
CB_{0-7}	LE_{IN}	4	4
$DATA_{0-31}$	LE_{OUT}	23	0
CB_{0-7} (CODE ID 00, 11)	LE_{OUT}	18	0
CB_{0-7} (CODE ID 10)	LE_{OUT}	18	0
CORRECT	LE_{OUT}	14	0
DIAG MODE	LE_{OUT}	20	0
CODE $ID_{0,1}$	LE_{OUT}	20	0
LE_{IN}	LE_{OUT}	23	0
$DATA_{0-31}$	LE_{DIAG}	4	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE		DISABLE	
		MIN.	MAX.	MIN.	MAX.
$\overline{OE}$ $BYTE_{0-3}$	$DATA_{0-31}$	10	25	10	21
$\overline{OE}_{SC}$	SC_{0-7}	10	27	10	22

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12

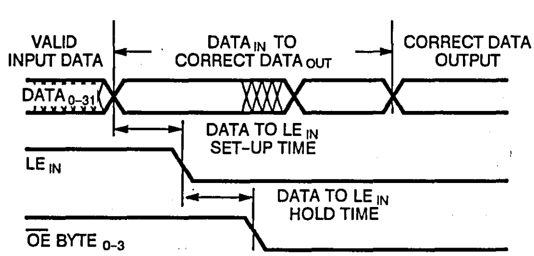


Figure 6A.

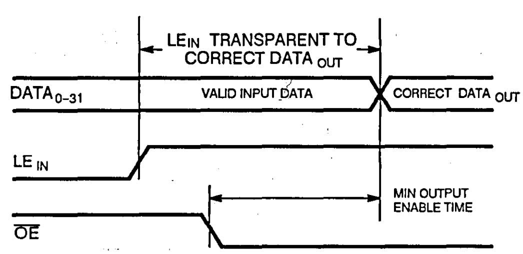


Figure 6B.

IDT49C460A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT49C460A over the 0°C to +70°C commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 5%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-7}	$DATA_{0-31}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-31}$	27	36[1]	30	33
CB_{0-7} (CODE ID 00, 11)	16	34	19	23
CB_{0-7} (CODE ID 10)	16	20	19	21
$\overline{GENERATE}$	21	23	25	25
CORRECT (Not Internal Control Mode)	–	23	–	–
DIAG MODE (Not Internal Control Mode)	17	26	20	24
CODE $ID_{0,1}$	18	26	21	26
LE_{IN} (From latched to transparent)	27	38[2]	30	33
LE_{OUT} (From latched to transparent)	–	12	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	15	29	19	22
Internal Control Mode: LE_{DIAG} (From latched to transparent)	16	32	19	24
Internal Control Mode: $DATA_{0-31}$ (Via Diagnostic Latch)	16	32	20	25

NOTES:

1. $DATA_{IN}$ to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 7A below.
2. LE_{IN} to correct $DATA_{OUT}$ measurement requires timing as shown in Figure 7B below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-31}$	LE_{IN}	5	4
CB_{0-7}	LE_{IN}	5	4
$DATA_{0-31}$	LE_{OUT}	23	0
CB_{0-7} (CODE ID 00, 11)	LE_{OUT}	15	0
CB_{0-7} (CODE ID 10)	LE_{OUT}	15	0
CORRECT	LE_{OUT}	11	0
DIAG MODE	LE_{OUT}	17	0
CODE $ID_{0,1}$	LE_{OUT}	17	0
LE_{IN}	LE_{OUT}	25	0
$DATA_{0-31}$	LE_{DIAG}	5	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE		DISABLE	
		MIN.	MAX.	MIN.	MAX.
$\overline{OE}$ $BYTE_{0-3}$	$DATA_{0-31}$	10	23	10	19
$\overline{OE}_{SC}$	SC_{0-7}	10	24	10	20

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	9

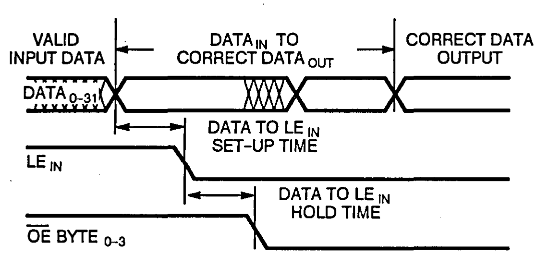


Figure 7A.

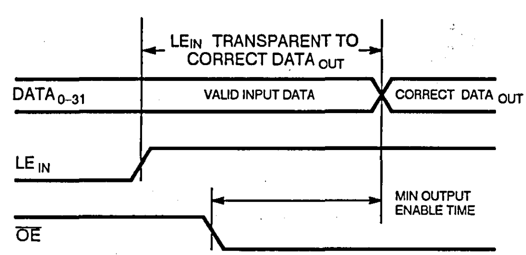


Figure 7B.

IDT49C460A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT49C460A over the -55°C to +125°C military temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 10%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-7}	$DATA_{0-31}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-31}$	30	39[1]	33	36
CB_{0-7} (CODE ID 00, 11)	19	37	22	26
CB_{0-7} (CODE ID 10)	19	23	22	24
$\overline{GENERATE}$	24	26	28	28
CORRECT (Not Internal Control Mode)	–	26	–	–
DIAG MODE (Not Internal Control Mode)	20	29	23	27
CODE $ID_{0,1}$	21	29	24	29
LE_{IN} (From latched to transparent)	30	41[2]	33	36
LE_{OUT} (From latched to transparent)	–	15	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	18	32	22	25
Internal Control Mode: LE_{DIAG} (From latched to transparent)	19	35	22	27
Internal Control Mode: $DATA_{0-31}$ (Via Diagnostic Latch)	19	35	23	28

NOTES:

1. $DATA_{IN}$ to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 8A below.
2. LE_{IN} to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 8B below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-31}$	LE_{IN}	5	4
CB_{0-7}	LE_{IN}	5	4
$DATA_{0-31}$	LE_{OUT}	27	0
CB_{0-7} (CODE ID 00, 11)	LE_{OUT}	18	0
CB_{0-7} (CODE ID 10)	LE_{OUT}	18	0
CORRECT	LE_{OUT}	14	0
DIAG MODE	LE_{OUT}	20	0
CODE $ID_{0,1}$	LE_{OUT}	20	0
LE_{IN}	LE_{OUT}	28	0
$DATA_{0-31}$	LE_{DIAG}	5	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L= 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE		DISABLE	
		MIN.	MAX.	MIN.	MAX.
$\overline{OE}$ $BYTE_{0-3}$	$DATA_{0-31}$	10	25	10	21
$\overline{OE}_{SC}$	SC_{0-7}	10	27	10	22

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12

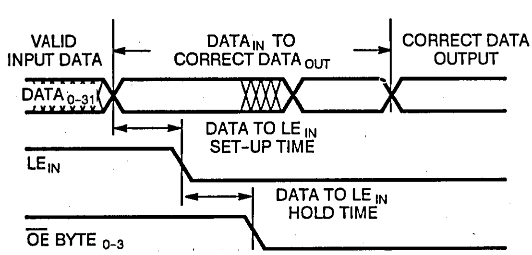


Figure 8A.

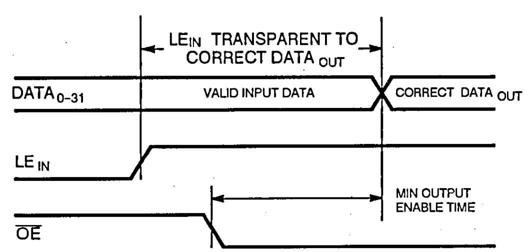


Figure 8B.

IDT49C460 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT49C460 over the 0°C to +70°C commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 5%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-7}	$DATA_{0-31}$	$\overline{\text{ERROR}}$	$\overline{\text{MULT ERROR}}$
$DATA_{0-31}$	37	49(1)	40	45
CB_{0-7} (CODE ID 00, 11)	22	46	26	31
CB_{0-7} (CODE ID 10)	22	30	26	29
$\overline{\text{GENERATE}}$	29	31	30	30
CORRECT (Not Internal Control Mode)	–	31	–	–
DIAG MODE (Not Internal Control Mode)	23	35	27	33
CODE $ID_{0,1}$	25	35	29	35
LE_{IN} (From latched to transparent)	37	51(2)	41	45
LE_{OUT} (From latched to transparent)	–	17	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	21	38	26	30
Internal Control Mode: LE_{DIAG} (From latched to transparent)	22	42	26	33
Internal Control Mode: $DATA_{0-31}$ (Via Diagnostic Latch)	22	42	27	34

NOTES:
1. $DATA_{IN}$ to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 9A below.
2. LE_{IN} to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 9B below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-31}$	LE_{IN}	6	4
CB_{0-7}	LE_{IN}	5	4
$DATA_{0-31}$	LE_{OUT}	30	0
CB_{0-7} (CODE ID 00, 11)	LE_{OUT}	20	0
CB_{0-7} (CODE ID 10)	LE_{OUT}	20	0
CORRECT	LE_{OUT}	16	0
DIAG MODE	LE_{OUT}	23	0
CODE $ID_{0,1}$	LE_{OUT}	23	0
LE_{IN}	LE_{OUT}	31	0
$DATA_{0-31}$	LE_{DIAG}	6	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE		DISABLE	
		MIN.	MAX.	MIN.	MAX.
$\overline{\text{OE}}$ $BYTE_{0-3}$	$DATA_{0-31}$	10	27	10	23
$\overline{\text{OE}}_{SC}$	SC_{0-7}	10	28	10	24

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12

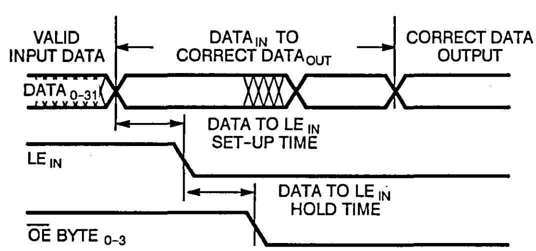


Figure 9A.

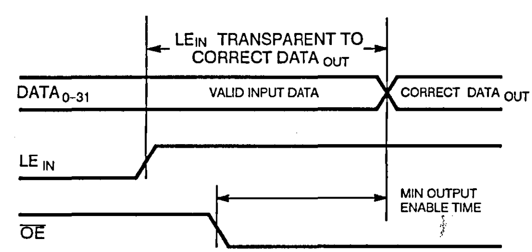


Figure 9B.

IDT49C460 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT49C460 over the -55°C to +125°C military temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 10%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-7}	$DATA_{0-31}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-31}$	40	52[1]	44	48
CB_{0-7} (CODE ID 00, 11)	25	49	29	34
CB_{0-7} (CODE ID 10)	25	33	29	32
$\overline{GENERATE}$	32	34	33	33
CORRECT (Not Internal Control Mode)	–	34	–	–
DIAG MODE (Not Internal Control Mode)	26	38	30	36
CODE $ID_{0,1}$	28	38	32	38
LE_{IN} (From latched to transparent)	40	54[2]	44	48
LE_{OUT} (From latched to transparent)	–	20	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	24	42	29	33
Internal Control Mode: LE_{DIAG} (From latched to transparent)	25	47	29	36
Internal Control Mode: $DATA_{0-31}$ (Via Diagnostic Latch)	25	47	30	37

NOTES:

1. $DATA_{IN}$ to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 10A below.
2. LE_{IN} to Correct $DATA_{OUT}$ measurement requires timing as shown in Figure 10B below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-31}$	LE_{IN}	6	4
CB_{0-7}	LE_{IN}	5	4
$DATA_{0-31}$	LE_{OUT}	36	0
CB_{0-7} (CODE ID 00, 11)	LE_{OUT}	24	0
CB_{0-7} (CODE ID 10)	LE_{OUT}	24	0
CORRECT	LE_{OUT}	20	0
DIAG MODE	LE_{OUT}	28	0
CODE $ID_{0,1}$	LE_{OUT}	28	0
LE_{IN}	LE_{OUT}	37	0
$DATA_{0-31}$	LE_{DIAG}	6	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE		DISABLE	
		MIN.	MAX.	MIN.	MAX.
$\overline{OE}$ $BYTE_{0-3}$	$DATA_{0-31}$	10	29	10	25
$\overline{OE}_{SC}$	SC_{0-7}	10	30	10	26

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

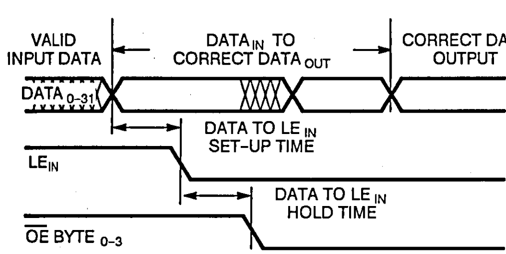


Figure 10A.

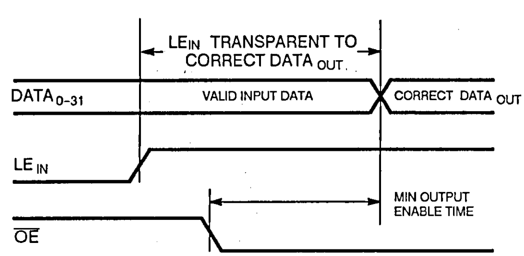


Figure 10B.

INPUT/OUTPUT INTERFACE CIRCUIT

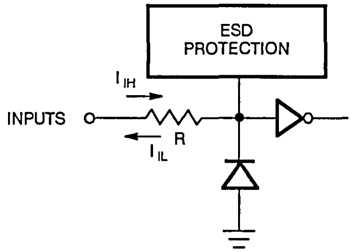


Figure 11. Input Structure (All Inputs)

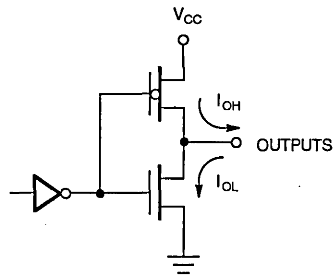


Figure 12. Output Structure

TEST LOAD CIRCUIT

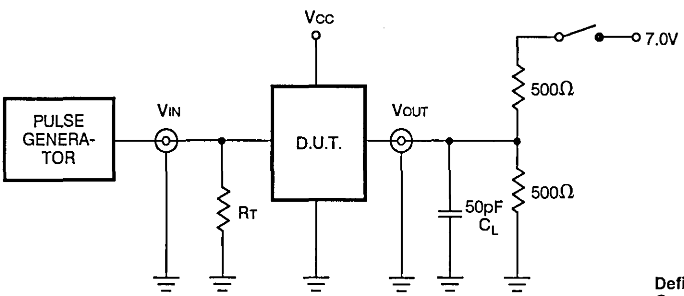


Figure 13.

Test	Switch
Open Drain Disable Low Enable Low	Closed
All other outputs	Open

Definitions:
C_L = Load capacitance includes jig and probe capacitance.
R_T = Termination should be equal to Z_{OUT} of pulse generator.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 13

ORDERING INFORMATION

IDT 49C460 X X X
Device Type / Speed / Package / Process/Temperature Range

Process/Temperature Range:
- BLANK — Commercial (0°C to +70°C)
- B — Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:
- XC — SHRINK-DIP Sidebraze (70 mil centers)
- L — Leadless Chip Carrier (50 mil centers)
- XL — Leadless Chip Carrier (25 mil centers)
- G — Pin Grid Array
- J — Plastic Leaded Chip Carrier
- PG — Plastic Pin Grid Array

Speed:
- Blank — Standard Speed
- A — High-Speed
- B — Ultra-High-Speed

Device Type:
- 49C460 — 32-Bit E.D.C.

9

REDUCED INSTRUCTION SET COMPUTER (RISC) PROCESSORS

The broadening scope and increasing complexity of modern computer applications demand computer architectures that deliver high performance across a wide range of applications, at increasingly lower cost. This need is most effectively addressed by a new computer architecture known as Reduced Instruction Set Computer (RISC). Over ten years ago, researchers at IBM discovered that, although microprocessors and their instruction sets (Complex Instruction Set Computers, or CISC) were growing more complex, high-level language compilers such as Pascal, FORTRAN and C actually used only a fraction of those instructions. Further research at IBM, Stanford University and University of California, Berkeley led to the development of the RISC architecture.

Unlike traditional CISC processors that force increased circuit complexity to improve performance, a RISC processor has a very small instruction set that performs basic functions. With fewer instructions, RISC processors use little or no microcode, eliminating the need for translation between machine instructions and microcode to deliver higher system performance. The machine instructions performed in a CISC processor's hardware are, instead, handled by software functions in a RISC processor.

The IDT79R2000 family of RISC processors, including the IDT79R2000 Central Processing Unit (CPU), IDT79R2010 Floating-Point Unit (FPU) and IDT79R2020 Write Buffers, was developed at MIPS Computer Systems, founded by researchers from Stanford University. The IDT79R2000 family offers a path to significant improvements in system performance without the increasingly complex circuitry used to improve the performance of CISC processors.

TABLE OF CONTENTS

CONTENTS **PAGE**

Integrated Device Technology, Inc.

RISC CPU PROCESSOR

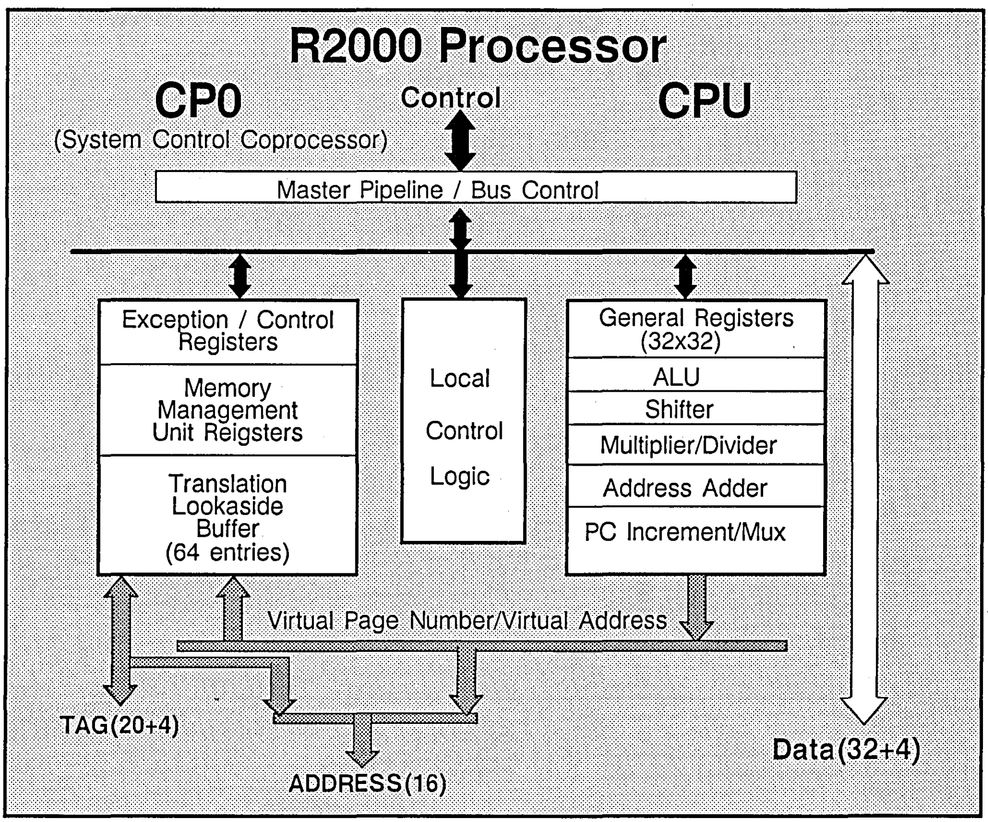
ADVANCE INFORMATION IDT79R2000

FEATURES:

- Full 32-bit Operation—Thirty-two 32-bit registers and all instructions and addresses are 32-bit
- Efficient Pipelining—The CPU's 5-stage pipeline design assists in obtaining an execution rate approaching one instruction per cycle. Pipeline stalls and exceptions are handled precisely and efficiently
- On-Chip Cache Control—The IDT79R2000 provides a high bandwidth memory interface that handles separate external Instruction and Data Caches ranging in size from 4 to 64 Kbytes each. Both the caches are accessed during a single CPU cycle. All cache control is on-chip
- On-Chip Memory Management Unit—A fully-associative, 64 entry Transition Lookaside Buffer (TLB) provides fast address translation for virtual-to-physical memory mapping of the 4 Gigabyte virtual address space
- Coprocessor Interface—The IDT79R2000 generates all addresses and handles memory interface control for up to three additional tightly coupled external processors
- Optimizing Compilers are available for C, Fortran, Pascal
- UNIX™ System V.3 and BSD 4.3 operating systems supported
- High-speed CEMOS™ technology
- Pin, functionally and software compatible with the MIPS Computer Systems R2000 RISC CPU
- 20-25MHz clock rate yields 12 to 15 MIPS sustained throughput
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT79R2000 processor consists of two tightly-coupled processors implemented on a single chip. The first processor is a full 32-bit CPU incorporating RISC (Reduced Instruction Set Computer) techniques to achieve a new standard of microprocessor performance. The second processor is a system control coprocessor (CP0), containing a TLB (Translation Lookaside Buffer) and control registers to support a virtual memory subsystem with a dual-cache bandwidth of up to 133 Mbytes/second. Figure 1 shows the functions incorporated within the IDT79R2000.



9

IDT79R2000 CPU Registers

The IDT79R2000 CPU provides 32 general purpose 32-bit registers, a 32-bit Program Counter, and two 32-bit registers that hold the results of integer multiply and divide operations. The CPU registers are shown in Figure 2. Note that there is no Program Status Word (PSW) register shown in this figure: the functions traditionally provided by a PSW register instead provided in the *Status* and *Cause* registers incorporated within the System Control Coprocessor (CP0).

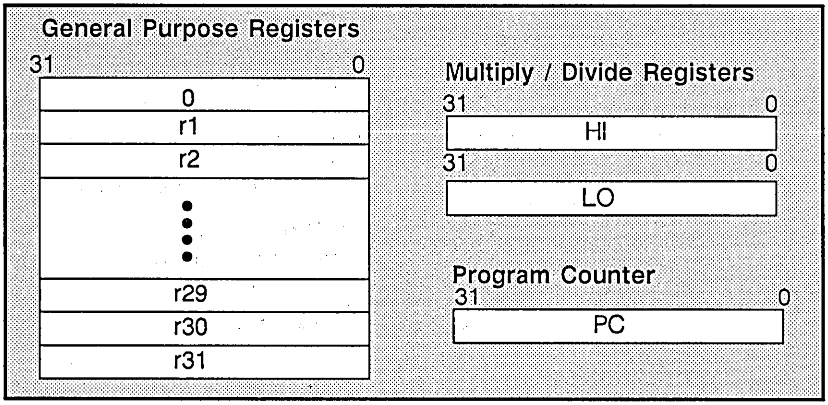


Figure 2. IDT79R2000 CPU Registers

Instruction Set Overview

All IDT79R2000 instructions are 32 bits long and there are only three instruction formats as shown in Figure 3. This approach simplifies instruction decoding. More complicated (and less frequently used) operations and addressing modes can be synthesized by the compiler using sequences of simple instructions.

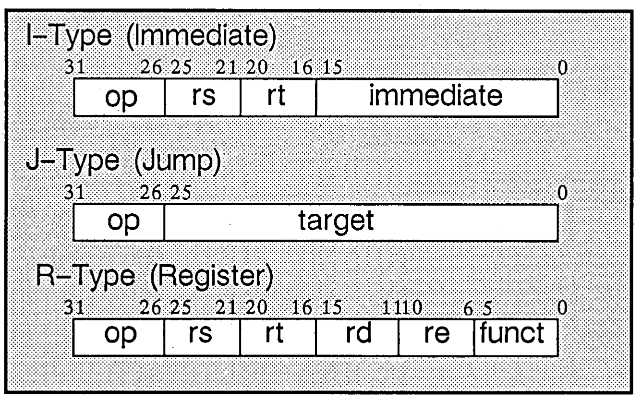


Figure 3. IDT79R2000 Instruction Formats

The IDT79R2000 instruction set can be divided into the following groups:

- **Load/Store** instructions move data between memory and general registers. They are all I-type instructions, since the only addressing mode supported is base register plus 16-bit, signed immediate offset.
- **Computational** instructions perform arithmetic, logical and shift operations on values in registers. They occur in both R-type (both operands and the result are registers) and I-type (one operand is a 16-bit immediate) formats.
- **Jump and Branch** instructions change the control flow of a program. Jumps are always to a paged absolute address formed by combining a 26-bit target with four bits of the Program counter (J-type format, for subroutine calls), or 32-bit register byte addresses (R-type, for returns and dispatches). Branches have 16-bit offsets relative to the program counter (I-type). Jump and Link instructions save a return address in Register 31.
- **Coprocessor** instructions perform operations in the coprocessors. Coprocessor Loads and Stores are I-type. Coprocessor computational instructions have coprocessor-dependent formats (see coprocessor manuals).
- **Coprocessor 0** instructions perform operations on the System Control Coprocessor (CP0) registers to manipulate the memory management and exception handling facilities of the processor.
- **Special** instructions perform a variety of tasks, including movement of data between special and general registers, system calls, and breakpoint. They are always R-type.

Table 1 lists the instruction set of the IDT79R2000 processor.

OP	DESCRIPTION	OP	DESCRIPTION
	Load/Store Instructions		**Multiply/Divide Instructions**
LB	Load Byte	MULT	Multiply
LBU	Load Byte Unsigned	MULTU	Multiply Unsigned
LH	Load Halfword	DIV	Divide
LHU	Load Halfword Unsigned	DIVU	Divide Unsigned
LW	Load Word	MFHI	Move From HI
LWL	Load Word Left	MTHI	Move To HI
LWR	Load Word Right	MFLO	Move From LO
SB	Store Byte	MTLO	Move To LO
SH	Store Halfword		**Jump and Branch Instructions**
SW	Store Word	J	Jump
SWL	Store Word Left	JAL	Jump and Link
SWR	Store Word Right	JR	Jump to Register
	Arithmetic Instructions (ALU Immediate)	JALR	Jump and Link Register
ADDI	Add Immediate	BEQ	Branch on Equal
ADDIU	Add Immediate Unsigned	BNE	Branch on Not Equal
SLTI	Set on Less Than Immediate	BLEZ	Branch on Less than or Equal to Zero
SLTIU	Set on Less Than Immediate Unsigned	BGTZ	Branch on Greater Than Zero
ANDI	AND Immediate	BLTZ	Branch on Less Than Zero
ORI	OR Immediate	BGEZ	Branch on Greater than or Equal to Zero
XORI	Exclusive OR Immediate	BLTZAL	Branch on Less Than Zero and Link
LUI	Load Upper Immediate	BGEZAL	Branch on Greater than or Equal to Zero and Link
	Arithmetic Instructions (3-operand, register-type)		**Special Instructions**
ADD	Add	SYSCALL	System Call
ADDU	Add Unsigned	BREAK	Break
SUB	Subtract		**Coprocessor Instructions**
SUBU	Subtract Unsigned	LWCz	Load Word from Coprocessor
SLT	Set on Less Than	SWCz	Store Word to Coprocessor
SLTU	Set on Less Than Unsigned	MTCz	Move To Coprocessor
AND	AND	MFCz	Move From Coprocessor
OR	OR	CTCz	Move Control to Coprocessor
XOR	Exclusive OR	CFCz	Move Control From Coprocessor
NOR	NOR	COPz	Coprocessor Operation
	Shift Instructions	BCzT	Branch on Coprocessor z True
SLL	Shift Left Logical	BCzF	Branch on Coprocessor z False
SRL	Shift Right Logical		**System Control Coprocessor (CP0) Instructions**
SRA	Shift Right Arithmetic	MTC0	Move To CP0
SLLV	Shift Left Logical Variable	MFC0	Move From CP0
SRLV	Shift Right Logical Variable	TLBR	Read indexed TLB entry
SRAV	Shift Right Arithmetic Variable	TLBWI	Write Indexed TLB entry
		TLBWR	Write Random TLB entry
		TLBP	Probe TLB for matching entry
		RFE	Restore From Exception

Table 1. IDT79R2000 Instruction Summary

IDT79R2000 System Control Coprocessor (CP0)

The IDT79R2000 can operate with up to four tightly-coupled coprocessors (designated CP0 through CP3). The System Control Coprocessor (or CP0), is incorporated on the IDT79R2000 chip and supports the virtual memory system and exception handling functions of the IDT79R2000. The virtual memory system is implemented using a Translation Lookaside Buffer and a group of programmable registers as shown in Figure 4.

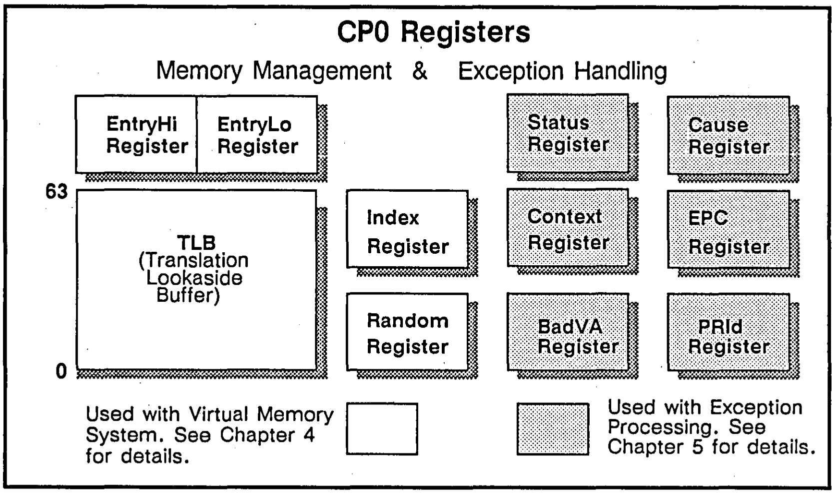


Figure 4. The CP0 Registers

System Control Coprocessor (CP0) Registers

The CP0 registers shown in Figure 4 are used to manipulate the memory management and exception handling capabilities of the IDT79R2000. Table 2 provides a brief description of each register.

REGISTER	DESCRIPTION
EntryHi	High half of a TLB entry
EntryLo	Low half of a TLB entry
Index	Programmable pointer into TLB array
Random	Pseudo-random pointer into TLB array
Status	Mode, interrupt enables, and diagnostic status info
Cause	Indicates nature of last exception
EPC	Exception Program Counter
Context	Pointer into kernel's virtual Page Table Entry array
BadVA	Most recent bad virtual address
PRId	Processor revision identification

Table 2. System Control Coprocessor (CP0) Registers

Memory Management System

The IDT79R2000 has an addressing range of 4 Gbytes. However, since most IDT79R2000 systems implement a physical memory smaller than 4 Gbytes, the IDT79R2000 provides for the logical expansion of memory space by translating addresses composed in a large virtual address space into available physical memory addresses. The 4 GByte address space is divided into 2 Gbytes for users and 2 GBytes for the kernel.

The TLB (Translation Lookaside Buffer)

Virtual memory mapping is assisted by the Translation Lookaside Buffer (TLB). The on-chip TLB provides very fast virtual memory access and is well-matched to the requirements of multi-tasking operating systems. The fully-associative TLB contains 64 entries, each of which maps a 4-Kbyte page, with controls for read/write access, cacheability, and process identification. The TLB allows each user to access up to 2 Gbytes of virtual address space.

IDT79R2000 Operating Modes

The IDT79R2000 has two operating modes: *User* mode and *Kernel* mode. The IDT79R2000 normally operates in the User mode until an exception is detected forcing it into the Kernel mode. It remains in the Kernel mode until a Restore From Exception *(RFE)* instruction is executed. The manner in which memory addresses are translated or *mapped* depends on the operating mode of the IDT79R2000. Figure 5 shows the virtual address space for the two operating modes.

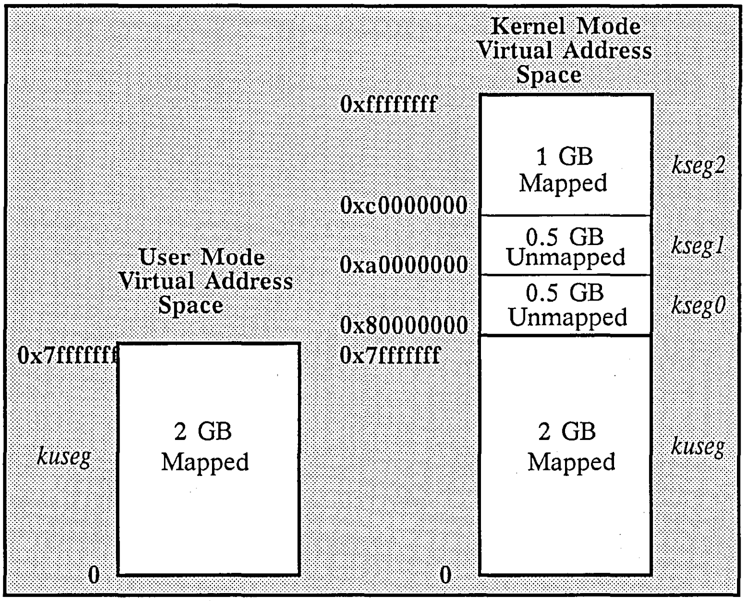


Figure 5. IDT79R2000 Virtual Addressing

User Mode—in this mode, a single, uniform virtual address space (kuseg) of 2 Gbyte is available. Each virtual address is extended with a 6-bit process identifier field to form unique virtual addresses for up to 64 user processes. All references to this segment are mapped through the TLB. Use of the cache is determined by bit settings for each page within the TLB entries.

Kernel Mode—four separate segments are defined in this mode:

- *kuseg*—when in the kernel mode, references to this segment are treated just like user mode references, thus streamlining kernel access to user data.
- *kseg0*—references to this 512 Mbyte segment use cache memory but are not mapped through the TLB. Instead, they always map to the first 0.5 GBytes of physical memory.
- *kseg1*—references to this 512 Mbyte segment are not mapped through the TLB and do not use the cache. Instead, they are hard-mapped into the same 0.5 GByte segment of physical memory space as *kseg0*.
- *kseg2*—references to this 1 Gbyte segment are always mapped through the TLB and use of the cache is determined by bit settings within the TLB entries.

IDT79R2000 Pipeline Architecture

9

The execution of a single IDT79R2000 instruction consists of five primary steps:

1) **IF** – Fetch the instruction (I-Cache).
2) **RD** – Read any required operands from CPU registers while decoding the instruction.
3) **ALU** – Perform the required operation on instruction operands.
4) **MEM** – Access memory (D-Cache).
5) **WB** – Write back results to register file.

Each of these steps requires approximately one CPU cycle as shown in Figure 6 (parts of some operations lap over into another cycle while other operations require only 1/2 cycle).

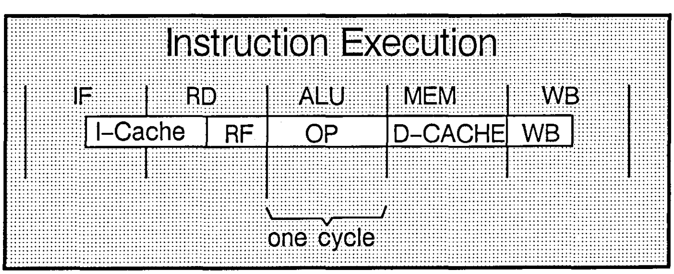


Figure 6. Instruction Execution Sequence

The IDT79R2000 uses a 5-stage pipeline to achieve an instruction execution rate approaching one instruction per CPU cycle. Thus, execution of five instructions at a time are overlapped as shown in Figure 7.

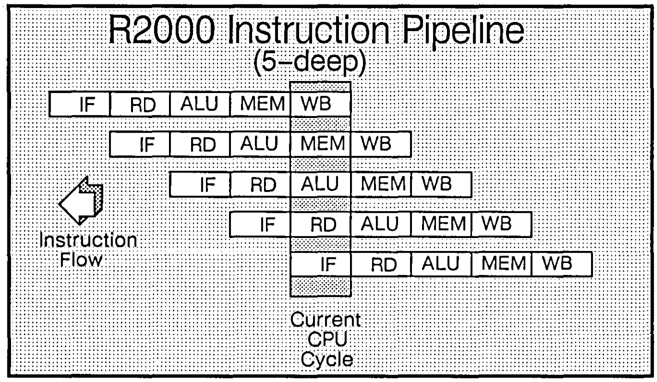


Figure 7. IDT79R2000 Instruction Pipeline

This pipeline operates efficiently because different CPU resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

Memory System Hierarchy

The high performance capabilities of the IDT79R2000 processor demand system configurations incorporating techniques frequently employed in large, mainframe computers but seldom encountered in systems based on more traditional microprocessors.

A primary goal of systems employing RISC techniques is to achieve an instruction execution rate of one instruction per CPU cycle. This approach to achieving this goal incorporates a number of RISC techniques including a compact and uniform instruction set, a deep instruction pipeline (as described above), and utilization of optimizing compilers. Many of the advantages obtained from these techniques can, however, be negated by an in efficient memory system.

Figure 8 illustrates memory in a simple microprocessor system. In this system, the CPU outputs addresses to memory and reads instructions and data from memory or writes data to memory. The memory space is completely undifferentiated: instructions, data, and I/O devices are all treated the same. In such a system, a primary limiting performance factor is memory bandwidth.

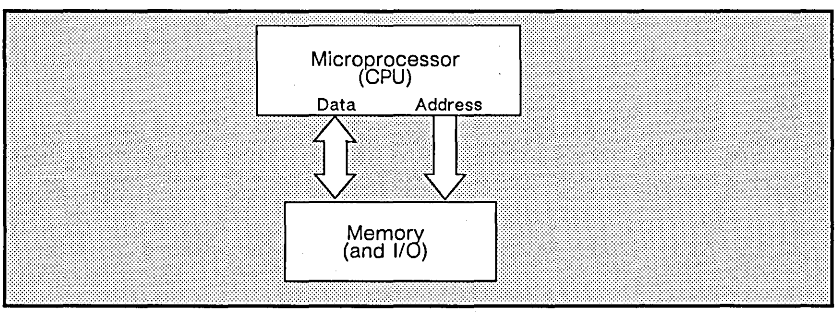


Figure 8. A Simple Microprocessor Memory System

Figure 9 illustrates a memory system that supports the significantly greater memory bandwidth required to take full advantage of the IDT79R2000's performance capabilities. The key features of this system are:

- **External Cache Memory**—Local, high-speed memory (called *cache* memory) is used to hold instructions and data that is repetitively accessed by the CPU (for example, within a program loop) and thus reduces the number of references that must be made to the slower speed main memory. Some microprocessors provide a limited amount of cache memory on the CPU chip itself. The external caches supported by the IDT79R2000 can be much larger; while a small cache can improve performance of some programs, significant improvements for a wide range of programs require large caches.
- **Separate Caches for data and Instructions**—Even with high-speed caches, memory speed can still be a limiting factor because of the fast cycle time of a high-performance microprocessor. The IDT79R2000 supports separate caches for instructions and data and alternates accesses of the two caches during each CPU cycle. Thus, the processor can obtain data and instructions at the cycle rate of the CPU using caches constructed with commercially available IDT static RAM devices.
- **Write Buffer**—In order to ensure data consistency, all data that is written to the data cache must also be written out to main memory. To relieve the CPU of this responsibility (and the inherent performance burden) the IDT79R2000 supports an interface to a write buffer. The IDT79R2020 Write Buffer captures data (and associated addresses) output by the CPU and ensures that the data is passed on to main memory.

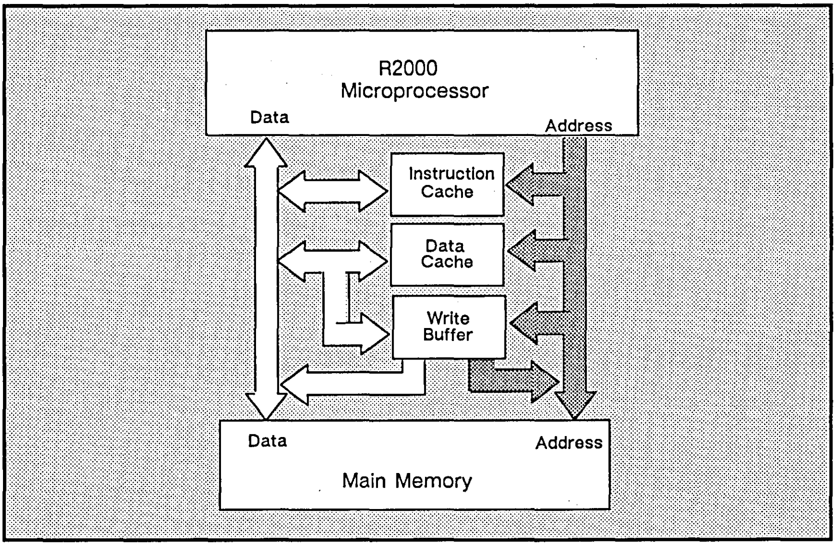


Figure 9. An IDT79R2000 System with a High-Performance Memory System

IDT79R2000 Processor Subsystem Interfaces

Figure 10 illustrates the three subsystem interfaces provided by the IDT79R2000 processor:

- **Cache control** interface (on-chip) for separate data and instruction caches permits implementation of off-chip caches using standard IDT SRAM devices.
- **Memory controller** interface for system (main) memory. This interface also includes the logic and signals to allow operation with a write buffer to further improve memory bandwidth.
- **Coprocessor** interface for tightly-coupled coprocessors such as a floating point accelerator. The IDT79R2000 generates all required cache and memory control signals including cache and memory addresses for attached coprocessors. Therefore, only the data bus and a few control signals need be connected to a coprocessor.

9

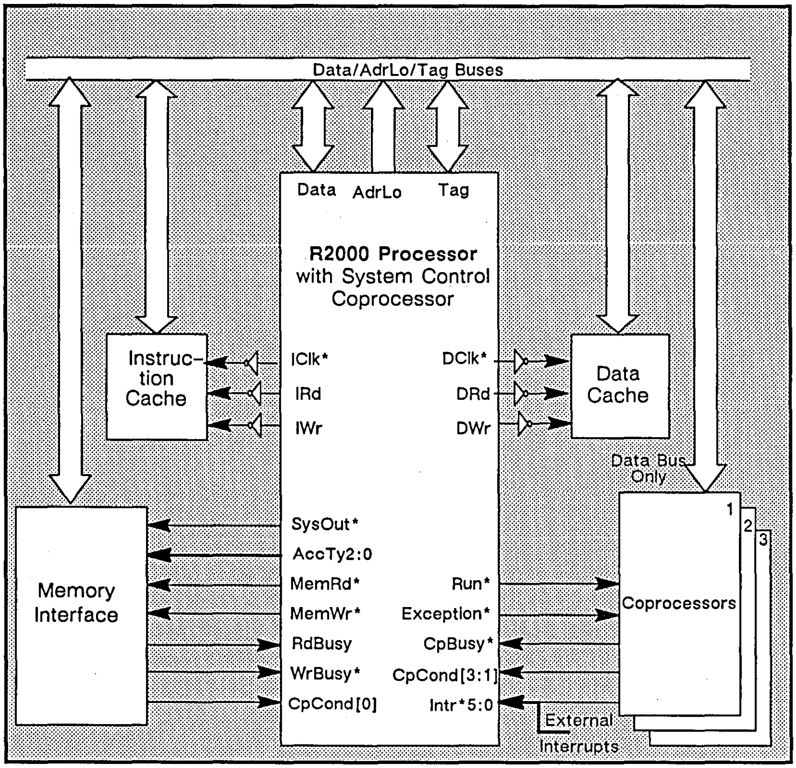


Figure 10. IDT79R2000 Subsystem Interfaces

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VCC14	AdrLo 6	AdrLo 10	AdrLo 11	VCC12	AdrLo 14	AdrLo 15	CpCond 0	CpCond 2	CpCond 3	Intr* 2	Intr* 5	Wr Busy*	Reset*	VCC10
B	AdrLo 3	reserved2	AdrLo 7	AdrLo 9	AdrLo 12	reserved3	AdrLo 13	CpCond 1	Intr* 1	Intr* 3	Cp Busy*	Bus Error*	reserved4	Tag12	Tag15
C	AdrLo 0	AdrLo 4	VCC13	AdrLo 5	AdrLo 8	Gnd13	Gnd12	VCC11	Intr* 0	Intr* 4	Rd Busy	Gnd11	Tag13	TagP0	Tag18
D	Data1	AdrLo 2	Gnd0										Tag14	Tag17	Tag19
E	Data P0	Data0	AdrLo 1										Tag16	Tag20	VCC9
F	VCC0	Data7	Data2										Gnd10	Tag21	Tag23
G	Data4	Data3	Gnd1										Gnd9	Tag22	TagP1
H	Data6	Data5	Data8										VCC8	Tag25	Tag24
J	Data 10	Data P1	Data 9										Tag28	Tag29	Tag26
K	Data 15	Data 11	Gnd2										Gnd8	Tag P2	Tag27
L	VCC1	Data 12	Data 17										Acc Typ2	Tag31	Tag30
M	Data 13	Data 16	Data P2										Gnd7	Acc Typ1	VCC7
N	Data 14	Data 18	Data 19	Gnd3	Data 24	Data P3	VCC3	VCC4	Gnd5	Gnd6	DRd	MemWr*	MemRd*	Run*	TagV
P	Data 23	Data 20	reserved0	Data 22	Data 26	Data 27	reserved1	Data 30	Clk2x Sys	Clk2x Rd	DClk*	IRd	IWr	Cp Sync*	Acc Typ0
Q	VCC2	Data 21	Data 25	Data 31	Data 28	Gnd4	Data 29	Exc*	Clk2x Phi	Clk2x Smp	Sys Out*	VCC5	IClk*	DWr	VCC6

Integrated Device Technology, Inc.

RISC FLOATING POINT ACCELERATOR (FPA)

ADVANCE INFORMATION
IDT79R2010

FEATURES:

- Hardware Support of Single- and Double-Precision Operations:
  - Floating-Point Add
  - Floating-Point Subtract
  - Floating-Point Multiply
  - Floating-Point Divide
  - Floating-Point Comparisons
  - Floating-Point Conversions
- Peak Speed: 20-25 mips (loads, stores and moves)
- Peak Speed: 10-12 MFLOPS (single- or double-precision)
- Cycle Time: 40-50ns (20-25MHz)
- Direct, High-Speed Interface to IDT79R2000 Processor
- Supports Full Conformance With IEEE 754-1985 Floating-Point Specification
- Floating-Point Registers: Sixteen 64-bit registers
- High-speed CEMOS™ technology
- Pin, functionally and software compatible with the MIPS Computer Systems R2010 RISC FPA
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT79R2010 Floating-Point Accelerator (FPA) operates in conjunction with the IDT79R2000 Processor and extends the IDT79R2000's instruction set to perform arithmetic operations on values in floating-point representations. The IDT79R2010 FPA, with associated system software, fully conforms to the requirements of ANSI/IEEE Standard 754-1985, "IEEE Standard for Binary Floating-Point Arithmetic." In addition, the architecture fully supports the standard's recommendations.

- **Full 64-bit Operation** - The IDT79R2010 contains sixteen, 64-bit registers that can each be used to hold single-precision or double-precision values. The FPA also includes a 32-bit status/control register that provides access to all IEEE-Standard exception handling capabilities.
- **Load/Store Instruction set** - like the IDT79R2000 processor, the IDT79R2010 uses a load/store-oriented instruction set, with single-cycle loads and stores. Floating-point operations are started in a single cycle and their execution is overlapped with other fixed point or floating-point operations.
- **Tightly-coupled coprocessor interface** - the FPA connects to the IDT79R2000 RISC processor to form a tightly-coupled unit with a seamless integration of floating point and fixed point instruction sets. Since each unit receives and executes instructions in parallel, some floating point instructions can execute at the same single-cycle per instruction rate as fixed point instructions.

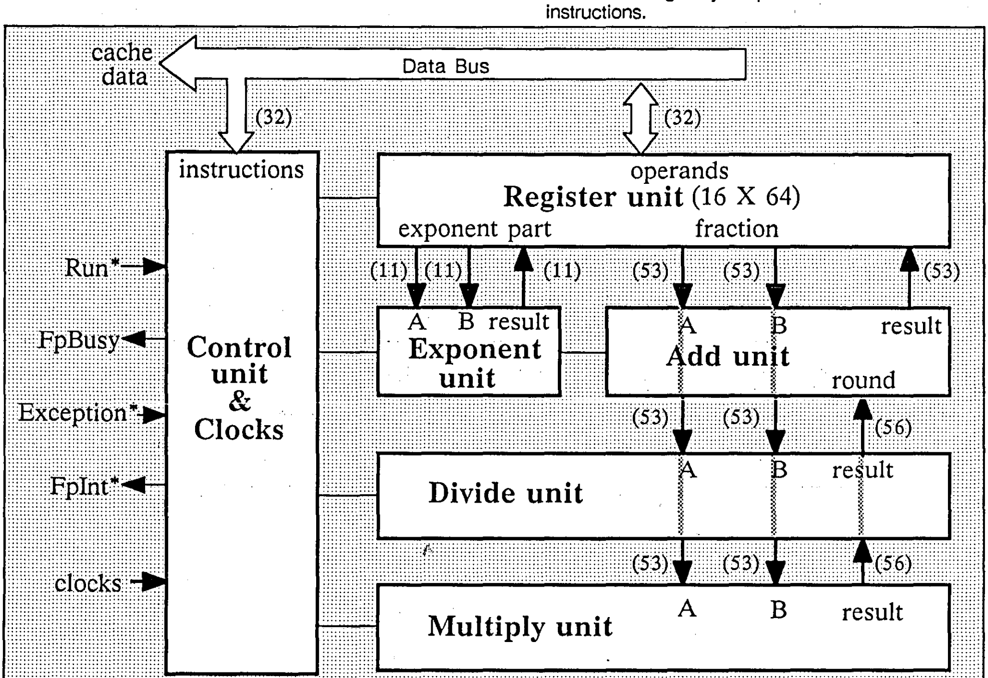


Figure 1 IDT79R2010 Functional Block Diagram

CEMOS is a trademark of Integrated Device Technology, Inc.

IDT79R2010 FPA REGISTERS

The IDT79R2010 FPA provides 32 general purpose 32-bit registers, a Control/Status register, and a Revision Identification register. The FPA registers are shown in Figure 2.

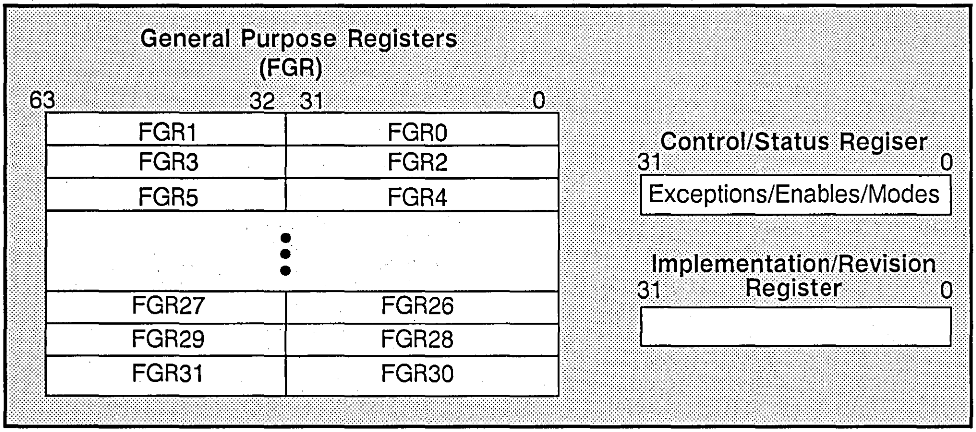


Figure 2 IDT79R2010 FPA Registers

Floating-point coprocessor operations reference three types of registers:

- Floating-Point Control Registers (FCR)
- Floating-Point General Registers (FGR)
- Floating-Point Registers (FPR).

Floating-Point General Registers (FGR)

There are 32 Floating-Point General Registers (FGR) on the FPA. They represent directly-addressable 32-bit registers, and can be accessed by Load, Store, or Move Operations.

Floating-Point Registers (FPR)

The 32 FGRs described in the preceding paragraph are also used to form sixteen 64-bit Floating-Point Registers (FPR). Pairs of general registers (FGRs), for example FGR0 and FGR1 (refer to Figure 2) are physically combined to form a single 64-bit FPR. The FPRs hold a value in either single- or double-precision floating-point format. Double-precision format FPRs are formed from two adjacent FGRs.

Floating-Point Control Registers (FCR)

There are 2 Floating-Point Control Registers (FCR) on the FPA. They can be accessed only by Move operations and include the following:

- Control/Status register, used to control and monitor exceptions, operating modes, and rounding modes;
- Revision register, containing revision information about the FPA.

COPROCESSOR OPERATION

The FPA continually monitors the IDT79R2000 processor instruction stream. If an instruction does not apply to the coprocessor, it is ignored; if an instruction does apply to the coprocessor, the FPA executes that instruction and transfers necessary result and exception data synchronously to the IDT79R2000 main processor.

The FPA performs three types of operations:

- Loads and Stores;
- Moves;
- Two- and three-register floating-point operations.

Load, Store, and Move Operations

Load, Store, and Move operations move data between memory or the IDT79R2000 Processor registers and the IDT79R2010 FPA registers. These operations perform no format conversions and cause no floating-point exceptions. Load, Store, and Move operations reference a single 32-bit word of either the Floating-Point General Registers (FGR) or the Floating-Point Control Registers (FCR).

Floating-Point Operations

The FPA supports the following single- and double-precision format floating-point operations:

- Add
- Subtract
- Multiply
- Divide
- Absolute Value
- Move
- Negate
- Compare

In addition, the FPA supports conversions between single-, double-precision floating-point formats and fixed-point formats.

Exceptions

The IDT79R2010 FPA supports all five IEEE standard exceptions:

- Invalid Operation
- Inexact Operation
- Division by Zero
- Overflow
- Underflow

The FPA also supports the optional, Unimplemented Operation exception that allows unimplemented instructions to trap to software emulation routines.

INSTRUCTION SET OVERVIEW

All IDT79R2010 instructions are 32 bits long and they can be divided into the following groups:

- **Load/Store and Move** instructions move data between memory, the main processor and the FPA general registers.
- **Computational** instructions perform arithmetic operations on floating point values in the FPA registers.
- **Conversion** instructions perform conversion operations between the various data formats.
- **Compare** instructions perform comparisons of the contents of registers and set a condition bit based on the results.

Table 1 lists the instruction set of the IDT79R2010 FPA.

OP	Description	OP	Description
	Load/Store/Move Instructions		**Computational Instructions**
LWC1	Load Word to FPA	ADD.fmt	Floating-point Add
SWC1	Store Word from FPA	SUB.fmt	Floating-point Subtract
MTC1	Move word To FPA	MUL.fmt	Floating-point Multiply
MFC1	Move word From FPA	DIV.fmt	Floating-point Divide
CTC1	Move Control word To FPA	ABS.fmt	Floating-point Absolute value
CFC1	Move Control word From FPA	MOV.fmt	Floating-point Move
		NEG.fmt	Floating-point Negate
	Conversion Instructions		**Compare Instructions**
CVT.S.fmt	Floating-point Convert to Single FP	C.cond.fmt	Floating-point Compare
CVT.D.fmt	Floating-point Convert to Double FP		
CVT.W.fmt	Floating-point Convert to fixed-point		

Table 1 IDT79R2010 Instruction Summary

IDT79R2010 PIPELINE ARCHITECTURE

The IDT79R2010 FPA provides an instruction pipeline that parallels that of the IDT79R2000 processor. The FPA, however, has a 6-stage pipeline instead of the 5-stage pipeline of the IDT79R2000: the additional FPA pipe stage is used to provide efficient coordination of exception responses between the FPA and main processor.

The execution of a single IDT79R2010 instruction consists of six primary steps:

1) **IF**—Instruction Fetch. The main processor calculates the instruction address required to read an instruction from the I-Cache. No action is required of the FPA during this pipe stage since the main processor is responsible for address generation.
2) **RD**—The instruction is present on the data bus during phase 1 of this pipe stage and the FPA decodes the data on the bus to determine if it is an instruction for the FPA.
3) **ALU**—If the instruction is an FPA instruction, instruction execution commences during this pipe stage.
4) **MEM**—If this is a coprocessor load or store instruction, the FPA presents or captures the data during phase 2 of this pipe stage.
5) **WB**—The FPA uses this pipe stage solely to deal with exceptions.
6) **FWB**—The FPA uses this stage to write back ALU results to its register file. This stage is the equivalent of the WB stage in the IDT79R2000 main processor.

Each of these steps requires approximately one FPA cycle as shown in Figure 6 (parts of some operations spill over into another cycle while other operations require only 1/2 cycle).

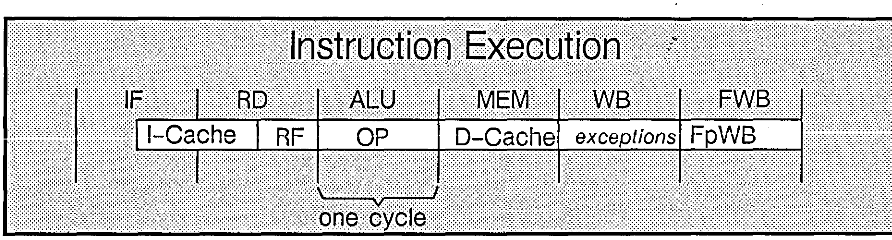


Figure 6 Instruction Execution Sequence

The IDT79R2010 uses a 6-stage pipeline to achieve an instruction execution rate approaching one instruction per FPA cycle. Thus, execution of six instructions at a time are overlapped as shown in Figure 7.

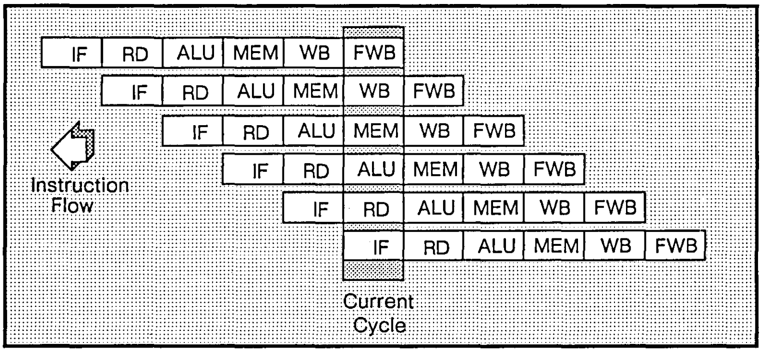
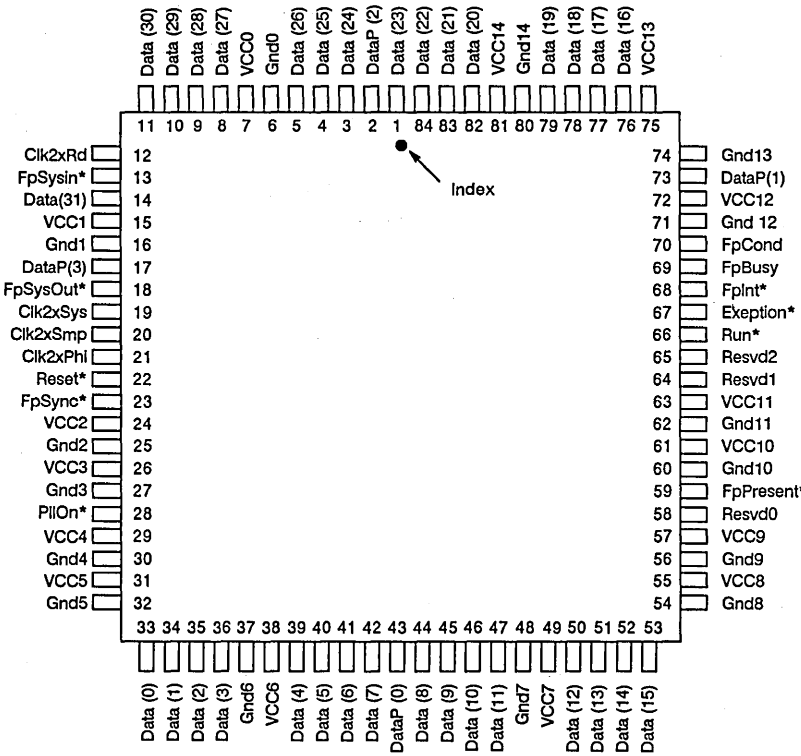


Figure 7 IDT79R2010 Instruction Pipeline

This pipeline operates efficiently because different FPA resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

PIN CONFIGURATION



PLCC

Integrated Device Technology, Inc.

RISC CPU WRITE BUFFER

ADVANCE INFORMATION
IDT79R2020

FEATURES

- Temporary storage buffers to enhance the performance of the IDT79R2000 RISC CPU processor
- Allows for write operations by the RISC CUP processor during Run cycles
- Each Write Buffer has four locations to handle an 8-bit address slice and a 9-bit data slice (including a parity bit)
- High-speed CEMOS™ technology
- Pin, functionally and software compatible with the MIPS Computer Systems R2020 Write Buffer
- Used in a 20-25MHz IDT79R2000 system configuration
- Military product complaint to MIL-STD-883, Class B

DESCRIPTION

The IDT79R2020 Write Buffer enhances the performance of IDT79R2000 systems by allowing the processor to perform write operations during Run cycles instead of resorting to time-consuming stall cycles. Each IDT79R2020 device handles an 8-bit slice of address, and a 9-bit slice of data (one parity bit per byte); thus, four IDT79R2020s provide 4-deep buffering of 32 bits of address and 36 bits of data and parity. Figure 1 illustrates the functional position of the Write Buffer in an IDT79R2000 system.

Whenever the processor performs a write operation, the write buffer captures the output data and its address (including the access type bits). The write buffer can hold up to four data-address sets while it waits to pass the data on to main memory. Transfers from the processor to the write buffers occur synchronously at the cycle rate of the processor and the write buffer signals the processor if it is unable to accept data. The write buffer also provides a set of handshake signals to communicate with a main memory controller and coordinate the transfer of write data to main memory.

The sections that follow describe these IDT79R2020 Write Buffer interfaces:

- the processor-write buffer interface
- the write buffer-main memory interface
- a miscellaneous, write buffer-board control interface.

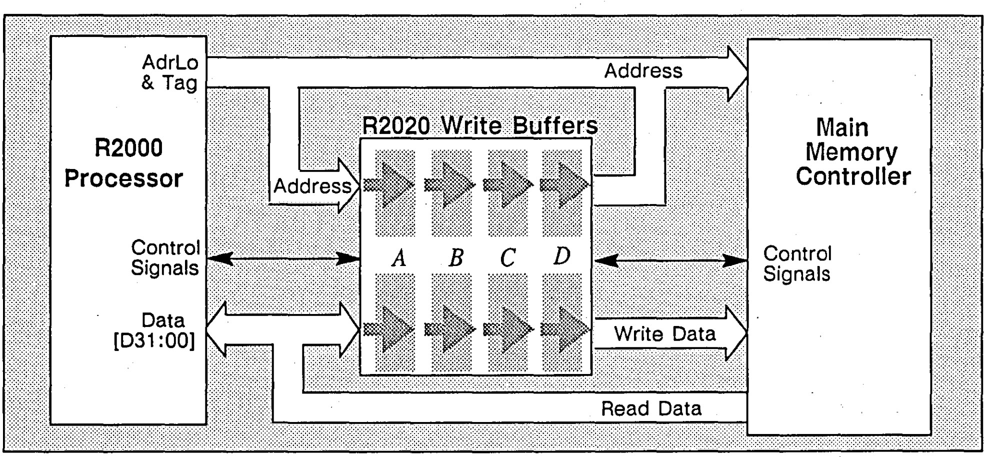


Figure 1. The IDT79R2020 Write Buffer in an IDT79R2000 System.

CEMOS is a trademark of Integrated Device Technology, Inc.

WRITE BUFFER - IDT79R2000 PROCESSOR INTERFACE

Figure 2 shows the signals comprising the write buffer interface to the IDT79R2000 (all descriptions in this appendix assume that four IDT79R2020 write buffers are used to implement a 32-bit, buffered interface). The AdrLo bus and Tag bus bits from the processor are both connected to the write buffer to form a 32-bit physical address that is captured by the buffers. Thirty-two bits of data, four bits of parity, and two access type bits are also captured by the write buffer. The paragraphs that follow describe the write buffer-processor interface signals and the timing of processor-to-write buffer data transfers.

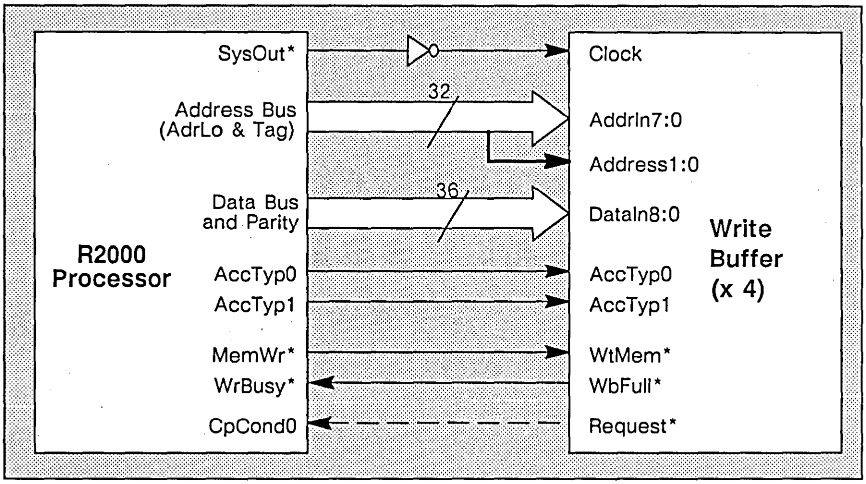


Figure 2. Write Buffer-IDT79R2000 Processor Interface.

Write Buffer–Processor Interface Signals

Clock

An inverted version of the IDT79R2000's SysOut* signal from the IDT79R2000 processor that synchronizes data transfers. The write buffer uses the trailing edge of *Clock* to latch the contents of the AdrLo bus and uses the leading *Clock* edge to latch the contents of the Data and Tag buses.

DataIn8:0

Nine input data lines from the IDT79R2000 processor's Data bus (eight bits of data and one bit of parity).

AddrIn7:0

Eight input address lines from the IDT79R2000 processor. The address lines are taken from the AdrLo and Tag buses.

Address1:0

The two least significant address bits from the IDT79R2000 processor. These two address bits must be connected to all four write buffers and are used in conjunction with the access type (*AcTyp1:0*) signals, the *Position1:0* signals, and the *BigEndian* signal to determine which byte(s) in a word are being written into a particular write buffer.

AccTypIn1:0

The access type signals from the IDT79R2000 processor specifying the size of a data access: word, tri-byte, half-word, or byte.

WtMem*

This input is connected to the MemWr* signal from the IDT79R2000 processor that is asserted whenever the processor is performing a store (write) operation.

Request*

The primary purpose of this signal is to request access to memory and is described later when the Write Buffer-Main Memory Interface is discussed. The Request* signal can also be connected to the CpCond0 input of the IDT79R2000 and can then be tested by software to determine if there is any data in the write buffer. Since Request* is deasserted if there is no data in the write buffer, software can determine if a previous write operation (for example, to an I/O device) has been completed before initiating a read or read status operation from that device.

WbFull*

The write buffer asserts this signal to the IDT79R2000's WrBusy* input whenever it cannot accept any more data; that is, when the current write will fill the buffer or the buffer has all address-data pairs occupied. The IDT79R2000 processor performs a write-busy stall if it needs to store data while the WbFull*/WrBusy* signal is asserted.

Data & Address Connections

Figure 3 illustrates how four write buffers are connected to the address and data outputs of the IDT79R2000 processor.

Address Inputs

Each write buffer device has eight address inputs (AdrIn7:0). The four low-order bits (AdrIn3:0) are clocked into the device on the trailing edge of the Clock signal and are taken from the IDT79R2000's AdrLo bus. The four high-order bits (AdrIn7:4) are clocked into the device on the rising edge of the Clock signal and are taken from the IDT79R2000's Tag bus.

Each device also has separate inputs (Address1, Address0) for the two low-order bits from the AdrLo bus. These bits must be input to each device since they comprise the byte pointer. Note in Figure 3 that the two low-order AdrIn inputs (AdrIn1:0) to write buffer device 0 are connected to ground since the Address1, Address0 inputs already supply these bits to the device.

Data Inputs

Each write buffer device has nine data inputs that are clocked into the device on the leading edge of the Clock signal and are taken from the IDT79R2000's Data bus. In Figure 3, each device captures eight bits of data and one bit of parity. Also note that the data bits assigned to each device correspond to the address bits connected to the device. This arrangement is required since data selection is dependent on a combination of the AccType signals and the two low order address bits. The arrangement also simplifies system utilization of the "Read Error Address" feature described later in this appendix.

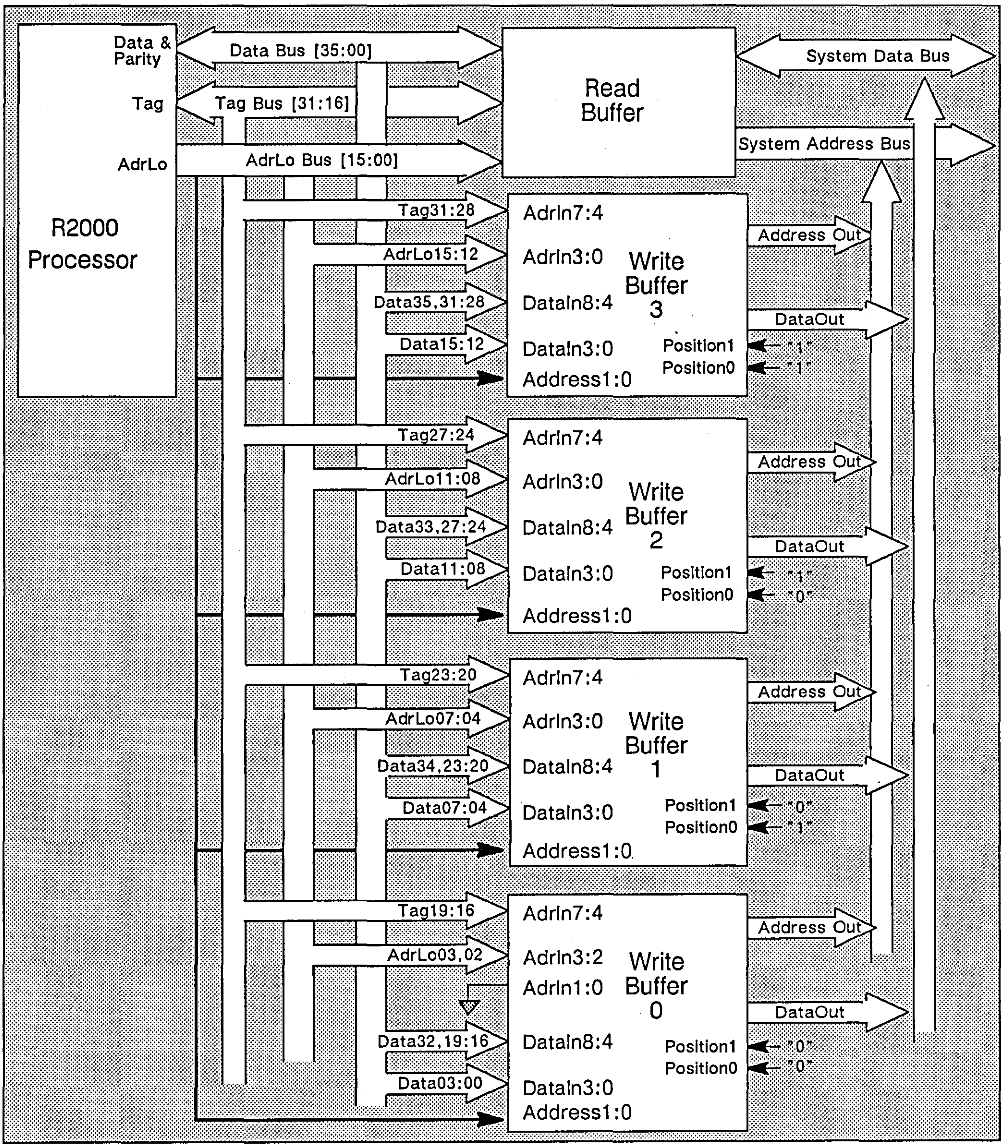
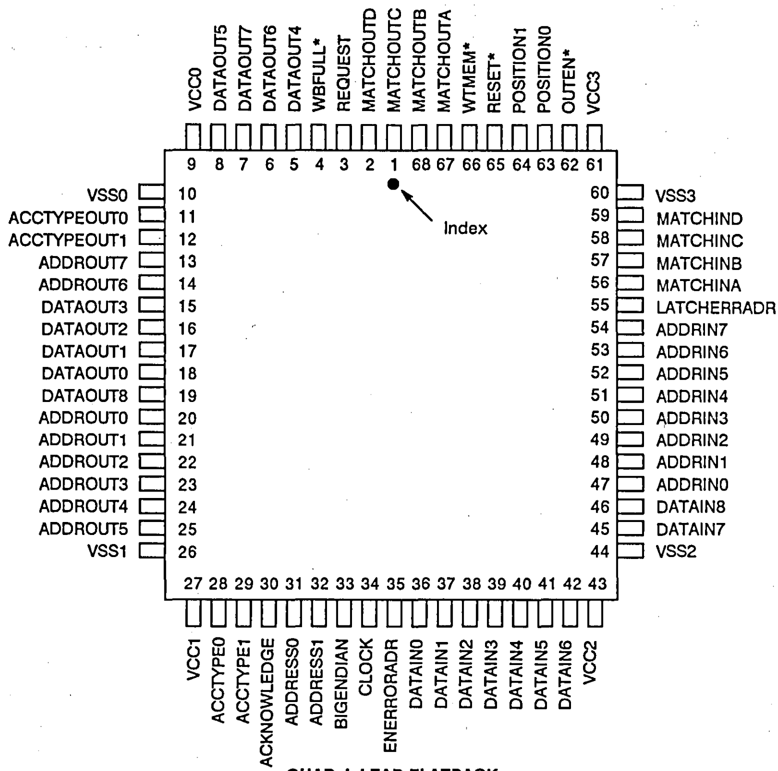


Figure 3. Write Buffer Data and Address Line Connections.

The *Position1* and *Position0* signals shown in Figure 3 specify the nibble position within a halfword that each write buffer device comprises.

PIN CONFIGURATION



QUAD J-LEAD FLATPACK

LOGIC DEVICES

IDT's pioneering in CMOS technology has yielded a family of advanced high-speed CMOS logic products. This technology utilizes the sub 1 micron and double layer metal processing that allows the family to surpass the performance and power requirements of the FAST™, AS and Am29800 families.

This family, designated FCT (Fast CMOS TTL-Compatible), represents the memory and bus interface devices. These devices were designed to allow easy upgrade of existing 54/74F and Am29000 series designs to the CMOS equivalent of the bipolar logic devices. Key features of this family include:

- Direct replacement of FAST™ family of products
- Direct replacement of Am29800 family of products
- Performance upgrades to 35% over FAST™ and Am29800
- Consistent with JEDEC Standard No. 18 for 54/74FCTXXX logic
- Output drive to 64mA (commercial) and 48mA (military)
- Substantially lower input current levels (5µA maximum)
- Excellent ESD and latch-up immunity

All FCT devices are manufactured and assembled on the MIL-STD-883, Class B compliant line. Key features of the military products include:

- Fully compliant to MIL-STD-883, Class B
- Offer numerous devices to DESC drawings
- Available in Radiation Tolerant and Enhanced versions
- Packages include Hermetic DIP, LCC and CERPACK

Using the same fabrication line and stringent quality requirements acquired from manufacturing military products, a completely new line of commercial products are now offered. This has resulted in quality levels significantly higher than previous technologies. All commercial products are available in dual in-line as well as surface mount packages.

Combined with all the features and inherent advantages of low-power supply drain, high input impedance, lower junction temperature and the resultant higher reliability, FCT logic devices are now the preferred logic family for today's designers.

TABLE OF CONTENTS

CONTENTS PAGE

TABLE OF CONTENTS (CON'T.)

CONTENTS **PAGE**

Logic Devices

Integrated Device Technology, Inc.

FAST CMOS OCTAL REGISTERED TRANSCEIVERS

PRELIMINARY
IDT29FCT52A/B
IDT29FCT53A/B
(Replaces 39C52/B and 39C53/B)

FEATURES:

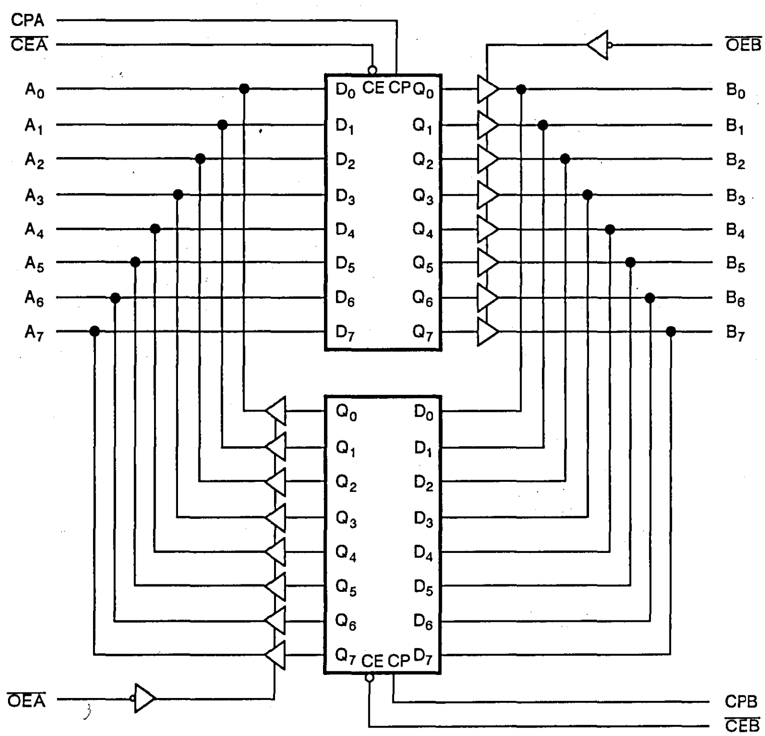
- Equivalent to AMD's Am2952/53 and Fairchild's 29F52/53 in pinout/function
- IDT29FCT52A/53A equivalent to FAST™ speed; **IDT29FCT52B/53B 35% faster than FAST™**
- I_{OL} = 64mA (commercial) and 48mA (military)
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 24-pin DIP, SOIC and 28-pin LCC with JEDEC standard pinout
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT52 and IDT29FCT53 are 8-bit registered transceivers manufactured using advanced CEMOS™, a dual-metal CMOS technology. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.

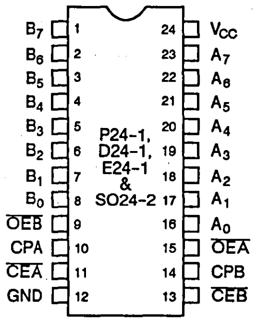
The IDT29FCT52 is an inverting option of the IDT29FCT53.

FUNCTIONAL BLOCK DIAGRAM

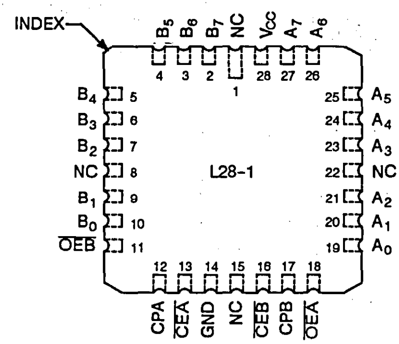


CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Company.

PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
A_{0-7}	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs.
B_{0-7}	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs.
CPA	I	Clock for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	I	Clock Enable for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A Register holds its contents, regardless of CPA signal transitions.
$\overline{OEB}$	I	Output Enable for the A Register. When $\overline{OEB}$ is LOW, the A Register outputs are enabled onto the B_{0-7} lines. When $\overline{OEB}$ is HIGH, the B_{0-7} outputs are in the high impedance state.
CPB	I	Clock for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	I	Clock Enable for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B Register holds its contents, regardless of CPB signal transitions.
$\overline{OEA}$	I	Output Enable for the B Register. When $\overline{OEA}$ is LOW, the B Register outputs are enabled onto the A_{0-7} lines. When $\overline{OEA}$ is HIGH, the A_{0-7} outputs are in the high impedance state.

REGISTER FUNCTION TABLE
(Applies to A or B Register)

INPUTS			INTERNAL	FUNCTION
D	CP	$\overline{CE}$	Q	
X	X	H	NC	Hold Data
L H	↑ ↑	L L	L H	Load Data

OUTPUT CONTROL

$\overline{OE}$	INTERNAL Q	Y-OUTPUTS		FUNCTION
		IDT29FCT52A/B	IDT29FCT53A/B	
H	X	Z	Z	Disable Outputs
L L	L H	L H	H L	Enable Outputs

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER [1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP. [2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V [4]	–	–	5	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V [4]	–	–	-5	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V [4]	–	–	15	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V [4]	–	–	-15	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., [3] V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -15mA MIL.	2.4	4.0	–	
			I_{OH} = -24mA COM'L.	2.4	4.0	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{CC} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ (4) $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current (6)	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_I = -2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ (5) $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8	
			V_{IN} = 3.4V(5) or V_{IN} = GND	–	6.0	16.8	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITIONS(1)	IDT29FCT52A/53A					IDT29FCT52B/53B					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to B_n, A_n		5.5	2.0	10.0	2.0	11.0	4.5	2.0	6.5	2.0	7.2	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n		5.5	1.5	10.5	1.5	13.0	4.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n		5.5	1.5	10.0	1.5	10.0	4.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up time HIGH or LOW A_n, B_n to CPA, CPB	$C_L = 50pF$ $R_L = 500\Omega$	1.0	2.0	–	2.5	–	1.0	2.0	–	2.0	–	ns
t_H	Hold time HIGH or LOW A_n, B_n to CPA, CPB		0.5	2.0	–	2.0	–	0.5	1.5	–	1.5	–	ns
t_{SU}	Set-up time HIGH or LOW. $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		–	2.0	–	2.0	–	–	2.0	–	2.0	–	ns
t_H	Hold time HIGH or LOW. $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		–	2.0	–	2.0	–	–	2.0	–	2.0	–	ns
t_W	Pulse Width, HIGH or LOW CPA or CPB		–	3.0	–	3.0	–	–	3.0	–	3.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDT 29FCTXXX (Device Type) XX (Package) X (Process/Temperature Range)

Process/Temperature Range:
- Blank — Commercial (0°C to +70°C)
- B — Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:
- P — Plastic DIP
- D — CERDIP
- E — CERPACK
- SO — Small Outline IC
- L — Leadless Chip Carrier

Device Type:
- 52A — Non-inverting Octal Registered Transceiver
- 53A — Inverting Octal Registered Transceiver
- 52B — Fast Non-inverting Octal Registered Transceiver
- 53B — Fast Inverting Octal Registered Transceiver

10

Integrated Device Technology, Inc.

MULTILEVEL PIPELINE REGISTERS

IDT29FCT520A/B IDT29FCT521A/B

FEATURES:

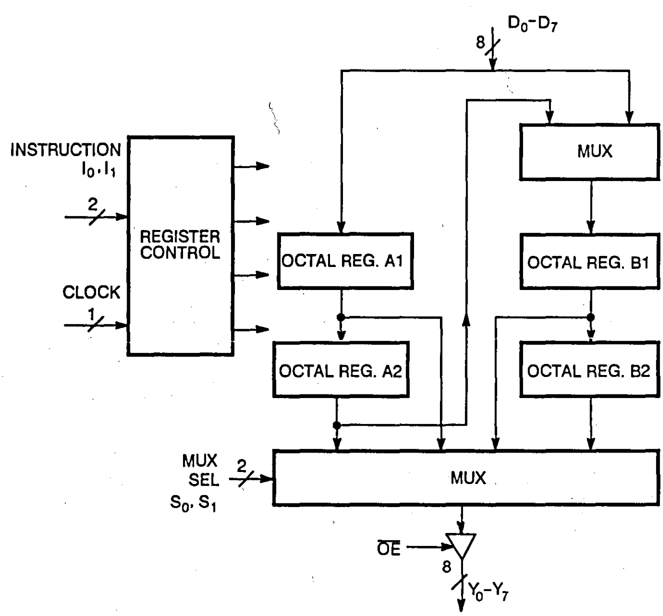
- Equivalent to AMD's Am29520/21 bipolar Multilevel Pipeline Registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- Four 8-bit high-speed registers
- Dual two-level or single four-level push-only stack operation
- All registers available at multiplexed output
- Hold, transfer and load instructions
- Provides temporary address or data storage
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (5µW typ. static)
- Substantially lower input current levels than AMD's bipolar (5µA typ.)
- TTL input and output level compatible
- CMOS output level compatible
- Manufactured using advanced CEMOS™ processing
- Available in 300 mil plastic and hermetic THINDIP, as well as LCC and CERPACK
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT520A/B and IDT29FCT521A/B each contain four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input is provided and any of the four registers is available at the 8-bit, 3-state output.

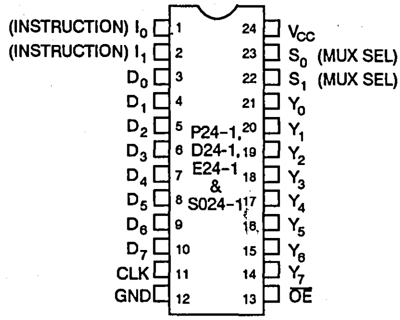
These devices differ only in the way data is loaded into and between the registers in 2-level operation. The difference is illustrated in Figure 1. In the IDT29FCT520A/B when data is entered into the first level (I = 2 or I = 1), the existing data in the first level is moved to the second level. In the IDT29FCT521A/B, these instructions simply cause the data in the first level to be overwritten. Transfer of data to the second level is achieved using the 4-level shift instruction (I = 0). Transfer also causes the first level to change. In either part I = 3 is for hold.

FUNCTIONAL BLOCK DIAGRAM

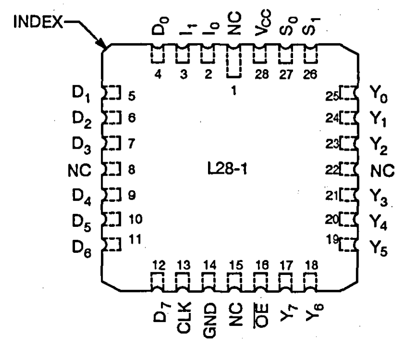


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW

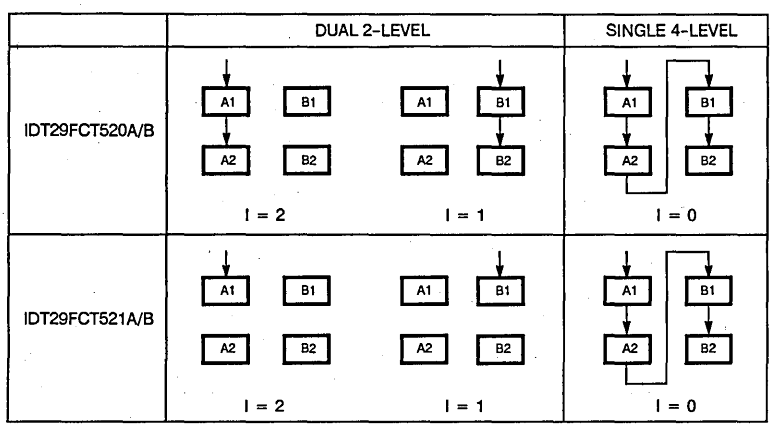


LCC
TOP VIEW

PIN DESCRIPTION

PIN NO.(1)	NAME	I/O	DESCRIPTION
3-10	D_0 - D_7	I	Register input port.
11	CLK	I	Clock input. Enter data into registers on LOW-to-HIGH transitions.
1, 2	I_0, I_1	I	Instruction inputs. See Figure 1 and Instruction Control Tables.
23, 22	S_0, S_1	I	Multiplexer select. Inputs either register A_1, A_2, B_1 or B_2 data to be available at the output port.
13	$\overline{OE}$		Output enable for 3-state output port.
14-21	Y_0 - Y_7	O	Register output port

NOTE:
1. DIP configuration.



NOTE:
1. I=3 for hold.

Figure 1. Data Loading in 2-Level Operation

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A= +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10[4]	
			V_O = 0.5V	–	–	-10[4]	
			V_O = GND	–	–	-10	
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	2.3	5.3	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.8	7.3	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits and Four Controls Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	9.8	17.8[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	13.0	30.8[5]	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITIONS(1)	IDT29FCT520A/21A					IDT29FCT520B/21B					UNIT
				COM'L.		MIL.			COM'L.		MIL.		
			TYP.(3)	MIN.(2)	MAX.	MIN.(2)	MAX.	TYP.(3)	MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PHL}	Clock to Data Output		7.0	–	14.0	–	16.0	–	–	–	–	–	ns
t_{PLH}	S_0, S_1 to Data Output		7.0	–	13.0	–	15.0	–	–	–	–	–	ns
t_{SU}	Set-up Time Input Data to Clock		–	5.0	–	6.0	–	–	–	–	–	–	ns
t_H	Hold Time Input Data to Clock	$R_L = 500\Omega$ $C_L = 50pF$	–	1.0	–	2.0	–	–	–	–	–	–	ns
t_{SU}	Set-up Time Instruction to Clock		–	5.0	–	6.0	–	–	–	–	–	–	ns
t_H	Hold Time Instruction to Clock		–	1.0	–	2.0	–	–	–	–	–	–	ns
t_{PHZ} t_{PLZ}	Output Enable Time		6.0	–	12.0	–	13.0	–	–	–	–	–	ns
t_{PZH} t_{PZL}	Output Disable Time		9.0	–	15.0	–	16.0	–	–	–	–	–	ns
t_W	Clock Pulse Width HIGH or LOW	–	4.0	7.0	–	8.0	–	–	–	–	–	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDT29FCT XXXX (Device Type) A (Package) A (Process/Temperature Range)

Code	Description
Process/Temperature Range	
Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	
P	Plastic DIP
D	CERDIP
L	Leadless Chip Carrier
E	CERPACK
SO	Small Outline IC
Device Type	
520A	Multilevel Pipeline Register
521A	Multilevel Pipeline Register
520B	Fast Multilevel Pipeline Register
521B	Fast Multilevel Pipeline Register

HIGH-PERFORMANCE CMOS BUS INTERFACE

IDT39C8XXX

Integrated Device Technology, Inc.

The part numbering scheme for the IDT39C8XXX family has been changed to conform with the new proposed JEDEC part numbering system. The new system is as follows:

Previous Part Number	New Part Number
IDT39C821	IDT54/74FCT821A
IDT39C822	IDT54/74FCT822A
IDT39C823	IDT54/74FCT823A
IDT39C824	IDT54/74FCT824A
IDT39C825	IDT54/74FCT825A
IDT39C826	IDT54/74FCT826A
IDT39C827	IDT54/74FCT827A
IDT39C828	IDT54/74FCT828A
IDT39C841	IDT54/74FCT841A
IDT39C842	IDT54/74FCT842A
IDT39C843	IDT54/74FCT843A
IDT39C844	IDT54/74FCT844A
IDT39C845	IDT54/74FCT845A
IDT39C846	IDT54/74FCT846A
IDT39C861	IDT54/74FCT861A
IDT39C862	IDT54/74FCT862A
IDT39C863	IDT54/74FCT863A
IDT39C864	IDT54/74FCT864A

Refer to data sheets under the new part number system for all specifications.

HIGH-SPEED 16-BIT BIDIRECTIONAL LATCH

ADVANCE INFORMATION
IDT49FCT601

Integrated Device Technology, Inc.

FEATURES:

- 16-bit bidirectional latch
- Byte swap control to match bus byte ordering
- Independent upper and lower byte output enables
- Independent latch enable controls for both directions
- I_{OL} = 48mA (commercial) and 32mA (military) for back plane drive capability
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 48-pin plastic and sidebraze DIP, 52-pin PLCC and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

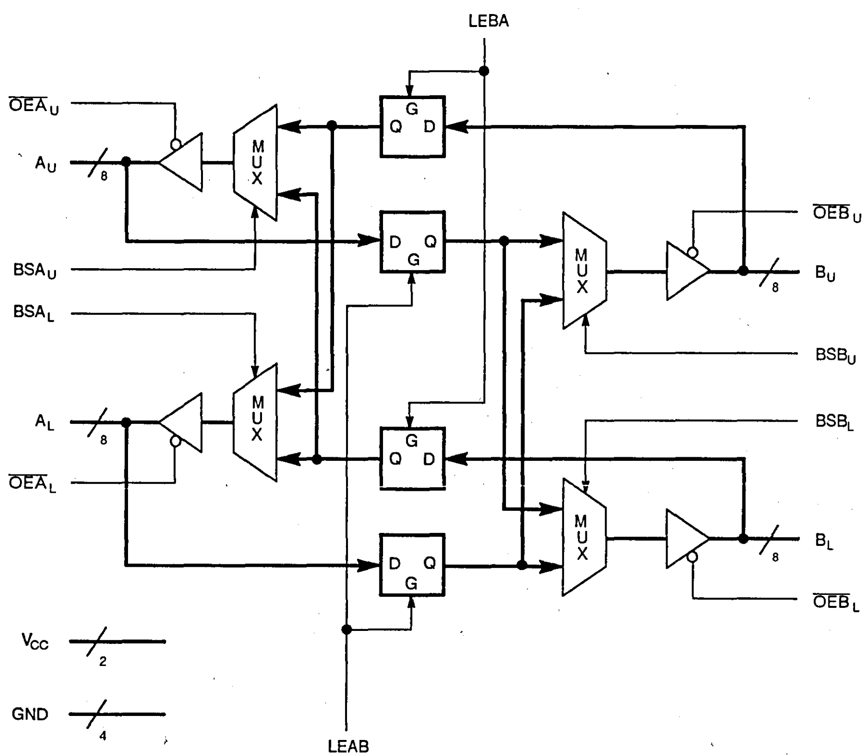
DESCRIPTION:

The IDT49FCT601 is a 16-bit bidirectional latch with byte swap/reordering capability for 16-bit buses. This device can be used in pairs to provide support for 32-bit buses like the VME bus. The byte swap facility allows upper order bytes to be brought down to lower positions for transfer on the bus. The byte swap facility can be used to solve byte ordering conflicts when interfacing Motorola-type devices with Intel-type devices and for resizing data widths.

The high output drive makes this device suitable for driving back plane buses. The four ground pins in the center of the package greatly reduce package inductance and, therefore, ground noise.

This device is manufactured using advanced CEMOS™, a dual metal CMOS technology.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technoloy, Inc.

Integrated Device Technology, Inc.

HIGH SPEED 16-BIT REGISTER WITH SPC™

PRELIMINARY
IDT49FCT618
IDT49FCT618A

FEATURES:

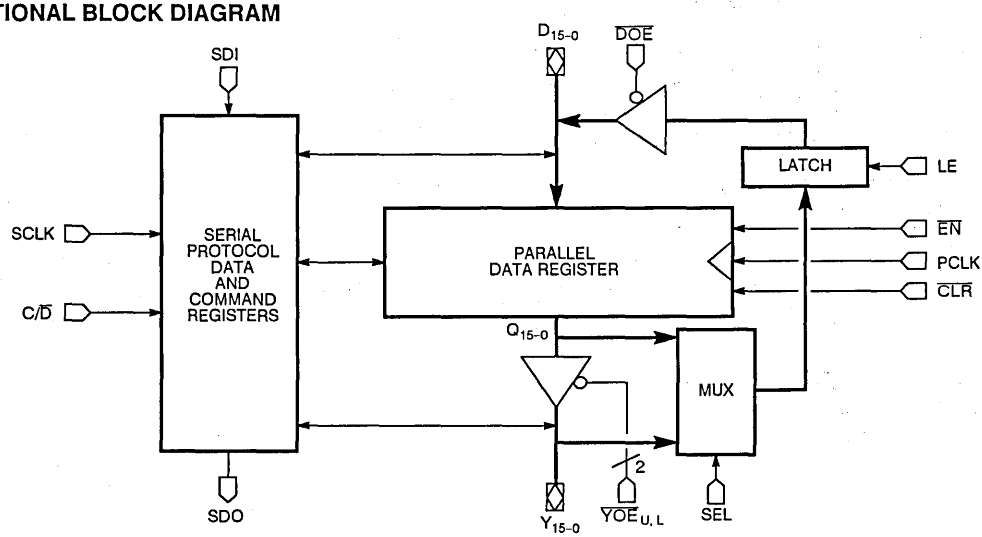
- High-speed non-inverting 16-bit parallel data register for any data path, control path or pipelining application
- Read back path from the data output back to the data input allows for convenient interface to a microprocessor as a parallel high-speed/high-output drive I/O port
- Clock enable and asynchronous clear lines
- High-speed Serial Protocol Channel (SPC™) which provides access to 16 bit parallel data register using four pins
  - Controllability:
    - Serial scan in new machine state
    - Load new machine state "on the fly" synchronous with PCLK
    - Temporarily force Y output bus
    - Temporarily force data out the D input bus (as in loading WCS)
  - Observability:
    - Directly observe D and Y buses
    - Serial scan out current machine state
    - Capture machine state "on the fly" synchronous with PCLK
- I_{OL} = 32mA (commercial), 24mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 48-pin DIP and 52-pin LCC/PLCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

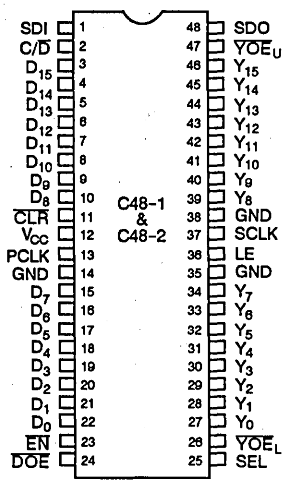
The IDT49FCT618/A are high-speed, general purpose 16-bit parallel data registers with a Serial Protocol Channel (SPC). The D-to-Y path of the register provides a data path that is designed for normal system operation wherever a high-speed clocked register is required. This device also incorporates a latched read back path from the Y bus to the D bus. The SPC is used to communicate with SPC command and data registers.

The SPC command and data registers are used to observe and control the operation of the 16-bit parallel data register for diagnostic purposes. The SPC command and data registers can be accessed while the system is performing normal system function. Diagnostic operations then can be performed "on the fly", synchronous with the system clock, or can be performed in the "single step" environment. The SPC port utilizes serial data in and out pins (a concept originated at IBM) which can participate in a serial scan loop throughout the system where normal data, address, status and control registers are replaced with the IDT49FCT618/A. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then, after a specified number of clock cycles, the data can be clocked out and compared with expected results. An "oscilloscope mode" can be achieved by loading data from the SPC data register into the parallel data register synchronous to the system clock (PCLK) using an SPC command which transfers data synchronously. When repeated every Nth clock, the repeating states of the system can be observed on an oscilloscope. When used as a pipeline register, Writable Control Store (WCS) loading can be accomplished by scanning in data through the SPC port and enabling the data onto the D bus pins.

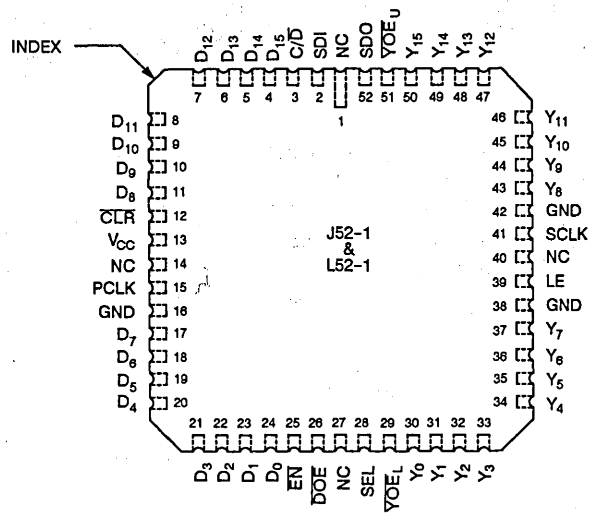
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
PCLK	I	Parallel Data Register Clock
$\overline{EN}$	I	Clock Enable for PCLK (enabled when low)
$\overline{CLR}$	I	Asynchronous 16-Bit Clear (active low)
D_{15-0}	I/O	Parallel Data Register Input Pins (D_0 = LSB, D_{15} = MSB)
Y_{15-0}	I/O	Parallel Data Register Output Pins (Y_0 = LSB, Y_{15} = MSB)
$\overline{YOE}_{U,L}$	I	Output Enables for Y Bus (Overidden by SPC Inst. 8 and 14)
SEL	I	Selects Between Parallel Data Register Q or Y Bus for Read Back Data
LE	I	Controls a Latch in the Read Back Path (transparent when High)
$\overline{DOE}$	I	Output Enable for D Bus (Overidden by SPC Inst. 9)
SDI	I	Serial Data In for SPC operation
SDO	O	Serial Data Out for SPC operation
C/$\overline{D}$	I	Mode Control for SPC
SCLK	I	Shift clock for SPC operations

TRUTH TABLE (1)

C/$\overline{D}$	SCLK	PCLK	$\overline{EN}$	$\overline{CLR}$	$\overline{DOE}$	SEL	LE	$\overline{YOE}_{U,L}$	D	Y	FUNCTION
X	X	X	X	X	X	X	X	H	X	High Z	Tri-State Y
X	X	X	X	L	X	X	X	H	X	L	Clear Parallel Data Register
X	X	↑	H	H	X	X	X	L	X	NC	Hold Parallel Data Register
X	X	↑	L	H	X	X	X	L	Input	D	Clock D-to-Y
X	X	X	X	H	L	H	H	H	Q	X	Read Back Parallel Data Register
X	X	X	X	H	L	L	H	H	Y	Input	Read Back Y Data Bus
H	↑	X	X	X	X	X	X	X	X	X	Shift Bit into SPC Command Register
L	↑	X	X	X	X	X	X	X	X	X	Shift Bit into SPC Data Register
↓	↑	H or L (Static)	X	X	X	X	X	X	X	X	Execute SPC Command During Time Between C/$\overline{D}$ & SCLK
X	X	X	X	X	L	X	L	X	X	X	Read data stored in feedback latch

NOTE:
H = HIGH Voltage Level, L= LOW Voltage Level, X= Don't Care, Z= High Impedance, ↑/↓ = Low-to-High/High-to-Low Transition

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15(4)	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 24mA MIL.	–	0.3	0.5	
			I_{OL} = 32mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clocks Only	–		–	200	–	mV

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{YOE}_{U,L}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{YOE}_{U,L}$ = GND One Bit Toggling at f_I = 5MHz 50% Duty Cycle SEL, $\overline{DOE}$, $\overline{CLR}$, LE, SDI, C/$\overline{D}$, SCLK = V_{CC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{YOE}_{U,L}$ = GND Sixteen Bits Toggling at f_I = 2.5MHz 50% Duty Cycle SEL, $\overline{DOE}$, $\overline{CLR}$, LE, SDI, C/$\overline{D}$, SCLK = V_{CC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	6.8	12.8[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	11.0	29.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL		PARAMETER	CONDITION[1]	IDT49FCT618				IDT49FCT618A				UNIT
				COM'L.		MIL.		COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	
	T1	PCLK ↑ to Y		3.0	12.5	3.0	14.0					
	T2	SCLK ↑ to SDO		3.0	12.5	3.0	14.0					
	T3	SDI to SDO (in stub mode)		3.0	12.5	3.0	14.0					
	T4	C/$\overline{D}$ ↓ to Y ($\overline{YOE}_{U,L}$ = Low Inst. 8 & 14)		3.0	12.5	3.0	14.0					ns
t_{PLH} t_{PHL}	T5	SCLK ↑ to Y ($\overline{YOE}_{U,L}$ = High, Inst. 8)		3.0	12.5	3.0	14.0					
	T6	C/$\overline{D}$ to SDO (Inst. 0,1,2,4)		2.0	12.5	3.0	14.0					
	T7	LE to D		2.0	12.5	3.0	14.0					
	T8	Y to D		2.0	12.5	3.0	14.0					
	T9	SEL or $\overline{CLR}$ to Y		2.0	12.5	3.0	14.0					
	T10	SEL to D		2.0	12.5	3.0	14.0					ns
	S1	D to PCLK ↑		2.5	–	3.0	–					
	S2	C/$\overline{D}$ to SCLK ↑		12.0	–	14.0	–					
	S3	SDI to SCLK ↑		4.0	–	5.0	–					
	S4	Y or D to C/$\overline{D}$ (Inst. 0, 2 & 4)		2.0	–	2.5	–					
t_{SU}	S5	C/$\overline{D}$ (Low) to PCLK ↑ (Inst. 3 & 13)	C_L = 50pF R_L = 500Ω	8.0	–	9.0	–					
	S6	Y to PCLK ↑ (Inst. 3)		2.0	–	2.5	–					
	S7	Y to LE		3.0	–	4.0	–					ns
	S8	SEL to LE		3.0	–	4.0	–					
	S9	$\overline{EN}$ to PCLK		3.0	–	4.0	–					
	S10	PCLK ↑ to LE (Low)		3.0	–	4.0	–					
	H1	D to PCLK ↑		2.0	–	2.5	–					
	H2	C/$\overline{D}$ to SCLK ↑		12.0	–	14.0	–					
	H3	SDI to SCLK ↑		1.0	–	1.0	–					
	H4	Y or D to C/$\overline{D}$ ↓ (Inst. 0, 2 & 4)		2.0	–	2.5	–					
t_H	H5	SCLK (Low) to PCLK ↑ (Inst. 3 & 13)		2.0	–	2.5	–					ns
	H6	C/$\overline{D}$ (Low) to PCLK ↑ (Inst. 3 & 13)		2.0	–	2.5	–					
	H7	Y to PCLK ↑ (Inst. 3)		3.0	–	3.0	–					
	H8	Y to LE		2.0	–	2.0	–					
	H9	SEL to LE		2.0	–	2.0	–					
	H10	$\overline{EN}$ to PCLK ↑		2.0	–	2.0	–					

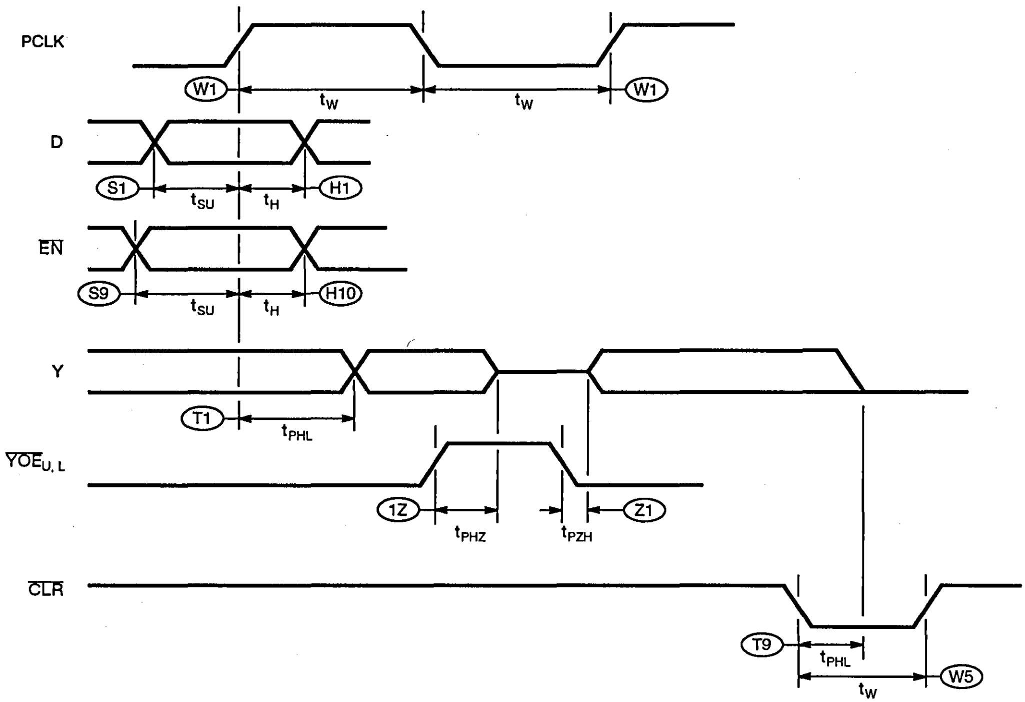
(Continued)

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

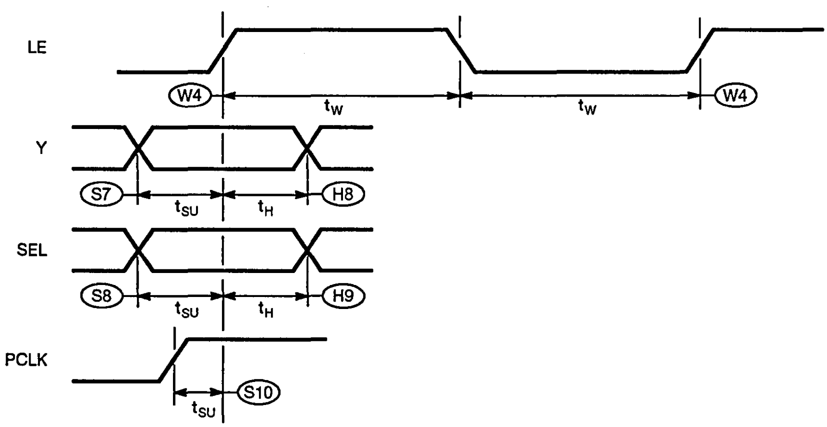
SYMBOL		PARAMETER	CONDITION[1]	IDT49FCT618				IDT49FCT618A				UNIT
				COM'L.		MIL.		COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PHZ} t_{PLZ}	1Z	$\overline{YOE}_{U,L}$ to Y	C_L = 50pF R_L = 500Ω	3.0	8.0	3.0	8.0					ns
	2Z	SCLK $\uparrow$ to D (Inst. 9)		3.0	9.0	3.0	9.0					
	3Z	C/$\overline{D}$ $\uparrow$ to D or Y (Inst. 9)		3.0	9.0	3.0	9.0					
	4Z	SCLK $\uparrow$ to Y ($\overline{YOE}_{U,L}$ = High Inst. 8 & 14)		3.0	9.0	3.0	9.0					
	5Z	C/$\overline{D}$ to $\uparrow$ to D or Y ($\overline{YOE}_{U,L}$ = High Inst. 14)		3.0	9.0	3.0	9.0					
	6Z	$\overline{DOE}$ to D		2.0	9.0	3.0	10.0					ns
t_{PZH} t_{PZL}	Z1	$\overline{YOE}_{U,L}$ to Y		3.0	10.0	3.0	10.0					
	Z2	C/$\overline{D}$ $\downarrow$ to D (Inst. 9)		3.0	10.0	3.0	10.0					
	Z3	C/$\overline{D}$ $\downarrow$ to Y ($\overline{YOE}_{U,L}$ = High Inst. 14)		3.0	10.0	3.0	10.0					
	Z4	$\overline{DOE}$ to D		2.0	9.0	3.0	10.0					
t_W	W1	PCLK (High & Low)		7.0	–	8.0	–					
	W2	SCLK (High & Low)		25.0	–	25.0	–					
	W3	C/$\overline{D}$ (High)		25.0	–	25.0	–					
	W4	LE (High-Low)		7.0	–	8.0	–					
	W5	$\overline{CLR}$ (Low)		7.0	–	8.0	–					

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

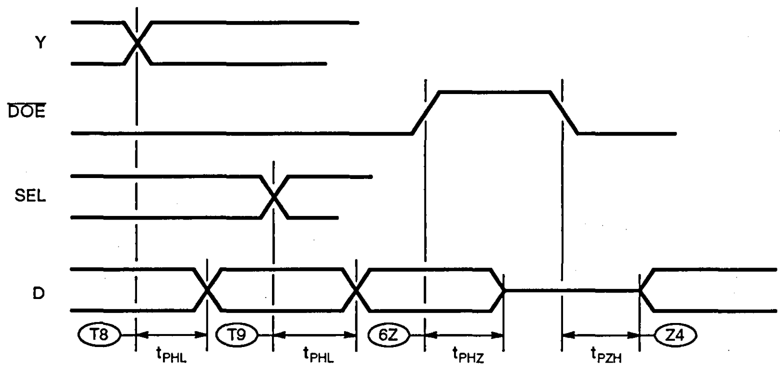
GENERAL WAVEFORMS FOR PARALLEL INPUTS AND OUTPUTS



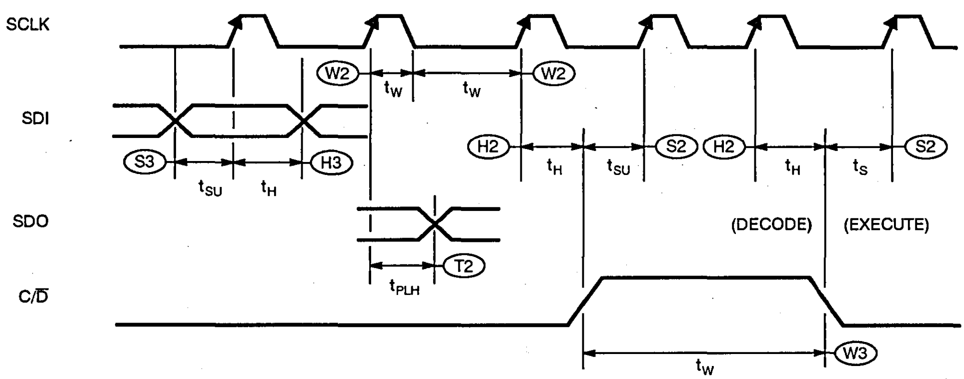
READ BACK LATCH SETUP & HOLD ITEMS



READ BACK PROPOGATION DELAYS



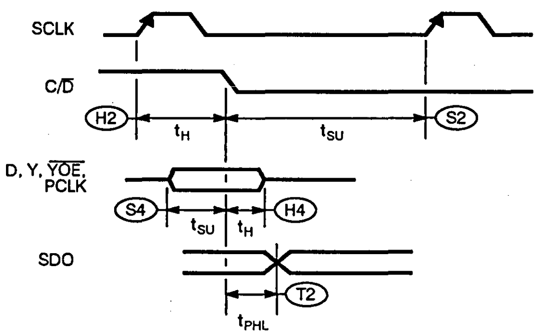
GENERAL WAVEFORMS FOR SERIAL PROTOCOL INPUTS AND OUTPUTS



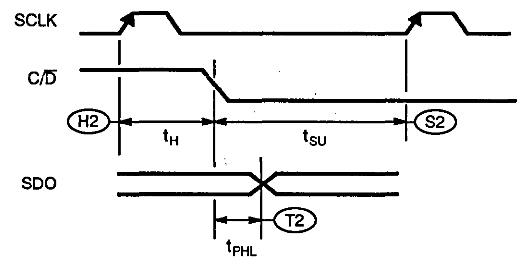
10

DETAILED WAVEFORMS OF SERIAL PROTOCOL OPERATIONS

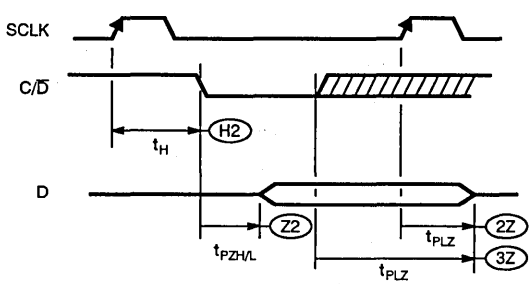
Y ⟶ SPC Data (Inst. 0)
D ⟶ SPC Data (Inst. 2)
STATUS ⟶ SPC Data (Inst. 4)



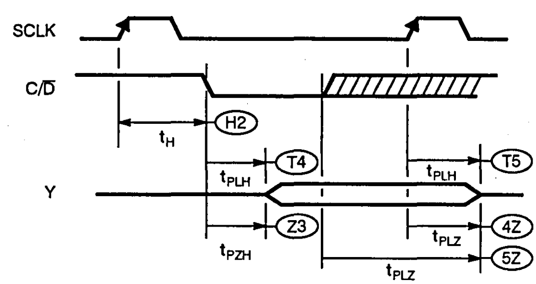
PARALLEL DATA REGISTER ⟶ SPC Data (Inst. 1)
SET SERIAL MODE (Inst. 11)
SET STUB MODE (Inst.12)



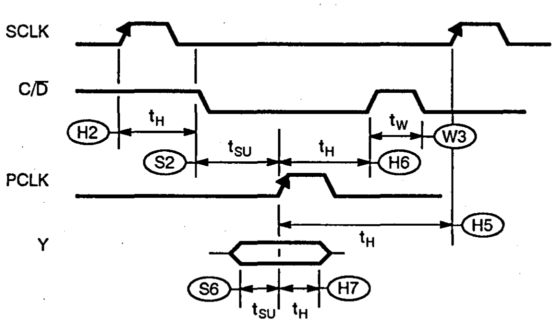
SPC Data ⟶ D (Inst. 9)



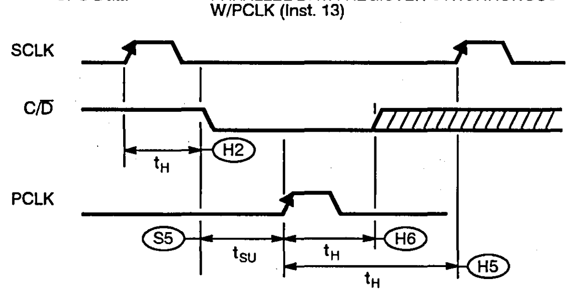
SPC Data ⟶ PARALLEL DATA REGISTER (Inst. 10)
SPC Data ⟶ Y (Inst. 8)
CONNECT D TO Y (Inst. 14)



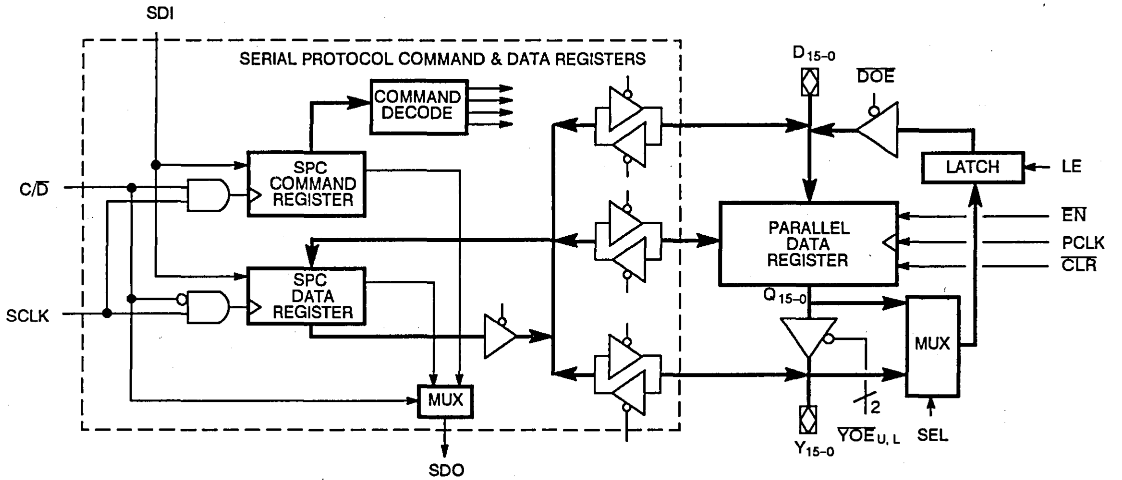
Y ⟶ SPC Data SYNCHRONOUS W/PCLK (INST.3)



SPC Data ⟶ PARALLEL DATA REGISTER SYNCHRONOUS W/PCLK (Inst. 13)



DETAILED FUNCTIONAL BLOCK DIAGRAM



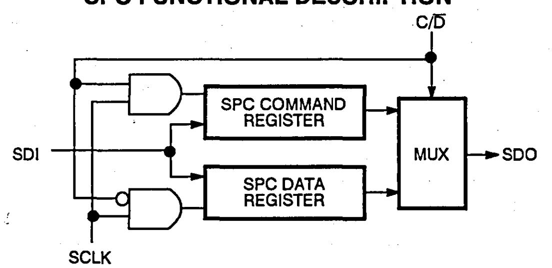
The block diagram consists of three main data paths and two logic blocks. The main data path is from the D inputs down to the parallel data register and through the Y outputs. This is the path that will be used most of the time in normal operation. For serial protocol operations, there are data paths from the Y pins into the SPC data register and control block. Coming out of this block is the data path that allows data to be put back onto the D input pins or into the parallel data register. The PCLK is used to clock the parallel data register. The $\overline{EN}$ signal is a clock enable for the 16-bit parallel data path. The $\overline{CLR}$ line offers an asynchronous 16-bit clear. $\overline{YOE}_{U,L}$ inputs are used to control the tri-state output of the Y pins.

The other main data path is a read back from the output of the 16-bit parallel data register to the D bus. This path is convenient when using the IDT49FCT618 with a processor because it provides the mechanism to read the contents of the data register. The SEL pin selects data from the internal Q bus or the data output pins Y. The LE signal controls a latch in the read back path. In this way data can be latched "on the fly" and allowed to settle before a processor reads it back on the D pins. The $\overline{DOE}$ input is a tri-state control which selects whether the D bus is an input or an output.

SPC data and commands are shifted through the SDI pin which is a serial input pin and the SDO pin which is a serial output pin. Data and commands are shifted in Least Significant Bit first, Most Significant Bit last (Y_0 = LSB, Y_{15} = MSB). The SCLK is used to shift the data through. The C/$\overline{D}$ line is used as a control input to determine whether data or command information is being shifted in.

The Serial Protocol Channel (SPC) has been optimized for the minimum number of pins and maximum flexibility. The data is passed in on a serial data input pin (SDI) and out on a serial data output pin (SDO). The transfer of the data is controlled by a serial clock (SCLK) and a command/data mode input (C/$\overline{D}$). These four pins are the basic SPC pins. To the outside, the SPC appears as two serial shift registers in parallel; one for command and the other data. The serial clock shifts data and the command/data (C/$\overline{D}$) line selects which register is being shifted. The SPC command register is used to control loading of data to and from the parallel data register with other storage elements in the device.

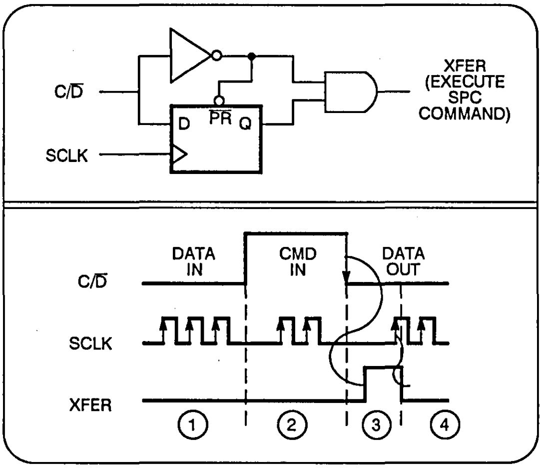
SPC FUNCTIONAL DESCRIPTION



With respect to executing an SPC command, there are four distinct phases: (1) data is shifted in, (2) followed by the SPC command, (3) the SPC command is executed, (4) data is shifted out. During the data mode, data is simultaneously shifted into the SPC data register while the data in the register is shifted out. During the command mode, opcode type information is shifted through the serial ports.

The command is executed when the last bit is shifted in and the C/$\overline{D}$ line is brought low. The execution phase is ended with the next serial clock edge. Execution of SPC commands is performed by stopping the SPC clock, SCLK, and lowering the C/$\overline{D}$ line from high-to-low. Later the SCLK may be transitioned from low-to-high. SPC commands and data can be shifted any time without regard for operation. During the execution phase, care must be taken that there is no conflict between the SPC operation and parallel operation. This means that if the SPC operation attempts to load the parallel data register (opcode 10) while PCLK is in transition, the results are undefined. In general, it is required that the PCLK be static during SPC operations. The synchronous commands (opcodes 3 and 13), however, allow the PCLK to run. In these operations the HIGH-to-LOW transition of the C/$\overline{D}$ line takes on the function of an arm signal in preparation for the next LOW-to-HIGH transition of the PCLK.

10



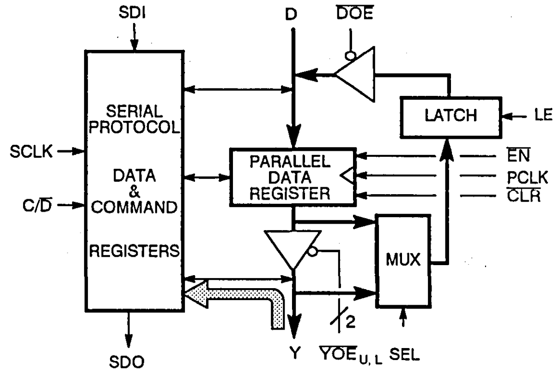
SPC COMMANDS

There are 16 possible SPC opcodes. Thirteen of these are utilized; the other three are reserved and perform NO-OP functions. The top eight opcodes, 0 through 7, are used for transferring data into the SPC data register for shifting out. The lower eight opcodes, 8 through 15, are used for transferring data from the SPC data register to other parts of the device. Two of the commands are also used for connecting the data in and out pins.

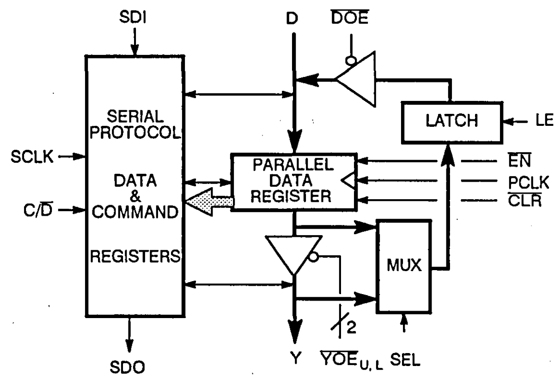
OPCODE	SPC COMMAND
0	Y to SPC Data Register
1	Parallel Data Register to SPC Data Register
2	D to SPC Data Register
3	Y to SPC Data Register Synchronous w/PCLK
4	Status ($\overline{YOE}_{U,L}$, PCLK, etc) to SPC Data Register
5-7	Reserved (NO-OP)
8	SPC Data to Y ($\overline{YOE}_{U,L}$ is overidden)
9	SPC Data to D ($\overline{DOE}$ is overidden)
10	SPC Data to Parallel Data Register
11	Select Serial Mode
12	Select Stub Mode
13	SPC Data to Y Synchronous w/PCLK
14	Connect D to Y ($\overline{YOE}_{U,L}$ is overidden)
15	NO-OP

Opcode 0 is used for transferring data from the Y output pins into the SPC data register. Opcode 1 transfers data from the output of the parallel data register into the SPC data register.

Y → SPC Data (Inst. 0)

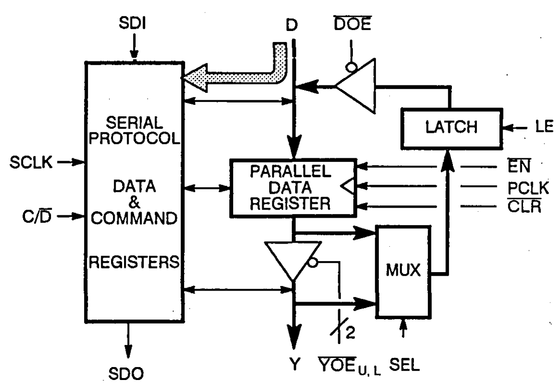


PARALLEL DATA REG → SPC Data (Inst. 1)



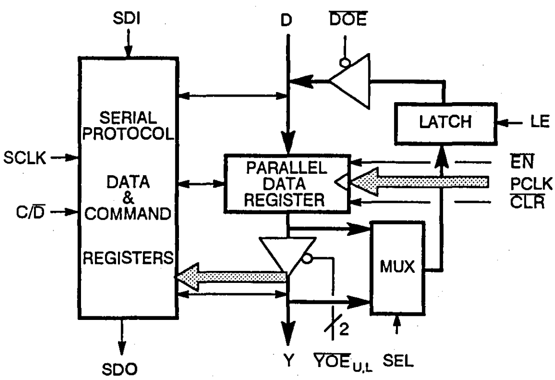
Opcode 2 transfers data which is on data input pin D into the SPC data register.

D → SPC Data (Inst. 2)



Opcode 3 transfers data on the Y pins to the SPC data register on the next PCLK, thus achieving a synchronous observation of the parallel data register in real time. This operation can be forced to repeat without shifting in a new command by pulsing C/$\overline{D}$ LOW-HIGH-LOW after each PCLK. As soon as data is shifted out using SCLK, the command is terminated and must be loaded in again.

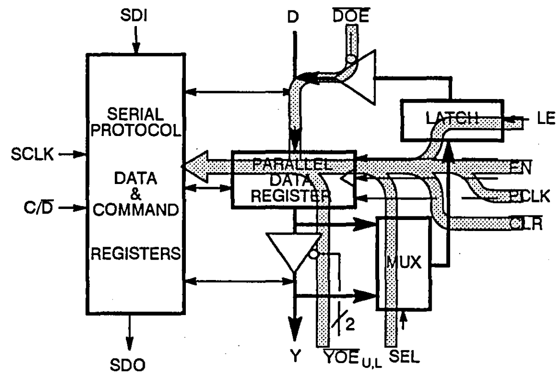
Y ⟶ SPC Data SYNCHRONOUS w/PCLK (Inst. 3)



Opcode 4 is used for loading status into the SPC data register. The format of bits is shown below.

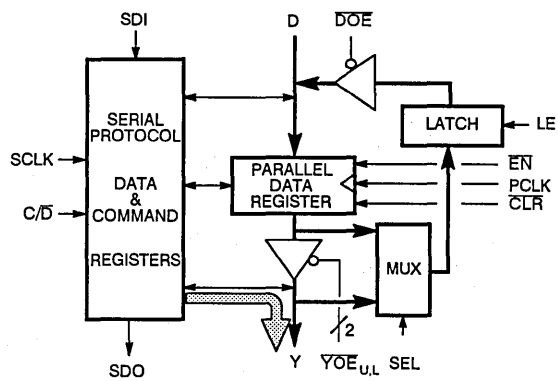
15	14	13	12	11	10	9	8	7	6 0
$\overline{DOE}$	PLCK	$\overline{YOE}_U$	LE	$\overline{EN}$	$\overline{CLR}$	$\overline{YOE}_L$		SEL	

STATUS ⟶ SPC Data (Inst. 4)



Opcodes 5 through 7 are reserved, hence designated NO-OP.

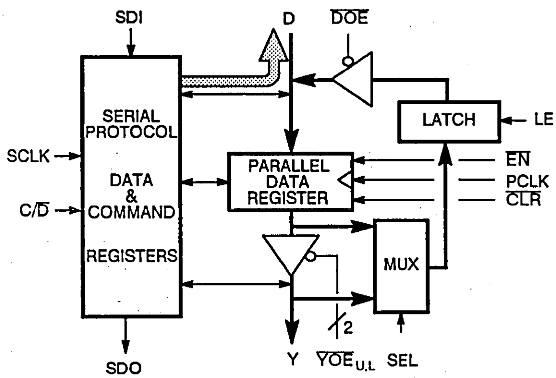
SPC Data ⟶ Y (Inst. 8)



Opcode 8 is used for transferring data directly to the Y pins. When executing opcode 8, the state of $\overline{YOE}_{U,L}$ is a don't care and data will be output even if $\overline{YOE}_{U,L}$= HIGH. Opcode 9 is used for transferring SPC data to the D pins. Operations 8 and 9 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$. As soon as SCLK completes transition, the command is terminated.

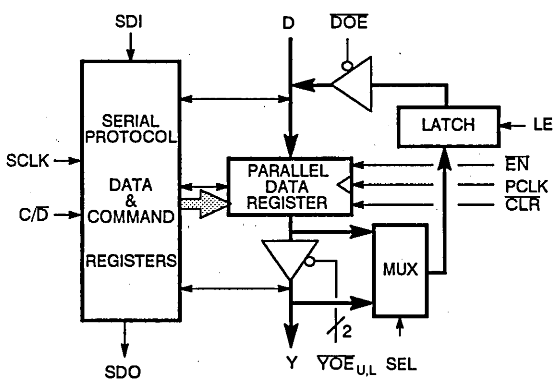
10

SPC Data ⟶ D (Inst. 9)



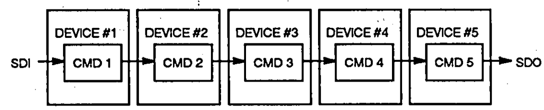
Opcode 10 is used for transferring data from the SPC Data register into the parallel data register, irrespective of the state of PCLK. However, PCLK must be static between C/D̄ going HIGH-to-LOW and SCLK going LOW-to-HIGH.

SPC Data ⟶ PARALLEL DATA REGISTER (Inst. 10)



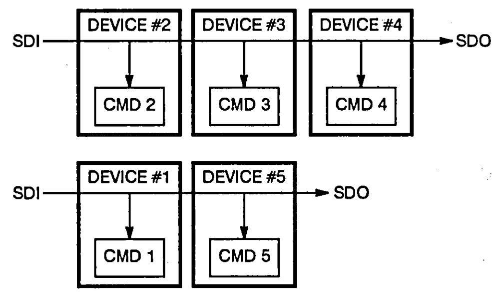
Opcodes 11 and 12 are used to set Serial and Stub mode, respectively. After executing one of these opcodes, the device remains in this mode through other Serial Protocol operations until reprogrammed using either command. The serial mode is the default mode that the IDT49FCT618 powers up in. In Serial mode, commands are shifted through the command register and then to the SDO pin. This is the typical mode used when several varieties of devices that utilize the SPC access method are employed on one serial ring.

SERIAL MODE



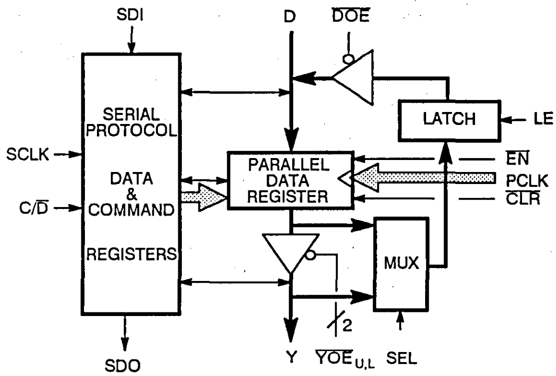
In Stub mode, SDI is connected directly to SDO. The serial input of the command register is connected to SDI. In this way, the same SPC command can be loaded into multiple devices of like type. For example, in four clock cycles the same command could be loaded into 8 IDT49FCT618s (128-bit pipeline register). Dissimilar devices must be segregated into serial scan loops of similar type as shown below (i.e., other devices from IDT that incorporate SPC). During the command phase, the serial shift clock must be slowed down to accommodate the delay from SDI to SDO through all of the devices. The slower clock is typically a small tradeoff compared to the reduced number of clock cycles.

STUB MODE

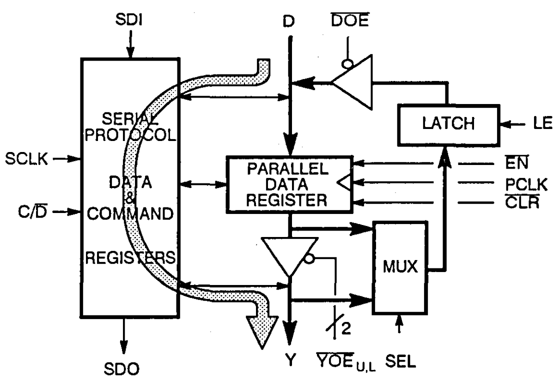


Opcode 13 transfers data from the SPC data register to the pipeline register on the next PCLK. Opcode 14 connects the D bus to the Y bus. Operation 14 can be temporarily suspended by raising the C/D̄ input and resumed by lowering the C/D̄ input again. The operation is terminated by SCLK.

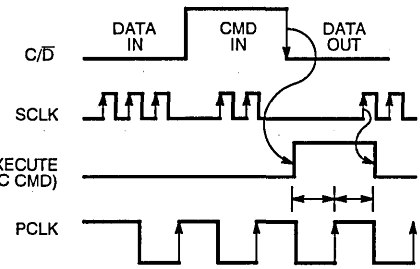
SPC Data → PARALLEL DATA REGISTER SYNCHRONOUS w/PCLK (Inst. 13)



CONNECT D TO Y (Inst. 14)



Opcodes 3 and 13 transfer data synchronous to the PCLK which means that the High-to-Low on the C/$\overline{\text{D}}$ input is an arm signal. The data and command can be shifted in while the PCLK is running. The C/$\overline{\text{D}}$ line is dropped prior to the desired PCLK edge and raised afterwards, before the next edge. Instruction 13 can be repeated many times by leaving the C/$\overline{\text{D}}$ line low during multiple transitions of the PCLK while not clocking SCLK. PCLK cycles can even be skipped by raising the C/$\overline{\text{D}}$ input during the desired clock periods. Instruction 3 can be repeated by pulsing the C/$\overline{\text{D}}$ high after each PCLK.



The ability to repeatedly execute a synchronous command can provide major benefits. For example, the synchronous read (Instruction 3, Y to SPC data) instruction could be clocked into the serial command register. Then, it could be continuously executed by pulsing the C/$\overline{\text{D}}$ line HIGH. When the whole system is stopped (PCLK quiescent), the serial data register will contain the next to the last state of the parallel data register. That value can be shifted out and the current state of the parallel data register can then be observed, allowing for the observation of two states of the parallel data register (the current and the previous).

10

TYPICAL APPLICATION

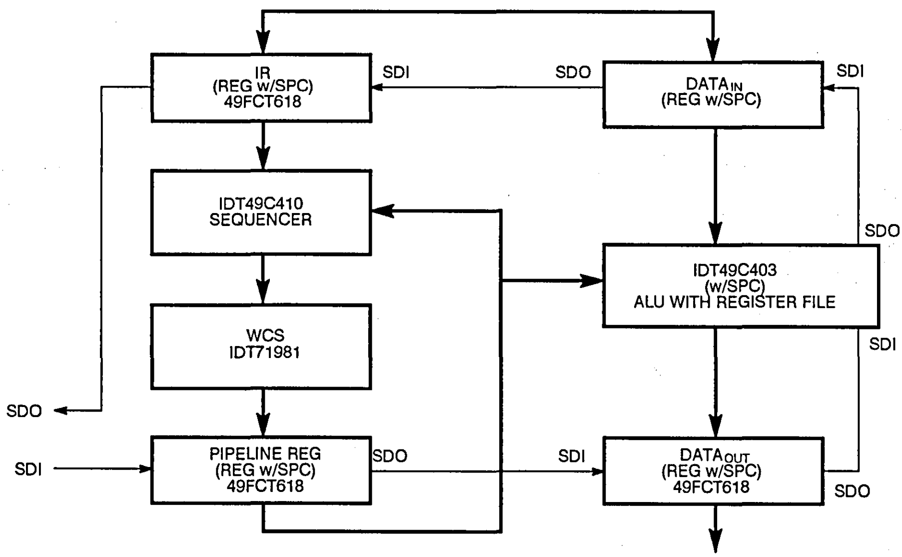
In the block diagram of the typical application, the register with SPC register is shown being used with a writable control store in a microprogrammed design. The control store can be initialized through the diagnostics path. The SPC data register with SPC is used for the instruction register going into the IDT49C410, as well as parallel data registers around the IDT49C403. In this way, the designer may use the SPC register to observe and modify the microcode coming out of the writable control store, as well as observing and being able to modify data and instructions in the overall machine. The IDT49C403 is a 16-bit version of the 2903A/203 which includes an SPC port for diagnostic and break point purposes.

The block diagram of the diagnostic ring shows how the devices with SPC Data are hooked together in a serial ring via the SDI and SDO signals. The SPC signals may be generated through registers which are hooked up to a microprocessor. This microprocessor could conceivably be an IBM PC.

As companies like IDT continue to integrate more onto each device and put each device into smaller packages such as surface mount devices, the board level testing becomes more complex for the designer and the manufacturing divisions of companies. To help this situation, SPC was invented. This allows for observation of critical signals deep within the system. During system test when an error is observed, these signals may be modified in order to zero in on the fault in the system.

SPC is primarily a scheme utilizing only a few pins (4) to examine and alter the internal state of a system for the purpose of monitoring and diagnosing system faults. It can be used at many points in the life of a product: design debug and verification, manufacturing test and field service. This document describes a serial diagnostic scheme which was developed at IDT and will be used in future VLSI logic devices designed by IDT.

TYPICAL MICROPROGRAM APPLICATION WITH SPC™



ORDERING INFORMATION

IDT XXXX (Device Type) X (Package) X (Process/Temperature Range)

Process/Temperature Range:
- Blank — Commercial (0°C to +70°C)
- B — Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:
- XC — Sidebraze Shrink-DIP
- C — Sidebraze DIP
- J — Plastic Leaded Chip Carrier
- L — Leadless Chip Carrier

Device Type:
- 49FCT618 — 16-Bit Register with SPC™
- 49FCT618A — High-Speed 16-Bit Register with SPC™

Integrated Device Technology, Inc.

HIGH SPEED 16-BIT SYNCHRONOUS BINARY COUNTER

ADVANCE INFORMATION
IDT49FCT661

FEATURES:

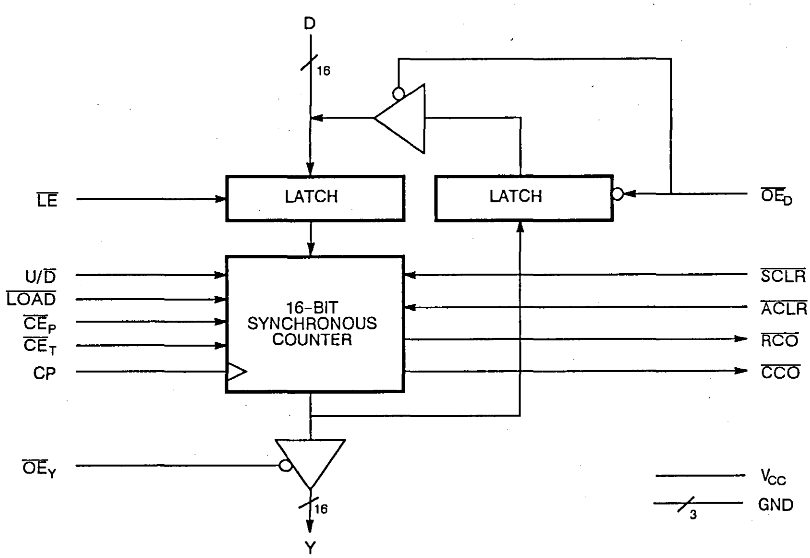
- 16-bit synchronous up/down counter, synchronously programmable
- Maximum frequency of 50MHz commercial
- Clock to Y-bus of 15ns commercial
- Both synchronous and asynchronous clear inputs
- Three-state counter outputs interface directly with bus-organized systems
- Ripple carry output for cascading
- Clocked carry output for convenient modulo configuration
- Latched inputs provide for modulo load function or interface to a processor
- Latched readback path for interface to a processor
- I_{OL} = 48mA commercial and 32mA military
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 48-pin Shrink-DIP, 52-pin PLCC and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49FCT661 is a programmable 16-bit synchronous up/down binary counter which is conveniently organized for operation in a standalone configuration, as well as interfaced with a processor. All operations except latch, output enable and asynchronous clear happen on the rising edge of the Clock Input (CP).

With a $\overline{LOAD}$ input LOW, the counter will load the value at the output of the input latch. The input latch is transparent when $\overline{LE}$ is LOW, allowing for easy connection to processor address decode and strobe logic. The D-Bus Output Enable, ($\overline{OE}_D$) is used for reading back the state of the counter in processor-based applications. When $\overline{OE}_D$ is LOW, the latch is closed and the D bus is driven with the contents of the latch; otherwise the output buffer is in a high-impedance state when $\overline{OE}_D$ is HIGH. Counting is enabled only when $\overline{CE}_P$ and $\overline{CE}_T$ are LOW and $\overline{LOAD}$ is HIGH. The Up/Down Input, (U/$\overline{D}$), controls direction of the count. Internal carry look-ahead logic and an active LOW on Ripple Carry Output ($\overline{RCO}$) allow for counting and cascading. During up-count, the $\overline{RCO}$ is LOW at binary 65K and upon down-count is LOW at binary 0. Normal cascade operations require only the $\overline{RCO}$ to be connected to the succeeding block at $\overline{CE}_T$. When counting, the Clock Carry Output ($\overline{CCO}$) provides a HIGH-LOW-HIGH pulse for a duration equal to the clock LOW time of the input clock only when $\overline{RCO}$ is LOW. Two active LOW resets are available: synchronous clear ($\overline{SCLR}$) and Master Asynchronous Clear ($\overline{ACLR}$). The output control ($\overline{OE}_Y$) input forces the output to high impedance when LOW, otherwise the Y-bus reflects the output of the counter.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

10

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-4001/-

Integrated Device Technology, Inc.

HIGH-SPEED OCTAL REGISTER WITH SPC™

PRELIMINARY
IDT49FCT818A
IDT49FCT818B

FEATURES:

- High-speed, non-inverting 8-bit parallel register for any data path, control path or pipelining application
- New, unique command capability which allows for multiplicity of diagnostic functions
- High-speed Serial Protocol Channel (SPC™) provides
  - Controllability:
    - Serial scan in new machine state
    - Load new machine state "on the fly"
    - Temporarily force Y output bus
    - Temporarily force data out the D input bus (as in loading WCS)
  - Observability:
    - Direct observe D and Y buses
    - Serial scan out current machine state
    - Capture machine state "on the fly"
- I_{OL} = 32mA (commercial) and 24mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than 29818 and 54/74AS818 (5μA max.)
- Available in plastic and sidebraze DIP, PLCC and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

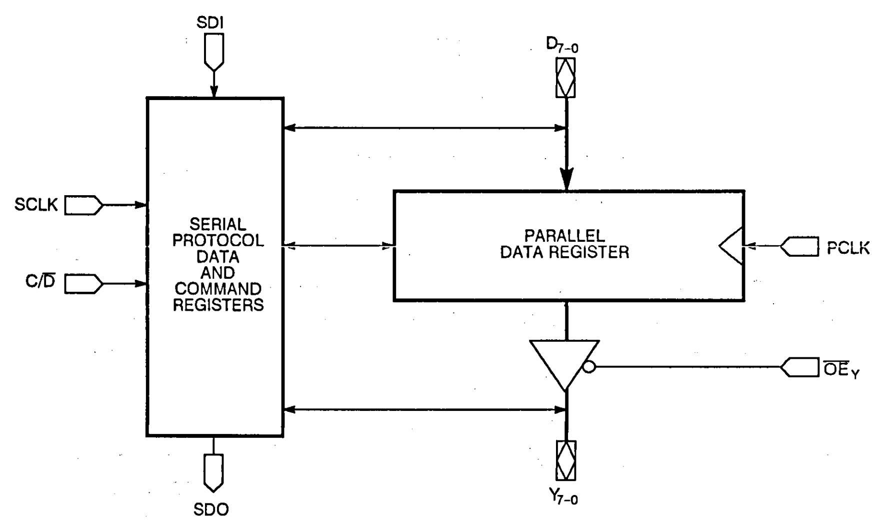
DESCRIPTION:

The IDT49FCT818 is a high-speed, general purpose octal register with Serial Protocol Channel (SPC). The D-to-Y path of the octal register provides a data path that is designed for normal system operation wherever a high-speed clocked register is required.

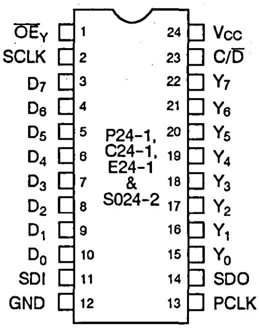
The SPC command and data registers are used to observe and control the octal data register for diagnostic purposes. The SPC command and data registers can be accessed while the system is performing normal system function. Diagnostic operations then can be performed "on the fly", synchronous with the system clock, or can be performed in the "single step" environment. The SPC port utilizes serial data in and out pins (a concept originated at IBM) which can participate in a serial scan loop throughout the system. Here normal data, address, status and control registers are replaced with the IDT49FCT818. The loop can be used to scan in a complete test routine starting point (data, address, etc). Then, after a specified number of clock cycles, the data can be clocked out and compared with expected results.

As well as diagnostic operations, SPC can be used for initializing at power-on time functions such as Writable Control Store (WCS).

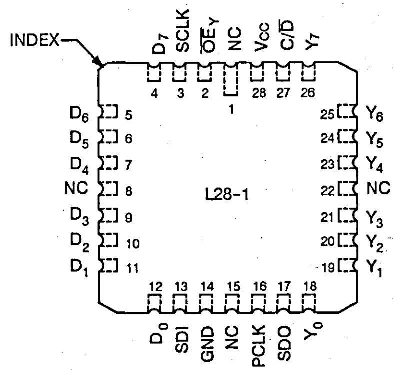
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

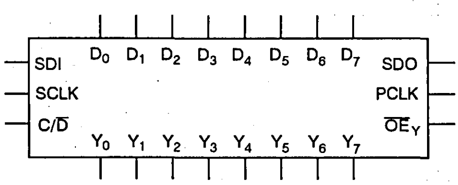


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



TRUTH TABLE (1)

C/D̅	SCLK	PCLK	OE̅Y	D	Y	FUNCTION
X	X	X	H	X	High Z	Tri-state Y
X	X	↑	L	H	H	Clock D to Y
X	X	↑	L	L	L	Clock D to Y
H	↑	X	X	X	X	Shift bit into SPC Command register
L	↑	X	X	X	X	Shift bit into SPC Data register
↓	↑	H or L (Static)	X	X	X	Execute SPC command during time between C/D̅ & SCLK

NOTE:
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↓ ↑ = Transition, H to L or L to H

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
PCLK	I	Parallel Data Register Clock
D_{7-0}	I/O	Parallel Data Register Input Pins (D_0 = LSB, D_7 = MSB)
Y_{7-0}	I/O	Parallel Data Register Output Pins (Y_0 = LSB, Y_7 = MSB)
$\overline{OE}_Y$	I	Output Enable for Y Bus (Overidden by SPC Inst. 8 & 14)
SDI	I	Serial Data In for SPC Operation. Data and command shifts in the Least Significant Bit first
SDO	O	Serial Data Out for SPC Operation. Data and command shifts out the Least Significant Bit first
C/D̅	I	Mode Control for SPC
SCLK	I	Serial Shift Clock for SPC Operations

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15[4]	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15[4]	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 24mA MIL.	–	0.3	0.5	
			I_{OL} = 32mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clocks Only	–		–	200	–	mV

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V^{(3)}$		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open $\overline{OE}_Y$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current (6)	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_Y$ = GND One Bit Toggling at f_I = 5MHz 50% Duty Cycle SCLK = C/$\overline{D}$ = SDI = V_{CC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_Y$ = GND Eight Bits Toggling at f_I = 5MHz 50% Duty Cycle SCLK = C/$\overline{D}$ = SDI = V_{CC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8(5)	
			V_{IN} = 3.4V V_{IN} = GND	–	6.0	16.8(5)	

NOTES:

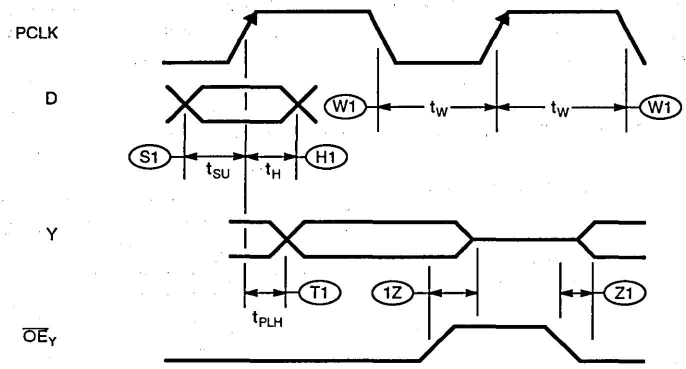
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

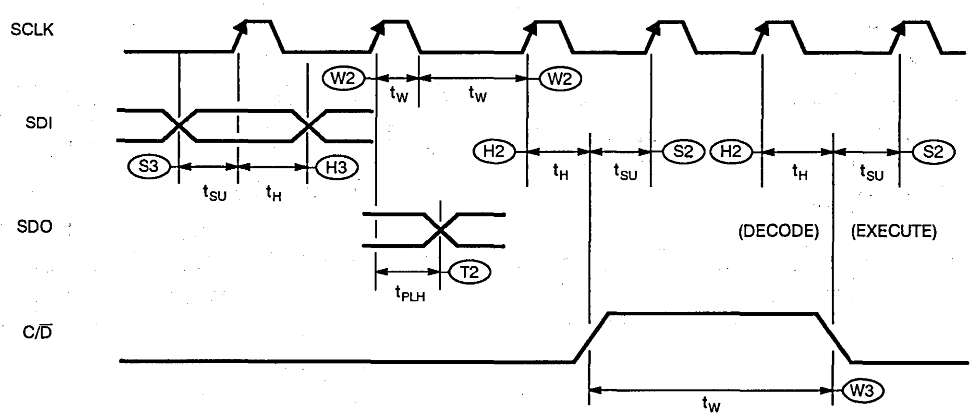
SYMBOL		PARAMETER	CONDITION[1]	IDT49FCT818				IDT49FCT818A				IDT49FCT818B				UNIT
				COM'L.		MIL.		COM'L.		MIL.		COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PHL} t_{PLH}	T1	PCLK ↑ to Y		3.0	12.5	3.0	14.0	3.0	10.0	3.0	11.0	–	–	–	–	ns
	T2	SCLK ↑ to SDO		3.0	12.5	3.0	14.0	3.0	10.0	3.0	11.0	–	–	–	–	
	T3	SDI to SDO (in stub mode)		3.0	12.5	3.0	14.0	3.0	10.0	3.0	11.0	–	–	–	–	
	T4	C/$\overline{D}$ ↓ to Y ($\overline{OE}_Y$ = Low Inst. 8 & 14)		3.0	12.5	3.0	14.0	3.0	10.0	3.0	11.0	–	–	–	–	
	T5	SCLK ↑ to Y ($\overline{OE}_Y$ = High, Inst. 8)		3.0	12.5	3.0	14.0	3.0	10.0	3.0	11.0	–	–	–	–	
	T6	C/$\overline{D}$ to SDO (Inst. 0, 1, 2 & 4)		3.0	12.5	3.0	14.0	3.0	10.0	3.0	11.0	–	–	–	–	
t_{SU}	S1	D to PCLK ↑		2.5	–	3.0	–	2.5	–	3.0	–	–	–	–	–	ns
	S2	C/$\overline{D}$ to SCLK ↑		12.0	–	14.0	–	12.0	–	14.0	–	–	–	–	–	
	S3	SDI to SCLK ↑		4.0	–	5.0	–	4.0	–	5.0	–	–	–	–	–	
	S4	Y or D to C/$\overline{D}$ ↓ (Inst. 0, 2 & 4)		2.0	–	2.5	–	2.0	–	2.5	–	–	–	–	–	
	S5	C/$\overline{D}$ (Low) to PCLK ↑ (Inst. 3 & 13)		8.0	–	9.0	–	8.0	–	9.0	–	–	–	–	–	
	S6	Y to PCLK ↑ (Inst. 3)		2.0	–	2.5	–	2.0	–	2.5	–	–	–	–	–	
t_H	H1	D to PCLK ↑		2.0	–	2.5	–	2.0	–	2.5	–	–	–	–	–	ns
	H2	C/$\overline{D}$ to SCLK ↑		12.0	–	14.0	–	12.0	–	14.0	–	–	–	–	–	
	H3	SDI to SCLK ↑		1.0	–	1.0	–	1.0	–	1.0	–	–	–	–	–	
	H4	Y or D to C/$\overline{D}$ ↓ (Inst. 0, 2 & 4)	C_L = 50pF R_L = 500Ω	2.0	–	2.5	–	2.0	–	2.5	–	–	–	–	–	
	H5	SCLK (Low) to PCLK ↑ (Inst. 3 & 13)		2.0	–	2.5	–	2.0	–	2.5	–	–	–	–	–	
	H6	C/$\overline{D}$ (Low) to PCLK ↑ (Inst. 3 & 13)		2.0	–	2.5	–	2.0	–	2.5	–	–	–	–	–	
	H7	Y to PCLK ↑ (Inst. 3)		3.0	–	3.0	–	3.0	–	3.0	–	–	–	–	–	
t_{PHZ} t_{PLZ}	1Z	$\overline{OE}_Y$ to Y		3.0	8.0	3.0	8.0	3.0	8.0	3.0	8.0	–	–	–	–	ns
	2Z	SCLK ↑ to D (Inst. 5 & 9)		3.0	9.0	3.0	9.0	3.0	9.0	3.0	9.0	–	–	–	–	
	3Z	C/$\overline{D}$ ↑ to D or Y (Inst. 5 & 9)		3.0	9.0	3.0	9.0	3.0	9.0	3.0	9.0	–	–	–	–	
	4Z	SCLK ↑ to Y ($\overline{OE}_Y$ = High Inst. 8 & 14)		3.0	9.0	3.0	9.0	3.0	9.0	3.0	9.0	–	–	–	–	
	5Z	C/$\overline{D}$ to ↑ to D or Y ($\overline{OE}_Y$ = High Inst. 14)		3.0	9.0	3.0	9.0	3.0	9.0	3.0	9.0	–	–	–	–	
t_{PZH} t_{PZL}	Z1	$\overline{OE}_Y$ to Y		3.0	10.0	3.0	10.0	3.0	10.0	3.0	10.0	–	–	–	–	ns
	Z2	C/$\overline{D}$ ↓ to D (Inst. 5 & 9)		3.0	10.0	3.0	10.0	3.0	10.0	3.0	10.0	–	–	–	–	
	Z3	C/$\overline{D}$ ↓ to Y ($\overline{OE}_Y$ = High Inst. 14)		3.0	10.0	3.0	10.0	3.0	10.0	3.0	10.0	–	–	–	–	
t_W	W1	PCLK (High & Low)		7.0	–	8.0	–	7.0	–	8.0	–	–	–	–	–	ns
	W2	SCLK (High & Low)		25	–	25	–	25	–	25	–	–	–	–	–	
	W3	C/$\overline{D}$ (High)		25	–	25	–	25	–	25	–	–	–	–	–	

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

GENERAL AC WAVEFORMS FOR PARALLEL INPUTS AND OUTPUTS



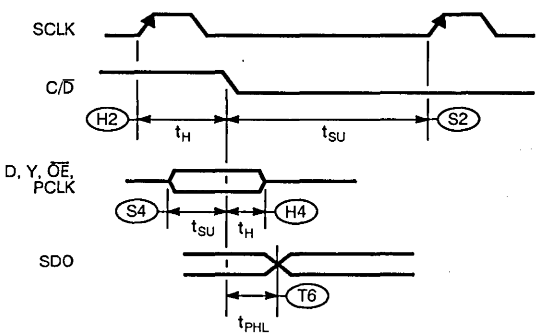
GENERAL AC WAVEFORMS FOR SERIAL PROTOCOL INPUTS AND OUTPUTS



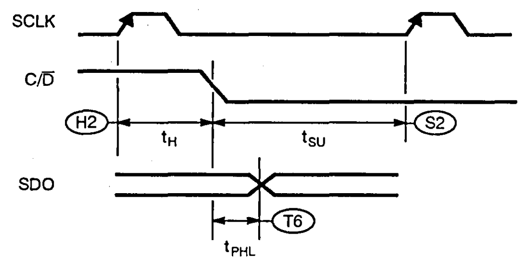
10

DETAILED WAVEFORMS OF SERIAL PROTOCOL OPERATIONS

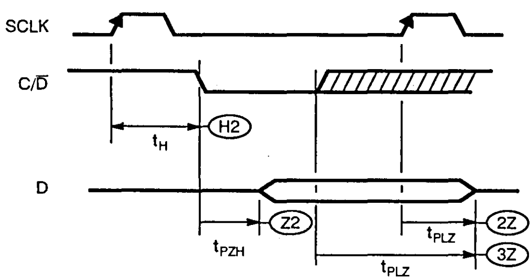
Y ⟶ SPC Data (Inst. 0)
D ⟶ SPC Data (Inst. 2)
Status ⟶ SPC Data (Inst. 4)



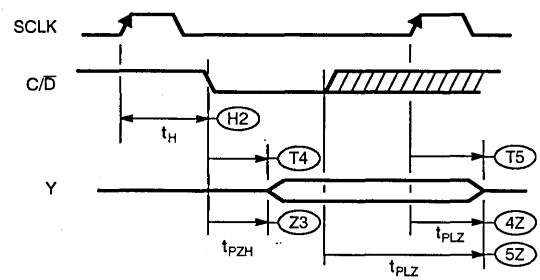
PARALLEL DATA REGISTER ⟶ SPC Data (Inst. 1)
SET SERIAL MODE (Inst. 11)
SET STUB MODE (Inst. 12)



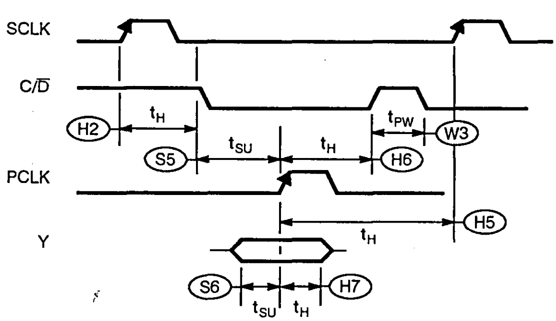
CONNECT Y TO D (Inst. 5)
SPC Data ⟶ D (Inst. 9)



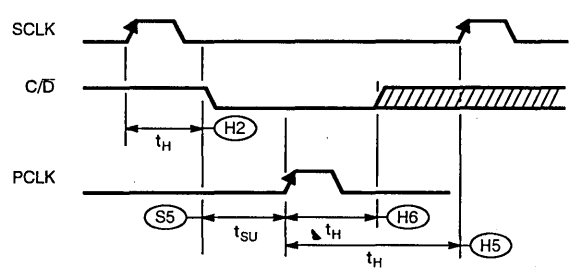
SPC Data ⟶ PARALLEL DATA REGISTER (Inst. 10)
SPC Data ⟶ Y (Inst. 8)
CONNECT D TO Y (Inst. 14)



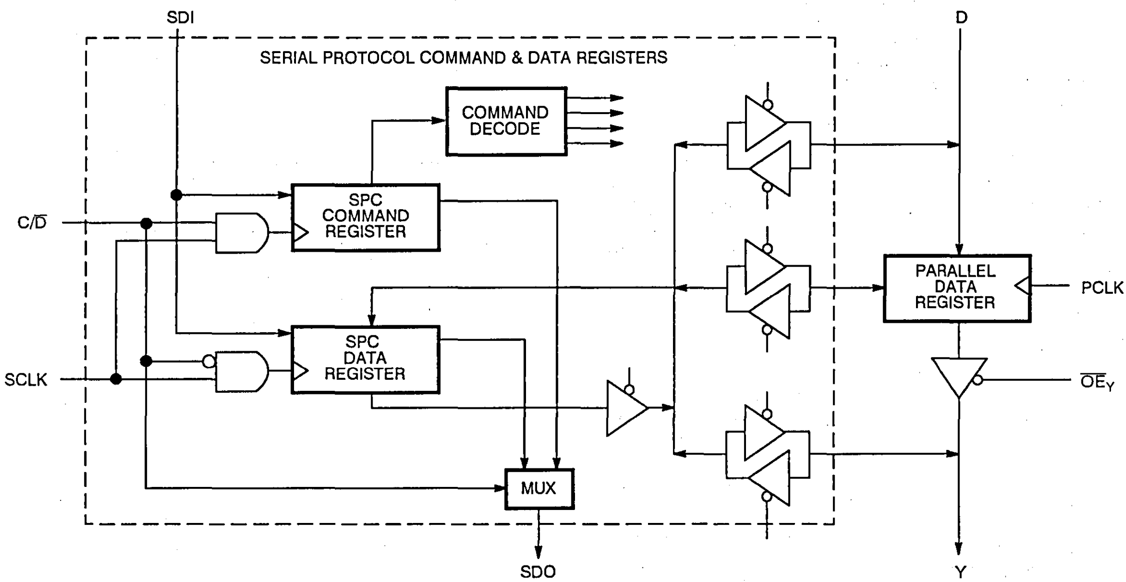
Y ⟶ SPC Data SYNCHRONOUS W/PCLK (Inst. 3)



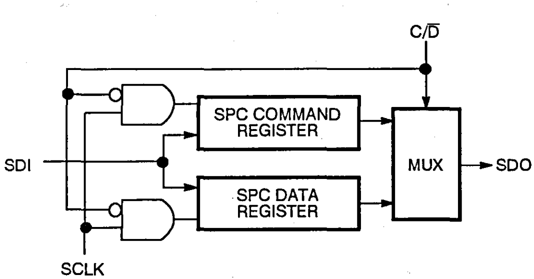
SPC Data ⟶ PARALLEL DATA REGISTER SYNCHRONOUS W/PCLK (Inst. 13)



DETAILED FUNCTIONAL BLOCK DIAGRAM



The detailed block diagram consists of two main elements: the parallel data register and the SPC data/command registers. The main data path is from the D inputs down to the data register and through to the Y outputs. This path is typically used during standard operations. For diagnostic or systems initialization, the internal SPC data path is used. This path allows access between the SPC data and command registers and the standard data path, pins and data register. The SPC data and command registers are accessed via the SDI, SDO, C/D̄ and SCLK pins.

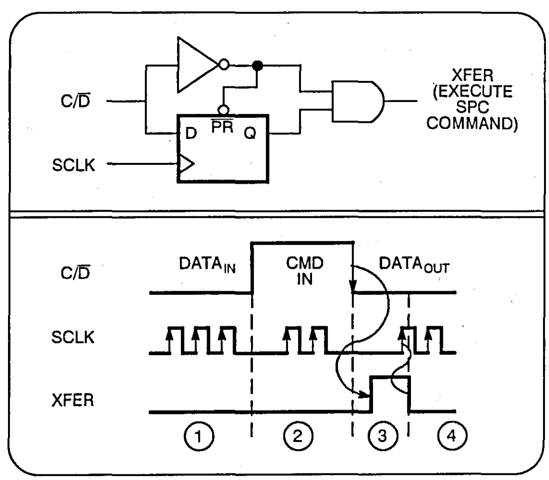


SPC FUNCTIONAL DESCRIPTION

The Serial Protocol Channel (SPC) has been optimized for the minimum number of pins and the maximum flexibility. The data is passed in on a Serial Data Input pin (SDI) and out on a Serial Data Output pin (SDO). The transfer of the data is controlled by a Serial Clock (SCLK) and a Command/Data mode input (C/D̄). These four pins are the basic SPC pins. To the outside, the SPC appears as two serial shift registers in parallel—one for command and the other data. The serial clock shifts data and the Command/Data (C/D̄) line selects which register is being shifted. The command register is used to control loading of data to and from the data register with other storage elements in the device.

With respect to executing an SPC command, there are four distinct phases: (1) data is shifted in, (2) followed by the command, (3) the command is executed, and (4) data is shifted out. During the data mode, data is simultaneously shifted into the serial data register while the data in the register is shifted out. During the command mode, opcode-type information is shifted through the serial ports. The command is executed when the last bit is shifted in and the C/D̄ line is brought low. The execution phase is ended with the next serial clock edge.

10



SPC data and commands are shifted in through the SDI pin, which is a serial input pin, and out through the SDO pin, which is a serial output pin. Data and commands are shifted in Least Significant Bit first; Most Significant Bit last (Y_0 = LSB, Y_{15} = MSB). Execution of SPC commands is performed by stopping the shift clock, SCLK, and lowering the C/$\overline{D}$ line from high-to-low. Later the SCLK may then be transitioned from low-to-high. SPC commands and data can be shifted anytime, without regard for operation. During the execution phase, care must be taken that there is no conflict between the SPC operation and parallel operation. This means that if the SPC operation attempts to load the parallel data register (opcode 10) while PCLK is in transition, the results are undefined. In general, it is required that the PCLK be static during SPC operations. The synchronous commands (opcode 3 and 13), however, allow the PCLK to run. In these operations, the high-to-low transition of the C/$\overline{D}$ line takes on the function of an arm signal in preparation for the next low-to-high transition of the PCLK.

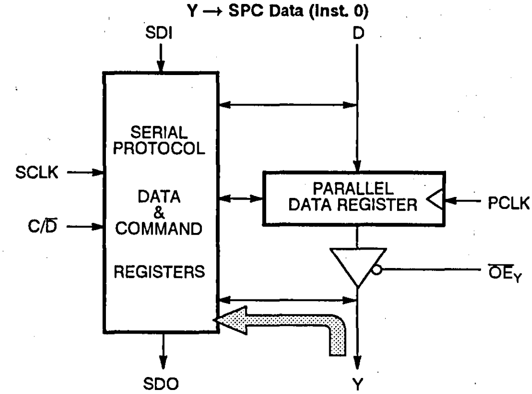
SPC COMMANDS

There are 16 possible SPC opcodes. Fourteen of these are utilized, the other two are reserved and perform NO-OP functions. The top eight opcodes, 0 through 7, are reserved for transferring data into the SPC data register for shifting out. The lower eight opcodes, 8 through 15, are used for transferring data from the SPC data register to other parts of the device. Two of the commands are also used for connecting the data in and out pins.

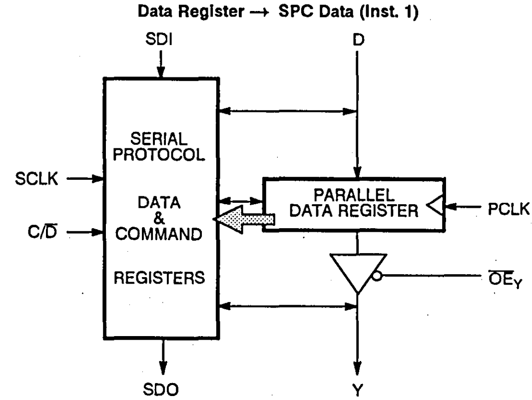
OPCODE	SPC COMMAND
0	Y to SPC Data Register
1	Parallel Data Register to SPC Data Register
2	D to SPC Data Register
3	Y to SPC Data Register Synchronous w/PCLK
4	Status ($\overline{OE}_Y$, PCLK) to SPC Data Register
5	Connect Y to D
6-7	Reserved (NO-OP)
8	SPC Data to Y ($\overline{OE}$ is overidden)
9	SPC Data to D
10	SPC Data to Parallel Data Register
11	Select Serial Mode
12	Select Stub Mode
13	SPC Data to Parallel Data Register Synchronous w/PCLK
14	Connect D to Y ($\overline{OE}$ is overidden)
15	NO-OP

Opcode 0 is used for transferring data from the Y output pins into the SPC data register. Opcode 1 transfers data from the output of the register, before the tri-state gate, into the SPC data register. Opcode 2 transfers data from the D input pins into the SPC data register.

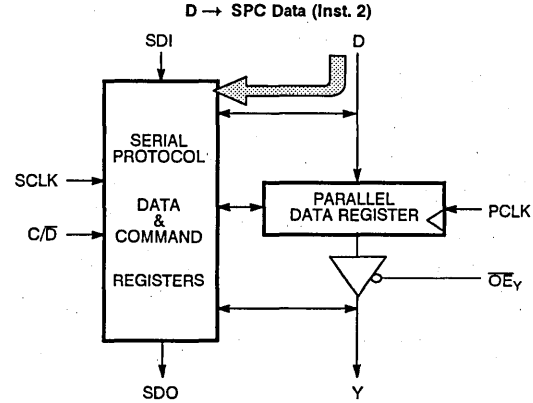
Y → SPC Data (Inst. 0)



Data Register → SPC Data (Inst. 1)

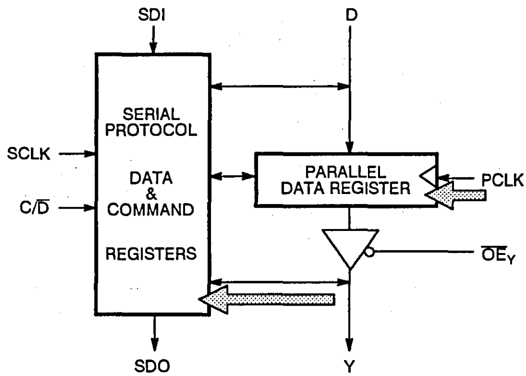


D → SPC Data (Inst. 2)

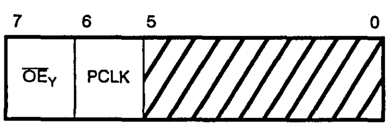


Opcode 3 transfers data on the Y pins to the SPC data register on the next PCLK, thus achieving a synchronous observation of the SPC data register in real time. This operation can be forced to repeat without shifting in a new command by pulsing C/$\overline{D}$ low-high-low after each PCLK. As soon as data is shifted out using SCLK, the command is terminated and must be loaded in again.

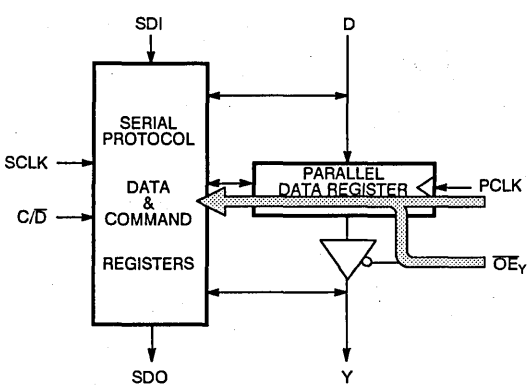
Y → SPC Data Synchronous w/PCLK (Inst. 3)



Opcode 4 is used for loading status into the SPC data register. The format of bits is shown below.

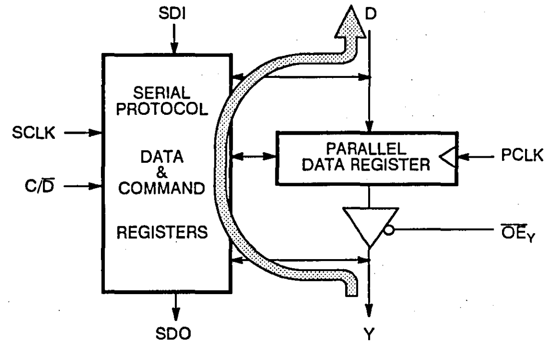


Status → SPC Data (Inst. 4)

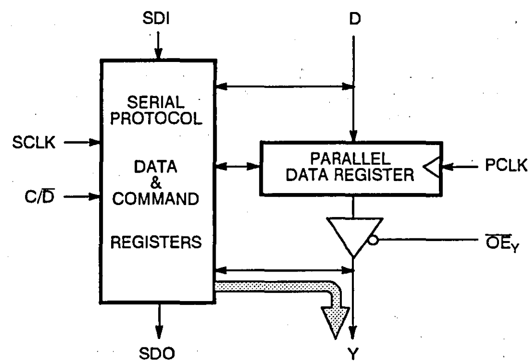


Opcode 5 connects Y to D. Opcodes 6 and 7 are reserved, hence designated NO-OP.

Connect Y to D (Inst. 5)

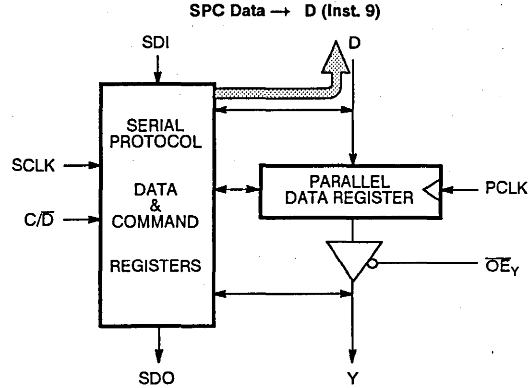


SPC Data → Y (Inst. 8)



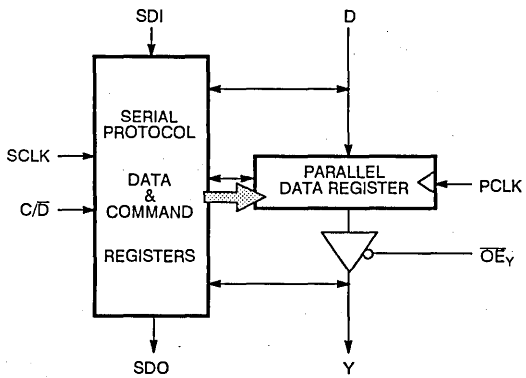
Opcode 8 is used for transferring SPC data directly to the Y pins. When executing opcode 8, the state of $\overline{OE}_Y$ is a "do not care"; that is, data will be output even if $\overline{OE}_Y$ = HIGH. Opcode 9 is used for transferring SPC data to the D pins. Operands 8 and 9 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$. As soon as SCLK completes transition, the command is terminated.

SPC Data → D (Inst. 9)



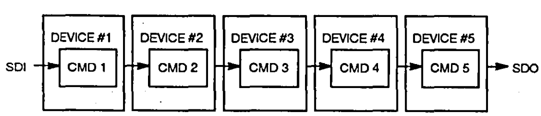
Opcode 10 is used for transferring data from the SPC data register into the parallel data register, irrespective of the state of PCLK. However, PCLK must be static between C/$\overline{D}$ going high-to-low and SCLK going low-to-high.

SPC Data → Parallel Data Register (Inst. 10)



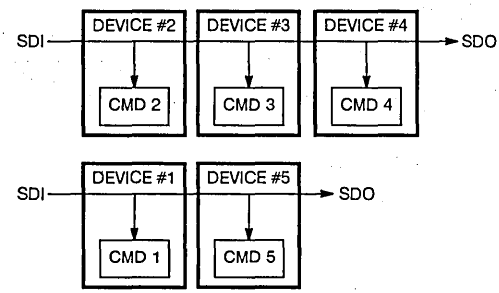
Opcodes 11 and 12 are used to set Serial and Stub Mode, respectively. After executing one of these opcodes, the device remains in this mode until programmed otherwise. The Serial mode is the default mode that the IDT49FCT818 powers up in. In Serial mode, commands are shifted through the SPC command register and then to the SDO pin. This is the typical mode used when several varieties of devices that utilize the SPC access method are employed on one serial ring.

SERIAL MODE



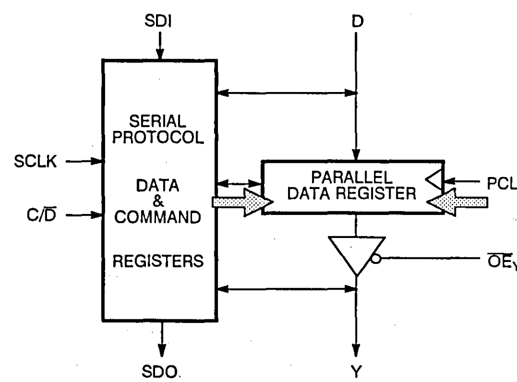
In Stub mode, SDI is connected directly to SDO. In this way, the same diagnostic command can be loaded into multiple devices of like type. For example, in four clock cycles the same command could be loaded into 8 IDT49FCT818s (64-bit pipeline register). Dissimilar devices must be segregated into serial scan loops of similar type, as shown below. During the command phase, the serial shift clock must be slowed down to accommodate the delay from SDI to SDO through all of the devices. The slower clock is typically a small tradeoff compared to the reduced number of clock cycles.

STUB MODE

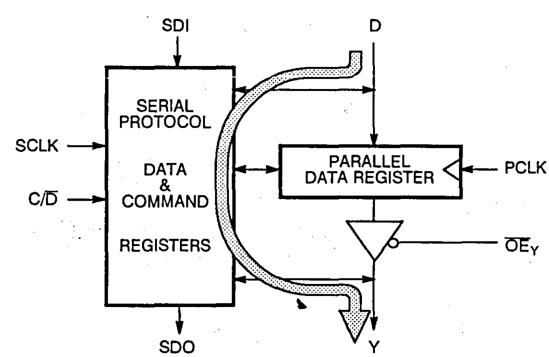


Opcode 13 transfers data from the SPC data register to the parallel data register on the next PCLK. Opcode 14 connects the D bus to the Y. Operation 14 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$ input again. The operation is terminated by SCLK.

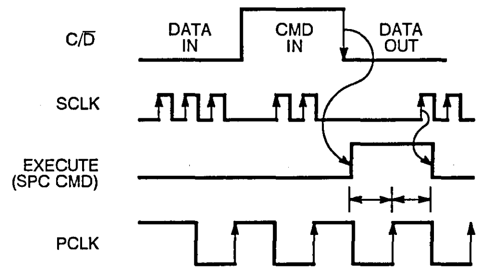
SPC Data → Parallel Data Register Synchronous w/PCLK (Inst. 13)



Connect D to Y (Inst. 14)



Opcodes 3 and 13 transfer data synchronous to the PCLK which means that the high-to-low on the C/$\overline{D}$ input is an arm signal. The data and command can be shifted in while the PCLK is running. The C/$\overline{D}$ line is dropped prior to the desired PCLK edge and raised before the next edge. Instruction 13 can be repeated over many times by leaving the C/$\overline{D}$ line low during multiple transitions of the PCLK while not clocking SCLK. PCLK cycles can even be skipped by raising the C/$\overline{D}$ input during the desired clock periods. Instruction 3 can be repeated by pulsing the C/$\overline{D}$ high after each PCLK.



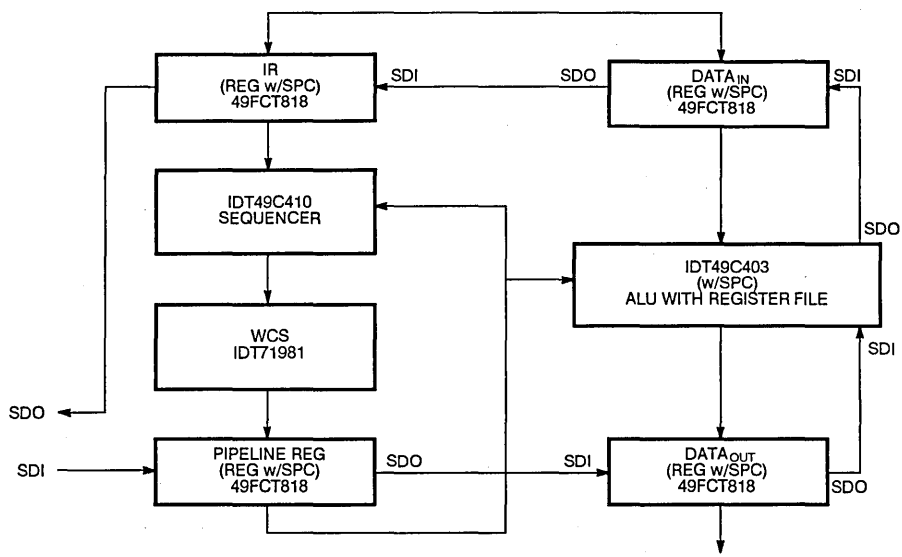
The ability to continuously execute a synchronous command can provide major benefits. For example, the synchronous read (Instruction 3, Y to SPC data) instruction could be clocked into the SPC data register. Then, it could be continuously executed by pulsing the C/$\overline{D}$ line high. When the whole system is stopped (PCLK quiescent), the serial data register will contain the next to the last state of the parallel data register. That value can be shifted out and the current state of the parallel register can then be observed, allowing for the observation of two states of the parallel register (the current and the previous).

TYPICAL APPLICATION

In the block diagram of the typical application, the SPC data register is shown being used with a writable control store in a microprogrammed design. The control store can be initialized through the diagnostics path. The SPC data register is used for the instruction register going into the IDT49C410, as well as for data registers around the IDT49C403. In this way, the designer may use the SPC data register to observe and modify the microcode coming out of the writable control store, as well as observing and being able to modify data and instructions in the overall machine. The IDT49C403 is a 16-bit version of the 2903A/203 which includes an SPC port for diagnostic and break point purposes.

The block diagram of the diagnostics ring shows how devices with diagnostics are hooked together in a serial ring via the SDI and SDO signals, The diagnostics signals may be generated through registers which are hooked up to a microprocessor. This microprocessor could conceivably be an IBM PC.

TYPICAL MICROPROGRAM APPLICATION WITH SPC™



10

As companies like IDT continue to integrate more onto each device and put each device into smaller packages such as surface mount devices, the board level testing becomes more complex for the designer and the manufacturing divisions of companies. To help this situation, serial diagnostics was invented. This allows for observation of critical signals deep within the system. During system test, when an error is observed, these signals may be modified in order to zero in on the fault in the system.

Serial diagnostics is primarily a scheme utilizing only a few pins (4) to examine and alter the internal state of a system for the purpose of monitoring and diagnosing system faults. It can be used at many points in the life of a product: design debug and verification, manufacturing test and field service. This document describes a serial diagnostic scheme which was developed at IDT and will be used in future VLSI logic devices designed by IDT.

ORDERING INFORMATION

IDT XXXX (Device Type) XX (Package) X (Process)

Field	Code	Description
Process	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	P	Plastic DIP
	C	Sidebraze DIP
	E	CERPACK
	L	Leadless Chip Carrier
	SO	Small Outline IC
Device Type	49FCT818	Octal Register with SPC™
	49FCT818A	High-Speed Octal Register with SPC™
	49FCT818B	High-Speed Octal Register with SPC™

FAST CMOS 1-OF-8 DECODER

IDT54/74FCT138
IDT54/74FCT138A

Integrated Device Technology, Inc.

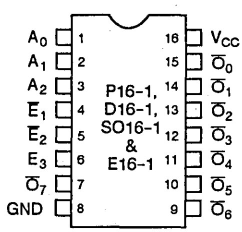
FEATURES:

- IDT54/74FCT138 equivalent to FAST™ speed; **IDT54/74FCT138A 35% faster than FAST™**
- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5µW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5µA max.)
- 1-of-8 decoder with enables
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87654 is listed on this function. Refer to Section 2/page 2-4.

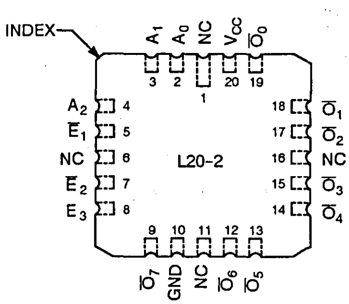
DESCRIPTION:

The IDT54/74FCT138 and IDT54/74FCT138A are 1-of-8 decoders built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT138 and IDT54/74FCT138A accept three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provide eight mutually exclusive active LOW outputs ($\overline{O}_0$ - $\overline{O}_7$). The IDT54/74FCT138 and IDT54/74FCT138A feature three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four IDT54/74FCT138 or IDT54/74FCT138A devices and one inverter.

PIN CONFIGURATIONS

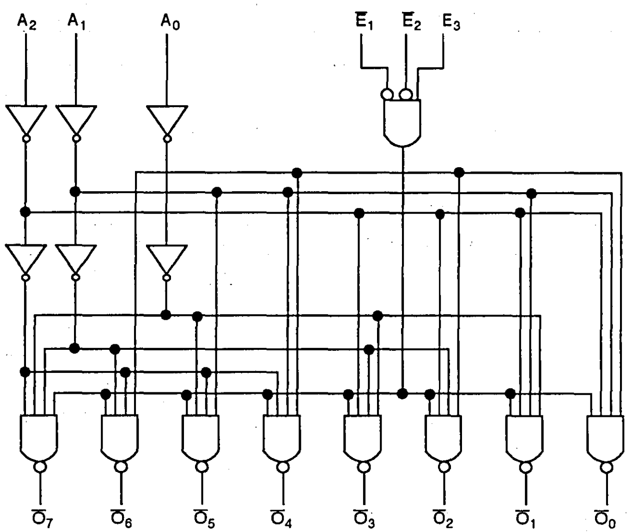


DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



10

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER [1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = − 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP. [2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5 [4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5 [4]	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300 µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_I = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.5	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.5	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	0.38	2.3[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	0.63	3.3[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

10

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0 - A_2	Address Inputs
$\bar{E}_1$, $\bar{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\bar{O}_0$ - $\bar{O}_7$	Outputs (Active LOW)

TRUTH TABLE

INPUTS						OUTPUTS							
$\bar{E}_1$	$\bar{E}_2$	E_3	A_0	A_1	A_2	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT138					IDT54/74FCT138A					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_0 to $\bar{O}_n$	C_L = 50pF R_L = 500Ω	7.0	1.5	9.0	1.5	12.0	4.5	1.5	5.8	1.5	7.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{E}_1$ or $\bar{E}_2$ to $\bar{O}_n$		6.0	1.5	9.0	1.5	12.5	4.5	1.5	5.9	1.5	8.0	ns
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\bar{O}_n$		6.0	1.5	9.0	1.5	12.5	4.5	1.5	5.9	1.5	8.0	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT	XXXX	X	X
Temp. Range	Device Type	Package	Process

Code	Description
Blank	Commercial
B	MIL-STD-883, Class B
P	Plastic DIP
D	CERDIP
SO	Small Outline IC
E	CERPACK
L	Leadless Chip Carrier
138	1-of-8 Decoder
138A	Fast 1-of-8 Decoder
54	-55°C to +125°C
74	0°C to +70°C

FAST CMOS DUAL 1-OF-4 DECODER

IDT54/74FCT139
IDT54/74FCT139A

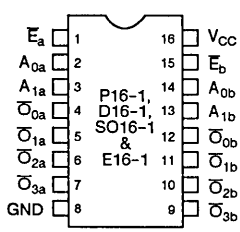
FEATURES:

- IDT54/74FCT139 equivalent to FAST™ speed; **IDT54/74FCT139A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Dual 1-of-4 decoder with enable
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

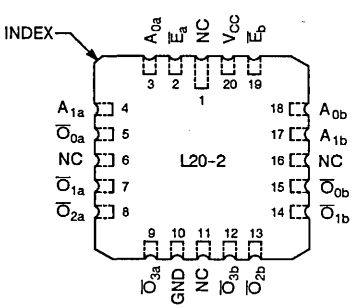
DESCRIPTION:

The IDT54/74FCT139 and IDT54/74FCT139A are dual 1-of-4 decoders built using advanced CEMOS™, a dual metal CMOS technology. The devices have two independent decoders, each of which accept two binary weighted inputs (A_0-A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH, all outputs are forced HIGH.

PIN CONFIGURATIONS

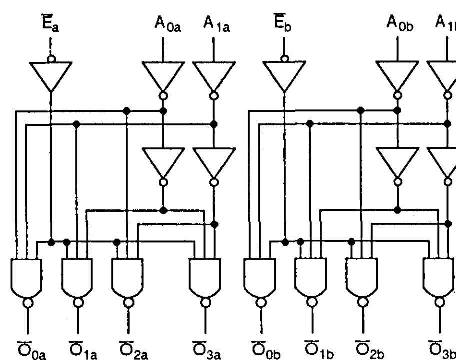


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	–	
			I_{OH} = –12mA MIL.	2.4	4.3	–	
			I_{OH} = –15mA COM'L.	2.4	4.3	–	
V_{OL}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.5	mA
			$V_{IN} = 3.4V$ V_{IN} = GND	–	1.8	5.5	
		V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle One Input Toggling on Each Decoder	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	7.5[5]	
			$V_{IN} = 3.4V$ V_{IN} = GND	–	3.5	9.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0V$, $+25°C$ ambient and maximum loading.
3. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0, A_1	Address Inputs
$\overline{E}_A$, $\overline{E}_B$	Enable Inputs (Active LOW)
$\overline{O}_0$-$\overline{O}_3$	Outputs (Active LOW)

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT139					IDT54/74FCT139A					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	6.0	1.5	9.0	1.5	12.0	4.5	1.5	5.9	1.5	7.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_A$ or $\overline{E}_B$ to $\overline{O}_n$		5.5	1.5	8.0	1.5	9.0	4.0	1.5	5.5	1.5	7.2	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT | A | X | X
Temp. Range | Device Type | Package | Process

Process:
- Blank — Commercial
- B — MIL-STD-883, Class B

Package:
- P — Plastic DIP
- D — CERDIP
- SO — Small Outline IC
- L — Leadless Chip Carrier
- E — CERDIP

Device Type:
- 139 — Dual 1-of-4 Decoder
- 139A — Fast Dual 1-of-4 Decoder

Temp. Range:
- 54 — -55°C to +125°C
- 74 — 0°C to +70°C

10

Integrated Device Technology, Inc.

FAST CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

IDT54/74FCT161/A
IDT54/74FCT163/A

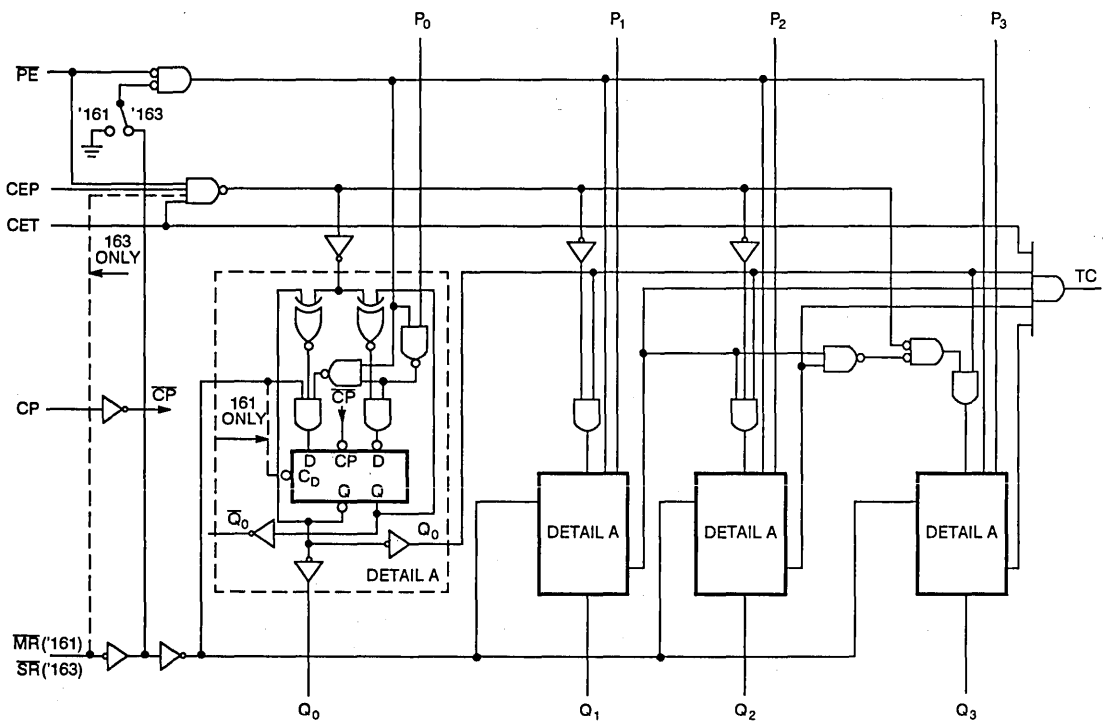
FEATURES:

- IDT54/74FCT161/163 equivalent to FAST™ speed; **IDT54/74FCT161A/163A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT161/163 and IDT54/74FCT161A/163A are high-speed synchronous modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology.They are synchronously presettable for application in programmable dividers and have two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-stage counters. The IDT54/74FCT161 and IDT54/74FCT161A have asynchronous Master Reset inputs that override all other inputs and force the outputs LOW. The IDT54/74FCT163 and IDT54/74FCT163A have Synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAM

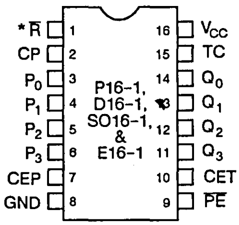


CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Company

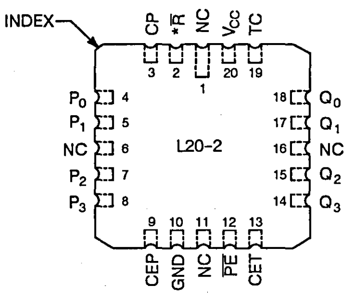
MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-4007/-

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

* M̄R̄ FOR '161
* S̄R̄ FOR '163

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300µA	V_{HC}	V_{CC}	–	
			I_{OH} = −12mA MIL.	2.4	4.3	–	
			I_{OH} = −15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS (IDT54/74FCT161/A)

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{CC} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Power Supply Current per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open Load Mode CEP = CET = $\overline{PE}$ = GND $\overline{MR}$ = V_{CC} One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current(6)	V_{CC} = Max. Outputs Open Load Mode f_{CP} = 10MHz 50% Duty Cycle CEP = CET = $\overline{PE}$ = GND $\overline{MR}$ = V_{CC} Four Bits Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.75(5)	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	5.0	12.75(5)	

POWER SUPPLY CHARACTERISTICS (IDT54/74FCT163/A)

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{CC} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Power Supply Current per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open Load Mode CEP = CET = $\overline{PE}$ = GND $\overline{SR}$ = V_{CC} One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current(6)	V_{CC} = Max. Outputs Open Load Mode f_{CP} = 10MHz 50% Duty Cycle CEP = CET = $\overline{PE}$ = GND $\overline{SR}$ = V_{CC} Four Bits Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.75(5)	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	5.0	12.75(5)	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('163)	Synchronous Reset Input (Active LOW)
P_{0-3}	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q_{0-3}	Flip-Flop Outputs
TC	Terminal Count Output

TRUTH TABLE (2)

$\overline{SR}$ (1)	$\overline{PE}$	CET	CEP	ACTION ON THE RISING CLOCK EDGE (S)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

NOTES:
1. For FCT163/163A only.
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

		(1)	IDT54/74FCT161 IDT54/74FCT163					IDT54/74FCT161A IDT54/74FCT163A					
			TYP.(3)	MIL.		COM'L.		TYP.(3)	MIL.		COM'L.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	C_L = 50pF R_L = 500Ω	7.0	2.0	11.5	2.0	11.0	4.5	2.0	7.5	2.0	7.2	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)		7.0	2.0	10.0	2.0	9.5	4.5	2.0	6.5	2.0	6.2	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		10.0	2.0	16.5	2.0	15.0	6.5	2.0	10.8	2.0	9.8	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC		4.5	1.5	9.0	1.5	8.5	3.0	1.5	5.9	1.5	5.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('F161)		9.0	2.0	14.0	2.0	13.0	5.9	2.0	9.1	2.0	8.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC		8.0	2.0	12.5	2.0	11.5	5.2	2.0	8.2	2.0	7.5	ns
t_{SU}(H) t_{SU}(L)	Set-up Time, HIGH or LOW P_n to CP		5.0	5.5	–	5.0	–	4.0	4.5	–	4.0	–	ns
t_H(H) t_H(L)	Hold Time, HIGH or LOW P_n to CP		2.0	2.0	–	1.5	–	1.5	2.0	–	1.5	–	ns
t_{SU}(H) t_{SU}(L)	Set-up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		11.0	13.5	–	11.5	–	9.0	11.5	–	9.5	–	ns
t_H(H) t_H(L)	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		2.0	1.5	–	1.5	–	1.5	1.5	–	1.5	–	ns
t_{SU}(H) t_{SU}(L)	Set-up Time, HIGH or LOW CEP or CET to CP		11.0	13.0	–	11.5	–	9.0	11.0	–	9.5	–	ns
t_H(H) t_H(L)	Hold Time, HIGH or LOW CEP or CET to CP		0	0	–	0	–	0	0	–	0	–	ns
t_W(H) t_W(L)	Clock Pulse Width (Load) HIGH or LOW		5.0	5.0	–	5.0	–	4.0	4.0	–	4.0	–	ns
t_W(H) t_W(L)	Clock Pulse Width (Count) HIGH or LOW		6.0	8.0	–	7.0	–	5.0	7.0	–	6.0	–	ns
t_W(L)	$\overline{MR}$ Pulse Width, LOW ('F161)		5.0	5.0	–	5.0	–	4.0	4.0	–	4.0	–	ns
t_{REM}	Recovery Time $\overline{MR}$ to CP ('F161)		6.0	6.0	–	6.0	–	5.0	5.0	–	5.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT	XXXX	X	X
Temp. Range	Device Type	Package	Process

Process

Blank	Commercial
B	MIL-STD-883, Class B

Package

P	Plastic DIP
D	CERDIP
L	Leadless Chip Carrier
SO	Small Outline IC
E	CERPACK

Device Type

161	Synchronous Binary Counter with Asynchronous Master Reset
163	Synchronous Binary Counter with Synchronous Reset
161A	Fast Synchronous Binary Counter with Asynchronous Master Reset
163A	Fast Synchronous Binary Counter with Synchronous Reset

Temp. Range

54	-55°C to +125°C
74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS CARRY LOOKAHEAD GENERATOR

IDT54/74FCT182
IDT54/74FCT182A

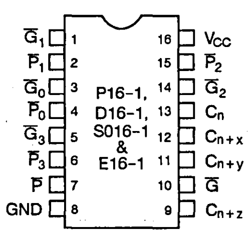
FEATURES:

- IDT54/74FCT182 equivalent to FAST™ speed; **IDT54/74FCT182A 35% faster than FAST™**
- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5µW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5µA max.)
- Carry lookahead generator
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

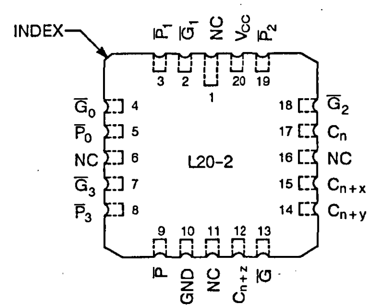
DESCRIPTION:

The IDT54/74FCT182 and IDT54/74FCT182A are high-speed carry lookahead generators built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT182 and IDT54/74FCT182A are carry lookahead generators that accept up to four pairs of active LOW Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH carry input (C_n) and provides anticipated HIGH carries (C_{n+y}, C_{n+z}) across four groups of binary adders. These products also have active LOW Carry Propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs which may be used for further levels of lookahead.

PIN CONFIGURATIONS

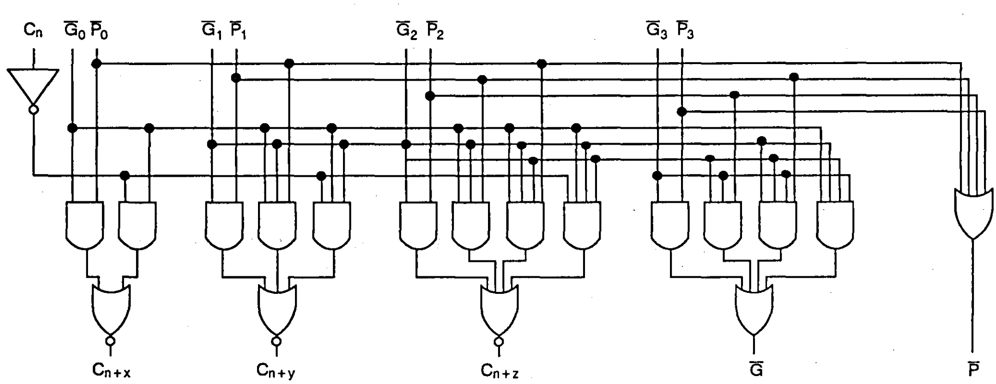


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	–	
			I_{OH} = –12mA MIL.	2.4	4.3	–	
			I_{OH} = –15mA COM'L.	2.4	4.3	–	
V_{OL}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current(5,6)	V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.5	mA
			$V_{IN} = 3.4V$ V_{IN} = GND	–	1.8	5.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0V$, +25°C ambient and maximum loading.
3. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
C_n	Carry Input
$\bar{G}_0$, $\bar{G}_2$	Carry Generate Inputs (Active LOW)
$\bar{G}_1$	Carry Generate Input (Active LOW)
$\bar{G}_3$	Carry Generate Input (Active LOW)
$\bar{P}_0$, $\bar{P}_1$	Carry Propagate Inputs (Active LOW)
$\bar{P}_2$	Carry Propagate Input (Active LOW)
$\bar{P}_3$	Carry Propagate Input (Active LOW)
C_{n+x} - C_{n+z}	Carry Outputs
$\bar{G}$	Carry Generate Output (Active LOW)
$\bar{P}$	Carry Propagate Output (Active LOW)

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\bar{G}_0$	$\bar{P}_0$	$\bar{G}_1$	$\bar{P}_1$	$\bar{G}_2$	$\bar{P}_2$	$\bar{G}_3$	$\bar{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\bar{G}$	$\bar{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT182					IDT54/74FCT182A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+y}, C_{n+y}, C_{n+z}	C_L = 50pF R_L = 500Ω	6.0	2.0	10.0	2.0	16.5	4.0	2.0	6.5	2.0	10.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, to C_{n+y}, C_{n+y}, C_{n+z}		6.0	1.5	9.0	1.5	11.5	4.0	1.5	5.8	1.5	7.4	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ to C_{n+x}, C_{n+y}, C_{n+z}		6.0	1.5	9.5	1.5	11.5	4.0	1.5	6.0	1.5	7.4	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_1$, $\overline{P}_2$ $\overline{P}_3$ to $\overline{G}$		7.0	2.0	11.0	2.0	16.5	4.8	2.0	7.0	2.0	10.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_n$ to $\overline{G}$		7.5	2.0	11.5	2.0	16.5	5.0	2.0	7.4	2.0	10.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_n$ to $\overline{P}$		6.0	1.5	8.5	1.5	12.5	4.0	1.5	5.5	1.5	7.4	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT — Temp. Range
XXXX — Device Type
X — Package
X — Process/ Temperature Range

Process/Temperature Range:
- Blank — Commercial
- B — MIL-STD-883, Class B

Package:
- P — Plastic DIP
- D — CERDIP
- SO — Small Outline IC
- L — Leadless Chip Carrier
- E — CERPACK

Device Type:
- 182 — Carry Lookahead Generator
- 182A — Fast Carry Lookahead Generator

Temp. Range:
- 54 — -55°C to +125°C
- 74 — 0°C to +70°C

10

Integrated Device Technology, Inc.

FAST CMOS UP/DOWN BINARY COUNTER

IDT54/74FCT191
IDT54/74FCT191A

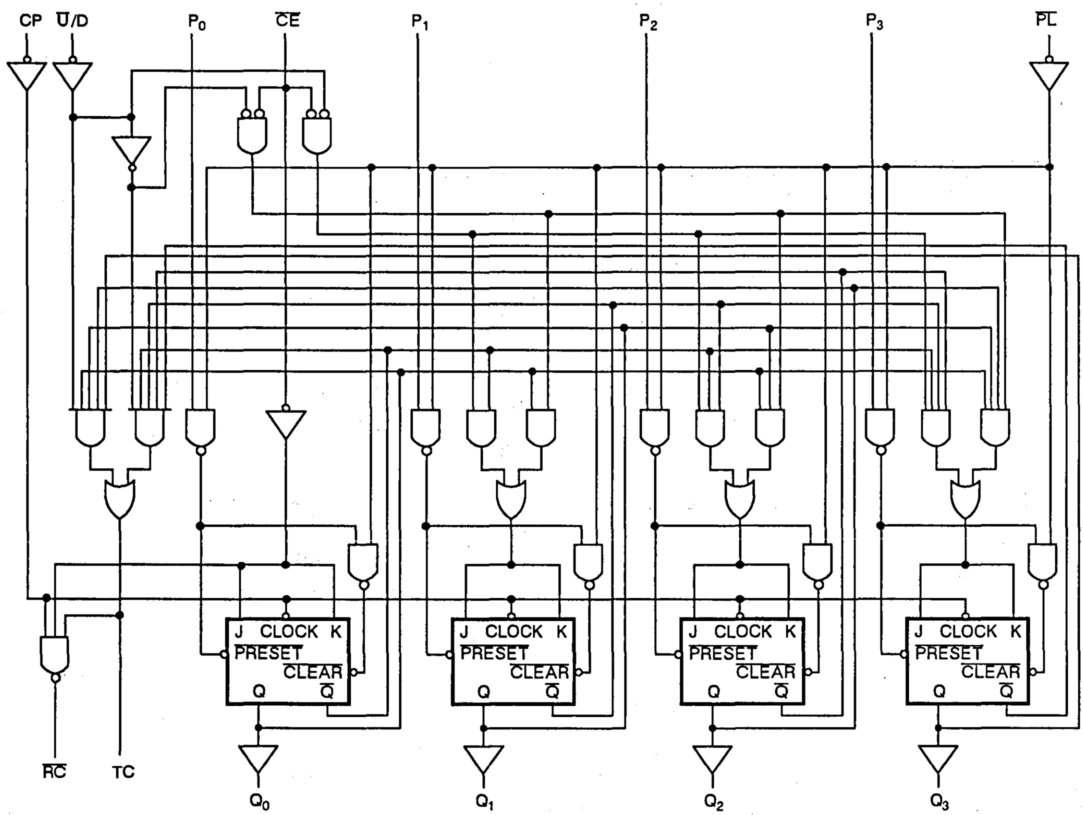
FEATURES:

- IDT54/74FCT191 equivalent to FAST™ speed; **IDT54/74FCT191A 35% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST (5μA max.)
- JEDEC standard pinout for DIP, LCC and SOIC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

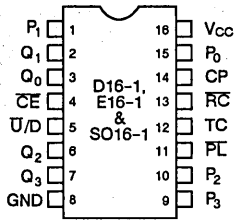
The IDT54/74FCT191 and IDT54/74FCT191A are reversible modulo-16 binary counters, featuring synchronous counting and asynchronous presetting and built using advanced CEMOS™, a dual metal CMOS technology. The preset feature allows the IDT54/74FCT191 and IDT54/74FCT191A to be used in programmable dividers. The count enable input, the terminal count output and the ripple clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAM

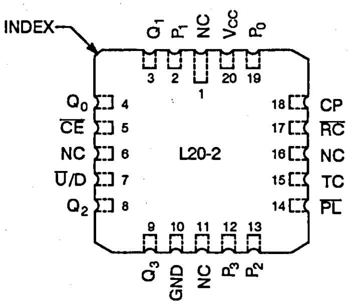


CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	$V_I = V_{CC}$	–	–	5	μA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300μA	V_{HC}	V_{CC}	–	
			I_{OH} = –12mA MIL.	2.4	4.3	–	
			I_{OH} = –15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

10

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Preset Mode $\overline{PL} = \overline{CE} = \overline{U}/D$ = CP = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Preset Mode $\overline{PL} = \overline{CE} = \overline{U}/D$ = CP = GND Four Bits Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	4.0	10.5[5]	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Count Pulse Input (Active Rising Edge)
P_{0-3}	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U}/D$	Up/Down Count Control Input
Q_{0-3}	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Clock Output (Active HIGH)

$\overline{RC}$ TRUTH TABLE

INPUTS			OUTPUT
$\overline{CE}$	TC[1]	CP	$\overline{RC}$
L	H	⊔	⊔
H	X	X	H
X	L	X	H

NOTES:
1. TC is generated internally.
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care

TRUTH TABLES
MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Preset (Asynch.)
H	H	X	X	No Change (Hold)

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT191					IDT54/74FCT191A					UNIT
			TYP.(3)	MIL. MIN.(2)	MIL. MAX.	COM'L. MIN.(2)	COM'L. MAX.	TYP.(3)	MIL. MIN.(2)	MIL. MAX.	COM'L. MIN.(2)	COM'L. MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		8.5	1.5	16.0	2.5	12.0	5.5	1.5	10.5	2.5	7.8	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		10.0	2.0	16.0	3.0	14.0	6.5	2.0	10.5	3.0	9.1	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$		5.5	1.5	12.5	2.5	8.5	3.6	1.5	8.2	2.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$		5.5	2.0	8.5	2.0	8.0	3.6	2.0	5.6	2.0	5.2	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$		11.0	4.0	22.5	4.0	20.0	7.2	4.0	14.7	4.0	13.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to TC		7.0	3.0	13.0	3.0	11.0	4.6	3.0	8.5	3.0	7.2	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		10.0	1.5	16.0	2.0	14.0	6.5	1.5	10.4	2.0	9.1	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		9.0	3.0	14.0	3.0	13.0	5.9	3.0	9.1	3.0	8.5	ns
t_{SU}(H) t_{SU}(L)	Setup Time HIGH or LOW P_n to $\overline{PL}$	C_L = 50pF R_L = 500Ω	4.5	6.0	–	5.0	–	4.0	5.0	–	4.0	–	ns
t_H (H) t_H (L)	Hold Time HIGH or LOW P_n to $\overline{PL}$		2.0	1.5	–	1.5	–	1.5	1.5	–	1.5	–	ns
t_{SU}(L)	Setup Time LOW $\overline{CE}$ to CP		10.0	10.5	–	10.0	–	9.0	9.5	–	9.0	–	ns
t_H (L)	Hold Time LOW $\overline{CE}$ to CP		0	0	–	0	–	0	0	–	0	–	ns
t_{SU}(H) t_{SU}(L)	Setup Time HIGH or LOW $\overline{U}$/D to CP		12.0	12.0	–	12.0	–	10.0	10.0	–	10.0	–	ns
t_H (H) t_H (L)	Hold Time HIGH or LOW $\overline{U}$/D to CP		0	0	–	0	–	0	0	–	0	–	ns
t_W(L)	$\overline{PL}$ Pulse Width LOW		6.0	8.5	–	6.0	–	5.5	8.0	–	5.5	–	ns
t_W(L)	CP Pulse Width LOW		5.0	7.0	–	5.0	–	4.0	6.0	–	4.0	–	ns
t_{REM}	Recovery Time $\overline{PL}$ to CP		6.0	7.5	–	6.0	–	5.0	6.5	–	5.0	–	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT (Temp. Range) XXXX (Device Type) X (Package) X (Process)

Process	Blank	Commercial
	B	MIL-STD-883, Class B
Package	D	CERDIP
	E	CERPACK
	SO	Small Outline IC
	L	Leadless Chip Carrier
Device Type	191	Up/Down Binary Counter
	191A	Fast Up/Down Binary Counter
Temp. Range	54	-55°C to +125°C
	74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS UP/DOWN BINARY COUNTERS

IDT54/74FCT193
IDT54/74FCT193A

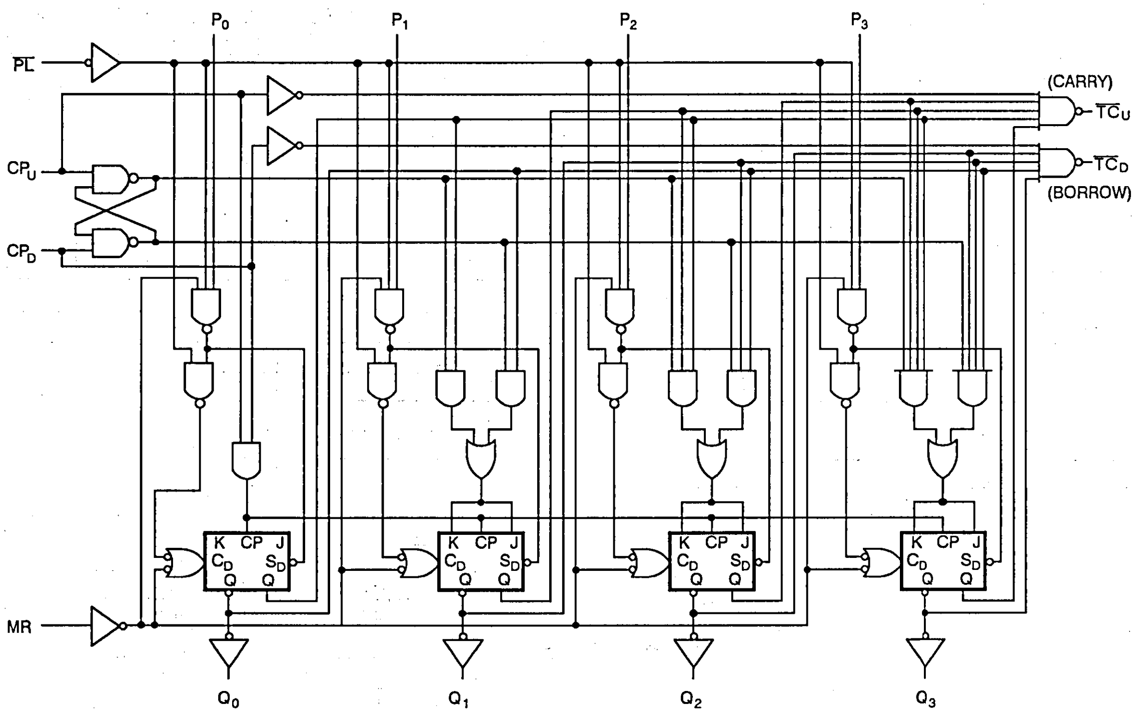
FEATURES:

- IDT54/74FCT193 equivalent to FAST ™ speed; **IDT54/74FCT193A 35% faster than FAST ™**
- Equivalent to FAST ™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST ™ (5μA max.)
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT193 and IDT54/74FCT193A are up/down modulo-16 binary counters built using advanced CEMOS ™, a dual metal CMOS technology. Separate count-up and count-down clocks are used and, in either counting mode, the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate terminal count-up and terminal count-down outputs are provided that are used as the clocks for subsequent stages without extra logic, thus simplifying multiusage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

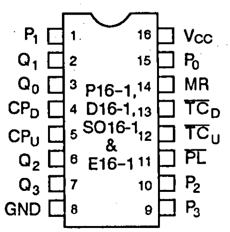
FUNCTIONAL BLOCK DIAGRAM



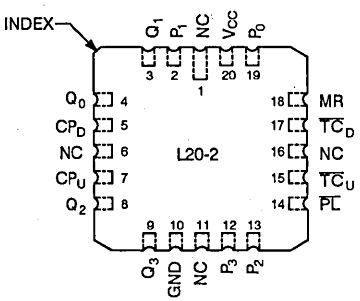
10

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.,(3) V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP_U} = f_{CP_D} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open Preset Mode $\overline{PL}$ = MR = CP_U = CP_D = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current (6)	V_{CC} = Max. Outputs Open Preset Mode $\overline{PL}$ = MR = CP_U = CP_D = GND Four Bits Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5(5)	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	4.0	10.5(5)	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0V$, +25°C ambient and maximum loading.
3. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CP_U	Count Up Clock Input (Active Rising Edge)
CP_D	Count Down Clock Input (Active Rising Edge)
MR	Asynchronous Master Reset (Active HIGH)
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
P_{0-3}	Parallel Data Inputs
Q_{0-3}	Flip-flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)

FUNCTION TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↑	H	Count Up
L	H	H	↑	Count Down

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT193					IDT54/74FCT193A					UNIT
			TYP.(3)	MIL.		COM'L.		TYP.(3)	MIL.		COM'L.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D $\overline{TC}_U$ or $\overline{TC}_D$	C_L = 50pF R_L = 500Ω	7.0	2.0	10.5	2.0	10.0	4.6	2.0	6.9	2.0	6.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n		9.5	2.0	14.0	2.0	13.5	6.2	2.0	9.1	2.0	8.8	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		11.0	2.0	16.5	2.0	15.5	7.2	2.0	10.8	2.0	10.1	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		10.0	2.0	13.5	2.0	14.0	6.5	2.0	9.1	2.0	8.8	ns
t_{PHL}	Propagation Delay MR to Q_n		11.0	3.0	16.0	3.0	15.5	7.0	3.0	10.4	3.0	10.1	ns
t_{PLH}	Propagation Delay MR to $\overline{TC}_U$		10.5	3.0	15.0	3.0	14.5	6.5	3.0	9.8	3.0	9.4	ns
t_{PHL}	Propagation Delay MR to $\overline{TC}_D$		11.5	3.0	16.0	3.0	15.5	7.5	3.0	10.4	3.0	10.1	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$		12.0	3.0	18.5	3.0	16.5	8.0	3.0	12.0	3.0	10.8	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$		11.5	3.0	16.5	3.0	15.5	7.5	3.0	10.8	3.0	10.1	ns
$t_{SU}(H)$ $t_{SU}(L)$	Set-up Time, HIGH or LOW P_n to $\overline{PL}$		4.5	6.0	—	5.0	—	4.0	5.0	—	4.0	—	ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW P_n to $\overline{PL}$		2.0	2.0	—	2.0	—	1.5	1.5	—	1.5	—	ns
$t_W(L)$	$\overline{PL}$ Pulse Width, LOW		6.0	7.5	—	6.0	—	5.0	6.5	—	5.0	—	ns
$t_W(L)$	CP_U or CP_D Pulse Width, LOW		5.0	7.0	—	5.0	—	4.0	6.0	—	4.0	—	ns
$t_W(L)$	CP_U or CP_D Pulse Width, LOW (Change of Direction)		10.0	12.0	—	10.0	—	8.0	10.0	—	8.0	—	ns
$t_W(H)$	MR Pulse Width, HIGH		6.0	6.0	—	6.0	—	5.0	5.0	—	5.0	—	ns
t_{REM}	Recovery Time $\overline{PL}$ to CP_U or CP_D		6.0	8.0	—	6.0	—	5.0	7.0	—	5.0	—	ns
t_{REM}	Recovery Time MR to CP_U or CP_D		4.0	4.5	—	4.0	—	3.0	3.5	—	3.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = –5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT	XXXX	X	X
Temp. Range	Device Type	Package	Process

Field	Code	Description
Process	Blank	Commercial
	B	MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	SO	Small Outline IC
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	193	Up/Down Binary Counter
	193A	Fast Up/Down Binary Counter
Temp. Range	54	-55°C to +125°C
	74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74FCT240/A

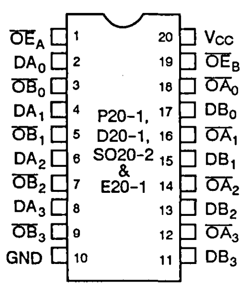
FEATURES:

- IDT54/74FCT240 equivalent to FAST™ speed; **IDT54/74FCT240A 40% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal buffer/line driver with 3-state output
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87655 is listed on this function. Refer to Section 2/page 2-4.

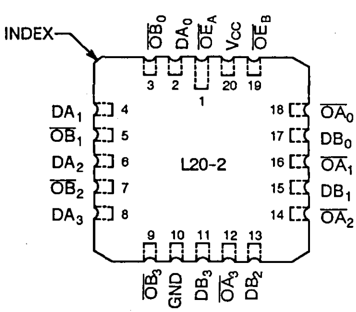
DESCRIPTION:

The IDT54/74FCT240/A are octal buffer/line drivers built using advanced CEMOS™, a dual metal CMOS technology. The devices are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitter/receivers which provide improved board density.

PIN CONFIGURATIONS

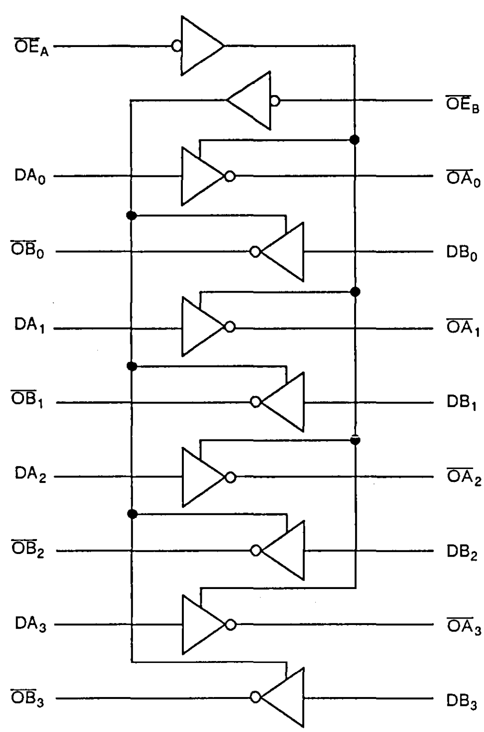


DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTES:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10[4]	
			V_O = 0.5V	–	–	-10[4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS FOR 'FCT240

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_I = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A = \overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$[6] $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V[6] V_{IN} = GND	–	5.0	14.5[5]	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
D_{xx}	Inputs
$\bar{O}_{xx}$	Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT240					IDT54/74FCT240A					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to $\bar{O}_n$	$C_L = 50pF$ $R_L = 500\Omega$	5.0	1.5	8.0	1.5	9.0	3.5	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		7.0	1.5	10.0	1.5	10.5	4.8	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		6.0	1.5	9.5	1.5	12.5	4.3	1.5	5.6	1.5	5.9	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT — Temp. Range; A — Device Type; X — Package; X — Process

Process	Blank	Commercial
	B	MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	SO	Small Outline IC
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	240	Inverting Octal Buffer/Line Driver
	240A	Fast Inverting Octal Buffer/Line Driver
Temp. Range	54	–55°C to +125°C
	74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74FCT241/A IDT54/74FCT244/A

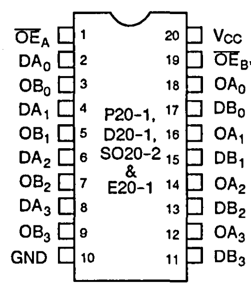
FEATURES:

- IDT54/74FCT241/244 equivalent to FAST™ speed; **IDT54/74FCT241A/244A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (Commercial), 48mA (Military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal buffer/line driver with 3-state output
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87630 is listed on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

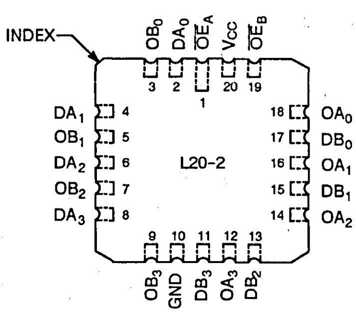
The IDT54/74FCT241/244 and IDT54/74FCT241A/244A are octal buffer/line drivers built using advanced CEMOS™, a dual metal CMOS technology. The devices are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitter/ receivers which provide improved board density.

PIN CONFIGURATIONS



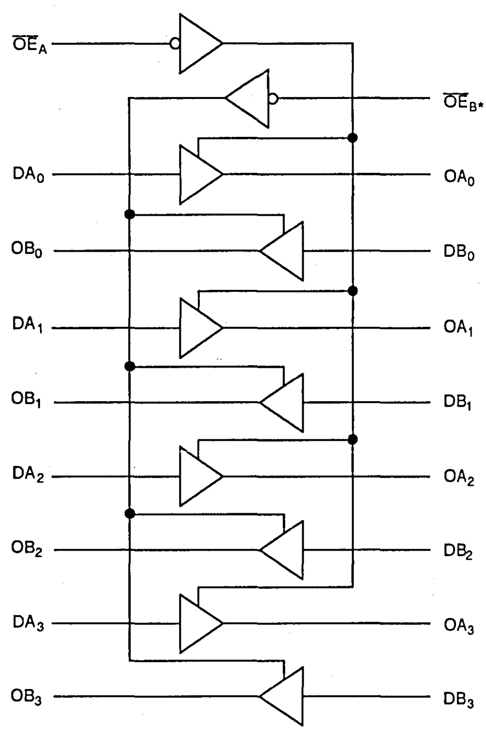
DIP/SOIC/CERPACK TOP VIEW

*OE_B for 'FCT241
$\overline{OE}_B$ for 'FCT244



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10[4]	
			V_O = 0.5V	–	–	-10[4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300µA	V_{HC}	V_{CC}	–	
			I_{OH} = −12mA MIL.	2.4	4.3	–	
			I_{OH} = −15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS FOR 'FCT241

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_I = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = OE_B = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle $\overline{OE}_A$ = OE_B = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle $\overline{OE}_A$ = OE_B = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$[6] $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V[6] V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC}\ D_H N_T + I_{CCD}\ (f_{CP}/2 + f_I\ N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

POWER SUPPLY CHARACTERISTICS FOR 'FCT244

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_I = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open $\overline{OE}_A = \overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current(6)	V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$(6) $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5(5)	
			V_{IN} = 3.4V(6) V_{IN} = GND	–	5.0	14.5(5)	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$[1]	3-State Output Enable Input (Active LOW)
D_{xx}	Inputs
O_{xx}	Outputs

NOTE:
1. For 'FCT241 use OE_B, and for 'FCT244 use $\overline{OE}_B$.

TRUTH TABLE FOR 'FCT241

INPUTS			OUTPUT
$\overline{OE}_A$,	OE_B	D	
L	H	L	L
L	H	H	H
H	L	X	Z

TRUTH TABLE FOR 'FCT244

INPUTS		OUTPUT
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR 'FCT241

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT241					IDT54/74FCT241A[4]					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	C_L = 50pF R_L = 500Ω	4.0	1.5	6.5	1.5	7.0	3.0	1.5	4.5	1.5	4.8	ns
t_{PZH} t_{PZL}	Output Enable Time		5.5	1.5	8.0	1.5	8.5	4.0	1.5	5.6	1.5	6.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time		4.5	1.5	7.0	1.5	7.5	3.0	1.5	5.0	1.5	5.5	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
4. These numbers are preliminary only.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR 'FCT244

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT244					IDT54/74FCT244A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	C_L = 50pF R_L = 500Ω	4.5	1.5	6.5	1.5	7.0	3.1	1.5	4.3	1.5	4.6	ns
t_{PZH} t_{PZL}	Output Enable Time		6.0	1.5	8.0	1.5	8.5	3.8	1.5	5.2	1.5	5.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		5.0	1.5	7.0	1.5	7.5	3.3	1.5	4.6	1.5	4.9	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT	A	X	X
Temp. Range	Device Type	Package	Process

Process

Blank	Commercial
B	MIL-STD-883, Class B

Package

P	Plastic DIP
D	CERDIP
SO	Small Outline IC
L	Leadless Chip Carrier
E	CERPACK

Device Type

241	Octal Buffer/Line Driver
241A	Fast Octal Buffer/Line Driver
244	Octal Buffer/Line Driver
244A	Fast Octal Buffer/Line Driver

Temp. Range

54	–55°C to +125°C
74	0°C to +70°C

FAST CMOS NON-INVERTING BUFFER TRANSCEIVER

IDT54/74FCT245
IDT54/74FCT245A

Integrated Device Technology, Inc.

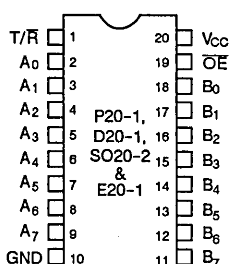
FEATURES:

- IDT54/74FCT245 equivalent to FAST™ speed; **IDT54/74FCT245A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial) and 48mA (military) for both ports
- CMOS power levels (5µW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5µA max.)
- Non-inverting buffer transceiver
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87629 is listed on this function. Refer to Section 2/page 2-4.

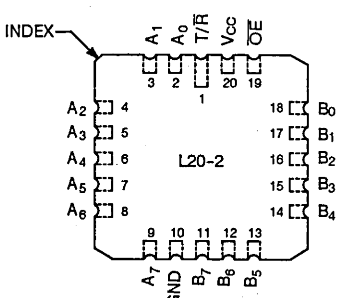
DESCRIPTION:

The IDT54/74FCT245 and IDT54/74FCT245A are 8-bit non-inverting, bidirectional buffers built using advanced CEMOS™, a dual metal CMOS technology. These bidirectional buffers have 3-state outputs and are intended for bus-oriented applications. The Transmit/Receive (T/R̄) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports. Receive (active LOW) enables data from B ports to A ports. The Output Enable (O̅E̅) Input, when HIGH, disables both A and B ports by placing them in High Z condition.

PIN CONFIGURATIONS

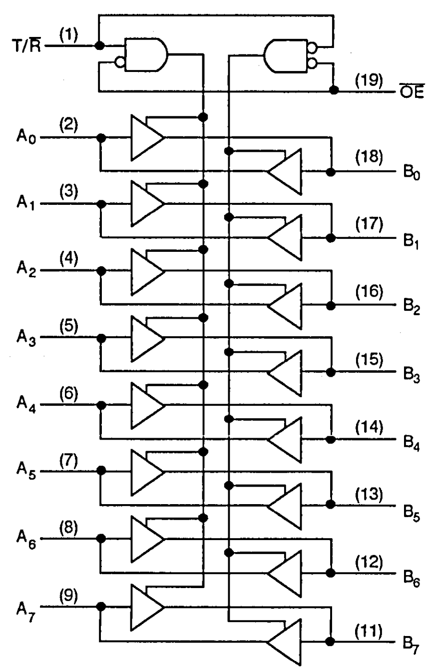


DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15[4]	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15[4]	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage (Port A and Port B)	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

10

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$[6] $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V[6] V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
$T/\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-State Outputs
B_0–B_7	Side B Inputs or 3-State Outputs

TRUTH TABLE

INPUTS		OUTPUTS
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT245					IDT54/74FCT245A					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A		5.0	1.5	7.0	1.5	7.5	3.3	1.5	4.6	1.5	4.9	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		6.0	1.5	9.5	1.5	10.0	4.8	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B	C_L = 50pF R_L = 500Ω	6.0	1.5	7.5	1.5	10.0	4.5	1.5	5.0	1.5	6.0	ns
t_{PZH} t_{PZL}	Output Enable Time $T/\overline{R}$ to A or B(4)		6.0	1.5	9.5	1.5	10.0	4.8	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Enable Time $T/\overline{R}$ to A or B(4)		6.0	1.5	7.5	1.5	10.0	4.5	1.5	5.0	1.5	6.0	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
4. This parameter is guaranteed but not tested.

ORDERING INFORMATION

IDTXXFCT	XXXX	X	X
Temp. Range	Device Type	Package	Process

Process

Blank	Commercial
B	MIL-STD-883, Class B

Package

P	Plastic DIP
D	CERDIP
SO	Small Outline IC
L	Leadless Chip Carrier
E	CERPACK

Device Type

245	Non-inverting Buffer Transceiver
245A	Fast Non-inverting Buffer Transceiver

Temp. Range

54	-55°C to +125°C
74	0°C to +70°C

10

Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH CLEAR

IDT54/74FCT273
IDT54/74FCT273A

FEATURES:

- IDT54/74FCT273 equivalent to FAST™ speed; **IDT54/74FCT273A 45% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5µW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5µA max.)
- Octal D flip-flop with clear
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87656 is listed on this function. Refer to Section 2/page 2-4.

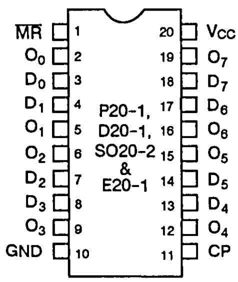
DESCRIPTION:

The IDT54/74FCT273 and IDT54/74FCT273A are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT273 and IDT54/74FCT273A have eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

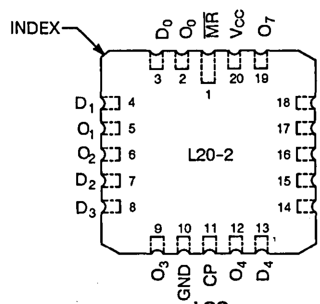
The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

PIN CONFIGURATIONS

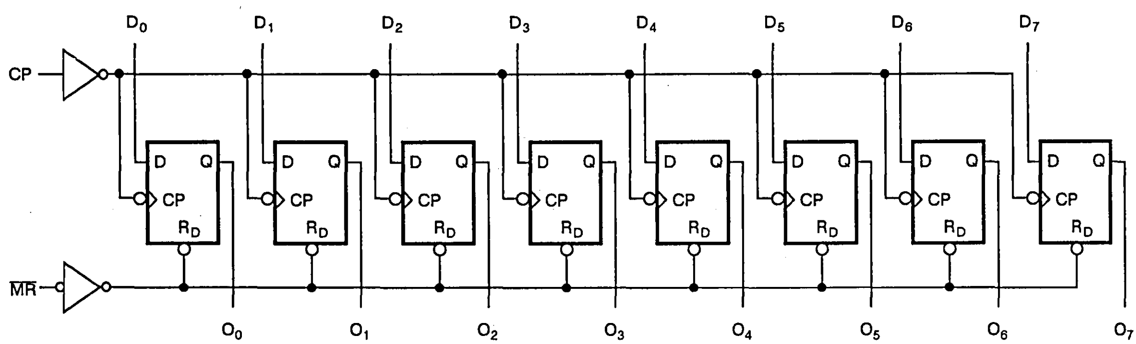


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = – 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	–	
			I_{OH} = –12mA MIL.	2.4	4.3	–	
			I_{OH} = –15mA COM'L.	2.4	4.3	–	
V_{OL}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current (4)	V_{CC} = Max. Outputs Open $\overline{MR} = V_{CC}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current (6)	V_{CC} = Max. Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{MR} = V_{CC}$ One Bit Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{MR} = V_{CC}$ Eight Bits Toggling f_I = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8(5)	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	16.8(5)	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$D_0 - D_7$	Data Inputs
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
$O_0 - O_7$	Data Outputs

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUT
	$\overline{MR}$	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

H = HIGH voltage steady state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady rate
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't Care
↑ = LOW-to-HIGH clock transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT273					IDT54/74FCT273A					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Clock to Output		7.0	2.0	13.0	2.0	15.0	5.0	2.0	7.2	2.0	8.3	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output		8.0	2.0	13.0	2.0	15.0	5.0	2.0	7.2	2.5	8.3	ns
t_{SU}	Set-up Time HIGH or LOW Data to CP		3.0	3.0	–	3.5	–	1.0	2.0	–	2.0	–	ns
t_H	Hold Time HIGH or LOW Data to CP	C_L = 50pF R_L = 500Ω	1.0	2.0	–	2.0	–	1.0	1.5	–	1.5	–	ns
t_W	Clock Pulse Width HIGH or LOW		4.0	7.0	–	7.0	–	3.0	6.0	–	6.0	–	ns
t_W	$\overline{MR}$ Pulse Width HIGH or LOW		4.0	7.0	–	7.0	–	3.0	6.0	–	6.0	–	ns
t_{REM}	Recovery Time $\overline{MR}$ to CP		3.0	4.0	–	5.0	–	1.5	2.0	–	2.5	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT XXXX X X
Temp. Range Device Type Package Process

Process	Blank	Commercial
	B	MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	SO	Small Outline IC
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	273	Octal D Flip-Flop w/Clear
	273A	Fast Octal D Flip-Flop w/Clear
Temp. Range	54	-55°C to +125°C
	74	0°C to +70°C

10

Integrated Device Technology, Inc.

FAST CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54/74FCT299
IDT54/74FCT299A

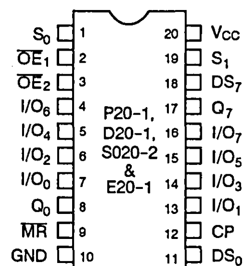
FEATURES:

- IDT54/74FCT299 equivalent to FAST™ speed; **IDT54/74FCT299A 25% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5µW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5µA max.)
- 8-input universal shift register
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86862 is listed on this function. Refer to Section 2/page 2-4.

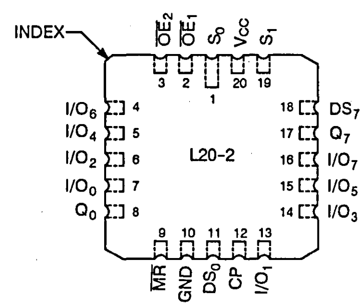
DESCRIPTION:

The IDT54/74FCT299 and IDT54/74FCT299A are built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT299 and IDT54/74FCT299A are 8-input universal shift/storage registers with 3-state outputs. Four modes of operation are possible; hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0-Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

PIN CONFIGURATIONS

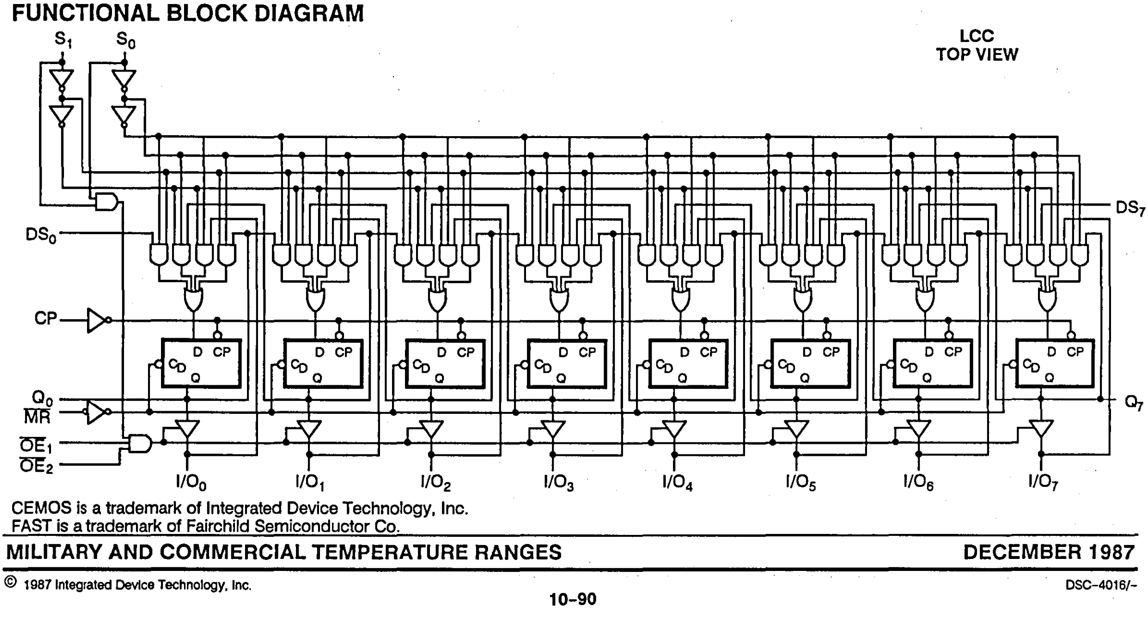


DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Currents (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15[4]	
I_{IL}	Input LOW Currents (I/O pins only)		V_I = 0.5V	–	–	-15[4]	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300µA	V_{HC}	V_{CC}	–	
			I_{OH} = −12mA MIL.	2.4	4.3	–	
			I_{OH} = −15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC}= 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR} = V_{CC}$ $S_0 = S_1 = V_{CC}$ $DS_0 = DS_1$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 1.0MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR} = V_{CC}$ $S_0 = S_1 = V_{CC}$ $DS_0 = DS_7$ = GND One Bit Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR} = V_{CC}$ $S_0 = S_1 = V_{CC}$ $DS_0 = DS_7$ = GND Eight Bits Toggling at f_I = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	6.0	16.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CP	Clock Pulse Input (Active Edge Rising)
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_7	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)
I/O_0 – I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
Q_0, Q_7	Serial Outputs

TRUTH TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset Q_0–Q_7 = LOW
H	H	H	↑	Parallel Load; I/O $\rightarrow Q_n \rightarrow Q_n$
H	L	H	↑	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↑	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT299					IDT54/74FCT299A					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7		7.0	2.5	10.0	2.5	14.0	5.0	2.5	7.2	2.5	9.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		6.0	2.5	12.0	2.5	12.0	5.0	2.5	7.2	2.5	9.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		7.0	2.5	10.0	2.5	10.5	5.0	2.5	7.2	2.5	9.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n		7.0	2.5	15.0	2.5	15.0	6.0	2.5	8.7	2.5	11.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n		8.0	1.5	11.0	1.5	15.0	5.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n		5.5	1.5	7.0	1.5	9.0	4.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW S_0 or S_1 to CP	C_L = 50pF R_L = 500Ω	2.0	8.5	–	8.5	–	2.5	4.0	–	5.0	–	ns
t_H	Hold Time HIGH or LOW S_0 or S_1 to CP		0	0	–	0	–	-1.5	0	–	0	–	ns
t_{SU}	Set-up Time HIGH or LOW I/O_n, DS_0 or DS_7 to CP		0.5	5.5	–	5.5	–	2.5	4.0	–	5.0	–	ns
t_H	Hold Time HIGH or LOW I/O_n, DS_0 or DS_7 to CP		0	2.0	–	2.0	–	1.0	2.0	–	2.0	–	ns
t_W	CP Pulse Width HIGH or LOW		7.0	7.0	–	7.0	–	4.0	5.0	–	6.0	–	ns
t_W	$\overline{MR}$ Pulse Width LOW		7.0	7.0	–	7.0	–	4.0	5.0	–	6.0	–	ns
t_{REM}	Recovery Time $\overline{MR}$ to CP		7.0	7.0	–	7.0	–	4.0	5.0	–	6.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT XXXX X X
Temp. Range / Device Type / Package / Process

Field	Code	Description
Process	Blank	Commercial
	B	MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	SO	Small Outline IC
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	299	8-Input Universal Shift Register
	299A	Fast 8-Input Universal Shift Register
Temp. Range	54	-55°C to +125°C
	74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSPARENT LATCH

IDT54/74FCT373
IDT54/74FCT373A

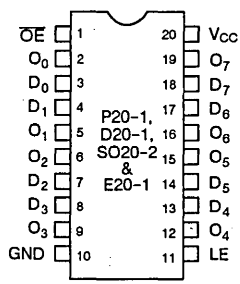
FEATURES:

- IDT54/74FCT373 equivalent to FAST™ speed; **IDT54/74FCT373A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal transparent latch with enable
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87644 is listed on this function. Refer to Sction 2/page 2-4.

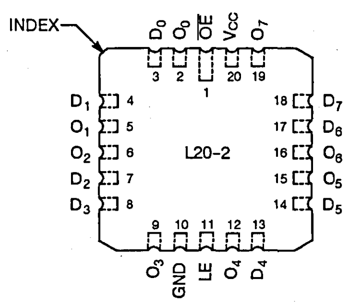
DESCRIPTION:

The IDT54/74FCT373 and IDT54/74FCT373A are 8-bit latches built using advanced CEMOS™, a dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus-oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS

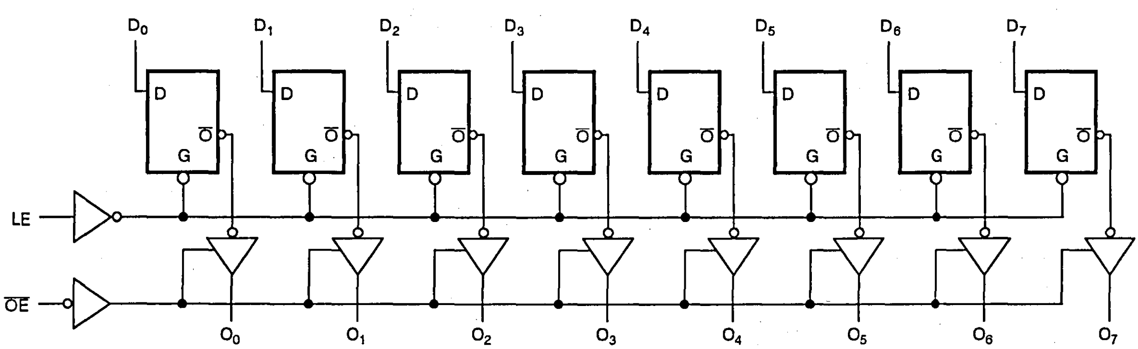


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10[4]	
			V_O = 0.5V	–	–	-10[4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_I = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

10

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$D_0 - D_7$	Data Inputs
LE	Latch Enables Input (Active HIGH)
$\overline{OE}$	Output Enables Input (Active LOW)
$O_0 - O_7$	3-State Latch Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT373					IDT54/74FCT373A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	$C_L = 50pF$ $R_L = 500\Omega$	5.0	1.5	8.0	1.5	8.5	4.0	1.5	5.2	1.5	5.6	ns
t_{PZH} t_{PZL}	Output Enable Time		7.0	1.5	12.0	1.5	13.5	5.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		6.0	1.5	7.5	1.5	10.0	4.0	1.5	5.5	1.5	6.5	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n		9.0	2.0	13.0	2.0	15.0	7.0	2.0	8.5	2.0	9.8	ns
t_{SU}	Set-up Time HIGH or LOW D_n to LE		1.0	2.0	–	2.0	–	1.0	2.0	–	2.0	–	ns
t_H	Hold Time HIGH or LOW D_n to LE		1.0	1.5	–	1.5	–	1.0	1.5	–	1.5	–	ns
t_W	LE Pulse Width HIGH or LOW		5.0	6.0	–	6.0	–	4.0	5.0	–	6.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at $V_{CC} = 5.0V$, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT XXXX X X
Temp. Range Device Type Package Process

Field	Code	Description
Process	Blank	Commercial
	B	MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	SO	Small Outline IC
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	373	Octal Transparent Latch
	373A	Fast Octal Transparent Latch
Temp. Range	54	-55°C to +125°C
	74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTER (3-STATE)

IDT54/74FCT374
IDT54/74FCT374A

FEATURES:

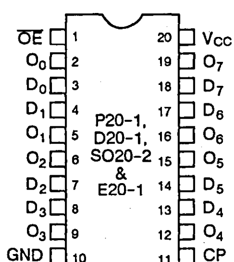
- IDT54/74FCT374 equivalent to FAST™ speed; **IDT54/74FCT374A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5µW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5µA max.)
- Positive, edge-triggered Master/Slave, D-type flip-flops
- Buffered common clock and buffered common three-state control
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87628 is listed on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

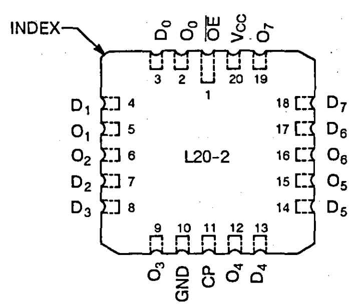
The IDT54/74FCT374 and IDT54/74FCT374A are 8-bit registers built using advanced CEMOS™, a dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state conditions.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

PIN CONFIGURATIONS

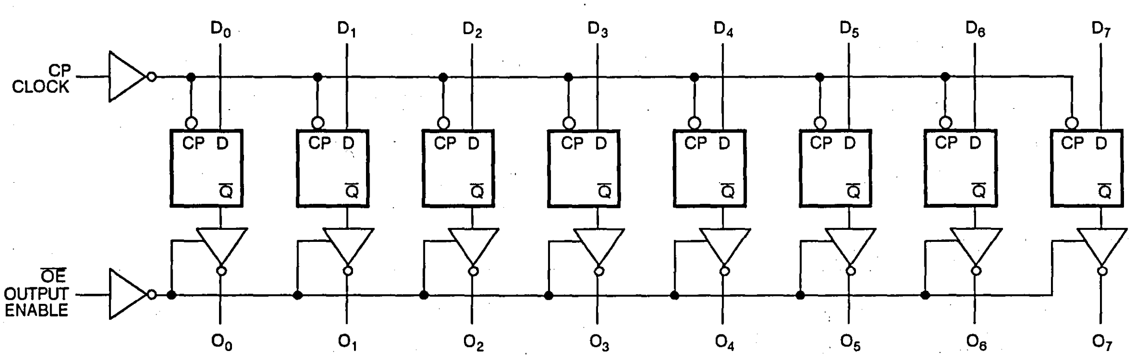


DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER [1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP. [2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	μA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	μA
			V_O = 2.7V	–	–	10[4]	
			V_O = 0.5V	–	–	-10[4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300μA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_{CP} = f_I = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_I = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	16.8[5]	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_I	The D flip-flop data inputs.
CP	Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
O_I	The register three-state outputs.
$\overline{OE}$	Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CLOCK	D_I	O_I	$\overline{Q}_I$
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↑	L	L	H
	L	↑	H	H	L
	H	↑	L	Z	H
	H	↑	H	Z	L

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
NO = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT374					IDT54/74FCT374A					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	$C_L = 50pF$ $R_L = 500\Omega$	6.6	2.0	10.0	2.0	11.0	4.5	2.0	6.5	2.0	7.2	ns
t_{PZH} t_{PZL}	Output Enable Time		9.0	1.5	12.5	1.5	14.0	5.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		6.0	1.5	8.0	1.5	8.0	4.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW D_n to CP		1.0	2.0	–	2.5	–	1.0	2.0	–	2.0	–	ns
t_H	Hold Time HIGH or LOW D_n to CP		0.5	2.0	–	2.0	–	0.5	1.5	–	1.5	–	ns
t_W	CP Pulse Width HIGH or LOW		4.0	7.0	–	7.0	–	4.0	5.0	–	6.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at $V_{CC} = 5.0V$, $+25°C$ ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT XXXX X X
Temp. Range / Device Type / Package / Process/Temperature Range

Process/Temperature Range	Blank	Commercial
	B	MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	SO	Small Outline IC
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	374	Octal D Register (3-state)
	374A	Fast Octal D Register
Temp. Range	54	-55°C to +125°C
	74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT54/74FCT377
IDT54/74FCT377A

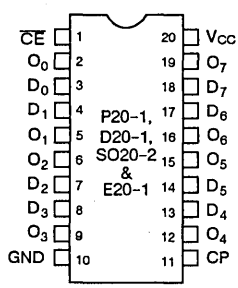
FEATURES:

- IDT54/74FCT377 equivalent to FAST™ speed; **IDT54/74FCT377A 45% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal D flip-flop with clock enable
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87627 is pending listing on this function. Refer to Section 2/page 2-4.

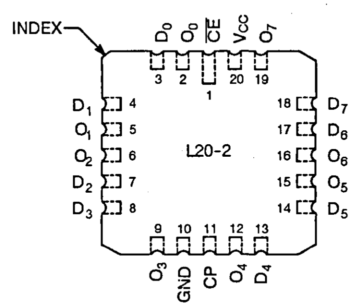
DESCRIPTION:

The IDT54/74FCT377 and IDT54/74FCT377A are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74AFCT377 and IDT54/74FCT377A have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

PIN CONFIGURATIONS

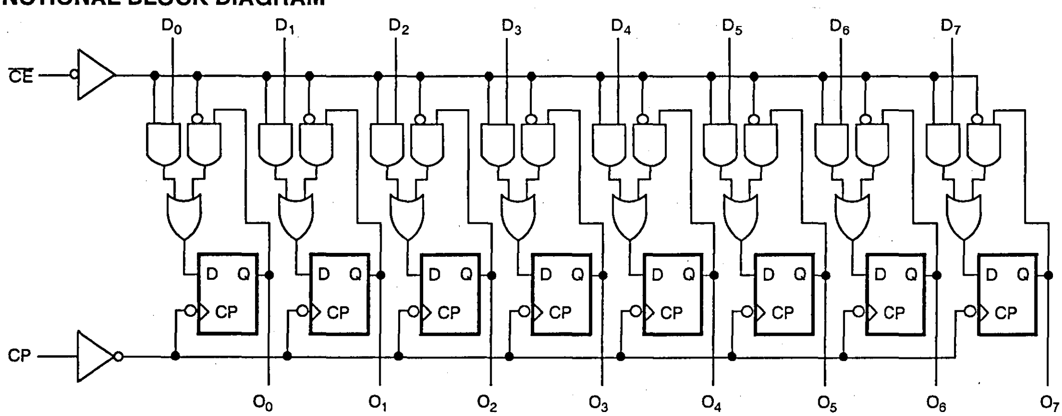


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-4019/-

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10[4]	
			V_O = 0.5V	–	–	-10[4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300µA	V_{HC}	V_{CC}	–	
			I_{OH} = −12mA MIL.	2.4	4.3	–	
			I_{OH} = −15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open $\overline{CE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current(6)	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CE}$ = GND One Bit Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{CE}$ = GND Eight Bits Toggling at f_I = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	3.75	7.8(5)	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	16.8(5)	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
O_0-O_7	Data Outputs
CP	Clock Pulse Input

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D	O
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑ X	h H	X X	No Change No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
↑ = LOW-to-HIGH Clock Transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT377					IDT54/74FCT377A					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$		7.0	2.0	13.0	2.0	15.0	5.0	2.0	7.2	2.0	8.3	ns
t_{SU}	Set-up Time HIGH or LOW D_n to CP		1.0	2.5	–	3.0	–	1.0	2.0	–	2.0	–	ns
t_H	Hold Time HIGH or LOW D_n to CP	C_L = 50pF R_L = 500Ω	1.0	2.0	–	2.5	–	1.0	1.5	–	1.5	–	ns
t_{SU}	Set-up Time HIGH or LOW $\overline{CE}$ to CP		1.5	3.0	–	3.0	–	1.0	2.0	–	2.0	–	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$ to CP		3.0	4.0	–	5.0	–	1.0	2.0	–	2.0	–	ns
t_W	Clock Pulse Width, LOW		4.0	7.0	–	7.0	–	4.0	6.0	–	7.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT (Temp. Range) XXXX (Device Type) X (Package) X (Process)

Process	Blank	Commercial
	B	MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	E	CERPACK
	SO	Small Outline IC
	L	Leadless Chip Carrier
Device Type	377	Octal D Flip-Flop w/Clock Enable
	377A	Fast Octal D Flip-Flop w/Clock Enable
Temp. Range	54	-55°C to +125°C
	74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS QUAD DUAL-PORT REGISTER

PRELIMINARY
IDT54/74FCT399
IDT54/74FCT399A

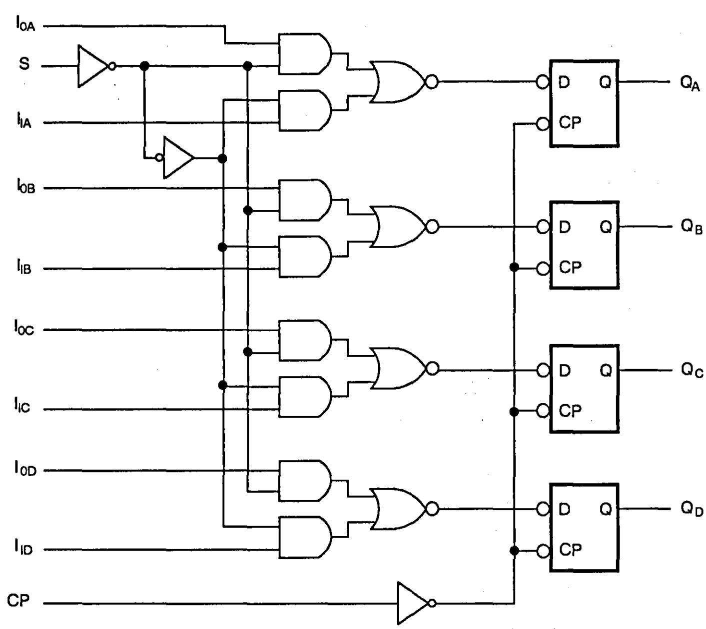
FEATURES:

- IDT54/74FCT399 equivalent to FAST™ speed; **IDT54/74FCT399A 30% faster than FAST™**
- Equivalent to FAST™ pinout/function and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 16-pin DIP and SOIC, and 20-pin LCC
- Military product compliant to MIL-STD-883, Class B
- Product available in Radiation Tolerant and Enhanced versions

DESCRIPTION:

Both these devices are high-speed quad dual-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0X}, I_{1X}) and Select input (S) must be stable only one set-up time prior to, and hold time after, the LOW-to-HIGH transition of the Clock input for predictable operation.

FUNCTIONAL BLOCK DIAGRAM

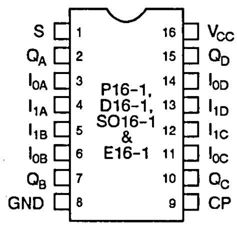


CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

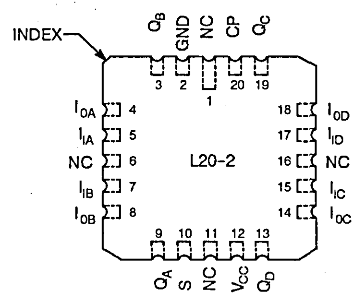
MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-4023/-

PIN CONFIGURATIONS

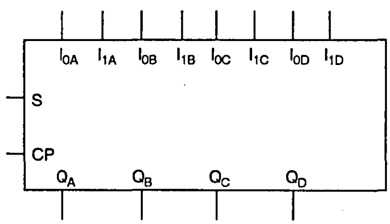


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN DESCRIPTION

PIN NAMES	DESCRIPTION
S	Common Select Input
CP	Clock Pulse Input (Active Rising Edge)
$I_{0A}-I_{0D}$	Data Inputs from Source 0
$I_{1A}-I_{1D}$	Data Inputs from Source 1
$Q_A - Q_D$	Register True Outputs

FUNCTIONAL TABLE

INPUTS			OUTPUTS
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

H = HIGH Voltage Level
L = LOW Voltage Level
h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
X = Immaterial

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle One Input Toggling at f_I = 5MHz 50% Duty Cycle S = Steady State	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle Four Inputs Toggling at f_I = 5MHz 50% Duty Cycle S = Steady State	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.75[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	5.0	12.75[5]	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITIONS(1)	IDT54FCT399					IDT54FCT399A					UNIT
				COM'L.		MIL.			COM'L.		MIL.		
			TYP.(3)	MIN.(2)	MAX.	MIN.(2)	MAX.	TYP.(3)	MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q or $\overline{Q}$	$C_L = 50pF$ $R_L = 500\Omega$	6.8	3.0	10.0	3.0	11.5	4.0	2.5	7.0	2.5	7.5	ns
t_{SU}	Set-Up Time HIGH or LOW I_n to CP		3.0	3.0	–	4.5	–	2.5	2.5	–	2.5	–	ns
t_H	Hold Time HIGH or LOW I_n to CP		1.0	1.0	–	1.5	–	1.0	1.0	–	1.0	–	ns
t_{SU}	Set-Up Time HIGH or LOW S to CP		–	8.5	–	9.5	–	–	6.0	–	6.0	–	ns
t_H	Hold Time HIGH or LOW S to CP		–	0	–	0	–	–	0	–	0	–	ns
t_W	CP Pulse Width, HIGH or LOW(4)		–	5.0	–	7.0	–	–	5.0	–	6.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V and +25°C ambient and maximum loading.
4. This parameter is guaranteed but not tested.

10

ORDERING INFORMATION

IDTXXFCT	XXXX	A	A
Temperature Range	Device Type	Package	Process

Process

Blank	Commercial
B	MIL-STD-883, Class B

Package

P	Plastic DIP
D	CERDIP
L	Leadless Chip Carrier
SO	Small Outline IC
E	CERPACK

Device Type

399	Quad Dual-Port Register
399A	FAST Quad Dual-Port Register

Temperature Range

54	-55°C to +125°C
74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS 8-BIT IDENTITY COMPARATOR

IDT54/74FCT521
IDT54/74FCT521A
IDT54/74FCT521B

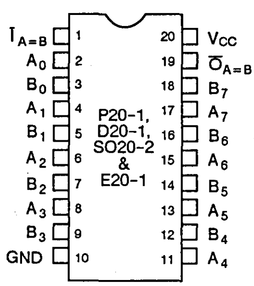
FEATURES:

- IDT54/74FCT521 15.0ns max. propagation delay; **IDT54/74FCT521A 9.3ns max. propagation delay** **IDT54/74FCT521B 7.3ns max. propagation delay**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST (5μA max.)
- 8-bit identity comparator
- Product available in Radiation Tolerant and Enhanced versions
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

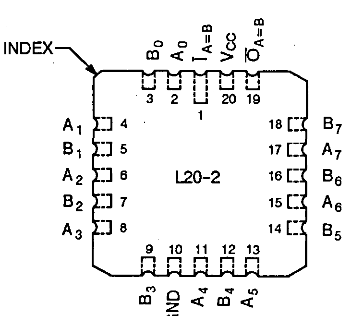
DESCRIPTION:

The IDT54/74FCT521/A/B are 8-bit identity comparators built using advanced CEMOS™, a dual metal CMOS technology. The devices compare two words of up to eight bits each and provide a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

PIN CONFIGURATIONS

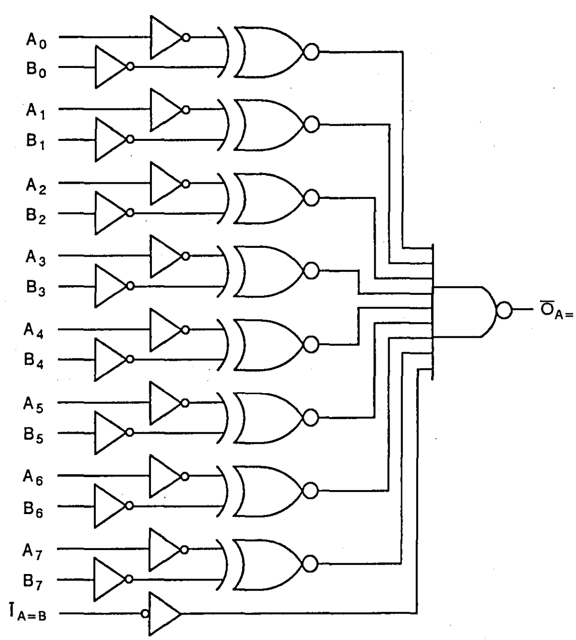


DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

10

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120		mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V^{(3)}$		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current (4)	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current (6)	V_{CC} = Max. Outputs Open f_I = 10MHz, 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	$4.0^{(5)}$	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	$4.8^{(5)}$	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$A_0 - A_7$	Word A Inputs
$B_0 - B_7$	Word B Inputs
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\overline{O}_{A=B}$	Identity Output (Active LOW)

TRUTH TABLE

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT521					IDT54/74FCT521A					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	C_L = 50pF R_L = 500Ω	7.0	1.5	11.0	1.5	15.0	5.5	1.5	7.2	1.5	9.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$		5.0	1.5	10.0	1.5	9.0	4.4	1.5	6.0	1.5	7.8	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (CONTINUED)

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT521B				UNIT
			COM'L.		MIL.		
			MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	C_L = 50pF R_L = 500Ω	1.5	5.5	1.5	7.3	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$		1.5	4.6	1.5	6.0	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT — Temp. Range
XXXX — Device Type
X — Package
X — Process

Blank	Commercial
B	MIL-STD-883, Class B
P	Plastic DIP
D	CERDIP
E	CERPACK
L	Leadless Chip Carrier
SO	Small Outline IC
521	8-Bit Comparator
521A	Fast 8-Bit Comparator
521B	Very Fast 8-Bit Comparator
54	-55°C to +125°C
74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSPARENT LATCH (3-STATE)

IDT54/74FCT533
IDT54/74FCT533A

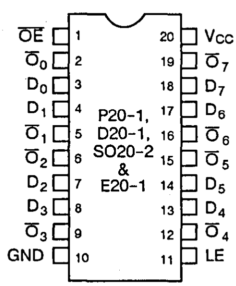
FEATURES:

- IDT54/74FCT533 10.0ns max. clock to output; **IDT54/74FCT533A 5.2ns max. clock to output**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal transparent latch with 3-state output
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

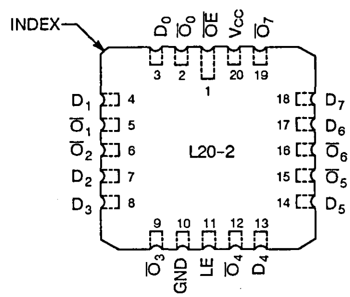
DESCRIPTION:

The IDT54/74FCT533 and IDT54/74FCT533A are octal transparent latches built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT533 and IDT54/74FCT533A consist of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS



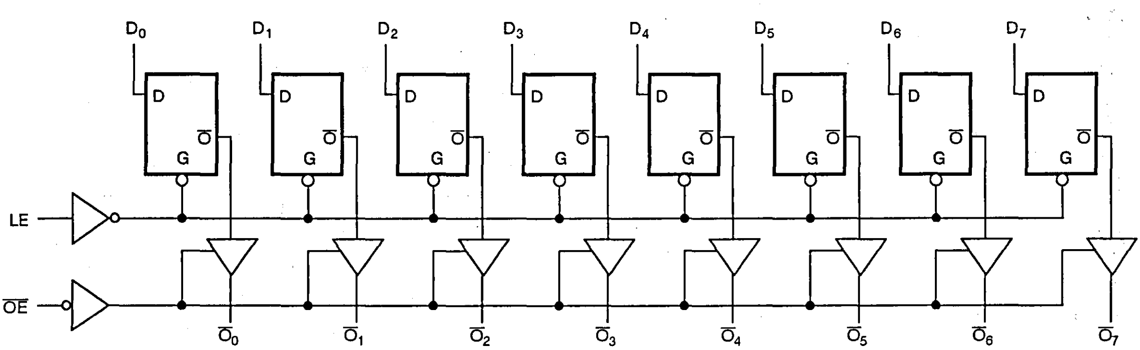
DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

10

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	μA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	μA
			V_O = 2.7V	–	–	10[4]	
			V_O = 0.5V	–	–	-10[4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300μA	V_{HC}	V_{CC}	–	
			I_{OH} = –12mA MIL.	2.4	4.3	–	
			I_{OH} = –15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current(6)	V_{CC} = Max. Outputs Open f_I = 10MHz, 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
		$\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5(5)	
		$\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	–	5.0	14.5(5)	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0V$, +25°C ambient and maximum loading.
3. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$D_0 - D_7$	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{O}_0 - \overline{O}_7$	Complementary 3-State Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	LE	$\overline{OE}$	$\overline{O}_n$
H	H	L	L
L	H	L	H
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance

10

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT533					IDT54/74FCT533A					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$		6.0	1.5	10.0	1.5	12.0	4.0	1.5	5.2	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$		9.0	2.0	13.0	2.0	14.0	7.0	2.0	8.5	2.0	9.8	ns
t_{PZH} t_{PZL}	Output Enable Time		8.0	1.5	11.0	1.5	12.5	5.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time	$C_L = 50pF$ $R_L = 500\Omega$	6.0	1.5	7.0	1.5	8.5	4.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW D_n to LE		1.0	2.0	–	2.0	–	1.0	2.0	–	2.0	–	ns
t_H	Hold Time HIGH or LOW D_n to LE		1.0	1.5	–	1.5	–	1.0	1.5	–	1.5	–	ns
t_W	LE Pulse Width HIGH or LOW		5.0	6.0	–	6.0	–	4.0	5.0	–	6.0	–	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT XXXX X X
Temp. Range / Device Type / Package / Process

Field	Code	Description
Process	Blank	Commercial
	B	MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	SO	Small Outline IC
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	533	Octal Transparent Latch (3-State)
	533A	Fast Octal Transparent Latch (3-State)
Temp. Range	54	-55°C to +125°C
	74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP (3-STATE)

IDT54/74FCT534
IDT54/74FCT534A

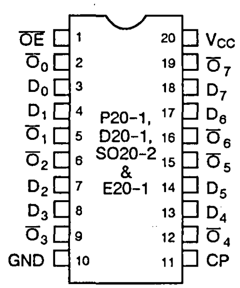
FEATURES:

- IDT54/74FCT534 10.0ns max. clock to output; **IDT54/74FCT534A 6.5ns max. clock to output**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal D flip-flop with 3-state output
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

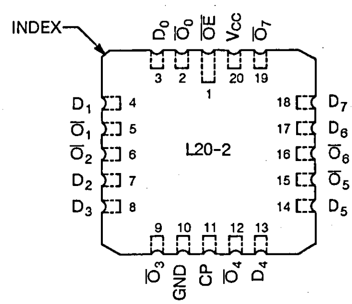
DESCRIPTION:

The IDT54/74FCT534 and IDT54/74FCT534A are octal D-type flip-flops built using IDT's advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT534 and IDT54/74FCT534A are high-speed, low-power octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

PIN CONFIGURATIONS

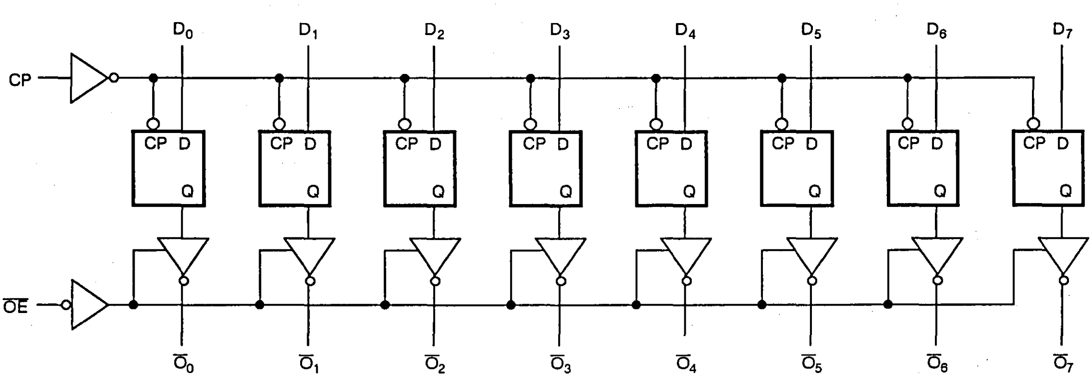


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	μA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	μA
			V_O = 2.7V	–	–	10(4)	
			V_O = 0.5V	–	–	-10(4)	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300μA	V_{HC}	V_{CC}	–	
			I_{OH} = −12mA MIL.	2.4	4.3	–	
			I_{OH} = −15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current (4)	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current (6)	V_{CC} = Max. Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_I = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8(5)	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	16.8(5)	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$D_0 - D_7$	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	3-State Output Enable Input (Active LOW)
$\overline{O}_0 - \overline{O}_7$	Complementary 3-State Outputs

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CP	D_I	$\overline{O}_I$	Q_I
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↑	L	H	L
	L	↑	H	L	H
	H	↑	L	Z	L
	H	↑	H	Z	H

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
NC = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT534					IDT54/74FCT534A					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	6.5	1.5	10.0	1.5	11.0	4.5	1.5	6.5	1.5	7.2	ns
t_{PZH} t_{PZL}	Output Enable Time		9.0	1.5	12.5	1.5	14.0	5.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		6.0	1.5	8.0	1.5	8.0	4.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW D_n to CP		1.0	2.0	–	2.5	–	1.0	2.0	–	2.0	–	ns
t_H	Hold Time HIGH or LOW D_n to CP		0.5	1.5	–	1.5	–	1.0	1.5	–	1.5	–	ns
t_W	CP Pulse Width HIGH or LOW		4.0	7.0	–	7.0	–	4.0	5.0	–	6.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT — Temp. Range
XXXX — Device Type
X — Package
X — Process/Temperature Range

Blank	Commercial
B	MIL-STD-883, Class B
P	Plastic DIP
D	CERDIP
SO	Small Outline IC
L	Leadless Chip Carrier
E	CERPACK
534	Octal D Flip-Flop (3-State)
534A	Fast Octal D Flip-Flop (3-State)
54	-55°C to +125°C
74	0°C to +70°C

FAST CMOS OCTAL BUFFER/ LINE DRIVER

PRELIMINARY
IDT54/74FCT540/A
IDT54/74FCT541/A

FEATURES:

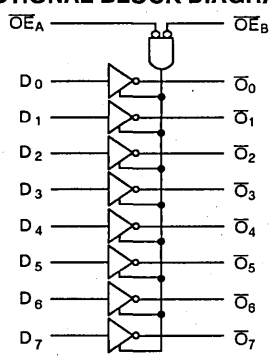
- IDT54/74FCT540/41 equivalent to FAST™ speed; **IDT54/74FCT540A/41A 30% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial), 48mA (military)
- Octal buffer/line driver with 3-state output
- Pinout arrangement for flow-through architecture
- CMOS power levels (5μW typ. static)
- Substantially lower input current levels than FAST™ (5μA max.)
- Available in CERDIP, Plastic DIP, LCC and SOIC
- TTL input and output level compatible
- CMOS output level compatible
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

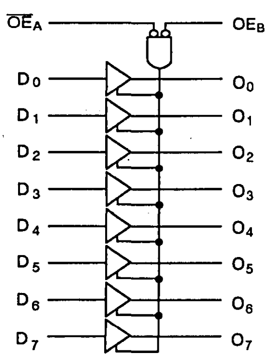
The IDT54/74FCT540/A and IDT54/74FCT541/A are octal buffer/line drivers built using advanced CEMOS™, a dual metal CMOS technology.

These devices are similar in function to the IDT54/74FCT240 and IDT54/74FCT241, respectively, except that the inputs and outputs are on opposite sides of the package. This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater board density.

FUNCTIONAL BLOCK DIAGRAM

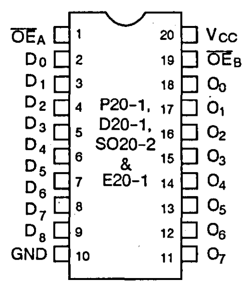


IDT54/74FCT540

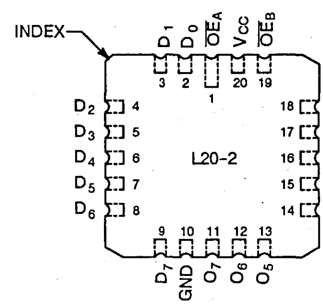


IDT54/74FCT541

PIN CONFIGURATIONS



DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
D_{XX}	Inputs
O_{XX}	Outputs

TRUTH TABLE

INPUTS		OUTPUT	
$\overline{OE}_A$, $\overline{OE}_B$	D	540	541
L	L	H	L
L	H	L	H
H	X	Z	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10[4]	
			V_O = 0.5V	–	–	-10[4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V^{(3)}$		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open $\overline{OE}_A = \overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current(6)	V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND Eight Inputs Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	$6.5^{(5)}$	
			V_{IN} = 3.4V V_{IN} = GND	–	5.0	$14.5^{(5)}$	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITIONS(1)	IDT54/74FCT540/541					IDT54/74FCT540A/541A					UNIT
				COM'L		MIL			COM'L		MIL		
			TYP.(3)	MIN.(2)	MAX.	MIN.(2)	MAX.	TYP.(3)	MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n IDT54/74FCT540	C_L = 50pF R_L = 500Ω	5.0	2.0	8.5	2.0	9.5	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n IDT54/74FCT541		5.0	2.0	8.0	2.0	9.0	–	–	–	–	–	ns
t_{PZH} t_{PZL}	Output Enable Time		7.0	2.0	10.0	2.0	10.5	–	–	–	–	–	ns
t_{PHZ} t_{PLZ}	Output Disable Time		6.0	2.0	9.5	2.0	12.5	–	–	–	–	–	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT XXXX A A

Field	Code	Description
Process	Blank	Commercial
	B	MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	E	CERPACK
	L	Leadless Chip Carrier
	SO	Small Outline IC
Device Type	540	Non-Inverting Octal Buffer/Line Driver
	541	Inverting Octal Buffer/Line Driver
	540A	Fast Non-inverting Octal Buffer/Line Driver
	541A	Fast Inverting Octal Buffer/Line Driver
Temperature Range	54	-55°C to +125°C
	74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS OCTAL REGISTERED TRANSCEIVER

PRELIMINARY
IDT54/74FCT543
IDT54/74FCT543A

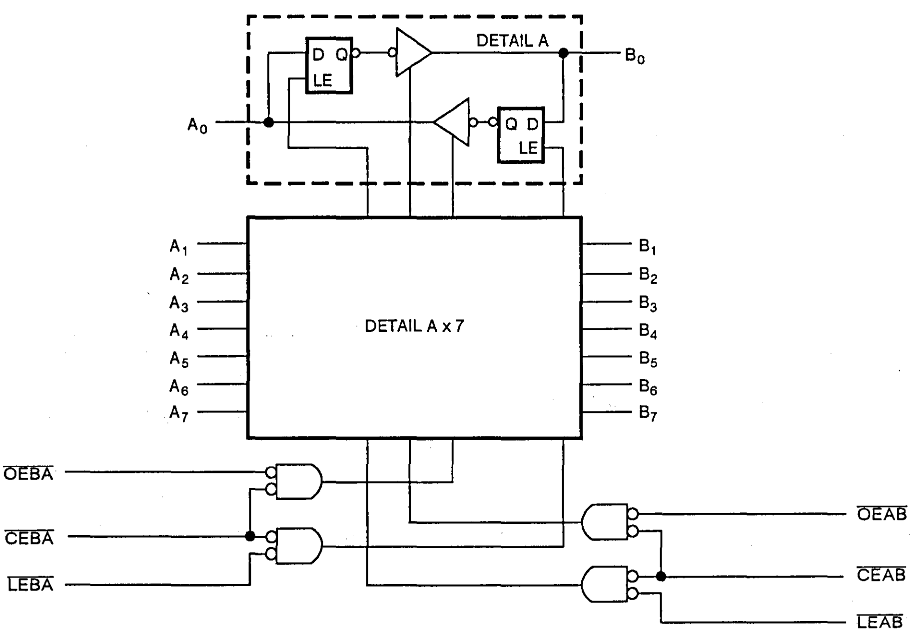
FEATURES:

- IDT54/74FCT543 equivalent to FAST™ speed; **IDT54/74FCT543A is 25% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial), 48mA (military)
- 8-bit octal latched transceiver
- Separate controls for data flow in each direction
- Back-to-back latches for storage
- CMOS power levels (5μW typ. static)
- Substantially lower input current levels than FAST™ (5μA max.)
- TTL input and output level compatible
- CMOS output level compatible
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

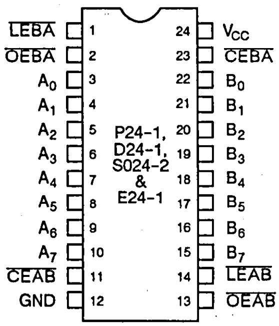
The IDT54/74FCT543 and IDT54/74FCT543A are non-inverting octal transceivers built using advanced CEMOS™, a dual metal CMOS technology. These devices contain two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0-A_7 or to take data from B_0-B_7, as indicated in the Truth Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEAB}$, $\overline{LEAB}$ and $\overline{OEAB}$ inputs.

FUNCTIONAL BLOCK DIAGRAM

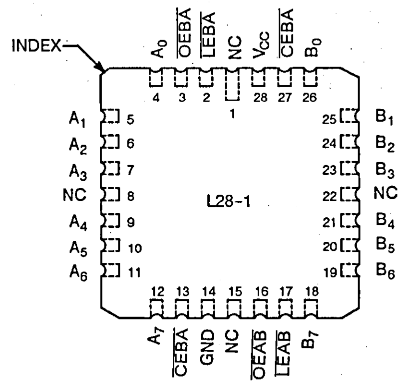


CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

PIN CONFIGURATIONS

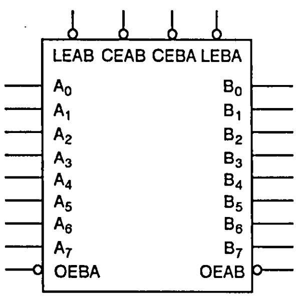


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



TRUTH TABLE For A-TO-B (Symmetric with B-TO-A)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-TO-B	B_0-B_7
H	X	X	Storing	High Z
X	H	–	Storing	–
X	–	H	–	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

* Before $\overline{LEAB}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

A-to-B data flow shown: B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

PIN DESCRIPTIONS

PIN NAMES	DESCRIPTION
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0-A_7	A-to-B Data Inputs or B-to-A 3-State Outputs
B_0-B_7	B-to-A Data Inputs or A-to-B 3-State Outputs

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Currents (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15[4]	
I_{IL}	Input LOW Currents (I/O pins only)		V_I = 0.5V	–	–	-15[4]	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open $\overline{CEAB}$ & $\overline{OEAB}$ = Low $\overline{CEBA}$ = High One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current(6)	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CEAB}$ & $\overline{OEAB}$ = Low $\overline{CEBA}$ = High f_{CP} = $\overline{LEAB}$ = 10MHz One Bit Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	5.6	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CEAB}$ & $\overline{OEAB}$ = Low $\overline{CEBA}$ = High f_{CP} = $\overline{LEAB}$ = 10MHz Eight Bits Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8(5)	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	15.0(5)	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT543					IDT54/74FCT543A					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	$C_L = 50pF$ $R_L = 500\Omega$	5.0	3.0	8.5	2.0	10.0	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A_n, $\overline{LEAB}$ to B_n		8.5	3.0	12.5	3.0	14.0	–	–	–	–	–	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n		7.0	3.0	12.0	3.0	14.0	–	–	–	–	–	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n		5.5	2.5	9.0	2.5	13.0	–	–	–	–	–	ns
t_{SU}	Set-up Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$		–	3.0	–	3.0	–	–	–	–	–	–	ns
t_H	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$		–	3.0	–	3.0	–	–	–	–	–	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at $V_{CC} = 5.0V$, $+25°C$ ambient and maximum loading.

10

ORDERING INFORMATION

IDT XX (Temperature) XX (Device Type) A (Package) A (Process)

Process	Blank	Commercial
	B	MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	L	Leadless Chip Carrier
	SO	Small Outline IC
	E	CERPACK
Device Type	543	Octal Registered Transceiver
	543A	Fast Octal Registered Transceiver
Temperature	54	-55°C to +125°C
	74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSPARENT LATCH

IDT54/74FCT573
IDT54/74FCT573A

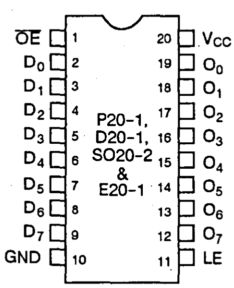
FEATURES:

- IDT54/74FCT573 equivalent to FAST™ speed; **IDT54/74FCT573A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal transparent latch with enable
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

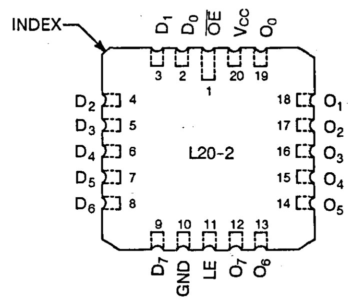
DESCRIPTION:

The IDT54/74FCT573 and IDT54/74FCT573A are 8-bit latches built using advanced CEMOS™, a dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus-oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS

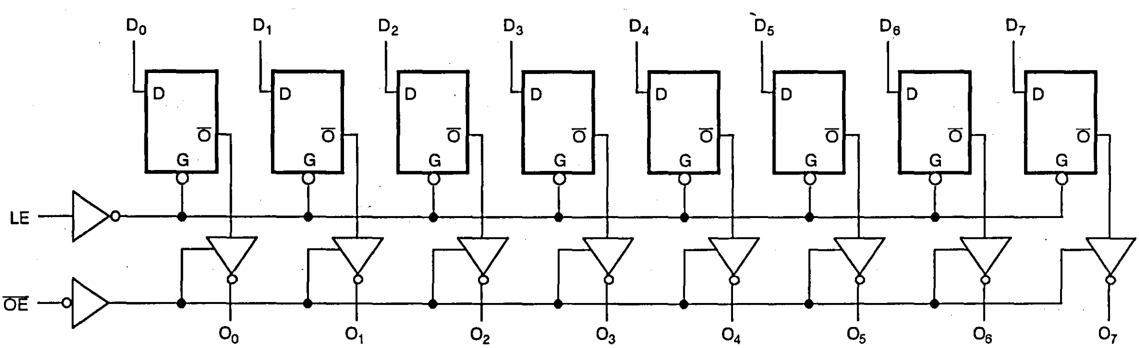


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

10

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10[4]	
			V_O = 0.5V	–	–	-10[4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_{CP} = f_I = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current(6)	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_{CP} = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5(5)	
			V_{IN} = 3.4V or V_{IN} = GND	–	5.0	14.5(5)	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
LE	Latch Enables Input (Active HIGH)
$\overline{OE}$	Output Enables Input (Active LOW)
O_0-O_7	3-State Latch Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT573					IDT54/74FCT573A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n		5.0	1.5	8.0	1.5	8.5	4.0	1.5	5.2	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n		9.0	2.0	13.0	2.0	15.0	7.0	2.0	8.5	2.0	9.8	ns
t_{PZH} t_{PZL}	Output Enable Time		7.0	1.5	12.0	1.5	13.5	5.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time	$C_L = 50pF$ $R_L = 500\Omega$	6.0	1.5	7.5	1.5	10.0	4.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW D_n to LE		1.0	2.0	–	2.0	–	1.0	2.0	–	2.0	–	ns
t_H	Hold Time HIGH or LOW D_n to LE		1.0	1.5	–	1.5	–	1.0	1.5	–	1.5	–	ns
t_W	LE Pulse Width HIGH or LOW		5.0	6.0	–	6.0	–	4.0	5.0	–	6.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT — Temp. Range
XXXX — Device Type
X — Package
X — Process

Process:
- Blank — Commercial
- B — MIL-STD-883, Class B

Package:
- P — Plastic DIP
- D — CERDIP
- SO — Small Outline IC
- L — Leadless Chip Carrier
- E — CERPACK

Device Type:
- 573 — Octal Transparent Latch
- 573A — Fast Octal Transparent Latch

Temp. Range:
- 54 — -55°C to +125°C
- 74 — 0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTER (3-STATE)

IDT54/74FCT574 IDT54/74FCT574A

FEATURES:

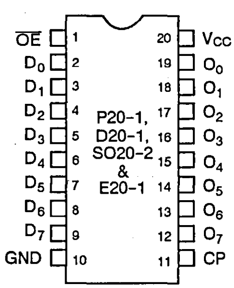
- IDT54/74FCT574 equivalent to FAST™ speed; **IDT54/74FCT574A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5µW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5µA max.)
- Positive, edge-triggered Master/Slave, D-type flip-flops
- Buffered common clock and buffered common three-state control
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

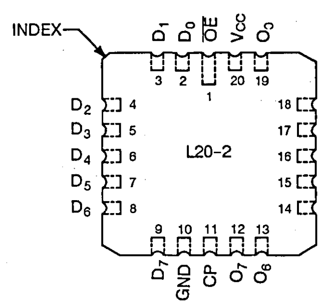
The IDT54/74FCT574 and IDT54/74FCT574A are 8-bit registers built using advanced CEMOS™, a dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered three-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state conditions.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

PIN CONFIGURATIONS

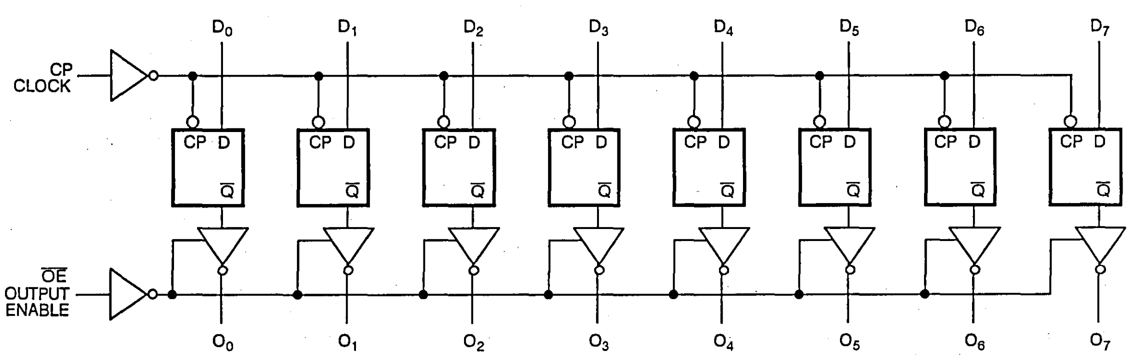


DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER [1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP. [2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5 [4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5 [4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10 [4]	
			V_O = 0.5V	–	–	-10 [4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max. [3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300µA	V_{HC}	V_{CC}	–	
			I_{OH} = −12mA MIL.	2.4	4.3	–	
			I_{OH} = −15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current (4)	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current (6)	V_{CC} = Max. Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_I = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8 (5)	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	16.8 (5)	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

10

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_I	The D flip-flop data inputs.
CP	Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
O_I	The register three-state outputs.
$\overline{OE}$	Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CLOCK	D_I	O_I	$\overline{Q}_I$
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↑	L	L	H
	L	↑	H	H	L
	H	↑	L	Z	H
	H	↑	H	Z	L

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
NC = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT574					IDT54/74FCT574A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	$C_L = 50pF$ $R_L = 500\Omega$	6.6	2.0	10.0	2.0	11.0	4.5	2.0	6.5	2.0	7.2	ns
t_{PZH} t_{PZL}	Output Enable Time		9.0	1.5	12.5	1.5	14.0	5.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		6.0	1.5	8.0	1.5	8.0	4.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW D_n to CP		1.0	2.0	–	2.5	–	1.0	2.0	–	2.0	–	ns
t_H	Hold Time HIGH or LOW D_n to CP		0.5	2.0	–	2.0	–	0.5	1.5	–	1.5	–	ns
t_W	CP Pulse Width HIGH or LOW		4.0	7.0	–	7.0	–	4.0	5.0	–	6.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT XXXX X X
Temp. Range Device Type Package Process

Process	Blank	Commercial
	B	MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	SO	Small Outline IC
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	574	Octal D Register (3-State)
	574A	Fast Octal D Register (3-State)
Temp. Range	54	-55°C to +125°C
	74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS OCTAL INVERTING BUFFER TRANSCEIVER

IDT54/74FCT640
IDT54/74FCT640A

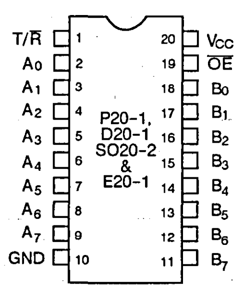
FEATURES:

- IDT54/74FCT640 7.0ns max. data to output; **IDT54/74FCT640A 5.0ns max. data to output**
- Equivalent to FAST ™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA commercial and 48mA military
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST ™ (5μA max.)
- Inverting buffer transceiver
- JEDEC standard pinout for DIP, LCC and SOIC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

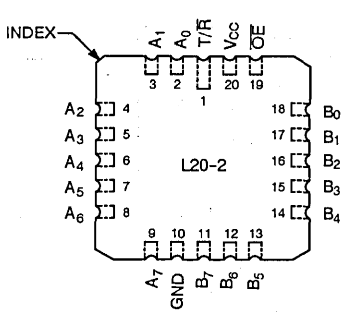
DESCRIPTION:

The IDT54/74FCT640 and IDT54/74FCT640A are 8-bit inverting buffer transceivers built using advanced CEMOS ™, a dual metal CMOS technology. These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control (T/$\overline{R}$) input. The enable input ($\overline{OE}$) can be used to disable the device so the buses are effectively isolated.

PIN CONFIGURATIONS

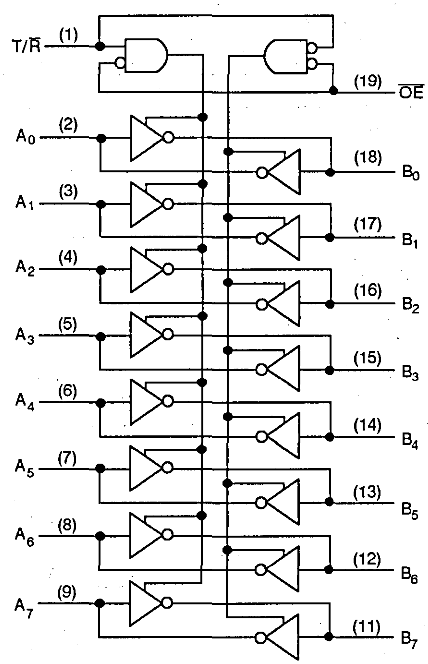


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



10

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a registered trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} -0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.4V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15[4]	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.4V	–	–	-15[4]	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH}= -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.55	
			I_{OL} = 48mA COM'L.	–	0.3	0.55	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	5.0	14.5[5]	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC}\, D_H N_T + I_{CCD}\, (f_{CP}/2 + f_I\, N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

INPUTS		OPERATION
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-State Outputs
B_0–B_7	Side B Inputs or 3-State Outputs

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	IDT54/74FCT640					IDT54/74FCT640A					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	C_L = 50pF R_L = 500Ω	6.0	2.0	7.0	2.0	8.0	3.5	1.5	5.0	1.5	5.3	ns
t_{PZH} t_{PZL}	Output Enable Time for $\overline{OE}$ and T/$\overline{R}$		11.0	2.0	13.0	2.0	16.0	4.8	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time for $\overline{OE}$ and T/$\overline{R}$		7.0	2.0	10.0	2.0	12.0	4.5	1.5	5.0	1.5	6.0	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT XXXX X X
Temp. Range / Device Type / Package / Process

Process:
- Blank — Commercial
- B — MIL-STD-883, Class B

Package:
- P — Plastic DIP
- D — CERDIP
- SO — Small Outline IC
- L — Leadless Chip Carrier
- E — CERPACK

Device Type:
- 640 — Octal Inverting Buffer Transceiver (equivalent to FAST™)
- 640A — Octal Inverting Buffer Transceiver (faster than FAST™)

Temp. Range:
- 54 — -55°C to +125°C
- 74 — 0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS NON-INVERTING BUFFER TRANSCEIVER

IDT54/74FCT645
IDT54/74FCT645A

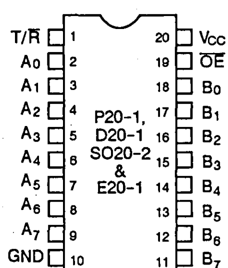
FEATURES:

- IDT54/74FCT645 equivalent to FAST™ speed; **IDT54/74FCT645A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (5μW typ. static)
- Substantially lower input current levels than FAST™ (5μA max.)
- Non-inverting buffer transceiver
- TTL input and output level compatible
- CMOS output level compatible
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

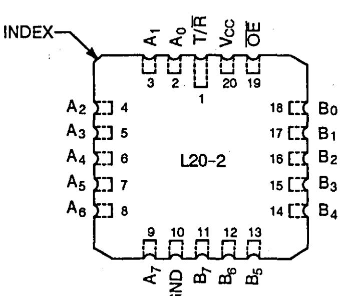
DESCRIPTION:

The IDT54/74FCT645 and IDT54/74FCT645A are 8-bit non-inverting buffer transceivers built using advanced CEMOS™, a dual metal CMOS technology. These non-inverting buffer transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control (T/R̄) input. The enable input (O̅E̅) can be used to disable the device so the buses are effectively isolated.

PIN CONFIGURATIONS

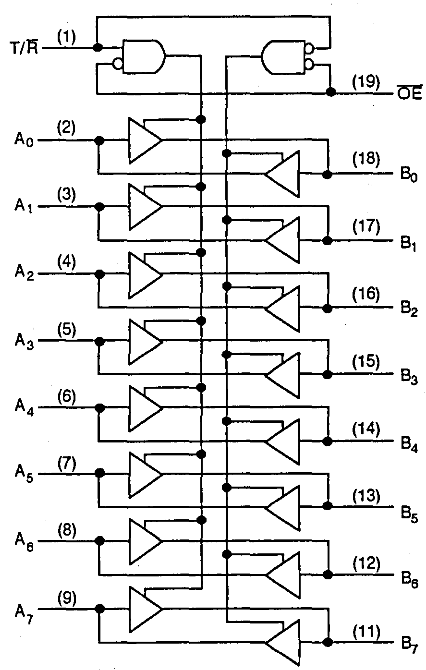


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	μA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	μA
			V_I = 2.7V	–	–	15[4]	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15[4]	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300μA	V_{HC}	V_{CC}	–	
			I_{OH} = –12mA MIL.	2.4	4.3	–	
			I_{OH} = –15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current [4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open f_I = 10MHz, 50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5 [5]	
			V_{IN} = 3.4V V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

TRUTH TABLE

INPUTS		OPERATION
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT645					IDT54/74FCT645A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	C_L = 50pF R_L = 500Ω	6.0	1.5	9.5	1.5	11.0	3.3	1.5	4.6	1.5	4.9	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		9.0	1.5	11.0	1.5	12.0	4.8	1.5	6.2	1.5	6.5	ns
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ to A or B		9.0	1.5	11.0	1.5	12.0	4.8	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B[4]		6.0	1.5	12.0	1.5	13.0	4.5	1.5	5.0	1.5	6.0	ns
t_{PHZ} t_{PLZ}	Output Enable Time T/$\overline{R}$ to A or B[4]		6.0	1.5	12.0	1.5	13.0	4.5	1.5	5.0	1.5	6.0	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
4. This parameter is guaranteed but not tested.

ORDERING INFORMATION

IDTXXFCT (Temp. Range) XXXX (Device Type) X (Package) X (Process)

Process	Blank	Commercial
	B	MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	SO	Small Outline IC
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	645	Non-Inverting Buffer Transceiver
	645A	Fast Non-Inverting Buffer Transceiver
Temp. Range	54	-55°C to +125°C
	74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSCEIVER/ REGISTER

PRELIMINARY
IDT54/74FCT646/A
IDT54/74FCT648/A

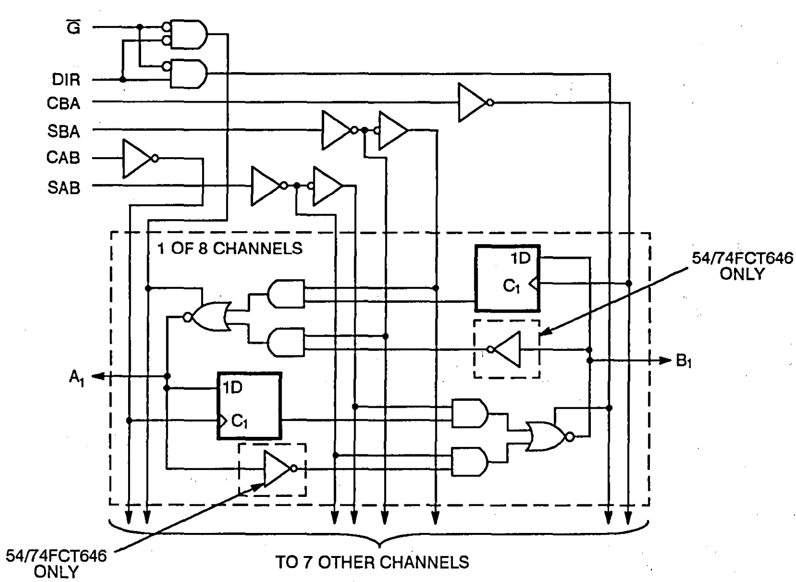
FEATURES:

- IDT54/74FCT646 and IDT54/74FCT648 equivalent to FAST™ speed;
- **IDT54/74FCT646A and IDT54/74FCT648A are 30% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of true and inverting data paths
- 3-state outputs
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 24-pin, 300 mil CERDIP, plastic DIP, SOIC, CERPACK and 28-pin LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT646/A and IDT54/74FCT648/A consist of a bus transceiver circuit with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Enable Control $\overline{G}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (Enable Control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

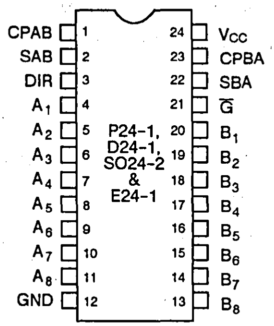
FUNCTIONAL BLOCK DIAGRAM



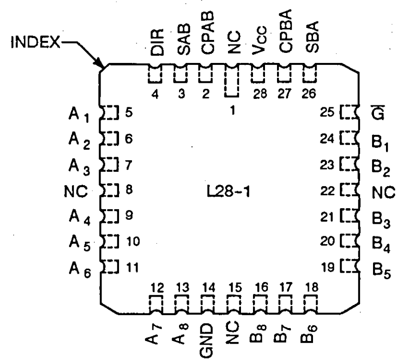
CEMOS is a registered trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

PIN CONFIGURATIONS

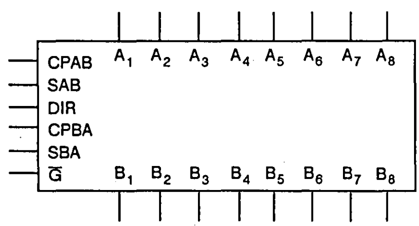


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN DESCRIPTION

PIN NAMES	DESCRIPTION
$A_1 - A_8$	Data Register A Inputs Data Register B Outputs
$B_1 - B_8$	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
DIR, $\overline{G}$	Output Enable Inputs

FUNCTION TABLE

INPUTS						DATA I/O(1)		OPERATION or FUNCTION	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	$A_1 - A_8$	$B_1 - B_8$	FCT646/A	FCT648/A
H H	X X	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
L L	L L	X X	X H or L	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus	Real Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus	Real Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data to B Bus

NOTES:
1. The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.
2. H = HIGH
   L = LOW
   X = Don't Care
   ↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is guaranteed by characterization and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.,	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.,	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15[4]	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15[4]	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output High Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = −32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300µA	V_{HC}	V_{CC}	–	
			I_{OH} = −12mA MIL.	2.4	4.0	–	
			I_{OH} = −15mA COM'L.	2.4	4.0	–	
V_{OL}	Output Low Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	

NOTES:
1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These parameters are guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current [4]	V_{CC} = Max. Outputs Open $\overline{G}$ = GND DIR = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{G}$ = GND DIR = GND One Bit Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{G}$ = GND DIR = GND Eight Bits Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	6.75	12.75[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	9.75	21.75[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITIONS(1)	IDT54/74FCT646					IDT54/74FCT646A(4)					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	8.0	2.0	9.0	2.0	11.0	–	2.0	6.3	2.0	7.7	ns
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus & DIR to A or B		9.0	2.0	14.0	2.0	15.0	–	2.0	9.8	2.0	10.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus & Direction to Bus		9.0	2.0	9.0	2.0	11.0	–	2.0	6.3	2.0	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		8.0	2.0	9.0	2.0	10.0	–	2.0	6.3	2.0	7.0	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B		10.0	2.0	11.0	2.0	12.0	–	2.0	7.7	2.0	8.4	ns
t_{SU}	Set-up time HIGH or LOW Bus to Clock		3.0	4.0	–	4.5	–	–	2.0	–	2.0	–	ns
t_H	Hold time HIGH or LOW Bus to Clock		1.0	2.0	–	2.0	–	–	1.5	–	1.5	–	ns
t_{PW}	Pulse Width, HIGH or LOW		4.0	6.0	–	6.0	–	–	5.0	–	5.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
4. These are preliminary numbers only.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITIONS(1)	IDT54/74FCT648(4)					IDT54/74FCT648A(4)					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	7.0	2.0	8.0	2.0	9.0	–	2.0	5.6	2.0	6.3	ns
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus & DIR to A or B		9.0	2.0	15.0	2.0	18.0	–	2.0	10.5	2.0	12.6	ns
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus & Direction to Bus		9.0	2.0	9.0	2.0	11.0	–	2.0	6.3	2.0	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		7.0	2.0	9.0	2.0	10.0	–	2.0	6.3	2.0	7.0	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B		10.0	2.0	11.0	2.0	12.0	–	2.0	7.7	2.0	8.4	ns
t_{SU}	Set-up time HIGH or LOW Bus to Clock		3.0	4.0	–	4.5	–	–	2.0	–	2.0	–	ns
t_H	Hold time HIGH or LOW Bus to Clock		1.0	2.0	–	2.0	–	–	1.5	–	1.5	–	ns
t_{PW}	Pulse Width, HIGH or LOW		4.0	6.0	–	6.0	–	–	5.0	–	5.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
4. These are preliminary numbers only.

ORDERING INFORMATION

IDTXXFCT	XXXX	XX	X
Temperature Range	Device Type	Package	Process/ Temperature Range

Process/Temperature Range	Blank	Commercial
	B	MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	SO	Small Outline IC
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	646	Non-inverting Octal Transceiver/Register
	646A	Fast Non-inverting Fast Octal Transceiver/ Register
	648	Inverting Octal Transceiver/Register
	648A	Fast Inverting Fast Octal Transceiver/Register
Temperature Range	54	(-55°C to +125°C)
	74	(0°C to +70°C)

Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSCEIVER/ REGISTER

PRELIMINARY
IDT54/74FCT651/A
IDT54/74FCT652/A

FEATURES:

- IDT54/74FCT651 and IDT54/74FCT652 are equivalent to FAST™ speeds
- **IDT54/74FCT651A and IDT54/74FCT652A 30% faster than FAST™ speeds**
- Bidirectional bus transceiver and registers
- Independent registers for A and B buses
- Real-time data transfer or stored data transfer
- Choice of true and inverting data transfer
- 3-state outputs
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 24-pin 300 mil DIP, SOIC and 28-pin LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

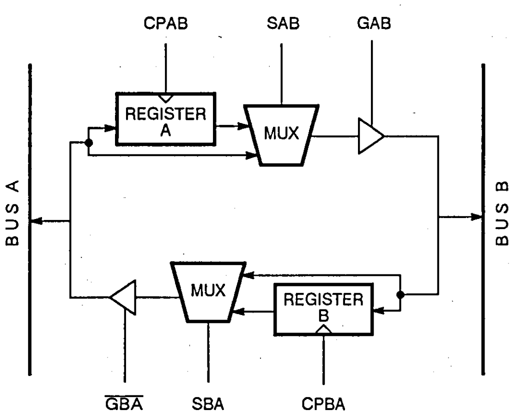
DESCRIPTION:

The IDT54/74FCT651/A and IDT54/74FCT652/A, built in CEMOS™, consist of bus transceiver circuits, D-type flip-flops and control circuitry arranged for multiplex transmission of data directly from the data bus or from the internal storage registers. GAB and $\overline{GBA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data.

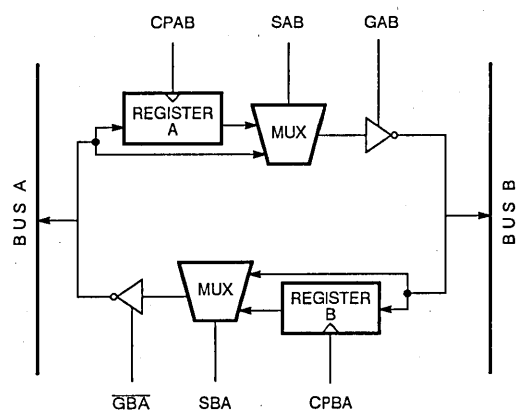
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{GBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT652/A (Non-inverting)

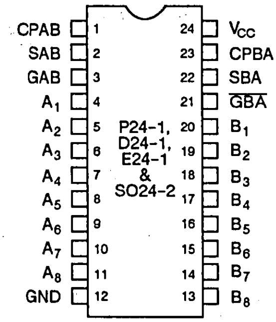


IDT54/74FCT651/A (Inverting)

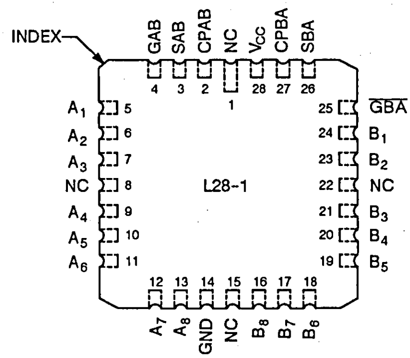


CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

PIN CONFIGURATIONS

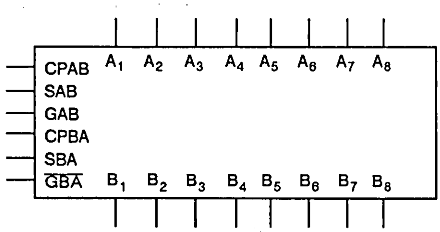


DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN DESCRIPTION

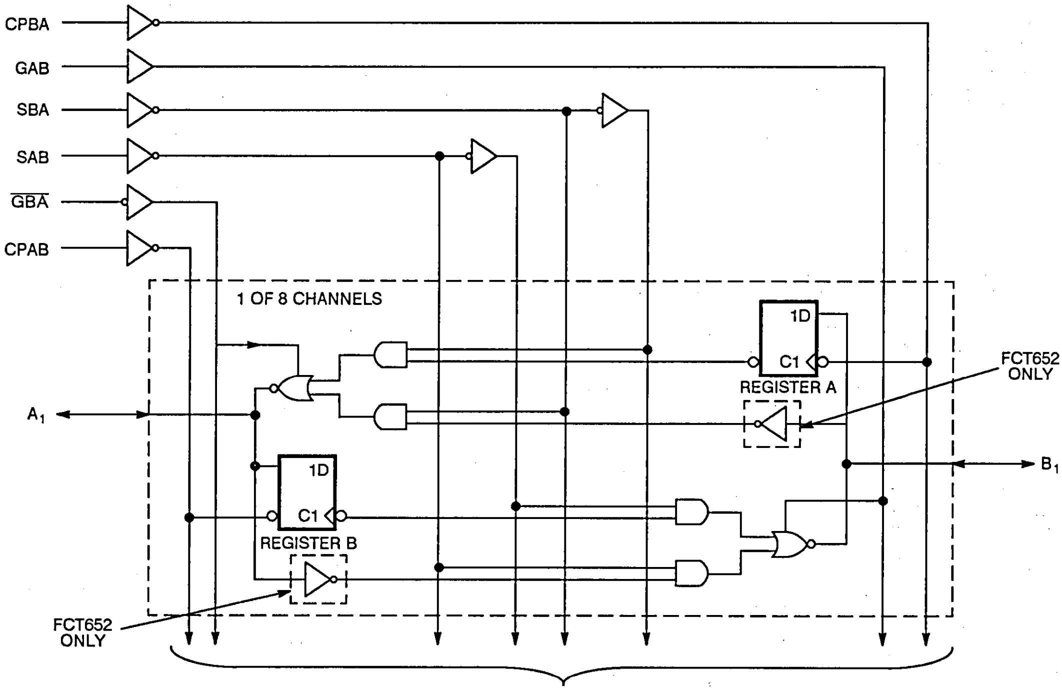
PIN NAMES	DESCRIPTION
A_1-A_8	Data Register Inputs Data Register A Outputs
B_1-B_8	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
GAB, $\overline{GBA}$	Output Enable Inputs

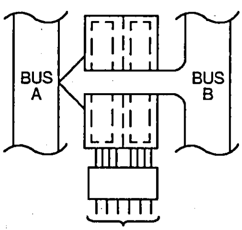
FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 THRU A_8	B_1 THRU B_8	FCT651/A	FCT652/A
L L	H H	H or L $\uparrow$	H or L $\uparrow$	X X	X X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
X H	H H	$\uparrow$ $\uparrow$	H or L $\uparrow$	X X(2)	X X	Input Input	Unspecified(1) Output	Store A, Hold B Store A in both registers	Store A, Hold B Store A in both registers
L L	X L	H or L $\uparrow$	$\uparrow$ $\uparrow$	X X	X X(2)	Unspecified(1) Output	Input Input	Hold A, Store B Store B in both registers	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real-Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real-Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

NOTES:
1. The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = HIGH, L = LOW, X = Don't Care, $\uparrow$ LOW-to-HIGH Transition

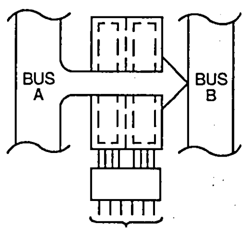
DETAILED BLOCK DIAGRAM





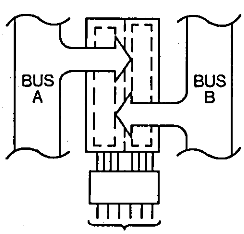
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



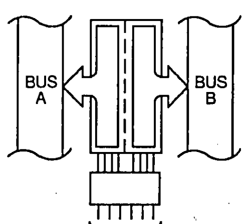
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A AND/OR B



GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER
STORED DATA
TO A AND/OR B

10

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15[4]	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15[4]	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open GAB = GND $\overline{GBA}$ = GND SAB = CPAB = GND SBA = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle GAB = GND $\overline{GBA}$ = GND SAB = CPAB = GND SBA = V_{CC} One Bit Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle GAB = GND $\overline{GBA}$ = GND SAB = CPAB = GND SBA = V_{CC} Eight Bits Toggling at f_I = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	16.8[5]	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT651/652					IDT54/74FCT651A/652A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	8.0	2.0	9.0	2.0	10.0	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		8.0	2.0	9.0	2.0	11.0	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B		10.0	2.0	11.0	2.0	12.0	–	–	–	–	–	ns
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus		9.0	2.0	10.0	2.0	12.0	–	–	–	–	–	ns
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus		9.0	2.0	10.0	2.0	12.0	–	–	–	–	–	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		3.0	4.0	–	4.5	–	–	–	–	–	–	ns
t_H	Hold Time HIGH or LOW Bus to Clock		1.0	2.0	–	2.0	–	–	–	–	–	–	ns
t_W	Pulse Width, HIGH or LOW		4.0	6.0	–	6.0	–	–	–	–	–	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

IDTXXFCT XXX (Device Type) X (Package) X (Process/Temperature)

Process/Temperature	Blank	Commercial
	B	Compliant to MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	E	CERPACK
	L	Leadless Chip Carrier
	SO	Small Outline IC
Device Type	651	Inverting Octal Transceiver/Register
	652	Non-inverting Octal Transceiver/Register
	651A	Inverting Fast Octal Transceiver/Register
	652A	Non-inverting Fast Octal Transceiver/Register
IDTXX	54	-55°C to +125°C
	74	0°C to +70°C

HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT54/74FCT821A/B- IDT54/74FCT826A/B

FEATURES:

- Equivalent to AMD's Am29821-26 bipolar registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed parallel registers with positive edge-triggered D-type flip-flops
  - Non-inverting CP-Y t_{PD} = 7.5ns typ.
  - Inverting CP-Y t_{PD} = 7.5ns typ.
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- I_{OL} = 48mA (commercial), 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (5µW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5µA max.)
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

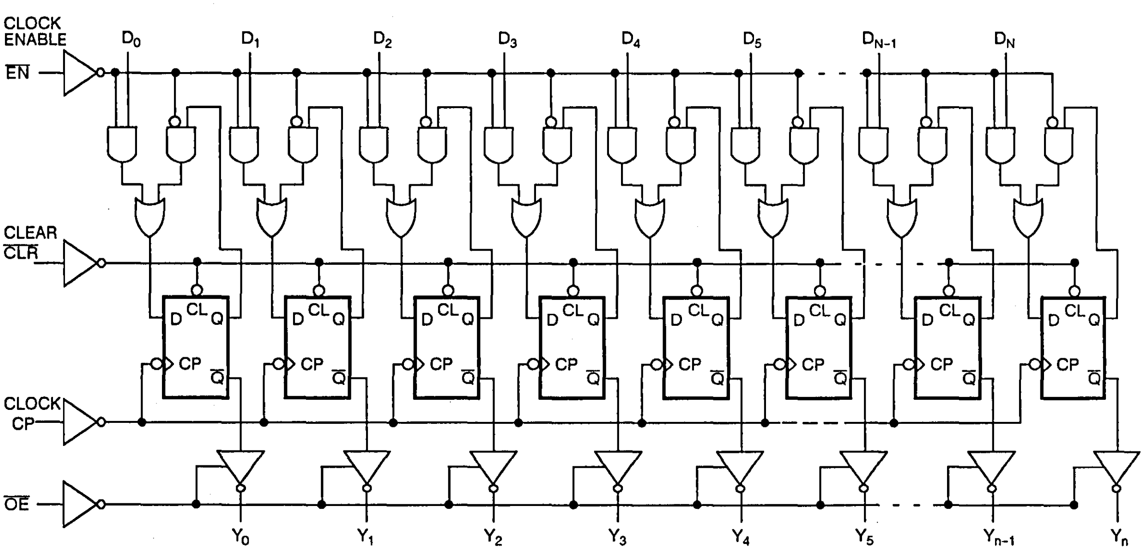
DESCRIPTION:

The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT821 and IDT54/74FCT822 are buffered, 10-bit wide versions of the popular '374/'534 functions. The IDT54/74FCT823 and IDT54/74FCT824 are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$)—ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT54/74FCT825 and IDT54/74FCT826 are 8-bit buffered registers with all the '823/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT SELECTOR GUIDE

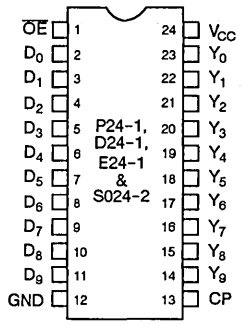
	DEVICE		
	10-BIT	9-BIT	8-BIT
Non-inverting	54/74FCT821A/B	54/74FCT823A/B	54/74FCT825A/B
Inverting	54/74FCT822A/B	54/74FCT824A/B	54/74FCT826A/B

CEMOS is a trademark of Integrated Device Technology, Inc.

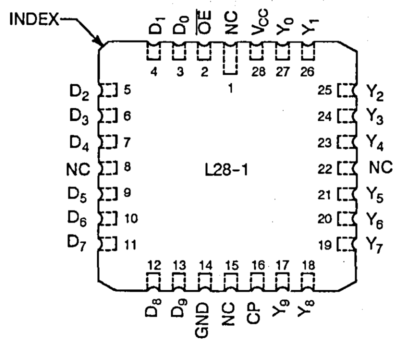
PIN CONFIGURATIONS

LOGIC SYMBOLS

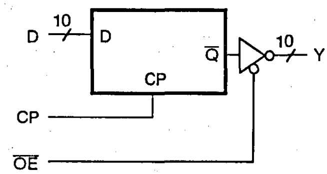
IDT54/74FCT821/IDT54/74FCT822 10-BIT REGISTERS



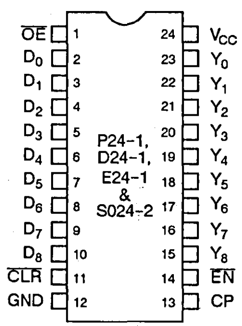
DIP/CERPACK/SOIC
TOP VIEW



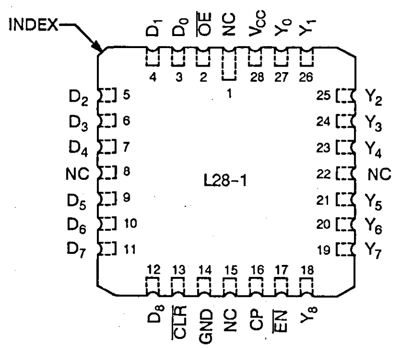
LCC
TOP VIEW



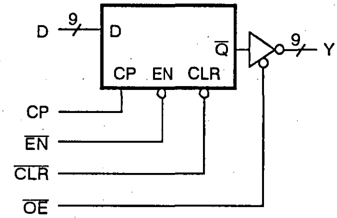
IDT54/74FCT823/IDT54/74FCT824 9-BIT REGISTERS



DIP/CERPACK/SOIC
TOP VIEW

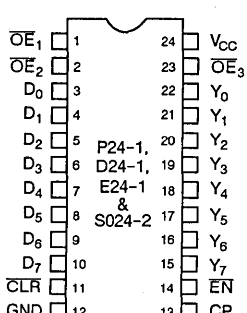


LCC
TOP VIEW

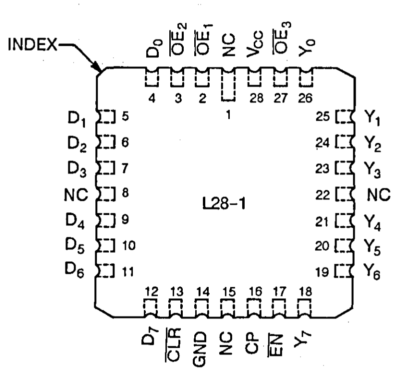


10

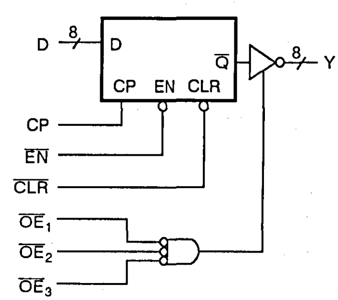
IDT54/74FCT825/IDT54/74FCT826 8-BIT REGISTERS



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW



PIN DESCRIPTION

NAME	I/O	DESCRIPTION
D_I	I	The D flip-flop data inputs.
$\overline{\text{CLR}}$	I	For both inverting and non-inverting registers, when the clear input is LOW and $\overline{\text{OE}}$ is LOW, the Q_I outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y_I, $\overline{Y}_I$	O	The register three-state outputs.
$\overline{\text{EN}}$	I	Clock Enable. When the clock enable is LOW, data on the D_I input is transferred to the Q_I output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_I outputs do not change state, regardless of the data or clock input transitions.
$\overline{\text{OE}}$	I	Output Control. When the $\overline{\text{OE}}$ input is HIGH, the Y_I outputs are in the high impedance state. When the $\overline{\text{OE}}$ input is LOW, the TRUE register data is present at the Y_I outputs.

FUNCTION TABLES [1]
IDT54/74FCT821/23/25

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	$\overline{\text{EN}}$	D_I	CP	Q_I	Y_I	
H	X	L	L	↑	L	Z	High Z
H	X	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

FUNCTION TABLES [1]
IDT54/74FCT822/24/26

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	$\overline{\text{EN}}$	D_I	CP	Q_I	Y_I	
H	X	L	L	↑	H	Z	High Z
H	X	L	H	↑	L	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	H	
L	H	L	H	↑	L	L	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	μA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	μA
			V_O = 2.7V	–	–	10(4)	
			V_O = 0.5V	–	–	-10(4)	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-75	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = −32μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300μA	V_{HC}	V_{CC}	–	
			I_{OH} = −15mA MIL.	2.4	4.3	–	
			I_{OH} = −24mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current (6)	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_I = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8(5)	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	16.8(5)	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0V$, +25°C ambient and maximum loading.
3. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETER	DESCRIPTION	TEST CONDITIONS[1]	IDT54/74FCT821A-26A				IDT54/74FCT821B-26B				UNIT
			COM'L.		MIL.		COM'L.		MIL.		
			MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)	C_L = 50pF R_L = 500Ω	–	12	–	12	–	7.5	–	8.5	ns
t_{PLH} t_{PHL}		C_L = 300pF[3] R_L = 500Ω	–	20	–	20	–	15	–	16	ns
t_{SU}	Data to CP Set-up Time	C_L = 50pF R_L = 500Ω	4	–	4	–	3	–	3	–	ns
t_H	Data CP Hold Time		2	–	2	–	1.5	–	1.5	–	ns
t_{SU}	Enable ($\overline{EN}$ ↑) to CP Set-up Time		4	–	4	–	3.0	–	3.0	–	ns
t_{SU}	Enable ($\overline{EN}$ ↑) to CP Set-up Time		4	–	4	–	3.0	–	3.0	–	ns
t_H	Enable ($\overline{EN}$) Hold Time		2	–	2	–	0	–	0	–	ns
t_{PHL}	Propagation Delay, Clear to Y_i		–	20	–	20	–	9.0	–	9.5	ns
t_{SU}	Clear Recovery ($\overline{CLR}$ ↑) Time		7	–	7	–	6.0	–	6.0	–	ns
t_{PWH}	Clock Pulse Width HIGH		7	–	7	–	6.0	–	6.0	–	ns
t_{PWL}	Clock Pulse Width LOW		7	–	7	–	6.0	–	6.0	–	ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width		7	–	7	–	6.0	–	6.0	–	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ ↑ to Y_i	C_L = 50pF R_L = 500Ω	–	14	–	15	–	8	–	9	ns
t_{PZH} t_{PZL}		C_L = 300pF[3] R_L = 500Ω	–	23	–	25	–	15	–	16	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ ↑ to Y_i	C_L = 5pF[3] R_L = 500Ω	–	9	–	10	–	6.5	–	7	ns
t_{PHZ} t_{PLZ}		C_L = 50pF R_L = 500Ω	–	16	–	18	–	7.5	–	8	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

ORDERING INFORMATION

IDTXXFCT	XXXX	X	X
Temp. Range	Device Type	Package	Process

Blank	Commercial
B	MIL-STD-883, Class B
P	Plastic DIP
D	CERDIP
E	CERPACK
L	Leadless Chip Carrier
SO	Small Outline IC
821A	10-Bit Non-Inverting Register
821B	Fast 10-Bit Non-Inverting Register
822A	10-Bit Inverting Register
822B	Fast 10-Bit Inverting Register
823A	9-Bit Non-Inverting Register
823B	Fast 9-Bit Non-Inverting Register
824A	9-Bit Inverting Register
824B	Fast 9-Bit Inverting Register
825A	8-Bit Non-Inverting Register
825B	Fast 8-Bit Non-Inverting Register
826A	8-Bit Inverting Register
826B	Fast 8-Bit Inverting Register
54	-55°C to +125°C
74	0°C to +70°C

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUFFERS

IDT54/74FCT827A/B IDT54/74FCT828A/B

FEATURES:

- **Faster than AMD's Am29827-28 series**
- Equivalent to AMD's Am29827-28 bipolar buffers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed buffers
  - Non-inverting t_{PD} = 3.5ns typ.
  - Inverting t_{PD} = 4.0ns typ.
- I_{OL} = 48mA (commercial), 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (5µW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 Series (5µA max.)
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

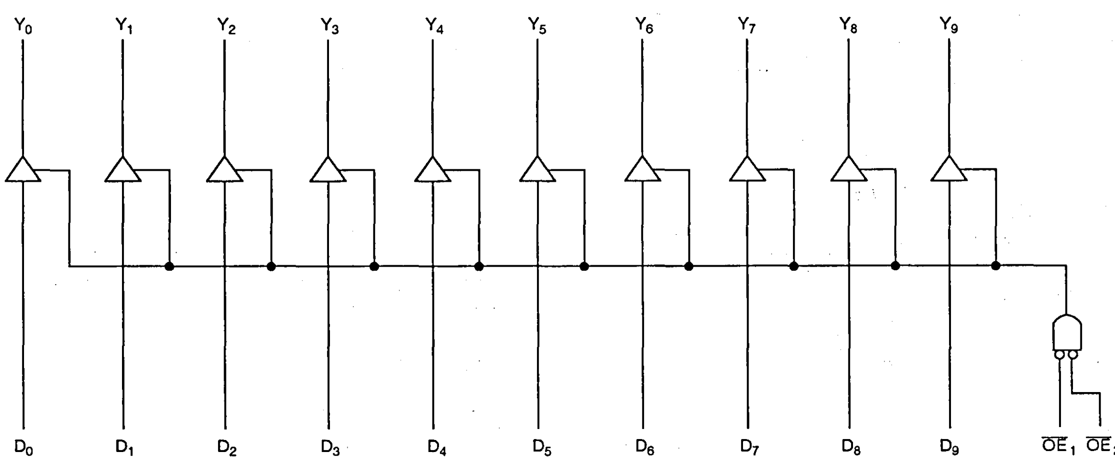
DESCRIPTION:

The IDT54/74FCT800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT827A/B and IDT54/74FCT828A/B 10-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR-ed output enables for maximum control flexibility. All buffer data inputs have 200mV minimum input hysteresis to provide improved noise rejection.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM
IDT54/74FCT827A/B–IDT5474FCT828A/B 10-BIT BUFFERS



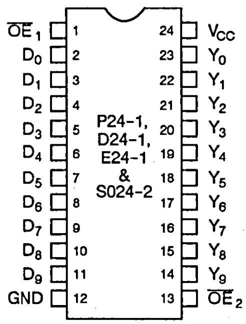
10

PRODUCT SELECTOR GUIDE

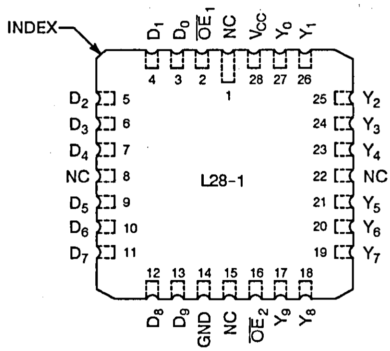
	10-BIT BUFFER
Non-inverting	IDT54/74FCT827A/B
Inverting	IDT54/74FCT828A/B

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS
IDT54/74FCT827A/B/IDT54/74FCT828A/B

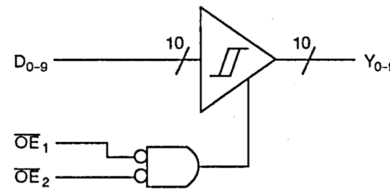


DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN DESCRIPTION

NAME	I/O	DESCRIPTION
$\overline{OE}_I$	I	When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are High Z.
D_I	I	10-bit data input.
Y_I	O	10-bit data output.

FUNCTIONAL TABLES
IDT54/74FCT827A/B (NON-INVERTING)(1)

INPUTS			OUTPUT	FUNCTION
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	
L L	L L	L H	L H	Transparent
H X	X H	X X	Z Z	Three-State

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

IDT54/74FCT828A/B (INVERTING)(1)

INPUTS			OUTPUT	FUNCTION
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	
L L	L L	L H	H L	Transparent
H X	X H	X X	Z Z	Three-State

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10[4]	
			V_O = 0.5V	–	–	-10[4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-75	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -15mA MIL.	2.4	4.0	–	
			I_{OH} = -24mA COM'L.	2.4	4.0	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current (4)	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current (6)	V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5(5)	
			V_{IN} = 3.4V V_{IN} = GND	–	5.0	14.5(5)	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETER	DESCRIPTION	TEST CONDITIONS(1)	IDT54/74FCT827A/28A				IDT54/74FCT827B/28B				UNIT
			COM'L.		MIL.		COM'L.		MIL.		
			MIN.(2)	MAX.	MIN.(2)	MAX.	MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay from D_I to Y_I IDT54/74FCT827A/B (Non-inverting)	C_L = 50pF R_L = 500Ω	–	8	–	10	–	5.0	–	6.5	ns
t_{PLH} t_{PHL}		C_L = 300pF(3) R_L = 500Ω	–	15	–	17	–	13.0	–	14.0	ns
t_{PLH} t_{PHL}	Propagation Delay from D_I to Y_I IDT54/74FCT828A/B (Inverting)	C_L = 50pF R_L = 500Ω	–	7.5	–	9.5	–	5.5	–	6.5	ns
t_{PLH} t_{PHL}		C_L = 300pF(3) R_L = 500Ω	–	14	–	16	–	13.0	–	14.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_I	C_L = 50pF R_L = 500Ω	–	15	–	17	–	8.0	–	9.0	ns
t_{PZH} t_{PZL}		C_L = 300pF(3) R_L = 500Ω	–	23	–	25	–	15.0	–	16.0	ns
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_I	C_L = 5pF(3) R_L = 500Ω	–	9	–	10	–	6.0	–	7.0	ns
t_{PHZ} t_{PHL}		C_L = 50pF R_L = 500Ω	–	17	–	19	–	7.0	–	8.0	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

10

ORDERING INFORMATION

IDTXXFCT XX (Device Type) X (Package) X (Process)

Field	Code	Description
Process	Blank	Commercial
	B	MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP
	E	CERPACK
	L	Leadless Chip Carrier
	SO	Small Outline IC
Device Type	827A	Non-inverting 10-Bit Buffer
	828A	Inverting 10-Bit Buffer
	827B	Fast Non-inverting 10-Bit Buffer
	828B	Fast Inverting 10-Bit Buffer
XX	54	-55°C to +125°C
	74	0°C to +70°C

Integrated Device Technology, Inc.

FAST CMOS PARITY BUS TRANSCEIVER

PRELIMINARY
IDT54/74FCT833A/B
IDT54/74FCT834A/B
IDT54/74FCT853A/B
IDT54/74FCT854A/B

FEATURES:

- Equivalent to AMD's Am29833-34 and Am29853-54 bipolar parity bus transceivers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High speed bidirectional bus transceiver for processor-organized devices
  Non-inverting propagation delay = 7.0ns max.
  Inverting propagation delay = 7.0ns max.
- Buffered direction three state control
- Error Flag with open-drain output
- I_{OL} = 48mA (commercial) and 32mA (military)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Available in Plastic DIP, CERDIP, LCC and SOIC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

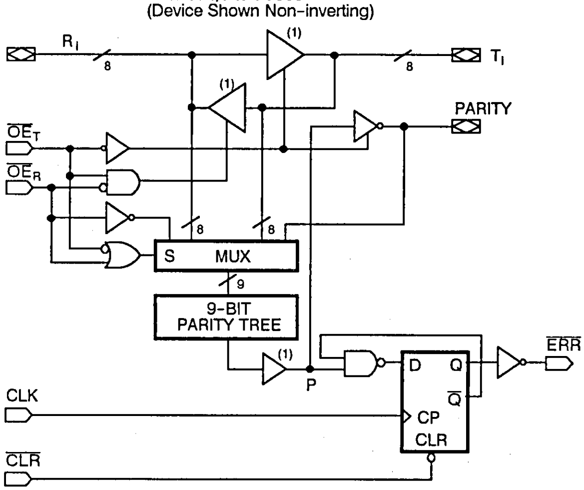
DESCRIPTION:

The IDT54/74FCT833/34/53/54 are high-performance bus transceivers designed for two-way communications. They each contain an 8-bit data path from the R (port) to the T (port), a 8-bit data path from the T (port) to the R (port), and a 9-bit parity checker/generator. Two options are available: the IDT54/74FCT833/34 register option and the IDT54/74FCT853/54 latch option. With the register option, the error flag can be clocked and stored in a register and read at the $\overline{ERR}$ output. The clear ($\overline{CLR}$) input is used to clear the error flag register. With the latch option, the error can be either passed, stored, sampled or cleared at the error flag output by using the $\overline{EN}$ and $\overline{CLR}$ controls.

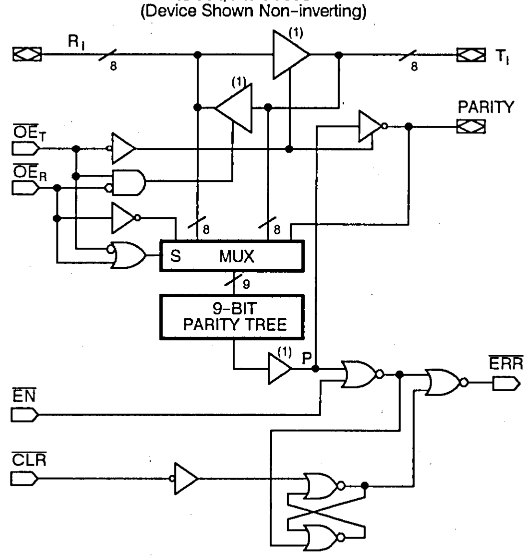
The output enables $\overline{OE_T}$ and $\overline{OE_R}$ are used to force the port outputs to the high-impedance state so that the device can drive bus lines directly. In addition, $\overline{OE_R}$ and $\overline{OE_T}$ can be used to force a parity error by enabling both lines simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability. The IDT54/74FCT833 and IDT54/74FCT853 are non-inverting, while the IDT54/74FCT834 and IDT54/74FCT854 present inverting data at the outputs. The devices are specified at 48mA and 32mA output sink current over the commercial and military temperature ranges, respectively.

FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT833
(Device Shown Non-inverting)



IDT54/74FCT853
(Device Shown Non-inverting)

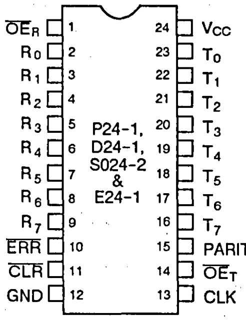


10

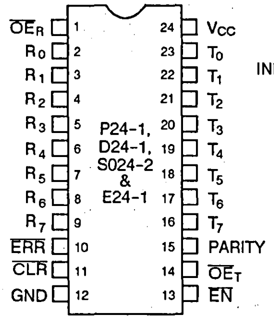
NOTE:
1. Non-inverting buffer for IDT54/74FCT833/53, inverting buffer for IDT54/74FCT834/54, note that the inverting device converts the positive logic "R" bus levels to negative levels on "T" bus.

PIN CONFIGURATIONS

IDT54/74FCT833/34

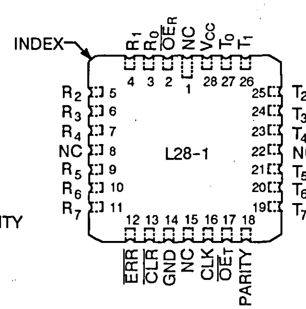


IDT54/74FCT853/54

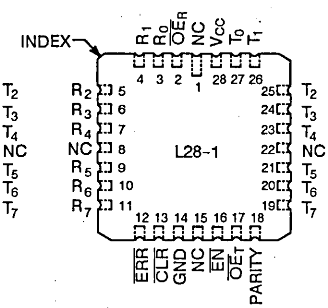


DIP/SOIC/CERPACK
TOP VIEW

IDT54/74FCT833/34



IDT54/74FCT853/54



LCC
TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
IDT54/74FCT833/34			
1	$\overline{OE}_R$	I	RECEIVE enable input.
2-9	R_I	I/O	8-bit RECEIVE data output.
10	$\overline{ERR}$	O	Output from fault registers. Registers detection of odd parity fault on using clock edge (CLK). A registered $\overline{ERR}$ output remains low until cleared. Open drain output, requires pull up resistor.
11	$\overline{CLR}$	O	Clears the fault register output.
16-23	T_I	I/O	8-bit TRANSMIT data output.
15	PARITY	I/O	1-bit PARITY output.
14	$\overline{OE}_T$	I	TRANSMIT enable input.
13	CLK	I	External clock pulse input for fault register flag.
IDT54/74FCT853/54			
1	$\overline{OE}_R$	I	RECEIVE enable input.
2-9	R_I	I/O	8-bit RECEIVE data output.
10	$\overline{ERR}$	O	Output from fault latches. Latches detection of odd parity fault on active enable $\overline{EN}$. A latched $\overline{ERR}$ output remains LOW until cleared. Open drain output, requires pull up resistor.
11	$\overline{CLR}$	O	Clears the fault latch output.
16-23	T_I	I/O	8-bit TRANSMIT data output.
15	PARITY	I/O	1-bit PARITY output.
14	$\overline{OE}_T$	I	TRANSMIT enable input.
13	$\overline{EN}$	I	Enable latch input for fault flag.

ERROR FLAG OUTPUT TRUTH TABLE

IDT54/74FCT833/IDT54/74FCT834 (REGISTER OPTION)

INPUTS		INTERNAL TO DEVICE	OUTPUTS PRE-STATE	OUTPUT	FUNCTION
$\overline{CLR}$	CLK	POINT "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	
H	↑	H	H	H	Sample (1's Capture)
H	↑	–	L	L	
H	↑	L	–	L	
L	–	–	–	H	Clear

$\overline{OE}_T$ is HIGH and $\overline{OE}_R$ is LOW.

IDT54/74FCT853/IDT54/74FCT854 (LATCH OPTION)

INPUTS		INTERNAL TO DEVICE	OUTPUTS PRE-STATE	OUTPUT	FUNCTION
$\overline{EN}$	$\overline{CLR}$	POINT "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	
L	L	L	–	L	Pass
L	L	H	–	H	
L	H	L	–	L	Sample (1's Capture)
L	H	–	L	L	
L	H	H	H	H	
H	L	–	–	H	Clear
H	H	–	L	L	Store
H	H	–	H	H	

$\overline{OE}_T$ is HIGH and $\overline{OE}_R$ is LOW.

FUNCTION TABLES

IDT54/74FCT833 NON-INVERTING REGISTER OPTION

INPUTS						OUTPUTS				FUNCTION
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	CLK	R_i (Σ OF H'S)	T_i INCL PARITY (Σ OF H'S)	R_i	T_i	PARITY	$\overline{ERR}$(1)	
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	H	H	NA	
L	H	–	–	L (Odd)	NA	NA	L	L	NA	
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	H	↑	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	H	↑	NA	H (Even)	H	NA	NA	L	
H	L	H	↑	NA	L (Odd)	L	NA	NA	H	
H	L	H	↑	NA	L (Even)	L	NA	NA	L	
–	–	L	–	–	–	–	NA	NA	H	Clear the state of error flag register.
H	H	H	–	–	–	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	–	–	–	Z	Z	Z	H	
H	H	H	↑	L (Odd)	–	Z	Z	Z	H	
H	H	H	↑	H (Even)	–	Z	Z	Z	L	
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

IDT54/74FCT834 INVERTING REGISTER OPTION(2)

INPUTS						OUTPUTS				FUNCTION
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	CLK	R_i (Σ OF L'S)	T_i INCL PARITY (Σ OF H'S)	R_i	T_i	PARITY	$\overline{ERR}$(1)	
L	H	–	–	H (Odd)	NA	NA	L	H	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	L	L	NA	
L	H	–	–	L (Odd)	NA	NA	H	H	NA	
L	H	–	–	L (Even)	NA	NA	H	L	NA	
H	L	H	↑	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	H	↑	NA	H (Even)	L	NA	NA	L	
H	L	H	↑	NA	L (Odd)	H	NA	NA	H	
H	L	H	↑	NA	L (Even)	H	NA	NA	L	
–	–	L	–	–	–	–	–	–	H	Clear the state of error flag register.
H	H	H	–	–	–	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	–	–	–	Z	Z	Z	H	
H	H	H	↑	L (Odd)	–	Z	Z	Z	L	
H	H	H	↑	H (Even)	–	Z	Z	Z	H	
L	L	–	–	H (Odd)	NA	NA	L	L	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	L	H	NA	
L	L	–	–	L (Odd)	NA	NA	H	L	NA	
L	L	–	–	L (Even)	NA	NA	H	H	NA	

H = High
L = Low
↑ = Low to high transition of clock
*Store the Error State of the Last Receive Cycle

Z = High Impedance
NA = Not Applicable
– = Don't Care or Irrelevant

Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7

NOTES:
1. Output state assumes HIGH output pre-state.
2. Note that for the negative levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1".

10

FUNCTION TABLES (CONTINUED)

IDT54/74FCT853 NON-INVERTING LATCH OPTION

INPUTS						OUTPUTS				FUNCTION
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	$\overline{EN}$	R_i (Σ OF H'S)	T_i INCL PARITY (Σ OF H'S)	R_i	T_i	PARITY	$\overline{ERR}$(1)	
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	H	H	NA	
L	H	–	–	L (Odd)	NA	NA	L	L	NA	
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	L	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	L	L	NA	H (Even)	H	NA	NA	L	
H	L	L	L	NA	L (Odd)	L	NA	NA	H	
H	L	L	L	NA	L (Even)	L	NA	NA	L	
H	L	H	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port, pass the error test resulting to error flag; transmitting path is disabled.
H	L	H	L	NA	H (Even)	H	NA	NA	L	
H	L	H	L	NA	L (Odd)	L	NA	NA	H	
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	H	NA	–	–	NA	NA	*	Store the state of error flag register.
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register.
H	H	H	H	–	–	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	H	–	–	Z	Z	Z	H	
H	H	–	L	L (Odd)	–	Z	Z	Z	H	
H	H	–	L	H (Even)	–	Z	Z	Z	L	
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

IDT54/74FCT854 INVERTING LATCH OPTION (2)

INPUTS						OUTPUTS				FUNCTION
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	$\overline{EN}$	R_i (Σ OF H'S)	T_i INCL PARITY (Σ OF H'S)	R_i	T_i	PARITY	$\overline{ERR}$(1)	
L	H	–	–	H (Odd)	NA	NA	L	H	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	L	L	NA	
L	H	–	–	L (Odd)	NA	NA	H	H	NA	
L	H	–	–	L (Even)	NA	NA	H	L	NA	
H	L	L	L	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	L	L	NA	H (Even)	L	NA	NA	L	
H	L	L	L	NA	L (Odd)	H	NA	NA	H	
H	L	L	L	NA	L (Even)	H	NA	NA	L	
H	L	H	L	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port, pass the error test resulting to error flag; transmitting path is disabled.
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	L	NA	L (Odd)	H	NA	NA	H	
H	L	H	L	NA	L (Even)	H	NA	NA	L	
H	L	H	H	NA	–	–	NA	NA	*	Store the state of error flag register.
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register.
H	H	H	H	–	–	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	H	–	–	Z	Z	Z	H	
H	H	–	L	L (Odd)	–	Z	Z	Z	L	
H	H	–	L	H (Even)	–	Z	Z	Z	H	
L	L	–	–	H (Odd)	NA	NA	L	L	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	L	H	NA	
L	L	–	–	L (Odd)	NA	NA	H	L	NA	
L	L	–	–	L (Even)	NA	NA	H	H	NA	

H = High
L = Low
Z = High impedance
NC = No Change

NA = Not Applicable
*Store the Error State of the Last Receive Cycle
– = Don't Care or Irrelevant

Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7

NOTES:
1. Output state assumes HIGH output pre-state.
2. Note that for negative logic levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1".

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)			MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level			2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level			–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.		V_I = V_{CC}	–	–	5	µA
				V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)			V_I = 0.5V	–	–	-5(4)	
				V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.		V_I = V_{CC}	–	–	15	µA
				V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)			V_I = 0.5V	–	–	-15(4)	
				V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA			–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND			-60	-120	–	mA
V_{OH}	Output HIGH Voltage (Except $\overline{ERR}$)	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA			V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		I_{OH} = –300µA	V_{HC}	V_{CC}	–	
				I_{OH} = –15mA MIL.	2.4	4.3	–	
				I_{OH} = –24mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA			–	GND	V_{LC}	V
		V_{CC} = Min.	All other outputs V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
				I_{OL} = 32mA MIL.	–	0.3	0.5	
				I_{OL} = 48mA COM'L.	–	0.3	0.5	
			$\overline{ERR}$	I_{OL} = 48mA	–	0.3	0.5	
V_H	Input Hysteresis on T_I and R_I	–			–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \leq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open $\overline{OE}_T = \overline{OE}_R$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current(6)	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (CLK or $\overline{EN}$) 50% Duty Cycle $\overline{OE}_T$ = GND $\overline{OE}_R = V_{CC}$ f_I = 2.5MHz One Input Toggling	$V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ (FCT)	–	1.2	3.4	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.6	5.4	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (CLK or $\overline{EN}$) 50% Duty Cycle $\overline{OE}_T$ = GND f_I = 2.5MHz $\overline{OE}_R = V_{CC}$ Eight Inputs Toggling	$V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ (FCT)	–	3.8	7.8(5)	
			V_{IN} = 3.4V V_{IN} = GND	–	6.0	16.8(5)	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER TEMPERATURE RANGE

PARAMETERS	DESCRIPTION		TEST CONDITIONS(4)	IDT54/74FCT8XXA(3) COM'L. MIN.	IDT54/74FCT8XXA(3) COM'L. MAX.	IDT54/74FCT8XXA(3) MIL. MIN.	IDT54/74FCT8XXA(3) MIL. MAX.	IDT54/74FCT8XXB(3) COM'L. MIN.	IDT54/74FCT8XXB(3) COM'L. MAX.	IDT54/74FCT8XXB(3) MIL. MIN.	IDT54/74FCT8XXB(3) MIL. MAX.	UNIT
t_{PLH}	Propagation Delay R_I to T_I, T_I to R_I		C_L = 50pF	–	10.0	–	14.0	–	7.0	–	10.0	ns
t_{PHL}				–	10.0	–	14.0	–	7.0	–	10.0	ns
t_{PLH}			C_L = 300pF(6)	–	17.5	–	21.5	–	14.5	–	17.5	ns
t_{PHL}				–	17.5	–	21.5	–	14.5	–	17.5	ns
t_{PLH}	Propagation Delay R_I to PARITY		C_L = 50pF	–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PHL}				–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PLH}			C_L = 300pF(6)	–	22.5	–	27.5	–	18.0	–	21.5	ns
t_{PHL}				–	22.5	–	27.5	–	18.0	–	21.5	ns
t_{PZH}	Output Enable Time $\overline{OE}_R$, $\overline{OE}_T$ to R_I, T_I		C_L = 50pF	–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{PZL}				–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{PZH}			C_L = 300pF(6)	–	19.5	–	23.5	–	16.0	–	18.5	ns
t_{PZL}				–	19.5	–	23.5	–	16.0	–	18.5	ns
t_{PHZ}	Output Disable Time $\overline{OE}_R$, $\overline{OE}_T$ to R_I, T_I		C_L = 5pF(6)	–	10.7	–	14.7	–	7.2	–	9.8	ns
t_{PLZ}				–	10.7	–	14.7	–	7.2	–	9.8	ns
t_{PHZ}			C_L = 50pF	–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{PLZ}				–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{SU}	T_I, PARITY to CLK Set-up Time (1)		C_L = 50pF	12.0	–	16.0	–	8.5	–	11.0	–	ns
t_H	T_I, PARITY to CLK Hold Time (1)			0	–	0	–	0	–	0	–	ns
t_{SU}	Clear Recovery Time $\overline{CLR}$ to CLK (2)			–	15.0	–	20.0	–	10.5	–	14.0	ns
t_W	Clock Pulse Width (1)	HIGH		7.0	–	9.5	–	5.5	–	7.0	–	ns
		LOW		7.0	–	9.5	–	5.5	–	7.0	–	ns
t_W	Clear Pulse Width	LOW		7.0	–	9.5	–	5.5	–	7.0	–	ns
t_{PHL}	Propagation Delay CLK to $\overline{ERR}$ (1)		C_L = 50pF	–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$		C_L = 50pF	–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{PLH}	Propagation-Delay T_I, PARITY TO $\overline{ERR}$ (PASS Mode Only) IDT54/74FCT853 and IDT54/74FCT854		C_L = 50pF	–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PHL}				–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PLH}	Propagation Delay $\overline{OE}_R$ to PARITY		C_L = 50pF	–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PHL}				–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PLH}			C_L = 300pF(6)	–	22.5	–	27.5	–	18.0	–	21.5	ns
t_{PHL}				–	22.5	–	27.5	–	18.0	–	21.5	ns

NOTES:
1. For IDT54/74FCT853/54, replace CLK with $\overline{EN}$.
2. Not applicable to IDT54/74FCT853/54.
3. XX represents 33, 34, 53 and 54.
4. See test circuit and waveforms.
5. Minimum limits are guaranteed but not tested on Propagation Delays.
6. These parameters are guaranteed but not tested.

ORDERING INFORMATION

IDTXXFCT	XXXX	A	A
Temp. Range	Device Type	Package	Process/Temperature

Process/Temperature

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

P	Plastic DIP
D	Cerdip
L	Leadless Chip Carrier
SO	Small Outline IC
E	CERPACK

Device Type

833A	Non-inverting Parity Bus Transceiver (Register Option)
833B	Fast non-inverting Parity Bus Transceiver (Register Option)
834A	Inverting Parity Bus Transceiver (Register Option)
834B	Fast inverting Parity Bus Transceiver (Register Option)
853A	Non-inverting Parity Bus Transceiver (Latch Option)
853B	Fast non-inverting Parity Bus Transceiver (Latch Option)
854A	Inverting Parity Bus Transceiver (Latch Option)
854B	Fast inverting Parity Bus Transceiver (Latch Option)

Temp. Range

54	-55°C to +125°C
74	0°C to +70°C

HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

IDT54/74FCT841A/B–IDT54/74FCT846A/B
(Replaces 39C841-46)

Integrated Device Technology, Inc.

FEATURES:

- Equivalent to AMD's Am29841-46 bipolar registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed parallel latches
  - Non-inverting transparent t_{PD} = 5.5ns typ.
  - Inverting transparent t_{PD} = 6.0ns typ.
- Buffered common latch enable, clear and preset input
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 Series (5μA max.)
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

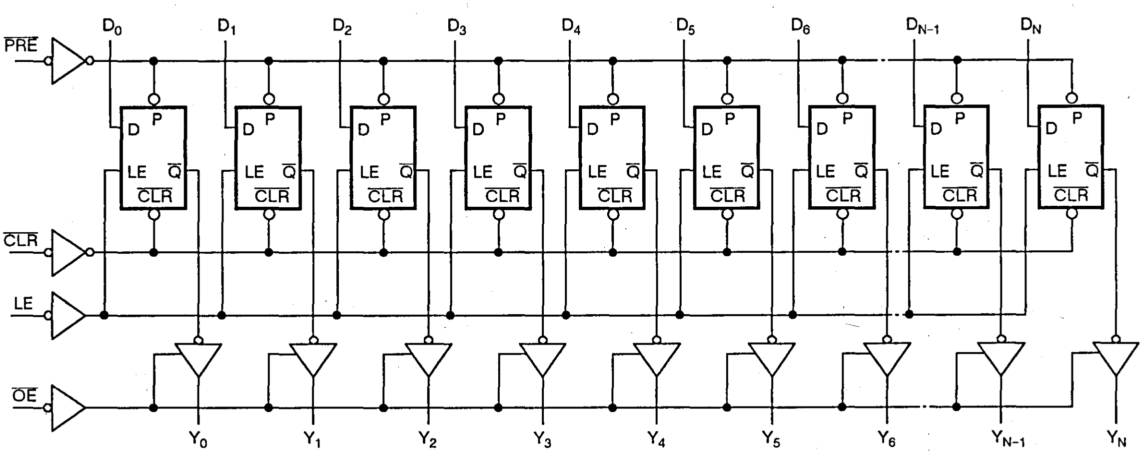
DESCRIPTION:

The IDT54/74FCT800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT840 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841 and IDT54/74FCT842 are buffered, 10-bit wide versions of the popular '373 function. The IDT54/74FCT843 and IDT54/74FCT844 are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance systems. The IDT54/74FCT845 and IDT54/74FCT846 are 8-bit buffered latches with all the '843/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT SELECTOR GUIDE

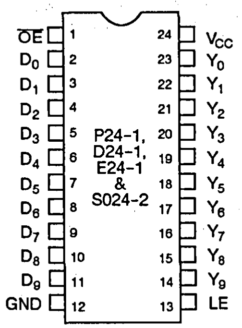
	DEVICE		
	10-BIT	9-BIT	8-BIT
Non-inverting	54/74FCT841A/B	54/74FCT843A/B	54/74FCT845A/B
Inverting	54/74FCT842A/B	54/74FCT844A/B	54/74FCT846A/B

CEMOS is a trademark of Integrated Device Technology, Inc.

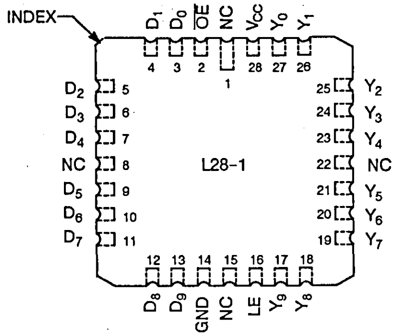
PIN CONFIGURATIONS

LOGIC SYMBOLS

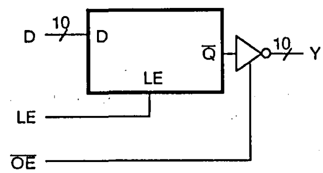
IDT54/74FCT841/IDT54/74FCT842 10-BIT LATCHES



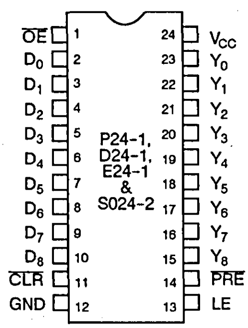
DIP/CERPACK/SOIC
TOP VIEW



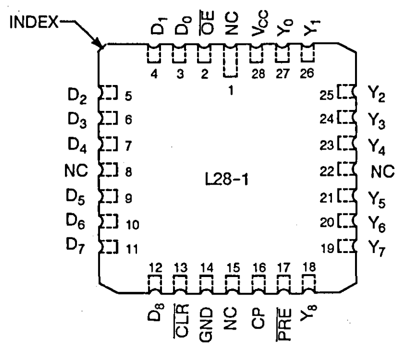
LCC
TOP VIEW



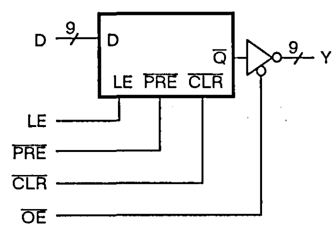
IDT54/74FCT843/IDT54/74FCT844 9-BIT LATCHES



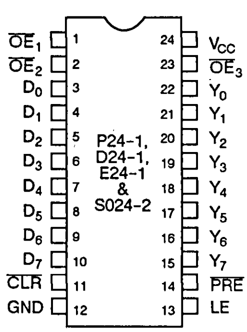
DIP/CERPACK/SOIC
TOP VIEW



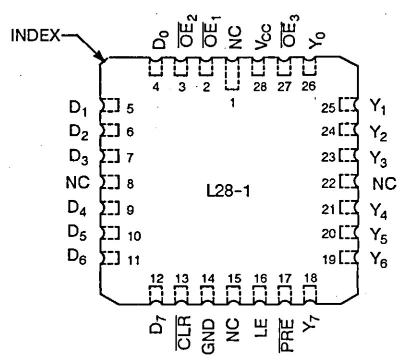
LCC
TOP VIEW



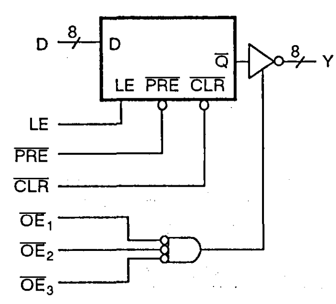
IDT54/74FCT845/IDT54/74FCT846 8-BIT LATCHES



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW



PIN DESCRIPTION

NAME	I/O	DESCRIPTION
IDT54/74FCT841/43/45 (Non-inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_I	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_I	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_I are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.
IDT54/74FCT842/44/46 (Inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_I	I	The latch inverting data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_I	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_I are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

FUNCTION TABLES [1]
IDT54/74FCT841/43/45

INPUTS					INTERNAL	OUTPUTS	FUNCTION
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_I	Q_I	Y_I	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

FUNCTION TABLES [1]
IDT54/74FCT842/44/46

INPUTS					INTERNAL	OUTPUTS	FUNCTION
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_I	Q_I	Y_I	
H	H	H	X	X	X	Z	High Z
H	H	H	H	H	L	Z	High Z
H	H	H	H	L	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER [1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following conditions apply unless otherwise specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP. [2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5 [4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5 [4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10 [4]	
			V_O = 0.5V	–	–	-10 [4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max. [3], V_O = GND		-75	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -15mA MIL.	2.4	4.3	–	
			I_{OH} = -24mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current (4)	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current (6)	V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5(5)	
			V_{IN} = 3.4V V_{IN} = GND	–	5.0	14.5(5)	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

10

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETER	DESCRIPTION	TEST CONDITIONS[1]	IDT54/74FCT841A-46A				IDT54/74FCT841B-46B				UNIT
			COM'L.		MIL.		COM'L.		MIL.		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} (IDT54/74FCT841, 43, 45) t_{PHL}	Data (D_I) to Output (Y_I) (LE = HIGH)	C_L = 50pF R_L = 500Ω	–	9.5	–	11	–	6.5	–	7.5	ns
t_{PLH} t_{PHL}		C_L = 300pF[3] R_L = 500Ω	–	13	–	15	–	13	–	15	ns
t_{SU}	Data to LE Set-up Time	C_L = 50pF R_L = 500Ω	2.5	–	2.5	–	2.5	–	2.5	–	ns
t_H	Data to LE Hold Time		2.5	–	3	–	2.5	–	2.5	–	ns
t_{PLH} (IDT54/74FCT842, 44, 46) t_{PHL}	Data (D_I) to Output (Y_I) (LE = HIGH)	C_L = 50pF R_L = 500Ω	–	10	–	12	–	8.0	–	9.0	ns
t_{PLH} t_{PHL}		C_L = 300pF[3] R_L = 500Ω	–	13	–	15	–	13	–	15	ns
t_{SU}	Data to LE Set-up Time	C_L = 50pF R_L = 500Ω	2.5	–	2.5	–	2.5	–	2.5	–	ns
t_H	Data to LE Hold Time		2.5	–	3	–	2.5	–	2.5	–	ns
t_{PLH} t_{PHL}	Latch Enable (LE) to Y_I	C_L = 50pF R_L = 500Ω	–	12	–	16	–	8.0	–	10.5	ns
t_{PLH} t_{PHL}		C_L = 300pF[3] R_L = 500Ω	–	16	–	20	–	15.5	–	18	ns
t_{PLH}	Propagation Delay, Preset to Y_I	C_L = 50pF R_L = 500Ω	–	12	–	14	–	8.0	–	10	ns
t_{SU}	Preset Recovery ($\overline{PRE}$ ⨼) Time		–	14	–	17	–	10	–	13	ns
t_{PHL}	Propagation Delay, Clear to Y_I		–	13	–	15	–	10	–	11	ns
t_{SU}	Clear Recovery ($\overline{CLR}$ ⨼) Time		–	14	–	17	–	10	–	10	ns
t_{PWH}	LE Pulse Width HIGH	C_L = 50pF R_L = 500Ω	6	–	6	–	4	–	4	–	ns
t_{PWL}	Preset Pulse Width LOW		8	–	9	–	4	–	4	–	ns
t_{PWL}	Clear Pulse Width LOW		8	–	9	–	4	–	4	–	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ ⨽ to Y_I	C_L = 50pF R_L = 500Ω	–	14	–	15	–	8	–	8.5	ns
t_{PZH} t_{PZL}		C_L = 300pF[3] R_L = 500Ω	–	23	–	25	–	14	–	15	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ ⨼ to Y_I	C_L = 5pF[3] R_L = 500Ω	–	9	–	10	–	6	–	6.5	ns
t_{PHZ} t_{PLZ}		C_L = 50pF R_L = 500Ω	–	12	–	12	–	7.0	–	7.5	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not tested.

ORDERING INFORMATION

IDTXXFCT	XXXX	X	X
Temp. Range	Device Type	Package	Process

Process

Blank	Commercial
B	MIL-STD-883, Class B

Package

P	Plastic DIP
D	CERDIP
E	CERPACK
L	Leadless Chip Carrier
SO	Small Outline IC

Device Type

841A	10-Bit Non-inverting Latch
842A	10-Bit Inverting Latch
843A	9-Bit Non-inverting Latch
844A	9-Bit Inverting Latch
845A	8-Bit Non-inverting Latch
846A	8-Bit Inverting Latch
841B	Fast 10-Bit Non-inverting Latch
842B	Fast 10-Bit Inverting Latch
843B	Fast 9-Bit Non-inverting Latch
844B	Fast 9-Bit Inverting Latch
845B	Fast 8-Bit Non-inverting Latch
846B	Fast 8-Bit Inverting Latch

Temp. Range

54	-55°C to +125°C
74	0°C to +70°C

10

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS TRANSCEIVERS

IDT54/74FCT861A/B IDT54/74FCT864A/B (Replaces 39C861-64)

FEATURES:

- Equivalent to AMD's Am29861-64 bipolar registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed symmetrical bidirectional transceivers
  - Non-inverting t_{PD} = 5.5ns typ.
  - Inverting t_{PD} = 6.0ns typ.
- I_{OL} = 48mA (commercial), and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (5µW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 Series (5µA max.)
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

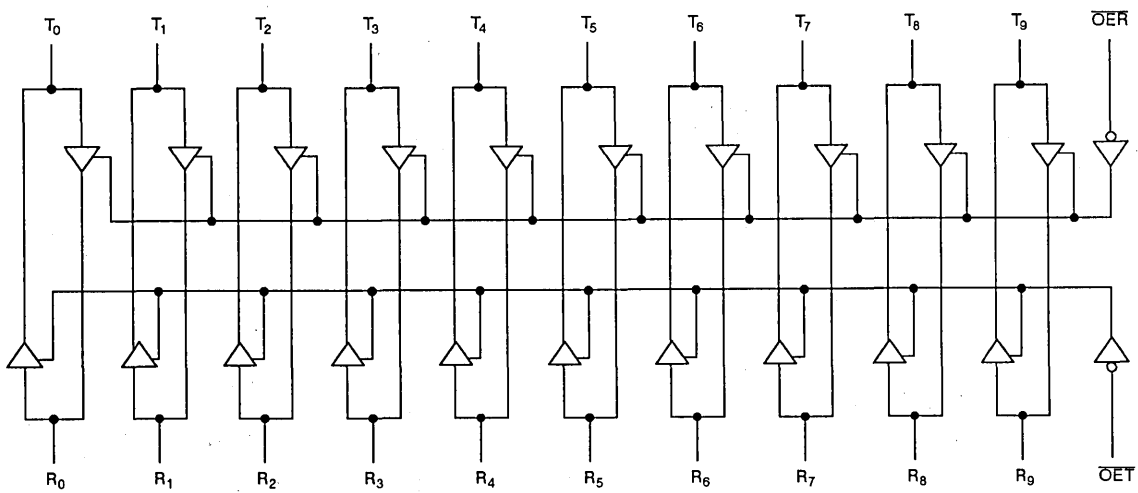
DESCRIPTION:

The IDT54/74FCT800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT860 Series bus transceivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The IDT54/74FCT863/64 9-bit transceivers have NOR-ed output enables for maximum control flexibility.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM
IDT54/74FCT861/IDT54/74FCT862 10-BIT TRANSCEIVERS

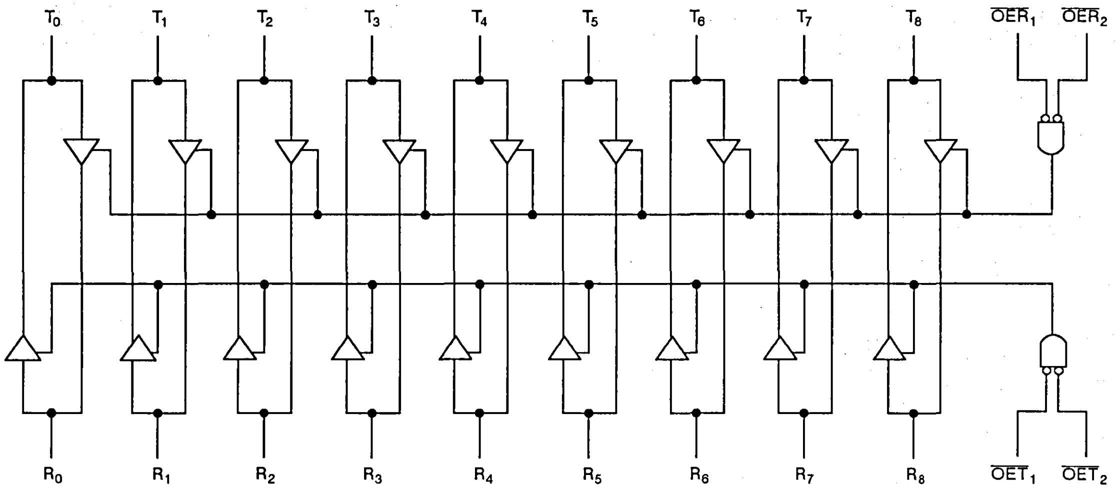


PRODUCT SELECTOR GUIDE

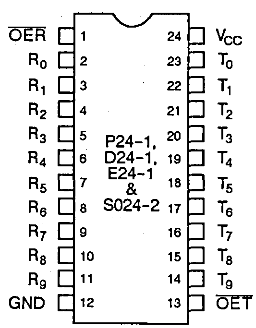
	DEVICE	
	10-BIT	9-BIT
Non-inverting	IDT54/74FCT861	IDT54/74FCT863
Inverting	IDT54/74FCT862	IDT54/74FCT864

CEMOS is a trademark of Integrated Device Technology, Inc.

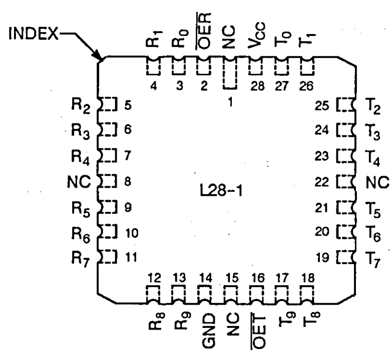
FUNCTIONAL BLOCK DIAGRAM
IDT54/74FCT863/IDT54/74FCT864 9-BIT TRANSCEIVERS



PIN CONFIGURATIONS
IDT54/74FCT861/IDT54/74FCT862 10-BIT TRANSCEIVERS

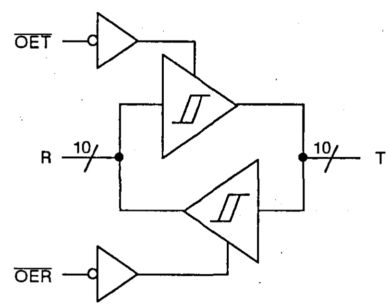


DIP/CERPACK/SOIC
TOP VIEW

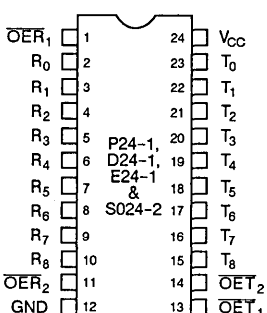


LCC
TOP VIEW

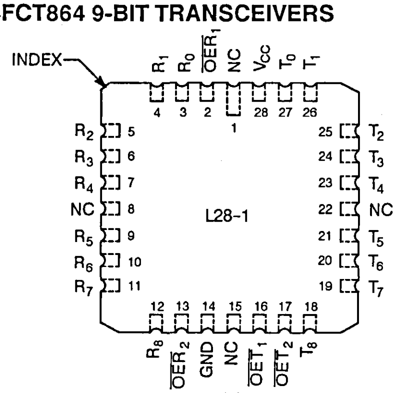
LOGIC SYMBOLS
IDT54/74FCT861



IDT54/74FCT863/IDT54/74FCT864 9-BIT TRANSCEIVERS

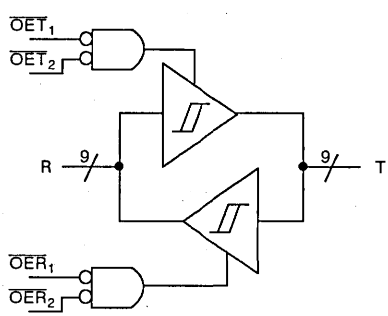


DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

IDT54/74FCT863



PIN DESCRIPTION

NAME	I/O	DESCRIPTION
IDT54/74FCT861/62		
$\overline{OER}$	I	When LOW in conjunction with $\overline{OET}$, HIGH activates the RECEIVE mode.
$\overline{OET}$	I	When LOW in conjunction with $\overline{OER}$, HIGH activates the TRANSMIT mode.
R_I	I/O	10-bit RECEIVE input/output.
T_I	I/O	10-bit TRANSMIT input/output.
IDT54/74FCT863/64		
$\overline{OER}_I$	I	When LOW in conjunction with $\overline{OET}_I$, HIGH activates the RECEIVE mode.
$\overline{OET}_I$	I	When LOW in conjunction with $\overline{OER}_I$, HIGH activates the TRANSMIT mode.
R_I	I/O	9-bit RECEIVE input/output.
T_I	I/O	9-bit TRANSMIT input/output.

FUNCTION TABLES (1)
IDT54/74FCT861/63 (Non-inverting)

INPUTS				OUTPUTS		FUNCTION
$\overline{OET}$	$\overline{OER}$	R_I	T_I	R_I	T_I	
L	H	L	N/A	N/A	L	Transmitting
L	H	H	N/A	N/A	H	Transmitting
H	L	N/A	L	L	N/A	Receiving
H	L	N/A	H	H	N/A	Receiving
H	H	X	X	Z	Z	High Z

NOTE:
1. H = HIGH, L = LOW, Z = High Impedance, X = Don't Care, N/A = Not Applicable

FUNCTION TABLES (1)
IDT54/74FCT862/64 (Inverting)

INPUTS				OUTPUTS		FUNCTION
$\overline{OET}$	$\overline{OER}$	R_I	T_I	R_I	T_I	
L	H	L	N/A	N/A	H	Transmitting
L	H	H	N/A	N/A	L	Transmitting
H	L	N/A	L	H	N/A	Receiving
H	L	N/A	H	L	N/A	Receiving
H	H	X	X	Z	Z	High Z

NOTE:
1. H = HIGH, L = LOW, Z = High Impedance, X = Don't Care, N/A = Not Applicable

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER [1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP. [2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.,	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5 [4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5 [4]	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.,	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15 [4]	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15 [4]	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-75	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -15mA MIL.	2.4	4.3	–	
			I_{OH} = -24mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on T_I and R_I Only	–		–	200	–	mV

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND $T/\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC}\, D_H N_T + I_{CCD}\,(f_{CP}/2 + f_I\, N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETER	DESCRIPTION	TEST CONDITIONS(1)	IDT54/74FCT861A-64A				IDT54/74FCT861B-64B				UNIT
			COM'L.		MIL.		COM'L.		MIL.		
			MIN.(2)	MAX.	MIN.(2)	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay from R_I to T_I or T_I to R_I IDT54/74FCT861/IDT54/74FCT863 (Non-inverting)	C_L = 50pF R_L = 500Ω	–	8	–	10	–	6.0	–	6.5	ns
t_{PLH} t_{PHL}		C_L = 300pF(3) R_L = 500Ω	–	15	–	17	–	13	–	14	ns
t_{PLH} t_{PHL}	Propagation Delay from R_I to T_I or T_I to R_I IDT54/74FCT862/IDT54/74FCT864 (Inverting)	C_L = 50pF R_L = 500Ω	–	7.5	–	9.5	–	5.5	–	6.5	ns
t_{PLH} t_{PHL}		C_L = 300pF(3) R_L = 500Ω	–	14	–	16	–	13	–	14	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OET}$ to T_I or $\overline{OER}$ to R_I	C_L = 50pF R_L = 500Ω	–	15	–	17	–	8.0	–	9.0	ns
t_{PZH} t_{PZL}		C_L = 300pF(3) R_L = 500Ω	–	20	–	22	–	15	–	16	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OET}$ to T_I or $\overline{OER}$ to R_I	C_L = 5pF(3) R_L = 500Ω	–	9	–	10	–	6	–	7	ns
t_{PHZ} t_{PLZ}		C_L = 50pF R_L = 500Ω	–	17	–	19	–	7.0	–	8.0	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not tested.

ORDERING INFORMATION

IDTXXFCT (Temp. Range) XXXX (Device Type) X (Package) X (Process)

Process:
- Blank — Commercial
- B — MIL-STD-883, Class B

Package:
- P — Plastic DIP
- D — CERDIP
- E — CERPACK
- SO — Small Outline IC
- L — Leadless Chip Carrier

Device Type:
- 861 — 10-Bit Non-Inverting Transceiver
- 862 — 10-Bit Inverting Transceiver
- 863 — 9-Bit Non-Inverting Transceiver
- 864 — 9-Bit Inverting Transceiver

Temp. Range:
- 54 — -55°C to +125°C
- 74 — 0°C to +70°C

10

Integrated Device Technology, Inc.

HIGH-SPEED CMOS 1-OF-8 DECODER

IDT54AHCT138

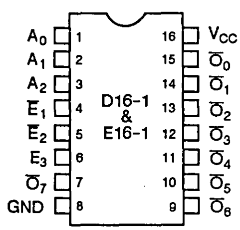
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 11ns typical address to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5µW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5µA max.)
- 1-of-8 decoder with enables
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

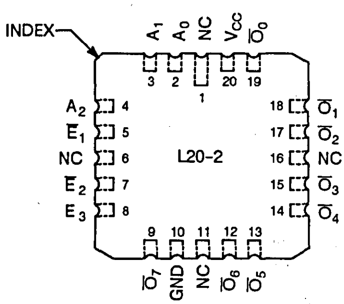
DESCRIPTION:

The IDT54AHCT138 are 1-of-8 decoders built using advanced CEMOS™, a dual metal CMOS technology. The IDT54AHCT138 accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\overline{O}_0$ - $\overline{O}_7$). The IDT54AHCT138 features three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four IDT54AHCT138 devices and one inverter.

PIN CONFIGURATIONS

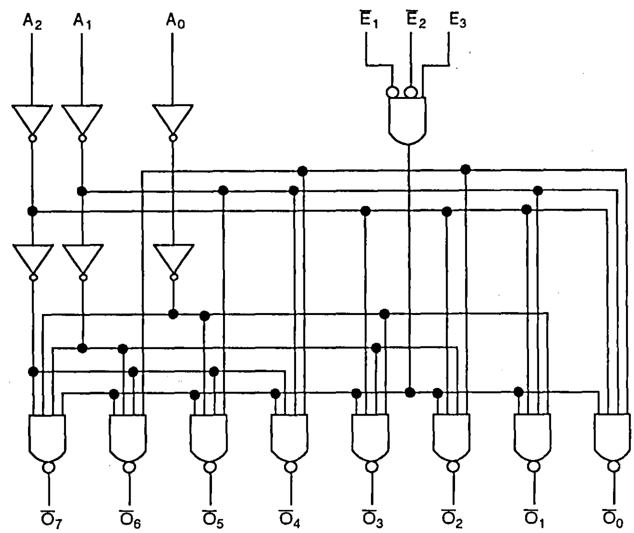


DIP/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER [1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP. [2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5.0	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.[3]		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	mA
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[5]	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply Current [4]	V_{CC} = Max. Outputs Open f_I = 1.0MHz 50% Duty Cycle One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.4	2.8	
		V_{CC} = Max. Outputs Open f_I = 250kHz 50% Duty Cycle Six Inputs Toggling	$V_{IN} \geq V_{HC}$[6] $V_{IN} \leq V_{LC}$ (AHCT)	–	0.23	2.0	
			V_{IN} = 3.4V or [6] V_{IN} = GND	–	1.7	8.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}\, D_H\, N_T + I_{CCD}\, (f_{CP}/2 + f_I\, N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$A_0 - A_2$	Address Inputs
$\bar{E}_1$, $\bar{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\bar{O}_0 - \bar{O}_7$	Outputs (Active LOW)

TRUTH TABLE

INPUTS						OUTPUTS							
$\bar{E}_1$	$\bar{E}_2$	E_3	A_0	A_1	A_2	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	TYP.	MIN.[2]	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay A_n to $\bar{O}_n$	$C_L = 50pF$ $R_L = 500\Omega$	11.0	1.5	27.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{E}_1$ or $\bar{E}_2$ to $\bar{O}_n$		13.0	1.5	20.0	ns
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\bar{O}_n$		13.0	1.5	20.0	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT — Temp. Range
XXXX — Device Type
X — Package
X — Process

Process:
- B — MIL-STD-883, Class B

Package:
- D — CERDIP
- L — Leadless Chip Carrier
- E — CERPACK

Device Type:
- 138 — 1-of-8 Decoder

Temp. Range:
- 54 — −55°C to +125°C

HIGH-SPEED DUAL 1-OF-4 DECODER

IDT54AHCT139

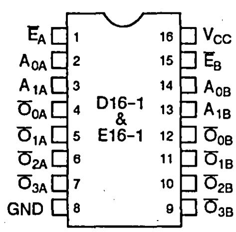
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 9ns typical address to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Dual 1-of-4 decoder with enable
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

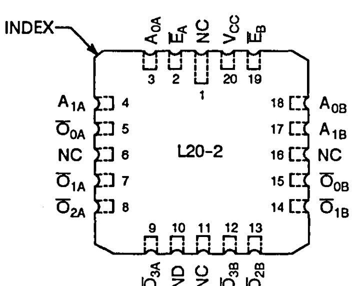
DESCRIPTION:

The IDT54AHCT139 are dual 1-of-4 decoders built using advanced CEMOS™, a dual metal CMOS technology. The device has two independent decoders, each of which accept two binary weighted inputs (A_0 - A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$ - $\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH, all outputs are forced HIGH.

PIN CONFIGURATIONS

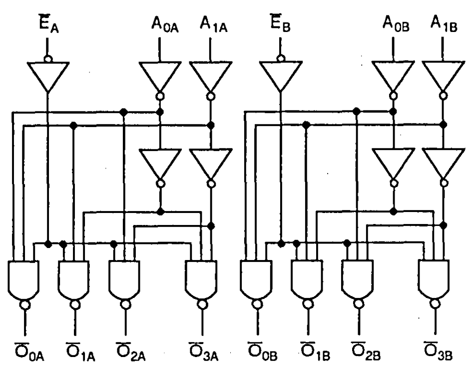


DIP/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5.0	µA
I_{SC}	Input Short Circuit Current	V_{CC} = Max.[3]		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	mA
		V_{CC} = Min.	I_{OH} = -150µA	V_{HC}	V_{CC}	–	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	–	GND	V_{LC}	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 14mA	–	–	0.4	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(5)	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply Current (4)	V_{CC} = Max. Outputs Open f_I = 1.0MHz 50% Duty Cycle One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			$V_{IN} = 3.4V$ V_{IN} = GND	–	0.4	2.8	
		V_{CC} = Max. Outputs Open f_I = 1.0MHz 50% Duty Cycle One Input Toggling on Each Decoder	$V_{IN} \geq V_{HC}$ (6) $V_{IN} \leq V_{LC}$ (AHCT)	–	0.3	2.1	
			$V_{IN} = 3.4V$ (6) V_{IN} = GND	–	0.8	4.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0V$, +25°C ambient and maximum loading.
3. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0, A_1	Address Inputs
$\overline{E}$	Enable Inputs (Active LOW)
$\overline{O}_0$-$\overline{O}_3$	Outputs (Active LOW)

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	TYP.	MIN.(2)	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	9.0	1.5	25.0	ns
t_{PLH} t_{PHL}	Propagation Delay E to $\overline{O}_n$		11.0	1.5	18.0	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT XXXX X X
Temp. Range, Device Type, Package, Process

Process:
B MIL-STD-883, Class B

Package:
D CERDIP
L Leadless Chip Carrier
E CERPACK

Device Type:
139 Dual 1-of-4 Decoder

Temp. Range:
54 -55°C to +125°C

Integrated Device Technology, Inc.

HIGH-SPEED CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

IDT54AHCT161/163

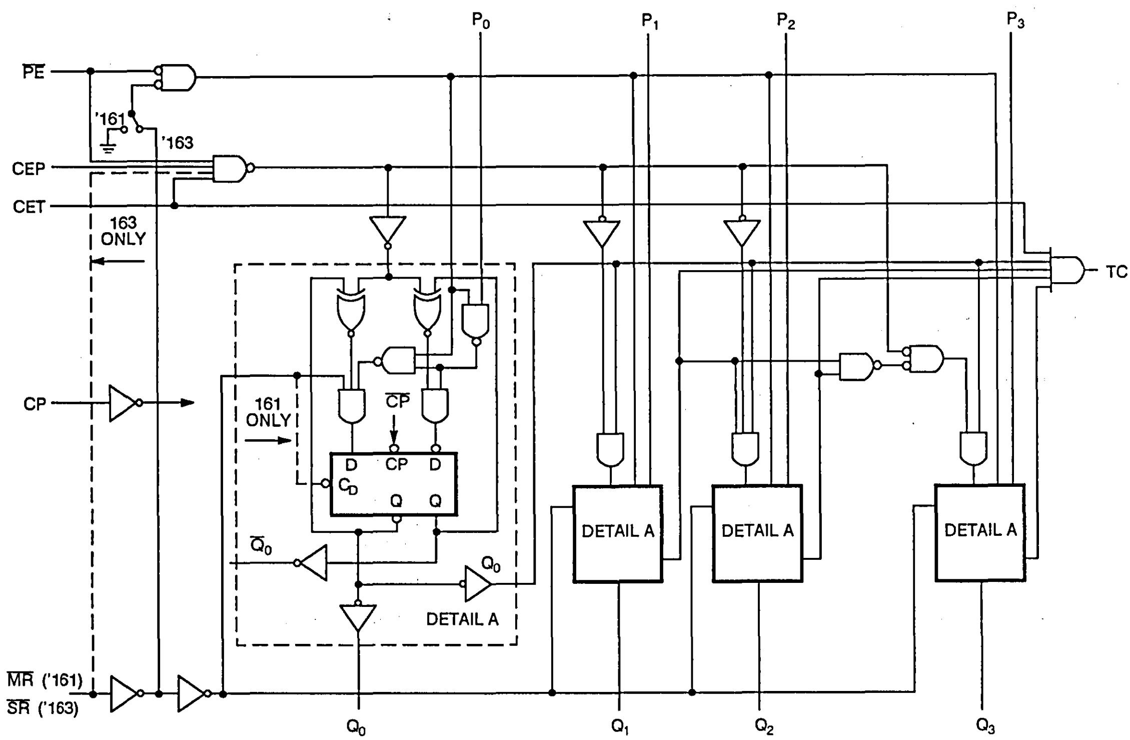
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54AHCT161/163 are high-speed synchronous modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multi-stage counters. The IDT54AHCT161 have asynchronous Master Reset inputs that override all other inputs and force the outputs LOW. The IDT54AHCT163 have synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAM

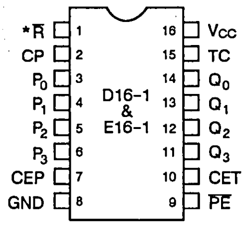


CEMOS is a trademark of Integrated Device Technology, Inc.

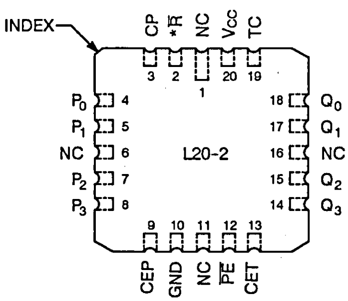
MILITARY TEMPERATURE RANGE **DECEMBER 1987**

DSC-4040/-

PIN CONFIGURATIONS



DIP/CERPACK
TOP VIEW



LCC/PLCC
TOP VIEW

* $\overline{MR}$ for 161
* $\overline{SR}$ for 163

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –150µA	V_{HC}	V_{CC}	–	
			I_{OH} = –1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:
1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS (IDT54AHCT161) V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Power Supply Current per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(4)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(5)	V_{CC} = Max. Outputs Open Count Mode CEP = CET = $\overline{MR}$ = $\overline{PE}$ = V_{HC} $P_{0-3} = V_{LC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.2	0.3	mA/MHz
I_{CC}	Total Power Supply Current(4)	V_{CC} = Max. Outputs Open f_{CP} = 10MHz, 50% Duty Cycle Count Mode CEP = CET = $\overline{MR}$ = $\overline{PE}$ = V_{HC} $P_{0-3} = V_{LC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)(6)	–	1.0	3.0	mA
			CP V_{IN} = 3.4V or V_{IN} = GND(6)	–	1.3	4.0	

POWER SUPPLY CHARACTERISTICS (IDT54AHCT163) V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Power Supply Current per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(4)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(5)	V_{CC} = Max. Outputs Open Count Mode CEP = CET = $\overline{SR}$ = $\overline{PE}$ = V_{HC} $P_{0-3} = V_{LC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.2	0.3	mA/MHz
I_{CC}	Total Power Supply Current(4)	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz, 50% Duty Cycle Count Mode CEP = CET = $\overline{SR}$ = $\overline{PE}$ = V_{HC} $P_{0-3} = V_{LC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)(6)	–	1.0	3.0	mA
			CP V_{IN} = 3.4V or(6) V_{IN} = GND	–	1.3	4.0	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = ClockFrequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('163)	Synchronous Reset Input (Active LOW)
P_{0-3}	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q_{0-3}	Flip-Flop Outputs
TC	Terminal Count Output

TRUTH TABLE

$\overline{SR}$ (1)	$\overline{PE}$	CET	CEP	ACTION ON THE RISING CLOCK EDGE (_┌‾)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

NOTES:
1. For AHCT163 only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	TYP.	MIN.(2)	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	C_L = 50pF R_L = 500Ω	12.0	2.0	20.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)		12.0	2.0	20.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		18.0	2.0	30.0	ns
t_{PHL} t_{PHL}	Propagation Delay CET to TC		10.0	1.5	16.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n (161)		10.0	2.0	27.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC		10.0	2.0	31.0	ns
t_S (H) t_S (L)	Set-up Time, HIGH or LOW P_n to CP		–	20.0	–	ns
t_H (H) t_H (L)	Hold Time, HIGH or LOW P_n to CP		–	0	–	ns
t_S (H) t_S (L)	Set-up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		–	20.0	–	ns
t_H (H) t_H (L)	Set-up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		–	0	–	ns
t_S (H) t_S (L)	Set-up Time, HIGH or LOW CEP or CET to CP		–	25.0	–	ns
t_H (H) t_H (L)	Set-up Time, HIGH or LOW CEP to CET to CP		–	0	–	ns
t_W(H) t_W(L)	Clock Pulse Width (Load) HIGH or LOW		–	20.0	–	ns
t_W(H) t_W(L)	Clock Pulse Width (Count) HIGH or LOW		–	20.0	–	ns
t_W(L)	$\overline{MR}$ Pulse Width, LOW (161)		–	20.0	–	ns
t_{REC}	Recovery Time $\overline{MR}$ to CP (161)		–	20.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

10

ORDERING INFORMATION

IDTXXAHCT (Temp. Range) XXXX (Device Type) X (Package) X (Process)

Field	Code	Description
Process	B	MIL-STD-883, Class B
Package	D	CERDIP
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	161	Synchronous Presettable Binary Counter with Asynchronous Master Reset
	163	Synchronous Presettable Binary Counter with Synchronous Reset
Temp. Range	54	-55°C to +125°C

Integrated Device Technology, Inc.

HIGH-SPEED CMOS CARRY LOOKAHEAD GENERATOR

IDT54AHCT182

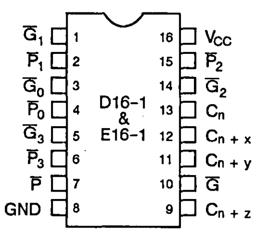
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 8ns typical propagation delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Carry lookahead generator
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

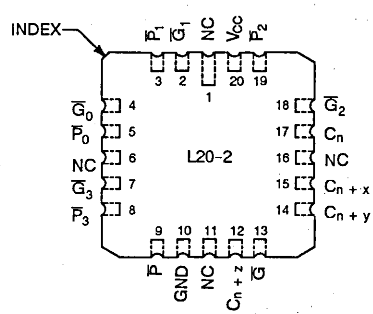
DESCRIPTION:

The IDT54AHCT182 is a lookahead generator built using advanced CEMOS™, a dual metal CMOS technology. The IDT54AHCT182 is generally used with a 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

PIN CONFIGURATIONS

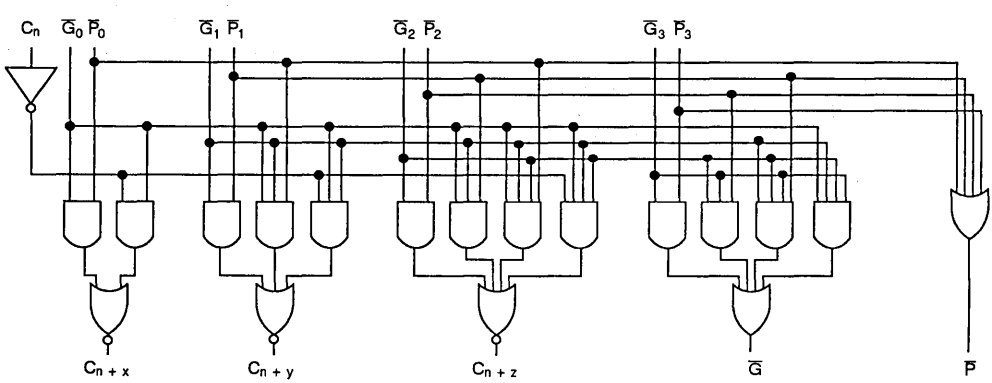


DIP/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5.0	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5.0	μA
I_{SC}	Short Circuit Current	V_{CC} = Max. (3)		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32μA		V_{HC}	V_{CC}	–	mA
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –200μA	V_{HC}	V_{CC}	–	V
			I_{OH} = –12mA	2.4	4.3	–	V
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	V
			I_{OL} = 14mA	–	–	0.4	V

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(5)	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.3	mA/MHz
I_{CC}	Total Power Supply Current (4)	V_{CC} = Max. Outputs Open f_I = 1.0MHz 50% Duty Cycle One Bit Toggling	$V_{IN} \geq V_{HC}$ (6) $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or (6) V_{IN} = GND	–	0.4	2.8	mA

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
C_n	Carry Input
$\bar{G}_0$, $\bar{G}_2$	Carry Generate Inputs (Active LOW)
$\bar{G}_1$	Carry Generate Input (Active LOW)
$\bar{G}_3$	Carry Generate Input (Active LOW)
$\bar{P}_0$, $\bar{P}_1$	Carry Propagate Inputs (Active LOW)
$\bar{P}_2$	Carry Propagate Input (Active LOW)
$\bar{P}_3$	Carry Propagate Input (Active LOW)
C_{n+x}–C_{n+z}	Carry Outputs
$\bar{G}$	Carry Generate Output (Active LOW)
$\bar{P}$	Carry Propagate Output (Active LOW)

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	G_0	P_0	G_1	P_1	G_2	P_2	G_3	P_3	C_{n+x}	C_{n+y}	C_{n+z}	$\bar{G}$	$\bar{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	TYP.	MIN.[2]	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+x}, C_{n+y}, C_{n+z}		8.0	–	20.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{P}_0$, $\bar{P}_1$, or $\bar{P}_2$, to C_{n+x}, C_{n+y}, C_{n+z}		8.0	–	15.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{G}_0$, $\bar{G}_1$, or $\bar{G}_2$, to C_{n+x}, C_{n+y}, C_{n+z}	C_L = 50pF R_L = 500Ω	8.0	–	15.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{P}_1$, $\bar{P}_2$, or $\bar{P}_3$, to $\bar{G}$		9.0	–	20.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{G}_n$ to $\bar{G}$		9.5	–	20.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\bar{P}_n$ to $\bar{P}$		8.0	–	16.5	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT XXXX X X
Temp. Range / Device Type / Package / Process

Field	Code	Description
Process	B	MIL-STD-883, Class B
Package	D	CERDIP
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	182	Carry Lookahead Generator
Temp. Range	54	-55°C to +125°C

Integrated Device Technology, Inc.

HIGH-SPEED CMOS BINARY UP/DOWN COUNTER

IDT54AHCT191

FEATURES:

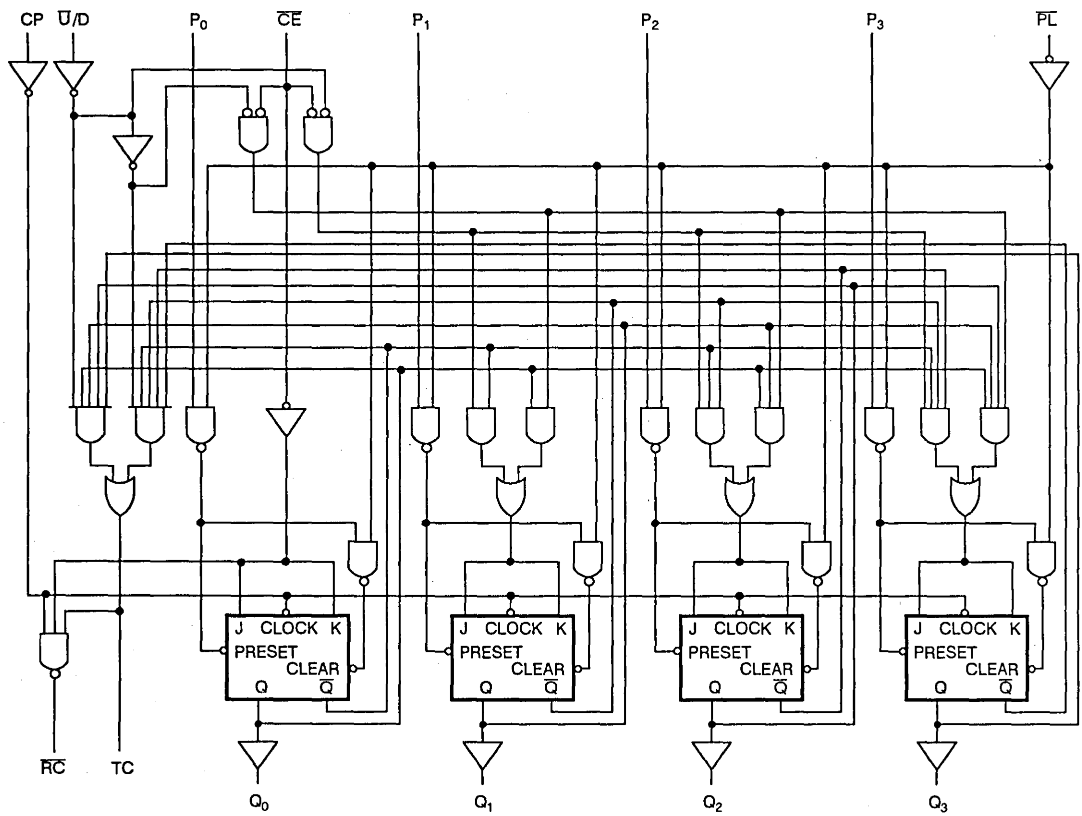
- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54AHCT191 is a reversible modulo-16 binary counter, featuring synchronous counting and asynchronous presetting, built using advanced CEMOS™, a dual metal CMOS technology.

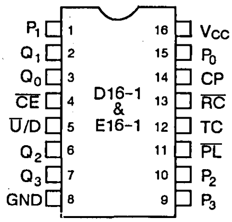
The preset feature allows the IDT54AHCT191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAM

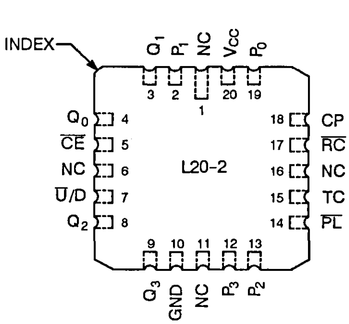


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/CERPACK
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

10

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5.0	µA
I_{SC}	Short Circuit Current	V_{CC} = Max. (3)		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	mA
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(5)	V_{CC} = Max. Outputs Open Count Up or Down $\overline{CE} = V_{LC}$ $\overline{PL} = P_0 - P_3 = V_{HC}$ $\overline{U}/D = V_{HC}$ or V_{LC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.2	0.3	mA/ MHz
I_{CC}	Total Power Supply Current (4)	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle Count Up or Down $\overline{CE} = V_{LC}$ $\overline{PL} = P_0 - P_3 = V_{HC}$ $\overline{U}/D = V_{HC}$ or V_{LC}	$V_{IN} \geq V_{HC}$ (6) $V_{IN} \leq V_{LC}$ (AHCT)	–	0.2	1.7	mA
			V_{IN} = 3.4V or (6) V_{IN} = GND	–	0.3	2.7	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

RC TRUTH TABLE

$\overline{CE}$	TC (1)	CP	$\overline{RC}$
L	H	⊔	⊔
H	X	X	H
X	L	X	H

NOTES:
1. TC is generated internally.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Count Pulse Input (Active Rising Edge)
P_{0-3}	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U}/D$	Up/Down Count Control Input
Q_{0-3}	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Clock Output (Active HIGH)

TRUTH TABLES
MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Preset (Asynch.)
H	H	X	X	No Change (Hold)

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	TYP.	MIN.[2]	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		–	1.5	22.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		–	2.0	34.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$		–	1.5	24.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$		–	2.0	21.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$		–	4.0	30.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to TC		–	3.0	30.0	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		–	1.5	25.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		–	3.0	34.0	ns
$t_S(H)$ $t_S(L)$	Set-up Time HIGH or LOW P_n to $\overline{PL}$	C_L = 50pF R_L = 500Ω	–	25.0	–	ns
$t_H(H)$ $t_H(L)$	Hold Time HIGH or LOW P_n to $\overline{PL}$		–	1.5	–	ns
$t_S(L)$	Set-up Time LOW $\overline{CE}$ to CP		–	25.0	–	
$t_H(L)$	Hold Time LOW $\overline{CE}$ to CP		–	0	–	
$t_S(H)$ $t_S(L)$	Set-up Time HIGH or LOW $\overline{U}$/D to CP		–	20.0	–	ns
$t_H(H)$ $t_H(L)$	Hold Time HIGH or LOW $\overline{U}$/D to CP		–	0	–	ns
$t_W(L)$	$\overline{PL}$ Pulse Width LOW		–	25.0	–	ns
$t_W(L)$	CP Pulse Width LOW		–	20.0	–	ns
t_{REC}	Recovery Time $\overline{PL}$ to CP		–	20.0	–	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT XXXX X X
Temp. Range / Device Type / Package / Process

B — MIL-STD-883, Class B

D — CERDIP
L — Leadless Chip Carrier
E — CERPACK

191 — Binary Up/Down Counter

54 — –55°C to +125°C

10

Integrated Device Technology, Inc.

HIGH-SPEED CMOS UP/DOWN BINARY COUNTER

IDT54AHCT193

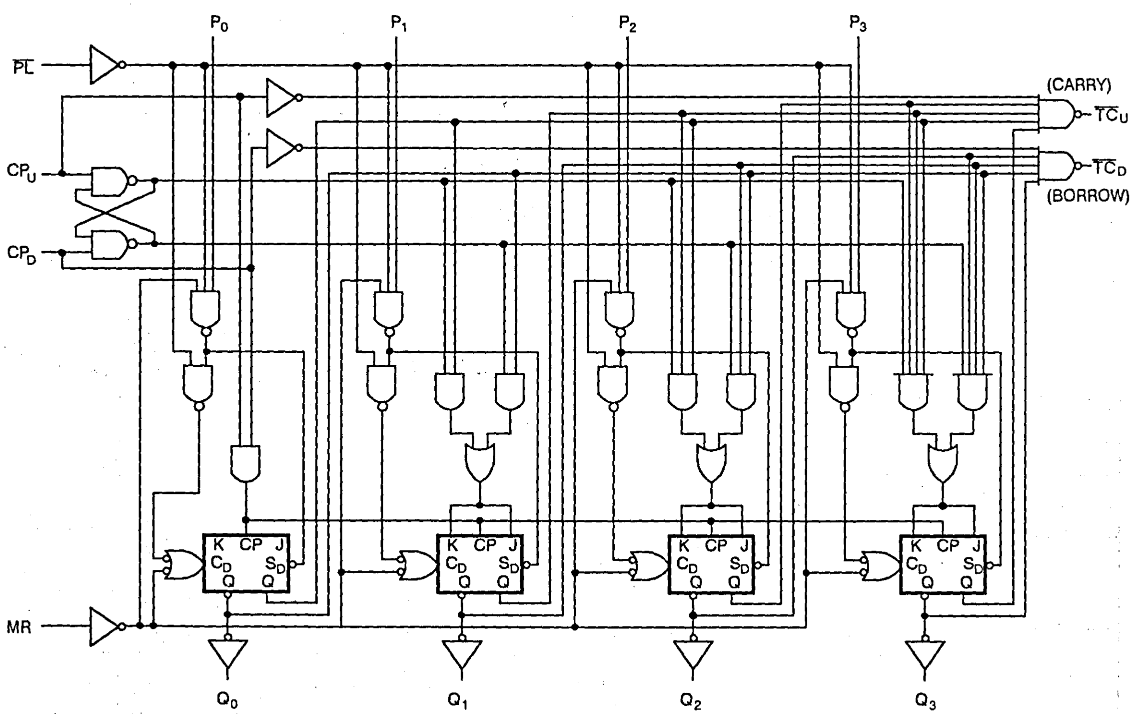
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

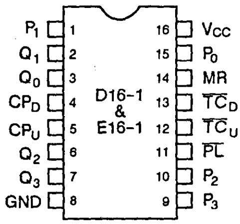
The IDT54AHCT193 is an up/down modulo-16 binary counter built using advanced CEMOS™, a dual metal CMOS technology. Separate count-up and count-down clocks are used and, in either counting mode, the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate Terminal Count-up and Terminal Count-down outputs are provided that are used as the clocks for subsequent stages without extra logic, thus simplifying multiusage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

FUNCTIONAL BLOCK DIAGRAM

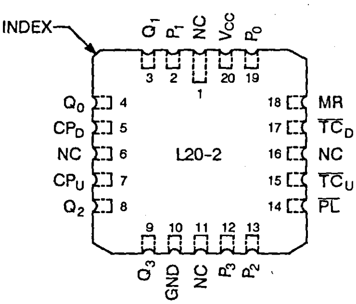


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/CERPACK TOP VIEW



LCC TOP VIEW

ABSOLUTE MAXIMUM RATINGS [(1)]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[(1)]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V + 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[(1)]		MIN.	TYP.[(2)]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.[(3)]		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	–	
			I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP_U} = f_{CP_D} = f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[5]	V_{CC} = Max. Outputs Open Count Up or Down $\overline{PL} = P_0 - P_3 = V_{HC}$ $MR = V_{LC}$	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.2	0.3	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle Count Up or Down $\overline{PL} = P_0 - P_3 = V_{HC}$ $MR = V_{LC}$	$V_{IN} \geq V_{HC}$[6] $V_{IN} \leq V_{LC}$ (AHCT)	–	0.2	1.7	mA
			V_{IN} = 3.4V or[6] V_{IN} = GND	–	0.3	2.7	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CP_U	Count Up Clock Input (Active Rising Edge)
CP_D	Count Down Clock Input (Active Rising Edge)
MR	Asynchronous Master Reset Input (Active HIGH)
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
P_{0-3}	Parallel Data Inputs
Q_{0-3}	Flip-Flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)

FUNCTION TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↑	H	Count Up
L	H	H	↑	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	TYP.	MIN.(2)	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D $\overline{TC}_U$ or $\overline{TC}_D$	C_L = 50pF R_L = 500Ω	–	2.0	19.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n		–	2.0	20.0	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		–	2.0	20.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		–	2.0	31.0	ns
t_{PHL}	Propagation Delay MR to Q_n		–	3.0	31.0	ns
t_{PLH}	Propagation Delay MR to $\overline{TC}_U$		–	3.0	31.0	ns
t_{PHL}	Propagation Delay MR to $\overline{TC}_D$		–	3.0	31.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$		–	3.0	31.0	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$		–	3.0	20.0	ns
$t_S(H)$ $t_S(L)$	Set-up Time, HIGH or LOW P_n to $\overline{PL}$		–	25.0	–	ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW P_n to $\overline{PL}$		–	1.5	–	ns
$t_W(L)$	$\overline{PL}$ Pulse Width, LOW		–	25.0	–	ns
$t_W(L)$	CP_U or CP_D Pulse Width, LOW		–	20.0	–	ns
$t_W(L)$	CP_U or CP_D Pulse Width, LOW (Change of Direction)		–	20.0	–	ns
$t_W(H)$	MR Pulse Width, HIGH		–	10.0	–	ns
t_{REC}	Recovery Time $\overline{PL}$ to CP_U or CP_D		–	20.0	–	ns
t_{REC}	Recovery Time MR to CP_U or CP_D		–	20.0	–	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT	XXXX	X	X
Temp. Range	Device Type	Package	Process

Code	Description
B	MIL-STD-883, Class B
D	CERDIP
L	Leadless Chip Carrier
E	CERPACK
193	Up/Down Binary Counter
54	-55°C to +125°C

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL BUFFER/LINE DRIVER

IDT54AHCT240

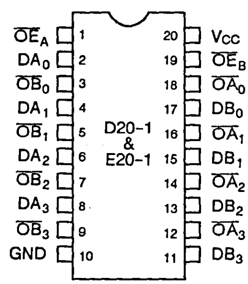
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 7ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal buffer/line driver with 3-state output
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

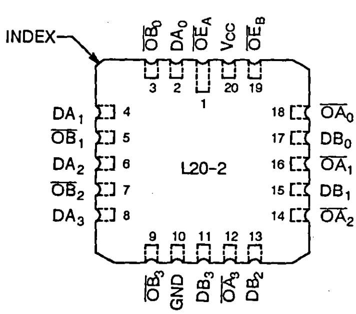
DESCRIPTION:

The IDT54AHCT240 is an octal buffer/line driver built using advanced CEMOS ™, a dual metal CMOS technology. The device is designed to be employed as a memory and address driver, clock driver and bus-oriented transmitter/receiver which provides improved board density.

PIN CONFIGURATIONS

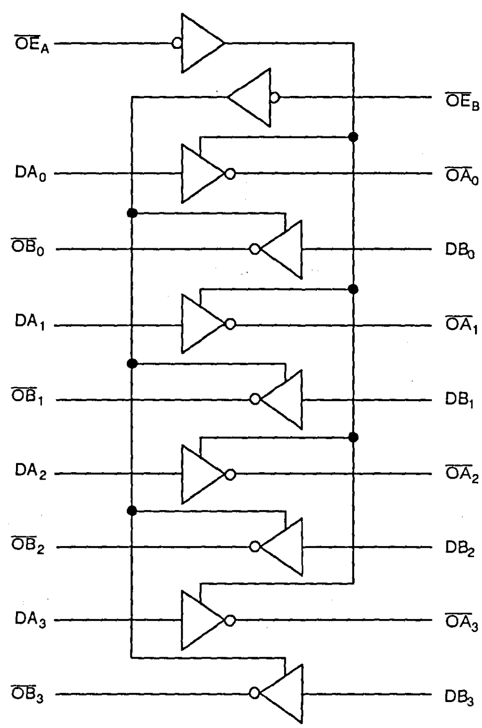


DIP/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



10

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	µA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = GND	–	–	-10	
I_{SC}	Short Circuit Current	V_{CC} = Max.[3]		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:
1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(5)	V_{CC} = Max. Outputs Open $\overline{OE}_A = \overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current (4)	V_{CC} = Max. Outputs Open f_I = 1.0MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V V_{IN} = GND	–	0.4	2.8	
		V_{CC} = Max. Outputs Open f_I = 250kHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ (6) $V_{IN} \leq V_{LC}$ (AHCT)	–	0.3	2.0	
			V_{IN} = 3.4V (6) V_{IN} = GND	–	2.3	10.0	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}\,D_H\,N_T + I_{CCD}\,(f_{CP}/2 + f_I\,N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
Dxx	Inputs
$\bar{O}$xx	Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	TYP.	MIN.[2]	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	7.0	1.5	12.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	1.5	20.0	ns
t_{HZ} t_{LZ}	Output Disable Time		10.0	1.5	18.0	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT	XXXX	X	X
Temp. Range	Device Type	Package	Process

Field	Code	Description
Process	B	MIL-STD-883, Class B
Package	D	CERDIP
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	240	Octal Buffer/Line Driver
Temp. Range	54	-55°C to +125°C

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL BUFFER/LINE DRIVER

IDT54AHCT244

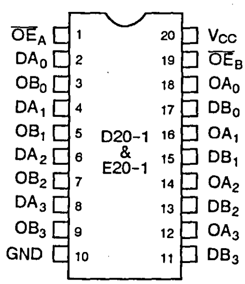
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 7ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal buffer/line driver with 3-state output
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

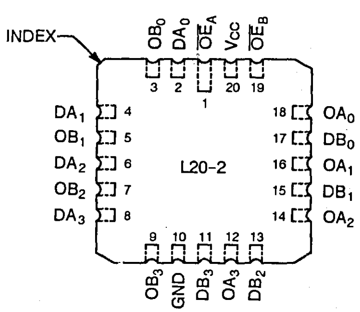
DESCRIPTION:

The IDT54AHCT244 are octal buffer/line drivers built using advanced CEMOS™, a dual metal CMOS technology. The devices are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved board density.

PIN CONFIGURATIONS

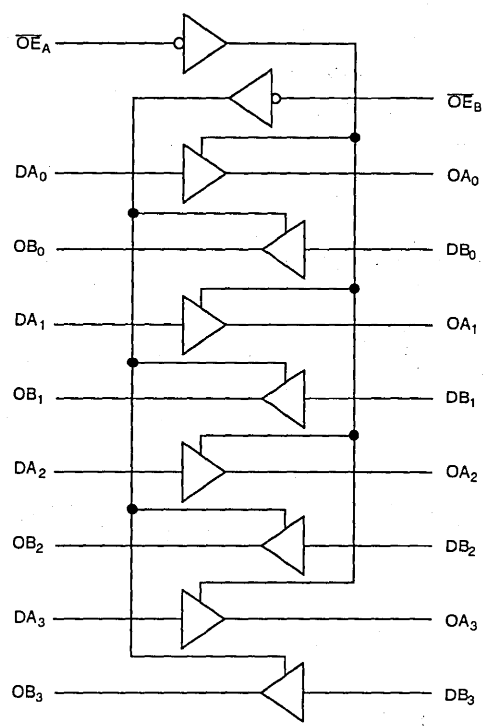


DIP/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



10

CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY TEMPERATURE RANGE **DECEMBER 1987**

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V + 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	µA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = GND	–	–	-10	
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}		
			I_{OH} = -12mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[5]	V_{CC} = Max. Outputs Open $\overline{OE}_A = \overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_I = 1.0MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V V_{IN} = GND	–	0.4	2.8	
		V_{CC} = Max. Outputs Open f_I = 250KHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$[6] $V_{IN} \leq V_{LC}$ (AHCT)	–	0.3	2.0	
			V_{IN} = 3.4V[6] V_{IN} = GND	–	2.3	10.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}\, D_H\, N_T + I_{CCD}\, (f_{CP}/2 + f_I\, N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
Dxx	Inputs
Oxx	Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	TYP.	MIN.(2)	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay D to O	C_L = 50pF R_L = 500Ω	7.0	1.5	13.0	ns
t_{ZH} t_{ZL}	Output Enable Time		16.0	1.5	25.0	ns
t_{HZ} t_{LZ}	Output Disable Time		10.0	1.5	18.0	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT — Temp. Range; XXXX — Device Type; X — Package; X — Process

Process	B	MIL-STD-883, Class B
Package	D	CERDIP
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	244	Octal Buffer/Line Driver
Temp. Range	54	-55°C to +125°C

Integrated Device Technology, Inc.

HIGH-SPEED CMOS NON-INVERTING BUFFER TRANSCEIVER

IDT54AHCT245

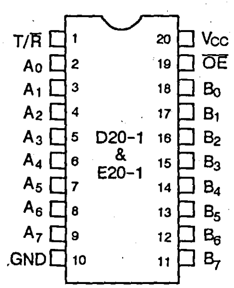
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 8ns typical data to output
  I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Non-inverting buffer transceiver
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

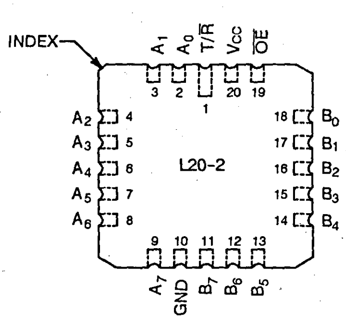
DESCRIPTION:

The IDT54AHCT245 are 8-bit non-inverting, bidirectional buffers built using advanced CEMOS™, a dual metal CMOS technology. This bidirectional buffer has 3-state outputs and is intended for bus-oriented applications. The Transmit/Receive (T/$\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports. Receive (active LOW) enables data from B ports to A ports. The Output Enable Input, when HIGH, disables both A and B ports by placing them in High Z condition.

PIN CONFIGURATIONS

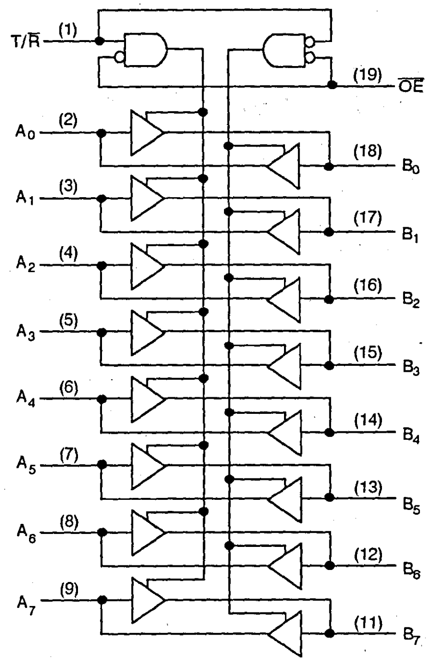


DIP/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



10

CEMOS is a registered trademark of Integrated Device Technology, Inc.

MILITARY TEMPERATURE RANGE **DECEMBER 1987**

DSC-4046/-

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V + 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = GND		–	–	-5	µA
I_{IH}	Input HIGH Current (I/O Pins)	V_{CC} = Max., V_O = V_{CC}		–	–	15	µA
I_{IL}	Input LOW Current (I/O Pins)	V_{CC} = Max., V_O = GND		–	–	-15	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	–	mA
V_{OH}	Output HIGH Voltage Port A and B	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage Port A and B	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP. [2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V [3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current [5]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND $T/\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current [4]	V_{CC} = Max. Outputs Open f_I = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V V_{IN} = GND	–	0.4	2.8	
		V_{CC} = Max. Outputs Open f_I = 250kHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ [6] $V_{IN} \leq V_{LC}$ (AHCT)	–	0.3	2.0	
			V_{IN} = 3.4V [6] V_{IN} = GND	–	2.3	10.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}\, D_H\, N_T + I_{CCD}\, (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

TRUTH TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	TYP.	MIN.(2)	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay A to B B to B	C_L = 50pF R_L = 500Ω	8.0	1.5	15.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	1.5	25.0	ns
t_{HZ} t_{LZ}	Output Disable Time		11.0	1.5	18.0	ns
t_{DLH} t_{DHL}	Propagation Delay T/$\overline{R}$ to A or B(3)		14.0	–	–	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed by design.

ORDERING INFORMATION

IDTXXAHCT XXXX X X
Temp. Range Device Type Package Process

Code	Description
B	MIL-STD-883, Class B
D	CERDIP
L	Leadless Chip Carrier
E	CERPACK
245	Non-Inverting Buffer Transceiver
54	-55°C to +125°C

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL D FLIP-FLOP WITH CLEAR

IDT54AHCT273

FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal D flip-flop with clear
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

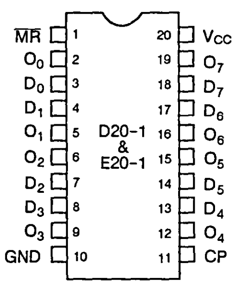
DESCRIPTION:

The IDT54AHCT273 are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54AHCT273 has eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

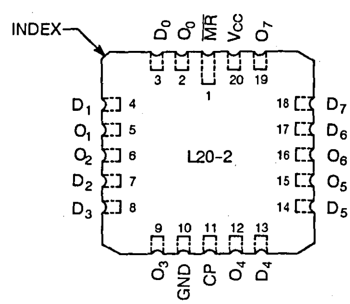
The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

PIN CONFIGURATIONS

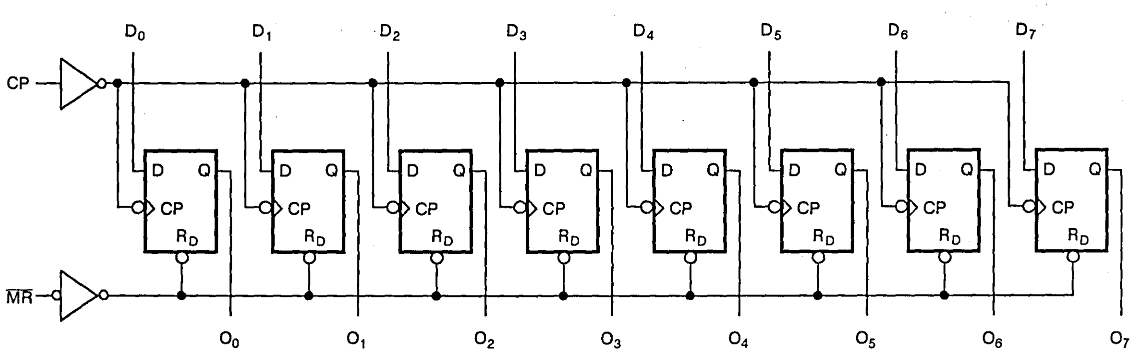


DIP/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5.0	µA
I_{SC}	Short Circuit Current	V_{CC} = Max. [3]		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	mA
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current (5)	V_{CC} = Max. Outputs Open $\overline{MR} = V_{CC}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current (4)	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz, 50% Duty Cycle $\overline{MR} = V_{CC}$ One Bit Toggling at f_I = 500kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.65	3.8	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz, 50% Duty Cycle $\overline{MR} = V_{CC}$ Eight Bits Toggling f_I = 250kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ (6) $V_{IN} \leq V_{LC}$ (AHCT)	–	0.63	2.2	
			V_{IN} = 3.4V(6) or V_{IN} = GND	–	2.88	11.2	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}\, D_H\, N_T + I_{CCD}\, (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = ClockFrequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$D_0 - D_7$	Data Inputs
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
$O_0 - O_7$	Data Outputs

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUT
	$\overline{MR}$	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

H = HIGH Voltage steady state
h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level steady state
l = LOW voltage Level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't Care
↑ = LOW-to-HIGH clock transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	TYP.	MIN.[2]	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	$C_L = 50pF$ $R_L = 500\Omega$	10.0	2.0	17.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output		12.0	2.0	21.0	ns
t_S	Set-up Time High or Low Data to CP		3.0	10.0	–	ns
t_H	Hold Time High or Low Data to CP		0.6	1.0	–	ns
t_W	Clock Pulse Width High or Low		10.0	16.0	–	ns
t_{REC}	Recovery Time $\overline{MR}$ to CP		5.0	15.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT XXXX X X
Temp. Range / Device Type / Package / Process

Process	B	MIL-STD-883, Class B
Package	D	CERDIP
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	273	Octal D Flip-Flop with Clear
Temp. Range	54	-55°C to +125°C

Integrated Device Technology, Inc.

HIGH-SPEED CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54AHCT299

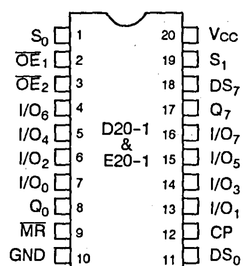
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 9ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- 8-input universal shift register
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

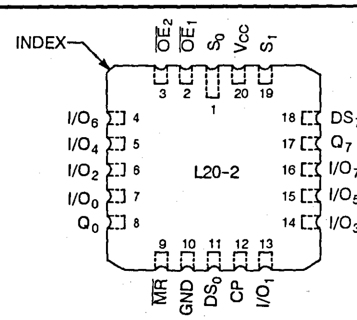
DESCRIPTION:

The IDT54AHCT299 is an 8-input universal shift register built using advanced CEMOS™, a dual metal CMOS technology. The IDT54AHCT299 is an 8-input universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0–Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

PIN CONFIGURATIONS

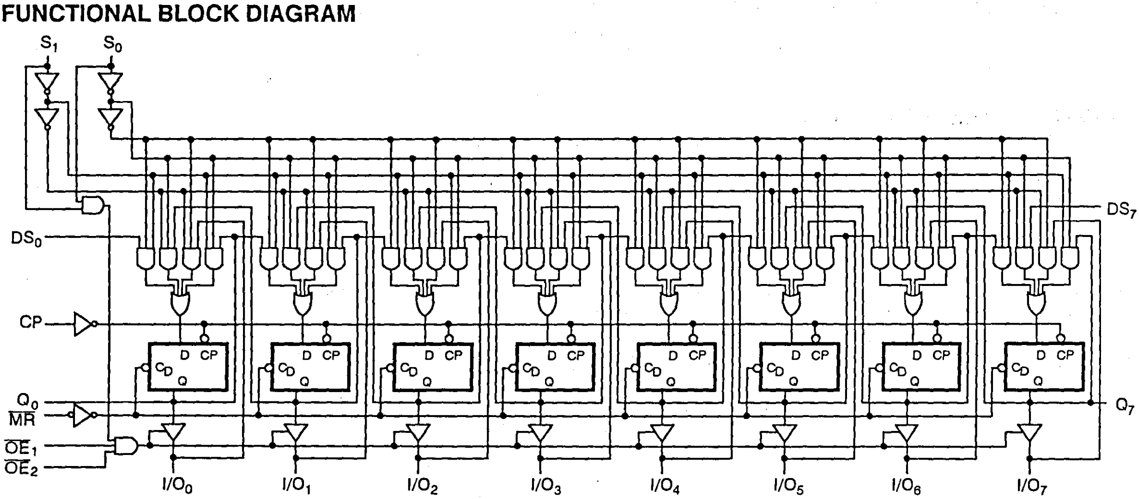


DIP/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a registered trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V + 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	μA
I_{IL}	Input LOW Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = GND		–	–	-5	μA
I_{IH}	Input HIGH Current (I/O Pins)	V_{CC} = Max., V_I = V_{CC}		–	–	15	μA
I_{IL}	Input LOW Current (I/O Pins)	V_{CC} = Max., V_I = GND		–	–	-15	μA
I_{SC}	Short Circuit Current	V_{CC} = Max.[3]		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -200μA	V_{HC}	V_{CC}	–	
			I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(5)	V_{CC} = Max. Outputs Open $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR} = V_{CC}$ $S_0 = S_1 = V_{CC}$ $DS_0 = DS_1$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current(4)	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR} = V_{CC}$ $S_0 = S_1 = V_{CC}$ $DS_0 = DS_1$ = GND One Bit Toggling at f_I = 500kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.65	3.8	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR} = V_{CC}$ $S_0 = S_1 = V_{CC}$ $DS_0 = DS_1$ = GND Eight Bits Toggling at f_I = 250kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$(6) $V_{IN} \leq V_{LC}$ (AHCT)	–	0.63	2.2	
			V_{IN} = 3.4V(6) V_{IN} = GND	–	2.88	11.2	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CP	Clock Pulse Input (Active Edge Rising)
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_7	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)
I/O_0 - I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
Q_0, Q_7	Serial Outputs

TRUTH TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset Q_0, Q_7 = LOW
H	H	H	↑	Parallel Load; $I/O_N \rightarrow Q_N$
H	L	H	↑	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↑	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	TYP.	MIN.[2]	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7		9.0	–	17.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_N		8.0	–	15.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		9.0	–	15.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_N		9.0	–	15.0	ns
t_{ZH} t_{ZL}	Output Enable Time $\overline{OE}$ to I/O_N		10.0	–	18.0	ns
t_{HZ} t_{LZ}	Output Disable Time $\overline{OE}$ to I/O_N	C_L = 50pF R_L = 500Ω	7.5	–	12.0	ns
t_S	Setup Time HIGH or LOW S_0 or S_1 to CP		4.0	8.5	–	ns
t_H	Hold Time HIGH or LOW S_0 or S_1 to CP		1.0	0.0	–	ns
t_S	Setup Time HIGH or LOW I/O_N, DS_0 or DS_7 to CP		1.5	5.5	–	ns
t_H	Hold Time HIGH or LOW I/O_N, DS_0 or DS_7 to CP		0	2.0	–	ns
t_W	CP Pulse Width HIGH or LOW		8.0	8.0	–	ns
t_W	$\overline{MR}$ Pulse Width Low		8.0	8.0	–	ns
t_{REC}	Recovery Time $\overline{MR}$ to CP		8.0	8.0	–	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT (Temp. Range) XXXX (Device Type) X (Package) X (Process)

Field	Code	Description
Process	B	MIL-STD-883, Class B
Package	D	CERDIP
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	299	8-Input Universal Shift Register
Temp. Range	54	-55°C to +125°C

HIGH-SPEED CMOS OCTAL TRANSPARENT LATCH

IDT54AHCT373

Integrated Device Technology, Inc.

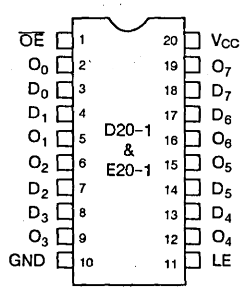
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal transparent latch with enable
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

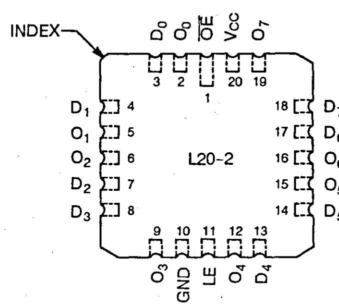
DESCRIPTION:

The IDT54AHCT373 are 8-bit latches built using advanced CEMOS™, a dual metal CMOS technology. This octal latch has 3-state output and is intended for bus-oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS

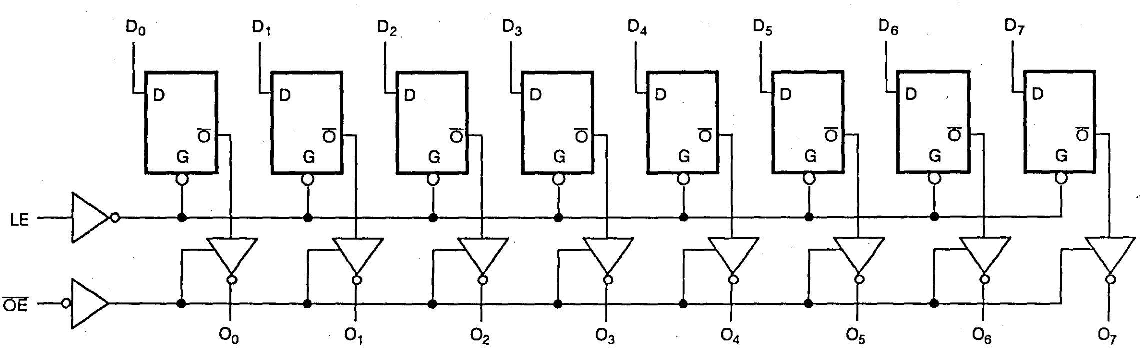


DIP/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5.0	µA
I_{SC}	Short Circuit Current	V_{CC} = Max. (3)		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	mA
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current (5)	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current (4)	V_{CC} = Max. Outputs Open f_I = 1.0MHz, 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.4	2.8	
		V_{CC} = Max. Outputs Open f_I = 250kHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT) (6)	–	0.3	2.0	
			V_{IN} = 3.4V (6) or V_{IN} = GND	–	2.3	10.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = ClockFrequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

10

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$D_0 - D_7$	Data Inputs
LE	Latch Enables Input (Active HIGH)
$\overline{OE}$	Output Enables Input (Active LOW)
$O_0 - O_7$	3-State Latch Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	TYP.	MIN.(2)	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	$C_L = 50pF$ $R_L = 500\Omega$	10.0	1.5	19.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	1.5	24.0	ns
t_{HZ} t_{LZ}	Output Disable Time		9.0	1.5	16.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n		20.0	2.0	27.0	ns
t_S	Set-up Time HIGH or LOW D_n to LE		4.0	10.0	–	ns
t_H	Hold Time HIGH or LOW D_n to LE		3.0	1.5	–	ns
t_W	LE Pulse Width HIGH or LOW		7.0	10.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT — Temp. Range
XXXX — Device Type
X — Package
X — Process

Process	B	MIL-STD-883, Class B
Package	D	CERDIP
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	373	Octal Transparent Latch
Temp. Range	54	-55°C to +125°C

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL D REGISTER (3-STATE)

IDT54AHCT374

FEATURES:

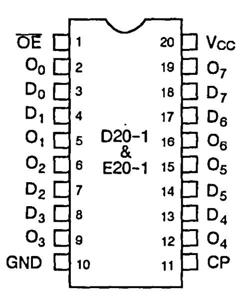
- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical address to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal D register (3-state)
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

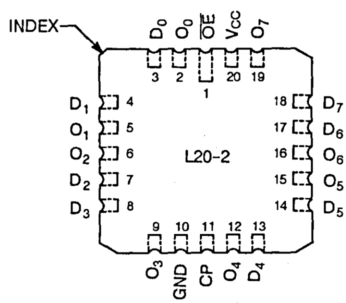
The IDT54AHCT374 are 8-bit registers built using advanced CEMOS™, a dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state conditions.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

PIN CONFIGURATIONS

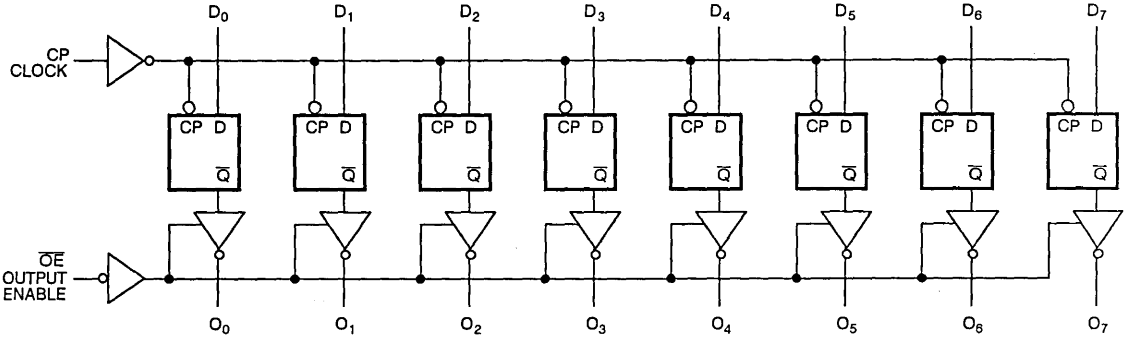


DIP/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.[3]		-60	120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	–	
			I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:
1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[5]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current [4]	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_I = 500kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.65	3.8	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_I = 250kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ [6] $V_{IN} \leq V_{LC}$ (AHCT)	–	0.63	2.2	
			V_{IN} = 3.4V or [6] V_{IN} = GND	–	2.88	11.2	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

10

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_I	The D flip-flop data inputs.
CP	Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
O_I	The register three-state outputs.
$\overline{OE}$	Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CLOCK	D_I	O_I	Q_I
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↑	L	L	L
	L	↑	H	H	H
	H	↑	L	Z	L
	H	↑	H	Z	H

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
NO = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	TYP.	MIN.(2)	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	C_L = 50pF R_L = 500Ω	10.0	2.0	18.0	ns
t_{ZH} t_{ZL}	Output Enable Time		11.0	1.5	20.0	ns
t_{HZ} t_{LZ}	Output Disable Time		9.0	1.5	24.0	ns
t_S	Set-up Time HIGH or LOW D_N to CP		2.0	10.0	–	ns
t_H	Hold Time HIGH or LOW D_N to CP		0.5	1.5	–	ns
t_W	CP Pulse Width HIGH or LOW		10.0	16.5	–	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT (Temp. Range) XXXX (Device Type) X (Package) X (Process)

Process	B	MIL-STD-883, Class B
Package	D	CERDIP
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	374	Octal D Register (3-State)
Temp. Range	54	–55°C to +125°C

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT54AHCT377

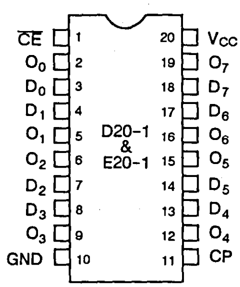
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical propagation delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5µW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5µA max.)
- Octal D flip-flop with clock enable
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

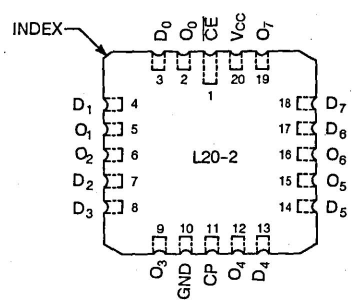
DESCRIPTION:

The IDT54AHCT377 is an octal D flip-flop built using advanced CEMOS™, a dual metal CMOS technology. The IDT54AHCT377 has eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

PIN CONFIGURATIONS

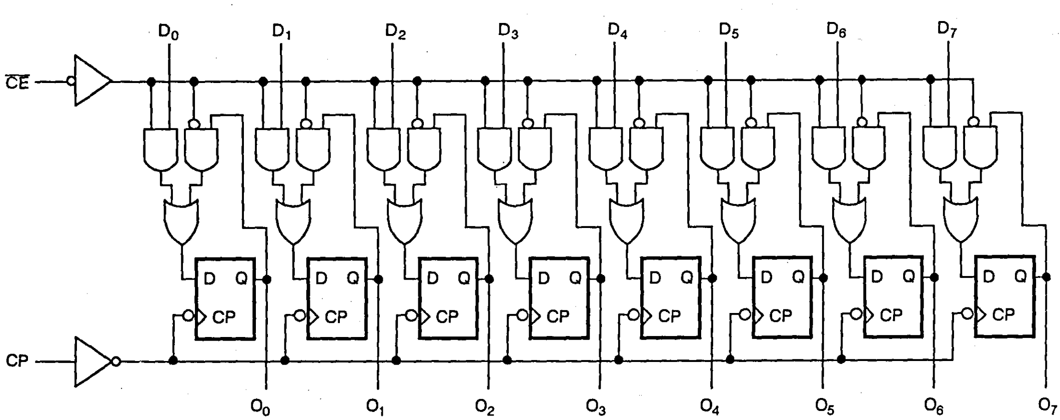


DIP/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5.0	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5.0	μA
I_{SC}	Short Circuit Current	V_{CC} = Max.[3]		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	–	mA
		V_{CC} = Min.	I_{OH} = -150μA	V_{HC}	V_{CC}	–	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300μA	–	GND	V_{LC}	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 14mA	–	–	0.4	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[5]	V_{CC} = Max. Outputs Open $\overline{CE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current [4]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CE}$ = GND One Bit Toggling at f_I = 500kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.65	3.8	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{CE}$ = GND Eight Bits Toggling at f_I = 250kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ [6] $V_{IN} \leq V_{LC}$ (AHCT)	–	0.63	2.2	
			V_{IN} = 3.4V or [6] V_{IN} = GND	–	2.88	11.2	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
O_0-O_7	Data Outputs
CP	Clock Pulse Input

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D	O
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑ X	h H	X X	No Change No Change

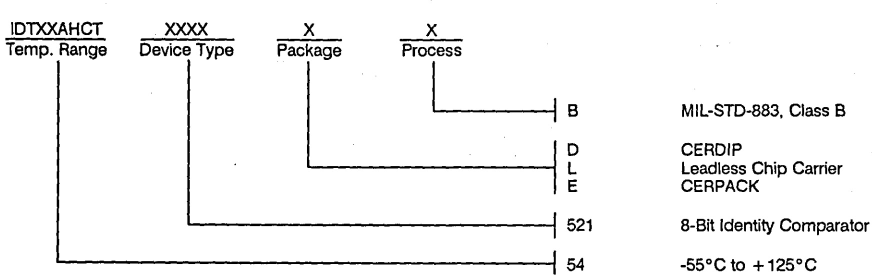
H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
↑ = LOW-to-HIGH Clock Transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	TYP.	MIN.[2]	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	$C_L = 50pF$ $R_L = 500\Omega$	10.0	2.0	20.0	ns
t_S	Set-up Time HIGH or LOW D_N to CP		5.0	2.0	–	ns
t_H	Hold Time HIGH or LOW D_N to CP		2.0	1.5	–	ns
t_S	Set-up Time HIGH or LOW $\overline{CE}$ to CP		3.0	2.0	–	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$ to CP		2.0	2.0	–	ns
t_W	Clock Pulse Width, LOW		7.0	7.0	–	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED CMOS 8-BIT IDENTITY COMPARATOR

IDT54AHCT521

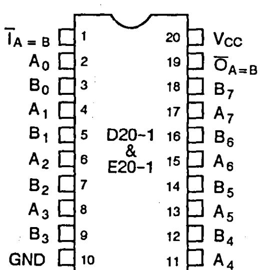
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 9ns typical propagation delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5µW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5µA max.)
- 8-bit identity comparator
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

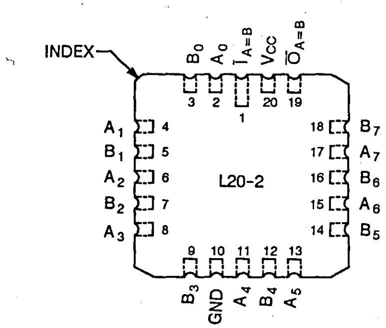
DESCRIPTION:

The IDT54AHCT521 is an 8-bit identity comparator built using advanced CEMOS™, a dual metal CMOS technology. The device compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

PIN CONFIGURATIONS

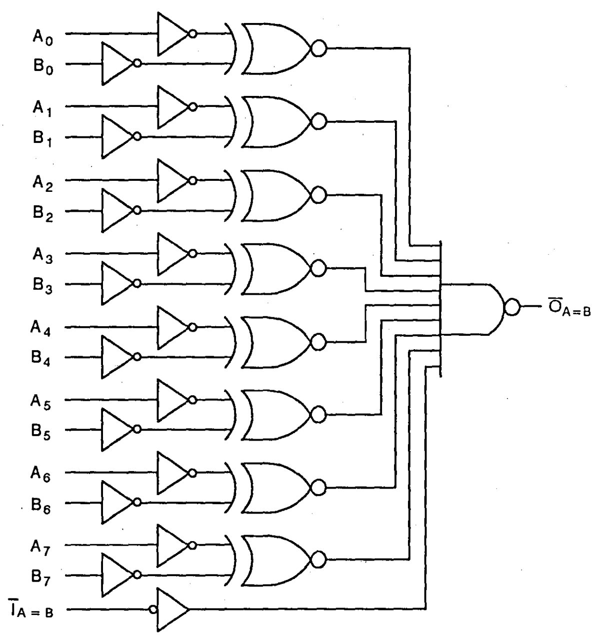


DIP/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	μA
I_{SC}	Short Circuit Current	V_{CC} = Max.[3]		-60	120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300μA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current (5)	V_{CC} = Max. Output Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current (4)	V_{CC} = Max. Output Open f_I = 1.0MHz, 50% Duty Cycle On Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.4	2.8	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = ClockFrequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$A_0 - A_7$	Word A Inputs
$B_0 - B_7$	Word B Inputs
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\overline{O}_{A=B}$	Identity Output (Active LOW)

TRUTH TABLE

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	TYP.	MIN.(2)	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay A_N or B_N to $\overline{O}_{A=B}$	C_L = 50pF R_L = 500Ω	9.0	–	17.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$		5.0	–	11.0	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT	XXXX	X	X
Temp. Range	Device Type	Package	Process

Code	Description
B	MIL-STD-883, Class B
D	CERDIP
L	Leadless Chip Carrier
E	CERPACK
521	8-Bit Identity Comparator
54	$-55°C$ to $+125°C$

IDT logo: Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL TRANSPARENT LATCH (3-STATE)

IDT54AHCT533

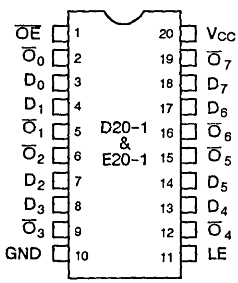
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 11ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal transparent latch with 3-state output
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

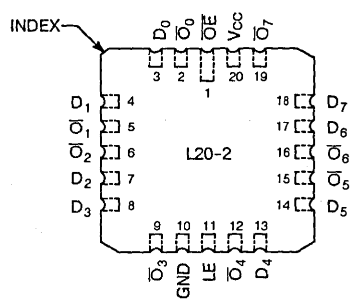
DESCRIPTION:

The IDT54AHCT533 are octal transparent latches built using advanced CEMOS™, a dual metal CMOS technology. The IDT54AHCT533 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS

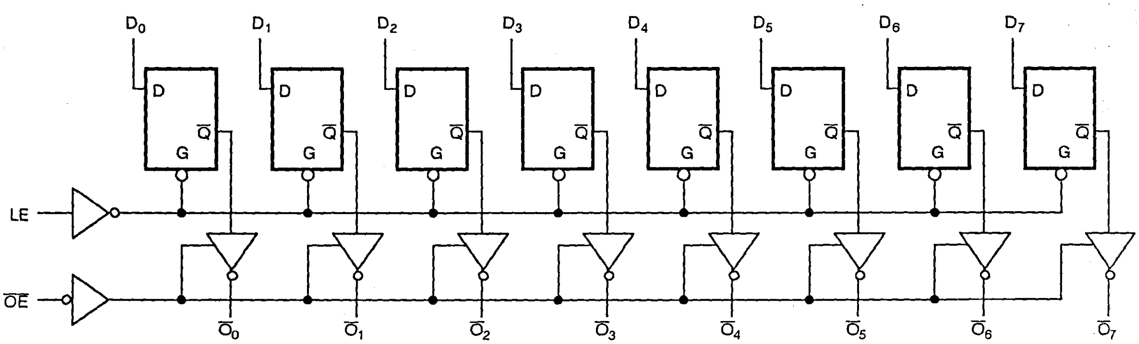


DIP/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	μA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	μA
			V_O = GND	–	–	-10	
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150μA	V_{HC}	V_{CC}	–	
			I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:
1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP. (2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = 3.4V$ (3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current (5)	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current (4)	V_{CC} = Max. Outputs Open f_I = 1.0MHz, 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.4	2.8	
		V_{CC} = Max. Outputs Open f_I = 250kHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT) (6)	–	0.3	2.0	
			V_{IN} = 3.4V (6) or V_{IN} = GND	–	2.3	10.0	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = ClockFrequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$D_0 - D_7$	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{O}_0 - \overline{O}_7$	Complementary 3-State Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_N	LE	$\overline{OE}$	$\overline{O}_N$
H	H	L	L
L	H	L	H
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	TYP.	MIN.(2)	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	$C_L = 50pF$ $R_L = 500\Omega$	11.0	1.5	24.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	1.5	20.0	ns
t_{HZ} t_{LZ}	Output Disable Time		11.0	1.5	22.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_N$		15.0	2.0	28.0	ns
t_S	Set-up Time HIGH or LOW D_n to LE		7.0	15.0	–	ns
t_H	Hold Time HIGH or LOW D_n to LE		5.0	1.5	–	ns
t_W	LE Pulse Width HIGH or LOW		7.0	15.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT (Temp. Range) XXXX (Device Type) X (Package) X (Process)

Field	Code	Description
Process	B	MIL-STD-883, Class B
Package	D	CERDIP
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	533	Octal Transparent Latch (3-state)
Temp. Range	54	-55°C to +125°C

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL D FLIP-FLOP (3-STATE)

IDT54AHCT534

FEATURES:

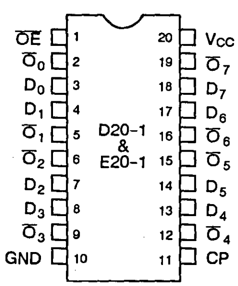
- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal D flip-flop with 3-state output
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

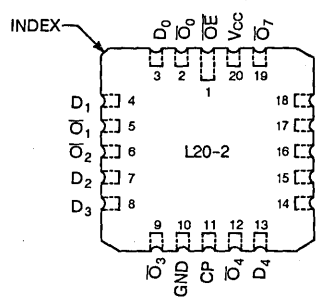
The IDT54AHCT534 are high-speed, low-power octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

They are built using IDT's advanced CEMOS™, a dual metal CMOS technology.

PIN CONFIGURATIONS

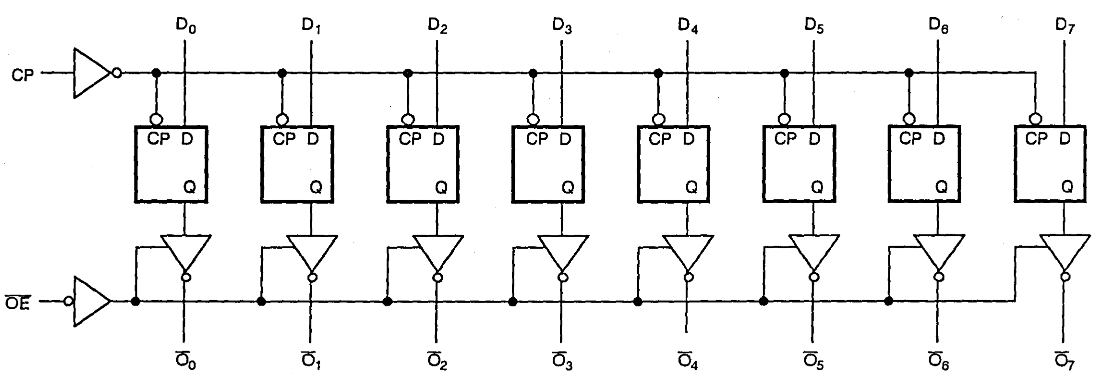


DIP/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY TEMPERATURE RANGE **DECEMBER 1987**

DSC-4054/-

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	µA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = GND	–	–	-10	
I_{SC}	Short Circuit Current	V_{CC} = Max.[3]		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	–	
			I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:
1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(4)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current (5)	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current (4)	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz, 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_I = 500kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.65	3.8	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz, 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_I = 250kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT) (6)	–	0.63	2.2	
			V_{IN} = 3.4V (6) or V_{IN} = GND	–	2.88	11.2	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = ClockFrequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0 - D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	3-State Output Enable Input (Active LOW)
$\overline{O}_0$ - $\overline{O}_7$	Complementary 3-State Outputs

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CP	D_I	$\overline{O}_N$	Q_I
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↑	L	H	L
	L	↑	H	L	H
	H	↑	L	Z	L
	H	↑	H	Z	H

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
NC = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	TYP.	MIN.(2)	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$	$C_L = 50pF$ $R_L = 500\Omega$	10.0	2.0	18.0	ns
t_{ZH} t_{ZL}	Output Enable Time		11.0	1.5	20.0	ns
t_{HZ} t_{LZ}	Output Disable Time		11.0	1.5	16.0	ns
t_S	Set-up Time HIGH or LOW D_n to CP		2.0	10.0	–	ns
t_H	Hold Time HIGH or LOW D_n to CP		0.5	1.5	–	ns
t_W	CP Pulse Width HIGH or LOW		7.0	16.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT XXXX X X
Temp. Range Device Type Package Process

Field	Code	Description
Process	B	MIL-STD-883, Class B
Package	D	CERDIP
	L	Leadless Chip Carrier
	E	CERPACK
Device Type	534	Octal D Flip-Flop (3-state)
Temp. Range	54	-55°C to +125°C

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL TRANSPARENT LATCH

IDT54AHCT573

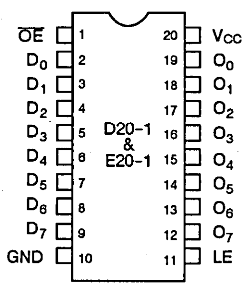
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal transparent latch with enable
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

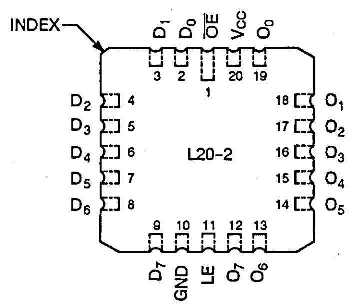
DESCRIPTION:

The IDT54AHCT573 are 8-bit latches built using advanced CEMOS™, a dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus-oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times are latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS

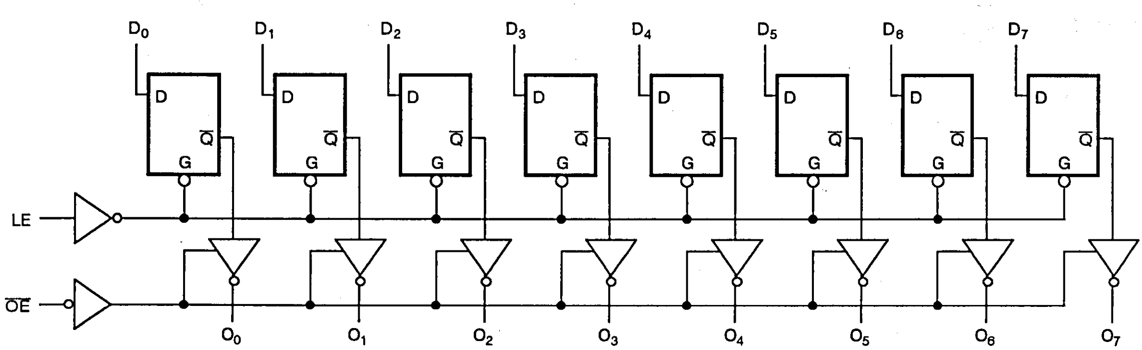


DIP/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V + 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	μA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	μA
			V_O = GND	–	–	-10	
I_{SC}	Short Circuit Current	V_{CC} = Max.[3]		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150μA	V_{HC}	V_{CC}	–	
			I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_I = 0		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[5]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_I = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.4	2.8	
		V_{CC} = Max. Outputs Open f_I = 250kHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ [6] $V_{IN} \leq V_{LC}$ (AHCT)	–	0.3	2.0	
			V_{IN} = 3.4V or [6] V_{IN} = GND	–	2.3	10.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

10

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
LE	Latch Enables Input (Active HIGH)
$\overline{OE}$	Output Enables Input (Active LOW)
O_0-O_7	3-State Latch Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	TYP.	MIN.[2]	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	10.0	1.5	15.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	1.5	21.0	ns
t_{HZ} t_{LZ}	Output Disable Time		9.0	1.5	15.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_N		20.0	2.0	27.0	ns
t_S	Set Up Time HIGH or LOW D_N to LE		4.0	2.0	–	ns
t_H	Hold Time HIGH or LOW D_N to LE		3.0	1.8	–	ns
t_W	LE Pulse Width HIGH or LOW		7.0	5.0	–	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT XXXX X X
Temp. Range / Device Type / Package / Process

Process:
B — MIL-STD-883, Class B

Package:
D — CERDIP
L — Leadless Chip Carrier
E — CERPACK

Device Type:
573 — Octal Transparent Latch

Temp. Range:
54 — -55°C to +125°C

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL D REGISTER (3-STATE)

IDT54AHCT574

FEATURES:

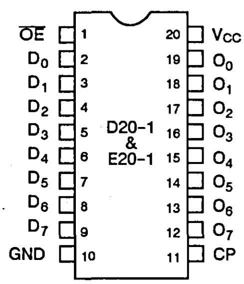
- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical address to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal D register (3-state)
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

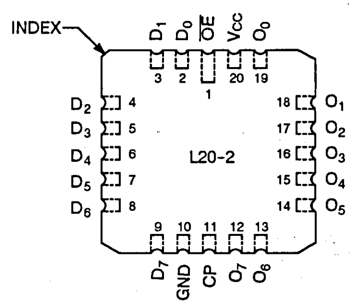
The IDT54AHCT574 are 8-bit registers built using advanced CEMOS™, a dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered three-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state condition.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

PIN CONFIGURATIONS

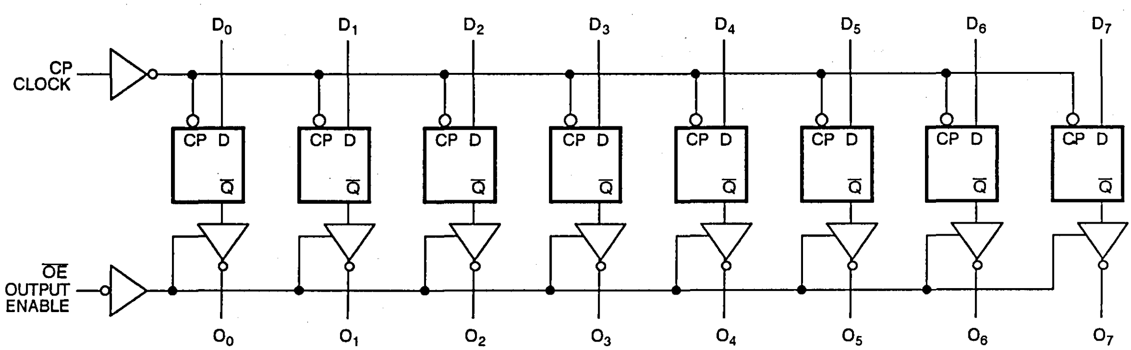


DIP/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	µA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = GND	–	–	-10	
I_{SC}	Short Circuit Current	V_{CC} = Max.[3]		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	–	
			I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[5]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz, 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_I = 500kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.65	3.8	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz, 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_I = 250kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$[6] $V_{IN} \leq V_{LC}$ (AHCT)	–	0.63	2.2	
			V_{IN} = 3.4V[6] or V_{IN} = GND	–	2.88	11.2	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input Transition pair (HLH or LHL)
   f_{CP} = ClockFrequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

10

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_I	The D flip-flop data inputs.
CP	Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
O_I	The register three-state outputs.
$\overline{OE}$	Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CLOCK	D_I	O_I	Q_I
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↑	L	L	L
	L	↑	H	H	H
	H	↑	L	Z	L
	H	↑	H	Z	H

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
NC = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION(1)	TYP.	MIN.(2)	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	C_L = 50pF R_L = 500Ω	10.0	2.0	15.0	ns
t_{ZH} t_{ZL}	Output Enable Time		11.0	1.5	21.0	ns
t_{HZ} t_{LZ}	Output Disable Time		9.0	1.5	15.0	ns
t_S	Set-up Time HIGH or LOW D_N to CP		2.0	2.0	–	ns
t_H	Hold Time HIGH or LOW D_N to CP		0.5	1.5	–	ns
t_W	CP Pulse Width HIGH or LOW		10.0	6.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT	XXXX	X	X
Temp. Range	Device Type	Package	Process

B	MIL-STD-883, Class B
D	CERDIP
L	Leadless Chip Carrier
E	CERPACK
574	Octal D Register (3-state)
54	-55°C to +125°C

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL INVERTING BUFFER TRANSCEIVER

IDT54AHCT640

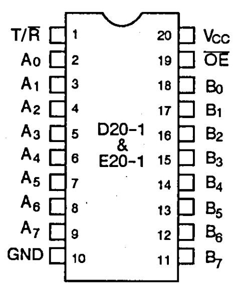
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns data to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5µW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5µA max.)
- Inverting buffer transceiver
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

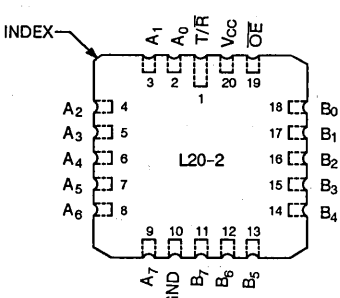
DESCRIPTION:

The IDT54AHCT640 are 8-bit inverting buffer transceivers built using advanced CEMOS ™, a dual metal CMOS technology. These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control ($T/\overline{R}$) input. The enable input ($\overline{OE}$) can be used to disable the device so the buses are effectively isolated.

PIN CONFIGURATIONS

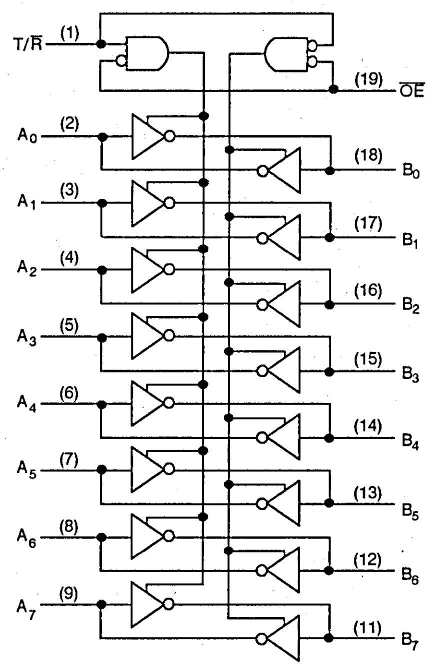


DIP/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



10

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V + 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	μA
I_{IL}	Input LOW Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = GND		–	–	-5	μA
I_{IH}	Input HIGH Current (I/O Pins)	V_{CC} = Max., V_I = V_{CC}		–	–	15	μA
I_{IL}	Input LOW Current (I/O Pins)	V_{CC} = Max., V_I = GND		–	–	-15	μA
I_{SC}	Short Circuit Current	V_{CC} = Max.[3]		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150μA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(5)	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current (4)	V_{CC} = Max. Outputs Open f_I = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.4	2.8	
		V_{CC} = Max. Outputs Open f_I = 250kHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ (6) $V_{IN} \leq V_{LC}$ (AHCT)	–	0.3	2.0	
			V_{IN} = 3.4V or (6) V_{IN} = GND	–	2.3	10.0	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

10

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-State Outputs
B_0–B_7	Side B Inputs or 3-State Outputs

TRUTH TABLE

INPUTS		OPERATION
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	TYP.	MIN.[2]	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay A to B B to A	C_L = 50pF R_L = 500Ω	10.0	1.5	14.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	1.5	27.0	ns
t_{HZ} t_{LZ}	Output Disable Time		12.0	1.5	20.0	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

IDTXXAHCT — Temp. Range
XXXX — Device Type
X — Package
X — Process

B — MIL-STD-883, Class B

D — CERDIP
L — Leadless Chip Carrier
E — CERPACK

640 — Octal Inverting Buffer Transceiver

54 — -55°C to +125°C

HIGH-SPEED CMOS NON-INVERTING BUFFER TRANSCEIVER

IDT54AHCT645

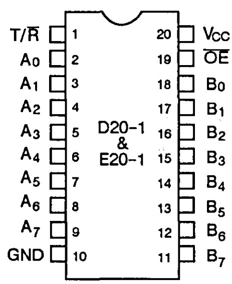
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 8ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Non-inverting buffer transceiver
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

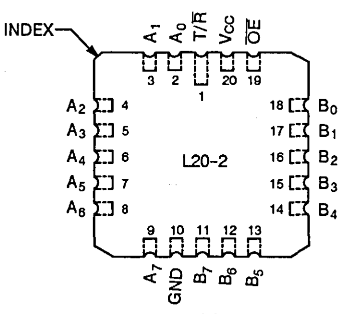
DESCRIPTION:

The IDT54AHCT645 are 8-bit non-inverting buffer transceivers built using advanced CEMOS™, a dual metal CMOS technology. These non-inverting buffer transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the I/74evel at the direction control (T/$\overline{R}$) input. The enable input ($\overline{OE}$) can be used to disable the device so the buses are effectively isolated.

PIN CONFIGURATIONS

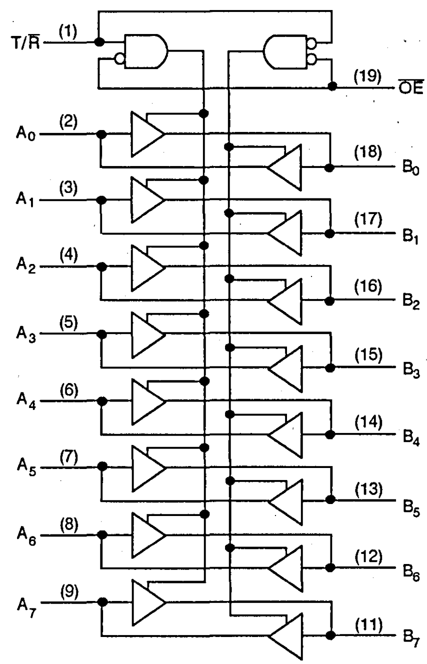


DIP/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



10

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to + 125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	μA
I_{IL}	Input LOW Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = GND		–	–	-5	μA
I_{IH}	Input HIGH Current (I/O Pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	μA
I_{IL}	Input LOW Current (I/O Pins)	V_{CC} = Max.	V_I = GND	–	–	-15	μA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150μA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:
1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current [5]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND $T/\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current [4]	V_{CC} = Max. Outputs Open f_I = 1.0MHz, 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.4	2.8	
		V_{CC} = Max. Outputs Open f_I = 250kHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT) [6]	–	0.3	2.0	
			V_{IN} = 3.4V[6] or V_{IN} = GND	–	2.3	10.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input Transition pair (HLH or LHL)
   f_{CP} = ClockFrequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	TYP.	MIN.[2]	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay A to B B to A	C_L = 50pF R_L = 500Ω	8.0	1.5	15.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	1.5	25.0	ns
t_{HZ} t_{LZ}	Output Disable Time		11.0	1.5	18.0	ns
t_{PLH} t_{PHL}	Propagation Delay T/$\overline{R}$ to A or B[3]		15.0	–	–	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

ORDERING INFORMATION

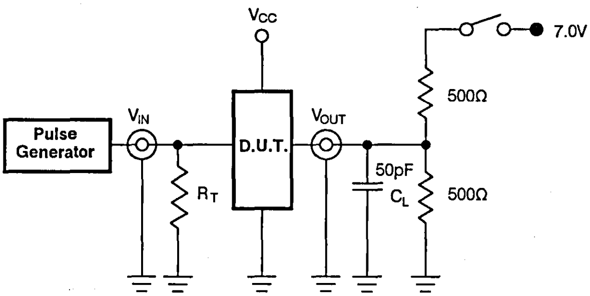
IDTXXAHCT XXXX X X
Temp. Range Device Type Package Process

B	MIL-STD-883, Class B
D	CERDIP
L	Leadless Chip Carrier
E	CERPACK
645	Non-inverting Buffer Transceiver
54	-55°C to +125°C

COMMON WAVEFORM–LOGIC

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR THREE-STATE OUTPUTS



SWITCH POSITION

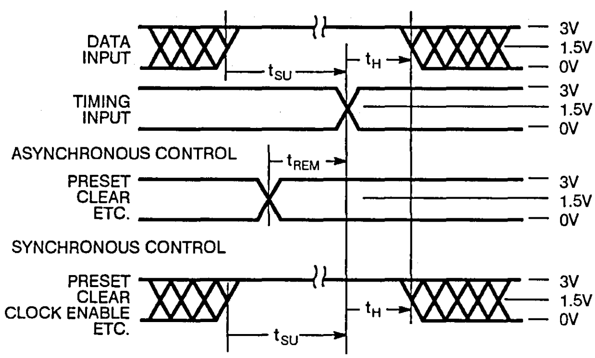
TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS

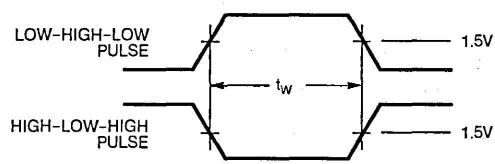
C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

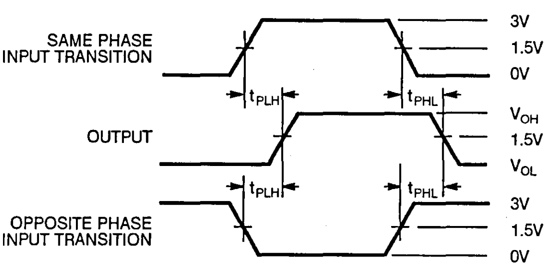
SET–UP, HOLD, AND RELEASE TIMES



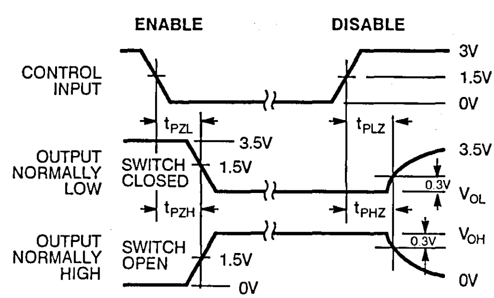
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate $\leq$ 1.0 MHz; $Z_O \leq 50\Omega$; $t_F \leq 2.5$ns; $t_R \leq 2.5$ns

DATA CONVERSION INTRODUCTION

The Data Conversion Group is one of the newest members of IDT's product family. Mixing high-speed digital logic with high-performance analog functions opens a number of product opportunities

Video-Speed Analog products are a primary area of concentration for the Data Conversion Group. Integration advances in digital logic have allowed video/graphic resolutions to reach levels approaching broadcast quality in a personal computer. Until now, however, similar advances on the analog side have not been made.

IDT has targeted this area with a family of DACs featuring clock rates in excess of 100MHz (more than 1,000 by 1,000 CRT pixel resolution) and outputs which directly drive the coaxial cable connections to the display. Merging IDT's SRAM technology with analog, it is now possible to integrate all of the functions needed for a high-resolution, RGB graphic output without power-hungry ECL logic.

Many of today's video systems must do extensive computations on the analog signal to enhance, convert and recognize patterns. These computations are done most easily in the digital domain, requiring a high-performance Analog-to-Digital Converter at the front end. IDT's first product offering in this area allows the conversion of video speed analog signals at clock rates exceeding four times the color subcarrier (~ 14MHz NTSC, ~ 17MHz PAL). Along with the low power consumption, these parts include, a first for the industry, on-chip error detection and correction making it more immune to digital noise and much easier to use.

IDT is dedicated to providing complete CMOS solutions for high-performance system designs. High speed SRAMs, FIFOs, MICROSLICE™ components, Arithmetic Processors, DSP units and FCT fast logic elements form the basis for leading-edge designs. The Data Conversion Group completes this picture with mixed analog and digital chips for front – and back – end interface. Look to IDT for innovative Data Conversion solutions.

TABLE OF CONTENTS

CONTENTS **PAGE**

Data Conversion

Integrated Device Technology, Inc.

8-BIT CMOS VIDEO DAC

IDT75C18

FEATURES:

- Graphics-ready
- Pin- and function-compatible with TRW TDC1018
- 8 bits, 1/2 LSB linearity
- 70, 100, 125MHz models available
- ECL-compatible inputs
- Low power dissipation < 400mW
- Power supply noise rejection > 50dB
- Registered data and video controls
- Differential current outputs
- Flexible video controls
- Inherently low glitch energy
- Multiplying mode capability
- Single 5V power supply
- Available in 24-pin hermetic DIP, 24-pin plastic DIP and 28-pin LCC
- Military product is compliant to MIL-STD-883, Class B

DESCRIPTION:

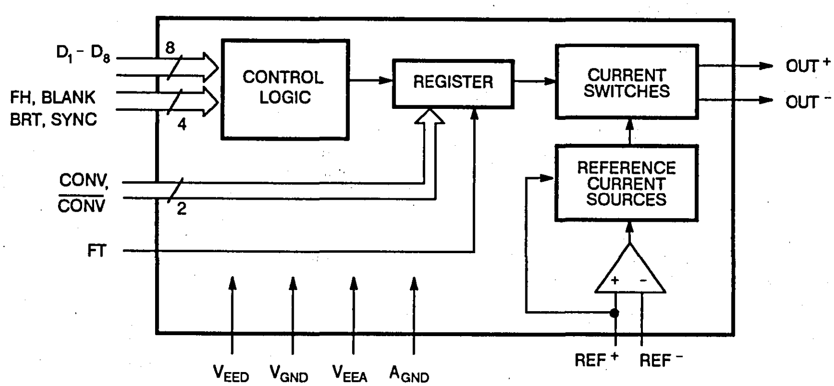
The IDT75C18 is a 70/100/125 MegaSample per Second (MSPS), 8-bit Digital to Analog Converter. It can directly drive a doubly terminated 75Ω load to levels compatible with RS-343A. Four special controls for blanking, synchronization and highlighting allow the device to be used in typical video applications with no extra components

The IDT75C18 is built using IDT's high-performance CEMOS™ process. Innovative design methods, which include on-chip data registers and precise matching of propagation delays, as well as an improved segmenting/decoding architecture, significantly reduce glitch energy. The IDT75C18 offers high-performance and low power in a 24-pin hermetic DIP, 24-pin plastic DIP or 28-pin LCC.

The IDT75C18 is pin- and function-compatible with the TRW TDC1018, with the advantage of low power due to CMOS processing. Besides providing higher reliability by running cooler, power supply requirements are reduced. Another advantage of the lower power dissipation is that this part may be packaged in a space-saving, cost-effective, 0.3-inch plastic package.

The IDT75C18 military DAC is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

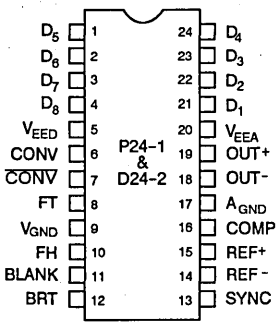


11

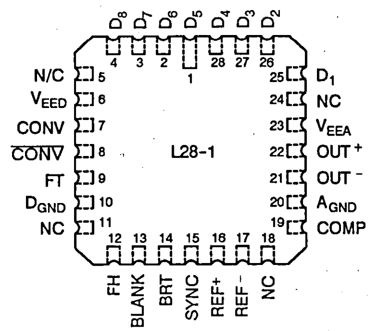
CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES — DECEMBER 1987

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL DESCRIPTION
GENERAL INFORMATION

The IDT75C18 output current is proportional to the product of the digital input data and the analog reference current. All the digital inputs, data and control are compatible with standard ECL logic levels. The IDT75C18 is normally operated synchronously with data being latched by the rising edge of the convert clock, CONV. FT, the feedthrough control input, determines the operating mode. When FT is LOW, the part operates in the synchronous mode and the low-to-high transition of the convert clock, CONV, latches data and control values into internal D-type registers. The registered values are then decoded and presented to switched current sinks which produce the appropriate analog output values. When FT is HIGH, the part operates asynchronously and the digital inputs are not latched. The analog output, then, changes in response to the digital inputs without regard to clock. FT is the only asynchronous input and is typically tied to the appropriate DC level.

The IDT75C18 uses a 6x2 segmented DAC approach where the six MSBs of the input data are decoded into a parallel "Thermometer" code which produces sixty-four "coarse" output levels. The remaining two LSBs of the input data drive three binary weighted current switches with a total contribution of one-sixty-fourth of full scale. The MSB and LSB currents are summed at the output to produce 256 analog levels.

SYNC, BLANK, FH (Force High) and BRT (BRighT) are special control inputs which drive appropriately weighted current switches. These currents are summed at the output with the level produced by the data inputs to allow for specific levels required by video applications such as the sync pulses and the blanking levels.

POWER CONSIDERATIONS

The IDT75C18 operates from separate analog and digital supplies to provide the highest noise immunity on the analog output to digital switching spikes. All power and ground pins must be connected.

REFERENCE CONSIDERATIONS

The IDT75C18 has two reference inputs, REF+ and REF−, which are simply the non-inverting and inverting inputs to an internal buffer amplifier. The output of this amplifier serves as the reference for the transistors in the DAC. The feedback loop internally includes current sources which are identical to the current sink transistors, guaranteeing that the reference current will be precisely mirrored in the DAC.

Since the output currents are proportional to the digital data and the reference current, the full-scale output current may be adjusted over a limited range by varying the reference current. In the same vein, the stability of the output depends strongly on the stability of the reference. The reference current is normally applied to REF+, while REF− is usually connected to a negative reference through a resistor equal to the effective impedance seen on REF+.

Through careful design of the reference amplifier, no external compensation capacitor is required and the COMP pin should be left unconnected.

CONTROLS

The IDT75C18 has four special control inputs: SYNC, BLANK, FH (Force High) and BRT (BRighT), as well as FT (Feed Through control). Typically, the IDT75C18 is operated in the synchronous mode which ensures the lowest output noise. When FT is forced HIGH, the input registers pass the data and control information through without latching, allowing the analog output to change asynchronously.

In the synchronous mode, the control inputs are registered by the rising edge of CONV in the same manner as the data inputs. The controls, like the data, must be stable for a set-up time (t_S) before, and a hold time (t_H) after, the rising edge of CONV. In the asynchronous mode, only the minimum pulse widths are relevant.

The video controls produce specific output levels which are used for frame synchronization, horizontal blanking, etc. as described in various standards such as RS-343A. The effect of these controls on the analog output is shown below. The internal logic simplifies the use of the controls in video applications. BLANK, SYNC and FH override the data inputs. SYNC overrides all other inputs and produces a full negative level. FH drives the analog output to full-scale producing a reference white level. The BRT control creates a "whiter than white" level by adding 10% of full-scale to the present output value.

VIDEO CONTROL OUTPUT VALUES[4]

DESCRIPTION	SYNC	BLANK	FH	BRT	DATA	OUT⁻(mA)[1]	OUT⁻(V)[2]	OUT⁻(IRE)[3]
Sync	1	X	X	X	X	28.57	-1.071	-40.0
Blank	0	1	X	X	X	20.83	-0.781	0.0
10% White	0	0	1	1	X	0.00	0.00	110.0
White	0	0	1	0	X	1.95	-0.073	100.0
Black	0	0	0	0	00	19.40	-0.728	7.5
White	0	0	0	0	FF	1.95	-0.073	100.0
10% Black	0	0	0	1	00	17.44	-0.654	17.5
10% White	0	0	0	1	FF	0.00	0.00	110.0

NOTES:
1. OUT^+ is complementary to OUT^-. Current is specified as conventional current when flowing into the device. $I_{OUT+} = 28.57 - I_{OUT-}$.
2. Voltage produced when driving the standard load configuration (37.5 ohms). See Figure 4.
3. 140 IRE units = 1.00V
4. RS-343A tolerance on all control values is assumed.

DATA INPUTS

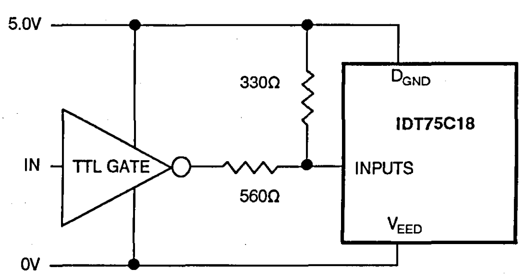
The inputs of the IDT75C18 are single ended, ECL-compatible. Internal pull down resistors force unconnected pins to a logic LOW level.

In the synchronous mode (FT is LOW), the data inputs are registered by the rising edge of CONV. The data inputs must be stable for a set-up time (t_S) before, and a hold time (t_H) after, the rising edge of CONV. In the asynchronous mode (FT is HIGH), the input registers are disabled and only the minimum pulse widths are relevant. In this mode, the analog output changes asynchronously in response to the input data.

SYMBOL	FUNCTION
D_1	Data Bit 1 (MSB)
D_2	
D_3	•
D_4	
D_5	•
D_6	
D_7	•
D_8	Data Bit 8 (LSB)

The inputs of the IDT75C18 are voltage comparators with the threshold level set to approximately -1.27V, ensuring the correct logic state when driven by standard ECL outputs. It is possible to overdrive the inputs without harming the device, allowing a direct interface to CMOS logic. In general, the input signals will correctly drive the IDT75C18 as long as they remain between V_{EED}, V_{EEA} and A_{GND}, D_{GND} and meet the V_{IL} and V_{IH} specifications.

The diagram below shows a simple two resistor level shifter which allows the IDT75C18 to be driven from TTL signals.

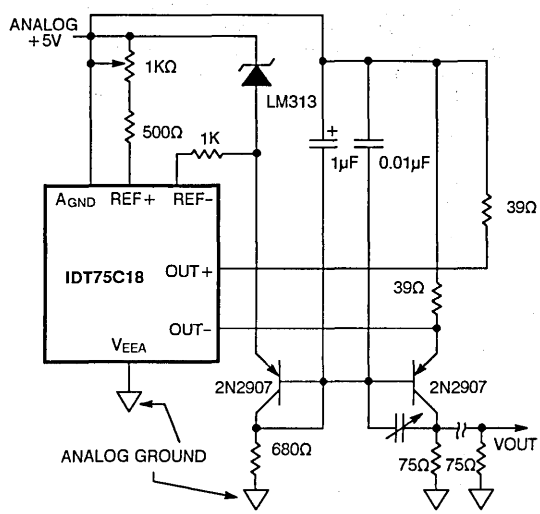


CLOCK INPUT CONV

The clock input to the IDT75C18 (CONV) is a differential ECL-compatible input. This signal may be driven single ended by connecting $\overline{CONV}$ to a suitable bias voltage (V_{BB}) which determines the switching threshold of CONV.

ANALOG OUTPUTS

The two analog outputs of the IDT75C18 are high impedance complementary current sinks which are capable of driving a doubly terminated 75 ohm load to standard video levels. The output voltage will be the product of the output current and the effective load impedance and will usually be between 0 and -1V when the V_{EE} = -5.2V. The outputs sink current from A_{GND}, so that in the positive supply case (interfacing to CMOS or TTL), the output voltage swings between +5V and +4V. In AC coupled applications, this DC bias is unimportant. Shown below is a simple circuit which references the output voltage to the most negative supply.



ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
POWER SUPPLIES			
V_{EED}	Measured to D_{GND}	-7.0 to +0.05	V
V_{EEA}	Measured to D_{GND}	-7.0 to +0.05	V
A_{GND}	Measured to D_{GND}	-0.5 to +0.5	V
INPUT VOLTAGES			
CONV, Data & Controls	Measured to D_{GND}	V_{EED} to 0.5	V
REF Input, Applied Voltage (2)	Measured to A_{GND}	V_{EEA} to 0.5	V
REF Input, Applied Current (3,4)	REF +	6.0	mA
	REF -	0.5	mA
OUTPUT			
Analog Output, Applied Voltage (2)	Measured to A_{GND}	-2.0 to +0.4	V
Analog Output, Applied Current (3,4)		50	mA
Short Circuit Duration		Unlimited	
TEMPERATURE			
Operating, Ambient	Military	-55 to +125	°C
	Commercial	0 to +70	°C
Storage	Military	-65 to +150	°C
	Commercial	-55 to +125	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{EED}	Digital Supply Voltage (REF D_{GND})		-4.9	-5.2	-5.5	V
V_{EEA}	Analog Supply Voltage (REF A_{GND})		-4.9	-5.2	-5.5	V
V_{AGND}	Analog Ground Voltage (REF D_{GND})		-0.1	0	+0.1	V
V_{EEA}-V_{EED}	Supply Voltage Differential		-0.1	0	+0.1	V
V_{ICM}	CONV, Common Mode Range		-0.5	—	-2.5	V
V_{IDF}	CONV, Differential Range		0.4	—	1.2	V
V_{IL}	Input Voltage, Logic LOW		-1.49	—	—	V
V_{IH}	Input Voltage, Logic HIGH		—	—	-1.045	V
I_{REF}	Reference Current, Video Std.(1)		1.059	1.115	1.171	mA
	8-Bit Lin.		1.0	–	1.3	mA
T_A	Ambient Temperature	MIL.	-55	–	+125	°C
		COM'L.	0	–	+70	°C

NOTE:
1. Minimum and maximum values allowed by ±5% variation given in RS-343A and RS-170 after initial gain correction of device.

DC ELECTRICAL CHARACTERISTICS

Specified over the Recommended Operating Conditions unless otherwise stated.

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
I_{EEA}+ I_{EED}	Supply Current	V_{EEA} = V_{EED} = Max.,[1]Static	—	125	mA
C_{REF}	Equivalent Input C, REF (+), REF (-)		—	5	pF
C_I	Input Capacitance, Data & Controls		—	5	pF
V_{OCP}	Compliance Voltage, +Output		-1.2	+0.1	V
V_{OCN}	Compliance Voltage, -Output		-1.2	+0.1	V
R_O	Equivalent Out R		20	—	kΩ
C_O	Equivalent Out C		—	20	pF
I_{OP}	Max. I, +Output	V_{EEA} = Typ., SYNC = BLANK= 0 FH = BRT = 1	30	—	mA
I_{ON}	Max. I, -Output	V_{EEA} = Typ.,SYNC = 1	30	—	mA
I_{IL}	Input Current, Logic LOW, Data & Controls	V_{EED} = Max.; V_I = -1.40V	—	200	µA
I_{IH}	Input Current, Logic HIGH, Data & Controls	V_{EED} = Max.; V_I = -1.00V	—	200	µA
I_{IC}	Input Current, CONV	V_{EED} = Max.; -2.5 < V_I < -0.5	—	50	µA

NOTE:
1. Worst case for all Data and Control States. No termination on I_{OUT+} or I_{OUT-}.

AC ELECTRICAL CHARACTERISTICS

Specified over the Recommended Operating Conditions unless otherwise stated.

SYMBOL	PARAMETERS	TEST CONDITIONS	IDT75C18x70 MIN.	IDT75C18x70 MAX.	IDT75C18x100 MIN.	IDT75C18x100 MAX.	IDT75C18x125 MIN.	IDT75C18x125 MAX.	UNIT
F_S	Max. Conversion Rate	V_{EEA}, V_{EED} = Min.	—	70	—	100	—	125	MHz
t_{PWL}	CONV LOW Time	V_{EEA}, V_{EED} = Min.	6	—	5	—	4	—	ns
t_{PWH}	CONV HIGH Time	V_{EEA}, V_{EED} = Min.	6	—	5	—	4	—	ns
t_S	Set-up Time, Data & Control	V_{EEA}, V_{EED} = Min.	8	—	6	—	5	—	ns
t_H	Hold Time, Data & Control	V_{EEA}, V_{EED} = Min.	5	—	1	—	0	—	ns
t_{DSC}	CONV to OUT Delay	V_{EEA}, V_{EED} = Min. FT = 0	—	14	—	10	—	8	ns
t_{DST}	DATA to OUT Delay	V_{EEA}, V_{EED} = Min. FT = 1	—	20	—	16	—	13	ns
t_{SI}	Current Setting Time	V_{EEA}, V_{EED} = Min. FT = 0							
		0.2%	—	—	—	—	—	—	ns
		0.8%	—	—	—	—	—	—	ns
		3.2%	—	—	—	—	—	—	ns
t_{RI}	Current Rise Time	10% to 90% of Full Scale	—	3.0	—	2.1	—	1.7	ns

11

SYSTEM PERFORMANCE CHARACTERISTICS

Specified over the Recommended Operating Conditions unless otherwise stated.

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
ELI	Linearity Error Integral	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	0.2	%FS
ELD	Linearity Error Differential	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	0.2	%FS
IOF	Output Offset I	V_{EEA}, V_{EED} = Max. SYNC = BLANK = 0, FH = BRT = 1	–	±10	μA
EG	Abs. Gain Error	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	±5	%FS
TCG	Gain Error Tempco		–	±0.024	%FS/°C
BWR	Ref. Bandwidth -3dB	ΔV_{REF} = 1mV	1		MHz
DP	Differential Phase	4 x NTSC	–	1.0	Deg.
DG	Differential Gain	4 x NTSC	–	2.0	%
PSRR	Power Supp. Rej. Ratio	V_{EEA}, V_{EED}, I_{REF} = Typ.(1)	–	45	dB
		V_{EEA}, V_{EED}, I_{REF} = Typ.(2)	–	55	dB
PSS	Power Supp. Sensitivity	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	120	μV/V
GC	Peak Glitch Charge	Registered Mode Typ. (3, 4)	–	800	f_c
GI	Peak Glitch Current	Registered Mode	–	1.2	mA
GE	Peak Glitch Energy	Registered Mode Typ. (4)	–	30	pV-Sec
FT_C	Clock Feedthrough	Data Constant (5)	–	-50	dB
FT_D	Data Feedthrough	Clock Constant (5)	–	-50	dB

NOTES:

1. 20kHz, ±0.3V ripple superimposed on V_{EEA}, V_{EED} ; dB relative to full gray scale.
2. 60Hz, ±0.3V ripple superimposed on V_{EEA}, V_{EED} ; dB relative to full gray scale.
3. $f_{Coulombs}$ = microamps x nanoseconds.
4. 37.5Ω load. Because glitches tend to be symmetric, average glitch area approaches zero.
5. dB relative to full gray scale, 250MHz bandwidth limit.

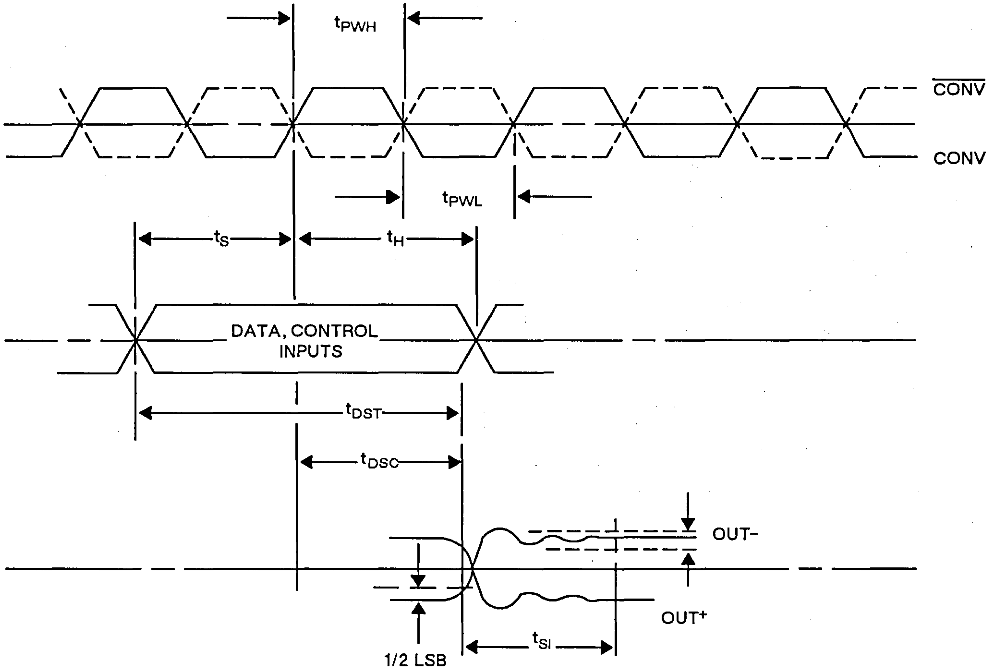


Figure 1. Timing Diagram

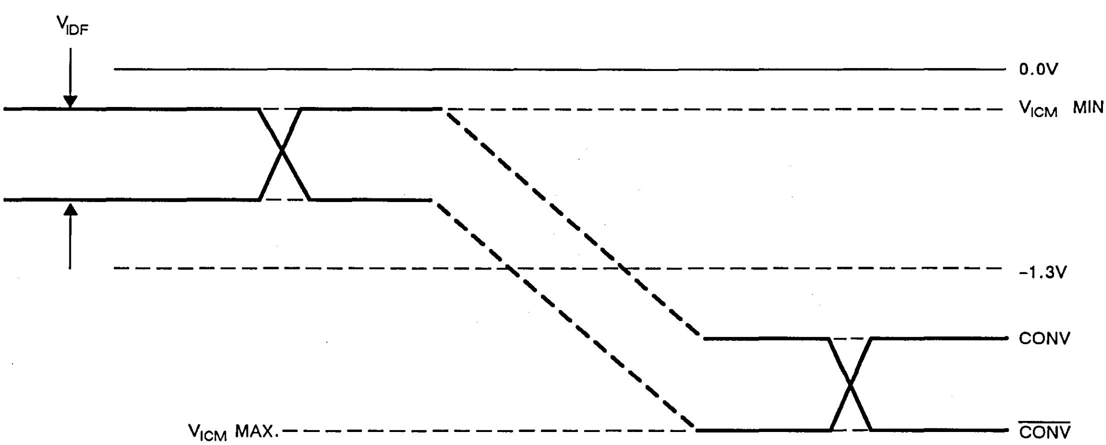


Figure 2. $\overline{\text{CONV}}$ert, CONVert Switching Levels

11

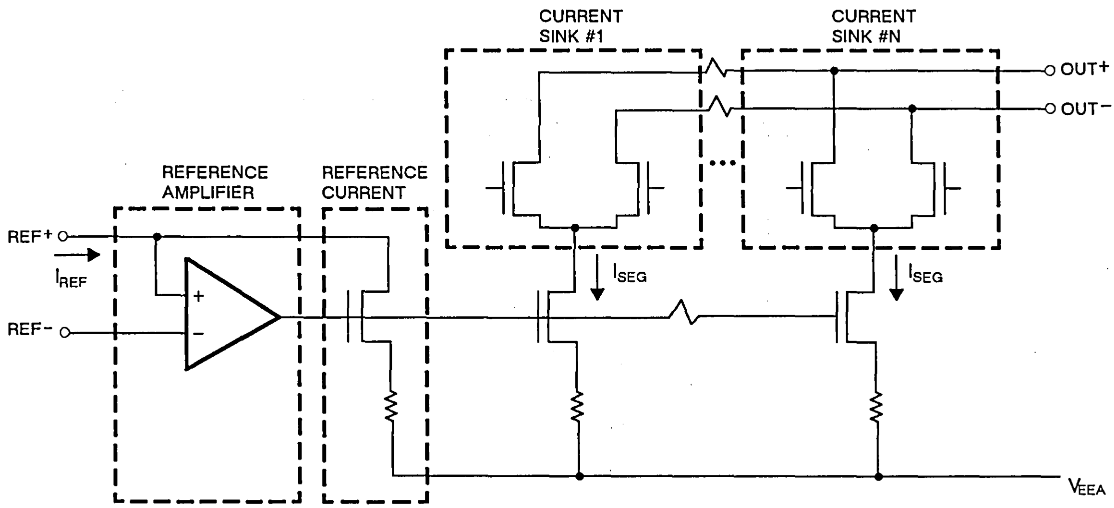


Figure 3. Equivalent Output Circuit

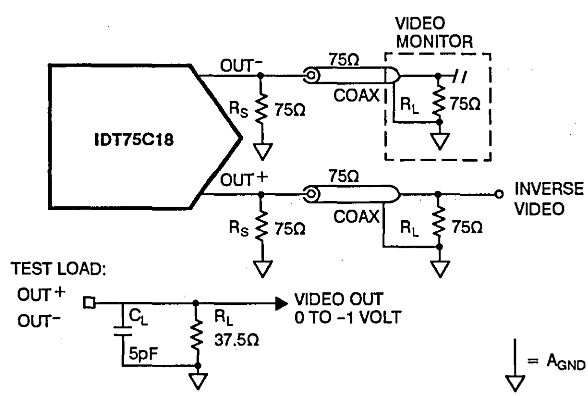


Figure 4. Standard Load Configuration

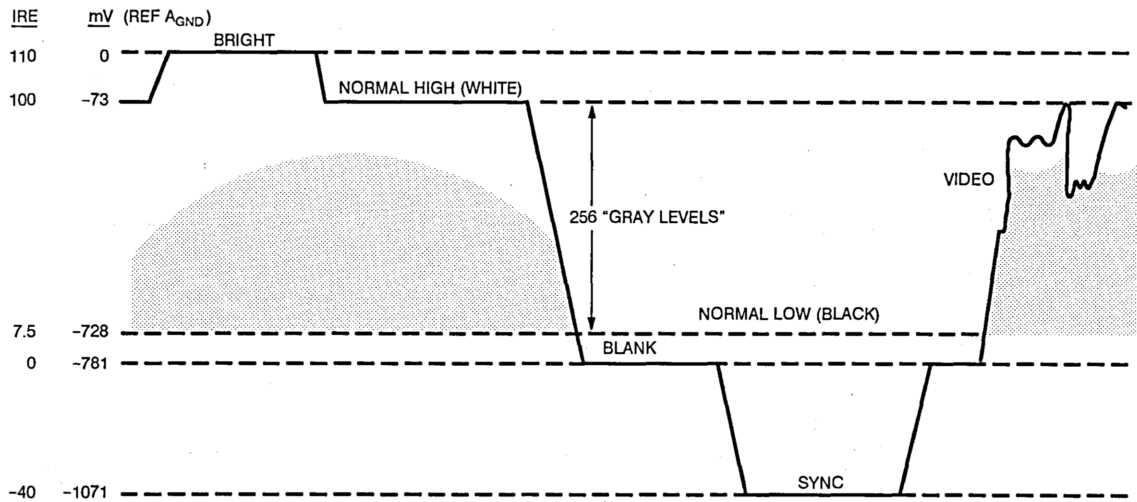
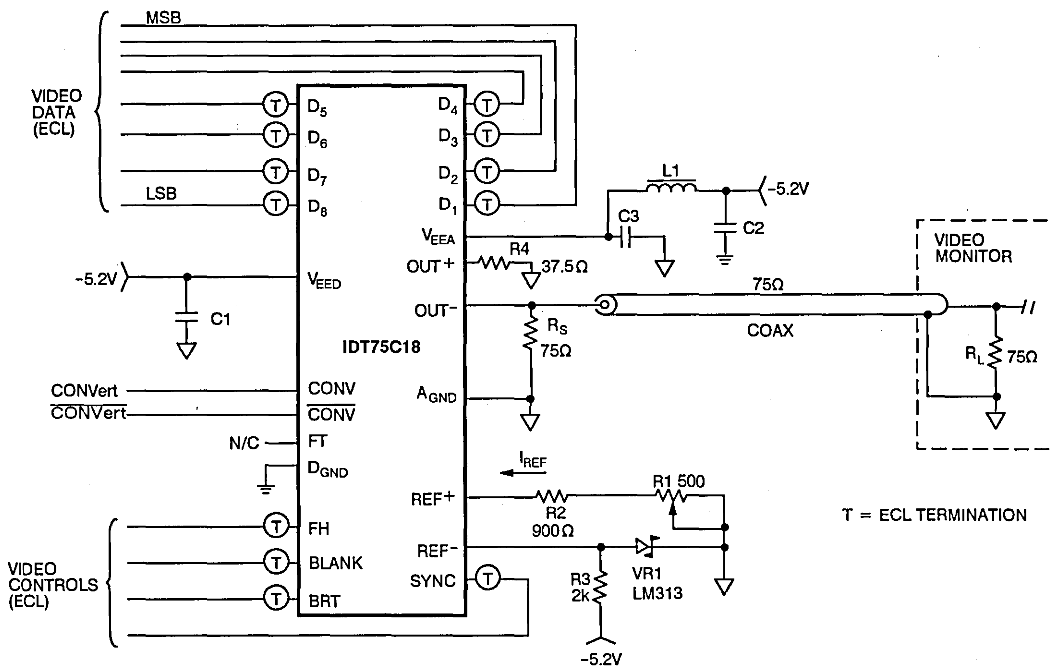


Figure 5. Video Output Waveform for Out- and Standard Load Configuration



PARTS LIST

RESISTORS			
R1	1kΩ	Pot	10 Turn
R2	900Ω	1/8W	1% Metal Film
R3	2.00kΩ	1/8W	1% Metal Film
R4	37.5Ω	1/8W	1% Metal Film
CAPACITORS			
C1-C3	0.1μF	50V	Ceramic disc
INTEGRATED CIRCUITS			
U1	IDT75C18	D/A Converter	
VOLTAGE REFERENCES			
VR1	LM113 or LM313	Bandgap Reference	
INDUCTORS			
L1	Ferrite Bead Shield Inductor Fair-Rite P/N 2743001112 or Similar		

Figure 6. Typical Interface Circuit

ORDERING INFORMATION

IDT XXXX (Device Type) X (Power) X (Speed) X (Package) X (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	BLANK	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	TP	Plastic THINDIP
	D	CERDIP
	L	Leadless Chip Carrier
Speed	70	Speed in Megahertz
	100	Speed in Megahertz
	125	Speed in Megahertz
Power	S	Standard Power
Device Type	75C18	ECL-Compatible

Integrated Device Technology, Inc.

9-BIT CMOS VIDEO DAC

IDT75C19

FEATURES:

- Graphics-ready
- Function-compatible with TRW TDC1018
- 9 bits, 1/2 LSB linearity
- 70, 100, 125MHz models available
- ECL-compatible inputs
- Low power dissipation < 400mW
- Power supply noise rejection > 50dB
- Registered data and video controls
- Differential current outputs
- Flexible video controls
- Inherently low glitch energy
- Multiplying mode capability
- Single 5V power supply
- Available in 24-pin hermetic DIP, 24-pin plastic DIP and 28-pin LCC
- Military product is compliant to MIL-STD-883, Class B

DESCRIPTION:

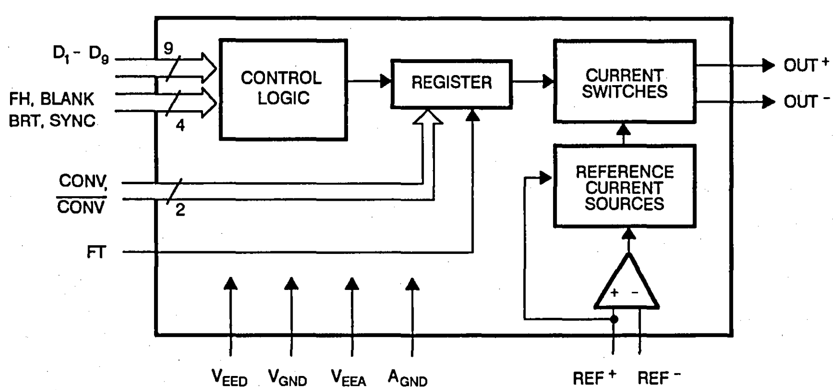
The IDT75C19 is a 70/100/125 MegaSample per Second (MSPS), 9-bit Digital to Analog Converter. It can directly drive a doubly terminated 75Ω load to levels compatible with RS-343A. Four special controls for blanking, synchronization and highlighting allow the device to be used in typical video applications with no extra components.

The IDT75C19 is built using IDT's high-performance CEMOS ™ process. Innovative design methods, which include on-chip data registers and precise matching of propagation delays, as well as an improved segmenting/decoding architecture, significantly reduce glitch energy. The IDT75C19 offers high-performance and low power in a 24-pin hermetic DIP, 24-pin plastic DIP or 28-pin LCC.

The IDT75C19 is functionally compatible with the TRW TDC1018, with the advantage of low power due to CMOS processing. Besides providing higher reliability by running cooler, power supply requirements are reduced. Another advantage of the lower power dissipation is that this part may be packaged in a space-saving, cost-effective, 0.3 inch plastic package.

The IDT75C19 military DAC is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

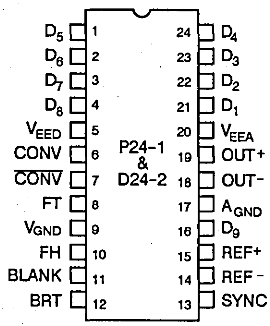


CEMOS is a trademark of Integrated Device Technology, Inc.

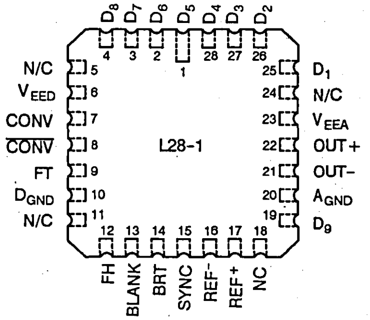
MILITARY AND COMMERCIAL TEMPERATURE RANGES — DECEMBER 1987

DSC-5001/-

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL DESCRIPTION
GENERAL INFORMATION

The IDT75C19 output current is proportional to the product of the digital input data and the analog reference current. All the digital inputs, data and control, are compatible with standard ECL logic levels. The IDT75C19 is normally operated synchronously with data being latched by the rising edge of the convert clock, CONV. FT, the feedthrough control input, determines the operating mode. When FT is LOW, the part operates in the synchronous mode and the low-to-high transition of the convert clock, CONV, latches data and control values into internal D-type registers. The registered values are then decoded and presented to switched current sinks which produce the appropriate analog output values. When FT is HIGH, the part operates asynchronously and the digital inputs are not latched. The analog output, then, changes in response to the digital inputs without regard to clock. FT is the only asynchronous input and is typically tied to the appropriate DC level.

The IDT75C19 uses a 6x3 segmented DAC approach where the six MSBs of the input data are decoded into a parallel "Thermometer" code which produces sixty-four "coarse" output levels. The remaining three LSBs of the input data drive seven binary weighted current switches with a total contribution of one-sixty-fourth of full scale. The MSB and LSB currents are summed at the output to produce 512 analog levels.

SYNC, BLANK, FH (Force High) and BRT (BRighT) are special control inputs which drive appropriately weighted current switches. These currents are summed at the output with the level produced by the data inputs to allow for specific levels required by video applications such as the sync pulses and the blanking levels.

POWER CONSIDERATIONS

The IDT75C19 operates from separate analog and digital supplies to provide the highest noise immunity on the analog output to digital switching spikes. All power and ground pins must be connected.

REFERENCE CONSIDERATIONS

The IDT75C19 has two reference inputs, REF^+ and REF^-, which are simply the non-inverting and inverting inputs to an internal buffer amplifier. The output of this amplifier serves as the reference for the current sources in the DAC. The feedback loop internally includes a transistor which is identical to the current sink transistors, guaranteeing that the reference current will be precisely mirrored in the DAC.

Since the output currents are proportional to the digital data and the reference current, the full-scale output current may be adjusted over a limited range by varying the reference current. In the same vein, the stability of the output depends strongly on the stability of the reference. The reference current is normally applied to REF^+, while REF^- is usually connected to a negative reference through a resistor equal to the effective impedance seen on REF^+.

CONTROLS

The IDT75C19 has four special control inputs: SYNC, BLANK, FH (Force High) and BRT (BRighT), as well as FT (Feed Through control). Typically, the IDT75C19 is operated in the synchronous mode which ensures the lowest output noise. When FT is forced HIGH, the input registers pass the data and control information through without latching, allowing the analog output to change asynchronously.

In the synchronous mode, the control inputs are registered by the rising edge of CONV in the same manner as the data inputs. The controls, like the data, must be stable for a set-up time (t_S) before, and a hold time (t_H) after, the rising edge of CONV. In the asynchronous mode, only the minimum pulse widths are relevant.

The video controls produce specific output levels which are used for frame synchronization, horizontal blanking, etc. as described in various standards such as RS-343A. The effect of these controls on the analog output is shown below. The internal logic simplifies the use of the controls in video applications. BLANK, SYNC and FH override the data inputs. SYNC overrides all other inputs and produces a full negative level. FH drives the analog output to full-scale producing a reference white level. The BRT control creates a "whiter than white" level by adding 10% of full-scale to the present output value.

VIDEO CONTROL OUTPUT VALUES [4]

DESCRIPTION	SYNC	BLANK	FH	BRT	DATA	OUT⁻(mA)[1]	OUT⁻(V)[2]	OUT⁻(IRE)[3]
Sync	1	X	X	X	X	28.57	-1.071	-40.0
Blank	0	1	X	X	X	20.83	-0.781	0.0
10% White	0	0	1	1	X	0.00	0.00	110.0
White	0	0	1	0	X	1.95	-0.073	100.0
Black	0	0	0	0	000	19.40	-0.728	7.5
White	0	0	0	0	1FF	1.95	-0.073	100.0
10% Black	0	0	0	1	000	17.44	-0.654	17.5
10% White	0	0	0	1	1FF	0.00	0.00	110.0

NOTES:
1. OUT^+ is complementary to OUT^-. Current is specified as conventional current when flowing into the device. $I_{OUT^+} = 28.57 - I_{OUT^-}$.
2. Voltage produced when driving the standard load configuration (37.5 ohms). See Figure 4.
3. 140 IRE units = 1.00V
4. RS-343A tolerance on all control values is assumed.

DATA INPUTS

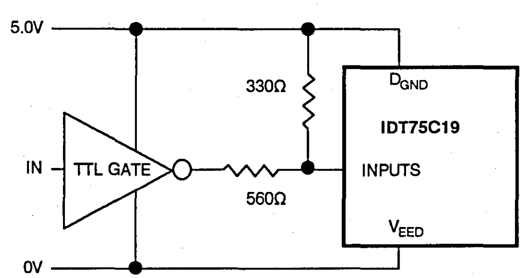
The inputs of the IDT75C19 are single ended, ECL-compatible. Internal pull down resistors force unconnected pins to a logic LOW level.

In the synchronous mode (FT is LOW), the data inputs are registered by the rising edge of CONV. The data inputs must be stable for a set-up time (t_S) before, and a hold time (t_H) after, the rising edge of CONV. In the asynchronous mode (FT is HIGH), the input registers are disabled and only the minimum pulse widths are relevant. In this mode, the analog output changes asynchronously in response to the input data.

SYMBOL	FUNCTION
D_1	Data Bit 1 (MSB)
D_2	
D_3	
D_4	•
D_5	•
D_6	•
D_7	
D_8	
D_9	Data Bit 9 (LSB)

The inputs of the IDT75C19 are voltage comparators with the threshold level set to approximately -1.27V, ensuring the correct logic state when driven by standard ECL outputs. It is possible to overdrive the inputs without harming the device, allowing a direct interface to CMOS logic. In general, the input signals will correctly drive the IDT75C19 as long as they remain between V_{EED}, V_{EEA} and A_{GND}, D_{GND} and meet the V_{IL} and V_{IH} specifications.

The diagram below shows a simple two resistor level shifter which allows the IDT75C19 to be driven from TTL signals.

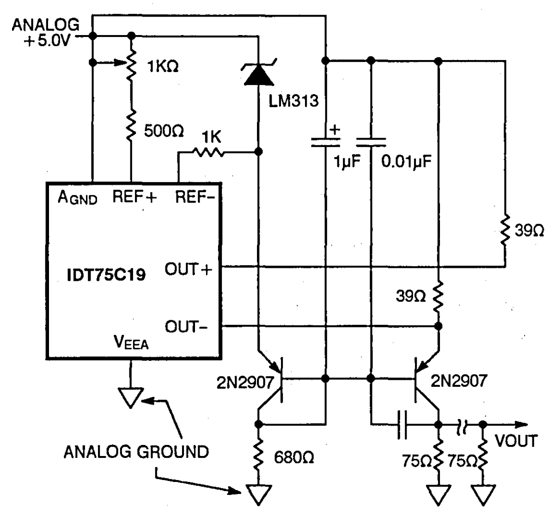


CLOCK INPUT CONV

The clock input to the IDT75C19 (CONV) is a differential ECL-compatible input. This signal may be driven single ended by connecting $\overline{CONV}$ to a suitable bias voltage (V_{BB}) which determines the switching threshold of CONV.

ANALOG OUTPUTS

The two analog outputs of the IDT75C19 are high impedance complementary current sinks which are capable of driving a doubly terminated 75 ohm load to standard video levels. The output voltage will be the product of the output current and the effective load impedance and will usually be between 0V and -1V when V_{EE} = -5.2V. The outputs sink current from A_{GND}, so that in the positive supply case (interfacing to CMOS or TTL), the output voltage swings between +5V and +4V. In AC coupled applications, this DC bias is unimportant. Shown below is a simple circuit which references the output voltage to the most negative supply.



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	VALUE	UNIT
POWER SUPPLIES			
V_{EED}	Measured to D_{GND}	-7.0 to +0.05	V
V_{EEA}	Measured to D_{GND}	-7.0 to +0.05	V
A_{GND}	Measured to D_{GND}	-0.5 to +0.5	V
INPUT VOLTAGES			
CONV, Data & Controls	Measured to D_{GND}	V_{EED} to 0.5	V
REF Input, Applied Voltage[2]	Measured to A_{GND}	V_{EEA} to 0.5	V
REF Input, Applied Current[3,4]	REF +	6.0	mA
	REF -	0.5	mA
OUTPUT			
Analog Output, Applied Voltage[2]	Measured to A_{GND}	-2.0 to +0.4	V
Analog Output, Applied Current[3,4]		50	mA
Short Circuit Duration		Unlimited	
TEMPERATURE			
Operating, Ambient	Military	-55 to +125	°C
	Commercial	0 to +70	°C
Storage	Military	-65 to +150	°C
	Commercial	-55 to +125	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{EED}	Digital Supply Voltage (REF D_{GND})		-4.9	-5.2	-5.5	V
V_{EEA}	Analog Supply Voltage (REF A_{GND})		-4.9	-5.2	-5.5	V
V_{AGND}	Analog Ground Voltage (REF D_{GND})		-0.1	0	+0.1	V
V_{EEA}-V_{EED}	Supply Voltage Differential		-0.1	0	+0.1	V
V_{ICM}	CONV, Common Mode Range		-0.5	—	-2.5	V
V_{IDF}	CONV, Differential Range		0.4	—	1.2	V
V_{IL}	Input Voltage, Logic LOW		-1.49	—	—	V
V_{IH}	Input Voltage, Logic HIGH		—	—	-1.045	V
I_{REF}	Reference Current, Video Std.[1]		1.059	1.115	1.171	mA
	9-Bit Lin.		1.0	—	1.3	mA
T_A	Ambient Temperature	MIL.	-55	—	125	°C
		COM'L.	0	—	70	°C

NOTE:

1. Minimum and maximum values allowed by ±5% variation given in RS-343A and RS-170 after initial gain correction of device.

11

DC ELECTRICAL CHARACTERISTICS

Specifications over the recommended operating conditions, unless otherwise stated.

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
$I_{EEA}+$ I_{EED}	Supply Current	$V_{EEA} = V_{EED} = $ Max.(1), Static	–	125	mA
C_{REF}	Equivalent Input C, REF (+), REF (-)		–	5	pF
C_I	Input Capacitance, Data & Controls		–	5	pF
V_{OCP}	Compliance Voltage, +Output		-1.2	+0.1	V
V_{OCN}	Compliance Voltage, -Output		-1.2	+0.1	V
R_O	Equivalent Out R		20	–	kΩ
C_O	Equivalent Out C		–	20	pF
I_{OP}	Max. I, +Output	V_{EEA} = Typ.,SYNC = BLANK= 0 FH = BRT = 1	30	–	mA
I_{ON}	Max. I, -Output	V_{EEA} = Typ., SYNC = 1	30	–	mA
I_{IL}	Input Current, Logic LOW, Data & Controls	V_{EED} = Max.; V_I = -1.40V	–	200	µA
I_{IH}	Input Current, Logic HIGH, Data & Controls	V_{EED} = Max.; V_I = -1.00V	–	200	µA
I_{IC}	Input Current, CONV	V_{EED} = Max.; $-2.5 < V_I < -0.5$	–	50	µA

NOTE:

1. Worst case for all Data and Control States. No termination on $I_{OUT}+$ or $I_{OUT}-$.

AC ELECTRICAL CHARACTERISTICS

Specifications over the recommended operating conditions, unless otherwise stated.

SYMBOL	PARAMETERS	TEST CONDITIONS	IDT75C19 x 70 MIN.	IDT75C19 x 70 MAX.	IDT75C19 x 100 MIN.	IDT75C19 x 100 MAX.	IDT75C19 x 125 MIN.	IDT75C19 x 125 MAX.	UNIT
F_S	Max. Conversion Rate	V_{EEA}, V_{EED} = Min.	–	70	–	100	–	125	MHz
t_{PWL}	CONV LOW Time	V_{EEA}, V_{EED} = Min.	6	–	5	–	4	–	ns
t_{PWH}	CONV HIGH Time	V_{EEA}, V_{EED} = Min.	6	–	5	–	4	–	ns
t_S	Set-up Time, Data & Control	V_{EEA}, V_{EED} = Min.	8	–	6	–	5	–	ns
t_H	Hold Time, Data & Control	V_{EEA}, V_{EED} = Min.	5	–	1	–	0	–	ns
t_{DSC}	CONV to OUT Delay	V_{EEA}, V_{EED} = Min. FT = 0	–	14	–	10	–	8	ns
t_{DST}	DATA to OUT Delay	V_{EEA}, V_{EED} = Min. FT = 1	–	20	–	16	–	13	ns
t_{SI}	Current Setting Time	V_{EEA}, V_{EED} = Min. FT = 0							
		0.2%	–	–	–	–	–	–	ns
		0.8%	–	–	–	–	–	–	ns
		3.2%	–	–	–	–	–	–	ns
t_{RI}	Current Rise Time	10% to 90% of Full Scale	–	3.0	–	2.1	–	1.7	ns

SYSTEM PERFORMANCE CHARACTERISTICS

Specifications over the recommended operating conditions, unless otherwise stated.

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
ELI	Linearity Error Integral	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	0.1	%FS
ELD	Linearity Error Differential	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	0.1	%FS
IOF	Output Offset I	V_{EEA}, V_{EED} = Max. SYNC = BLANK = 0, FH = BRT = 1	–	±10	µA
EG	Abs. Gain Error	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	±5	%FS
TCG	Gain Error Tempco		–	±0.024	%FS/°C
BWR	Ref. Bandwidth -3dB	ΔV_{REF} = 1mV	1		MHz
DP	Differential Phase	F_S = 4 x NTSC	–	1.0	Deg.
DG	Differential Gain	F_S = 4 x NTSC	–	2.0	%
PSRR	Power Supp. Rej. Ratio	V_{EEA}, V_{EED}, I_{REF} = Typ.(1)	–	45	dB
		V_{EEA}, V_{EED}, I_{REF} = Typ.(2)	–	55	dB
PSS	Power Supp. Sensitivity	V_{EEA}, V_{EED}, I_{REF} = Typ.(3,4)	–	120	µV/V
GC	Peak Glitch Charge	Registered Mode Typ.	–	800	f_C
GI	Peak Glitch Current	Registered Mode	–	1.2	mA
GE	Peak Glitch Energy	Registered Mode Typ.(4)	–	30	pV-Sec
FT_C	Clock Feedthrough	Data Constant(5)	–	-50	dB
FT_D	Data Feedthrough	Clock Constant(5)	–	-50	dB

NOTES:

1. 20kHz, ±0.3V ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
2. 60Hz, ±0.3V ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
3. $f_{Coulombs}$ = microamps x nanoseconds
4. 37.5Ω load. Because glitches tend to be symmetric, average glitch area approaches zero.
5. dB relative to full gray scale, 250MHz bandwidth limit.

11

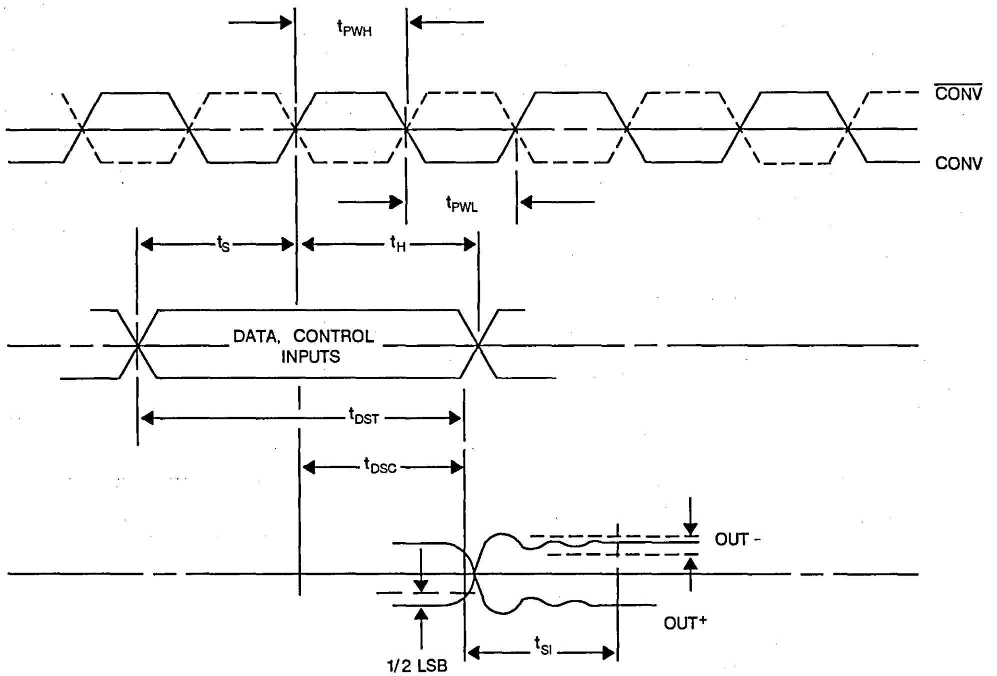


Figure 1. Timing Diagram

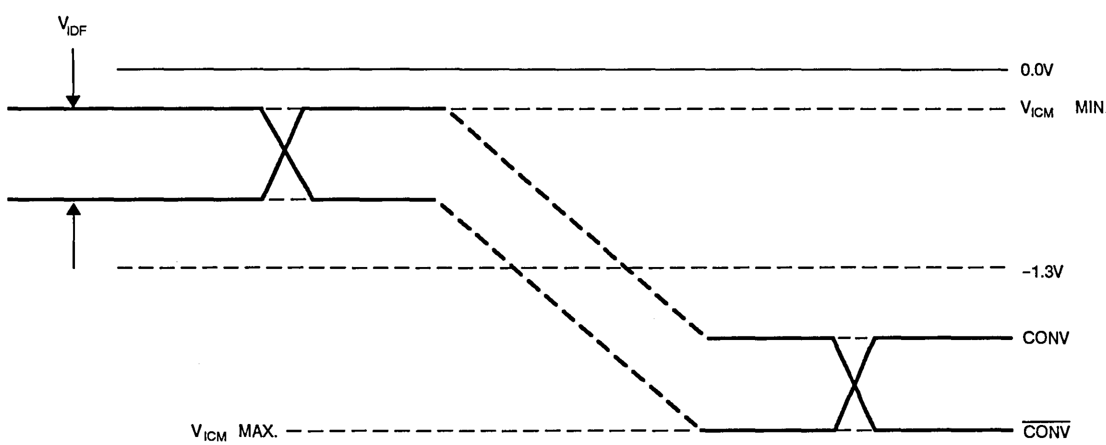


Figure 2. $\overline{\text{CONV}}$ert, CONVert Switching Levels

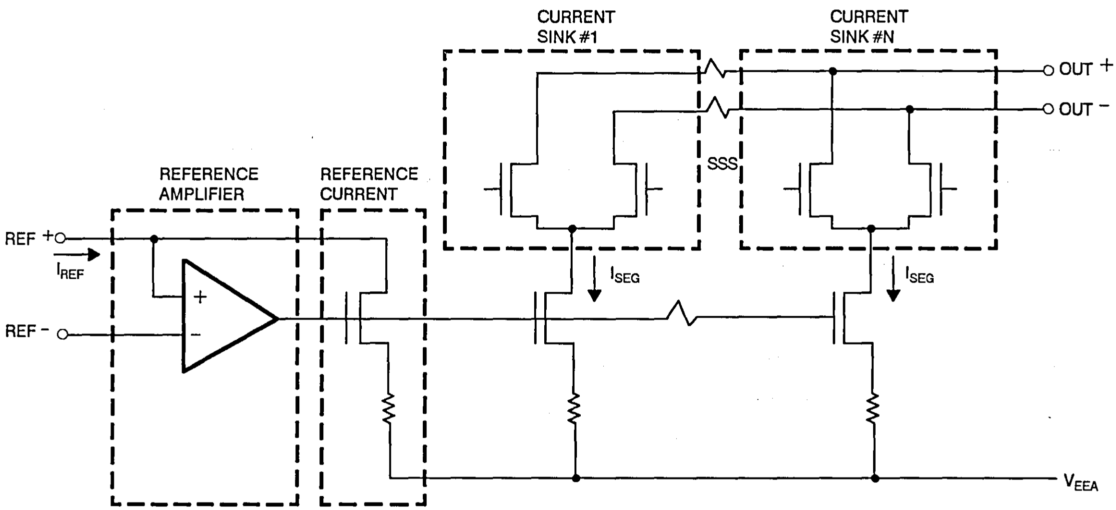


Figure 3. Equivalent Output Circuit

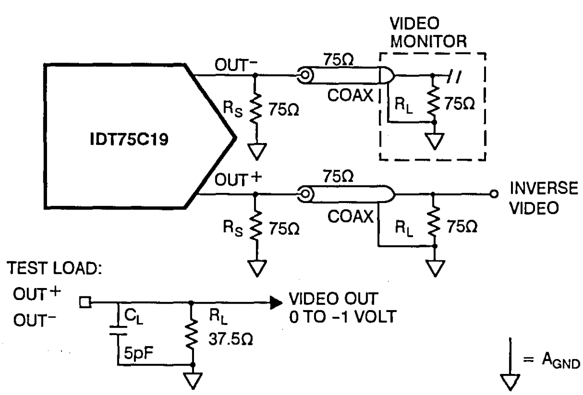


Figure 4. Standard Load Configuration

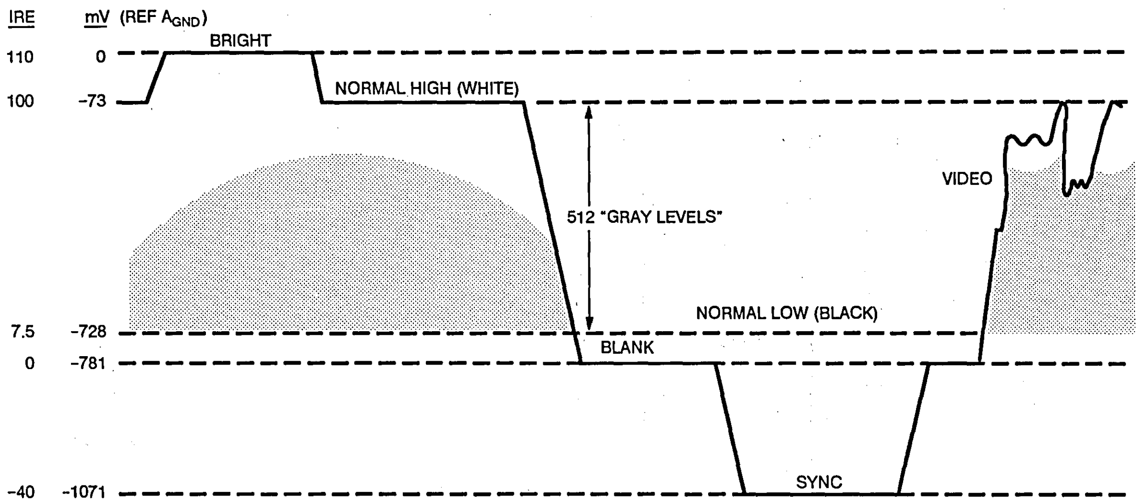
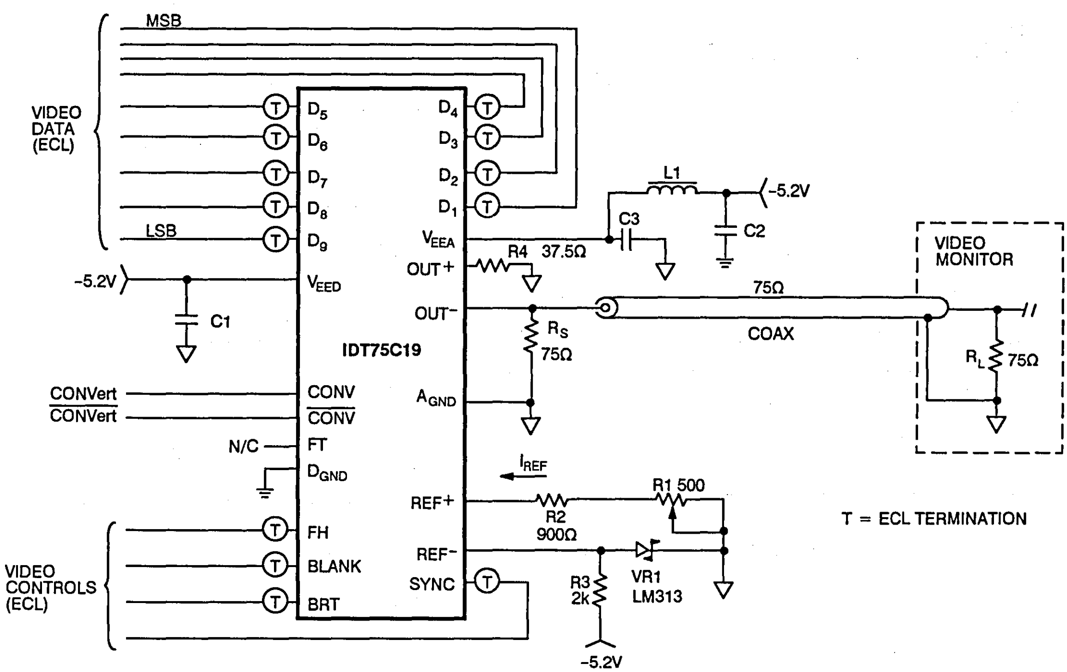


Figure 5. Video Output Waveform for Out- and Standard Load Configuration



PARTS LIST

RESISTORS			
R1	1kΩ	Pot	10 Turn
R2	900Ω	1/8W	1% Metal Film
R3	2.00kΩ	1/8W	1% Metal Film
R4	37.5Ω	1/8W	1% Metal Film
CAPACITORS			
C1-C3	0.1μF	50V	Ceramic disc
INTEGRATED CIRCUITS			
U1	IDT75C19	D/A Converter	
VOLTAGE REFERENCES			
VR1	LM113 or LM313	Bandgap Reference	
INDUCTORS			
L1	Ferrite Bead Shield Inductor Fair-Rite P/N 2743001112 or Similar		

Figure 6. Typical Interface Circuit

ORDERING INFORMATION

IDT XXXX X X X X

Device Type	Power	Speed	Package	Process/Temperature Range
XXXX	X	X	X	X

Process/Temperature Range

BLANK	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

TP	Plastic THINDIP
D	CERDIP
L	Leadless Chip Carrier

Speed

70	Speed in Megahertz
100	
125	

Power

S	Standard Power

Device Type

75C19	9-Bit CMOS Video DAC

Integrated Device Technology, Inc.

CMOS TRIPLE 8-BIT VIDEO DAC MODULE

ADVANCE INFORMATION IDT75MB38

FEATURES:

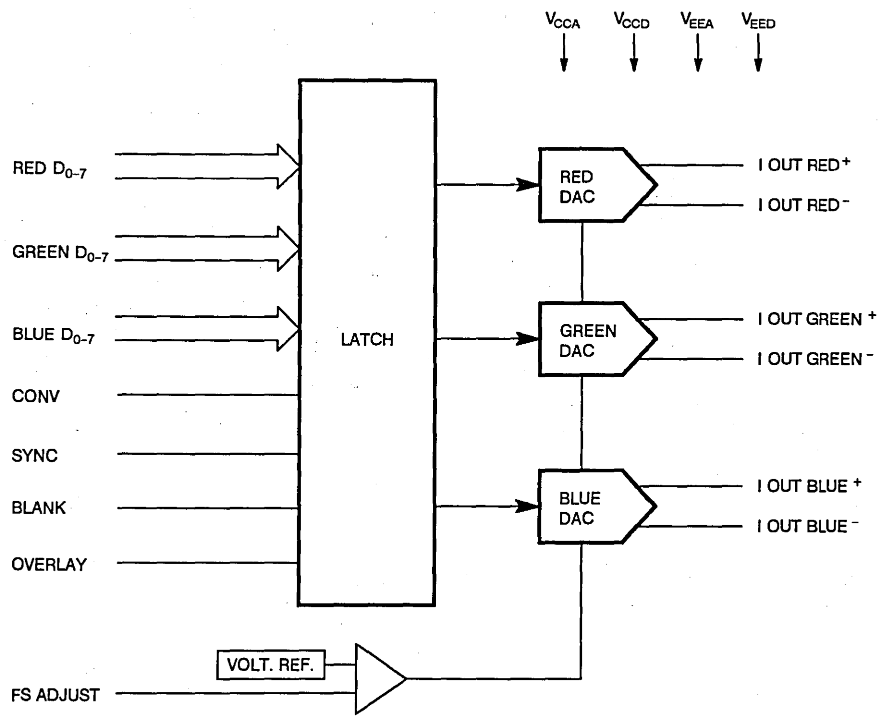
- Graphics Ready
- Pin-compatible with TDC1318 & BT109
- Triple 8-bit DACs, 1/2 LSB linearity
- 70/100/125MHz update rate
- ECL-compatible inputs
- Low power consumption: 1500mW
- On-board voltage reference
- Complementary current outputs
- Registered SYNC, BLANK and OVERLAY inputs
- Surface mount packages on an epoxy laminate substrate

DESCRIPTION:

The IDT75MB38 is a 70/100/125 MegaSample per Second (MSPS), triple 8-bit Digital to Analog Converter capable of directly driving a 75Ω load to standard video levels. Most applications require no extra registering, buffering or deglitching. All inputs are ECL-compatible and the part runs from a single -5.2V supply.

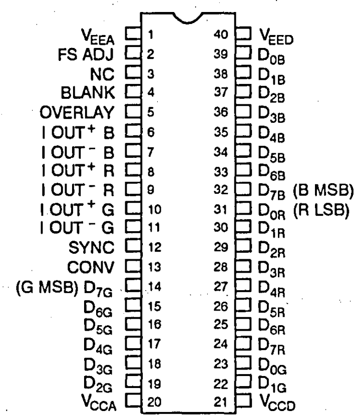
The IDT75MB38 is built using three IDT75C18 Video DACs in small outline plastic packages, mounted on an epoxy laminate (FR4) substrate. The module fits into a standard 40-pin DIP (600 mil) footprint. Due to IDT's high-performance CEMOS™ process, power consumption is kept under 1500mW.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP
TOP VIEW

GENERAL INFORMATION

The IDT75MB38 is built using three monolithic Video DACs, a voltage reference and an operational amplifier to control the full-scale output current. All devices are housed in plastic SOIC packages and are mounted on a multilayer FR4 substrate. Conventional through-hole pins are attached for connection to the user's printed circuit board.

The IDT75MB38 provides 24 data input pins (8 each for red, blue and green) which are ECL-compatible. Data are latched on the rising edge of the clock input, CONV. In addition, three control signals are available which ease the interface to RS-343 systems.

The IDT75MB38 outputs three pairs of complementary analog current signals which will directly drive the 75Ω inputs of a color video CRT. The current produced by these outputs is directly proportional to the product of the digital input data and the reference current.

POWER

The IDT75MB38 operates from separate analog and digital supplies to provide the highest noise immunity on the analog output to digital switching spikes. All power and ground pins must be connected and properly decoupled.

REFERENCE

The IDT75MB38 has an on-board voltage reference and associated circuitry which provides a bias voltage for the DAC current switches and sets the full-scale current. Typically, a 1.1K resistor is connected between the FS Adjust pin and V_{CCA} which provides the reference current to the DACs.

DATA INPUTS

The IDT75MB38 has 24 data inputs which are ECL-compatible and have an internal pull-down resistor which forces unconnected pins to their inactive state. Each DAC, red, green and blue, has 8 data inputs which are latched on the rising edge of the clock, CONV. Data must be valid for a set-up time (t_S) before and a hold time (t_H) after this edge to be correctly latched.

SYMBOL	FUNCTION
D_7	MSB
D_6	
D_5	•
D_4	•
D_3	•
D_2	
D_1	
D_0	LSB

CONTROL INPUTS

The IDT75MB38 has three special control inputs, SYNC, BLANK and OVERLAY, which ease the interface in video applications. These inputs are ECL-compatible and have an internal pull-down resistor which forces unconnected pins to their inactive state. The controls, as the data inputs, are latched on the rising edge of clock.

The video controls produce specific output levels for RS-343 compatible synchronization and blanking. Also provided is a 110% white Overlay function. SYNC is only active on the IOG output and overrides all other data and control on that output only. BLANK is active on all three DACs, overrides OVERLAY and data, and produces a "blacker than black" level. OVERLAY produces a "whiter than white" level and overrides data on all three DACs.

CLOCK

The clock input, CONV, is a single-ended, ECL-compatible input. On the rising edge of CONV, all data and control inputs are latched provided that they were valid for a set-up time before and a hold time after the edge.

ANALOG OUTPUTS

The IDT75MB38 has three complementary current outputs corresponding to the red, green and blue DACs. These outputs are high-impedance current sinks which can directly drive a doubly terminated 75Ω load to video levels compatible with the RS-343A standard. The output current is proportional to the product of the DAC input data and the reference current set on the FS Adj pin.

VIDEO OUTPUT VALUES[4]

DESCRIPTION	SYNC	BLANK	OVERLAY	DATA	I_{OUT-}[2] mA	V_{OUT-}[3] mV	I_{OUT+}[2] mA	V_{OUT+}[3] mV
110% White	0	0	1	X	0.00	0.00	28.56	-1071
Reference White	0	0	0	FF	1.95	-73	26.61	-998
Reference Black	0	0	0	00	19.41	-728	9.15	-343
Blank	0	1	X	X	20.83	-781	7.73	-290
Sync[1]	1	X	X	X	28.56	-1071	0	0

NOTES:

1. IOG output only. IOR and IOB have no SYNC input.
2. Current is specified as conventional current when flowing into the device.
3. Voltage produced when driving the standard load configuration, 37.5Ω.
4. RS-343A tolerance on all control values assumed.

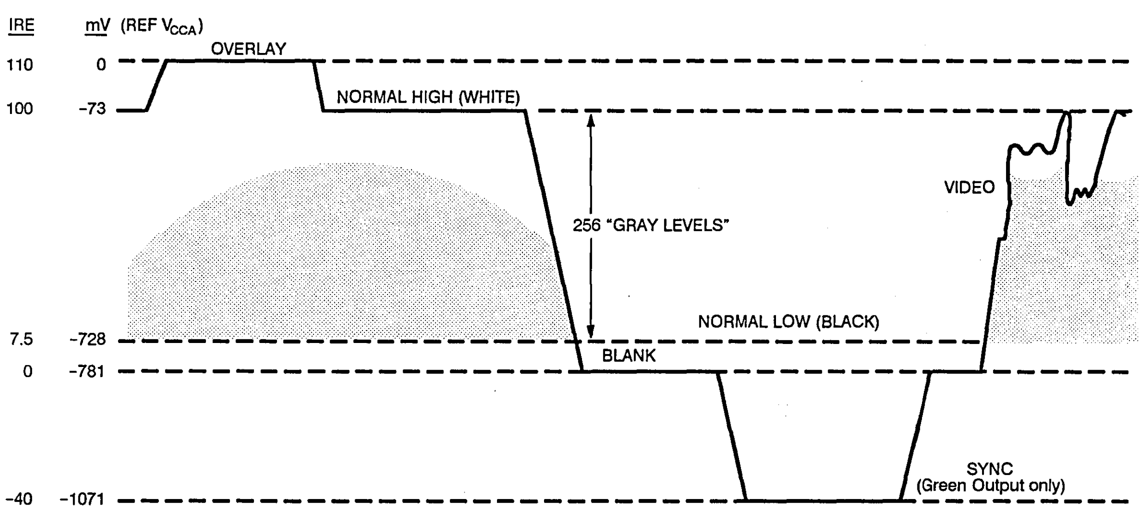


Figure 1. Video Output Waveform for Out- and Standard Load Configuration

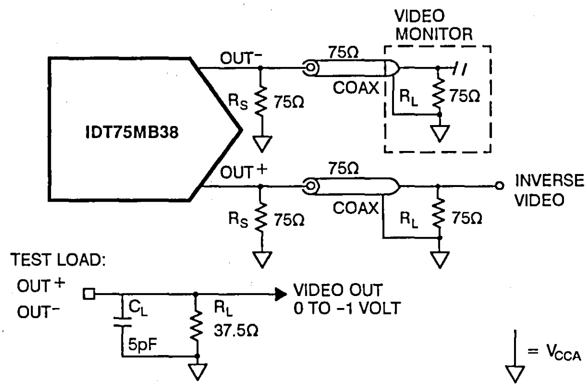


Figure 2. Standard Load Configuration

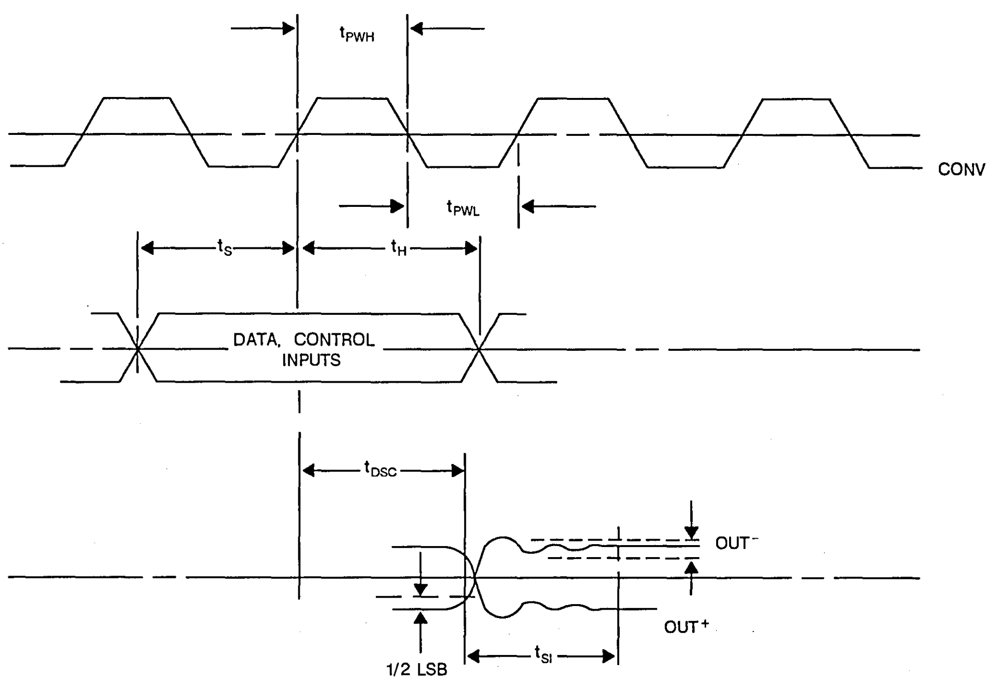


Figure 3. Timing Diagram

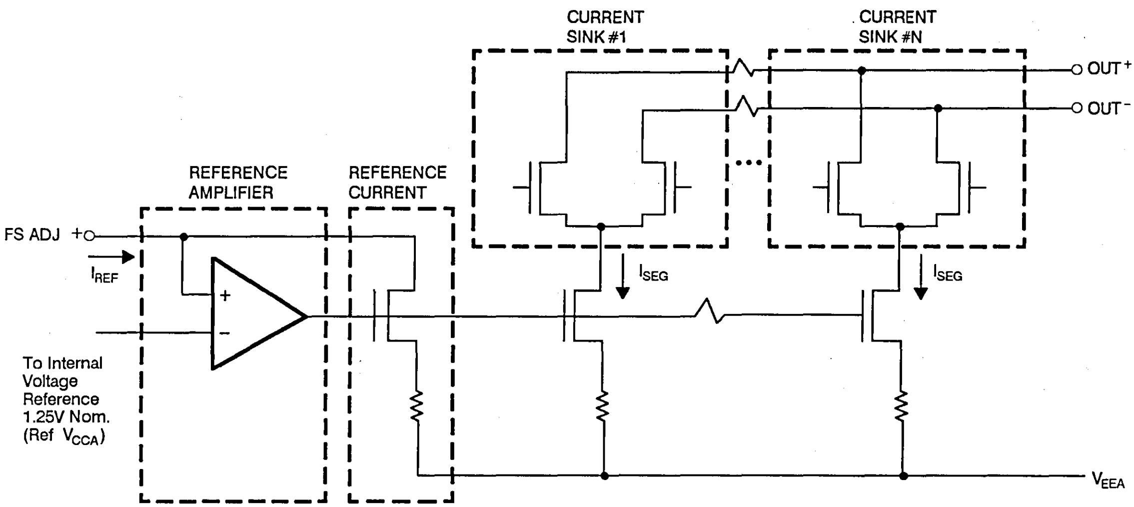


Figure 4. Equivalent Output Circuit

ORDERING INFORMATION

IDT XXXX X X X X
Device Type / Power / Speed / Package / Process/ Temperature Range

Process/Temperature Range	BLANK	Commercial (0°C to +70°C)
Package	P	Plastic DIP (Module)
Speed	70 100 125	Speed in Megahertz
Power	S	Standard Power
Device Type	75MB38	Triple 8-Bit Video DAC Module

Integrated Device Technology, Inc.

CMOS TRIPLE 8-BIT PALETTEDAC™

PRELIMINARY
IDT75C458

FEATURES:

- 125/110/80MHz operating speed
- Fixed pipeline delay: 8 clock cycles
- Triple 8-bit DACs
- Integral and differential linearity < 1/2LSB
- 256 x 24 Dual-Ported Color Palette RAM
- 4 x 24 Dual-Ported Overlay Palette RAM
- Multiplexed TTL pixel and overlay inputs
- RS-343A compatible RGB outputs
- Universal 8-bit MPU interface
- CEMOS ™ monolithic construction
- Single 5V power supply
- 84-pin ceramic and plastic PGA package
- Typical power dissipation: 1000mW
- Pin- and function-compatible with Brooktree BT458
- Military product is compliant to MIL-STD-883, Class B

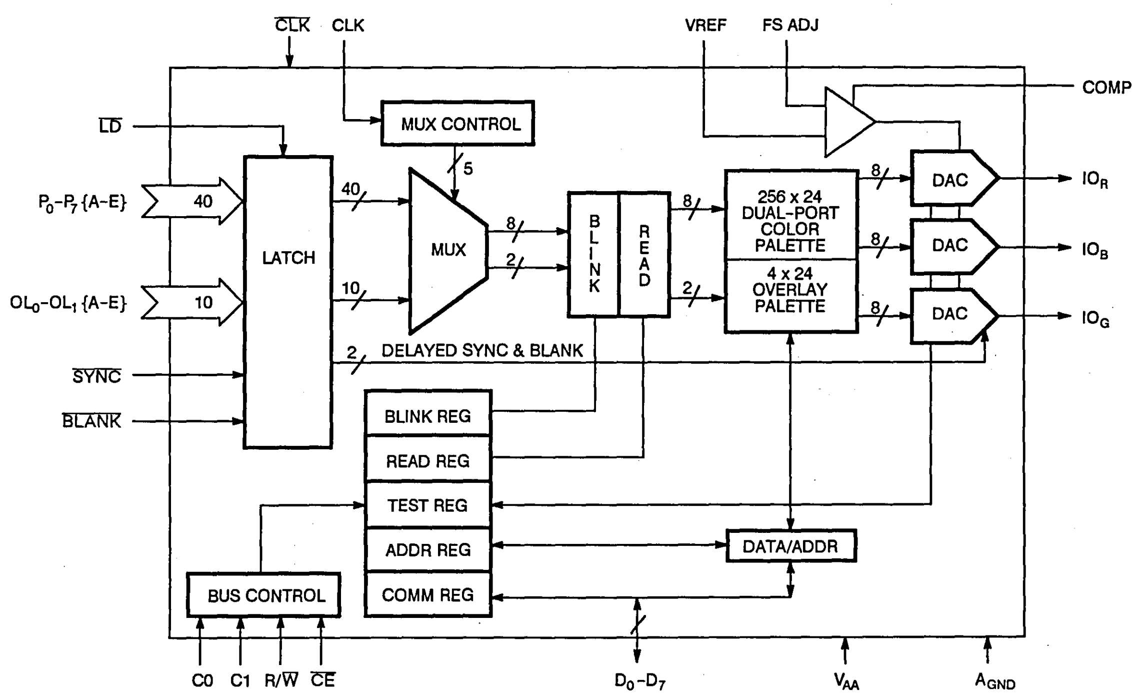
DESCRIPTION:

The IDT75C458 is a triple 8-bit video DAC with on-chip, dual-ported color palette memory. This chip is specifically designed for the display of high resolution color graphics. The architecture eliminates the ECL pixel interface by providing multiple TTL-compatible pixel ports and by multiplexing the pixel data on-chip.

The IDT75C458 supports up to 259 simultaneous colors from a palette of 16.8 million. Other features included on-chip are programmable blink rates, bit plane masking and blinking as well as a color overlay capability. The IDT75C458 generates RS-343A compatible red, green, and blue video outputs which are capable of directly driving a doubly terminated 75Ω coaxial cable.

The IDT75C458 military DACs are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS and PaletteDAC are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

	A	B	C	D	E	F	G	H	J	K	L	M
12	COMP	A_{GND}	V_{AA}	P_7\{D\}	P_7\{B\}	P_6\{E\}	P_6\{C\}	P_6\{B\}	P_5\{E\}	P_5\{C\}	P_5\{B\}	P_4\{E\}
11	IO_B	A_{GND}	V_{AA}	P_7\{E\}	P_7\{C\}	P_7\{A\}	P_6\{D\}	P_6\{A\}	P_5\{D\}	P_5\{A\}	P_4\{C\}	P_4\{A\}
10	IO_G	FSADJ	V_{REF}							P_4\{D\}	P_4\{B\}	$\overline{\text{SYNC}}$
9	V_{AA}	IO									$\overline{\text{BLANK}}$	$\overline{\text{LD}}$
8	C1	R/$\overline{\text{W}}$									$\overline{\text{CLK}}$	CLK
7	V_{AA}	C0									V_{AA}	V_{AA}
6	A_{GND}	A_{GND}									P_3\{E\}	A_{GND}
5	$\overline{\text{CE}}$	D_7									P_3\{C\}	P_3\{D\}
4	D_6	D_5									P_3\{A\}	P_3\{B\}
3	D_4	D_2	D_0							P_2\{A\}	P_2\{C\}	P_2\{E\}
2	D_3	D_1	OL_0\{B\}	OL_0\{E\}	OL_1\{B\}	OL_1\{E\}	P_0\{B\}	P_0\{D\}	P_1\{A\}	P_1\{D\}	P_1\{E\}	P_2\{D\}
1	OL_0\{A\}	OL_0\{C\}	OL_0\{D\}	OL_1\{A\}	OL_1\{C\}	OL_1\{D\}	P_0\{A\}	P_0\{C\}	P_0\{E\}	P_1\{B\}	P_1\{C\}	P_2\{B\}

CONSULT FACTORY
FOR PACKAGE INFO

△ ALIGNMENT MARK

PGA
TOP VIEW

GENERAL INFORMATION:

The IDT75C458 triple 8-bit PaletteDAC is a highly integrated building block which interfaces a relatively low bandwidth frame buffer memory to an analog RS-343A, high bandwidth output. To decrease the frame buffer memory requirements, the IDT75C458 has a color lookup table (dual-port RAM) included on-chip.The basic functional blocks are the microprocessor bus interface, the frame buffer memory interface and multiplexer, a dual-port RAM with one R/W port and one high-speed R/O port and three 8-bit video speed DACs.

MICROPROCESSOR BUS INTERFACE

The IDT75C458 supports a standard microprocessor bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and overlay registers allow color updating without contention with the display refresh process.

The bus interface consists of eight bidirectional data pins, D_0 - D_7, with two control inputs, C0 and C1, a read/write direction input, R/$\overline{\text{W}}$, and a clock input, $\overline{\text{CE}}$. All data and control information are latched on the falling edge of $\overline{\text{CE}}$, as shown in Figure 1. All accesses to the chip are controlled by the data in the address register combined with the control inputs C0, C1 and R/$\overline{\text{W}}$, depicted in the Truth Table (Table 1).

An access to a control register requires writing a 4 through 7 into the address register (C0 = C1 = 0) and then writing or reading data to the selected register (C0 = 0, C1 = 1). When accessing the control registers, the address register is not changed, facilitating read-modify-write operations. If an invalid address is loaded into the address register, data written is ignored or invalid data is read out.

It is also possible to access the color palette information. The palette is organized as 256 addresses with 8 bits of red, blue and green information. Additionally, there are four extra addresses assigned to overlay information, yielding a total memory size of 260 x 24.

Access to the palette entries is, again, through the address register. The desired palette address is loaded into the address register, C0 and C1 are modified to point to the color palette or overlay and the information is read or written. In this case, however, an internal counter is used to access the red, green or blue color information. The first color palette or overlay access reads or writes red. The next access is for green, while the third access is for blue. After the third access, the address register is incremented, allowing the reading or writing of the red information of the next palette address. When writing, red and green information is temporarily stored in registers and, during the blue cycle, all 24 bits are written.

The internal counter is reset by an access to the address or any of the control registers. After setting the address register, it is possible to read or write the entire palette without accessing the address register again. Some care is needed; only continuous reads or writes are allowed and it is not possible to switch between the color palette and overlay.

The color palette RAM and overlay registers are dual-ported which allows simultaneous access from the MPU port (D_0 - D_7) and the pixel port (P_0 - P_7 {A-E}). If the pixel port is reading the same palette entry as the MPU is writing, it is possible that the DAC output may be invalid. It is recommended that the palette and overlay entries be updated during the blanking time.

ADDRESS REGISTER DATA	C1	C0	ACCESS
X	0	0	Address Register
\$00-\$FF	0	1	Color Palette
\$00	1	1	Overlay Color 0
\$01	1	1	Overlay Color 1
\$02	1	1	Overlay Color 2
\$03	1	1	Overlay Color 3
\$04	1	0	Read Mask Register
\$05	1	0	Blink Mask Register
\$06	1	0	Command Register
\$07	1	0	Test Register

NOTE:
Control input C0 = 1 enables the internal counter which accesses the red, green and blue colors individually and increments the address counter after the blue access. C0 = 0 disables auto-increment of the address register allowing read-modify-write operations.

Table 1. Truth Table for MPU Operations

FRAME BUFFER INTERFACE

The frame buffer interface consists of five 8-bit input ports which correspond to five consecutive pixels. In addition, there are two extra bits per port which may be used for overlay information. To reduce the bandwidth requirements for the pixel data, the IDT75C458 latches 4 or 5 pixels (the multiplex factor is programmable to 4 or 5 by bit 7 of the command register) on each rising edge of $\overline{LD}$. The color and overlay information is internally multiplexed at the pixel clock frequency, CLK, and sequentially output. This arrangement allows pixel data to be transferred at a rate 4 or 5 times slower than the pixel clock. Typically, $\overline{LD}$ is the pixel clock divided by 4 or 5 and is used to clock data out of the frame buffer memory.

As shown in Figure 2, sync, blank, color and overlay information are latched on the rising edge of $\overline{LD}$. Up to 40 bits of color information are input through P_0 - P_7 {A-E} and up to 10 bits of overlay information are input through OL_0 - OL_1 {A-E}. Both sync and blank have separate inputs, $\overline{SYNC}$ and $\overline{BLANK}$, respectively. The IDT75C458 outputs color information on each clock cycle. Four or five pixels are output sequentially, beginning with the {A} information, then the {B} information, until the cycle is completed with the {D} or {E} information. In this configuration, sync and blank times are limited to multiples of four or five clock cycles.

The multiplexing factor, 4:1 or 5:1, is programmable from the command register, bit 7. In the 4:1 mode, the {E} color and overlay inputs are not used and the $\overline{LD}$ clock should be CLOCK divided by 4. The {E} color and overlay inputs must be connected to a valid logic level.

The overlay inputs (OL_0 - OL_1) have the same timing as the pixel inputs (P_0 - P_7). It is possible to use additional bit planes or external logic to control the overlay selection for cursor generation.

INTERNAL MULTIPLEXING

$\overline{LD}$ is typically CLK divided by four or five and it latches color and overlay information on every rising edge, independent of CLK. A digital PLL allows $\overline{LD}$ to be phase independent of CLK. The only restriction is that only one rising edge of $\overline{LD}$ is allowed to occur per four (4:1 multiplexing) or five (5:1 multiplexing) CLK cycles.

Color Palette

On the rising edge of each CLK cycle, eight bits of color information (P_0 - P_7) and two bits of overlay information (OL_0 - OL_1) for each pixel are processed by the read mask, blink mask and command registers. This information provides the address to the dual-port color palette RAM. Note that P_0 is the LSB when addressing the color palette RAM. The value stored at a selected address determines the displayed color. In this way, 8 bits of information can select from a palette of over 16 million with 256 simultaneous displayed colors (plus 3 overlay colors). Through the use of the control register, individual bit planes may be enabled or disabled for display and/or blinked at one of four blink rates and duty cycles.

The blink timing is based on vertical retrace intervals which are defined by at least 256 $\overline{LD}$ cycles since the last falling edge of $\overline{BLANK}$. The color changes during this normally blanked time.

The processed pixel data is then used to select which color palette entry or overlay register is used to provide color information. Table 2 illustrates the truth table used for color selection.

CR6	OL_1	OL_0	P_7 - P_0	PALETTE ENTRY
1	0	0	\$00	Color palette entry \$00
1	0	0	\$01	Color palette entry \$01
		.		.
		.		.
		.		.
1	0	0	\$FF	Color palette entry \$FF
0	0	0	\$xx	Overlay color 0
x	0	1	\$xx	Overlay color 1
x	1	0	\$xx	Overlay color 2
x	1	1	\$xx	Overlay color 3

NOTE:
CR6 is bit 6 of the Command Register.

Table 2. Palette and Overlay Select

11

Video Generation, DACs

On every CLK cycle, the selected 24 bits of color information (8 bits each of red, green and blue) from the Color Palette RAM are presented to the three 8-bit D/A converters. The IDT75C458 uses a 5 x 3 segmented approach where the four MSBs of the input data are decoded into a parallel "Thermometer" code which produces thirty two "course" output levels. The remaining three LSBs of input data drive eight binary weighted current switches with a total contribution of one-thirty second of full scale. The MSB and LSB currents are summed at the output to produce 256 levels.

The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs are pipelined to maintained synchronization with the pixel data. Both inputs drive appropriately weighted current switches which are summed at the output of the DACs to produce the specific output levels required by RS-343, as shown in Figure 3. Note that the sync information is only available at the IO_G (green) output and that the input data to the DAC sums with the sync current. Table 3 details the output levels associated with $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and data.

Monitor Interface

The analog outputs of the IDT75C458 are high-impedance current sources which are capable of directly driving a doubly terminated 75Ω coaxial cable to standard video levels. A typical output circuit is shown in Figure 3.

Description	S	B	DAC data	IO_G (mA)	IO_R, IO_B (mA)
WHITE	1	1	$FF	26.67	19.05
DATA	1	1	data	data+9.05	data+1.44
DATA & SYNC	0	1	data	data+1.44	data+1.44
BLACK	1	1	$0	9.05	1.44
BLACK & SYNC	0	1	$0	1.44	1.44
BLANK	1	0	X	7.62	0
SYNC	0	0	X	0	0

NOTE:

Typical values with full scale IOG = 26.67mA. RSET = 523Ω, VREF = 1.235V. S is $\overline{\text{SYNC}}$, B is $\overline{\text{BLANK}}$.

Table 3. Video Output Truth Table

IO_R, IO_B mA	IO_R, IO_B V	IO_G mA	IO_G V
19.05	0.714	26.67	1.000
•	•	•	•
•	•	•	•
•	•	•	•
1.44	9.954	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

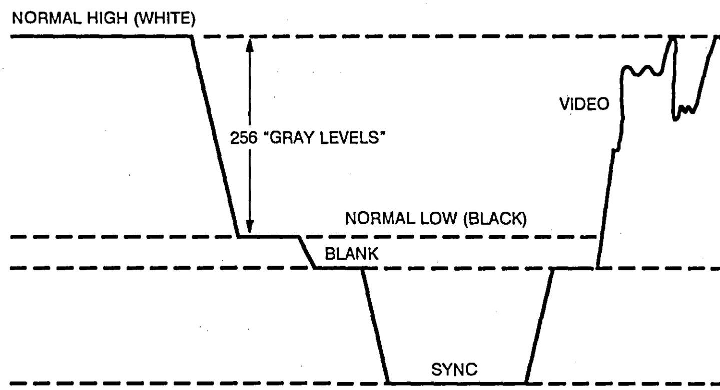


Figure 1. Composite Video Output Waveform

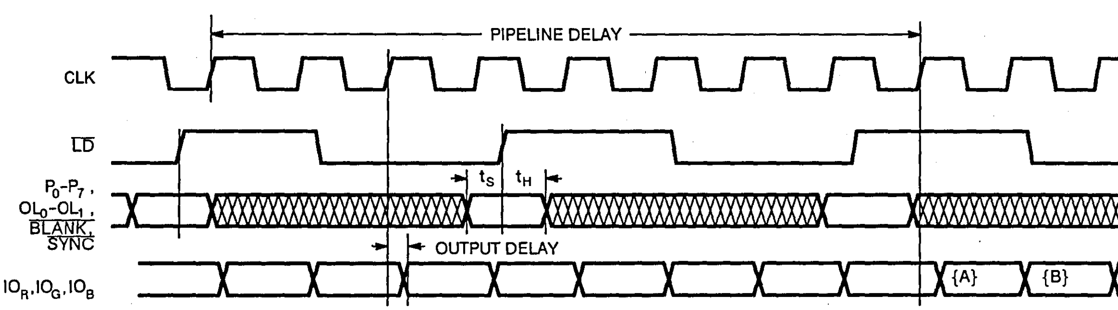


Figure 2. Pixel Timing

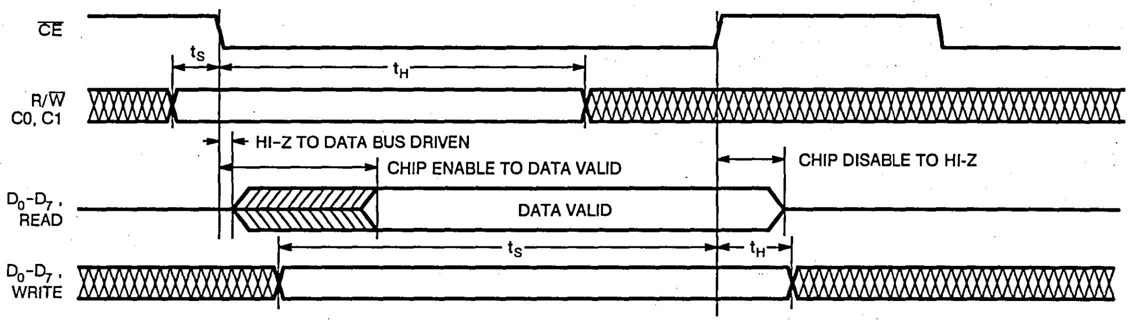


Figure 3. Data Bus Timing

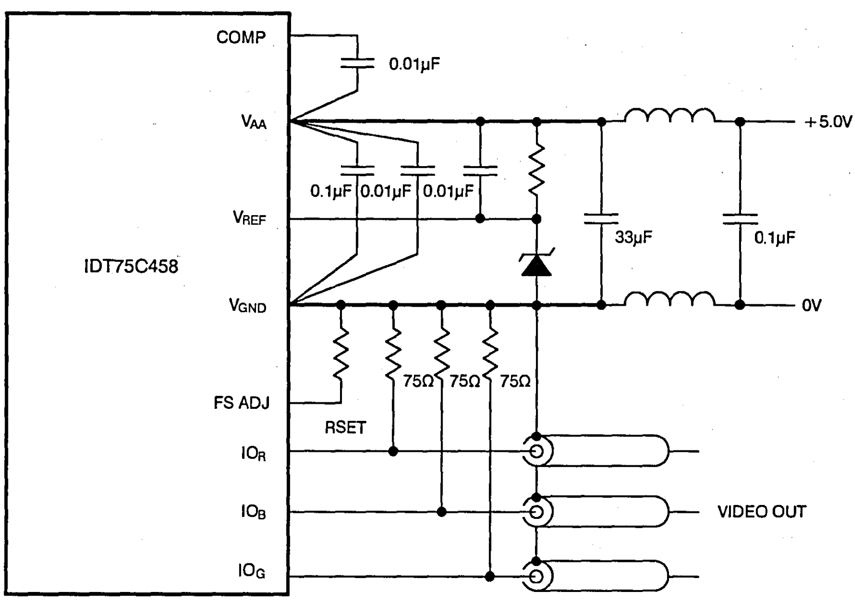


Figure 4. Typical Application

PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
DATA BUS	
D_0 - D_7	8-bit, bidirectional data bus. Data is input and output over this bus and the flow is controlled by R/$\overline{W}$ and $\overline{CE}$. D_7 is the most significant bit.
$\overline{CE}$	Chip Enable input. The chip is enabled when this control pin is LOW. During a write cycle (R/$\overline{W}$ LOW), the data present on D_0 - D_7 is internally latched on the LOW-to-HIGH transition of this pin.
R/$\overline{W}$	Read/Write Control input. The Read/Write input is latched on the HIGH-to-LOW transition of $\overline{CE}$ and determines the direction of the bidirectional data bus D_0 - D_7. If R/$\overline{W}$ is HIGH during the falling edge of $\overline{CE}$, a read cycle occurs. If R/$\overline{W}$ is LOW during the falling edge of $\overline{CE}$, a write cycle occurs and, additionally, D_0 - D_7 are latched on the rising edge of $\overline{CE}$.
C0, C1	Register Control inputs. C0 and C1 determine which register or palette entry is accessed during a read or write cycle. These inputs are latched on the HIGH-to-LOW transition of $\overline{CE}$.
PIXEL	
CLK, $\overline{CLK}$	Pixel Clock inputs. These inputs are differential and may be driven by ECL operating from a +5V supply. The clock frequency is normally the system pixel clock rate.
$\overline{LD}$	Load Clock input. The Load Clock is normally CLK divided by 4 or 5 (determined by the Control Register, bit 7). The pixel data, P_0 - P_7 {A-E} and OL_0 - OL_1 {A-E}, $\overline{BLANK}$ and $\overline{SYNC}$ are internally latched on the LOW-to-HIGH transition of $\overline{LD}$.
P_0 - P_7 {A-E}	Pixel Input Data. These inputs provide the address input to the color palette RAM. The data stored at a particular address is the color output by the DAC. Four or five consecutive pixels, as determined by bit 7 in the Command Register, are internally latched on the LOW-to-HIGH transition of $\overline{LD}$. The pixels are output sequentially, first {A} then {B}. After all four or five pixels have been output, the cycle repeats. Unused inputs must be connected to a valid logic level.
OL_0 - OL_1 {A-E}	Pixel Overlay Inputs. The Overlay inputs have the same timing as P_0 - P_7 and select between either the color palette or the overlay palette. When the overlay palette is selected, the pixel information P_0 - P_7 {A-E} is ignored. Bit 6 of the command register determines if Overlay = 0 displays overlay color 0 or the color palette entry. See Table 2 for details.
$\overline{BLANK}$	Composite Blank Input. A LOW on this input forces the analog outputs (IO_R, IO_G, IO_B) to the blanking level. The $\overline{BLANK}$ input is internally latched on the LOW-to-HIGH transition of $\overline{LD}$. This input overrides all other pixel information.
$\overline{SYNC}$	Composite Sync Input. A LOW on this input subtracts approximately 7mA from the IO_G analog output and overrides no other pixel information. For the correct SYNC level, this input should be LOW only when $\overline{BLANK}$ is also LOW. The $\overline{SYNC}$ input is internally latched on the LOW-to-HIGH transition of $\overline{LD}$.
ANALOG	
A_{GND}	Analog Ground Power Supply, 0V.
V_{AA}	Analog Power Supply, 5V.
V_{REF}	Voltage Reference Input, 1.235V. This input supplies a reference voltage for the DAC circuitry. Care must be taken to correctly decouple this voltage because noise on this pin will couple directly to the DAC outputs.
FS AD	Full-Scale Adjust Input. The current flowing from this pin to A_{GND} is directly proportional to the full-scale analog output current. Normally, a resistor is connected between this pin and A_{GND}. The voltage on this pin is approximately equal to V_{REF}. The relationship between the full-scale output current and RSET is: IO_G (mA) = 11.294 x V_{REF} (V)/RSET (KΩ) IO_R, IO_B (mA) = 8.067 x V_{REF} (V)/RSET (KΩ)
IO_G, IO_R, IO_B	Green, Red and Blue DAC current outputs.
COMP	Compensation Input. This pin provides the ability to compensate the internal reference operational amplifier.

INTERNAL REGISTERS

Command Register

The Command Register is accessed by reading or writing with the Address Register = \$06, C0 = 0 and C1 = 1 (see Table 1). It provides control over multiplexing and blink rate selection. The Command Register may be read or written at any time. CR7 (Command Register bit 7) corresponds to D7 (Data Bus bit 7).

CR0	OL_0 display enable. This bit is ANDed internally with the data from OL_0 prior to the palette selection. If CR0 is LOW, the internal OL_0 bits are set LOW allowing only overlay colors 0 and 2 to be selected.
CR1	OL_1 display enable. This bit is ANDed internally with the data from OL_1 prior to the palette selection. If CR1 is LOW, the internal OL_1 bits are set LOW allowing only overlay colors 0 and 1 to be selected.
CR2	OL_0 blink enable. If this bit is set HIGH, the OL_0 bit is internally switched between the value input and 0 at the rate specified by the CR4 and CR5 bits. CR0 must be set HIGH for this function.
CR3	OL_1 blink enable. If this bit is set HIGH, the OL_1 bit is internally switched between the value input and 0 at the rate specified by the CR4 and CR5 bits. CR1 must be set HIGH for this function.
CR4, CR5	Blink Rate Select. These bits select blink rates based on Vertical Sync cycles, defined as more than 256 $\overline{LD}$ cycles during BLANK.
CR6	Color Palette RAM enable. This bit specifies whether to use the Color Palette or the Overlay Palette when $OL_0 = OL_1$ = LOW.
CR7	Multiplex Select. This bit selects between 4:1 (CR7 = 0) or 5:1 (CR7 = 1) multiplexing. When using 4:1 multiplexing, the {E} inputs are never used and must be connected to a valid logic level.

Read Mask Register

The Read Mask Register is accessed by reading or writing with the Address Register = \$04, C0 = 0 and C1 = 1 (see Table 1). It internally ANDs the pixel information with a bit from the register before the color palette selection, effectively enabling (HIGH) or disabling (LOW) the entire pixel plane. The Read Mask Register may be read or written at any time. RMR7 (Read Mask Register bit 7) corresponds to D7 (Data Bus bit 7).

Blink Mask Register

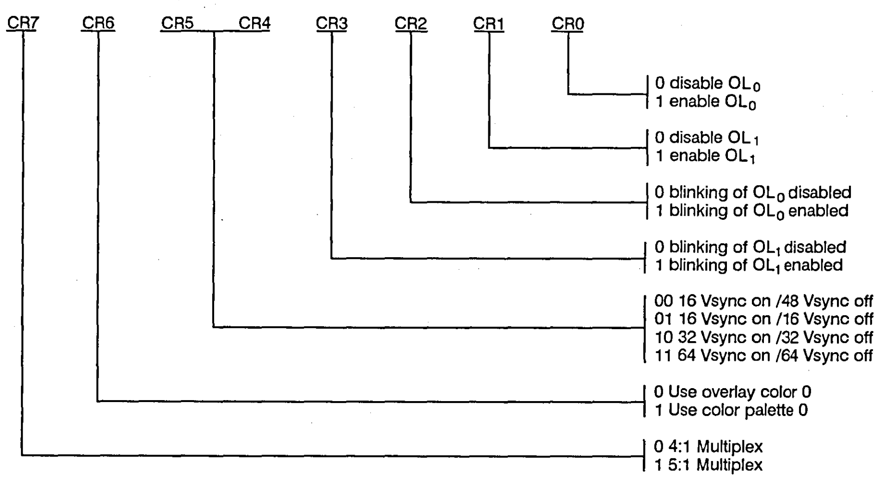
The Blink Mask Register is accessed by reading or writing with the Address Register = \$05, C0 = 0 and C1 = 1 (see Table 1). Each register bit causes the corresponding pixel bit (P_0 - P_7) to internally switch between the input value and 0 at the blink rate specified in the Command Register. For this function to work, the corresponding enable bit in the Read Mask Register must be set HIGH. The Blink Mask Register may be read or written at any time. BMR7 (Blink Mask Register bit 7) corresponds to D_7 (Data Bus bit 7).

Test Register

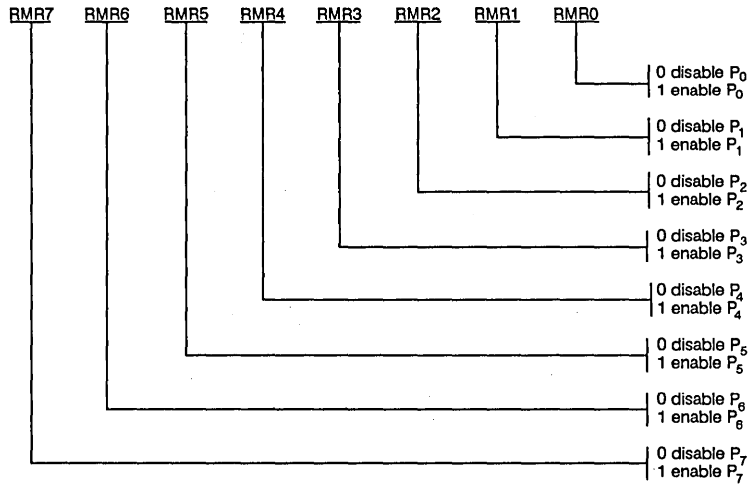
The Test Register is accessed by reading or writing with the Address Register = \$07, C0 = 0 and C1 = 1 (see Table 1). This register allows the MPU to read the 24 input bits of the DACs. The register bits are defined below.

TR7-TR4	Read data (one nibble of red, blue or green)
TR3	Upper (LOW) or Lower (HIGH) nibble select
TR2	Blue enable
TR1	Green enable
TR0	Red enable

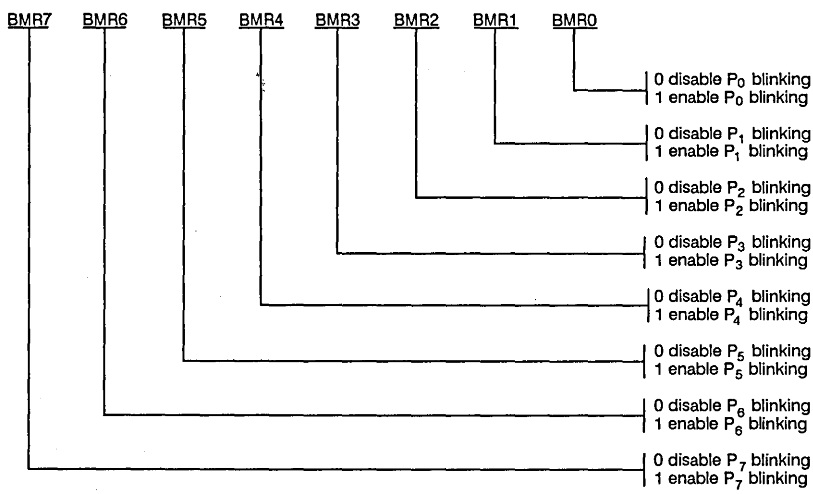
The desired DAC is selected by setting only one color enable bit (D_0 - D_2) HIGH and the upper or lower nibble is selected with D_3. After this write operation, a subsequent read yields the DAC data on D_7 - D_4 and the previously written enable data on D_0 - D_3. For a correct read, pixel and overlay data must remain constant for the entire MPU read cycle. When $\overline{BLANK}$ is asserted, the Test Register information D_7 - D_4 will be forced to zero. TR7 (Test Register bit 7) corresponds to D_7 (Data Bus bit 7).



COMMAND REGISTER DESIGNATIONS



READ MASK REGISTER DESIGNATIONS



BLINK MASK REGISTER DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
POWER SUPPLIES			
V_{AA}	Measured to A_{GND}	-0.5 to +7.0	V
INPUT VOLTAGE			
Applied Voltage (2)	Measured to A_{GND}	-0.5V to V_{AA}+05	V
OUTPUT			
Applied Voltage (2)	Measured to A_{GND}	-0.5V to V_{AA}+05	V
Applied Current (2,3,4)	Externally forced	-1.0 to +6.0	mA
Short Circuit Duration	Single output High to A_{GND}	1.0	S
TEMPERATURE			
Operating, Ambient	Military	-55 to +125	°C
	Commercial	0 to +70	°C
Storage	Military	-65 to +150	°C
	Commercial	-55 to +125	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{AA}	Power Supply	Measured to V_{GND}	4.75	5.0	5.25	V
I_{AA}	Power Supply Current	V_{AA} = Typ.	–	200	–	mA
V_{IH}(1)	Input Voltage HIGH		2.0	–	V_{AA} +0.5	V
V_{IL}(1)	Input Voltage LOW		A_{GND} -0.5	–	0.8	V
V_{CIH}	Clock Input Voltage HIGH		V_{AA} -1.0	–	V_{AA} +0.5	V
V_{CIL}	Clock Input Voltage LOW		A_{GND} -0.5	–	V_{AA} -1.6	V
I_{IH}	Input Current HIGH	V_{IN} = 2.4V	–	–	1	μA
I_{IL}	Input Current LOW	V_{IN} = 0.8V	–	–	1	μA
V_{OH}	Output Voltage HIGH	V_{AA} = Min., I_{OH} = −800μA	2.4	–	–	V
V_{OL}	Output Voltage LOW	V_{AA} = Min., I_{OL} = 6.4mA	–	–	0.4	V
I_{OZ}	Output 3-State Current		–	–	10	μA

NOTE:
1. All digital inputs except CLK and $\overline{CLK}$.

AC ELECTRICAL CHARACTERISTICS

Following conditions apply unless otherwise specified:
T_A = 0°C to +70°C (Commercial Temperature Range)
T_A = -55°C to +125°C (Military Temperature Range)
V_{AA} = 5.0V ±5%
TTL Inputs, V_{IL} = 0.8V, V_{IH} = 2.0V, rise/fall time <5ns
CLK Inputs, V_{IH} = V_{AA} -1.0V, V_{IL} = V_{AA} -1.6V, rise/fall time <2ns
Timing reference points at 50% of signal swing

		IDT75C458-125			IDT75C458-110			IDT75C458-80			
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
F_{CLK}	Clock Frequency	–	–	125	–	–	110	–	–	80	MHz
F_{LD}	$\overline{LD}$ Clock Frequency	–	–	32	–	–	28	–	–	20	MHz
t_{MPUCY}	MPU Cycle Time	100	–	–	110	–	–	125	–	–	ns
t_{CS}	Control Set-up Time	0	–	–	0	–	–	0	–	–	ns
t_{CH}	Control Hold Time	15	–	–	15	–	–	15	–	–	ns
t_{CEH}	$\overline{CE}$ HIGH Time	25	–	–	25	–	–	25	–	–	ns
t_{CEZO}	$\overline{CE}$ to Data Bus Driven	10	–	–	10	–	–	10	–	–	ns
t_{CED}	$\overline{CE}$ to Data Valid	–	–	75	–	–	75	–	–	100	ns
t_{CEOZ}	$\overline{CE}$ to Data Bus HI-Z	–	–	15	–	–	15	–	–	15	ns
t_{WDS}	Write Data Set-up Time	35	–	–	40	–	–	50	–	–	ns
t_{WDH}	Write Data Hold Time	0	–	–	0	–	–	0	–	–	ns
t_{CLKCY}	Clock Cycle Time	8	–	–	9	–	–	12	–	–	ns
t_{CLKPL}	Clock Pulse Width LOW	3.2	–	–	4	–	–	5	–	–	ns
t_{CLKPH}	Clock Pulse Width HIGH	3.2	–	–	4	–	–	5	–	–	ns
t_{CLKT}	Clock Transition Time	–	–	1.6	–	–	1.6	–	–	2.0	ns
t_{LDCY}	$\overline{LD}$ Cycle Time	32	–	–	36	–	–	50	–	–	ns
t_{LDPH}	$\overline{LD}$ Pulse Width HIGH	13	–	–	15	–	–	20	–	–	ns
t_{LDPL}	$\overline{LD}$ Pulse Width LOW	13	–	–	15	–	–	20	–	–	ns
t_{PS}	Pixel Data Set-up Time	3	–	–	4	–	–	4	–	–	ns
t_{PH}	Pixel Data Hold Time	2	–	–	2	–	–	2	–	–	ns

ANALOG OUTPUT DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Res	Resolution		–	8	–	bits
I_{LSB}	LSB Current Size		–	69.1	–	μA
L_I	Integral Linearity		–	1/2	±1	LSB
L_D	Differential Linearity		–	1/2	±1	LSB
I_O	Offset Error		–	10	50	μA
V_{CC}	Output Compliance Voltage		-1.0	–	1.2	V
E_M	Matching Error (DAC to DAC)		–	2	5	%
PSRR	Power Supply Rejection Ratio		–	50	–	dB
I_W (1)	White Current	Measured to BLANK	17.69	19.05	20.40	mA
I_W (1)	White Current	Measured to BLACK	16.74	17.62	18.50	mA
I_B (1)	Black Current	Measured to BLANK	0.95	1.44	1.90	mA
I_{BLANK}	Blank Current IO_R, IO_B		–	0	–	mA
I_{BLANK} (1)	Blank Current IO_G		6.29	7.62	8.96	mA
I_{SYNC}	Sync Current IO_G		–	0	–	mA

NOTE:
1. $R_{SET} = 523\Omega$, $V_{REF} = 1.235V$

ANALOG OUTPUT AC ELECTRICAL CHARACTERISTICS

Following conditions apply unless otherwise specified:
$T_A = 0°C$ to $+70°C$ (Commercial Temperature Range)
$T_A = -55°C$ to $+125°C$ (Military Temperature Range)
$V_{AA} = 5.0V \pm 5\%$
TTL Inputs, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$, rise/fall time $< 5ns$
CLK Inputs, $V_{IH} = V_{AA} - 1.0V$, $V_{IL} = V_{AA} - 1.6V$, rise/fall time $< 2ns$
Timing reference points at 50% of signal swing

		IDT75C458-125			IDT75C458-110			IDT75C458-80			
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
F_{CLK}	Clock Frequency	–	–	125	–	–	110	–	–	80	MHz
t_{VD}	Video Output Delay Time	–	5	–	–	5	–	–	5	–	ns
t_{VT}	Video Output Transition Time	–	2	–	–	2	–	–	2	–	ns
t_S	Video Output Skew (1)	–	0	2	–	0	2	–	0	2	ns
t_{SI}	Video Output Settling Time	–	8	–	–	10	–	–	12	–	ns
FT	Clock and Data Feedthrough	–	50	–	–	50	–	–	50	–	pV-s
G_E	Glitch Energy	–	50	–	–	50	–	–	50	–	pV-s
CT	Crosstalk, DAC to DAC	–	100	–	–	100	–	–	100	–	pV-s
t_{VP}	Pipeline Delay	8	–	8	8	–	8	8	–	8	clock

NOTE:
1. $C_L = 10pF$, 10%-90% points

11

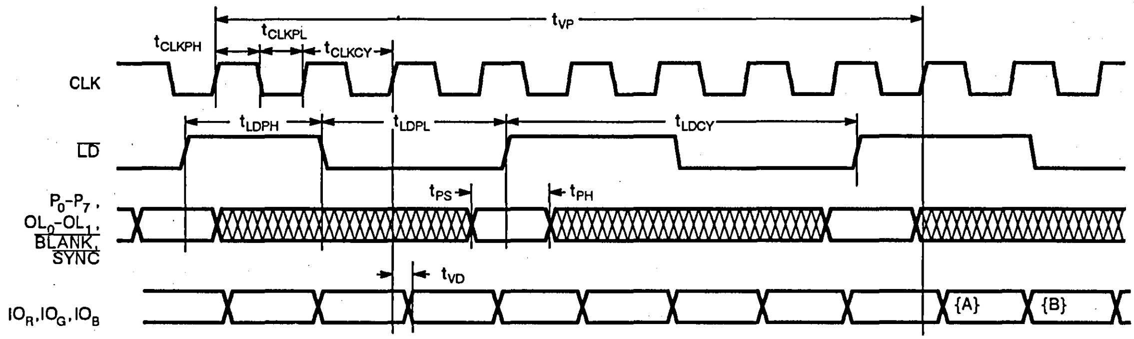


Figure 5. Video I/O Timing Diagram

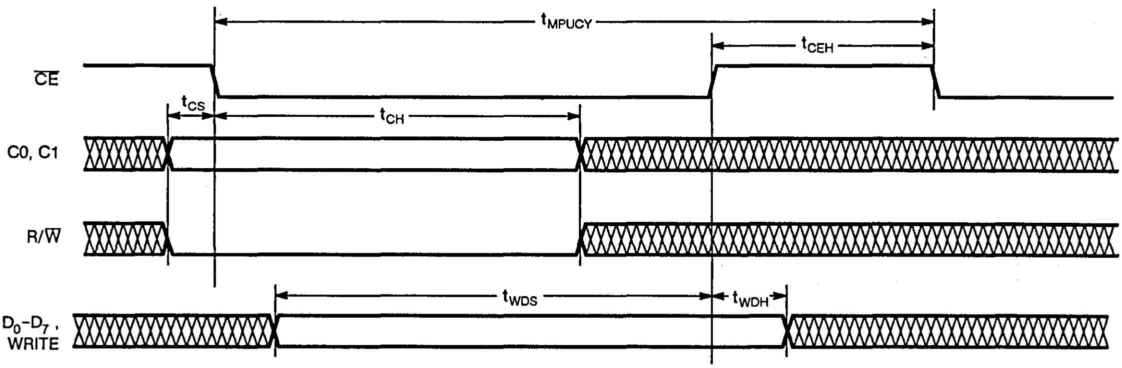


Figure 6. MPU WRITE Timing Diagram

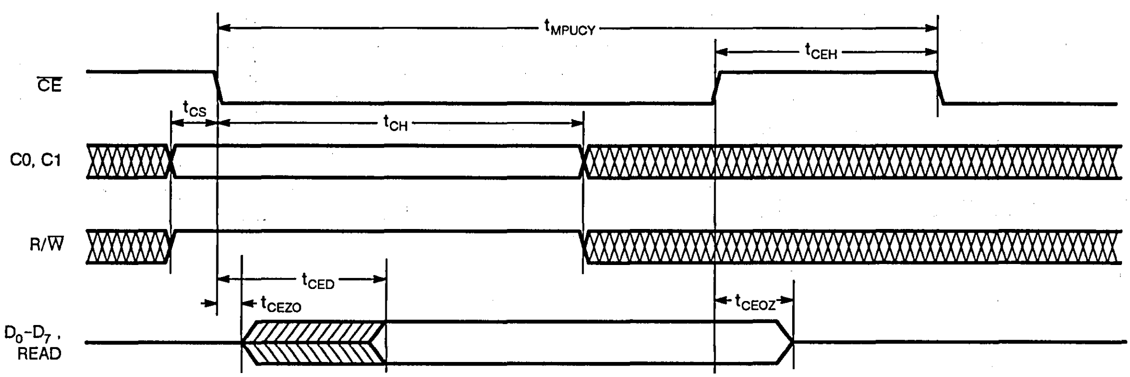


Figure 7. MPU READ Timing Diagram

ORDERING INFORMATION

IDT XXXX (Device Type) X (Power) X (Speed) X (Package) X (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	BLANK	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	G	Pin Grid Array
Speed	80 110 125	Speed in Megahertz
Power	S	Standard Power
Device Type	75C458	Triple 8-bit PaletteDAC™

11

Integrated Device Technology, Inc.

CMOS FLASH A/D CONVERTER

IDT75C48

FEATURES:

- 8-bit resolution
- 20 MSPS conversion rate
- Pin- and function-compatible with TRW 1048
- Low power consumption: 500mW
- Extended analog input range
- On-chip EDC (Error Detection and Correction)
- Improved output logic HIGH drive, no pull-up needed
- No sample and hold required
- Differential Phase < 1 Degree
- Differential Gain < 2%
- 1/2 LSB linearity
- Selectable output formats
- TTL-compatible
- Available in 28-pin Plastic DIP, CERDIP and LCC
- Military product is compliant to MIL-STD-883, Class B

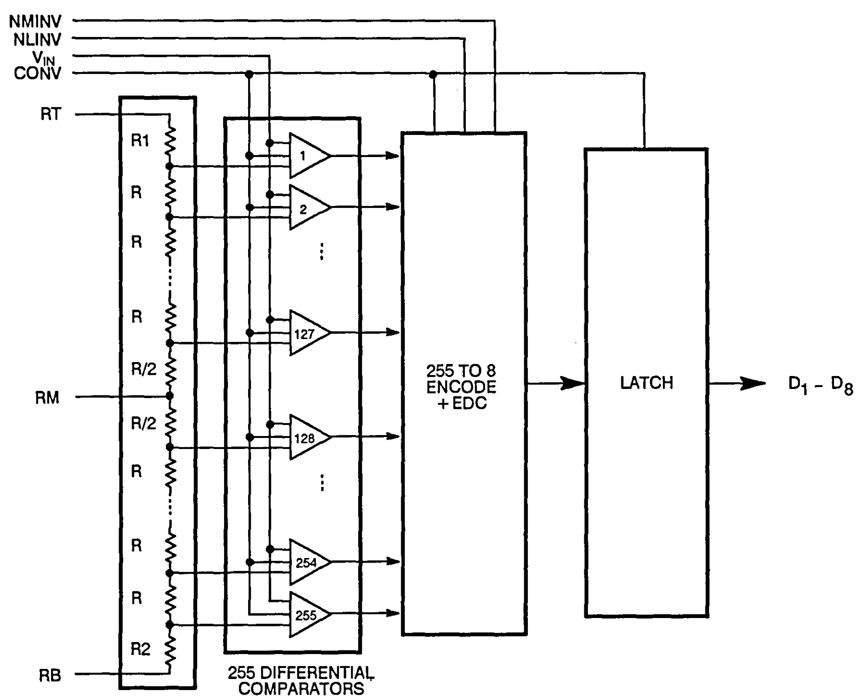
DESCRIPTION:

The IDT75C48 is a 20 MegaSample per Second (MSPS), fully parallel, 8-bit Flash Analog to Digital Converter. The wide input analog bandwidth of 7MHz permits the conversion of analog input signals with full-power frequency components up to this limit with no input sample and hold. Low power consumption, due to CEMOS™ processing, virtually eliminates thermal considerations. The IDT75C48 is available in 28-pin plastic and hermetic DIPs and a 28-pin LCC.

The IDT75C48 consists of a reference voltage generator, 255 comparators, encoding and EDC (Error Detection and Correction) logic and an output data register. A single clock starts the conversion process and controls all internal operations. Two control inputs allow the output coding format to be programmed for straight binary or offset two's complement in either the true or inverted form.

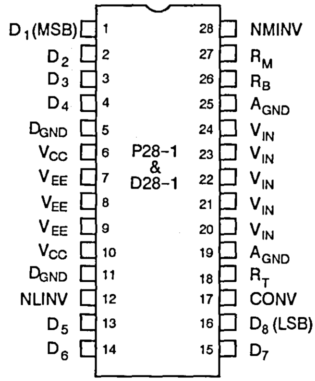
The IDT75C48 military Flash A/D Converters are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

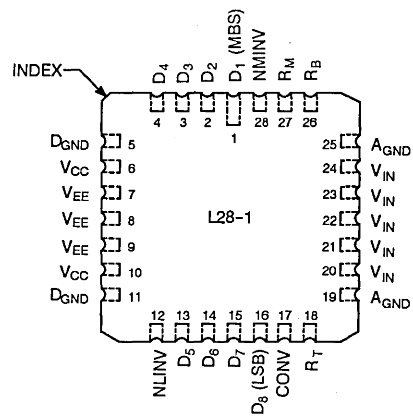


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

GENERAL INFORMATION

The IDT75C48 has four functional sections: a comparator array, a reference voltage generator, encoding logic with EDC and output logic. The comparator array compares the input signal with 255 reference voltages to produce an N - of - 255 code. This is sometimes called a "Thermometer" code because all of the comparators with their reference voltage less than the input signal will be "on," while those with their reference above the input will be "off."

The reference voltage generator consists of a string of precisely matched resistors which generate the 255 voltages needed by the comparators. The voltages at the ends of the resistor string set the maximum and minimum conversion range and are typically 0V and -2V, respectively.

The encoding logic converts the "Thermometer" code into binary or offset two's complement numbers and can invert either code. Included in the encoding function is Error Detection and Correction logic which ensures that a corrupted Thermometer code is correctly encoded.

The output logic latches and holds the data constant between samples. The output timing is designed for an easy interface to external latches or memories using the same clock as the ADC.

POWER

The IDT75C48 requires two power supply voltages, V_{CC} and V_{EE}. Typically, V_{EE} = -5.2V and V_{CC} = +5.0V. Two separate grounds are provided, A_{GND} and D_{GND}, the analog and digital grounds. The difference between A_{GND} and D_{GND} must not exceed ±0.1V and all power and ground pins must be connected.

REFERENCE

The IDT75C48 converts analog input signals that are within the range of the reference ($V_{RB} \leq V_{IN} \leq V_{RT}$) into digital form. V_{RB} (Reference Bottom) and V_{RT} (Reference Top) are applied across the reference resistor chain and both must be within the range of +0.1V to -2.1V. In addition, the voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 1.8V and 2.2V, with V_{RT} more positive than V_{RB}. Nominally, V_{RT} = 0.0V and V_{RB} = -2.0V.

The IDT75C48 provides a midpoint tap, RM, which allows the converter to be adjusted for optimum linearity or a non-linear transfer function. Adjustment of RM is not necessary to meet the linearity specification. Figure 5 shows a circuit which will provide approximately 1/2 LSB adjustment of the midpoint. The characteristic impedance of RM is about 170Ω and this node should be driven from a low impedance source. Any noise introduced at this point will couple directly into the resistor chain, seriously affecting performance.

Due to the unavoidable coupling with the clock and the input signal, RT and RB should provide low AC impedance to ground. For applications with a fixed reference, a bypass capacitor is recommended.

CONTROL

The IDT75C48 provides two function control pins, NMINV and NLINV. These controls are for steady state use and are usually tied to the appropriate voltages. They control the output coding format in either straight binary or offset two's complement. In addition, both formats may be either true or inverted. These pins are active low and perform the functions as shown in Figure 1.

CONVERT

The IDT75C48 begins a conversion with every rising edge of the convert signal, CONV. The analog input signal is sampled on the rising edge of CONV, while the outputs of the comparators are encoded on the falling edge. The next rising edge latches the encoder output which is presented on the output pins.

The input sample is taken within 15ns of the rising edge of CONV and is called t_{STO} or the Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature, but the short term uncertainty or jitter is less than 60ps.

If the maximum CONV pulse width HIGH time (t_{PWH}) is exceeded, the accuracy of the input sample may be impaired. The maximum CONV pulse width LOW time (t_{PWL}) may be exceeded, but the digital output data for the sample taken by the previous rising edge of CONV will be meaningless. It is recommended that CONV be held LOW during longer periods of inactivity,

The digital output data is presented at t_D, the Digital Output Delay Time, after the next rising edge of CONV. Previous output data is held for the t_{HO} (Output Hold Time) after the rising edge of CONV to allow for non-critical timing in the external circuitry. This means that the data for sample N is acquired while the converter is taking sample N+2.

ANALOG INPUT

The IDT75C48 uses strobed, auto-zeroing, latching comparators. For optimum performance, the source impedance of the analog driver must be less than 25Ω. All five analog input pins must be connected together as close to the package as possible.

If the analog input signal is within the reference voltage range, the output will be a binary number between 0 and 255. An input signal above V_{RT} will yield a full-scale positive output while an input below V_{RB} will cause a full-scale negative output.

STEP	RANGE		BINARY		OFFSET TWO'S	
	-2.0000V FS -7.8431mV/STEP	-2.0480V FS -8.000mV/STEP	NMINV=1 NLINV=1	NMINV=0 NLINV=0	NMINV=0 NLINV=1	NMINV=1 NLINV=0
000	0.0000V	0.0000V	00000000	11111111	10000000	01111111
001	-0.0078V	-0.0080V	00000001	11111110	10000001	01111110
.	.	.	.	.	.	.
.	.	.	.	.	.	.
127	-0.9961V	-1.0160V	01111111	10000000	11111111	00000000
128	-1.0039V	-1.0240V	10000000	01111111	00000000	11111111
129	-1.0118V	-1.0320V	10000001	01111110	00000001	11111110
.	.	.	.	.	.	.
.	.	.	.	.	.	.
254	-1.9921V	-2.0320V	11111110	00000001	01111110	10000001
255	-2.0000V	-2.0400V	11111111	00000000	01111111	10000000

Figure 1. Output Coding

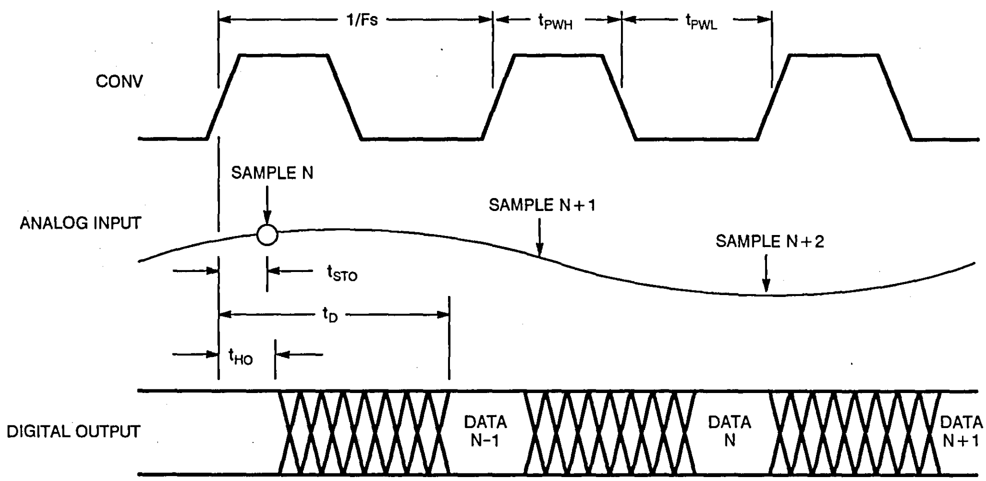


Figure 2. Timing Diagram

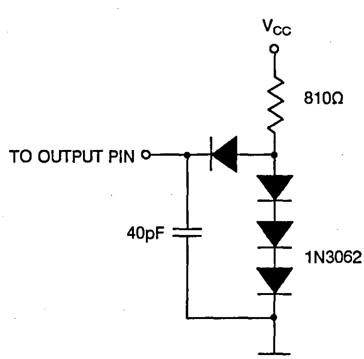


Figure 3. Output Load 1

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
POWER SUPPLY			
V_{CC}	Measured to D_{GND}	-0.5 to +7.0	V
V_{EE}	Measured to A_{GND}	+0.5 to -7.0	V
A_{GND}	Measured to D_{GND}	-0.5 to +0.5	V
INPUT VOLTAGE			
CONV, NMINV, NLINV	Measured to D_{GND}	-0.5 to V_{CC} +0.5	V
V_{IN} ,V_{RT},V_{RB}	Measured to A_{GND}	V_{CC} to V_{EE}	V
V_{RT}	Measured to VRB	-2.2 to +2.2	V
OUTPUT			
Applied Voltage [2]	Measured to D_{GND}	-0.5 to V_{CC} +0.5	V
Applied Current [2, 3, 4]	Externally forced	-3.0 to +6.0	mA
Short Circuit Duration	Single output High to D_{GND}	1.0	S
TEMPERATURE			
Operating, Ambient	Military	-55 to +125	°C
	Commercial	0 to +70	°C
Storage	Military	-65 to +150	°C
	Commercial	-55 to +125	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

AC ELECTRICAL CHARACTERISTICS

Specifications over the Recommended Operating Conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	TEMPERATURE RANGE COMMERCIAL MIN.	COMMERCIAL MAX.	MILITARY MIN.	MILITARY MAX.	UNIT
F_S	Max. Conversion Rate	V_{CC} = Min.,V_{EE} = Min.	20	–	20	–	MSPS
t_{STO}	Sampling Time Offset	V_{CC} = Min.,V_{EE} = Min.	0	10	0	15	ns
t_D	Digital Output Delay	V_{CC} = Min.,V_{EE} = Min., Load 1	–	30	–	35	ns
t_{HO}	Digital Output Hold Time	V_{CC} = Max.,V_{EE} = Max., Load 1	5	–	5	–	ns

DC ELECTRICAL CHARACTERISTICS

Specifications over the Recommended Operating Conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	TEMPERATURE RANGE COMMERCIAL MIN.	COMMERCIAL MAX.	MILITARY MIN.	MILITARY MAX.	UNIT
I_{CC}	Positive Supply Current	V_{CC} = Max., Static(1)		70		80	mA
I_{EE}	Negative Supply Current	V_{EE} = Max., Static(1)	–	-35	–	-35	mA
I_{REF}	Reference Current (R_T to R_B)	V_{RT}, V_{RB} = NOM	–	9		10	mA
R_{REF}	Reference Resistance (R_T to R_B)	V_{RT}, V_{RB} = NOM	250	–	220	–	Ohm
R_{IN}	Equiv. Input Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = VRB	100	–	100	–	KOhm
C_{IN}	Equiv. Input Capacitance	V_{RT}, V_{RB} = NOM, V_{IN} = VRB	–	50	–	50	pF
I_{CB}	Input Const. Bias Current	V_{EE} = Max.	–	10	–	10	µA
I_{IL}	Input Current Logic LOW	V_{CC} = Max., V_{IH} = 0.5V CONV, NMINV, NLINV	–	±25	–	±25	µA
I_{IH}	Input Current, Logic HIGH	V_{CC}=Max., V_{IL}= 2.4V	–	±25	–	±25	µA
I_I	Input Current, Max. Input Voltage	V_{CC} = Max., V_I = V_{CC}	–	50	–	50	µA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min., I_{OL} = 4.0mA	–	0.5	–	0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min., I_{OH} = -2.0mA	2.4		2.4	–	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max. (2)	–	-50	–	-50	mA
C_I	Digital Input Capacitance	T_A = +25°C, F = 1MHz	–	15	–	15	pF

NOTES:
1. Worst case, all digital inputs and outputs LOW.
2. Output HIGH one pin to ground, one second duration.

SYSTEM PERFORMANCE

Specifications over the Recommended Operating Conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	TEMPERATURE RANGE COMMERCIAL MIN.	COMMERCIAL MAX.	MILITARY MIN.	MILITARY MAX.	UNIT
E_{LI}	Linearity Error, Integral	V_{RT}, V_{RB} = NOM	–	0.2	–	0.2	%FS
E_{LD}	Linearity Error, Differential	V_{RT}, V_{RB} = NOM	–	0.2	–	0.2	%FS
C_S	Code Size		25	175	25	175	%NOM
E_{OT}	Offset Error, Top	V_{IN} = V_{RT}	–	45	–	45	mV
E_{OB}	Offset Error, Bottom	V_{IN} = V_{RB}	–	-30	–	-30	mV
T_{CO}	Offset Error, Temperature Coefficient	V_{IN} = V_{RB}	–	±20	–	±20	µV/°C
B_W	Bandwidth, Full Power Input		7	–	5	–	MHz
T_{TR}	Transient Response, Full Scale		–	20	–	20	ns
SNR	Signal to Noise Ratio	20MSPS Conversion Rate, 10MHz Bandwidth					
	Peak Signal /RMS Noise	1.248MHz Input 2.438MHz Input	54 53	– –	53 52	– –	dB
	RMS Signal/RMS Noise	1.248MHz Input 2.438MHz Input	45 44	– –	44 43	– –	dB
E_{AP}	Aperture Error		–	60	–	60	ps
DP	Differential Phase Error	F_S = 4xNTSC	–	1	–	1	Degree
DG	Differential Gain Error	F_S = 4xNTSC	–	2	–	2	%
NPR	Noise Power Ratio	DC to 8MHz White Noise Bandwidth 4 Sigma Loading 1.248 MHz Slot 20MSPS Conversion Rate	36.5	–	36.5	–	dB

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TEMPERATURE RANGE						UNIT
		COMMERCIAL			MILITARY			
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
V_{CC}	Positive Power Supply	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Power Supply	-4.9	-5.2	-5.5	-4.9	-5.2	-5.5	V
V_{AGND}	Analog Ground Voltage (ref D_{GND})	-0.1	0	+0.1	-0.1	0	+0.1	V
t_{PWL}	CONV, Pulse Width LOW	18	–	100,000	18	–	100,000	ns
t_{PWH}	CONV, Pulse Width HIGH	22	–	20,000	22	–	20,000	ns
V_{IL}	Input Voltage, Logic LOW	-0.5	–	0.8	-0.5	–	0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0	–	V_{CC}+0.1	2.0	–	V_{CC}+0.1	V
I_{OL}	Output Current, Logic LOW	–	–	4.0	–	–	4.0	mA
I_{OH}	Output Current, Logic HIGH	–	–	-2.0	–	–	-2.0	mA
V_{RT}	Most Positive Reference Voltage (1)	-0.1	0	+0.1	-0.1	0	+0.1	V
V_{RB}	Most Negative Reference Voltage (1)	-1.9	-2.0	-2.1	-1.9	-2.0	-2.1	V
$V_{RT}-V_{RB}$	Reference Voltage Range	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage Range	V_{RB}	–	V_{RT}	V_{RB}	–	V_{RT}	V
T_A	Ambient Temperature, Still Air	0	–	70	–	–	–	°C
T_C	Case Temperature	–	–	–	-55	–	+125	°C

NOTE:
1. V_{RT} must be more positive than V_{RB} and the voltage reference differential must be within the specified range.

CALIBRATION

The calibration of the IDT75C48 involves the setting of the 1st and 255th comparator thresholds to the desired voltages. This is done by varying the top and bottom voltages on the reference resistor chain, V_{RT} and V_{RB}, to compensate for any internal offsets. Assuming a nominal 0V to -2V reference range, apply -0.0039V (1/2 LSB from 0V) to the analog input, continuously strobe the device and adjust V_{RT} until the converter output toggles between the codes of 0 and 1. To adjust the 255th comparator, apply -1.996V (1/2 LSB from -2V) to the analog input and adjust V_{RB} until the converter output toggles between the codes 254 and 255.

The offset errors are caused by the parasitic resistance between the package pins and the actual resistor chain on chip and are shown as R1 and R2 in the Functional Block Diagram. The offset errors, E_{OT} and E_{OB} are specified in the System Performance Table and indicate the degree of adjustment needed.

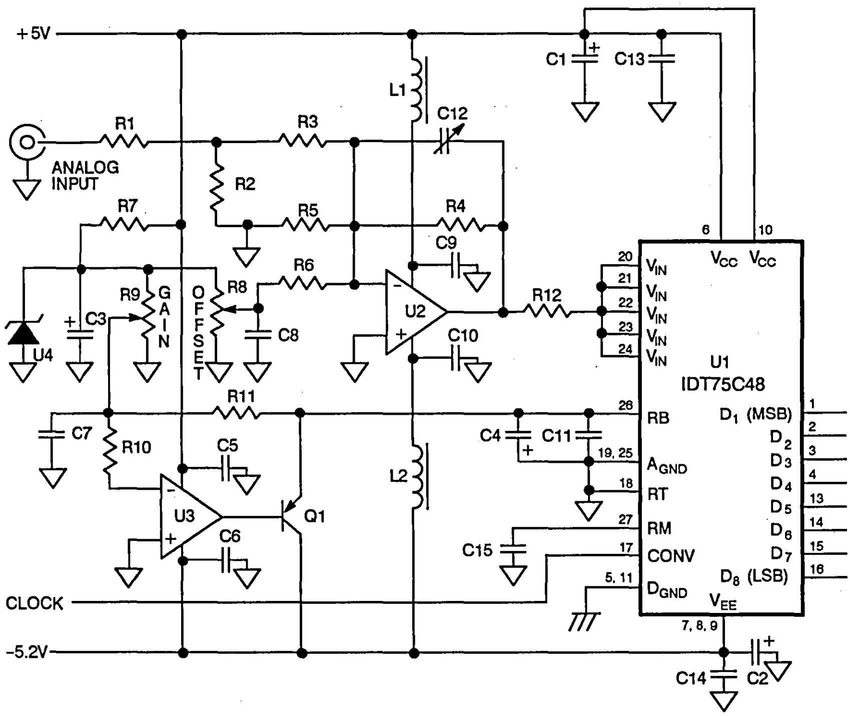
The previously described calibration scheme requires that both ends of the reference resistor chain be adjustable, i.e., be driven by operational amplifiers. A simpler method is to connect the top of the resistor chain. RT, to analog ground or 0V and to adjust this end of the range with the input buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error, which can be compensated for by varying the voltage applied to RB. This is a preferred method for gain adjustment since it is not in the input signal path. See Figure 4 for a detailed circuit diagram of this method.

TYPICAL INTERFACE

Figure 4 shows a typical application example for the IDT75C48. The analog input amplifier is a bipolar wideband operational amplifier those low impedance output directly drives the A/D Converter. The input buffer amplifier is configured with a gain of minus two which will convert a standard video input signal (1V p-p) to the recommended 2V converter input range. All five V_{IN} pins are connected together as close to the package as possible and the input buffer feedback loop is closed at this point. Bipolar inputs, as well as the calibration of the reference top, are accomplished using the offset control. A band-gap reference is used to provide a stable voltage for both the offset and gain control. A variable capacitor in the input buffer feedback loop allows optimization of either the step or frequency response and may be replaced by a fixed value in the final version of the printed circuit board.

To ensure operation to the rated specifications, proper decoupling is needed. The bypass capacitors should be located close to the chip with the shortest lead length possible. Massive ground planes are recommended. If separate digital and analog ground planes are used, they should be connected together at one point close to the IDT75C48.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier buffered by a PNP transistor. The transistor provides a low impedance source and is necessary to provide the current flowing through the resistor chain. The bottom reference voltage may be adjusted to cancel the gain error introduced by the offset voltage, E_{OB}, as discussed in the calibration section.



PARTS LIST

R1	0.0Ω
R2	80.7Ω
R3	1KΩ
R4	2KΩ
R5	220Ω
R6	2KΩ
R7	1KΩ
R8	2KΩ
R9	2KΩ
R10	10KΩ
R11	20KΩ
R12	27Ω
C1-C4	10μF
C5-C15	0.1μF
C12	1-6pF Variable
U1	IDT75C48
U2	HA-2539-5
U3	uA741C
U4	LM313
Q1	2N2907
L1, L2	Ferrite Bead

Figure 4. Application Example

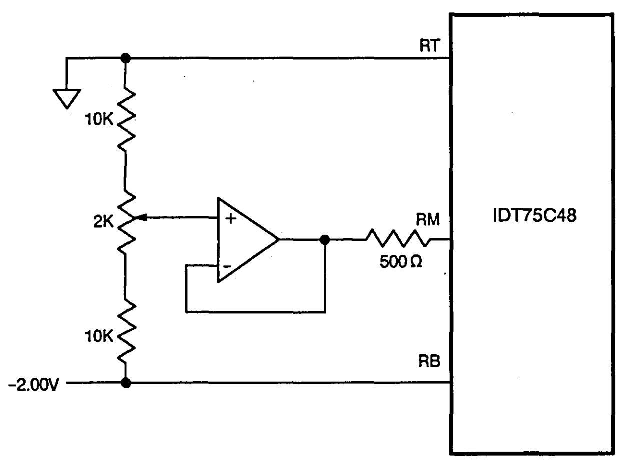


Figure 5. Mid-Point Adjust

ORDERING INFORMATION

IDT XXXX X X X X

IDT	XXXX	X	X	X	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Field	Code	Description
Process/Temperature Range	BLANK	Commercial (0°C to +70°C)
	B	Military (−55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	P	Plastic DIP
	D	CERDIP (600 mil)
	L	Leadless Chip Carrier
Speed	20	MHz
Power	S	Standard Power
Device Type	75C48	Flash A/D Converter

Integrated Device Technology, Inc.

CMOS FLASH A/D CONVERTER

PRELIMINARY
IDT75C58

FEATURES:

- 8-bit resolution
- 20 MSPS conversion rate
- Overflow Output
- Low power consumption: 500mW
- Extended analog input range
- On-chip EDC (Error Detection and Correction)
- Tri-state outputs
- Improved output logic HIGH drive, no pull-up needed
- No sample and hold required
- Differential Phase = 1 Degree
- Differential Gain = 2%
- 1/2 LSB linearity
- TTL-compatible
- Available in 28-pin CERDIP and Plastic DIP or LCC
- Military product is compliant to MIL-STD-883, Class B

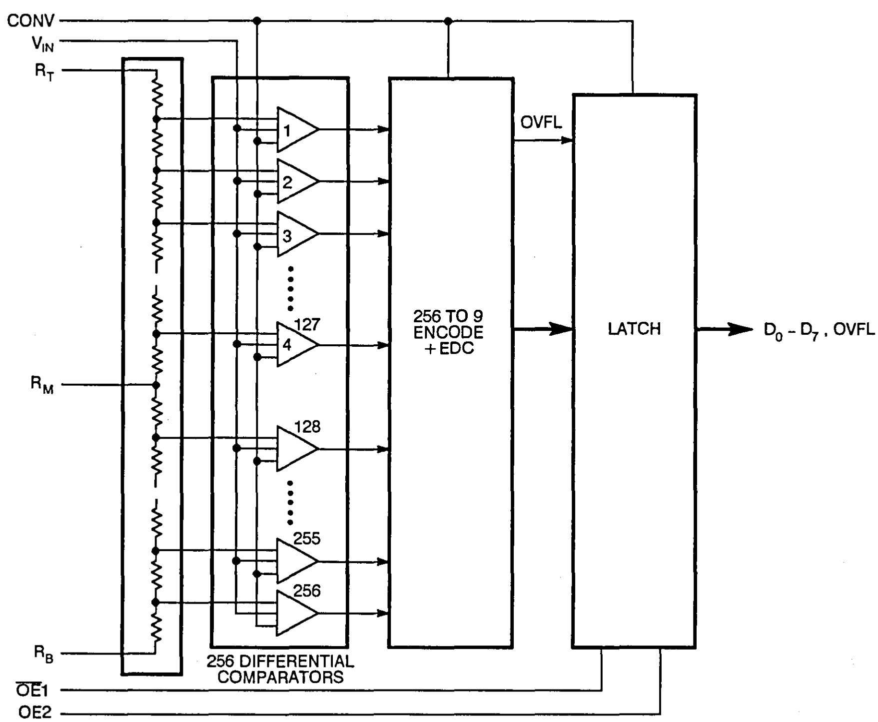
DESCRIPTION:

The IDT75C58 is a 20 MegaSample per Second (MSPS), fully parallel, 8-bit Flash Analog to Digital Converter. The wide input analog bandwidth of 7MHz permits the conversion of analog input signals with full-power frequency components up to this limit with no input sample and hold. Low power consumption due to CEMOS™ processing virtually eliminates thermal considerations. The IDT75C58 is available in 28-pin plastic and hermetic DIPs and a 28-pin LCC.

The IDT75C58 consists of a reference voltage generator, 255 comparators, encoding and EDC (Error Detection and Correction) logic and an output data register. A single clock starts the conversion process and controls all internal operations. An additional comparator detects an Overflow condition (V_{IN} more positive than Full-Scale + 1LSB) and activates the $\overline{OVFL}$ output. This output, together with two output enable inputs ($\overline{OE1}$ and OE2), allow the stacking of two IDT75C58s for 9-bit resolution with no external components.

The IDT75C58 military Flash A/D Converters are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

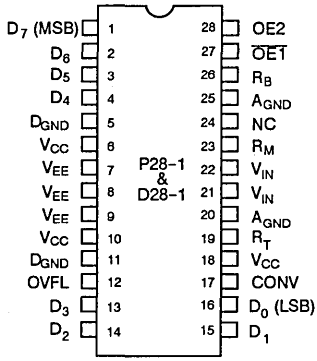
FUNCTIONAL BLOCK DIAGRAM



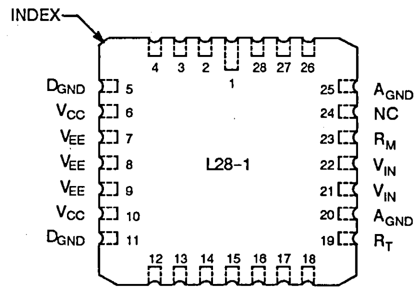
CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

GENERAL INFORMATION

The IDT75C58 has four functional sections: a comparator array, a reference voltage generator, encoding logic with EDC and output logic. The comparator array compares the input signal with 256 reference voltages to produce an N - of - 256 code. This is sometimes called a "Thermometer" code because all of the comparators with their reference voltage less than the input signal will be "on" while those with their reference above the input will be "off".

The reference voltage generator consists of a string of precisely matched resistors which generate the 256 voltages needed by the comparators. The voltages at the ends of the resistor string set the maximum and minimum conversion range and are typically 0V and -2V, respectively.

Included in the encoding function is Error Detection and Correction logic which ensures that a corrupted Thermometer code is correctly encoded.

The output logic latches and holds the data constant between samples. The output timing is designed for an easy interface to external latches or memories using the same clock as the ADC.

POWER

The IDT75C58 requires two power supply voltages, V_{CC} and V_{EE}. Typically, $V_{EE} = -5.0V$ and $V_{CC} = +5.0V$. Two separate grounds are provided, A_{GND} and D_{GND}, the analog and digital grounds. The difference between A_{GND} and D_{GND} must not exceed $\pm$ 0.1V and all power and ground pins must be connected.

REFERENCE

The IDT75C58 converts analog input signals that are within the range of the reference ($V_{RB} \leq V_{IN} \leq V_{RT}$) into digital form. V_{RB} (Reference Bottom) and V_{RT} (Reference Top) are applied across the reference resistor chain and both must be within the range of +0.1V to -2.1V. In addition, the voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 1.8V and 2.2V, with V_{RT} more positive than V_{RB}. Nominally, $V_{RT} = 0.0V$ and $V_{RB} = -2.0V$.

The IDT75C58 provides a midpoint tap, RM, which allows the converter to be adjusted for optimum linearity or a non-linear transfer function. Adjustment of RM is not necessary to meet the linearity specification. Figure 6 shows a circuit which will provide approximately 1/2 LSB adjustment to the midpoint. The characteristic impedance of RM is about 170Ω and this node should be driven from a low impedance source. Any noise introduced at this point will couple directly into the resistor chain, seriously affecting performance.

Due to the unavoidable coupling with the clock and the input signal, R_T and R_B should provide low AC impedance to ground. For applications with a fixed reference, a bypass capacitor is recommended.

CONTROL

Two function control pins, $\overline{OE1}$ and OE2 control the outputs with the function shown in Table 1.

CONVERT

The IDT75C58 begins a conversion with every rising edge of the convert signal, CONV. The analog input signal is sampled on the rising edge of CONV, while the outputs of the comparators are encoded on the falling edge. The next rising edge latches the encoder output which is presented on the output pins.

The input sample is taken within 15ns of the rising edge of CONV. This is called t_{STO} or the Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature, but the short term uncertainty or jitter is less than 60ps. If the maximum CONV pulse width HIGH time (t_{PWH}) is exceeded, the accuracy of the input sample may be impaired. The maximum CONV pulse width LOW time (t_{PWL}) may be exceeded, but the digital output data for the sample taken by the previous rising edge of CONV will be meaningless. It is recommended that CONV be held LOW during longer periods of inactivity.

The digital output data is presented at t_D, the Digital Output Delay Time, after the next rising edge of CONV. Previous output data is held for the t_{HO} (Output Hold Time) after the rising edge of CONV to allow for non-critical timing in the external circuitry. This means that the data for sample N is acquired while the converter is taking sample N+2.

ANALOG INPUT

The IDT75C58 uses strobed, auto-zeroing, latching comparators. For optimum performance, the source impedance of the analog driver must be less than 25Ω. All three analog input pins must be connected together as close to the package as possible. The input signal must remain within the range of V_{CC} to V_{EE} to prevent damage to the device.

If the analog input signal is within the reference voltage range, the output will be a binary number between 0 and 255. An input signal below V_{RB} will yield a full-scale (all outputs low) output while an input above V_{RT} will cause an OVFL output.

STEP	RANGE		OUTPUT	OVFL
	-2.0000V FS -7.8431mV/Step	-2.0480V FS -8.000mV/Step		
256	0.0000V	0.0000V	11111111	1
255	-0.0078V	-0.0080V	11111111	0
254	-0.0156V	-0.0160V	11111110	0
:	:	:	:	:
129	-0.9961V	-1.0160V	10000000	0
128	-1.0039V	-1.0240V	01111111	0
127	-1.0118V	-1.0320V	01111110	0
:	:	:	:	:
001	-1.9921V	-2.0320V	00000001	0
000	-2.0000V	-2.0400V	00000000	0

Figure 1. Output Coding

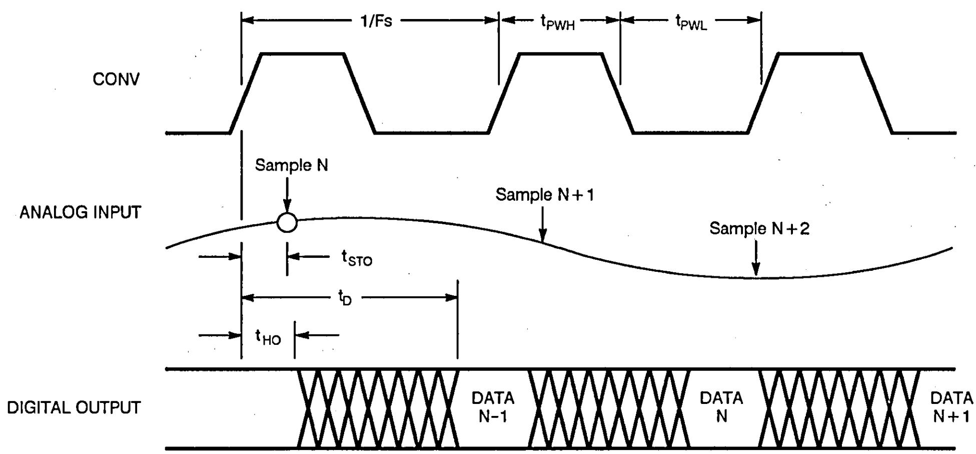


Figure 2. Timing Diagram

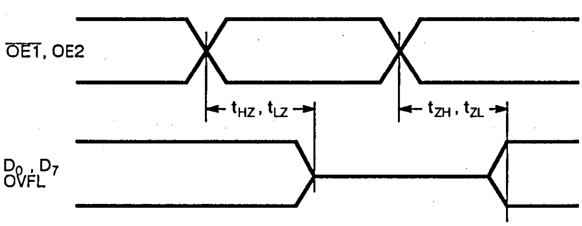


Figure 3. Output, Enable/Disable Timing

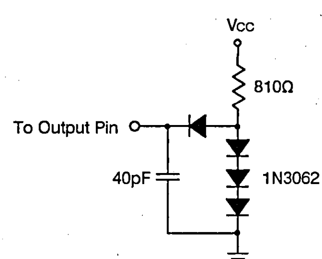


Figure 4. Output Load 1

$\overline{OE1}$	OE2	D_0 - D_7	OVFL
0	1	Valid	Valid
1	1	High Z	Valid
X	0	High Z	High Z

Table 1. Function Control

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
POWER SUPPLY			
V_{CC}	Measured to D_{GND}	-0.5 to +7.0	V
V_{EE}	Measured to A_{GND}	-0.5 to -7.0	V
A_{GND}	Measured to D_{GND}	-0.5 to +0.5	V
INPUT VOLTAGE			
CONV, $\overline{OE1}$, OE2	Measured to D_{GND}	-0.5 to V_{CC} +0.5	V
V_{IN} ,V_{RT},V_{RB}	Measured to A_{GND}	V_{CC} to V_{EE}	V
V_{RT}	Measured to V_{RB}	-2.2 to +2.2	V
OUTPUT			
Applied Voltage (2)	Measured to D_{GND}	-0.5 to V_{CC} +0.5	V
Applied Current (2, 3, 4)	Externally forced	-3.0 to +6.0	mA
Short Circuit Duration	Single output High to D_{GND}	1.0	S
TEMPERATURE			
Operating, Ambient	Military	-55 to +125	°C
	Commercial	0 to +70	°C
Storage	Military	-65 to +150	°C
	Commercial	-55 to +125	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

AC ELECTRICAL CHARACTERISTICS

Specifications over the Recommended Operating Conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	TEMPERATURE RANGE COMMERCIAL MIN.	COMMERCIAL MAX.	MILITARY MIN.	MILITARY MAX.	UNIT
F_S	Max. Conversion Rate	V_{CC}=Min.,V_{EE}=Min.	20	–	20	–	MSPS
t_{STO}	Sampling Time Offset	V_{CC}=Min.,V_{EE}=Min.	0	10	0	15	ns
t_D	Digital Output Delay	V_{CC}=Min.,V_{EE}=Min., Load 1	–	30	–	35	ns
t_{HO}	Digital Output Hold Time	V_{CC}=Max.,V_{EE}=Max., Load 1	5	–	5	–	ns
t_{HZ}	Output Disable Time from HIGH	V_{CC}=Min.,V_{EE}=Min., Load 1	–	–	–	–	ns
t_{LZ}	Output Disable Time from LOW	V_{CC}=Min.,V_{EE}=Min., Load 1	–	–	–	–	ns
t_{ZH}	Output Enable Time to HIGH	V_{CC}=Min.,V_{EE}=Min., Load 1	–	–	–	–	ns
t_{ZL}	Output Enable Time to LOW	V_{CC}=Min.,V_{EE}=Min., Load 1	–	–	–	–	ns

11

DC ELECTRICAL CHARACTERISTICS

Specifications over the Recommended Operating Conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	TEMPERATURE RANGE COMMERCIAL MIN.	COMMERCIAL MAX.	MILITARY MIN.	MILITARY MAX.	UNIT
I_{CC}	Positive Supply Current	V_{CC} = Max., static (1)		70		80	mA
I_{EE}	Negative Supply Current	V_{EE} = Max., static (1)	–	-35	–	-35	mA
I_{REF}	Reference Current (R_T to R_B)	V_{RT}, V_{RB} = NOM	–	9		10	mA
R_{REF}	Reference Resistance (R_T to R_B)	V_{RT}, V_{RB} = NOM	250	–	220	–	Ohm
R_{IN}	Equiv. Input Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = VRB	100	–	100	–	KOhm
C_{IN}	Equiv. Input Capacitance	V_{RT}, V_{RB} = NOM, V_{IN} = VRB	–	50	–	50	pF
I_{CB}	Input Const. Bias Current	V_{EE} = Max.	–	10	–	10	μA
I_{IL}	Input Current Logic LOW	V_{CC} = Max., V_{IH} = 0.5V CONV, NMINV, NLINV	–	±25	–	±25	μA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max., V_{IL} = 2.4V	–	±25	–	±25	μA
I_I	Input Current, Max. Input Voltage	V_{CC} = Max., V_I = V_{CC}	–	50	–	50	μA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min., I_{OL} = 4.0mA	–	0.5	–	0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min., I_{OH} = -2.0mA	2.4		2.4	–	V
I_{OZ}	Output High Z Current	V_{CC} = Max.	–	–	–	–	μA
C_I	Digital Input Capacitance	T_A = +25°C, F = 1MHz	–	15	–	15	pF
C_O	Digital Output Capacitance	T_A = +25°C, F = 1MHz	–	20	–	20	pF

NOTE:

1. Worst case, all digital inputs and outputs LOW.

SYSTEM PERFORMANCE

Specifications over the Recommended Operating Conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	TEMPERATURE RANGE COMMERCIAL MIN.	COMMERCIAL MAX.	MILITARY MIN.	MILITARY MAX.	UNIT
E_{LI}	Linearity Error, Integral	V_{RT}, V_{RB} = NOM	–	0.2	–	0.2	%FS
E_{LD}	Linearity Error, Differential	V_{RT}, V_{RB} = NOM	–	0.2	–	0.2	%FS
C_S	Code Size		25	175	25	175	%NOM
E_{OT}	Offset Error, Top	V_{IN} = V_{RT}	–	45	–	45	mV
E_{OB}	Offset Error, Bottom	V_{IN} = V_{RB}	–	-30	–	-30	mV
T_{CO}	Offset Error, Temperature Coefficient	V_{IN} = V_{RB}	–	±20	–	±20	μV/°C
B_W	Bandwidth, Full Power Input		7	–	5	–	MHz
T_{TR}	Transient Response, Full Scale		–	20	–	20	ns
SNR	Signal to Noise Ratio	20MSPS Conversion Rate, 10MHz Bandwidth					
	Peak Signal /RMS Noise	1.248MHz Input 2.438MHz Input	54 53	– –	53 52	– –	dB
	RMS Signal/RMS Noise	1.248MHz Input 2.438MHz Input	45 44	– –	44 43	– –	dB
E_{AP}	Aperture Error		–	60	–	60	ps
DP	Differential Phase Error	F_S = 4xNTSC	–	1	–	1	Degree
DG	Differential Gain Error	F_S = 4xNTSC	–	2	–	2	%
NPR	Noise Power Ratio	DC to 8MHz White Noise Bandwidth 4 Sigma Loading 1.248 MHz Slot 20MSPS Conversion Rate	36.5	–	36.5	–	dB

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TEMPERATURE RANGE COMMERCIAL MIN.	NOM	MAX.	MILITARY MIN.	NOM	MAX.	UNIT
V_{CC}	Positive Power Supply	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Power Supply	-4.75	-5.0	-5.5	-4.5	-5.0	-5.5	V
V_{AGND}	Analog Ground Voltage (ref D_{GND})	-0.1	0	+0.1	-0.1	0	+0.1	V
t_{PWL}	CONV, Pulse Width LOW	18	–	100,000	18	–	100,000	ns
t_{PWH}	CONV, Pulse Width HIGH	22	–	20,000	22	–	20,000	ns
V_{IL}	Input Voltage, Logic LOW	-0.5	–	0.8	-0.5	–	0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0	–	V_{CC}+.1	2.0	–	V_{CC}+.1	V
I_{OL}	Output Current, Logic LOW	–	–	4.0	–	–	4.0	mA
I_{OH}	Output Current, Logic HIGH	–	–	-400	–	–	-400	μA
V_{RT}	Most Positive Reference Voltage(1)	-0.1	0	+0.1	-0.1	0	+0.1	V
V_{RB}	Most Negative Reference Voltage(1)	-1.9	-2.0	-2.1	-1.9	-2.0	-2.1	V
$V_{RT}-V_{RB}$	Reference Voltage Range	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage Range	V_{RB}	–	V_{RT}	V_{RB}	–	V_{RT}	V
T_A	Ambient Temperature, Still Air	0	–	70	–	–	–	°C
T_C	Case Temperature	–	–	–	-55	–	+125	°C

NOTE:
1. V_{RT} must be more positive than V_{RB} and the voltage reference differential must be within the specified range.

CALIBRATION

The calibration of the IDT75C58 involves the setting of the 1st and 255th comparator thresholds to the desired voltages. This is done by varying the top and bottom voltages on the reference resistor chain, V_{RT} and V_{RB}, to compensate for any internal offsets. Assuming a nominal 0V to -2V reference range, apply -0.0039V (1/2 LSB from 0V) to the analog input, continuously strobe the device and adjust V_{RT} until the OVFL output toggles between 0 and 1. To adjust the 256th comparator, apply -1.996V (1/2 LSB from -2V) to the analog input and adjust V_{RB} until the converter output toggles between the codes 0 and 1.

The offset errors are caused by the parasitic resistance between the package pins and the actual resistor chain on-chip and are shown as R1 and R2 in the Functional Block Diagram. The offset errors, E_{OT} and E_{OB}, are specified in the System Performance Table and indicate the degree of adjustment needed.

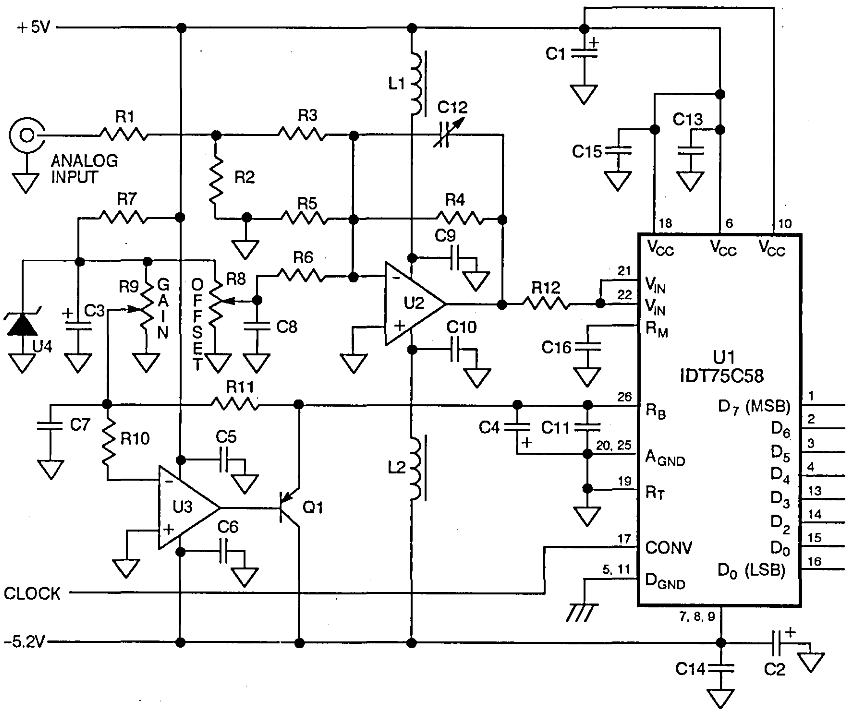
The previously described calibration scheme requires that both ends of the reference resistor chain be adjustable, i.e. be driven by operational amplifiers. A simpler method is to connect the top of the resistor chain, R_T, to analog ground or 0V and to adjust this end of the range with the input buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error which can be compensated for by varying the voltage applied to R_B. This is a preferred method for gain adjustment since it is not in the input signal path. See Figure 5 for a detailed circuit diagram of this method.

TYPICAL INTERFACE

Figure 5 shows a typical application example for the IDT75C58. The analog input amplifier is a bipolar wideband operational amplifier whose low impedance output directly drives the A/D Converter. The input buffer amplifier is configured with a gain of minus two which will convert a standard video input signal (1V p-p) to the recommended 2V converter input range. Both V_{IN} pins are connected together as close to the package as possible and the input buffer feedback loop is closed at this point. Bipolar inputs, as well as the calibration of the reference top, are accomplished using the offset control. A band-gap reference is used to provide a stable voltage for both the offset and gain control. A variable capacitor in the input buffer feedback loop allows optimization of either the step or frequency response and may be replaced by a fixed value in the final version of the printed circuit board.

To ensure operation to the rated specifications, proper decoupling is needed. The bypass capacitors should be located close to the chip with the shortest lead length possible. Massive ground planes are recommended. If separate digital and ground planes are used, they should be connected together at one point close to the IDT75C48.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier buffered by a PNP transistor. The transistor provides a low impedance source and is necessary to provide the current flowing through the resistor chain. The bottom reference voltage may be adjusted to cancel the gain error introduced by the offset voltage, E_{OB}, as discussed in the calibration section.



PARTS LIST

R1	0.0Ω
R2	80.7Ω
R3	1KΩ
R4	2KΩ
R5	220Ω
R6	2KΩ
R7	1KΩ
R8	2KΩ
R9	2KΩ
R10	10KΩ
R11	20KΩ
R12	27Ω
C1–C4	10µF
C5–C16	0.1µF
C12	1–6pF Variable
U1	IDT75C58
U2	HA-2539-5
U3	uA741C
U4	LM313
Q1	2N2907
L1, L2	Ferrite Bead

Figure 5. Application Example

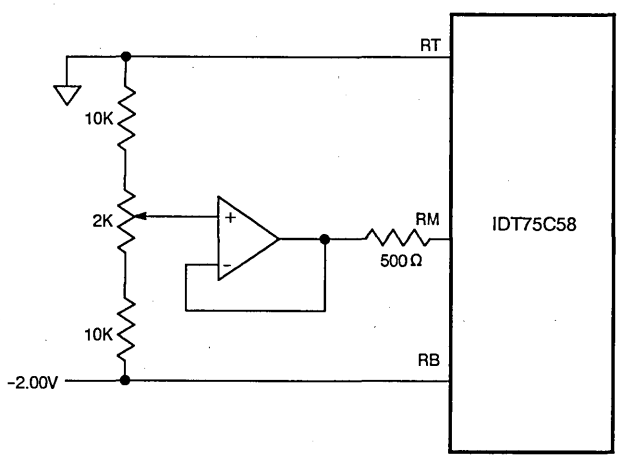


Figure 6. Mid-Point Adjust

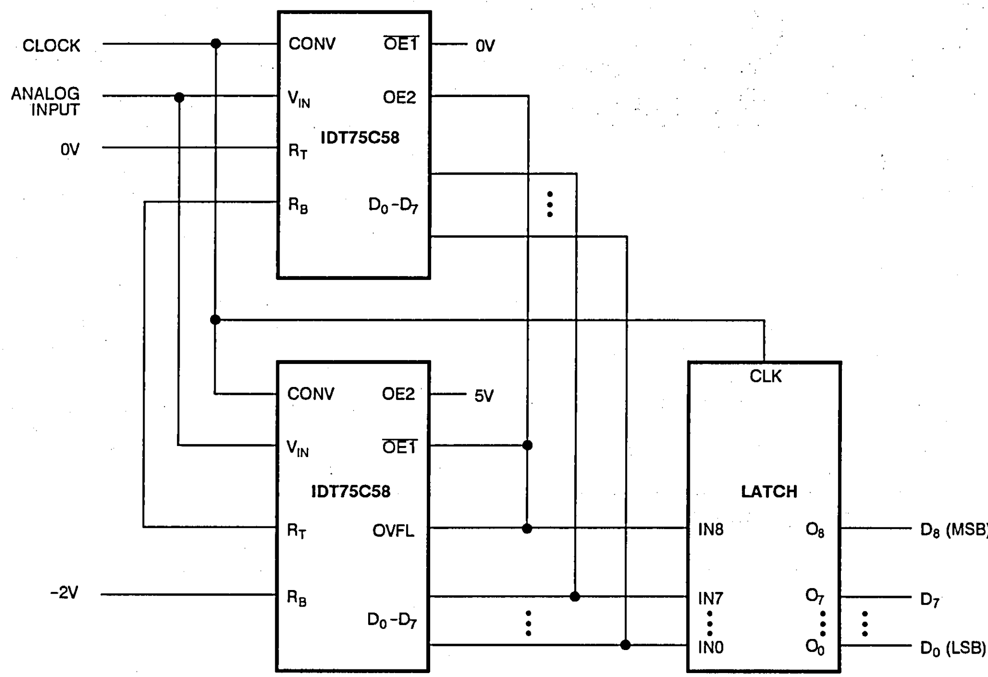


Figure 7. Simplified 9-Bit Application

ORDERING INFORMATION

IDT XXXX (Device Type) X (Power) X (Speed) X (Package) X (Process/Temperature Range)

Code	Description
BLANK	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
D	CERDIP (600 mil)
L	LCC (450 mil square)
20	MHz
S	Standard Power
75C58	Flash A/D Converter

11

CMOS 8-BIT FLASH ADC MODULE

ADVANCE INFORMATION
IDT75M48

Integrated Device Technology, Inc.

FEATURES:

- 20 MSPS conversion rate
- 8-bit resolution
- 1/2 LSB linearity
- Low power consumption: 750mW
- 24-pin, 600 mil DIP footprint
- Input bandwidth >7MHz, no sample and hold required
- On-board voltage reference and analog input buffer
- TTL-compatible inputs and outputs
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Modules available with the semiconductor components compliant to MIL-STD-883, Class B

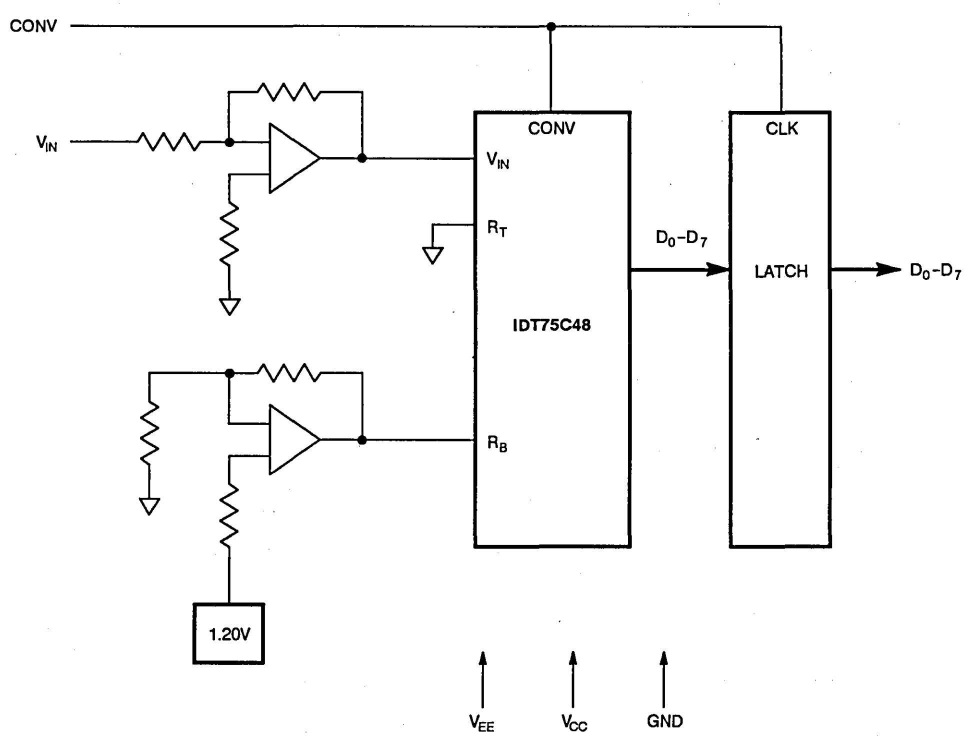
DESCRIPTION:

The IDT75M48 is a 20 MegaSample per Second (MSPS), fully parallel Flash Analog to Digital Converter subsystem. Contained within the module is the IDT75C48 Flash ADC and all the peripheral components needed to make a fully functional converter. Careful attention has been paid to the substrate layout and power supply bypassing to ensure the highest performance.

The IDT75M48 is built using LCC packages mounted on a multilayer ceramic substrate using IDT's high-reliability vapor phase solder reflow process.

The IDT75M48 military ADC module is available with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

CMOS 9-BIT FLASH ADC MODULE

ADVANCE INFORMATION
IDT75M49

FEATURES:

- 20 MSPS conversion rate
- 9-bit resolution
- 1/2 LSB linearity
- Low power consumption: 950mW
- 24-pin, 600 mil DIP footprint
- Input bandwidth >7MHz
- On-board voltage reference and analog input buffer
- TTL-compatible inputs and outputs
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

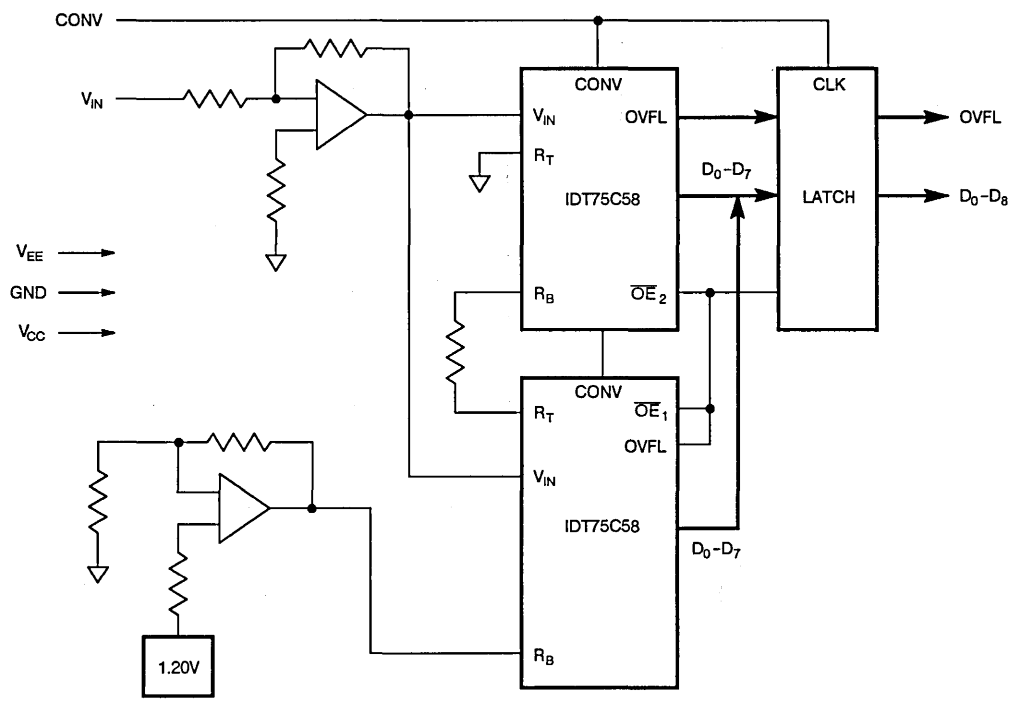
DESCRIPTION:

The IDT75M49 is a 9-bit, 20 MegaSample per Second (MSPS), fully parallel Flash Analog to Digital Converter subsystem. Contained within the module are two IDT75C58 Flash ADCs and all the peripheral components needed to make a fully functional 9-bit converter. Careful attention has been paid to the substrate layout and power supply bypassing to ensure the highest performance.

The IDT75M49 is built using LCC packages mounted on a multilayer ceramic substrate using IDT's high-reliability vapor phase solder reflow process.

The IDT75M49 military ADC module is available with the semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORIES

An Electrically Erasable (E^2) CEMOS technology has been developed to produce high-performance, programmable, nonvolatile devices that include E^2PROMs. In memory products, it is IDT's intent to develop E^2PROMs that mimic SRAM performance. IDT E^2 products will closely follow IDT SRAM innovations in speed, density and application specific features. Products include JEDEC pin-function compatible E^2 PROMs, E^2 PROMs with serial accessibility and registers, and high density E^2PROM modules. IDT nonvolatile products utilize the industry standard floating gate thin oxide technology and are fully tested to meet endurance and data retention specifications.

IDT E^2PROMs are designed for military and commercial temperature applications. Radiation tolerant and radiation enhanced E^2PROMs will also be available.

TABLE OF CONTENTS

CONTENTS **PAGE**

EEPROMs—Electrically Erasable Programmable Read Only Memories

Integrated Device Technology, Inc.

FAST CMOS EEPROM 16K (2K x 8-BIT)

IDT78C16A

FEATURES:

- 5 volt only operation
- Fast access times
  - Military: 75ns (max.)
  - Commercial: 70ns (max.)
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ms max.
- $\overline{\text{DATA}}$ Polling—detection of write cycle completion
- Low-power CEMOS™ technology
  - 125mA active current
  - 0.9mA standby current (full CMOS)
- Data protection circuitry (V_{CC} lockout for V_{CC} < 3.8V) provides data integrity on power up/power down
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- JEDEC approved byte-wide pinout
- 24-pin THINDIP (300 mil.), 24-pin DIP (600 mil.) and 32-pin LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

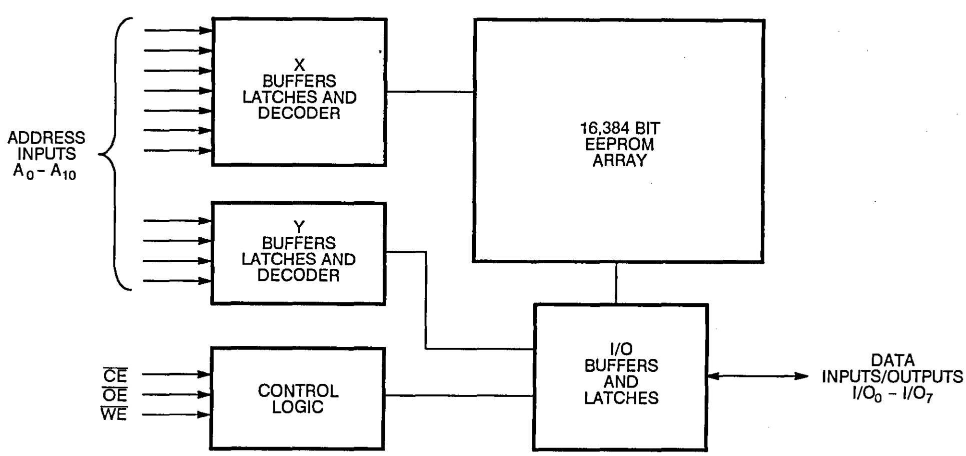
The IDT78C16A is a 5 volt only 2K x 8 Electrically Erasable Programmable Read-Only Memory (EEPROM). This high-speed CEMOS™ EEPROM is written on a byte basis and provides 16,384 bits of non-volatile data storage (data retention in excess of 100 years). Its fast read access time allows zero wait state read cycles with high-performance microprocessors.

Writing is simplified by an internal charge-pump and timer circuit which eliminates the need for special external programming voltage and write pulse shaping circuits. Byte erase before write occurs automatically and input buffers, latches and internal timer free the host system for other tasks during the write cycle. A $\overline{\text{DATA}}$ Polling mode provides a method for determining write cycle completion. The IDT78C16A also contains a dual voltage detection logic circuit which allows the device to be used in older applications which incorporate external programming circuits.

The IDT78C16A is function- and pinout-compatible with the IDT6116, 2K x 8 static RAM. It is ideal for systems requiring non-volatility and in-system data modifications.

Military grade product is manufactured in compliance to the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

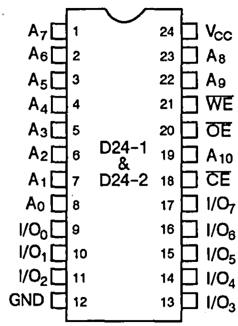
FUNCTIONAL BLOCK DIAGRAM



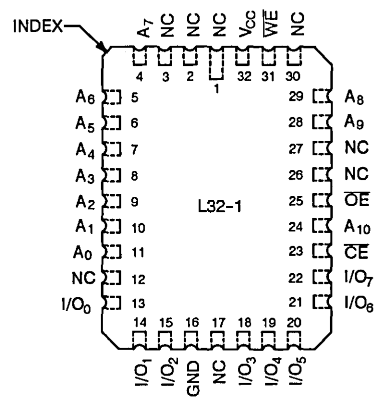
12

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

PIN NAMES

$A_0 - A_3$	Addresses-Column
$A_4 - A_{10}$	Addresses-Row
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O_0 - I/O_7	Data Input (I_0 - I_7) during write; Data Output (O_0 - O_7) during read
V_{CC}	Power
GND	Ground

DEVICE OPERATIONAL MODE [1]

MODE	PIN			$I/O_0 - I/O_7$
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	
Read	V_{IL}	V_{IL}	V_{IH}	$Data_{OUT}$ ($O_0 - O_7$)
Byte Write	V_{IL}	V_{IH}	V_{IL}	$Data_{IN}$ ($I_0 - I_7$)
Standby	V_{IH}	Don't Care	Don't Care	High Z
Write Inhibit	Don't Care	V_{IL}	Don't Care	High Z
	Don't Care	Don't Care	V_{IH}	High Z

NOTE:
1. All control inputs are TTL-compatible.

READ MODE

Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) must be logically active in order for data to be available at the outputs. After a selected byte address is stable, $\overline{CE}$ is taken to a TTL LOW (enabling chip). The Write Enable ($\overline{WE}$) pin should remain deselected (TTL HIGH) during the entire read cycle. Data is gated from the device outputs by selecting the $\overline{OE}$ pin (TTL LOW).

WRITE MODE

The IDT78C16A is programmed electrically in-circuit and does not require any external latching, erasing or timing. Writing to the IDT78C16A is as easy as writing to a static RAM. When a write cycle is initiated, the device automatically latches the address, data and control signals as it begins its write operation.

A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The IDT78C16A supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. All inputs, except for data, are latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Data is then latched in by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurred first. An automatic byte erase of the existing data at the addressed location is performed before the new data byte is written. Once initiated, a byte write operation will automatically proceed to completion within 10ms.

STANDBY MODE

The IDT78C16A features a standby mode which reduces the maximum active current from 125mA to 20mA for TTL levels and to 0.9mA for CMOS levels. With $\overline{CE} \geq V_{IH}$ all outputs are in the high impedance state.

DATA PROTECTION

Nonvolatile data is protected from inadvertent writes in the following manner:

Power Up/Down

On-chip circuitry provides protection against false write during V_{CC} power up/down. The IDT78C16A features an internal sensing circuit that disables the internal programming circuit if $V_{CC} < 3.8V$. This prevents input signals at $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ from triggering a write cycle during a V_{CC} power up/down event.

Noise Protection

The IDT78C16A will typically reject write pulses that are less than 15ns. This prevents spurious noise from initiating a write cycle.

Write Inhibit

Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during a power-on and power-off, will inhibit inadvertent writes.

$\overline{\text{DATA}}$ Polling

The IDT78C16A has a maximum write cycle time of 10ms; a write will always be completed in less than the maximum cycle time. Write cycle completion is readily determined via a simple software routine ($\overline{\text{DATA}}$ Polling) that performs a read operation while the device is in an automatic write mode. If a read command (addressed to the last byte written) is given while the IDT78C16A is still writing, the inverse of the most significant bit (I/O_7 pin) of the last byte written will be present. True data is not released until the write cycle is completed. Thus, a $\overline{\text{DATA}}$ polling monitor of the output (or periodic read of the last written byte) for true data can be used to detect early completion of a write cycle.

ENDURANCE

IDT's EEPROM technology employs the Fowler-Nordheim method of tunneling across a thin oxide. IDT78C16A EEPROMs are designed and tested for applications requiring extended endurance.

The endurance failure mechanism associated with EEPROMs results from the charge trapping in the thin tunneling dielectric. This failure is a function of the number of write cycles that each byte in the part has experienced. Trapped charges accumulate slowly with each write cycle, eventually becoming large enough to prevent reliable writing to the bit cell. Since some bits may be more sensitive than others, an endurance failure is typically a single bit failure (i.e. a failure of a single bit to properly write or retain data).

To test for endurance, sample devices are written 10,000 times at every byte location and checked for data retention capability. IDT's tests ensure that shipped devices will write a minimum of 10,000 times (at every byte location) with a maximum failure rate of 1%. This means that up to 1% of a sample of devices will fail to write or retain data after being written to 10,000 times. Those devices that do fail typically have a single bit(s) that fails to retain data after being written.

For more detailed information please refer to the *IDT Reliability Report on Endurance*.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ENDURANCE

PARAMETER	VALUE	UNIT
Minimum Endurance	10,000	Cycles/Byte

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-0.3	0.4	0.8	V
V_{WI}	Write Inhibit	3.8	–	–	V

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 5.0V)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified

T_A = 0°C to +70°C V_{CC} = 5.0V ± 10% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V V_{HC} = V_{CC} -0.2V
C_L = 30pF

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	–	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	–	10	µA
I_{CC1}	Operating Power Supply Current V_{CC} = Max., f = 0	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	–	125	mA
I_{CC2}	Dynamic Operating Current V_{CC} = Max., f = f_{MAX}	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	–	125	mA
I_{SB}	Standby Power Supply Current (TTL Level)	$\overline{CE} \geq V_{IH}$, V_{CC} = Max., $I_{I/O}$ = 0mA $V_{IN} \geq V_{IH}$ or $0 \leq V_{IN} \leq V_{IL}$	–	20	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level)	$\overline{CE} \geq V_{HC}$, V_{CC} = Max., $I_{I/O}$ = 0mA $V_{IN} \geq V_{CC}$ -0.2V or $0 \leq V_{IN} \leq 0.2V$	–	0.9	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2mA	2.4	–	V

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, C_L = 30pF, 0°C to +70°C)

SYMBOL	PARAMETER	COMMERCIAL 0°C to +70°C										UNIT
		78C16A70		78C16A90/100		78C16A120		78C16A150		78C16A200		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{CE}	Chip Enable Access Time	–	70	–	90/100	–	120	–	150	–	200	ns
t_{AA}	Address Access Time	–	70	–	90/100	–	120	–	150	–	200	ns
t_{OE}	Output Enable to Output Valid	–	50	–	60/65	–	70	–	70	–	70	ns
t_{CLZ}	Chip Enable to Output in Low Z(1)	5	–	5	–	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z(1)	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Disable to Output in High Z(1)	0	20	0	20	0	20	0	20	0	20	ns
t_{OHZ}	Output Disable to Output in High Z(1)	0	20	0	20	0	20	0	20	0	20	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns

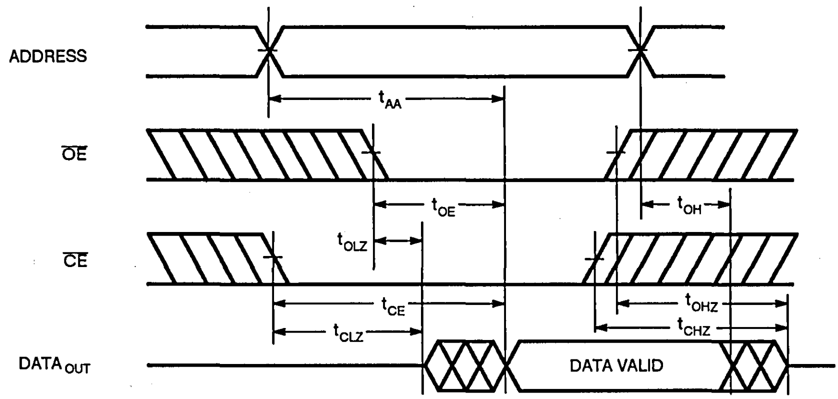
NOTE:
1. This parameter is guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, C_L = 30pF, -55°C to +125°C)

SYMBOL	PARAMETER	MILITARY -55°C to +125°C										UNIT
		78C16A75		78C16A90/100		78C16A120/150		78C16A200/250		78C16A300/350		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{CE}	Chip Enable Access Time	–	75	–	90/100	–	120/150	–	200/250	–	300/350	ns
t_{AA}	Address Access Time	–	75	–	90/100	–	120/50	–	200/250	–	300/350	ns
t_{OE}	Output Enable to Output Valid	–	50	–	60/65	–	70	–	70	–	70	ns
t_{CLZ}	Chip Enable to Output in Low Z(1)	5	–	5	–	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z(1)	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Disable to Output in High Z(1)	0	30	0	30	0	30	0	30	0	30	ns
t_{OHZ}	Output Disable to Output in High Z(1)	0	30	0	30	0	30	0	30	0	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns

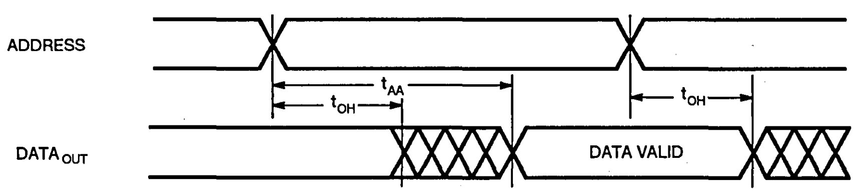
NOTE:
1. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



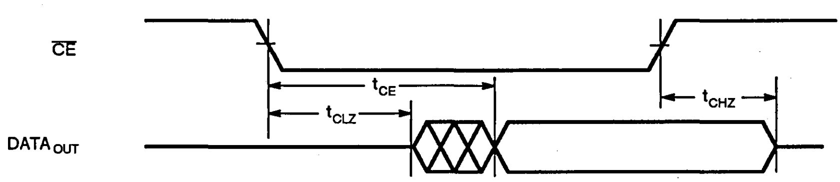
NOTE:
1. $\overline{\text{WE}}$ is HIGH for Read Cycle.

TIMING WAVEFORM OF READ CYCLE NO. 2[1]



NOTE:
1. $\overline{\text{WE}}$ is HIGH; $\overline{\text{CE}} = V_{IL}$; $\overline{\text{OE}} = V_{IL}$

TIMING WAVEFORM OF READ CYCLE NO. 3[1]



NOTE:
1. $\overline{\text{WE}}$ is HIGH; $\overline{\text{OE}} = V_{IL}$; address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges; C_L = 30pF)

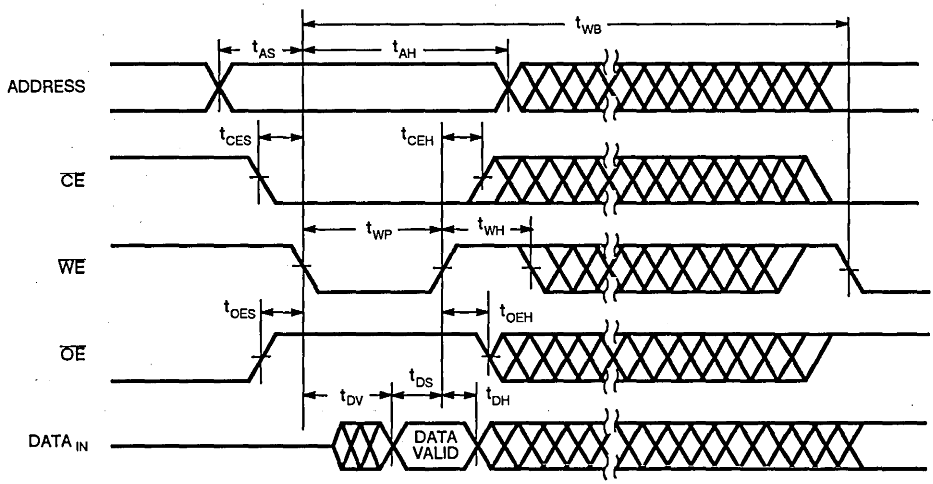
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
WRITE CYCLE				
t_{AS}	Address Set-up Time	5	–	ns
t_{AH}	Address Hold Time	50	–	ns
t_{DS}	Data Set-up Time	20	–	ns
t_{DH}	Data Hold from Write Time	15	–	ns
t_{OES}	Output Enable Set-up Time	5	–	ns
t_{OEH}	Chip Enable Hold from Write Time	15	–	ns
t_{CES}	Chip Enable Set-up Time	0	–	ns
t_{CEH}	Chip Enable Hold Time	0	–	ns
t_{WP}	Write Pulse Width	50	–	ns
t_{WB}	Byte Write Cycle	–	10	ms
t_{DBV}	$\overline{\text{DATA}}$ Polling to $\overline{\text{DATA}}$ Valid	–	t_{OE}	
t_{WH}	Write Hold Time	15	–	ns
t_{DP}	End of Write Pulse to $\overline{\text{DATA}}$ Polling	15	–	ns
t_{WES}	Write Enable Set-up Time	0	–	ns
t_{WEH}	Write Enable Hold Time	0	–	ns
t_{DV}	Data Valid Time [1, 2]	–	1	µs

NOTES:
1. Data must be valid within 1µs maximum and must remain valid if t_{WP} is longer than 1µs.
2. This parameter is guaranteed but not tested

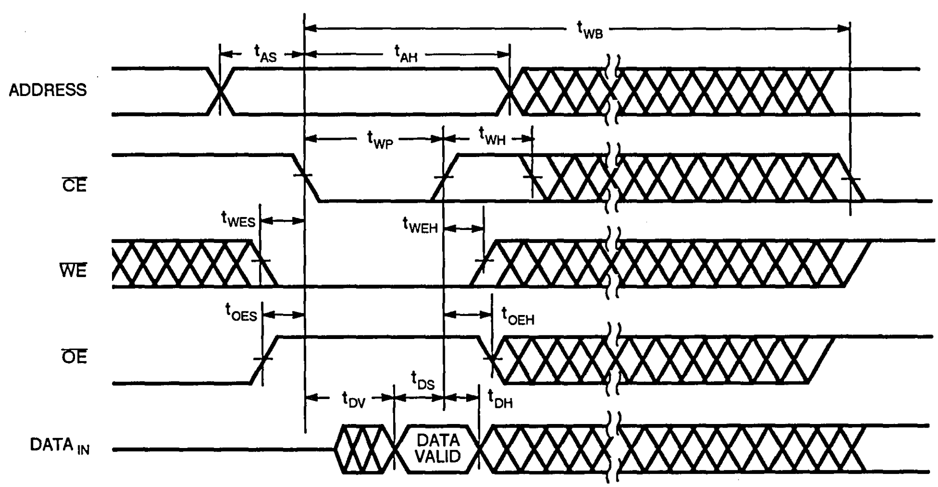
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

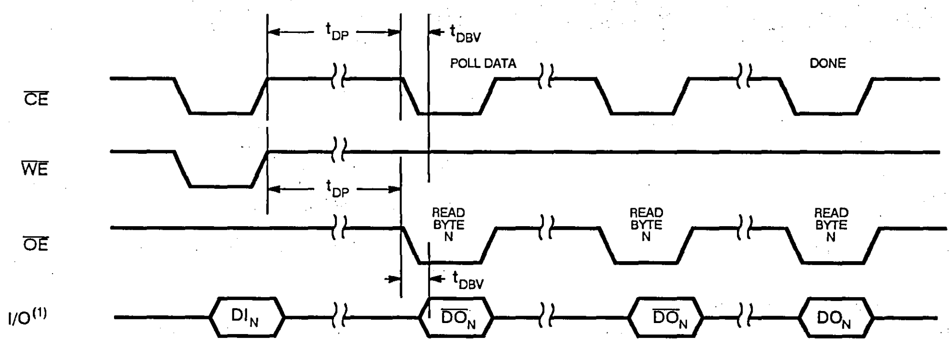
TIMING WAVEFORM OF WRITE CYCLE NO. 1, $\overline{WE}$ CONTROLLED



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED



DATA POLLING



NOTE:
1. Most significant bit of the byte being written is inverted and available at I/O_7 if a Read command is issued. All other outputs are high impedance at this time. True data will not be released until the Write cycle is completed.

ORDERING INFORMATION

IDT XXXX (Device Type) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range:

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

TD	THINDIP (CERDIP)
D	CERDIP
L	Leadless Chip Carrier

Speed (Speed in Nanoseconds):

70	Commercial Only
75	Military Only
90	
100	
120	
150	
200	
250	Military Only
300	Military Only
350	Military Only

Device Type:

78C16A	16K (2K x 8-Bit) Fast CMOS EEPROM

12

FAST CMOS EEPROM WITH SERIAL PROTOCOL CHANNEL (SPC™) 16K (2K x 8-BIT)

IDT78C18A

Integrated Device Technology, Inc.

FEATURES:

- 2K x 8 EEPROM with serial write and readback
- 5 volt only operation
- Fast access times
  - Military: 75ns (max.)
  - Commercial: 70ns (max.)
- Low-power CEMOS™ technology
  - Active Current: 125mA
  - Standby Current (full CMOS): 0.9mA
- Serial Protocol Channel (SPC) allows load and readout of the memory array over a 4-wire channel
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ms max.
- $\overline{\text{DATA}}$ Polling—detection of write cycle completion
- Data protection circuitry (V_{CC} lockout for $V_{CC} < 3.8V$) provides data integrity on power up/power down
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- Available in 28-pin THINDIP and 32-pin LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

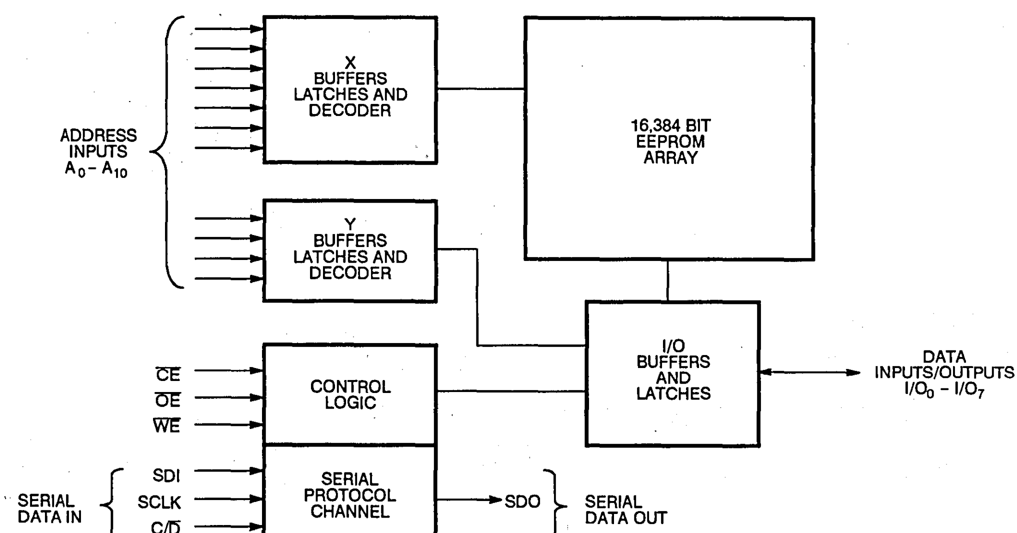
The IDT78C18A is a 5 volt only 2K x 8 Electrically Erasable Programmable Read-Only Memory (EEPROM) with Serial Protocol Channel (SPC). SPC complements the EEPROM's parallel information path by providing a serial link (4 additional pins) by which its nonvolatile array can be loaded or read. The IDT78C18A is written on a byte basis and provides 16,384 bits of nonvolatile data storage (data retention in excess of 100 years). Fast read access times allow zero wait state cycles with high-performance microprocessors.

Writing is simplified by an internal charge-pump and timer circuit which eliminates the need for external programming voltage and write pulse shaping circuits. Internal latches free the host system for other tasks during a write cycle. Byte erase before write occurs automatically. A $\overline{\text{DATA}}$ Polling mode is provided for determining write cycle completion.

The IDT78C18A is ideal for systems requiring nonvolatility and in-system data modifications. With SPC, a serial link can be established during board layout for easy field updates of code changes.

The IDT78C18A military EEPROM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

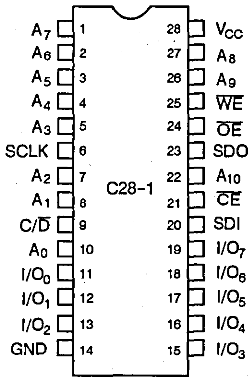
FUNCTIONAL BLOCK DIAGRAM



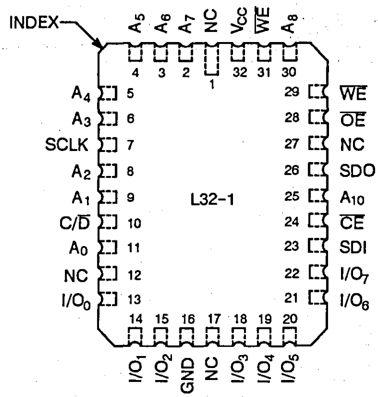
CEMOS and SPC are trademarks of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

DEVICE OPERATIONAL MODE [1,2]

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_7$
Read	V_{IL}	V_{IL}	V_{IH}	$Data_{OUT}$ $(O_0 - O_7)$
Byte Write	V_{IL}	V_{IH}	V_{IL}	$Data_{IN}$ $(I_0 - I_7)$
Standby	V_{IH}	Don't Care	Don't Care	High Z
Write Inhibit	Don't Care	V_{IL}	Don't Care	High Z
	Don't Care	Don't Care	V_{IH}	High Z
Chip Erase	V_{IL}	V_H (2)	V_H (2)	High Z

NOTES:
1. All control inputs are TTL-compatible.
2. V_H = High Voltage; optional function, consult IDT for more details.

PIN NAMES

$A_0 - A_3$	Addresses-Column
$A_4 - A_{10}$	Addresses-Row
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$I/O_0 - I/O_7$	Data Input $(I_0 - I_7)$ during write; Data Output $(O_0 - O_7)$ during read
SDI	Serial Data Input
SDO	Serial Data Output
SCLK	Data Clock Input
C/$\overline{D}$	Command/$\overline{Data}$

12

SPC OPERATIONAL MODES [1]

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	C/$\overline{D}$	SCLK	FUNCTION
Command	X	X	X	H	↑	Shift bit into command register
Data	X	X	X	L	↑	Shift bit into data register
Execute	X	X	X	↓	↑	Execute command during time between C/$\overline{D}$ and SCLK

NOTE:
1. X = Don't Care

READ MODE

Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) must be logically active in order for data to be available at the outputs. After a selected byte address is stable, $\overline{CE}$ is taken to a TTL LOW (enabling chip). The Write Enable ($\overline{WE}$) pin should remain deselected (TTL HIGH) during the entire read cycle. Data is gated from the device outputs by selecting the $\overline{OE}$ pin (TTL LOW). For serial read function, see description within "Serial Protocol Channel" section.

WRITE MODE

The IDT78C18A is programmed electrically in-circuit and does not require any external latching, erasing or timing. Writing to the IDT78C18A is as easy as writing to a static RAM. When a write cycle is initiated, the device automatically latches the address, data and control signals as it begins its write operation.

A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The IDT78C18A supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. All inputs, except for data, are latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Data is then latched in by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurred first. An automatic byte erase of the existing data at the addressed location is performed before the new data byte is written. Once initiated, a byte write operation will automatically proceed to completion within 10ms. For serial write function, see description within "Serial Protocol Channel" section.

STANDBY MODE

The IDT78C18A features a standby mode which reduces the maximum active current from 125mA to 20mA for TTL levels and to 0.9mA for CMOS levels. With $\overline{CE} \geq V_{IH}$ all outputs are in the high impedance state.

DATA PROTECTION

Nonvolatile data is protected from inadvertent writes in the following manner:

Power Up/Down

On-chip circuitry provides protection against false write during V_{CC} power up/down. The IDT78C18A features an internal sensing circuit that disables the internal programming circuit if $V_{CC} < 3.8V$. This prevents input signals at $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ from triggering a write cycle during a V_{CC} power up/down event.

Noise Protection

The IDT78C18A will typically reject write pulses that are less than 15ns. This prevents the initiation of a write cycle by a noise occurrence.

Write Inhibit

Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during a power-on and power-off, will inhibit inadvertent writes.

$\overline{\text{DATA}}$ POLLING

The IDT78C18A has a maximum write cycle time of 10ms; a write will always be completed in less than the maximum cycle time. Write cycle completion is readily determined via a simple software routine ($\overline{\text{DATA}}$ Polling) that performs a read operation while the device is in an automatic write mode. If a read command (addressed to the last byte written) is given while the IDT78C18A is still writing, the inverse of the most significant bit (I/O_7 pin) of the last byte written will be present. The most significant bit becomes valid when the write cycle is completed. Thus, a $\overline{\text{DATA}}$ Polling monitor of the output (or periodic read of the last written byte) for true data can be used to detect early completion of a write cycle.

CHIP ERASE

In particular applications, erasure of the entire chip (all bytes simultaneously) may be desired. An optional chip erase feature of the IDT78C18A allows erasure of the entire chip within 5ms. Contact IDT for more details regarding this optional function.

ENDURANCE

IDT's EEPROM technology employs the Fowler-Nordheim method of tunneling across a thin oxide. IDT78C18A EEPROMs are designed and tested for applications requiring extended endurance.

The endurance failure mechanism associated with EEPROMs results from the charge trapping in the thin tunneling dielectric. This failure is a function of the number of write cycles that each byte in the part has experienced. Trapped charges accumulate slowly with each write cycle and eventually become large enough to prevent reliable writing to the bit cell. Since some bits are more sensitive than others, an endurance failure is typically a single bit failure (i.e. a failure of a single bit to properly write or retain data).

To test for endurance, sample devices are written 10,000 times at every byte location and checked for data retention capability. IDT's tests ensure that shipped devices will write a minimum of 10,000 times (at every byte location) with a maximum failure rate of 1%. This means that up to 1% of a sample of devices will fail to write or retain data after being written to 10,000 times. Those devices that do fail typically have a single bit(s) that fails to retain data after being written.

For more detailed information please refer to the *IDT Reliability Report on Endurance*.

SERIAL PROTOCOL CHANNEL

The Serial Protocol Channel (SPC™) provides a method by which data can be entered or extracted from the memory array via four unique pins C/$\overline{D}$, SCLK, SDI and SDO. SPC logic consists of a 24-bit data shift register, a 4-bit command register and clock logic consisting of gates and a flip-flop (see block diagram). From the outside, SPC appears like two parallel serial shift registers; one for command and the other data. Data is clocked in on a Serial Data Input pin (SDI) and out on a Serial Data Output pin (SDO). The transfer of data is controlled by a serial clock (SCLK) and a Command/$\overline{\text{Data}}$ mode input (C/$\overline{D}$). The serial clock (SCLK input) shifts information and the Command/$\overline{\text{Data}}$ (C/$\overline{D}$) input selects the register that will be shifted. The command register (when loaded and executed) controls the loading of data into and out of the data register with regard to writing to or reading from an addressed location of the memory array.

There are two modes for the shift operation: when C/$\overline{D}$ input is LOW, data information is shifted through the device and, when C/$\overline{D}$ is HIGH, command is shifted through. As the C/$\overline{D}$ line transitions from HIGH (command) to LOW (data), a clock pulse is internally generated to the command decode logic and is used to execute the instruction in the command register (clock pulse ends when serial clock transitions from LOW to HIGH). There are four steps to executing an SPC command: data is shifted in, command bits are then shifted in, the command is then executed and data is clocked (shifted) out. (Note: The data to the SPC is shifted in LSB first.) During the data mode, data is simultaneously shifted into the serial data register while data in the register is shifted out.

Command codes that are utilized for read/write operations are shown below:

Command Words (4-bit Command Register):

0000	Read
0001	Write (Byte)
0010	Invalid Command—Reserved for Optional Chip Erase
3 → 15	No Operation

All functions can be performed serially, including $\overline{\text{DATA}}$ Polling. The operation of serial $\overline{\text{DATA}}$ Polling is the same as SPC read. The byte being written is read and bit 23 (representing I/O_7) will be the complement of the most significant data bit until the write cycle is completed. (After completion of the write cycle, bit 23 will show true data.)

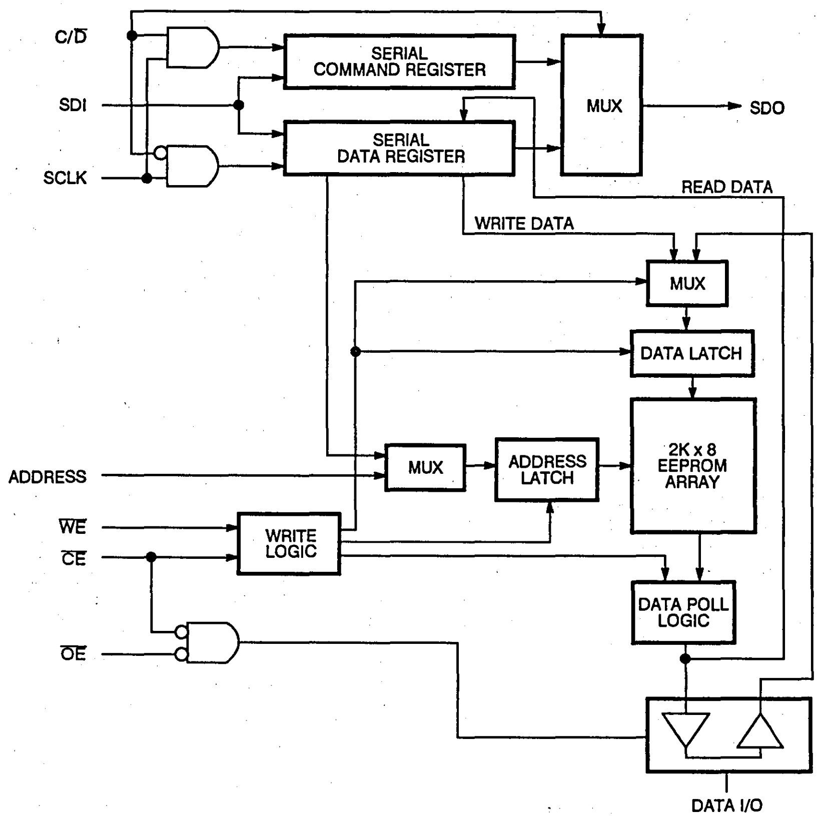
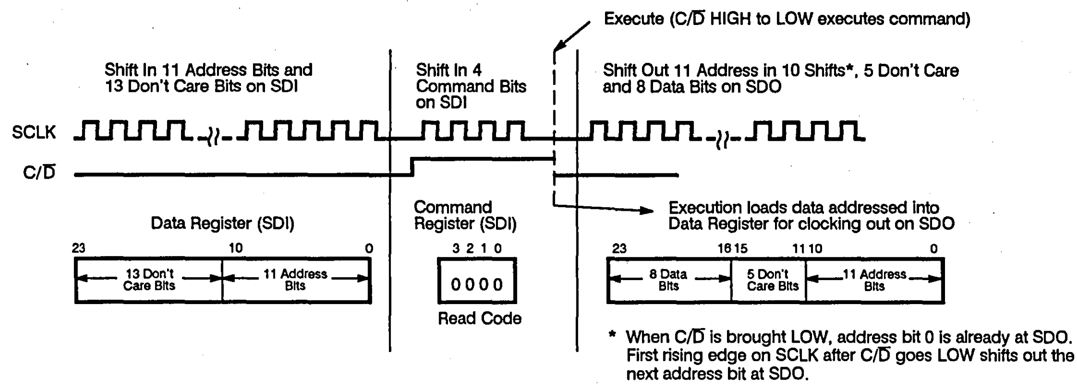
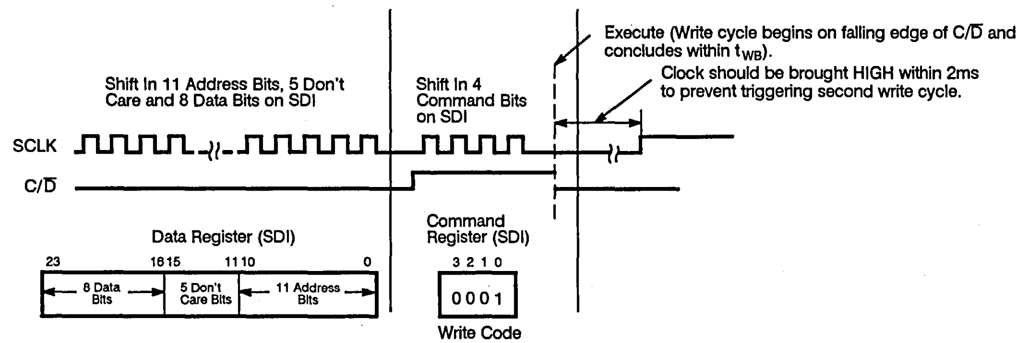


Figure 1. Detailed SPC Block Diagram

To Read Data Out:



To Write Data In:



ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ENDURANCE

PARAMETER	VALUE	UNIT
Minimum Endurance	10,000	Cycles/Byte

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-0.3	0.4	0.8	V
V_{WI}	Write Inhibit	3.8	–	–	V

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 5.0V)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:
T_A = 0°C to +70°C V_{CC} = 5.0V ±10% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ±10% (Military)
V_{LC} = 0.2V V_{HC} = V_{CC} - 0.2V
C_L = 30pF

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	–	10	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	–	10	µA
I_{CC1}	Operating Power Supply Current V_{CC} = Max., f = 0	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	–	125	mA
I_{CC2}	Dynamic Operating Current V_{CC} = Max., f = f_{MAX}	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	–	125	mA
I_{SB}	Standby Power Supply Current (TTL Level)	$\overline{CE} \geq V_{IH}$, V_{CC} = Max., $I_{I/O}$ = 0mA $V_{IN} \geq V_{IH}$ or $0 \leq V_{IN} \leq V_{IL}$	–	20	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level)	$\overline{CE} \geq V_{HC}$, V_{CC} = Max., $I_{I/O}$ = 0mA $V_{IN} \geq V_{CC}$ -0.2V or $0 \leq V_{IN} \leq 0.2V$	–	0.9	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2mA	2.4	–	V

12

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges; C_L = 30pF)

SYMBOL	PARAMETER	COM'L. ONLY IDT78C18A70 MIN.	MAX.	COMMERCIAL/MILITARY IDT78C18A75[2]/90 MIN.	MAX.	IDT78C18A100/120 MIN.	MAX.	IDT78C18A150/200 MIN.	MAX.	UNIT
READ CYCLE										
t_{CE}	Chip Enable Access Time	–	70	–	75/90	–	100/120	–	150/200	ns
t_{AA}	Address Access Time	–	70	–	75/90	–	100/120	–	150/200	ns
t_{OE}	Output Enable to Output Valid	–	50	–	50/60	–	65/70	–	70	ns
t_{CLZ}	Chip Enable to Output in Low Z[1]	5	–	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z[1]	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Disable to Output in High Z[1]	0	20	0	20/30	0	20/30	0	20/30	ns
t_{OHZ}	Output Disable to Output in High Z[1]	0	20	0	20/30	0	20/30	0	20/30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	ns

NOTES:
1. This parameter is guaranteed but not tested.
2. Military temperature range only.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges; C_L = 30pF)

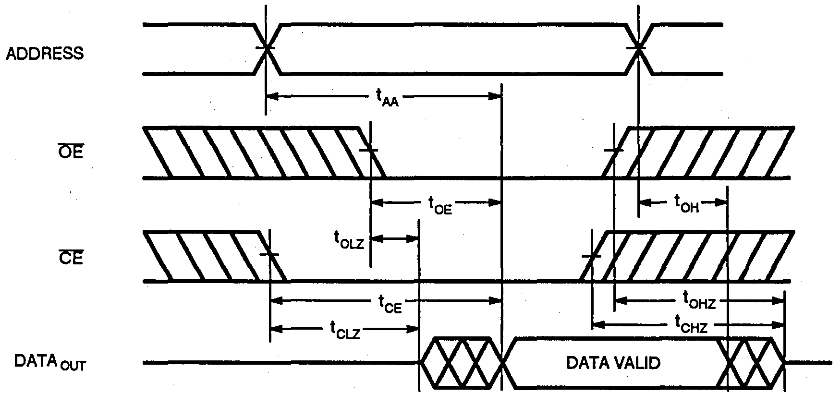
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
WRITE CYCLE				
t_{AS}	Address Set-up Time	5	–	ns
t_{AH}	Address Hold Time	50	–	ns
t_{DS}	Data Set-up Time	20	–	ns
t_{DH}	Data Hold from Write Time	15	–	ns
t_{OES}	Output Enable Set-up Time	5	–	ns
t_{OEH}	Chip Enable Hold from Write Time	15	–	ns
t_{CES}	Chip Enable Set-up Time	0	–	ns
t_{CEH}	Chip Enable Hold Time	0	–	ns
t_{WP}	Write Pulse Width	50	–	ns
t_{WB}	Byte Write Cycle	–	10	ms
t_{DBV}	$\overline{\text{DATA}}$ Polling to $\overline{\text{DATA}}$ Valid	–	t_{OE}	
t_{WH}	Write Hold Time	15	–	ns
t_{DP}	End of Write Pulse to $\overline{\text{DATA}}$ Polling	15	–	ns
t_{WES}	Write Enable Set-up Time	0	–	ns
t_{WEH}	Write Enable Hold Time	0	–	ns
t_{DV}	Data Valid Time[1, 2]	–	1	µs

NOTES:
1. Data must be valid within 1µs maximum and must remain valid if t_{WP} is longer than 1µs.
2. This parameter is guaranteed but not tested.

AC TEST CONDITIONS

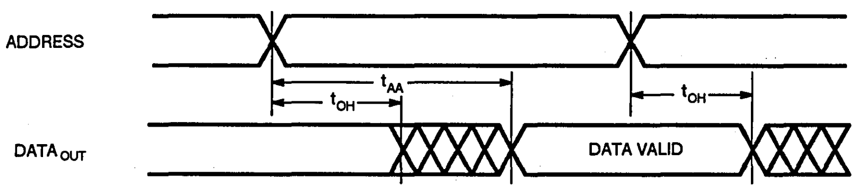
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



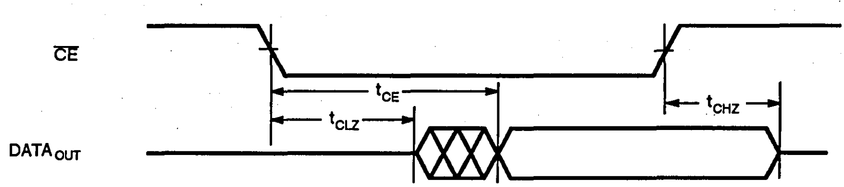
NOTE:
1. $\overline{WE}$ is HIGH for Read Cycle.

TIMING WAVEFORM OF READ CYCLE NO. 2[1]



NOTE:
1. $\overline{WE}$ is HIGH; $\overline{CE} = V_{IL}$; $\overline{OE} = V_{IL}$

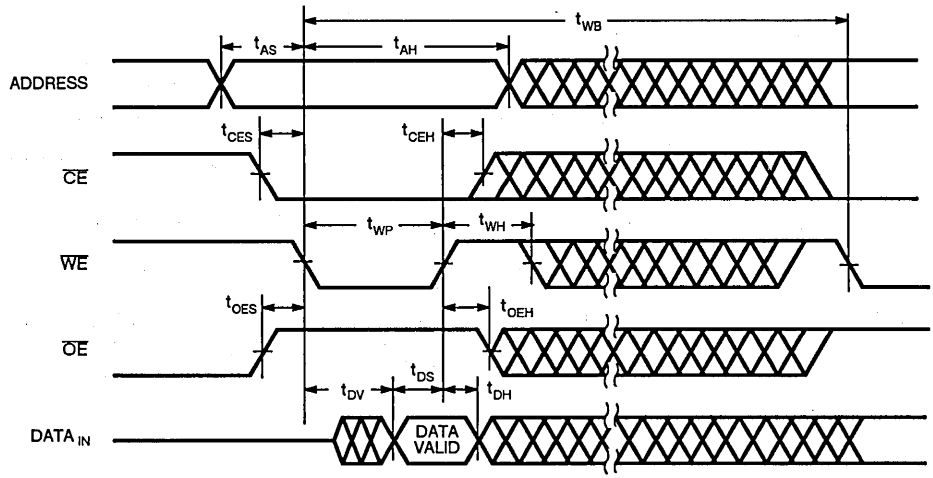
TIMING WAVEFORM OF READ CYCLE NO. 3[1]



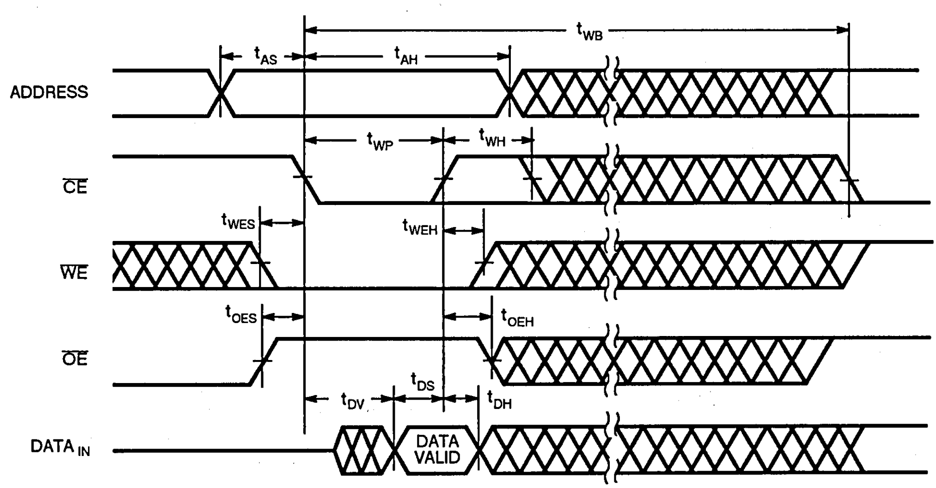
NOTE:
1. $\overline{WE}$ is HIGH; $\overline{OE} = V_{IL}$; address valid prior to or coincident with $\overline{CE}$ transition LOW.

12

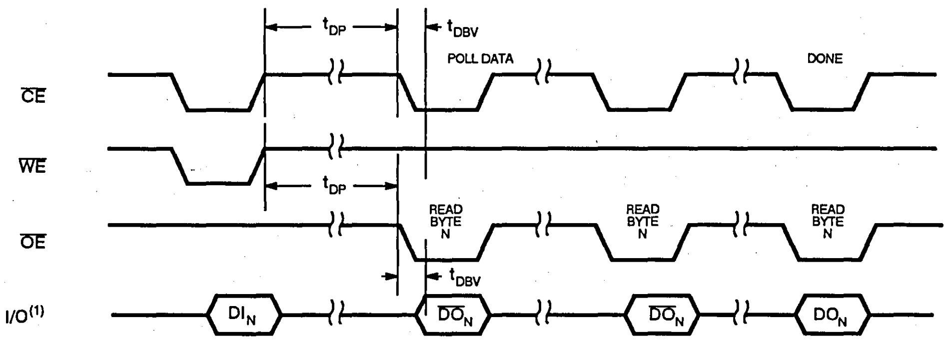
TIMING WAVEFORM OF WRITE CYCLE NO. 1, $\overline{WE}$ CONTROLLED



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED



$\overline{\text{DATA}}$ POLLING

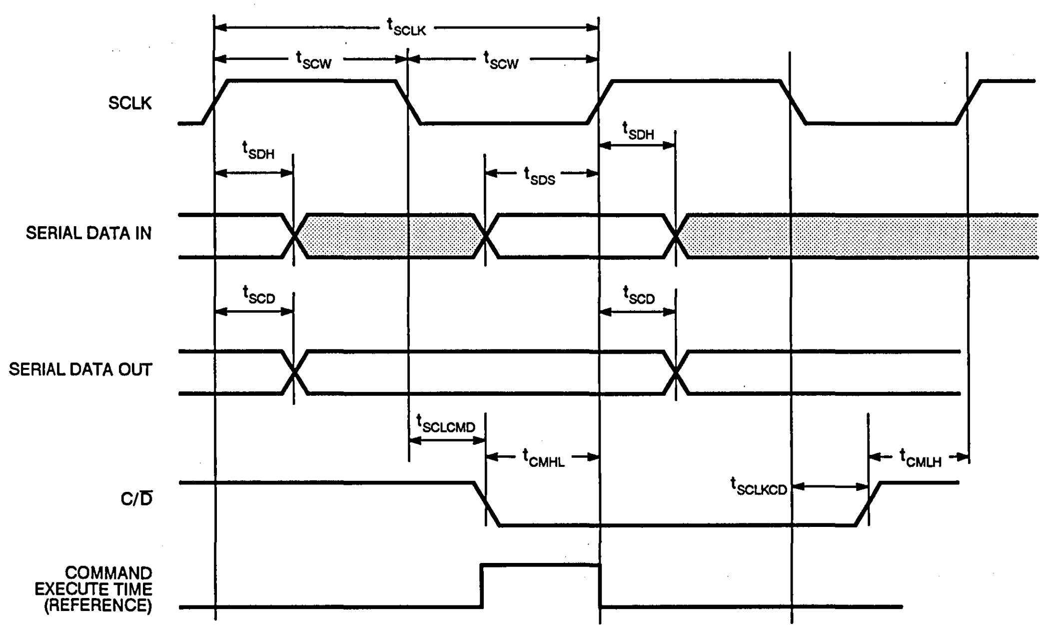


NOTE:
1. Most significant bit of the byte being written is inverted and available at I/O_7 if a Read command is issued. All other outputs are high impedance at this time. True data will not be released until the Write cycle is completed.

SPC AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±10%, All Temperature Ranges

SYMBOL	PARAMETER		COMMERCIAL[1] MIN.	COMMERCIAL[1] MAX.	MILITARY[1] MIN.	MILITARY[1] MAX.	UNIT
t_{SCLK}	SCLK Period		100	–	100	–	ns
t_{SCW}	SCLK Pulse Width		50	–	50	–	ns
t_{SDS}	Serial Data Set-up Time		15	–	15	–	ns
t_{SDH}	Serial Data Hold Time		5	–	5	–	ns
t_{SCD}	Clock to Serial Data Output Delay		4	25	4	25	ns
t_{SCLCMD}	Clock to Command Set-up Time[3]		50	–	50	–	ns
t_{CMLH}	Command/Data Set-up Time, LOW to HIGH		50	–	50	–	ns
t_{CMHL}	Command Set-up Time, HIGH to LOW (Execution Time)[4]	Read Cycle	t_{AA}	–	t_{AA}	–	ns
		Write/Erase Cycle	100	2(10)[6]	100	2(10)[6]	
t_{SCLKCD}	Clock LOW to C/$\overline{D}$ HIGH		0	–	0	–	ns

NOTES:
1. These specifications apply to all speed grades of the product.
2. This parameter guaranteed but not tested.
3. C/$\overline{D}$ cannot change while clock is high.
4. During a write/erase cycle SCLK should be brought HIGH within 2ms to prevent triggering another write/erase cycle.



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

ORDERING INFORMATION

IDT XXXXX (Device Type) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

TD	THINDIP (CERDIP)
L	Leadless Chip Carrier

Speed (Speed in Nanoseconds)

70	Commercial Only
75	Military Only
90	
100	
120	
150	
200	

Device Type

78C18A	16K (2K x 8-Bit) EEPROM with SPC

12

Integrated Device Technology, Inc.

64K (8K x 8) CMOS EEPROM MODULE

IDT78M64

FEATURES:

- Equivalent to JEDEC standard 8K x 8 monolithic EEPROM
- 8,192 x 8 CMOS EEPROM module complete with decoder and decoupling capacitor
- Fast access times
  - Military: 85ns (max.)
  - Commercial: 70ns (max.)
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ns max.
- $\overline{\text{DATA}}$ Polling—detection of write cycle completion
- Utilizes IDT78C16As—high-performance 16K EEPROMs
- Single 5V (±10%) power supply
- Data protection circuitry (V_{CC} lockout for V_{CC} < 3.8V)
- Provides data integrity on power up/power down
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- Available in 28-pin, 600 mil DIP
- Military modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

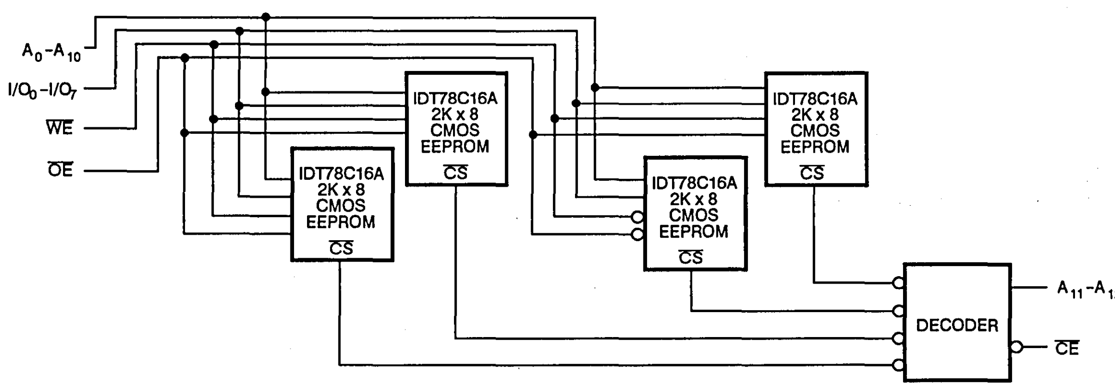
The IDT78M64 is a 5 volt only 8K x 8 Electrically Erasable Programmable Read-Only Memory (EEPROM) constructed on a co-fired ceramic substrate using four IDT78C16A (2K x 8) EEPROMs in leadless chip carriers. Functional equivalence to monolithic 64K EEPROMs is achieved by utilization of an on-board decoder circuit that interprets the higher order address A_{11} and A_{12} to select one of the four 2K x 8 EEPROMs.

The IDT78M64 offers a reduced power standby mode. When $\overline{CE}$ goes HIGH, the circuit will automatically go to, and remain in, a standby mode as long as these conditions are held. In standby mode, the module consumes less than 440mW. Substantially lower power levels can be achieved in the I_{SB1} mode (less than 20mW max.).

The pinout of the IDT78M64 is equivalent to monolithic 64K EEPROMs. Its fast read access time allows zero wait state read cycles with high-performance microprocessors.

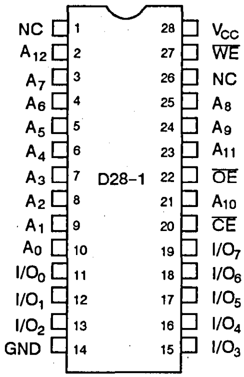
All IDT module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW

DEVICE OPERATIONAL MODE [1]

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0 – I/O_7
Read	V_{IL}	V_{IL}	V_{IH}	$DATA_{OUT}$ (O_0 - O_7)
Byte Write	V_{IL}	V_{IH}	V_{IL}	$DATA_{IN}$ (I_0 - I_7)
Standby	V_{IH}	Don't Care	Don't Care	High Z
Write Inhibit	Don't Care	V_{IL}	Don't Care	High Z
	Don't Care	Don't Care	V_{IH}	High Z

NOTE:
1. All control inputs are TTL-compatible.

PIN NAMES

A_0 – A_{12}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O_0 – I/O_7	Data Input (I_0 – I_7) during write; Data Output (O_0 – O_7) during read

READ MODE

Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) must be logically active in order for data to be available at the outputs. After a selected byte address is stable, $\overline{CE}$ is taken to a TTL LOW (enabling chip). The Write Enable ($\overline{WE}$) pin should remain deselected (TTL HIGH) during the entire read cycle. Data is gated from the device outputs by selecting the $\overline{OE}$ pin (TTL LOW).

WRITE MODE

The IDT78M64 is programmed electrically in-circuit and does not require any external latching, erasing or timing. Writing to the IDT78M64 is as easy as writing to a static RAM. When a write cycle is initiated the device automatically latches the address, data and control signals as it begins its write operation.

A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The IDT78M64 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. All inputs, except for data, are latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Data is then latched in by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurred first. An automatic byte erase of the existing data at the addressed location is performed before the new data byte is written. Once initiated, a byte write operation will automatically proceed to completion within 10ms.

STANDBY MODE

The IDT78M64 features a standby mode which reduces the maximum active current from 250mA to 80mA for TTL levels and to 4mA for CMOS levels. With $\overline{CE} \geq V_{IH}$, all outputs are in the high impedance state.

DATA PROTECTION

Nonvolatile data is protected from inadvertent writes in the following manner:

Power Up/Down

On-chip circuitry provides protection against false write during V_{CC} power up/down. The IDT78M64 features an internal sensing circuit that disables the internal programming circuit if $V_{CC} < 3.8V$. This prevents input signals at $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ from triggering a write cycle during a V_{CC} power up/down event.

Noise Protection

The IDT78M64 will typically reject write pulses that are less than 15ns. This prevents the initiation of a write cycle by a noise occurence.

Write Inhibit

Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during a power-on and power-off will inhibit inadvertent writes.

$\overline{\text{DATA}}$ POLLING

The IDT78M64 has a maximum write cycle time of 10ms; a write will always be completed in less than the maximum cycle time. Write cycle completion is readily determined via a simple software routine ($\overline{\text{DATA}}$ Polling) that performs a read operation while the device is in an automatic write mode. If a read command (addressed to the last byte written) is given while the IDT78M64 is still writing, the inverse of the most significant bit (I/O_7 pin) of the last byte written will be present. True data is not released until the write cycle is completed. Thus, a $\overline{\text{DATA}}$ polling monitor of the output (or periodic read of the last written byte) for true data can be used to detect early completion of a write cycle.

ENDURANCE

IDT's EEPROM technology employs the industry accepted Fowler-Nordheim tunneling across a thin oxide. IDT78M64 EEPROM modules are designed and tested for applications requiring extended endurance.

The endurance failure mechanism associated with EEPROMs results from the charge trapping in the thin tunneling dielectric. This failure is a function of the number of write cycles that each byte in the part has experienced. Trapped charges accumulate slowly with each write cycle and eventually become large enough to prevent reliable writing to the cell. Since some bits may be more sensitive than others, an endurance failure is typically a single bit failure (i.e. a failure of a single bit to properly write or retain data).

To test for endurance, a sample of devices is written 10,000 times at every byte location and checked for data retention capability. IDT test screens ensure that shipped devices will write a minimum of 10,000 times (at every byte location) with a maximum failure rate of 1%. This means that up to 1% of a sample of devices will fail to write or retain data after being written to 10,000 times. Those devices that do fail typically have a single bit(s) that fails to retain data after being written.

For more detailed information please refer to the *IDT Reliability Report on Endurance*.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ENDURANCE

PARAMETER	VALUE	UNIT
Minimum Endurance	10,000	Cycles/Byte

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-0.3	0.4	0.8	V
V_{WI}	Write Inhibit	3.8	–	–	V

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 5.0V)

SYMBOL	PARAMETER [1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	28	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	33	pF

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified

T_A = 0°C to +70°C V_{CC} = 5.0V ± 10% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V V_{HC} = V_{CC} -0.2V
C_L = 30pF

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	–	15	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	–	15	µA
I_{CC1}	Operating Power Supply Current V_{CC} = Max., f = 0	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	–	250	mA
I_{CC2}	Dynamic Operating Current V_{CC} = Max., f = f_{MAX}	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	–	250	mA
I_{SB}	Standby Power Supply Current (TTL Level)	$\overline{CE} \geq V_{IH}$, V_{CC} = Max., $I_{I/O}$ = 0mA $V_{IN} \geq V_{IH}$ or $0 \leq V_{IN} \leq V_{IL}$	–	80	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level)	$\overline{CE} \geq V_{HC}$, V_{CC} = Max., $I_{I/O}$ = 0mA $V_{IN} \geq V_{CC}$ -0.2V or $0 \leq V_{IN} \leq 0.2V$	–	4.0	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	–	V

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, C_L = 30pF)

SYMBOL	PARAMETER	MILITARY ONLY												UNIT
		78M6485/100		78M64120/150		78M64200		78M64250		78M64300		78M64350		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{CE}	Chip Enable Access Time	–	85/100	–	120/150	–	200	–	250	–	300	–	350	ns
t_{AA}	Address Access Time	–	85/100	–	120/150	–	200	–	250	–	300	–	350	ns
t_{OE}	Output Enable to Output Valid	–	60/65	–	70	–	70	–	70	–	70	–	70	ns
t_{CLZ}	Chip Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Disable to Output in High Z	0	30	0	30	0	30	0	30	0	30	0	30	ns
t_{OHZ}	Output Disable to Output in High Z	0	30	0	30	0	30	0	30	0	30	0	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, C_L = 30pF)

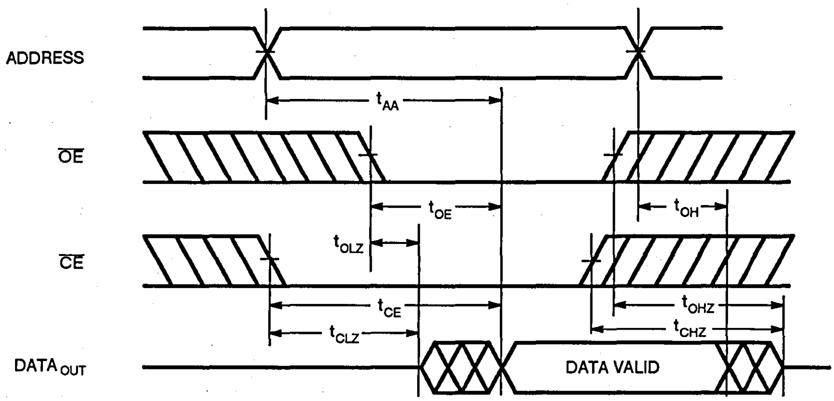
SYMBOL	PARAMETER	COMMERCIAL ONLY												UNIT
		78M6470		78M6485		78M64100		78M64120		78M64150		78M64200		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{CE}	Chip Enable Access Time	–	70	–	85	–	100	–	120	–	150	–	200	ns
t_{AA}	Address Access Time	–	70	–	85	–	100	–	120	–	150	–	200	ns
t_{OE}	Output Enable to Output Valid	–	50	–	60	–	65	–	70	–	70	–	70	ns
t_{CLZ}	Chip Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Disable to Output in High Z	0	20	0	20	0	20	0	20	0	20	0	20	ns
t_{OHZ}	Output Disable to Output in High Z	0	20	0	20	0	20	0	20	0	20	0	20	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges; C_L = 30pF)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
WRITE CYCLE				
t_{AS}	Address Set-up Time	5	–	ns
t_{AH}	Address Hold Time	50	–	ns
t_{DS}	Data Set-up Time	20	–	ns
t_{DH}	Data Hold from Write Time	15	–	ns
t_{OES}	Output Enable Set-up Time	5	–	ns
t_{OEH}	Chip Enable Hold from Write Time	15	–	ns
t_{CES}	Chip Enable Set-up Time	0	–	ns
t_{CEH}	Chip Enable Hold Time	0	–	ns
t_{WP}	Write Pulse Width	50	–	ns
t_{WB}	Byte Write Cycle	–	10	ms
t_{DBV}	$\overline{\text{DATA}}$ Polling to $\overline{\text{DATA}}$ Valid	–	t_{OE}	
t_{WH}	Write Hold Time	15	–	ns
t_{DP}	End of Write Pulse to $\overline{\text{DATA}}$ Polling	15	–	ns
t_{WES}	Write Enable Set-up Time	0	–	ns
t_{WEH}	Write Enable Hold Time	0	–	ns
t_{DV}	Data Valid Time	–	1	μs

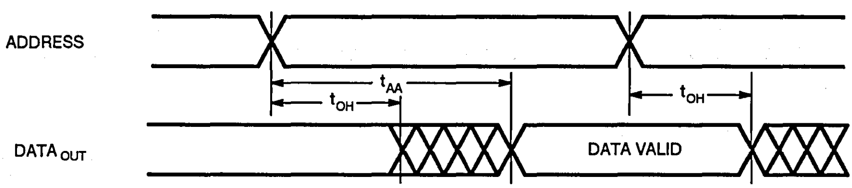
NOTES:
1. Data must be valid within 1μs maximum and must remain valid if t_{WP} is longer than 1μs.
2. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



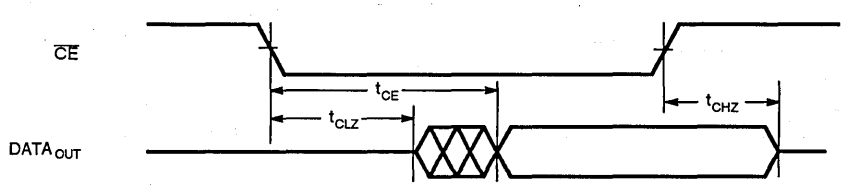
NOTE:
1. $\overline{WE}$ is HIGH for Read Cycle.

TIMING WAVEFORM OF READ CYCLE NO. 2[1]



NOTE:
1. $\overline{WE}$ is HIGH; $\overline{CE} = V_{IL}$; $\overline{OE} = V_{IL}$

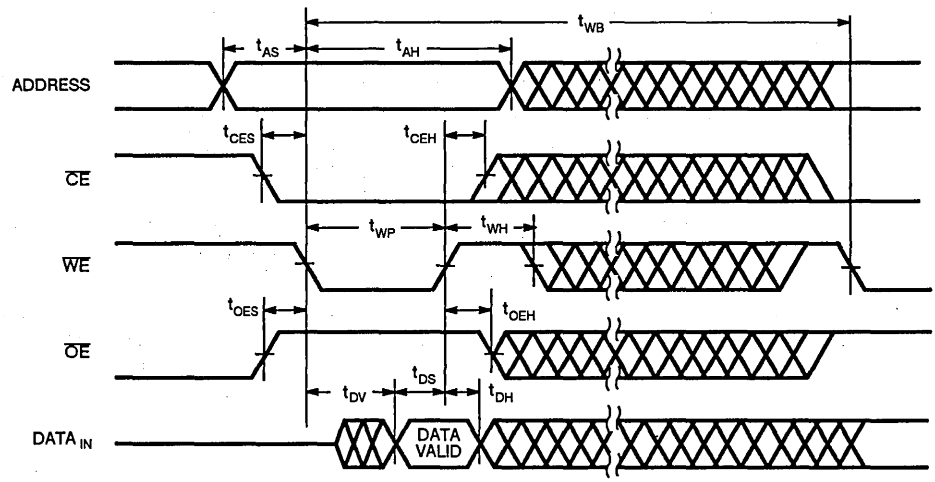
TIMING WAVEFORM OF READ CYCLE NO. 3[1]



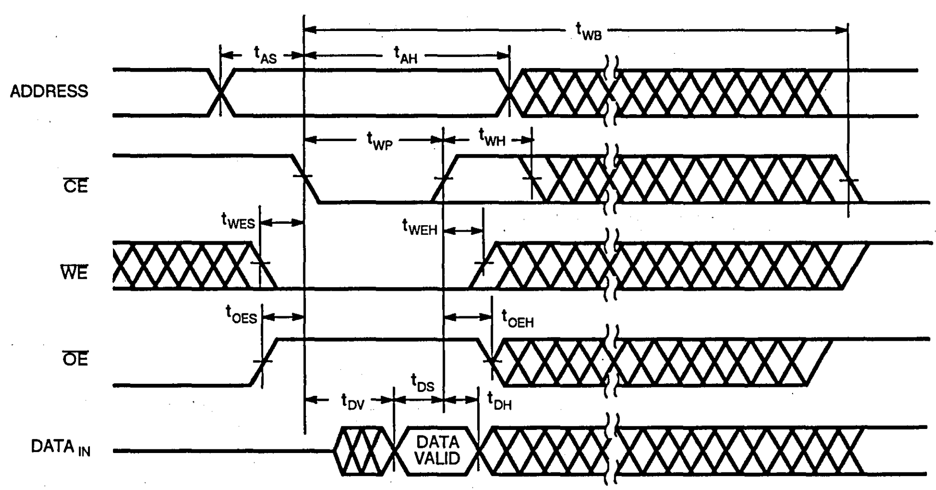
NOTE:
1. $\overline{WE}$ is HIGH; $\overline{OE} = V_{IL}$; address valid prior to or coincident with $\overline{CE}$ transition LOW.

12

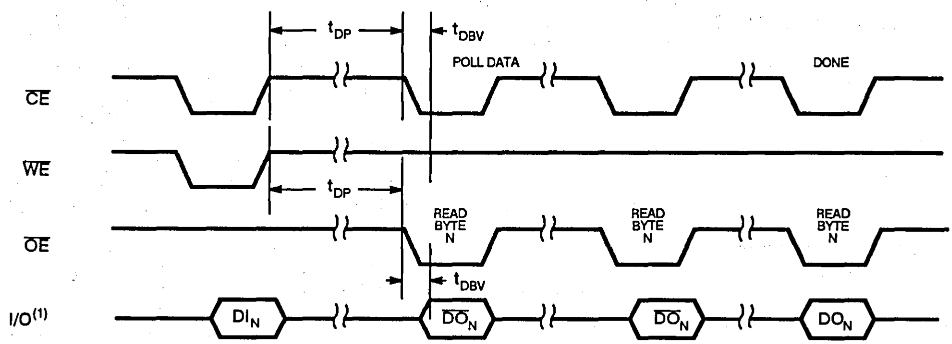
TIMING WAVEFORM OF WRITE CYCLE NO. 1, $\overline{WE}$ CONTROLLED



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED



$\overline{\text{DATA}}$ POLLING



NOTE:
1. Most significant bit of the byte being written is inverted and available at I/O_7 if a Read command is issued. All other outputs are high impedance at this time. True data will not be released until the Write cycle is completed.

ORDERING INFORMATION

IDT XXXXX (Device Type) XX (Power) XXX (Speed) XX (Package) X (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	D	CERDIP
Speed	70	Commercial Only
	85	
	100	
	120	
	150	
	200	
	250	Military Only
	300	Military Only
	350	Military Only
Power	S	Standard Power
Device Type	78M64	64K (8K x 8-Bit) EEPROM Module

Speed in Nanoseconds

12

Integrated Device Technology, Inc.

FAST CMOS EEPROM 64K (8K x 8-BIT)

ADVANCE INFORMATION IDT78C64A

FEATURES:

- 5 volt only operation
- Fast access times
  - Military: 70ns (max.)
  - Commercial: 55ns (max.)
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ms max.
- $\overline{\text{DATA}}$ Polling—detection of write cycle completion
- 64-byte page write operation, page write 10ms max.
- Low-power CEMOS™ technology
  - Active Current: 100mA
  - Standby Current (full CMOS): 0.9mA
- Data protection circuitry (V_{CC} lockout for V_{CC} < 3.8V) provides data integrity on power up/power down
- Software write protection
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- JEDEC approved byte-wide pinout
- Available in 28-pin DIP and 32-pin LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

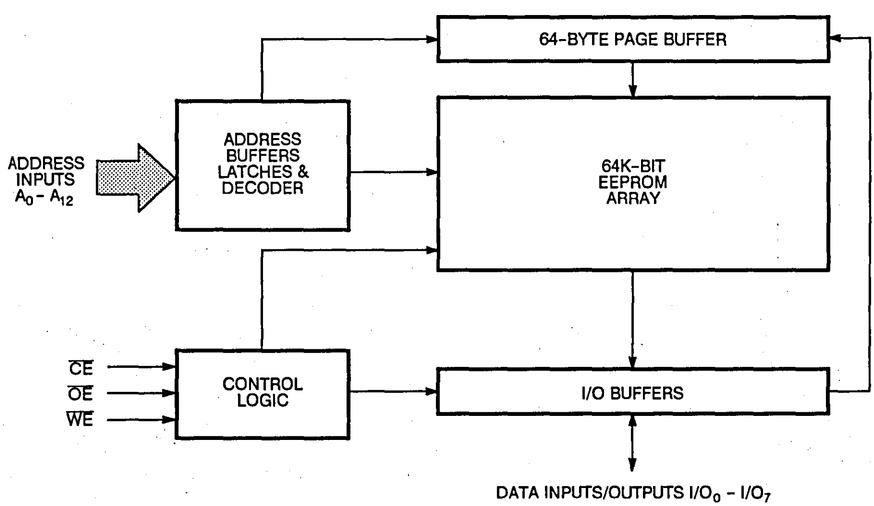
The IDT78C64A is a 5 volt only 8K x 8 Electrically Erasable Programmable Read-Only Memory (EEPROM). Fabricated using IDT's CEMOS™ process, this EEPROM provides 64K bits of non-volatile data storage (data retention in excess of 100 years).

The IDT78C64A features fast read access times, allowing zero wait state read cycles with high-performance microprocessors. Write time is automatically timed out by an internal timer and input latches secure address/data information, freeing the host system for other tasks during a write cycle. A 64-byte page mode allows 1 to 64 bytes to be written within a single write cycle, to minimize total write time. The $\overline{\text{DATA}}$ Polling method for determining write cycle completion is supported by the IDT78C64A. Data protection features include V_{CC} lockout, write inhibit, noise protection for the $\overline{\text{WE}}$ pin and software write protection.

The IDT78C64A is function- and pinout-compatible with the IDT7164, 8K x 8 static RAM. It is ideal for systems requiring non-volatility and in-system data modifications.

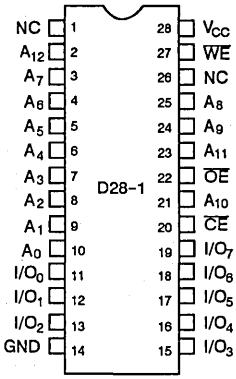
The IDT78C64A Military EEPROM is manufactured in compliance to the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

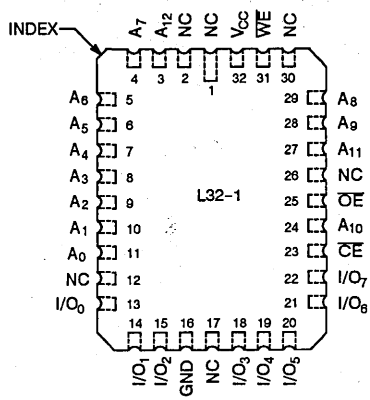


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

DEVICE OPERATIONAL MODE [1]

PIN / MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_7$
Read	V_{IL}	V_{IL}	V_{IH}	$DATA_{OUT}$ $(O_0 - O_7)$
Byte Write	V_{IL}	V_{IH}	V_{IL}	$DATA_{IN}$ $(I_0 - I_7)$
Standby	V_{IH}	Don't Care	Don't Care	High Z
Write Inhibit	Don't Care	V_{IL}	Don't Care	High Z
	Don't Care	Don't Care	V_{IH}	High Z

NOTE:
1. All control inputs are TTL-compatible.

PIN NAMES

$A_0 - A_{12}$	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$I/O_0 - I/O_7$	Data Input $(I_0 - I_7)$ During Write; Data Output $(O_0 - O_7)$ During Read

12

FAST CMOS REGISTERED EEPROM 64K (8K x 8-BIT)

ADVANCE INFORMATION
IDT78C464A

Integrated Device Technology, Inc.

FEATURES:

- 5 volt only operation
- Fast access times
  - Military: 70ns (max.)
  - Commercial: 55ns (max.)
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ms max.
- $\overline{\text{DATA}}$ Polling—detection of write cycle completion
- 64-byte page write operation, page write 10ms max.
- On-chip edge triggered registers
- Synchronous and asynchronous output enable
- Programmable asynchronous register ($\overline{\text{INIT}}$)
- Low-power CEMOS™ technology
  - 100mA active current
- Data protection circuitry (V_{CC} lockout for $V_{CC} < 3.8V$) provides data integrity on power up/power down
- Software write protection
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- 28-pin Dip, 32-pin LCC
- Military product compliant to MIL-STD-883, Class B

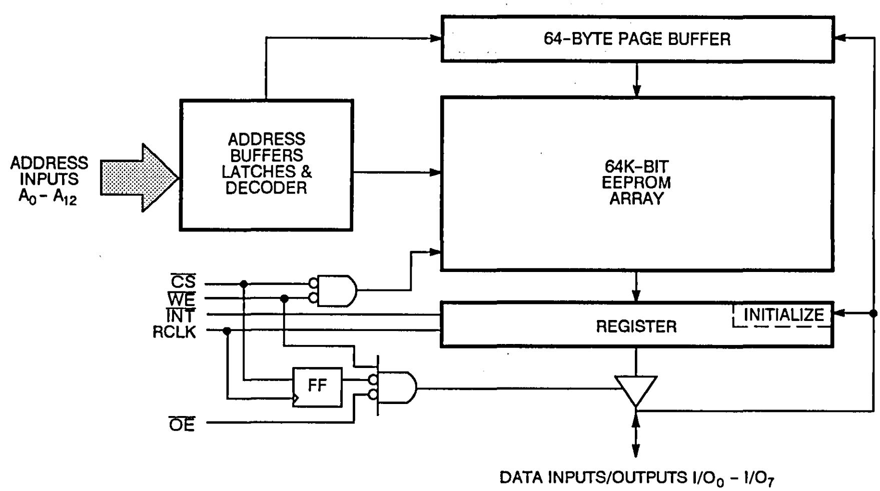
DESCRIPTION:

The IDT78C464A is a 5 volt only 8K x 8 Registered Electrically Erasable Programmable Read-Only Memory (Registered EEPROM). Fabricated in IDT's CEMOS process, this Registered EEPROM provides 64K bits of non-volatile data storage (data retention in excess of 100 years).

The IDT78C464A features fast read access times, allowing zero wait state read cycles with high-performance microprocessors. Write time is automatically timed out by an internal timer and input latches secure address/data information, freeing the host system for other tasks during a write cycle. A 64-byte page mode allows one to 64 bytes to be written within a single write cycle to minimize total write time. The $\overline{\text{DATA}}$ Polling method for determining write cycle completion is supported by the IDT78C464A. Data protection features include V_{CC} lock-out, write inhibit, noise protection for the $\overline{\text{WE}}$ pin and software write protection.

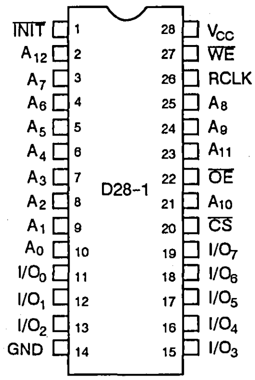
The IDT78C464A has an initialize function ($\overline{\text{INIT}}$) which activates an 8-bit word loaded into the on-chip Initialize register. This registered word is user-programmable with any desired word (i.e. can be used to establish a PRESET or CLEAR word on the outputs). The IDT78C464A Military EEPROM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

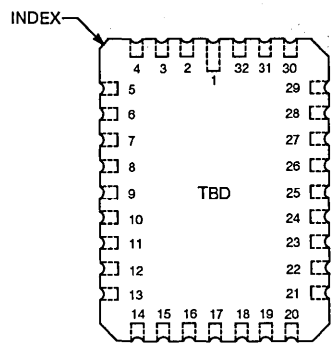


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

DEVICE OPERATIONAL MODES [1]

MODE \ PIN	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	RCLK	I/O_0 - I/O_7
Deselected	H	X	L	↑	High Z
Read	X	H	H	X	High Z
Read	H	H	L	↑	High Z
Read	L	H	L	↑	Data Out at Addresses
Write	L	L	X	X	Data In at Addresses

NOTE:
1. "X" = Don't Care

PIN NAMES

A_0 - A_{12}	Addresses
$\overline{CS}$	Synchronous Output Enable/ Chip Enable (Write)
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O_0 - I/O_7	Data Input (I_0 - I_7) During Write; Data Output (O_0 - O_7) During Read
$\overline{INIT}$	Initialize
RCLK	Register Clock

12

FAST CMOS REGISTERED EEPROM WITH SPC™ 64K (8K x 8-BIT)

ADVANCE INFORMATION
IDT78C564A

Integrated Device Technology, Inc.

FEATURES:

- 5 volt only operation
- Fast access times
  - Military: 70ns (max.)
  - Commercial: 55ns (max.)
- Serial Protocol Channel (SPC) allows load and read-out of the memory array over a 4-wire channel
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ms max.
- $\overline{\text{DATA}}$ Polling—detection of write cycle completion
- 64-byte page write operation, page write 10ms max.
- On-chip edge triggered registers
- Programmable asynchronous register ($\overline{\text{INIT}}$)
- Low-power CEMOS™ technology
  - Active Current: 100mA
- Data protection circuitry (V_{CC} lockout for V_{CC} < 3.8V) provides data integrity on power up/power down
- Software write protection
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

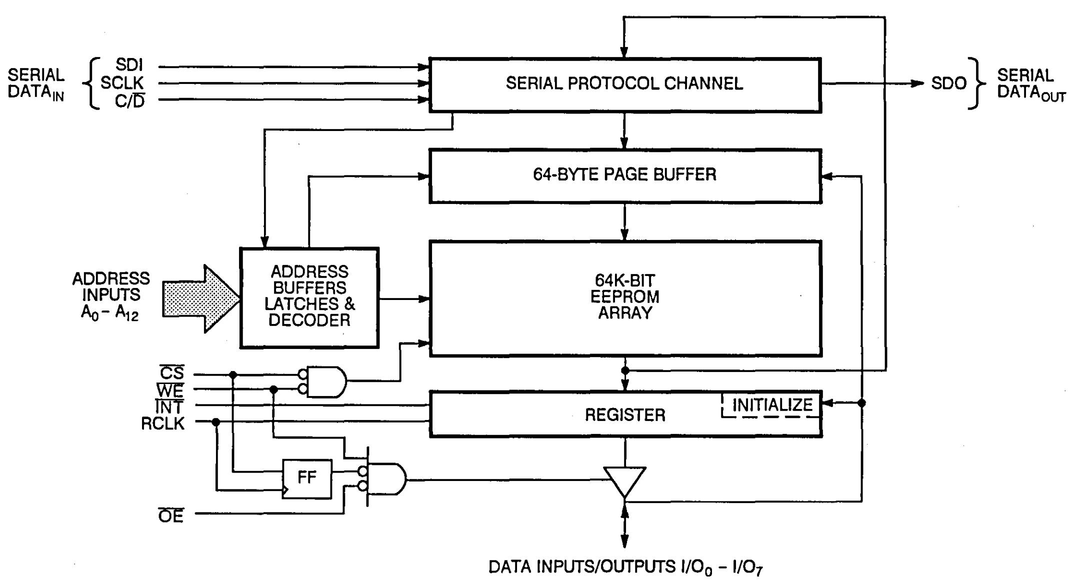
The IDT78C564A is a 5 volt only 8K x 8 Registered Electrically Erasable Programmable Read-Only Memory (Registered EEPROM) with Serial Protocol Channel (SPC). SPC complements the EEPROM's parallel information path by providing a serial link (four additional pins) by which its memory array can be written or read. Fabricated using IDT's CEMOS™ process, this EEPROM provides 64K bits of non-volatile data storage (data retention in excess of 100 years).

The IDT78C564A features fast read access times, allowing zero wait state cycles with high-performance microprocessors. Write time is automatically timed out by an internal timer and input latches secure address/data information, freeing the host system for other tasks during a write cycle. A 64-byte write page buffer allows 1 to 64 bytes to be written within a single write cycle to minimize total write time. The $\overline{\text{DATA}}$ Polling method for determining completion of the write cycle is supported by the IDT78C564A. Data protection features include V_{CC} lockout, write inhibit, noise protection for the $\overline{\text{WE}}$ pin and software write protection.

The IDT78C564A is ideal for systems requiring nonvolatility and in-system data modifications. With SPC, a serial link can be established during board layout for easy field updates of code changes. The initialize function ($\overline{\text{INIT}}$) can be used to activate an 8-bit word loaded into the on-chip Initialize register. This registered word is user-programmable with any desired word.

The IDT78C564A Military EEPROM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS and SPC are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

(CONSULT FACTORY)

DEVICE OPERATIONAL MODES[1]

PIN / MODE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{RCLK}$	$I/O_0 - I/O_7$
Deselected	H	X	L	$\uparrow$	High Z
Read	X	H	H	X	High Z
Read	H	H	L	$\uparrow$	High Z
Read	L	H	L	$\uparrow$	Data Out at Addresses
Write	L	L	X	X	Data In at Addresses

NOTE:
1. X = Don't Care

PIN NAMES

$A_0 - A_{12}$	Addresses
$\overline{CS}$	Synchronous Output Enable/Chip Enable (Write)
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$I/O_0 - I/O_7$	Data Input ($I_0 - I_7$) During Write; Data Output ($O_0 - O_7$) During Read
SDI	Serial Data Input
SDO	Serial Data Output
SCLK	Data Clock Input
$C/\overline{D}$	Command/$\overline{\text{Data}}$
$\overline{INIT}$	Initialize
RCLK	Register Clock

SPC OPERATIONAL MODES[1]

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$C/\overline{D}$	SCLK	FUNCTION
Command	X	X	X	H	$\uparrow$	Shift bit into command register
Data	X	X	X	L	$\uparrow$	Shift bit into data register
Execute	X	X	X	$\uparrow$	$\uparrow$	Execute command during time between $C/\overline{D}$ and SCLK

NOTE:
1. X = Don't Care

Integrated Device Technology, Inc.

FAST CMOS EEPROM 256K (32K x 8-BIT)

ADVANCE INFORMATION
IDT78C256A

FEATURES:

- 5 volt only operation
- Fast access times
  - Military: 70ns (max.)
  - Commercial: 55ns (max.)
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ms max.
- $\overline{\text{DATA}}$ Polling—detection of write cycle completion
- 64-byte page write operation (page write 10ms max.)
- Low-power CEMOS™ technology
  - Active Current: 100mA
  - Standby Current (full CMOS): 0.9mA
- Data protection circuitry (V_{CC} lockout for V_{CC} < 3.8V) provides data integrity on power up/power down
- Software write protection
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- JEDEC approved byte wide pinout
- Available in 28-pin DIP and 32-pin LCC
- Military product compliant to MIL-STD-883, Class B

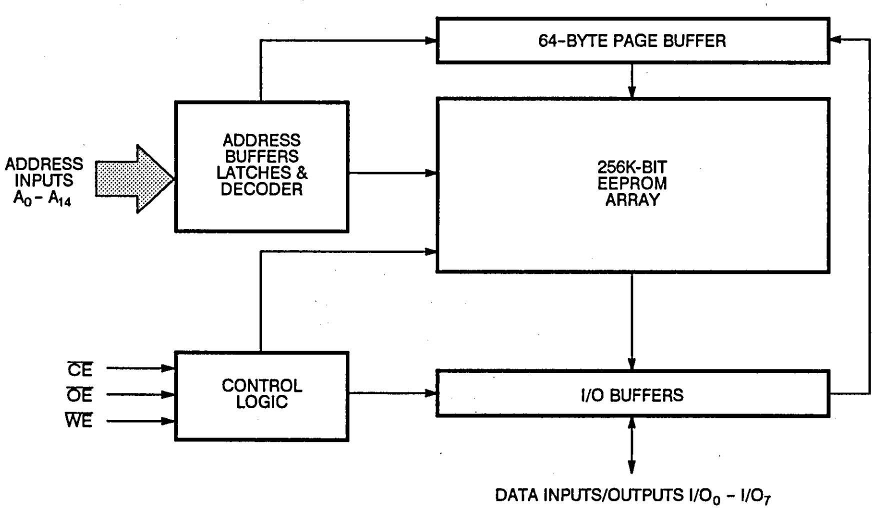
DESCRIPTION:

The IDT78C256A is a 5 volt only 32K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). Fabricated using IDT's CEMOS process, this EEPROM provides 256K bits of non-volatile data storage (data retention in excess of 100 years).

The IDT78C256A features fast read access times allowing zero wait state read cycles with high-performance microprocessors. Write time is automatically timed out by an internal timer and input latches secure address/data information, freeing the host system for other tasks during a write cycle. A 64-byte page mode allows 1 to 64 bytes to be written within a single write cycle to minimize total write time. The $\overline{\text{DATA}}$ Polling method for determining write cycle completion is supported by the IDT78C256A. Data protection features include V_{CC} lockout, write inhibit, noise protection for the $\overline{\text{WE}}$ pin and software write protection.

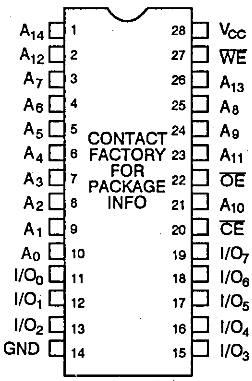
The IDT78C256A is function and pinout compatible with the IDT71256, 32K x 8 static RAM. It is ideal for systems requiring non-volatility and in-system data modifications. The IDT78C256 military EEPROM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

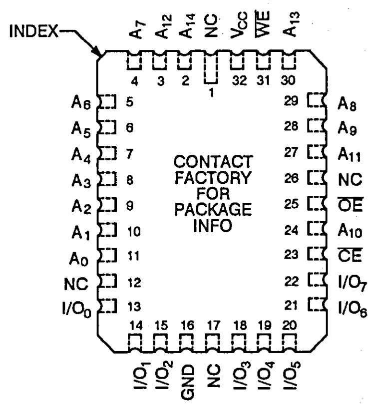


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

DEVICE OPERATIONAL MODE [1]

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_7$
Read	V_{IL}	V_{IL}	V_{IH}	$DATA_{OUT}$ $(O_0 - O_7)$
Byte Write	V_{IL}	V_{IH}	V_{IL}	$DATA_{IN}$ $(I_0 - I_7)$
Standby	V_{IH}	Don't Care	Don't Care	High Z
Write Inhibit	Don't Care	V_{IL}	Don't Care	High Z
	Don't Care	Don't Care	V_{IH}	High Z

NOTE:
1. All control inputs are TTL-compatible.

PIN NAMES

$A_0 - A_{14}$	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O_0	Data Input $(I_0 - I_7)$ During Write
I/O_7	Data Output $(O_0 - O_7)$ During Read

12

Integrated Device Technology, Inc.

FAST CMOS REGISTERED EEPROM 256K (32K x 8-BIT)

ADVANCE INFORMATION
IDT78C4256A

FEATURES:

- 5 volt only operation
- Fast access times
  - Military: 70ns (max.)
  - Commercial: 55ns (max.)
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ms max.
- $\overline{\text{DATA}}$ Polling—detection of write cycle completion
- 64-byte page write operation, page write 10ms max.
- On-chip edge triggered registers
- Synchronous and asynchronous output enable
- Programmable asynchronous register ($\overline{\text{INIT}}$)
- Low-power CEMOS™ technology
  - 100mA active current
- Data protection circuitry (V_{CC} lockout for $V_{CC} < 3.8V$) provides data integrity on power up/power down
- Software write protection
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- Military product compliant to MIL-STD-883, Class B

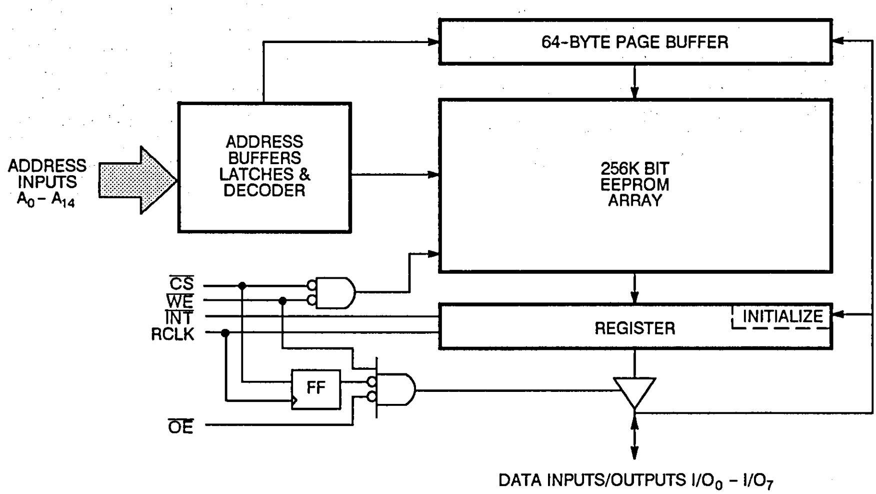
DESCRIPTION:

The IDT78C4256A is a 5 volt only 32K x 8 Registered Electrically Erasable Programmable Read-Only Memory (Registered EEPROM). Fabricated in IDT's CEMOS process, this Registered EEPROM provides 256K bits of non-volatile data storage (data retention in excess of 100 years).

The IDT78C4256A features fast read access times allowing zero wait state read cycle with high-performance microprocessors. Write time is automatically timed out by an internal timer and input latches secure address/data information, freeing the host system for other tasks during a write cycle. A 64-byte page mode allows one to 64 bytes to be written within a single write cycle to minimize total write time. The $\overline{\text{DATA}}$ Polling method for determining write cycle completion is supported by the IDT78C4256A. Data protection features include V_{CC} lock-out, write inhibit, noise protection for the $\overline{\text{WE}}$ pin and software write protection.

The IDT78C4256A has an initialize function $\overline{\text{INIT}}$ which activates an 8-bit word loaded into the on-chip Initialize register. This registered word is user programmable with any desired word (i.e. can be used to establish a PRESET or CLEAR word on the outputs). The IDT78C4256A military EEPROM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION

TO BE DETERMINED

DEVICE OPERATIONAL MODES [1]

MODE \ PIN	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	RCLK	I/O_0 - I/O_7
Deselected	H	X	L	↑	High Z
Read	X	H	H	X	High Z
Read	H	H	L	↑	High Z
Read	L	H	L	↑	Data Out at Addresses
Write	L	L	X	X	Data In at Addresses

NOTE:
1. "X" = Don't Care

PIN NAMES

A_0 - A_{14}	Addresses
$\overline{CS}$	Synchronous Output Enable/ Chip Enable (Write)
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O_0 - I/O_7	Data Input (I_0 - I_7) During Write; Data Output (O_0 - O_7) During Read
$\overline{INIT}$	Initialize
RCLK	Register Clock

12

Integrated Device Technology, Inc.

FAST CMOS REGISTERED EEPROM WITH SPC™ 256K (32K x 8-BIT)

ADVANCE INFORMATION
IDT78C5256A

FEATURES:

- 5 volt only operation
- Fast access times
  - Military: 70ns (max.)
  - Commercial: 55ns (max.)
- Serial Protocol Channel (SPC) allows load and readout of the memory array over a 4-wire channel
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ms max.
- $\overline{\text{DATA}}$ Polling—detection of write cycle completion
- 64-byte page write operation (page write 10ms max.)
- On-chip edge triggered registers
- Programmable asynchronous register ($\overline{\text{INIT}}$)
- Low-power CEMOS™ technology
  - Active Current: 100mA
- Data protection circuitry (V_{CC} lockout for V_{CC} < 3.8V) provides data integrity on power up/power down
- Software write protection
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- Military product compliant to MIL-STD-883, Class B

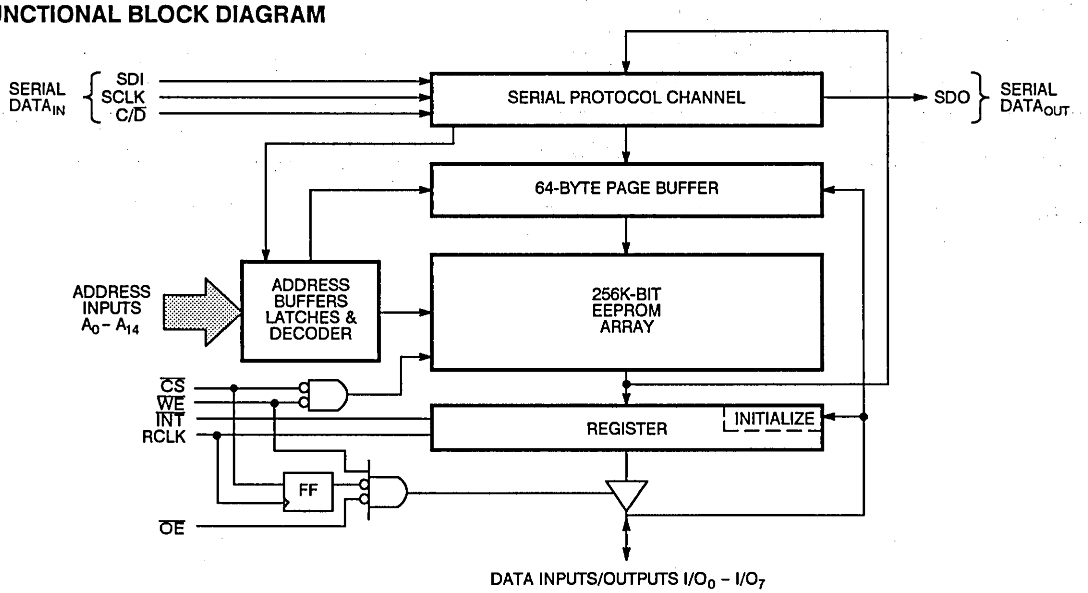
DESCRIPTION:

The IDT78C5256A is a 5 volt only 32K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM) with Serial Protocol Channel (SPC). SPC complements the EEPROM's parallel information path by providing a serial link (4 additional pins) by which its memory array can be written or read. Fabricated in IDT's CEMOS process, this EEPROM provides 256K bits of nonvolatile data storage (data retention in excess of 100 years).

The IDT78C5256A features fast read access times allowing zero wait state cycles with high-performance microprocessors. Write time is automatically timed out by an internal timer and input latches secure address/data information, freeing the host system for other tasks during a write cycle. A 64-byte write page buffer allows 1 to 64 bytes to be written within a single write cycle to minimize total write time. The $\overline{\text{DATA}}$ Polling method for determining completion of the write cycle is supported by the IDT78C5256A. Data protection features include V_{CC} lockout, write inhibit, noise protection for the $\overline{\text{WE}}$ pin and software write protection.

The IDT78C5256A is ideal for systems requiring nonvolatility and in-system data modifications. With SPC, a serial link can be established during board layout for easy field updates of code changes. The initialize function ($\overline{\text{INIT}}$) can be used to activate an 8-bit word loaded into the on-chip Initialize register. This registered word is user programmable with any desired word. The IDT78C5256A military EEPROM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS and SPC are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATIONS
(CONSULT FACTORY)

DEVICE OPERATIONAL MODES[1]

MODE \ PIN	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	RCLK	I/O_0 – I/O_7
Deselected	H	X	L	$\uparrow$	High Z
Read	X	H	H	X	High Z
Read	H	H	L	$\uparrow$	High Z
Read	L	H	L	$\uparrow$	Data Out at Addresses
Write	L	L	X	X	Data In at Addresses

NOTE:
1. X = Don't care

PIN NAMES

A_0 – A_{14}	Addresses
$\overline{CS}$	Synchronous Output Enable/ Chip Enable (Write)
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O_0 I/O_7	Data Input (I_0 – I_7) during write Data Output (O_0 – O_7) during read
SDI	Serial Data Input
SDO	Serial Data Output
SCLK	Data Clock Input
C/$\overline{D}$	Command/$\overline{\text{Data}}$
$\overline{INIT}$	Initialize
RCLK	Register Clock

SPC OPERATIONAL MODES[1]

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{C/D}$	SCLK	FUNCTION
Command	X	X	X	H	$\uparrow$	Shift bit into command register
Data	X	X	X	L	$\uparrow$	Shift bit into data register
Execute	X	X	X	$\downarrow$	$\uparrow$	Execute command during time between C/$\overline{D}$ and SCLK

NOTE:
1. X = Don't Care

Product Selector and Cross Reference Guides

Technology/Capabilities

Quality and Reliability

Static RAMs

Dual-Port RAMs

FIFO Memories

Digital Signal Processing (DSP)

Bit-Slice Microprocessor Devices (MICROSLICE™) and EDC

Reduced Instruction Set Computer (RISC) Processors

Logic Devices

Data Conversion

E^2PROMS-Electrically Erasable Programmable Read Only Memories

Subsystems Modules

Application and Technical Notes

Package Diagram Outlines

13

SUBSYSTEM PRODUCTS INTRODUCTION

A unique combination of resources and experience sets the Subsystems Division apart from its competitors. IDT's advanced technology, multiple manufacturing plants and the backing of sister divisions allow us to offer a diverse range of module products quickly and cost-effectively. In addition, our capabilities are flexible enough to include standard and custom modules, as well as a complete, self-contained, U.S.-based military device assembly and module operation.

IDT's subsystems provide a modular approach which allows designers to meet several important criteria needed in a modern electronics system. These features include:

High Performance

High Reliability

Compact Size

Low Power

Quick Design Time

Ease of Manufacture

Competitive Cost

High-performance CMOS products in surface mounted packages are combined with thermally matched substrates to produce very dense and highly reliable modules. Conventional pins are then attached to these modules so that they can be plugged into a circuit board in a conventional through-hole manner.

This process allows production of a Megabit static RAM in a standard size dual in-line package several years before the available technology can produce a comparable monolithic device. In addition, an application specific product can be manufactured that could not be easily or cost-effectively produced as a monolithic device. These ASIC products can include error detection, parity, address latching or buffering and wide words (x16 and x32).

Complete memory systems, such as megabyte-size high-speed caches or writable control stores, can also be produced on a single plug-in module. Systems can now be designed with the major memory portions supplied as a single fully-tested high density component. This approach gives customers access to surface mount technology without the need to invest in special design, manufacturing and testing facilities.

TABLE OF CONTENTS

CONTENTS **PAGE**

MODULE PART NUMBER GUIDE

IDT 8M 824 S 70 C B

DEVICE TYPE POWER SPEED PACKAGE PROCESS

- PROCESS:
  - BLANK - COMMERCIAL 0° C to +70°C
  - B - Military -55°C to +125°C
- PACKAGE: SEE PACKAGE TABLE
- SPEED - Guaranteed Minimum Performance in Nanoseconds
- POWER -
  - S - Standard Power
  - L - Low Power
- Device Type

PACKAGE TABLE

CODE	SUBSTRATE	COMPONENTS
C	CO-FIRED CERAMIC SIDEBRAZE, DUAL IN-LINE	CERAMIC
N	CO-FIRED CERAMIC SIDEBRAZE, DUAL IN-LINE	PLASTIC
P	FR4 EPOXY LAMINATE, DUAL IN-LINE	PLASTIC
S	FR4 EPOXY LAMINATE, SINGLE IN-LINE (SIP)	PLASTIC
CS	CO-FIRED CERAMIC, SINGLE IN-LINE	CERAMIC
Z	FR4 EPOXY LAMINATE, STAGGERED SIP (ZIP)	PLASTIC
V	FR4 EPOXY LAMINATE, VERTICAL, DUAL ROW (SIP TYPE)	PLASTIC
CV	CO-FIRED CERAMIC, VERTICAL, DUAL ROW (SIP TYPE)	CERAMIC
K	FR4 EPOXY LAMINATE, QUAD IN-LINE (QIP)	PLASTIC
CK	CO-FIRED CERAMIC, QUAD IN-LINE	CERAMIC

Integrated Device Technology, Inc.

1 MEGABIT CMOS STATIC RAM PLASTIC MODULE

ADVANCE INFORMATION
IDT7MB624

FEATURES:

- High-density 1024K-bit CMOS static RAM module
- Customer-configured to 64K x 16, 128K x 8 or 256K x 4
- Fast access times
  - 25ns (max.)
- Low power consumption
  - Active: 4.8W (typ.) (in 64K x 16 organization)
  - Standby: 1.6mW (typ.)
- Utilizes 16 IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Offered in 40-pin, 900 mil center plastic DIP, achieving very high memory density
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate

DESCRIPTION:

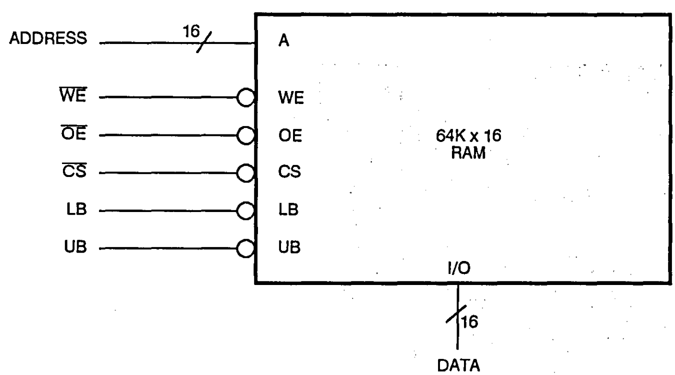
The IDT7MB624 is a 1024K-bit high-speed CMOS static RAM constructed on an epoxy laminate substrate using 16 IDT7187 (64K x 1) static RAMs in plastic surface mount packages. Making four chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 64K x 16, 128K x 8 or 256K x 4 organization. In addition, extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

The IDT7MB624 is available with access times as fast as 25ns over the commercial temperature range, with maximum operating power consumption of only 9.6W (significantly less if organized 128K x 8 or 256K x 4). The module also offers a standby power mode of 4.4W (max.) and a full standby mode of 1.7W (max.).

The IDT7MB624 is offered in a high-density 40-pin, 900 mil center plastic DIP to take full advantage of the compact IDT7187s in plastic surface mount packages.

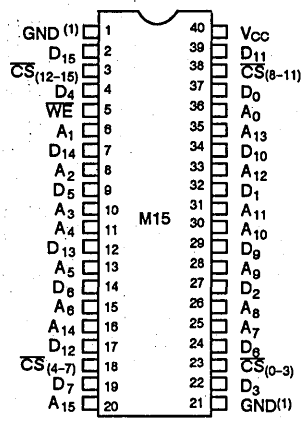
All inputs and outputs of the IDT7MB624 are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP
TOP VIEW

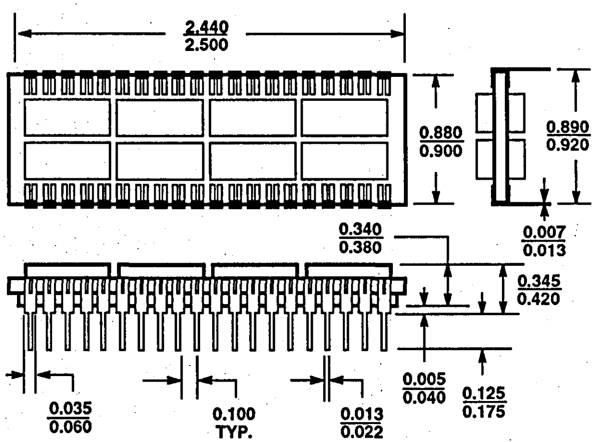
NOTES:
1. Both GND pins need to be grounded for proper operation.

PIN NAMES

$A_0 - A_{15}$	Addresses
$D_0 - D_{15}$	Data Input/Output
$\overline{CS}_{XX}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

PACKAGE DIMENSIONS

(M15) 40-PIN PLASTIC DIP



Integrated Device Technology, Inc.

256K (256K x 1-BIT) CMOS STATIC RAM SIP MODULE

IDT7MC156

FEATURES:

- High-density 256K (256K x 1) CMOS static RAM module
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Available in low profile 28-pin ceramic SIP (single in-line package) for maximum space saving
- Fast access times: 25ns (max.) over commercial temperature
- Low power consumption
  - Dynamic: less than 600mW (typ.)
  - Full standby: less than 30mW (typ.)
- Utilizes IDT7187s high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

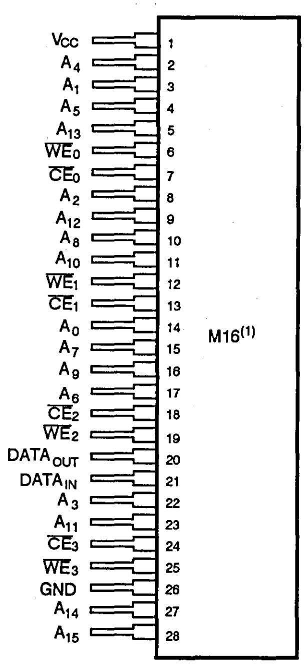
The IDT7MC156 is a 256K (256K x 1-bit) high-speed static RAM module constructed on a co-fired ceramic substrate using four IDT7187 64K x 1 static RAMs in surface mount packages.

The 7MC family of ceramic SIPs offers the optimum in packing density and profile height. The IDT7MC156 is offered in a 28-pin ceramic SIP (single in-line package). At only 350 mils high, this low profile package is ideal for systems with minimal board spacing. Surface mount SIP technology also yields very high packing density, allowing greater than three IDT7MC156 modules to be stacked per inch of board space.

The IDT7MC156 is available with maximum access times as fast as 25ns and maximum power consumption of 1.8 watts. The module also offers a full standby mode of 440mW (max.).

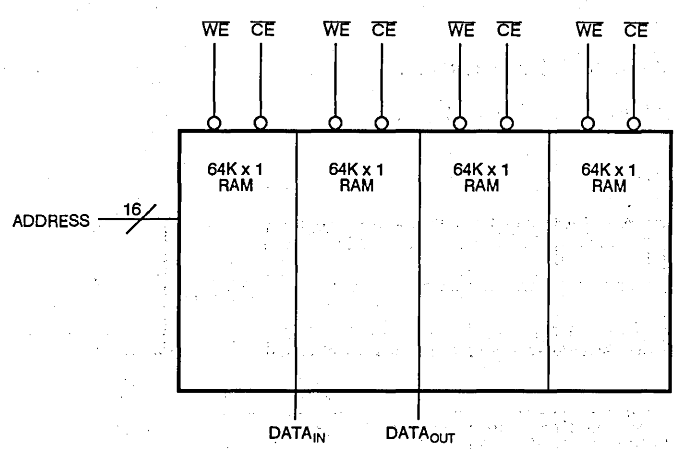
All inputs and outputs of the IDT7MC156 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access times for ease of use.

PIN CONFIGURATION



SIP
SIDE VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0–A_{15}	Address Lines
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CS}_{0-3}$	Chip Enable
$\overline{WE}_{0-3}$	Write Enable
V_{CC}	Power
GND	Ground

NOTE:

1. For module dimensions, please refer to module drawing M16 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE **DECEMBER 1987**

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MC156 MIN.	TYP.[1]	MAX.[2]	MAX.[3]	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	–	15	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	15	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = 0	–	110	225	300	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = f_{MAX}	–	120	245	330	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ or (TTL Level) V_{CC} = Max., Output Open	–	90	180	240	mA
I_{SB1}	Full Standby Power Supply Current	CS $\geq V_{HC}$, $V_{IN} \geq V_{HC}$ or V_{LC} V_{CS} = Max., Output Open	–	6	60	80	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	–	–	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	–	–	–	V

NOTES:

1. V_{CC} = 5V, T_A = +25°C
2. t_{AA} = 35, 45, 45, 55ns
3. t_{AA} = 25, 30ns

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

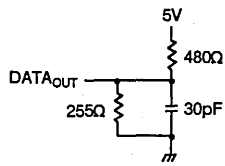


Figure 1. Output Load

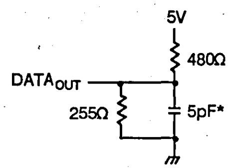


Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7MC156S25 MIN.	IDT7MC156S25 MAX.	IDT7MC156S30 MIN.	IDT7MC156S30 MAX.	IDT7MC156S35 MIN.	IDT7MC156S35 MAX.	IDT7MC156S45 MIN.	IDT7MC156S45 MAX.	IDT7MC156S55 MIN.	IDT7MC156S55 MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	25	–	30	–	35	–	45	–	55	ns
$t_{CLZ1,2}$ (1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ} (1)	Chip Select to Output in High Z	–	20	–	25	–	25	–	30	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{PU} (1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD} (1)	Chip Deselect to Power Down Time	–	25	–	30	–	35	–	45	–	55	ns

NOTE:
1. This parameter guaranteed but not tested.

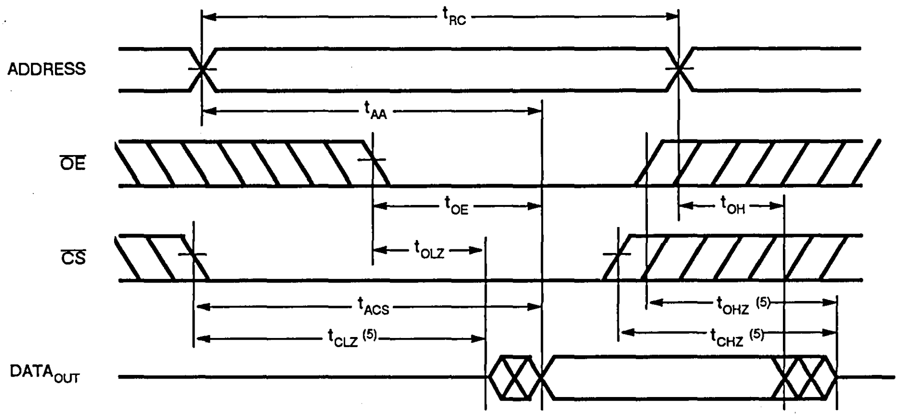
AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

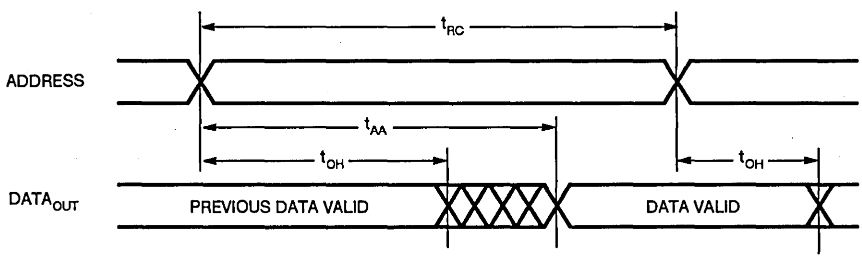
SYMBOL	PARAMETER	IDT7MC156S25 MIN.	IDT7MC156S25 MAX.	IDT7MC156S30 MIN.	IDT7MC156S30 MAX.	IDT7MC156S35 MIN.	IDT7MC156S35 MAX.	IDT7MC156S45 MIN.	IDT7MC156S45 MAX.	IDT7MC156S55 MIN.	IDT7MC156S55 MAX.	UNIT
WRITE CYCLE												
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	55	–	ns
t_{CW}	Chip Selection to End of Write	25	–	25	–	30	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	25	–	25	–	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	25	–	35	–	45	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ} (1)	Write Enable to Output in High Z	–	20	–	25	–	25	–	30	–	30	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	20	–	25	–	25	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	5	–	ns
t_{OW} (1)	Output Active from End of Write	0	–	0	–	0	–	0	–	0	–	ns

NOTE:
1. This parameter guaranteed but not tested.

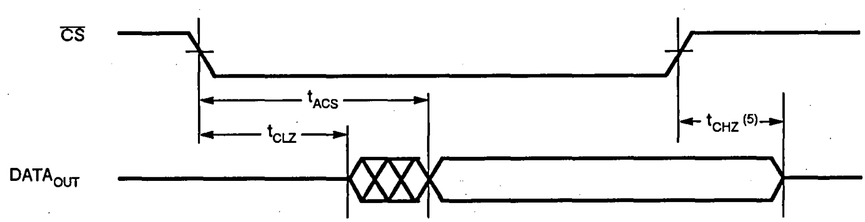
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]

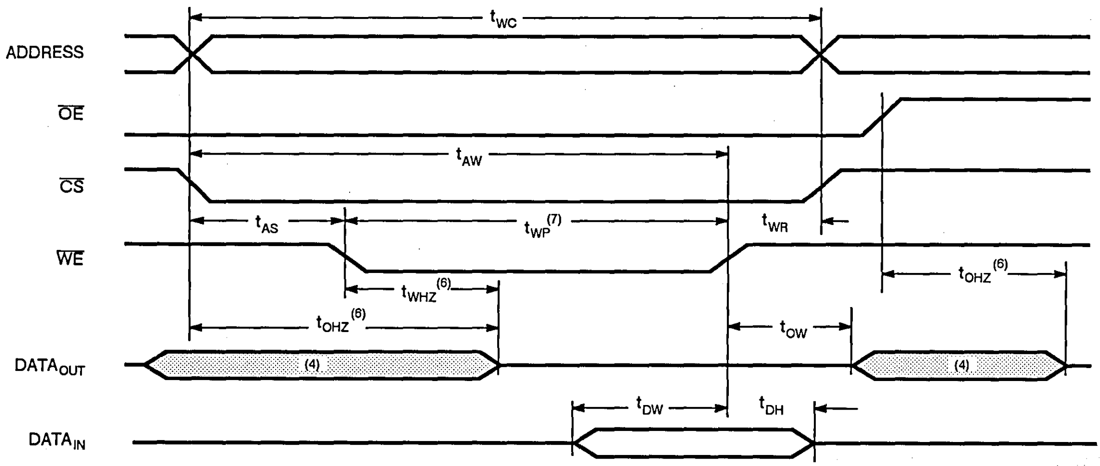


TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]

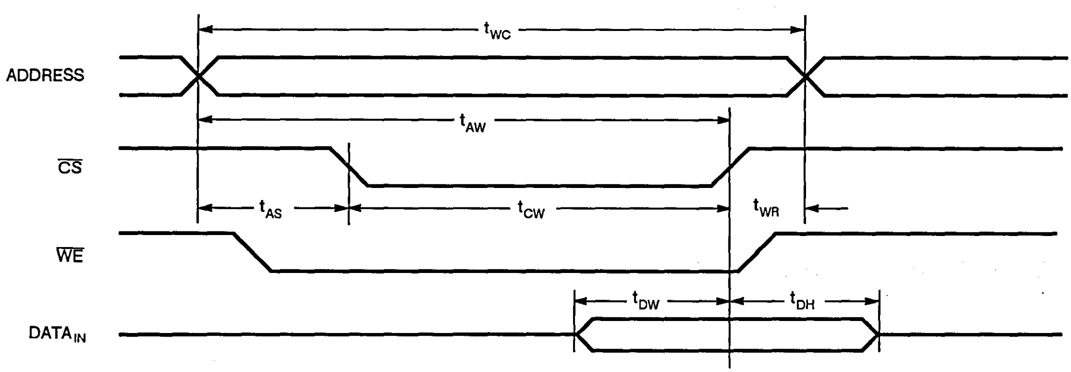


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



13

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > $t_{WHZ} + t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	X	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:

1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

- Process/Temperature Range: Blank — Commercial (0°C to +70°C)
- Package: CS — Ceramic SIP
- Speed: 25, 30, 35, 45, 55 — Speed in Nanoseconds
- Power: S — Standard Power
- Device Type: 7MC156 — 256K x 1-Bit

Integrated Device Technology, Inc.

1 MEGABIT (1024K x 1-BIT) CMOS STATIC RAM SIP MODULE

PRELIMINARY
IDT7MC4001

FEATURES:

- High-density 1 megabit (1024K x 1) CMOS static RAM module
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Available in low profile 30-pin ceramic SIP (single in-line package) for maximum space saving
- Fast access times: 35ns (max.)
- Separate I/O lines
- Low power consumption
  - Dynamic: 1.35W (max.)
  - Full standby: 330mW (max.)
- Single 5V(±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

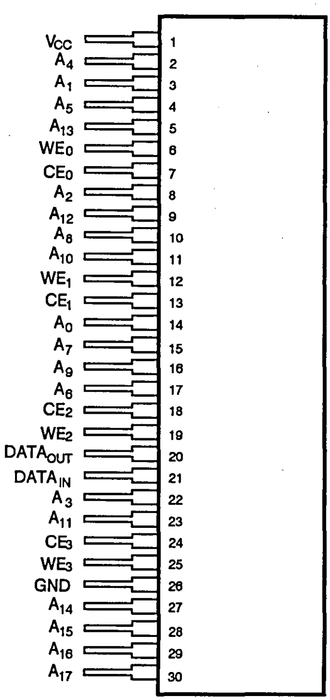
The IDT7MC4001 is a 1 megabit (1024K x 1-bit) high-speed static RAM module with separate I/O. The module is constructed on a co-fired ceramic substrate using four IDT71257 256K x 1 static RAMs in surface mount packages.

The 7MC family of ceramic SIPs offers the optimum in packing density and profile height. The IDT7MC4001 is offered in a 30-pin ceramic SIP (single in-line package). At only 420 mils high, this low profile package is ideal for systems with minimal board spacing. Surface mount SIP technology also yields very high packing density, allowing five IDT7MC4001 modules to be stacked per inch of board space.

The IDT7MC4001 is available with maximum access times as fast as 35ns, with maximum power consumption of 1.35 watts. The module also offers a full standby mode of 330mW (max.).

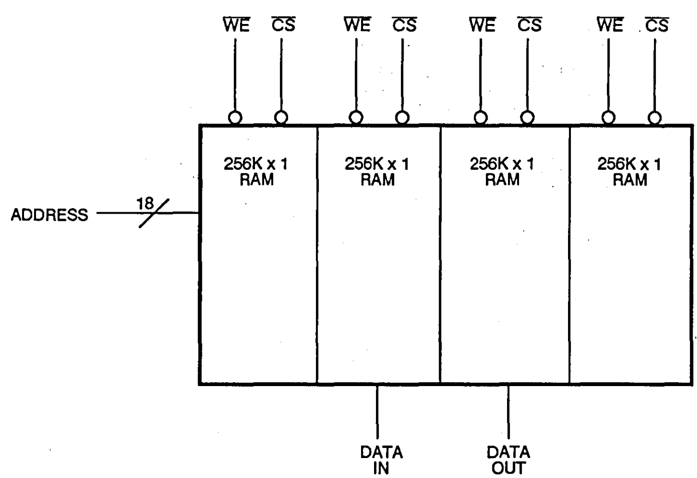
All inputs and outputs of the IDT7MC4001 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access times for ease of use.

PIN CONFIGURATION



SIP SIDE VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{0-17}	Address
$DATA_{IN}$	Data Input
$DATA_{OUT}$	Data Output
$\overline{CS}_{0-3}$	Chip Select
$\overline{WE}_{0-3}$	Write Enable
V_{CC}	Power
GND	Ground

CEMOS is a trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE **DECEMBER 1987**

DSC-7003/-

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MC4001 MIN.	IDT7MC4001 MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	50	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = 0	–	225	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = f_{MAX}	–	245	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ or (TTL Level) V_{CC} = Max., Output Open	–	180	mA
I_{SB1}	Full Standby Power Supply Current	CS $\geq V_{HC}$, $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$ V_{CS} = Max., Output Open	–	60	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	–	V

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

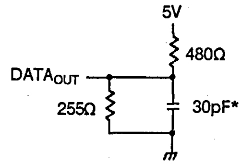


Figure 1. Output Load

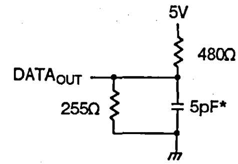


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7MC4001S35 MIN.	MAX.	IDT7MC4001S45 MIN.	MAX.	IDT7MC4001S55 MIN.	MAX.	UNIT
READ CYCLE								
t_{RC}	Read Cycle Time	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	35	–	45	–	55	ns
$t_{CLZ1,2}$ (1)	Chip Select to Output in Low Z	10	–	10	–	10	–	ns
t_{CHZ} (1)	Chip Select to Output in High Z	–	25	–	35	–	45	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	ns
t_{PU} (1)	Chip Select to Power Up Time	0	–	0	–	0	–	ns
t_{PD} (1)	Chip Deselect to Power Down Time	–	35	–	45	–	55	ns

NOTE:
1. This parameter guaranteed but not tested.

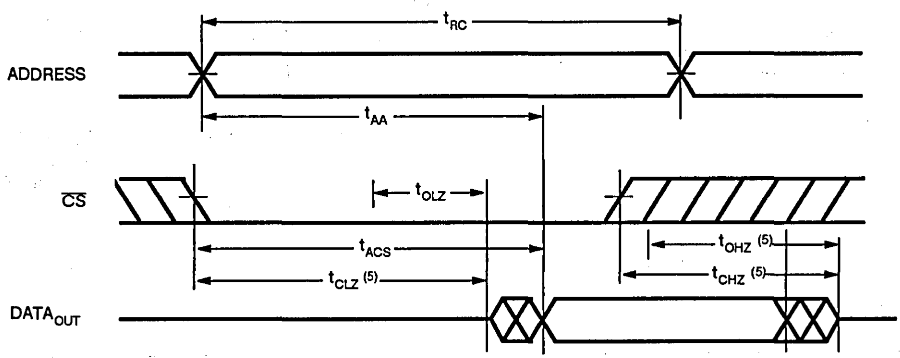
AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

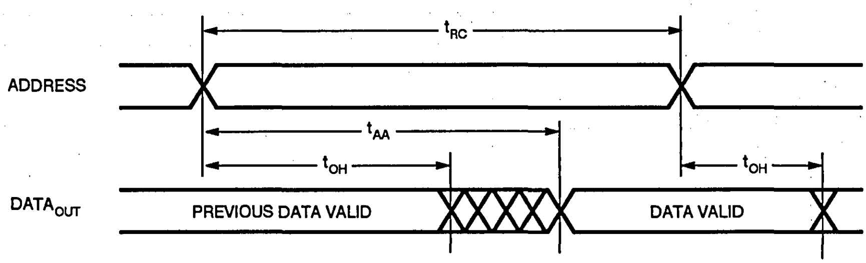
SYMBOL	PARAMETER	IDT7MC4001S35 MIN.	MAX.	IDT7MC4001S45 MIN.	MAX.	IDT7MC4001S55 MIN.	MAX.	UNIT
WRITE CYCLE								
t_{WC}	Write Cycle Time	35	–	45	–	55	–	ns
t_{CW}	Chip Selection to End of Write	30	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	25	–	35	–	45	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	ns
t_{WHZ} (1)	Write Enable to Output in High Z	–	25	–	30	–	40	ns
t_{DW}	Data Valid to End of Write	20	–	25	–	35	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	ns
t_{OW} (1)	Output Active from End of Write	5	–	5	–	5	–	ns

NOTE:
1. This parameter guaranteed but not tested.

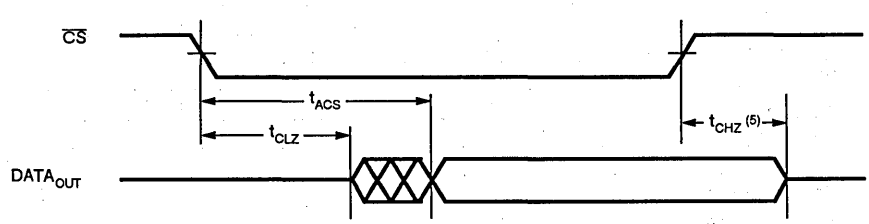
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



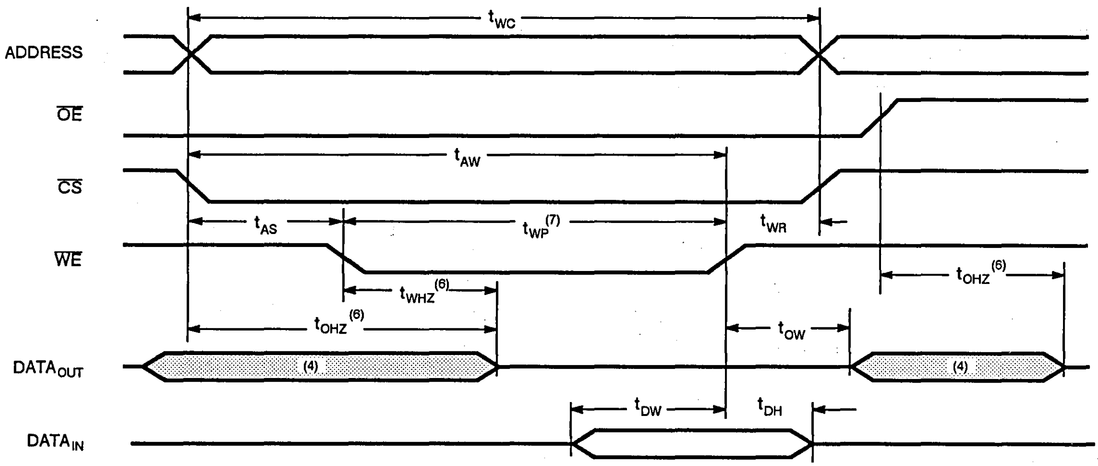
TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]



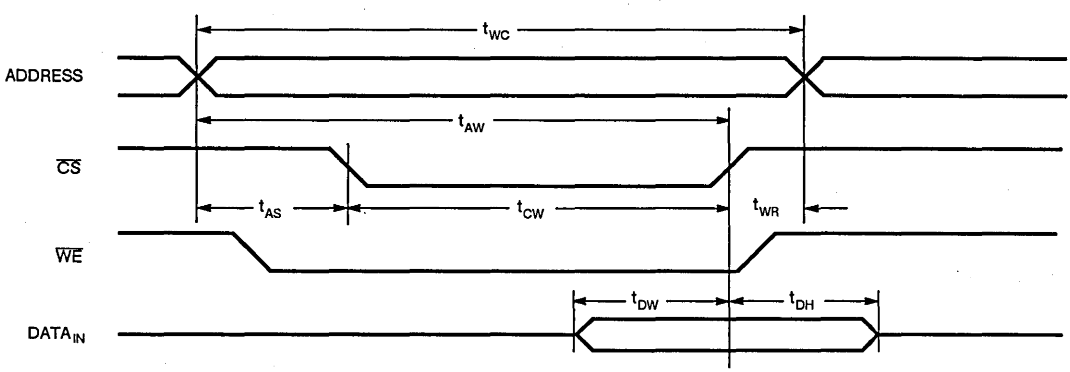
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TRUTH TABLE

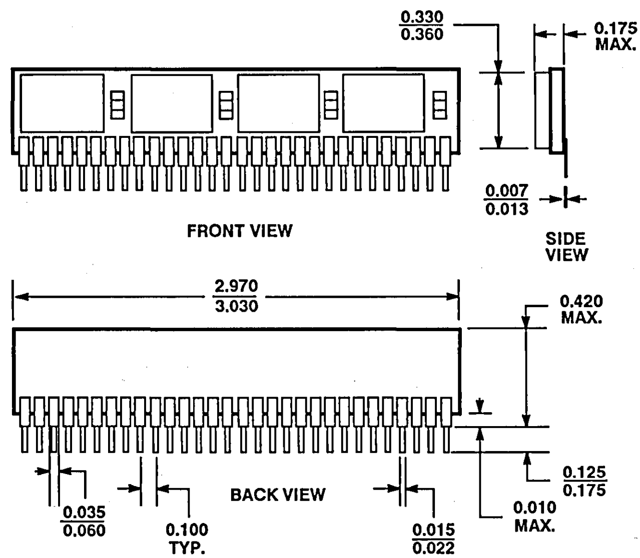
MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

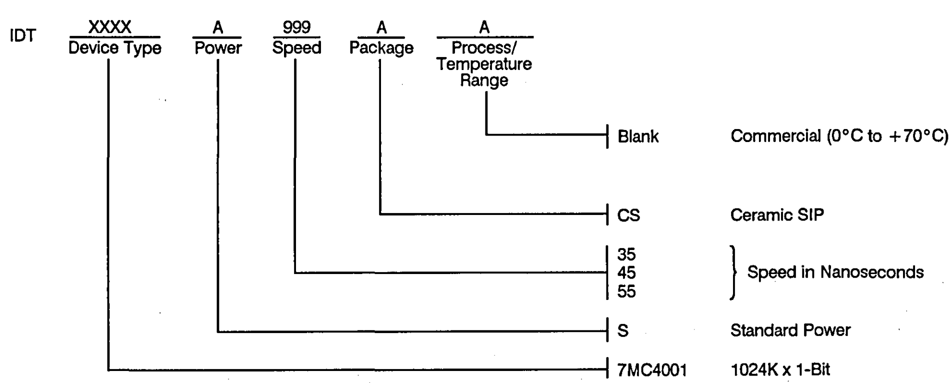
SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

NOTE:
1. This parameter is sampled and not 100% tested.

PACKAGE OUTLINE



ORDERING INFORMATION



Integrated Device Technology, Inc.

512K (16K x 32) CMOS STATIC RAM DUAL CERAMIC SIP MODULE

PRELIMINARY
IDT7MC4032

FEATURES:

- High-density 32 bit word 512K (16K x 32) static RAM module
- Available in low profile 88-pin sidebraze dual ceramic SIP (single in-line package)
- Separate I/O
- Fast access time: 30ns (max.)
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- High impedance outputs during write mode
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled in IDT's high reliability vapor phase solder reflow process
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible
- Multiple GND pins for maximum noise immunity

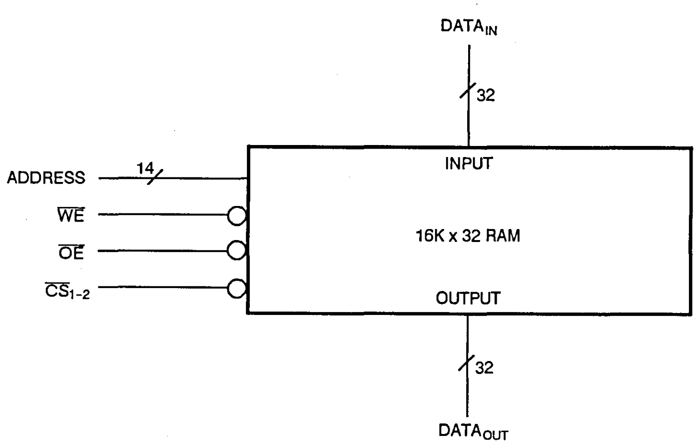
DESCRIPTION:

The IDT7MC4032 is a 32-bit wide 512K (16K x 32) static RAM module with separate I/O constructed on a co-fired ceramic substrate using eight IDT71982 16K x 4 static RAMs in leadless chip carriers. Extremely fast speeds can be achieved due to the use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS™ technology. The IDT7MC4032 is available with access time as fast as 30ns, with minimal power consumption.

The 7MC family of ceramic SIPs offers the optimum is packing density and profile height. The IDT7MC4032 is packaged in a 88-pin dual ceramic SIP. The dual row configuration allows 88 pins to be placed on a package less than 4.5 inches long and .27 inches wide. At only 520 mils high, this profile package is ideal for systems with minimum board spacing. Extremely high packing density can also be achieved allowing four IDT7MC4032 modules to be stacked per inch of board space.

All inputs and outputs of the IDT7MC4032 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



13

CEMOS is a trademark of Integrated Device Technology, Inc.

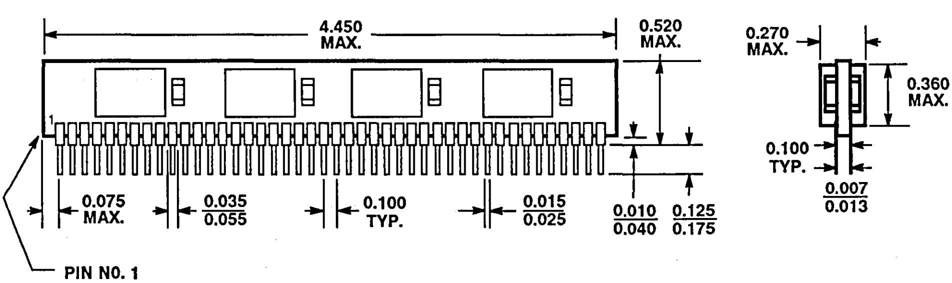
PIN OUT

Name	Pin	Pin	Name
GND	1	88	V_{CC}
DI_0	2	87	DO_0
DI_1	3	86	DO_1
DI_2	4	85	DO_2
DI_3	5	84	DO_3
DI_4	6	83	DO_4
DI_5	7	82	DO_5
DI_6	8	81	DO_6
DI_7	9	80	DO_7
A_0	10	79	A_1
A_2	11	78	A_3
A_4	12	77	A_5
DI_8	13	76	DO_8
DI_9	14	75	DO_9
DI_{10}	15	74	DO_{10}
DI_{11}	16	73	DO_{11}
DI_{12}	17	72	DO_{12}
DI_{13}	18	71	DO_{13}
DI_{14}	19	70	DO_{14}
DI_{15}	20	69	DO_{15}
$\overline{WE}$	21	68	$\overline{CS}_L$
V_{CC}	22	67	GND
$\overline{OE}$	23	66	$\overline{CS}_U$
DI_{16}	24	65	DO_{16}
DI_{17}	25	64	DO_{17}
DI_{18}	26	63	DO_{18}
DI_{19}	27	62	DO_{19}
DI_{20}	28	61	DO_{20}
DI_{21}	29	60	DO_{21}
DI_{22}	30	59	DO_{22}
DI_{23}	31	58	DO_{23}
A_6	32	57	A_7
A_8	33	56	A_9
A_{10}	34	55	A_{11}
A_{12}	35	54	A_{13}
DI_{24}	36	53	DO_{24}
DI_{25}	37	52	DO_{25}
DI_{26}	38	51	DO_{26}
DI_{27}	39	50	DO_{27}
DI_{28}	40	49	DO_{28}
DI_{29}	41	48	DO_{29}
DI_{30}	42	47	DO_{30}
DI_{31}	43	46	DO_{31}
GND	44	45	V_{CC}

PIN NAMES

A_{0-13}	Addresses
DI_{0-31}	Data Input
DO_{0-31}	Data Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}_L$	Chip Select (Lower)
$\overline{CS}_U$	Chip Select (Upper)
V_{CC}	Power
GND	Ground

PACKAGE OUTLINE



Integrated Device Technology, Inc.

256K (256K x 1-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

IDT7MP156

FEATURES:

- High-density 256K (256K x 1) CMOS static RAM module
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Available in 28-pin SIP (single in-line package) for maximum space saving
- Fast access times: 25ns (max.) over commercial temperature
- Low power consumption
  - Dynamic: less than 600mW (typ.)
  - Full standby: less than 30mW (typ.)
- Utilizes IDT7187 high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION

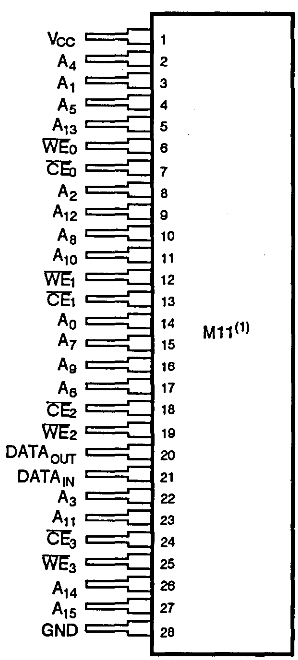
The IDT7MP156 is a 256K (256K x 1-bit) high-speed static RAM module constructed on an epoxy laminate surface using four IDT7187 64K x 1 static RAMs in surface mount packages. Extremely fast speeds can be achieved with this technique due to use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS technology.

The 7MP family of surface mounted SIP technology is a cost-effective solution allowing for very high packing density. The IDT7MP156 is offered in a 28-pin SIP (single in-line package). The IDT7MP156 can be mounted on 200 mil centers, yielding 1.25 megabits of memory in less than 3 square inches of board space.

The IDT7MP156 is available with maximum access times as fast as 25ns with maximum power consumption of 1.8 watts. The module also offers a full standby mode of 440mW (max.).

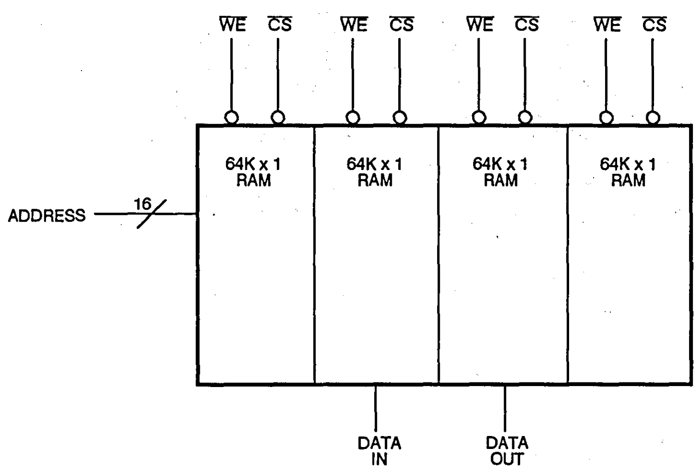
All inputs and outputs of the IDT7MP156 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

PIN CONFIGURATION



SIP TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0–A_{15}	Address Lines
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}_{0-3}$	Chip Enable
$\overline{WE}_{0-3}$	Write Enable
Vcc	Power
GND	Ground

NOTE:

1. For module dimensions, plese refer to module drawing M11 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC}– 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MP156 MIN.	TYP.[1]	MAX.[2]	MAX.[3]	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	–	15	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	15	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = 0	–	110	225	300	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = f_{MAX}	–	120	245	330	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or (TTL Level) V_{CC} = Max., Output Open	–	90	180	240	mA
I_{SB1}	Full Standby Power Supply Current	CS ≥ V_{HC}, V_{IN} ≥ V_{HC} or V_{LC} V_{CS} = Max., Output Open	–	6	60	80	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	–	–	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	–	–	–	V

NOTES:
1. V_{CC} = 5V, T_A = +25°C
2. t_{AA} = 35, 45, 45, 55ns
3. t_{AA} = 25, 30ns

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

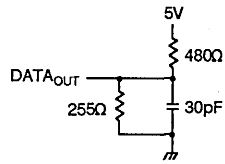


Figure 1. Output Load

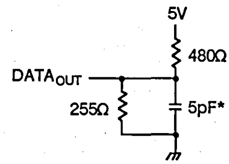


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

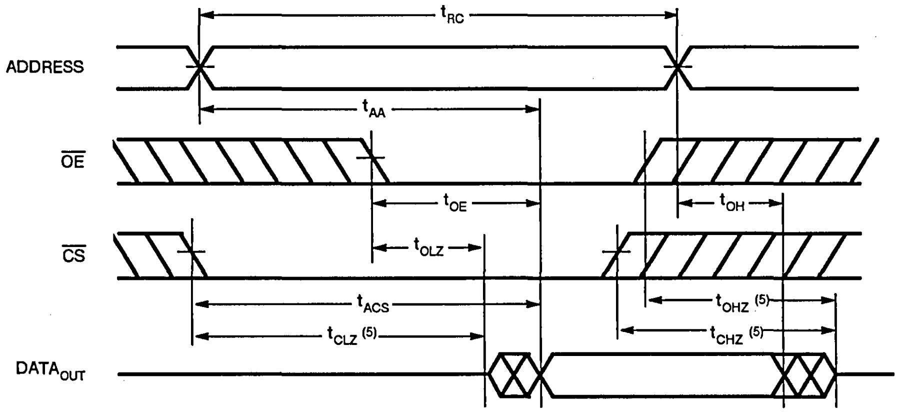
AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = –55°C to +125°C and 0°C to 70°C)

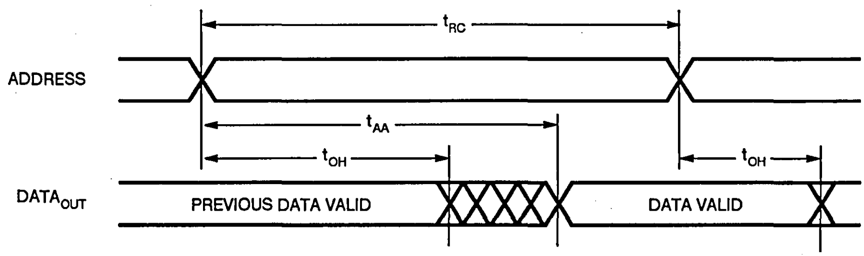
SYMBOL	PARAMETER	IDT7MP156S25 MIN.	IDT7MP156S25 MAX.	IDT7MP156S30 MIN.	IDT7MP156S30 MAX.	IDT7MP156S35 MIN.	IDT7MP156S35 MAX.	IDT7MP156S45 MIN.	IDT7MP156S45 MAX.	IDT7MP156S55 MIN.	IDT7MP156S55 MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	25	–	30	–	35	–	45	–	55	ns
$t_{CLZ1,2}$[1]	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}[1]	Chip Select to Output in High Z	–	20	–	25	–	25	–	30	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}[1]	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}[1]	Chip Deselect to Power Down Time	–	25	–	30	–	35	–	45	–	55	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	55	–	ns
t_{CW}	Chip Selection to End of Write	25	–	25	–	30	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	25	–	25	–	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	25	–	35	–	45	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}[1]	Write Enable to Output in High Z	–	20	–	25	–	25	–	30	–	30	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	20	–	25	–	25	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	5	–	ns
t_{OW}[1]	Output Active from End of Write	0	–	0	–	0	–	0	–	0	–	ns

NOTE:
1. This parameter guaranteed but not tested.

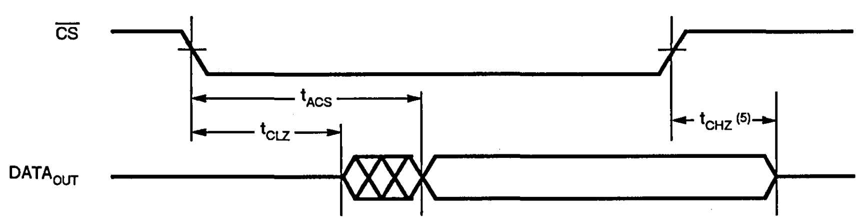
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



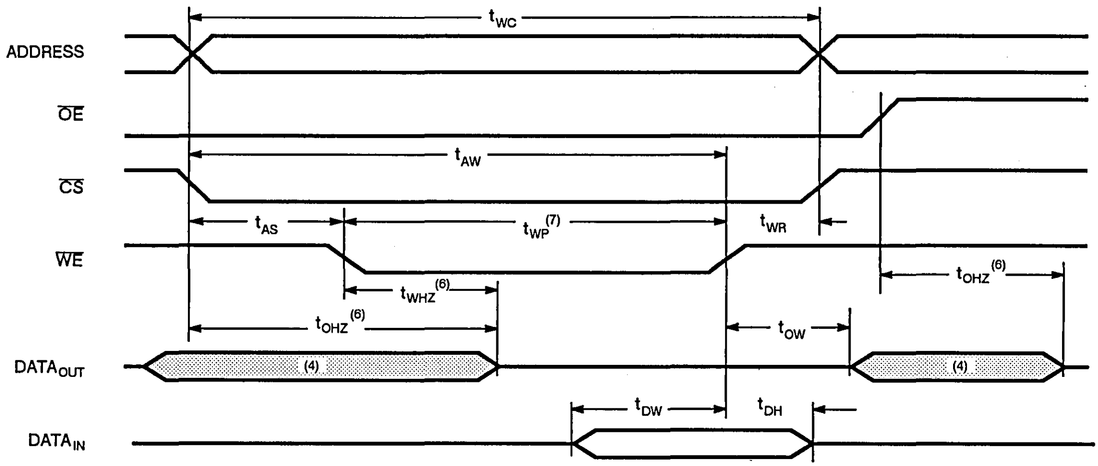
TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]



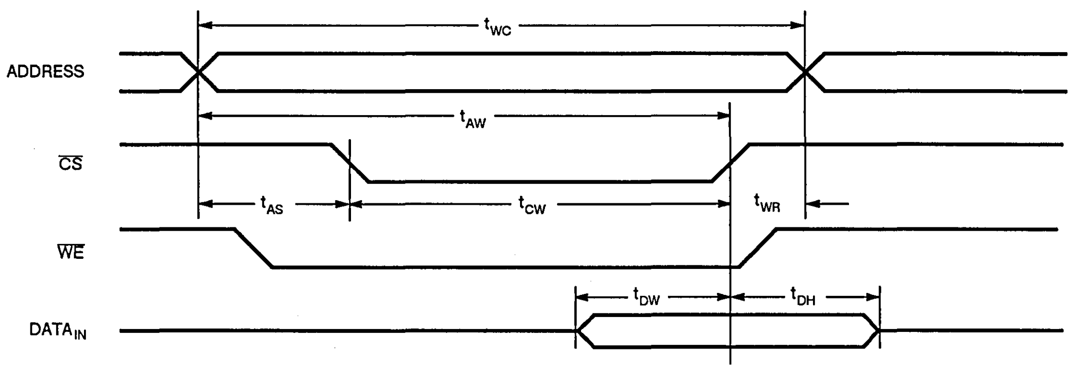
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{UB}$, $\overline{LB}$ = V_{IL} for 16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



13

NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
Package	S	Plastic SIP
Speed	25 30 35 45 55	Speed in Nanoseconds
Power	S	Standard Power
Device Type	7MP156	256K x 1-Bit

Integrated Device Technology, Inc.

256K (64K x 4-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

IDT7MP456

FEATURES:

- High-density 256K (64K x 4) CMOS static RAM module
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Available in 28-pin SIP (single in-line package) for maximum space saving
- Fast access times: 25ns (max.) over commercial temperature
- Low power consumption
  - Dynamic: less than 1.2W (typ.)
  - Full standby: less than 30 mW(typ.)
- Utilizes IDT7187 high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

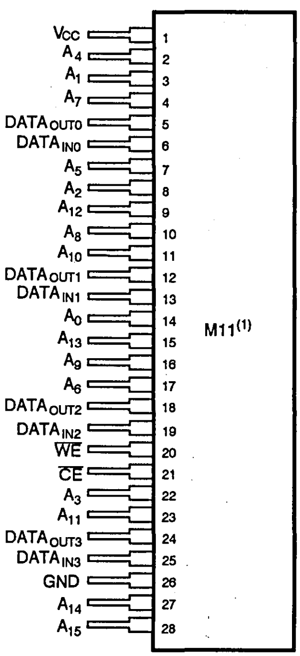
The IDT7MP456 is a 256K (64K x 4-bit) high-speed static RAM module constructed on an epoxy laminate surface using four IDT7187 64K x 1 static RAMs in plastic surface mount packages. Extremely fast speeds can be achieved with this technique due to the use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS technology.

The 7MP family of surface mounted SIP technology is a cost-effective solution allowing for very high packing density. The IDT7MP456 is offered in a 28-pin SIP. The IDT7MP456 can be mounted on 200 mil centers, yielding 1.25 megabits of memory in less than 3 square inches of board space.

The IDT7MP456 is available with maximum access times as fast as 25ns, with maximum power consumption of 3.3 watts. The module also offers a full standby mode of 440mW(max.).

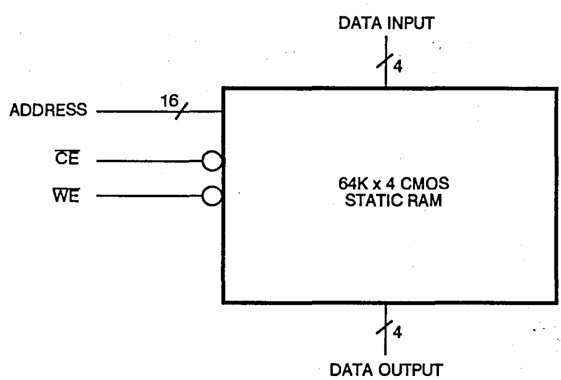
All inputs and outputs of the IDTMP456 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

PIN CONFIGURATION



SIP
SIDE VIEW

FUNCTIONAL BLOCK DIAGRAM



NOTE:

1. For module dimensions, please refer to module drawing M11 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN NAMES

A_0-A_{15}	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
D_{IN0} - D_{IN3}	Data Input
D_{OUT0} - D_{OUT3}	Data Output
V_{CC}	Power
GND	Ground

13

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MP456 MIN.	TYP.[1]	MAX.[2]	MAX.[3]	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	–	15	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH} , V_{OUT} = GND to V_{CC}	–	–	15	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL} V_{CC} = Max. , Output Open F = 0	–	180	360	480	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	–	240	440	600	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ or (TTL Level) V_{CC} = Max. Output Open	–	90	180	240	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{HC}$, $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$ V_{CC} = Max., Output Open	–	6	60	80	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	–	–	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	–	–	–	V

NOTES:

1. V_{CC} = 5V, t_{AA} = 25°C
2. t_{AA} = 35, 45, 55ns
3. t_{AA} = 25, 30ns

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

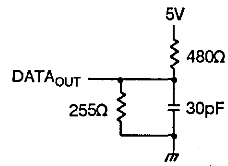


Figure 1. Output Load

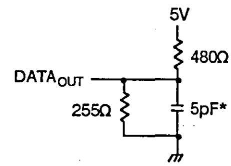


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

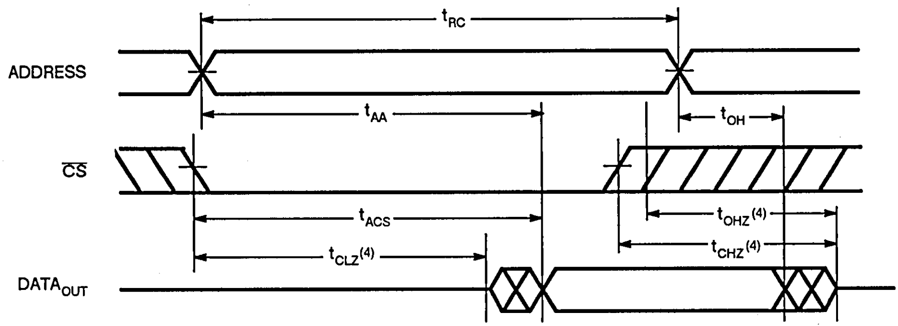
(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7MP456S25 MIN.	IDT7MP456S25 MAX.	IDT7MP456S30 MIN.	IDT7MP456S30 MAX.	IDT7MP456S35 MIN.	IDT7MP456S35 MAX.	IDT7MP456S45 MIN.	IDT7MP456S45 MAX.	IDT7MP456S55 MIN.	IDT7MP456S55 MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	25	–	30	–	35	–	45	–	55	ns
$t_{CLZ1,2}$ (1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ} (1)	Chip Select to Output in High Z	–	20	–	25	–	30	–	35	–	40	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{PU} (1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD} (1)	Chip Deselect to Power Down Time	–	25	–	30	–	35	–	45	–	55	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	55	–	ns
t_{CW}	Chip Selection to End of Write	25	–	25	–	30	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	25	–	25	–	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	25	–	35	–	45	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ} (1)	Write Enable to Output in High Z	–	20	–	25	–	25	–	30	–	30	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	20	–	25	–	25	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	5	–	ns
t_{OW} (1)	Output Active from End of Write	0	–	0	–	0	–	0	–	0	–	ns

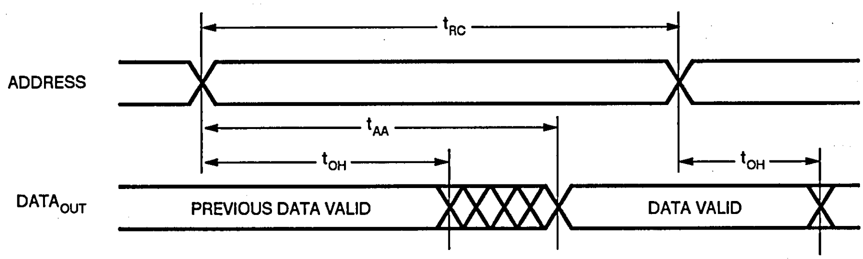
NOTE:

1. This parameter guaranteed but not tested.

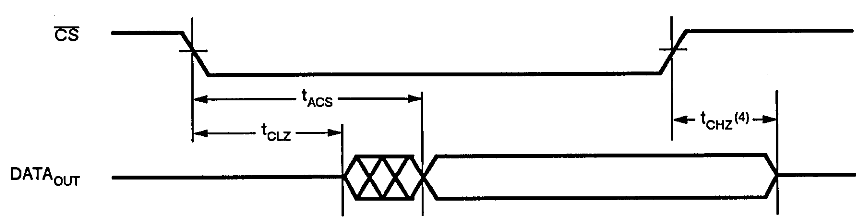
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 3]



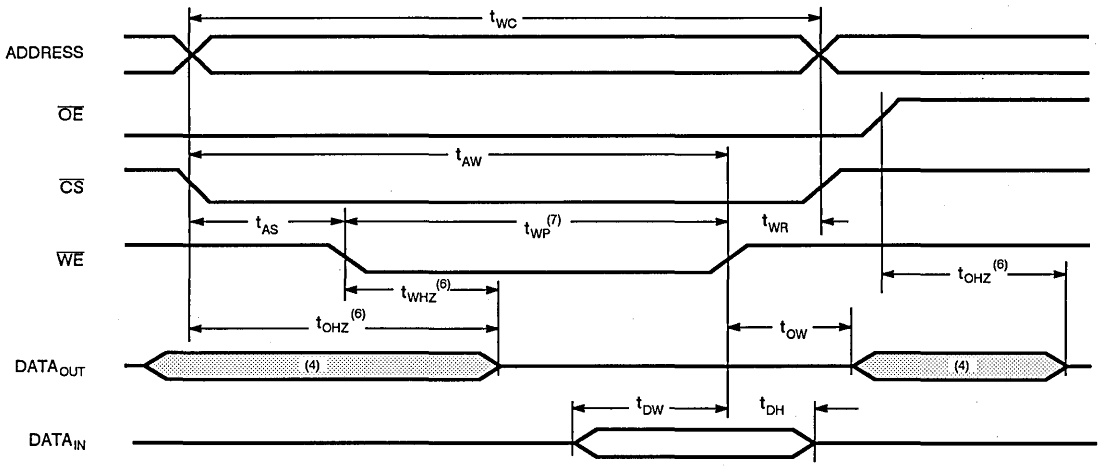
TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3]



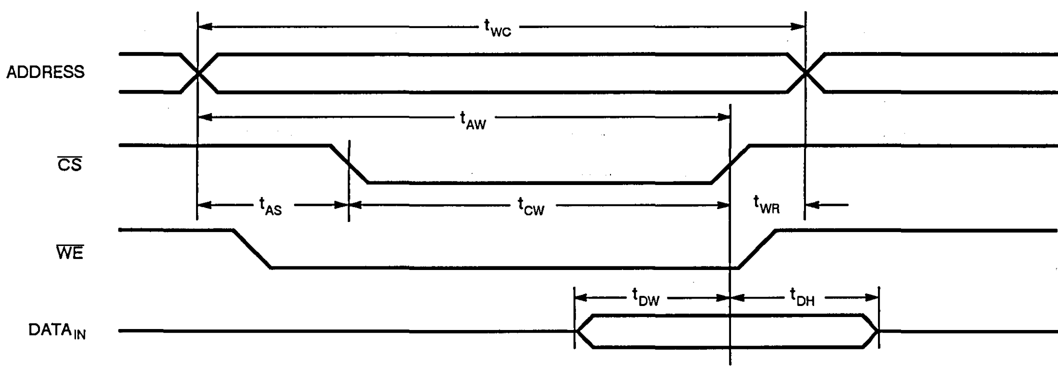
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL} .
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



13

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION

IDT XXXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
Package	S	Plastic SIP
Speed	25 30 35 45 55	Speed in Nanoseconds
Power	S	Standard Power
Device Type	8MP456	64K x 4-bit

CMOS STATIC RAM PLASTIC SIP MODULE (16K x 5-BIT)

IDT7MP564

Integrated Device Technology, Inc.

FEATURES:

- 81,920-bit CMOS static RAM module with decoupling capacitor
- High speed: 20ns max.
- Low power consumption: 1.1W typ.
- IDT7MP564 package options reduce overall height
- Utilizes IDT6167s—high-performance 16K RAMs produced with advanced CEMOS™
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

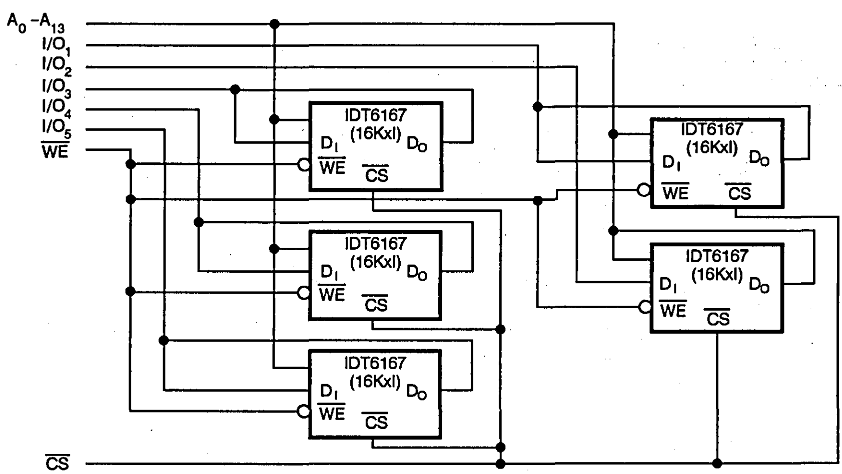
DESCRIPTION:

The IDT7MP564 is an 80K (16,384 x 5-bit) high-speed CMOS static RAM constructed on an epoxy laminate substrate using 5 IDT6167 (16,384 x 1-bit) CMOS static RAMs in plastic surface mount packages. Extremely fast speeds can be achieved with this technique due to use of the IDT6167 RAMs, fabricated in IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 16K static RAMs available.

The IDT7MP564 is available with access times as fast as 20ns, with maximum power consumption of only 2.2 watts. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit automatically goes to, and remains in, a standby mode as long as $\overline{CS}$ remains high, consuming only 963mW maximum. Substantially lower power levels can be achieved in the I_{SB1} mode (less than 138mW max.).

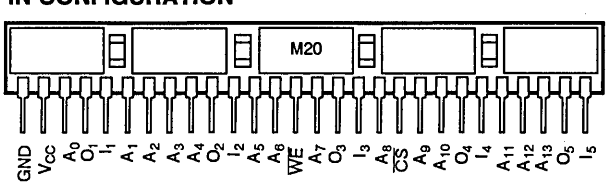
All inputs and outputs of the IDT7MP564 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



13

PIN CONFIGURATION



SIP SIDE VIEW

PIN NAMES

$A_0 - A_{13}$	Addresses	$\overline{WE}$	Write Enable
$I/O_1 - I/O_5$	Data Inputs/Outputs	V_{CC}	Power
$\overline{CS}$	Chip Select	GND	Ground

CEMOS is a trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE **DECEMBER 1987**

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = −1.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MP564 MIN.	TYP.[1]	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	–	15	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	–	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = 0	–	200	400	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = f_{MAX}	–	200	400	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$	–	80	175	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $\leq$ 0.2V	–	5	25	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4	–	–	V

NOTES:
1. V_{CC} = 5V, T_A = +25°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A=+25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	22	pF

NOTE:
1. This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

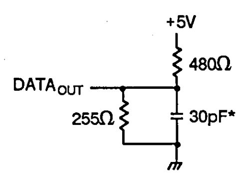


Figure 1. Output Load

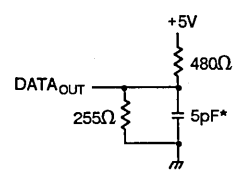


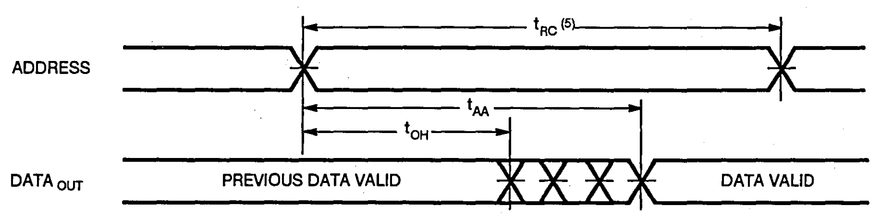
Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig

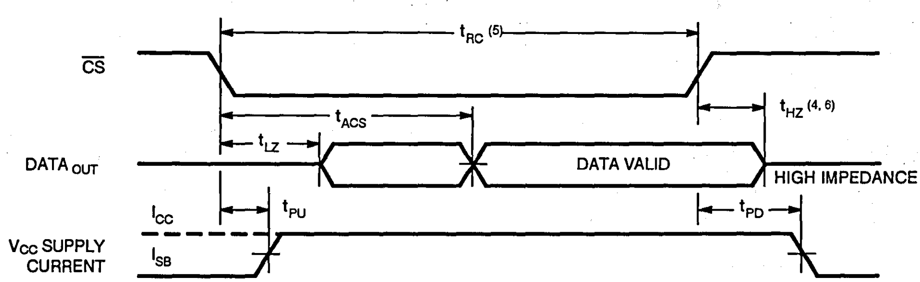
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7MP564L20 MIN.	IDT7MP564L20 MAX.	IDT7MP564L25 MIN.	IDT7MP564L25 MAX.	IDT7MP564L35 MIN.	IDT7MP564L35 MAX.	IDT7MP564L45 MIN.	IDT7MP564L45 MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	20	–	25	–	35	–	45	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	35	–	45	ns
t_{ACS}	Chip Select Access Time	–	20	–	25	–	35	–	45	ns
t_{OH}	Output Hold from Address Change	3	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Select to Output in Low Z	3	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselect to Output in High Z	–	10	–	10	–	15	–	20	ns
t_{PU}	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time	–	20	–	25	–	35	–	45	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	20	–	25	–	35	–	45	–	ns
t_{CW}	Chip Select to End of Write	15	–	20	–	30	–	40	–	ns
t_{AW}	Address Valid to End of Write	15	–	20	–	30	–	40	–	ns
t_{AS}	Address Set-up Time	2	–	3	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	13	–	17	–	25	–	35	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	3	–	ns
t_{DW}	Data Valid to End of Write	13	–	15	–	20	–	25	–	ns
t_{DH}	Data Hold Time	2	–	3	–	3	–	3	–	ns
t_{WZ}	Write Enable to Output in High Z	–	7	–	10	–	15	–	20	ns
t_{OW}	Output Active from End of Write	0	–	0	–	0	–	0	–	ns

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]



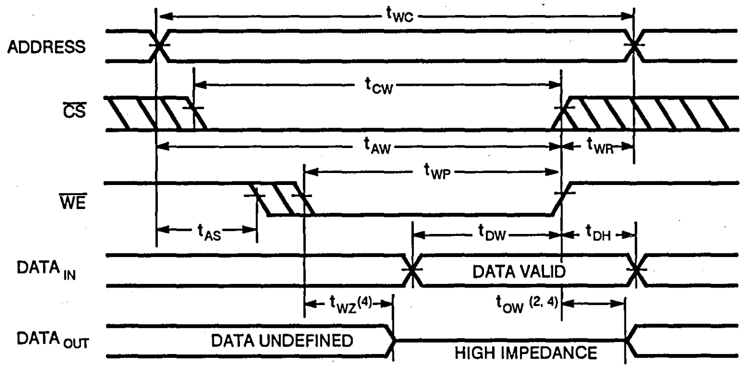
TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]



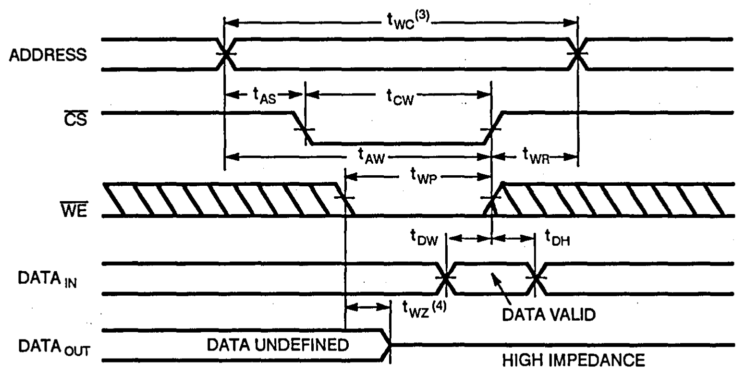
NOTES:
1. $\overline{WE}$ is high for read cycle.
2. $\overline{CS}$ is low for read cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. For any given speed, operating voltage and temperature, t_{HZ} will be less than or equal to t_{LZ}.

13

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



NOTES:

1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. IF $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

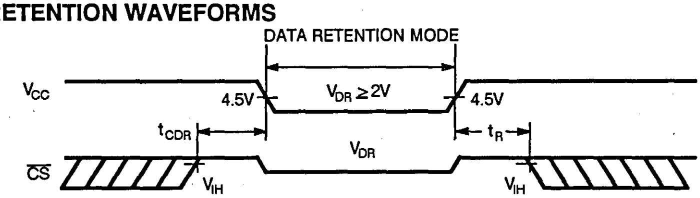
LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $\leq$ 0.2V	– –	10[2] 15[3]	300[2] 400[3]	µA
t_{CDR}	Chip Deselect to Data Retention Time		0	–	–	ns
t_R	Operation Recovery Time		t_{RC}[4]	–	–	ns

NOTES:

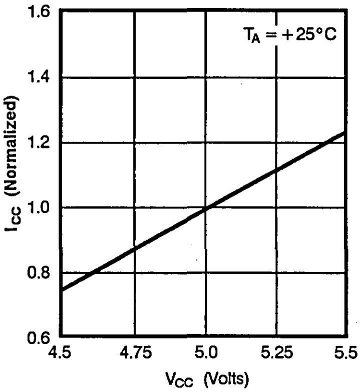
1. T_A = +25°C
2. @ V_{CC} = 2V
3. @ V_{CC} = 3V
4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORMS

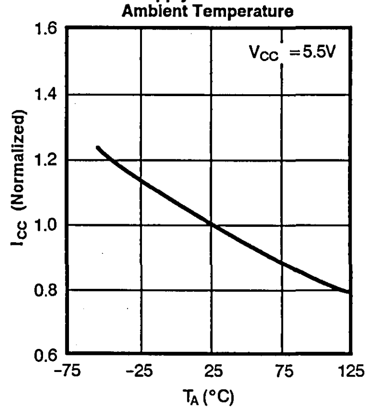


NORMALIZED TYPICAL PERFORMANCE CHARACTERISTICS

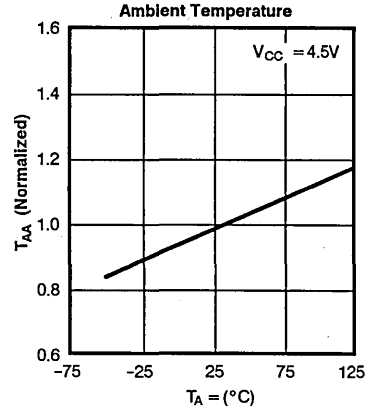
Supply Current vs. Voltage



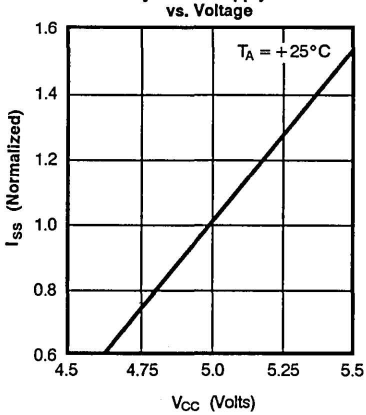
Supply Current vs. Ambient Temperature



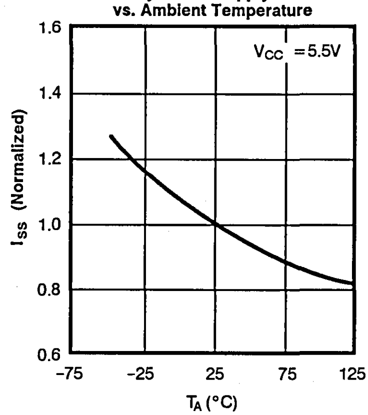
Address Access Time vs. Ambient Temperature



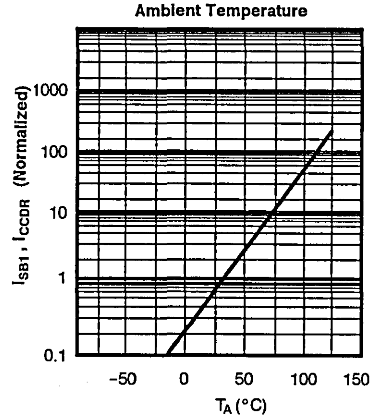
Standby Power Supply Current vs. Voltage



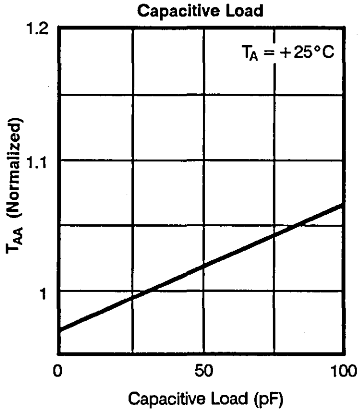
Standby Power Supply Current vs. Ambient Temperature



Full Standby Power Supply Current Data Retention Current vs. Ambient Temperature



Address Access Time vs. Capacitive Load



13

ORDERING INFORMATION

IDT	XXXX	A	999	A	A
	Device Type	Power	Speed	Package	Process/ Temperature Range

BLANK	Commercial (0°C to +70°C)
S	Plastic SIP
20 25 35 45	Speed in Nanoseconds
L	Low Power
7MP564	16K x 5-Bit Static RAM Module

Integrated Device Technology, Inc.

4 MEGABIT (512K x 8) CMOS STATIC RAM PLASTIC SIP MODULE

IDT7MP4008S

FEATURES:

- High-density 4 megabit (512K x 8) CMOS static RAM module
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Available in 36-pin SIP (single in-line package) for maximum space saving
- Fast access times
  - 45ns (max.)
- Low power consumption
  - Dynamic: 2.6W (max.)
  - Full standby: 1.9 (max.)
- CEMOS ™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

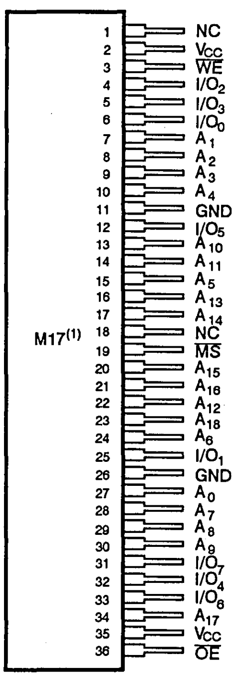
The IDT7MP4008 is a 4 megabit (512K x 8-bit) high-speed static RAM module constructed on an epoxy laminate surface using sixteen IDT71256 32K x 8 static RAMs in plastic surface mount packages. Extremely fast speeds can be achieved with this technique due to the use of 256K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS technology.

The 7MP family of surface mounted SIP technology is a cost-effective solution allowing for very high packing density. The IDT7MP4008 is offered in a 36-pin SIP. The 7MP4008 can be stacked on 300 mil centers, yielding greater than 12 megabits of RAM in less than 5 square inches of board space.

The IDT7MP4008 is available with maximum access times as fast as 45ns with maximum power consumption of 2.6 watts. The IDT7MP4008 also offers a full standby mode of 1.9W (max.).

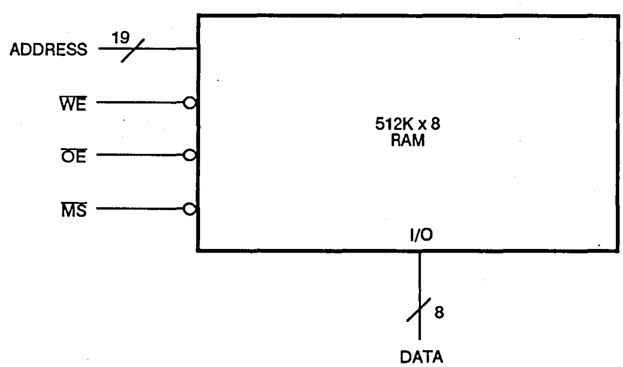
All inputs and outputs of the IDT7MP4008 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

PIN CONFIGURATION



SIP SIDE VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{0-18}	Addresses
I/O_{0-7}	Data Inputs/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{MS}$	Module Select
V_{CC}	Power
GND	Ground

13

NOTE:

1. For module dimensions, please refer to module drawing M17 in the packaging section.

COMMERCIAL TEMPERATURE RANGE **DECEMBER 1987**

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ±10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MP4008S MIN.	IDT7MP4008S MAX.	UNIT
$\lvert I_{LI} \rvert$	Input Leakage Current [1]	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	80	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open f = 0	—	390	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	—	470	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ or (TTL Level) V_{CC} = Max. Output Open	—	350	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{HC}$, $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$ V_{CS} = Max., Output Open	—	350	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

NOTE:

1. $\lvert I_{LI} \rvert$ for A_{15} - A_{18} and $\overline{MS}$ = 400 µA (max.).

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

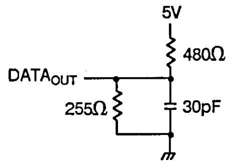


Figure 1. Output Load

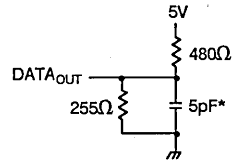


Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

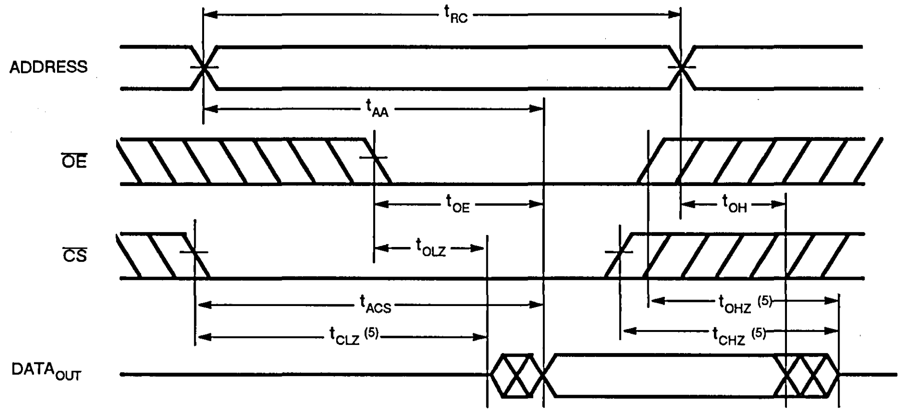
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7MP4008S45 MIN.	IDT7MP4008S45 MAX.	IDT7MP4008S55 MIN.	IDT7MP4008S55 MAX.	IDT7MP4008S70 MIN.	IDT7MP4008S70 MAX.	UNIT
READ CYCLE								
t_{RC}	Read Cycle Time	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time	–	45	–	55	–	70	ns
$t_{CLZ1,2}$ (1)	Chip Select to Output in Low Z	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	20	–	25	–	30	ns
t_{OLZ} (1)	Output Enable to Output in Low Z	0	–	0	–	0	–	ns
t_{CHZ} (1)	Chip Select to Output in High Z	–	25	–	30	–	35	ns
t_{OHZ} (1)	Output Disable to Output in High Z	–	25	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	–	55	–	70	–	ns
t_{CW}	Chip Selection to End of Write	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	35	–	45	–	55	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	10	–	ns
t_{WHZ} (1)	Write Enable to Output in High Z	–	15	–	20	–	25	ns
t_{DW}	Data Valid to End of Write	20	–	25	–	30	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	ns
t_{OW} (1)	Output Active from End of Write	5	–	5	–	5	–	ns

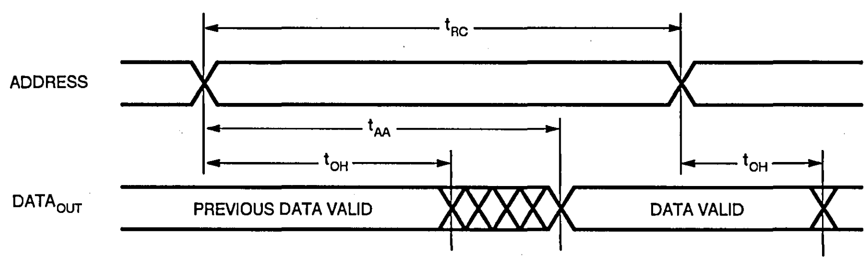
NOTE:
1. This parameter guaranteed but not tested.

13

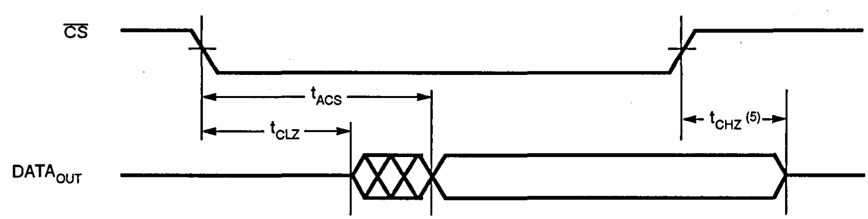
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1,2,4]

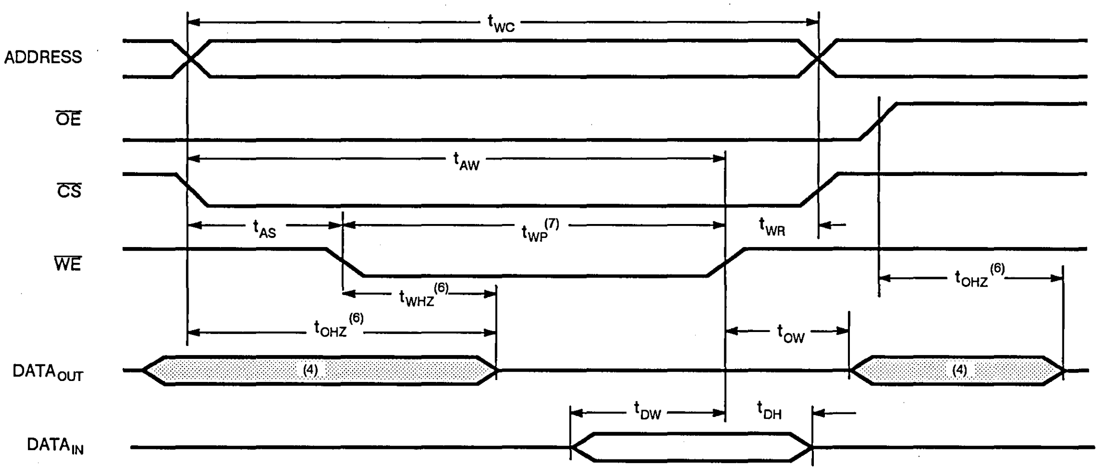


TIMING WAVEFORM OF READ CYCLE NO. 3[1,3,4]

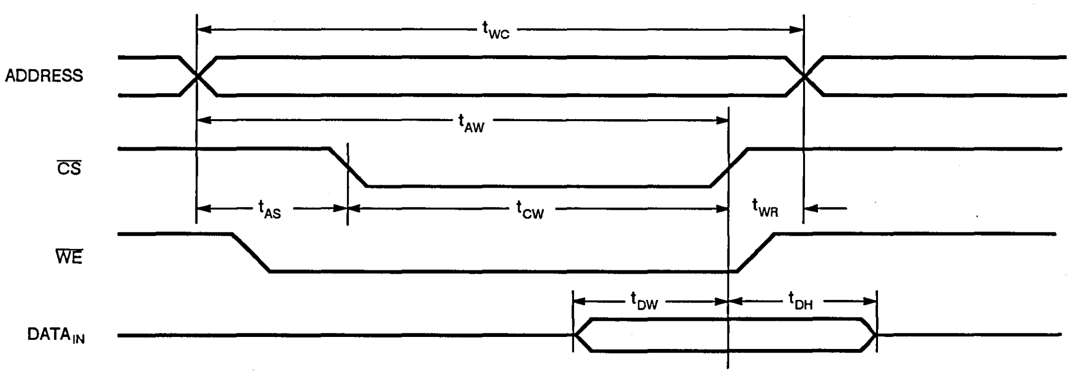


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

13

TRUTH TABLE

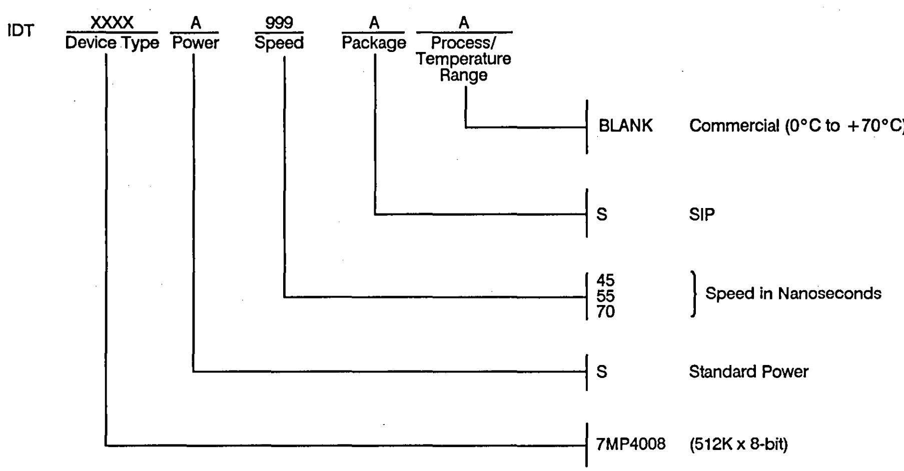
MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Read	L	H	H	High Z	Active
Write	L	X	L	$DATA_{IN}$	Active

CAPACITANCE ($T_A = +25°C$, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	96	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	128	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

1 MEGABIT CMOS STATIC RAM MODULE

IDT7M624S

FEATURES:

- High-density 1024K-bit CMOS static RAM module
- Customer-configured to 64K x 16, 128K x 8 or 256K x 4
- Fast access times
  - Military: 35ns (max.)
  - Commercial: 25ns (max.)
- Low power consumption
  - Active: 4.8W (typ. in 64K x 16 organization)
  - Standby: 1.6mW (typ.)
- Utilizes 16 IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Pin-compatible with IDT7M656 (256K RAM module)
- Single 5V(±10%) power supply
- Dual GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT7M624 is a 1024K-bit high-speed CMOS static RAM constructed on a multi-layered ceramic substrate using 16 IDT7187 64K x 1 static RAMs in leadless chip carriers. Making four chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 64K x 16, 128K x 8 or 256K x 4 organization. In addition, extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

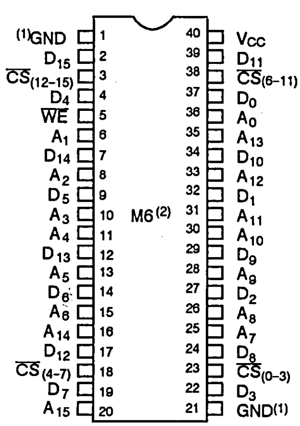
The IDT7M624 is available with access times as fast as 25ns commercial and 35ns military temperature range, with maximum operating power consumption of only 12.3W (significantly less if organized 128K x 8 or 256K x 4). The module also offers a standby power mode of 5.7W (max.) and a full standby mode of 1.7W (max.).

The IDT7M624 is offered in a 40-pin, 900 mil center sidebraze DIP to take advantage of the compact IDT7187s in leadless chip carriers.

All inputs and outputs of the IDT7M624 are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access times for ease of use.

All IDT military module semiconductor components are compliant with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

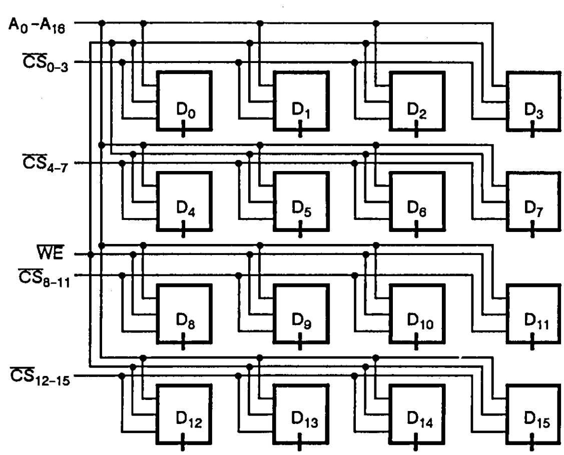


DIP
TOP VIEW

PIN NAMES

A_{0-16}	Address
D_{0-15}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

FUNCTIONAL BLOCK DIAGRAM



13

NOTES:

1. Both GND pins need to be grounded for proper operation.
2. For module dimensions, please refer to module drawing M6 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M624S MIN.	TYP.[1]	MAX.[3]	MAX.[4]	UNIT
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	–	–	20	20	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	V_{CC} = 5.5V, $\overline{CS}_{XX}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	20	20	µA
I_{CCX16}	Operating Current in X16 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = f_{MAX}	–	960	1950	2240	mA
I_{CCX8}	Operating Current in X8 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, Min. Duty Cycle = 100%	–	720	1380	1640	mA
I_{CCX4}	Operating Current in X4 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, Min. Duty Cycle = 100%	–	600	1100	1340	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}_{XX}$ ≥ V_{IH} (TTL Level), V_{CC} = 5.5V, Output Open	–	480	820	1040	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}_{XX}$ ≥ V_{CC} -0.2V, V_{IN} ≥ V_{CC} -0.2V or ≤ 0.2V (CMOS Level)	–	0.32	320[2]	320	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = 4.5V	–	–	0.5	0.5	V
		I_{OL} = 8mA, V_{CC} = 4.5V	–	–	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = 4.5V	2.4	–	–	–	V

NOTES:
1. Typical limits are at V_{CC} = 5.0V, +25°C.
2. I_{SB1} max. at commercial temperature = 240mA.
3. t_{AA} = 30, 35, 45, 55, 65ns
4. t_{AA} = 25ns

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

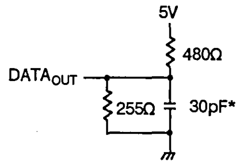


Figure 1. Output Load

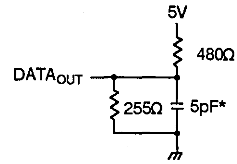


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = –55°C to +125°C and 0°C to 70°C)

SYMBOL	PARAMETER	7M624S25 COM'L. ONLY MIN.	7M624S25 COM'L. ONLY MAX.	7M624S30 COM'L. ONLY MIN.	7M624S30 COM'L. ONLY MAX.	7M624S35 MIN.	7M624S35 MAX.	7M624S45 MIN.	7M624S45 MAX.	7M624S55 MIN.	7M624S55 MAX.	7M624S65 MIN.	7M624S65 MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	55	–	65	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	–	55	–	65	ns
t_{ACS}	Chip Select Access Time	–	25	–	30	–	35	–	45	–	55	–	65	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Selection to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselection to Output in High Z	–	20	–	25	–	30	–	30	–	30	–	30	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Selection to Power Down Time	–	25	–	30	–	35	–	35	–	35	–	35	ns

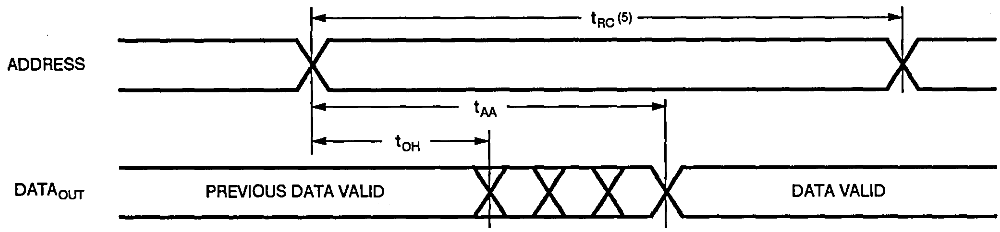
AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = –55°C to +125°C and 0°C to 70°C)

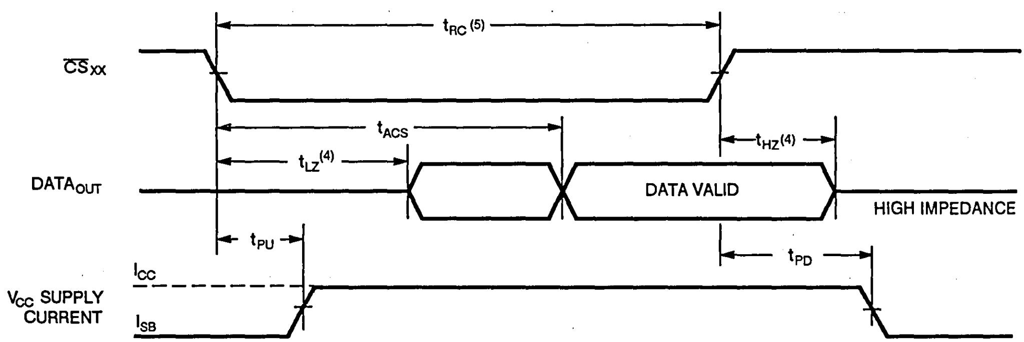
SYMBOL	PARAMETER	7M624S25 COM'L. ONLY MIN.	7M624S25 COM'L. ONLY MAX.	7M624S30 COM'L. ONLY MIN.	7M624S30 COM'L. ONLY MAX.	7M624S35 MIN.	7M624S35 MAX.	7M624S45 MIN.	7M624S45 MAX.	7M624S55 MIN.	7M624S55 MAX.	7M624S65 MIN.	7M624S65 MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	55	–	65	–	ns
t_{CW}	Chip Selection to End of Write	22	–	25	–	30	–	40	–	50	–	55	–	ns
t_{AW}	Address Valid to End of Write	22	–	25	–	30	–	40	–	50	–	55	–	ns
t_{AS}	Address Set-up Time	2	–	3	–	5	–	5	–	5	–	10	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	25	–	30	–	35	–	40	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	15	–	20	–	20	–	25	–	25	–	30	–	ns
t_{DH}	Data Hold Time	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{WZ}	Write Enable to Output in High Z	0	20	0	25	0	25	0	30	0	30	0	35	ns
t_{OW}	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	5	–	ns

13

TIMING WAVEFORM OF READ CYCLE NO. 1 (1, 2)

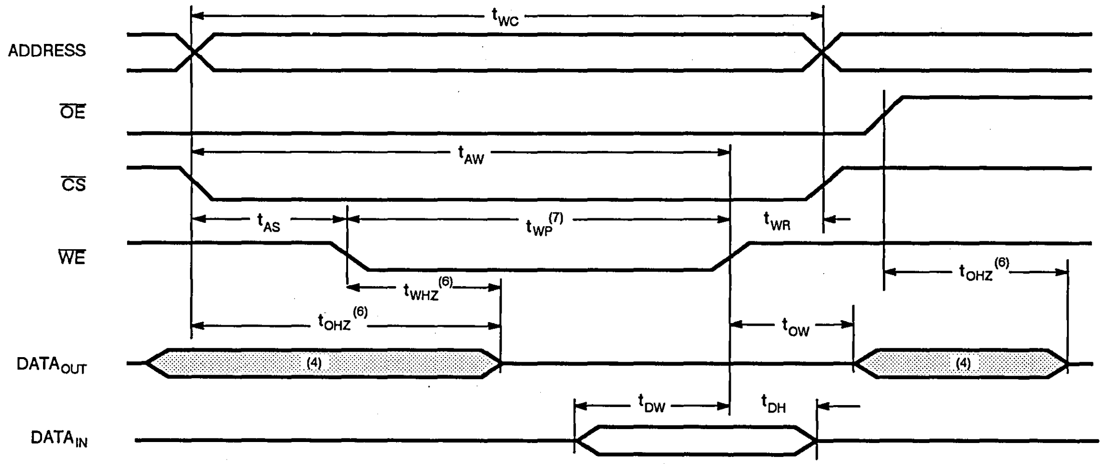


TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 3)

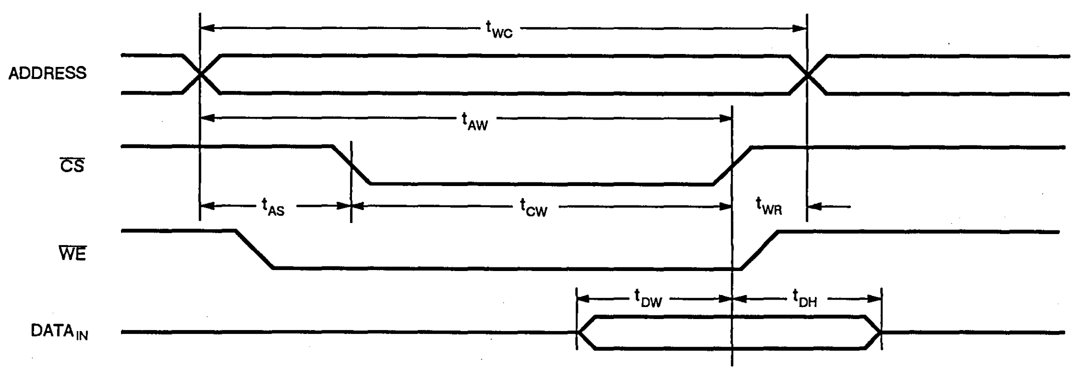


NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}_{XX}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}_{XX}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



13

NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TRUTH TABLE

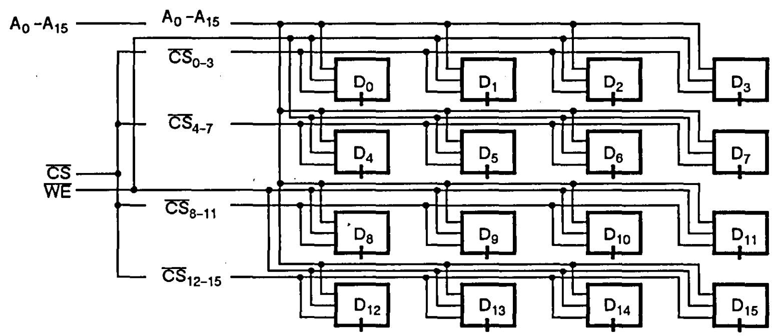
MODE	$\overline{CS}_{XX}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	High Z	Active

CAPACITANCE ($T_A = +25°C$, f = 1.0MHz)

SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	130	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	35	pF

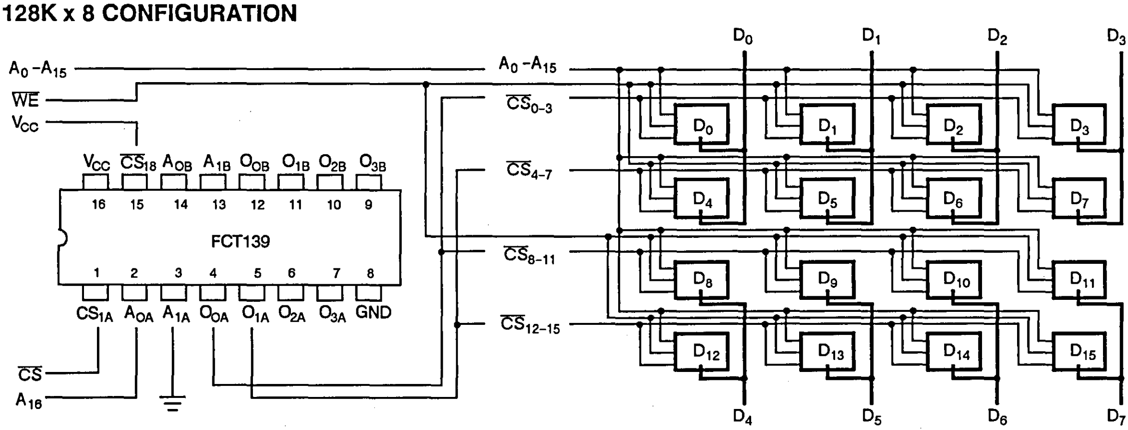
NOTE:
1. This parameter is sampled and not 100% tested.

IDT7M624
64K x 16 CONFIGURATION



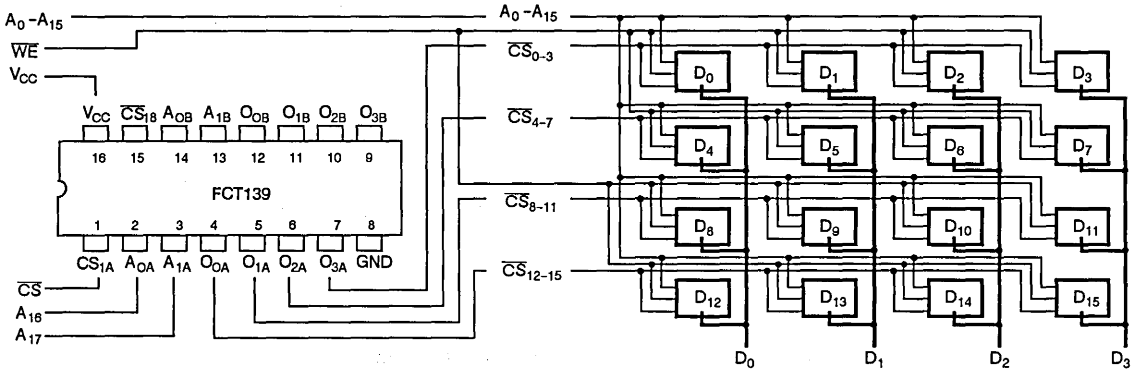
NOTE:
All chip selects tied together since, in a by 16 configuration, all chips are either on or off.

IDT7M624
128K x 8 CONFIGURATION



NOTE:
The chip selects are tied together in groups of two. The decoder uses the new higher order address pin (A_{16}) to determine which of the two banks of memory are enabled.

IDT7M624
256K x 4 CONFIGURATION



NOTE:
Each chip is now controlled by the two higher order address pins A_{16} and A_{17}.

ORDERING INFORMATION

IDT XXXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Semiconductor Components Compliant to MIL-STD-883, Class B
Package	C	Sidebraze DIP
Speed	25	Commercial Only
	30	Commercial Only
	35	
	45	
	55	
	65	
		Speed in Nanoseconds
Power	S	Standard Power
Device Type	7M624	1 Megabit (1024K-Bit)

13

256K CMOS STATIC RAM MODULE

IDT7M656L

Integrated Device Technology, Inc.

FEATURES:

- High-density 256K-bit CMOS static RAM module
- Customer-configured to 16Kx16, 32Kx8 or 64Kx4
- Fast access times
  - Military: 20ns
  - Commercial: 15ns
- Low power consumption
  - Active: 3.2mW (typ.) (in 16K x 16 organization)
  - Standby: 0.16mW (typ.)
- Utilizes 16 IDT6167s high-performance 16K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Single 5V (±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Module available with semiconductor components compliant to MIL-STD-883, Class B.

DESCRIPTION:

The IDT7M656 is a 256K-bit high-speed CMOS static RAM constructed on a multilayered ceramic substrate using 16 IDT6167 (16Kx1) static RAMs in leadless chip carriers. Making 4 chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 16Kx16, 32Kx8 or 64Kx4 organization. In addition, extremely high speeds are achievable by the use of IDT6167s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides some of the fastest 16K static RAMs available.

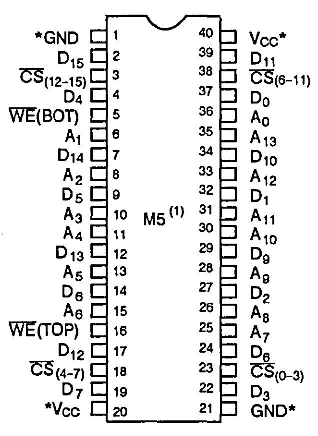
The IDT7M656 is available with access times as fast as 15ns commercial and 20ns military temperature range, with maximum operating power consumption of only 7.9W (significantly less if organized 32Kx8 or 64Kx4). The RAM module also offers a maximum standby power mode of 3.0W and a maximum full standby mode of 176mW.

The IDT7M656 is offered in a high-density 40-pin, 900 mil center sidebraze DIP to take full advantage of the compact IDT6167s in leadless chip carriers.

All inputs and outputs of the IDT7M656 are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

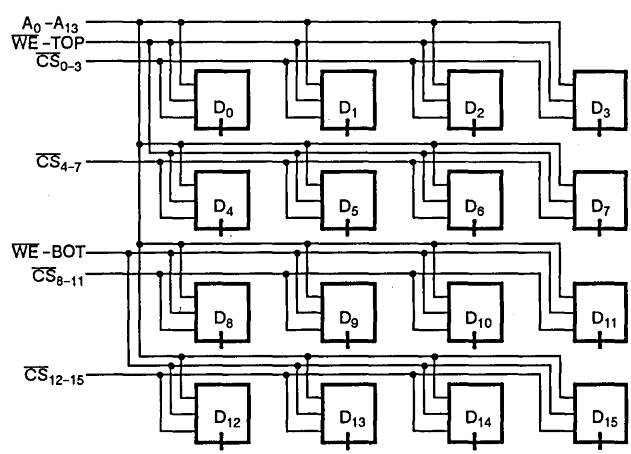
PIN CONFIGURATION



DIP
TOP VIEW

1. For module dimensions, please refer to module drawing M5 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{xx}	Addresses	D_{xx}	$DATA_{IN/OUT}$
$\overline{CS}_{xx}$	Chip Selects	V_{CC}	Power
$\overline{WE}_{xx}$	Write Enable	GND	Ground

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC}= 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M656L MIN.	TYP.[1]	MAX.[3]	MAX.[4]	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} =5.5V, V_{IN} = 0V to V_{CC}	–	–	20	20	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}=V_{IH}$, V_{OUT} = 0V to V_{CC}	–	–	20	20	µA
I_{CCX16}	Operating Current in X16 mode	$\overline{CS}_{xx}$ = V_{IL}, Output Open, V_{CC}= 5.5V, f=f_{MAX}	–	640	1280	1440	mA
I_{CCX8}	Operating Current in X8 mode	$\overline{CS}_{xx}$ = V_{IL}, Output Open, V_{CC}= 5.5V, f=f_{MAX}	–	420	840	920	mA
I_{CCX4}	Operating Current in X4 Mode	$\overline{CS}_{xx}$ = V_{IL}, Output Open, V_{CC}= 5.5V, f=f_{MAX}	–	310	620	660	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}_{xx}$ ≥ V_{CC} (TTL Level), V_{CC} =5.5V, Output Open	–	200	400	560	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}_{xx}$ ≥ V_{CC} -0.2V (CMOS Level V_{IN} ≥ V_{CC} -0.2V or <0.2V	–	0.032	15[2]	32	mA
V_{OL}	Output Low Voltage	I_{OL} =8mA	–	–	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4mA	2.4	–	–	–	V

NOTES:
1. V_{CC} = 5V, T_A=+25°C
2. I_{SB1} max. at commercial temperature = 5.0mA
3. t_{AA}=25, 35, 55, 65ns
4. t_{AA}=15, 20ns

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A= +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	200	pF
C_{OUT}[2]	Output Capacitance	V_{OUT} = 0V	60	pF

NOTE:
1. This parameter is determined by device characterization, but is not 100% tested.
2. For each output, 16K x 16 mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

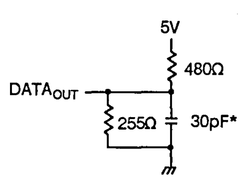


Figure 1. Output Load

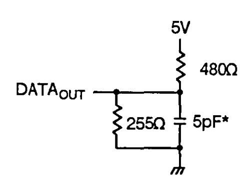


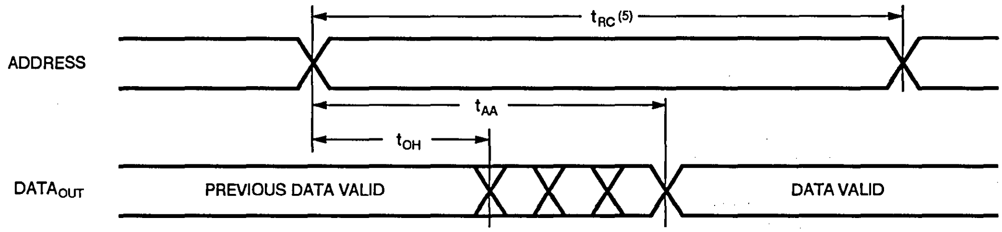
Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

* Including scope and jig.

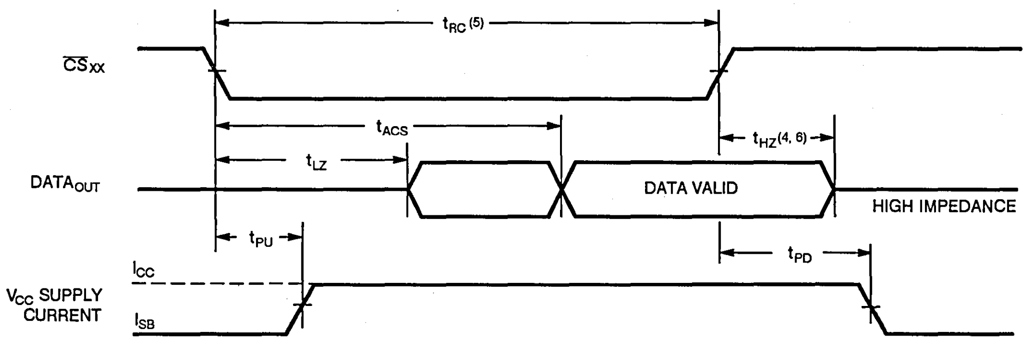
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7M656L15 (COM'L. ONLY)		IDT7M656L20		IDT7M656L25		IDT7M656L35		IDT7M656L55		IDT7M656L65		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	15	–	20	–	25	–	35	–	55	–	65	–	ns
t_{AA}	Address Access Time	–	15	–	20	–	25	–	35	–	55	–	65	ns
t_{ACS}	Chip Select Access Time	–	15	–	20	–	25	–	35	–	55	–	65	ns
t_{OH}	Output Hold from Address Change	3	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Selection to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselect to Output in High Z	–	10	–	15	–	15	–	20	–	40	–	40	ns
t_{PU}	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Select to Power Down Time	–	15	–	20	–	25	–	35	–	55	–	65	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	15	–	20	–	25	–	35	–	55	–	65	–	ns
t_{CW}	Chip Select to End of Write	15	–	20	–	20	–	30	–	45	–	55	–	ns
t_{AW}	Address Valid to End of Write	15	–	20	–	25	–	35	–	45	–	55	–	ns
t_{AS}	Address Set-up Time	2	–	2	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	13	–	17	–	20	–	30	–	35	–	40	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	13	–	15	–	15	–	20	–	25	–	30	–	ns
t_{DH}	Data Hold Time	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{IY}	Write Enable to Output in HIGH Z	–	10	–	10	–	10	–	15	–	40	–	40	ns
t_{WY}	Output Active from End of Write	0	–	0	–	0	–	0	–	0	–	0	–	ns

TIMING WAVEFORM OF READ CYCLE NO. 1 [1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 3]

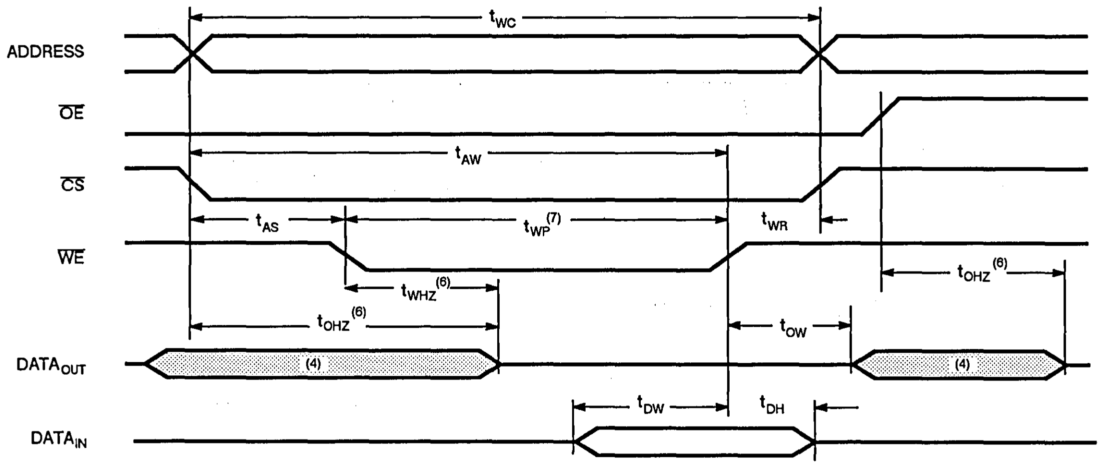


NOTES:

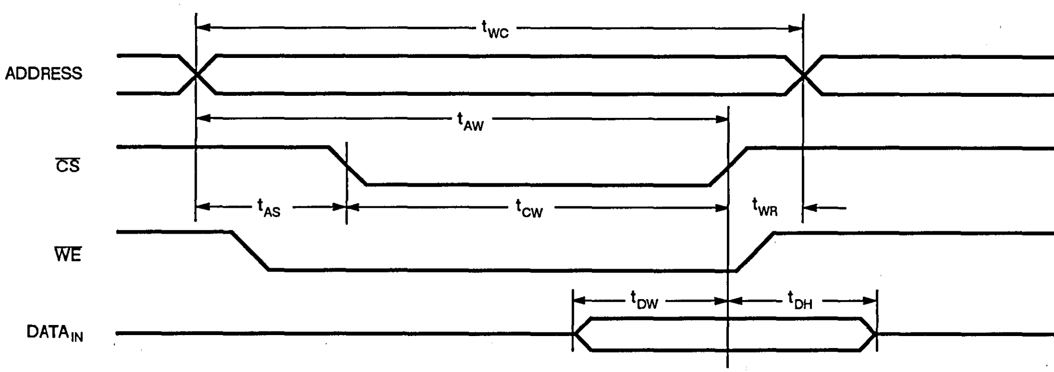
1. $\overline{WE}_{XX}$ is High for READ cycle.
2. $\overline{CS}_{XX}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}_{XX}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. For any given speed grade, operating voltage, and temperature, t_{HZ} will be less than or equal to t_{LZ}.

13

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1,2,3,7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1,2,3,5]



NOTES:

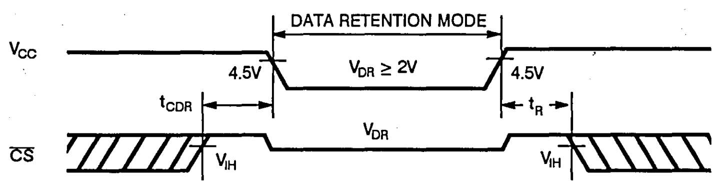
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

DATA RETENTION CHARACTERISTICS (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX. COM'L.	MAX. MIL.	UNIT
V_{DR}	V_{CC} for Retention Data	$\overline{CS}_{xx} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	2.0	–	–	–	V
I_{CCDR}	Data Retention Current		– –	.01(2) .02(3)	2.0(2) 3.0(3)	6.0 9.0	mA
t_{CDR}	Chip Deselect to Data Retention Time		0	–	–	–	ns
t_R	Operation Recovery Time		t_{RC}(4)	–	–	–	ns

NOTES:
1. T_A = +25°C.
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time.

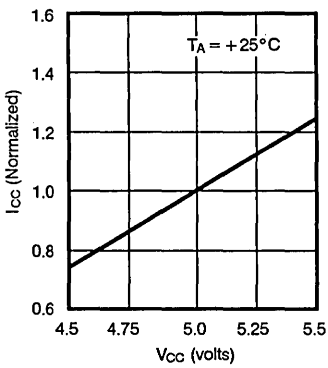
LOW V_{CC} DATA RETENTION WAVEFORM



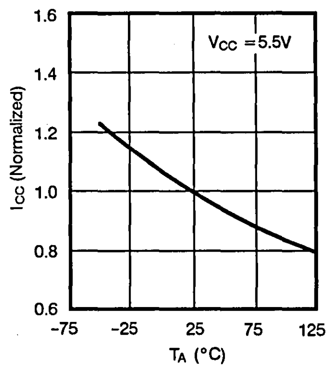
13

NORMALIZED TYPICAL PERFORMANCE CHARACTERISTICS

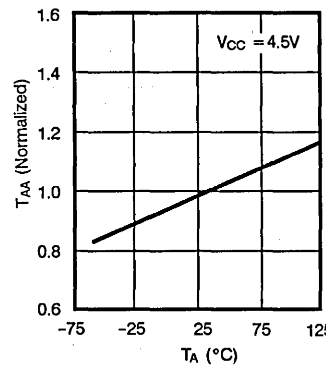
Supply Current vs. Voltage



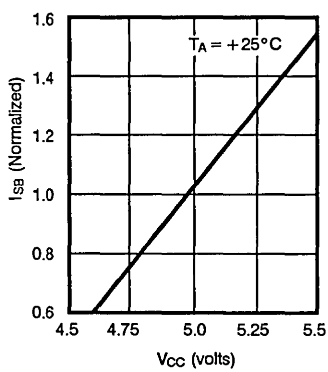
Supply Current vs. Ambient Temperature



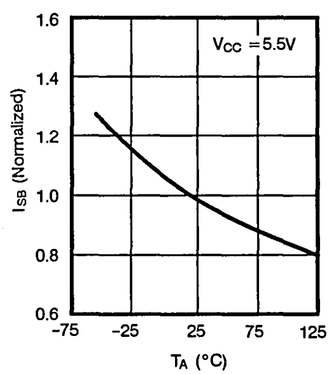
Address Access Time vs. Ambient Temperature



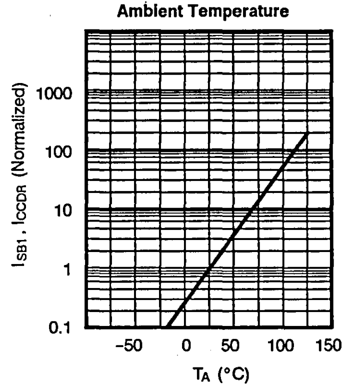
Stand-by-Power Supply Current vs. Voltage



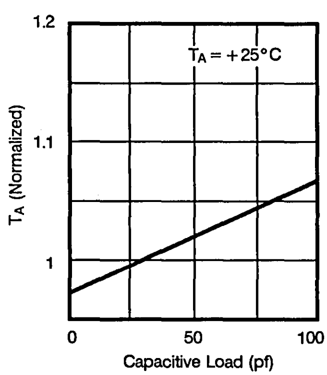
Stand-by-Power Supply Current vs. Ambient Temperature



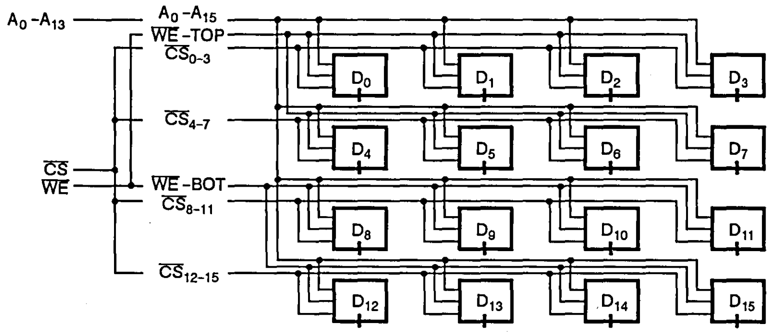
Full Stand-by Power Supply Current. Data Retention Current vs. Ambient Temperature



Address Access Time vs. Capacitive Load

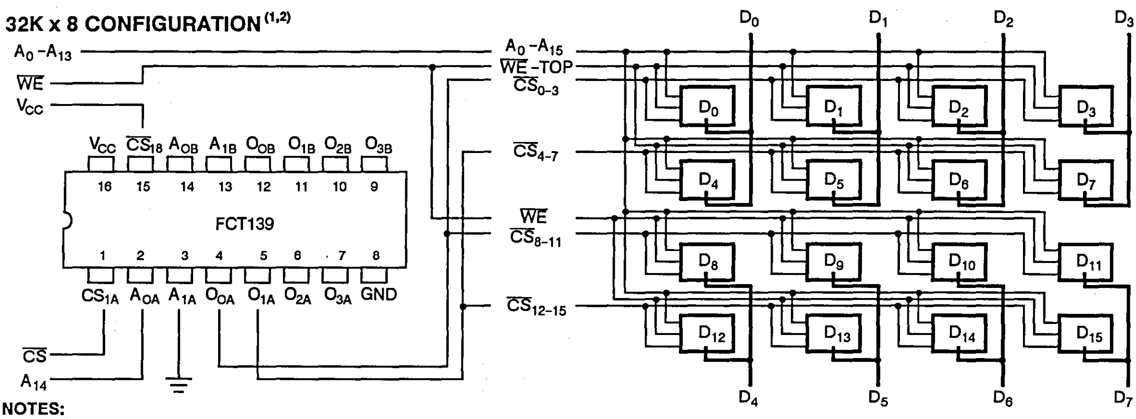


IDT7M656
16K x 16 CONFIGURATION[1,2]



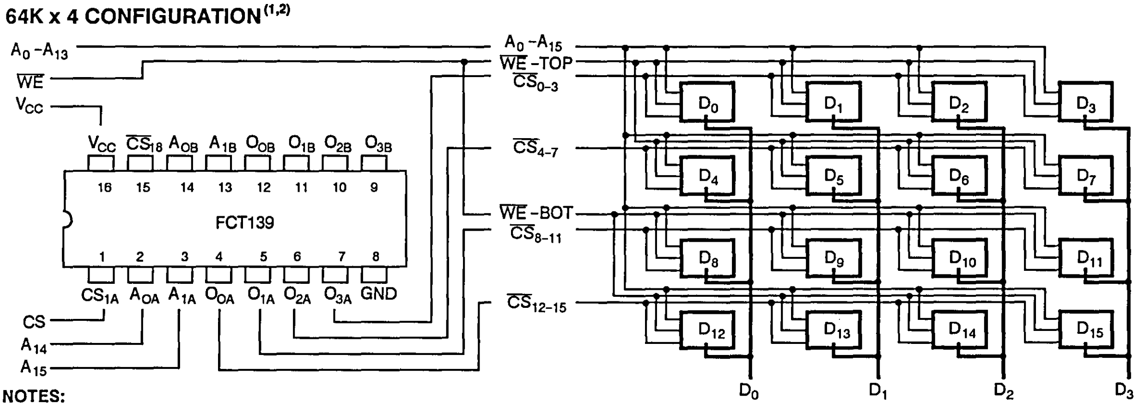
NOTES:
1. All chip selects tied together since, in a by-16 configuration, all chips are either on or off.
2. The two write enables are tied together allowing control of the write enable for entire memory at one time (necessary) in a by-16 organization since all chips are either writing or reading at any given time.

32K x 8 CONFIGURATION[1,2]



NOTES:
1. All chip selects tied together in groups of two. The decoder uses the new higher order address pin (A_{14}) to determine which of the two banks of memory are disabled.
2. The two write enables are tied together for ease of layout. They could be controlled by the decoder similar to the chip selects but would save only a minimal amount of power and add complexity to the layout.

64K x 4 CONFIGURATION[1,2]



NOTES:
1. Each chip select is now controlled by the two higher order address pins A $_{14}$(necessary in 64K deep memory).
2. Again the two write enables are tied together for ease of layout (the megabit part will only have one write enable pin).

13

ORDERING INFORMATION

IDT XXXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Semiconductor Components Compliant to MIL-STD-883
Package	C	Sidebraze DIP
Speed	15	Commercial Only; Speed in Nanoseconds
	20	Speed in Nanoseconds
	25	Speed in Nanoseconds
	35	Speed in Nanoseconds
	55	Speed in Nanoseconds
	65	Speed in Nanoseconds
Power	L	Low Power
Device Type	7M656	256K

Integrated Device Technology, Inc.

512K (64K x 8-BIT or 64K x 9-BIT) CMOS STATIC RAM MODULE

IDT7M812
IDT7M912

FEATURES:

- High-density 512K-bit CMOS static RAM module
- 64K x 8 (IDT7M812) or 64K x 9 (IDT7M912) configuration
- Fast access times
  - Military: 35ns (max.)
  - Commercial: 25ns (max.)
- Low power consumption
  - Active: 2.4W (typ. in 64K x 8 organization)
  - Standby: 240μW (typ. in 64K x 8 organization)
- Utilizes 8 (IDT7M812) or 9 (IDT7M912) IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in 40-pin, 600 mil center sidebraze DIP, achieving very high memory density
- Single 5V(±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT7M812/IDT7M912 are 512K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic substrate using 8 IDT7187 64K x 1 static RAMs (IDT7M812) or 9 IDT7187 static RAMs (IDT7M912) in leadless chip carriers. Extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

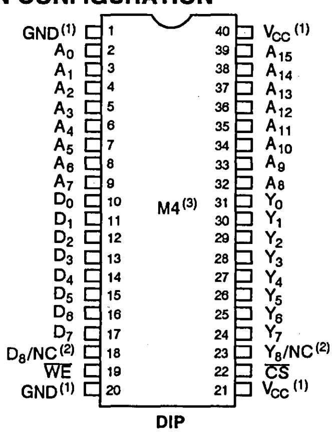
The IDT7M812/IDT7M912 are available with access times as fast as 25ns commercial and 35ns military temperature range, with maximum operating power consumption of only 6.9W (IDT7M912, 64K x 9 option). The module also offers a standby power mode of less than 3.2W (max.) and a full standby mode of 1.2W (max.).

The IDT7M812/IDT7M912 are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT7187s in leadless chip carriers. The IDT7M912 (64K x 9) option can provide more flexibility in system application for error detection, parity bit, etc.

All inputs and outputs of the IDT7M812/IDT7M912 are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing access and cycles times for ease of use.

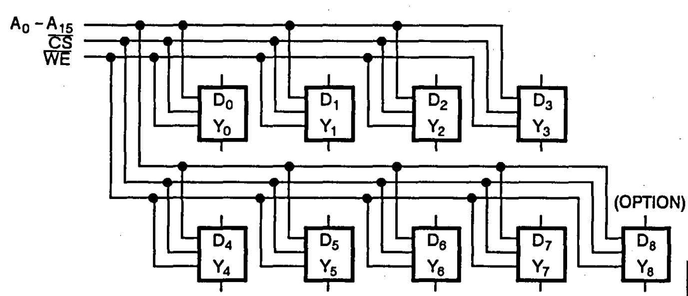
All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



13

PIN NAMES

A_0-A_{15}	Address
D_0-D_8	Data Input
Y_0-Y_8	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

NOTES:

1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. Pin 18 is D_8 and pin 23 is Y_8 in 64K x 9 (IDT7M912) option and both 18 and 23 are NC in 64K x 8 (IDT7M812) option.
3. For module dimensions, please refer to module drawing M4 in the packaging section.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M912 MIN.	IDT7M912 TYP.	IDT7M912 MAX.[3]	IDT7M912 MAX.[4]	IDT7M812 MIN.	IDT7M812 TYP.	IDT7M812 MAX.[3]	IDT7M812 MAX.[4]	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V; V_{IN} = GND to V_{CC}	–	–	20	20	–	–	20	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = 5.5V $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	20	20	–	–	20	20	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open Min. Duty Cycle = 100%	–	540	1080	1260	–	480	960	1120	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100% Output Open	–	540	1080	1530	–	480	960	1360	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ Min. Duty Cycle = 100%	–	270	450	585	–	240	400	520	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $\leq$ 0.2V	–	0.2	180[2]	225	–	0.05	160[2]	200	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	–	–	0.5	0.5	–	–	0.5	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	–	–	0.4	0.4	–	–	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	–	–	–	2.4	–	–	–	V

NOTES:
1. Typical limits are at V_{CC} = 5.0V, +25°C.
2. I_{SB1} (max.) of IDT7M812/912 at commercial temperature = 80mA/90mA.
3. t_{AA} = 30, 35, 45, 55ns
4. t_{AA} = 25ns

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

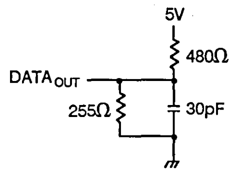


Figure 1. Output Load

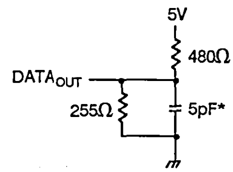


Figure 2. Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

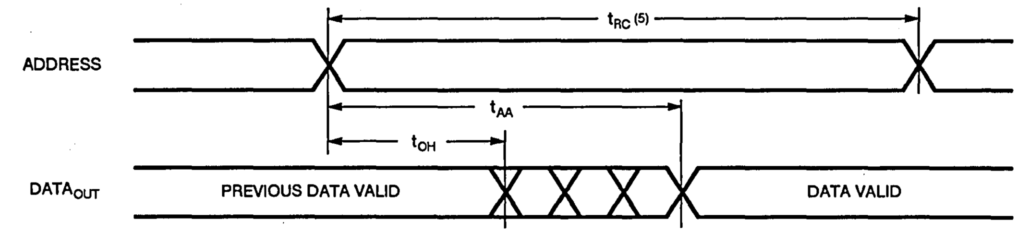
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

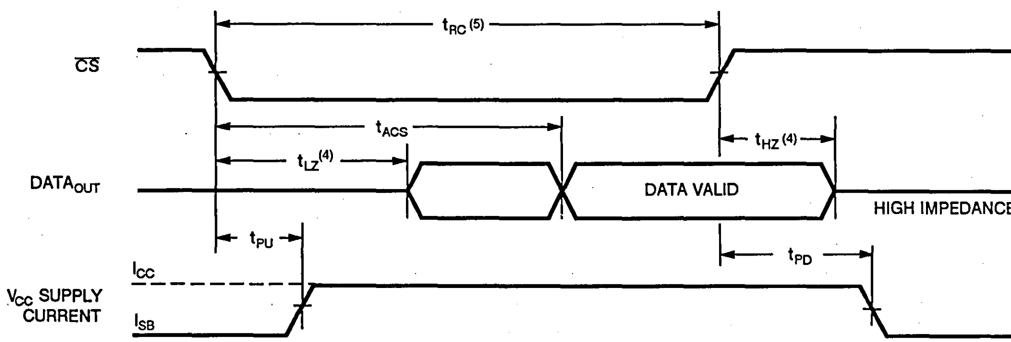
(V_{CC} = 5V ±10%, T_A = –55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	7M912S25 7M812S25 COM'L. ONLY		7M912S30 7M812S30 COM'L. ONLY		7M912S35 7M812S35		7M912S45 7M812S45		7M912S55 7M812S55		7M912S65 7M812S65		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	55	–	65	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	–	55	–	65	ns
t_{ACS}	Chip Select Access Time	–	25	–	30	–	35	–	45	–	55	–	65	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Selection to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselection to Output in High Z	–	20	–	25	–	25	–	30	–	30	–	30	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Selection to Power Down Time	–	25	–	30	–	35	–	35	–	35	–	35	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	55	–	65	–	ns
t_{CW}	Chip Selection to End of Write	23	–	28	–	35	–	40	–	50	–	55	–	ns
t_{AW}	Address Valid to End of Write	23	–	28	–	35	–	40	–	50	–	55	–	ns
t_{AS}	Address Set-up Time	3	–	3	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	20	–	25	–	30	–	30	–	35	–	40	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	15	–	20	–	20	–	25	–	25	–	30	–	ns
t_{DH}	Data Hold Time	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{WZ}	Write Enable to Output in High Z	0	20	0	25	0	25	0	30	0	30	0	35	ns
t_{OW}	Output Active from End of Write	0	–	0	–	0	–	0	–	0	–	0	–	ns

TIMING WAVEFORM OF READ CYCLE NO. 1 (1, 2)

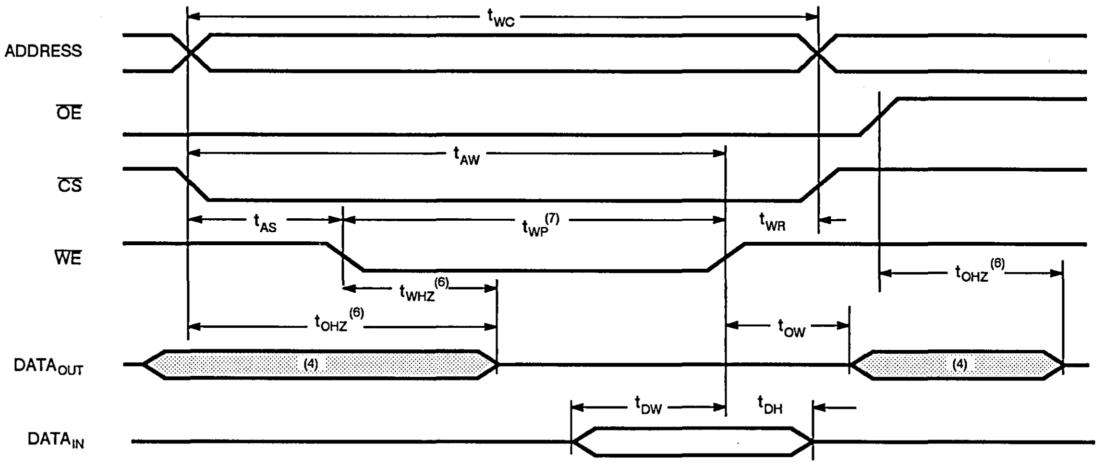


TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 3)

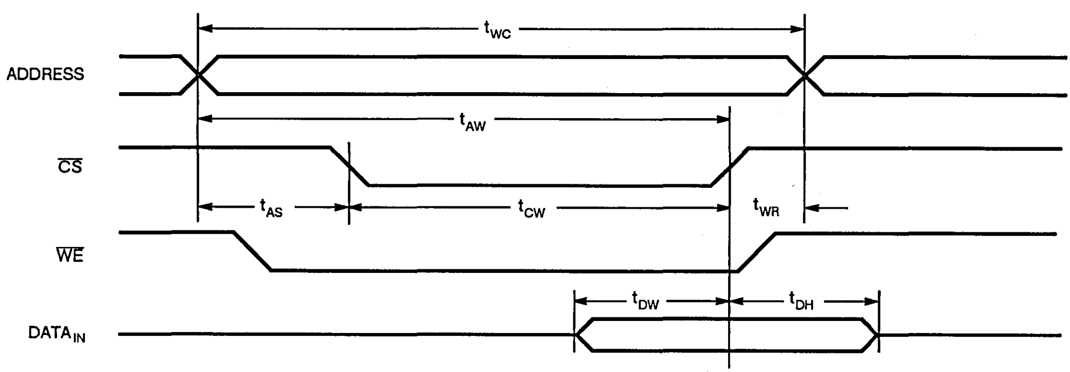


NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	80	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

NOTE:

1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION

IDT XXXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range:
- Blank — Commercial (0°C to +70°C)
- B — Military (–55°C to +125°C) Semiconductor Components Compliant to MIL-STD-883, Class B

Package:
- C — Sidebraze DIP

Speed (Speed in Nanoseconds):
- 25 — Commercial Only
- 30 — Commercial Only
- 35
- 45
- 55
- 65

Power:
- S — Standard Power

Device Type:
- 7M812 — 64K x 8-Bit
- 7M912 — 64K x 9-Bit

Integrated Device Technology, Inc.

256K (32K x 8-BIT) CMOS STATIC RAM MODULE

IDT7M856S

FEATURES:

- High-density 256K (32K x 8-bit) CMOS static RAM module
- Equivalent to JEDEC standard for future monolithic 32K x 8 static RAMs
- High-speed — 40ns (max.) commercial; 55ns (max.) military
- Low-power consumption; typically less than 1W operating, less than 1mW in standby
- Utilizes IDT7198s—high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Pin compatible with IDT7M864 (8K x 8 SRAM module)
- Offered in the JEDEC standard 28-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirements

DESCRIPTION:

The IDT7M856 is a 256K (32,768 x 8-bit) high-speed static RAM constructed on a co-fired ceramic substrate using four IDT7198 (16,384 x 4) static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic 256K static RAMs is achieved by utilization of an on-board decoder, used as an inverter, that interprets the higher order address A_{14} to select two of the four 16K x 4 RAMs. Extremely fast speeds can be achieved with this technique due to use of 64K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

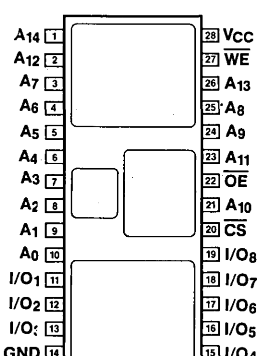
The IDT8M856 is available with maximum access times as fast as 40ns for commercial and 55ns for military temperature ranges, with maximum power consumption of only 2 watts. The circuit also offers a reduced power standby mode. When CS goes high, the circuit will automatically go to a standby mode with power consumption of only 1.1mW (max.). Substantially lower power levels can be achieved in a full standby mode (440mW max.).

The IDT8M856 is offered in a 28-pin, 600 mil center sidebraze DIP. This provides four times the density of the IDT7M864 (8K x 8 module) in the same socket with only minor pin assignment changes. In addition, the JEDEC standard for 256K monolithic pinouts has been adhered to, allowing for compatibility with future monolithics.

All inputs and outputs of the IDT7M856 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

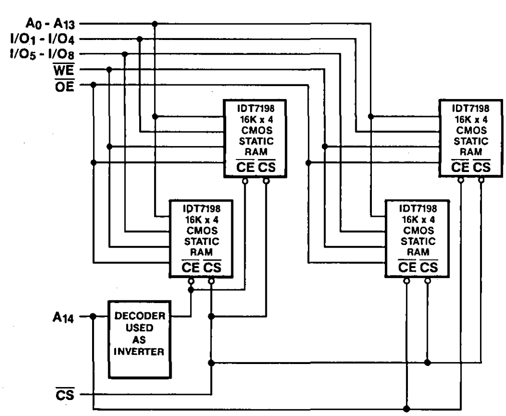


DIP
TOP VIEW

PIN NAMES

A_0 - A_{14}	ADDRESSES
I/O_1 - I/O_8	DATA INPUT/OUTPUT
$\overline{CS}$	CHIP SELECT
V_{CC}	POWER
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
GND	GROUND

FUNCTIONAL BLOCK DIAGRAM



13

CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **JULY 1986**

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} min = -3.0V pulse width less than 20ns.

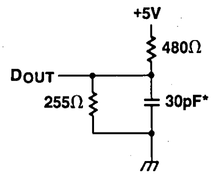
DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = 5.5V, $\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = 0	—	190	380	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = f Max.	—	190	380	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} (TTL Level), V_{CC} = 5.5V, Output Open	—	90	200	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V (CMOS Level) V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	0.2	80(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = 4.5V I_{OL} = 8mA, V_{CC} = 4.5V	— —	— —	0.5 0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = 4.5V	2.4	—	—	V

NOTES:
1. V_{CC} = 5V, T_A = +25°C
2. I_{SB1} at commercial temperature = 60mA.

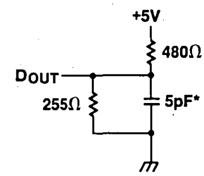
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2



SRD7198S/L-005

Figure 1. Output Load



SRD7198S/L-006

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig**

AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

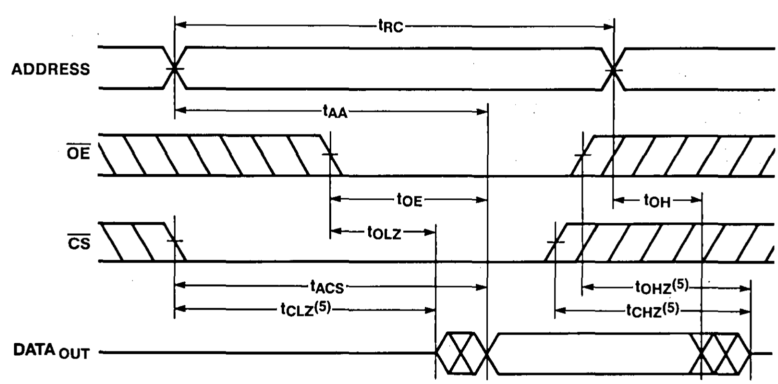
SYMBOL	PARAMETER	IDT7M856S40 MIN.	IDT7M856S40 MAX.	IDT7M856S50 MIN.	IDT7M856S50 MAX.	IDT7M856S60 MIN.	IDT7M856S60 MAX.	IDT7M856S70 MIN.	IDT7M856S70 MAX.	IDT7M856S85 MIN.	IDT7M856S85 MAX.	UNITS
READ CYCLE												
t_{RC}	Read Cycle Time	40	—	50	—	60	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	40	—	50	—	60	—	70	—	85	ns
t_{ACS}	Chip Select Access Time	—	40	—	50	—	55	—	65	—	80	ns
t_{CLZ}	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	30	—	35	—	40	—	45	—	55	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Select to Output in High Z	—	15	—	15	—	20	—	25	—	30	ns
t_{OHZ}	Output Disable to Output in High Z	—	15	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time	—	40	—	50	—	60	—	70	—	85	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	40	—	50	—	60	—	70	—	85	—	ns
t_{CW}	Chip Select to End of Write	35	—	45	—	50	—	60	—	75	—	ns
t_{AW}	Address Valid to End or Write	35	—	45	—	50	—	60	—	75	—	ns
t_{AS}	Address Setup Time	5	—	5	—	10	—	10	—	10	—	ns
t_{WP}	Write Pulse Width	30	—	35	—	40	—	45	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output High Z	—	20	—	20	—	25	—	30	—	40	ns
t_{DW}	Data to Write Time Overlap	20	—	20	—	25	—	30	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

13

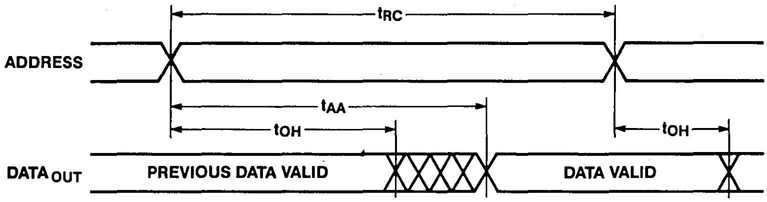
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = –55°C to +125°C)

SYMBOL	PARAMETER	IDT7M856S55 MIN.	IDT7M856S55 MAX.	IDT7M856S65 MIN.	IDT7M856S65 MAX.	IDT7M856S75 MIN.	IDT7M856S75 MAX.	IDT7M856S90 MIN.	IDT7M856S90 MAX.	IDT7M856S100 MIN.	IDT7M856S100 MAX.	UNITS
READ CYCLE												
t_{RC}	Read Cycle Time	55	—	65	—	75	—	90	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	65	—	75	—	90	—	100	ns
t_{ACS}	Chip Select Access Time	—	55	—	55	—	65	—	80	—	90	ns
t_{CLZ}	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	40	—	45	—	50	—	60	—	65	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Select to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OHZ}	Output Disable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time	—	55	—	65	—	75	—	90	—	100	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	55	—	65	—	75	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	50	—	55	—	65	—	75	—	85	—	ns
t_{AW}	Address Valid to End of Write	50	—	55	—	65	—	75	—	85	—	ns
t_{AS}	Address Setup Time	5	—	10	—	10	—	15	—	15	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	45	—	50	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output High Z	—	25	—	30	—	40	—	50	—	50	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	35	—	45	—	45	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

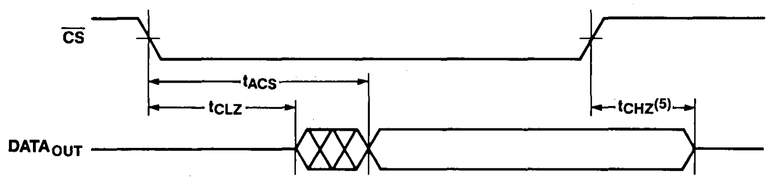


TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



SRD7198S/L-008

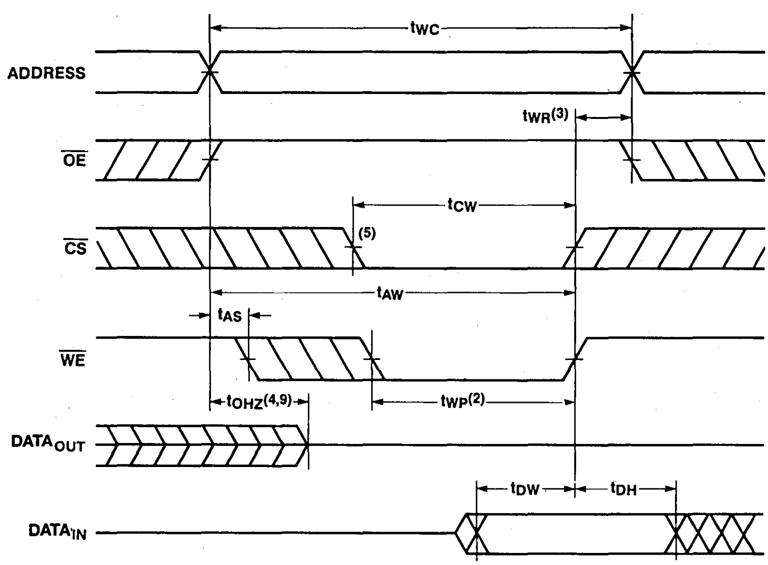
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



SRD7198S/L-009

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

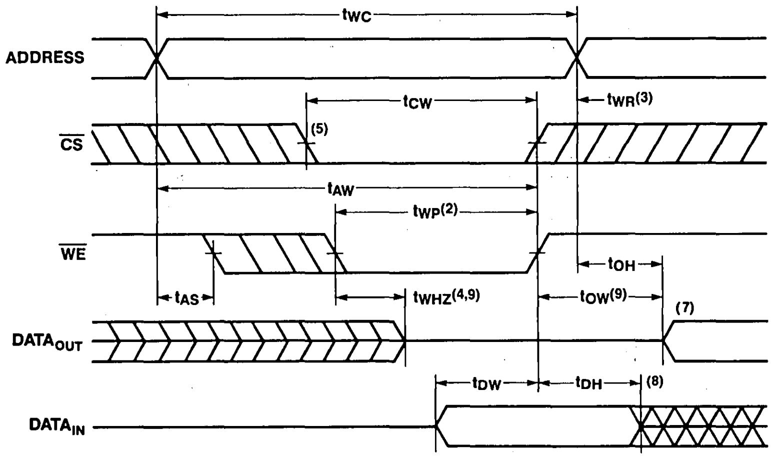
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)



SRD7198S/L-010

13

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1,6)



SRD7198S/L-011

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. DATA OUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TRUTH TABLE

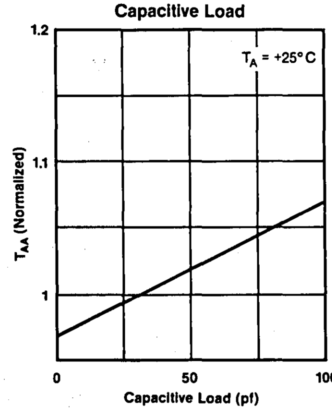
MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	X	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	26	pF

NOTE:
1. This parameter is sampled and not 100% tested.

Address Access Time vs. Capacitive Load



SRD7M656-016

ORDERING INFORMATION

IDT XXXX A 999 A A

XXXX	A	999	A	A
Device Type	Power	Speed	Package	Process/ Temperature Range

Blank	Commercial (0°C to +70°C)	
B	Military (-55°C +125°C) Semiconductor components screened to MIL-STD-883, Method 5004, Class B	
C	Sidebraze	
40	Commercial Only	Speed in Nanoseconds
50	Commercial Only	
60	Commercial Only	
70	Commercial Only	
85	Commercial Only	
55	Military Only	
65	Military Only	
75	Military Only	
90	Military Only	
100	Military Only	
S	Standard	
7M856	32K x 8-Bit	

Integrated Device Technology, Inc.

4 MEGABIT (256K x 16) CMOS STATIC RAM MODULE

ADVANCE INFORMATION
IDT7M4016

FEATURES:

- High-density 4 megabit (256K x 16) CMOS static RAM module
- Low power consumption
- Utilizes 16 IDT71257 high-performance 256K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in 48-pin, 900 mil wide ceramic sidebraze DIP
- 4X the density of the IDT7M624 (1024K RAM module) in the same size package
- Multiple GND pins for maximum noise immunity
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

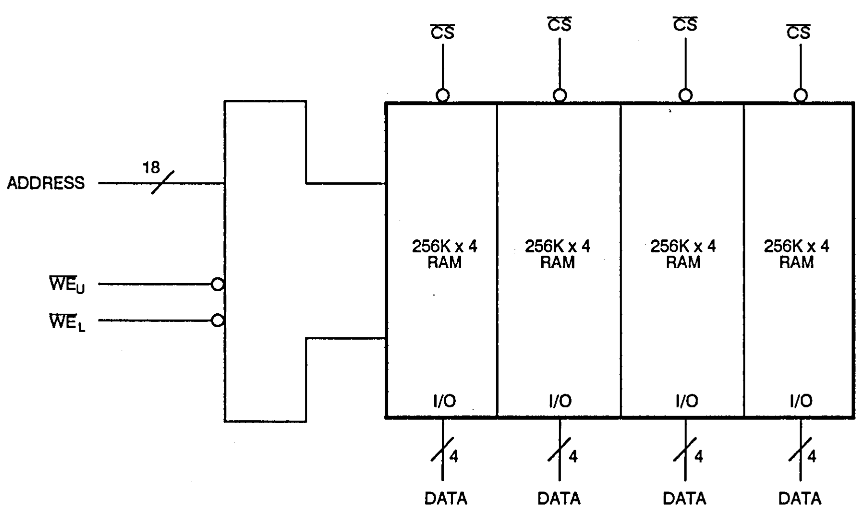
The IDT7M4016 is a 4-megabit high-speed CMOS static RAM module constructed on a multi-layered ceramic substrate using sixteen IDT71257 (256K x 1) static RAMs in leadless chip carriers. The IDT7M4016 is an upgrade from the IDT7M624 (1024K RAM module) offering four times the memory density in the same size package. Making four chip select lines available (one for each group of four RAMs) allows the user to configure the memory into a 256K x 16, 512K x 8 or 1024K x 4 organization. In addition, extremely high speeds are achievable by the use of IDT71257s, fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 256K static RAMs available.

The IDT7M4016 is packaged in a 48-pin, 900 mil center sidebraze DIP to take advantage of the compact leadless chip carriers. This enables four megabits of static RAM memory to be placed in less than 2.2 square inches of board space.

All inputs and outputs of the IDT7M4016 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

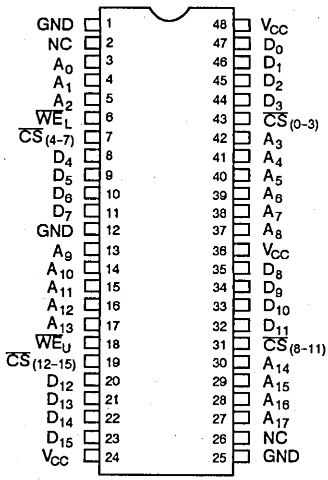


CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-7009/-

PIN CONFIGURATION

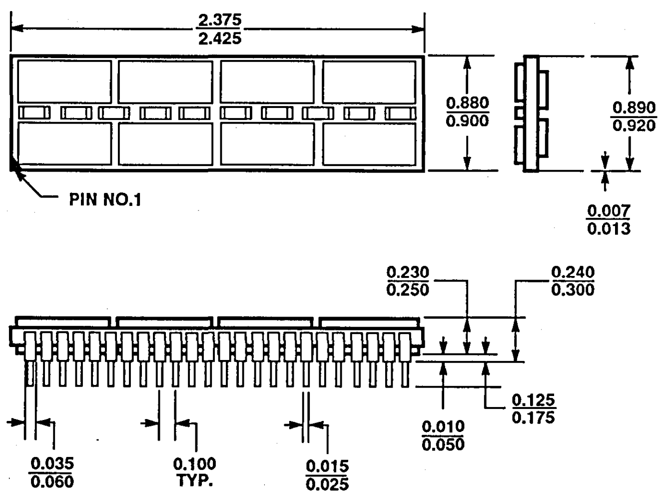


DIP
TOP VIEW

PIN NAMES

V_{CC}	Power
GND	Ground
A_{0-17}	Addresses
D_{0-15}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}_L$	Write Enable (Lower Byte)
$\overline{WE}_U$	Write Enable (Upper Byte)

PACKAGE DIMENSIONS



Integrated Device Technology, Inc.

2 MEGABIT (64K x 32) CMOS STATIC RAM MODULE

ADVANCE INFORMATION
IDT7M4017

FEATURES:

- High-density 2 megabit (64K x 32) CMOS static RAM module
- Fast access times
  - Military: 60ns (max.)
  - Commercial: 45ns (max.)
- Individual byte selects
- Upper and lower word write enables
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in 60-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M4017 is a 2 megabit (64K x 32) high-speed static RAM module constructed on a co-fired ceramic substrate using eight IDT71256 32K x 8 static RAMs in leadless chip carriers. On-board decoders use A_{15} to select the upper or lower bank of RAMs. Four chip selects control individual byte selection. Extremely fast speeds can be achieved due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

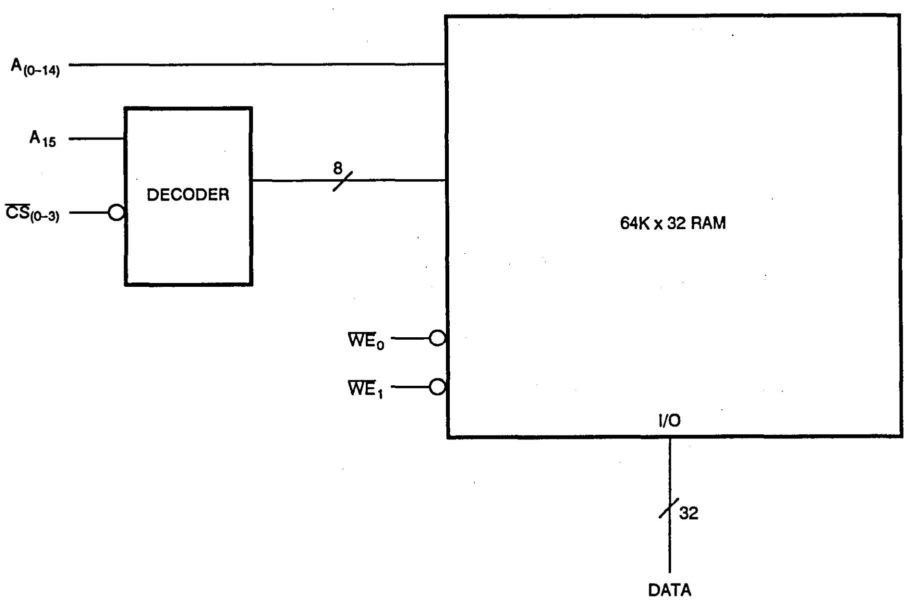
The IDT7M4017 is offered in a 60-pin, 600 mil center sidebraze DIP which enables two megabits of memory to be placed in less than 1.9 square inches of board space.

The IDT7M4017 is available with fast access times over the commercial and military temperature ranges, with minimal power consumption. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to a substantially lower power mode.

All inputs and outputs of the IDT7M4017 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

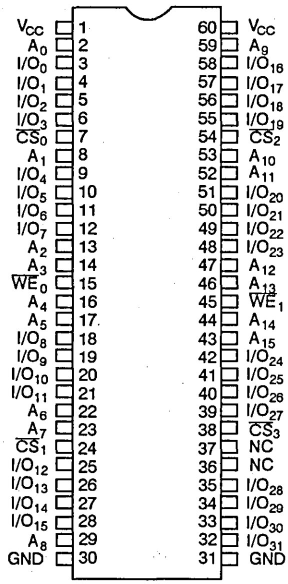
All IDT military module semiconductor components are manufactured in compliance with MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION

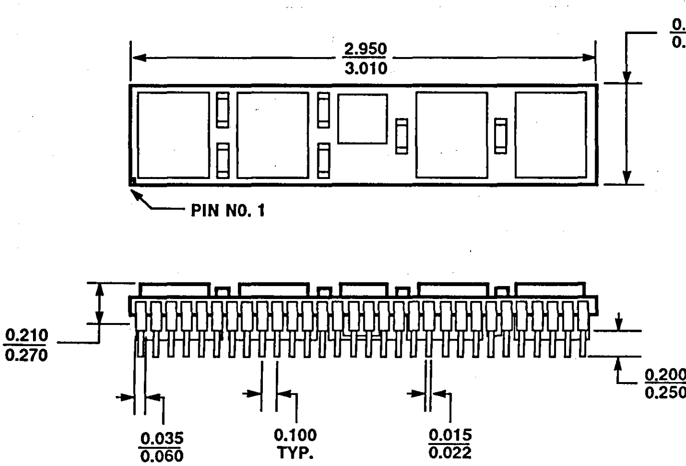


DIP
TOP VIEW

PIN NAMES

$A_0 - A_{15}$	Addresses
I/O_{0-31}	Data Input/Output
$\overline{CS}_{0-3}$	Chip Select
$\overline{WE}$	Write Enable

PACKAGE DIMENSIONS



13

Integrated Device Technology, Inc.

1 MEGABIT (64K x 16-BIT) & 512K (32K x 16-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

IDT8MP624S
IDT8MP612S

FEATURES:

- High-density 1024K/512K-bit CMOS static RAM module
- 64K x 16 organization (IDT8MP624) with 32K x 16 option (IDT8MP612)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  - Allows flexibility in application
- Fast access time: 40ns (max.)
- Low power consumption
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Offered in a SIP (single in-line) package for maximum space-savings
- Cost-effective plastic surface-mounted RAM packages on an epoxy laminate (FR4) substrate
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

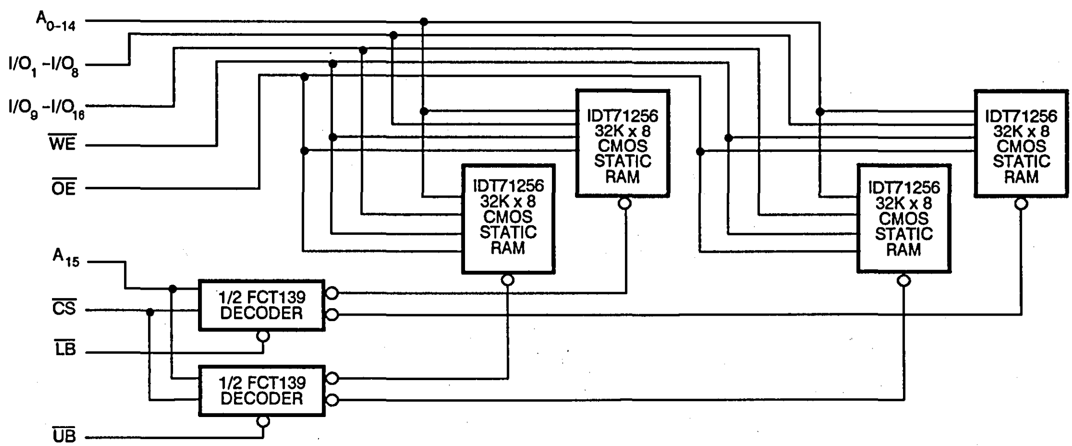
The IDT8MP624S/IDT8MP612S are 1024K/512K high-speed CMOS static RAMs constructed on an epoxy laminate substrate using four IDT71256 32K x 8 static RAMs (IDT8MP624S) or two IDT71256 static RAMs (IDT8MP612S) in plastic surface-mount packages. Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} to select one of the two 32K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On the IDT8MP612S 32K x 16 option, A_{15} needs to be externally grounded for proper operation.) Extremely high speeds are achieved by the use of IDT71256s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 1024K/512K static RAMs available.

The IDT8MP624S/IDT8MP612S are available with access times as fast as 40ns over the commercial temperature range, with maximum operating power consumption of only 1.8W (64K x 16 option). The module also offers a full standby mode of 330mW (max.)

The IDT8MP624S/IDT8MP612S are offered in a 40-pin plastic SIP package. For the 40-pin JEDEC standard DIP, refer to the IDT8M624S/IDT8M612S.

All inputs and outputs of the IDT8MP624S/IDT8MP612S are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

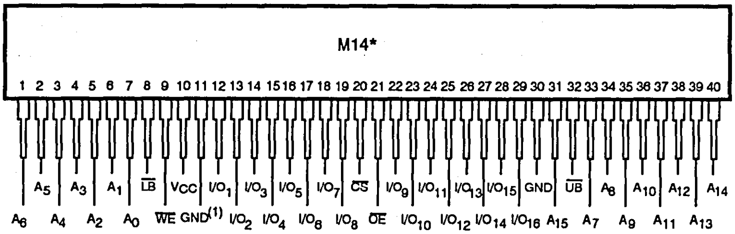
FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE **DECEMBER 1987**

PIN CONFIGURATION



SIP
FRONT VIEW

NOTE:
* For module dimensions, please refer to module drawing M14 in the packaging section.

PIN NAMES

A_{0-15}	Addresses
I/O_{1-16}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground
$\overline{OE}$	Output Enable
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control

NOTES:
1. Both GND pins need to be grounded for proper operation.
2. On IDT8MP612S, 512K (32K x 16-bit) option, A_{15} (Pin 31) requires external grounding for proper operation.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT8MP624S MIN.	IDT8MP624S TYP.[1]	IDT8MP624S MAX.	IDT8MP612S MIN.	IDT8MP612S TYP.[1]	IDT8MP612S MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	—	15	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	15	—	—	15	µA
I_{CCX16}	Operating Current In X16 Mode	$\overline{CS}$, $\overline{UB}$ & $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	—	175	340	—	150	300	mA
I_{CCX8}	Operating Current In X8 Mode	$\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	—	100	200	—	80	170	mA
I_{SB} & I_{SB1}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or $\overline{UB}$ ≥ V_{IH} and $\overline{LB}$ ≥ V_{IH} V_{CC} = Max. Output Open	—	4	60	—	2	30	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	—	2.4	—	—	V

NOTE:
1. V_{CC} = 5V, T_A = +25°C

13

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

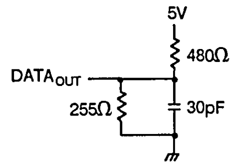


Figure 1. Output Load

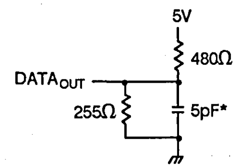


Figure 2. Output Load
(for $t_{CLZ1,2}, t_{OLZ}, t_{CHZ1,2}, t_{OHZ}, t_{OW}, t_{WHZ}$)

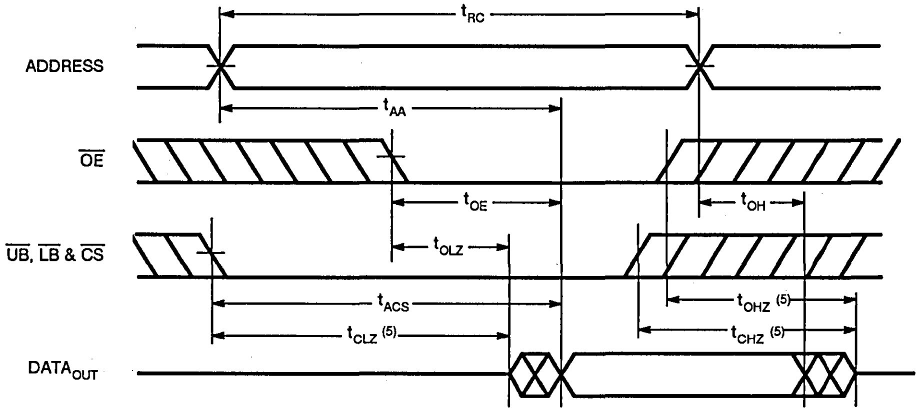
*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

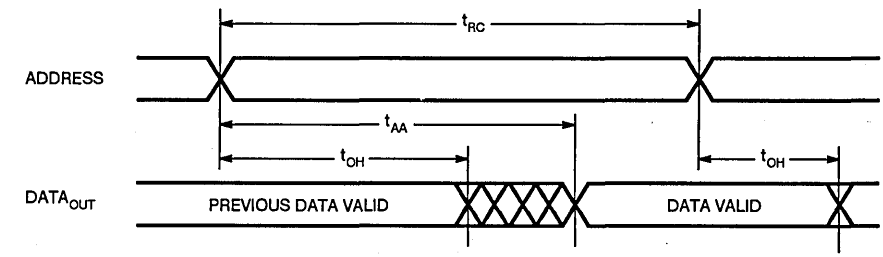
SYMBOL	PARAMETERS	IDT8MP624S40 IDT8MP612S40 MIN.	IDT8MP624S40 IDT8MP612S40 MAX.	IDT8MP624S45 IDT8MP612S45 MIN.	IDT8MP624S45 IDT8MP612S45 MAX.	IDT8MP624S50 IDT8MP612S50 MIN.	IDT8MP624S50 IDT8MP612S50 MAX.	IDT8MP624S60 IDT8MP612S60 MIN.	IDT8MP624S60 IDT8MP612S60 MAX.	IDT8MP624S70 IDT8MP612S70 MIN.	IDT8MP624S70 IDT8MP612S70 MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	40	–	45	–	50	–	60	–	70	–	ns
t_{AA}	Address Access Time	–	40	–	45	–	50	–	60	–	70	ns
t_{ACS}	Chip Select Access Time	–	40	–	45	–	50	–	60	–	70	ns
$t_{CLZ1,2}$(1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	25	–	25	–	30	–	35	–	40	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}(1)	Chip Select to Output in High Z	–	20	–	20	–	20	–	25	–	30	ns
t_{OHZ}(1)	Output Disable to Output in High Z	–	20	–	20	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	3	–	5	–	5	–	5	–	5	–	ns
t_{PU}(1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}(1)	Chip Deselect to Power Down Time	–	40	–	45	–	50	–	60	–	70	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	40	–	45	–	50	–	60	–	70	–	ns
t_{CW}	Chip Selection to End of Write	35	–	40	–	45	–	55	–	65	–	ns
t_{AW}	Address Valid to End of Write	35	–	40	–	45	–	55	–	65	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	30	–	35	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	5	–	5	–	ns
t_{WHZ}(1)	Write Enable to Output in High Z	–	15	–	15	–	20	–	25	–	30	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	20	–	25	–	30	–	ns
t_{DH}	Data Hold from Write Time	3	–	5	–	5	–	5	–	5	–	ns
t_{OW}(1)	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	ns

NOTE:
1. This parameter guaranteed but not tested.

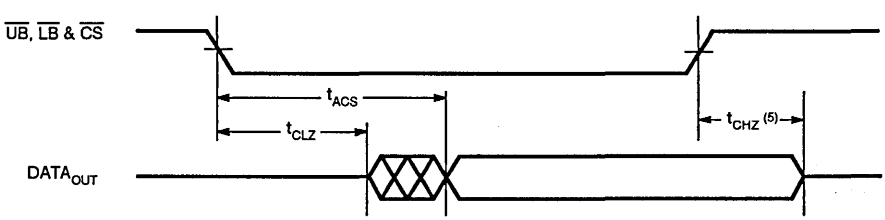
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



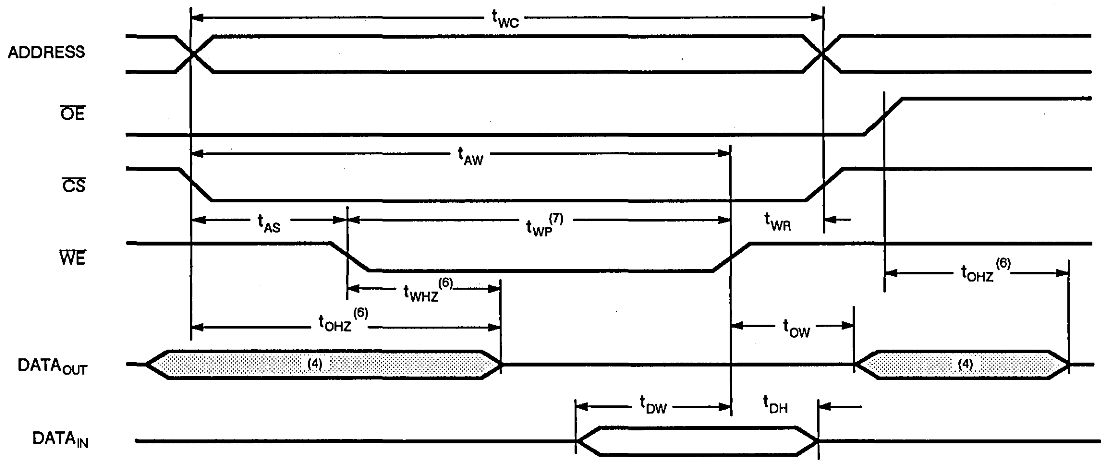
TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]



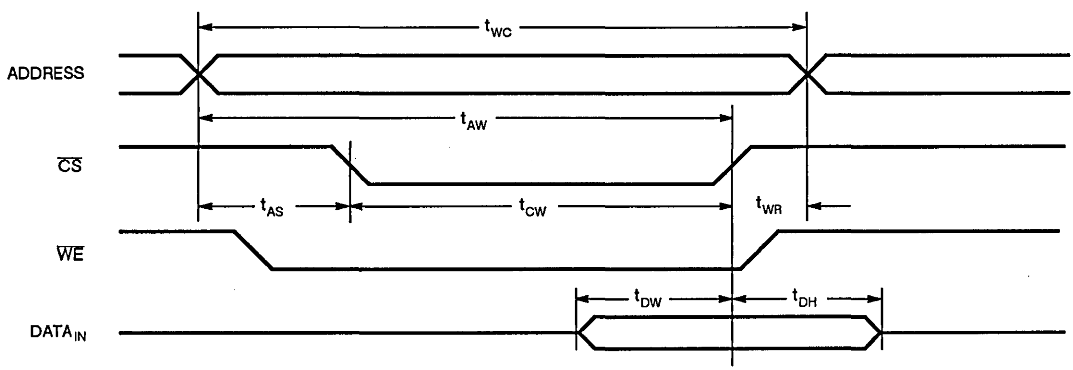
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{UB}$, $\overline{LB}$ = V_{IL} for 16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	X	X	High Z	Standby
Standby	L	H	H	X	X	High Z	Standby
Read	L	L	L	L	H	$D_{OUT\ 1-16}$	Active
Lower Byte Read	L	H	L	L	H	$D_{OUT\ 1-8}$	Active (X8)
Upper Byte Read	L	L	H	L	H	$D_{OUT\ 9-16}$	Active (X8)
Read	L	L	L	H	H	High Z	Active
Lower Byte Read	L	H	L	H	H	High Z	Active (X8)
Upper Byte Read	L	L	H	H	H	High Z	Active (X8)
Write	L	L	L	X	L	$D_{IN\ 1-16}$	Active
Lower Byte Write	L	H	L	X	L	$D_{IN\ 1-8}$	Active (X8)
Upper Byte Write	L	L	H	X	L	$D_{IN\ 9-16}$	Active (X8)

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER [1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

- Process/Temperature Range: BLANK — Commercial (0°C to +70°C)
- Package: S — Plastic SIP
- Speed: 40, 45, 50, 60, 70 — Speed in Nanoseconds
- Power: S — Standard Power
- Device Type: 8MP624 — 64K x 16-Bit; 8MP612 — 32K x 16-Bit

13

Integrated Device Technology, Inc.

256K (16K x 16-BIT) & 128K (8K x 16-BIT) CMOS STATIC RAM PLASTIC SIP MODULES

IDT8MP656S
IDT8MP628S

FEATURES:

- High-density 256K/128K CMOS static RAM modules
- 16K x 16 organization (IDT8MP656S) with 8K x 16 option (IDT8MP628)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  - Flexibility in application
- Fast access times
  - 40ns (max.)
- Low power consumption
  - Active: less than 825mW (typ. in 16K x 16 organization)
  - Standby: less than 20mW (typ.)
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Offered in an SIP (single in-line) package for maximum space-savings
- Utilizes IDT7164s—high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT8MP656S/IDT8MP628S are 256K/128K-bit high-speed CMOS static RAMs constructed on an epoxy laminate substrate using four IDT7164 8K x 8 static RAMs (IDT8MP656S) or two IDT7164 static RAMs (IDT8MP628S) in plastic surface mount packages.

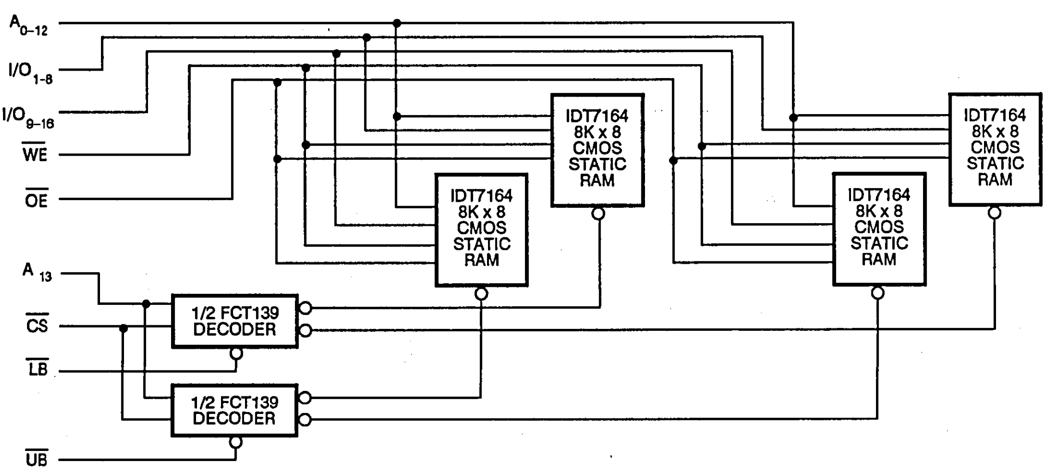
Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{13} to select one of the two 8K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On the IDT8MP628S 8K x 16 option, A_{13} needs to be externally grounded for proper operation.) Extremely high speeds are achievable by the use of IDT7164s, fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 256K/128K static RAMs available.

The IDT8MP656S/IDT8MP628S are available with maximum operating power consumption of only 1.8W (IDT8MP656S 16K x 16 option). The modules also offer a full standby mode of 330mW (max.).

The IDT8MP656S/IDT8MP628S are offered in a 40-pin plastic SIP. For the JEDEC standard 40-pin DIP, refer to the IDT8M656S/ IDT8M628S.

All inputs and outputs of the IDT8MP656S/IDT8MP628S are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM

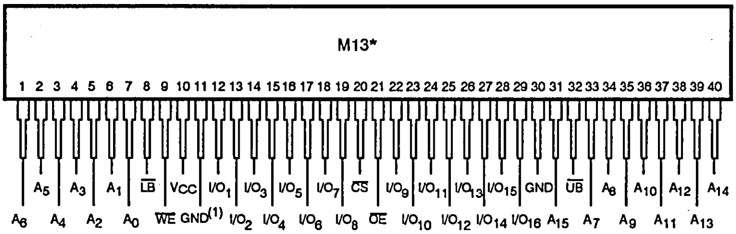


CEMOS is a trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE **DECEMBER 1987**

DSC-7016/-

PIN CONFIGURATION



SIP
FRONT VIEW

NOTE:
* For module dimensions, please refer to module drawing M13 in the packaging section.

PIN NAMES

A_{0-13}	Addresses
I/O_{1-16}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control

NOTES:
1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. On IDT8MP628S, 128K (8K x 16-Bit) option, A_{13}(Pin 35) is required external grounding for proper operation.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} = - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT8MP656S MIN.	IDT8MP656S TYP.	IDT8MP656S MAX.	IDT8MP628S MIN.	IDT8MP628S TYP.	IDT8MP628S MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	—	15	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	15	—	—	15	µA
I_{CCX16}	Operating Current In X16 Mode	$\overline{CS}$, $\overline{UB}$ & $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	—	165	330	—	150	300	mA
I_{CCX8}	Operating Current In X8 Mode	$\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	—	100	200	—	80	170	mA
I_{SB} & I_{SB1}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or UB ≥ V_{IH} and $\overline{LB}$ ≥ V_{IH} V_{CC} = Max. Output Open	—	4	60	—	2	30	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	—	2.4	—	—	V

13

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

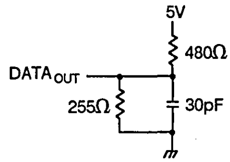


Figure 1. Output Load

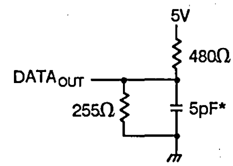


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

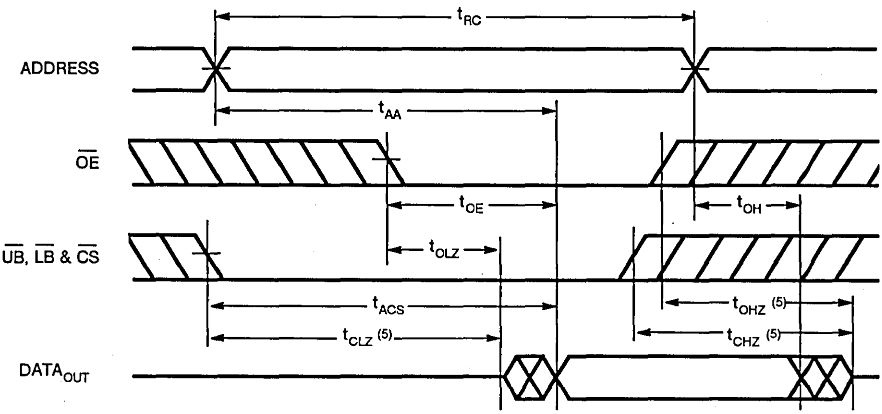
*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

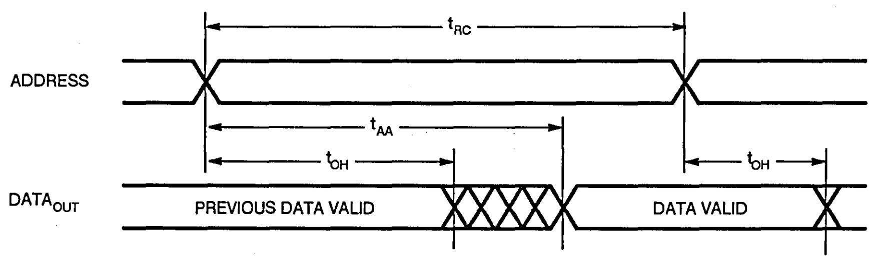
SYMBOL	PARAMETERS	IDT8MP656S40 IDT8MP628S40 MIN.	MAX.	IDT8MP656S50 IDT8MP628S50 MIN.	MAX.	IDT8MP656S70 IDT8MP628S70 MIN.	MAX.	IDT8MP656S85 IDT8MP628S85 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	40	–	50	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	40	–	50	–	70	–	85	ns
t_{ACS}	Chip Select Access Time	–	40	–	50	–	70	–	85	ns
$t_{CLZ1,2}$(1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	25	–	30	–	40	–	50	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{CHZ}(1)	Chip Select to Output in High Z	–	15	–	20	–	30	–	35	ns
t_{OHZ}(1)	Output Disable to Output in High Z	–	15	–	20	–	30	–	35	ns
t	Output Hold from Address Change	5	–	5	–	5	–	5	–	ns
t_{PU}(1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}(1)	Chip Deselect to Power Down Time	–	40	–	50	–	70	–	85	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	40	–	50	–	70	–	85	–	ns
t_{CW}	Chip Selection to End of Write	5	–	45	–	65	–	75	–	ns
t_{AW}	Address Valid to End of Write	35	–	45	–	65	–	75	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	10	–	10	–	ns
t_{WP}	Write Pulse Width	30	–	40	–	55	–	65	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	10	–	ns
t_{WHZ}(1)	Write Enable to Output in High Z	–	15	–	20	–	25	–	30	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	30	–	35	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	ns
t_{OW}(1)	Output Active from End of Write	5	–	5	–	5	–	5	–	ns

NOTE:
1. This parameter guaranteed but not tested.

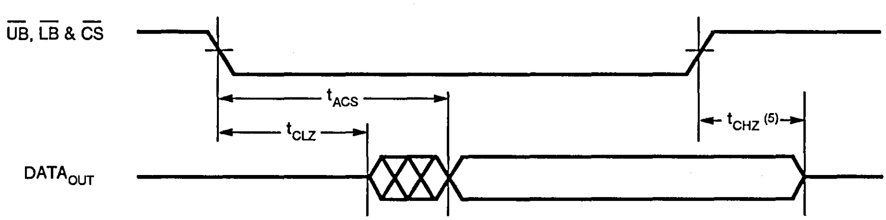
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]

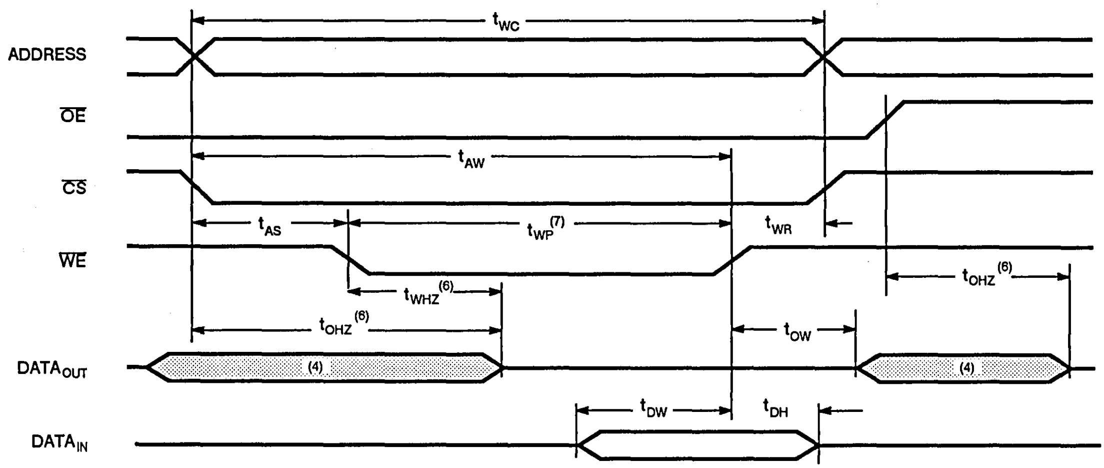


NOTES:

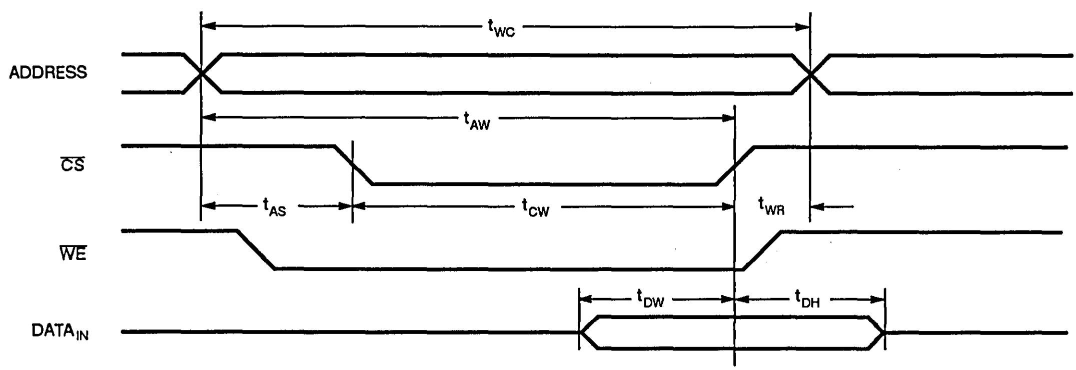
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{UB}$, $\overline{LB} = V_{IL}$ for 16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

13

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1,2,3,7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1,2,3,5]



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	X	X	High Z	Standby
Standby	L	H	H	X	X	High Z	Standby
Read	L	L	L	L	H	$D_{OUT\ 1-16}$	Active
Lower Byte Read	L	H	L	L	H	$D_{OUT\ 1-8}$	Active (X8)
Upper Byte Read	L	L	H	L	H	$D_{OUT\ 9-16}$	Active (X8)
Read	L	L	L	H	H	High Z	Active
Lower Byte Read	L	H	L	H	H	High Z	Active (X8)
Upper Byte Read	L	L	H	H	H	High Z	Active (X8)
Write	L	L	L	X	L	$D_{IN\ 1-16}$	Active
Lower Byte Write	L	H	L	X	L	$D_{IN\ 1-8}$	Active (X8)
Upper Byte Write	L	L	H	X	L	$D_{IN\ 9-16}$	Active (X8)

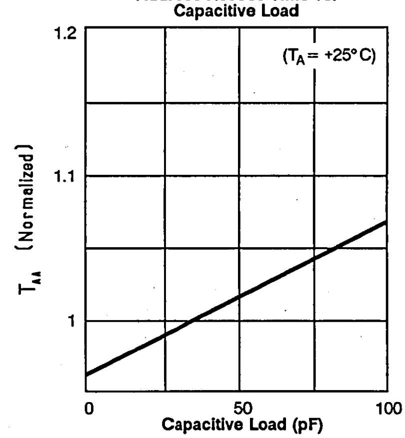
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:

1. This parameter is sampled and not 100% tested.

Address Access Time vs. Capacitive Load



ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/ Temperature Range)

Process/Temperature Range	BLANK	Commercial (0°C to +70°C)
Package	S	Plastic SIP
Speed	40 50 70 85	Speed in Nanoseconds
Power	S	Standard Power
Device Type	8MP656 8MP628	16K x 16-Bit 8K x 16-Bit

13

1 MEGABIT (128K x 8-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

IDT8MP824S

FEATURES:

- High-density 1024K (128K x 8) CMOS static RAM module
- Fast access time
  - 40ns (max.) over commercial temperature range
- Low power consumption
  - Active: less than 500mW (typ.)
  - Standby: less than 8mW (typ.)
- Cost-effective plastic surface-mounted RAM packages on an epoxy laminate (FR4) substrate
- Offered in a SIP (single in-line package) for maximum space-saving
- Utilizes IDT71256s—high-performance 256K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

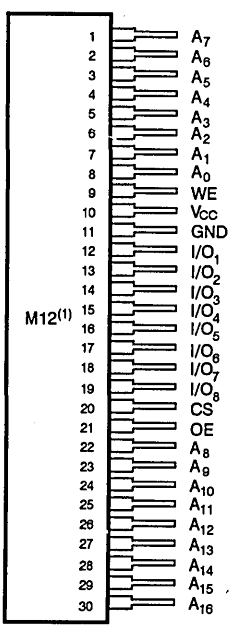
The IDT8MP824S is a1024K (131, 072 x 8-bit) high-speed static RAM constructed on an epoxy laminate substrate using four IDT71256 32K x 8 static RAMs in plastic surface mount packages. Functional equivalence to proposed monolithic one megabit static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} and A_{16} to select one of the four 32K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

The IDT8MP824S is available with maximum access times as fast as 40ns over the commercial temperature range, with maximum operating power consumption of 825mW. The module also offers a full standby mode of 330mW (max.).

The IDT8MP824S is offered in a 30-pin SIP. For the 32-pin JEDEC standard DIP, refer to the IDT8M824S.

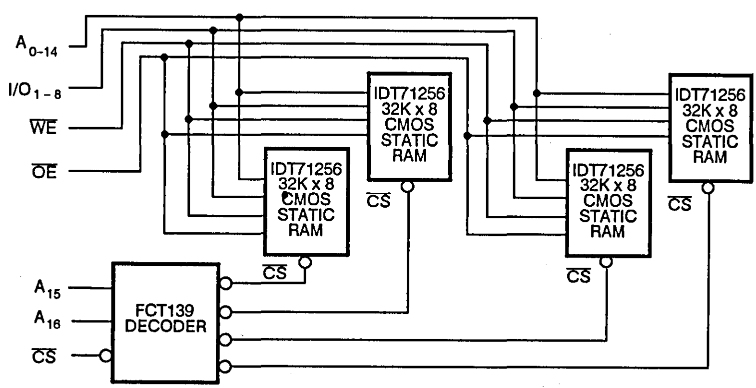
All inputs and outputs of the IDT8MP824S are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

PIN CONFIGURATION



SIP
SIDE VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{0-16}	Addresses
I/O_{1-8}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground

1. For module dimensions, please refer to module drawing M12 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ±10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT8MP824S MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	–	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open f = 0	–	60	150	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	–	100	200	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or (TTL Level) V_{CC} = Max. Output Open	–	2	80	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{HC}, V_{IN} ≥ V_{HC} or ≤ V_{LC} V_{CC} = Max., Output Open	–	1.6	60	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	–	–	V

NOTE:

1. V_{CC} = 5V, T_A = +25°C

David 4928354
$60 @ 1K

8MP824S60S

13

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

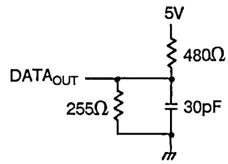


Figure 1. Output Load

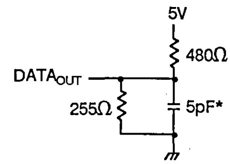


Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

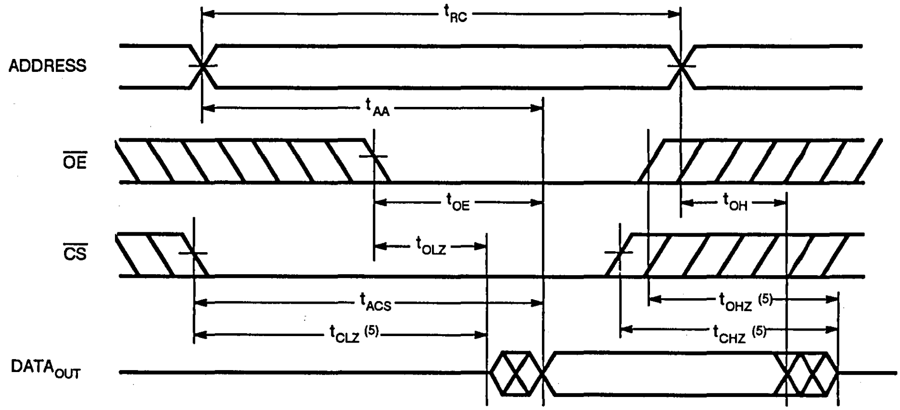
*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

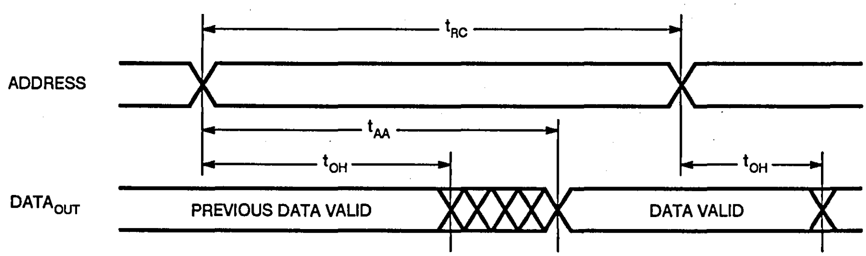
SYMBOL	PARAMETERS	8MP824S40 MIN.	8MP824S40 MAX.	8MP824S45 MIN.	8MP824S45 MAX.	8MP824S50 MIN.	8MP824S50 MAX.	8MP824S60 MIN.	8MP824S60 MAX.	8M824S70 MIN.	8M824S70 MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	40	–	45	–	50	–	60	–	70	–	ns
t_{AA}	Address Access Time	–	40	–	45	–	50	–	60	–	70	ns
t_{ACS}	Chip Select Access Time	–	40	–	45	–	50	–	60	–	70	ns
$t_{CLZ1,2}$(1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	25	–	25	–	30	–	35	–	40	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}(1)	Chip Select to Output in High Z	–	20	–	20	–	20	–	25	–	30	ns
t_{OHZ}(1)	Output Disable to Output in High Z	–	20	–	20	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	3	–	5	–	5	–	5	–	5	–	ns
t_{PU}(1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}(1)	Chip Deselect to Power Down Time	–	40	–	45	–	50	–	60	–	70	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	40	–	45	–	50	–	60	–	70	–	ns
t_{CW}	Chip Selection to End of Write	35	–	40	–	45	–	55	–	65	–	ns
t_{AW}	Address Valid to End of Write	35	–	40	–	45	–	55	–	65	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	30	–	35	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	5	–	5	–	ns
t_{WHZ}(1)	Write Enable to Output in High Z	–	15	–	15	–	20	–	25	–	30	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	20	–	25	–	30	–	ns
t_{DH}	Data Hold from Write Time	3	–	5	–	5	–	5	–	5	–	ns
t_{OW}(1)	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	ns

NOTE:
1. This parameter guaranteed but not tested.

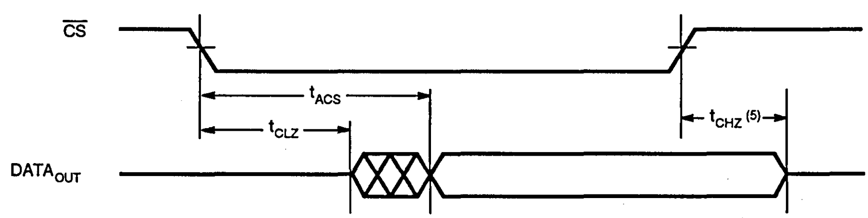
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]

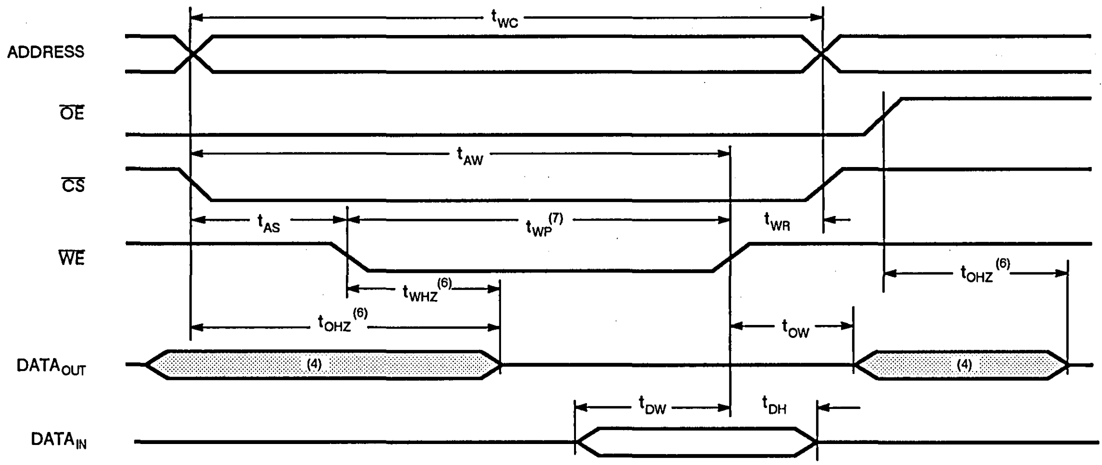


NOTES:

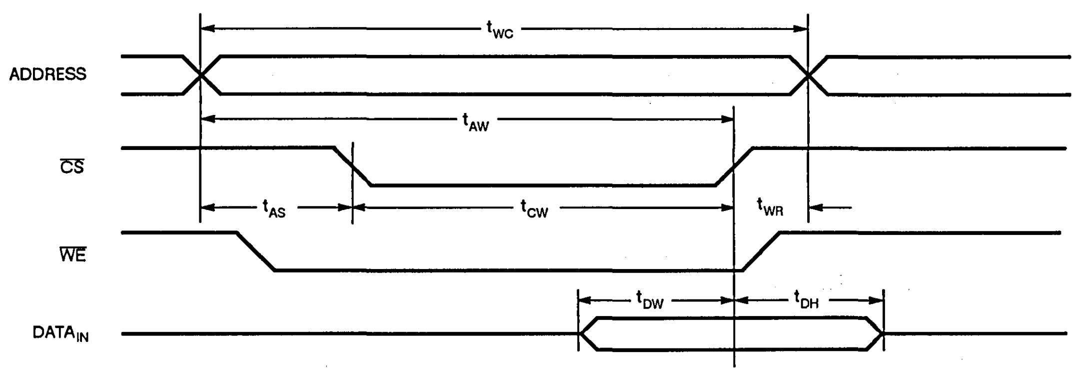
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

13

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	X	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/ Temperature Range)

- Process/Temperature Range: BLANK — Commercial (0°C to +70°C)
- Package: S — Plastic SIP
- Speed: 40, 45, 50, 60, 70 — Speed in Nanoseconds
- Power: S — Standard Power
- Device Type: 8MP824 — 1 Megabit

Integrated Device Technology, Inc.

1 MEGABIT (64K x 16-BIT) & 512K (32K x 16-BIT) CMOS STATIC RAM MODULE

IDT8M624S
IDT8M612S

FEATURES:

- High-density 1024K/512K-bit CMOS static RAM module
- 64K x 16 organization (IDT8M624S) with 32K x 16 option (IDT8M612S)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  - Allows flexibility in application
- Equivalent to JEDEC standard for future monolithic 64K x 16/ 32K x 16 static RAMs
- High speed, 40ns (max.) over commercial temperature range
- Low power consumption
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 40-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT8M624S/IDT8M612S are 1024K/512K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic-substrate using four IDT71256 32K x 8 static RAMs (IDT8M624S) or two IDT71256 static RAMs (IDT8M612S) in leadless chip carriers. Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} to select one of the two 32K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On the IDT8M612S 32K x 16 option, A_{15} needs to be externally grounded for proper operation.) Extremely high speeds are achievable by the use of IDT71256s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 1024K/512K static RAMs available.

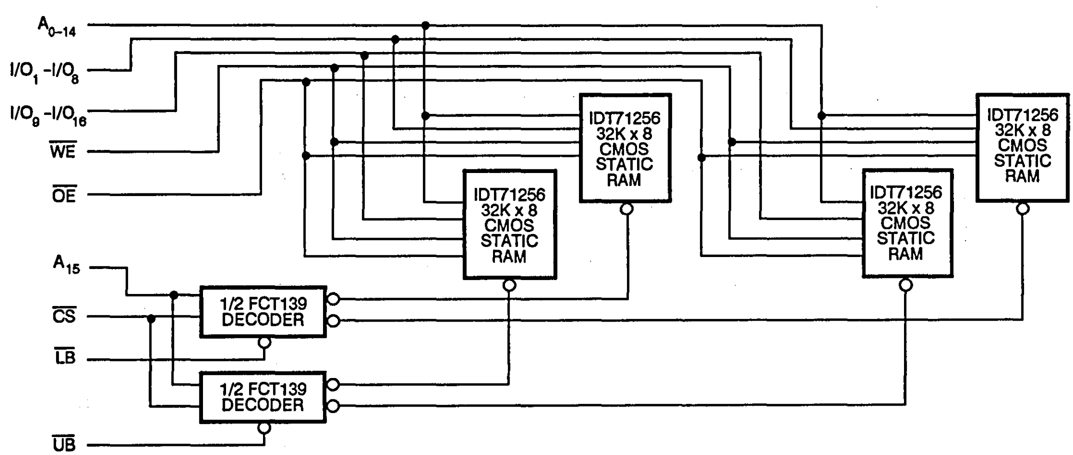
The IDT8M624S/IDT8M612S are available with access times as fast as 40ns commercial and 60ns military temperature range, with maximum operating power consumption of only 1.8W (max.—IDT8M624S 64K x 16 option). The module also offers a full standby mode of 440mW (max.).

The IDT8M624S/IDT8MP612S are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT71256s in leadless chip carriers.

All inputs and outputs of the IDT8M624S/IDT8M612S are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

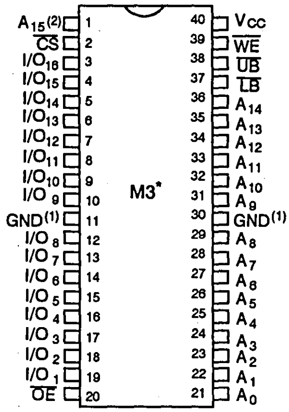
FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

PIN CONFIGURATION



DIP
TOP VIEW

NOTE:

* For module dimensions, please refer to module drawing M3 in the packaging section.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN NAMES

A_{0-15}	Addresses
I/O_{1-16}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground
$\overline{OE}$	Output Enable
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control

NOTES:

1. Both GND pins need to be grounded for proper operation.
2. On IDT8M612S, 512K (32K x 16-bit) option, A_{15} (pin 1) requires external grounding for proper operation.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to 125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

13

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT8M624S MIN.	IDT8M624S TYP.(1)	IDT8M624S MAX.	IDT8M612S MIN.	IDT8M612S TYP.(1)	IDT8M612S MAX.	UNIT
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	—	15	—	—	15	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH} V_{OUT} = GND to V_{CC}	—	—	15	—	—	15	µA
I_{CCX16}	Operating Current In X16 Mode	$\overline{CS}$, $\overline{UB}$ & $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	—	175	340	—	150	300	mA
I_{CCX8}	Operating Current In X8 Mode	$\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	—	100	200	—	80	170	mA
I_{SB} & I_{SB1}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or UB ≥ V_{IH} and $\overline{LB}$ ≥ V_{IH} V_{CC} = Max. Output Open	—	4	80(2)	—	2	40(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	—	2.4	—	—	V

NOTES:
1. V_{CC} = 5V, T_A = +25°C
2. I_{SB} and I_{SB1} of IDT8M624S/IDT8M612S at commercial temperature = 60mA/30mA.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

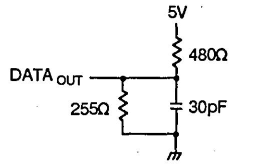


Figure 1. Output Load

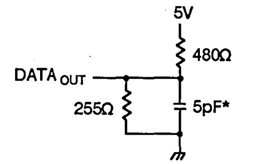


Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

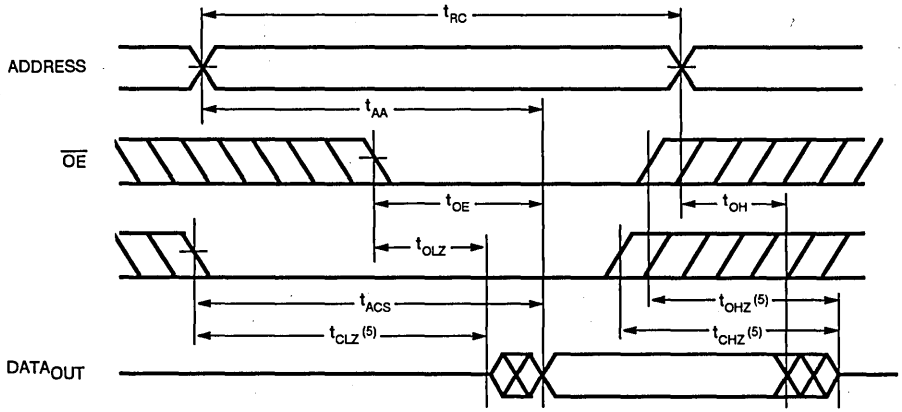
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	8M624S40 8M612S40 (COM'L.)		8M624S45 8M612S45 (COM'L.)		8M624S50 8M612S50 (COM'L.)		8M624S60 8M612S60		8M624S70 8M612S70		8M624S85 8M612S85 (MIL.)		8M624S100 8M612S100 (MIL.)		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE																
t_{RC}	Read Cycle Time	40	–	45	–	50	–	60	–	70	–	85	–	100	–	ns
t_{AA}	Address Access Time	–	40	–	45	–	50	–	60	–	70	–	85	–	100	ns
t_{ACS}	Chip Select Access Time	–	40	–	45	–	50	–	60	–	70	–	85	–	100	ns
$t_{CLZ1,2}$(1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	25	–	25	–	30	–	35	–	40	–	50	–	60	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}(1)	Chip Select to Output in High Z	–	20	–	20	–	20	–	25	–	30	–	35	–	40	ns
t_{OHZ}(1)	Output Disable to Output in High Z	–	20	–	20	–	20	–	25	–	30	–	35	–	40	ns
t_{OH}	Output Hold from Address Change	3	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}(1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}(1)	Chip Deselect to Power Down Time	–	40	–	45	–	50	–	60	–	70	–	85	–	100	ns
WRITE CYCLE																
t_{WC}	Write Cycle Time	40	–	45	–	50	–	60	–	70	–	85	–	100	–	ns
t_{CW}	Chip Selection to End of Write	35	–	40	–	45	–	55	–	65	–	75	–	90	–	ns
t_{AW}	Address Valid to End of Write	35	–	40	–	45	–	55	–	65	–	75	–	90	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	30	–	35	–	40	–	50	–	60	–	70	–	80	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	5	–	5	–	10	–	10	–	ns
t_{WHZ}(1)	Write Enable to Output in High Z	–	15	–	15	–	20	–	25	–	30	–	35	–	40	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	20	–	25	–	30	–	35	–	40	–	ns
t_{DH}	Data Hold from Write Time	3	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OW}(1)	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns

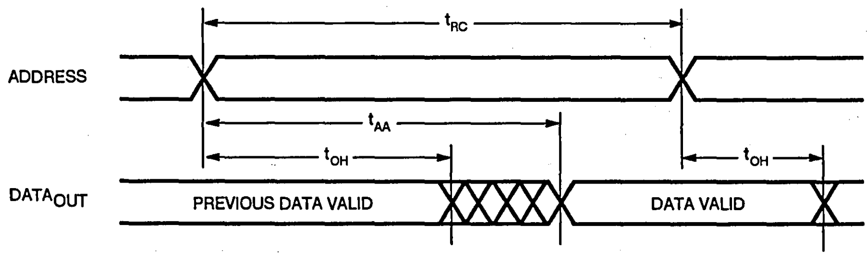
NOTE:
1. This parameter guaranteed but not tested.

13

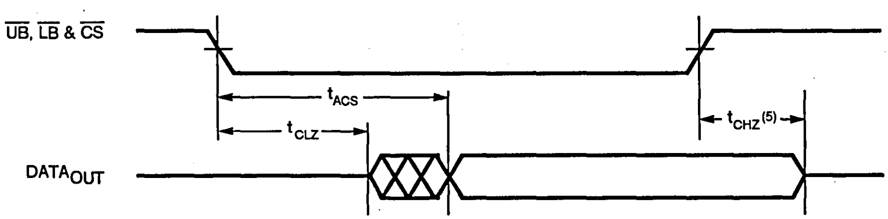
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1,2,4]



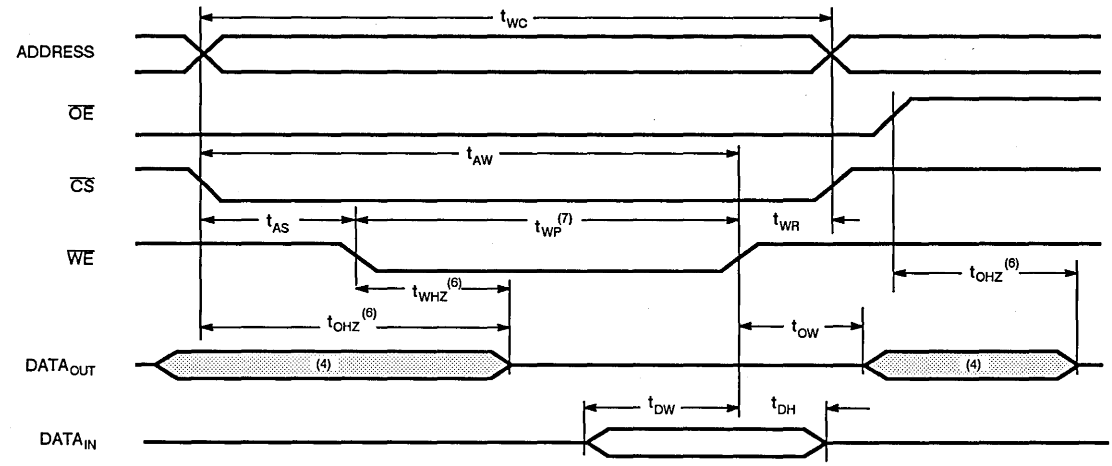
TIMING WAVEFORM OF READ CYCLE NO. 3[1,3,4]



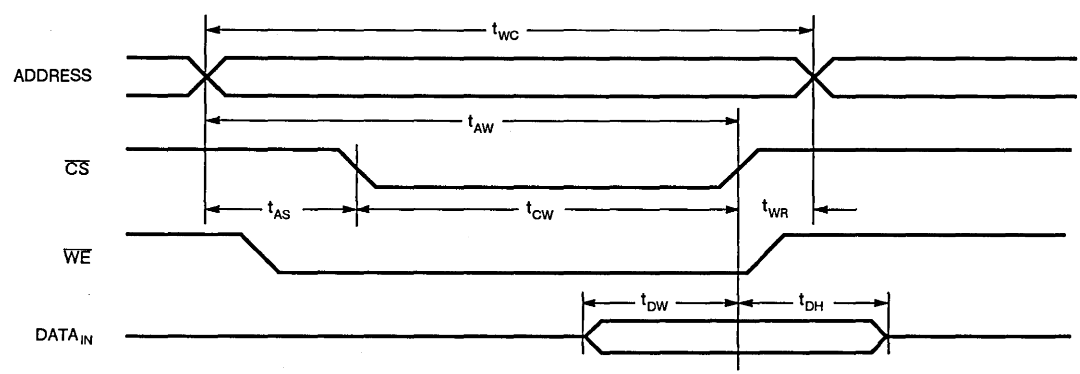
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{UB}$, $\overline{LB} = V_{IL}$ for 16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



13

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	X	X	High Z	Standby
Standby	L	H	H	X	X	High Z	Standby
Read	L	L	L	L	H	$D_{OUT\ 1-16}$	Active
Lower Byte Read	L	H	L	L	H	$D_{OUT\ 1-8}$	Active (X8)
Upper Byte Read	L	L	H	L	H	$D_{OUT\ 9-16}$	Active (X8)
Read	L	L	L	H	H	High Z	Active
Lower Byte Read	L	H	L	H	H	High Z	Active (X8)
Upper Byte Read	L	L	H	H	H	High Z	Active (X8)
Write	L	L	L	X	L	$D_{IN\ 1-16}$	Active
Lower Byte Write	L	H	L	X	L	$D_{IN\ 1-8}$	Active (X8)
Upper Byte Write	L	L	H	X	L	$D_{IN\ 9-16}$	Active (X8)

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION

IDT XXXX A 999 A A

Device Type · Power · Speed · Package · Process/Temperature Range

Process/Temperature Range:
- Blank — Commercial (0°C to +70°C)
- B — Military (55°C to +125°C) Semiconductor Components Compliant to the latest revision of MIL-STD-883, Class B

Package:
- C — Sidebraze DIP

Speed (Speed in Nanoseconds):
- 40 — Commercial Only
- 45 — Commercial Only
- 50 — Commercial Only
- 60
- 70
- 85 — Military Only
- 100 — Military Only

Power:
- S — Standard Power

Device Type:
- 8M624 — 64K x 16-Bit
- 8M612 — 32K x 16-Bit

Integrated Device Technology, Inc.

256K (16K x 16-BIT) & 128K (8K x 16-BIT) CMOS STATIC RAM MODULE

IDT8M656S
IDT8M628S

FEATURES:

- High-density 256K/128K-bit CMOS static RAM modules
- 16K x 16 organization (IDT8M656) with 8K x 16 option (IDT8M628)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  - Flexibility in application
- Equivalent to JEDEC standard for future monolithic 16K x 16/8K x 16 static RAMs
- High-speed
  - Military: 50ns (max.)
  - Commercial: 40ns (max.)
- Low power consumption: typically less than 825mW operating (IDT8M656), less than 40mW in standby
- Utilizes IDT7164s—high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 40-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT8M656S/IDT8M628S are 256K/128K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic substrate using four IDT7164 8K x 8 static RAMs (IDT8M656S) or two IDT7164 static RAMs (IDT8M628S) in leadless chip carriers.

Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{13} to select one of the two 8K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On the IDT8M628S 8K x 16 option, A_{13} needs to be externally grounded for proper operation.) Extremely high speeds are achievable by the use of IDT7164s fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 256K/128K static RAMs available.

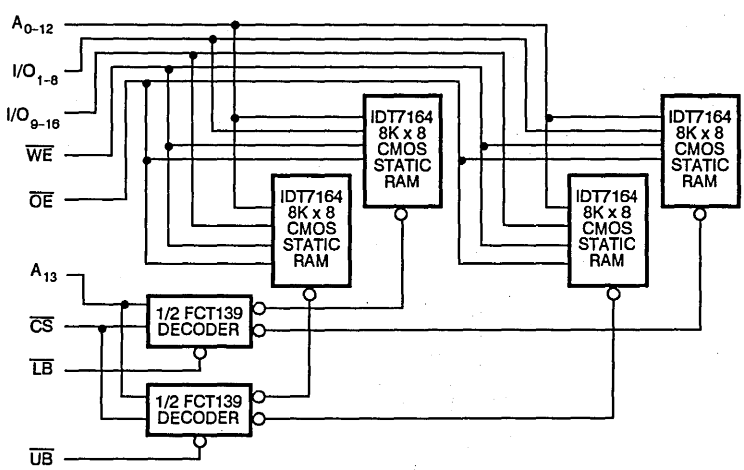
The IDT8M656S/IDT8M628S are available with access times as fast as 40ns over the commercial temperature range, with maximum operating power consumption of only 1.98W (IDT8M656S 16K x 16 option). The module also offers a full standby mode of 440mW (max.).

The IDT8M656S/IDT8M628S are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT7164s in leadless chip carriers.

All inputs and outputs of the IDT8M656S/IDT8M628S are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



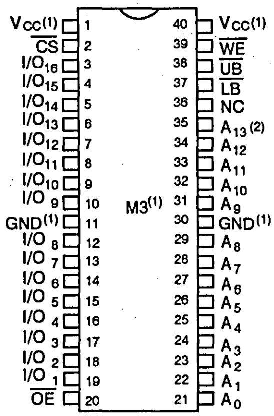
CEMOS is a trademark of Integrated Device Technology, Inc.

13

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-7018/-

PIN CONFIGURATION



DIP
TOP VIEW

1. For module dimensions, please refer to module drawing M3 in the packaging section.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN NAMES

A_{0-13}	Addresses
I/O_{1-16}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control

NOTES:

1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. On IDT8M628S, 128K (8K x 16-Bit) option, A_{13} (pin 35) is required external grounding for proper operation.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5 [1]	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to 125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} = - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT8M656S MIN.	IDT8M656S TYP.[1]	IDT8M656S MAX.	IDT8M628S MIN.	IDT8M628S TYP.[1]	IDT8M628S MAX.	UNIT
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	—	15	—	—	15	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	15	—	—	15	µA
I_{CCX16}	Operating Current In X16 Mode	$\overline{CS}$, $\overline{UB}$ & $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	—	165	360	—	160	320	mA
I_{CCX8}	Operating Current In X8 Mode	$\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	—	100	220	—	82	180	mA
I_{SB} & I_{SB1}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or $\overline{UB}$ ≥ V_{IH} and $\overline{LB}$ ≥ V_{IH} V_{CC} = Max. Output Open	—	8	80[2]	—	4	40[2]	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	—	2.4	—	—	V

NOTE:
1. V_{CC} = 5V, T_A = +25°C
2. I_{SB} and I_{SB1} of IDT8M656S/IDT8M628S at commercial temperature = 60mA/30mA.

13

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

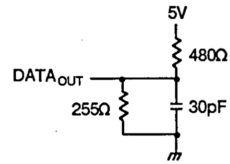


Figure 1. Output Load

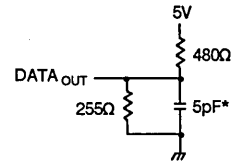


Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT8M656S40 IDT8M628S40 MIN.	MAX	IDT8M656S50 IDT8M628S50 MIN.	MAX	IDT8M656S70 IDT8M628S70 MIN.	MAX.	IDT8M628S85 IDT8M656S85 MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	40	–	50	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	40	–	50	–	70	–	85	ns
t_{ACS}	Chip Select Access Time	–	40	–	50	–	70	–	85	ns
$t_{CLZ1,2}$(1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	25	–	30	–	40	–	50	ns
t_{OLZ}	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{CHZ}(1)	Chip Select to Output in High Z	–	15	–	20	–	30	–	35	ns
t_{OHZ}(1)	Output Disable to Output in High Z	–	15	–	20	–	30	–	35	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	ns
t_{PU}(1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}(1)	Chip Deselect to Power Down Time	–	40	–	50	–	70	–	85	ns
t_{WC}	Write Cycle Time	40	–	50	–	70	–	85	–	ns
t_{CW}	Chip Selection to End of Write	35	–	45	–	65	–	75	–	ns
t_{AW}	Address Valid to End of Write	35	–	45	–	65	–	75	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	10	–	10	–	ns
t_{WP}	Write Pulse Width	30	–	40	–	55	–	65	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	10	–	ns
t_{WHZ}(1)	Write Enable to Output in High Z	–	15	–	20	–	30	–	35	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	30	–	35	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	ns
t_{OW}(1)	Output Active from End of Write	5	–	5	–	5	–	5	–	ns

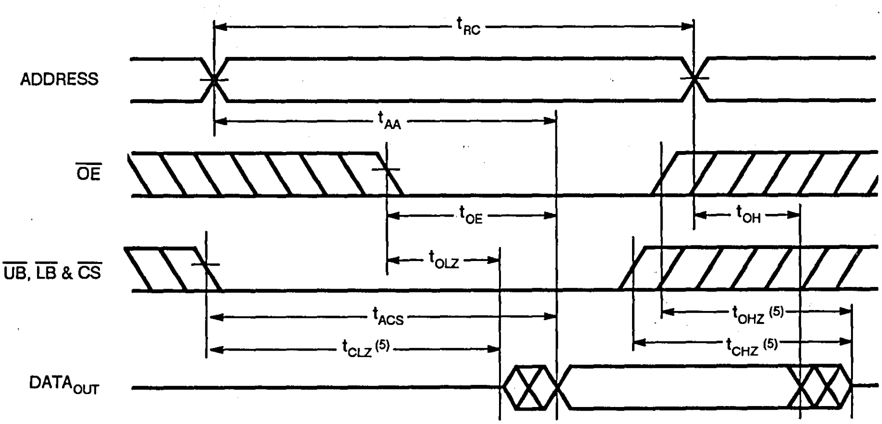
NOTE:
1. This parameter guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS (V_{CC}= 5V ±10%, T_A= -55°C to +125°C)

SYMBOL	PARAMETER	IDT8M656S50 IDT8M628S50 MIN.	MAX.	IDT8M656S60 IDT8M628S60 MIN.	MAX	IDT8M656S70 IDT8M628S70 MIN.	MAX.	IDT8M656S85 IDT8M628S85 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	50	–	60	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	50	–	60	–	70	–	85	ns
t_{ACS}	Chip Select Access Time	–	50	–	60	–	70	–	85	ns
$t_{CLZ1,2}$(1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	30	–	35	–	40	–	50	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{CHZ}(1)	Chip Select to Output in High Z	–	20	–	25	–	30	–	35	ns
t_{OHZ}(1)	Output Disable to Output in High Z	–	20	–	25	–	30	–	35	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	ns
t_{PU}(1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}(1)	Chip Deselect to Power Down Time	–	50	–	60	–	70	–	85	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	50	–	60	–	70	–	85	–	ns
t_{CW}	Chip Selection to End of Write	45	–	55	–	65	–	75	–	ns
t_{AW}	Address Valid to End of Write	45	–	55	–	65	–	75	–	ns
t_{AS}	Address Set-up Time	5	–	10	–	10	–	10	–	ns
t_{WP}	Write Pulse Width	40	–	45	–	55	–	65	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	10	–	ns
t_{WHZ}(1)	Write Enable to Output in High Z	–	20	–	20	–	25	–	30	ns
t_{DW}	Data to Write Time Overlap	20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	ns
t_{OW}(1)	Output Active from End of Write	5	–	5	–	5	–	5	–	ns

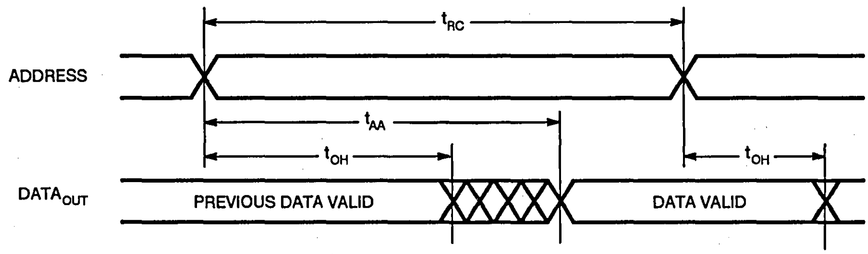
NOTE:
1. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

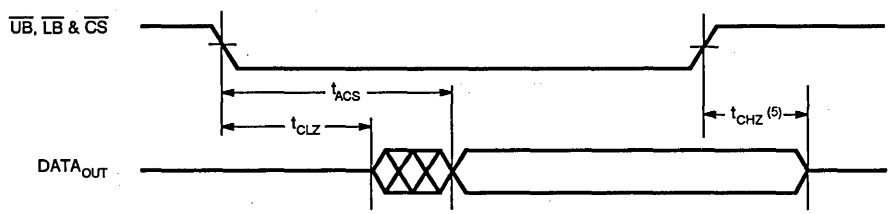


13

TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



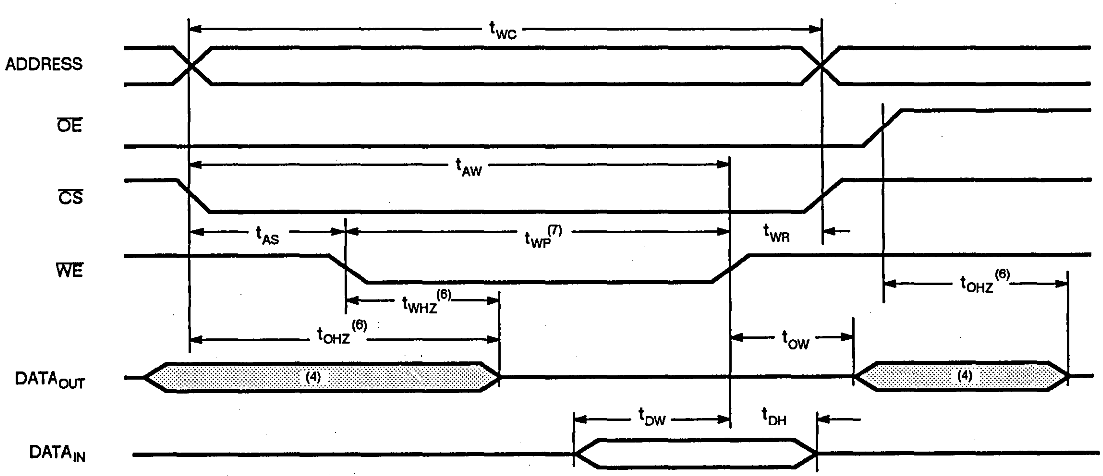
TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]



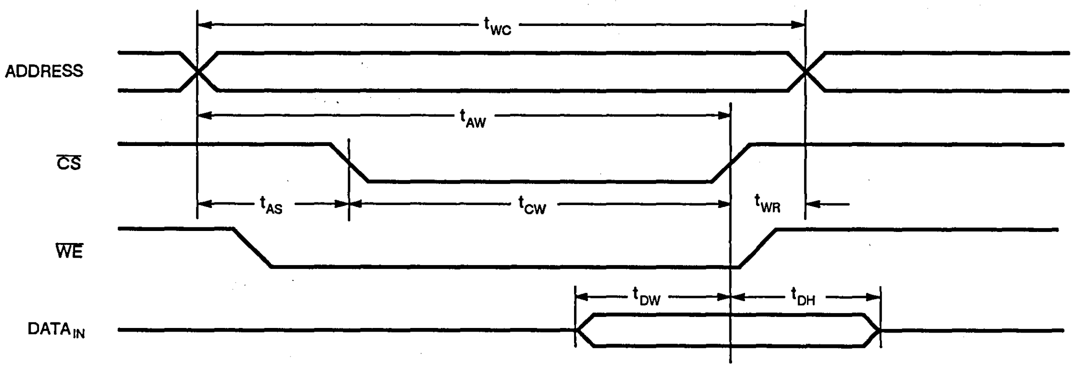
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{UB}$, $\overline{LB}$ = V_{IL} for 16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ± 200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	X	X	High Z	Standby
Standby	L	H	H	X	X	High Z	Standby
Read	L	L	L	L	H	$DATA_{OUT\,1-16}$	Active
Lower Byte Read	L	H	L	L	H	$DATA_{OUT\,1-8}$	Active (X8)
Upper Byte Read	L	L	H	L	H	$DATA_{OUT\,9-16}$	Active (X8)
Read	L	L	L	H	H	High Z	Active
Lower Byte Read	L	H	L	H	H	High Z	Active (X8)
Upper Byte Read	L	L	H	H	H	High Z	Active (X8)
Write	L	L	L	X	L	$DATA_{IN\,1-16}$	Active
Lower Byte Write	L	H	L	X	L	$DATA_{IN\,1-8}$	Active (X8)
Upper Byte Write	L	L	H	X	L	$DATA_{IN\,9-16}$	Active (X8)

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER (1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

13

ORDERING INFORMATION

IDT XXXX A 999 A A

IDT	XXXX	A	999	A	A
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range:

BLANK	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

C	Sidebraze DIP

Speed:

40 50 60 70 85	Speed in Nanoseconds

Power:

S	Standard Power

Device Type:

8M656	16K x 16 - Bit
8M628	8K x 16 - Bit

Integrated Device Technology, Inc.

1 MEGABIT (128K x 8-BIT) CMOS STATIC RAM MODULE

IDT8M824S

FEATURES:

- High-density 1024K (128K x 8) CMOS static RAM module
- Equivalent to JEDEC standard for future monolithic 128K x 8 static RAMs
- High-speed
  - Military: 60ns (max.)
  - Commercial: 40ns (max.)
- Low power consumption
  - Active: less than 550mW (typ.)
  - Standby: less than 20mW (typ.)
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 32-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT8M824S is a1024K (131,072 x 8-bit) high-speed static RAM constructed on a co-fired ceramic substrate using four IDT71256 32K x 8 static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic one megabit static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} and A_{16} to select one of the four 32K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

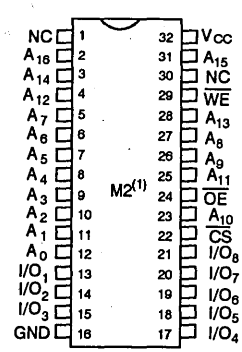
The IDT8M824S is available with maximum access times as fast as 40ns for commercial temperature range, with maximum power consumption of 1.2 watts. The module offers a full standby mode of 440mW (max.).

The IDT8M824S is offered in a 32-pin, 600 mil center sidebraze DIP, adhering to JEDEC standards for one megabit monolithic pinouts, allowing for compatibility with future monolithics.

All inputs and outputs of the IDT8M824S are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

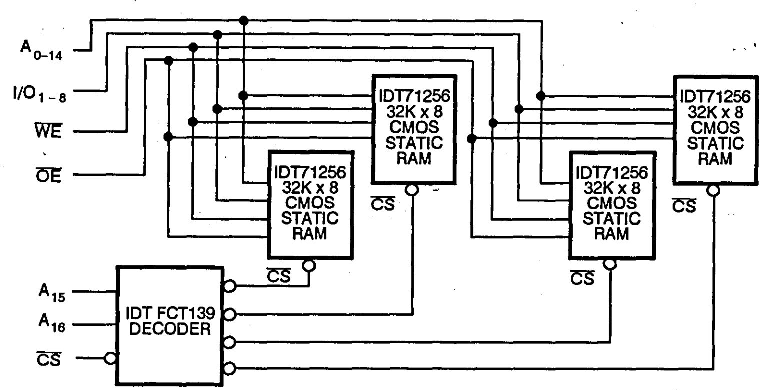
PIN CONFIGURATION



DIP
TOP VIEW

1. For module dimensions, please refer to module drawing M2 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{0-16}	Addresses	$\overline{WE}$	Write Enable
I/O_{0-8}	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	GND	Ground
V_{CC}	Power		

CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ±10%
Commercial	0°C to +70°C	0V	5.0V ±10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT8M824S MIN.	TYP.[1]	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	–	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open f = 0	–	60	160	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	–	110	210	mA
I_{SB} & I_{SB1}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} V_{CC} = Max. Output Open	–	4	80[2]	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	–	–	V

NOTES:
1. V_{CC} = 5V, T_A = +25°C
2. I_{SB} and I_{SB1} of IDT8M824S at commercial temperature = 60mA.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

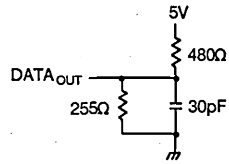


Figure 1. Output Load

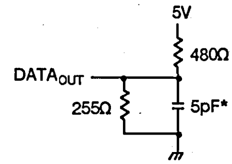


Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

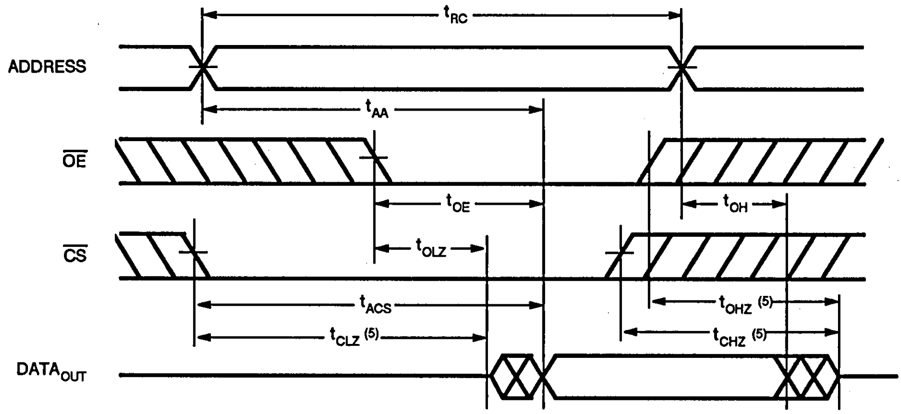
*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to +70°C and -55°C to +125°C)

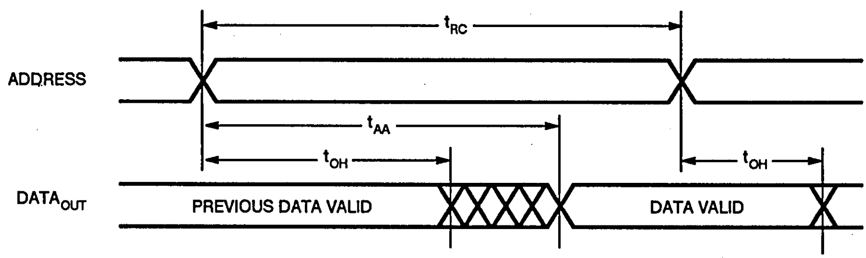
SYMBOL	PARAMETERS	8M824S40 (COM'L ONLY)		8M824S45 (COM'L ONLY)		8M824S50 (COM'L ONLY)		8M824S60		8M824S70		8M824S85 (MIL ONLY)		8M824S100 (MIL ONLY)		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE																
t_{RC}	Read Cycle Time	40	–	45	–	50	–	60	–	70	–	85	–	100	–	ns
t_{AA}	Address Access Time	–	40	–	45	–	50	–	60	–	70	–	85	–	100	ns
t_{ACS}	Chip Select Access Time	–	40	–	45	–	50	–	60	–	70	–	85	–	100	ns
$t_{CLZ1,2}{}^{(1)}$	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	25	–	25	–	30	–	35	–	40	–	50	–	60	ns
$t_{OLZ}{}^{(1)}$	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
$t_{CHZ}{}^{(1)}$	Chip Select to Output in High Z	–	20	–	20	–	20	–	25	–	30	–	35	–	40	ns
$t_{OHZ}{}^{(1)}$	Output Disable to Output in High Z	–	20	–	20	–	20	–	25	–	30	–	35	–	40	ns
t_{OH}	Output Hold from Address Change	3	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
$t_{PU}{}^{(1)}$	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	0	–	ns
$t_{PD}{}^{(1)}$	Chip Deselect to Power Down Time	–	40	–	45	–	50	–	60	–	70	–	85	–	100	ns
WRITE CYCLE																
t_{WC}	Write Cycle Time	40	–	45	–	50	–	60	–	70	–	85	–	100	–	ns
t_{CW}	Chip Selection to End of Write	35	–	40	–	45	–	55	–	65	–	75	–	90	–	ns
t_{AW}	Address Valid to End of Write	35	–	40	–	45	–	55	–	65	–	75	–	90	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	30	–	35	–	40	–	50	–	60	–	70	–	80	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	5	–	5	–	10	–	10	–	ns
$t_{WHZ}{}^{(1)}$	Write Enable to Output in High Z	–	15	–	15	–	20	–	25	–	30	–	35	–	40	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	20	–	25	–	30	–	35	–	40	–	ns
t_{DH}	Data Hold from Write Time	3	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
$t_{OW}{}^{(1)}$	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns

NOTE:
1. This parameter guaranteed but not tested.

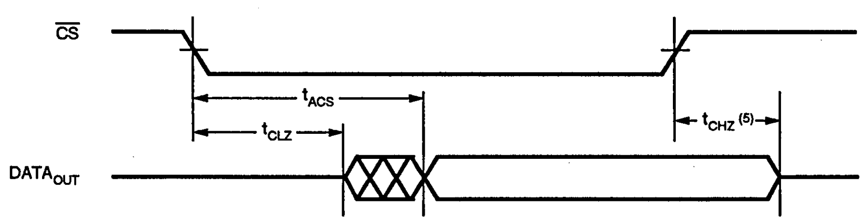
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 2, 4]



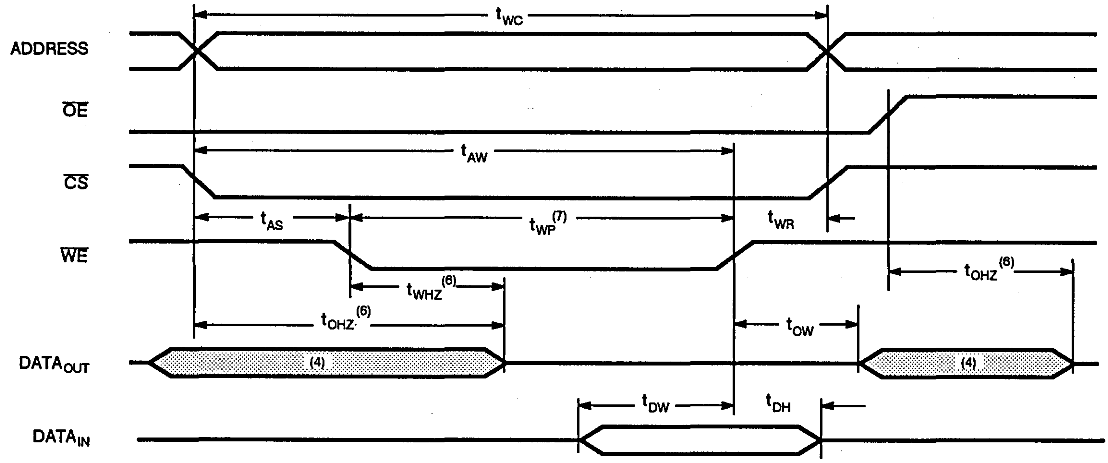
TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]



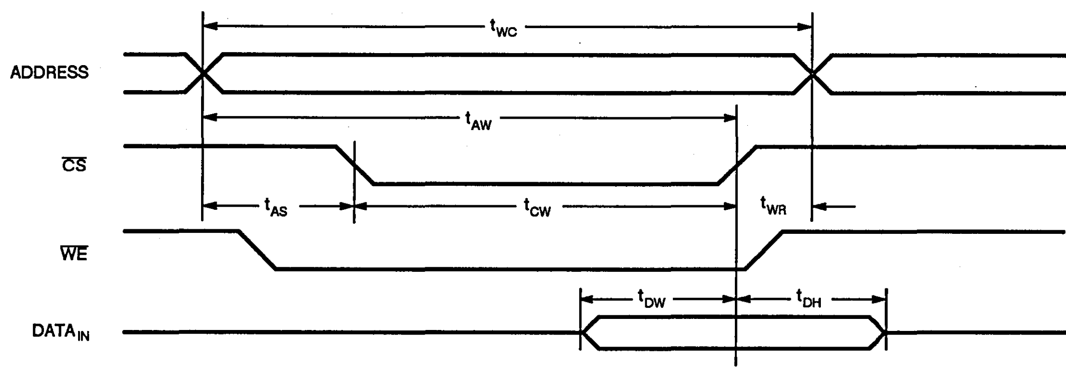
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



13

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TRUTH TABLE

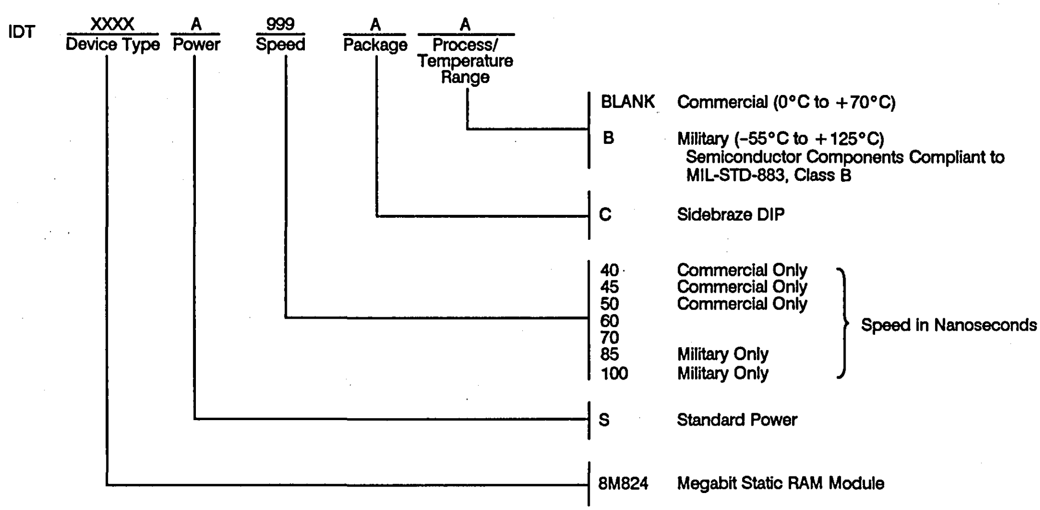
MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	X	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER [1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

256K (32K x 8-BIT) CMOS STATIC RAM MODULE (Low-Power Version)

IDT8M856L

FEATURES:

- High-density 256K (32K x 8-bit) CMOS static RAM module
- Equivalent to JEDEC standard for future monolithic 32K x 8 static RAMs
- High-speed—45ns (max.) commercial; 55ns (max.) military
- Low power consumption; typically less than 225mW operating, less than 500μW in full standby
- Utilizes IDT7164s—high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Pin-compatible with IDT7M864 (8K x 8 SRAM module)
- Offered in the JEDEC standard 28-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT8M856 is a 256K (32,768 x 8-bit) high-speed static RAM constructed on a co-fired ceramic substrate using four IDT7164 (8,192 x 8) static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic 256K static RAMs is achieved by utilization of an on-board decoder circuit that interprets the higher order address A_{13} and A_{14} to select one of the four 8K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 64K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

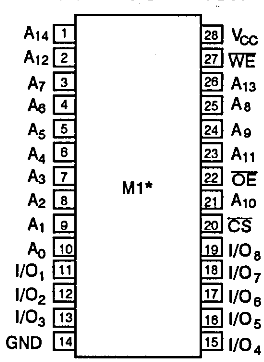
The IDT8M856 is available with maximum access times as fast as 45ns for commercial and 55ns for military temperature ranges, with maximum power consumption of only 825mW. The circuit also offers a substantially low-power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to a standby mode with power consumption of only 83mW (max.).

The IDT8M856 is offered in a 28-pin, 600 mil center sidebraze DIP. This provides four times the density of the IDT7M864 (8K x 8 module) in the same socket, with only minor pin assignment changes. In addition, the JEDEC standard for 256K monolithic pinouts has been adhered to, allowing for compatibility with 256K monolithics.

All inputs and outputs of the IDT8M856 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

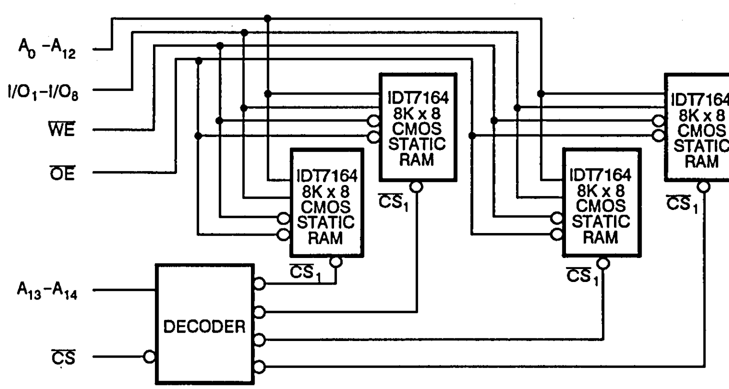
All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



NOTE:

* For module dimensions, please refer to module drawing M1 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN NAMES

A_0 - A_{14}	Addresses	$\overline{WE}$	Write Enable
I/O_1 - I/O_8	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	GND	Ground
V_{CC}	Power		

13

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, T_A = –55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.[1]	COM'L. MAX.	MIL. MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	–	5	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = 5.5V, $\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	–	5	10	µA
I_{CC1}	Operating Power Supply Current	V_{CC} = 5.5V, $\overline{CS}$ = V_{IL}, Output Open, f = 0	–	45	90	100	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = 5.5V, $\overline{CS}$ = V_{IL}, Output Open, f = f_{MAX}	–	70	140	150	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} (TTL Level), V_{CC} = 5.5V, Output Open	–	2.5	15	20	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V (CMOS Level) V_{IN} ≥ V_{CC} – 0.2V or ≤ 0.2V	–	0.1	1	4.5	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = 4.5V I_{OL} = 8mA, V_{CC} = 4.5V	– –	– –	0.5 0.4	0.5 0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = 4.5V	2.4	–	–	–	V

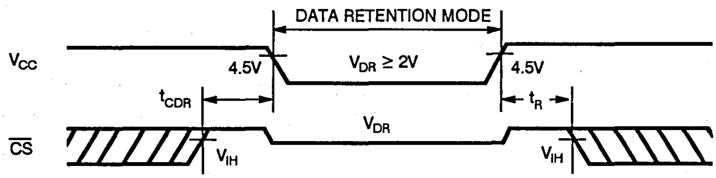
NOTE:
1. V_{CC} = 5V, T_A = +25°C

DATA RETENTION CHARACTERISTICS (T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	COM'L. MAX.	MIL. MAX.	UNIT
V_{DR}	V_{CC} for Retention Data	–	2.0	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} \leq V_{CC}$ -0.2V or ≥ 0.2V	– –	– –	1000(2) 1500(3)	4000(2) 6000(3)	µA
t_{CDR}	Chip Deselect to Data Retention Time		0	–	–	–	ns
t_R	Operation Recovery Time		t_{RC} (4)	–	–	–	ns

NOTES:
1. T_A = +25°C
2. @ V_{CC} = 2V
3. @ V_{CC} = 3V
4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

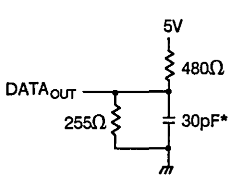


Figure 1. Output Load

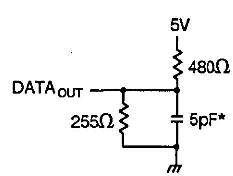


Figure 2. Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

* Including scope and jig.

13

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

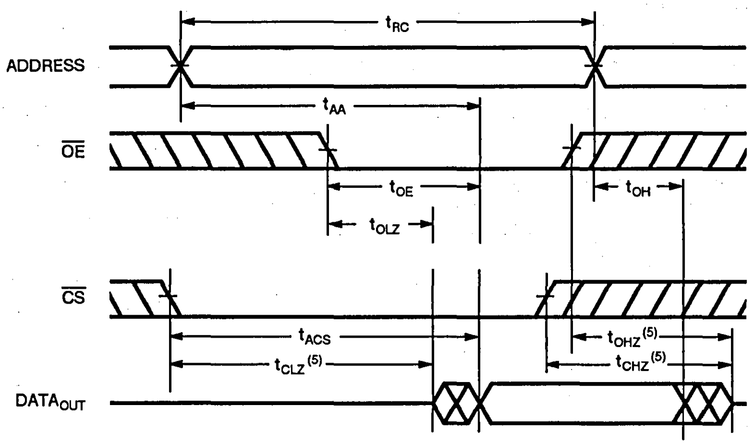
SYMBOL	PARAMETER	IDT8M856L45 MIN.	IDT8M856L45 MAX.	IDT8M856L50 MIN.	IDT8M856L50 MAX.	IDT8M856L60 MIN.	IDT8M856L60 MAX.	IDT8M856L70 MIN.	IDT8M856L70 MAX.	IDT8M856L85 MIN.	IDT8M856L85 MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	45	–	50	–	60	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	45	–	50	–	60	–	70	–	85	ns
t_{ACS}	Chip Select Access Time	–	45	–	50	–	55	–	65	–	85	ns
t_{CLZ}	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	25	–	35	–	40	–	45	–	55	ns
t_{OLZ}	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Select to Output in High Z	–	20	–	20	–	20	–	25	–	30	ns
t_{OHZ}	Output Disable to Output in High Z	–	20	–	20	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time	–	45	–	50	–	60	–	70	–	85	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	45	–	50	–	60	–	70	–	85	–	ns
t_{CW}	Chip Select to End of Write	40	–	45	–	50	–	60	–	70	–	ns
t_{AW}	Address Valid to End of Write	40	–	45	–	50	–	60	–	70	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	10	–	10	–	15	–	ns
t_{WP}	Write Pulse Width	35	–	35	–	40	–	45	–	50	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output High Z	–	20	–	20	–	25	–	30	–	40	ns
t_{DW}	Data to Write Time Overlap	20	–	20	–	25	–	30	–	40	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	5	–	ns
t_{OW}	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

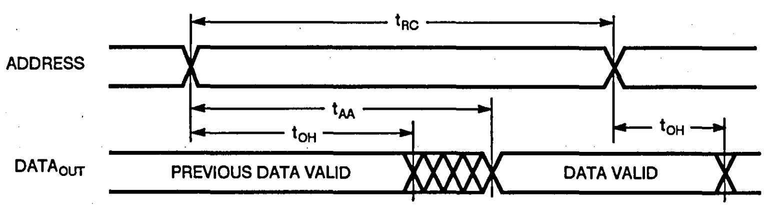
SYMBOL	PARAMETER	IDT8M856L55 MIN.	IDT8M856L55 MAX.	IDT8M856L65 MIN.	IDT8M856L65 MAX.	IDT8M856L75 MIN.	IDT8M856L75 MAX.	IDT8M856L90 MIN.	IDT8M856L90 MAX.	IDT8M856L100 MIN.	IDT8M856L100 MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	55	–	65	–	75	–	90	–	100	–	ns
t_{AA}	Address Access Time	–	55	–	65	–	75	–	90	–	100	ns
t_{ACS}	Chip Select Access Time	–	55	–	55	–	65	–	80	–	90	ns
t_{CLZ}	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	40	–	45	–	50	–	60	–	65	ns
t_{OLZ}	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Select to Output in High Z	–	20	–	25	–	30	–	35	–	40	ns
t_{OHZ}	Output Disable to Output in High Z	–	20	–	25	–	30	–	35	–	40	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time	–	55	–	65	–	75	–	90	–	100	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	55	–	65	–	75	–	90	–	100	–	ns
t_{CW}	Chip Select to End of Write	50	–	55	–	65	–	75	–	85	–	ns
t_{AW}	Address Valid to End of Write	50	–	55	–	65	–	75	–	85	–	ns
t_{AS}	Address Set-up Time	5	–	10	–	10	–	15	–	15	–	ns
t_{WP}	Write Pulse Width	40	–	45	–	45	–	50	–	55	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output High Z	–	25	–	30	–	40	–	50	–	50	ns
t_{DW}	Data to Write Time Overlap	25	–	30	–	35	–	45	–	45	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	5	–	ns
t_{OW}	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	ns

13

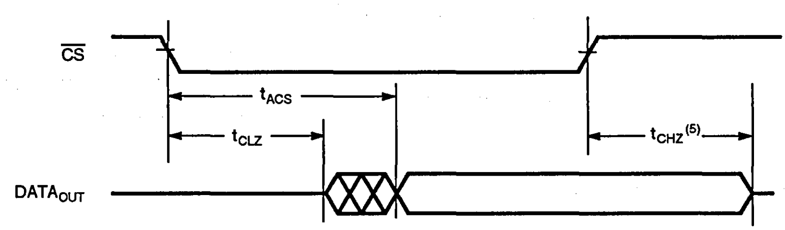
TIMING WAVEFORM OF READ CYCLE NO. 1 [1]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 2, 4]

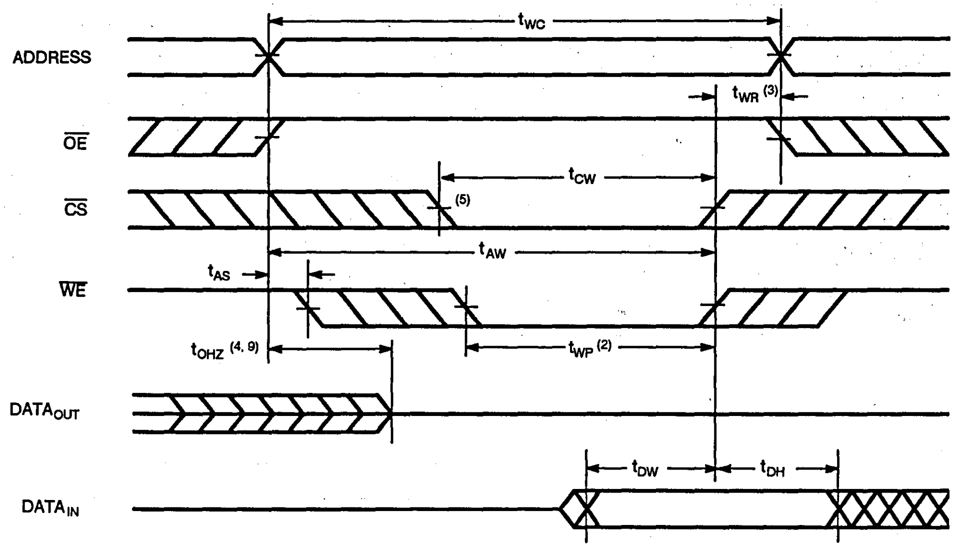


TIMING WAVEFORM OF READ CYCLE NO. 3 [1, 3, 4]

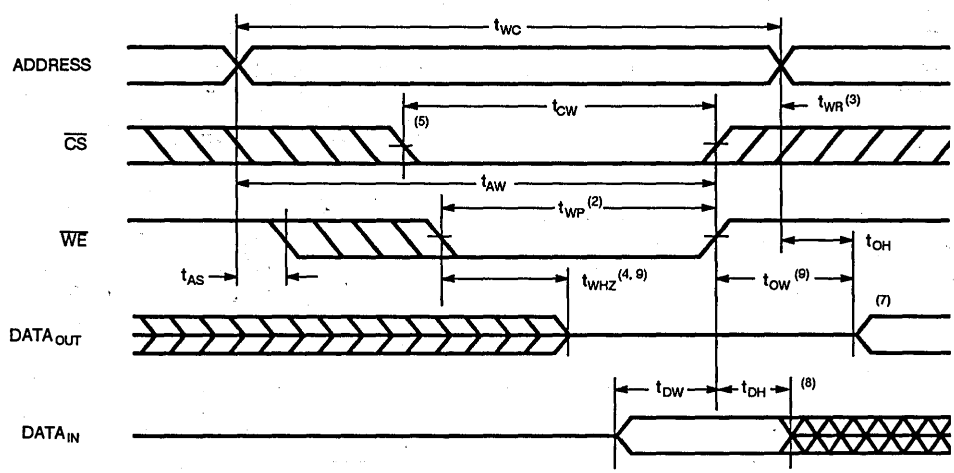


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (1, 6)



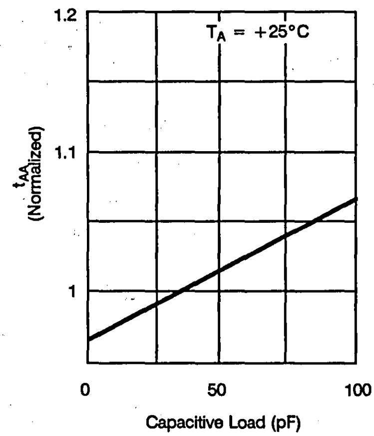
NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. DATA$_{OUT}$ is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	X	L	D_{IN}	Active

Address Access Time vs. Capacitive Load



CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	26	pF

NOTE:

1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Semiconductor Components Compliant to MIL-STD-883, Class B
C	Sidebraze DIP
COM'L. 45 50 60 70 85	MIL. 55 65 75 90 100 — Speed in Nanoseconds
L	Low Power
8M856	32K x 8-Bit

8K x 112 WRITABLE CONTROL STORE STATIC RAM MODULE

ADVANCE INFORMATION
IDT7MB6042

Integrated Device Technology, Inc.

FEATURES:

- 8K x 112 high-performance Writable Control Store (WCS)
- Serial Protocol Channel (SPC™)—reading, writing and interrogation
- High fanout pipeline register
- Width expandable
- Designed for high-speed writable control store applications
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Compact quad in-line module
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

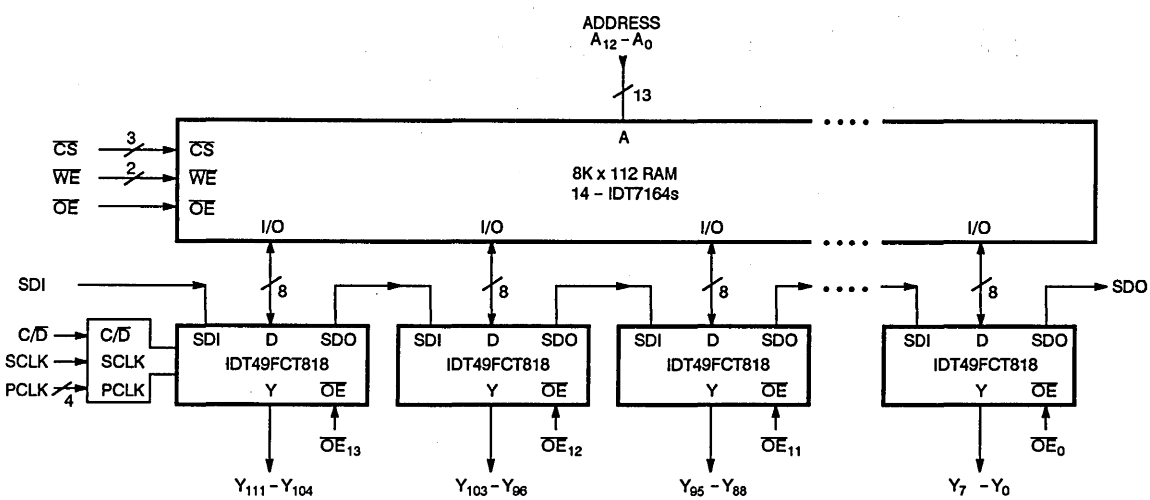
DESCRIPTION:

The IDT7MB6042 is an 8K x 112-bit Writable Control Store (WCS) RAM and pipeline register. It features fourteen 8K x 8 IDT7164 high-performance static RAMs and fourteen IDT49FCT818 Serial Protocol Channel (SPC) registers. These devices are arranged to form the 8K x 112 Writable Control Store RAM with Serial Protocol Channel for loading of the memory. Each eight outputs of the RAM are connected to the D inputs of an IDT49FCT818 in the normal fashion. The device has the serial data-in and serial data-output bits connected to form a 112-bit Serial Protocol Channel register. The command/data (C/$\overline{D}$) and Serial Shift Clock (SCLK) are all bus organized across the fourteen IDT49FCT818 registers. The 112 register output bits, 8 from each device, are separately brought out to form a 112-bit wide pipeline register on the Writable Control Store.

In normal operation, data from the 112-bit wide memory is loaded into the IDT49FCT818 registers on the low-to-high transition of PCLK. Reading and writing of the memory by means of the Serial Protocol Channel are performed using the protocol of the IDT49FCT818. (For details of this operation, please refer to the IDT49FCT818 data sheet.) The data to be loaded can be shifted in the serial data input by using the SCLK and a load command executed by shifting the proper command word in the serial data input when the C/$\overline{D}$ line is in the command mode. This command will then be executed by manipulating the C/$\overline{D}$ line and SCLK line in the desired fashion. Data is then written into the RAM by bringing the write enable line on the RAM memory from the high state to the low state and back to the high state.

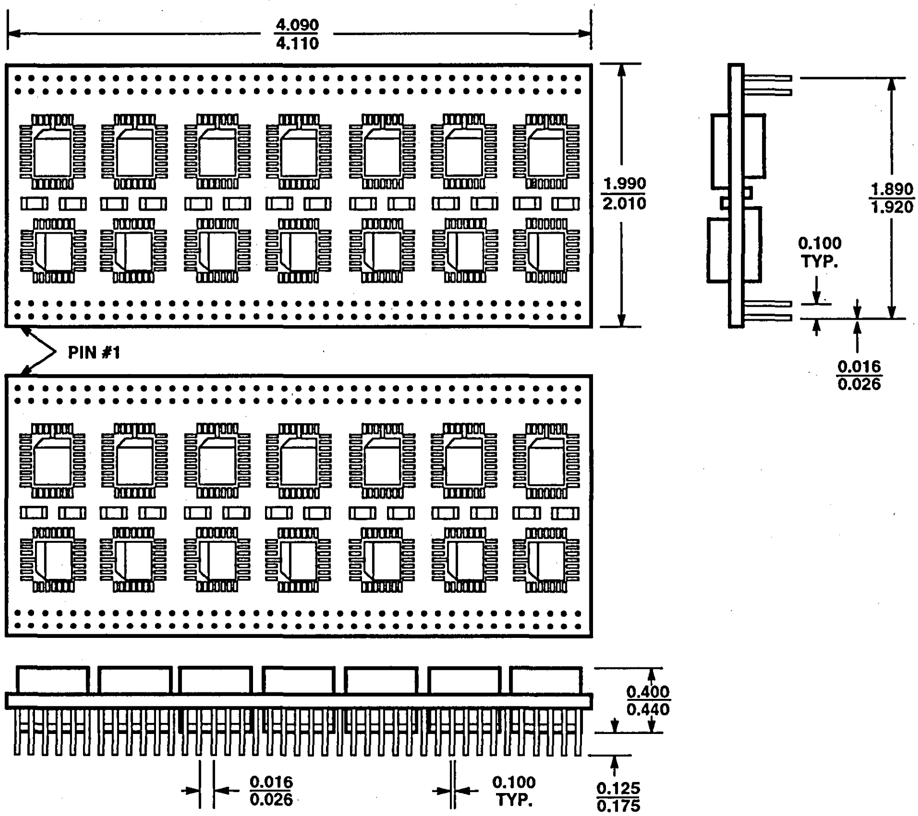
The IDT7MB6042 is offered as a compact, cost-effective plastic quad in-line module and occupies less than 9 square inches of board space.

FUNCTIONAL BLOCK DIAGRAM



13

PACKAGE OUTLINE
164–PIN DIP



Integrated Device Technology, Inc.

512K (64K x 8) SYNCHRONOUS STATIC RAM PLASTIC SIP MODULE

ADVANCE INFORMATION
IDT7MP6025

FEATURES:

- 64K x 8 fully synchronous memory
- High-speed—20MHz read cycle time
- 16-bit synchronous address input
- 8-bit synchronous data input
- Synchronous chip select and write enable
- Separate clock enable for each register
- Low standby power
- Onboard decoupling capacitors
- Available in 43-pin SIP (single in-line package) configuration
- 2 Ground and 2 V_{CC} pins

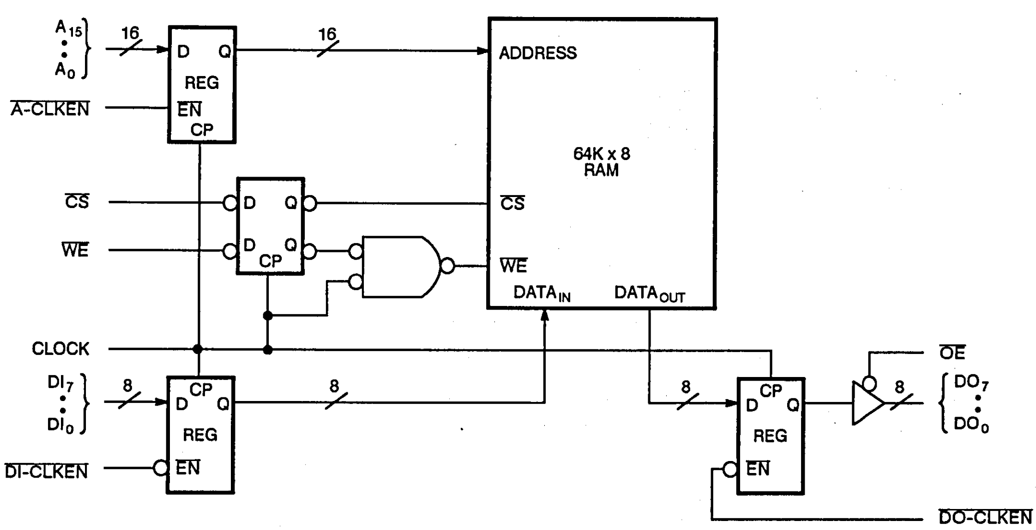
DESCRIPTION:

The IDT7MP6025 is a 64K x 8 synchronous RAM with edge triggered registers on the address lines, data-in bus, data-out bus, chip select and write enable. The edge triggered register of the 16 address lines features an independent clock enable that allows the address register to be selectively loaded. The address register will be loaded on the low-to-high transition of the clock when the clock enable line is low and will hold its current contents on the low-to-high transition of the clock when the clock enable is high. Similarly, the 8-bit data-in register will be loaded with new data on the low-to-high transition of the clock when the data-in clock enable is low and will hold its contents when the data-in clock enable is high. The data-out register will receive new data from the 64K x 8 RAM when the clock enable line is low and will hold its data when the clock enable line is high at the low-to-high transition of the clock. All clock enables, as well as address and data inputs, must meet the appropriate set-up and hold times with respect to the clock.

The eight data output bits are enabled when the output enable is low and are in the high-impedance state when the output enable is high. The chip select and write enable signals are also registered in D flip-flops. These two flip-flops are loaded with new data on each low-to-high transition of the clock. The chip select is passed directly from the Q output of the D-type flip-flop to the 64K x 8 RAM. The write enable signal is gated with the clock signal to generate a delayed write enable pulse. In essence, this gives the output of the address register time to settle and internally select the appropriate byte of RAM before the write enable goes low to write new data into the RAM. Thus, the low-to-high transition of the clock causes the chip select and write enable flip-flops to be loaded with new data and immediately deselects a previous write by means of the clock going high. The data lines to the RAM and the address lines to the RAM may indeed change to new values based on the low-to-high transition of the clock. When the clock goes from high-to-low, if the chip select is low and the write enable is low, a write cycle is begun and the data at the RAM data inputs will be written into the selected address. If the write enable is high or the chip enable is high, data will not be written into the memory.

One of the features of this configuration of memory that have registers on all of the address lines, data input lines and data output lines as well as the control lines, is to provide the highest possible clock rate in the system. All that is necessary is that the data, address, chip select, write enable and clock enables signals meet the required set-up and hold time with respect to the clock. In this manner, fully asynchronous operation is achieved. The IDT7MP6025 is offered as a compact, cost-effective 43-pin plastic SIP module.

FUNCTIONAL BLOCK DIAGRAM



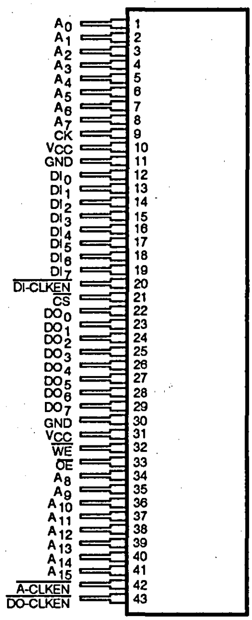
CEMOS is a trademark of Integrated Device Technology, Inc.

13

COMMERCIAL TEMPERATURE RANGE **DECEMBER 1987**

DSC-7022/-

PIN CONFIGURATION

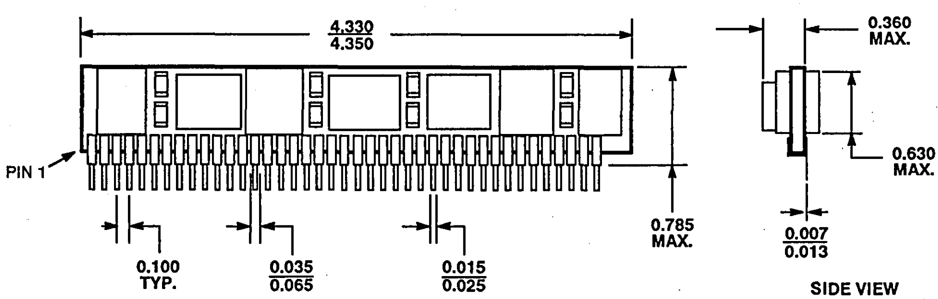


SIP
SIDE VIEW

PIN NAMES

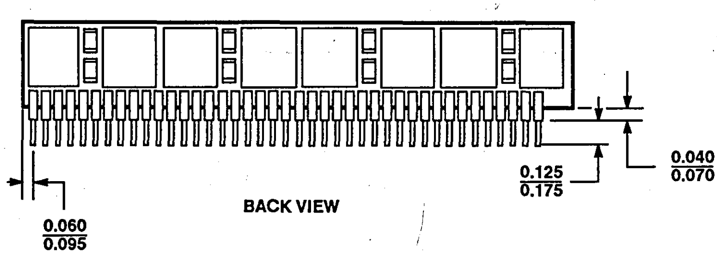
A_{0-15}	Addresses
CK	Clock
DI_{0-7}	Data Input
DO_{0-7}	Data Output
$\overline{\text{DI-CLKEN}}$	Data Input Clock Enable
$\overline{\text{A-CLKEN}}$	Address Clock Enable
$\overline{\text{DO-CLKEN}}$	Data Output Clock Enable
V_{CC}	Power
GND	Ground
$\overline{\text{CS}}$	Chip Select
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable

PACKAGE DIMENSIONS



SIDE VIEW

FRONT VIEW



BACK VIEW

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM MODULE 64K (8K x 8-BIT) & 128K (16K x 8-BIT)

IDT7M134S
IDT7M135S

FEATURES:

- High-density 64K/128K-bit CMOS dual-port RAM modules
- 16K x 8 organization (IDT7M135) with 8K x 8 option (IDT7M134)
- Low power consumption
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- On-chip port arbitration logic
- $\overline{\text{BUSY}}$ flags
- Fully asynchronous operation from either port
- Single 5V (±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- On-chip pull up resistors for open-drain $\overline{\text{BUSY}}$ flag option
- Inputs and outputs directly TTL-compatible
- Fully static operation
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT7M134/135 are 64K/128K-bit high-speed CMOS dual-port static RAM modules constructed on a multi-layered ceramic substrate using four IDT7132 2K x 8 dual-port RAMs (IDT7M134) or eight IDT7132 dual-port RAMs (IDT7M135) in leadless chip carriers. Dual-port function is achieved by utilization of the two on-board IDT54/74FCT138 decoder circuits that interpret the higher order addresses A_{L11-13} and A_{R11-13} to select one of the eight 2K x 8 dual-port RAMs. (On IDT7M134 8K x 8 option, the A_{L13} and A_{R13} need to be externally grounded and the selection becomes one of the four 2K x 8 dual-port RAMs.) Extremely high speeds are achieved in this fashion due to the use of the IDT7132 dual-port RAM, fabricated in IDT's high-performance CEMOS technology.

The IDT7M134/135 provide two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in the memory. The $\overline{\text{BUSY}}$ flags are provided for the situation when both ports simultaneously access the same memory location. The on-chip arbitration logic will determine which port has access and sets the $\overline{\text{BUSY}}$ flag of the delayed port. $\overline{\text{BUSY}}$ is set at speeds that permit the processor to hold the operation and its respective address and data. The delayed port will have access when $\overline{\text{BUSY}}$ goes high (inactive).

The IDT7M134/135 are available with access times as fast as 45ns commercial and 60ns military temperature range, with operating power consumption of only 2.1W/3.5W (max.). The module also offers a standby power mode of 1.4W/2.8W (max.) and a full standby mode of 660mW/1.3W (max.).

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

GND(1)	1	58	V_{CC}(1)
$\overline{CE}_L$	2	57	$\overline{CE}_R$
$R/\overline{W}_L$	3	56	$R/\overline{W}_R$
$R330_L$	4	55	$R330_R$
$\overline{BUSY}_L$	5	54	$BUSY_R$
$\overline{OE}_L$	6	53	$\overline{OE}_R$
A_{0L}	7	52	A_{0R}
A_{1L}	8	51	A_{1R}
A_{2L}	9	50	A_{2R}
A_{3L}	10	49	A_{3R}
A_{4L}	11	48	A_{4R}
A_{5L}	12	47	A_{5R}
A_{6L}	13	46	A_{6R}
A_{7L}	14	45	A_{7R}
A_{8L}	15	M7(3) 44	A_{8R}
A_{9L}	16	43	A_{9R}
A_{10L}	17	42	A_{10R}
A_{11L}	18	41	A_{11R}
A_{12L}	19	40	A_{12R}
A_{13L}(2)	20	39	A_{13}(2)
I/O_{0L}	21	38	I/O_{0R}
I/O_{1L}	22	37	I/O_{1R}
I/O_{2L}	23	36	I/O_{2R}
I/O_{3L}	24	35	I/O_{3R}
I/O_{4L}	25	34	I/O_{4R}
I/O_{5L}	26	33	I/O_{5R}
I/O_{6L}	27	32	I/O_{6R}
I/O_{7L}	28	31	I/O_{7R}
GND(1)	29	30	V_{CC}(1)

DIP
TOP VIEW

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$\overline{BUSY}_L$	$\overline{BUSY}_R$	$\overline{\text{BUSY}}$ Flag (Open Drain)
$R330_L$	$R330_R$	PULL-UP Resistors for Open-drain $\overline{\text{BUSY}}$ Flag option
A_{0L} - A_{13L}	A_{0R} - A_{13R}	Address
I/O_{0L} - IO_{7L}	I/O_{0R} - I/O_{7R}	Data Input/Output
V_{CC}		Power
GND		Ground

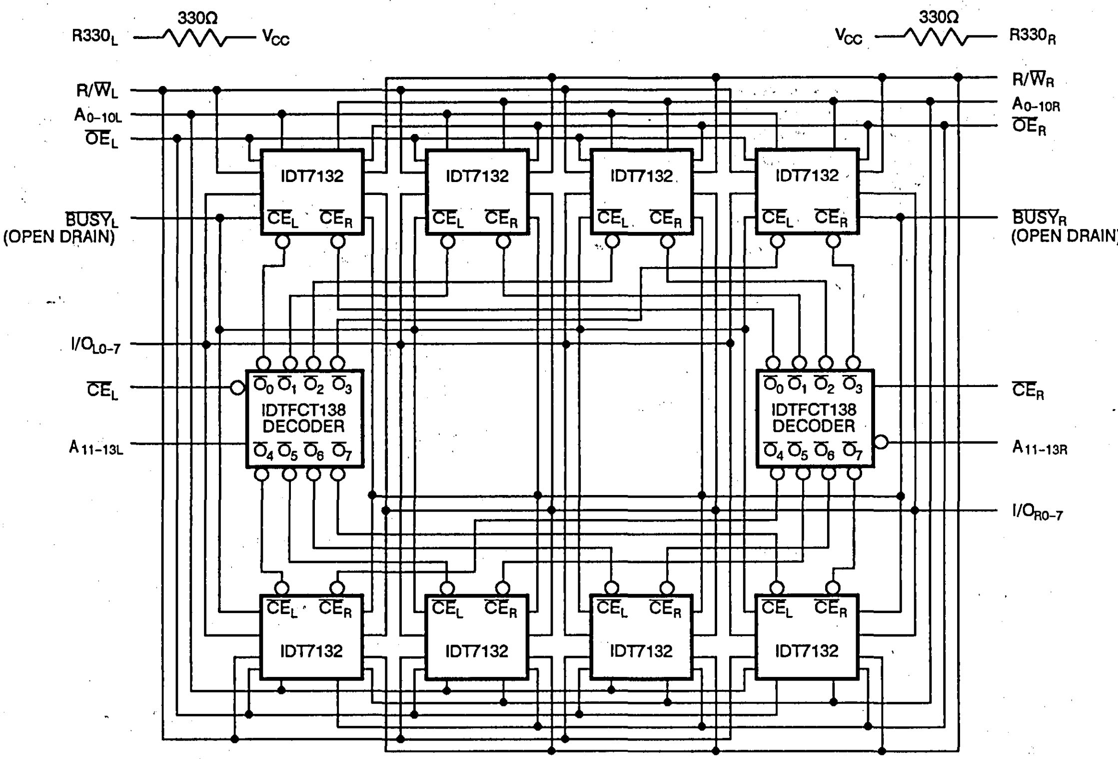
13

NOTES:

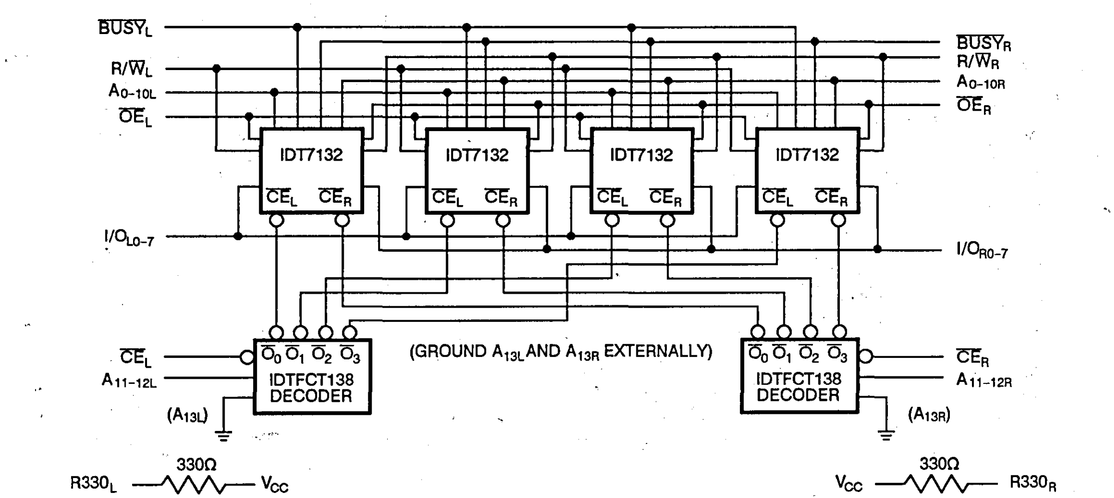
1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. On 8K x 8 IDT7M134 option A_{13L} and A_{13R} need to be externally connected to ground for proper operation.
3. For module dimensions, please refer to module drawing M7 in the packaging section.

FUNCTIONAL BLOCK DIAGRAMS

(A) IDT7M135 (16K x 8-BIT)



(B) IDT7M134 (8K x 8-BIT)



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} = -3.5V for pulse width less than 30ns.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M134S MIN.	IDT7M134S TYP.[1]	IDT7M134S MAX.	IDT7M135S MIN.	IDT7M135S TYP.[1]	IDT7M135S MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	–	15	–	–	20	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	–	15	–	–	20	µA
V_{IH}	Input High Voltage		2.2	–	6.0	2.2	–	6.0	V
V_{IL}	Input Low Voltage		-1.0[2]	–	0.8	-1.0[2]	–	0.8	V
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open	–	190	380	–	320	640	mA
I_{SB}	Standby Current (Both Ports Standby)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$	–	130	260	–	260	520	mA
I_{SB_1}	Standby Current (One Port Standby)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open	–	160	320	–	290	580	mA
I_{SB_2}	Full Standby Current (Both Ports Full Standby)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V	–	4	120[3]	–	10	240[3]	mA
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 3.5mA, V_{CC} = 4.5V	–	–	0.4	–	–	0.4	V
		I_{OL} = 8mA, V_{CC} = 4.5V	–	–	0.5	–	–	0.5	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA, V_{CC} = 4.5V	–	–	0.5	–	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = 4.5V	2.4	–	–	2.4	–	–	V

NOTES:

1. V_{CC} = 5V, T_A = +25°C
2. V_{IL} min. = -3.5V for pulse width less than 30ns.
3. I_{SB_2} max. of IDT7M134/IDT7M135 at commercial temperature = 80mA/150mA.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	7M134S45 7M135S45 (COM'L ONLY)		7M134S50 7M135S50 (COM'L ONLY)		7M134S60 7M135S60		7M134S70 7M135S70		7M134S90 7M135S90		7M134S100 7M135S100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	45	–	50	–	60	–	70	–	90	–	100	–	ns
t_{AA}	Address Access Time	–	45	–	50	–	60	–	70	–	90	–	100	ns
t_{ACE}	Chip Enable Access Time	–	45	–	50	–	60	–	70	–	90	–	100	ns
t_{AOE}	Output Enable Access Time	–	30	–	35	–	40	–	40	–	45	–	50	ns
t_{OH}	Output Hold from Address Change	0	–	0	–	0	–	5	–	10	–	10	–	ns
t_{CLZ}	Chip Select to Output in Low Z	10	–	10	–	10	–	10	–	15	–	15	–	ns
t_{CHZ}	Chip Select to Output in High Z	–	20	–	25	–	35	–	35	–	45	–	50	ns
t_{OHZ}	Output Enable to Output in High Z	–	30	–	40	–	40	–	30	–	40	–	40	ns
t_{OLZ}	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Enable to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Enable to Power Down Time	–	50	–	50	–	50	–	50	–	50	–	50	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	45	–	50	–	60	–	70	–	90	–	100	–	ns
t_{CW}	Chip Selection to End of Write	40	–	45	–	50	–	60	–	80	–	95	–	ns
t_{AW}	Address Valid to End of Write	40	–	45	–	50	–	60	–	80	–	95	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	10	–	10	–	10	–	ns
t_{WP}	Write Pulse Width	35	–	40	–	45	–	40	–	50	–	55	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{DW}	Data Valid to End of Write	25	–	25	–	25	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	5	–	5	–	5	–	10	–	10	–	10	–	ns
t_{OHZ}	Output Enable to Output in High Z	–	20	–	25	–	35	–	35	–	40	–	40	ns
t_{WZ}	Write Enable to Output in High Z	–	20	–	25	–	35	–	35	–	40	–	40	ns
t_{OW}	Output Active from End of Write	0	–	0	–	0	–	0	–	0	–	0	–	ns
BUSY TIMING														
t_{BAA}	$\overline{BUSY}$ Access Time to Address	–	40	–	40	–	45	–	45	–	45	–	50	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	–	35	–	40	–	45	–	45	–	45	–	50	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	–	40	–	40	–	40	–	40	–	40	–	50	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	–	35	–	35	–	35	–	35	–	35	–	50	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data	–	30	–	35	–	40	–	50	–	50	–	60	ns
t_{WDD}	Write Pulse To Data Delay	–	65	–	75	–	85	–	90	–	100	–	120	ns
t_{DDD}	Write Data Valid to Read Data Delay	–	40	–	50	–	60	–	70	–	80	–	100	ns
t_{APS}	Arbitration Priority Set-up Time	10	–	10	–	10	–	10	–	10	–	10	–	ns

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figs. 1, 2 and 3

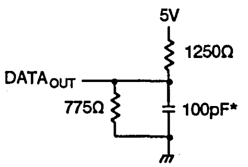


Figure 1. Output Load

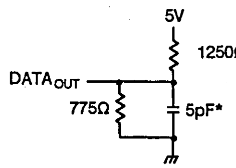


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

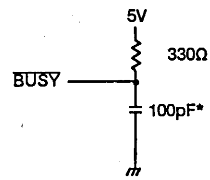


Figure 3. $\overline{\text{BUSY}}$ Output Load

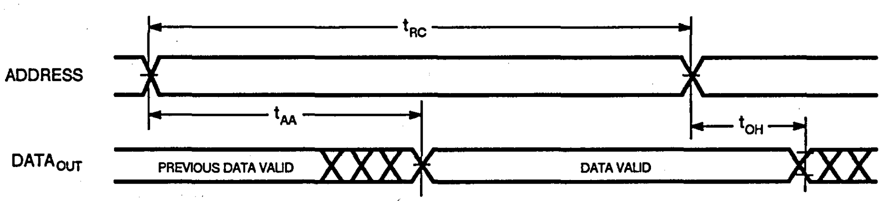
* Including scope and jig.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

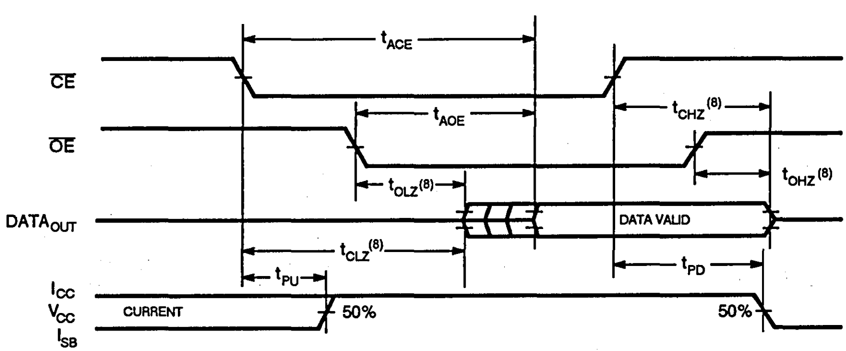
SYMBOL	PARAMETER [1]	CONDITIONS	IDT7M134S [2]	IDT7M135S [2]	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	80	100	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	30	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.
2. Typical value.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE [1, 2, 6]

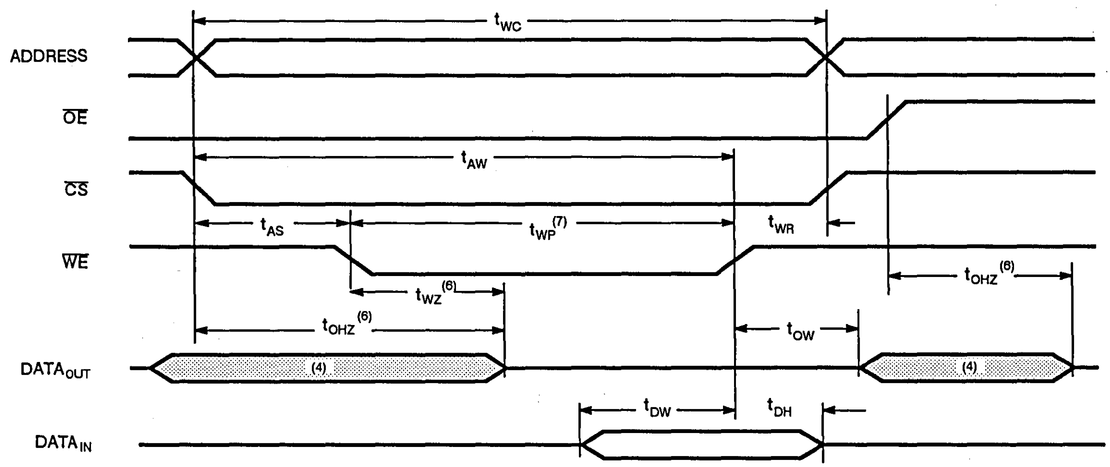


TIMING WAVEFORM OF READ CYCLE NO. 2 EITHER SIDE [1, 3]

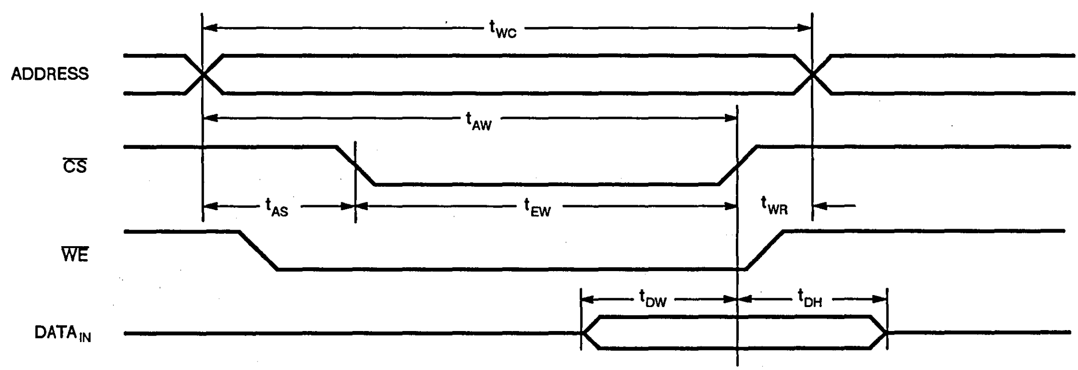


13

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)

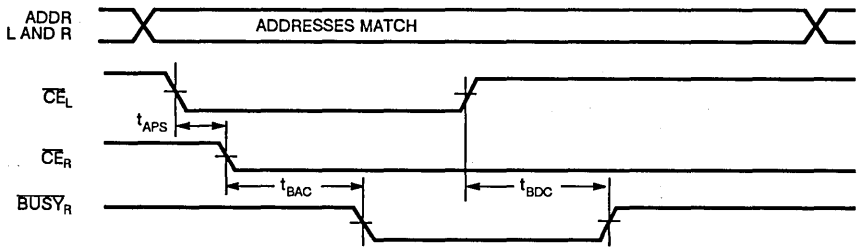


NOTES:

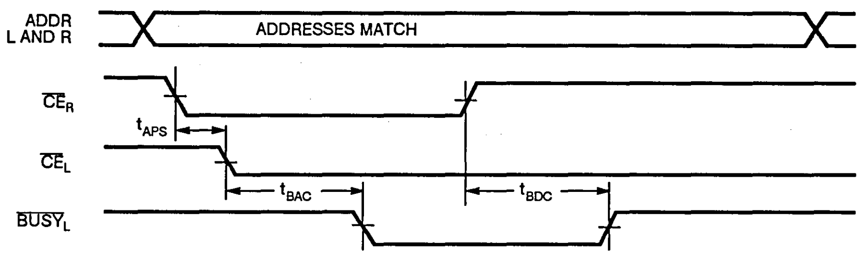
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:

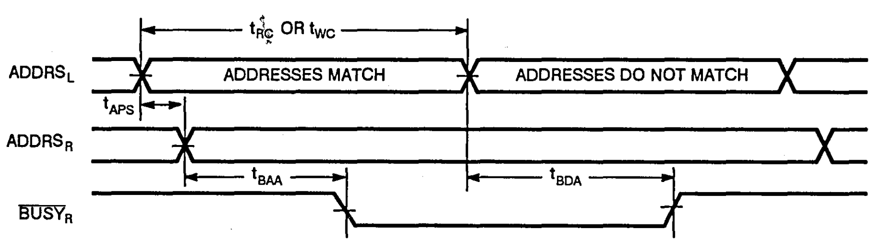


$\overline{CE}_R$ VALID FIRST:

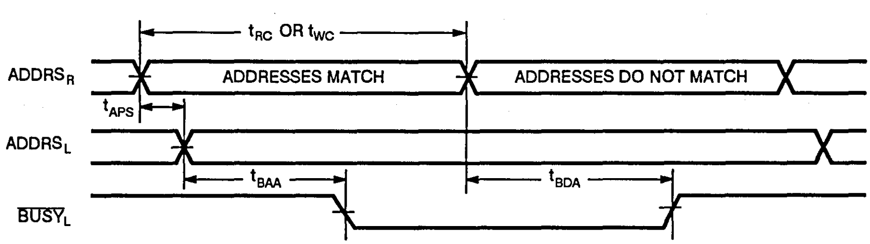


TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(5)

LEFT ADDRESS VALID FIRST:

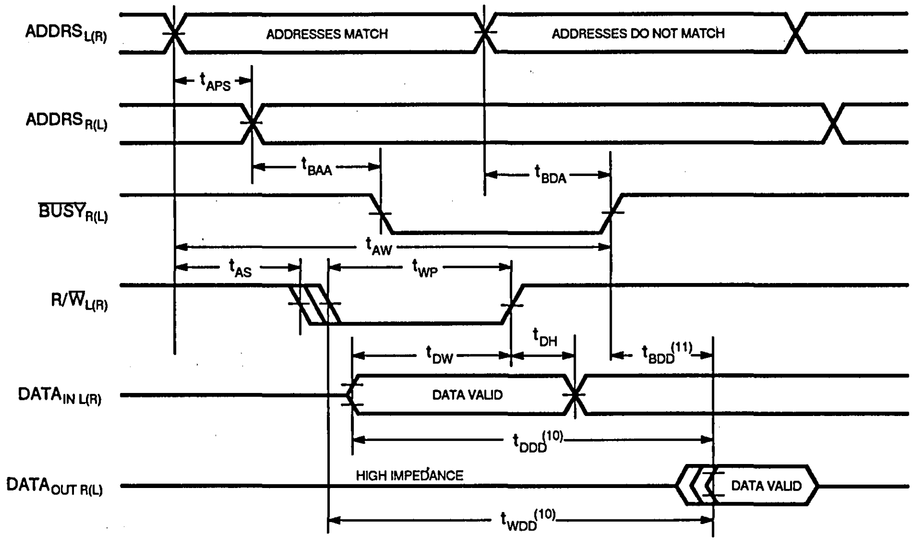


RIGHT ADDRESS VALID FIRST:

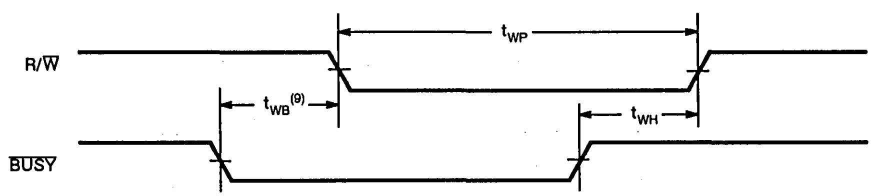


13

TIMING WAVEFORM OF READ WITH BUSY(5)



TIMING WAVEFORM OF WRITE WITH BUSY(5)



NOTES:
1. R/W̄ is high for Read Cycles.
2. Device is continuously enabled, C̄Ē = V_{IL}.
3. Addresses valid prior to or coincident with C̄Ē transition low.
4. If C̄Ē goes high simultaneously with R/W̄ high, the outputs remain in the high impedance state.
5. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
6. $\overline{OE} = V_{IL}$
7. R/W̄ = V_{IH} during address transition.
8. Transition is measured at +500mV from low or high impedance voltage with load (Figures 1, 2 & 3). This parameter is guaranteed by design, but not tested.
9. For SLAVE port (IDT7M144/IDT7M145) only.
10. Port-to-port delay through RAM cells from writing port to reading port.
11. This parameter guaranteed by design, but not tested.

FUNCTIONAL DESCRIPTION

The IDT7M134/135 provide two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7M134/135 have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match down to 10ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and set the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III, Address Arbitration). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "busy lock-out" problem, IDT has developed a MASTER/SALVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I—NON-CONTENTION READ/WRITE CONTROL, LEFT OR RIGHT PORT [1]

$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	I/O_{0-7}	FUNCTION
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB} or I_{SB2}
L	L	X	$DATA_{IN}$	Data on Port Written into Memory [2]
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port [3]
H	L	H	Z	High Impedance Outputs

NOTE:

1. $A_{0L} - A_{13L} \neq A_{0R} - A_{13R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

13

TABLE III – ARBITRATION

LEFT PORT		RIGHT PORT		FLAGS (1)		FUNCTION
$\overline{CE}_L$	A_{0L} – A_{13L}	$\overline{CE}_R$	A_{0L} – A_{13R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R}$–A_{13R}	L	$\neq A_{0L}$–A_{13L}	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV10R	L	LV10R	H	L	Left-Port Wins
L	RV10L	L	LV10L	L	H	Right-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL10R	$= A_{0R}$–A_{13R}	LL10R	$= A_{0L}$–A_{13L}	H	L	Left-Port Wins
RL10L	$= A_{0R}$–A_{13R}	RL10R	$= A_{0L}$–A_{13L}	L	H	Right-Port Wins
LW10R	$= A_{0R}$–A_{13R}	LW10R	$= A_{0L}$–A_{13L}	H	L	Arbitration Resolved
LW10R	$= A_{0R}$–A_{13R}	LW10R	$= A_{0L}$–A_{13L}	L	H	Arbitration Resolved

NOTE:
1. X = DON'T CARE, L = LOW, H = HIGH, Same = Left and Right Addresses match within 10ns of each other.
   LV10R = Left Address Valid $\geq$10ns before Right Address.
   RV10L = Right Address Valid $\geq$10ns before Left Address.
   LL10R = Left $\overline{CE}$ = LOW $\geq$ 10ns before Right $\overline{CE}$.
   RL10L = Right $\overline{CE}$ = LOW $\geq$ 10ns before Left $\overline{CE}$.
   LW10R = Left and Right $\overline{CE}$ = LOW within 10ns of each other.

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range:
- BLANK — Commercial (0°C to +70°C)
- B — Military (-55°C to +125°C) Semiconductor components compliant to MIL-STD-883, Class B

Package:
- C — Sidebraze DIP

Speed in Nanoseconds:
- 45 — Commercial Only
- 50 — Commercial Only
- 60
- 70
- 90
- 100

Power:
- S — Standard Power

Device Type:
- 7M134 — 64K (8K x 8-bit)
- 7M135 — 128K (16K x 8-bit)

Integrated Device Technology, Inc.

256K (32K x 8-BIT) DUAL-PORT CMOS STATIC RAM MODULE

IDT7M137

FEATURES:

- High-density 256K-bit CMOS dual-port RAM module
- 32K x 8 organization
- Low power consumption
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Battery backup operation—2V data retention
- Fully asynchronous operation from either port
- Single 5V(±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Fully static operation
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M137 is a 256K-bit high-speed CMOS dual-port static RAM module constructed on a multi-layered ceramic substrate using eight IDT7134 dual-port RAMs in leadless chip carriers. The full 32K bytes of dual-port RAM are directly addressable by utilization of the two on-board IDT54/74FCT138 decoder circuits that interpret the higher order addresses A_{L12-14} and A_{R12-14} to select one of the eight 4K x 8 dual-port RAMs. Extremely high speeds are achieved in this fashion due to the use of the IDT7134 dual-port RAM, fabricated in IDT's high-performance CEMOS technology.

The IDT7M137 provides two ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in the memory. The IDT7M137 is designed to be used in systems where on-chip hardware port arbitration is not needed. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7M137 is available with access times as fast as 55ns commercial and 60ns military temperature range, with operating power consumption of only 4W (max.) The modules also offer a standby power mode of 3.6W (max.) and full standby mode of 1.3W (max.).

All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

Pin name	Pin	Pin	Pin name
GND(1)	1	58	V_{CC}(1)
$\overline{CE}_L$	2	57	$\overline{CE}_R$
$R/\overline{W}_L$	3	56	$R/\overline{W}_R$
NC	4	55	NC
A_{11L}	5	54	A_{11R}
$\overline{OE}_L$	6	53	$\overline{OE}_R$
A_{0L}	7	52	A_{0R}
A_{1L}	8	51	A_{1R}
A_{2L}	9	50	A_{2R}
A_{3L}	10	49	A_{3R}
A_{4L}	11	48	A_{4R}
A_{5L}	12	47	A_{5R}
A_{6L}	13	46	A_{6R}
A_{7L}	14	45	A_{7R}
A_{8L}	15	44	A_{8R}
A_{9L}	16	43	A_{9R}
A_{10L}	17	42	A_{10R}
A_{12L}	18	41	A_{12R}
A_{13L}	19	40	A_{13R}
A_{14L}(2)	20	39	A_{14R}(2)
I/O_{0L}	21	38	I/O_{0R}
I/O_{1L}	22	37	I/O_{1R}
I/O_{2L}	23	36	I/O_{2R}
I/O_{3L}	24	35	I/O_{3R}
I/O_{4L}	25	34	I/O_{4R}
I/O_{5L}	26	33	I/O_{5R}
I/O_{6L}	27	32	I/O_{6R}
I/O_{7L}	28	31	I/O_{7R}
GND(1)	29	30	V_{CC}(1)

M7(3)

DIP
TOP VIEW

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L-14L}	A_{0R-14R}	Address
I/O_{0L-7L}	I/O_{0R-7R}	Data Input/Output
V_{CC}		Power
GND		Ground

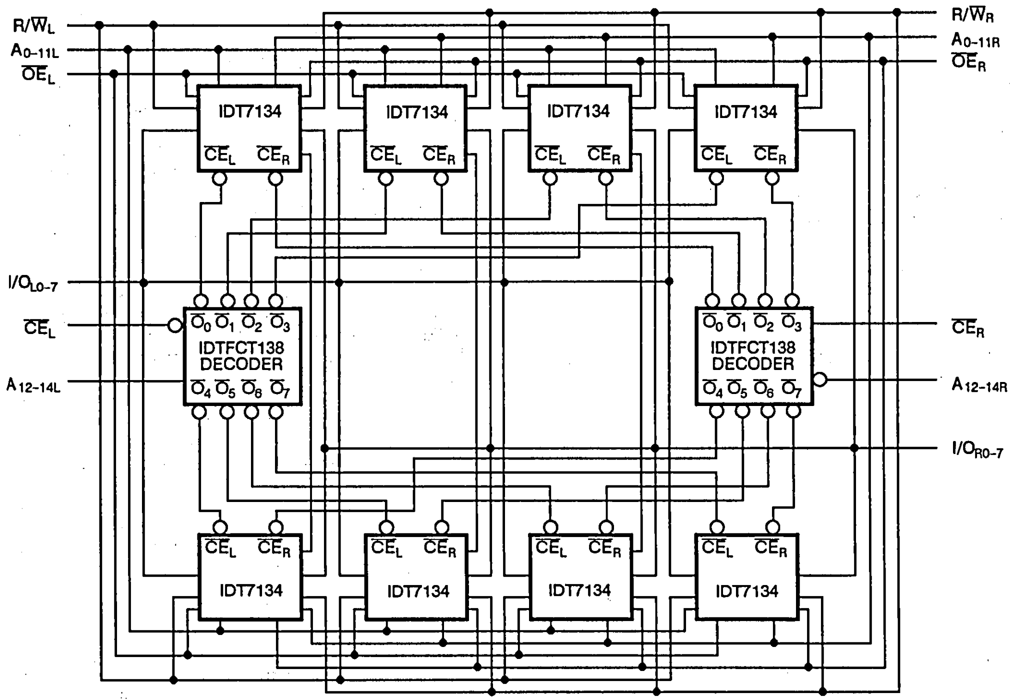
NOTES:

1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. On 16K x 8 IDT7M136 option, A_{14L} and A_{14R} need to be externally connected to ground for proper operation.
3. For module dimensions, please refer to module drawing M7 in the packaging section.

13

CEMOS is a trademark of Integrated Device Technology, Inc.

FUNCTIONAL BLOCK DIAGRAM
IDT7M137 (32K x 8-BIT)



FUNCTIONAL DESCRIPTION:

The IDT7M137 provides two ports with separate controls, address and I/O that permit independent access for reads or writes to any location in memory. The IDT7M137 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} = -3.5V for pulse width less than 30ns.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M137 MIN.	TYP.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	–	20	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	–	20	µA
V_{IH}	Input High Voltage		2.2	–	6.0	V
V_{IL}	Input Low Voltage		-1.0[2]	–	0.8	V
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open	–	275	730	mA
I_{SB}	Standby Current (Both Ports Standby)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$	–	200	560	mA
I_{SB_1}	Standby Current (One Port Standby)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open	–	225	650	mA
I_{SB_2}	Full Standby Current (Both Ports Full Standby)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V	–	8	240[3]	mA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 8mA	–	–	0.4	V
		I_{OL} = 10mA	–	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	–	V

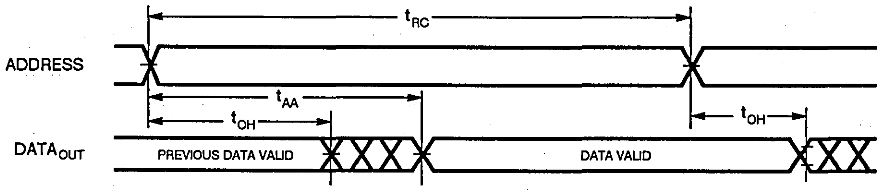
NOTES:
1. V_{CC} = 5V, T_A = +25°C
2. V_{IL} min. = -3.5V for pulse width less than 30ns.
3. I_{SB_2} max. of IDT7M137 at commercial temperature = 150mA.

AC ELECTRICAL CHARACTERISTICS

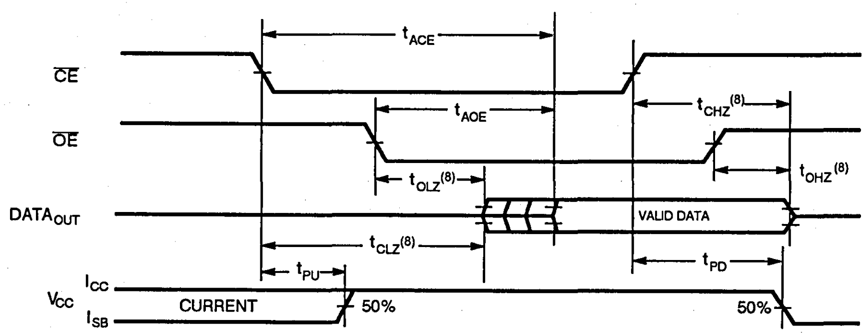
(V_{CC} = 5V ±10%, T_A = –55°C to +125°C and 0°C to 70°C)

SYMBOL	PARAMETER	IDT7M137S55 (COM'L. ONLY) MIN.	MAX.	IDT7M137S60 MIN.	MAX.	IDT7M137S70 MIN.	MAX.	IDT7M137S90 MIN.	MAX.	IDT7M137S100 (MIL. ONLY) MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	55	–	60	–	70	–	90	–	100	–	ns
t_{AA}	Address Access Time	–	55	–	60	–	70	–	90	–	100	ns
t_{ACE}	Chip Enable Access Time	–	55	–	60	–	70	–	90	–	100	ns
t_{AOE}	Output Enable Access Time	–	35	–	35	–	40	–	40	–	40	ns
t_{OH}	Output Hold From Address Change	0	–	0	–	0	–	10	–	10	–	ns
t_{CLZ}	Chip Select to Output in Low Z	15	–	15	–	15	–	5	–	5	–	ns
t_{CHZ}	Chip Select to Output in High Z	–	35	–	40	–	40	–	40	–	40	ns
t_{OLZ}	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{OHZ}	Output Enable to Output in High Z	–	30	–	35	–	40	–	40	–	40	ns
t_{PU}	Chip Enable to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time	–	60	–	60	–	60	–	60	–	60	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	55	–	60	–	70	–	90	–	100	–	ns
t_{EW}	Chip Enable to End of Write	50	–	55	–	60	–	80	–	90	–	ns
t_{AW}	Address Valid to End of Write	50	–	55	–	60	–	80	–	90	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	10	–	10	–	ns
t_{WP}	Write Pulse Width	45	–	50	–	55	–	70	–	80	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	10	–	10	–	ns
t_{DW}	Data Valid to End of Write	25	–	30	–	35	–	45	–	50	–	ns
t_{DH}	Data Hold Time	5	–	5	–	5	–	10	–	10	–	ns
t_{OHZ}	Output Enable to Output in High Z	–	35	–	40	–	40	–	40	–	50	ns
t_{WZ}	Write Enabled to Output in High Z	0	35	0	40	0	40	0	40	0	50	ns
t_{OW}	Output Active From End of Write	0	–	0	–	0	–	0	–	0	–	ns

TIMING WAVEFORM OF READ CYCLE NO. 1 EITHER SIDE (1, 2, 6)

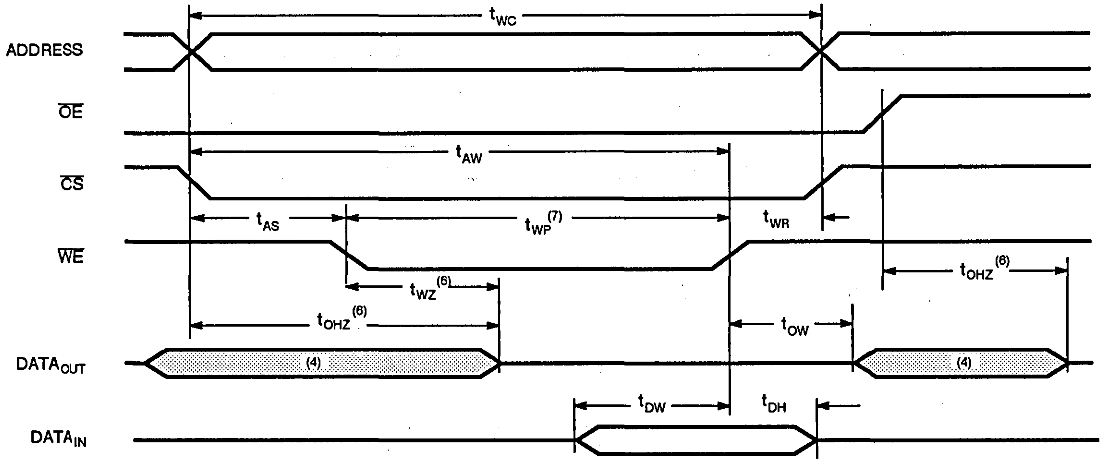


TIMING WAVEFORM OF READ CYCLE NO. 2 EITHER SIDE (1, 3)

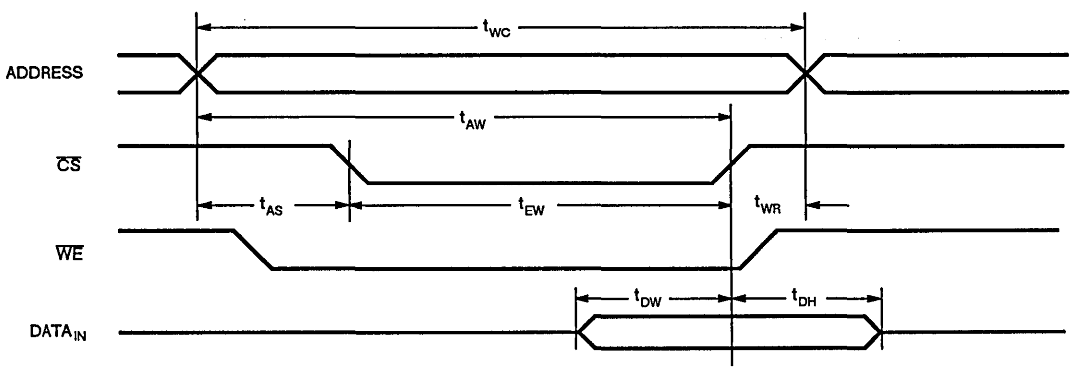


13

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{OUT}	Output Capacitance	V_{IN} = 0V	120	pF
C_{IN}	Input Capacitance	V_{OUT} = 0V	50	pF

NOTE:
1. This parameter is sampled and not 100% tested.

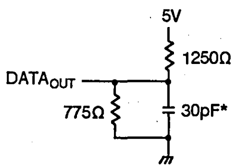


Figure 1.
Output Load

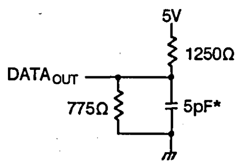


Figure 2.
Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

* Including scope and jig.

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (−55°C to +125°C) Semiconductor components compliant to MIL-STD-883, Class B
Package	C	Sidebraze
Speed	55	Commercial Only (Speed in Nanoseconds)
	60	
	70	
	90	
	100	Military Only (Speed in Nanoseconds)
Power	S	Standard Power
Device Type	7M137	32K x 8-Bit

13

Integrated Device Technology, Inc.

CMOS SLAVE DUAL-PORT RAM MODULE 64K (8K x 8-BIT) & 128K (16K x 8-BIT)

IDT7M144S
IDT7M145S

FEATURES:

- High-density 64K/128K-bit CMOS SLAVE dual-port RAM modules
- Easily expands data bus width to 16-or-more-bits when used with MASTER IDT7M134 or IDT7M135
- 16K x 8 organization (IDT7M145) or 8K x 8 option (IDT7M144)
- High-speed access
  - Military: 60ns (max.)
  - Commercial: 45ns (max.)
- Low power operation
  - Active: 950mW (typ.) (IDT7M144)
  - Standby: 20mW (typ.) (IDT7M144)
- $\overline{BUSY}$ input flags
- Fully asynchronous operation from either port
- Fully static operation
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Single 5V(±10%) power supply
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M144/145 are 64K/128K-bit high-speed CEMOS™ SLAVE dual-port static RAM modules constructed on a multi-layered, co-fired, ceramic substrate using four IDT7142 2K x 8 SLAVE dual-port RAMs (IDT7M144) or eight IDT7142 SLAVE dual-port RAMs (IDT7M145) in leadless chip carriers. Dual-port function is achieved by utilization of the two on-board IDT54/74FCT138 decoder circuits that interpret the higher order addresses A_{L11-13} and A_{R11-13} to select one of the eight 2K x 8 dual-port RAMs. (On IDT7M144 8K x 8 option, the A_{L13} and A_{R13} need to be externally grounded and the selection becomes one of the four 2K x 8 dual-port RAMs.)

The IDT7M144/145 are designed as "SLAVE" dual-port RAM modules to be used together with the IDT7M135/135 "MASTER" dual-port RAM modules in 16-or-more-bit systems, whereas the IDT7M134/135 are designed to be used as stand-alone 8-bit dual-port RAM modules. Using the IDT MASTER/SLAVE dual-port RAM module approach in 16-or-more-bit memory system applications results in full speed operation without the need for additional discrete logic.

Both SLAVE IDT7M144/145 and MASTER IDT7M134/135 modules provide two ports with separate control, address and I/O pins that permit independent asynchronous access for reads or writes to any location in the memory. The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. The delayed port will have access when $\overline{BUSY}$ goes high (inactive). The $\overline{BUSY}$ pins are outputs on the MASTER and inputs on the SLAVE.

PIN CONFIGURATION

Left signal	Pin	Pin	Right signal
GND(1)	1	58	V_{CC}(1)
$\overline{CE}_L$	2	57	$\overline{CE}_R$
$R/\overline{W}_L$	3	56	$R/\overline{W}_R$
NC	4	55	NC
$\overline{BUSY}_L$(3)	5	54	$\overline{BUSY}_R$(3)
$\overline{OE}_L$	6	53	$\overline{OE}_R$
A_{0L}	7	52	A_{0R}
A_{1L}	8	51	A_{1R}
A_{2L}	9	50	A_{2R}
A_{3L}	10	49	A_{3R}
A_{4L}	11	48	A_{4R}
A_{5L}	12	47	A_{5R}
A_{6L}	13	46	A_{6R}
A_{7L}	14	45	A_{7R}
A_{8L}	15	44	A_{8R}
A_{9L}	16	43	A_{9R}
A_{10L}	17	42	A_{10R}
A_{11L}	18	41	A_{11R}
A_{12L}	19	40	A_{12R}
A_{13L}(2)	20	39	A_{13R}(2)
I/O_{0L}	21	38	I/O_{0R}
I/O_{1L}	22	37	I/O_{1R}
I/O_{2L}	23	36	I/O_{2R}
I/O_{3L}	24	35	I/O_{3R}
I/O_{4L}	25	34	I/O_{4R}
I/O_{5L}	26	33	I/O_{5R}
I/O_{6L}	27	32	I/O_{6R}
I/O_{7L}	28	31	I/O_{7R}
GND(1)	29	30	V_{CC}(1)

M7(4)

DIP
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
A_{0L}-A_{13L}	A_{0R}-A_{13R}	Address
I/O_{0L}-I/O_{7L}	I/O_{0R}-I/O_{7R}	Data Input/Output
V_{CC}		Power
GND		Ground

NOTES:

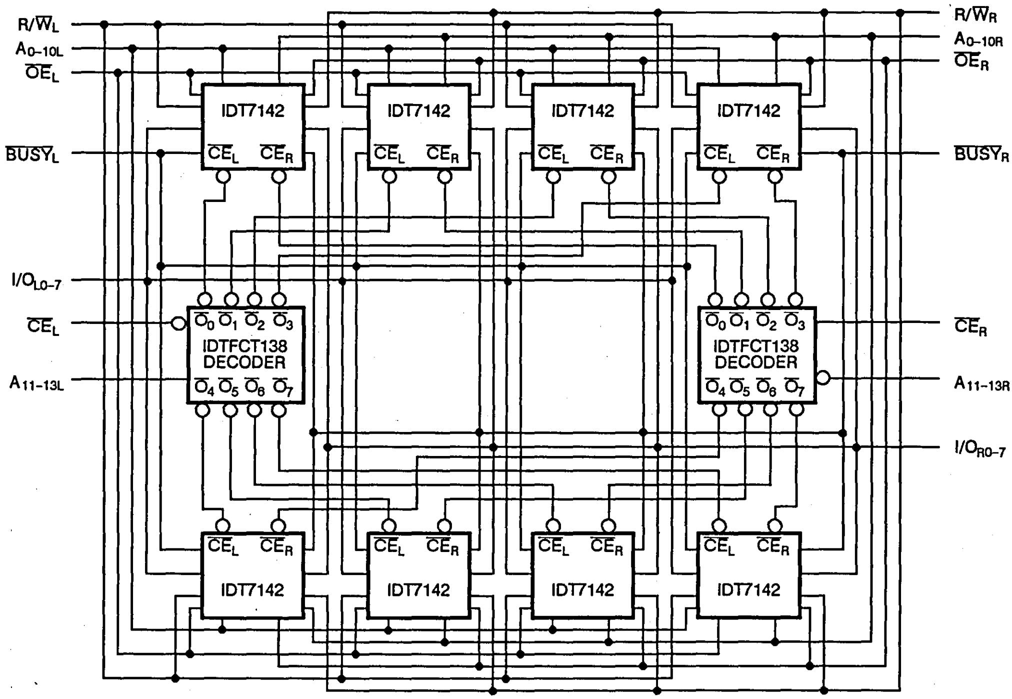
1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. On 8K x 8 IDT7M134 option, A_{13L} and A_{13R} need to be externally connected to ground for proper operation.
3. IDT7M134/135 (MASTER): $\overline{BUSY}$ is open drain output and requires pull up resistor. IDT7M144/145 (SLAVE): $\overline{BUSY}$ is input.
4. For module dimensions, please refer to module drawing M7 in the packaging section.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

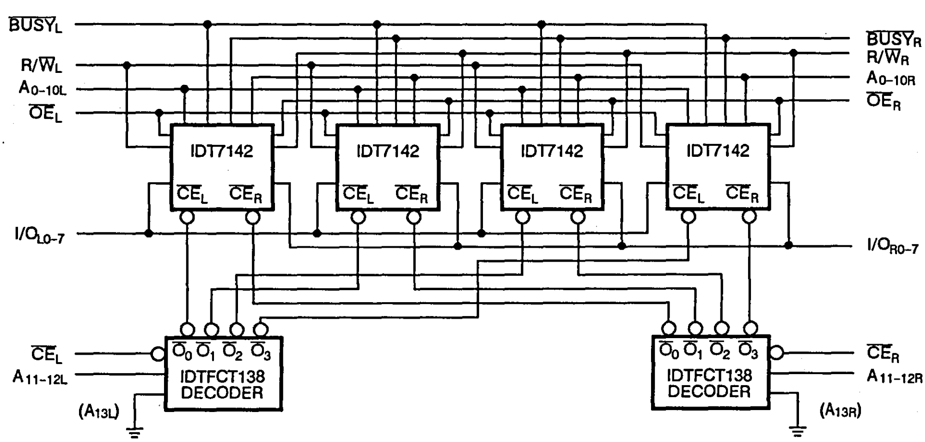
DSC-7025/-

FUNCTIONAL BLOCK DIAGRAMS

(A) IDT7M145 (16K x 8-BIT)



(B) IDT7M144 (8K x 8-BIT)



(GROUND A_{13L} AND A_{13R} EXTERNALLY)

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

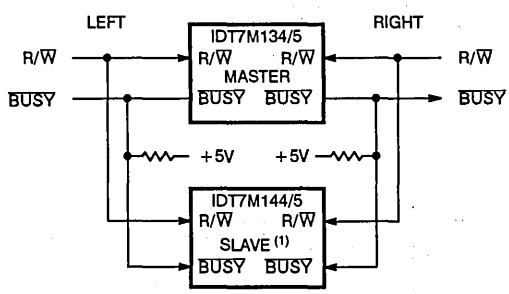
(DC electricals for the IDT7M144/IDT7M145 SLAVE dual-port are identical to the IDT7M134/IDT7M135 MASTER dual-port. Reference the IDT7M134/IDT7M135 CMOS dual-port RAM data sheet.)

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

(AC electricals for the IDT7M144/IDT7M145 SLAVE dual-port are identical to the IDT7M134/IDT7M135 MASTER dual-port *except* where noted below.)

SYMBOL	PARAMETER	7M144S45 7M145S45 (COM'L. ONLY)		7M144S50 7M145S50 (COM'L. ONLY)		7M144S60 7M145S60		7M144S70 7M145S70		7M144S90 7M145S90		7M144S100 7M145S100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WP}	Write Pulse Width	35	–	40	–	45	–	45	–	50	–	60	–	ns
t_{WB}	Write to $\overline{BUSY}$	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WH}	Write Hold After $\overline{BUSY}$	20	–	20	–	20	–	20	–	20	–	20	–	ns

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEM



NOTE:
1. No arbitration in IDT7M144/IDT7M145 (SLAVE): $\overline{BUSY}$ IN inhibits write in IDT7M144/IDT7M145.

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (–55°C to +125°C) Semiconductor Components Compliant to MIL-STD-883, Class B
Speed	45	Commercial Only — Speed in Nanoseconds
	50	Commercial Only — Speed in Nanoseconds
	60	Speed in Nanoseconds
	70	Speed in Nanoseconds
	90	Speed in Nanoseconds
	100	Speed in Nanoseconds
Power	S	Standard Power
Device Type	7M144	64K (8K x 8-bit) SLAVE Dual-Port RAM
	7M145	128K (16K x 8-bit) SLAVE Dual-Port RAM

13

Integrated Device Technology, Inc.

CMOS PARALLEL IN-OUT FIFO MODULE 2K x 9-BIT & 4K x 9-BIT

IDT7M203S
IDT7M204S

FEATURES:

- First-In, First-Out memory module
- 2K x 9 organization (IDT7M203S)
- 4K x 9 organization (IDT7M204S)
- Low-power consumption
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Single 5V (±10%) power supply
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- High-performance CEMOS™ technology
- Pin compatible with IDT7201 and Mostek MK4501, but with four times word depth (IDT7M203S) or eight times (IDT7M204S)
- Module available with semiconductor components 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M203/204 are FIFO memory modules that utilize a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

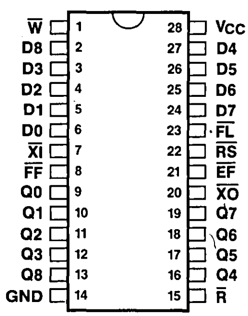
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 65ns (15MHz) for commercial and 70ns (14MHz) for military temperature ranges.

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

The IDT7M203/204 are constructed on a multi-layered ceramic substrate using four IDT7201 (512x9) or four IDT7202 (1Kx9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7201s and IDT7202s fabricated in IDT's high-performance CEMOS technology.

IDT's military FIFO modules have semiconductor components 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

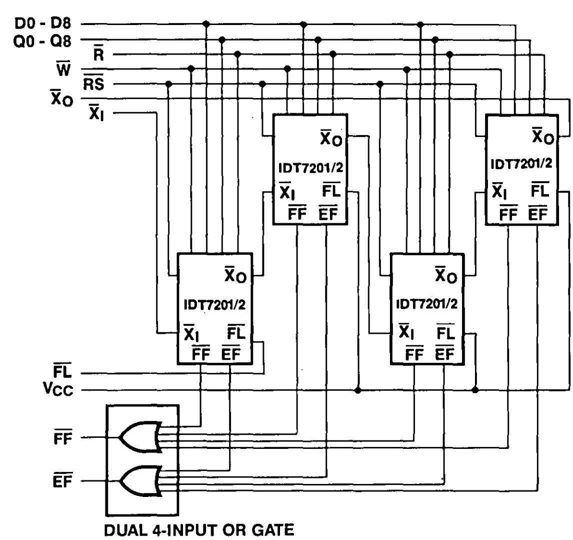


DIP
TOP VIEW

PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = DATA IN	$\overline{XO}$ = EXPANSION OUT	V_{CC} = 5V
$\overline{RS}$ = RESET	Q = DATA OUT	$\overline{FF}$ = FULL FLAG	GND = GROUND

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **JULY 1986**

ABSOLUTE MAXIMUM RATING[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8K x 9 50 TP
7205 L
SKINNY DIP
$.46 @ 1K
DAVID 492 8554

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}[1]	Input Low Voltage Commercial & Military	—	—	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	IDT7M203S IDT7M204S COMMERCIAL MIN.	TYP.	MAX.	IDT7M203S IDT7M204S MILITARY MIN.	TYP.	MAX.	UNIT	NOTES
I_{IL}	Input Leakage Current (Any Input)	-5	—	5	-10	—	10	μA	1
I_{OL}	Output Leakage Current	-10	—	10	-10	—	10	μA	2
V_{OH}	Output Logic "1" Voltage I_H = -2mA	2.4	—	—	2.4	—	—	V	—
V_{OL}	Output Logic "0" Voltage I_L = 8mA	—	—	0.4	—	—	0.4	V	—
I_{CC1}	Average V_{CC} Power Supply Current	—	110	176	—	155	230	mA	3
I_{CC2}	Average Standby Current ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL} = V_{IH}$)	—	20	33	—	30	60	mA	3
I_{CC3}	Power Down Current (All Input = V_{CC} -0.2V)	—	—	20	—	—	36	mA	3

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
3. I_{CC} measurements are made with outputs open.

CAPACITANCE (T_A = +25° C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

AC CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C and 0°C to +70°C)

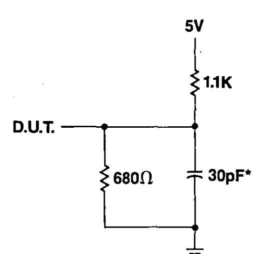
SYMBOL	PARAMETER	7M203/4S40 COM'L. ONLY MIN.	MAX.	7M203/4S50 MIN.	MAX.	7M203/4S55 MIN.	MAX.	7M203/4S65 MIN.	MAX.	7M203/4S100 MIN.	MAX.	7M203/4S140 MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	50	—	65	—	70	—	85	—	125	—	165	—	ns
t_A	Access Time	—	40	—	50	—	55	—	65	—	100	—	140	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	20	—	25	—	25	—	ns
t_{RPW}	Read Pulse Width[2]	40	—	50	—	55	—	65	—	100	—	140	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	5	—	10	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3,4]	10	—	15	—	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	25	—	30	—	30	—	35	—	40	—	50	ns
t_{WC}	Write Cycle Time	50	—	65	—	70	—	85	—	125	—	165	—	ns
t_{WPW}	Write Pulse Width[2]	40	—	50	—	55	—	65	—	100	—	140	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	20	—	25	—	25	—	ns
t_{DS}	Data Setup Time	20	—	25	—	30	—	40	—	50	—	50	—	ns
t_{DH}	Data Hold Time	0	—	5	—	10	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	70	—	85	—	125	—	165	—	ns
t_{RS}	Reset Pulse Width[2]	40	—	50	—	55	—	65	—	100	—	140	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	20	—	25	—	25	—	ns
t_{EFL}	Reset to Empty Flag Low	—	45	—	65	—	70	—	85	—	125	—	165	ns
t_{REF}	Read Low to Empty Flag Low	—	45	—	50	—	55	—	60	—	95	—	135	ns
t_{RFF}	Read High to Full Flag High	—	45	—	50	—	55	—	60	—	95	—	135	ns
t_{WEF}	Write High to Empty Flag High	—	45	—	50	—	55	—	60	—	95	—	135	ns
t_{WFF}	Write Low to Full Flag Low	—	45	—	50	—	55	—	60	—	95	—	135	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

NOTE:
Generating $\overline{R}/\overline{W}$ Signals — When using these high-speed FIFO devices, it is necessary to have clean inputs on the $\overline{R}$ and $\overline{W}$ signals. It is important to not have glitches, spikes or ringing on the $\overline{R}$, $\overline{W}$ lines (violates the V_{IH}, V_{IL} requirements); although the minimum pulse width low for the $\overline{R}$ and $\overline{W}$ are specified in tens of nanosecond, a glitch of 5ns can affect the read or write pointer and cause it to increment.



*Includes jig and scope capacitances.

Figure 1. Output Load.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D0-D8)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2: i.e., t_{RPW} or t_{WPW} before the rising edge of $\overline{RS}$, and $\overline{W}$ should not change until t_{RSR} after the rising edge of $\overline{RS}$.

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data setup and hold times must be adhered to with respect to the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a First-In, First-Out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the data outputs (Q0 through Q8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF}, and a valid READ can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$; so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD ($\overline{FL}$)

This pin is grounded to indicate that it is the first device. In the multiple mode (depth expansion mode) application, this pin on the rest of the devices should connect to V_{CC} for proper operation.

EXPANSION IN ($\overline{XI}$)

EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous (in depth expansion) or same device for proper application.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

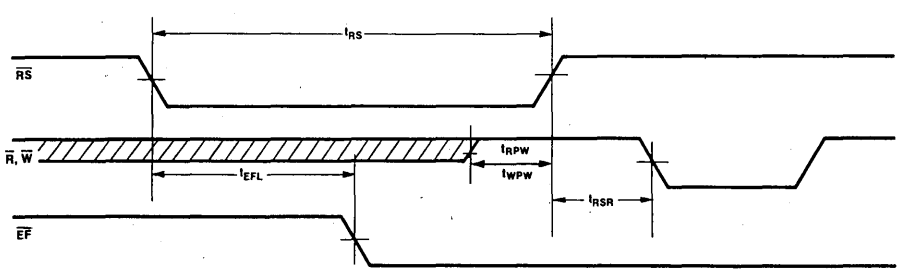
The FULL FLAT ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indiciating that the device is full. If the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 2048 writes for the IDT7M203 and 4096 writes for the IDT7M204.

EXPANSION OUT ($\overline{XO}$)

EXPANSION OUT ($\overline{XO}$) is connected to the EXPANSION IN ($\overline{XI}$) of the same device (single device mode) or the EXPANSION IN ($\overline{XI}$) of the next device (multiple device, depth expanion mode) for proper operation. This output acts as a signal to the next device by providing a pulse to the next device when the current device reaches the last location of memory.

DATA OUTPUTS (Q0-Q8)

Data outputs for 9-bit wide data. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.



NOTES:

1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. $\overline{W}$ and $\overline{R} = V_{IH}$ around the rising edge of $\overline{RS}$.

Figure 2. Reset

13

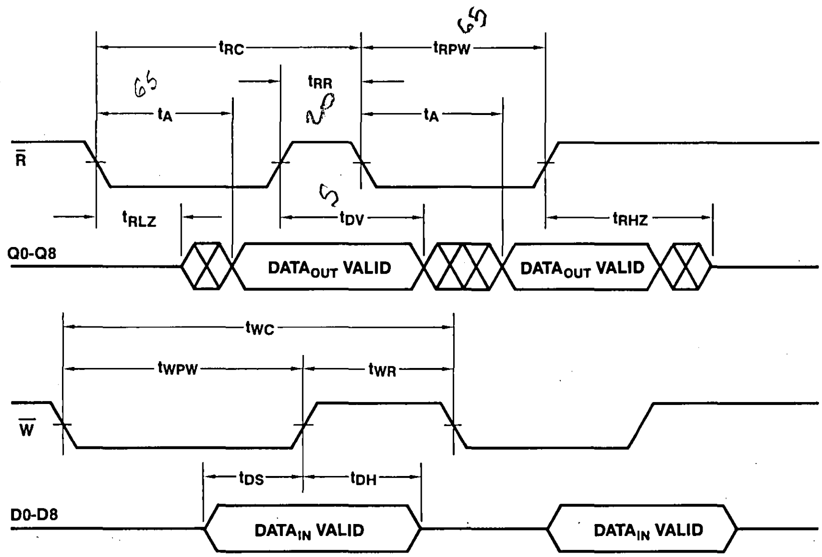


Figure 3. Asynchronous Write and Read Operation

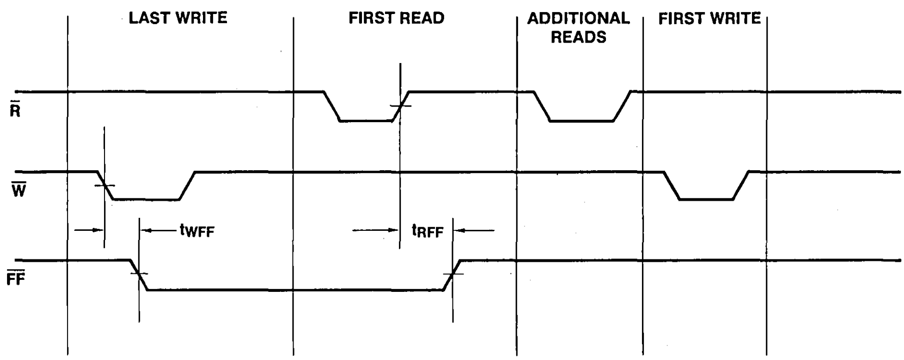


Figure 4. Full Flag From Last Write to First Read

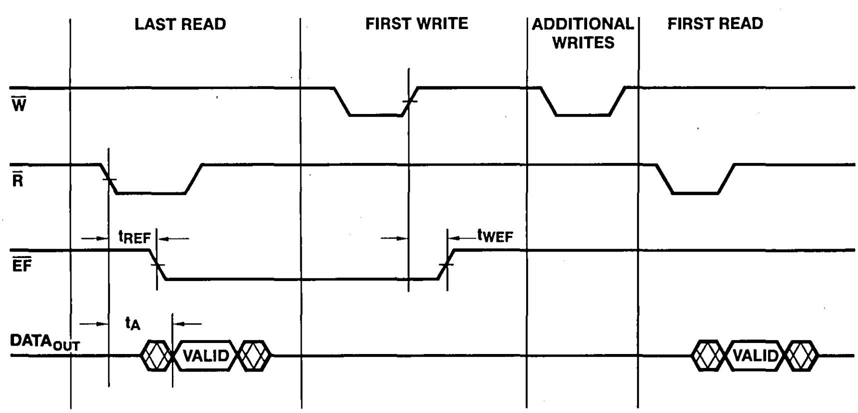
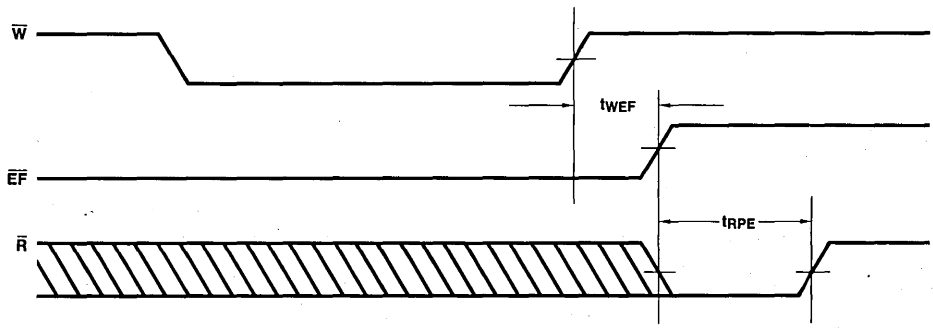


Figure 5. Empty Flag From Last Read to First Write

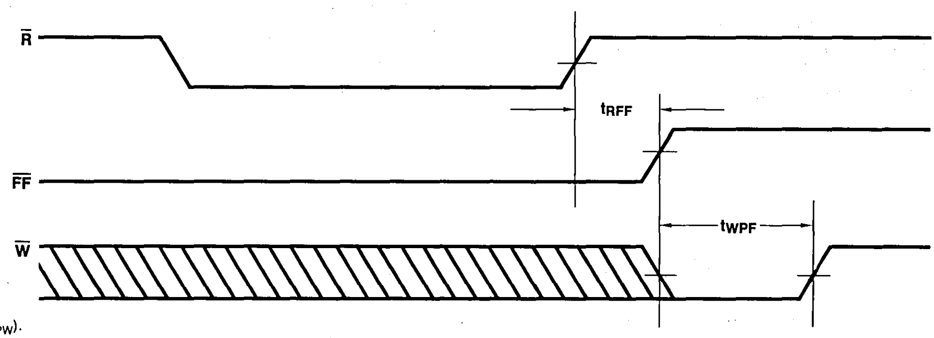
t_{RPE}: EFFECTIVE READ PULSE WIDTH AFTER EMPTY FLAG HIGH



NOTE:
1. ($t_{RPE} = t_{RPW}$)

Figure 6. Empty Flag Timing

t_{WPF}: EFFECTIVE WRITE PULSE WIDTH AFTER FULL FLAG HIGH



NOTE:
1. ($t_{WPF} = t_{WPW}$).

Figure 7. Full Flag Timing

OPERATING MODES: SINGLE DEVICE MODE

A single IDT7M203/IDT7M204 may be used when the application requirements are for 2048/4096 words or less. The IDT7M203/IDT7M204 is a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is connected to the EXPANSION OUT ($\overline{XO}$) of the device and the FIRST LOAD ($\overline{FL}$) control pin is grounded (see Figure 8).

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$) can be detected from any one device. Figure 9 demonstrates an 18-bit word width by using two IDT7M203/ IDT7M204s. Any word width can be attained by adding additional IDT7M203/IDT7M204s.

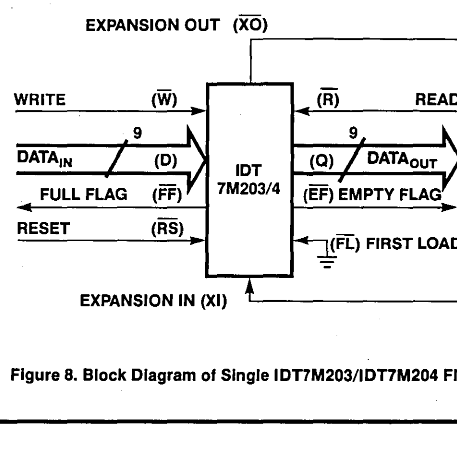


Figure 8. Block Diagram of Single IDT7M203/IDT7M204 FIFO

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7M203/IDT7M204 can easily be adapted to applications when the requirements are for greater than 2048/4096 words. Figure 10 demonstrates Depth Expansion using three IDT7M203/IDT7M204s. Any depth can be attained by adding additional IDT7M203/IDT7M204s. The IDT7M203/IDT7M204 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. See Figure 10.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 10.

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays. (See Figure 11.)

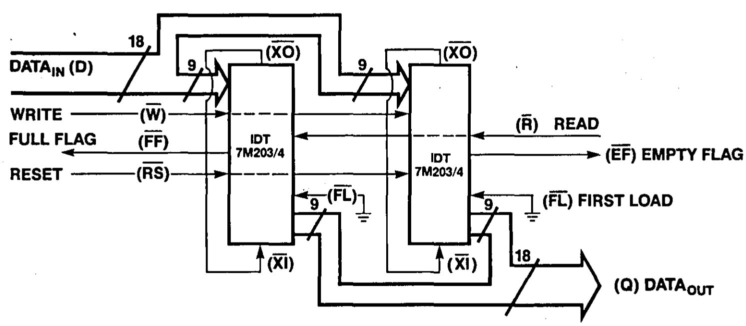
BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7M203/IDT7M204s as is shown in Figure 12. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted with the IDT7M203/IDT7M204: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 13), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in (t_{WEF} + t_A)ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ}ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge would deassert the empty flag); however, the same word (written on the first edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In a write flow-through mode (Figure 14), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted, but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, a new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and increment the write pointer.



NOTES:
Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 9. Block Diagram of 2048x18/4096x18 FIFO Memory Used In Width Expansion Mode

TABLE I — RESET — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUT	INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset	0	Location Zero	Location Zero	0	1
Read/Write	1	Increment(1)	Increment(1)	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II — RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 10.

$\overline{RS}$ = Reset Input, $\overline{FL}$ = First Load, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

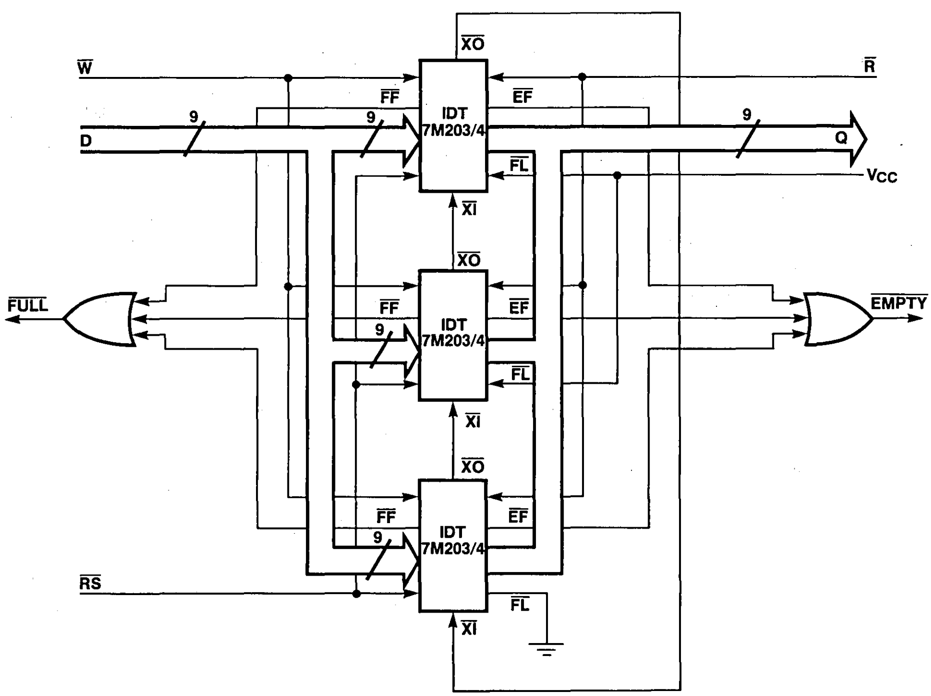
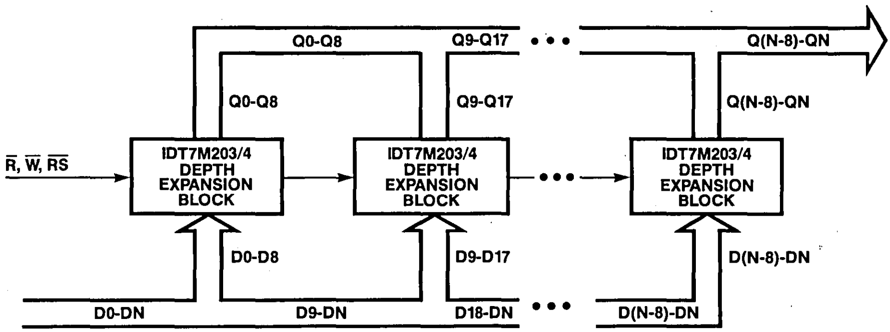


Figure 10. Block Diagram of 6144x9/12288x9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For flag detection see WIDTH expansion Section and Figure 9.

Figure 11. Compound FIFO Expansion

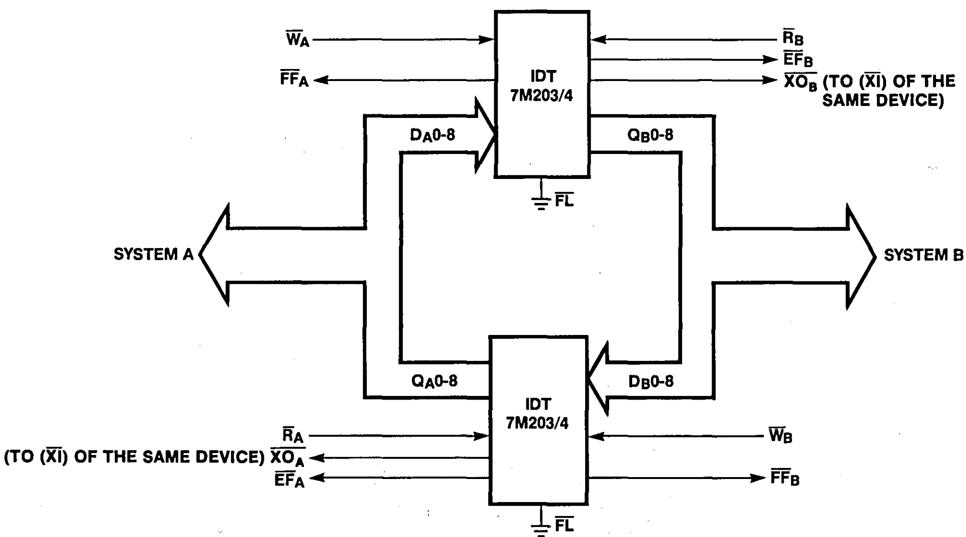
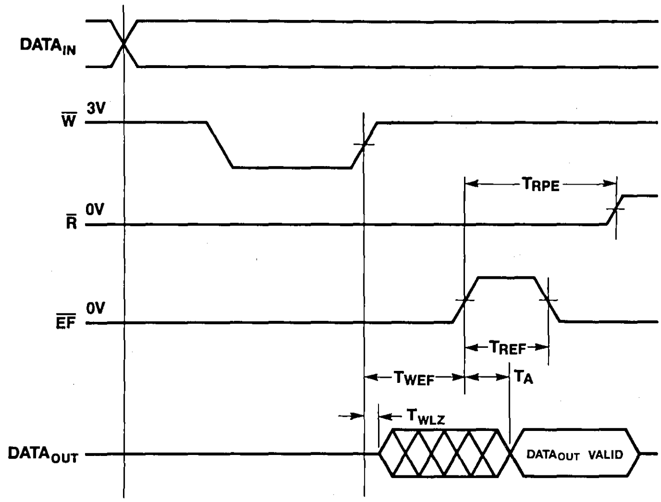
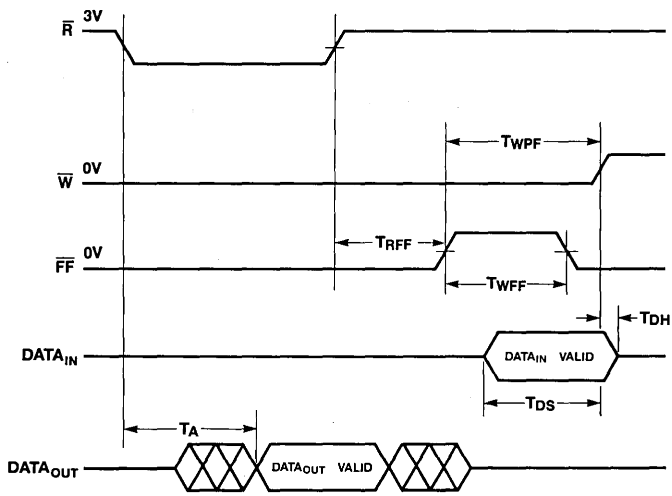


Figure 12. Bidirectional FIFO Mode



NOTE:
($T_{RPE} = T_{RPW}$)

Figure 13. Read Data Flow-Through Mode



NOTE:
($T_{WPF} = T_{WPW}$)

Figure 14. Write Data Flow-Through Mode

13

ORDERING INFORMATION

IDT	XXXX	Power	Speed	A	A
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range	Blank	Commercial (0°C to +70°C)	
	B	Military (-55°C to +125°C) Semiconductor Components Screened to MIL-STD-883, Method 5004, Class B	
Package	C	Sidebraze	
Speed	40	Commercial Only	Speed in Nanoseconds
	50		
	55		
	65		
	100		
	140		
Power	S	Standard-Power	
Device Type	7M203	2K x 9-Bit	
	7M204	4K x 9-Bit	

CMOS PARALLEL IN-OUT FIFO MODULE 8K x 9-BIT & 16K x 9-BIT

IDT7M205S
IDT7M206S

Integrated Device Technology, Inc.

FEATURES:

- First-In/First-Out memory module
- 8K x 9 organization (IDT7M205S)
- 16K x 9 organization (IDT7M206S)
- Low power consumption
  - Active: 840mW (typ. Com'l.)
  - Power Down: 176mW (max. Com'l)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Single 5V (±10%) power supply
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning flags
- High-performance CEMOS™ technology
- Pin-compatible with IDT7201 and Mostek MK4501, but with 16 times word depth (IDT7M205S) or 32 times (IDT7M206S)
- Module available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

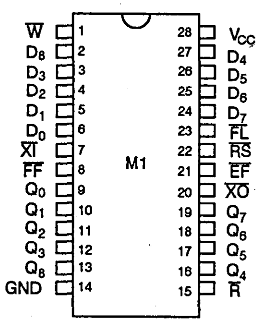
The IDT7M205S/206S are FIFO memory modules constructed on a multi-layered ceramic substrate using four IDT7203 (2K x 9) or four IDT7204 (4K x 9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7203s and IDT7204s fabricated in IDT's high-performance CEMOS technology. These devices utilize a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The devices have a read/write cycle time of 50ns (25MHz) for commercial and 65ns (15MHz) for military temperature ranges.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

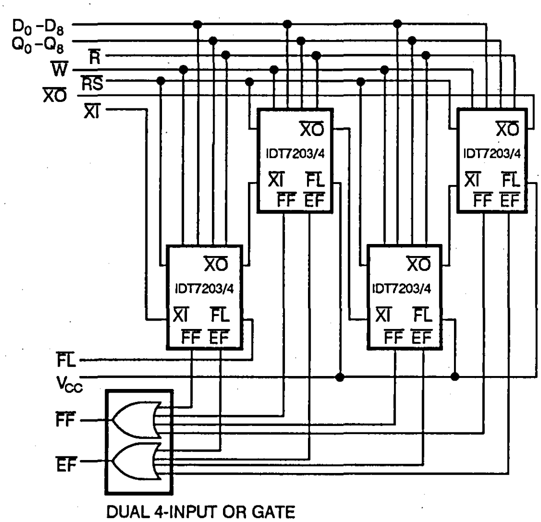
IDT's Military FIFO modules have semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = $DATA_{IN}$	$\overline{XO}$ = EXPANSION OUT	V_{CC} = 5V
$\overline{RS}$ = RESET	Q = $DATA_{OUT}$	$\overline{FF}$ = FULL FLAG	GND = GROUND

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH} [1]	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL} [1]	Input Low Voltage Commercial & Military	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7M205S IDT7M206S COMMERCIAL MIN.	TYP.	MAX.	IDT7M205S IDT7M206S MILITARY MIN.	TYP.	MAX.	UNIT
I_{IL} [1]	Input Leakage Current (Any Input)	-5	–	5	-10	–	10	µA
I_{OL} [2]	Output Leakage Current	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA	–	–	0.4	–	–	0.4	V
I_{CC1} [3]	Average V_{CC} Power Supply Current	–	168	264	–	224	350	mA
I_{CC2} [3]	Average Standby Current ($\overline{R} = \overline{W} = \overline{RST} = \overline{FL}/\overline{RT} = V_{IH}$)	–	32	48	–	48	100	mA
I_{CC3} [3]	Power Down Current (All Input = V_{CC} = -0.2V)	–	–	32	–	–	48	mA

NOTES:
1. Measurements with $0.4 \le V_{IN} \le V_{OUT}$.
2. $R \ge V_{IH}$, $0.4 \le V_{OUT} \le V_{CC}$
3. I_{CC} measurements are made with outputs open.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	40	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	60	pF

NOTE:
1. This parameter is sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS [1]

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = –55°C to +125°C)

SYMBOL	PARAMETER	7M205S40 7M206S40 (COM'L ONLY)		7M205S50 7M206S50		7M205S60 7M206S60		7M205S70 7M206S70		7M205S85 7M206S85		7M205S120 7M206S120		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	50	–	65	–	75	–	85	–	105	–	140	–	ns
t_A	Access Time	–	40	–	50	–	60	–	70	–	85	–	120	ns
t_{RR}	Read Recovery Time	10	–	15	–	15	–	15	–	20	–	20	–	ns
t_{RPW} [2]	Read Pulse Width	40	–	50	–	60	–	70	–	85	–	120	–	ns
t_{RLZ} [3]	Read Pulse Low to Data Bus at Low Z	5	–	10	–	10	–	10	–	10	–	10	–	ns
t_{WLZ} [3]	Write Pulse High to Data Bus at Low Z	10	–	15	–	15	–	15	–	20	–	20	–	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ} [3]	Read Pulse High to Data Bus at High Z	–	25	–	30	–	30	–	30	–	30	–	35	ns
t_{WC}	Write Cycle Time	50	–	65	–	75	–	85	–	105	–	140	–	ns
t_{WPW} [2]	Write Pulse Width	40	–	50	–	60	–	70	–	85	–	120	–	ns
t_{WR}	Write Recovery Time	10	–	15	–	15	–	15	–	20	–	20	–	ns
t_{DS}	Data Set-up Time	20	–	30	–	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	0	–	5	–	5	–	10	–	10	–	10	–	ns
t_{RSC}	Reset Cycle Time	50	–	65	–	75	–	85	–	105	–	140	–	ns
t_{RS} [2]	Reset Pulse Width	40	–	50	–	60	–	70	–	85	–	120	–	ns
t_{RSR}	Reset Recovery Time	10	–	15	–	15	–	15	–	20	–	20	–	ns
t_{EFL}	Reset to Empty Flag Low	–	50	–	65	–	75	–	85	–	105	–	140	ns
t_{REF}	Read Low to Empty Flag Low	–	40	–	50	–	60	–	70	–	85	–	120	ns
t_{RFF}	Read High to Full Flag High	–	40	–	50	–	60	–	70	–	85	–	120	ns
t_{WEF}	Write High to Empty Flag High	–	40	–	50	–	60	–	70	–	85	–	120	ns
t_{WFF}	Write Low to Full Flag Low	–	40	–	50	–	60	–	70	–	85	–	120	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

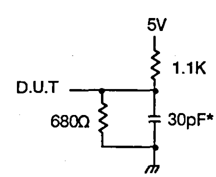


Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0 - D_8)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During RESET, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during reset.

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a first-in/first-out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the Data Outputs (Q_0 through Q_8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF} and a valid READ can then begin.

FIRST LOAD ($\overline{FL}$)

This pin is grounded to indicate that it is the first device. In the multiple module (depth expansion mode) application, this pin on the rest of devices should connect to V_{CC} for proper operation.

EXPANSION IN ($\overline{XI}$)

EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous (in depth expansion) or same device for proper application.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

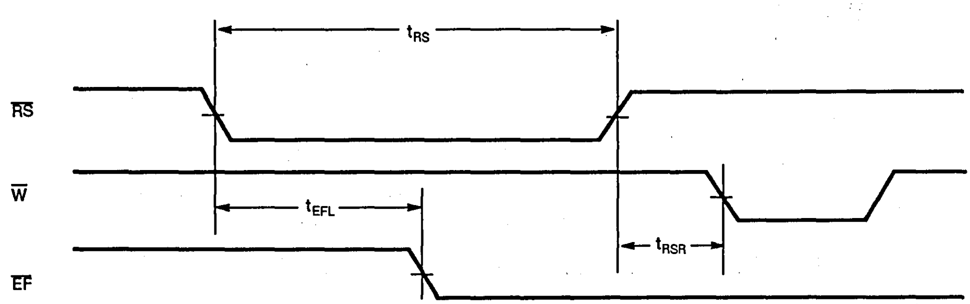
The FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 8,192 writes for the IDT7M205 and 16,384 writes for the IDT7M206.

EXPANSION OUT ($\overline{XO}$)

EXPANSION OUT ($\overline{XO}$) is connected to the EXPANSION IN ($\overline{XI}$) of the same device (single device mode) or the EXPANSION IN ($\overline{XI}$) of the next device (multiple device, depth expansion mode) for proper operation. This output acts as a signal to the next device by providing a pulse to the next device when the current device reaches the last location of memory.

DATA OUTPUTS (Q_0 - Q_8)

Data outputs for 9-bit wide data. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.



NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

Figure 2. RESET (1, 2)

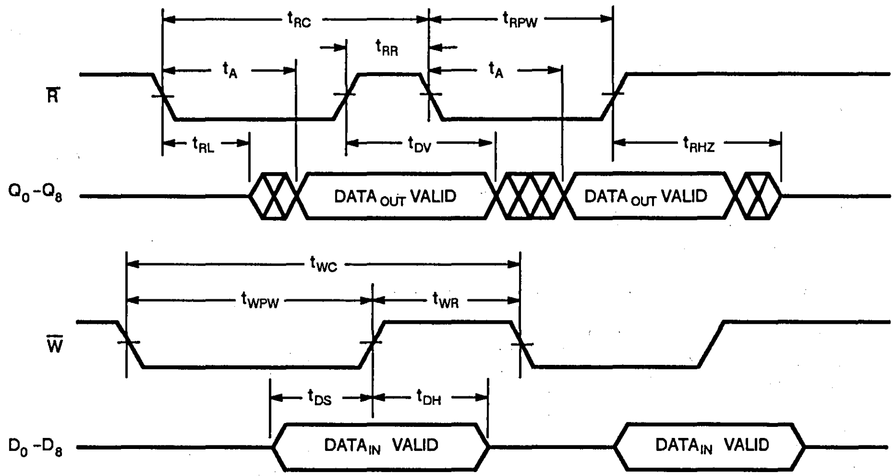


Figure 3. Asynchronous Write and Read Operation

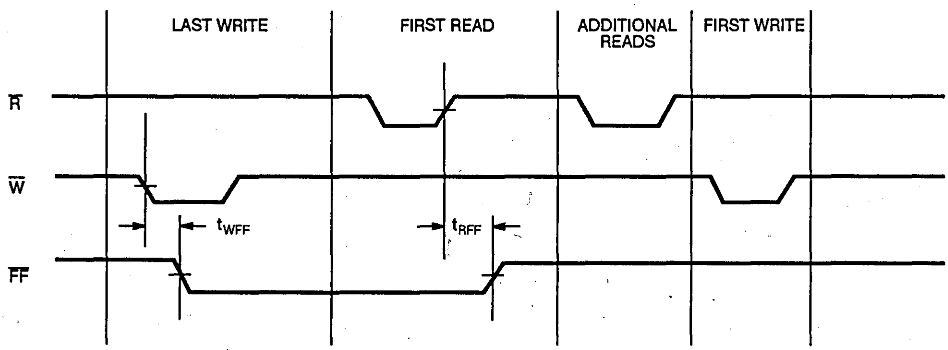


Figure 4. Full Flag From Last Write to First Read

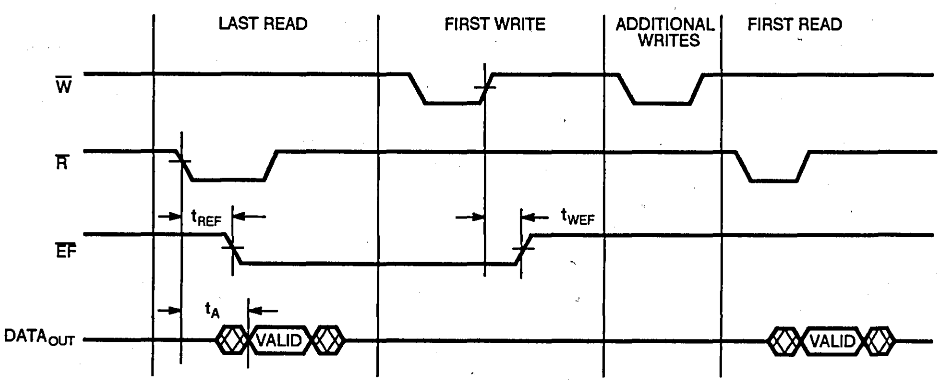
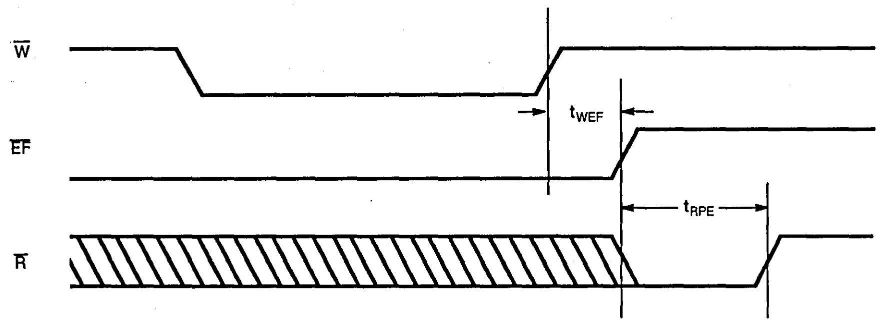


Figure 5. Empty Flag From Last Read to First Write

13

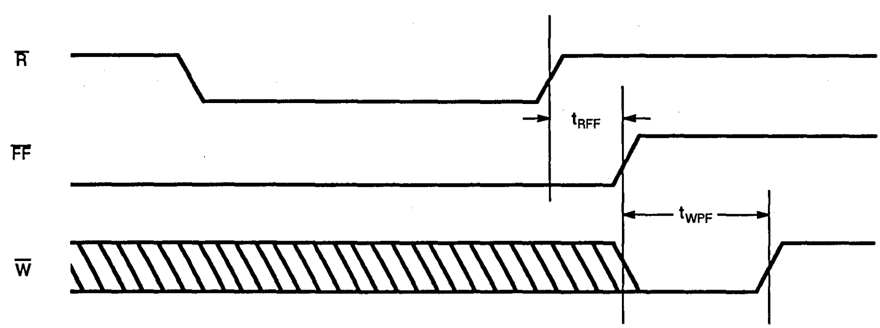
t_{RPE} :EFFECTIVE READ PULSE WIDTH AFTER FULL FLAG HIGH [1]



NOTE:
1. ($t_{RPE} = t_{RPW}$)

Figure 6. Empty Flag Timing

t_{RPE} EFFECTIVE READ PULSE WIDTH AFTER FULL FLAG HIGH [1]



NOTE:
1. ($t_{WPF} = t_{WPW}$)

Figure 7. Full Flag Timing

OPERATING MODES: SINGLE DEVICE MODE

A single IDT7M205/206 may be used when the application requirements are for 8,192/16,384 words or less. The IDT7M205/206 is in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is connected to the EXPANSION OUT ($\overline{XO}$) of the device and the FIRST LOAD ($\overline{FL}$) control pin is grounded (see Figure 8).

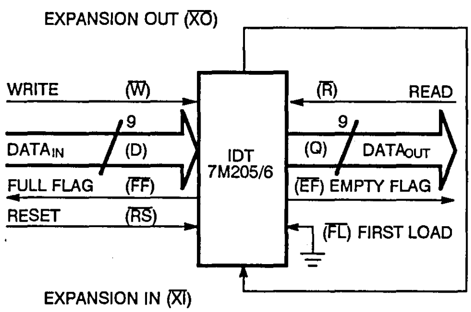


Figure 8. Block Diagram of Single IDT7M205206 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 9 demonstrates an 18-bit word width by using two IDT7M205/206s. Any word width can be attained by adding additional IDT7M205/206s.

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7M205/206 can easily be adapted to applications when the requirements are for greater than 8,192/16,384 words. Figure 10 demonstrates Depth Expansion using three IDT7M205/206. Any depth can be attained by adding additional IDT7M205/206s. The IDT7M205/206 operate in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. (See Figure 10.)
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the logical ANDing of all $\overline{EF}$s and logical ANDing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). (See Figure 10.)

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays. (See Figure 11.)

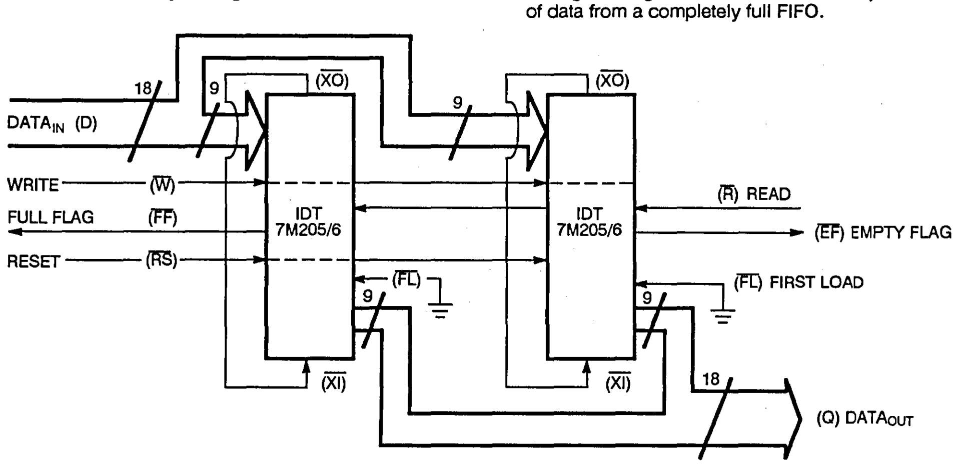
BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7M205/206s as shown in Figure 12. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted with the IDT7M205/206: a read flow-through mode and write flow-through mode. For the read flow-through mode (Figure 13), the FIFO permits a reading of a single word of data immediately after writing one word of data into the completely empty FIFO.

In the write flow-through mode (Figure 14), the FIFO permits a writing of a single word of data immediately after reading one word of data from a completely full FIFO.



NOTE:

Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 9. Block Diagram of 8,192 x 18/16,384 x 18 FIFO Memory Used In Width Expansion Mode

TRUTH TABLES

TABLE I – RESET – SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS		INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset	0	0	Location Zero	Location Zero	0	1
Read/Write	1	0	Increment(1)	Increment(1)	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II – RESET AND FIRST LOAD TRUTH TABLE – DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 10.
2. $\overline{RS}$ = Reset Input $\overline{FL}$ = First Load, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

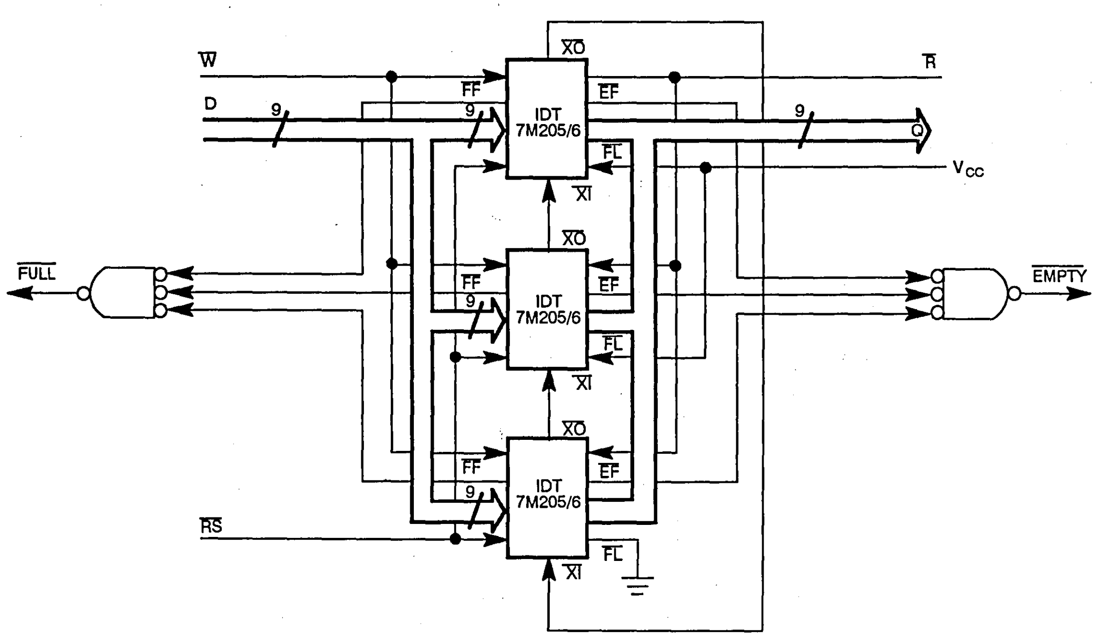
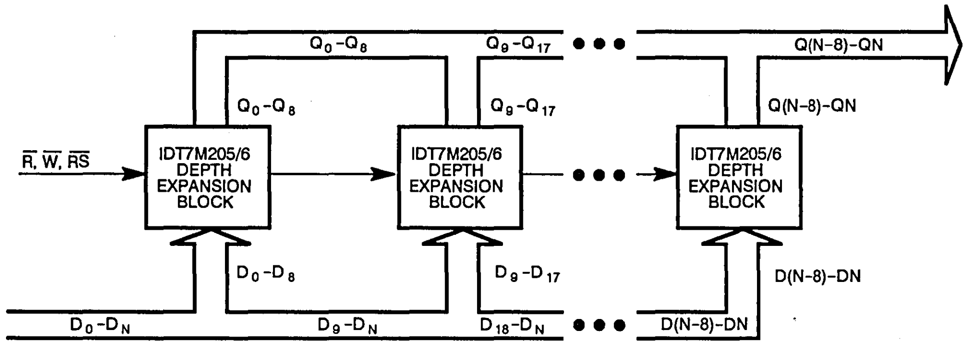


Figure 10. Block Diagram of 24,576 x 9/49,152 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag detection see WIDTH EXPANSION Section and Figure 9.

Figure 11. Compound FIFO Expansion

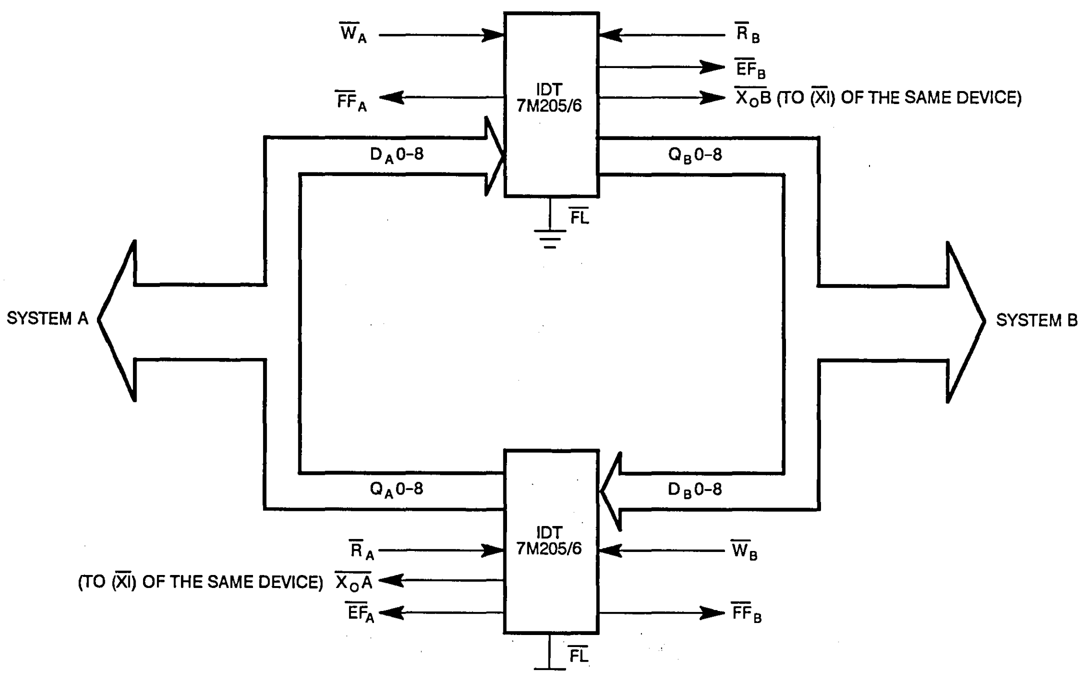
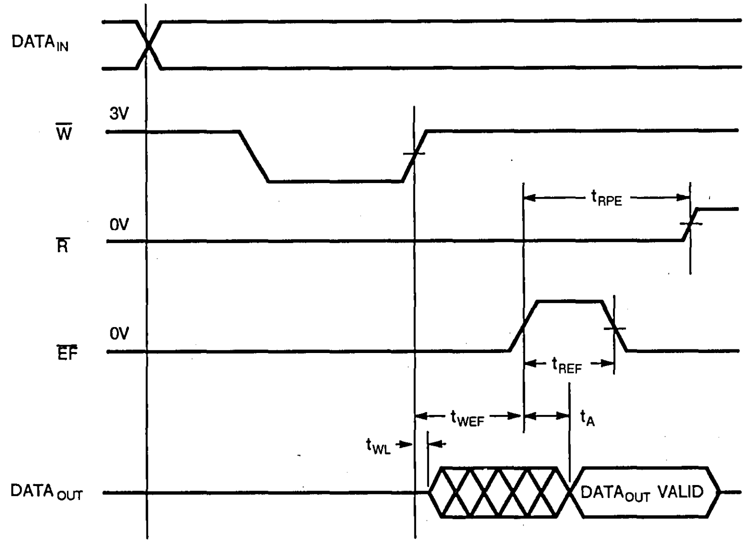


Figure 12. Bidirectional FIFO Mode

13



NOTE:
1. $t_{RPE} = t_{RPW}$

Figure 13. Read Data Flow-Through Mode

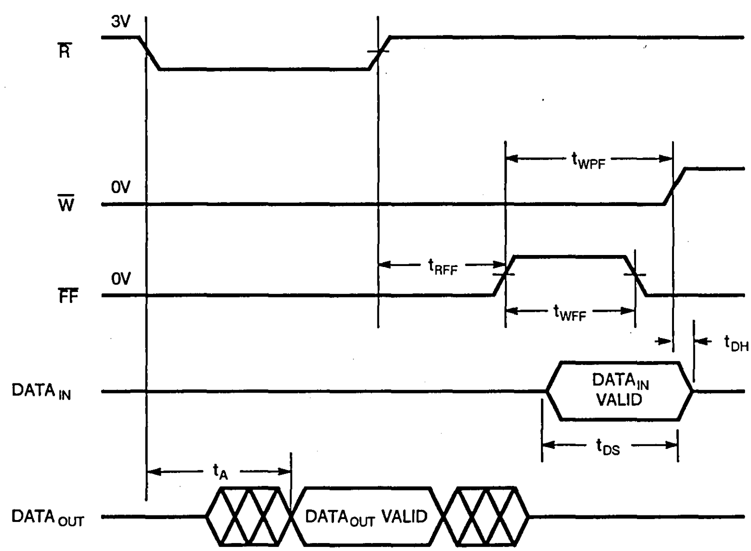


Figure 14. Write Data Flow-Through Mode

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military -55°C to +125°C Compliant to MIL-STD-883, Class B
Package	C	Sidebraze DIP
Speed	40 50 60 70 85 120	Speed in Nanoseconds
Power	S	Standard Power
Device Type	7M205 7M206	8K x 9-Bit 16K x 9-Bit

13

1 MEGABIT (128K x 8) REGISTERED/BUFFERED/ LATCHED CMOS STATIC RAM SUBSYSTEMS

IDT7M824 FAMILY

Integrated Device Technology, Inc.

FEATURES:

- High-density 1024K-bit (128K x 8-bit) CMOS static RAM modules with registered/buffered/latched addresses and I/Os
- High-speed registered access time:
  - Military temperature range: 60ns (max.)
  - Commercial temperature range: 50ns (max.)
- 20MHz read cycle time
- Low power consumption (typ.)
  - Active: 1.5W
  - Standby: 75mW
- Low input capacitance (typ.): input 20pF; output 25pF
- High output drive (min.): I_{OL} = 48mW; I_{OH} = -15mA
- Available in 64-pin, 900 mil centre sidebraze DIP (with LCCs on both sides), achieving very high memory density
- Module select output
- Separate inputs and outputs
- Clear data and clock enables on all registers
- Address, input and outputs on separate clocks or latch enables
- Registered write enable
- Internal bypass capacitors for minimizing power supply noise
- TTL-compatible; single 5V (±10%) power supply
- Five GND pins for maximum noise immunity, five V_{CC} pins
- Military grade module available with semiconductor components compliant to the latest revision of MIL-STD-883, Class B

DESCRIPTION:

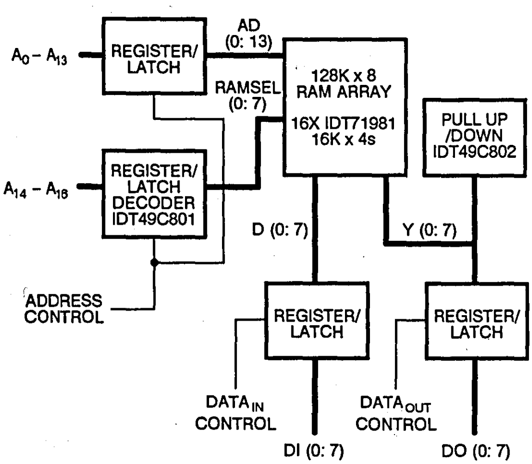
The IDT7M824 family is a set of 1024K-bit (128K x 8-bit) high-speed CMOS static RAM modules with registered/buffered/ latched addresses and I/Os. They are constructed on co-fired, multi-layered ceramic substrates with sidebrazed leads using 16 IDT71981 (16K x 4) static RAMs, IDT logic devices and decoupling capacitors. Devices in leadless chip carriers are mounted top and bottom for maximum density.

Extremely high speeds are achievable by the use of IDT71981s and logic devices fabricated in IDT's high-performance, high-reliability CEMOS ™ technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest circuits possible. The IDT7M824 has registered access times of 50ns (max.) over the commercial temperature range and can be operated with cycle times as fast as 20MHz.

Designing with this device can be very flexible because of such features as module select output and clock enables on all registers, registered write enable and 8-bit separate inputs and outputs. Because of the proprietary IDT49C801, the modules are cascadable in terms of depth with no additional external decoding. The write enable can be turned off when the module is deselected. Immunity to noise has been extended with such features as 8-bit separate inputs and outputs; addresses, inputs, and outputs on separate clocks; internal decoupling capacitors; five ground pins and five V_{CC} pins.

The semiconductor components used on all IDT military modules are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT SELECTOR GUIDE

PART NO.	I/O AND ADDRESS FEATURES		
	ADDRESS BUS	INPUT DATA BUS	OUTPUT DATA BUS
IDT7M820	L/B	L/B	L/B
IDT7M821	L/B	R	R
IDT7M822	L/B	R	L/B
IDT7M823	L/B	L/B	R
IDT7M825	R	R	R
IDT7M826	R	R	L/B
IDT7M827	R	L/B	R
IDT7M828	R	L/B	L/B

NOTES:
1. L/B = LATCHED/BUFFERED
   R = REGISTERED
2. For module dimensions, please refer to module drawing M8 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN NAMES

NAME	DESCRIPTION
$A_0 - A_{16}$	Addresses
$DI_0 - DI_7$	Data input
$DO_0 - DO_7$	Data output
$\overline{CLRDIN}$	Data input clear
CPDIN/LEDIN	Data input register clock/latch enable
$\overline{ENDIN/PREDIN}$	Data input register clock enable/latch preset
$\overline{OE}_1, \overline{OE}_2, \overline{OE}_3$	Output enable
CPDOUT/LEDOUT	Data output register clock/latch enable
$\overline{ENDOUT/PREDOUT}$	Data output register clock enable/latch preset
$\overline{CS}_1, \overline{CS}_2$, & CS_3	Chip select
$\overline{WE}$	Write enable
$\overline{SEL}$	Select output
LE/CP	Latch enable/clock pulse control input
$\overline{CE}$/GND	Clock enable/ground
REG/$\overline{LAT}$	Register/latch (low active) input control
V_{CC}	Power
GND	Ground

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	25	pF

NOTE:

1. This parameter is sampled and not 100% tested.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	–	0.4	
			I_{OL} = 48mA COM'L.	–	–	0.5	
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open f = 0		–	300	600	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}		–	320	650	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} V_{CC} = Max. Output Open, f = f_{MAX}		–	15	330	mA

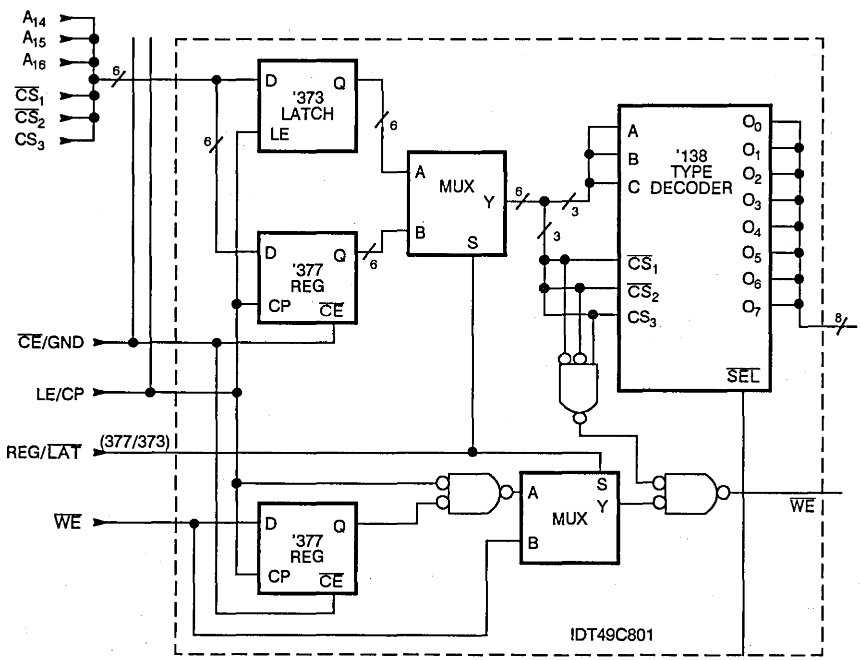
NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

IDT49C801

REGISTERED/LATCHED DECODER

The IDT49C801 is a proprietary IDT gate array that includes a 138-type 1-of-8 decoder, as well as latches and registers for all inputs and controls for WRITE ENABLE ($\overline{WE}$). The latch or register mode is controlled by a single input, REG/$\overline{LAT}$.

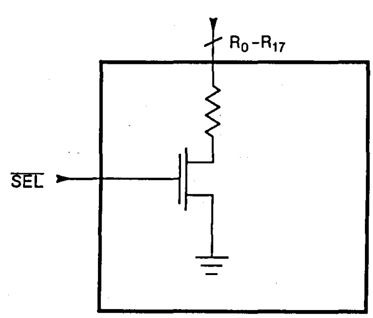
With the IDT49C801 in the Latch mode, the three address and the three chip select inputs are latched by a 373-type latch. When LE is high, the latch is transparent and, when LE goes low, all data that meets the required set-up time is latched. The $\overline{WE}$ input is not latched but it is gated by the result of the three chip select inputs. With the IDT49C801 in the Register mode, the three address and chip select inputs are registered by a 377-type register. All data that meets the set-up time requirements before the rising edge of CP will be transferred to the output of the register provided Clock Enable ($\overline{CE}$) is asserted. In this mode, $\overline{WE}$ is also registered but the output of its register is gated with CP so that when CP goes low, the output of $\overline{WE}$ is applied to the RAMs.



IDT49C802

UNIVERSAL PULL-UP/DOWN RESISTORS

The IDT49C802 is a proprietary gate array that has 18 selectable pull-up or pull-down resistors, only eight of which are used on these parts. The purpose of the pull-down resistor, as used in these parts, is to prevent the RAM DO pins from floating when the RAM array is deselected. When the RAM array is selected, the pull-down resistor is inhibited. The value of the resistors is approximately 15KΩ.



13

Integrated Device Technology, Inc.

128K x 8 SRAM WITH LATCHED/ BUFFERED ADDRESS LINES AND LATCHED/BUFFERED DATA LINES

IDT7M820

FEATURES:

- Latched and buffered address lines
- Latched and buffered input data lines
- Latched and buffered output data lines
- Separate I/O
- High-speed access time:
  - Military temperature range: 55ns (max.)
  - Commercial temperature range: 45ns (max.)
- 20MHz read/write cycle time

DESCRIPTION:

The IDT7M820 is a 128K x 8 RAM with latched address, latched $DATA_{IN}$ and latched $DATA_{OUT}$ lines. Each of the three buses has its own Latch Enable (LE), allowing the latch to be used as a buffer by connecting the appropriate LE to V_{CC}.

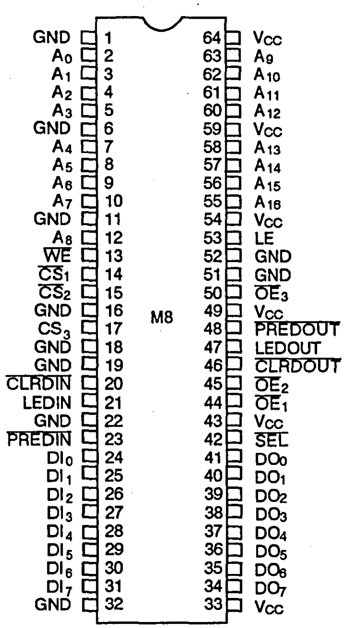
Address, Write Enable and the three chip select lines are controlled by LE. When LE is high, the address latches and decoder are transparent, or in the buffer mode. All address, Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) data that meets the specified set-up time will be latched when LE goes low.

$DATA_{IN}$ is controlled by its own enable, LEDIN. With this line in the high state, the latch is in the transparent or buffer mode. All $DATA_{IN}$ that meets the specified set-up time will be latched when LEDIN goes low. $\overline{PREDIN}$ and $\overline{CLRDIN}$ are asynchronous controls that can be used to preset or clear the $DATA_{IN}$ latch. The preset function overrides the clear so that, with both asserted, the latch will be preset.

$DATA_{OUT}$ is controlled by its own enable, LEDOUT. With this line in the high state, the latch is in the transparent or buffer mode. $DATA_{OUT}$ of the RAM array that meets the set-up time requirements will be latched when LEDOUT goes low. $\overline{PREDOUT}$ and $\overline{CLRDOUT}$ are asynchronous controls that can be used to preset or clear the $DATA_{OUT}$ latch. The preset function overrides the clear so that, with both asserted, the latch will be preset. There are three active low output enables for $DATA_{OUT}$. Unless all three of these lines are asserted, the output will be in the high impedance state.

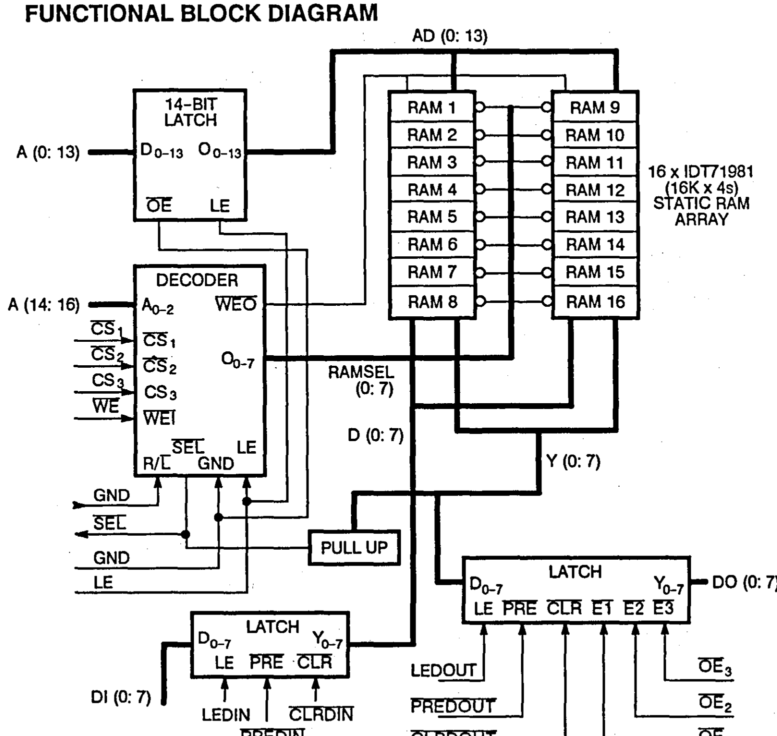
The $\overline{SEL}$ signal is an output that can be used to monitor the state of the internal RAM array output bus.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

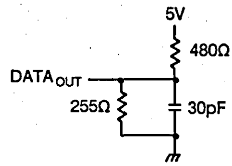


Figure 1. Output Load

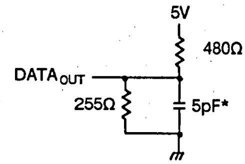


Figure 2. Output Load (for t_{OHZ})

* Including scope and jig.

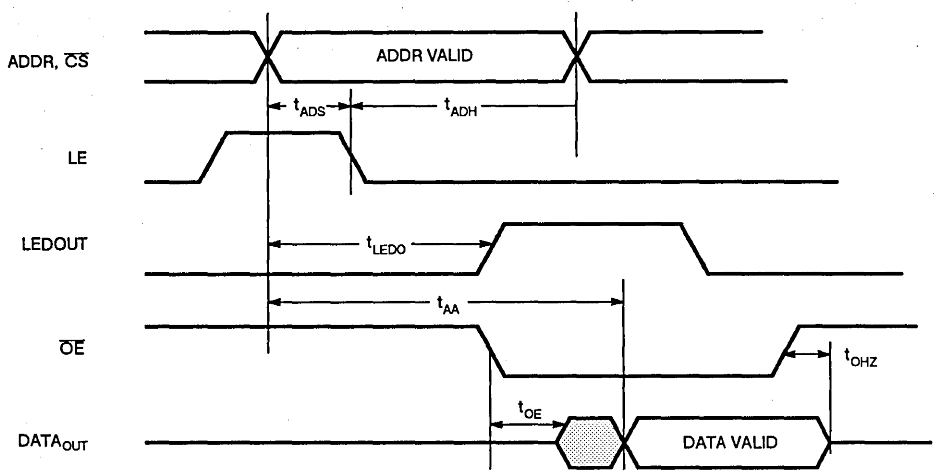
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, T_A = 0°C to +70°C and -55°C to +125°C)

SYMBOL	PARAMETER	IDT7M820S45 (COM'L ONLY) MIN.	IDT7M820S45 (COM'L ONLY) MAX.	IDT7M820S55 MIN.	IDT7M820S55 MAX.	IDT7M820S70 MIN.	IDT7M820S70 MAX.	UNIT
READ CYCLE								
t_{AA}	Address, $\overline{CS}$ Access Time	–	45	–	55	–	70	ns
t_{ADS}	Address, $\overline{CS}$ to LE Set-up Time	2	–	2	–	2	–	ns
t_{ADH}	Address, $\overline{CS}$ from LE Hold Time	2	–	2	–	3	–	ns
t_{LEDO}(2)	$DATA_{OUT}$ Latch Enable from Address, $\overline{CS}$	–	36	–	40	–	55	ns
t_{OE}	$\overline{OE}$ to Data Valid	–	8	–	9	–	15	ns
t_{OHZ}(3)	$\overline{OE}$ to High Z	–	7	–	9	–	15	ns
WRITE CYCLE								
t_{AW}	Address, $\overline{CS}$ to End of Write	31	–	41	–	55	–	ns
t_{WP}	Write Pulse Width	27	–	37	–	50	–	ns
t_{ADS}	Address, $\overline{CS}$ to LE Set-up Time	2	–	2	–	2	–	ns
t_{ADH}	Address, $\overline{CS}$ from LE Hold Time	2	–	2	–	3	–	ns
t_{DW}	Data Valid to End of Write	26	–	36	–	50	–	ns

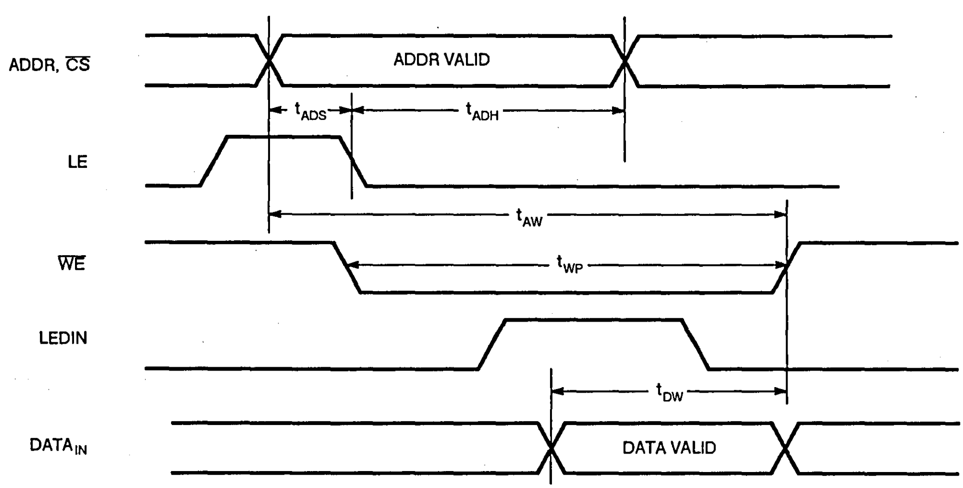
NOTES:
1. $\overline{WE}$ Must be high for read cycles.
2. Latch Enable signal arriving after this maximum will delay overall access time (t_{AA})
3. Transition is measured -200mV from steady state voltage with specified loading in Figure 2.

13

TIMING WAVEFORM OF READ CYCLE



TIMING WAVEFORM OF WRITE CYCLE



128K x 8 SRAM WITH LATCHED/ BUFFERED ADDRESS LINES AND REGISTERED DATA LINES

IDT7M821

Integrated Device Technology, Inc.

FEATURES:

- Latched/buffered address lines
- Registered input data lines
- Registered output data lines
- Separate I/O
- High-speed access time:
  - Military temperature range: 55ns (max.)
  - Commercial temperature range: 45ns (max.)
- 20MHz read/write cycle time

DESCRIPTION:

The IDT7M821 is a 128K x 8 RAM with latched address, registered $DATA_{IN}$ and registered $DATA_{OUT}$ lines. The address latch can be used as a buffer by connecting its Latch Enable LE to V_{CC}.

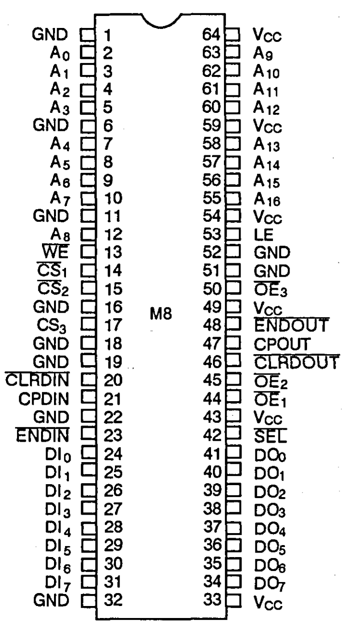
Address, Write Enable ($\overline{WE}$) and the three Chip Select ($\overline{CS}$) lines are controlled by LE. When LE is high, the address latches and decoder are transparent or in the buffer mode. All address, $\overline{CS}$ and $\overline{WE}$ data that meets the specified set-up time will be latched when LE goes low.

$DATA_{IN}$ is controlled by its own clock, CPDIN. When ENDIN (clock enable) is asserted, all $DATA_{IN}$ data that meets the specified set-up time will be registered on the rising edge of CPDIN. $\overline{CLRDIN}$ is an asynchronous control that can be used to clear the $DATA_{IN}$ register.

$DATA_{OUT}$ is controlled by its own enable, CPDOUT. When ENDOUT (clock enable) is asserted, all data out of the RAM array that meets the set-up time requirements will be registered on the rising edge of CPDOUT. $\overline{CLRDOUT}$ is an asynchronous control that can be used to clear the $DATA_{OUT}$ register. There are three active low output enables for $DATA_{OUT}$. Unless all three of these lines are asserted, the output will be in the high impedance state.

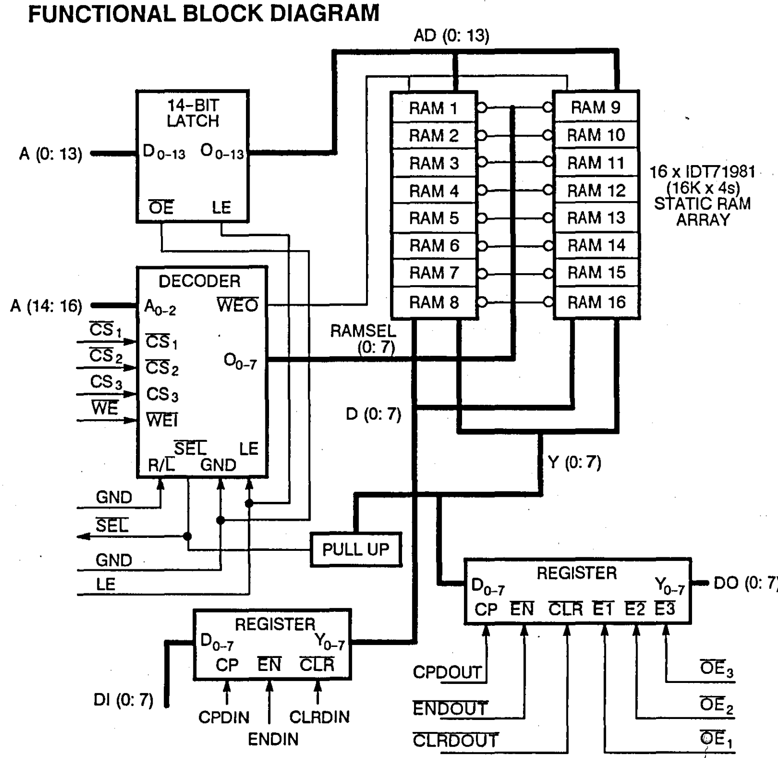
The $\overline{SEL}$ signal is an output that can be used to monitor the state of the internal RAM array output bus.

PIN CONFIGURATION



DIP TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

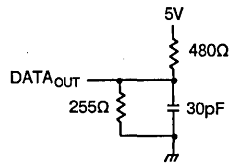


Figure 1. Output Load

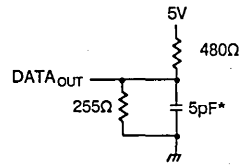


Figure 2. Output Load (for t_{OHZ})

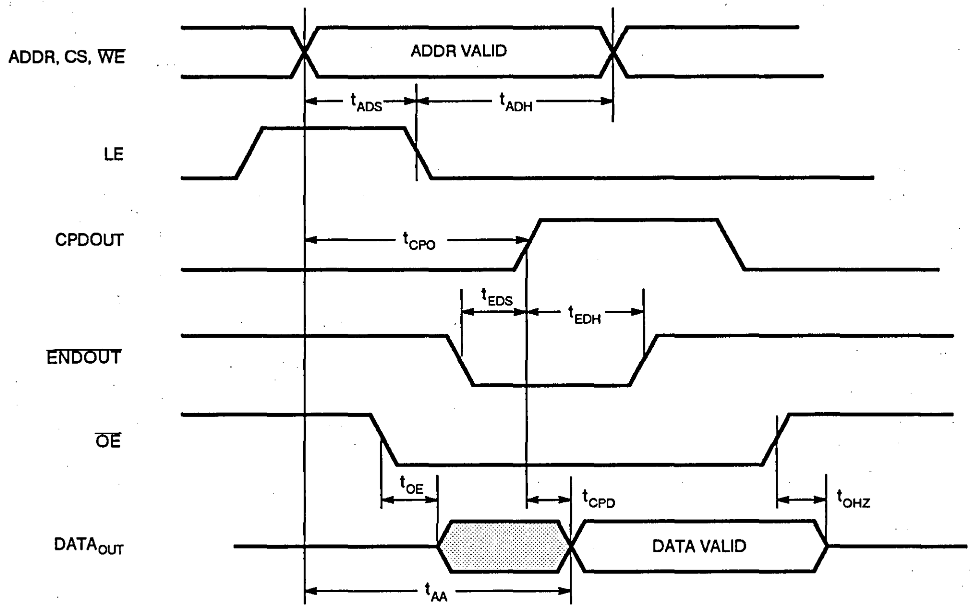
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, T_A = 0°C to +70°C and -55°C to +125°C)

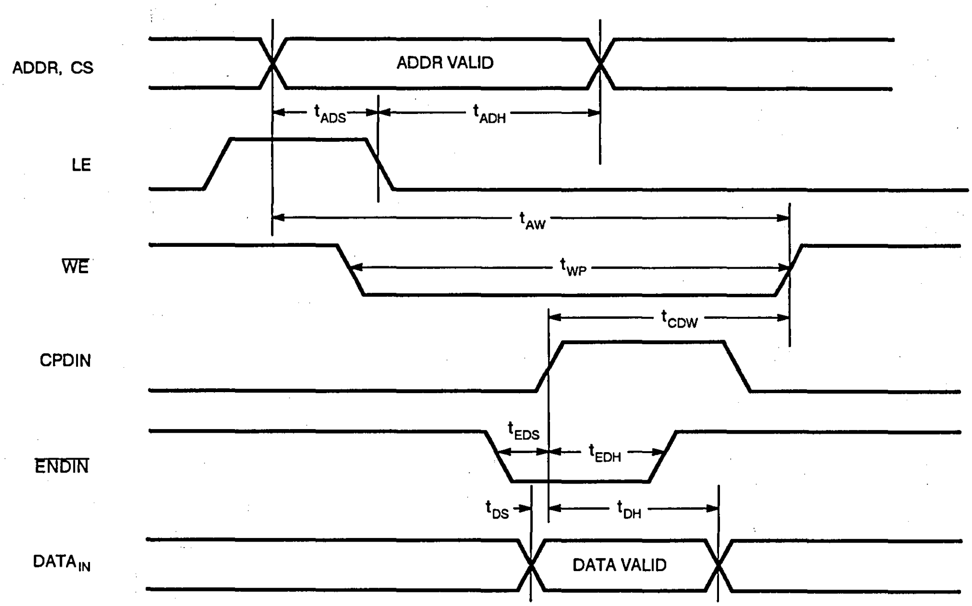
SYMBOL	PARAMETER	IDT7M821S45 (COM'L. ONLY)		IDT7M821S55		IDT7M821S70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE[1]								
t_{AA}	Address, $\overline{CS}$ Access Time	–	45	–	55	–	70	ns
t_{ADS}	Address, $\overline{CS}$ to LE Set-up Time	2	–	2	–	2	–	ns
t_{ADH}	Address, $\overline{CS}$ from LE Hold Time	2	–	2	–	3	–	ns
t_{CPO}	$DATA_{OUT}$ Clock from Address, $\overline{CS}$	36	–	45	–	57	–	ns
t_{EDS}	$DATA_{OUT}$ Clock Enable to Clock Set-up Time	3	–	3	–	3	–	ns
t_{EDH}	$DATA_{OUT}$ Clock Enable from Clock Hold Time	0	–	0	–	2	–	ns
t_{OE}	$\overline{OE}$ to Data Valid	–	8	–	9	–	15	ns
t_{OHZ}[2]	$\overline{OE}$ to High Z	–	7	–	9	–	15	ns
t_{CPD}	$DATA_{OUT}$ Clock to Data Valid	–	8	–	10	–	13	ns
WRITE CYCLE								
t_{AW}	Address, $\overline{CS}$ to End of Write	31	–	45	–	55	–	ns
t_{WP}	Write Pulse Width	27	–	35	–	45	–	ns
t_{ADS}	Address, $\overline{CS}$ to LE Set-up Time	2	–	2	–	2	–	ns
t_{ADH}	Address, $\overline{CS}$ from LE Hold Time	2	–	2	–	3	–	ns
t_{EDS}	$DATA_{IN}$ Clock Enable to Clock Set-up Time	3	–	3	–	3	–	ns
t_{EDH}	$DATA_{IN}$ Clock Enable from Clock Hold Time	0	–	0	–	2	–	ns
t_{DS}	$DATA_{IN}$ to $DATA_{IN}$ Clock Set-up Time	3	–	5	–	5	–	ns
t_{DH}	$DATA_{IN}$ from $DATA_{IN}$ Clock Hold Time	2	–	2	–	3	–	ns
t_{CDW}	$DATA_{IN}$ Clock to End of Write Cycle	27	–	31	–	40	–	ns

NOTES:
1. $\overline{WE}$ Must be high for read cycles.
2. Transition is measured -200mV from steady state voltage with specified loading in Figure 2.

TIMING WAVEFORM OF READ CYCLE



TIMING WAVEFORM OF WRITE CYCLE



13

Integrated Device Technology, Inc.

128K x 8 SRAM WITH LATCHED/ BUFFERED ADDRESS LINES, REGISTERED DATA$_{IN}$ LINES AND LATCHED/BUFFERED DATA$_{OUT}$ LINES

IDT7M822

FEATURES:

- Latched and buffered address lines
- Registered input data lines
- Latched and buffered output data lines
- Separate I/O
- High-speed access time:
  - Military temperature range: 55ns (max.)
  - Commercial temperature range: 45ns (max.)
- 20MHz read/write cycle time

DESCRIPTION:

The IDT7M822 is a 128K x 8 RAM with latched address, registered DATA$_{IN}$ and latched DATA$_{OUT}$ lines. The address and DATA$_{IN}$ latches have independent latch enables (LE) allowing the latch to be used as a buffer by connecting its Latch Enable LE to V_{CC}.

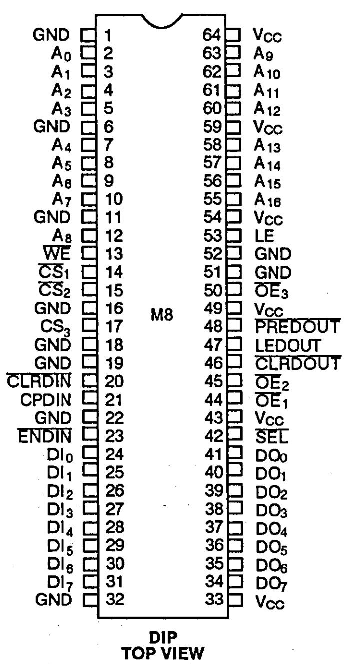
Address, Write Enable ($\overline{WE}$) and the three Chip Select ($\overline{CS}$) lines are controlled by LE. When LE is high, the address latches and decoder are transparent or in the buffer mode. All address, $\overline{CS}$ and $\overline{WE}$ data that meets the specified set-up time will be latched when LE goes low.

DATA$_{IN}$ is controlled by its own clock, CPDIN. When ENDIN (clock enable) is asserted, all DATA$_{IN}$ data that meets the specified set-up time requirements will be registered on the rising edge of CPDIN. $\overline{CLRDIN}$ is an asynchronous control that can be used to clear the DATA$_{IN}$ register.

DATA$_{OUT}$ is controlled by its own enable, LEDOUT. With this line in the high state, the latch is in the transparent or buffer mode. Data out of the RAM array that meets the set-up time requirements will be latched when LEDOUT goes low. $\overline{PREDOUT}$ and $\overline{CLRDOUT}$ are asynchronous controls that can be used to preset or clear the DATA$_{OUT}$ latch. The preset function overrides the clear so that, with both asserted, the latch will be preset. There are three active low output enables for DATA$_{OUT}$. Unless all three of these lines are asserted, the output will be in the high impedance state.

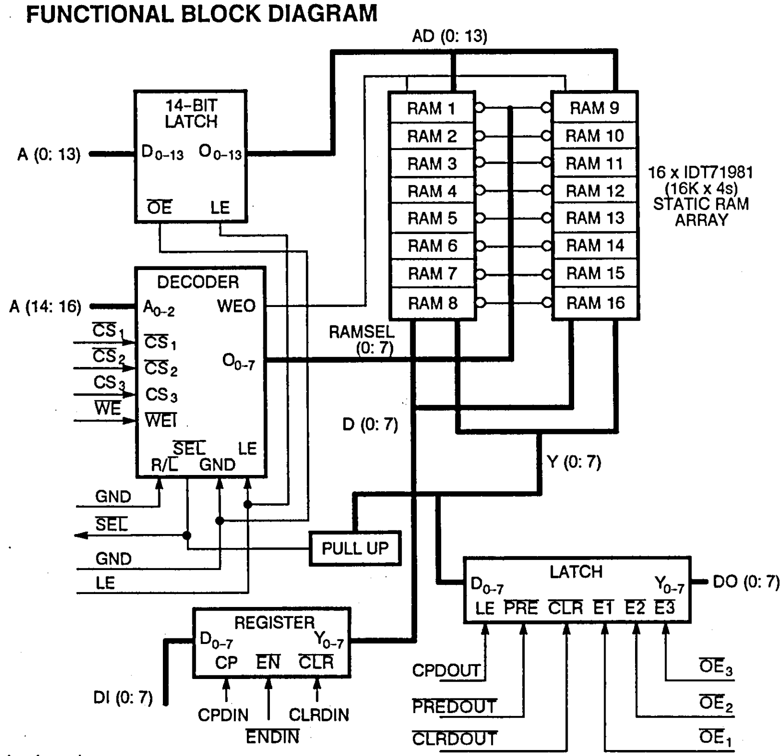
The $\overline{SEL}$ signal is an output that can be used to monitor the state of the internal RAM array output bus.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

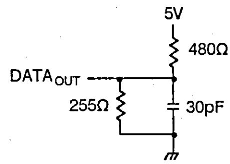


Figure 1. Output Load

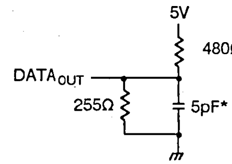


Figure 2. Output Load (for t_{OHZ})

* Including scope and jig.

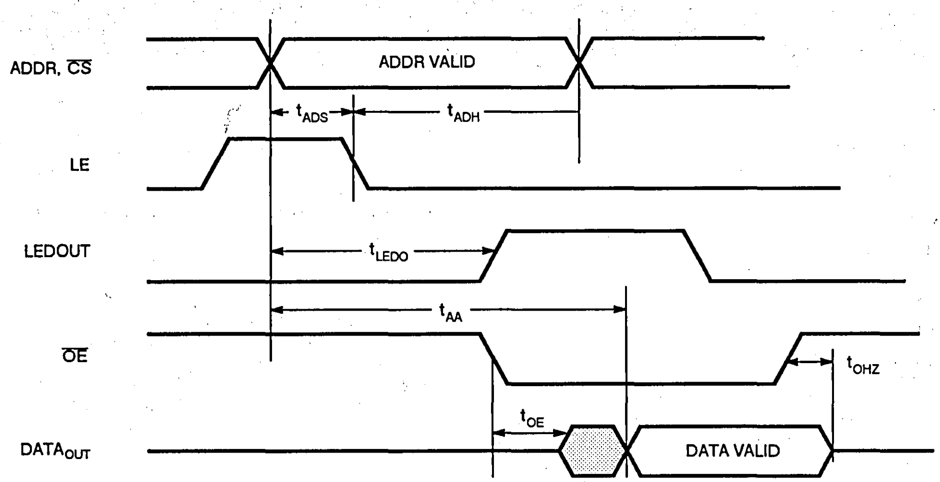
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, T_A = 0°C to +70°C and -55°C to +125°C)

SYMBOL	PARAMETER	IDT7M822S45 (COM'L. ONLY) MIN.	MAX.	IDT7M822S55 MIN.	MAX.	IDT7M822S70 MIN.	MAX.	UNIT
READ CYCLE(1)								
t_{AA}	Address, $\overline{CS}$ Access Time	–	45	–	55	–	70	ns
t_{ADS}	Address, $\overline{CS}$ to LE Set-up Time	2	–	2	–	2	–	ns
t_{ADH}	Address, $\overline{CS}$ from LE Hold Time	2	–	2	–	3	–	ns
t_{LEDO}(2)	$DATA_{OUT}$ Latch from Address, $\overline{CS}$	–	36	–	40	–	55	ns
t_{OE}	$\overline{OE}$ to Data Valid	–	8	–	9	–	15	ns
t_{OHZ}(3)	$\overline{OE}$ to High Z	–	7	–	9	–	15	ns
WRITE CYCLE								
t_{AW}	Address, $\overline{CS}$ to End of Write	31	–	45	–	55	–	ns
t_{WP}	Write Pulse Width	27	–	35	–	45	–	ns
t_{ADS}	Address, $\overline{CS}$ to LE Set-up Time	2	–	2	–	2	–	ns
t_{ADH}	Address, $\overline{CS}$ from LE Hold Time	2	–	2	–	3	–	ns
t_{EDS}	$DATA_{IN}$ Clock Enable to Clock Set-up Time	3	–	3	–	3	–	ns
t_{EDH}	$DATA_{IN}$ Clock Enable from Clock Hold Time	0	–	0	–	2	–	ns
t_{DS}	$DATA_{IN}$ to $DATA_{IN}$ Clock Set-up Time	3	–	3	–	5	–	ns
t_{DH}	$DATA_{IN}$ from $DATA_{IN}$ Clock Hold Time	2	–	2	–	3	–	ns
t_{CDW}	$DATA_{IN}$ Clock to End of Write Cycle	27	–	31	–	40	–	ns

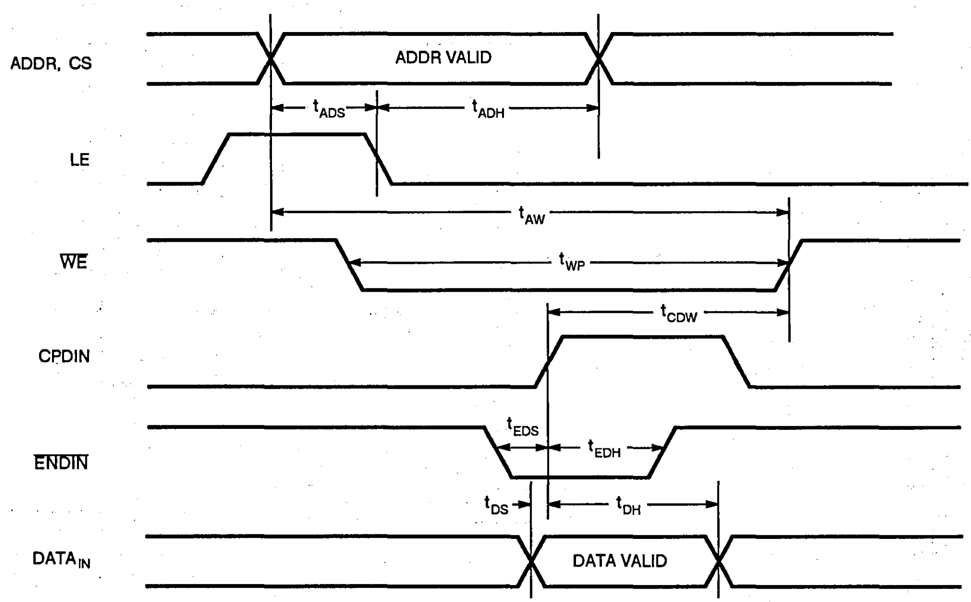
NOTES:

1. $\overline{WE}$ Must be high for read cycles.
2. Latch Enable signal arriving after this maximum will delay overall access time (t_{AA}).
3. Transition is measured -200mV from steady state voltage with specified loading in Figure 2.

TIMING WAVEFORM OF READ CYCLE



TIMING WAVEFORM OF WRITE CYCLE



Integrated Device Technology, Inc.

128K x 8 SRAM WITH LATCHED/ BUFFERED ADDRESS LINES, LATCHED/BUFFERED DATA$_{IN}$ LINES AND REGISTERED DATA$_{OUT}$ LINES

IDT7M823

FEATURES:

- Latched and buffered address lines
- Latched and buffered input data lines
- Registered output data lines
- Separate I/O
- High-speed access time:
  - Military temperature range: 55ns (max.)
  - Commercial temperature range: 45ns (max.)
- 20MHz read/write cycle time

DESCRIPTION:

The IDT7M823 is a 128K x 8 RAM with latched address, latched DATA$_{IN}$ and registered DATA$_{OUT}$ lines. The address and DATA$_{OUT}$ latches have independent latch enables, allowing the latch to be used as a buffer by connecting its Latch Enable (LE) to V_{CC}.

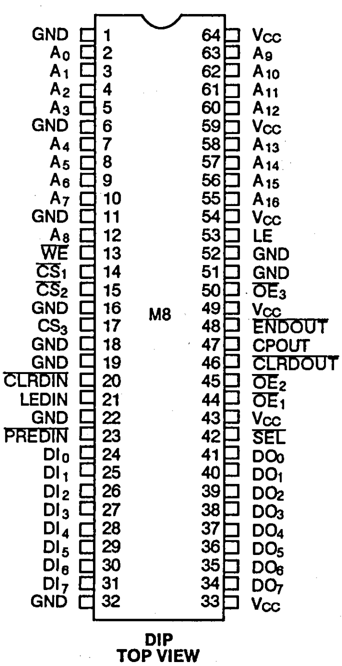
Address, Write Enable ($\overline{WE}$) and the three Chip Select ($\overline{CS}$) lines are controlled by LE. When LE is high, the address latches and decoder are transparent, or in the buffer mode. All address, $\overline{CS}$ and $\overline{WE}$ data that meets the specified set-up time will be latched when LE goes low.

DATA$_{IN}$ is controlled by its own enable, LEDIN. With this line in the high state, the latch is in the transparent or buffer mode. All DATA$_{IN}$ data that meets the specified set-up time will be latched when LEDIN goes low. $\overline{PREDIN}$ and $\overline{CLRDIN}$ are asynchronous controls that can be used to preset or clear the DATA$_{IN}$ latch. The preset function overrides the clear so that, with both asserted, the latch will be preset.

DATA$_{OUT}$ is controlled by its own clock, CPDOUT. When ENDOUT (clock enable) is asserted, all data out of the RAM array that meets the set-up time requirements will be registered on the rising edge of CPDOUT. $\overline{CLRDOUT}$ is an asynchronous control that can be used to clear the DATA$_{OUT}$ register. There are three active low output enables for DATA$_{OUT}$. Unless all three of these lines are asserted, the output will be in the high impedance state.

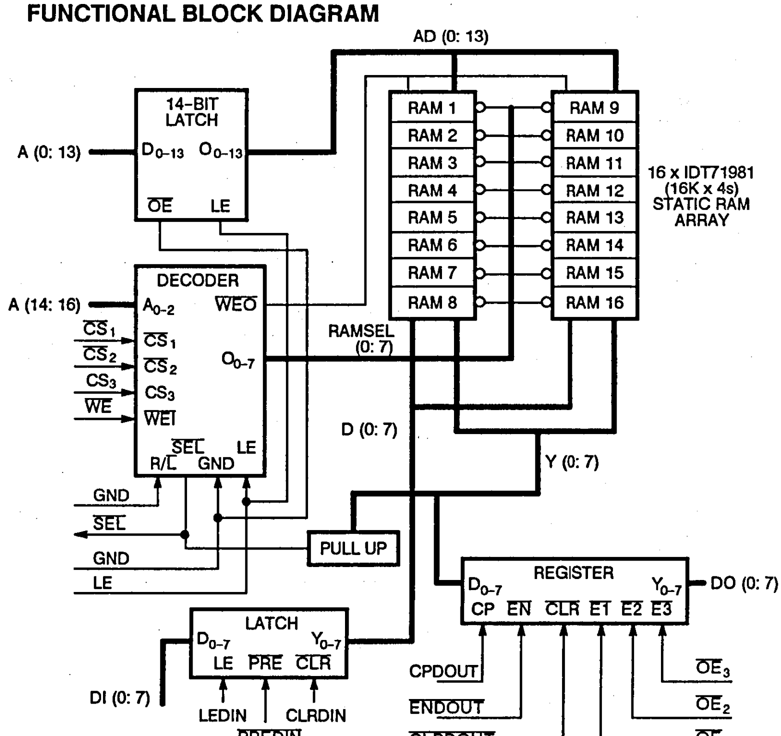
The $\overline{SEL}$ signal is an output that can be used to monitor the state of the internal RAM array output bus.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

13

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

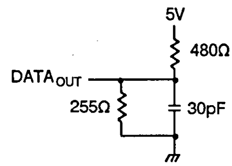


Figure 1. Output Load

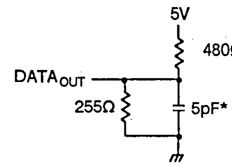


Figure 2. Output Load (for t_{OHZ})

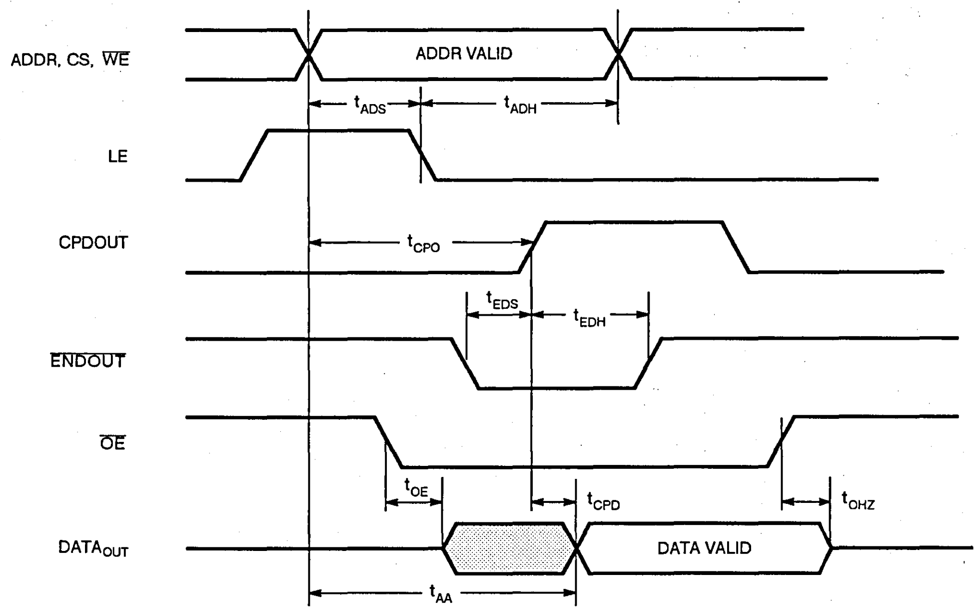
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, T_A = 0°C to +70°C and -55°C to +125°C)

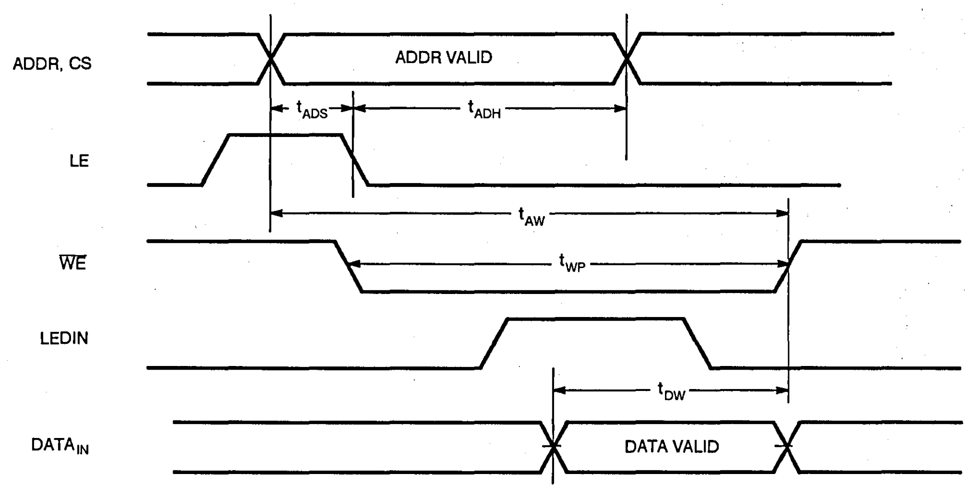
SYMBOL	PARAMETER	IDT7M823S45 (COM'L. ONLY) MIN.	MAX.	IDT7M823S55 MIN.	MAX.	IDT7M823S70 MIN.	MAX.	UNIT
READ CYCLE[1]								
t_{AA}	Address, $\overline{CS}$ Access Time	–	45	–	55	–	70	ns
t_{ADS}	Address, $\overline{CS}$ to LE Set-up Time	2	–	2	–	2	–	ns
t_{ADH}	Address, $\overline{CS}$ from LE Hold Time	2	–	2	–	3	–	ns
t_{CPO}	$DATA_{OUT}$ Clock from Address, $\overline{CS}$	36	–	45	–	57	–	ns
t_{EDS}	$DATA_{OUT}$ Clock Enable to Clock Set-up Time	3	–	3	–	3	–	ns
t_{EDH}	$DATA_{OUT}$ Clock Enable from Clock Hold Time	0	–	0	–	2	–	ns
t_{OE}	$\overline{OE}$ to Data Valid	–	8	–	9	–	15	ns
t_{OHZ}[2]	$\overline{OE}$ to High Z	–	7	–	9	–	15	ns
t_{CPD}	$DATA_{OUT}$ Clock to Data Valid	–	8	–	10	–	13	ns
WRITE CYCLE								
t_{AW}	Address, $\overline{CS}$ to End of Write	31	–	41	–	55	–	ns
t_{WP}	Write Pulse Width	27	–	37	–	50	–	ns
t_{ADS}	Address, $\overline{CS}$ to LE Set-up Time	2	–	2	–	2	–	ns
t_{ADH}	Address, $\overline{CS}$ from LE Hold Time	2	–	2	–	3	–	ns
t_{DW}	Data Valid to End of Write	26	–	36	–	50	–	ns

NOTES:
1. $\overline{WE}$ Must be high for read cycles.
2. Transition is measured -200mV from steady state voltage with specified loading in Figure 2.

TIMING WAVEFORM OF READ CYCLE



TIMING WAVEFORM OF WRITE CYCLE



13

Integrated Device Technology, Inc.

128K x 8 SRAM WITH REGISTERED ADDRESS LINES, AND REGISTERED DATA LINES

IDT7M825

FEATURES:

- Registered address lines
- Registered input data lines
- Registered output data lines
- Separate I/O
- High-speed access time:
  - Military temperature range: 60ns (max.)
  - Commercial temperature range: 50ns (max.)
- 20MHz read/write cycle time

DESCRIPTION:

The IDT7M825 is a 128K x 8 RAM with registered address, registered DATA$_{IN}$ and registered DATA$_{OUT}$ lines. Each of the three buses has its own independent clock.

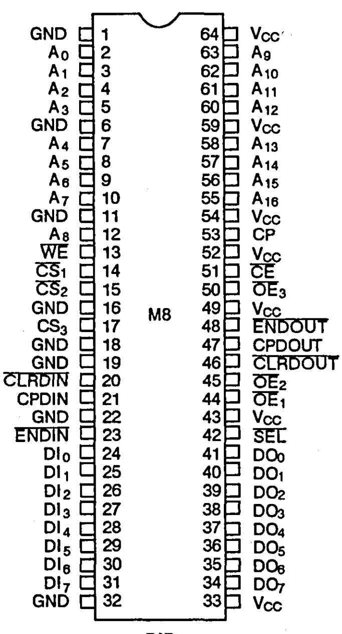
Address, Write Enable ($\overline{WE}$) and the three Chip Select ($\overline{CS}$) lines are controlled by CP. When $\overline{CE}$ (clock enable) is asserted, all address, $\overline{CS}$ and $\overline{WE}$ data that meets the specified set-up time will be registered on the rising edge of CP.

DATA$_{IN}$ is controlled by its own clock, CPDIN. When ENDIN (clock enable) is asserted, all DATA$_{IN}$ data that meets the specified set-up time will be registered on the rising edge of CPDIN. $\overline{CLRDIN}$ is an asynchronous control that can be used to clear the DATA$_{IN}$ register.

DATA$_{OUT}$ is controlled by its own clock, CPDOUT. When $\overline{ENDOUT}$ (clock enable) is asserted, all data out of the RAM array that meets the set-up time requirements will be registered on the rising edge of CPDOUT. $\overline{CLRDOUT}$ is an asynchronous control that can be used to clear the DATA$_{OUT}$ register. There are three active low output enables for DATA$_{OUT}$. Unless all three of these lines are asserted, the output will be in the high impedance state.

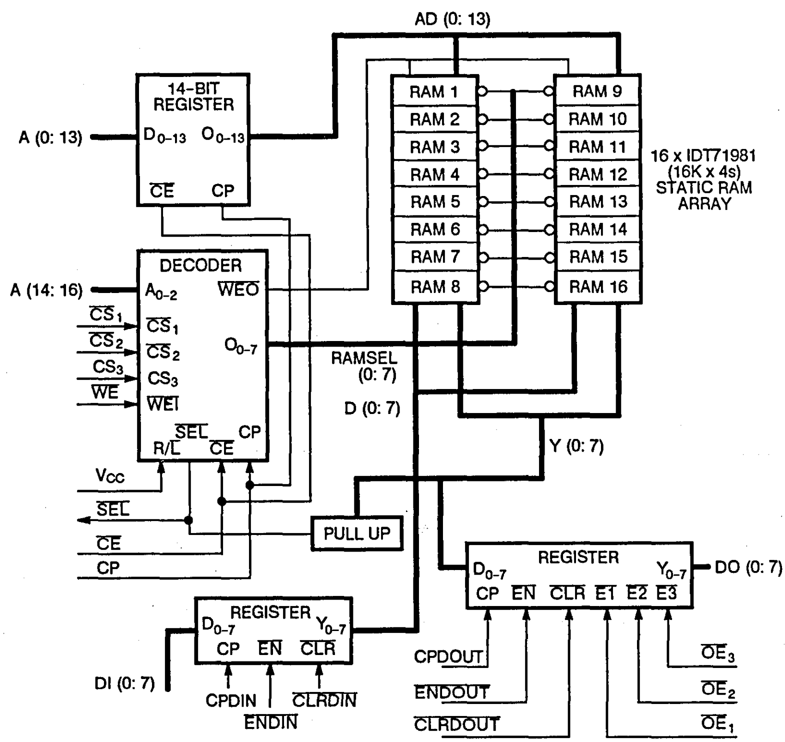
The $\overline{SEL}$ signal is an output that can be used to monitor the state of the internal RAM array output bus.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

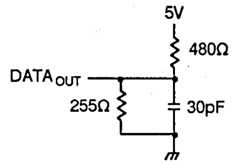


Figure 1. Output Load

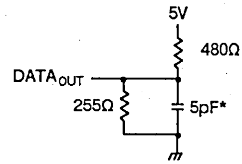


Figure 2. Output Load (for t_{OHZ})

* Including scope and jig.

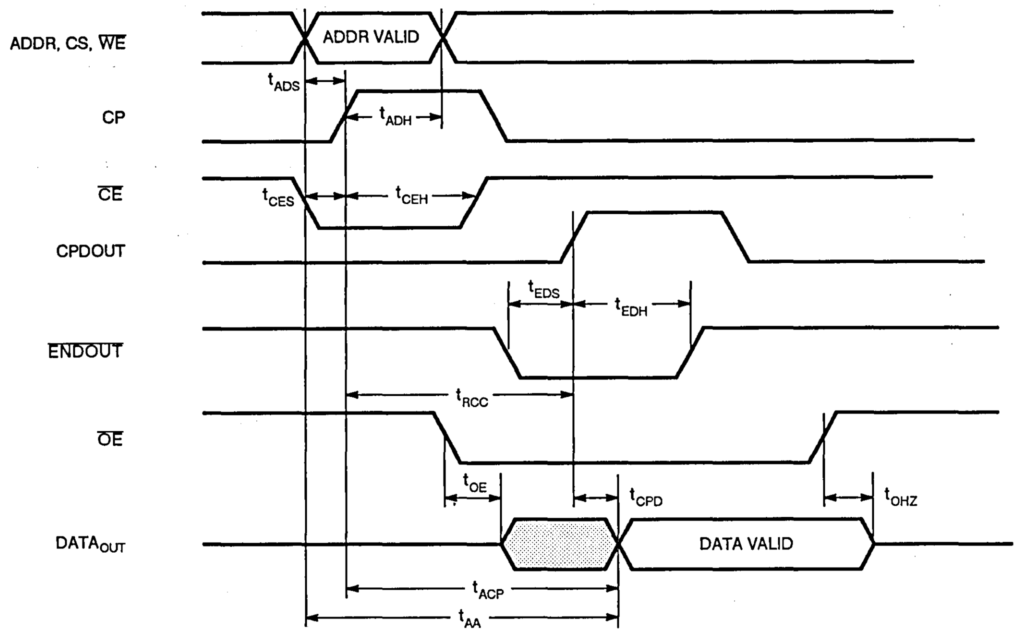
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, T_A = 0°C to +70°C and -55°C to +125°C)

SYMBOL	PARAMETER	IDT7M825S50 (COM'L. ONLY) MIN.	MAX.	IDT7M825S60 MIN.	MAX.	IDT7M825S70 MIN.	MAX.	UNIT
READ CYCLE[1]								
t_{RCC}	Min. Clock to Clock Time	40	–	50	–	60	–	ns
t_{ACP}[2]	Address, $\overline{CS}$ Clock to Data Valid	–	48	–	58	–	67	ns
t_{ADS}	Address, $\overline{CS}$ to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{ADH}	Address, $\overline{CS}$ from Address Clock Hold Time	2	–	2	–	3	–	ns
t_{CES}	Address Clock Enable to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{CEH}	Address Clock Enable from Address Clock Hold Time	2	–	2	–	5	–	ns
t_{EDS}	$DATA_{OUT}$ Clock Enable to $DATA_{OUT}$ Clock Set-up Time	3	–	3	–	5	–	ns
t_{EDH}	$DATA_{OUT}$ Clock Enable from $DATA_{OUT}$ Clock Hold Time	0	–	0	–	3	–	ns
t_{OE}	Output Enable to Output Data Valid	–	8	–	9	–	20	ns
t_{OHZ}[3]	Output Enable to Output in High Z	–	7	–	8	–	18	ns
t_{CPD}	$DATA_{OUT}$ Clock CPDOUT to Data Valid	–	8	–	9	–	15	ns
WRITE CYCLE								
t_{AW}	Write Cycle Time	35	–	45	–	60	–	ns
t_{CWPL}	Address Clock Low Pulse Width	20	–	30	–	35	–	ns
t_{CWPH}	Address Clock High Pulse Width	7	–	10	–	10	–	ns
t_{ADS}, t_{WES}	Address, $\overline{CS}$, $\overline{WE}$ to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{ADH}, t_{WEH}	Address, $\overline{CS}$, $\overline{WE}$ from Address Clock Hold Time	2	–	2	–	3	–	ns
t_{CES}	Address Clock Enable to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{CEH}	Address Clock Enable from Address Clock Hold Time	2	–	2	–	3	–	ns
t_{EDS}	$DATA_{IN}$ Clock Enable to $DATA_{IN}$ Clock Set-up Time	3	–	3	–	5	–	ns
t_{EDH}	$DATA_{IN}$ Clock Enable from $DATA_{IN}$ Clock Hold Time	0	–	0	–	3	–	ns
t_{DS}	$DATA_{IN}$ to $DATA_{IN}$ Clock Set-up Time	3	–	3	–	5	–	ns
t_{DH}	$DATA_{IN}$ from $DATA_{IN}$ Clock Hold Time	2	–	2	–	3	–	ns
t_{CDW}	$DATA_{IN}$ Clock to End of Write Cycle	27	–	35	–	50	–	ns

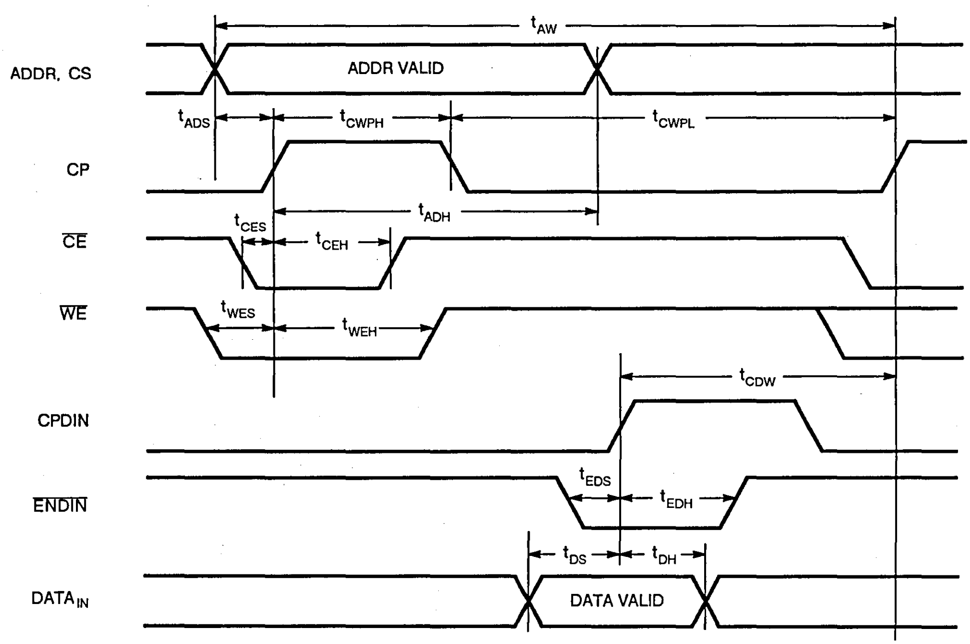
NOTES:
1. $\overline{WE}$ Must be high for read cycles.
2. Assumes min t_{RCC} is observed.
3. Transition is measured -200mV from steady state voltage with specified loading in Figure 2.

13

TIMING WAVEFORM OF READ CYCLE



TIMING WAVEFORM OF WRITE CYCLE



Integrated Device Technology, Inc.

128K x 8 SRAM WITH REGISTERED ADDRESS LINES, REGISTERED DATA$_{IN}$ LINES AND LATCHED/BUFFERED DATA$_{OUT}$ LINES

IDT7M826

FEATURES:

- Registered address lines
- Registered input data lines
- Latched and buffered output data lines
- Separate I/O
- High-speed access time:
  - Military temperature range: 55ns (max.)
  - Commercial temperature range: 45ns (max.)
- 20MHz read/write cycle time

DESCRIPTION:

The IDT7M826 is a 128K x 8 RAM with registered address, registered DATA$_{IN}$ and latched DATA$_{OUT}$ lines. The DATA$_{OUT}$ latch can be used as a buffer by connecting its Latch Enable (LE) to V_{CC}.

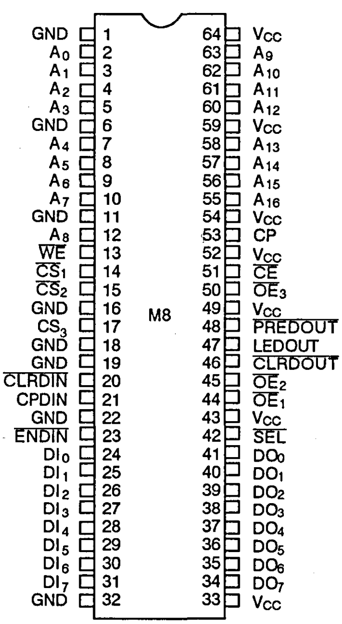
Address, Write Enable ($\overline{WE}$) and the three Chip Select ($\overline{CS}$) lines are controlled by CP. When $\overline{CE}$ (clock enable) is asserted, all address, $\overline{CS}$ and $\overline{WE}$ data that meets the specified set-up time will be registered on the rising edge of CP.

DATA$_{IN}$ is controlled by its own clock, CPDIN. When ENDIN (clock enable) is asserted, all DATA$_{IN}$ data that meets the specified set-up time will be registered on the rising edge of CPDIN. $\overline{CLRDIN}$ is an asynchronous control that can be used to clear the DATA$_{IN}$ register.

DATA$_{OUT}$ is controlled by its own enable, LEDOUT. With this line in the high state, the latch is in the transparent or buffer mode. Data out of the RAM array that meets the set-up time requirements will be latched when LEDOUT goes low. $\overline{PREDOUT}$ and $\overline{CLRDOUT}$ are asynchronous controls that can be used to clear the DATA$_{OUT}$ latch. The preset function overrides the clear so that, with both asserted, the latch will be preset. Unless all three of these lines are asserted, the output will be in the high impedance state.

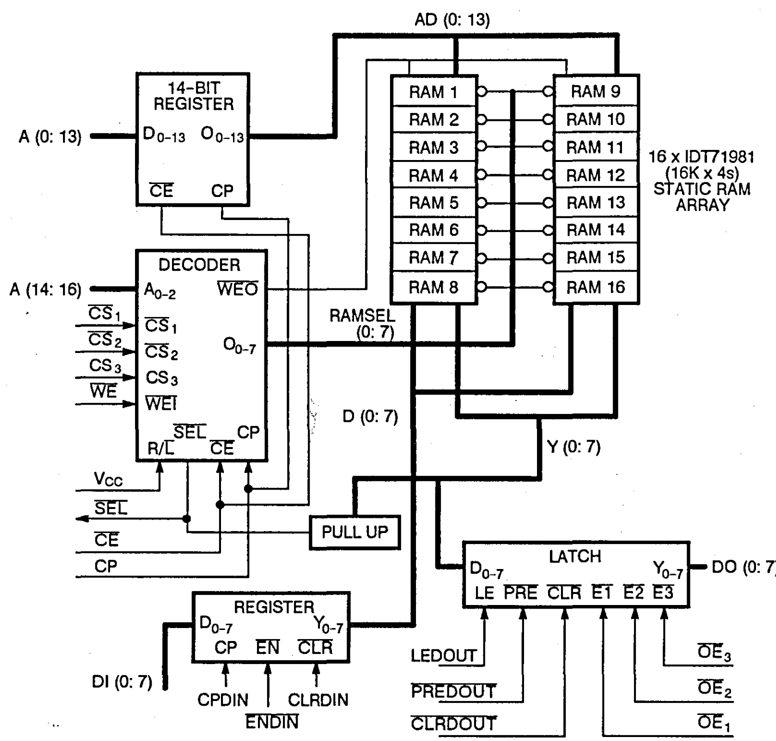
The $\overline{SEL}$ signal is an output that can be used to monitor the state of the internal RAM array output bus.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



13

CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-7000/-

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

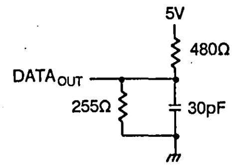


Figure 1. Output Load

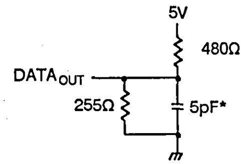


Figure 2. Output Load (for t_{OHZ})

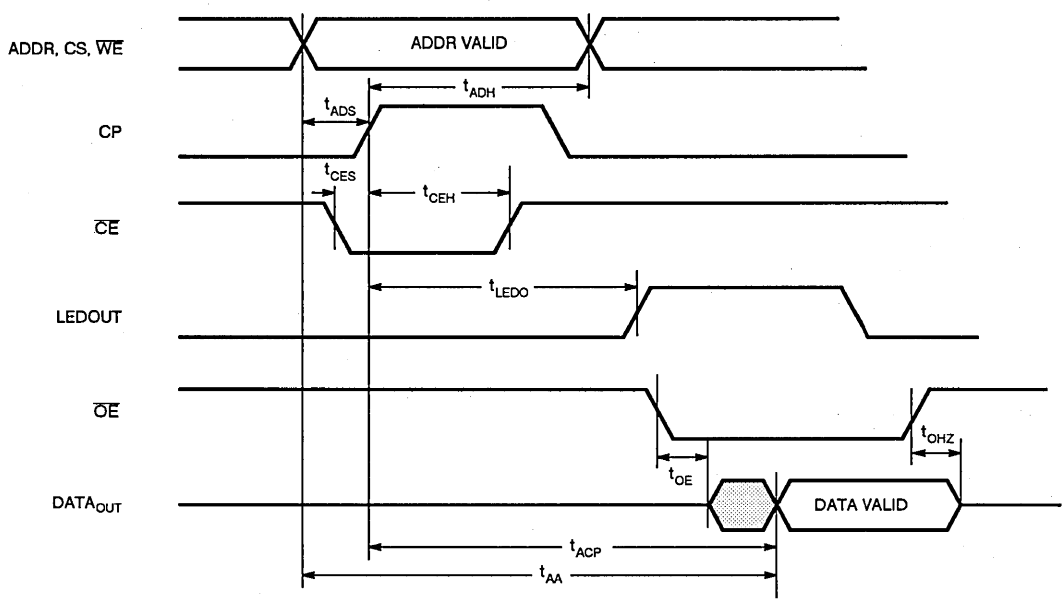
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, T_A = 0°C to +70°C and -55°C to +125°C)

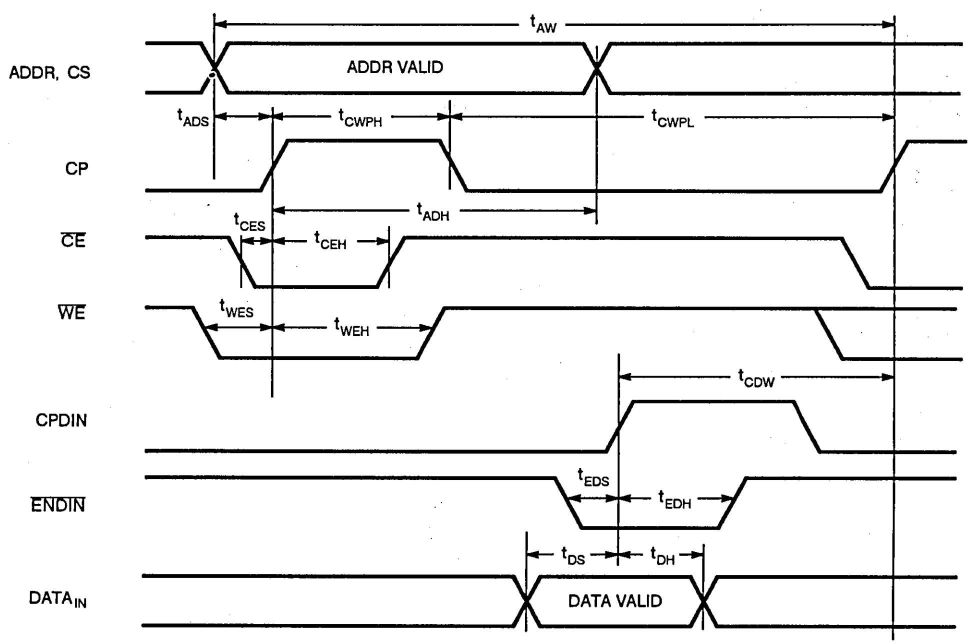
SYMBOL	PARAMETER	IDT7M826S45 (COM'L. ONLY) MIN.	MAX.	IDT7M826S55 MIN.	MAX.	IDT7M826S70 MIN.	MAX.	UNIT
READ CYCLE[1]								
t_{ACP}	Address, $\overline{CS}$ Clock to Data Valid	–	45	–	55	–	70	ns
t_{ADS}	Address, $\overline{CS}$ to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{ADH}	Address, $\overline{CS}$ from Address Clock Hold Time	2	–	2	–	3	–	ns
t_{CES}	Address Clock Enable to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{CEH}	Address Clock Enable from Address Clock Hold Time	2	–	2	–	5	–	ns
t_{LEDO}	$DATA_{OUT}$ LE from Address Clock	–	39	–	46	–	55	ns
t_{OE}	$\overline{OE}$ to Data Valid	–	8	–	9	–	15	ns
t_{OHZ}[2]	$\overline{OE}$ to High Z	–	7	–	9	–	13	ns
WRITE CYCLE								
t_{AW}	Write Cycle Time	35	–	45	–	60	–	ns
t_{CWPL}	Address Clock Low Pulse Width	20	–	30	–	35	–	ns
t_{CWPH}	Address Clock High Pulse Width	7	–	10	–	10	–	ns
t_{ADS}, t_{WEH}	Address, $\overline{CS}$, $\overline{WE}$ to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{ADH}, t_{WEH}	Address, $\overline{CS}$, $\overline{WE}$ from Address Clock Hold Time	2	–	2	–	3	–	ns
t_{CES}	Address Clock Enable to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{CEH}	Address Clock Enable from Address Clock Hold Time	2	–	2	–	3	–	ns
t_{EDS}	$DATA_{IN}$ Clock Enable to $DATA_{IN}$ Clock Set-up Time	3	–	3	–	5	–	ns
t_{EDH}	$DATA_{IN}$ Clock Enable from $DATA_{IN}$ Clock Hold Time	0	–	0	–	3	–	ns
t_{DS}	$DATA_{IN}$ to $DATA_{IN}$ Clock Set-up Time	3	–	3	–	5	–	ns
t_{DH}	$DATA_{IN}$ from $DATA_{IN}$ Clock Hold Time	2	–	2	–	3	–	ns
t_{CDW}	$DATA_{IN}$ Clock to End of Write Cycle	27	–	35	–	50	–	ns

NOTES:
1. $\overline{WE}$ Must be high for read cycles.
2. Transition is measured -200mV from steady state voltage with specified loading in Figure 2.

TIMING WAVEFORM OF READ CYCLE



TIMING WAVEFORM OF WRITE CYCLE



13

128K x 8 SRAM WITH REGISTERED ADDRESS LINES, LATCHED /BUFFERED DATA$_{IN}$ LINES AND REGISTERED DATA$_{OUT}$ LINES

IDT7M827

Integrated Device Technology, Inc.

FEATURES:

- Registered address lines
- Latched and Buffered input data lines
- Registered output data lines
- Separate I/O
- High-speed access time:
  - Military temperature range: 60ns (max.)
  - Commercial temperature range: 50ns (max.)
- 20MHz read/write cycle time

DESCRIPTION:

The IDT7M827 is a 128K x 8 RAM with registered address, latched DATA$_{IN}$ and registered DATA$_{OUT}$ lines. The DATA$_{IN}$ latch can be used as a BUFFER by connecting its Latch Enable (LE) to Vcc.

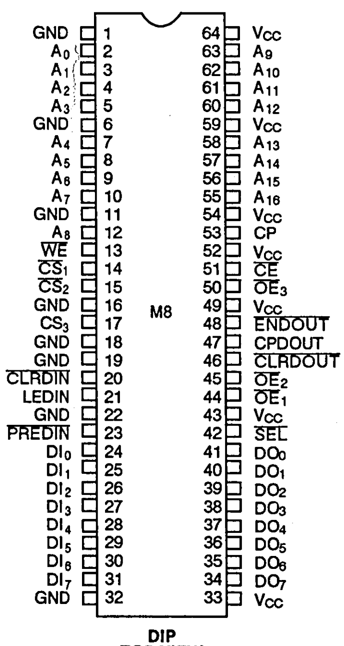
Address, Write Enable ($\overline{WE}$) and the three Chip Select ($\overline{CS}$) lines are controlled by CP. When $\overline{CE}$ (clock enable) is asserted, all address, $\overline{CS}$ and $\overline{WE}$ data that meets the specified set-up time will be registered on the rising edge of CP.

DATA$_{IN}$ is controlled by its own enable, LEDIN. With this line in the high state, the latch is in the transparent or buffer mode. All DATA$_{IN}$ data that meets the specified set-up time will be latched when LEDIN goes low. $\overline{PREDIN}$ and $\overline{CLRDIN}$ are asynchronous controls that can be used to preset or clear the DATA$_{IN}$ latch. The preset function overrides the clear so that, with both asserted, the latch will be preset.

DATA$_{OUT}$ is controlled by its own clock, CPDOUT. When $\overline{ENDOUT}$ (clock enable) is asserted, all data out of the RAM array that meets the set-up time requirements will be registered on the rising edge of CPDOUT. $\overline{CLRDOUT}$ is an asynchronous control that can be used to clear the DATA$_{OUT}$ register. There are three active low output enables for DATA$_{OUT}$. Unless all three of these lines are asserted, the output will be in the high impedance state.

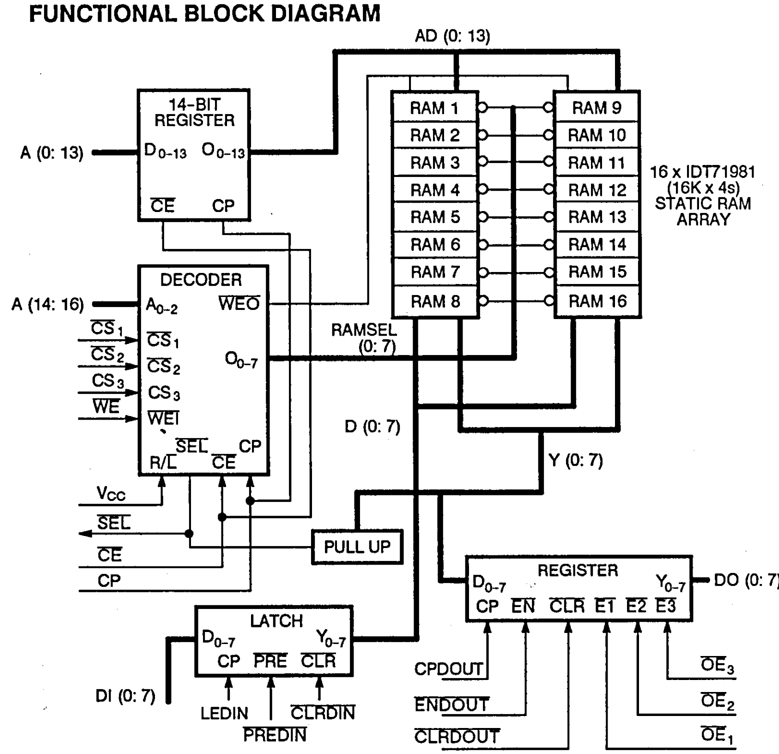
The $\overline{SEL}$ signal is an output that can be used to monitor the state of the internal RAM array output bus.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

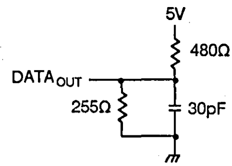


Figure 1. Output Load

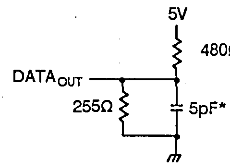


Figure 2. Output Load (for t_{OHZ})

* Including scope and jig.

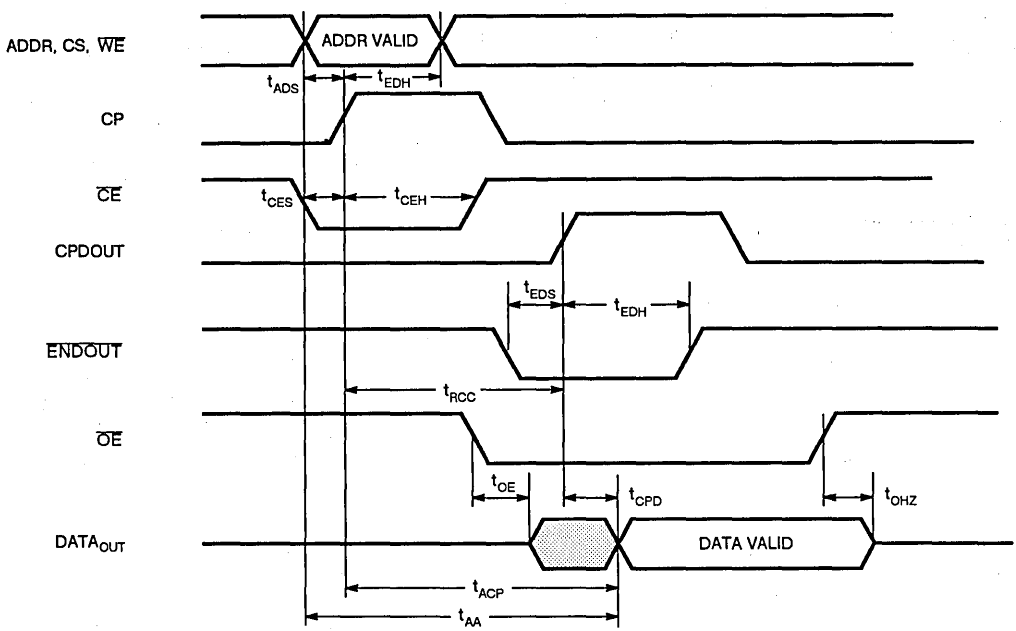
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, T_A = 0°C to +70°C and -55°C to +125°C)

SYMBOL	PARAMETER	IDT7M827S50 (COM'L ONLY) MIN.	IDT7M827S50 (COM'L ONLY) MAX.	IDT7M827S60 MIN.	IDT7M827S60 MAX.	IDT7M827S70 MIN.	IDT7M827S70 MAX.	UNIT
READ CYCLE[1]								
t_{RCC}	Min. Clock to Clock Time	40	–	50	–	60	–	ns
t_{ACP}[2]	Address, $\overline{CS}$ Clock to Data Valid	–	48	–	58	–	67	ns
t_{ADS}	Address, $\overline{CS}$ to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{ADH}	Address, $\overline{CS}$ from Address Clock Hold Time	2	–	2	–	3	–	ns
t_{CES}	Address Clock Enable to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{CEH}	Address Clock Enable from Address Clock Hold Time	2	–	2	–	5	–	ns
t_{EDS}	$DATA_{OUT}$ Clock Enable to $DATA_{OUT}$ Clock Set-up Time	3	–	3	–	5	–	ns
t_{EDH}	$DATA_{OUT}$ Clock Enable from $DATA_{OUT}$ Clock Hold Time	0	–	0	–	3	–	ns
t_{OE}	Output Enable to Output Data Valid	–	8	–	9	–	20	ns
t_{OHZ}[3]	Output Enable to Output in High Z	–	7	–	8	–	18	ns
t_{CPD}	$DATA_{OUT}$ Clock CPDOUT to Data Valid	–	8	–	9	–	15	ns
WRITE CYCLE								
t_{AW}	Write Cycle Time	35	–	45	–	60	–	ns
t_{CWPL}	Address Clock Low Pulse Width	20	–	27	–	35	–	ns
t_{CWPH}	Address Clock High Pulse Width	7	–	10	–	10	–	ns
t_{ADS}, t_{WES}	Address, $\overline{CS}$, $\overline{WE}$ to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{ADH}, t_{WEH}	Address, $\overline{CS}$, $\overline{WE}$ from Address Clock Hold Time	2	–	2	–	3	–	ns
t_{CES}	Address Clock Enable to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{CEH}	Address Clock Enable from Address Clock Hold Time	2	–	2	–	3	–	ns
t_{DW}	Data Valid to End of Write	26	–	32	–	45	–	ns

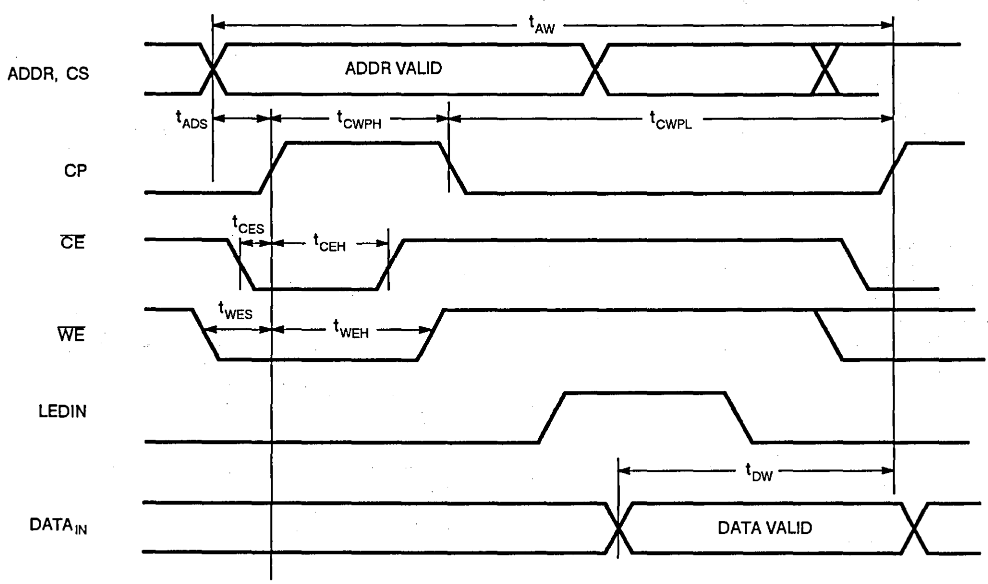
NOTES:
1. $\overline{WE}$ Must be high for read cycles.
2. Assumes min t_{RCC} is observed.
3. Transition is measured -200mV from steady state voltage with specified loading in Figure 2.

13

TIMING WAVEFORM OF READ CYCLE



TIMING WAVEFORM OF WRITE CYCLE



Integrated Device Technology, Inc.

128K x 8 SRAM WITH REGISTERED ADDRESS LINES AND LATCHED/ BUFFERED DATA LINES

IDT7M828

FEATURES:

- Registered address lines
- Latched and buffered input data lines
- Latched and buffered output data lines
- Separate I/O
- High-speed access time:
  - Military temperature range: 55ns (max.)
  - Commercial temperature range: 45ns (max.)
- 20MHz read/write cycle time

DESCRIPTION:

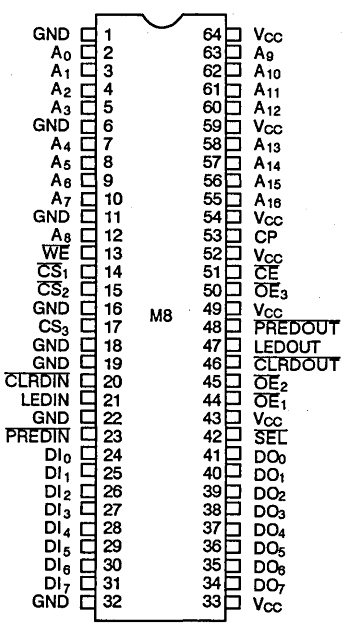
The IDT7M828 is a 128K x 8 RAM with registered address, latched $DATA_{IN}$ and latched $DATA_{OUT}$ lines. The two data buses have independent latch enables and this allows the latch to be used as a buffer by connecting the appropriate Latch Enable (LE) to V_{CC}.

Address, Write Enable ($\overline{WE}$) and the three Chip Select ($\overline{CS}$) lines are controlled by CP. When $\overline{CE}$ (clock enable) is asserted, all address, $\overline{CS}$ and $\overline{WE}$ data that meets the specified set-up time will be registered on the rising edge of CP.

$DATA_{IN}$ is controlled by its own enable, LEDIN. With this line in the high state, the latch is in the transparent or buffer mode. All $DATA_{IN}$ data that meets the specified set-up time will be latched when LEDIN goes low. $\overline{PREDIN}$ and $\overline{CLRDIN}$ are asynchronous controls that can be used to preset or clear the $DATA_{IN}$ latch. The preset function overrides the clear so that, with both asserted, the latch will be preset.

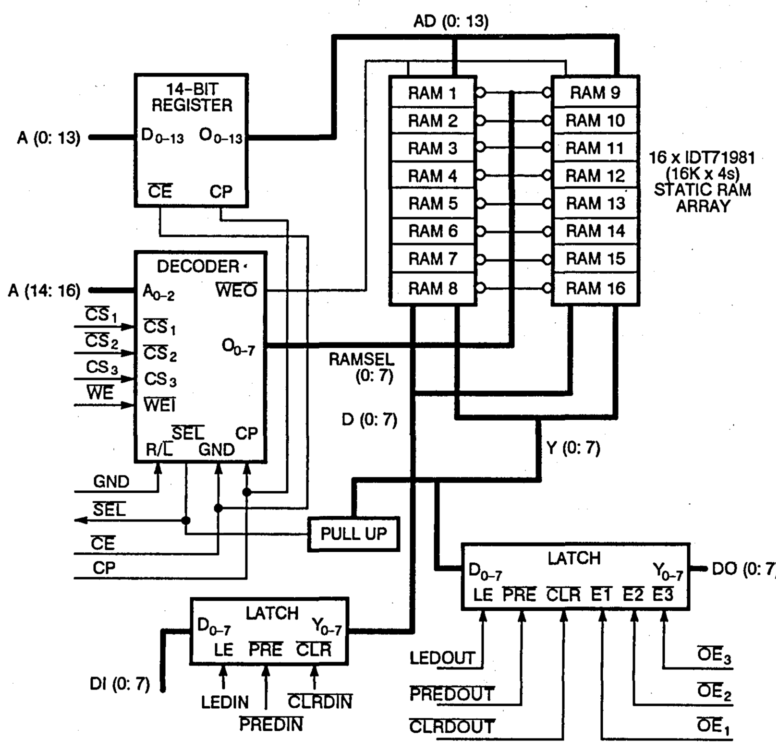
$DATA_{OUT}$ is controlled by its own enable, LEDOUT. With this line in the high state, the latch is in the transparent, or buffer mode. Data out of the RAM array that meets the set-up time requirements will be latched when LEDOUT goes low. $\overline{PREDOUT}$ and $\overline{CLRDOUT}$ are asynchronous controls that can be used to clear the $DATA_{OUT}$ latch. The preset function overrides the clear so that, with both asserted, the latch will be preset. There are three active low output enables for $DATA_{OUT}$. Unless all three of these lines are asserted, the output will be in the high impedance state.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



13

CEMOS is a trademark of Integrated Device Technology, Inc.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

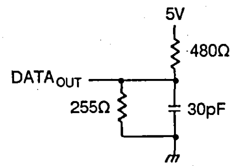


Figure 1. Output Load

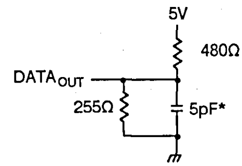


Figure 2. Output Load (for t_{OHZ})

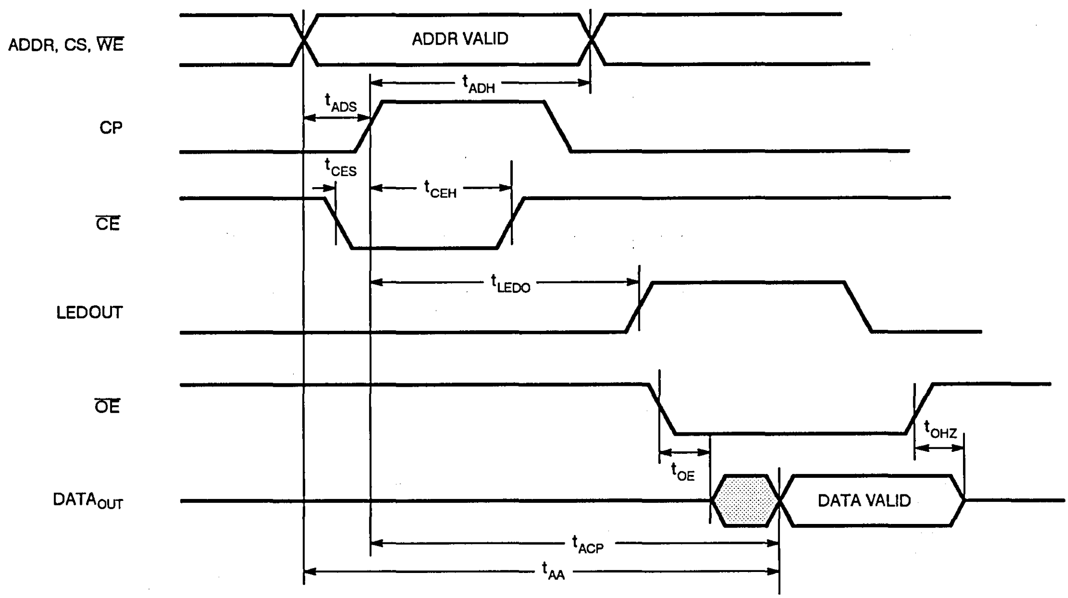
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, T_A = 0°C to +70°C and -55°C to +125°C)

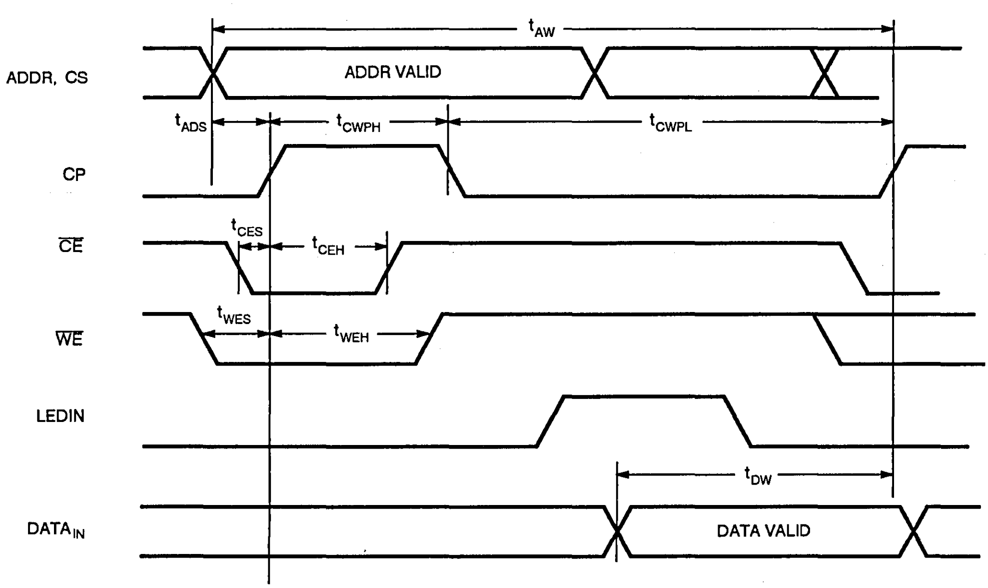
SYMBOL	PARAMETER	IDT7M828S45 (COM'L. ONLY) MIN.	MAX.	IDT7M828S55 MIN.	MAX.	IDT7M828S70 MIN.	MAX.	UNIT
READ CYCLE[1]								
t_{ACP}	Address, $\overline{CS}$ Clock to Data Valid	–	45	–	55	–	70	ns
t_{ADS}	Address, $\overline{CS}$ to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{ADH}	Address, $\overline{CS}$ from Address Clock Hold Time	2	–	2	–	3	–	ns
t_{CES}	Address Clock Enable to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{CEH}	Address Clock Enable from Address Clock Hold Time	2	–	2	–	5	–	ns
t_{LEDO}	DATA$_{OUT}$ LE from Address Clock	–	39	–	46	–	55	ns
t_{OE}	$\overline{OE}$ to Data Valid	–	8	–	9	–	15	ns
t_{OHZ}[2]	$\overline{OE}$ to High Z	–	7	–	9	–	13	ns
WRITE CYCLE								
t_{AW}	Write Cycle Time	35	–	45	–	60	–	ns
t_{CWPL}	Address Clock Low Pulse Width	20	–	27	–	35	–	ns
t_{CWPH}	Address Clock High Pulse Width	7	–	10	–	10	–	ns
t_{ADS}, t_{WES}	Address, $\overline{CS}$, $\overline{WE}$ to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{ADH}, t_{WEH}	Address, $\overline{CS}$, $\overline{WE}$ from Address Clock Hold Time	2	–	2	–	3	–	ns
t_{CES}	Address Clock Enable to Address Clock Set-up Time	2	–	2	–	3	–	ns
t_{CEH}	Address Clock Enable from Address Clock Hold Time	2	–	2	–	3	–	ns
t_{DW}	Data Valid to End of Write	26	–	32	–	45	–	ns

NOTES:
1. $\overline{WE}$ Must be high for read cycles.
2. Transition is measured -200mV from steady state voltage with specified loading in Figure 2.

TIMING WAVEFORM OF READ CYCLE



TIMING WAVEFORM OF WRITE CYCLE



ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (-55°C to +125°C) Semiconductor Components Screened to MIL-STD-883, Class B
Package	C	Sidebraze DIP
Speed	45 55 70	Speed in Nanoseconds
Power	S	Standard-Power
	L	Low-Power
Device Type	7M820-828	

Integrated Device Technology, Inc.

DUAL MULTIPLEXED 16K x 20 SYNCHRONOUS STATIC RAM MODULE

ADVANCE INFORMATION
IDT7M6001

FEATURES:

- Dual 16K x 20 synchronous RAM
- Edge triggered data input and data output registers
- Edge triggered data address registers
- Two address register sources individually selectable
- Separate chip select and write enables to each memory array
- Individual clock lines to each register
- Dual high-performance 16K x 20 memories
- Unique ping-pong operation capability
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in compact 92-pin ceramic sidebraze QIP (quad in-line) package
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Military modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

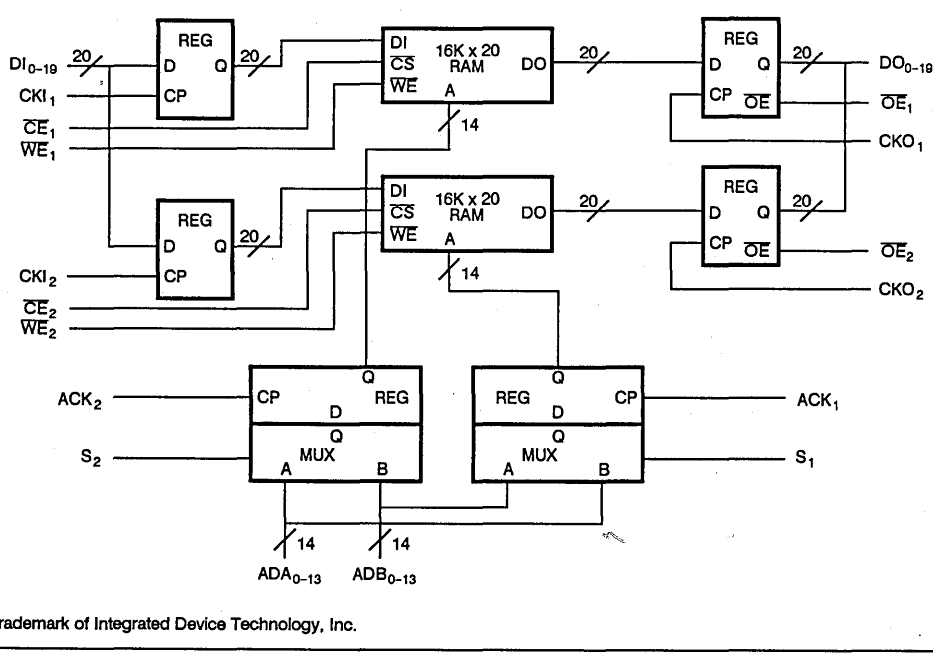
The IDT7M6001 is a dual multiplexed 16K x 20 synchronous RAM module. It utilizes ten IDT71981 high-speed synchronous memories, along with the appropriate input data, output data and address registers. The device features the ability to be used in a ping-pong mode. That is, data can be loaded into one memory array at one address and be read from the other memory array at a different address. This allows systems to be built that can perform fast Fourier Transforms in either a decimation-in-time or a decimation-in-frequency configuration. Data read from Memory 1 can be synchronously loaded into its output register, while data can be written into a different location in Memory 2. Similarly, data can be read from Memory 1 and Memory 2 in parallel from two different addresses and can be written into Memory 1 and Memory 2 at unique addresses. Registers at the data input and data output provide fully synchronous pipelined operation. The two memory systems are 20 bits wide and have multiplexed data input and data output bits from the module data pins. By taking advantage of the speed of the registers, data on the pins can run at a speed twice that of the memory. That is, both output registers can be read or both input registers can be loaded in a single memory cycle.

Two address sources are available to each address register to the RAM. Address Source A or Address Source B may be selected to load the edge triggered register for the 16K x 20-bit memory. The IDT54/74FCT399 is used for the two input multiplexer and address registers for each 16K x 20 memory. All inputs and outputs of the IDT7M4017 are TTL-compatible and operate from a single 5V supply.

The IDT7M6001 is offered as a compact 92-pin quad in-line (QIP) ceramic module. It is constructed using ceramic LCC components on a multilayer co-fired ceramic substrate and occupies only 4.2 square inches of board space.

All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

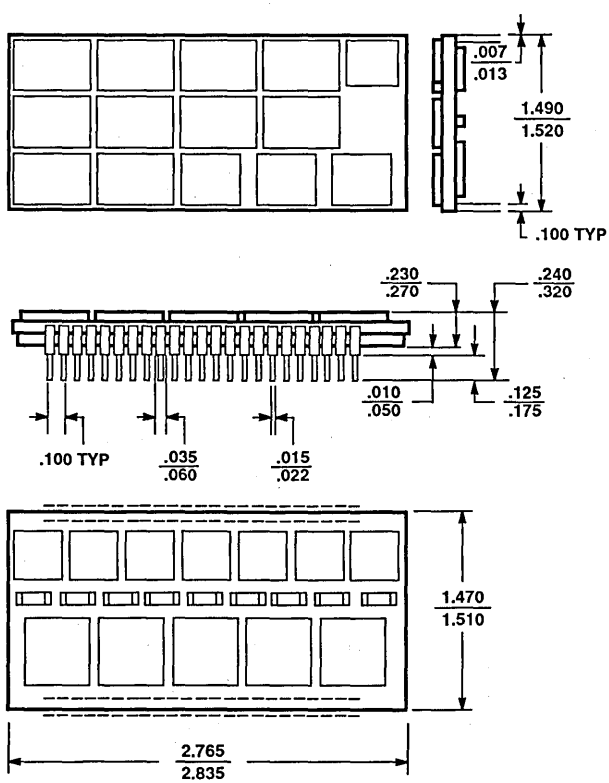
PIN CONFIGURATION

Signal	Pin	Pin	Signal	Signal	Pin	Pin	Signal
GND	1	47	GND	V_{CC}	92	46	V_{CC}
ADA_0	2	48	ADB_0	DI_0	91	45	DO_0
ADA_1	3	49	ADB_1	DI_1	90	44	DO_1
ADA_2	4	50	ADB_2	DI_2	89	43	DO_2
ADA_3	5	51	ADB_3	DI_3	88	42	DO_3
ADA_4	6	52	ADB_4	DI_4	87	41	DO_4
ADA_5	7	53	ADB_5	DI_5	86	40	DO_5
ADA_6	8	54	ADB_6	DI_6	85	39	DO_6
ADA_7	9	55	ADB_7	DI_7	84	38	DO_7
ADA_8	10	56	ADB_8	DI_8	83	37	DO_8
ADA_9	11	57	ADB_9	DI_9	82	36	DO_9
ADA_{10}	12	58	ADB_{10}	GND	81	35	GND
ADA_{11}	13	59	ADB_{11}	DI_{10}	80	34	DO_{10}
ADA_{12}	14	60	ADB_{12}	DI_{11}	79	33	DO_{11}
ADA_{13}	15	61	ADB_{13}	DI_{12}	78	32	DO_{12}
$\underline{CKI_1}$	16	62	$\underline{CKI_2}$	DI_{13}	77	31	DO_{13}
$\overline{CKO}_1$	17	63	$\overline{CKO}_2$	DI_{14}	76	30	DO_{14}
OE_1	18	64	OE_2	DI_{15}	75	29	DO_{15}
S_1	19	65	S_2	DI_{16}	74	28	DO_{16}
ACK_1	20	66	ACK_2	DI_{17}	73	27	DO_{17}
$\overline{CE}_1$	21	67	$\overline{CE}_2$	DI_{18}	72	26	DO_{18}
$\overline{WE}_1$	22	68	$\overline{WE}_2$	DI_{19}	71	25	DO_{19}
V_{CC}	23	69	V_{CC}	GND	70	24	GND

PIN NAMES

$\overline{OE}_1$-$\overline{OE}_2$	Data Out Register Output Enable
ADA_0-ADA_{13}	Address Inputs
ADB_0-ADB_{13}	
DI_0-DI_{19}	Data Inputs
DO_0-DO_{19}	Data Outputs
CKI_1-CLI_2	Data In Register Clock Input (Active Rising Edge)
ACK_1-ACK_2	Address Clock Input (Active Rising Edge)
S_1-S_2	Address MUX Select Input
$\overline{WE}_1$-$\overline{WE}_2$	Write Enable
$\overline{CE}_1$-$\overline{CE}_2$	RAM Select
CKO_1-CKO_2	Data Out Register Clock Input (Active Rising Edge)

PACKAGE OUTLINE



Integrated Device Technology, Inc.

16K x 32 WRITABLE CONTROL STORE STATIC RAM MODULE

ADVANCE INFORMATION
IDT7M6032

FEATURES:

- 16K x 32 high-performance Writable Control Store (WCS)
- Serial Protocol Channel (SPC™)—reading, writing and interrogation
- 4 byte/wide output enables
- Separate chip select, write enable and output enable memory controls
- High fanout pipeline register
- Fully width expandable
- Designed for high-speed writable control store applications
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Compact 64-pin ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Military modules available with semiconductor components manufactured in compliance to MIL-STD-883, Class B

DESCRIPTION:

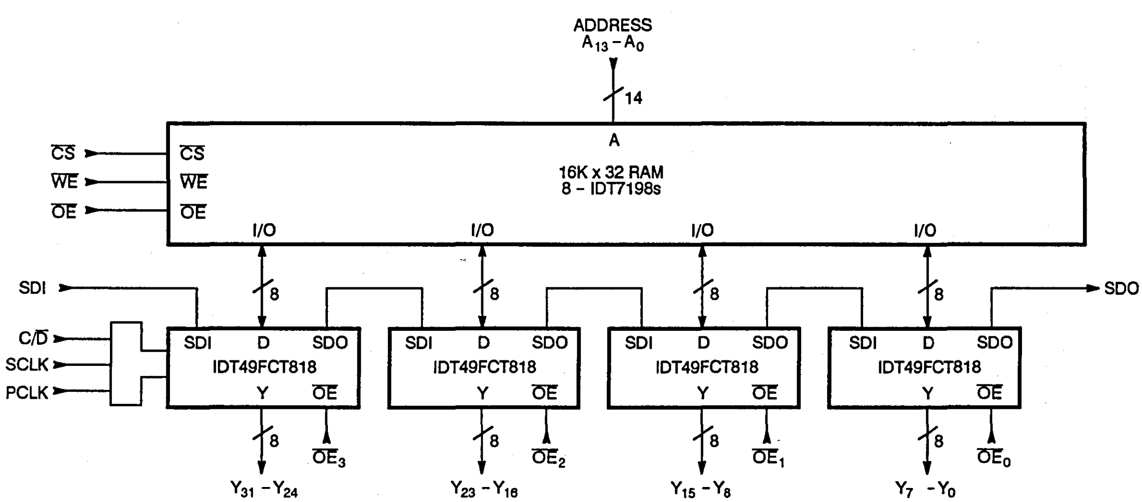
The IDT7M6032 is a 16K x 32-bit Writable Control Store (WCS) RAM and pipeline register. It features eight IDT7198 16K x 4 high-performance static RAMs and four IDT49FCT818 Serial Protocol Channel (SPC) registers. These devices are arranged to form the 16K x 32 Writable Control Store RAM with Serial Protocol Channel for loading of the memory. The address lines, chip select, write enable and output enable of the RAMs are all bused together to form one large 16K x 32 memory. Each eight outputs of the RAM are connected to the D inputs of an IDT49FCT818 in the normal fashion. The device has the serial data-in and serial data-output bits connected to form a 32-bit Serial Protocol Channel register. The module features four separate output enables, one for each of the IDT49FCT818 registers. Thus, the Y outputs from the IDT49FCT818 registers may be enabled or put into the high-impedance state on individual 8-bit boundaries. The Command/Data (C/$\overline{D}$), Serial Shift Clock (SCLK) and Parallel Clock (PCLK) are all bus organized across the four IDT49FCT818 registers. The thirty-two register output bits, eight from each device, are separately brought out to form a 32-bit wide pipeline register on the Writable Control Store.

In normal operation, data from the 32-bit wide memory is loaded into the IDT49FCT818 registers on the low-to-high transition of PCLK. Reading and writing of the memory by means of the Serial Protocol Channel is performed in the normal fashion using the IDT49FCT818. That is, the data to be loaded can be shifted in the serial data input by using the SCLK and a load command executed by shifting the proper command word in the serial data input when the C/$\overline{D}$ line is in the command mode. This command will then be executed by manipulating the C/$\overline{D}$ line and SCLK line in the desired fashion. Data is then written into the RAM by bringing the write enable line on the RAM memory from the high state to the low state and back to the high state.

The IDT7M6032 is offered in a compact 64-pin 600 mil wide ceramic dual in-line module. It is constructed using ceramic LCC components on a multilayer co-fired ceramic substrate and occupies less than 2 square inches of board space.

The semiconductor components used on all IDT military modules are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS and SPC are trademarks of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1987**

DSC-7030/-

PACKAGE OUTLINE

64–PIN DIP

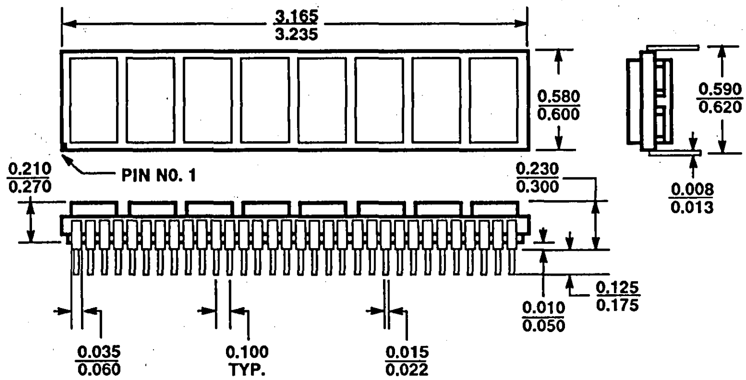


TABLE OF CONTENTS

CONTENTS **PAGE**

UNDERSTANDING THE IDT7201/7202 FIFO

APPLICATION NOTE AN-01

By Michael J. Miller

INTRODUCTION

This article discusses several different types of FIFO queues, their implementation, their performance and their use. Data, or information in computers, is processed as words or bytes in a predominantly serial fashion. There are producers and consumers of information that are connected by busses. Often there is a mismatch in the rate at which data is produced and the rate at which it can be accepted. The data is therefore buffered in serial lists until it can be used. The serial lists are stored in memory and require overhead to maintain them. These First-In-First-Out (FIFO) structures can be implemented at many levels from all software to all hardware. The software implementations are often the most flexible but yield the lowest performance. The hardware implementations, while less flexible, give the highest performance.

QUEUES

The elements of any computer or controller can be divided into three categories in relation to information: transformation, storage and transfer. Logic gates transform and combine information, memory elements store information and wires transfer information between the other elements.

Memory can be viewed as an element which transfers information with respect to time. The simplest of memory elements are latches and registers. RAMs are dense arrays of latches. While RAMs allow for dense information storage, they require an address to access individual pieces of information in the array. Therefore, addresses (information) must be generated and stored in order to access the desired information. The addresses are stored in programs and data structures such as linked lists.

Queues are a special organization of dense arrays of latches. Queues are a linear organization of groups of latches. Access to the linear string is restricted to either end. While RAMs allow for random access of any data in the array at any point in time, they require address inputs. Queues on the other hand, don't have an address thus avoiding the address generation and storage overhead. Queues can be divided into two categories: FIFOs and LIFOs.

Queues can be observed in the world about us. FIFO is an acronym for "First-In-First-Out". They can be observed in a bank line-up where customers enter at the end of a line and, after some wait, are serviced at the other end. The FIFO queue provides a mechanism by which customers, which arrive at an erratic rate, can wait until a teller can accommodate them.

LIFO is an acronym for "Last-In-First-Out". We can observe this phenomenon in the work place. As a person is working at a desk, interrupts occur. A higher priority interrupt such as a phone call or a request from people higher in management will cause the person to drop the work on the desk and start a new task. When the higher priority task is accomplished, the interrupted task on the desk is resumed. Depending on how many interrupts of sequentially higher priority tasks come in during the day, the stack of tasks on the desk grows. Another time honored example is the stacks of trays at the cafeteria. As trays are washed they are placed on a spring loaded elevator which sinks down to accommodate the new trays. When new customers enter the food line, trays are removed from the stack.

As can be seen in the above examples, queues are used to buffer between the flows of consumers and distributors of services. Groups of computing elements can be divided into consumers and producers of information with rates that must be matched. For example, a rotating Winchester disk is a source of information that must be serviced at a rate that may not be easily matched by the CPU which is consuming the information through the use of a data bus.

SIMPLE FIFO

The implementation of FIFOs is varied and presents many trade-offs. The simplest design treats the FIFO as a fixed number of memory elements in a linear array. When data is written (pushed) in at one end, all of the rest of the elements shift their data over to their neighbor at the same time. One can visualize (Figure 1) the structure as a shift register. The same structure can be implemented in software where the program manages an array of memory locations in RAM. To push data into the queue the program must first start by moving the contents of the next to the last location into the last location. The algorithm continues from the last to the first location. When all of the data has been rippled down, the first location in the queue will be vacated. The data to be pushed into the queue is written into that vacated location.

An improvement in the software solution could be made with the introduction of a pointer. A pointer is a variable which contains an address. The pointer would identify a location from which to read the output of the FIFO. When a new piece of

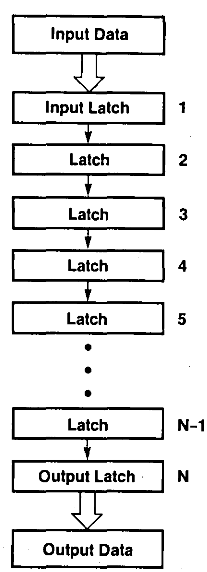


Figure 1. Hardware implementation of a fixed length FIFO.

14

 Printed in U.S.A.

information is written, it would go into the location identified by the pointer after which the pointer would be incremented. The pointer now points at the new output data. When the pointer reaches the end of the array, the next increment would be replaced by setting the pointer to the beginning of the array. The obvious advantage is that the program does less work and therefore is faster. This software technique is called a circular queue with one pointer. (See Figure 2.)

FIXED LENGTH FIFO: NO FALL-THROUGH

The FIFO described previously is called a Fixed Length FIFO and has the characteristic that it takes N cycles for a piece of information that was placed into it to emerge out of it. The number N is the number of locations in the FIFO. This implementation also has the characteristic that, when first started after power up, it will produce unknown data for N cycles until the first valid data arrives at the output. The latency is therefore N read/write cycles. The fixed length FIFO does not allow for differences between the rate of input and output rates. This type of FIFO is used where the arrival of data at the output is delayed to match parallel paths in a pipelined system.

VARIABLE LENGTH FIFO

The variable length FIFO solves the rate mismatch problem but requires more overhead to implement. Where the fixed length FIFO is like a steel pipe which information is fed through and has a fixed number of locations, the variable length FIFO is like a rubber hose that can stretch, holding from one to many items. The items are removed at will instead of being required to at write time. Every variable length system has a limit and therefore must signal when it is at capacity and must be serviced before bursting.

FALL-THROUGH FIFOs

In the real world of silicon and aluminum there is no such thing as rubber. Variable length FIFOs must therefore be implemented using fixed length queues. This fact creates some limitations which translate into trade-offs. The traditional hardware implementation uses two sets of shift registers. One set is used to hold the data in much the same way as in the fixed length FIFO. Data that is placed in the top emerges at the bottom. There is a second shift register that functions in parallel. The second shift register contains flags that indicate whether the associated data element at the same chronological position in the data queue is valid data or not. When data is written into the top location of the data queue, a true flag is placed into the "valid bit" queue. The variable length quality is achieved by allowing the data and its associated valid bit to "sink down" into the next location below it if there is no valid data in that location (see Figure 3). In this way valid data "sinks" to the bottom of the queue and stacks up in much the same way as pearls being dropped into a narrow tube filled with oil. The clocking of data down through the queue is controlled by an internal self-generated clock. The maximum latency or fall-through time is a product of the number of cells in the queue and the internal clock cycle length. This approach meets the requirement that differing rates may be accommodated. The valid bit data is brought out in parallel with the queue data. The valid bit data tells the consumer when valid data is present, thus avoiding the start-up period of invalid data as in the previous implementation of the fixed length FIFO. Examples of this approach are the shorter FIFOs such as the MMI 67401. Fall-through FIFOs tend to have very long undesirable fall-through times if the FIFO is deep.

The software approach could be designed to mirror the typical hardware approach by working with two arrays. One for the data and one of the valid bits. That approach uses too much memory. An alternate could use a wider array which carried the valid bit with the data. The algorithm would then start at the end of the array and pass to the front, advancing all elements which were valid to the end of the array until all valid data was collected at the end of the array. This approach would be very costly in terms of CPU cycles for what is achieved. There is a fall-through latency which is a product of the time to execute the updated software loop times the number of locations in the queue.

TWO-POINTER FIFO

A more economical approach would utilize two pointers and one array that was as wide as the data. One pointer would point to

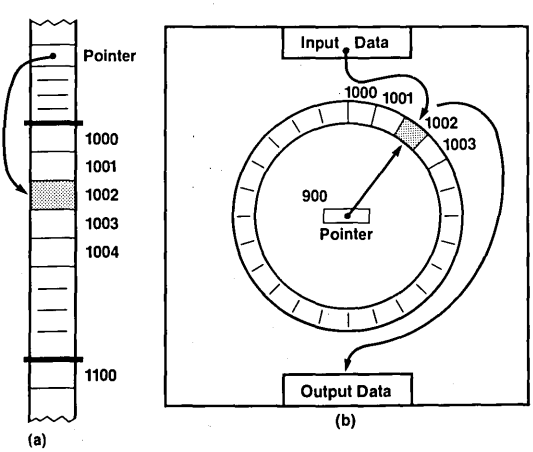


Figure 2. Circular queue with one pointer
a) As it is in memory.
b) Logical view.

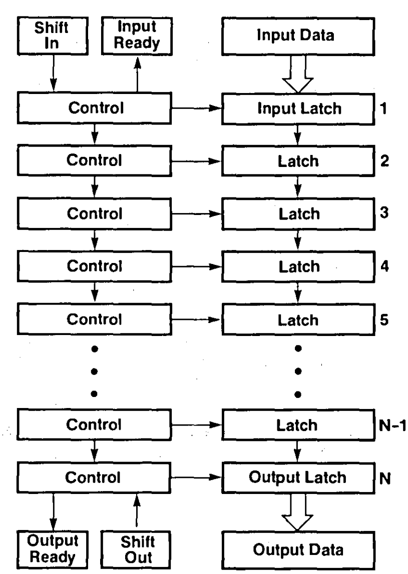


Figure 3. Classical FIFO architecture.

the location at which new data is written into. The second pointer identifies where data is to be read from for output from the queue (see Figure 4). When either pointer is used to access a location, it is incremented. When a pointer is incremented to the last location in the array, the next increment will be substituted with a reset of the pointer to the beginning of the array. The logical view of this structure is a circular queue with a read and a write pointer. This approach results in a much shorter fall-through time while still achieving the variable length feature. The fall-through time is the time that it takes to invoke the software to write the data into the queue, plus the time that it takes to invoke the software to read

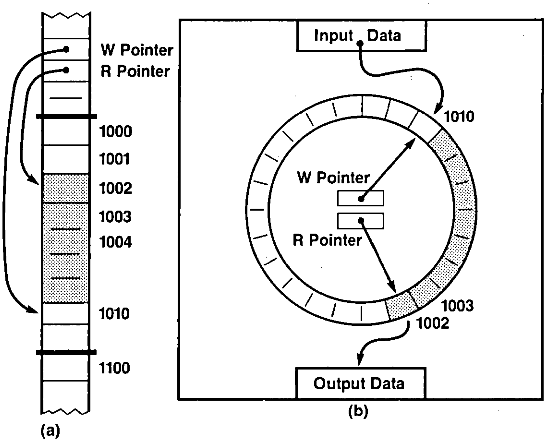


Figure 4. Circular queue with two pointers
a) As it is in memory.
b) Logical view.

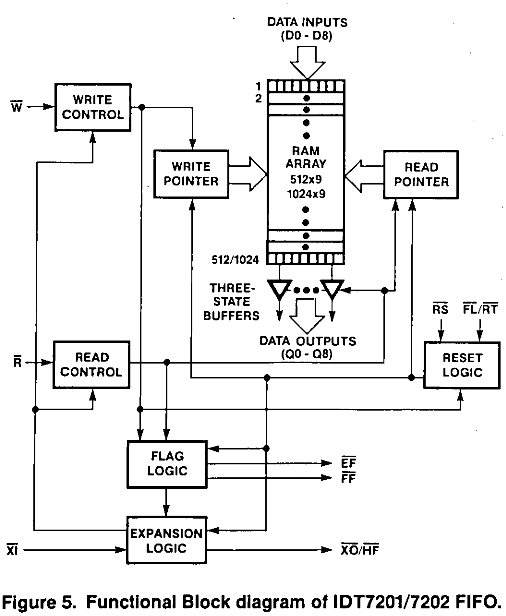


Figure 5. Functional Block diagram of IDT7201/7202 FIFO.

the data out of the queue. While this is much better than the previous approach, it still requires a reasonable amount of time to accomplish.

TODAY'S HIGH SPEED FIFOs

The hardware approach, which is used by the IDT7201 and IDT7202 devices, utilizes the software concepts demonstrated in the previous approach but at very fast hardware speeds (50ns typical military). The block diagram in Figure 5 shows the two pointers which locate where reading and writing is to take place in the queue (RAM Array). There is added logic which provides status about the queue: empty ($\overline{EF}$), half full ($\overline{HF}$) and full ($\overline{FF}$) ($\overline{\ }$ means an active LOW signal). Two pins, one input ($\overline{XI}$) and one output ($\overline{XO}$), provide for unlimited expansion while still maintaining the 50ns fall-through time. This part functions identically to the software approach utilizing the two pointers. When either pointer reaches the last location, it is reset to the first location thus achieving a circular queue via a wraparound approach. The status flags reflect the count of how many valid pieces of data are in the queue. After the device is reset, the empty flag ($\overline{EF}$) is asserted. As soon as a datum is written into the queue, the empty flag is deasserted. The empty flag is not asserted again until all pieces of data have been read from the queue. When the count of data elements reaches one-half the number of locations in the RAM array, the half full flag ($\overline{HF}$) is asserted. If a read is performed which reduces the count to just below the half way count, then the ($\overline{HF}$) is deactivated. The full flag is asserted when the count of data elements is exactly equal to the number of locations in the RAM array, thus flagging that there are no more empty locations in the queue.

WIDER FIFOs

Applications may vary widely as to the width and depth of the FIFO required. If an application's maximum requirement is 1024 locations or less and 9 bits in width or less, then the IDT7202 will fit. Wider word widths can be achieved by connecting two or more devices in parallel (control signals). The status flags can be detected from any one device because each device is working in lock step parallel. Figure 6 shows an example of an 18 bit-word composed of two IDT7201/7202 devices. The older classical architecture would require more external circuitry to match the Input Ready and Output Ready signals to account for differences in the internal self-generated clock frequencies. RAM-based FIFOs, such as the IDT7201/7202, do not have this problem.

DEEPER FIFOs

Some applications require deeper FIFOs. In the older architecture, deeper FIFOs mean longer fall-through times because they are connected end to end. The time increases in direct proportion to the number of devices. For example two devices yield a maximum fall-through time of twice that of one device. This can make some applications of FIFOs impractical or totally unusable.

With the two pointer approach used in the IDT7201/7202, the data input busses are connected together and the data output busses are common. This produces a parallel architecture (see Figure 7) as opposed to the serial approach above. The parallel structure is analogous to cascading standard RAM devices to achieve deeper memories.

Since FIFOs do not have chip selects and external decoding mechanisms, the task of choosing which device is selected must be provided for internally. The control (in the IDT7201/7202) is achieved through a unique serial structure. The first (or master)

FIFO is identified by grounding the $\overline{FL}$ input. All other FIFOs in the structure must have the $\overline{FL}$ input pulled up to V_{CC}. The $\overline{XO}$ output of the first FIFO is connected to the $\overline{XI}$ input on the next FIFO in the queue. The $\overline{XO}$ output of that FIFO is connected to the $\overline{XI}$ input of the next and so on until the $\overline{XO}$ output of the last FIFO is connected to the $\overline{XI}$ input of the first FIFO (see Figure 7).

After reset, the active read and write pointers are in the first device. When the write pointer has progressed to the end of the first FIFO device, it outputs a pulse on $\overline{XO}$ which activates the write pointer at the beginning of the next device and simultaneously deactivates the write pointer in the first device. Thus, write enable control is passed to the second device. When the

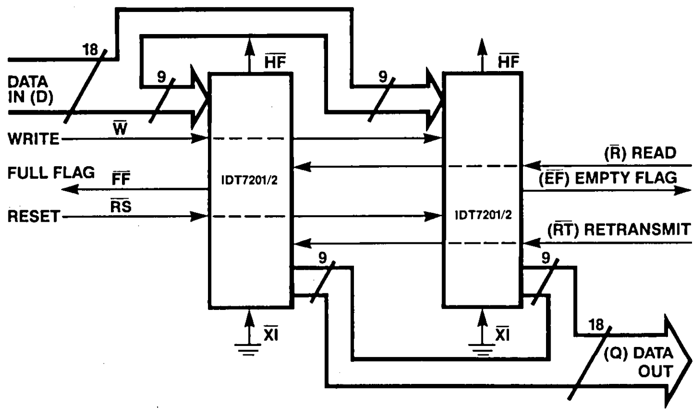


Figure 6. IDT7201/7202 FIFO Word-Width Expansion.

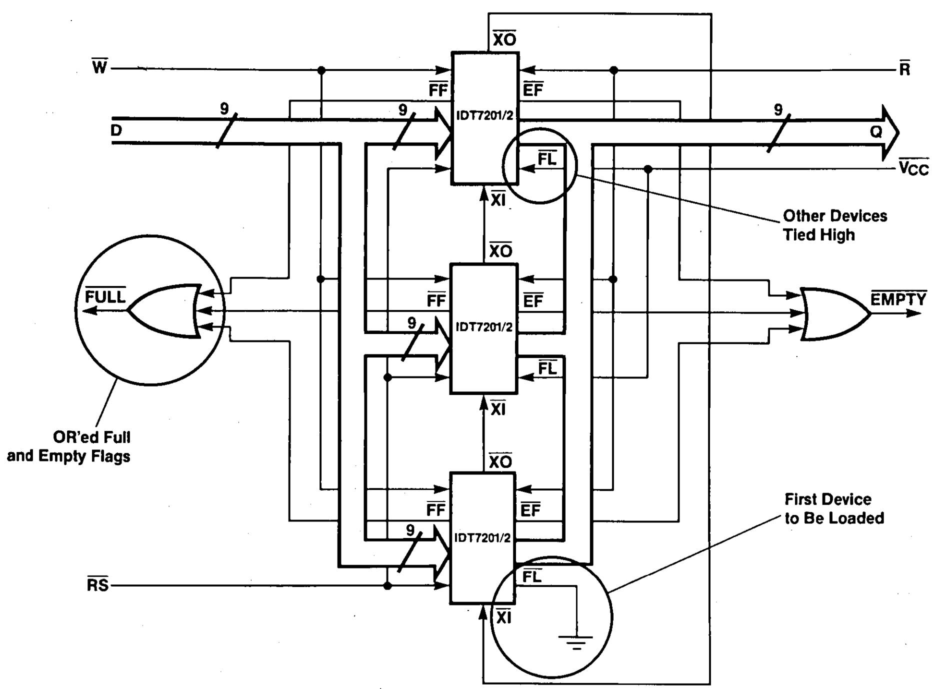


Figure 7. IDT7201/7202 FIFO Word-Depth Expansion.

active read pointer reaches the end of the first device, it terminates and activates the read pointer in the next device with another pulse on the $\overline{XO}$ output of the first device. Figure 8 shows the progression of read and write pointers across two devices. In this ring structure, the read pointer is always chasing the write pointer. The pointer enable crosses the device boundaries via sending an $\overline{XO}$ pulse onto the next device. This continues in a circular queue fashion.

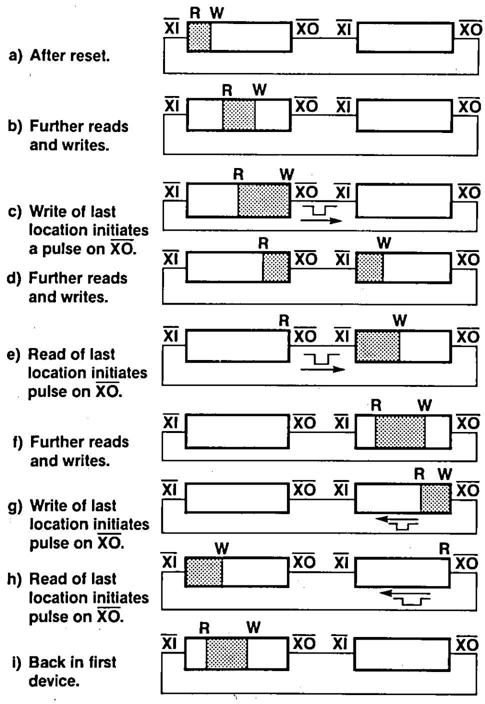


Figure 8. Example on $\overline{XO}/\overline{XI}$ expansion scheme.

The IDT7201/7202 has been designed such that the read and write pointer can never cross over each other even in the cascade mode. The $\overline{XO}$ pulse is synchronous with read and write. When the last location is read or written, the $\overline{XO}$ output goes low with the read or write enable input and back high with the read or write enable. To see why there is no conflict even though reads and writes are asynchronous, the usage must be examined. The case of concern is when the FIFO is empty and the read and write pointers are at the last location. It must be realized that the consumer will not read until the empty flag is deasserted. The empty flag output will go high after the write pulse has gone high again thus ensuring that the $\overline{XO}$ pulse, indicating the write pointer, has been passed on to the next device. The consumer will then read the last location causing another pulse on $\overline{XO}$ which will transfer the read pointer (see Figure 9).

There is one special case regarding read flow-through mode (discussed below). In this mode the consumer can anticipate the write, by producer, by lowering the read enable input. In this case the $\overline{XO}$ input does not go low with read enable. When write enable is lowered, $\overline{XO}$ goes low. $\overline{XO}$ goes high with write enable. At this point the empty flag is cleared, thus signaling to the consumer to terminate the read after the appropriate period specified in the data sheet. During this period the $\overline{XO}$ output, which went high at the end of the write enable pulse, has lowered again. When the read enable is raised by the consumer, the $\overline{XO}$ output goes high. In this way two pulses on $\overline{XO}$ are assured (see Figure 9).

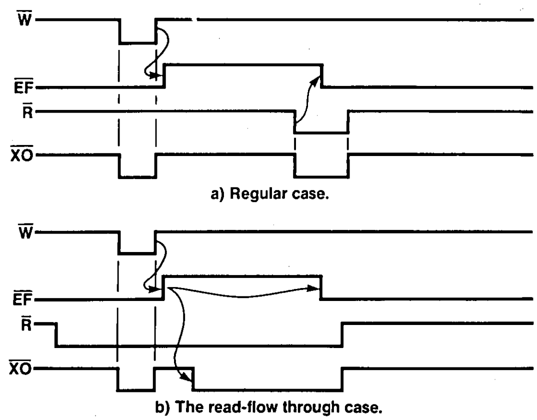


Figure 9. Generation on XO output when the FIFO is empty. a) Regular case. b) The read-flow through case.

Two examples of the IDT7201/7202 in expanded depth configuration are available from IDT commercially. The IDT7M203/204 are Subsystems modules which incorporate onto one ceramic substrate four FIFO LCCs and the $\overline{EF}$ & $\overline{FF}$ "OR" gating to produce 2Kx9 and 4Kx9 FIFOs. The Subsystem module has a lead frame which pins out like the 28-pin 0.6 inch IDT7201/7202. This allows for a plug compatible 4Kx9 FIFO in one socket.

SPECIAL FEATURES OF IDT7201/7202

The architecture used in the IDT7201/7202 provides some features that distinguish it from FIFOs with other architectures. One outstanding feature is the dual port implementation of the RAM array. The RAM is designed in such a way that the read and write ports are separate, allowing for simultaneous asynchronous reads and writes with no hand shaking or arbitration. In the classical architecture the consumer and producer circuits must monitor ready flags for each access.

The IDT7201/7202 support a retransmit function. In the single device solution, the $\overline{FL}/\overline{RT}$ input may be pulsed low signaling a retransmit.

A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 512/1024 writes are performed between resets. The retransmit feature is not compatible with Depth Expansion Mode and will affect HALF FULL FLAG ($\overline{HF}$) depending on the relative locations of the read and write pointers. For example in a communications application, during transmission of a message, the receiver may request a retransmit of the message. This can be accomplished by always starting new messages at the beginning of the queue via a pulse on the reset input. If and when the retransmit request arrives, the $\overline{FL}/\overline{RT}$ line is pulsed. The read pointer is repositioned at the beginning of the queue. The message producer may continue to write more of the same message into the queue as the retransmit

14

of the message continues. The retransmit can happen as many times as desired. At the start of the next complete message, the reset line ($\overline{RS}$) must be pulsed after the successful acknowledge by the receiver. The reset ensures that the new message will be placed in the FIFO at the start of internal queue. It should be noted that, when retransmit is possible, messages cannot be bigger than the maximum size of the queue. If the message is longer than the queue, even though the read pointer has progressed far enough to accommodate the extra data, resetting the read pointer back to the beginning with retransmit will produce data from the end of message instead of the beginning.

This architecture supports flow-through modes. In the read flow-through mode, when the buffer is empty, the consumer can anticipate the write, by the producer at the other end, by lowering the read input. When the empty flag ($\overline{EF}$) goes false, the consumer circuitry can terminate the early read cycle by reading the data and deasserting the read signal. The read input must go high for a brief period in order to clock the read pointer. The read flow-through mode avoids the standard sequence of monitoring flag going high before hitting a read cycle.

The write flow-through mode is a mode that is employed when the FIFO is full. The producer can anticipate a read by the consumer by lowering the write input before the read. When the full flag ($\overline{FF}$) raises, the producer knows that the consumer has read a location, thus freeing up a location that can receive the new data. The producer then raises the write input which actually writes the data into the RAM array. This flow-through mode avoids the overhead of monitoring the full flag before initiating a write cycle.

The IDT7201 is pin and functionally compatible with the Mostek MK4501, thus serving as an alternate source. The IDT7202 gives the same functionality as the IDT7201 but is twice as deep (1024x9). The IDT7202 is the largest FIFO made with the zero fall-through time architecture making it the logical choice for FIFO applications.

SOFTWARE VERSUS HARDWARE SOLUTIONS

With every application involving a computer or programmed controller, the designer can trade off between performing certain functions in software or hardware. In general, the software solution is a more flexible design (easily changed) but performs the task more slowly. The hardware solution is less flexible but performs the task very fast.

To clarify these concepts, a discussion of an application and how it could be solved at the various levels from software to hardware is beneficial. A good example is a file server. The server could be connected to a Local Area Network (LAN) and, on the other side, to a Winchester disk drive. Both I/O connections demand attention at unpredictable intervals and must be serviced on demand or data is lost.

If the data rate of both interfaces is sufficiently low, a total software solution might be considered. The data rate would have to be low enough such that the software code could poll the status of either I/O port. As data arrives it could be placed into software FIFO queues. When a full record is buffered, then processing would commence. During the processing, the I/O ports must still be monitored as another user on the LAN might make a request (see Figure 10). It is doubtful that a total software solution could be designed for the server application that would have acceptable system performance.

The next approach to consider might be to include hardware interrupts. Interrupts allow for one task to be running and almost immediately switching to an I/O service routine. Interrupts are something like a hardware subroutine call. This scheme would use the interrupt mechanism to call routines to move data to and from the I/O ports and the software FIFO queues. The overhead of constantly polling the I/O port status flags would be eliminated, thus allowing for higher system performance. An asynchronous-type problem is introduced with interrupts. To use interrupts properly, the I/O service routines may be called at any instance. Therefore, the interrupt routines must be designed in such a way that they do not destroy data that the interrupted task might be using. Usually, the routines must be careful to save the state of the machine, perform their task and restore the state of the machine. The extra code to maintain the state of the machine is an overhead that is not in the polled solution. Worse yet, saving the state of the machine may be too much overhead to allow for an interrupt during a time-critical piece of code. Because interrupts may not be acceptable at certain points in the code, the programmer must insert code to disable and re-enable interrupts around the critical sections.

Where the polling scheme provides a solution which has a more easily definable sequence of execution, the interrupt solution is indefinite. The programmer must spend a lot more time proving that all possible sequences caused by random interrupts will produce desirable results. Because interrupts may not be acceptable at certain points in the code, the programmer must insert code to disable and re-enable interrupts around the critical sections. The interrupt disable solution not only cuts performance by not accepting I/O during some periods, but also adds more overhead with the maintenance of the interrupt enable mechanism. In some sense, interrupts can be to software what the meta-stable flip-flop problem is to hardware.

The interrupt solution can be moved out of the software and more into the hardware realm through the use of a technique called Direct Memory Access (DMA). The DMA solution is provided by a block of circuitry which monitors the I/O ports. When the port requires attention, the DMA logic interrupts the current task at the bus transfer level and steals a memory cycle to transfer the data to or from the port and the FIFO queue in memory. The task that is running on the processor misses only a few memory cycles now and again which is much less than in the interrupt scheme where a whole subroutine of many memory cycles was executed to transfer each element of data. The DMA solution is not for free. DMA controllers are complex devices which must be programmed as well as designed into the bus structure. The DMA mechanism can only serve one source at any given instance in time thus still being a bottleneck in throughput.

So far, each solution proposed has moved the mechanism that feeds data to or from FIFOs in program memory away from the software and closer to the I/O port. The memory bus still remains the bottleneck because both FIFO queues are in memory. To simplify and improve performance, hardware FIFOs such as the IDT7201/7202 can be used. The processor would interface to the FIFO through an I/O port as before, but the FIFO would now be between the I/O port and the rest of the hardware. The software could then service the data at a steady rate and be sure that data was not lost without the problems or overhead of more complicated schemes such as interrupts or DMA.

Because the queues are between the controller and the peripheral, the peripheral can load or read the queue without interrupting the controller. Since the controller is not involved with maintaining both queues, there is no possibility of lost data because one queue was being serviced while data for the other queue arrived. For these reasons the hardware FIFO represents the highest performance solution.

If the designer uses large FIFOs like the IDT7202, there is a minimum of device count. Assuming 2 FIFOs (transmit and receive) for each I/O port gives a count of four 28-pin devices for the FIFO solution. The DMA solution would at least be one 40-pin device and several bus buffer/control devices. The interrupt solution would require a similar parts count to the DMA solution. Therefore, the FIFO solution is not only the highest performance solution but usually has the lowest part count of the hardware solutions.

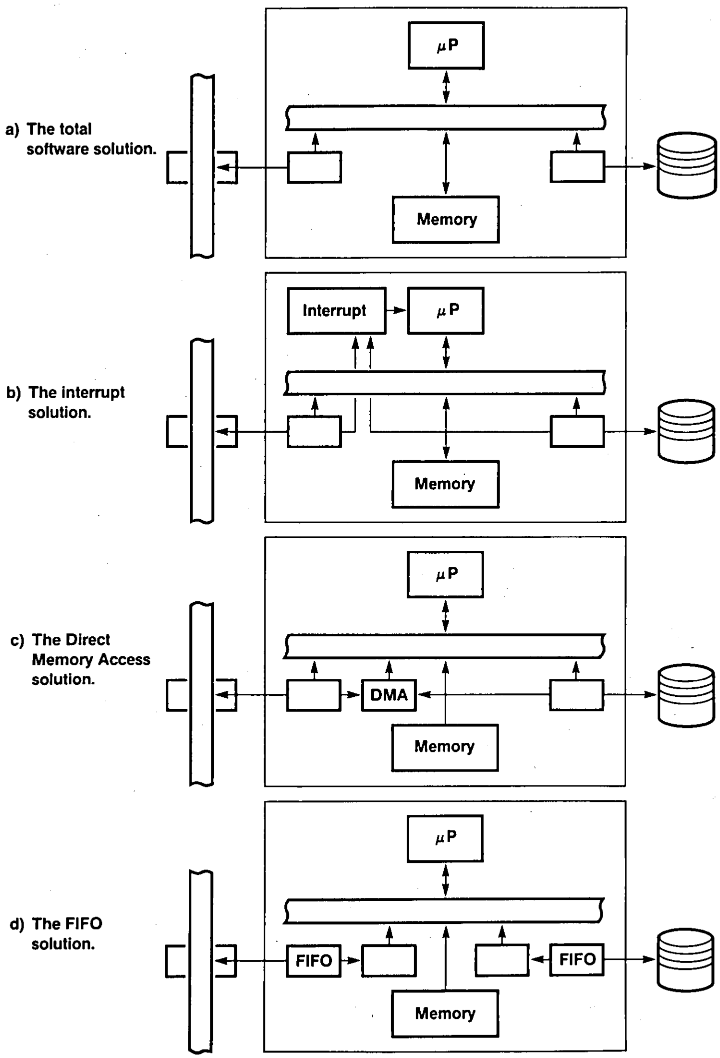


Figure 10. Example solutions for File Servers.

COMMUNICATIONS-MULTIPLEXOR APPLICATION

Another example of a rate mismatch problem is shown in a CRT terminal and CPU interface. In order to not load the CPU with the burden of monitoring the UARTs of multiple CRTs and printers, a communications controller is employed. The controller can serve as a communications multiplexor and data concentrator (see Figure 11).

As the controller receives characters it must buffer them such that if multiple characters are received close together from several terminals, they will not be lost as more characters come in. The natural structure to store them in is a queue of the FIFO type. The CPU will then need to respond to the characters. If the controller is inputing other characters, the CPU should not have to wait until the controller is done. Therefore, a FIFO can be employed on the transmit side as well as the receive side. To make the design simple, two sets of FIFOs could be placed between the CPU and controller. When characters are received they are placed in one end of a FIFO and read from the other end by the CPU. As the CPU prepares characters for transmission, it places them in a FIFO going the other direction. The controller then reads them from the other end of the transmit FIFO and sends them out through the UART.

Conceivably, there could be a pair of FIFOs for each UART. That way it would be easy for both the controller and the CPU to keep straight which characters correspond with which UART. While this provides for a large total of buffer space for characters, it is more than needed when using a part like the IDT7201/7202. For eight UARTs, this scheme would require a minimum of sixteen FIFO devices. A better solution would be to use one FIFO device in either direction. If an IDT7202 were used, it could provide a maximum of up to 128 characters per UART if all the UARTs input at the same time and rate. While the two FIFO techniques would most likely provide plenty of buffering at a minimal device count, it presents the problem of which character belongs to which UART. The solution is to make a wider FIFO which is 18 bits wide; thus using 4 devices instead of 16 devices for 8 UARTs. This would allow for a UART number to be placed in the FIFO along side each character. The remainder of the word could be used for flag, status and command information between the CPU and the controller. For example, several of the bits in the FIFO word could indicate whether the character information was a character to send or BAUD change rate information.

The empty and full flags of the IDT7201/7202 FIFO would be used as status flags. For example, the transmit buffer must be monitored from both sides. As the CPU prepares a character to transmit, it would first examine the full flag ($\overline{FF}$) to see if the FIFO is full. If the FIFO was full, it would delay outputting the character. If the buffer is not full then it would place the character in the FIFO. The empty flag ($\overline{EF}$) would be monitored by the controller. As soon as the CPU places a character into an empty FIFO, the empty flag would change to not true. At this point the controller would know there was a character in the buffer which could be transmitted. The controller would read characters from the buffer as long as the empty flag was not true (buffer contains more than one character).

CONCLUSION

Hardware FIFOs are an economical memory organization to use when lists of data items are to be buffered. Because they do not require an address to access items in the list, there is less overhead in terms of circuitry and access time. The FIFO buffer is most often used as a "system rubber band" to stretch between the differing and fluctuating rates of different elements in a system. The IDT7201/7202 FIFO device features the newest RAM-based architecture and provides the latest in technology in terms of access time, fall-through time and size, thus providing the most economical solution for today's design needs.

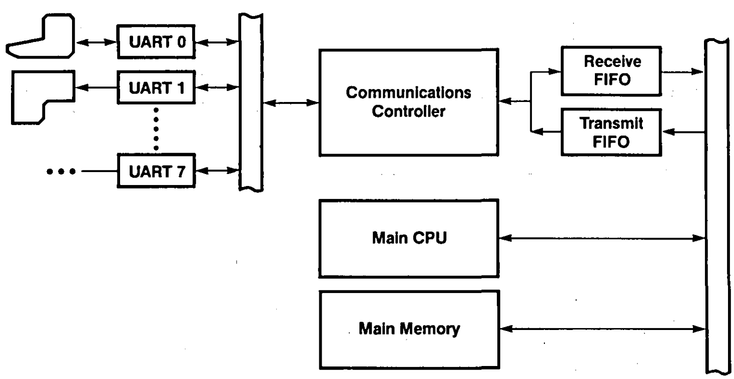


Figure 11. Communications Controller example.

Integrated Device Technology, Inc.

DUAL-PORT RAMS SIMPLIFY COMMUNICATION IN COMPUTER SYSTEMS

APPLICATION NOTE AN-02

By David C. Wyland

INTRODUCTION

Dual-port RAMs allow two independent devices to have simultaneous read and write access to the same memory. This allows the two devices to communicate with each other by passing data through the common memory. These devices might be a CPU and a disc controller or two CPUs working on different but related tasks. The dual-port memory approach is useful and popular because it allows the same memory to be used for both working storage and communication by both devices and avoids the need for any special data communication hardware between the devices. The latest development in dual-port RAMs has been the appearance of high speed dual-port RAM chips. These chips allow high speed access by both devices with the minimum amount of interference and delay. Integrated Device Technology offers a family of these devices as shown in Table 1.

Width	Size	Part	Support Logic				Comments
			Interrupt	Busy Logic		Semaphore	
				MASTER	SLAVE		
X8	1K	IDT7130	X	X			
		IDT7140	X		X		
	2K	IDT7132		X			
		IDT7142			X		
		IDT71321	X	X			52-pin
		IDT71421	X		X		52-pin
		IDT71322				X	
	4K	IDT7134					
		IDT71342				X	52-pin
X16	2K	IDT7133		X			
		IDT7143			X		

Table 1. Dual-Port RAMs Available from Integrated Device Technology

DUAL-PORT RAMS: SIMULTANEOUS ACCESS

A dual-port memory has two sets of address, data and read/write control signals, each of which access the same set of memory cells. This is shown in Figure 1. Each set of memory controls can independently and simultaneously access any word in the memory including the case where both sides are accessing the same memory location at the same time. Up to this time, there have been very few true dual-port memories available. Memories have a single set of controls for address, data and read/write logic and are single-port RAMs. If you wanted a dual-port RAM function, you had to design special logic to make the single-port RAM simulate a dual-port RAM in operation.

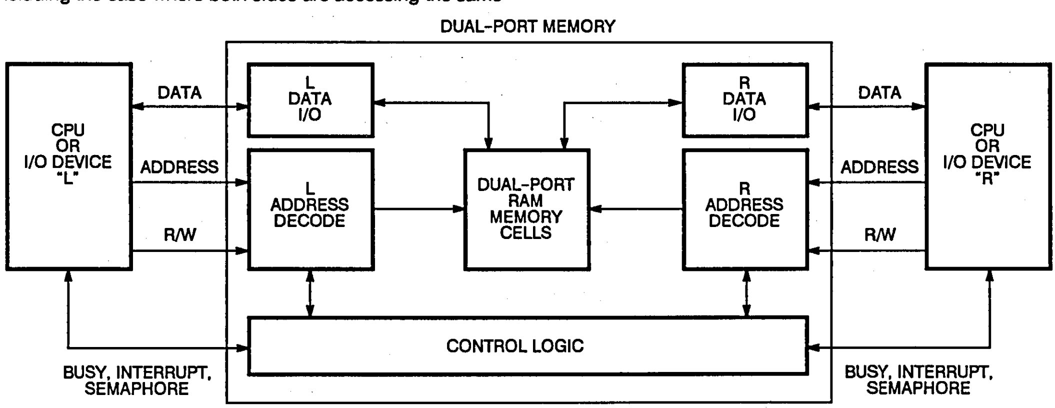


Figure 1. Dual-Port Memory Block Diagram

14

Printed in the U.S.A. Rev. 1-9/87

Direct Memory Access (DMA) as a Dual-Port Memory Simulation

The concept of using a conventional memory to simulate a dual-port RAM has been common in computer systems almost from the beginning. It is known under the name Direct Memory Access, or DMA. In the DMA concept, a single memory is shared between the CPU and one or more I/O devices as shown in Figure 2.

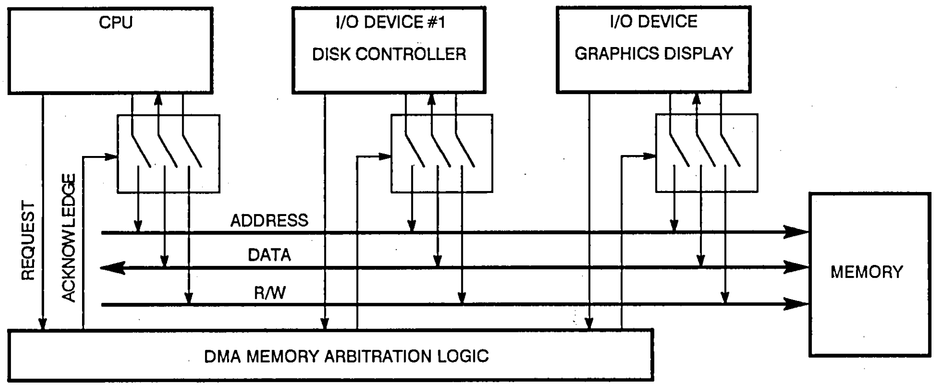


Figure 2. DMA Memory System Block Diagram

Each device wishing to use memory submits a request to the arbitration logic. The arbitration logic responds by connecting the memory address, data and control lines to one of the requesters and tells any other requesting devices to wait by issuing a busy signal. The busy signal causes the memory access logic in the device to wait until busy has gone away before performing a memory transfer.

DMA Limitations: Waiting for the Bus

In a computer system with DMA, the CPU must stop and wait while an I/O device is doing DMA transfers to memory. This works well in typical systems where the I/O devices are transferring data only a small percentage of the time and the impact on CPU processing time is minimal. These assumptions do not hold where you have two CPUs trying to use the same memory. In this case, one CPU must wait while the other uses the memory. As a result, the average speed of the CPUs will typically be cut in half.

There are two solutions to this problem: 1) You can provide local memory for both CPUs and limit use of the common memory to CPU/CPU communication only, in an attempt to reduce the time impact of DMA waiting, or 2) you can provide true hardware dual-port memory between the CPUs and all simultaneous high-speed access by both CPUs to the same memory without waiting. The introduction of high-speed dual-port RAM chips now makes the second option practical.

Dual-Port RAM Chips: How They Work

A true dual-port memory allows independent and simultaneous access of the same memory cells by both devices. This means two complete and independent sets of address, data and read/write logic and memory cells that are capable of being read and written by two different sources. An example of the dual-port memory cell is shown in Figure 3. In this cell both the left and right hand select lines can independently and simultaneously select the cell for read out. In addition, either side can write data into the cell independent of the other side. The only problem would be when both sides try to write into the same cell at the same time. We will discuss this in a moment.

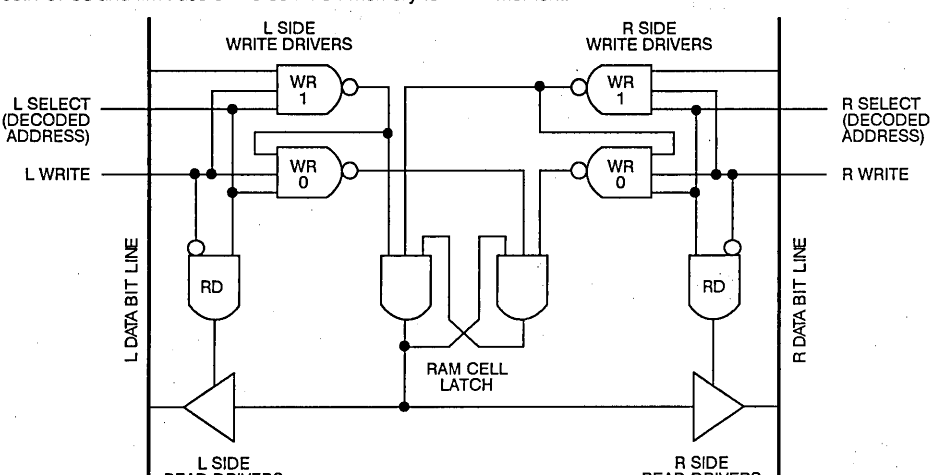


Figure 3. Dual-Port RAM Cell

DUAL-PORT RAM CONTROL LOGIC

Dual-port RAM chips include control logic to solve three common application problems: signaling between processors, timing interactions when both are using the same location and hardware support for temporary assignment (called allocation) of a block of memory to one side only.

Interrupt Logic For Signaling

A common problem in dual-processor systems is signaling between the processors. For example, processor A needs to signal processor B to request a task to be performed, as defined by data in the common memory. When processor B has completed the task, it needs to signal processor A that the task is done. Note that the signaling must occur in both directions. A common form of signaling is for one processor to cause an interrupt on the other processor. This allows the receiving processor to be informed of a communication without having to constantly check for it.

Hardware support for this signaling function is provided by interrupt logic, available on certain IDT dual-port RAM chips. A block diagram of this logic is shown in Figure 4. In these chips, the top two addresses of the memory chip also serve as interrupt generators for each of the ports. If the left side CPU writes into the even address of this pair (3FF in a 1K RAM) an interrupt latch is set and the interrupt line to the right hand port is activated. This interrupt latch is cleared when the right hand CPU reads from the even address. A similar set of logic is provided to allow the right hand CPU to interrupt the left hand one. This logic is associated with the odd address of the pair (3FE in a 1K memory). Providing this logic on chip saves the system designer from having to design in extra logic to allow one CPU to interrupt the other.

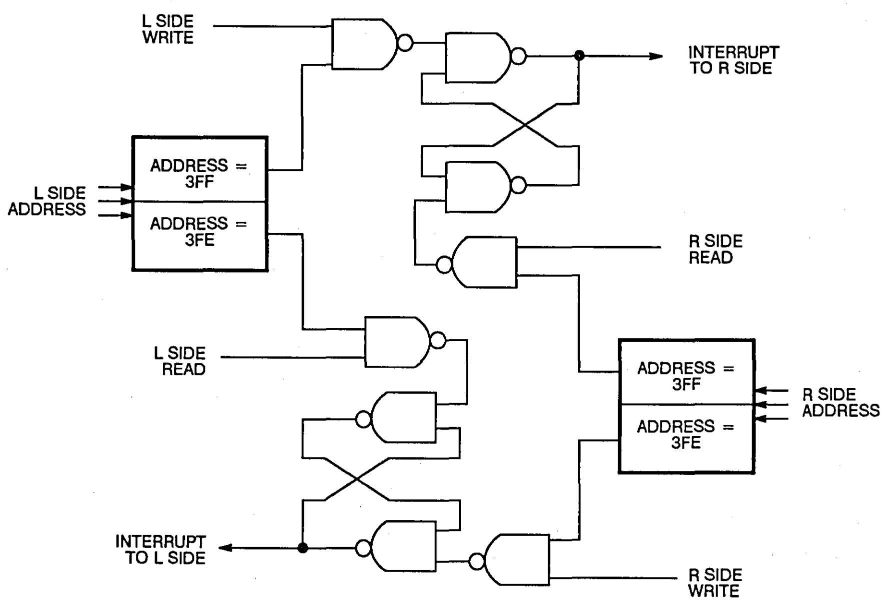


Figure 4. IDT7130 Interrupt Logic

Busy Logic Solves Interaction Problems

A problem can occur with dual-port memories when both ports attempt to access the same address at the same time. There are two significant cases: when one port is trying to read the same data that the other port is writing and when both ports attempt to write to the same word at the same time. If one port is reading while the other port is writing, the data on the read side will be changing during the read and a read error can be caused. If both ports attempt to write at the same time, the memory cell is being driven by both sides and the result can be a random combination of both data words rather than the data word from one side or the other. Busy logic solves this problem by detecting when both sides are using the same location at the same time and causing one side to wait until the other side is done.

Note that although one or the other processor may have to wait occasionally, the throughput loss is minimal, typically less than 0.1%. This is because the probability of both processors using the same location at the same time is small. For example, if there are a thousand words in memory with a relatively uniform and random access of these locations by either side, the probability of a given location being accessed by one side is of the order of one part of a thousand. The probability of both sides accessing the same location at the same time is, therefore, of the order of one part in a million. As a result, the average throughput of the system is reduced by only one part per million due to dual-port RAM access contention (again, assuming uniform random address access by both sides).

Busy Logic Design

Busy logic is called hardware address arbitration logic because it consists of hardware that decides which side will receive a busy signal if the addresses are equal. It consists of common address detection logic and a cross coupled arbitration latch. A logic diagram of the type of busy logic used in the IDT dual-port RAM chips is shown in Figure 5. The purpose of this logic is to provide a busy signal for the address that arrived last, to inhibit writing to the busy port and to make a decision in favor of one side or the other when both addresses arrive at the same time. This logic consists of a pair

14

of address comparators, a pair of delay buffers, a cross-coupled latch and a set of busy output drivers. The address comparator output goes true when the addresses at its inputs are equal.

In the logic shown in Figure 5, the ability to detect which address arrived last is provided by the time delay buffers between address lines and the comparators. If we assume that the L address is stable and the R address changes to match the L address, the R address comparator will go true immediately while the L address comparator will become active some time later as determined by the time delay gates.

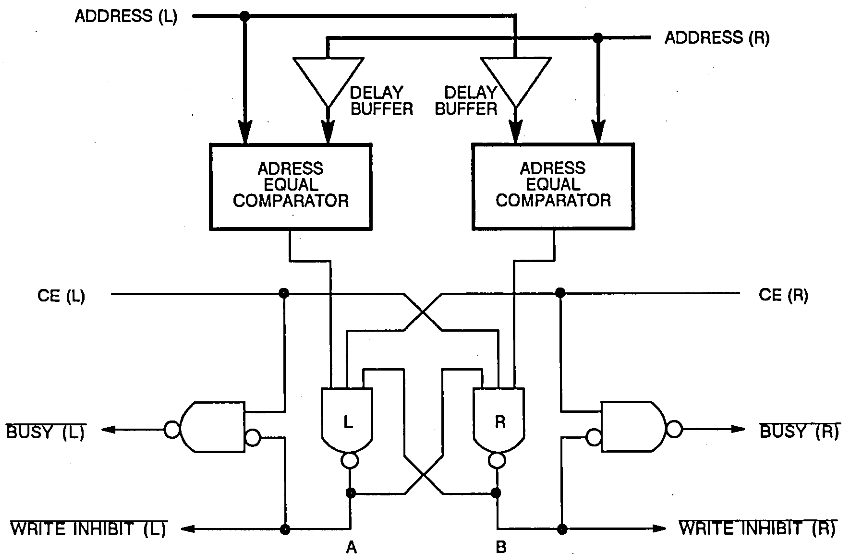


Figure 5. Dual-Port Busy Logic Design

The arbitration latch formed by the L and R gates reflects the address comparator output timing. This latch has three stable states, both latch outputs A and B high, A low/B high and A high/B low. Initially, both A and B are high because the outputs of both address comparators are low. We start with the L address stable and the R address arriving later. When the R comparator becomes active its output will go high and B will go low. The A output will remain high because its address comparator input will go high sometime later and the L gate input from B output will go low before this occurs. The result is that the R gate B output will be active inhibiting writing to the R side of the dual-port RAM and activating the busy signal to the R port.

The extreme case of busy logic decision making is when both addresses arrive at exactly the same time. In this case, the outputs of both address comparators go high at the same time activating both sides of the arbitration latch. The latch will settle into one of two states with either the A or the B latch output being active. The latch design ensures that a decision will be made in favor of one side or the other.

The chip enable lines come directly into the arbitration latch, although they could have been brought into the address comparators along with the other address lines. This is because if the chip enable for one side is inactive, both reading and writing for that side is automatically inhibited and/or arbitration is not needed. If the addresses are equal, the chip enable that arrives last will lose the arbitration. If both chip enables are active then arbitration will be determined by the settling of the address lines.

Temporary Assignment of Memory to One Side

A common problem in dual-port RAM application is the need to temporarily assign a block of memory to one side. For example, sometimes you need to update a data table as whole and you cannot allow the other processor to use the table until you are done. This is called block allocation of the memory.

Block allocation can also be used to avoid the address arbitration problem since it is a way of ensuring that both sides do not use the same address at the same time. This method is also called software arbitration because the software on both sides decides and agrees as to who has permission to use a given portion of the memory. Software allocation has the advantage of not requiring busy logic, which is useful in systems which cannot accommodate a busy signal.

The design problem with block allocation is communication of the assignments between the CPUs. A simple but time consuming method is to pass messages between the CPUs, perhaps aided by interrupt logic. In the message method, processor A requests use of a block from processor B. Processor B agrees and sends permission back to processor A. When A is finished it sends a release message to B which responds with a release acknowledge to A. In this system, four messages are sent for each block assigned and released.

Semaphore Logic Support for Memory Assignment

Although block allocation is a software technique, it can benefit from hardware support. In message passing allocation, four messages must be passed to assign and release a block of memory. Semaphore logic, available in certain IDT dual-port RAMs, can be used to eliminate this message passing and its associated overhead. Semaphore logic provides a set of flags especially designed for the block assignment function. Each flag is used as a token to indicate which CPU has permission to use a block of memory.

Each semaphore flag can be set to one side or the other but not both. This ensures that only one side has permission to use the block of memory.

The IDT semaphore logic bits are designed to be used in a set-and-test sequence. Each bit is normally in the logic one state, indicating that it is not assigned to either side. A processor, desiring to assign a bit and, therefore, its associated block of memory, attempts to write a zero into the bit. It then reads the bit to see if it was successful. If it was, the bit will read zero, and the processor has use of the block. If it reads a one, it was unsuccessful, and the block is in use by the other side. The processor must then wait until the bit becomes zero, indicating that the other side has released it.

Semaphore flags have a particular requirement: a given flag can be assigned to only one side at a time. Specifically, you must not have a situation where both sides simultaneously think they have permission to use a block. Semaphore logic is designed to resolve this problem. If both sides attempt to set a semaphore flag at exactly the same time, only one side sees it set.

Semaphore flags consist of eight individually addressable dual-port latches. Each latch can be read and written by either side. They are selected by a separate chip enable, addressed by the three last significant bits of the address lines and are read and written through the D_0 data bit. Except for sharing the address, data and read/write pins of the RAM, the semaphore latches are completely independent, as shown in Figure 6.

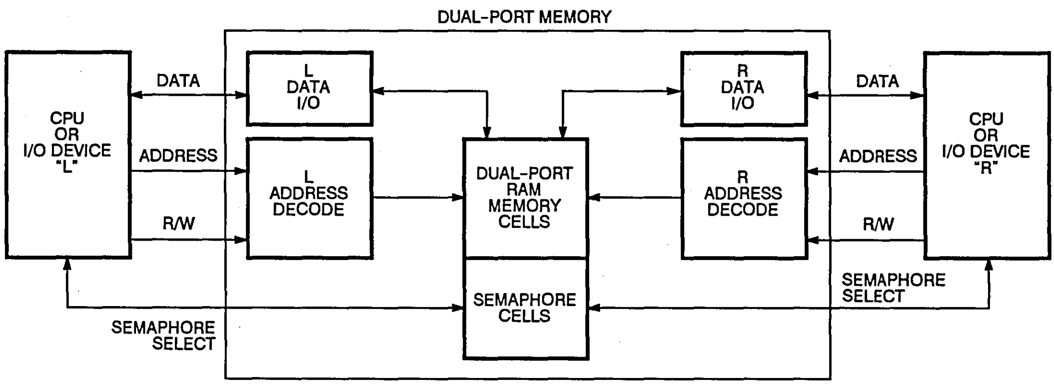


Figure 6. Dual-Port RAM Semaphore Logic

A logic diagram of a semaphore logic flag is shown in Figure 7. In this logic, both flip-flops are initially at logic one and both Grant outputs are high. If only one flip-flop is set to zero, its corresponding Grant output will go to zero. If the other flip-flop is set later, this will have no effect. If both flip-flops are set at the same time however, the latch will settle so that only one Grant output goes low, ensuring that only one side receives permission to use the resource.

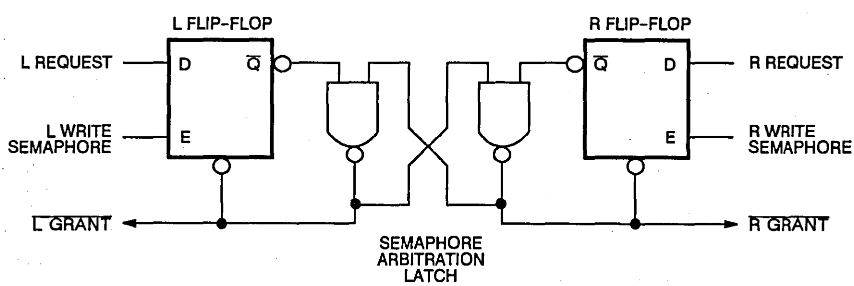


Figure 7. Semaphore Logic Design

DUAL-PORT RAM CHIP TIMING

The dual-port RAM has a simple static RAM interface and timing requirements. There are some special requirements associated with Busy, however. A timing diagram, shown in Figure 8, shows the relationships between address, data, read/write, chip select and busy signals for a dual-port RAM chip and busy logic. In this diagram, the chip select is used to enable the chip for a read or write operation after the addresses have settled. An arbitration is performed at the leading edge of the chip select.

14

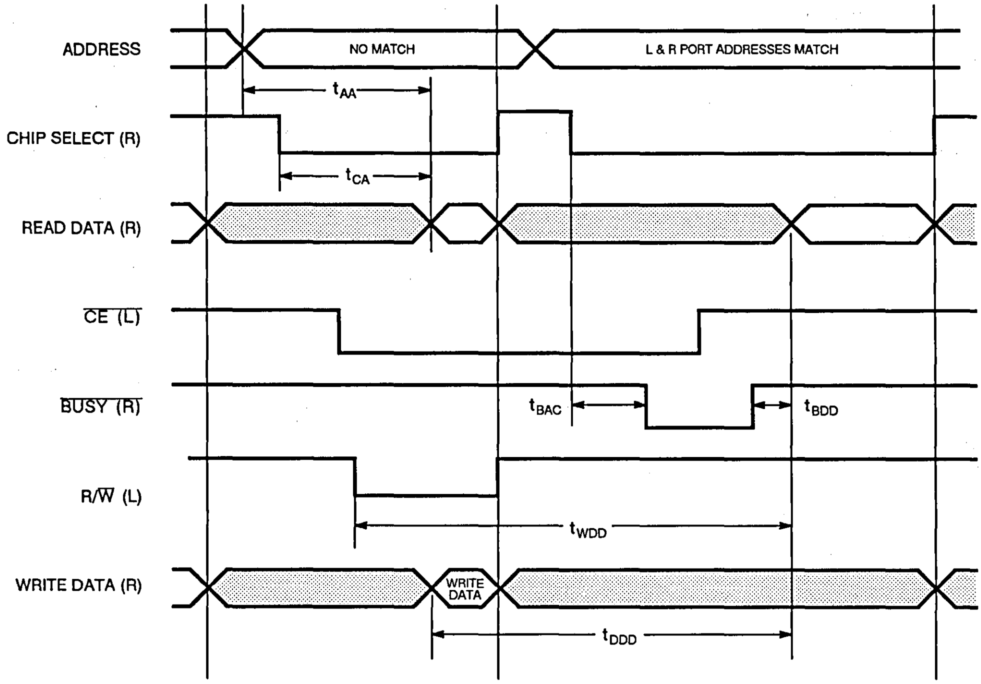


Figure 8. Dual-Port RAM Timing Diagram

Busy Logic Timing

In the case of address contention, the busy signal from the losing RAM port stabilizes some time after the leading edge of its chip select (or after its address settles, whichever comes last). If the busy signal is going to become active, it will become active during this time or not at all. If the busy signal is generated, the CPU must wait for busy to go away before completing the read or write cycle. Once the busy signal has gone high the memory read or write cycle can proceed to completion.

Note that during the arbitration time following the chip select the busy signal may be changing. Since it is possible to have a glich on the busy line during this indeterminate period, the busy line should be sensed as a level rather than as an edge.

Busy arbitration will be somewhat slower in the extreme case where both addresses arrive at exactly the same time. This is because both gates of the arbitrator latch are initially inactive and must settle into a state where only one of them is active. There will be a period of time when both gates are in transition. This is called the metastable condition and is a classic and unavoidable problem in latch and flip-flop design. As a result, the busy settling time is somewhat longer in the low probability worst case than in the commonly observed typical case. The maximum arbitration times, t_{BAA} and t_{BAC}, on the data sheet give the worst case values, including metastability setting, for these times.

Read/Write Timing with Busy

The read and write timing for either port of the dual-port RAM chip is the same as a simple static RAM in the absence of address contention. All the standard timing measures apply: read data address access time is t_{AA}, etc.

Dual-port RAMs have additional timing specifications for the case of address contention where one port is busy and waiting for access. For the most general and conservative case, the read or write cycle for the waiting side should begin after the busy signal goes away. The actual timing can be somewhat shorter than this in most cases.

For the case where the waiting side is waiting to write, the write timing requirement is that the write pulse width be measured from busy going away. For the case where both sides are reading, the data will be available at the outputs one access time after the address/chip select lines settle even though the busy line is active. In the most common case, the trailing edge of busy will occur more than one access time after the address and data for the busy side have settled. As a result, the read access time as measured from the trailing edge of busy, for this case t_{BDD}, is effectively zero.

The write/read case, waiting to read while the other side is writing to the same location, has some additional timing specifications. Since writing to a location by the L side, for example, will involve changing the data the cell being read by the R side, there is a write-to-read propagation delay time. This time is t_{WDD} for the delay for constant write data from the leading of the write pulse to the read data, and t_{DDD} for the delay for changing write data from a change of the write data to the read data.

If the writing side is running at minimum values for the write pulse or write data set-up times, the read access time, t_{BDD}, will no longer be zero. The actual t_{BDD} will be equal to t_{WDD} minus the actual write pulse width or t_{DDD} minus the actual write data set-up time, which ever is larger (and greater than zero). Note: t_{BDD} is always less than t_{AA} for the worst case of minimum write values. This is why the read or write cycle is begun from the trailing edge of busy for the most conservative case recommended above.

DUAL-PORT MEMORY EXPANSION: MAKING BIG ONES OUT OF LITTLE ONES

Dual-port RAM chips can be combined to form large dual-port memories. Expansion in memory depth with dual-port RAMs is similar to expansion in depth for conventional RAMs. An example of this kind of expansion is shown in Figure 9 where and 8K x 8 dual-port RAM has been made out of 2K x 8 dual-port RAM chips.

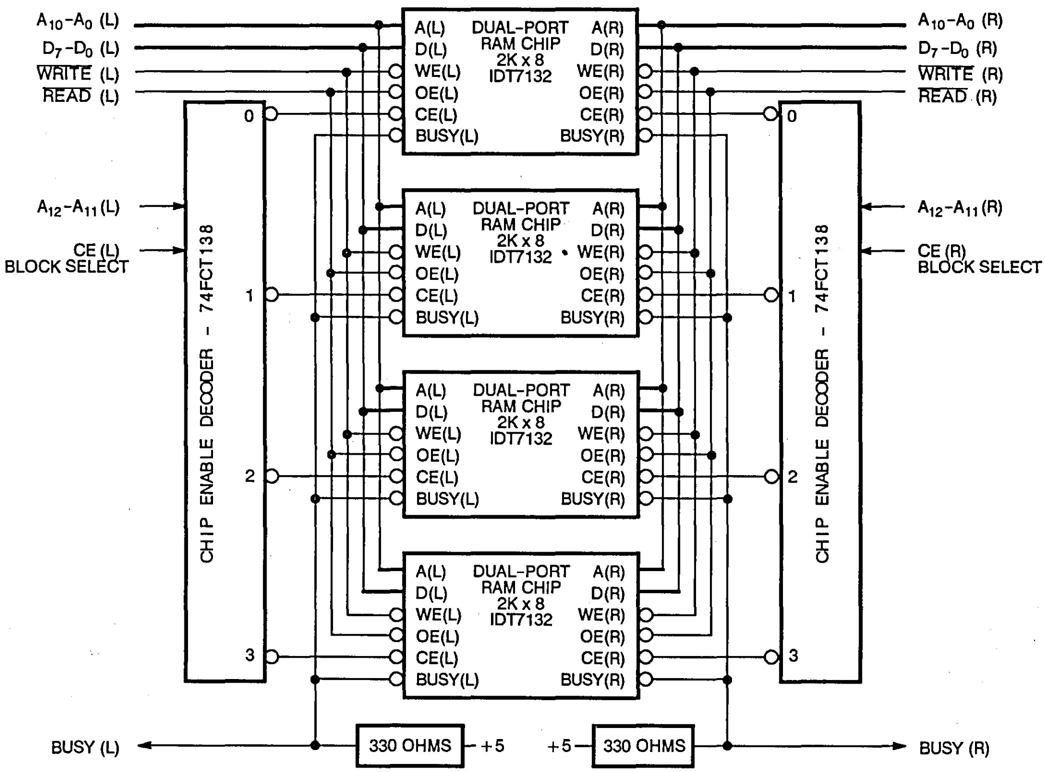


Figure 9. Depth Expansion of Dual-Port RAMs

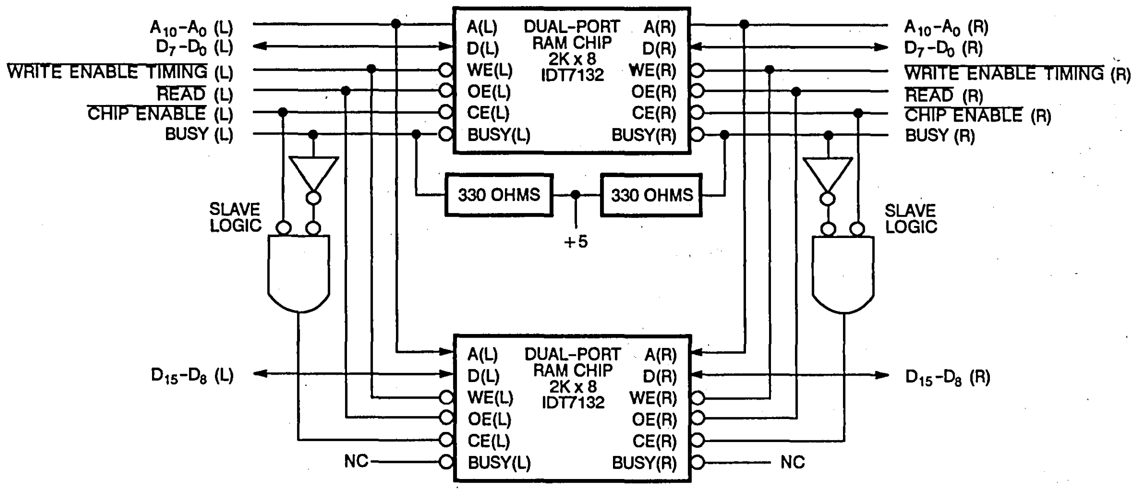
Width Expansion: The Busy Lock-up Problem

Dual-port RAMs can also be expanded in width. However, in this case, we have a subtle problem. Expansion in width implies that several dual-port RAM chips will be active at the same time. This is a problem if several hardware arbitrators are active at the same time. If we examine the case of a 16-bit RAM made out of two 8-bit RAMs, we can better understand the problem. If the addresses for both ports arrive simultaneously at both RAMs, it is possible for one RAM arbitrator to activate its L busy signal and the other RAM to activate its R busy signal. If both busy signals are used on each side, we now have a situation where both sides are simultaneously busy. The system is now locked up since both sides will be busy and both CPUs will wait indefinitely for their port to become free.

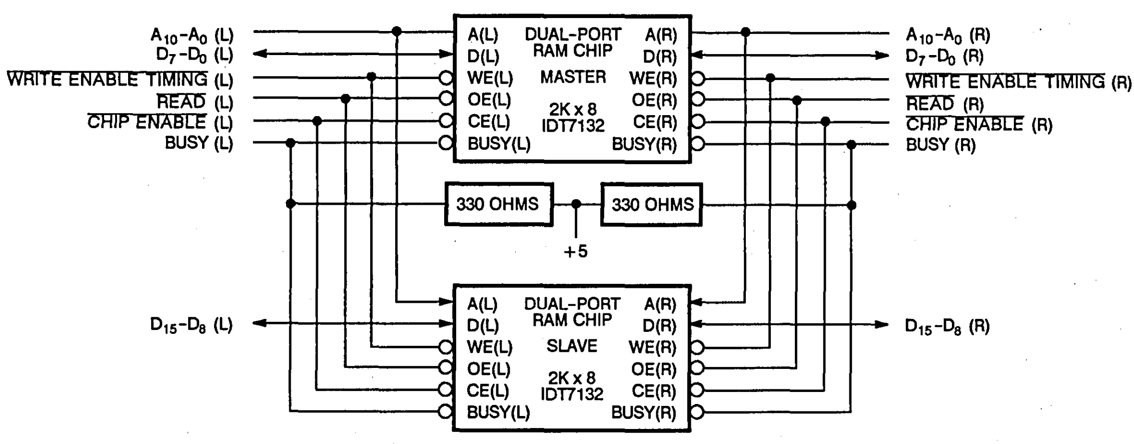
14

The Busy Lock-up Solution: Use Only One Arbitrator

The solution to this busy lock-up problem is to use the arbitration logic in only one RAM and to force the other RAM to follow it. In this case, one RAM is dedicated as the arbitration MASTER and additional RAM are designated as SLAVES. Two solutions to this problem are shown in Figure 10. One solution is to add external logic to the chip-enables of additional dual-port RAM chips. The logic gates shown cause the SLAVE RAM chip select to be disabled if the MASTER RAM is busy. Since only one set of arbitration logic is controlling the system the problem of SLAVE lock-up is avoided.



Width Expansion with SLAVE Logic (Not Recommended)



Width Expansion with SLAVE Chips (Recommended)

Figure 10. Width Expansion of Dual-Port RAMs

The second, more desirable solution, is to use specially designed dual-port RAM SLAVE chips which are part of IDT's product line. These SLAVE chips incorporate the SLAVE disable logic internally so that no additional logic is required to make a MASTER/SLAVE combination. In the SLAVE chip, the busy pin serves as an input rather than an output. If the MASTER chip activates busy, the SLAVE chip will sense this busy state and internally disable its write enable. SLAVE chips provide a speed advantage over systems which use external logic to implement the SLAVE function. Since the SLAVE logic is built into the SLAVE RAM chip, it can be designed so that there is no speed penalty when using SLAVE chips to expand the dual-port RAM width.

Width Expansion: Write Timing

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the busy input at the SLAVE has settled. Otherwise, the SLAVE chip may begin writing while the busy signal is settling. This is true for systems using SLAVE chips and for systems using conventional dual-port RAMs with SLAVE logic. This delay can be accomplished by delaying the write enable to the SLAVE by the arbitration time of the MASTER. This is shown in Figure 11.

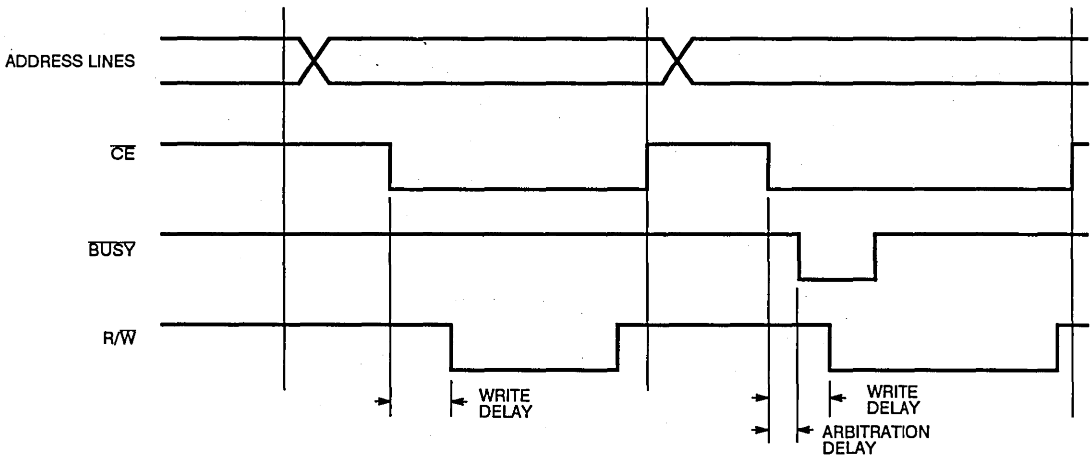


Figure 11. MASTER/SLAVE Write Timing

Note that the write delay is required only in width expanded systems which use SLAVE RAMs, not in single chip or depth expanded systems where only one chip is active at a time. This is because the individual chips have a built-in delay between the chip select and write enable inputs and the internal write enable to the RAM. Separate timing must be supplied in the SLAVE case because this internal delay time can be balanced to the arbitration time only within a chip and can vary from chip to chip. If the delay time for the SLAVE is less than the arbitration time of the MASTER, writing could begin before busy became active, as above.

14

Width and Depth Expansion: An Example

These techniques for expanding dual-port memories in width and depth are combined in the example shown in Figure 12. In this example, an 8K x 16 dual-port memory is made from 2K x 8 chips in MASTER/SLAVE combination.

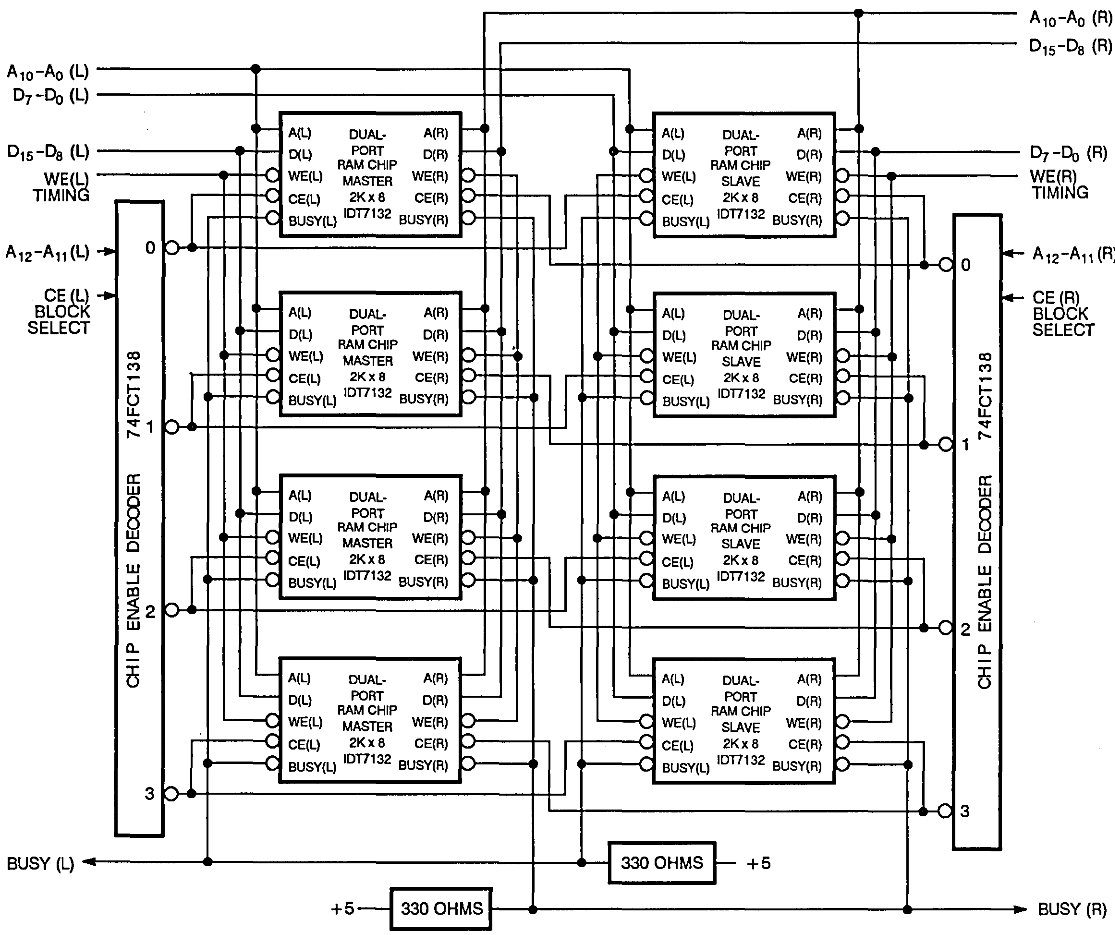


Figure 12. Width and Depth Expansion of Dual-Port RAMs

USING THEM: DUAL-PORT RAM APPLICATION EXAMPLES

Examples of dual-port RAMs used for CPU-to-CPU communication are shown in Figures 13, 14 and 15. In Figure 11, a pair of 8-bit processors communicate using a single 2K x 8 dual-port RAM chip. In Figure 12, there is a similar system where a pair of 16-bit processors communicate using a pair of dual-port RAM chips and a MASTER/SLAVE configuration. Finally, in Figure 13, we have an 8-bit processor communicating with a 16-bit processor through two 2K x 8 dual-port RAMs.

In Figure 13, two Z80 microprocessors communicate using a single IDT7132 dual-port RAM chip. The IDT7132 is controlled by the chip enable. The write enable is set up in advance by the WR signal from the Z80 and the chip enable is used to write data into the RAM or to gate the read data onto the Z80 bus. The output enable (not shown) is tied to ground (continuous enable). The write enable is used to disable the output drivers.

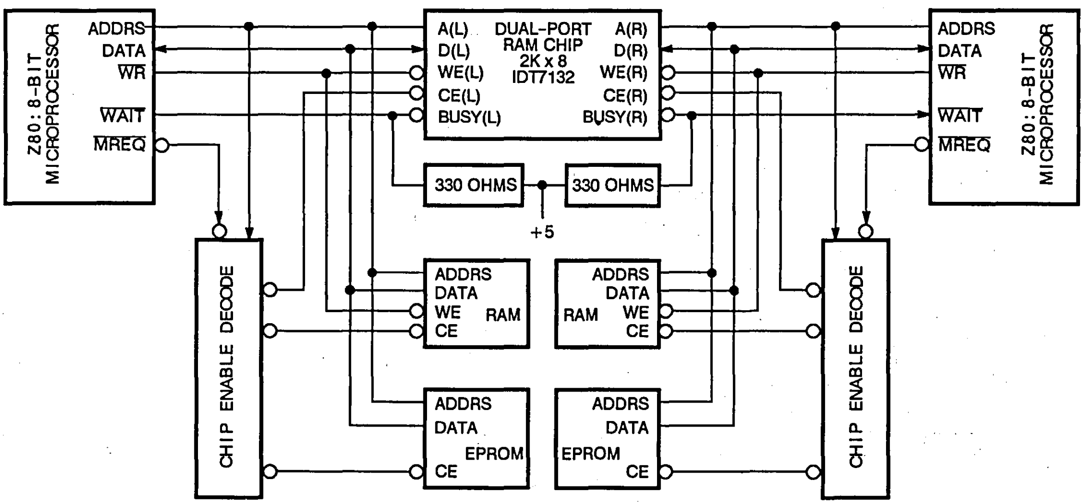


Figure 13. 8-bit to 8-bit CPU Communication

14

In Figure 14, two 68000 microprocessors communicate through a pair of dual-port RAMs. A IDT7132/7142 MASTER/SLAVE pair is used to avoid the busy lock-up problem. Note that the Address Strobe (AS) from each 68000 is used with an address decoder to enable the dual-port RAM chips. This is to maintain the address for read-modify-write cycles so that arbitration is not lost between the read and the write. This is important for test and set instructions, for example.

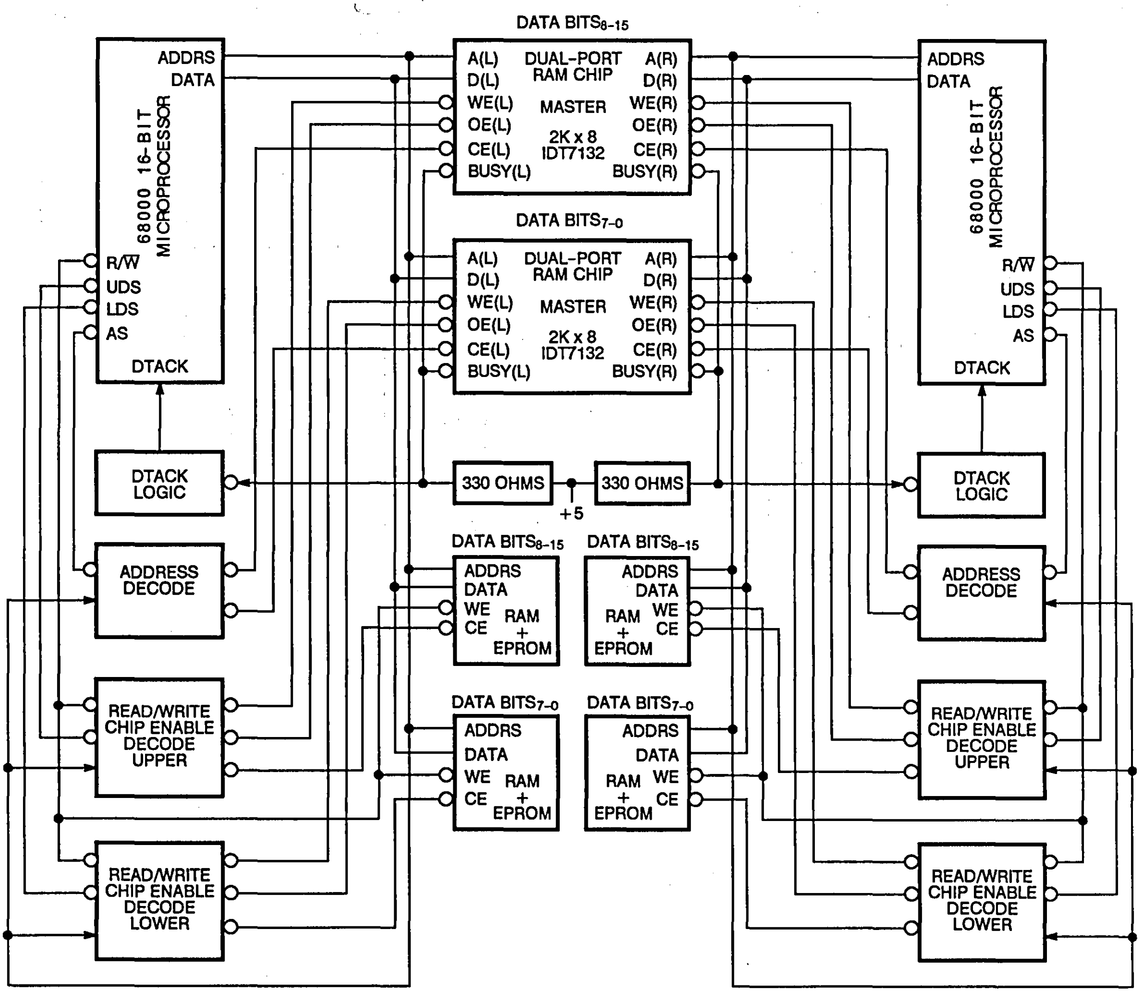


Figure 14. 16-bit to 16-bit CPU Communication

In Figure 15, a Z80 and a 68000 communicate using a pair of IDT7132 dual-port RAMs. No SLAVE logic is required because the Z80 side chip enable decode ensures that only one RAM chip will be enabled at a time. Otherwise, this figure is a combination of the logic from Figures 13 and 14.

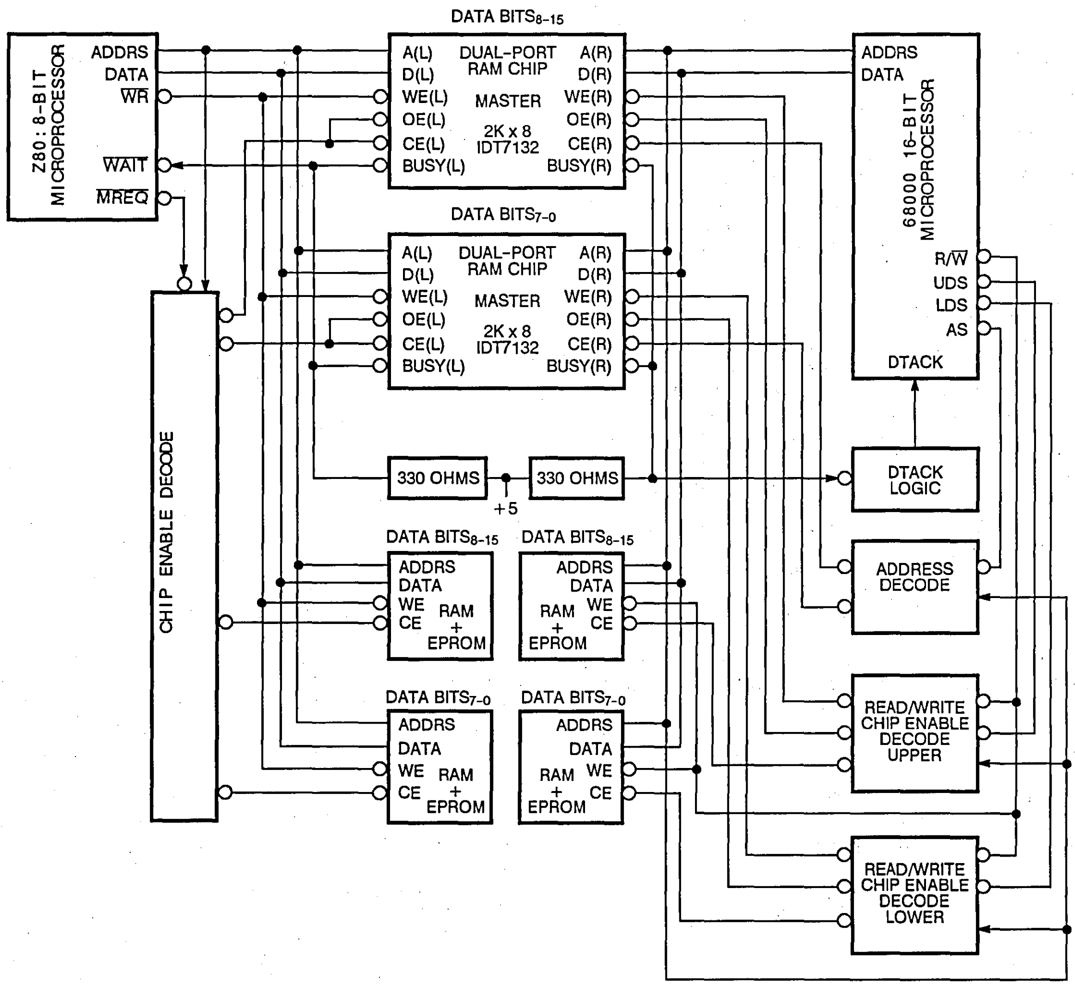


Figure 15. 8-bit to 16-bit CPU Communication

14

SUMMARY AND CONCLUSION

The development of true dual-port memories in integrated circuit form provides the designer with the ability to set up communication between components of a computer system while avoiding many of the problems of prior systems. While the concept of dual-port memory has been with us from the early days of computing in the form of DMA, the new dual-port ICs can provide this function at very high speeds and without the delays associated with earlier designs. Because of the utility of the dual-port memory concept these chips should come into wide spread use and become one of the standard components used by the computer designer.

Integrated Device Technology, Inc.

TRUST YOUR DATA WITH A HIGH-SPEED CMOS 16-, 32- OR 64-BIT EDC

APPLICATION NOTE AN-03

By Suneel Rajpal and John R. Mick

INTRODUCTION

As a computer-science corollary to Parkinson's First Law, "Work expands to fill the time available," it is observably always true that "Computer software expands to fill the memory available." There is an insatiable demand for higher speed and denser memory, be it dynamic RAM or static RAM. However, there are reliability considerations that have to be made in large memory systems that must always provide correct data. This application note deals with methods of enhancing data integrity and system performance by using Error Detection and Correction (EDC) logic circuits.

TYPES AND SOURCES OF ERROR

In memory systems, two types of errors can occur—hard errors or soft errors. A hard error is a permanent error and it occurs when a memory location is stuck-at-one or stuck-at-zero. A soft error is temporary, random and correctable. As these errors are non-recurring and non-destructive they can be corrected using EDC logic.

Hard errors are caused by factors such as interconnect failures, internal shorts and open leads. Soft errors can be caused by system noise, power surges, pattern sensitivity and alpha particle radiation. The charge of an alpha particle can become comparable to the charge on memory cells as geometries shrink. This implies that susceptibility to alpha particle radiation is likely to increase as memory densities increase; however, memory manufacturers try to reduce or eliminate the problem through design or packaging techniques.

In spite of that, there is a probability of failure or error, especially where large systems are concerned. A graph that shows the trend of error rate versus chip density for dynamic RAMs is presented in Figure 1. One can calculate the Mean Time Between Failures (MTBF) for a DRAM system quite easily based on such data from a DRAM manufacturer.

A common method to examine data integrity is to incorporate parity. In a simple case of a three-bit number and one parity bit, the following relationship exists as shown in Table 1:

TABLE 1

DATA	ODD PARITY
000	1
001	0
010	0
011	1
100	0
101	1
110	1
111	0

The odd parity is generated by an exclusive-NOR operation of the data bits. An error can be identified by taking the entire word and the parity bit, called a code, and performing an exclusive-OR operation. If the exclusive-OR result was a one, it indicates that the data was probably correct and the combination of the data and parity bits represent a valid code; "probably" is mentioned, and will be explained in the following lines. However, if the exclusive-OR result was a zero, then it can only be identified that an error occurred and the combination of the data and parity bits represent an invalid code.

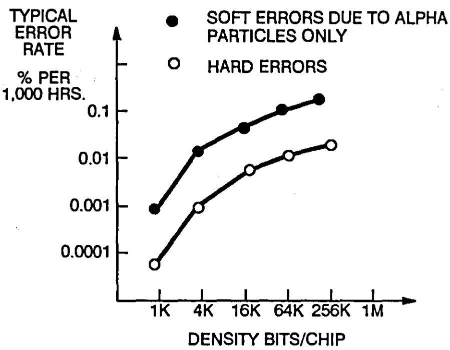


Figure 1: Typical Error Rates

Another interesting aspect of Table 1 is the fact that to go from one valid code, say 0001, to another valid code, 0100, at least two bits have to change. This is called a distance of two. If only one bit changed on the code, it could be used to identify an error, but it could not point to the correct valid code. For example, if an invalid code of 0011 is seen, it lies between 0001 and 0010 and it is not possible to tell if the last data bit is in error or the parity bit is in error. Now, back to the mention of the word "probably". If two bits in the data changed erroneously, the parity tree performing the exclusive-OR would not be able to catch that kind of an error. Detection codes using parity are therefore limited and useful only in detecting one bit in error (or any number of odd errors), and they cannot provide any correction. Unfortunately, they cannot detect two errors (or any even number or errors).

The detection capability of the codes with different distances are shown in Figure 2. An invalid code that occurs in the distance of two cannot tell which bit was erring as outlined in the previous paragraph. Codes that keep a distance of three (or least 3-bits have to change to go from one valid code to another) can detect single bit errors and also correct them. However, codes with a distance of three cannot detect two failing bits. As shown in the distance of three examples, if a two-bit error occurs, it would be identified as if one bit failed. An invalid code associates detection/correction with the valid code adjacent to it rather than the other valid code that is a distance of two from it. Codes with a distance of four can detect all single-bit errors, detect all double-bit errors and also correct all single-bit errors. Double-bit errors are equidistant from two valid codes as shown by the central invalid code in Figure 2. The Single Error Correction and Double Error Detection (SECDED) capability is highly desirable for data integrity in high-reliability computer systems.

Printed in the U.S.A.
6/87 Rev. 1

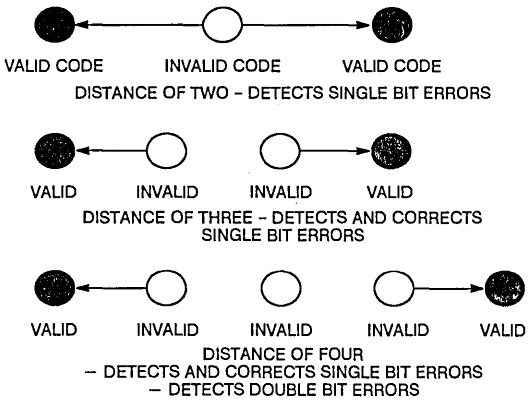


Figure 2: Codes of Various Distances and Their Effectiveness

EDC ICs TO THE RESCUE

Codes with the distance of four are used in the IDT39C60/IDT49C460 Error Detection and Correction ICs. The overhead in the EDC implementation is additional check bits to the words in memory. For example, 6 bits are needed for 16-bit data, 7 bits for 32-bit data, and 8 bits for 64-bit data to generate a distance of four. The code formed is a catenation of the word bits and the check bits and, as in the parity case, the code can be valid or invalid. The valid codes are a distance of four apart from the next valid code. Valid codes are implemented by generating check bits based on the data word and writing the check bits with the data bits to the memory. On reading the data and check bits from memory, a possibly valid or invalid code could have been read. The determination of whether the code was valid or not is done by regenerating check bits using the data bits; these are compared (ex-ORed) to the check bits that were read and the result is syndrome bits. These syndrome bits are indicative of an error-free situation, or a single or double-bit error, and are used to determine validity of a code, and also to point to single-bit errors and identify the occurrence of two or more bits in error.

As an example, let us write $(FFFF)_H$ as the data word. The corresponding check bits that will be written in the memory are 001100 and can be computed using Table 2 which is based on a modified Hamming code. On reading back, if the data was FFFE and the data in position 15 had erroneously flipped from a "1" to a "0", the regenerated check bits would be 000111 (based on FFFE). The syndrome bits are the ex-OR of the two sets of check bits and are 001011. Referring to Table 3, a syndrome of 001011 indicates bit 15 is in error and has to be flipped.

The internal hardware of the IDT39C60 16-bit EDC, shown in Figure 3A, consists of ex-OR trees that can generate check bits and syndromes and also contains hardware to correct data. In addition, two or four IDT39C60s and some SSI, MSI can be connected to form 32-bit or 64-bit EDC systems. The IDT39C60 is a functional and pin-compatible replacement of the 16-bit 2960, and runs at a quarter of the power. Faster versions, such as the IDT39C60 and the IDT39C60A (the IDT39C60-1 replaces the Am2960-1 and the IDT39C60A is the fastest 16-bit EDC available), demonstrate that CMOS circuits can not only run cooler than their equivalent bipolar circuits, but also run faster with higher output drive.

The architecture of a 32-bit EDC, the IDT49C460, is shown in Figure 3B. The IDT49C460 provides efficient means of generating check bits, calculating syndrome bits and correcting data bits on a 32-bit data path. In addition, diagnostic capability is provided to verify data operations in the memory system and verify that the EDC IC is functional too.

TABLE 3. SYNDROME DECODE TO ERROR LOCATION/TYPE

SYNDROME BITS	S8	0	1	0	1	0	1	0	1
	S4	0	0	1	1	0	0	1	1
	S2	0	0	0	0	1	1	1	1
SX S0 S1									
0 0 0		*	C8	C4	T	C2	T	T	M
0 0 1		C1	T	T	15	T	13	7	T
0 1 0		C0	T	T	M	T	12	6	T
0 1 1		T	10	4	T	0	T	T	M
1 0 0		CX	T	T	14	T	11	5	T
1 0 1		T	9	3	T	M	T	T	M
1 1 0		T	8	2	T	1	T	T	M
1 1 1		M	T	T	M	T	M	M	T

NOTES:
* = No errors detected
Number = Number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

TABLE 2. 16-BIT MODIFIED HAMMING CODE CHECK BIT GENERATION

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

14

Figures 4A and 4B show the dataflow for the generate and error detect/correct operations in the IDT49C460. In Figure 4A, check bits based on input data are generated by the EDC and are written to the check-bit memory along with the data. In Figure 4B, the data and check bits are read from the memory. Based on their values, the syndrome bits are generated inside the IDT49C460. If the EDC is in the correct mode, any single-bit error is corrected and the corrected data is placed in the output data latch. The syndrome bits are also available if error logging is done.

Another necessary operation that is required is byte handling. When the memory is organized as a 32-bit word and an 8-bit update is being performed, it requires a 2-step operation. The first step is to read the 32-bit data and check bits, and correct any erroneous single bit failure. The second step is to write the new byte with the three unmodified bytes back to the system memory. The check bits corresponding to the newly formed 32-bit word are generated and also written to the memory. This operation is supported by having four separate output byte enables in the IDT49C460. The two-step process is shown in Figures 5A and 5B.

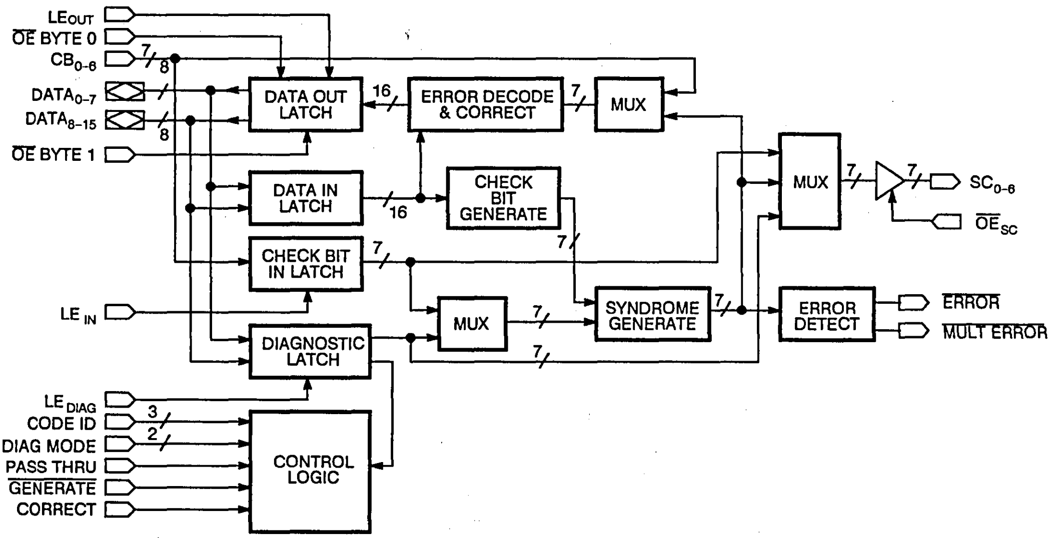


Figure 3A: The IDT39C60 16-Bit EDC Architecture

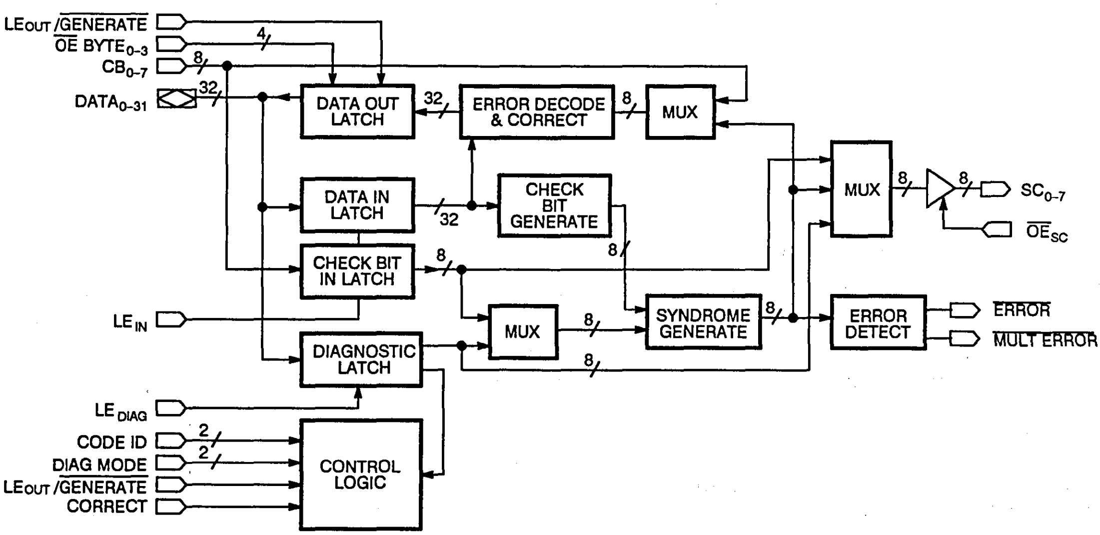


Figure 3B: The IDT49C460 32-Bit EDC Architecture

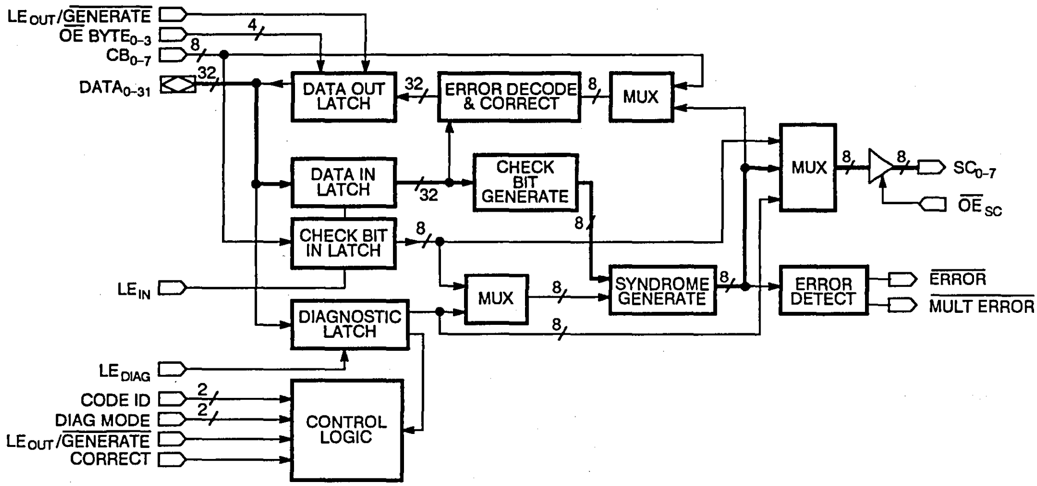


Figure 4A. Check Bit Generation in the IDT49C460

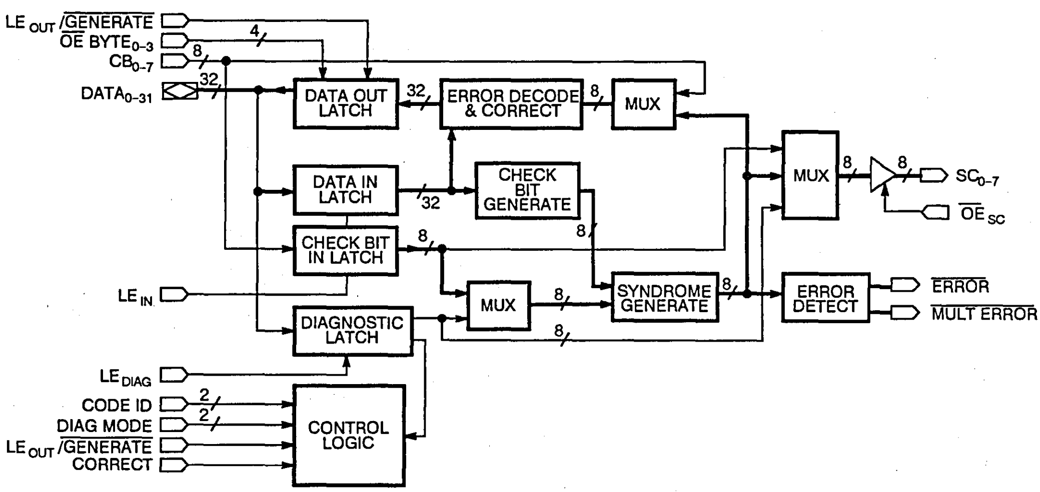


Figure 4B. Error Detection and Correction Data Flow in the IDT49C460

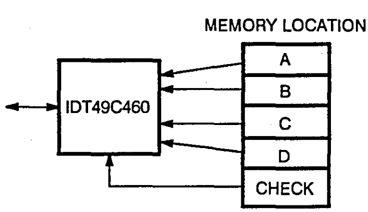


Figure 5A. Byte-Write Operation, Step 1. Read 32-Bit Word and Correct Any Single-Bit Error

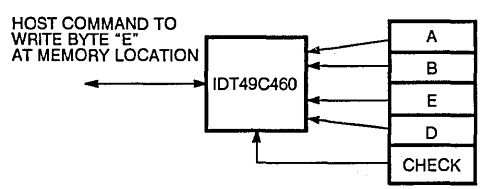


Figure 5B. Byte-Write Operation, Step 2. Newly Generated Check Bits Corresponding to Bytes A, B, E, and D Are Written To Memory Along With Bytes A, B, E, and D

14

The IDT49C460 is expandable to 64-bit wordlengths as shown in Figure 6A. The external buffer may not be required if the path from the memory already has a three-state buffer in its output stage or externally in the data path to the EDC. Figure 6B shows a 2-step operation when an error detection and correction occurs in bit 32-63 of the 64-bit word. The IC on the first level, with the code ID = 10, receives the data bits 0-31 and all the check bits. In the example shown, bit 63 has erroneously flipped from a "1" to a "0". The partial syndrome bits are passed from the first device to the second. (The actual syndrome bits are generated from a table not shown in this article but are in the IDT49C460 data sheet.) The check input latch of the second device is open, due to its code ID = 11, and the partial syndrome bits are combined with the data bits to generate the final syndrome bits. The final syndrome bits indicate that bit 63 is in error and it is inverted to produce a correct result. The final syndrome bits are also sent back to the first device, but the resulting syndrome does not alter any data bits in the first device. Therefore, the error correction is a 2-step process. In Figure 6C, an error occurs in the bits 0-31. In this case, the partial syndrome is sent to the second device. The second device generates the final syndrome and sends it back to the first device. Finally the erroneous bit is flipped over. In this case, a 3-step operation takes place.

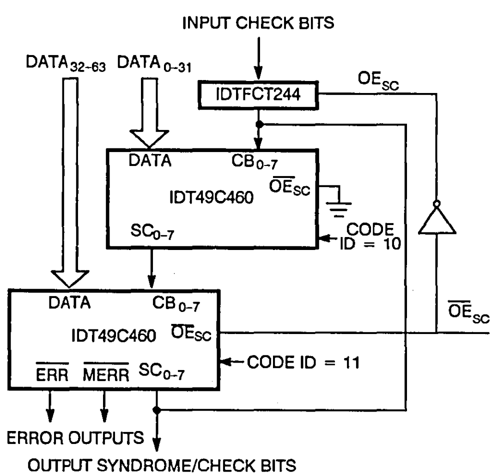


Figure 6A. The IDT49C460 in a 64-Bit Configuration

	DATA	CHECK		
	FFFFFFFFFFFFFFFF	30	WRITE	
	FFFFFFFFFFFFFFFE	30	READ	
CODE = 10	FFFFFFFF(BITS 0-31)	30(INPUT CHECK BITS)		STEP 1
		00(PARTIAL SYNDROME)		
CODE = 11	FFFFFFFE(BITS 32-63)	00(PARTIAL SYNDROME)		STEP 2
	FFFFFFFF(CORRECTED 32-63)	AE(FINAL SYNDROME)		
CODE = 10	FFFFFFFF(UNCHANGED 0-31)			

Figure 6B. Error Correction on a 64-Bit Word, When Error is in Bits 32-63

	DATA	CHECK/SYNDROME		
	FFFFFFFFFFFFFFFF	30(CHECK)	WRITE	
	FFFFFFFEFFFFFFFF	30(CHECK)	READ	
CODE = 10	FFFFFFFE(BITS 0-31)	30(INPUT CHECK BITS)		STEP 1
		2F(PARTIAL SYNDROME)		
CODE = 11	FFFFFFFF(BITS 32-63)	2F(PARTIAL SYNDROME)		STEP 2
	FFFFFFFF(BITS 32-63)	2F(FINAL SYNDROME)		
CODE = 10	FFFFFFFF(CORRECTED BITS 0-31)	2F(FINAL SYNDROME)	–	STEP 3

Figure 6C. Error Correction on a 64-Bit Word, With Error in Bits 0-31

HOW THE IDT49C460 FITS IN A SYSTEM

By virtue of their function, EDC ICs tie in closely with system memory architecture. Figure 7 shows a host that generates addresses and accesses a memory system. The memory contains memory elements, error detection logic and interface circuits. These are needed to start a memory cycle, to send/receive data on the system bus, and to inform the host that it has completed the memory operation.

One may use EDC for dynamic RAM memories or static RAM memories. Figures 8A and 8B show general configurations for DRAM arrays. Normally, in DRAM systems, separate pins exist for the DATAOUT and DATAIN. Therefore, IDT FCT244s can be used to provide an isolation between the DATA port of the EDC and the DATAOUT from the RAM. This isolation may be required after a read operation, and the EDC provides corrected data to the system and the DRAM. Another buffer is needed between the DATA port of the EDC and the system data bus to allow the corrected data to be placed on the system bus. The DRAM controller can be implemented using standard off-the-shelf products. An important operation that has to be supported is byte or word handling. The IDT49C460 EDC configuration shown in Figure 8A has four individual byte enable controls going to the IDT FCT244s and their complements to the IDT49C460. The IDT39C60 shown in Figure 8B has two individual byte controls to the IDT FCT244s and their complements going to the IDT39C60.

In static RAM systems, as shown in Figure 9, there is no need for a dynamic memory array controller; however, bidirectional buffers are required on the ports of the static RAMs as RAMs have common I/O lines for data. If the SRAMs had separate I/O pins for the data, the buffer configuration of the DRAM array could be used.

The timing controller, common to both DRAM and SRAM systems, controls the buffers and the EDC ICs. This is an interesting task to the memory system designer, as a choice of EDC architectures are available.

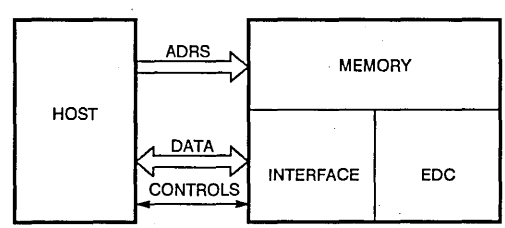


Figure 7. A Typical High-Reliability Memory System

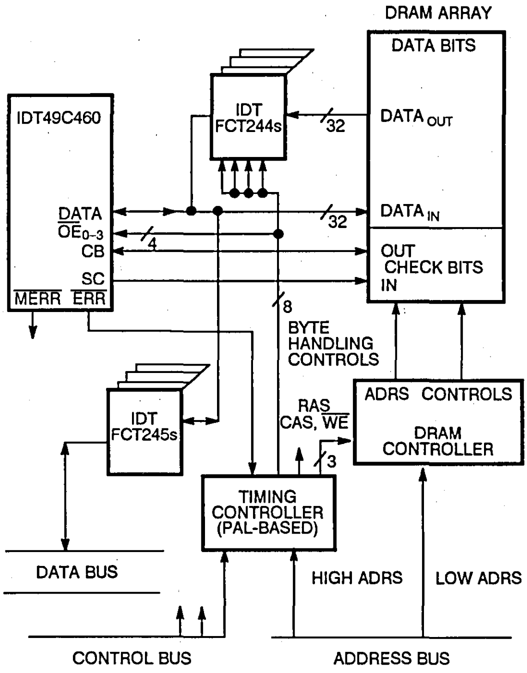


Figure 8A. EDC Logic in 32-Bit DRAM-Based Memory Systems

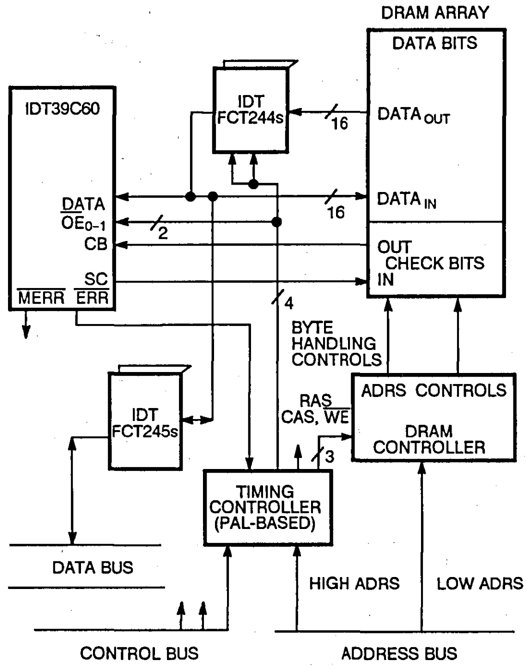


Figure 8B. EDC Logic in 16-Bit DRAM-Based Memory Systems

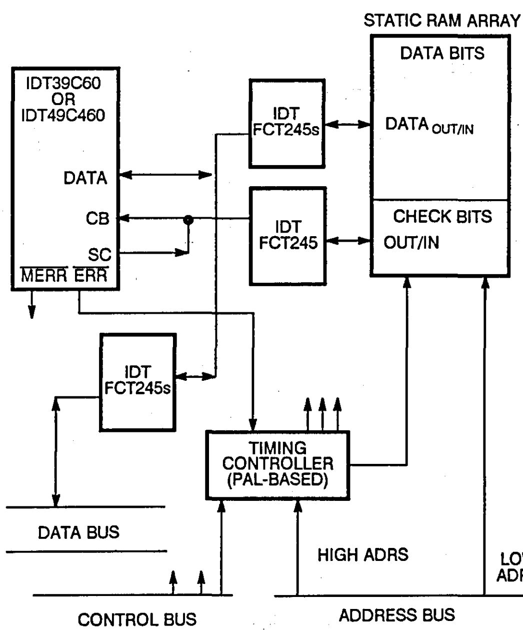


Figure 9. EDC Logic in 16-, 32- or 64-Bit Static RAM-Based Systems

BUS-WATCH AND FLOW-THROUGH EDC ARCHITECTURE

The architecture of EDC ICs can be categorized as Bus-Watch and Flow-Through as shown in Figure 10. In a bus-watch architecture, there is only one bus to handle the data and one set of pins that handle incoming data from the memory, corrected data from the EDC, and incoming data from the system to be written to the memory. The IDT39C60 and IDT49C460 are based on a bus-watch architecture. In a flow-through architecture, such as Intel's 8206, there are two ports that handle data movement. The WDIN/DOUT handle incoming data from the system so that the EDC can generate check bits. The second function of the WDIN/DOUT is to supply the corrected data to the system and the memory. The second set of pins, DIN, only handle incoming data from the RAM. These architectures lend themselves to "Check Only" and "Correct Always" configurations.

The "Check Only" method is used in high-performance systems. The memory system always sends data directly to the host when a read is requested. In the event a single bit error occurs, one approach is that the read cycle is delayed and a correction is performed. The corrected data is sent to the host and written into the memory. In this case, the timing control circuit would disable the Memory Data Out Buffer (the IDT FCT244 for the DRAM case and the IDT FCT245 for the SRAM case) and put corrected data from the EDC IC onto the system data bus, also writing the corrected data back into the memory array. For the "Check Only" method, a DATA TO ERR parameter is of key concern to designers as this can be used to generate the DTACK, READY or BERR signals to the host.

14

The other option is that a "Correct Always" method is used. In this case, the EDC always corrects data (regardless of the fact that it may be error-free), sends it on the system data bus and writes it back to the memory. In this case, the cycle time for the data read includes the "DATAIN TO CORRECTED DATAOUT" parameter for the EDC. The IDT49C460 and the IDT39C60 provide the fastest timings for the "DATAIN to ERR" and "DATAIN TO CORRECTED DATAOUT" parameters when compared to other currently available 32-bit and 16-bit EDCs. This was made possible by using IDT's CEMOS™ technology.

The IDT49C460B dissipates only 95mA and the IDT39C60A dissipates only 85mA over the commercial temperature range. The quiescent power consumption is only 5mA for the IDT49C460B and the IDT39C60A.

The delay for the DATAIN to ERR is only 25ns for the stand-alone 32-bit IDT49C460B (worst case commercial) and 42ns for the 64-bit cascaded case. The delay in DATAIN TO CORRECTED DATAOUT is only 32ns for the stand-alone case and 57ns for the 64-bit cascaded case. These parameters are very important when considering EDC ICs discussed further in a later section. They are, however, shown in Tables 4 and 5 for the 16-bit IDT39C60 and 32-bit IDT49C460, respectively.

The acid test is how a flow-through architecture compares in performance to a bus-watch architecture in the "Check Only" mode and the "Correct Always" mode. In Figure 11, a flow-through EDC device is connected to a DRAM array system for "Check Only" operations. Data from the memory goes through the IDT FCT244 buffer to the system bus directly and simultaneously to the EDC device. Within the DATAIN to ERR of the device, it is determined if a single-bit error occurred and, if so, a timing controller would disable the IDT FCT244 and allow corrected data to be sent on the system bus via the IDT FCT245.

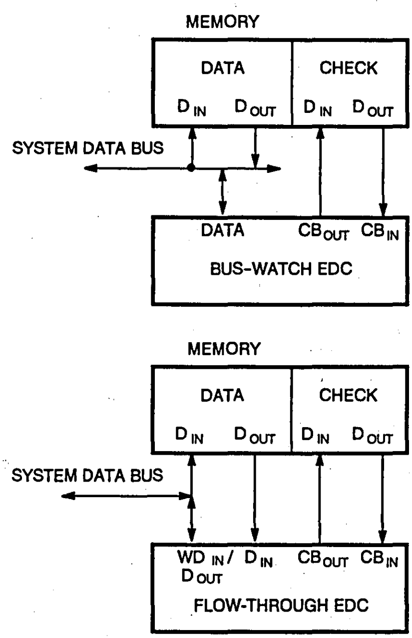


Figure 10. Architecture of Bus Watch and Flow-Through EDC Logic

A bus-watch EDC in a "Check Only" configuration is shown in Figure 12. The data path from the DRAM to the EDC goes through one IDT FCT244 delay and is identical to the flow-through case. After that, the DATAIN to ERR delay determines whether or not the cycle would be stretched. The data from the DRAM goes through an IDT FCT244 buffer and an IDT FCT245 buffer in the bus-watch case. One emerging fact is that the time it takes to make a decision to stretch a memory cycle is the same for bus-watch and flow-through EDC parts and is determined by the DATAIN to ERR of the respective devices.

In the flow-through "Correct Always" configuration, as shown in Figure 13, data has to always pass through the EDC and any IDT FCT245 and then go on to the system bus. In the case of bus-watch ICs, data from the DRAM goes through an IDT FCT244, in and out the EDC device and through an IDT FCT245, as shown in Figure 12. A bus switch has to take place every cycle as memory data comes into the EDC, is corrected and then transferred to the system bus. In a practical design this bus switch may be the longest delay path for "Correct Always".

TABLE 4: KEY PARAMETERS FOR THE IDT39C60/-1/A FOR COMMERCIAL RANGE

	IDT39C60	IDT39C60-1	IDT39C60A
$DATA_{IN}$ TO $\overline{ERR}$	32ns	25ns	20ns
$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$	65ns	52ns	30ns

TABLE 5: KEY PARAMETERS FOR THE IDT49C460/A/B FOR COMMERCIAL RANGE

CONDITIONS	IDT 49C460	IDT 49C460A	IDT 49C460B	2-49C460Bs FOR 64-BIT EDC
$DATA_{IN}$ TO $\overline{ERR}$	40ns	30ns	25ns	42ns
$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$	49ns	36ns	30ns	57ns

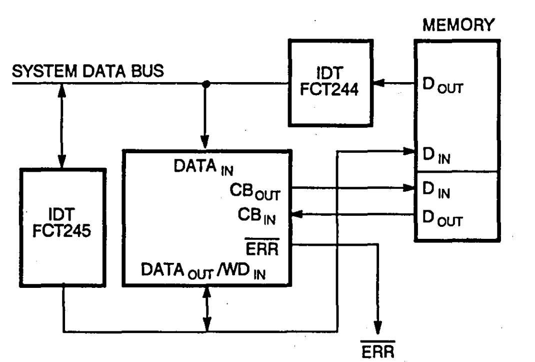


Figure 11. The "Check Only" Configuration for Flow-Through EDC ICs

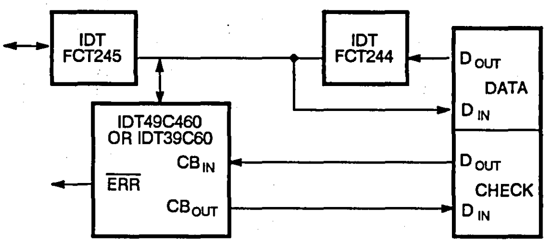


Figure 12. The Bus-Watch EDC in "Check Only" or "Correct Always" Configurations

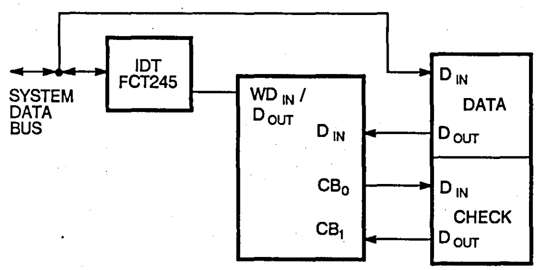
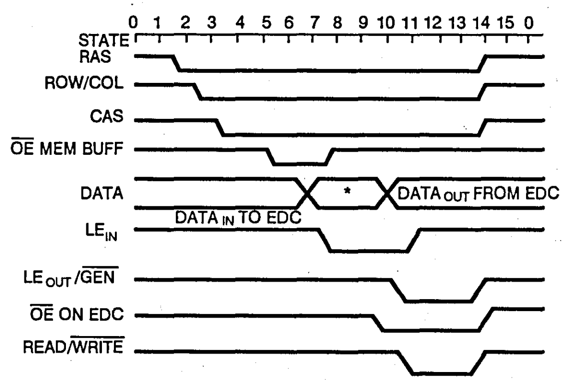


Figure 13. Flow-Through EDC in "Correct Always" Mode

However, if just the specification is being reviewed, the flow-through path is shorter by an IDT FCT244 delay. A specification comparison is that the "DATAIN TO CORRECTED DATAOUT" delay of a flow-through EDC part should be compared to the "DATAIN TO CORRECTED DATAOUT" delay of the IDT49C460 plus an external 7ns buffer delay (for the IDT FCT244). However, in an actual system such as the one in Figure 8A, a "bus-switch" has to take place, as explained below.

In a DRAM system that has a bus-watch EDC, a sequence of events has to be created by the timing controller that was shown in Figure 8A. The timings that the controller generates are shown in Figure 14. The example being considered is "Correct Always." The RAS, CAS, $\overline{\text{WE}}$ signals have to be generated to read data from the DRAM. The read takes place before state 7, and the read data is latched in the DATAIN latch of the EDC. It is then corrected and the corrected data can be latched in the DATAOUT latch. The data correction can take place between states 7 and 10. Any time after state 10, the EDC can place the corrected data on the bus. The bus that was loading the data in the EDC has to be turned around as the EDC is going to send corrected data to the host. The EDC also writes back the corrected data and the newly generated check bits to the memory. The memory buffers shown in Figure 8A are three-stated, as the $\overline{\text{OE}}$ MEM BUFF is high from state 7 onwards and the EDC would be enabling data on the bus. The timing diagram in Figure 14 explains a typical case and the users will have to customize it based on their memory speeds and the time the system has for receiving valid data.

Other factors that may be a consideration are package count and board space. The number of packages used in flow-through and bus-watch implementations are the same for "Check Only" configurations. In "Correct Always" configurations the bus-watch implementation requires four more IDT FCT244s than the flow-through implementation. Flow-through ICs have more pins and therefore leave a larger footprint on the PC. However, in terms of board space, since the footprint of the flow-through EDC is larger that the bus-watch, the bus-watch approach takes less space for "Check Only" configurations and there is a tie for the "Correct Always" configuration.



*NOTE: A BUS-SWITCH TAKES PLACE BETWEEN STATES 6 AND 10

Figure 14. Timing Diagram for Correct Always in Figure 7A

SUMMARY

This article has covered reliability issues in memory systems and solutions using EDC devices. In considering EDC devices, two parameters are critical: the "DATAIN to $\overline{\text{ERR}}$" and the "DATAIN TO CORRECTED DATAOUT". At Integrated Device Technology, we have optimized these two parameters and produce ultra-fast, TTL-compatible CMOS Error Detection and Correction devices for high-performance 16-, 32- and 64-bit systems.

14

Integrated Device Technology Inc

HIGH-SPEED CMOS TTL-COMPATIBLE NUMBER-CRUNCHING ELEMENTS FOR FIXED- AND FLOATING-POINT ARITHMETIC

APPLICATION NOTE AN-04

by Suneel Rajpal

INTRODUCTION

Traditionally, high-speed number-crunching requirements could only be fulfilled by bipolar (TTL) components. However, with the advent of advanced CMOS technologies, one can not only attain higher densities and lower power consumption, but also attain higher speeds. This paper deals with different building blocks that can be used to build integer or floating-point processors at speeds greater than 10MHz.

FIXED-POINT PROCESSORS

In order to build a high-speed efficient fixed-point processor, a number of computational elements are required. A high-speed ALU and a multiplier are all integral parts of a high-speed processor. These building blocks must be cascadable or expandable for higher-precision numbers. High-speed memories are also required for data storage and for control store which essentially drives the system. A typical microcoded system is shown in Figure 1. It consists of three sections: the control section, the address generation section and the number-crunching section. The key elements in the control block and number-crunching block, shown in Figure 1, are illustrated in Figures 2 and 3. (The address generation can be supported by the architecture in Figure 3.) An instruction is fetched from the main memory (not shown). Then the opcode is decoded to cause a jump to the appropriate address in the control store. This address is the start address of the microinstructions that emulate the macroinstruction.

The next step may be to fetch the operands; this is done by putting the address on the address bus and bringing data into the data input registers. If more parallelism is required, a separate ALU can be used to compute addresses concurrently with an ALU that is computing data from the previous instruction.

Figure 2 contains the microprogram sequencing and the control store section. This typically consists of a microprogram sequencer, a control store, pipelines, registers, and some MSI for condition code selection. The IDT39C10B is a 12-bit microprogram sequencer that is plug-compatible with all versions of the 2910. One of four sources can be selected as the next address: the microprogram address register, the LIFO stack, the internal register/counter, or the direct D input. An added feature in the IDT39C10 is the deeper stack with 33 locations instead of nine provided by the 2910 sequencer. Figure 3 shows a plausible arrangement of ALUs, multiplier/ multiplier-accumulators and extended data storage. A computation for worst-case cycle time for the control path is shown in Figure 4. The corresponding worst-case delay for the data path is shown in Figure 5. It is an interesting exercise to analyze these two delay paths. The control path has a 64ns delay and the data path has a 49ns delay, adding to the IDT49C402 delay and register propagation delay and setup time. The IDT49C402, shown in Figure 6, is code-compatible

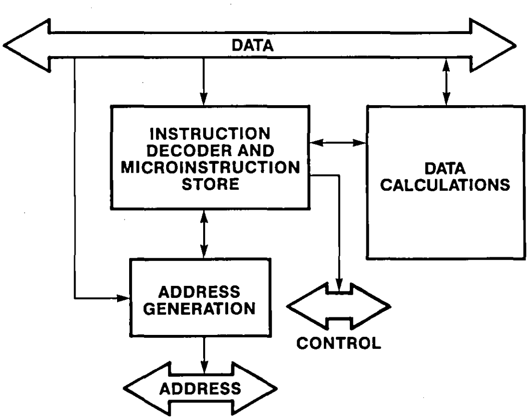


Figure 1. A Typical CPU

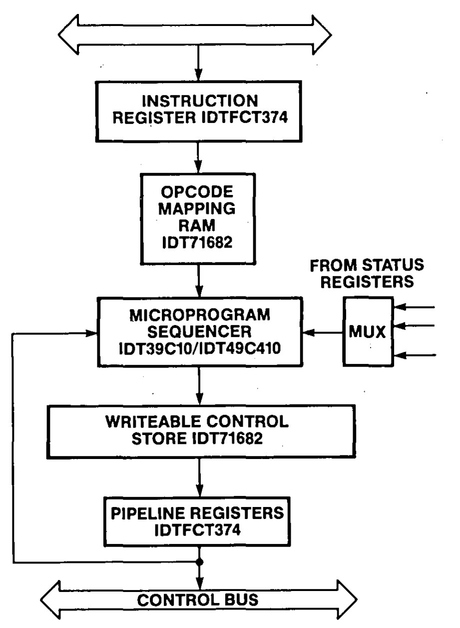


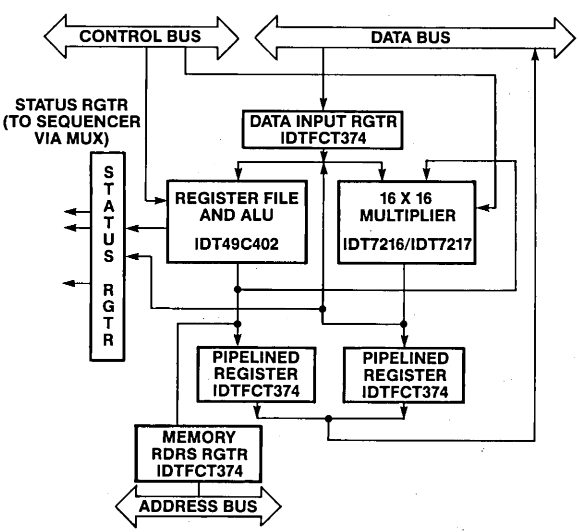
Figure 2. The Instruction Decoder and Microprogram Sequencer

to the 2901 and has 64 registers in the register file. There are eight additional destination functions that allow direct loading of the Q register or the RAM, thereby enhancing the overall performance. The additional destination functions are shown in Table 1.

If multipliers are used in the data path, the pipelined delay of 35ns for the IDT7216/IDT7217 (16 x 16 multipliers) is far less than the sequencer delays and ALU delays. The other data path of concern is a multiplier output that is added in the IDT49C402, shown as Path 2 in Figure 5. It is only 45ns, less than both the Data Path 1 delay and the Control Path delay. The IDT7216 is pin and functionally compatible to the TRW MPY-016H/K and Am29516. The IDT7217 is pin and functionally compatible to the Am29517. If a multiply-accumulate function is required, an IDT7210/IDT7243 (16 x 16 MACs) can provide sum-of-products at 35ns clocked speeds. The IDT7210/IDT7243 are pin and functionally compatible to the TRW TDC1010/1043 multiplier-accumulators. Generic block diagrams for the multipliers and multiplier-accumulators are shown in Figures 7 and 8.

The multipliers operate on unsigned two's complement or mixed mode numbers. In every clock cycle, a 32-bit product is generated and either the least significant or the most significant half can be read through the output lines. The least significant of the product is also shared with the Y_{0-15} input lines. IDT7216/IDT7217s are capable of running at 35ns clocked multiply rates over the commercial temperature range and 40ns over the military temperature range.

The multiplier-accumulator, IDT7210, provides the multiply, multiply-add and multiply-subtract functions. Three bits of overflow are provided, corresponding to a 35-bit accumulator. The IDT7243 is a trimmed version of the IDT7210 that does internal accumulates of 35 bits; but only the most significant 19 bits are available externally. Also, the IDT7243 has no preload capability. The multiply-accumulate operations can run at 35ns clocked speeds for the commercial temperature range. The summarized performance is shown in Table 2.



DSPAN04-003

Figure 3. The Address and Data Calculations Unit

Blazing fast speeds of the multipliers are needed in systems where the operands are of longer wordlength (>16 bits). For example, if fixed-point 32-bit operands are to be multiplied, four partial products have to be added, as shown in Figure 9. The four partial products can be generated in parallel using four multipliers and adding the partial products at their appropriate binary weighting. Alternately, the partial products can be added using one multiplier while doing shift and add operations in the IDT49C402, using the register space efficiently.

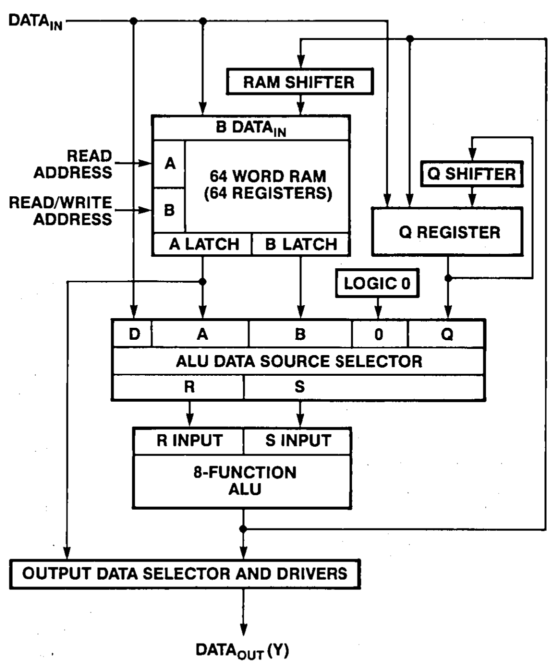
Pipeline register CLK-Q	10ns
Condition MUX (74F251)	13ns
IDT49C410: CC to Y	16ns
WCS RAM; IDT71682	25ns
Pipeline Register Set-Up	2ns
Total	64ns

Figure 4. The Control Path Delay

Pipeline register CLK-Q	10ns
IDT49C402:A/B to F = 0	37ns
Status Register Set-Up	2ns
Total	49ns

CLK-Q, IDT7216/IDT7217	25ns
Data to RAM, Set-Up	20ns
Total	45ns

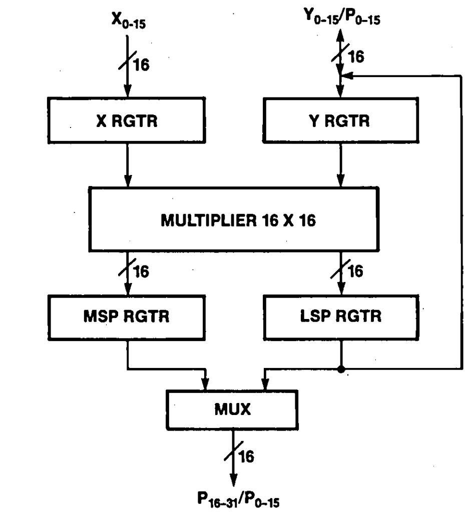
Figure 5. The Data Path Delay



DSPAN04-006

Figure 6. The IDT49C402 Block Diagram

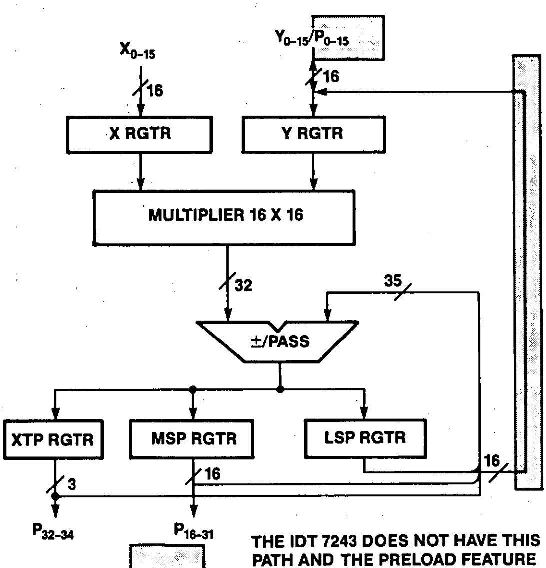
In the example shown in Figure 9, the partial product XA·YA is stored in two locations of the register file. The Most Significant (MS) part of XB·YB is added to the Least Significant (LS) part of XA·YB; the carry-out is saved for the next addition to the LS part of XB·YA. The carry-out again is saved for the next operation for



IDT7216 HAS SEPARATE CLOCKS FOR THE REGISTERS.
IDT7217 HAS A COMMON CLOCK AND SEPARATE ENABLES.

DSPAN04-007

Figure 7. The IDT7216/IDT7217 Multiplier Block Diagram



DSPAN04-008

Figure 8. The Block Diagram of the IDT7210/IDT7243

the additional of the MS part of the XB·YA and XA·YB. This result is added to the LS part of XA·YA. Finally, the sign extension of the previous operation is added to the MS part of XA·YA. By using the register file of the IDT49C402 efficiently, one does not have to perform 16-bit shifts with each partial product addition, resulting in a fairly efficient 32 x 32 multiplication.

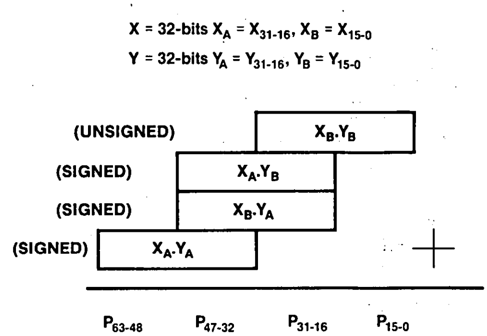
A high-speed 12MHz fixed-point processor can be built using the parts shown in Figures 2 and 3—namely the IDT39C10 12-bit sequencer or the IDT49C410 16-bit sequencer, the IDT49C402 16-bit ALU, the IDTFCT374, the IDT71682 RAMs, the IDT7216/IDT7217 multipliers or the IDT7210/IDT7243 multiplier-accumulators.

FLOATING-POINT PROCESSORS

In applications that need a larger dynamic range, floating-point number representation is used. A discrete solution to a 32-bit floating-point processor can be at least one board of SSI and MSI. Most designers prefer an IC or an IC set that implements the IEEE standard over a discrete solution. The implementation problem only worsens for double precision 64-bit floating point processors. The IDT72064/IDT72065 and IDT72264/IDT72265 provide compact, low-powered high-speed solutions to single-, and double-precision IEEE standard 754 version 10.0 calculations.

The IDT72064/IDT72264 are floating-point multipliers; the IDT72065/IDT72265 are floating point ALUs. All the parts have similar I/O structures. Data input and output transfers may occur at twice the maximum pipeline rate, allowing the devices to be used in a variety of bus configurations without degrading performance. The detailed block diagram of the IDT72264 is shown in Figure 10. The detailed block diagram for the IDT72265 is shown in Figure 11. Note that, in Figure 10, the IDT72264 takes two cycles for 32-bit operations and four cycles for 64-bit operations. The IDT72064, very similar to the IDT72264, takes four cycles for a 32-bit operation and eight cycles for a 64-bit operation.

The multiplier and ALU can operate in two modes: one with pipelined levels and the other with the pipelined registers made transparent (called the flow-through operation in the data sheets). For example, the multiplier in Figure 10 can have the following registers made transparent: PIPE1 and the STREG (Status Register), DM and DL registers. This allows the operands to "ripple" through the logic circuitry at a slower time, as compared to the pipelined case. A similar configuration is possible for the ALU,



DSPAN04-009

Figure 9. Partial Products for a 32 x 32 Multiply

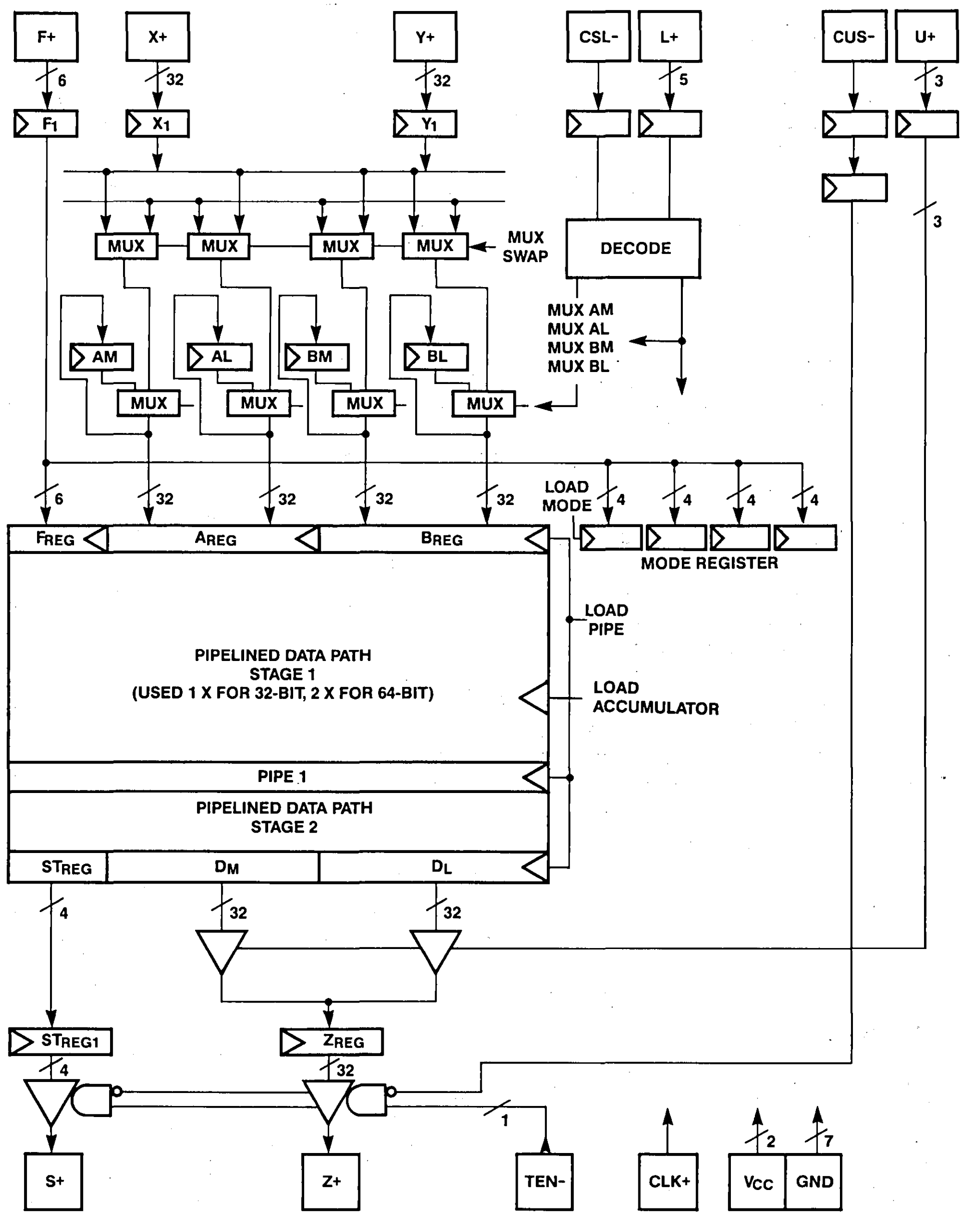


Figure 10. The IDT72264 Floating-Point Multiplier

14

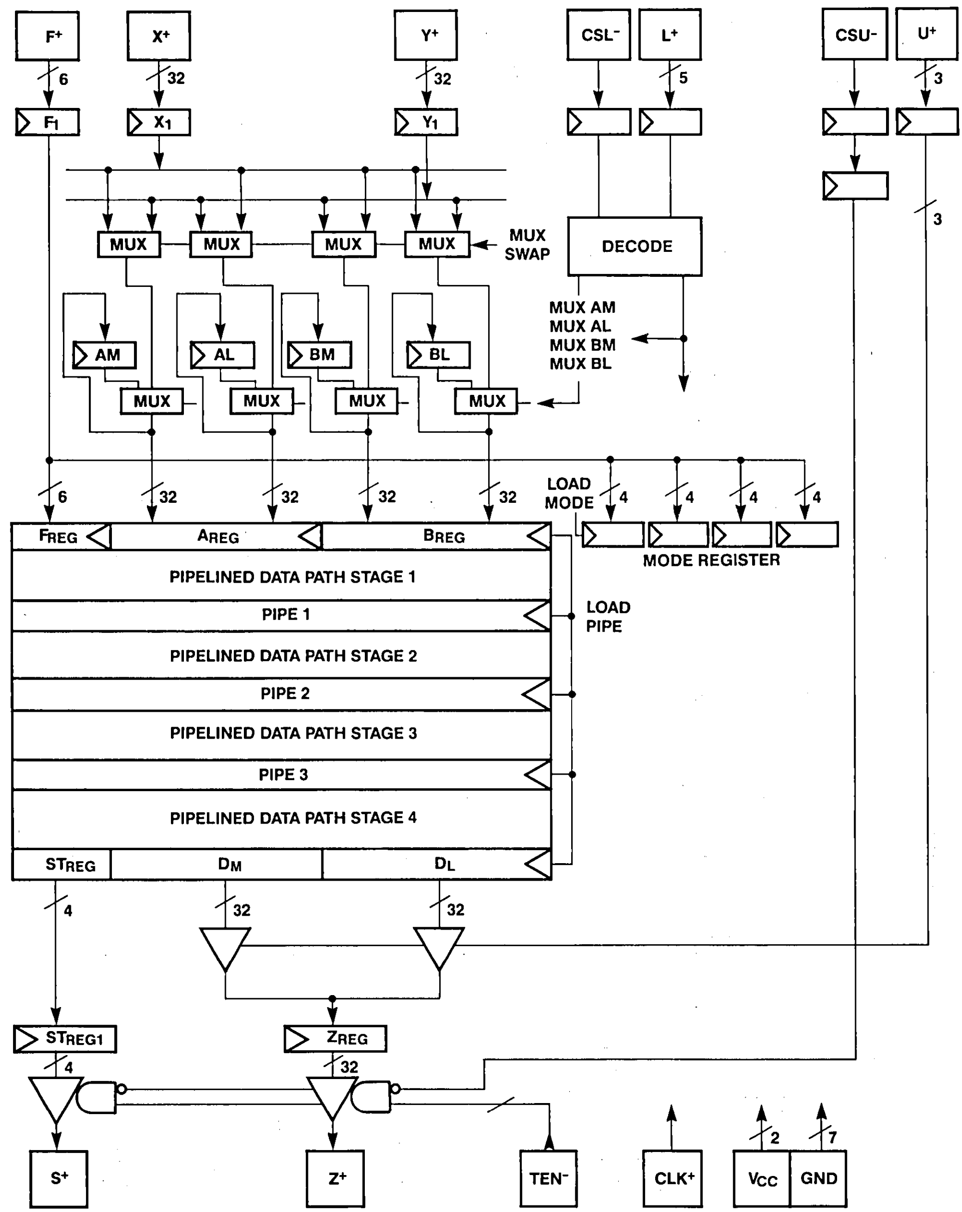


Figure 11. The IDT72265 Floating-Point ALU

shown in Figure 11, where the following registers can be made transparent: PIPE1, PIPE2, PIPE3, and STREG, DM and DL registers. The tradeoff in using pipelining is that one result is available every (pipeline) cycle once the pipe is full. Often this is a preferred method of computing if the pipe is not flushed. In the flow-through situation, one does not present any new operands to the inputs during the duration of the operating time. In a pipelined system, new values of X and Y are loaded every cycle and new results are read every cycle, with an understanding that the result being read currently is from operands loaded "n" cycles ago. "N" depends on the operation being performed and can range from 6 to 14.

The input stage allows easy interfacing to 16-bit, 32-bit, and 64-bit buses. The instruction set of the multipliers include single- and double-precision multiply and handling of wrapped multiply. A wrapped number is one that is smaller than the smallest representable number that is normally used. The ALU has a wide variety of instruction including add, subtract, convert, compare, negate, pass, wrap and unwrap for both single-precision and double precision operands.

The performance for these devices for the pipelined and flow-through operations are listed in Tables 3 and 4. These timings are based on a 50ns clock time. The IDT72064 and IDT72065 are compatible with Weitek's 1064 and 1065 in the IEEE mode. The IDT72264 and IDT72265 replace Weitek's 1264 and 1265. The performance is expected to be 20% faster when compared to currently available Weitek parts.

CONCLUSION

As the need for high-speed computing increases, so does the expected throughput of number-crunching chips. The availability of efficient building blocks from IDT allows users to build a 12MHz fixed-point processor and a 10MHz floating-point processor.

TABLE 1.
IDT49C402 16-Bit ALU Destination Functions

	RAM	Q	Y-OUT
2901 Functions (3-Bits I_6-I_8 I_9 HIGH	F-Up	Q-Up	F
	F-Up	—	F
	F-Down	Q-Down	F
	F-Down	—	F
	—	—	F
	—	Load F	F
	Load F	—	F
	Load F	—	A
Added IDT Functions (1 Additional Bit I_9) I_9 LOW	Load D	Load F	F
	Load D	Load F	A
	Load F	Load D	F
	Load F	Load D	A
	—	Q-Up	F
	—	Q-Down	F
	Load D	—	F
	—	Load D	F

TABLE 2.
Multiplier and MAC Performances

	Commercial	Military
IDT7216/IDT7217 16 x 16 Multiply Clocked Times	35ns	40ns
IDT7210/IDT7243 Multiply-Accumulate Clocked Times	35ns	40ns

TABLE 3.
The IDT72065/IDT72265 Performance

Single-Precision Pipelined Throughput	100ns
Single-Precision Latency	450ns
Double-Precision Pipelined Throughput	100ns
Double-Precision Latency	450ns

ALU Operations

TABLE 4.
The IDT72064/IDT72264 Performance

Single-Precision Pipelined Throughput	100ns	200ns
Single-Precision Latency	300ns	500ns
Double-Precision Pipelined Throughput	200ns	400ns
Double-Precision Latency	450ns	700ns

SEPARATE I/O RAMS INCREASE SPEED AND REDUCE PART COUNT

APPLICATION NOTE AN-05

INTRODUCTION:

Static RAMs with separate data inputs and data outputs, such as the IDT71681/71682 4K x 4-bit RAMs and the IDT71982/71982 16K x 4-bit RAMs, provide memory organizations that can improve system architecture in many applications. IDT makes a series of separate I/O RAMs, as shown in Table 1. In this application note, we will demonstrate several system ideas where RAMs with separate data inputs and data outputs offer improved system performance. Typically, the separate data inputs and data outputs eliminate the need for multiplexing of demultiplexing in the data path. Thus, not only is the output enable or disable time eliminated in a critical speed path, but a potential additional element (multiplexer or demultiplexer) may also be eliminated.

TABLE 1: IDT Separate I/O RAM CHIPS

Size	Organization	Outputs Track Inputs During Write	Outputs High Imped. During Write
16K	16K x 1	—	IDT6167
	4K x 4	IDT71681	IDT71682
64K	64K x 1	—	IDT7187
	16K x 4	IDT71981	IDT71982

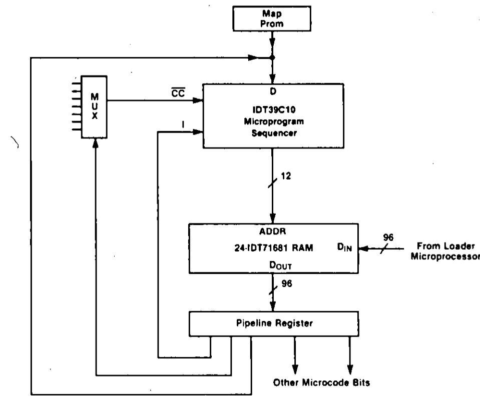


Figure 1. Typical Writeable Control Store in a Microprogrammed Machine.

SEPARATE I/O RAM APPLICATION EXAMPLES

MICROPROGRAM MEMORY

Separate I/O RAMs can be used in a high-speed writeable control store application and offer both speed improvement and a significant parts count reduction in the interface to a MOS microprocessor used to initialize the RAM at power up. Figure 1 shows a typical writeable control store design for a microprogrammed machine. Here we see an IDT39C10 microprogram sequencer driving the 12-address lines of the IDT71681/71682 4K word array. If we assume a microcode width of 96 bits, this design will use 24 of the IDT71681/71682 24-pin, 300 mil packages. As shown in Figure 1, the 12 address lines to all 24 packages are connected in parallel and are driven by the Y outputs of the IDT39C10 microprogram sequencer. This gives a total microcode depth of 4K words, which is sufficient for most microprogram applications. The four data outputs from each device provide microcode bits to the pipeline register to overlap the microinstruction fetching with the microinstruction execution. The pipeline register always contains the microinstruction currently executing, while the IDT39C10 is generating the next address to the RAM and the RAM is accessing the next microinstruction to be set up at the input to the pipeline register.

The advantages of using the IDT71681/71682 RAM in this application come from the speed of this device and from the parts savings associated with not having to demultiplex the data to be loaded into the memory. If the data path were to be bidirectional, such as would be required if we used the IDT6116 (2K x 8-bit RAM) on the IDT6168 (4K x 4-bit RAM), it would be necessary to demultiplex a MOS microprocessor data bus that provides the microcode at power up. This would require one 8-bit driver for each 8 bits of RAM to interface between the various RAMs and the 8-bit microprocessor data bus—an additional 12 parts in this case.

In a typical system, such as is shown in Figure 1, the microcode is read from a floppy disk and loaded into the writeable control store. An example of this type of microcode loading architecture as shown in Figure 2. The microprocessor system shown in Figure 2 requires three interface points to the writeable control store. First, you must define the address for the write operation. This is provided by means of a WCS address register to select which word in the writeable control store will be written into. Second, you must define the data you are going to write. This is provided by a data register which defines the data for a specific eight bits of the 96-bit word of the control store shown in Figure 1. A total of 12 bytes are required to load one microcode word into the writeable control store depicted in Figure 1. The specific byte to be written is selected by four additional address bits from the WCS address register which are directed to the decoder so that one of the 12 bytes can be selected for loading. Third, a control register is then used to select between the WCS load and operate modes and to manipulate the write enable (WRITE*) line connected to the decoder.

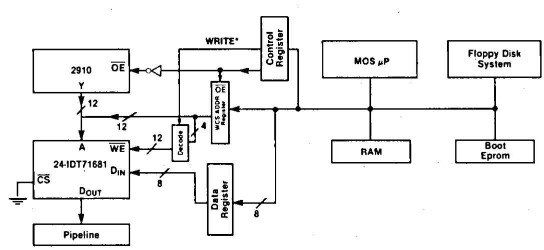


Figure 2. Autoload of the Writeable Control Store.

Printed in the U.S.A. 7/86

The complete cycle required can be described as follows. First, set up the control register to select the WCS address register onto the address bus and disable the IDT39C10 Y outputs. Second, move the address of the first byte to be loaded to the WCS address register. Third, move the data byte to be loaded to the data register. Fourth, change the WRITE* line from high-to-low-to-high by means of two MOS microprocessor I/O cycles. This will write one byte of data to the writeable control store memory. Continue by repeating the steps of loading the WCS address register, data register and then "writing" the data into the writeable control store memory.

A detailed connection diagram of the IDT71681/71682 interface to the MOS microprocessor is shown in Figure 3. Only 10 of the 24 devices are shown, but the connection scheme is similar for all 24-devices. The important point to recognize from the diagram is that the data-in lines are connected on a byte-wide basis. One IDT71681/71682 is connected to the D_0 to D_3 data inputs and the second IDT71681/71682 is connected to the D_4 through D_7 inputs. This means that each two devices are connected so as to accept one byte of data from the MOS microprocessor system. The 12 address lines to IDT71681/71682 are connected in parallel and are driven by a register with three state outputs such as the IDT74FCT374. The remaining address lines from the 29825 WCS address register are connected to decoders such as the IDT74FCT138. Each output for the IDT74FCT138 is connected to two write enable inputs on the IDT71681/71682 memories. This allows one byte to be written when the WRITE* line is changed high-low-high. The chip select line is simply grounded and not used in this application. As can be seen, the IDT71681/71682 offers a convenient interface in a writeable control store for external loading of the data. This connection concept can be extended and changed such that the writeable control store could be loaded with data provided by the host execution CPU itself, rather than the floppy disk.

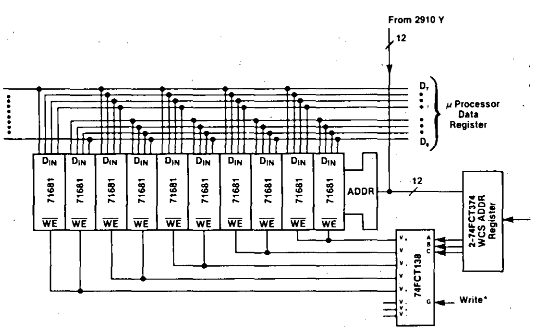


Figure 3. Detail of the MOS Microprocessor Interface to a Writeable Control Store.

VIRTUAL MEMORY AND MEMORY MAPPING

Separate I/O RAMs are ideally suited for use with MOS microprocessors to provide the memory mapping function associated with today's complex microprocessor operating systems. As shown in Figure 4, the IDT71681/71682 can be used to provide mapping from a microprocessor virtual address to a microprocessor physical address in main memory. In addition, status information about the map can also be present in the page table. In this example, a 24-bit virtual address is divided into a 12-bit virtual page consisting of 4K words per page. Depth into the page is provided by a 12-bit offset address. As shown in Figure 4, the 12-bit virtual page address can be connected to the page mapping memory and the resultant output will be a physical page address and status information. A detailed connection diagram is shown in Figure 5.

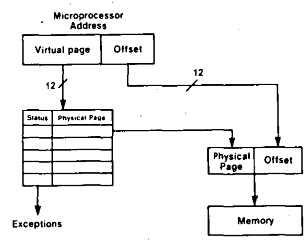


Figure 4. Memory Mapping.

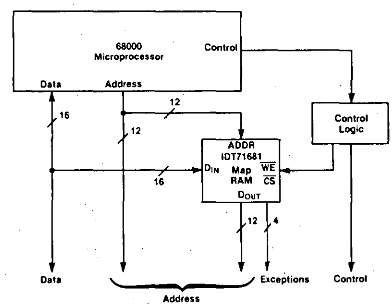


Figure 5. Memory Mapping.

A computer that provides any form of mapping other than the identity map between the central processing unit generated addresses and the physical memory address satisfies the most general definition of virtual memory. In Figure 5, we see the IDT71681/71682 address lines connected to the upper 12 bits of an address bus, such as those provided by the 68000 microprocessor. Here, the separate data output lines are used to provide mapped addresses as well as exception bit status vectors. The separate data-in lines can be connected to the data bus so that the page table provided by this memory is easily updated.

Many use the terminology of virtual memory in a more restrictive fashion. That is, a virtual memory is one where the actual physical memory is smaller than the total memory addressing capability of the machine. A page table memory map, such as that shown in Figure 5, is used to provide a translation from the virtual address to the physical address in such a memory. In a related definition called memory mapping, the physical memory is larger than the logical address space of the machine. This is often applied to such microprocessors as the 8085 and Z80. Here, the machine's logical address space is limited to 64K bytes, but it may be desirable to have a larger physical memory available to the machine. The connection scheme shown in Figure 6 can be used to perform this memory mapping. Some number of address lines, eight in this example, are connected to eight of the 12 IDT71681/71682 RAM address lines. The additional four RAM address lines are provided by a register and perform an additional mapping select function. The 12 RAM data output lines of the RAM are used in conjunction with the 8 remaining address lines from the microprocessor to provide a total of 20 address lines (1 megabyte) in this example. The 12 RAM data-in lines are connected to the data bus for easy loading of the page table.

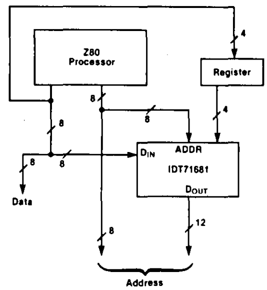


Figure 6. Z80 Memory Mapping.

Figures 5 and 6 indicate that some thought must be given to the exact mechanism for the address to be provided to the mapping RAM while it is being loaded. This can be handled in one of two ways. The simplest way is to provide an address register on one of the microprocessor I/O ports that is loaded with the target address, and then this address is used when the mapping memory is being written into. A more clever technique is to provide a control register that disables the main memory write and enables the mapping memory write such that no additional address register is required. Instead, data to be loaded into the mapping memory is simply moved to the address in the virtual space and is redirected to the mapping memory rather than the main memory.

Again, the examples of Figure 3 through 5 demonstrate the advantage of the IDT71681/71682 in having separate data inputs and data outputs.

CACHE MEMORY

A cache memory is a high-speed memory that is placed between the CPU and the main system bus. The purpose of a cache memory is to make a slow memory look like a fast memory. This is done by using two memories. The first is a small, high-speed memory called a cache memory, and the second is a large, slow memory called the main memory. Both memories are attached to the system bus which is connected to the CPU. The cache memory holds a copy of the most frequently used data in the main memory. If data requested by the CPU is in the cache memory, it responds first; if not, the CPU waits for the data from the slower main memory. If the data and instructions being executed most of the time are in the cache memory, a performance improvement is realized. This is commonly the case because most programs consist of loops and small pieces of code which are executed repetitively, and these occupy a small number of memory locations. The hardware associated with the cache memory attempts to keep this data in the high-speed memory. The term "hit ratio" is used to describe the number of times the data or instructions are in the cache memory versus the total number of memory accesses. It is not unusual to find hit ratios in the 90 percent range for some cache memory designs.

One of the most common cache memory organizations used is called the direct mapped cache memory. Figure 7 shows the block diagram for the implementation of the typical direct mapped cache. In this implementation, the cache memory consists of three main parts. These are the tag store, the data store and the match comparator. In the example shown in Figure 7, the tag buffer and data RAM are each 4K words deep using one row of the IDT71681/71682 static RAMs. The high order 12 bits of the address can be stored in the tag RAM so as to specify the unique memory space for which the data corresponds. The tag RAM usually contains additional bits which represent data validity and parity.

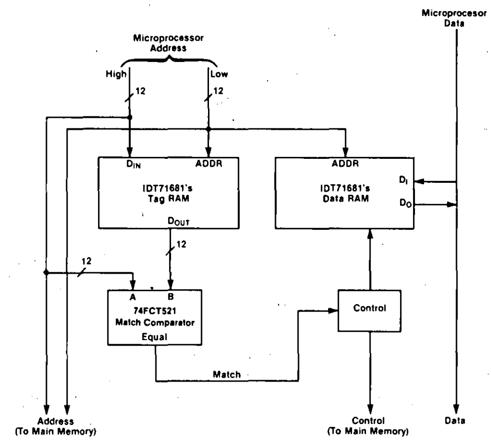


Figure 7. Direct Mapped Cache Memory.

The operation of such a cache memory is as follows. The microprocessor puts out an address on the address bus. The lower 12 bits are connected to the address inputs of the data and tag RAMs and cause the data and tag RAMs to begin fetching the word at the location. Then, the actual data value stored in the tag RAM is compared against the upper 12 address bits to look for a match. If a match is found, the valid bit is true and the data in the data RAM corresponds to the address on the address bus, we have a cache "hit" and the data in the data RAM is placed onto the microprocessor data bus. If no match is found or the valid bit is false, then a cache "miss" occurs and the data must be fetched from the main memory. As the data is brought in from the main memory to the microprocessor, it is also written into the data RAM and, at the same time, the tag RAM is loaded with the high order 12 address bits that represent the tag number from which the data was taken. Hopefully, the next time this address is used, it will still be in the cache memory.

STACK MACHINES AND HIGH-PERFORMANCE ALUS

A bit-slice microprocessor design can utilize separate I/O RAMs in the ALU architecture in several ways. A typical bit-slice microprocessor ALU configuration is shown in Figure 8. Here we see the IDT71681/71682 configured with its data inputs connected to the Y output of the 2903 bit-slice, and its data outputs connected to the DA input of the 2903 bit-slice. Two uses for such a connection are obvious. First, it is possible to use the tightly coupled RAM to increase the number of registers available to the

ALU. This could be used in certain high-performance algorithms such as floating point, Fast Fourier Transforms (FFTs), etc. Similarly, this register set might be used to allow very high-speed context switching of the processor ALU section. In this fashion, no register would have to be updated during the handling of interrupts or other system/user context switches.

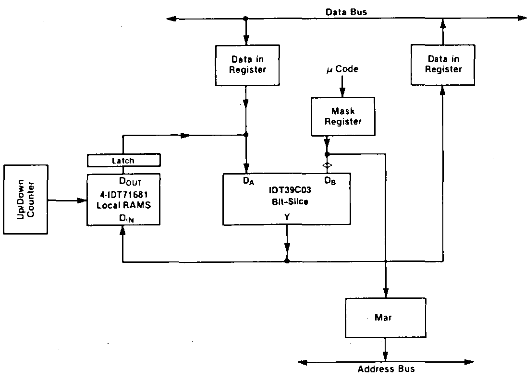


Figure 8. Stack Machines and High-Performance ALUs.

Another use for the IDT71681/71682 RAM shown in Figure 8 would be to provide a local stack for the ALU. This could be implemented using an up-down counter to drive the address lines to the RAM and the appropriate microcode to control pushing and popping of the stack. One or more such stacks could be very useful in high level language machines. For example, two such stacks might be used in a FORTH machine. One stack would be the operand stack, while the second stack would be the return stack.

A typical TTL ALU implementation is shown in Figure 9. Here, an MSI ALU, such as the 74S181, is used in a microprogrammed environment. Local register/accumulator storage is provided by IDT71681/71682 memories. The A and B inputs to the ALU are driven by the accumulator A and accumulator B RAM register/stack, respectively. Again, the advantage of the separate data inputs and data outputs is well displayed.

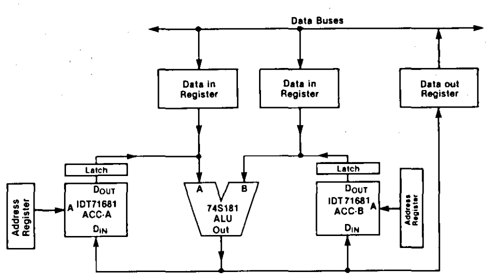


Figure 9. TTL ALU Implementation.

VIDEO DISPLAY CONTROLLER

The video display controller shown in Figure 10 can utilize separate I/O RAMs in two different ways. One area of the video display controller, the character generator, uses two IDT71681/71682s to hold 512 different 5-by-7 dot characters. In this configuration, the CRT controller provides the address to the character generator which generates the dot pattern for a particular line in the selected character. By using RAM in the character generator, the character font can be controlled by the host microprocessor and changed as often as desired. Two additional IDT71681/71682s are used for the screen refresh RAM. In this application, two RAM chips provide the local storage for the characters on the screen. Since a standard 24-row-by-80-column CRT display represents almost 2K bytes of data, the screen refresh RAM shown can store up to two pages of information for display.

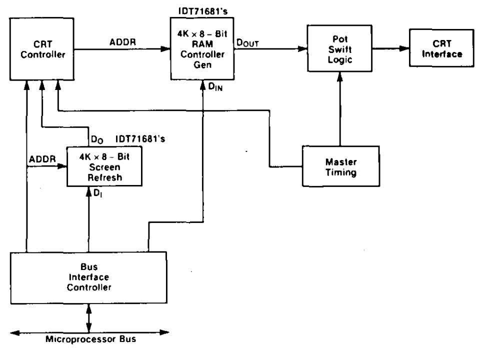


Figure 10. Video Display Controller.

DIGITAL FILTERS

The four-sample non-recursive digital filter in Figure 11 is another application which demonstrates the importance of separate data inputs and data outputs in the RAM memory. In this example, a 4096 word range-gated filter is shown. Digital filters consist primarily of memory, multipliers and adders. Range-gated filters are used in systems that quantify and otherwise process distance-related measurements such as radar, sonar and ultrasonic medical diagnostic instruments. Typically, the return signal is divided into increments of time (or distance) where each increment is to be individually processed. Thus, many different elements are to be processed and all may share the same multipliers and adders. However, different memory locations are needed for each time-sequential element. The example shown in Figure 11 can best be understood with the following description: the current output is equal to the sum of the present sample times the constant A_0, plus previous sample times the constant A_1, plus the second previous sample times the constant A_2, plus the third previous sample times the constant A_3. Four samples participate in generating each output, and because only input samples contribute to the output, the filter is said to have a finite impulse response.

Similarly, Figure 12 shows a range-gated recursive digital filter. It is similar in concept to that shown in Figure 11, except that a recursive filter contains feedback. Because feedback terms contribute to the output, it has an infinite impulse response. Again, separate I/O RAMs provide a unique performance advantage in this application.

Depending on the write timing, it may be necessary to place either latches or registers at the input or output of the RAMs shown in Figure 11 and 12.

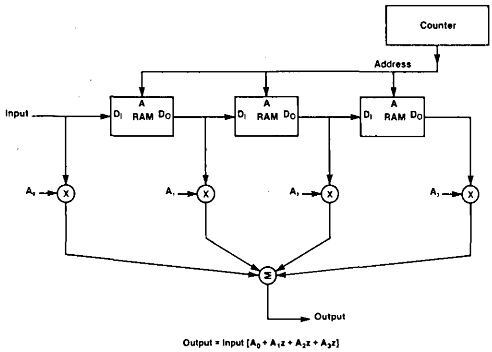


Figure 11. Four-Sample Non-Recursive Digital Filter.

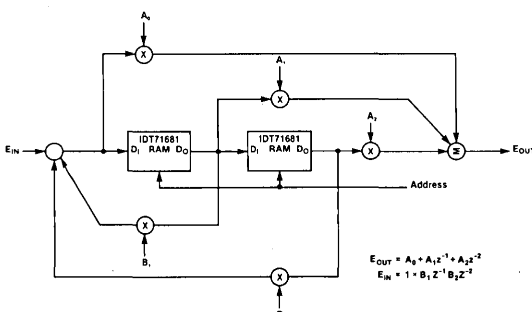


Figure 12. Recursive Digital Filter.

PING PONG RAM

A common problem in digital signal processing is the word-by-word transformation of a block of data, such as adding a constant to each word. This tranformation is usually done by reading each word from on RAM, modifying the data and writing the word into a second RAM. This type of operation may be done several times, with different transformations on each pass. This requires at least two RAMs. It is desirable to use a single bus system to tie the RAMs to the transformation logic, so that only one set of transformation logic is required.

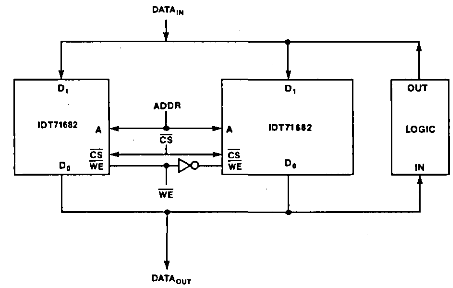


Figure 13. Pin Pong RAM.

A significant speed improvement in a common bus design can be realized by using two separate I/O RAMs in an alternate read/write mode, as shown in Figure 13. In this approach, data is initially read from the first RAM while transformed data is being stored in the second. Then, by changing the state of the $\overline{WE}$ input, data is read from the second RAM and new data can be written into the first RAM. In this fashion, one RAM is always in the read mode and the other is in the write mode. The $\overline{CS}$ can be used to remove both RAMs from the $DATA_{OUT}$ bus so it can be used by other devices. The $\overline{CS}$ line MUST be set inactive during a change of address to the RAM in the example shown in Figure 13. A speed improvement is realized in this configuration because the "data valid to end of write" time is faster than the "write cycle" time. This allows external logic to be performed on the $DATA_{OUT}$ and the result to be written back into the RAM at an overall higher system speed. In some designs, timing advantages can be realized by separating $\overline{CS}$, $\overline{WE}$, or both.

SUMMARY

Separate I/O CMOS static RAMs can provide the system designer with increased speed and reduced part count and their versatility will be demonstrated by creative design engineers in numerous applications beyond those discussed in this application note. These devices offer high-speed access times and high-speed cycle times. The low power inherent in CMOS allows new levels of performance to be achieved in small, compact designs without the thermal problems of earlier bipolar designs. Certainly, these devices offer the system design engineer another tool in the search for improved system performance.

Integrated Device Technology, Inc.

16-BIT CMOS SLICES — NEW BUILDING BLOCKS MAINTAIN MICROCODE COMPATIBILITY YET INCREASE PERFORMANCE

APPLICATION NOTE AN-06

by Michael J. Miller

INTRODUCTION

The electronics industry has been an evolutionary succession of dominating technologies. This has been true for semiconductor devices in general, as well as the product family called bit-slice microprocessors. With the extinction of each technology and the emergence of the new, there is an associated transition for both the manufacturer and the consumer. Each company seeks to minimize the effort of this transition.

In the 1950s it was a generation of germanium diodes and transistors. During the 1960s, silicon transistors and bipolar ICs dominated. The last decade saw the emergence of the NMOS microprocessor and dynamic memories. This decade will be dominated by very high-speed CMOS as the primary volume process. This evolution is not only taking place with the industry but, in specific, with the microprogrammed bit-slice microprocessors. Today very high-speed, low-power CMOS is taking the place of high-speed bipolar. CMOS is capable of operating faster and at 1/5 to 1/10 the power of bipolar technologies. Because of this, CMOS is becoming the technology of choice for bit-slice microprocessors.

In the past, technological changeovers have been expensive to the manufacturer as well as the consumer. The MICROSLICE™ Family from IDT seeks to facilitate this transition by offering two families of CMOS bit-slice devices: IDT39C000, IDT49C000. The IDT39C000 family provides high-speed CMOS devices that fit into the sockets of current designs which utilize the 2900 family of bit-slice devices. The IDT39C000 family is pin-for-pin compatible to the 2900 family as well as compatible with its highest speed grade. An easy upgrade path is provided by the IDT49C000 family of bit-slice devices. This family starts off by providing higher densities (families of 16- and 32-bit), improved architecture and progresses on into innovative architectures of the future.

RE-EMERGENCE OF MICROPROGRAMMING

As a result of CMOS, bit-slice microprogram designs are experiencing a new renaissance. In the mid-70s, the emergence of the 2900 family, as heralded by the 2901, was designed entirely using TTL bipolar technology. The 2901 has progressed from a propagation time — A/B to $\overline{G}/\overline{P}$ equal to 80ns — to the 2901C which sports 37ns. To achieve these final speeds though, the total TTL design had to be abandoned and ECL was substituted for the inner workings of the 2901, with TTL buffers interfacing to the outside world. Today at IDT, very high-speed CMOS is being used to produce an IDT39C01E with A/B to $\overline{G}/\overline{P}$ of 21ns, at 1/8 the power of the bipolar 2901C.

In parallel with the evolution of the 2901 has been the blossoming of the 2900 family to a multi-device product family. All of the latest designs use ECL internally. The trend in this family has been to add more and more gates on chip. To achieve this, though, more current has been consumed by each of the ICs starting with the 2901 at 1.25W to the 29300 family at approximately 8W. To handle the 8W, new packaging technology was developed which incorporates heat spreaders and cooling towers mounted on top.

Within the limits of maximum speed and density, tradeoffs can be made. For a given package, more speed can be achieved with less gates; or conversely, more gates can be incorporated at the expense of overall speed in critical paths. This relationship is referred to as the speed/power product of a given technology. The bipolar 2900 family has been extended to the limit of feasible packaging and cooling technology because of the density and speed requirements of today's applications. Very high-speed CMOS, in contrast, has a speed/power product an order-of-magnitude smaller than bipolar for the same speed. Therefore, CMOS requires less expensive packages and cooling systems.

COMPARISON OF FAMILY PERFORMANCE(1)

	MICROSLICE		BIPOLAR		SPEED PATH
	SPEED (ns)	DYNAMIC POWER (mA)	SPEED (ns)	DYNAMIC POWER (mA)	
IDT39C01C	37, 25	30	37, 25	265	A/B → $\overline{G}/\overline{P}$, C_n → F = 0
IDT39C01D	28, 17	35	—	—	A/B → $\overline{G}/\overline{P}$, C_n → F = 0
IDT39C01E	21, 14	40	—	—	A/B → $\overline{G}/\overline{P}$, C_n → F = 0
IDT39C03A	52, 35	60	52, 35	350	A/B → $\overline{G}/\overline{P}$, C_n → Z
IDT39C10B	30	80	30	340	$\overline{CC}$ → Y
IDT39C10C	16	80	—	340	$\overline{CC}$ → Y
IDT39C203	52, 35	60	52, 35	350	A/B → $\overline{G}/\overline{P}$, C_n → Z

NOTE:
1. Reflects performance over commercial temperature and voltage range.

14

A decade ago, CMOS was noted for lower power and low-performance. Today, CMOS is capable of running at speeds faster than bipolar at 1/5 to 1/10 the power. Dramatically smaller power consumption and smaller gate sizes allow for even higher levels of integration to be achieved. In previous bipolar designs, an ALU, a barrel shifter and a multiplier each required a package of their own for heat dissipation, whereas CMOS can incorporate them all on one piece of silicon while still having room to include a reasonable amount of RAM. This means that CMOS has room to grow, thus providing for new innovative architectures in the future.

While the lower power consumption allows for more gates in the same package, there is also freedom to shrink the size of the packages because the package is being used less as a means of dissipating the heat. This is timely because consumers are requesting more and more in smaller volumes of space.

THE LATEST IN CMOS TECHNOLOGY

CEMOS™ is used to produce the MICROSLICE family with its two sub-familes — named, respectively, the IDT39C000 Family and the IDT49C000 Family. These families address microprogrammable designs of the present and future. CEMOS is a trademark for the proprietary CMOS process technology of IDT. CEMOS is an enhanced CMOS technology which includes such features as high ESD protection, latch-up protection and high alpha particle immunity.

MICROSLICE IN EXISTING DESIGNS

The IDT39C000 family allows the designer to take advantage of very high-speed CMOS in existing designs. This family is a pin-for-pin compatible family with the 2900 counterparts. By replacing the current 2900 parts with IDT39C000 parts in existing sockets, the power consumption of that portion of the circuitry may be reduced down to 1/5 to 1/10 of the bipolar power consumption at full operating speeds. The IDT39C000 family is specified around the highest speed grade versions of the current bipolar devices. Currently in the IDT39C000 family are two of the common ALU architectures, the IDT39C01 and the IDT39C03/203. Included in the family are the sequencers IDT39C10 and IDT39C09/11. The IDT39C705/707 are registered file expansions for the IDT39C03/203. The family also includes the 16 x 16 multipliers, IDT39C516/517, and the 16 x 16 multiplier-accumulator, IDT39C510. Not to be ignored, the IDT39C60 family is available for high-performance error correcting memory designs. This family also includes the first speed upgrade beyond the bipolar technology. The IDT39C01D is 25% faster than the 2901C, while the IDT39C01E exhibits speeds 40% faster than the 2901C.

THE IDT49C000 FAMILY, THE NEXT GENERATION

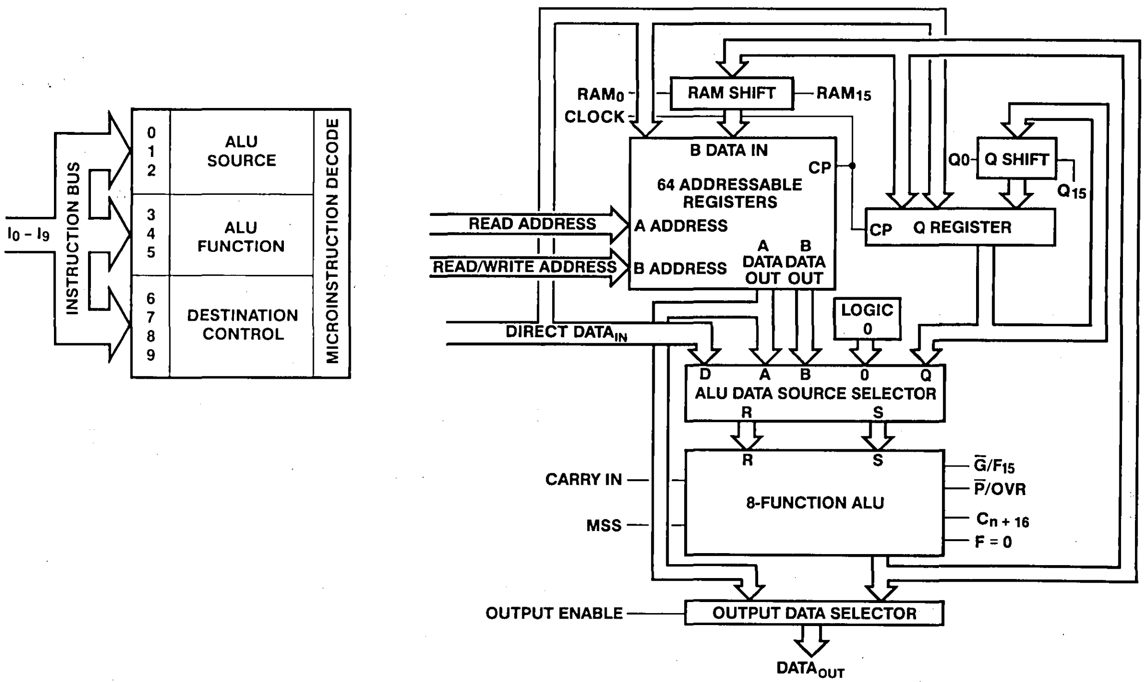
The IDT49C000 family takes advantage of all the benefits that CEMOS has to offer: high-speed, low-power, very large scale integration and smaller packages. Because of the new freedoms imparted by CEMOS, the IDT49C000 family is the next family of innovation for bit-slice microprogrammed designs.

While the IDT39C000 family minimizes upgrade costs by being pin-compatible, the IDT49C000 family addresses the aspect by providing parts in the family which are code-compatible, thus achieving conservation of previously written code. This is significant because, in the last decade, the cost of the software portion of the system has surpassed the hardware. The IDT49C000 family, however, is not limited to code-compatible devices and will, in the future, include devices with new and wider architectures.

THE IDT49C402A 16-BIT ALU PLUS

The first ALU in the IDT49C000 family is the IDT49C402A which is a 16-bit ALU and register file. This device is a superset of the 2901 architecture. It is a very high-speed, fully-cascadable 16-bit CMOS microprocessor slice, which combines the standard functions of four 2901s and one 2902 with additional control features aimed at enhancing the performance of bit-slice microprocessor designs. The IDT49C402A includes all of the normal functions associated with the standard 2901 bit-slice operation: (A) a 3-bit instruction field (I_0, I_1, I_2) which controls the source operands selection of the ALU; (B) a 3-bit microinstruction field (I_3, I_4, I_5) used to control the eight possible functions of the ALU; (C) eight destination control functions which are selected by the microcode inputs (I_6, I_7, I_8); and (D) a tenth instruction input (I_9) offering eight additional designation and control functions. This I_9 input, in conjunction with I_6, I_7 and I_8 allows for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU, and new combinations of destination functions with the RAM A-port output available at the Y output pins of the device. This eliminates bottlenecks of inputting data into the on-chip RAM.

The block diagram on page 3 shows the familiar architectures of the 2901 with register files which have both A and B data feeding into an ALU data source selector. This combines together the data from the register file along with direct data input (D) and the Q Register. The output of the ALU data source selector produces two operands, R and S. R and S are fed into an eight-function ALU, the output of which can go to the data output pins or be fed back into the register file and/or Q Register.



IDT49C402A 16-Bit Microprocessor Slice.

WHERE THE IDT49C402A EXCELS

The IDT49C402A, however, differs from the regular 2901 architecture by the addition of a new data bus that goes from the direct data input pins (D) into the register file and the Q Register, thus providing a data path directly into the register file and Q Register rather than passing through the ALU block. With conventional 2901 architecture, in order to get data into the register file the ALU must be placed in the pass mode taking data directly from the D inputs through the ALU and around to the register file. With this new architecture, data can be operated on out of the register file and the Q Register and the result placed back in the Q Register while new direct data is being brought into the register file. Conversely, the Q Register can be loaded while operations are being performed on the register file and placed back into the register file.

Whereas the 2901 has a 16-deep register file, the IDT49C402A has 64 addressable registers. The 2901 architecture does not allow for direct cascading of the register file. Dead cycles can be eliminated because 4 times more data can be cached on-chip with the ALU. Other applications may use the 64 registers as four banks of 16 registers. The bank selection could be thought of as task switching for interrupt-driven multi-tasked applications.

The third difference from the 2901 is the ALU expansion mechanism. The IDT49C402A incorporates an MSS input which programs the device, being the most significant device or not. When not the most significant slice, the P & G signals are brought out. When the most significant slice, the sign and overflow are brought out on the P & G.

IDT49C402A 16-Bit ALU Destination Functions

	RAM	Q	Y-OUT
2901 Functions (3-Bits I_6-I_8 I_9 HIGH	F-Up	Q-Up	F
	F-Up	—	F
	F-Down	Q-Down	F
	F-Down	—	F
	—	—	F
	—	Load F	F
	Load F	—	F
	Load F	—	A
Added IDT Functions (1 Additional Bit I_9) I_9 LOW	Load D	Load F	F
	Load D	Load F	A
	Load F	Load D	F
	Load F	Load D	A
	—	Q-Up	F
	—	Q-Down	F
	Load D	—	F
	—	Load D	F

14

CODE CONSERVATION

The microinstruction word of the IDT49C402A looks the same as the 2901 with the exception of the additional destination control line called I_9. Conservation of microcode can be achieved via two methods. The first and the most simple method is to tie the instruction line I_9 high on the socket and not connect it to the microcode. In this way, the remaining destination control lines I_8, I_7 and I_6 are compatible to the 2901.

For those systems that intend to add more code, or rewrite code for performance optimization, the second method is performed by making minor alterations on the microcode. For many designers this can be a fairly easily-achieved task by making minor alterations in the meta assembler used to compile the microcode source. The alteration in the meta assembler would add I_9 such that all previously written code would have this signal default to a Don't Care state of high, thus enabling the standard destination instructions (the traditional 2901 codes). Additional code could then be written which utilizes this instruction line and the extra features provided in the IDT49C402.

An alternative to the second method for achieving microcode compatibility would take the already-compiled microcode and run it through a simple program, written in another language, which would spread the microcode apart and introduce in this additional instruction bit. This method is used for microcode which no longer has existing source.

ONE IDT49C402A WINS RACE AGAINST FOUR 2901s

While the IDT49C402A seeks to improve performance through architectural enhancements, it also achieves improved performance through raw technology. The IDT49C402A achieves an A and B address to Y output of 41ns for military and 37ns for commercial temperature ranges, as compared to four 2901Cs and a 2902A which have A and B to Y and flag of 80ns for military and 68ns for commercial. Thus the IDT49C402A is 45% faster than five discrete parts of the older 2900 family. the IDT49C402A could achieve processing of approximately 15 MIPS.

COMPARISON OF 16-BIT MICROPROGRAMMED SOLUTIONS

	IDT49C402A CMOS	4 — 2901C & 2902A BIPOLAR	29116 BIPOLAR
Dynamic Power(1)	125mA	1049mA	735mA
ABI → Y/FLAG(1)	37ns	68ns	84ns
Package Space Sq. Inches	0.32 LCC 1.5 DIP	1.8 LCC 5.04 DIP	0.56 LCC 2.08 DIP
Features	ALU 64 RAM Q REG SHIFTER	ALU 16 RAM Q REG SHIFTER	ALU 32 RAM ACCUM BAR. SHIFT

NOTE:
1. Reflects performance over commercial temperature and voltage range.

THE IDT49C402A IS COOL

Even though the IDT49C402 has five times the circuitry on-chip as does the 2901, it is 1/2 the power of just one 2901.

The 16-bit solution of the IDT49C402A is 1/8 the power of four 2901Cs and one 2902A. While total power consumption is the concern of many designers because it has impact on power supplies and cooling systems, the lower power consumption also provides other benefits. Because less power is being consumed less of the package is needed as a heat sink. This allows for packages with much smaller outlines. Besides being offered in a standard 68-pin PGA, the IDT49C402A comes in a 68-pin dual in-line package with pins on 70 mil centers, 600 mils wide, which yields a package with an outline of 2.5 x 0.6 inches. A 68-pin LCC with pad spacing of 25 mil centers, as well as a standard 68-pin LCC with pad spacing of 50 mil centers, are offered. When the board space taken up by just the packages are added up, the LCC version of the IDT49C402A is 0.32 square inches, as opposed to 1.8 square inches for four 2901Cs and a 2902A. Respectively, the IDT49C402A in the SHRINK-DIP package (70 mil centers) is 1.5 square inches as opposed to 5 square inches for four 2901Cs and a 2902A. Not included in the calculations for the multi-chip solutions is the spacing between the ICs.

The next ALU, soon to be introduced in the IDT49C000 family, is the IDT49C403 which will be a 16-bit version of the 2903/203. This device will be at least as fast as the four 2903s and a 2902A, and will consume 1/5 to 1/10 the power of the multi-chip solution.

A 16-BIT SEQUENCER TO MATCH A 16-BIT ALU

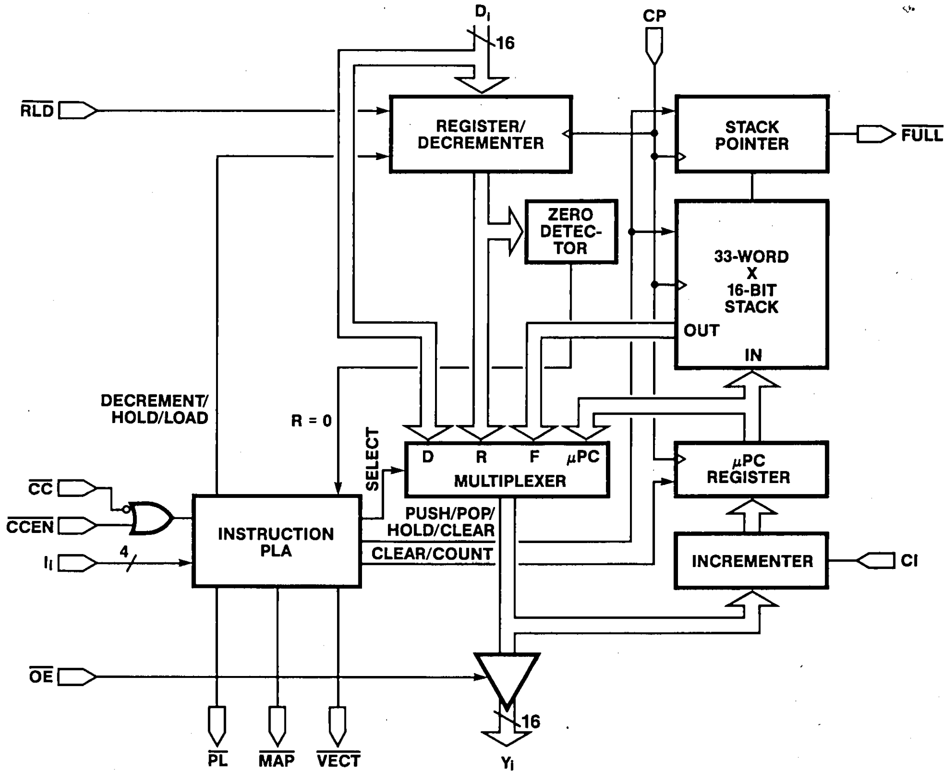
While ALUs provide the data path for performing computations, the sequencer is another important building block which orchestrates the entire machine. The first sequencer in the IDT49C000 family is the IDT49C410. The IDT49C410 is architecture- and function code-compatible to the 2910A, with an expanded 16-bit address path which allows for programs up to 64K words in length.

The IDT49C410 is a microprogram address sequencer intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the sequential accesses, it provides conditional branching to any microinstruction within its 64K word range.

While the 2910A incorporates a 9-deep stack, the IDT49C410 has a 33-deep stack which provides micro subroutine return linkage and looping capability. This deep stack can be used for highly nested microcode applications.

Referring to the block diagram on page 5, it can be observed that, during each microinstruction,the microprogram controller provides a 16-bit address from one of four sources: 1) the microprogram address register (μPC) which usually contains an address one greater than the previous address; 2) an internal direct input (D); 3) a register/counter (R) retaining data loaded during a previous microinstruction; or 4) a last-in first-out stack (F).

The IDT49C410 is completely code-compatible with the 2910A. This allows the IDT49C410 to execute previously written



IDT49C410 16-Bit Microprogram Sequencer.

microcode, while allowing for more microcode to be added to the application and taking the program beyond the 4K word boundary. Because the IDT49C410 is microcode-compatible, older microcode routines can be incorporated in new designs utilizing the IDT49C410.

The 16-bit IDT49C410 uses approximately 1/4 the power consumption of the 2910A (which is a 12-bit sequencer), thus maintaining the 1/5 power consumption on a bit-by-bit basis. The IDT49C410 consumes, over frequency and temperature ranges, 75mA for commercial and 90mA for military. The 2910A compares with 340mA for military and 344mA for commercial. Because of the lower power consumption, smaller packaging may be utilized. While the IDT49C410 is offered in a standard 600 mil wide package with pins on tenth inch spaces, it is also offered in a package which is 400 mils wide with pins on 70 mil centers. This is roughly 1/2 the standard package with regards to area taken up by each package.

COMPARISON OF MICROPROGRAM SEQUENCERS

	IDT49C410A	IDT49C410	2910A
$\overline{CC} \rightarrow Y$(1)	15ns	24ns	24ns
Stack Depth	33	33	9
Address Range	64K	64K	4K
Dynamic Power(1)	75mA	75mA	340mA

NOTE:
1. Reflects performance over commercial temperature and voltage range.

14

WORKING TOGETHER

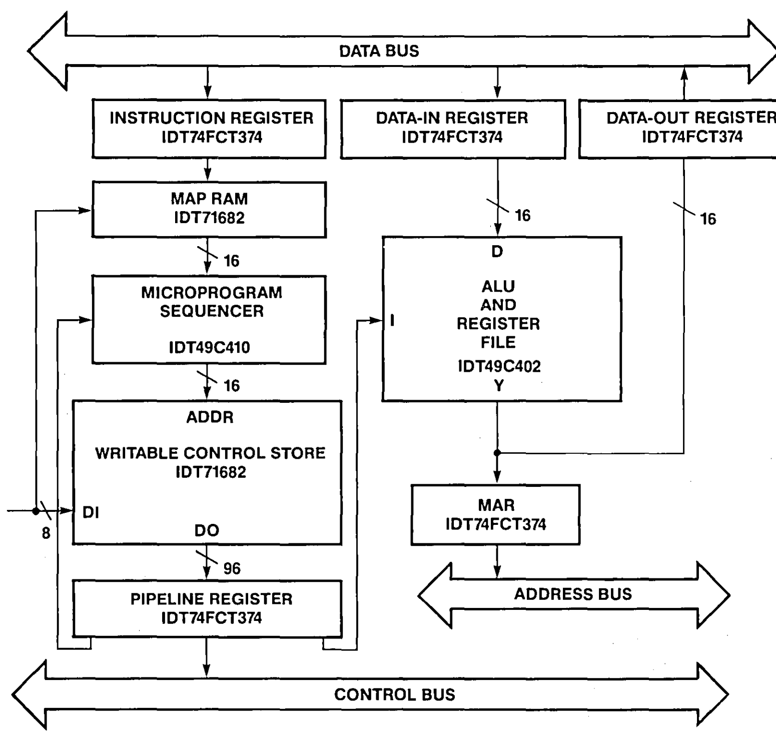
The simplified block diagram of an example Central Processing Unit (CPU) is shown below using devices manufactured by IDT. This CPU architecture can be viewed as two major sections which have a MICROSLICE family part at the heart of each. The major section of the left hand side of the diagram is the control path. The microprogram sequencer at the heart is the IDT49C410 which generates the address for the microprogram stored in the writeable control store (WCS). The output of the WCS is registered by the pipeline register. Together, the sequencer, WCS and pipeline register make up a state machine which controls the operation of the entire CPU. In this CPU, the state machine first fetches a machine instruction and captures it in the instruction register. The instruction register determines the starting address for each sequence of microinstructions associated with each machine opcode.

In this example, both the microprogram store and the instruction mapping memory are formed using RAM. The RAM has separate $DATA_{IN}$ and $DATA_{OUT}$ buses (IDT71682). This allows the input side to be connected conveniently to an 8-bit bus for initialization at power up.

The second major section is on the right hand side. This section is called the data path. The heart of this section is the IDT49C402A. In it is contained all of the working registers and the arithmetic logic unit for performing data computations. One of the internal registers always contains the value of the program counter (PC) which is the address at which the opcode for the machine instruction is fetched. When an opcode is fetched, the memory address register (MAR) is loaded with the value of the PC while, at the same time, the value of the PC plus one is loaded back into the internal register file. The $DATA_{IN}$ and $DATA_{OUT}$ registers are used to buffer data coming from and going to the memory during execution of the machine instruction.

CONCLUSION

The MICROSLICE family from IDT provides high-performance CMOS solutions for microprogrammed applications. Not only does the family provide for yesterday's designs with plug-compatible devices of the IDT39C000 family, it also provides solutions for future applications. With the IDT49C000 family, the designer can take advantage not only of the lower power consumption of CMOS, but utilize higher speeds and smaller board spacing, yielding smaller packaging concepts required by today's customers. In the future, the IDT49C000 MICROSLICE family will provide alternative architectures which will provide for yet higher performance solutions.



Integrated Device Technology, Inc.

CACHE TAG RAM CHIPS SIMPLIFY CACHE MEMORY DESIGN

APPLICATION NOTE AN-07

By David C. Wyland

ABSTRACT

Cache memories are a widely used tool for increasing the throughput of computer systems. The IDT7174 Cache Tag RAM is a new component designed to support direct mapped cache designs by providing the tag comparison on-chip. This allows relatively large cache memories to be designed with low chip count. The application of the IDT7174 to cache memory design is explored by designing a simple cache memory, reviewing its operation and performance, discussing methods of extending the design, and then reviewing the theory behind the design of cache memories in general.

INTRODUCTION

Cache memories are an important design tool for increasing computer performance by increasing the effective speed of the memory. Computer memories are usually implemented with slow, inexpensive devices such as dynamic RAMs. A cache memory is a small, high-speed memory that fits between the CPU and the main memory in a computer system. It increases the effective speed of the main memory by responding quickly with a copy of the most frequently used main memory data. When the CPU tries to read data from the main memory, the high-speed cache memory will respond first if it has a copy of the requested data. Otherwise, a normal main memory cycle will take place. In typical systems, the read data will be supplied by the cache memory over 90% of the time. The result is that the large main memory appears to the CPU to have the high speed of the cache memory.

The IDT7174 Cache Tag RAM introduced by IDT simplifies the design of high-speed cache memories. It can be used to make a high-performance cache memory with a low part count. The IDT7174 Cache Tag RAM consists of a 64K-bit static RAM organ-

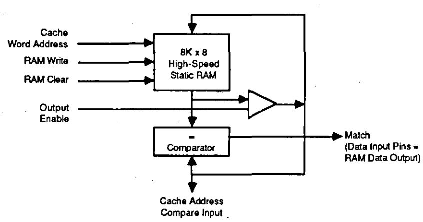


Figure 1: IDT7174 Cache Tag RAM Block Diagram

ized as 8K x 8 and an 8-bit comparator, as shown in Figure 1. The comparator is used in direct mapped cache memories to perform the address tag comparison, and allows a 16K byte cache for a 68000 microprocessor to be built with four memory chips. The IDT7174 also provides a single pin RAM clear control which clears all words in the internal RAM to zero when activated. This control is used to clear the tag bits for all locations at power-on or system-reset when the cache is empty of data. This allows one of the comparison bits to be used as a cache data valid bit.

DESIGN OF A CACHE MEMORY

To understand the application of the IDT7174 to cache memories, we will begin by designing one. A block diagram of a cache memory system using IDT7174 Cache Tag memory chips is shown in Figure 2. The cache memory serves a 16-bit microprocessor with a 24-bit address bus and a main memory. In this system, the 13 least significant bits of the address bus are connected to the address inputs of both the cache tag and the cache data RAM chips. The upper 11 bits of the address bus are connected to the data I/O pins of the cache tag RAMs. The remaining five I/O pins of the cache tag RAMs are connected to a logic 1 (+5).

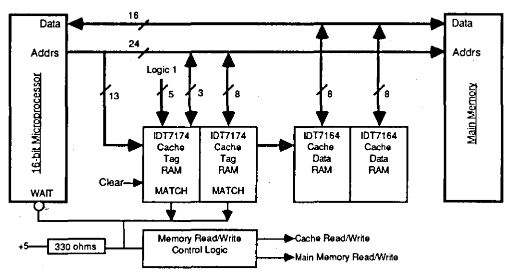


Figure 2: Cache Memory System Block Diagram

The MATCH outputs of the cache tag rams are tied together and connected to the WAIT input of the microprocessor. A 330 ohm pull-up resistor is used because the MATCH outputs are open-drain type. The MATCH outputs are positive-active. The MATCH output goes high when the contents of the internal RAM are equal to the data on the I/O pins. When several cache tag RAMs have their MATCH outputs connected together, a wire-AND function results: all of the comparators must each register a match before the common MATCH signal can go high.

In the system shown, the state of the WAIT input to the microprocessor determines whether the memory data is to come from the cache or the main memory. If the WAIT input to the microprocessor is high, the microprocessor will accept data immediately from the cache data RAMs; if the WAIT input is low, the microprocessor will wait for the slower main memory to respond with the data.

To understand how the cache memory operates, we will follow its operation from start-up in an initially empty state. When the system is powered-up, the cache tag RAMs are cleared to zero by a pulse to the initialize pins of the IDT7174 RAMs. This causes all cells in the RAM to be simultaneously cleared to logic zero. When the microprocessor begins its first read cycle, the 13 least significant bits of the address bus select a location in the cache tag RAMs. The location in the cache tag RAMs is compared against the upper bits of the address bus and against five bits of logic one.

The MATCH output of the cache tag RAMs will be low because all cache tag RAM cells were reset to zero, and the zeros from the selected cell are being compared against the five bits of logic one. In this case, the microprocessor waits for the slower main memory to respond. This is called a cache miss.

When the main memory responds with read data for the microprocessor, this data is also written into the cache data memory at the address defined by the 13 least significant bits of the address bus. At the same time, the upper 11 bits of the address bus and the five bits of logic one are written into the cache tag memory. This 11-bit address tag, in combination with the 13 bits of RAM address select, uniquely identify the copy of the main memory data that was stored. The five logic one bits serve as a data valid bits which indicate that the data in the cell is a valid copy of main memory data.

When the microprocessor requests data from the same location that has been written into the cache, the upper address bits on the address bus will be the same as the bits which were previously written into the cache tag RAM and the MATCH signal will go high. This is called a cache hit. In this case, the cache data is gated onto the data bus and the memory cycle is complete.

If the microprocessor requests data from an address with the same 13 least significant bits as a word in the cache, but with different upper address bits, a cache miss will result and the current (more recent) data will be written into the cache. In this manner, the cache is continuously updated with the most recently used data.

Memory write cycles are treated differently from read cycles. On write cycles, data is written directly into main memory and into the cache. This is called the write-through method of cache updating. Since all data is written immediately into main memory, it always contains current information. Data is written into the cache on full word writes or on byte (i.e. partial word) writes if a match occurred. Writing bytes into the cache only if a cache match occurs ensures that the full word in the cache is valid. For example, this ensures valid data for a byte write followed by a word read.

The design in Figure 2 uses unbuffered writes. In unbuffered writes, all write cycles occur at main memory speeds. This slows down the system for all write cycles at the expense of simple memory controls; however, this may be acceptable since only 15% of all memory cycles are write cycles in typical programs. Buffered write is a slightly more complicated method which improves performance. In buffered write cycles, the write data and address are loaded into registers, and the main memory write cycle proceeds in overlap with other processor operations. Since the next few cycles will probably be read cycles and their data will come from the cache, the result is that buffered write cycles are as short as cache read cycles.

CACHE MEMORY DESIGN: PERFORMANCE

Even a simple cache memory can improve system performmance. For a simple, 16-bit cache system such as described above, a hit rate (percentage of read cycles that are from the cache) of 68% can be expected. If IDT7174 Cache Tag RAMs and IDT7164 cache data RAMs are used, an access time at the chip level of 35ns results and a corresponding system cache read or write cycle time of 50ns is practical. Assuming a system cache access time of 50ns and a main memory system access time of 250ns, the average access time of an unbuffered cache would be 134ns and the average access time of a buffered cache would be 104ns. This corresponds to an improvement in access time of 1.9:1 and 2.4:1, respectively.

CACHE DESIGN DETAILS: CONTROL LOGIC

Figure 3 shows a block diagram of a control logic design and a typical timing diagram for the cache memory of Figure 2. The vertical lines in the timing diagram represent 50ns timing intervals. The microprocessor is assumed to have a 50ns clock and a 100ns memory cycle time. In the timing diagram and associated logic, a Read/Write Timing signal is used to determine whether to use the cache data or to start the main memory. This timing signal is the memory read/write request signal from the CPU delayed by 37ns; the address-to-match time of the IDT7174. If main memory is used, this timing signal is used to write the main memory data into the cache RAMs on both the main memory read and write cycles. Data is written into the cache on write cycles only if there is a match or if it is a word write operation. The state of the MATCH line is latched by the Read/write Timing signal so that it remains stable during cache write operations.

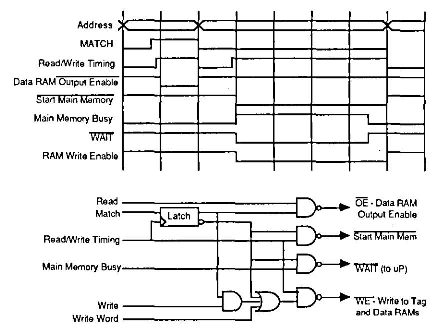


Figure 3: Cache Memory Control Timing and Logic Block Diagrams

CACHE DESIGN DETAILS: UNCACHED ADDRESSES

In the above cache design, we have assumed that all parts of memory are cached; however, there are significant exceptions to this assumption. Hardware I/O addresses should not be cached because they do not respond in the same way as normal memory locations. Bits in an I/O register can and must change at any time, asynchronously, with respect to the rest of the system. A cache copy of an earlier I/O state is clearly not a valid response to an I/O read request under these conditions. Also, an I/O register address may be used for different functions for read and write, so that what is read will not be the same as what was written. For example, write-only control bits will not appear when read, and read-only bits will not be affected by write operations. For these reasons, hardware I/O addresses must always force cache misses. This can be accomplished by adding an I/O address decoder to the memory address bus to force a cache miss. (This decoder aleady exists in many systems to enable the I/O subsystem.)

CACHE DESIGN DETAILS: DMA ADDRESSES

Direct Memory Access (DMA) allows I/O devices such as disk controllers to have direct access to main memory by temporarily stopping the CPU and taking control of the memory address and data busses. If DMA devices are allowed to write into main memory without updating the cache memory, cache data could become invalidated because it would no longer be a copy of the contents of main memory. The simplest solution to this problem is to have the cache monitor the memory bus and be updated if an address match occurs in the same manner as CPU write-through operations. Otherwise, the I/O DMA buffer areas of memory must be forced to be uncached in the same manner as hardware I/O addresses.

CACHE DESIGN DETAILS: EXPANDING THE CACHE IN WIDTH

The cache as described above, can be expanded in both width and depth. For a 32-bit system, two additional IDT7164 cache data RAMs (for a total of 4 chips) will be required to store the 32-bit data words. A block diagram of a 32-bit cache system, with a 32-bit address bus, is shown in Figure 4. Compared with Figure 2, the number of cache data RAMs has been expanded from two to four to handle the expansion of the data bus from 16 to 32 bits, and the number of cache tag RAMs has been expanded from two to three to handle the expansion of the address bus from 24 to 32 bits.

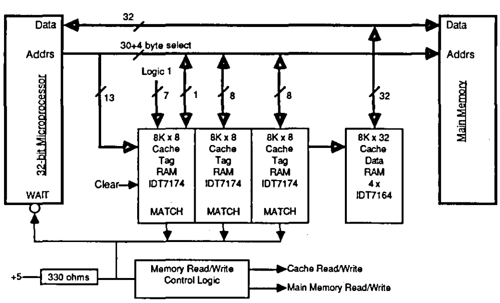


Figure 4: 32-Bit Cache Memory System

Note that the cache memory system uses the memory address lines corresponding to the 32-bit words stored in the cache. If a byte addressing memory address convention is used, the least significant bit of the address lines going to the cache RAM chips is A2, with A1 and A0 used to select the byte(s) within the word to be read or written in the cache data RAMs.

There is a benefit to expanding the cache width by adding data RAMs: the miss rate improves. The miss rate improves because of the increase in width, as well as in the amount of data stored. The miss rate for a 8K x 32-bit cache is estimated at 12.4%, as compared to 32% for a 8K x 16-bit cache. Doubling the cache width by adding RAM chips doubles the amount of data stored. We would expect an improvement in miss rate due to the increased probability of finding the data in the cache.

There is an additional improvement in miss rate, however, specifically due to the increase in width. This is because there is a high probability that the next word the CPU wants is the next word after the current one. If the cache width is doubled, there is a 50% probability that the next word is already in the cache, fetched from main memory along with the current word.

Studies have shown that the miss rate is cut almost in half for each doubling of the cache data word width — called line size in cache theory — up to 16 bytes and larger (Smith 85). The disadvantage of very wide cache data word width is either a wide main memory data bus or complex logic to transfer the word to the cache in a high-speed serial burst. Simply doubling the number of main memory cycles does not work well because you have doubled the effective access time of the main memory but have cut the miss rate by less than half, yielding a net decrease in performance.

CACHE DESIGN DETAILS: EXPANDING THE CACHE IN DEPTH

The cache memory can be expanded in depth by adding copies of the cache tag and data chips and using upper bits of the address bus for chip enable selection. An example of an expanded cache is shown in Figure 5. The primary reason for increasing the size of the cache memory is to decrease the miss rate percentage. For example, increasing the cache size from 8K x 16 to 16K x 16 decreases the estimated miss rate from 32% to 22%.

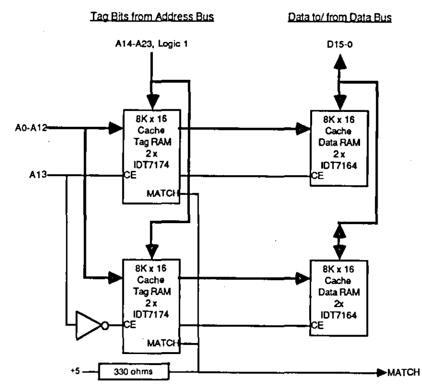


Figure 5: Depth Expanded Cache Memory System

CACHE DESIGN DETAILS: SET ASSOCIATIVE EXPANSION

A better way to expand the cache memory in depth is called set associative expansion (shown in Figure 6), and its control logic (shown in Figure 7). In this example, we have two independent cache memories which results in a two-way set associative cache. If a match is found in one of the memories, its data is gated to the data bus. If no match is found, one of the two memories is selected and updated. Selection of one of the two memories for cache write update is done by using an additional 8K x 1 memory to hold a flag for each cache word, indicating which memory was read last. This way, the least recently used cache word of the pair is updated.

The cache system described above attacks the problem of having two frequently used words mapped to the same cache word. For example, if a program loop included an instruction at 200B2 (hexadecimal) and called a subroutine at 800B2, the cache word 00B2 would be alternately registered as a cache miss and updated with memory data from each of these two addresses. The above design solves this problem by having two independent memories. One would cache the instruction at 200B2 and the other would cache 800B2.

Two way set associative expansion, while more complex in control logic, achieves a better miss rate. For example, the estimated miss rate for a 16K x 16 set associative cache is 18% versus 22% for a simple 16K x 16 cache.

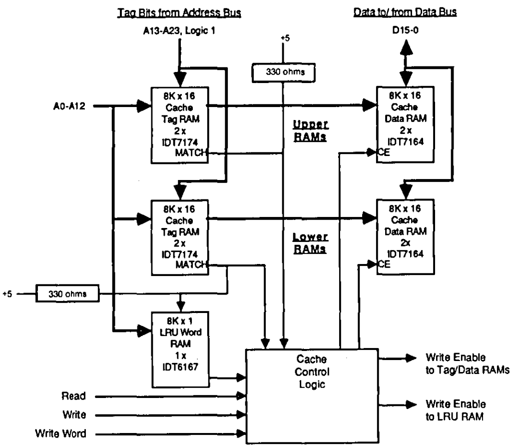


Figure 6: 2-Way Set Associative Cache Memory System

FUNCTION	MATCH	ACTION
Read	Yes	Enable corresponding data RAM for read
Write	Yes	Enable corresponding data RAM for write
Read	No	Write main memory data into LRU RAM
Write Word	No	Write data into LRU RAM

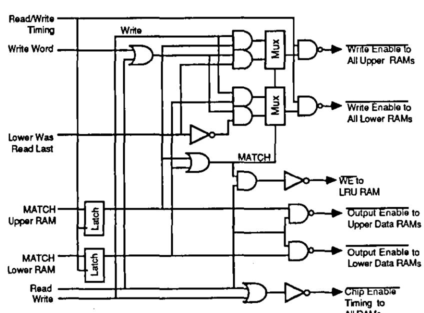


Figure 7: 2-Way Set Associative Cache Control Logic Block Diagram

CACHE THEORY: HOW IT WORKS

A cache memory cell holds a copy of one word of data corresponding to a particular address in main memory. It will respond with this word if the address on the main memory address bus matches the address of the word stored. A cache memory cell therefore has three components. These components are an address memory cell, an address comparator, and a data memory cell, as shown in Figure 8. The data and address memory cells record the cached data and its corresponding address in main memory. The address comparator checks the address cell contents against the address on the memory address bus. If they match, the contents of the data cell are placed on the data bus.

An ideal cache memory would have a large number of cache memory cells with each of them holding a copy of the most frequently used main memory data. This type of cache memory is called fully associative because access to the data in each memory cell is through its associated, stored address. This type of memory is expensive to build because the address cell and address comparator are generally several times larger, in terms of chip area or part count, than the data cell. Also, the address comparator required for each associative memory cell makes the design of the cell different from that of standard RAM memory cells. This makes a fully associative memory a custom design, precluding the use of efficient standard RAM designs.

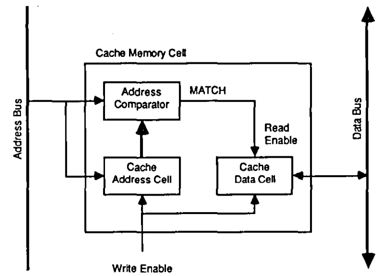


Figure 8: Cache Memory Cell Block Diagram

CACHE THEORY: WHY IT WORKS

Cache memories work because computer programs spend most of their memory cycles accessing a very small part of the memory. This is because most of the time the computer is executing instructions in program loops and using local variables for calculation. Because of this observation, a 64K byte cache can have a 90+% hit rate on programs that are megabytes in size.

HOW THE DIRECT MAPPED CACHE WORKS

The direct mapped cache memory is an alternative to the associative cache memory which uses a single address comparator for the cache memory system and standard RAM cells for the address and data cells. The direct mapped cache is based on an idea borrowed from software called hash coding which is a method for simulating an associative memory. In a hash coding approach, the memory address space is divided into a number of sets of words with the goal of each set having no more than one word of most-frequently-used data. In our case, there are 8K sets of 2048 words each.

Each set is assigned an index number derived from the main memory address by a calculation which is called the hashing algorithm. This algorithm is chosen to maximize the probability that each set has no more than one word of most-frequently-used data. In the direct mapped cache, the hashing algorithm uses the least significant bits of the memory address as the set number. This uses the concept of locality, which assumes that the most often used instructions and data are clustered in memory. If locality holds, the least significant bits of the address should be able to divide this cluster into individual words and assign each one to a separate set.

A memory map of a direct mapped cache of Figure 2 is shown in Figure 9 as an example of how the main memory words are related to the cache words. The 16M Word main memory is divided into 8K word pages, a total of 2048 pages. Each word within each 8K page is mapped to its corresponding word in the 8K words of the cache; i.e., word 0 of the cache corresponds to word 0 in each of the 2048 pages (8K sets at 2048 words/set).

Each word in the cache stores one word out of its set of 2048 corresponding to one of the 2048 possible pages. Both the data word and the page number (i.e. upper address bits), are stored.

Since only one word in each set (one of 2048 words in our case) is assumed to be one of the most-frequently-used words, each set has a single cache memory cell associated with it. This cache cell consists of an address cell and a data cell, but no comparator. One comparator is used for the cache memory system since only one set can be selected for a given memory cycle and only one comparison need be made. In a memory cycle, one set is selected, and the single cache address cell for that set is read and compared against the memory address, and the data from the cache data cell is placed on the bus if there is a match. The advantage of this scheme is that a single comparator is used, allowing standard RAM memories to be used to store the cache address and data for each set.

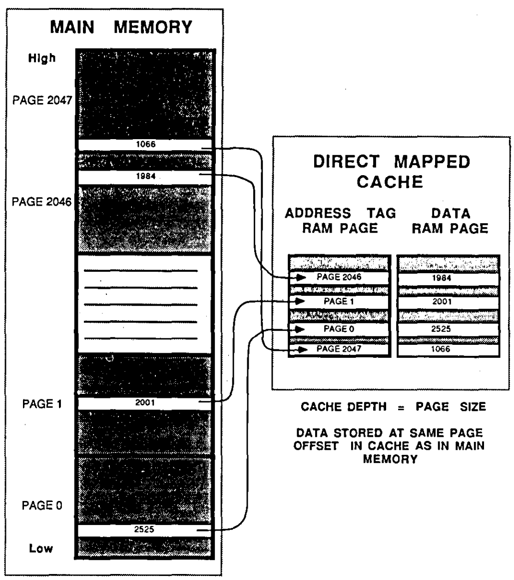


Figure 9: Cache System Memory Map

The cache cell for each set should hold the data that was most frequently used. However, since we do not know which data was the most frequently used until after the program is run, we approximate it by storing the most recently used data and replacing the least recently used (oldest) data. In the direct mapped cache, this is done by replacing the cache cell contents with the newer main memory data in the case of a cache miss.

CACHE PERFORMANCE

A cache memory improves a system by making data available from a small, high-speed memory sooner than would otherwise be possible from a larger, slower main memory. The performance of a cache memory system depends upon the speed of the cache memory relative to the speed of the main memory and on the hit rate or percentage of memory cycles that are serviced by the cache.

The cache performance equations below express the idea that the average speed of the cache memory is the weighted average of the cycle times for cache hits plus the main memory time for cache misses, with memory writes dealt with as a special case of 100% cache miss or 100% cache hit for the unbuffered and buffered cases, respectively.

CACHE SYSTEM PERFORMANCE: MISS RATE

One of the key parameters in a cache memory system is the miss rate. Miss rate figures are estimates derived from statistical studies of cache memory systems. The miss rate is an estimate because it varies, often significantly, with the program being run. Miss rate estimates for various cache memory configurations are given in Table 1. Miss rates for one example of two-way set associative expansion are also shown in this table.

Size: Words/Tag RAM	Miss Rate for Cache Data Word Width - Bits				Notes
	16	32	64	128	
2K	0.57	0.23	0.10	0.04	
4K	0.40	0.18	0.07	<0.04	
8K	0.32	0.12	0.05	<0.04	
16K	0.22	0.09	<0.04	<0.04	
16K (8K + 8K)	0.18	0.07	<0.04	<0.04	2-way Set Assoc

Table 1.

The miss rate estimates given in Table 1 are derived from simulation studies. (See references.) These studies covered cache sizes of up to 32K bytes and cache data word widths (called line sizes in cache terminology) from 4 bytes through 64 bytes. In the case of 16-bit word width caches, the figures given are extrapolations from the 32-bit data. Also, the figures for cache sizes above 32K bytes (i.e., 16K x 32, etc.) are extrapolations from 32K byte data.

CACHE SYSTEM PERFORMANCE FOR READ CYCLES

Cache memory system performance is determined by the access time of the main memory, the access time of the cache, the miss rate (the percentage of memory cycles that are not serviced by the cache) and the write time. The effective access time of a cache memory system can be expressed as a fraction of the main memory access time. This dimensionless number, Ps, is a measure of cache performance. If we consider read cycles only, the access time of a cache memory system is:

$$Ts = (1 - M)Tc + MTm = \underline{(1 - M)Tc + MTm}$$

$$Ps = Ts/Tm = (1 - M)\ (Tc/Tm) + M = \underline{(1 - M)Pc + M}$$

Where:

- Ts = Cache average system cycle time, averaged over read and write
- M = Miss rate of cache
- Tc = Cache cycle time, read or write (assumed to be equal)
- Tm = Main memory cycle time, read or write (assumed to be equal)
- Pc = Cache memory access time as a fraction of main memory cycle time
- Ps = Cache system access time as a fraction of main memory access time

If the miss rate of a cache memory is 100%, Pc = 1.00. If the cache memory is infinitely fast corresponding to a cache access time of zero, Pc will be equal to the miss rate, M. For real cache memories, the access time of the cache is finite. This means that the cache system access time will approach the cache access time as the miss rate approaches zero. This is shown in Figure 10.

14

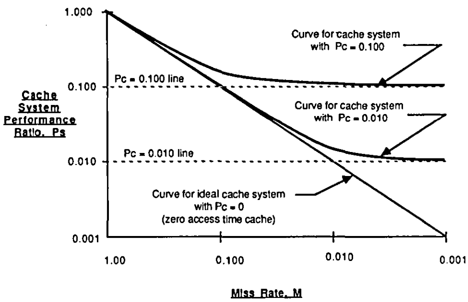


Figure 10: Cache Access Time vs Miss Rate for Read Cycles

CACHE SYSTEM PERFORMANCE FOR READ AND WRITE CYCLES

Memory write cycles affect the average access time of the cache system. In a write-through design, unbuffered write cycles are equivalent to cache misses, while buffered write cycles are equivalent to cache hits. Unbuffered write cycles take a main memory cycle to write data for every write. If the main memory write cycle time is the same as the read cycle time, this is equivalent to a cache miss. In buffered write, data is written into the cache and into a register for later off-line write into the memory. Thus, the write cycle in the buffered write case is equivalent to a cache cycle. Each write cycle in the buffered case is, therefore, equivalent to a cache hit. The performance equations for this case are:

$$Ps = R((1 - M)Pc + M) + W(Tw/Tm)$$

For unbuffered writes:

$$Ps = R((1 - M)Pc + M) + W$$

For buffered writes:

$$Ps = R((1 - M)Pc + M) + WPc$$

Where:

R = Fraction of total memory cycles that are read cycles
W = Fraction of total memory cycles that are write cycles
Tw = Write time = Tm for unbuffered, Tc for buffered writes

The effect of unbuffered write cycles is to limit the maximum performance of the cache system. For the average case where write cycles are approximately 15% of the total number of memory cycles, this is approximately equivalent to a cache memory performance of 0.15, as shown in Figure 11.

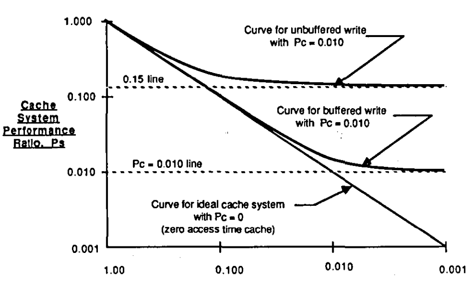


Figure 11: Cache Access Time vs Miss Rate for Buffered and Unbuffered Write Cycles

CACHE SYSTEM PERFORMANCE IN TERMS OF AVERAGE MEMORY ACCESS TIME

Although cache memory systems can be evaluated in terms of the dimensionless performance parameter, Ps, you often need to calculate the actual access time for a specific system. This is expressed by:

$$Ts = R((1 - M)\ Tcr + MTmr) + WTw$$

Where:

Ts = Cache average system cycle time, averaged over read and write
R = Percentage of memory cycles which are read cycles = 85% typical
W = Percentage of memory cycles which are write cycles = 15% typical
M = Miss rate of cache = 10+% typical
Tcr = Cache read cycle time
Tmr = Main memory read cycle time
Tw = Write cycle time: main memory for unbuffered write, cache for buffered

For typical values:

$$Ts = 0.85(0.9Tcr + 0.1\%mr) + 0.15Tw$$
$$= \underline{0.765Tcr + 0.085Tmr + 0.15Tw}$$

For unbuffered write and Tcr = 50ns, Tmr = Tw = 250ns:

$$Ts = 0.765(50) + 0.085(250) + 0.15(250) = \underline{97.0ns}$$

For buffered write and Tcr = Tw = 50ns, Tmr = 250ns:

$$Ts = 0.765(50) + 0.085(250) + 0.15(50) = \underline{67.0ns}$$

CACHE SYSTEM PERFORMANCE IN TERMS OF CPU WAIT STATES

In many computer and microprocessor systems, the purpose of the cache memory system is to eliminate CPU wait states, clock periods where the processor is stopped waiting for the memory. The cache performance calculations for this condition are more properly expressed in terms of processor wait states as follows:

$$Ncw = R((1 - M)\ Ncr + (1 - H)Nmr) + WNw$$
$$= RMNmr + WNw \quad \text{If: } Ncr = 0 \text{ (no wait states for cache)}$$

Where:

Ncw = CPU average number of wait states, averaged over read and write
R = Percentage of memory cycles which are read cycles = 85% typical
W = Percentage of memory cycles which are write cycles = 15% typical
M = Miss rate of cache = 10+% typical
Ncr = Cache read cycle time wait states (typically 0)
Nmr = Main memory read cycle wait states
Nw = Write cycle wait states: main memory wait states for unbuffered write, cache wait states for buffered

For unbuffered write and Ncr = 0 wait states, Nmr = 3 wait states:

Ncw = 0.085(3) 1m1 .15(3) = <u>0.535 wait states</u>

For buffered write and Ncr = Nw = 0 wait states, Nmr = 3 wait states:

Ncw = 0.085(3) + .15(0) = <u>0.255 wait states</u>

CACHE SYSTEM PERFORMANCE IN TERMS OF CPU THROUGHPUT

The reason for adding a cache to a CPU is to improve throughput by eliminating wait states. CPU throughput improvement, as a result of adding a cache, can be expressed as the ratio of the speeds before and after adding the cache. For our purposes, CPU throughput improvement can be equated to memory throughput improvement. CPU throughput for this case can be defined as the CPU clock frequency divided by the number of clock states per memory cycle. The speed improvement provided by the cache can therefore be expressed as the ratio of the throughput with the reduced number of wait states provided by the cache to the throughput with full wait states:

$$Fc = \frac{fclk/(No + Ncw)}{fclk/(No + Nm)}$$

$$= (No + Nm)/(No + Ncw)$$

Where:

fclk = Frequency of processor clock
N = Number of clock cycles per memory cycle
Ncw = Number of wait states for cache system (average)
Nm = Number of wait states for main memory
No = Number of processor states per memory cycle with no wait states
Fc = Processor throughput relative to throughput without cache

A 68010 microprocessor requires four clock states per memory cycle, i.e. No = 4. Assuming a 12.5MHz clock and 250ns main memory access time, Nm = 2 wait states. If we use the unbuffered write case from the clock state analysis above, Ncw = 0.535. The throughput improvement provided by the cache is therefore:

$$Fc = (4 + 2)/(4 + 0.535) = 6/4.535 = \underline{1.32 = 32\% \text{ throughput increase}}$$

This is equivalent to increasing the CPU clock speed from 12.5MHz to 16.5MHz.

CACHE MEMORY PERFORMANCE: HOW MUCH DO YOU NEED?

A simple, direct mapped cache memory system, as described above, is often the most cost effective design. In many cases, the effort to decrease the miss rate beyond that of a simple design may not be worth the increase in system performance.

For example, if Pc is greater than 0.20 corresponding to a cache access time greater than 20% of the main memory access time, it may not be cost effective to improve the hit rate above 90%. This is because there is a knee in the curve of performance improvement versus miss rate at the point where Pc = miss rate, as shown in Figure 10. In some cases, even the added expense of buffered write may not be justified. To examine the relationship between CPU throughput and miss rate, CPU thorughput improvement versus miss rate for various microprocessors is shown in Table 2.

Miss Rate	Throughput Relative to Uncached System			
	68010 Unbuffered	68010 Buffered	68020 Buffered	RISC Buffered
1.00	1.00	1.00	1.00	1.00
0.80	1.06	1.12	1.19	1.27
0.60	1.13	1.20	1.32	1.49
0.40	1.20	1.28	1.49	1.79
0.20	1.29	1.38	1.71	2.24
0.10	1.34	1.44	1.84	2.56
0.05	1.37	1.47	1.92	2.76
0.00	1.40	1.50	2.00	3.00

Table 2.

The data shown is for three CPU/cache systems. The 68010 microprocessor system has a 12.5MHz clock and a cache with unbuffered write. The 68020 system has a 16MHz clock and a buffered write cache. The RISC CPU assumes a 10MHz RISC computer with a 10MHz clock and a buffered write cache, and assumes one clock per memory cycle with wait states equal to an integral number of clock cycles.

Using the data in Table 2, we can make an interesting comparison between chip count and performance gained over an uncached system. Table 3 gives this comparison, showing the chip counts, miss ratios, and performance improvement gain for simple, depth expanded, and two-way set associative expanded caches. The chip counts given are for the cache tag and data RAM chips required, but do not include chip counts for the control logic. One RAM chip is added for the two-way set associative case for the least-recently-used cache flag RAM.

Tag RAM Size	68010 Unbuffered			68020 Buffered			RISC Buffered		
	Chips	Miss	Perf	Chips	Miss	Perf	Chips	Miss	Perf
8K	4	0.32	1.24	7	0.12	1.81	7	0.12	2.49
16K	8	0.22	1.28	14	0.09	1.86	14	0.09	2.60
8K+8K S.A.	9	0.17	1.31	15	0.07	1.89	15	0.07	2.68

Table 3.

Table 3 shows that the throughput improvement created by expanding the cache above a minimum chip count design is small. This table can be interpreted in two ways. In small systems where the goal is to achieve high-performance at minimum chip count, the table indicates that a mimum chip count cache is best since it buys the most performance improvement per chip; doubling the cache chip count purchased less than 10% further increase in performance in all cases. In larger systems where the goal is to achieve maximum performance at moderate chip count, the table indicates that a further increase in performance of 5–8% can be obtained by adding fewer than ten chips.

CACHE DESIGNS: DIFFERENT WAYS TO MAKE ONE

The cache memory described above is a direct mapped cache. It is a simple, commonly used design with respectable performance. Further investigation into the technology of cache memories will reveal a wealth of other approaches to cache design. Much of the variety comes from attempts to maximize the performance of relatively small cache memories typical of earlier technology. Fortunately, there exists some data to help sort out the relative value of the various approaches. This data is in the form of studies on cache memory performance as a function of cache size, organization, word width, etc., such as the excellent work done by Prof. Alan Jay Smith of the University of California at Berkeley (see references). These studies provide background and insight on how to achieve the highest performance out of cache memory systems, as well as documentation of a wide variety of cache schemes which do and do not work. The following comments are intended to provide a simplified guide to, and summary of, some of this data. The following comments are, in large part, judgments and opinions derived from the data in various reports and do not necessarily reflect the opinions of the original authors of the data.

WHAT WE HAVE LEARNED ABOUT CACHE MEMORY DESIGN

A simple, direct mapped cache as discussed above will give good performance if it is large enough. The ultimate measure of cache memory performance is its effect on system cycle time, which is a function of cache cycle time relative to main memory cycle time and the hit rate of the cache. Given a cache cycle time, miss rate becomes the measure of cache performance. Improving cache perfomrance, therefore, means improving the hit rate. However, a simple design with a moderate miss rate may be sufficient for many applications, giving most of the performance improvement that could be achieved by a more sophisticated design.

Much of the work that has been done on cache architecture and design was aimed at maximizing the performance of relatively small caches, consistent with the capabilities of earlier technologies. With today's technology, in the form of chips such as the IDT7174, we can easily make large cache memories at low chip counts that are at the upper limit of the earlier technologies. As a result, much of the sophistication required in smaller cache designs, in order to achieve an acceptable hit rate, is not required in today's large cache designs.

CACHE ARCHITECTURE: DIRECT MAPPED vs SET ASSOCIATIVE

A pure cache memory should be an associative memory, where the cache contains all of the most recently used data words. The direct mapped and set associative designs are approximations to this which sometimes exclude recently used words when there is more than one frequently used word per set. Fortunately, the difference between associative, set associative and direct mapped can be quantified. The ratios of miss rates for set associative and fully associative, relative to the direct mapped case, are shown in Table 3A. For example, if the miss rate for a direct mapped design is estimated at 0.20, the miss rate for a two-way set associative design of the same size would be (0.78)(0.20) = 0.156.

What this chart tells us is that two-way set associative caches have a significant performance improvement over simple direct mapped caches, but there is little additional improvement beyond four-way set associative designs. As was noted earlier, the set associative method can often be included in depth expanded cache designs where the two (or more) sets of cache hardware required for the expansion can be arranged to work in a set associative manner.

Cache Type	Ratio of Miss Rate to Direct Mapped
Direct Mapped	1.00
2-Way Set Assoc	0.78
4-Way Set Assoc	0.70
8-Way Set Assoc	0.67
Fully Associative	0.66

Table 3a.

CACHE SIZE

Cache sizes on commercial systems have tended to range from 16K to 64K bytes. Caches smaller than 16K can have significantly higher miss rates, while caches larger than 64K may not significantly improve the miss rate. This is shown above in Table 1. Much work has been done on the relationship between cache size and miss rate; however, most of this work is concerned with small caches, 32K bytes and under. The IDT7164/IDT7174 combination allows 16K byte cache memory design for 16-bit systems and a 32K-byte design for 32-bit systems using a minimum number of chips, and can be easily expanded to 64K and larger if desired.

WRITE THROUGH vs COPY BACK

There are two general approaches to handling the memory write problem: write through and copy back. In the write through approach, memory data is written into main memory as it is received from the CPU. In the copy back mode, memory data is written into the cache and flagged with a "dirty write" bit which indicates that the word has been written into the cache but not into the main memory. The cache data is copied into main memory as a separate operation at some later time, and the dirty write bit is cleared. There appears to be little performance difference between the write through and copy back approaches. Since the write through approach is simpler in concept and easier to implement, it is the most often used method.

WRITE BUFFERING

A significant performance increase can be achieved with a single level of write buffering. Complete write buffering requires more than one level of buffering to cover the case of two write cycles closer together than the main memory write cycle time. A FIFO can be used to buffer more than one word of write data; however, the FIFO need be no deeper than four words, since no further performance results from making it deeper.

SPLITTING THE CACHE: INSTRUCTION/DATA, SUPERVISOR/USER

Splitting the cache into two smaller caches, one for instructions and one for data, seems like it would improve the hit rate; however, it doesn't. In theory, the CPU spends most of its instruction cycles in a small part of the program. By caching these separately from the more random data memory, the hit rate on the instruction portion should be improved. Alas, the studies show that splitting the cache into two pieces typically does no better — and in some cases does a lot worse — than leaving the cache in one piece. This is, perhaps, because the miss rate for data is degraded by more than the hit rate for instructions is improved.

LINE SIZE: MAIN MEMORY WORD WIDTH vs CACHE WORD WIDTH

We have considered cache sizes where the CPU word width, memory word width and cache data word width are the same size. Performance improvement can result if the main memory and cache words are wider than the CPU word. If the cache word width (called the line size) is doubled the miss rate is cut almost in half. This is because the next word the CPU wants from memory is often the word adjacent to the one it just used. Increasing the line size by a factor of two will lower the miss rate by almost a factor of two up to line sizes of 16 bytes and beyond. This is shown in Table 4.

Cache Size in Bytes	Miss Ratio Reduction for Increasing Line Size			
	Line Size (Size of Block From Main Mem to Cache)			
	4 bytes	8 bytes	16 bytes	32 bytes
4K	1.00	0.586	0.364	0.262
8K	1.00	0.581	0.345	0.222
16K	1.00	0.569	0.330	0.203
32K	1.00	0.564	0.324	0.194

Table 4.

There are two approaches to increasing line size in order to reduce miss rate: by increasing the memory data bus width, and by fetching a block rather than a word of data from memory. Increasing the data bus width (from 16 to 32 bits, for example) may be practical in some systems where additional performance is desired.

The other alternative is to transfer a block of bytes to the cache instead of a single word. This becomes significant in systems where there is a delay before data transfer from main memory, but where several words can be transferred quickly after the initial delay. An example of this concept is the page mode in dynamic RAM designs. In such a system, there may be an initial latency of 200ns to begin a memory read cycle but, once started, the memory may be able to transfer words at 100ns per word for blocks of up to 256 words. In this case, a line (block) size of 2-4 words may be used to significantly reduce the miss rate with moderate increase in the main memory cycle time.

SUMMARY

Cache memories have been extensively used in large computer systems to improve performance. Cache tag RAM chips allow this technology to be adapted to the small-to-medium system design at reasonable cost. Simple, direct mapped cache designs with low chip counts can be used to achieve significant performance improvements. High-performance and low miss rates are possible with simple designs due to the high speed and relatively large cache sizes possible with high-speed CMOS technology.

REFERENCES

[Smith82] Alan Jay Smith, "Cache Memories," Computing Surveys, 14, 3, September 1982, pp. 473-530.

[Smith84] Alan Jay Smith, "CPU Cache Memories," April 1986. To appear in *Handbook for Computer Designers*, ed. Flynn and Rossman.

[Smith85] Alan Jay Smith, "Line (Block) Size Selection in CPU Cache Memories," June 1985. Available as UC Berkeley CS Report UCB/CSD 85/239.

[Smith86] Alan Jay Smith, "The Memory Architecture and the Cache and Memory Management Unit for the Fairchild CLIPPER™ Processor," April 1986. Available as UC Berkeley CS Report UCB/CSD 86/289.

[Smith86b] Alan Jay Smith, "Bibliography and Readings on CPU Cache Memories and Related Topics," 1986. from Computer Science Division, EECS Department, University of California, Berkeley, CA 94720.

CMOS BREATHES NEW LIFE INTO BIT-SLICE

APPLICATION NOTE AN-08

Integrated Device Technology, Inc.

By Michael J. Miller

INTRODUCTION

Today's high-performance systems are composed of multiple processors and controllers working together. Several decades ago, in all but the most sophisticated designs, there was one processor doing everything. Now, the descendants of these systems are more like multi-cell organisms where each cell is interacting with other cells and performing a specialized task. For example, a work station today is composed of a central processor (80286), a graphic/video controller, a communications controller for ETHERNET or token ring, a mathematics accelerator and a disk controller (Figure 1). Except for the main CPU, all of the other elements are dedicated controllers. When performance counts, microprogram designs today can provide controller solutions that operate at more than 15 MIPS, which is an order of magnitude over what a fixed instruction set processor can provide.

The requirement for many of today's system designs to provide the highest performance possible means there is a requirement for high-performance solutions such as microprogram architectures. The performance benefit, however, must always be traded off with the cost in terms of power consumed and number of parts in the design solution. The power and parts count for a solution provided by a given family of devices is directly related to the speed/power ratio of the technology used. For several years the speed/power performance advances in the bipolar bit-slice world have slowed to a mere crawl while other families have moved ahead. The new wave of very high-speed CMOS has entered the bit-slice world, thereby offering ever faster and denser functions.

At the current level of technology, the number of gates, or the speed at which the gates can run in bipolar ICs is limited by the heat dissipation capabilities of the package which houses the individual piece of silicon on which the gates are fabricated. If the speed/power product is lowered, more speed can be gained from the same number of gates in the package or more gates can be packaged inside the device at the same speed. Because high-speed CMOS has a speed/power product almost an order of magnitude better than bipoloar TTL-ECL internal, it is becoming the technology of choice for new bit-slice functions today. Many more gates, running at higher speeds than the conventional bipolar technologies, may be contained in inexpensive packages. This provides more freedom for new architectures running at higher performance levels. Therefore, very high-speed CMOS is here just in time to breath new life into bit-slice ICs.

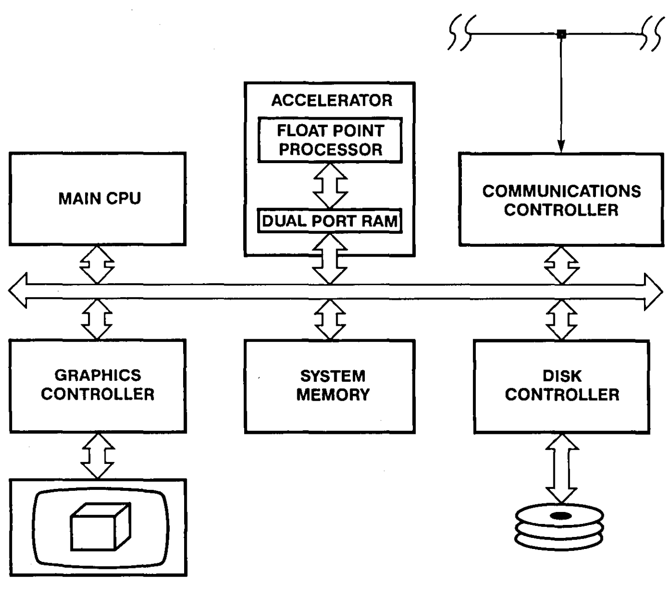


Figure 1: Work Station with Floating Point Math Accelerator

MICROSLICE is a trademark of Integrated Device Technology, Inc.

Printed in U.S.A.

11/86

COMPARISON OF MICROPROCESSOR ARCHITECTURES

In order to understand why microprogramming is still a very important architecture for today's designer, one must compare the fixed instruction set (8086, 68000) versus bit-slice microprocessor architectures. These two different approaches have their major strengths in different areas. The fixed instruction set processors have mainly filled the niche of lower parts count solutions and general purpose computation. In the controller area they have serviced the low-to-medium performance solutions. On the other hand, the microprogram bit-slice products have been utilized in very high-performance control applications and emulation of specialized computer architectures. To see why this is, one must inspect the architectures (shown in Figure 2) more closely.

The fixed instruction set processors, like the 68000, fall into a class of machines referred to as the Von Neumann-type architecture which has an address bus and a data bus linking together the processor and the memory. These two buses are sometimes referred to as the Von Neumann bottleneck. This is because all data and program instructions must pass through the address and data bus between the memory and processor. This limits the bandwidth because at any give time, only data or program instructions can be fetched or written. The performance is therefore directly related to the bandwidth of this data path. For example, in a 16MHz 68000 for one memory access, the clock must cycle three times, yielding 5 million data transfers in one second. To perform any instruction the processor must fetch the op code, source and destination designators, and the data. This can be anywhere from two memory cycles to many memory cycles and averages out around 3 to 5 memory cycles. At a bus cycle rate of 5MHz, this results in approximately 1 to 1.5 MIPS which is a theoretical number that exceeds actual benchmarks for the 68000. Through many years of optimizing the architecture and the instruction set, the fixed instruction microprocessors have become very good at performing general purpose-type computations. Because the instruction set is fixed and has been added to over the years, previous software written from these processors has been brought forward, creating a very rich base of application software to solve all sorts of applications such as operating sytems, compilers, editors, data base programs, etc. Use of high level languages has made this much easier.

The microprogram architecture can be thought of as a Harvard class architecture. This architecture allows instructions to be fetched at the same time that data is fetched, thus overlapping instruction fetch and decode along with data operations. The heart of the bit-slice architecture is found in the sequencer. The sole purpose of the sequencer is to generate a new address on every clock cycle. These addresses are fed into a programmed memory whose result is stored in an instruction register referred to as the pipeline register. The pipeline register and memory are very wide — anywhere from 32 bits to as large as 256 bits. The width of this register is tailored in each design in order to control a few or many operations in parallel, tuning the performance to the required application. The instruction register holds the instruction for the sequencer which is generating the next address. With a 20MHz signal clocking the sequencer, a new instruction can be fetched 20 million times per second. This sets an upper end performance level for the bit-slice architecture at 20 MIPS. This very high rate of instruction stream can be used to control such applications as disc controllers, high-speed graphics engines, dedicated DSP architectures for radar/sonar, imaging devices, communications, robotics and so on.

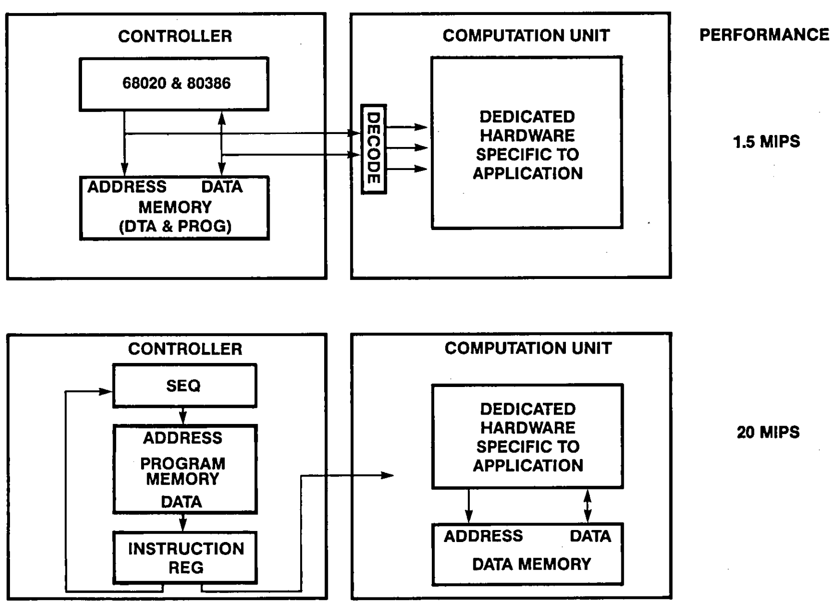


Figure 2: Comparison of Microprocessors as Controllers

14

The other half of the Harvard architecture is the portion which processes data (shown in Figure 2) as the computation. This section is typically composed of RAM, arithmetic logic units, multipliers and data conversion elements (for DSP applications). This portion of the architecture can have local memory which is used directly in the computation path, as well as larger more bulky memory. This architecture may be highly pipelined to get maximum performance or it may be very simple small architectures.

The 2900 family is a group of LSI/VLSI building blocks which provide such functions as sequencers, address generators and data path elements. Typically, devices like the 2910 are used for the sequencer and devices like the 2903 or 2901 are used for the ALUs and the data paths of microprogrammed-type machines. Because the microprogram devices are thought of more as building blocks, they therefore have the capability and flexibility to emulate many different types of structures, just as the NAND-gate is the ultimate in flexibility. For example, the 2901 is often used as a sophisticated, dedicated address generator which can perform PC relative operations, calculate pointers into complex data structures, etc. Because of the flexibility and instruction rate, the microprogram architecture is very suitable for high-performance controllers and the emulation of special purpose computer architectures not available as fixed instruction set machines.

NEW AND MORE POWERFUL BIT-SLICE DEVICES AS A RESULT OF CMOS

Because CMOS consumes an order of magnitude less power for the same speed as bipolar, many more gates may be packed into the same package and still have room to reduce the size of that package. This allows for ever increasing levels of integration. IDT has designed a new family of bit-slice devices which can execute the already-existing microcode of the AMD 2900 family, but at more than four times the integration level. This family is referred to as the IDT49C000 family, and the heart of it is made up of ALUs and sequencers. Three key devices in this family are the IDT49C410, the IDT49C402 and the IDT49C403. These parts characteristically have wider data paths, more internal paths, larger RAM and support much higher clock rates than their bipolar predecessors.

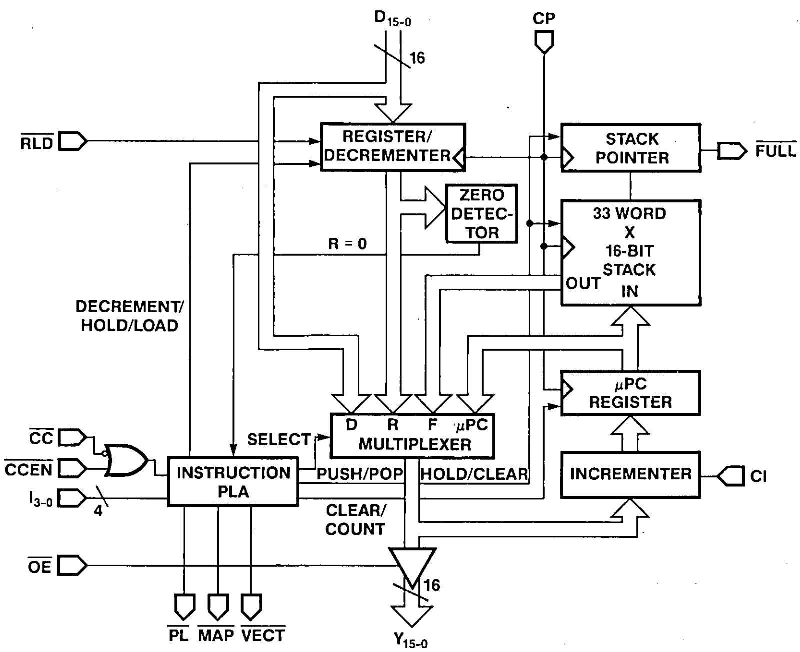


Figure 3: IDT49C410 16-Bit Microprogram Sequencer

The IDT49C410, shown in Figure 3, is architecture and function code compatible to the 2910A, with an extended 16-bit address path which allows for programs up to 64K words in length. It is a microprogram address sequencer intended for controlling the sequence of execution of microinstruction stored in microprogram memory. Besides the capability of sequential access, it provides conditional branching to any microinstruction within the 64K microword range. Unlike the 2910 which has a 9 deep stack, the IDT49C410 has a 33 deep stack which provides microsubroutine linkage and looping capability. This deep stack can be used for highy nested microcode applications, as well as microprogram loop control. At the center of the IDT49C410 is a multiplexer which selects the address for the next instruction to be executed. During each microinstruction, the microprogram controller provides a 16-bit address from one of four sources: 1) the microprogram address register (µPC) which usually contains an address one greater than the previous address; 2) an external direct input used for branching; 3) a register counter (R) which is used to retain data loaded during a previous microinstruction; or 4) the return stack which is a last-in first-out organization (F).

In a typical application, the worst-case performance path for the sequencer is from a pipeline register through the condition code mux and on into the instruction decoder of the sequencer which selects the next address. The address then passes through into the microprogram memory which must set up the next instruction into the pipeline register. Using the highest performance devices, this consists of a 6.5ns clocked Q pipeline register (IDT74FCT374A), 12ns condition code MUX (IDT74FCT153), 13ns through the sequencer (IDT49C410A), 15ns access time for 16Kx1 static RAM (IDT6168A) and 3ns set up to the pipeline register (IDT74FCT374A), thus yielding a 49.5ns cycle time. The 20 MIPS operation is twice as fast as what was realistically achievable (10 MIPS) using the 2900 family's corresponding support devices. This will allow designers to achieve performance levels never dreamed of before. Because of the enhanced CEMOS™ technology used to fabricate this device, the IDT49C410 draws no more than 80 milliamps commerical in the worst-case system configuration which is approximately 1/5 the power of its 12-bit predecessor, the 2910A, which is 344 milliamps.

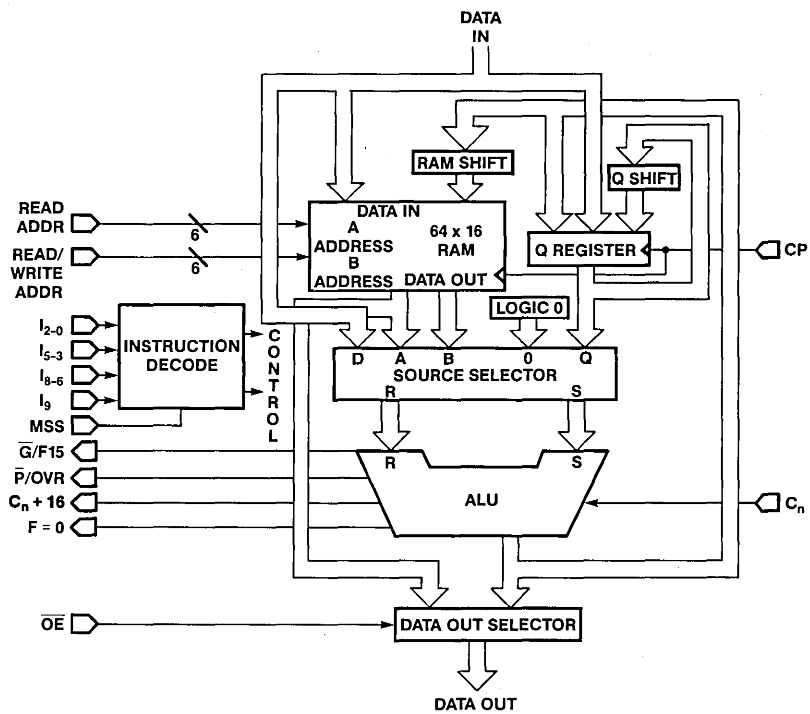


Figure 4: IDT49C402 — 16-Bit CMOS Microprocessor Slice (Quad 2901 Plus Extra Destination Functions)

The IDT49C402, shown in Figure 4, is a very high-speed, fully cascadeable, 16-bit CMOS microprocessor slice unit which combines the standard functions of four 2901s and a 2902 with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

The IDT49C402 includes all the normal functions associated with the standard 2901 bit-slice operation: 1) a 3-bit instruction field composed of I_0,I_1,I_2 which controls the source operand selection of the ALU: 2) a 3-bit microinstruction field composed of I_3,I_4,I_5 used to control the 8 possible functions of the ALU; 3) 8 destination control function lines which are selected by the microcode inputs I_6,I_7,I_8; and 4) a tenth microinstruction input, I_9, offering 8 additional destination control functions. This I_9 input, which is above and beyond the standard 2901 instruction lines, is used in conjunction with I_6,I_7,I_8 and allows for shifting the Q register up and down, loading the RAM or Q registers directly from the D inputs *without* going through the ALU, and new combinations of destination functions with RAM A-port output available at the Y output pins of the device. The new ability to load the RAM or the Q register directly for the D inputs without having to pass through the ALU means that new operands may be brought into the register file in parallel with ALU operations in critical sections of algorithms. Where the architecture used to take two cycles to load and operate, it now can be done in one cycle, providing twice the performance in critical portions of the code.

Also featured in the IDT49C402 is an on-chip dual-port RAM that contains 64 words by 16 bits. This is four times the number of working registers in the 2901. Because the on-board register file in the 2901 architecture is not readily cascadeable, the large memory is a significant advantage to the designer. The register file can be thought of as a high-speed cache on-board the device. The more room that is available to the programmer, the higher the hit ratio is for desired data.

The 64 on-board registers in the IDT49C402 can be alternately used in a bank selected architecture to yield four sets of 16 working registers. Each bank can then be set aside for one of four

14

microprogram tasks, thus making it easy to write multi-tasking microcode where any one of four tasks can be executed in each clock cycle. This means that the time to switch between tasks is one clock cycle for the ALU section of the circuitry. This can be very important in highly interrupt-driven controller-type architectures. For fixed instruction set processors (like the 68020 or 80386), a context switch requires the execution of multiple instructions.

The critical path through the IDT49C402 on most applications is the A and B addresses and instruction to the data output. This path in the IDT49C402A is 37ns commerical. In a typical application this means that, if the addresses come from the pipeline register which has a clocked Q of 10ns and the data output of the IDT49C402A goes into another register with a set-up of 3ns, the full cycle time of that portion of the circuitry is 50ns, thus yielding an operation of 20 MIPS. This can be compared with four 2901Cs (bipolar competitor) which require a system cycle time of 80ns, resulting in a maximum rate of 12 MIPS.

While the 2901/49C402 architecture can be thought of as a 2-bus architecture with 1 bus into the ALU and 1 bus out of the ALU, the 2903/203/49C403 is thought of as a 3-bus architecture. The IDT49C403 is a high-speed, fully cascadeable, 16-bit CMOS microprocessor slice unit which combines the standard functions of four 2903s and a 2902 — with additional control features aimed at enhancing the performance of classic bit-slice microprocessor designs.

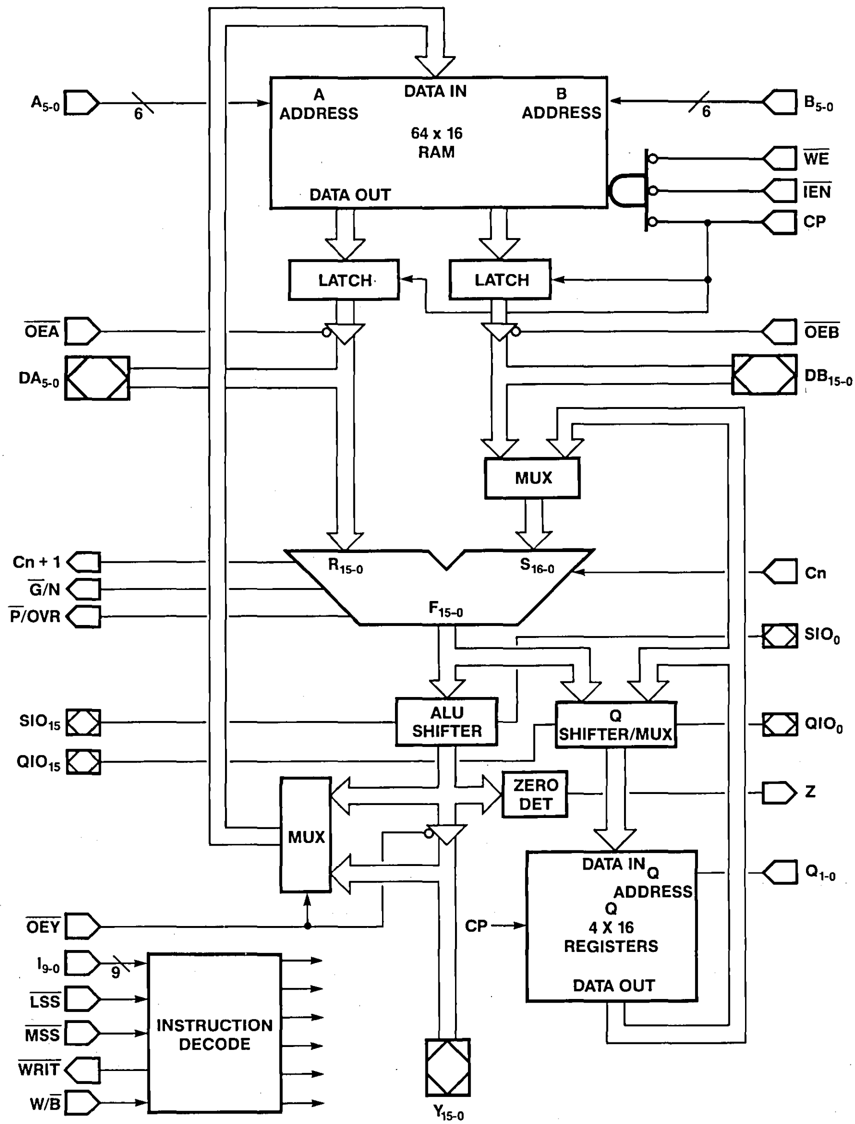


Figure 5: IDT49C403 16-Bit CMOS Microprocessor Slice (Quad 2903/203 Plus Expanded RAM)

Included in the extremely low-powered yet fast IDT49C403 device (shown in Figure 5) are three bi-directional data buses, 64 word x 16-bit dual-port expandable RAM, 4 word x 16-bit Q register, parity generation,sign extension, multiplication, division and normalization logic. Additionally, the IDT49C403 offers the special feature of enhanced byte support through both word/byte control and byte swap control. The IDT49C403A will support cycle times as fast as 65ns and will enhance the speed of all existing quad 2903A and 29203 systems by 40%. Being specified at an extremely low 185 milliamp maximum commercial power consumption, the IDT device offers an immediate system power savings and improved reliability over the existing designs. This device is packaged in either 108-pin PGA or a 144-pin leaded chip carrier.

The functional block diagram of the IDT49C403 shows that not only has the data path been widened to 16 bits, but the RAM and the Q registers are four times as deep. Thus, the IDT49C403 has been expanded in depth as well as in width, giving a two-fold improvement in performance. Not only can the expanded RAM and Q registers be used to provide more room for caching intermediate operands, they can also be thought of in bank-selected architectures as providing room for a least four tasks in a multi-task environment. Therefore, in a highly interrupt-driven application, the overhead to switch between one task and the next is zero.

Because the width of the IDT49C403 is 16 bits, a control line called $W/\overline{B}$ is provided to switch the IDT49C403 between working on 8 bits or 16 bits. When in the byte mode, the RAM location being written into has only the lower 8 bits enabled, leaving the upper 8 bits intact. All of the status flags coming out of the IDT49C403 come from the intermediate boundary between the 8th and the 9th bit of the ALU, all of which makes it convenient for the designer to operate on 8 bits at a time. The word/byte control, taken in conjunction with the instruction enable, allows the designer to cascade the IDT49C403 into larger words such as 32 bits or 64 bits by controlling each of the instruction enables and the word/byte line on the least significant device operand links of 8, 16, 32, and 64 bits. The additional instruction added to the instruction set with an IDT49C403 can be used to swap upper and lower bytes inside each IDT49C403 device.

CONSERVATION OF MICROCODE

IDT provides a solution that minimizes the total redesign cost of transition from bipolar technologies to CMOS technologies. This is achieved by having a series of parts designed in CMOS taking advantage of the VLSI capabilities yet utilizing the same instruction set as devices in the 2900 family. Each of the three devices mentioned above is capable of executing microcode previously written for their bipolar counterparts.

In the case of the IDT49C410 sequencer, the old microcode may be run with no alterations. For the two ALUs, the IDT49C402 and IDT49C403, compatibility can be handled at several levels. The simplest solution is to connect only the instruction lines which correspond to the 2901 or the 2903/203, respectively, and tie the remaining inputs to their respective default levels. In this way, the design can execute the previously assembled microcodes.

If the design requires the designer to take advantage of some of the new features in the ALU such as deeper register files or new data paths, microcode must be modified to control the additional instruction lines. This can be achieved by modifying the assembler and reassembling the old microcode.

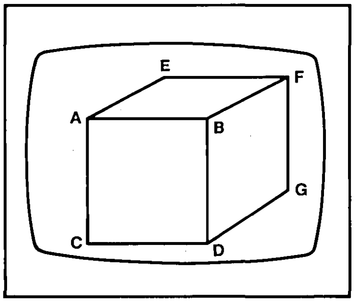
Because each microprogram design is different, the microprogram control word is different. This requires that microprogram assemblers have the ability to define mnemonics and relationships to define microprogram instructions and then assemble the user's microprogram written in the design's unique instructions. When upgrading from four 2901s to one IDT49C402, for example, the designer can add new mnemonics for the new operations to the definition phase of the microprogram assembler. At this point, consideration for the additional instruction input lines are made by simply widening the subfields. After the definitions have been modified, the older microcode can be reassembled along with new code using the new operations.

GRAPHICS ACCELERATOR EXAMPLE

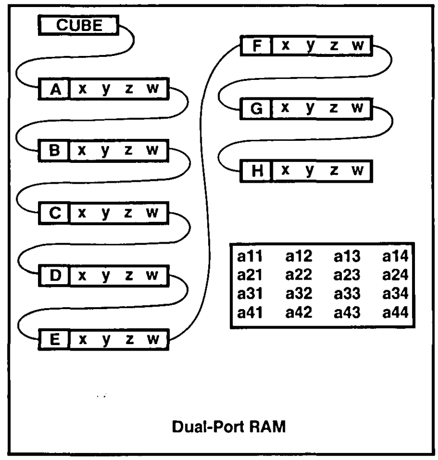
Today's high-end work stations use a processor like the 68020 or 8386 as the main CPU. Often augmenting the processing capability of the main CPU is a floating point math accelerator. While in some cases the floating point units are connected to the main CPU as a co-processor, in other cases the floating point is a separate processor itself. If the floating point processor is isolated from the main CPU through the use of a dual-port, higher overall system performance can be achieved because the accelerator can process in parallel to the main CPU.

In a graphics-type application, it is conceivable that the dual-port could contain a link list of data elements containing three dimensional point values and transformation instructions which are composed of 4 x 4 matrix. The floating point processor then could have the capability of traversing the link list and multiplying each point with the transformation matrice. This scenario could be used not only to rotate three dimensional objects, but also transformation of three dimensional objects onto two dimensional surfaces and performing clipping algorithms for final display on the video graphics terminal. Figure 6 shows how a cube might appear to a viewer of the work station and how it might be represented internally in memory.

The floating point accelerator can be broken into three main functional blocks: dual-port RAM, controller and floating point ALU, and multiplier. A block of dual-port RAMs is used as the interface between the global system bus and a local system bus used by the floating point processor. The control section generates sequences of instructions for a floating point ALU as well as the address generator indexing into the dual-port. The performance of the floating point accelerator is determined by how fast the controller can generate instructions for the ALU and the data band width of the ALU.



The User's View



The Processor's View

Figure 6

There are various floating point ALU devices on the market today. These devices can be grouped by the number of data buses used to get data in and out of them and the number of operations that can be performed at any given time (pipelining stages). The 1164/65 from Weitek each have one data bus in and out. These devices are meant to be connected to a common data bus which eventually is tied to the data bus of a fixed instruction set processor.

The 1264/65 floating point devices from Weitek and the IDT721264/1265 pin compatible CMOS versions have two data buses in and one data bus out, thus supporting the three bus-type architecture. Unlike the 1164/65, these devices can be operating on various pieces of data in several stages of completion through the use of pipeline registers, thus having a higher throughput. Both the IDT721264 and IDT721265 have a clock rate of 20MHz. The three data buses and pipelining makes the 1264/65 a very good match for high-performance bit-slice solutions.

The following is a discussion and comparison between two different types of solutions: the first being a fixed instruction set processor controlling the 1164/65 and the second solution being a 1264/65 controlled by bit-slice. The detailed description of the 1164/65 and 1264/65 are beyond the scope of this article, but Figures 8 and 10 show timing sequences of parameters, instructions and results.

FIXED INSTRUCTION PROCESSOR

As with any design problem, there are various solutions which present trade-offs in parts count and performance. The fixed instruction set processors provide solutions that are typically the lowest parts count but, when applied to dedicated control applications, do not provide the highest performance. The Intel 80386 is an example of a fixed instruction set processor that is popular as a general purpose CPU. Figure 7 shows a block diagram of how it would be used to control the 1164/65. While one approach could use a co-processor, the Weitek 1164/65 provides a higher performance solution.

In keeping with the possible structure for the floating point accelerator previously discussed, the 80386 serves the purpose of controlling the overall operation of the accelerator, shown in Figure 7. It serves the purpose of fetching data from the dual-port RAM. Through address decode circuitry and bus transceivers, the 386 sends commands as well as data to the ALU. The instructions are encoded as addresses in the 386's memory map where each address corresponds to a unique instruction for the 1164/65. While the address map is a clever concept, and probably the most efficient implementation, the decode and bus transceiver circuitry numbers more than a dozen parts.

To understand the performance, bus cycles must be counted and multiplied times the clock frequency. To perform one floating point operation, data must be fetched from the dual-port into the 80386 registers and then written out to the floating point chip. At this point, the floating point chips must be clocked multiple times to accomplish the desired operation. Finally, the 80386 must read the results into its register file where it might be saved as a temporary value or moved back to the dual-port.

The memory-to-register move instruction of the 386 requires four clock cycles. The register-to-memory move instruction requires two clock cycles. Therefore, to read data from the dual-port RAM into the floating point ALU requires six clock cycles. Instructions are passed from the 386 to the 1164/65 via the address bus. Each time the memory map is written to or read from, a clock is generated to the 1164/65. After placing the two operands in the floating point ALU, they must be clocked five times (shown in Figure 8), thus using ten clock cycles. Finally, to get data out of the floating point ALU, a memory-to-register move must be performed using four clock cycles. Therefore, to perform a floating point single precision floating point operation, 38 clock cycles must be utilized. In order to perform a three dimensional transformation requiring that a vector be multiplied by a matrix of 4 x 4 elements, 1,064 clock cycles must be utilized. At a clock rate of 16MHz, this means that a transformation can be done every 66 microseconds. This does not include the instructions to manage the linked lists and housekeeping.

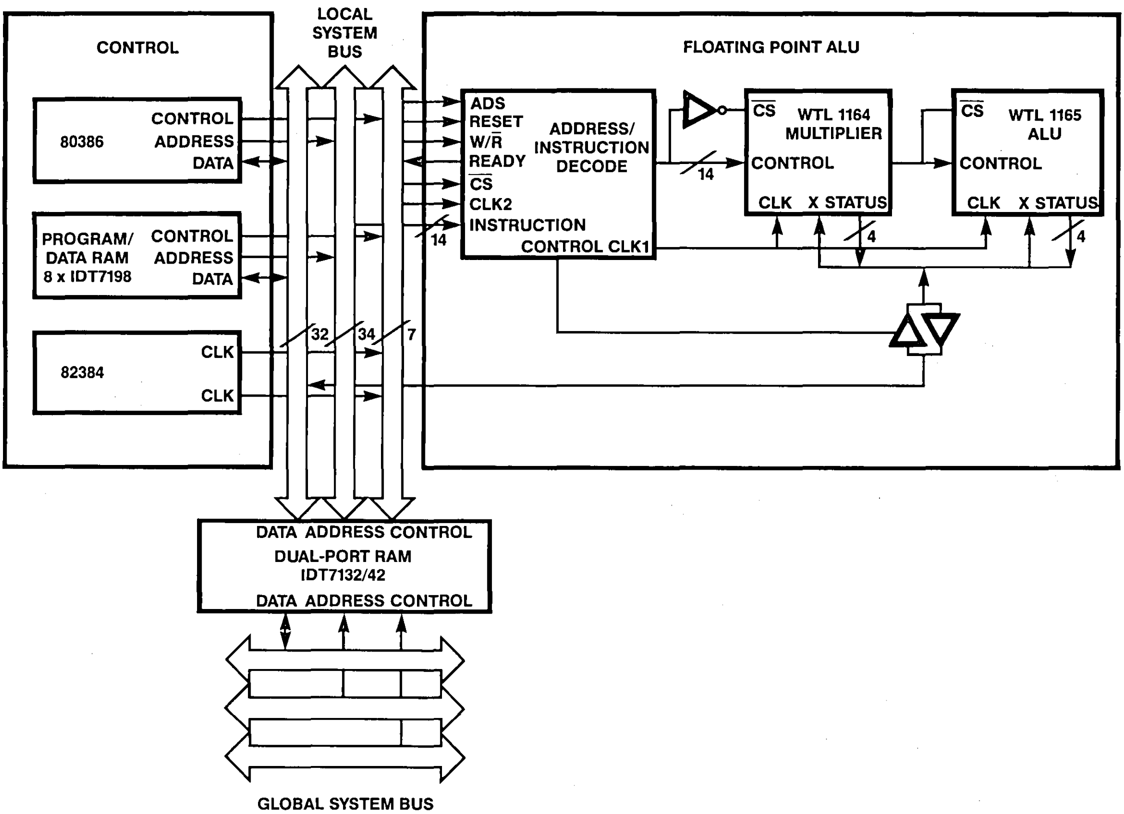


Figure 7: Floating Point Accelerator Using Fixed Instruction Set Processor

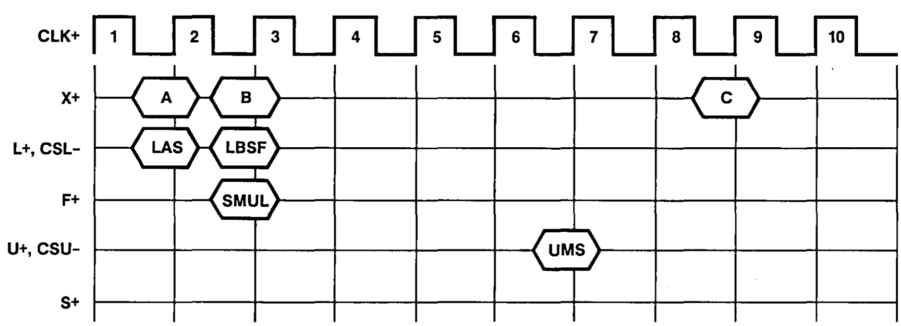


Figure 8: Single Precision Multiply for WTL1164

14

The need was recognized for a higher performance solution utilizing a processor like a 386. A product from Weitek, the 1163, replaces the address and instruction decode in the block diagram. The 1163 is a small sequencer and RAM which takes instructions from the 386's address bus and translates them into a series of instructions to the 1165 and 1165, thus reducing a floating point operation to 13 cycles. This results in a floating point transformation being done in 256 cycles which, with 16MHz clock, yields a transformation every 15.5 microseconds — a 5 fold improvement.

MICROSLICE™ SOLUTION

While a six fold increase in performance can be achieved using a special purpose sequencer like the 1163, by using general purpose sequencers (like the IDT49C410), another order of magnitude in improvement can be achieved. This improvement in performance is the direct result of three major characteristics of microprogram solutions. The first characteristic is that on every clock cycle a new instruction is fetched and executed, producing a sequence of very rapid fire instructions. The width of these instructions is chosen at design time to maximize the controllability of multiple devices. Therefore, the second characteristic of microprogram solutions is that multiple devices can be controlled in parallel. The third advantage of microprogram solutions is that multiple buses can be utilized and controlled in parallel, thereby allowing the designer to tailor the performance of the design to match the requirements of the application.

The MICROSLICE™ family is very well suited for controlling such devices as the floating point ALU or multiplier, like the IDT721264/1265, both of which are pin and functionally compatible with the 1264 and 1265. The control section of the floating point accelerator (shown in Figure 9) can be composed of the IDT49C410 which generates addresses to the writeable control store of the IDT71681. This, in turn, produces an instruction which is held in a pipeline register. The pipeline register is the current instruction being executed. From this register, control lines fan out to all instruction lines and control inputs of every device in the accelerator subsystem.

IDT49C402 AS AN ADDRESS GENERATOR

While most designers would think of the IDT49C402 and its class of devices only as ALUs with register files for data paths, it can be used for a larger variety of tasks. In the accelerator applications, it is used as an address generator. The data for a

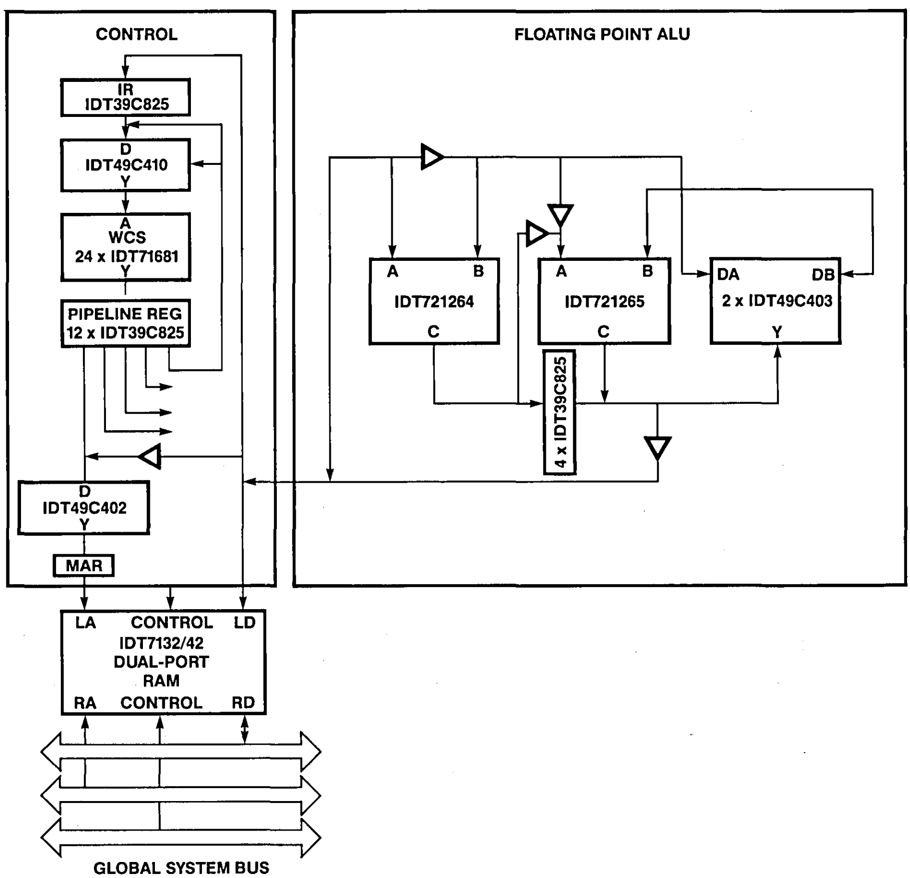


Figure 9: Floating Point Accelerator Using MICROSLICE™ Approach

4 x 4 matrice can be stored in the dual-port memory as a sequential list of 16 values. Any element can be located by adding together the address pointer to the start of the matrix, the row offset and the column offset. To perform a matrix multiplicaton with a vector, a column of values out of the matrix is individually multipled with the corresponding values in the vector and then the four products are summed. One way of efficiently generating the addresses using the IDT49C402, is to have the address pointer to the matrix and vector stored in the register file. To start, the address pointer of the matrix could be summed with a constant corresponding to the column to be operated on. This operation can be accomplished in one cycle by bringing the constant in through the "D" bus from the pipeline register, addressing the pointer with the A address and storing the result at a location specified by the B address. In the same cycle the new address could be output from the ALU through the Y port and placed in the MAR register. In this way, the MAR register would supply the dual-port RAM address on the next cycle,thus forming a pipeline mode of operation. On the next three cycles, the new address stored in the register file could be incremented and the respective calculated addresses passed on to the MAR. Therefore, in four cycles four addresses can be generated in rapid fire that correspond to four values in the column of the matrix. All of this function can be independent of, and working in parallel with, what is happening in the computation unit. With proper orchestration, address can be fed into the dual-port RAM and values read out in succession into the computation unit on every cycle. The minimum time from register file address to the Y output is 37ns, which is one of the fastest ways to generate complex 16-bit address.

Just as the IDT49C402 can be used to compute offsets into matrices, it can also be used to keep track of linked lists of complex data structures. The register file could be used to retain pointers of various lists, as well as intermediate pointers. In the accelerator described earlier, there are several required pointers: one pointer to the head of a list of XYZW points, an intermediate pointer to the current XYZW and a pointer to the transformation matrix.

HIGH-PERFORMANCE COMPUTATION

The computation portion of the accelerator is composed of the floating point devices and some local storage. The most efficient approach for multiplying a series of vectors with a transformation matrix is to start out by fetching the matrix from the dual-port RAM into local memory connected to the floating point chips. For this purpose, two IDT49C403s are incorporated as a 32-bit register file and ALU. Since the IDT49C403 has 64 registers, there is plenty of room to store the 4 x 4 matrix and still be able to accommodate temporary variables. The 32-bit ALU portion of the IDT49C403s can then be conveniently used to perform fixed point arithmetic and logic functions.

The IDT49C403 is a three bus architecture which allows for both of the output ports of register file to come off-chip and drive inputs into the floating point devices. In this way, two operands can come from the IDT49C403s and one from the dual-port addressed by the IDT49C402 each clock cycle. The results of the floating point multiplier or ALU can be stored back into the register file using the Y bus.

Once the transformation matrix is stored in the IDT49C403 registers, consecutive XYZW point values can be brought from the dual-port. In this way, a value from the XYZW vector and transformation matrix can be fed to the multiplier (IDT721265) on every cycle, thus keeping the multiplier constantly busy.

The multiply of a column with a vector is a sum of four products. The multiply of an XYZW vector with a 4 x 4 matrix is, therefore, 4 sums of products. Because it takes 8 clock cycles to perform the multiply and 12 clock cycles (shown in Figure 10) for the add operation (IDT721264), it is impractical to contemplate doing one sum of product in sequential cycles if the goal is to feed the multiplier and ALU on every cycle. To this end, the algorithm (pictured in Figure 11) works on all four sums of products in parallel.

To implement the parallel scheme the X,Y,Z and W must be multiplied in succession with each row of values in the matrix. When the four products of X with the first row of the matrix come out of the multiplier (a11, a12, a13, a14), they must be temporarily stored in the IDT49C403s until the four products of Y with the second row (a21, a22, a23, a24) start to come out. When the result of the first product of Y comes out (Y • a21), it can be immediately fed into the floating point ALU (IDT721265) with the first product of X (X • a11) which is stored in the register file of the IDT49C403s. As the results of the sum of X and Y vectors come out, they must be stored until the corresponding sums come out of the Z and W vectors. When the corresponding sums are available, the final sum of all four vectors may be computed.

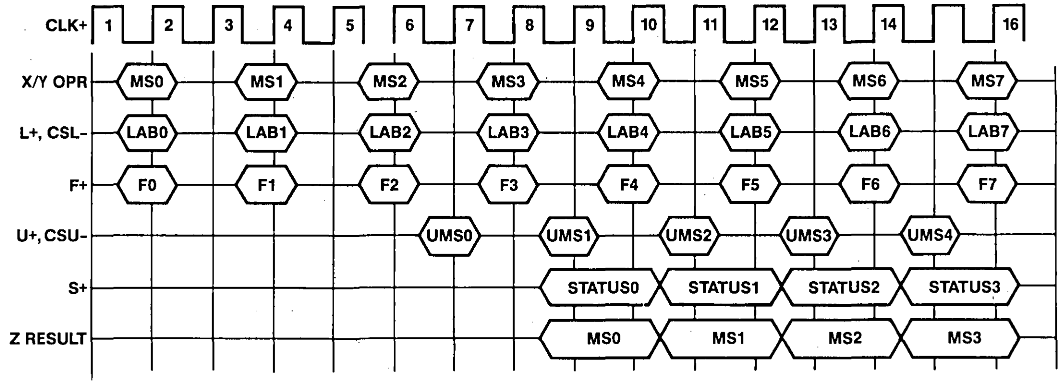
Figure 12 shows how the parallel algorithm can be implemented while taking into account pipelining of the floating point devices. The block is a graph which represents time as clock cycles on the horizontal axis and pipeline stages on the vertical axis. The input values start at the top and flow down to the bottom of the chart. Intermediate values out of the multiplier and the ALU are stored in the IDT49C403 and are reinserted into the floating point ALU in the middle of overall pipeline.

Since this is a pipelined parallel architecture, a new matrix multiply can be started every 32 clock cycles. This results in a matrix multiply every 2 microseconds, given a 16MHz system clock which is more than a 33 fold increase in performance over the 386 solution. One of the tradeoffs is that there is a 40 clock cycle latency to complete the matrix multiply after the last values are put into the top of the pipeline. This is not a technical problem because the dual-port memory can contain a complete list of XYZW vectors and be processing them in sequence.

FIXED INSTRUCTION SET VERSUS MICROSLICE

As can be seen, different solutions to the same application can result in a broad range of performances of much more than an order of magnitude, 1 to 33. The larger increase in performance must be viewed from the perspective of the tradeoff in hardware. On the level of VLSI devices, the control section of the 80386 solution uses one device, whereas the MICROSLICE solution uses two devices: the IDT49C410 for overall control and the IDT49C402 for operand address generation. The computation section maintains the one-to-two ratio with two devices for the 80386 solution (the 1164 and 1165) as opposed to the bit-slice solution which uses four devices (the IDT721264, IDT721265 and two IDT49C403s). In 1985, the disparity in the parts count of these areas would have been much greater because only 4-bit ALU slices were available, making the count for the control section 5 devices and the computation 6 devices.

The two areas where these solutions differ the most is in the control word formation for the floating point chip and the number of buses. For the 80386 solution, control signals are derived from the execution of a program stored in a 32-bit cycle wide memory which generates a succession of addresses which in turn are decoded into control words for the 1164/65. The decode logic is



Pipelined Single Precision Multiply for IDT721264

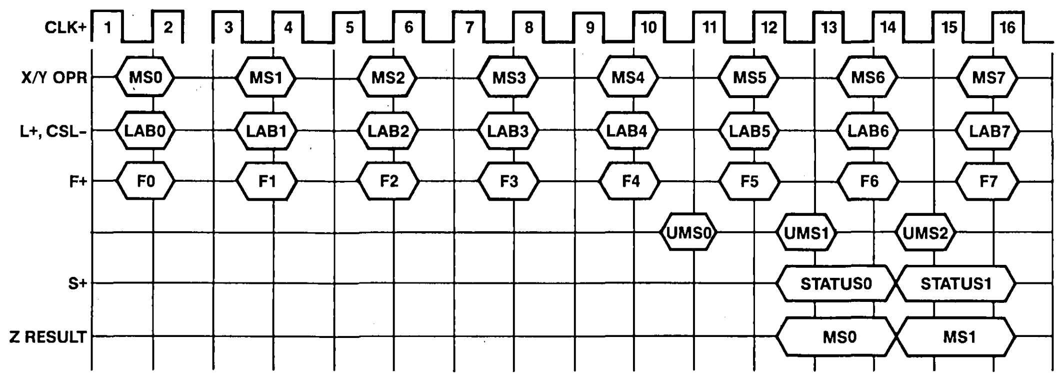


FIGURE 10: Pipelined Single Precision Add for IDT721265

$$\begin{bmatrix} a11 & a12 & a13 & a14 \\ a21 & a22 & a23 & a24 \\ a31 & a32 & a33 & a34 \\ a41 & a42 & a43 & a44 \end{bmatrix} \times \begin{bmatrix} XYZW \end{bmatrix} = \begin{array}{l} X' = X \cdot a11 + Y \cdot a21 + Z \cdot a31 + W \cdot a41 \\ Y' = X \cdot a12 + Y \cdot a22 + Z \cdot a32 + W \cdot a42 \\ Z' = X \cdot a13 + Y \cdot a23 + Z \cdot a33 + W \cdot a43 \\ W' = X \cdot a14 + Y \cdot a24 + Z \cdot a34 + W \cdot a44 \end{array}$$

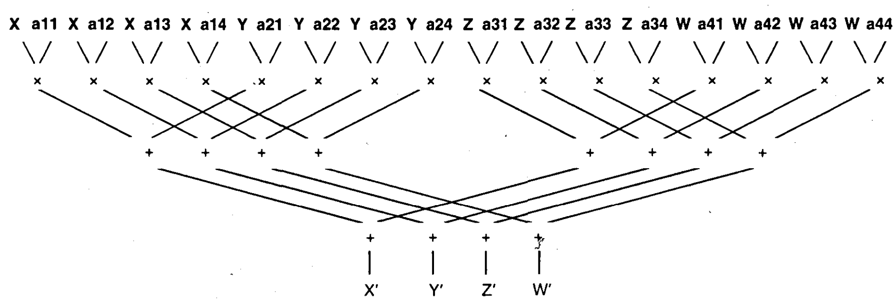


Figure 11: Mathematics of Matrix Multiply with Rearranged Order of Scalar Multiplies and Summations

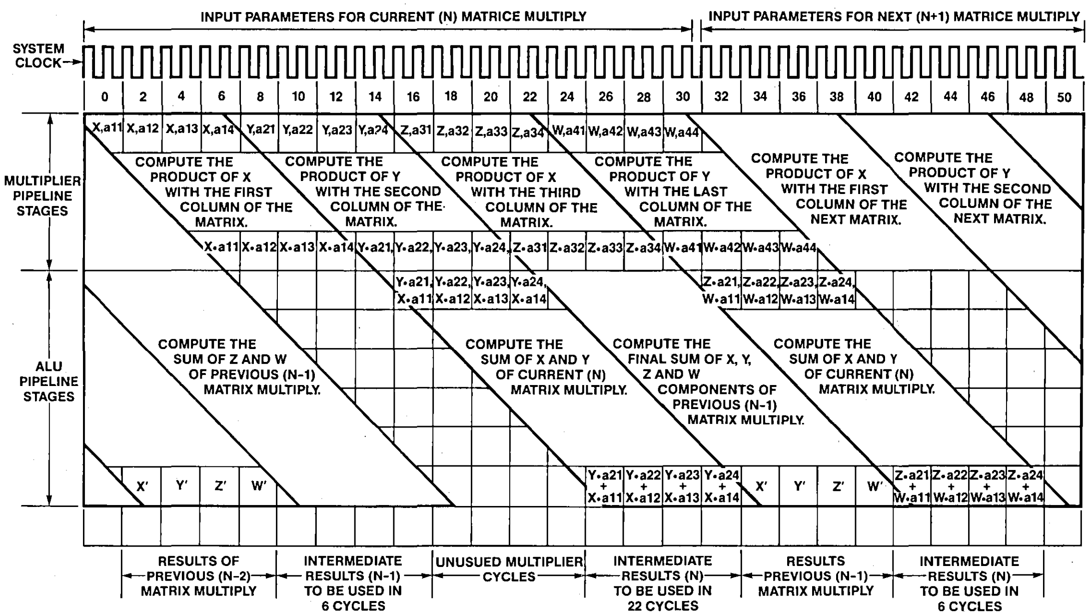


Figure 12: Pipeline of Matrix Multiply Using IDT721264/1DT721265

approximately a dozen devices which includes address buffers, address decode, transfer acknowledge, etc. The microprogram solution generates the control signals directly from a program memory of 16 bits wide which is stored in an instruction register called the pipeline register (12 IDT39C825A octal registers).

The area which has the largest variation in parts count is the bus structure. The 80386 has one address bus which it uses for control and one data bus which ties together the 80386, program RAM, dual-port RAM and the computation unit. There is one set of four bus transceivers required to isolate the floating point chips from the local data bus.

In contrast, the microprogram solution has numerous short buses which require interconnecting. One data bus comes from the dual-port RAM which ties together the control section as well as providing parameters to the computation section. The computation section, however, has four short buses which require four sets of four bus buffers (16 octal buffers) plus four octal registers for storing an intermediate value. The table in Figure 13 shows a summary of the performance and parts count of the two solutions. The total at the bottom is a sum of the sections compared. While it is not a total parts count, the ratio will be representative of the relation between the two solutions.

CONCLUSION

It can be concluded on a comparison basis that the MICROSLICE solution provides 33 times the performance of a fixed instruction set procressor like the 80386 for about 2 to 3 times the parts count. The advantage of the 80386 solution is that it utilizes single 32 address and data buses with one 32-bit wide memory, but has the disadvantage of requiring many clock cycles to perform a control operation. The advantage of the MICROSLICE solution is that it can control multiple devices in parallel at the cost of wider control memory and multiple bus interface parts. The speed/power product provided by very high-speed CMOS today offers the designer bit-slice tools for designing control structures and computation units which are on a comparable level of integration with fixed instruction set processors, but can offer significantly more than an order of magnitude in performance.

	Solution	80386	MICROSLICE
	Number of Floating Point Matrix Multiplies Per Second	15K	500K
PARTS COUNT	VLSI	3	6
	In Control	-12	12
	Memory	8 (32-Bits)	24 (96)
	(Width)		
	In Bus Interfact	4	20
	Total Compared Sections	27	62

Figure 13: Comparison of Different Solutions

14

Integrated Device Technology, Inc.

DUAL-PORT RAMs YIELD BIT SLICE DESIGNS WITHOUT MICROCODE

APPLICATION NOTE AN-09

By DAVID C. WYLAND

ABSTRACT

High-performance controller designs use bit-slice components for their speed and design flexibility. Speeds of 10-20 million instructions per second (MIPS) are common and the designer can use bit-slice design flexibility to perform speed-critical operations in one instruction. Bit-slice designs have the drawback, however, of requiring microcode design for their implementation, often with a long development cycle. The problem is that the microcode resides in a separate, stand-alone control memory which prevents use of the kind of interactive prototyping and debugging tools associated with conventional microprocessors. The problem can be eliminated by using a dual-port RAM for the control memory, making it part of the data memory address space, and converting the controller to a CPU by borrowing some techniques from Reduced Instruction Set Computer (RISC) designs. The result is a RISC controller where the microinstructions of the bit-slice approach become the instructions of a computer. The design approach provides all the speed and architectural flexibility of microcoded bit-slice designs, while allowing the use of interactive debugging methods associated with microprocssors.

BIT-SLICE VERSUS RISC ARCHITECTURES

An example of a typical bit-slice controller design is shown in Figure 1. It consists of a control flow section and a data flow section. The control flow section has a microinstruction counter and the control memory. The data flow section has a register and ALU element—the bit-slice—plus a data memory and I/O registers on a data bus. Note that the control and data memories are separate. The use of separate data and instruction memories is called the Harvard architecture. The separate control memory provides some of the speed associated with bit-slice designs because it operates in parallel with the data memory. This allows the next microinstruction to be fetched from the control memory, while data for the current instruction may be read from the data memory. This contrasts with conventional microprocessors which alternately get instructions and data from the same memory. This use of a single memory for instructions and data is called the Von Neumann architecture.

There is a remarkable similarity between the block diagram in Figure 1 and the block diagrams of RISC computers, as can be noted by comparing the block diagram in Figure 1 with the block diagram of a RISC CPU shown in Figure 2. The difference is that the control memory and the data memory of the controller have been replaced by an instruction cache memory and a data cache memory in the RISC CPU. The instruction and data cache memories work the same as their microcode counterparts except that they both contain copies of data in the common main memory. The programmer sees a single memory—the main memory—while the hardware works as if it has two independent memories. In this manner, the RISC computer has the speed advantage of the Harvard architecture and the single memory for programs and data of the Von Neumann architecture.

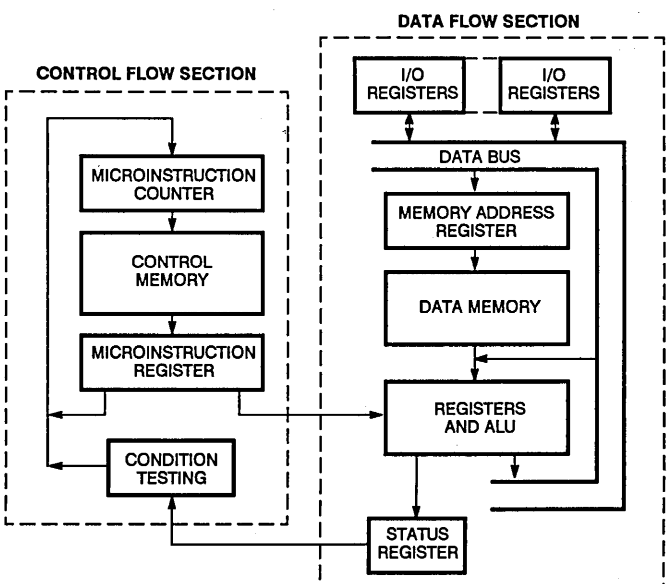


Figure 1. Bit-Slice Controller Block Diagram

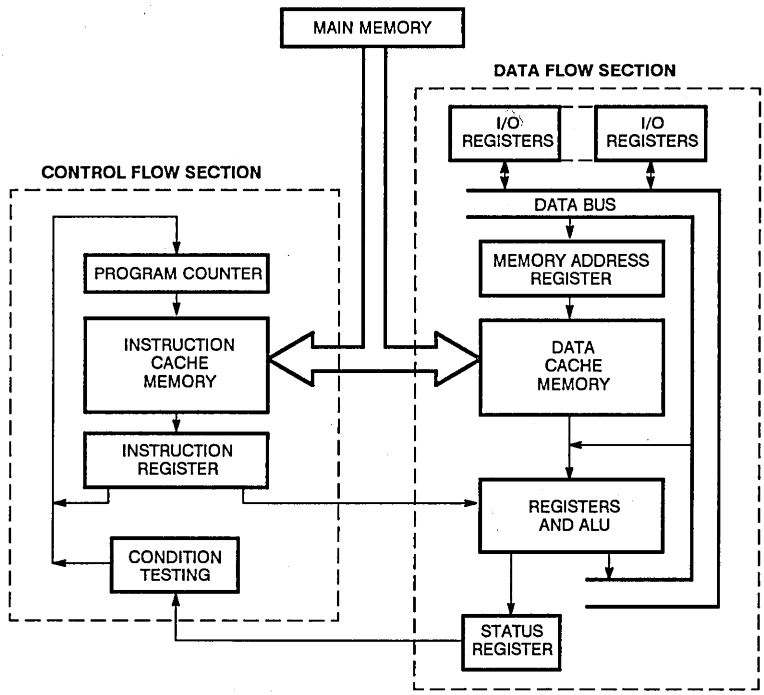


Figure 2. RISC CPU Block Diagram

The instruction and data caches of the RISC architecture are equivalent to having two ports on one memory. We can apply this concept to bit-slice controllers by using a high-speed dual-port memory in place of the cache memories, as shown in Figure 3. The dual-port RAM allows the instruction and data ports to be active simultaneously and independently, while providing both sides access to a common set of RAM cells. Since both ports are working from the same memory, the data flow section can load and move both data and instructions in the same manner as a conventional microprocessor. As a result, this design functions as a conventional CPU with a long instruction word. This allows conventional interactive software tools, such as interpreters and monitors, to be used in system development and debugging.

DESIGN OF A RISC CONTROLLER

The design of a RISC controller using a dual-port control memory is similar to a conventional bit-slice design except for inclusion of a minimum set of operations for a CPU. This allows use as a conventional computer for software coding and debugging. In ordinary bit-slice controller designs, the minimal CPU operation set already exists as a subset of the data flow and control operations already present.

A minimal set of CPU operations, suitable for bit-slice designs, can be derived from the instruction set of a RISC-like computer such as the Data General Nova minicomputer. It is a useful example because it is a 16-bit general register design having approximately 20 instructions and three addressing modes, yet is fully functional as a computer. From its instruction set, the list of 21 operations shown in Table 1 can be derived as a representative minimum working set. If the design includes these operations, it will function as a CPU.

Table 1. Minimal CPU Instruction Set

1.	Load register from memory at immediate address (address in instruction).
2.	Load register from memory at address in a register.
3.	Store register to memory at immediate address (address in instruction).
4.	Store register to memory at address in a register.
5-11.	Move/combine registers: move, negate, invert, add, subtract, AND, OR.
12-13.	Shift: rotate left through sign, rotate right through sign.
14.	Read status register.
15.	Write status register.
16.	Jump absolute: load program counter with immediate address.
17.	Jump register: load program counter with register contents.
18-20.	Jump absolute conditional: if zero result, if sign, if carry.
21.	Jump and save return (Program Counter) in a register.

This instruction set assumes a set of general purpose registers (typically 16 or more in bit-slice designs), a memory which contains both instructions and data and a status register which records the result of register-to-register operations. I/O registers are assumed to be mapped into the memory space so that separate instructions for them are not required.

14

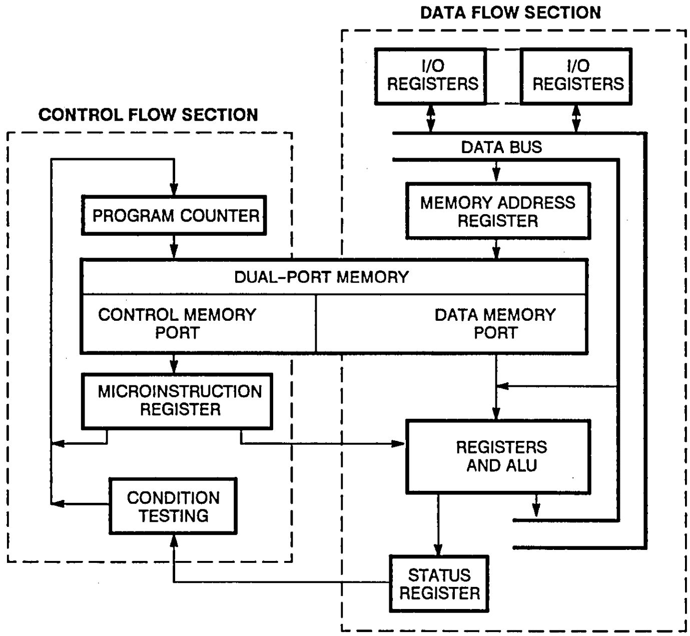


Figure 3. Bit-Slice Controller With Dual-Port Control Store

Some of the above operations are automatically included in bit-slice controllers as a result of staightforward design. The register combination operations are provided by the bit-slice RALUs and the jump operations are commonly required as part of the control flow design. All that is required to complete the set is the ability to transfer registers to and from memory, to save and restore the status register and to save the Program Counter in a register in Jump and Save Return instructions.

Figure 4 shows a block diagram of a general purpose bit-slice controller design, based on the RISC controller architecture in Figure 3, and capable of implementing the minimal instruction set. This is a 16-bit controller design using an IDT49C402 16-bit RALU and a 64-bit instruction word. The control flow section is fully pipelined for maximum speed and uses a simple counter as the Program Counter (PC). As a result, branch execution is delayed by one instruction: the instruction following the branch is executed before the branch takes effect. This method allows maximum speed in the control flow section and is commonly used in RISC designs. A path is provided from the PC to the data inputs of the IDT49C402 for saving the PC in a register during Jump and Save Return operations. Also shown in the block diagram is an initial-load EPROM. This EPROM holds the non-volatile copy of the program to be loaded at power up. A power up flip-flop and some sequencing logic cause the contents of this EPROM to be loaded into the RAM at power up.

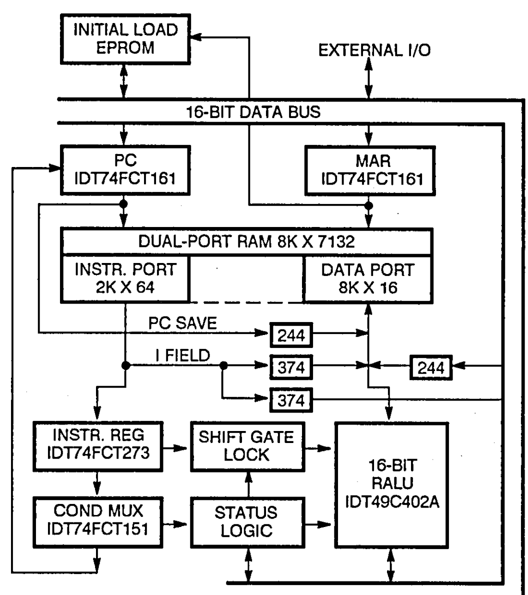


Figure 4. Dual-Port Bit-Slice RISC Controller Design Block Diagram

In the design in Figure 4, the instructions and data share the same memory. The mapping for instructions and the mapping for data are different, however, as is shown in Figure 5. The eight dual-port RAM chips are mapped as 2K words of 64 bits/word on the instruction port and as 8K words of 16 bits/word on the data port. Each 64-bit instruction word corresponds to four sequential 16-bit data words. The instruction at address 0000 on the instruction port corresponds to locations 0000, 0001, 0002 and 0003 on the data port. On the instruction port, all eight chips are enabled, resulting in 64 bits of instruction output. Only the upper 14 bits of the PC are used to address the RAM so that the address in the PC is consistent with the addressing on the data side. On the data port, the least significant two bits of the address in MAR select the appropriate 16-bit word by selecting the chip enable for the appropriate one of four pairs of chips.

RISC CONTROLLER INSTRUCTION FORMAT

The 64-bit instruction word is shown in Figure 6. Fifty of the 64 bits are used to control the basic data and control flow of the controller and 14 bits are available as additional control bits for the specific controller application. Each 64-bit instruction word from the control port of the RAM is mapped as four 16-bit words on the data memory port. A larger instruction word can be used in the same manner as in microcoded designs. It is convenient if the word width is a power of two, such as 64 or 128 bits, so that there are no gaps in the memory space as seen from the data flow side.

The IDT49C402 is controlled by the A and B fields, $I_{0\text{-}9}$, C_N, Stat Enable field and the Shift Gating field. The A and B fields provide the 6-bit addresses for the A and B register inputs on the IDT49C402. The $I_{0\text{-}9}$, C_N and Stat E_N field provide the 10 control bits to the IDT49C402, the carry-in bit and a status register load enable, respectively, and the Shift Gating field controls the shift-in/shift-out gating for shift operations. The data source for the D_{IN} pins of the IDT49C402 is selected by the D_{IN} field. This field can choose the data bus, the immediate data field or the PC as the data source.

The data bus is controlled by the A and B fields as well, which provide 6-bit select codes for bus read and write operations, respectively, and by the bus read/write, memory write and load MAR bits. The default operation is to gate the data from the IDT49C402 onto the data bus. The load MAR and memory write bits allow writing this data into the memory and/or MAR from the bus. The bus read bit disables the IDT49C402 outputs and gates an I/O register onto the bus as determined by the 6-bit A field. The bus write bit causes bus data to be written into an I/O register selected by the B field.

Branch operations are controlled by the Jump and A fields. The Jump field enables loading of the PC from the bus, which is the branch operation. The A field provides the 6-bit condition select code for conditional branch operations.

The Misc Control field provides 14 bits for direct control of additional devices. This field would typically be used for gates and strobes to additional devices such as parallel multipliers, FIFOs, disk controller chips and other devices which communicate with, and are controlled by, the RISC controller.

IMPLEMENTING THE MINIMAL INSTRUCTION SET

The RISC controller design must now be checked to ensure that it implements each instruction in the minimal instruction set.

Load and Store

Load and Store register operations are done in two instructions: load MAR and load or store register. The load MAR instruction places register data from the IDT49C402 or data from the immediate data field on the bus and enables MAR load. The load register instruction gates memory data into the data inputs of the IDT49C402. The store register instruction gates register data onto the bus and writes it into memory.

Move, Combine and Shift Register

Register-to-register and shift operations are performed directly by the IDT49C402 bit-slice.

Status Register Read/Write

Read and Write Status register operations select the Status Register and bus read and write, respectively.

Jump and Conditional Jump

Jump operations are done by enabling the PC to be loaded from the bus using either immediate or register data for the jump address. Conditional Jump is done by enabling a conditions select multiplexer to conditionally enable the PC load.

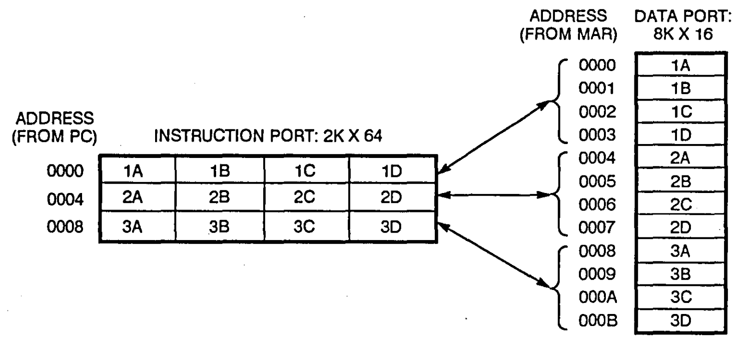
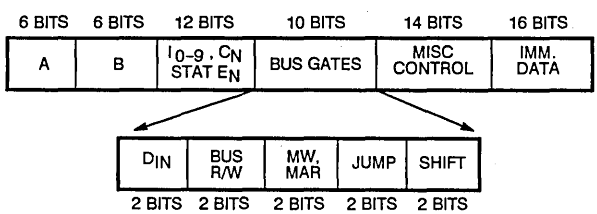


Figure 5. Dual-Port Controller Memory Map



FIELD	FUNCTION
A	402 reg address, bus read select, or jump condition select
B	402 reg address or bus write select
I_{0-9}	49C402 instructions + carry-in
Stat EN	Enable Status reg load
D_{IN}	402 D Bus: Memory, PC, Bus, I field
Bus R/W	Gate Bus read @ A, write @ B
MW, MAR	Memory write enable, ld MAR enable
Jump	Enable PC load, enable condition test
Shift	402 shift/rotate gating
Imm Data	Immediate Data - addresses, etc.
Misc Control	Misc bits for controller functions

Figure 6. Dual-Port Controller Instruction Format

Jump and Save Return

The Jump and Save Return operation is performed by using the immediate data field to provide the jump address and simultaneously storing the PC in a register selected by the B field. The immediate data field is gated to the bus, the PC is gated to the IDT49C402 data inputs and the IDT49C402 is instructed to perform a D-input-to-register-load operation.

RISC CONTROLLER TIMING

The design in Figure 4 is capable of a 55ns cycle time. A timing diagram for a 55ns cycle time, assuming the 35ns dual-port RAMs, is shown in Figure 7. The critical timing path, in this case, is the data path from the Memory Address Register (MAR) through the data port of the memory into the IDT49C402. If the dual-port RAMs are slower than 35ns, the cycle is extended proportionately.

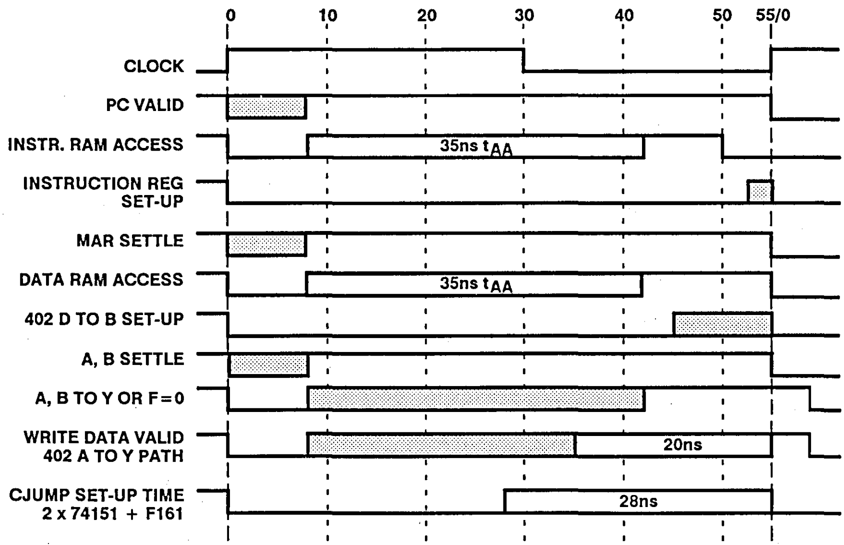


Figure 7. RISC Controller Timing Diagram

Table 2. Critical Path Timing

CONTROL PATH		DATA PATH	
PC settle: FCT161A	6.5ns	MAR settle: FCT161A	6.5ns
RAM Access	35.0	RAM Access	35.0
I reg set-up: FCT374A	2.5	IDT49C402A, Din Set-up	10.0
Total	**44.0ns**	**Total**	**51.5ns**

RISC CONTROLLER APPLICATION

The utility of the RISC controller design approach is that it allows interactive system development, debugging and diagnostic testing. It also provides the potential for high-level language support of the bit-slice design. Powerful interactive access to the RISC controller can be provided by an RS-232 interface and a FORTH language interpreter program. This allows interactive coding and testing of the system, speeding up the test-and-analyze debug cycles. This RS-232 interface can exist on a separate board external to the RISC controller, connected to the bus by a connector on the controller board. No additional hardware is required for access by the designer to the system and this access can allow direct activation and sensing of controller hardware, setting up timing loops for oscilloscope checks and on-line development of routines. If a floppy disk controller is included in the external I/O board, the RISC controller can function as a stand-alone development system in the same fashion as other stand-alone FORTH systems.

The RISC controller's ability to load programs also means that diagnostics can be loaded from the initial load EPROM . The initial load EPROM can hold both the normal control program and various test programs. The controller can load diagnostic programs from the EPROM for board and system test without requiring permanent space for them in the control memory. This allows self-diagnostics at the hardware level with minimum cost impact on the hardware.

SUMMARY

The RISC controller uses high-speed dual-port RAMs to blend the features of a bit-slice controller with the capabilities of a RISC computer, allowing the microinstructions of the bit-slice approach to become the instructions of a computer. This design approach provides all the speed and architectural flexibility of microcoded bit-slice designs, while allowing the use of interactive debugging methods associated with microprocessors to shorten development time.

LOW POWER AND BATTERY BACKUP OPERATION OF CMOS STATIC RAMS

Integrated Device Technology, Inc.

APPLICATION NOTE AN-10

By DAVID C. WYLAND

INTRODUCTION

High-speed CMOS static RAMs are capable of very low-power operation in the standby mode when the chip is disabled. In a properly designed circuit, the standby power may be a few microwatts, as compared with several hundred milliwatts when the RAM is operating. This low-power capability can be used by the designer to reduce system power and heat loading. It also makes these parts suitable for battery backed permanent storage applications. In these applications, power is kept on the RAM at all times to avoid the loss of data when power is removed from the part. This is done by using a battery to supply power to the RAM when system power is shut off. In these applications, low standby power drain is important in order to achieve long battery life with a reasonably sized battery. In this application note, we study the operating and standby power modes of the CMOS static RAM, the methods for achieving low-power standby operation and some of the methods for implementing battery backup operation.

CMOS RAM Power Consumption

CMOS RAMs have five regions of operation with a different power consumption for each region. These regions are: dynamic operating, DC operating, TTL standby, CMOS standby and battery backup standby. In the dynamic operating region, the RAM is reading and writing at speeds up to its rated read/write cycle time. In the DC operating region, the RAM is enabled but not cycling: its address, data and control inputs do not change. In the TTL standby mode, the RAM is disabled with its various address, data and control inputs at TTL levels, either static or cycling at the rated cycle time. In the CMOS standby region, the RAM is disabled and all inputs are at CMOS levels (i.e., within 0.20 volts of ground or V_{CC}).The battery backup standby region is similar to the CMOS standby region, but with a reduced power supply voltage of 2.0 or 3.0 volts rather than the normal 5.0 volts. The five regions of operation are shown in Figure 1. It shows a plot of I_{CC} versus operating region for an IDT7187L25, a 64Kx1 CMOS static RAM with a 25ns access time. The highest current, I_{CC2}, occurs under dynamic operating conditions where the part is cycling at its access time, a frequency equal to $1/t_{AA}$. The device current decreases linearly with frequency to the static operating current, I_{CC1}. When the chip is disabled, current drops immediately to I_{SB}, the TTL standby current, or below. I_{SB} corresponds to the current drawn by the chip when it is disabled and with all inputs at TTL high or with all inputs changing at the rated cycle time. With the inputs at TTL high, each input circuit is in its linear threshold determining region and drawing supply current. The device current linearly decreases from I_{SB} to I_{SB1} as the various inputs are changed from TTL high levels to CMOS levels which are within 0.20 volts of V_{CC} or ground. I_{SB1} is the full CMOS standby current for 5.0 volt V_{CC}. There are two other CMOS standby cases, specified by I_{CCDR}. I_{CCDR} corresponds to I_{SB1} but is measured at two other power supply voltages, 2.0 and 3.0 volts. The I_{CCDR} specification is used in battery backup applications to calculate the battery size required for a given battery lifetime. The 2.0 or 3.0 volt power supply voltages correspond to those typically available from battery systems in battery backed applications.

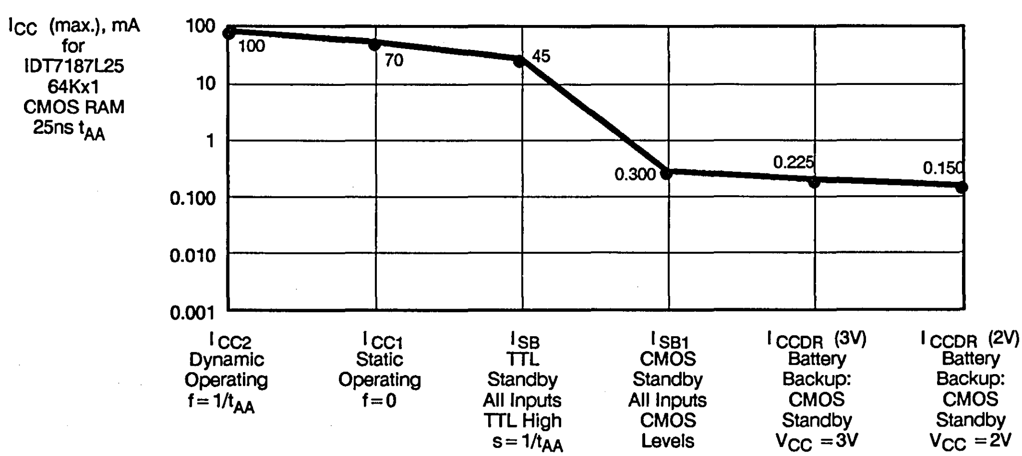


Figure 1. CMOS RAM Operating Regions

Printed in the U.S.A. 9/87

Components of Power Dissipation

There are five major sources of power dissipation in CMOS RAMs:

- The RAM array
- The sense amplifiers
- The input buffers
- Dynamic switching
- Diode leakage

The RAM array power is that required to power the RAM cells that hold the data. It is continuously drawn and is required to keep data stored in the RAM. The sense amplifier power is that required to read the data from the RAM array. It is drawn only when the chip is enabled. Each input to the RAM chip has a buffer which draws power when its input voltage is between 0.5 and 4.0 volts. In this region, the input buffer operates as a linear device, performing a logic threshold comparison. If the input is within 0.20 volts of V_{CC} or ground, the input buffer draws no power. Static RAMs draw additional power if they are cycled continuously at high speed. The additional power required is the dynamic switching power. It rises linearly with the average frequency of read/write cycles. Diode leakage is the current drawn by reversed biased diodes on the chip, such as CMOS gates that are not switching. It is a small value at room temperature, but it is strongly temperature-dependent, doubling approximately every +10°C. Because of its strong temperature dependence, it is usually the dominant component in CMOS standby power specifications, such as the I_{CCDR} specification used in battery backed RAM calculations. Diode leakage and RAM array power are two unavoidable components of RAM power dissipation.

Standard and Low-Power RAMS

IDT RAM chips are divided into two types, standard power and low power. This is indicated by a letter suffix to the part number, S or L, respectively. These part types are power dissipation test selections from a single product, similar to speed grade selections. The low-power part is selected for low-power standby operation and fully specified for the battery backup mode. The standard-power part has relaxed power specifications in the form of higher limits on all I_{CC} specifications, particularly the standby power modes, and it is not specified for battery backed operation. Because of its relaxed power specifications, it is usually less expensive. The standard-power part is used where very low standby power is not required, such as applications where the part is continuously enabled.

Dynamic Operating Current—I_{CC2}

The dynamic operating current specification applies when the RAM is cycling at its specified access time. In the case of the IDT7187L25, the access time is 25ns and the frequency at which I_{CC2} is measured is 1/25 = 40MHz. I_{CC2} consists of two components: the DC operating component, I_{CC1}, and a frequency dependent component equal to (I_{CC2} - I_{CC1}). In the case of the IDT7187L25, the I_{CC2} value is 100 milliamperes and the frequency dependent component is 100 - 70 = 30 milliamperes. Note that, as the specified access time goes down, the specified dynamic operating current goes up. This is because the dynamic operating current is measured at a frequency equal to the inverse of the access time. Fast access RAMs are measured at higher frequencies than slow ones and have higher frequency dependent current components.

The dynamic current component of I_{CC2} is the result of transient currents in the internal CMOS gates when they switch. These transient currents can be understood by examining the switching behavior of CMOS circuits. The basic building block of CMOS circuits, including RAMs, is the CMOS logic gate. An example of a simple CMOS gate, an inverter, is shown in Figure 2. It consists of an N-channel device, Q1, and a P channel device, Q2. If the input is high, Q1 will be on, Q2 will be off and the output will be low. If the input is low, Q2 will be on, Q1 will be off and the output will be high.

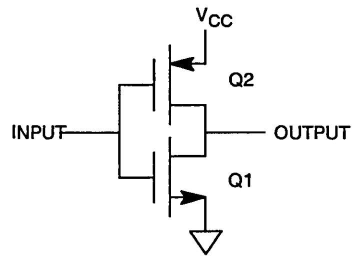


Figure 2. CMOS Inverter

This CMOS gate draws momentary current only when it changes state. It draws no current when its input is at ground or V_{CC} because one of the two transistors will be off, eliminating a direct path from V_{CC} to ground. This is what makes CMOS an inherently low-power technology—it draws no static current. However, it does draw current momentarily when it changes state. When the input transitions from low-to-high or high-to-low, it will pass through the middle region where both Q1 and Q2 are on. During this transition time, current will flow through Q1 and Q2. Since the current flows only during the transition time, there is a fixed amount of charge transferred from V_{CC} to ground for each transition. This results in a frequency-dependent current consisting of the sum of all the charges transferred for all the gates on the chip times the frequency of the charge transfers—i.e., the frequency of cycling the RAM.

Static Operating Current—I_{CC1}

The static current specification applies when the RAM is enabled but with its various inputs not changing and held at a TTL high. In this condition, the RAM array, sense amplifiers and input buffers are all drawing current. For the case of the IDT7187L25, this is 70 milliamperes.

TTL Standby Current—I_{SB}

The TTL standby current specification applies when the chip is disabled but its inputs are at TTL levels or changing at the rated cycle time. Since a TTL high represents the worst case condition, I_{SB} is specified for the case of all inputs at TTL high.

In the TTL standby mode, the RAM array and input buffers draw current, with the input buffers drawing the majority. The input buffers are CMOS circuits similar to the CMOS inverter shown in Figure 2, but with the geometry of the transistors designed so that the input threshold is at a TTL-compatible threshold voltage of approximately 1.40 volts. A diagram of the device current versus input voltage for one input is shown in Figure 3. When the input is within 0.20 volts of ground or V_{CC}, one of the two transistors is turned off and no current flows. Very little current flows even for the TTL low case of 0.50 volts input. However, for the TTL high case of 3.0 volts typical, both transistors will be on and approximately 1.50 milliamperes, typical, will flow through them.

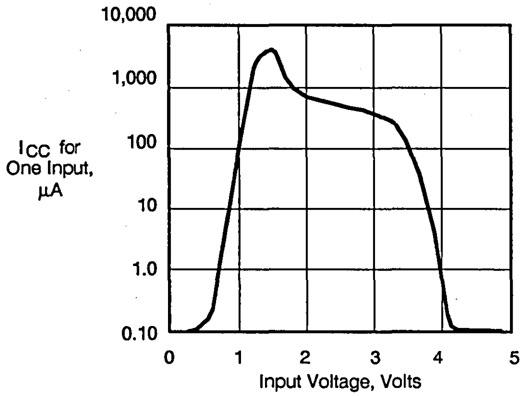


Figure 3. I_{CC} vs V_{IN} for One Input

CMOS Standby Current—I_{SB1}

The CMOS standby current specification applies when the chip is disabled and all its inputs are static (i.e., nonchanging) at CMOS levels—within 0.20 volts of V_{CC} or ground. In this state, only the RAM array and leakage currents are drawn. The RAM array current is relatively independent of temperature, while the diode leakage is strongly temperature dependent, rising dramatically with temperature. At +25°C, the total current for an IDT7187L25 consists primarily of RAM array current, which may be 25µA. However, at +70°C for commercial parts, the total current is specified at 300µA and is mostly leakage current. This rises to 1500µA at +125°C for military parts. A plot of I_{SB1} versus temperature is shown in Figure 4.

Battery Backed CMOS Standby Current—I_{CCDR}

The battery backed CMOS standby current specification applies when the chip is disabled and all its inputs are at CMOS levels (i.e. within 0.20 volts of V_{CC} or ground) and when V_{CC} is at a reduced voltage of 2.0 or 3.0 volts. It is the same as I_{SB1} except it is measured at V_{CC} voltages of 2.0 and 3.0 volts. In this state, only the RAM array and leakage currents are drawn.

When V_{CC} is reduced to 2.0 or 3.0 volts, the RAM is guaranteed to retain data stored at 5.0 volts, but may not function: i.e. it may or may not read or write reliably at these voltages. For this reason, the chip is kept disabled while V_{CC} is below 5.0 volts. When V_{CC} is restored to 5.0 volts, full functional operation is restored and the data will remain as it was before V_{CC} was reduced.

DESIGN OF A HIGH-SPEED CMOS RAM MEMORY ARRAY

CMOS RAMs are often used in memory arrays. Figure 5 shows a CMOS RAM array used as high-speed main memory for a 32-bit microprocessor. The high speed of the CMOS devices allows operation of the microprocessor at full speed without wait states. Figure 6 shows an example of a design of such a memory array using techniques which allow high-speed operation at low power.

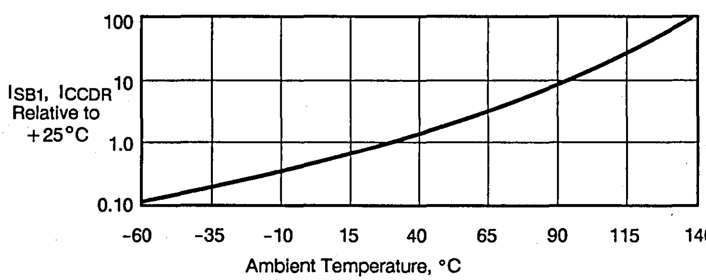


Figure 4. I_{SB1} and I_{CCDR} vs Temperature

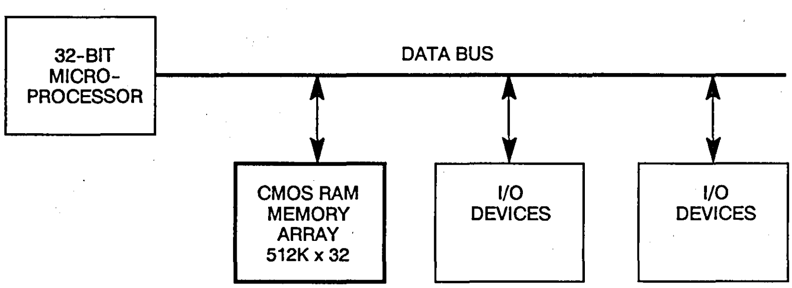


Figure 5. CMOS RAM Array with 32-bit Microprocessor

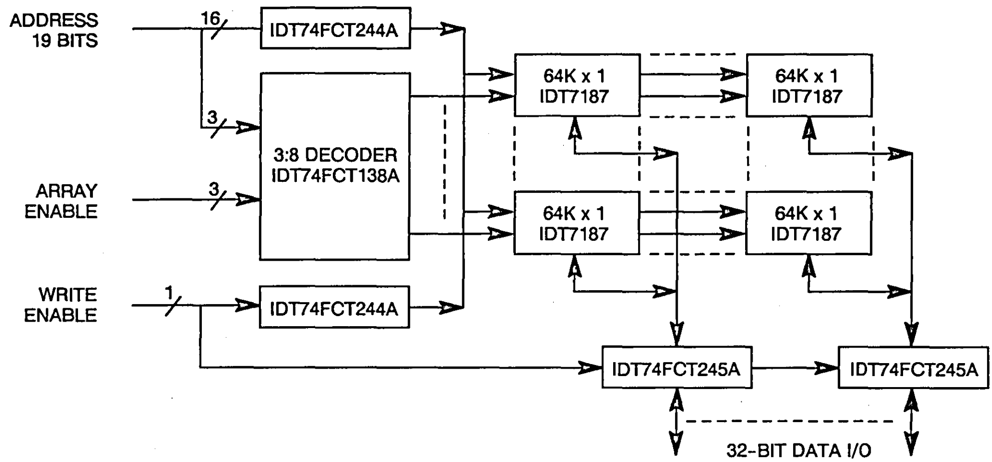


Figure 6. CMOS RAM Array Design

The 512Kx32 memory array of Figure 5 consists of 256 RAM chips, each 64Kx1, arranged as an array of eight rows of 32 devices. The array is driven by CMOS devices capable of driving the RAM inputs to CMOS levels within 0.2 volts of V_{CC} or ground. An IDT74FCT138A 3-to-8 line decoder enables one row at a time. If the decoder is disabled, all RAM chips are disabled. The address and write enable inputs are driven by IDT74FCT244A non-inverting buffers and the data lines are buffered by a set of IDT74FCT245A transceivers. Four sets of IDT74FCT244A buffers are used for the address and write enable inputs, with each buffer driving 64 chips. This reduces the capacitive loading on each buffer to maintain high speed. One set of IDT74FCT245A transceivers is used since each one drives only eight RAM data inputs.

CMOS RAM arrays draw significantly less power in standby mode if the RAM inputs are driven to CMOS levels. This is shown in Table 1 for the RAM array of Figure 6. In this table, the total current of the RAM array is shown for the case of TTL and CMOS drivers for the address and control lines.

Dynamic Operating Power for TTL vs CMOS Drivers				
Part	**Qty.**	**I_{CC} Using 74F Bipolar**	**I_{CC} Using FCTA CMOS**	**Comments**
IDT7187L25	32	3200	3200	Enabled, I_{CC2}
IDT7187L25	224	10,080	10,080	Disabled, I_{SB}
244	9	810	116	74F244/74FCT244A
245	4	440	52	74F245/74FCT245A
138	1	20	5	74F138/74FCT138A
Total		**14,550 mA**	**13,453 mA**	

Standby (non-operating) Power for TTL vs CMOS				
Part	**Qty.**	**I_{CC} Using 74F Bipolar**	**I_{CC} Using FCTA CMOS**	**Comments**
IDT7187L25	256	11,520	77	Disabled, I_{SB}/I_{SB1}
244	9	810	116	74F244/74FCT244A
245	4	440	52	74F245/74FCT245A
138	1	20	2	74F138/74FCT138A
Total		**12,790 mA**	**247 mA**	

Table 1. CMOS RAM Array Power

The power savings from using CMOS drivers can be dramatic, as shown in Table 1. The difference between the CMOS and bipolar current is only 7.6% in the dynamic case but, in the standby, non-operating case, the current differs by a factor of 51.8. The lower standby current with CMOS drivers occurs because the RAM inputs are kept at CMOS levels, putting them into the I_{SB1}, CMOS standby region. Using CMOS drivers does not, however, put the unselected rows into the I_{SB1} region during dynamic operation of the array. This is because the address and data inputs to the unselected RAM chips are changing rather than being held at static levels. Thus, I_{SB} must be used instead of I_{SB1} in these calculations.

The dynamic and standby I_{CC} specifications assume that the RAM is cycling at its rated cycle time. The cycle time of the RAM array will be longer than the rated cycle time of the RAM chips. This will reduce both the dynamic operating current of the enabled row and the standby power of the disabled rows. A conservative estimate of the current requirement reduction can be made by reducing the current of the disabled rows by the ratio of the RAM chip rated cycle time to the RAM array cycle time. If the RAM chip cycle time is 25ns and the RAM array cycle time is 100ns, the current required by the disabled rows will be (0.25*10,080 + 0.75*67) = 2,570mA. The current savings will be (10,080-2,570) = 7,510mA. The RAM array operating current will therefore be (13,453 - 7,510) = 5,943mA, a reduction of 56%.

RAM Array Speed Considerations

CMOS RAM arrays can achieve low power while maintaining high speed. This is done by using the high speed of the CMOS RAM chips and taking care that speed is not lost in the surrounding logic. The primary problem in driving large RAM arrays is driving the capacitance of the address and data inputs.

The speed of the array is a combination of the propagation delay of the RAM chips, the circuits driving them and the time delay caused by driving the capacitance of the array. The time delay caused by driving the capacitance depends on the design of the array. This delay is proportional to the capacitance being driven by each IC output, with a typical design value of 3.0ns/100pF for FCT logic and 6.0ns/100pF for RAM outputs. This delay applies to capacitance above the rated load capacitance for the device, which is 50pF for FCT devices and 30pF for the IDT7187 RAM. This delay applies for address and write enable drivers driving the RAM chip inputs and for each RAM chip driving other RAM outputs and its IDT74FCT245 input. In this design, the RAM chip input capacitance is 5.0pF/input, and the output capacitance is 7.0pF/output. Since the RAM data input and output pins are connected together, the total capacitance is (5.0+7.0) = 12.0pF/RAM chip. Thus, each RAM output must drive seven RAM outputs, eight RAM inputs and one IDT74FCT245 input for a total of (7*7+8*5+5=5)=94pF. The net capacitance used in the delay calculation is (94-30) = 64pF and the corresponding delay is (6*64/100) = 3.84ns.

If one set of drivers is used to drive all the devices, the capacitance can be high and the delay can be significant compared to the delay of the RAM chips. In high-speed designs, several drivers are used so that the capacitance seen by each driver is moderate and the speed delay is small. A comparison of the total propagation delay of a RAM array for various combinations of drivers is shown in Table 2.

To design a RAM array for high speed, both the address and chip select paths must be considered. In Table 2, the propagation delay with capacitive loading is calculated for both paths and the larger of the two numbers is used to calculate the access time of the array as a whole. Note that the critical path changes from address to chip select as the capacitive loading of the address drivers is reduced.

Address and Chip Select Path Delays vs Capacitive Drive

Delay Source	256/Driver		64/Driver		32/Driver		16/Driver	
	Cap	Delay	Cap	Delay	Cap	Delay	Cap	Delay
IDT74FCT244A	-	4.3	8	4.3	16	4.3	32	4.3
Addr Cap Delay *	1280	36.9	320	8.1	160	3.3	80	0.9
IDT7187L25 - t_{AA}	-	25.0	-	25.0	-	25.0	-	25.0
Addrs Path Delay	-	66.2	-	37.4	-	32.6	-	30.2
IDT74FCT138A	-	5.8	-	5.8	-	5.8	-	5.8
$\overline{CS}$ Cap Delay *	160	3.3	160	3.3	160	3.3	80	0.9
IDT7187L25 - t_{ACS}	-	25.0	256	25.0	256	25.0	256	25.0
$\overline{CS}$ Path Delay	-	34.1	-	34.1	-	34.1	-	31.7

* 3ns/100pF - 50pF

RAM Array Access Time vs Capacitive Drive

Delay Source	256/Driver		64/Driver		32/Driver		16/Driver	
	Chips	Delay	Chips	Delay	Chips	Delay	Chips	Delay
IDT74FCT244A	2	-	8	-	16	-	32	-
IDT7187L25	256	-	256	-	256	-	256	-
IDT74FCT138A	2	-	2	-	2	-	4	-
Path Delay	-	66.2	-	37.4	-	34.1	-	31.7
IDT74FCT245A	4	4.6	4	4.6	4	4.6	4	4.6
Out Cap Delay **	-	3.8	-	3.8	-	3.8	-	3.8
TOTAL	264	74.6	270	45.8	278	42.5	296	40.1

** 6ns/100pF - 30pF

Table 2. CMOS RAM Array Speed vs Drive

Using RAM Modules to Save PC Board Space

RAM modules can be used to significantly reduce the printed circuit (PC) board area required for a RAM array. A RAM array using 256 chips (of the IDT7187 type) will require approximately (0.4 * 1.2 * 256) = 122.88 square inches of board space, assuming 24-pin, 300 mil DIP devices with 0.1 inch spacing. RAM modules, such as the IDT7M624, use surface mounting to fit sixteen of the IDT7187 RAM chips on a 2.0 x 0.9 inch DIP module. Sixteen of these modules could directly replace the 256 RAM chips in the array. The PC board area using these modules would be (16*2.0*1.0) = 32 square inches, assuming 0.1 inch spacing, a savings of approximately a factor of four over mounting individual chips.

ARRAY DESIGN FOR LOW POWER

The RAM array design of Figure 6 can be redesigned for lower operating power by using CMOS RAM chips with input gating, such as the IDT7164, 8K x 8 RAM. An example of such a design is shown in Figure 7. Table 3 compares the characteristics of the low-power design in Figure 7 against the high-speed design in Figure 6.

In parts with input gating, the input circuits are powered down when the chip is disabled. These parts have very low TTL standby I_{SB} values because only the chip select inputs are on in the TTL standby case. In RAM array design, this means that the disabled rows have very low standby power when compared to RAMs with conventional inputs, as used in the design of Figure 6.

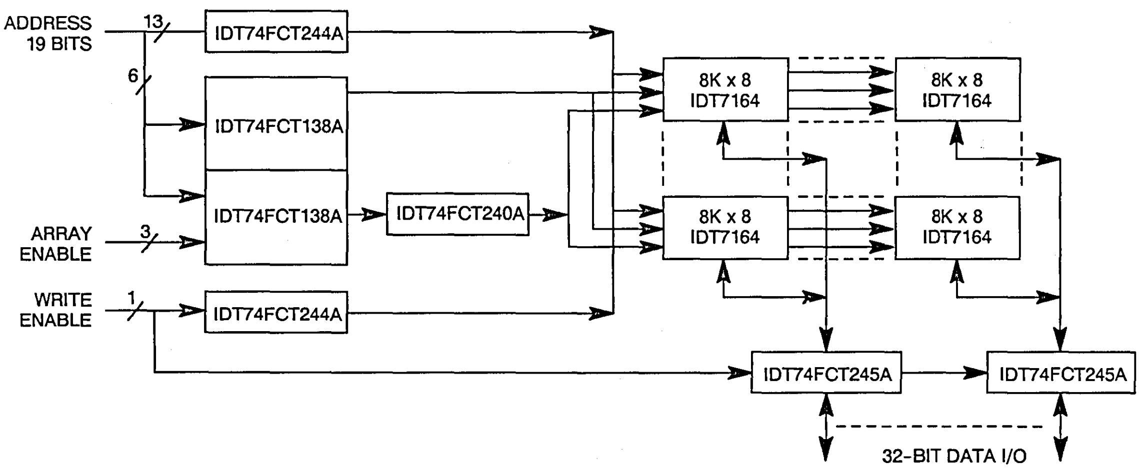


Figure 7. Low-Power CMOS RAM Array Design

Function	High-Speed Design	Low-Power Design	Units	Comments
RAM Chip Type	IDT7187	IDT7164		
Chip Organization	64Kx1	8Kx8		
Speed: t_{AA}	42.5	64.7	ns	32/driver
Operating Power	13,453	853	mA	
Standby Power	247	81	mA	
Part Count	278	276	ICs	32/driver
Battery Power, 3.0 V	81.6	30.5	mA	at +70°C

Table 3. Comparison of High-Speed vs Low-Power Array Designs

The 512K x 32 memory array in the low-power design shown in Figure 7 consists of 256 RAM chips, each 8K x 8, arranged as an array of 64 rows of 8 devices. The array is driven by CMOS devices capable of driving the RAM inputs to CMOS levels, within 0.2 volts of V_{CC} or ground. Two IDT74FCT138A, 3-to-8 line decoders are used with the two RAM chip selects to enable only one row at a time. An IDT74FCT240A inverter is used between one decoder and the RAM array to drive the positive active RAM chip enable. If either decoder is disabled, all RAM chips are disabled. The address and write enable inputs are driven by IDT74FCT244A non-inverting buffers and the data lines are buffered by a set of IDT74FCT245A transceivers. Four sets of IDT74FCT244A buffers are used for the address and write enable inputs, with each buffer driving 64 chips. This reduces the capacitive loading on each buffer in order to maintain high speed. Two sets of IDT74FCT245A transceivers are used to reduce the loading on the RAM output pins so that each RAM drives only 32 outputs.

The CMOS RAM array in Figure 7 draws significantly less power than the design in Figure 6, as is shown in Table 4. The primary reasons for this reduction are that the rows that are disabled draw very little power due to their gated inputs and only four RAMs in a row are enabled at any one time rather than 32. The result is that the dynamic power is reduced by a factor of 15.7 and the standby power is reduced by a factor of 3.0. Note that I_{SB1} is used in calculating the power of the disabled rows. This is because there is no dynamic standby effect with input gated RAMs since the input buffers are turned off. Also, since the chip enables are driven to CMOS levels by CMOS devices, there is no TTL standby current drawn by the chip select inputs.

Low-Power RAM Array Speed Considerations

RAM array speed considerations for the low-power design in Figure 7 are similar to those of the design in Figure 6. The delay for the address and chip select paths are calculated and the larger of the two numbers is used in calculating the total delay. The total delay for various combinations of driver loading is shown in Table 5.

RAMs with gated inputs (i.e., input buffers powered up by chip select) trade speed for low power. Gating the inputs with the chip select means that the chip select access time is equal to, or longer than, the address access time. This means that the chip select decode propagation delay is no longer hidden by a fast chip select access time. As a result, the chip select path is usually the critical path in gated input designs.

The design in Figure 7 is somewhat slower than the design in Figure 6 because x8 RAMs rather than x1 RAMs are used. In the minimum chip count configuration, each RAM output in Figure 6 drives seven other RAM outputs, plus an IDT74FCT245A input. In the minimum chip count design in Figure 7, each RAM output drives 63 other RAM outputs, plus an IDT74FCT245A input. This is the source of another tradeoff of speed versus chip count in the RAM output path. The output drive problem is helped by the fact that the IDT7164 RAMs are common I/O devices with a capacitance of 7.0pF per I/O pin, rather than the combined capacitance of 12.0pF for the IDT7187 design which ties the input and output pins together.

Dynamic Operating Power for Low-Power RAM Array			
Part	**Qty.**	**I_{CC} Using FCT CMOS**	**Comments**
IDT7164L30	4	560	Enabled, I_{CC2}
IDT7164L30	252	50	Disabled, I_{SB1}
IDT74FCT244A	8	103	
IDT74FCT245A	8	103	
IDT74FCT138A	2	11	
IDT74FCT240A	2	26	
Total		**853mA**	13,453mA for Fig. 6.

Standby Power for Low-Power RAM Array			
Part	**Qty.**	**I_{CC} Using FCT CMOS**	**Comments**
IDT7164L30	256	51	Disabled, I_{SB1}
IDT74FCT244A	8	12	
IDT74FCT245A	8	12	
IDT74FCT138A	2	3	
IDT74FCT240A	2	3	
Total		**81mA**	247mA for Figure 6

Table 4. CMOS RAM Array Power

Address and Chip Select Path Delays vs Capacitive Drive								
Delay Source	256/Driver		64/Driver		32/Driver		16/Driver	
	Cap	Delay	Cap	Delay	Cap	Delay	Cap	Delay
IDT74FCT244A	-	4.3	8	4.3	16	4.3	32	4.3
Addr Cap Delay *	1280	36.9	320	8.1	160	3.3	80	0.9
IDT7164L30 - t_{AA}	-	30.0	-	30	-	30	-	30
Addrs Path Delay	-	71.2	-	42.4	-	37.6	-	35.2
IDT74FCT138A	-	5.8	-	5.8	-	5.8	-	5.8
IDT74FCT244A	-	4.3	-	4.3	-	4.3	-	4.3
$\overline{CS}$ Cap Delay *	160	3.3	160	3.3	160	3.3	80	0.9
IDT7164L30 - t_{ACS}	-	35.0	256	35.0	256	35.0	256	35.0
$\overline{CS}$ Path Delay	-	48.4	-	48.4	-	48.4	-	46.0

* 3ns/100pF - 50pF

RAM Array Access Time vs Capacitive Drive								
Delay Source	256/Driver		64/Driver		32/Driver		16/Driver	
	Chips	Delay	Chips	Delay	Chips	Delay	Chips	Delay
IDT74FCT244A	2	-	8	-	8	-	8	-
IDT7164L30	256	-	256	-	256	-	256	-
IDT74FCT138A	2	-	2	-	2	-	4	-
IDT74FCT240A	2	-	2	-	2	-	3	-
Path Delay	-	71.2	-	48.4	-	48.4	-	46.0
IDT74FCT245A	4	4.6	4	4.6	8	4.6	16	4.6
Out Cap Delay **	-	25.1	-	25.1	-	11.7	-	4.9
TOTAL	266	100.9	272	78.1	276	64.7	287	55.5

** 6ns/100pF - 30pF

Table 5. CMOS RAM Array Speed vs Drive

BATTERY BACKUP OPERATION OF CMOS RAMS

Because of their low standby power, CMOS RAMs are often used as permanent memory where a battery is used to maintain data in the RAM by supplying power when the system power is off. These are called battery backup applications. In battery backup applications, the battery supplies a lower voltage—2.0 to 3.0 volts versus the 5.0 volts of normal operation. This lower voltage allows use of a smaller battery, both because of the lower voltage for the same ampere-hour rating and because the RAM draws less current at the lower voltage.

The design of a battery backed RAM array includes consideration of the following problems:

- Driving the RAM inputs to CMOS levels during battery operation
- Determining the power drain in battery backup mode
- Switching from the system supply to/from the battery supply while maintaining V_{CC} at the RAM

Driving the RAM Inputs to CMOS Levels During Battery Operation

In order to achieve the low power levels specified for battery backup operation, the RAM inputs must be driven to CMOS levels. In the array design of Figure 6, this is done by driving the RAM chips with FCT CMOS drivers for the 5.0 volt V_{CC} case. These levels must also be guaranteed for the 3.0 volt V_{CC}, battery backed case. In the case of the FCT CMOS devices, the output drive is also specified to be at CMOS levels for the 3.0 volt V_{CC} case.

The RAM array drivers must be able to maintain CMOS output levels with 3.0 volt V_{CC} and maximum leakage from the RAM inputs and/or outputs. CMOS FCT drivers are used for the address, write enable, chip select and data inputs of the design in Figure 6. The worst case leakage will be for 64 address inputs being driven by a single driver. The maximum specified leakage for any input of the IDT7187L25 RAM chips is 2.0 microamperes at 3.0 volts V_{CC} over the temperature range. The maximum total leakage for 64 inputs will then be 128 microamperes. The IDT74FCT244A drivers are rated at an I_{OL} of 300µA and an I_{OH} of 32µA at 3.0 volts V_{CC}. If the address drivers are kept in the low state, the 300µA I_{OL} specification is more than enough to keep the outputs at a CMOS low level.

Additional drivers are required to keep the write enable and chip select inputs in the CMOS high state. The write enable drivers can be kept in the low state if the RAM chips are kept disabled; however, it would be more prudent to keep them in the high state to ensure that no write can possibly occur. This requires more drivers for these lines than the address lines. With a 32µA I_{OH} specification, each CMOS FCT part can drive a maximum of 16 inputs. Since each IDT74FCT244A supplies eight drivers, this would mean two chips instead of one for the write enable input. Two IDT74FCT138A decoders will also be required in order to have each decoder output drive only 16 RAM enable inputs. A drawing of the RAM array with this implementation is shown in Figure 8.

The FCT CMOS drivers will keep the RAM inputs at CMOS levels during battery backup mode; however, the inputs to the FCT devices must also be kept at CMOS levels during this mode. If the rest of the system which communicates with the RAM array is powered down, these inputs should be at or near zero volts, which solves this problem. To ensure this case, a resistor to ground should be added to the input of each FCT CMOS device to provide a path for the input leakage of these devices. A 10K resistor will support the input leakage of ten FCT devices at 2µA per device and a V_{OL} of 0.20 volts.

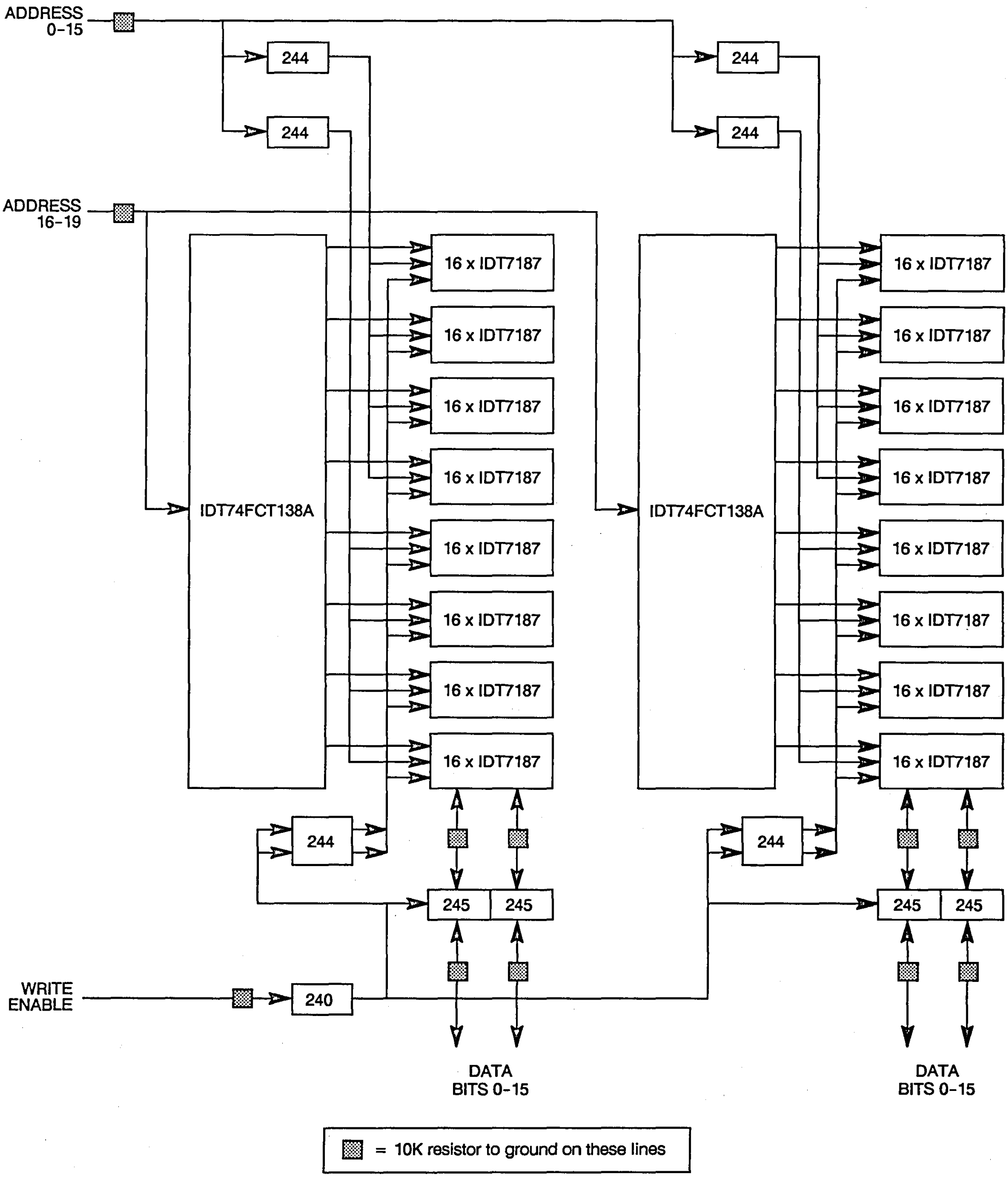


Figure 8. High-Speed CMOS RAM Array Design for Battery Standby

Determining the Current Drain in Battery Backup Mode

The RAM array standby current in battery backup can be calculated by adding the current required for the RAM chips and the current for the array drivers. A calculation of the current required for the RAM array of Figure 6 in the battery backup mode, including the additional drivers for write enable and chip select, is shown in Table 6.

Battery Backed Standby Current at 3.0 Volts				
Part	**Qty.**	**Typ., +25°C**	**Max., +70°C**	**Max., +125°C**
IDT7187L25	256	3.84	57.6	230.4
IDT74FCT244A	10	0.010	15.0*	15.0
IDT74FCT245A	4	0.004	6.0*	6.0
IDT74FCT138A	2	0.002	3.0*	3.0
Total	**272**	**3.9mA**	**81.6mA**	**254.4mA**

* Max. for commercially rated parts. Military rated parts will have lower values at +70°C.

Table 6. High-Speed CMOS RAM array Battery Standby Current

Battery Backed Operation of the Low-Power RAM Array Design

The low-power RAM array design in Figure 7 is well suited to battery backed operation. Because of the gated input design of the RAM chips, only the chip select inputs of the RAM need be driven to CMOS levels. This means increasing the number of decoders for the low active chip select from two to three so that each decoder drives a maximum of 16 inputs to V_{IH}. The non-inverting chip select input is not a problem because the IDTFCT240A driver will easily drive its 32 inputs to V_{IL}. Only the RAM chips, the IDTFCT138A decoders and the IDTFCT240A drivers need be powered by the battery.

The RAM array standby current in battery backup can be calculated by adding the current required for the RAM chips and the current for the array drivers. A calculation of the current required for the RAM array in Figure 7 in the battery backup mode, including the additional chip select decoders, is shown in Table 7.

Battery Backed Standby Current at 3.0 Volts				
Part	**Qty.**	**Typ., +25°C**	**Max., +70°C**	**Max., +125°C**
IDT7164L30	256	3.84	23.0	76.8
IDT74FCT138A	3	0.003	4.5*	4.5
IDT74FCT240A	2	0.002	3.0*	3.0
Total		**3.9mA**	**30.5mA**	**84.3mA**

* Max. for commercially rated parts. Military rated parts will have lower values at +70°C.

Table 7. Low-Power CMOS RAM Array Battery Standby Current

Switching Between System V_{CC} and the Battery

In a battery backup system, V_{CC} for the RAM array must switch between the battery and the system V_{CC} without causing the RAM to lose data in the battery backup mode and allowing the RAM to achieve full speed in the normal operation mode. This requires a switch design for V_{CC}. Also, the RAM array must be disabled during the battery backup mode and during switching between the battery and normal V_{CC}. This is done by using a power-down detect signal from the power supply which forces the RAM to be disabled.

When switching from the system to the battery, V_{CC} must be kept above the 2.0 volt minimum guaranteed data maintenance voltage at all times. When switching from the battery to the system, V_{CC} at the part must be within the V_{CC} specifications for nomal operation, (i.e., 4.5 volts minimum). These two requirements can be met by the circuit shown in Figure 9. In this circuit, the silicon diodes perform a smooth transfer of power from the system V_{CC} to the battery backed V_{CC} and vice-versa. The diode to V_{CC} is not strictly required because of the FET switch; however, it can reduce the switching transient when the FET turns on by reducing the voltage that must be switched, assuming that V_{CC} comes up slowly before the FET turns on.

The P-channel power FET is used to reduce the drop across the diode to 0.10 volt during normal operation so that the RAM array V_{CC} is kept within specifications. The IDT74FCT240A inverting driver is used to drive the gate of the P-channel power FET. When the power down signal is high, indicating normal system operation, the IDT74FCT240A output is low and the P-channel FET is on. When the power down signal is low, indicating that the power is going down or is already down, the IDT74FCT240A drives the

P-channel FET gate high to turn it off. When the battery is supplying the V_{CC}, the FET gate will be driven to the most positive voltage on either of its two terminals, ensuring that it will be off. Note that the circuit of Figure 1 is a typical example only—actual designs will differ depending on system requirements. For example, a PNP transistor or an N-channel FET with a gate drive to +12 volts could be used instead of the P-channel FET.

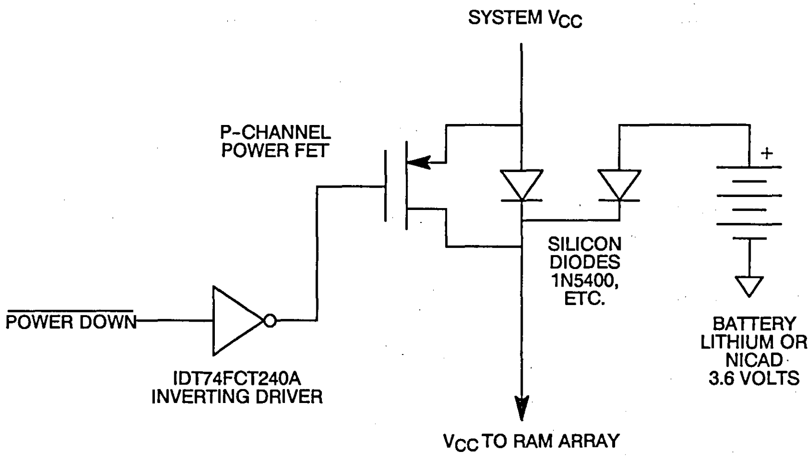


Figure 9. Battery Power Switch Circuit

CONCLUSION

CMOS RAMs have the capability of high speed and low power. In this application note, some of the possibilities for using these capabilities have been explored in the hope that the designer may use them to good advantage in new designs.

Integrated Device Technology, Inc.

A POWERFUL NEW ARCHITECTURE FOR A 32-BIT BIT-SLICE MICROPROCESSOR

APPLICATION NOTE AN-11

By Michael J. Miller

INTRODUCTION

Microprogram architectures are capable of meeting many of today's system design requirements. Nevertheless, trade-offs exist between performance and cost in terms of power consumption and the total number of parts needed to satisfy design functionality. For a given device family, cost considerations are directly related to the speed/power ratio. In recent years, advancements in speed/power performance for bipolar bit-slice technologies have slowed considerably while, at the same time, very high-speed CMOS has directly impacted the bit-slice world, offering greater functional speed and an increased level of integration.

Currently, packing density and the ultimate speed of performing a function in integrated circuits is limited by the heat dissipation capabilities of the chip package. Since CMOS has a speed/power ratio almost an order of magnitude higher than conventional bipolar device families, it is rapidly becoming the technology of choice for new bit-slice functions. Denser device packing at higher speeds gives CMOS technology more freedom for creating new high-performance architecture.

Historical Perspective

The most traditional bit-slice microprocessor architecture for the data path portion of the machine is the 2901 architecture, developed in the mid-seventies. A simplified diagram is shown in Figure 1. Here we see a tightly coupled RAM and ALU architecture which contains single input and output data paths. The 2901 is a 4-bit microprocessor slice that features 16 words of internal 4-bit wide RAM and an eight-function ALU capable of performing both arithmetic and logic operations on two operands. The ALU output can be loaded into the RAM, shifted up, shifted down or unshifted. Also included is an additional temporary register normally called the "Q Register". It is capable of performing double-length shift operations and facilitating multiplication and division. The 2901 has become the industry standard for bit-slice microprocessor architectures.

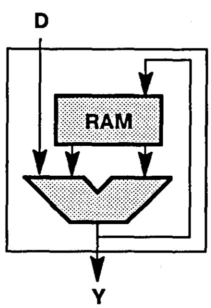


Figure 1. 2901 Architecture

An upgraded architecture, the 2903, was introduced in 1978 and is shown in Figure 2. The 2903 features a three-bus architecture for the data paths. Like the 2901, this slice contains a 16-word-by-4-bit dual-port RAM connected to an ALU which performs arithmetic and logic operations. This architecture, however, has the added capability of bringing external operands to the ALU via the DA and DB buses. The ALU can perform 16 different arithmetic and logic operations in all. Its output can be written shifted up or unshifted to either the RAM or the Y outputs. The 2903 architecture also incorporates several special functions which facilitate multiply, divide and sign magnitude to two's complement conversion. A special version of this architecture, known as the 29203, features both BCD and binary arithmetic capability. In addition, the DA, DB and Y buses are all bi-directional. Both the 2903 and 29203 also contain the internal Q Register used to perform double-length operations.

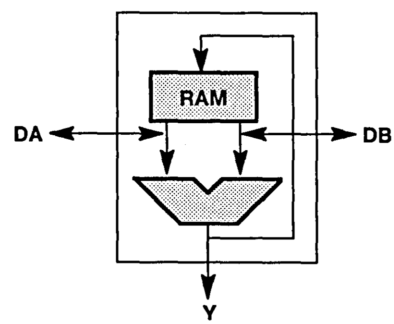


Figure 2. 2903/203 Architecture

A third architecture of historical importance is the 29116/29117. This architecture, shown in Figure 3, features a 32-word 16-bit single-port RAM, a 16-bit accumulator and a 16-bit D input latch. These three possible operand sources are connected to the ALU through a multiplexer. One path into the ALU contains a barrel shifter capable of rotating the 16-bit operand. The ALU can perform various combinations of operations on one or two operands. The three operand instructions are primarily rotate-and-merge or rotate-and-compare. The ALU output is fed back to both the RAM and the accumulator. In the 29116, the Y output is internally connected to the D input, forming a 16-bit bidirectional data bus. In the 29117, they remain separate and there is a 16-bit D input and a 16-bit Y output bus similar to the structure of the 2901. The 29116 contains an internal status register for the carry, overflow, sign and zero flags. Microinstruction to the 29116 is an encoded field instruction set.

CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.

Printed in the U.S.A. 10/87

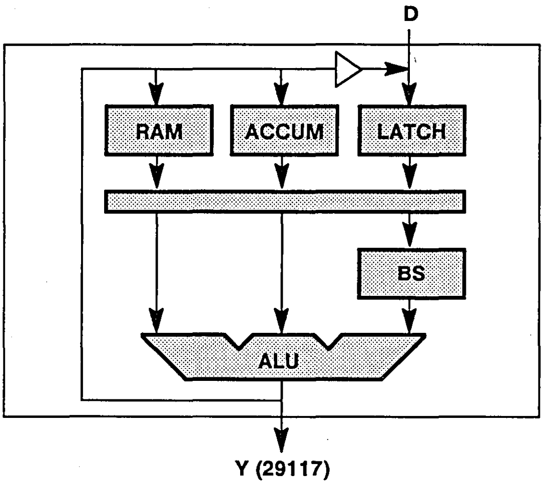


Figure 3. 29116/7 Architecture

New Technology for Bit-Slice

Integrated Device Technology's CEMOS™ technology offers greater speed and output drive at lower power levels. It was only natural to incorporate this technology into new bit-slice designs, thus offering improvements over the traditional "industry standards."

The IDT39C01 is totally pin-compatible and functionally identical to the 2901. The "C" grade version is equal to the fastest bipolar 4-bit slice and, in addition, IDT offers a "D" grade slice which is 25% faster than its "C" speed grade. Recently, IDT introduced an "E" grade which is 25% faster than the "D" grade.

The IDT39C03 and IDT39C203 are pin-compatible and functionally identical to the 2903 and 29203, respectively. IDT39C03 "B" grade and IDT39C203 "A" grade slices are also available. Again, these devices are about 25% faster and offer considerably higher output drive at lower operating power than their equivalent bipolar counterparts.

New and More Powerful Bit-Slice Devices

The order of magnitude difference in speed/power ratios between CMOS and bipolar technologies is leading to ever-increasing levels of CMOS integration. IDT has designed a new bit-slice family (the IDT49C000) which executes standard AMD 2900 microcode, but at greater than four times the circuit density. The key devices in this family are the IDT49C410, IDT49C402, IDT49C403 and IDT49C404. In general, these parts have wider data paths, more internal paths, larger RAM and support higher clock rates than their bipolar predecessors.

The IDT49C410 is architecture and function code-compatible with the 2910A and features an extended 16-bit address path which allows for programs up to 64K words in length. It is a microprogram address sequencer intended for controlling the execution sequence of microinstruction stored in microprogram memory. Thus, the IDT49C410 can be used at the heart of next generation designs to orchestrate the operation of other parts in IDT's MICROSLICE™ family of bit-slice devices.

The IDT49C402 and IDT49C403 are very-high-speed, fully cascadable 16-bit CMOS microprocessor slice units. The IDT49C402 performs the standard functions of four 2901s and a 2092 with a 2-bus architecture: one bus into the ALU and one bus out of the ALU. The IDT49C403, incorporating a three-bus architecture, combines the standard functions of four 2903s and a 2902. Both parts have additional control features aimed at enhancing the performance of traditional bit-slice microprocessor designs.

Conservation of Microcode

IDT has minimized bit-slice redesign cost in the CMOS-to-bipolar transition through "conservation of microcode". This is achieved by taking full advantage of CMOS integration capabilities while utilizing pre-existent 2900 family instruction sets.

The IDT49C410 sequencer is capable of executing old microcode with no alterations. The IDT49C402 and IDT49C403 ALUs can resolve compatibility issues at several levels. The simplest solution involves connecting only the instruction lines which correspond to the 2901 or the 2903/203, respectively, and tying the remaining inputs to their respective default levels. This permits the design to execute previously assembled microcode.

In some design instances, it may be advantageous to utilize some of the new features of the IDT ALUs—deeper register files or new data paths, for example. This involves changing microcode to control the additional instruction lines and can be achieved by modifying the assembler and reassembling the old microcode.

The design of new high-performance products may require writing new, more robust microcode. This should come as no surprise when considering the architectural complexity of modern state-of-the-art designs. A good example is the next generation of 32-bit processors capable of working on bit fields.

32-Bit Microprocessor Slice

Perhaps the best known architecture in the 32-bit microprocessor slice arena is the 29300 family of devices, illustrated in Figure 4. It is a non-cascadable architecture which involves multiple chips. This family contains an ALU and a RAM register, but multiple RAM register devices must be used to build a 32-bit microprocessor slice. This approach is most likely due to the relatively high power consumption inherent to bipolar technology. It is interesting to note that there are three tightly coupled buses (DA, DB and Y) with the ALU and, since the design uses multiple chips, we see a four-port RAM and a three-port ALU.

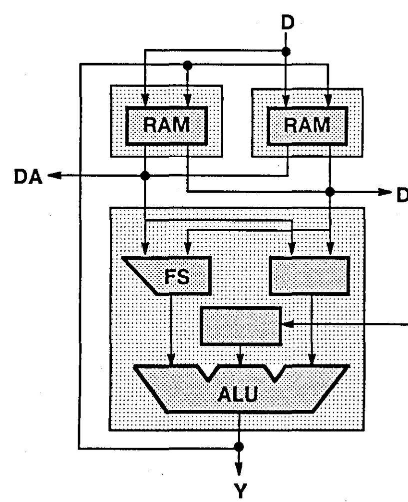


Figure 4. 29300 ALU & RAM Family Architecture
(2 x 16-Bit RAMs Plus ALU)

14

The IDT49C404 Enhances 32-Bit Architecture

The IDT49C404 microprocessor architecture exploits advanced CMOS technology to implement maximum functionality on a single chip. Figure 5 is a simplified block diagram of this slice. The IDT49C404 features a powerful seven-port 64-word-by-32-bit register file containing four output ports and three input ports under the control of four 6-bit address fields. The lower half of the block diagram shows the FS/ALU/ML portion of the IDT49C404 for manipulating 32-bit data. Figure 5 also shows a 32-bit Funnel Shifter which is capable of driving the multi-function 32-bit ALU whose output can be merged with another operand under the control of a merge mask. This is called Merge Logic. In this case, the ALU can perform operations on bit fields in 32-bit words. Applications are far-reaching and include graphics, communications, field searching, packed data operations, etc.

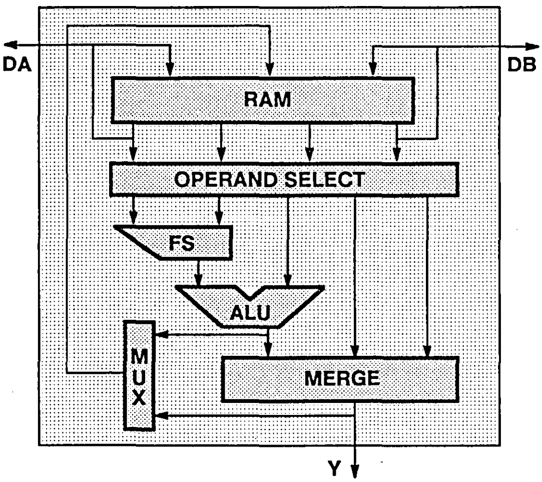


**Figure 5. The IDT49C404A
32-Bit Cascadable RAM and ALU Slice**

Detailed Description of the IDT49C404

The IDT49C404 is shown in more detail in Figure 6. This device is an expandable microprogrammable 32-bit microprocessor slice fabricated using advanced high-speed, low-power CMOS technology. This monolithic three-port (DA, DB and Y) slice contains a seven-port 64-word-by-32-bit RAM, 32-bit cascadable Funnel Shifter, 32-bit wide ALU, 32-bit wide Merge Logic block and a 32-bit mask generator. The IDT49C404 is capable of 32-bit counting for matrix operations as well as byte, word and double-word operations. This architecture and its instruction set are optimized for use in microprogrammable microprocessors, high-speed communications, graphics and disk controllers and digital signal processing algorithms. It also provides advanced internal diagnostics capabilities for detecting and locating hardware system failures. The versatility of these capabilities allows test and error detection during engineering development, in the manufacturing cycle or at the customer facility after delivery of the part.

The 64-word-by-32-bit working RAM has seven ports: three dedicated input ports (A-IN, B-IN and T-IN) and four dedicated output ports (A-OUT, B-OUT, T-OUT and Q-OUT). Each port output is latched. Any four RAM locations can be accessed at the address ports by using the A, B, T and Q address fields. Data can be read simultaneously from all four ports and each will contain identical data when the same address is applied to all of the four address inputs. As in all other bit-slice microprocessor devices, the internal latches are transparent at the output ports during a high clock signal. Data is held in the latches when the clock signal is low. As Figure 6 indicates, each data input path has a multiplexer which selects data from either the ALU/Y bus, the DA/DB bus or, in the case of the T input, the internal counter.

The Funnel Shifter is a powerful 32-bit shift unit which operates on two 32-bit inputs and generates a 32-bit output. It is capable of implementing all basic 32-bit barrel shift functions including shift up, shift down, rotate up and rotate down in any number of positions. Sixty-four-bit operations are performed by cascading devices. This high-speed shifting is particularly useful in operations such as mantissa normalization for floating-point arithmetic or in schemes which involve frequent packing and unpacking of data. The Funnel Shifter can also be used to extract 32-bit output from a sliding window applied to 64-bit input. Control can be supplied from a number of sources and can be either a 32-bit word or an encoded 7-bit start position and 7-bit shift select function. A positive start position moves the sliding window towards the least significant bit. Conversely, a negative start position moves the window towards the most significant bit. In addition, the Funnel Shifter can perform various types of sign extension and 0, 1 or M-link fills as required by the user.

The eight-function ALU has three arithmetic, four logic and one special opcode function. Arithmetic functions are R + S, R - S and S - R. The logic functions are OR, AND, exclusive-OR and exclusive-NOR. The eighth function places the IDT49C404 in a special opcode mode. These special instructions might include unsigned and two's complement conversion. The device is capable of performing two's complement multiply or divide on either 32-bit or 64-bit operands.

A 32-bit Merge Logic block is under the control of the 32-bit mask generator. Normally, the merge operation involves selecting bits from either the V or W operand and presenting a final 32-bit word to the Y bus (see Figure 6). The 32-bit mask is generated by the mask generator which is controlled by a 2-bit mask select field. Mask selection may occur in several different fashions in conjunction with the various RAM outputs and the start position and width input fields. The W operand can be selected from a number of different sources including all ones and zeros. The Merge Logic block also features a priority encoder conceptually similar to the 29116. It is valuable in floating-point operations, as well as various types of polled interrupt systems.

Diagnostic Capability

The IDT49C404 employs a diagnostic scheme involving data entry and extraction through serial input and output pins. This approach allows diagnostic evaluation at any stage of the development, manufacture and utilization cycle. In general, access to test debug points has become more and more difficult because board level packing densities have increased dramatically. For this reason, customers will find serial diagnostics to be of significant benefit. This is especially true in double-sided surface mount technologies.

IDT's method of employing serial diagnostics maintains maximum flexibility while using a minimum number of pins. The data is passed in and out on single pins, while transfer is controlled by a diagnostics clock and a command/data mode input. Thus, only four pins are required. Systems level diagnostics involves the serial connection of output and input of adjacent devices. In effect, this cascades devices into one long serial shift register. The diagnostics clock and command/data mode lines for the devices are connected in parallel. This approach minimizes the number of device connections required for diagnostics.

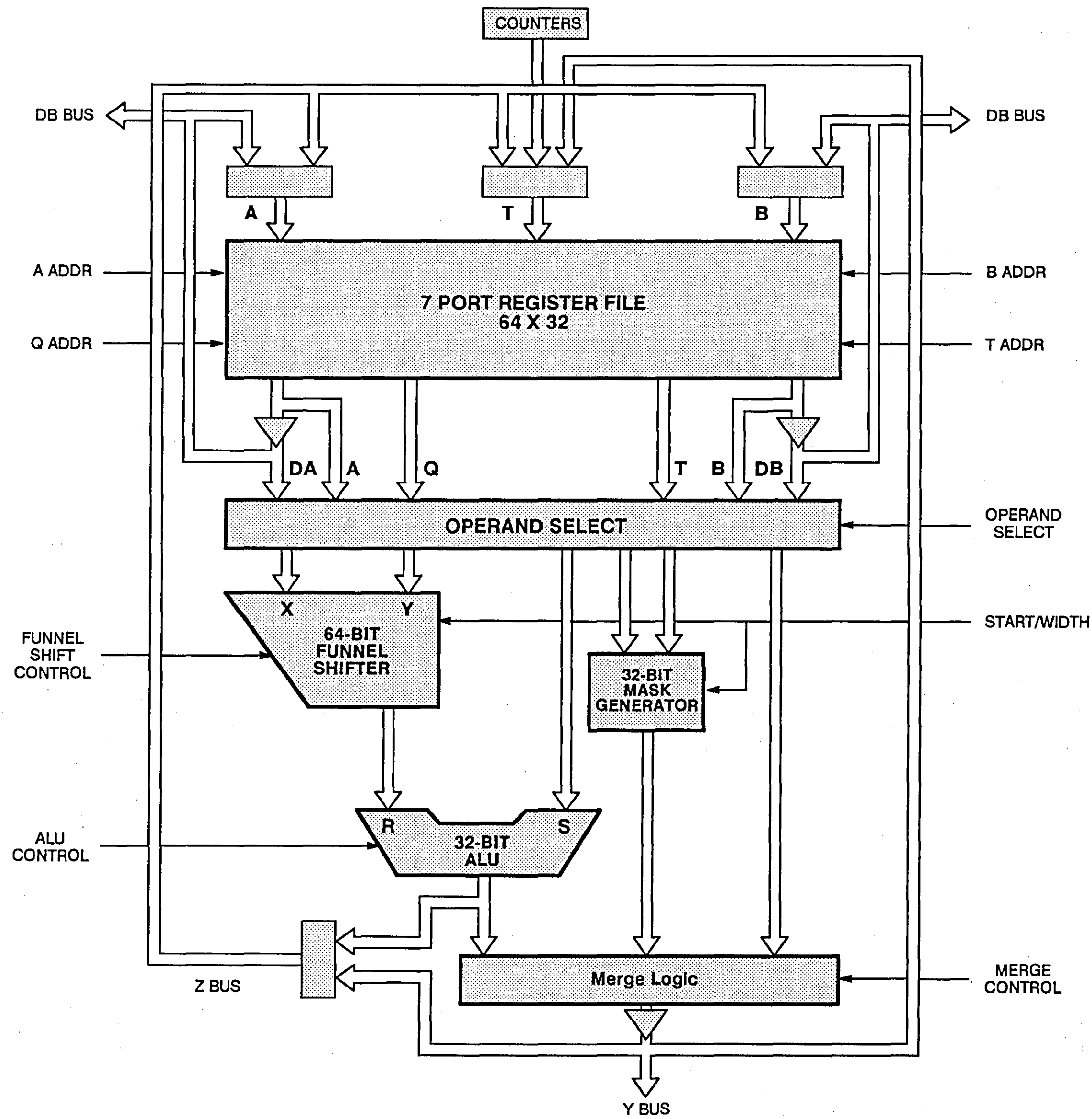


Figure 6. Detailed Block Diagram of the IDT49C404

14

Serial diagnostics capability allows data to be read from, or inserted to, the seven-port register file. Additionally, various input pins and output pins can be observed and some break-point capability is implemented. Figure 7 lists all of the instruction fields and their associated opcodes. The control lines of each functional block are brought out separately to achieve an orthogonal instruction set. This allows the highest degree of performance and flexibility. The unencoded control lines are especially useful to designers of RISC-type architectures.

49C404 Instruction Fields

44 43 42 41 40 39 38 37 36 35 34 30 29 24 23 17 16 14 13 12 11 9 8 7 6 5 4 3 2 0

OEY	OEA OEB	M SEL N SEL	S SEL	MASK SRC	ML	FUNNEL SHIFTER	WIDTH	START	T SEL	ALU	U SEL	MRG	Z SEL Z D	A/B SEL	$\overline{WE}$, A/T/B

16-BIT IMMEDIATE FIELD

7-BIT IMMEDIATE FIELD

SPECIAL INSTRUCTION FIELD

⊠ N.C. ON 32 BIT SYSTEM

49C404 Instruction Fields Opcodes

Mask Src	
Code	**Source**
0 0	Start and Width from Instruction
0 1	T & Q supply Start and Width
1 0	T as a 32-Bit Mask
1 1	Q as a 32-Bit Mask

X Source Selection		
$\overline{OEA}$	X Src	X Source
0	0	RAM A
0	1	RAM T
1	0	RAM A
1	1	DA

Merge Control	
MRG	**Function**
0 0	Pass F
0 1	Pass V
1 0	Merge F/V
1 1	Merge V/F

Y Source Selection		
$\overline{OEB}$	Y Src	Y Source
0	0	RAM B
0	1	RAM Q
1	0	RAM B
1	1	DB

S Source Selection	
Code	**Source**
0 0 0	DA
0 0 1	RAM A
0 1 0	RAM Q
0 1 1	RAM T
1 0 0	RAM B
1 0 1	DB
1 1 0	Y
1 1 1	MASK

Funnel Shift Operations		
Code	**Function**	**Operands**
00 000	Shift X and fill with O	O, X
00 001	Shift Y and fill with O	O, Y
00 010	Shift X and fill with M	M, X
00 011	Shift Y and fill with M	M, Y
00 100	Extract field from	Y, X
00 101	Extract field from	X, Y
00 110	Shift X arithmetic and fill O	Sign, X, O
00 111	Shift Y arithmetic and fill O	Sign, Y, O
01 000	Shift X arithmetic and fill M	Sign, X, M
01 001	Shift Y arithmetic and fill M	Sign, Y, M
01 010	Barrel shift X	X
01 011	Barrel shift Y	Y
01 100	Pass X	X
01 101	Pass Y	Y
01 110	Pass all O's	O
01 111	Pass all 1's	1
10 000	Shift X and fill with O, Bypass ALU	O, X
10 001	Shift Y and fill with O, Bypass ALU	O, Y
10 010	Shift X and fill with M, Bypass ALU	M, X
10 011	Shift Y and fill with M, Bypass ALU	M, Y
10 100	Extract field from Y & X, Bypass ALU	Y, X
10 101	Extract field from X & Y, Bypass ALU	X, Y
10 110	Shift X arith. and fill O, Bypass ALU	Sign, X, O
10 111	Shift Y arith. and fill O, Bypass ALU	Sign, Y, O
11 000	Shift X arith. and fill M, Bypass ALU	Sign, X M
11 001	Shift Y arith. and fill M, Bypass ALU	Sign, Y, M
11 010	Barrel shift X, Bypass ALU	X
11 011	Barrel shift Y, Bypass ALU	Y
11 100	Pass 1's Complement of X	X
11 101	Pass 1's Complement of Y	Y
11 110	Pass X and merge Cin from Bit0 to SP	X
11 111	Pass X and merge Cin from Bit0 to SP	Y

V Source Selection	
VSEL	**Selection**
0 00	DA
0 01	A
0 1 0	Q
0 1 1	T
1 00	B
1 01	DB
1 10	0's
1 11	1's

ALU	
Code	**Function**
0 0 0	R + S
0 0 1	S - R
0 1 0	R - S
0 1 1	R or S
1 0 0	R and S
1 0 1	Special Instruction
1 1 0	R exor S
1 1 1	R exnor S

Z BUS Control			
Code	**RAM DEST**		**Zero Test Src**
	A	**B**	
0 0 0	DA	F	F
0 0 1	DA	Y	F
0 1 0	F	DB	F
0 1 1	Y	DB	F
1 0 0	DA	F	Y
1 0 1	DA	Y	Y
1 1 0	F	DB	Y
1 1 1	Y	DB	Y

T Source	
Code	**Source**
0 0	Z BUS
0 1	Y BUS
1 0	T + C1
1 1	T + C2

Figure 7. The IDT49C404 Instruction Fields and Opcodes

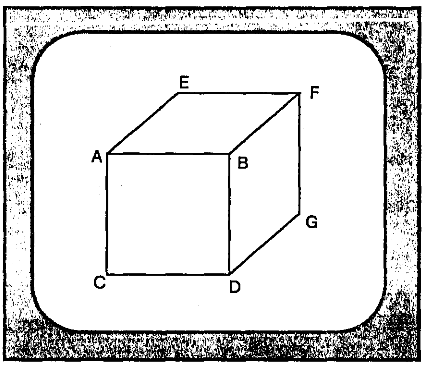
APPLICATIONS:

Floating-Point Math Accelerator

Modern work stations often use a processor such as the 68020 or 80386 as the main CPU. In many cases, the processing capability of the CPU is extended with the use of a floating-point math accelerator. If the floating-point processor is isolated from the main CPU through the use of a dual-port RAM, higher overall system per- formance can be achieved because the accelerator can process in parallel to the main CPU.

Consider a graphics application. Conceivably, the dual-port RAM could contain a link list of data elements containing three-dimensional point values and transformation instructions which are composed of 4x4 matrices. The floating-point processor could be capable of traversing the link list and multiplying each point with the transformation matrices. This approach could be used to rotate three-dimensional objects, transform them into two-dimensional surfaces and perform clipping algorithms for final display on a graphics terminal. Figure 8 compares a possible display representation and how it might be stored in memory internally.

THE USER'S VIEW



THE PROCESSOR'S VIEW

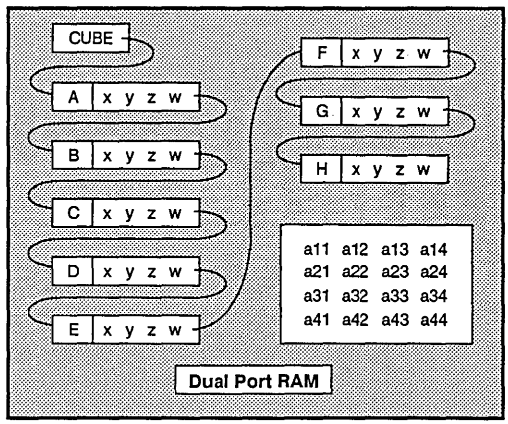


Figure 8. Different Views of the Same Cube

14

The floating-point math accelerator consists of a dual-port RAM, a controller and floating-point ALU and a multiplier. A block of dual-port RAMs serves as the interface between the global system bus and the local system bus used by the floating-point processor. The control section generates sequences of instructions for a floating-point ALU, as well as address generator indexing into the dual-port. The performance of the accelerator depends on the speed at which the controller can generate instructions and on the bandwidth of the ALU.

The MICROSLICE family contains a number of well-suited control devices. As shown in Figure 9, the control section of a floating-point accelerator can be composed on an IDT49C410 that generates addresses to the writable control store of an IDT71681 which, in turn, produces an instruction to be held in a pipeline register. The contents of the pipeline register are the current instructions being executed. Control lines can be fanned out to instruction lines and control inputs of every device in the accelerator subsystem.

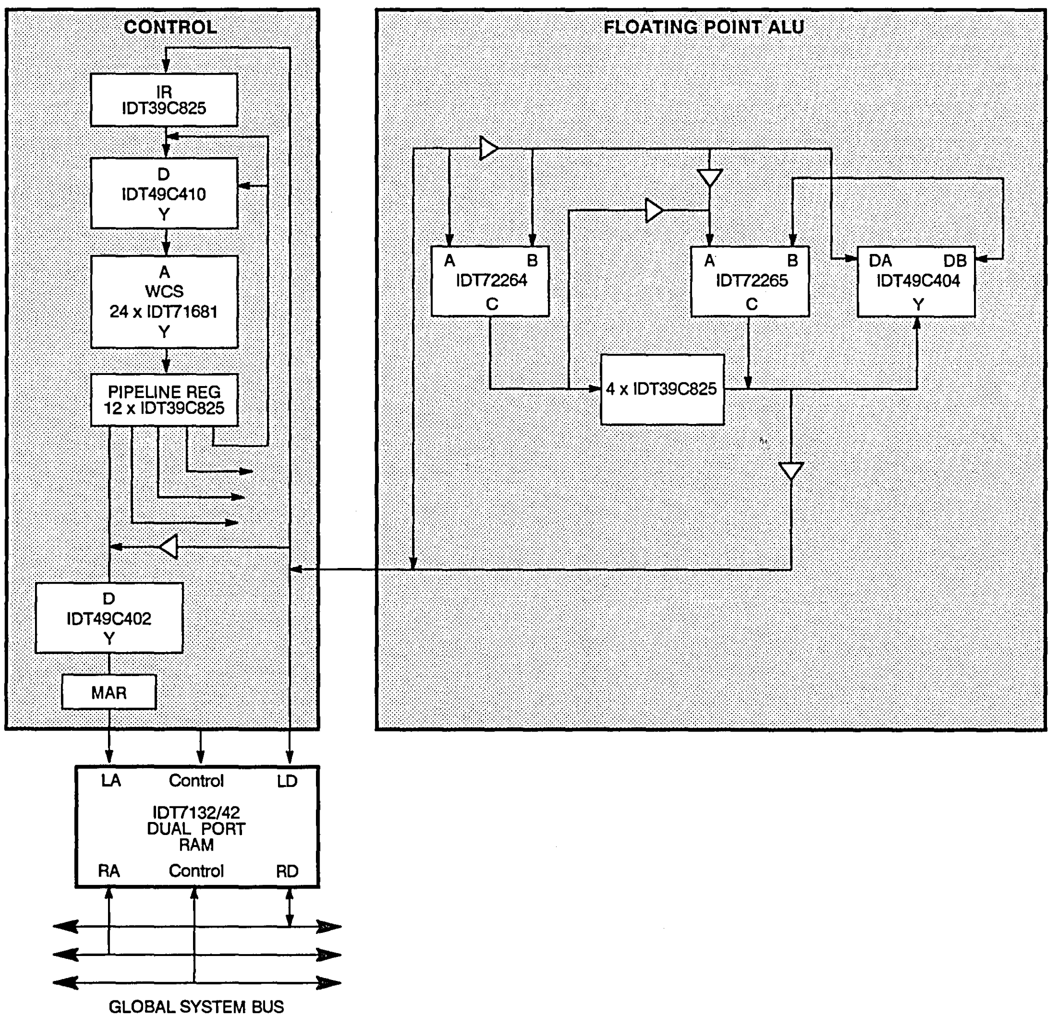


Figure 9. Floating-Point Math Accelerator Using the MICROSLICE Family

Most designers think of the IDT49C402 (and others in its class) only as an ALU with register files for data paths. However, it can be used for a larger variety of tasks. In the accelerator example, it is used as an address generator. Data for a 4x4 matrix can be stored in the dual-port memory as a sequential list of 16 values. Any element can be located by adding the address pointer to the start of the matrix, the row offset and the column offset. To multiply a matrix by a vector, a column of matrix elements is individually multiplied by the corresponding vector values and the four products are added together. One way to efficiently generate addresses with the IDT49C402 is to store the matrix address pointer and vector in the register file. To begin, the address pointer of the matrix can be added to a constant corresponding to the column to be operated on. This operation can be completed in a single cycle by bringing the constant from the pipeline register through the D bus, addressing the pointer with the A address and storing the result in a location specified by the B address. In the same cycle, the new address could be output from the ALU through the Y port and placed in the MAR register. In this way, the MAR register would supply the dual-port RAM address on the next cycle, forming a pipeline mode of operation. On the next three cycles, the new address in the register file could be incremented and the respective calculated addresses passed to the MAR. Consequently, it would require only four cycles to generate four addresses that correspond to four values in the matrix column. In addition, this entire process can be performed while the computation unit attends to other tasks. With proper design, addresses can be fed into the dual-port RAM and values can be read into the computation unit on every clock cycle. With the IDT49C402A, the minimum time from register file address to the Y output is only 37ns. This is one of the fastest ways to generate a complex 16-bit address.

The IDT49C402 can also be used to keep track of linked lists of complex data structures. The register file is capable of retaining pointers of various lists, as well as intermediate pointers. The accelerator described previously requires a pointer to the head of a list of XYZW values, an intermediate pointer to the current XYZW value and a pointer to the transformation matrix.

The computation portion of the accelerator is composed of floating-point devices and local storage elements. The most efficient way to multiply a series of vectors by a transformation matrix is to begin by fetching the matrix from the dual-port RAM into local memory connected to the floating-point chips. The register file of the IDT49C404 can be used to hold the matrix variables, as well as intermediate results. This poses no problem since the IDT49C404 has 64 registers—enough room to store the 4x4 matrix and any temporary variables. The 32-bit ALU portion of the chip can then be used to perform fixed-point arithmetic and logic functions.

The IDT49C404's three-bus architecture allows both output ports of the register file to come off-chip and drive inputs to the floating-point devices. Thus, two operands can come from the IDT49C404 and one from the dual-port RAM addressed by the IDT49C402 on each clock cycle. The Y bus can be used to put the results of the floating-point multiplier or ALU back into the register file.

Once the transformation matrix is stored in the IDT49C404 registers, consecutive XYZW point values can be brought in from the dual-port RAM. Consequently, values from the XYZW vector and transformation matrix can be delivered to the IDT721265 multiplier on every cycle.

Graphics Accelerator Example

Figure 10 shows the block diagram for a graphics accelerator. Once again, this scheme uses a dual-port RAM as the communication device between the main processor and the accelerator. The accelerator is composed of two blocks: a control unit containing the IDT49C410 sequencer and an image computation unit which utilizes the IDT49C404 as the main image computing processor. Both blocks use the IDT49C402 to generate addresses.

In the control unit, the IDT49C402 can be used to generate link list addresses, as well as indexes into complex data structures. The IDT49C402 is used in the computation unit to generate addresses into the video frame buffer. The video frame addresses might be used for bit block moves or for drawing complex line algorithms.

Within the computation unit, the IDT49C404 is used for performing mask and merge operations with data in the frame buffer. The Funnel Shifter rotates and aligns data and the ALU merge unit takes new data and merges it into old data in the frame buffer. The three-bus structure of the IDT49C404 is very useful. The DA bus may be used to bring icon and bit pattern data in from the dual-port memory on the system bus. The DB bus is used to bring in data from the video frame buffer. These two buses can be merged together using the Funnel Shifter, ALU and Merge Logic block to compute output which is the Y bus. The Y bus can then be used to write the result back into the frame buffer. Since address computation and data manipulation are done on separate chips, read modify writes can be performed very easily by holding the address steady. Data is read from the frame buffer and then the buffer write control line is brought low as data is delivered through the IDT49C404 and back into the frame buffer.

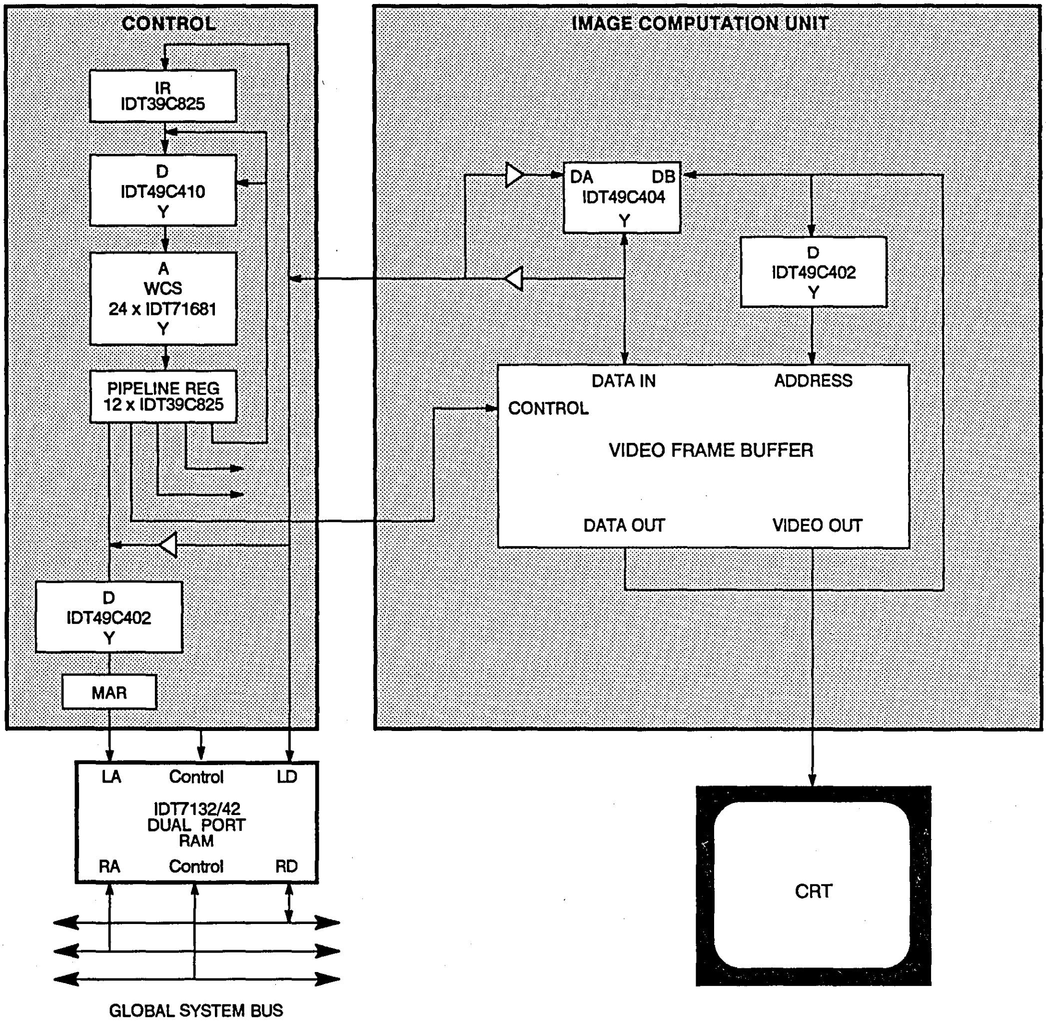


Figure 10. Graphics Accelerator Using the MICROSLICE Family

The previous examples of the IDT49C404 are two of many possible applications. This device is very well-suited for any operation which requires 1-bit to 32-bit data manipulation on any type of boundary. Other examples include business automation projects such as data base manipulation, graphics and special purpose CPUs. Industrial automation efforts like robotics and artificial intelligence could benefit from the IDT49C404. Telecommunications is another fast-paced application segment where bit field manipulation is of paramount importance, especially in video control strategies. Peripheral controls for high-speed communications and disk drives is yet another area where high-performance bit field processing is very important.

SUMMARY

Integrated Device Technology's 32-bit IDT49C404 cascadable bit-slice microprocessor is the most powerful introduced to date. It offers technical features which maximize system throughput and performance in a tremendously wide variety of applications. The 64-word-by-32-bit register file represents 2K bits of total multi-port memory. The Funnel Shift/ALU/Merge arrangement provides maximum data manipulation in a single clock cycle. Together with other IDT49C000 devices, the MICROSLICE family offers a complete set of building blocks for high-performance system solutions.

Integrated Device Technology, Inc.

USING THE IDT721264/65 FLOATING-POINT CHIP SET

APPLICATION NOTE AN-12

By DANH LE NGOC

INTRODUCTION

This article discusses floating-point in general terms: IEEE floating-point format, the pipelined architecture of IDT721264/65, how to perform division-algorithms and several DSP applications such as FIR, FFT and graphics accelerators.

Floating-Point Versus Fixed-Point

There are three major types of number representations: decimal, fixed-point and floating-point. The discussion here concentrates on fixed-point and floating-point. In the fixed-point data notation, data is represented with a radix point which remains in a fixed position within the number. The fixed-point data can be subdivided into two categories: integer number and fractional number. An integer number represented in the fixed-point notation has an implied radix point to the right of the number. The radix point is to the left of the number in the fixed fractional data representation. Figure 1 illustrates the two different fixed-point representations.

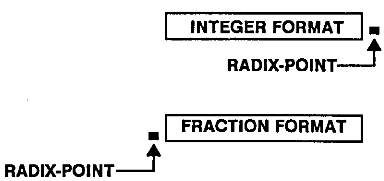


Figure 1.

Users of fixed-point processors have to maintain the correct position of the radix point at all times, resulting in scaling problems such as shifting the number in one direction or another to avoid the overflow or loss of precision. For example, a 32-bit fixed-point number can represent all integers roughly between $-2x10^9$ and $+2x10^9$ -1. An overflow or underflow occurs when a number is larger or smaller than this range. A fractional number like 4.25 can be represented as a integer number by scaling down by 0.25. The scaling process is also referred to as rounding. The scaling or rounding is normally fixed in the arithmetic operations. Therefore, the number of data bits of each fixed-point processor determines the magnitude (range of values) and precision of values (how accurately a number can be represented). These restrictions can cause some errors in the digital signal processing computations which result in a noise-like source in the digital systems.

Floating-point processors handle scaling automatically and expand the range of values represented by fixed-point processors. For example, a 32-bit floating-point number in the IEEE format can represent all numbers from roughly $1.2x10^{-38}$ to $1.7x10^{38}$. A floating-point number consists of two parts: a fraction and an exponent. The fractional and exponent parts of a floating-point number can also be referred to as the mantissa and the characteristic, respectively. The IDT721264/65 chip set supports the ANSI/IEEE standard 754 version 1985 floating-point notation which consists of two formats: single precision (32-bit) and double precision (64-bit). These two formats are described below:

— IEEE standard single precision:

31	30 ... 23	22 ... 0
SIGN	EXPONENT	FRACTION

In the single precision format, the floating-point number is divided into three fields: the sign-bit, an 8-bit exponent and a 23-bit fraction. The floating point value is determined by the following table:

E	F	Value	Name	Mnemonic
255	Not All Zero	—	Not A Number	NaN
255	All Zeros	$(-1)^S$ (Infinity)	Infinity	INF
1-254	Any	$(-1)^S (1.F)2^{E-127}$	Normalized Number	NOR
0	Not All Zeros	$(-1)^S (0.F)2^{-126}$	Denormalized Number	DNRM
0	Zero	$(-1)^S$ 0.0	Zero	ZERO

— Approximate Maximum positive number: $2^{128} = 1.7 \times 10^{38}$

— Approximate Minimum positive normalized number: $2^{-126} = 1.2 \times 10^{-38}$

— Precision: $2^{-23} = 10^{-7}$ (7 decimal places)

NaN

As the table indicates, the exponent values E=0 and E= 255 are reserved to specify the special numbers in the IEEE format. When the exponent E equals 255 and the fractional part F is not zero, the number is called "Not a Number" (NaN). NaN does not represent a numeric value, but it represents a symbol in the IEEE format. This special data format is usually used as a flag for data flow control, for uninitialized variables or to indicate an invalid operation such as 0 x INFINITY.

Infinity and Zero

When exponent E=255 and fraction F=0, this number defines INFINITY. When exponent E=0 and fraction F=0, the value is zero in the IEEE format.

Normalized Number and Denormalized Number

A floating-point number is called normalized when the hidden-bit is one. When the hidden-bit of a floating-point number is zero and the fractional part F is not zero, this number is called a denormalized number.

14

Hidden Bit and Biased Exponent

There are two additional significant items in the single precision floating-point format. The assumed "1" preceding the fraction is called the hidden bit which increases the precision of the fraction from 23 bits to 24 bits. The biased exponent representation, e=E-127, makes all of the exponents larger than zero, simplifying the hardware logic implementation for the floating-point numbers. This is illustrated in the two examples below:

Printed in the U.S.A. 6/87

Examples:

0 10110111.01000000000000000000000

sign = + E = 183 F = 1.25

1 10110111.10000000000000000000000

sign = - E = 183 F = 1.50

For applications requiring larger precision, the double precision IEEE format is preferred:

– IEEE standard double precision:

63	62 — 52	51 — 0
SIGN	EXPONENT	FRACTION

The range of values is defined by the following table:

E	F	Value	Name	Mnemonic
2047	Not All Zero	–	Not A Number	NaN
2047	All Zeros	$(-1)^S$ (Infinity)	Infinity	INF
1-2046	Any	$(-1)^S (1.F)2^{E-1023}$	Normalized Number	NOR
0	Not All Zeros	$(-1)^S (0.F)2^{-1022}$	Denormalized Number	DNRM
0	Zero	$(-1)^S$ 0.0	Zero	ZERO

The key differences between the single precision and double precision are the number of bits for the exponent and the fraction. In the double precision, the exponent is eleven bits and the fraction is fifty-two bits, which provides a larger dynamic range and greater accuracy.

– Approximate maximum positive number: $2^{1024} = 9 \times 10^{307}$
– Approximate minimum positive normalized number: $2^{-1022} = 2.2 \times 10^{-308}$
– Precision: $2^{-52} = 10^{-15}$ (15 decimal places)

Architectural Overview of the IDT Floating-Point Chip Set

The floating-point hardware implementation is inherently more complex than the fixed-point processor. Generally, the floating-point arithmetic processor consists of four basic elements: fixed-point logic to perform the fixed-point operation on the fraction, fixed-point logic to perform calculation on the exponent part of the floating-point format, logic to perform the rounding and format-adjustment to the floating-point formats and logic to detect and handle the exceptions. Figures 2 and 3 illustrate the data-flows for the multiplication and addition of two floating-point numbers, respectively.

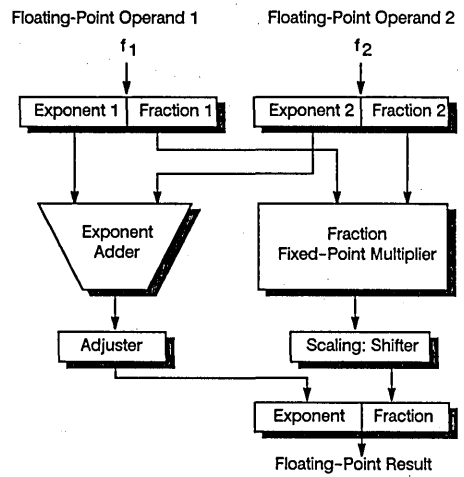


Figure 2. Floating-Point Multiplication Data Flow

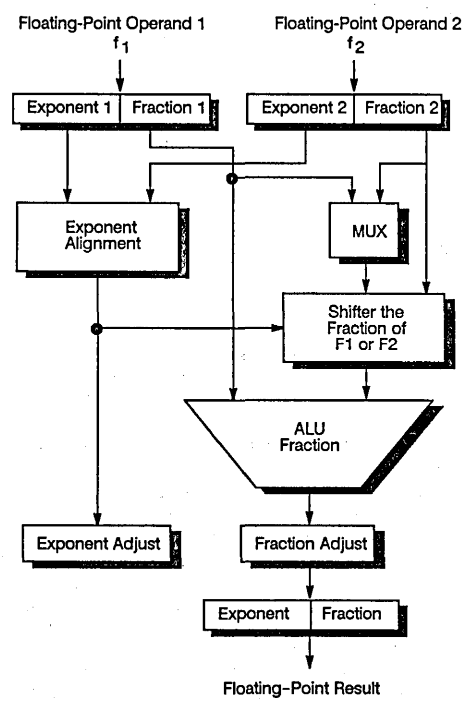


Figure 3. Floating-Point Addition Data Flow

As the data flow in Figures 2 and 3 demonstrates, performing a floating-point multiplication or addition will take a longer system clock-cycle than fixed-point operations. To reduce the long clock cycle, the pipelined approach is implemented in the IDT floating-point chip set.

The IDT721264/65 chip set consists of two devices: a floating-point multiplier and an ALU (see Figures 4 and 6).

The floating-point multiplier and ALU are architectured as three-bus devices. There are two dedicated 32-bit input ports (X and Y) to load the two operands, and one dedicated output port (Z) to unload the result of floating-point operations.

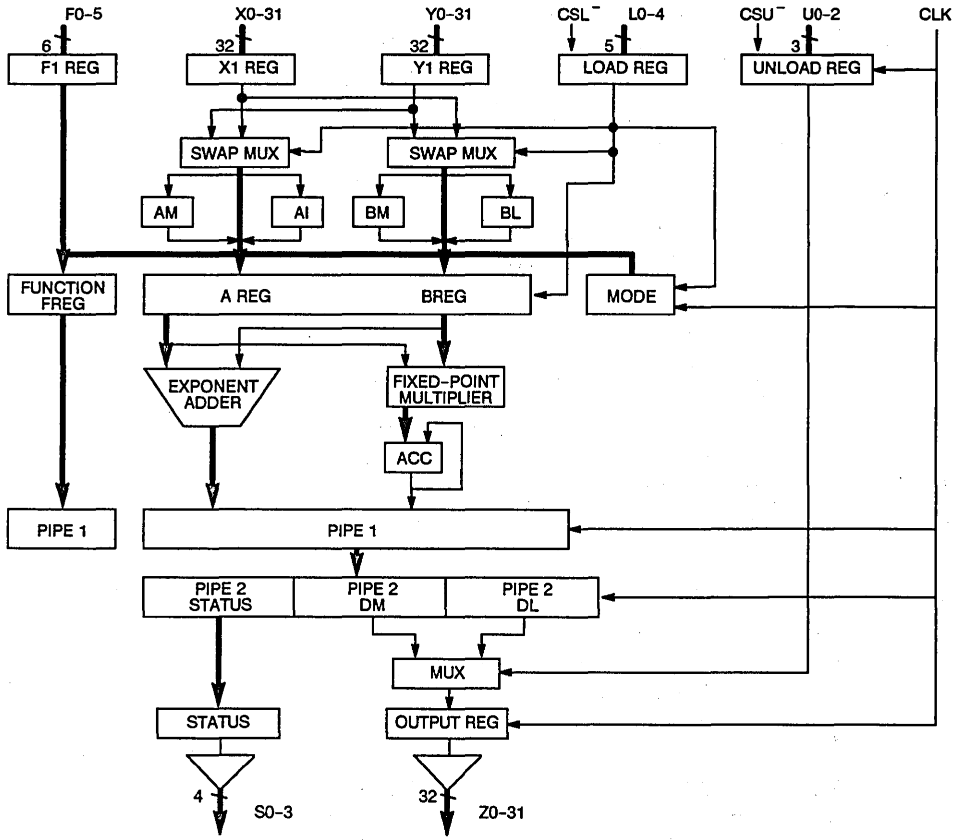


Figure 4. IDT721264 Floating-Point Multiplier

Five bits (L0-4) are used to specify the load operations. The result can be read on the Z bus under control of the 3-bit U0-2 in parallel with the 4-bit status S0-3. The 6-bit function controls F0-5 are used to select the opcodes for the floating-point multiplier and ALU. They are also used to load data into the mode register which specifies the different operating modes: flowthrough, pipelined, IEEE standard mode, fast mode and all rounding modes. The IDT721264 and IDT721265 provide a very flexible input/output structure which can be easily interfaced with a 16-bit, 32-bit or 64-bit bus. The two input buses X and Y can be configured as two independent 16-bit or 32-bit buses or as a single 64-bit bus under control of two mode-bits: MODE15, MODE14. In the 16-bit mode configuration, when MODE15 is high, two consecutive clocks are required to load a 32-bit number into the X1 and Y1 registers. In the single precision mode, the 32-bit operands must be loaded into the most significant bits of the AREG and BREG because the least significant 32 bits of the AREG and BREG are filled in with logic zeros by the hardware. Data on the X and Y buses are loaded into the X1 and Y1 registers on the low-to-high transition of the clock. From there the data is moved into the AM, AL, BM, BL, AREG and BREG registers on the low-to-high transition of the clock signal. When L0 is high, the two operands stored in the registers AM, AL, BM, BL, X1 and Y1, as well as the function-code in F1, are transferred to the first pipelined stage of the floating-point multiplier or ALU. At the same time, the pipe advance timer and accumulate timer are also reset to indicate the beginning of a new operation.

The internal architecture of the floating-point multiplier (see Figure 4) consists of five basic elements: a front end circuit to detect exceptions, a synchronous multiplier array, a circuit for handling the exponents, a shifter to normalize the result of the fixed-point multiplication and IEEE rounding circuitry. The five basic elements are partitioned into two pipelining stages. Under control of two mode bits MODE5/MODE4, the first pipe/second pipe of the floating-point multiplier can be made transparent. Making pipeline registers transparent reduces the worst-case latency of operation, but it also reduces the maximum throughput. This mode is also called the flowthrough mode.

14

A 56-bit-by-28-bit multiplier array is used to perform the fixed-point multiplication. One pass is required to perform the single precision multiplication. Two passes are required to perform the double precision multiplication. Figure 5 illustrates the internal architecture of the fixed-point multiplier array:

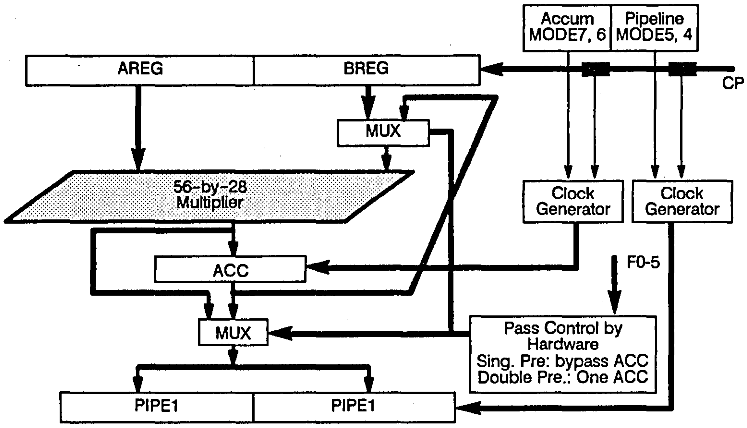


Figure 5. Multiplier Array of IDT721264

The floating-point ALU also consists of five basic elements: a front end circuit to detect the exceptions, a shifter to align the two operands, a 57-bit adder, a shifter to renormalize the results and a circuit to produce the IEEE format. These five basic elements are partitioned into five pipelined stages. The last four pipeline registers can be made transparent under control of four mode bits: MODE7, MODE6, MODE5 and MODE4. Figure 6 illustrates the simplified block diagram of the IDT721265.

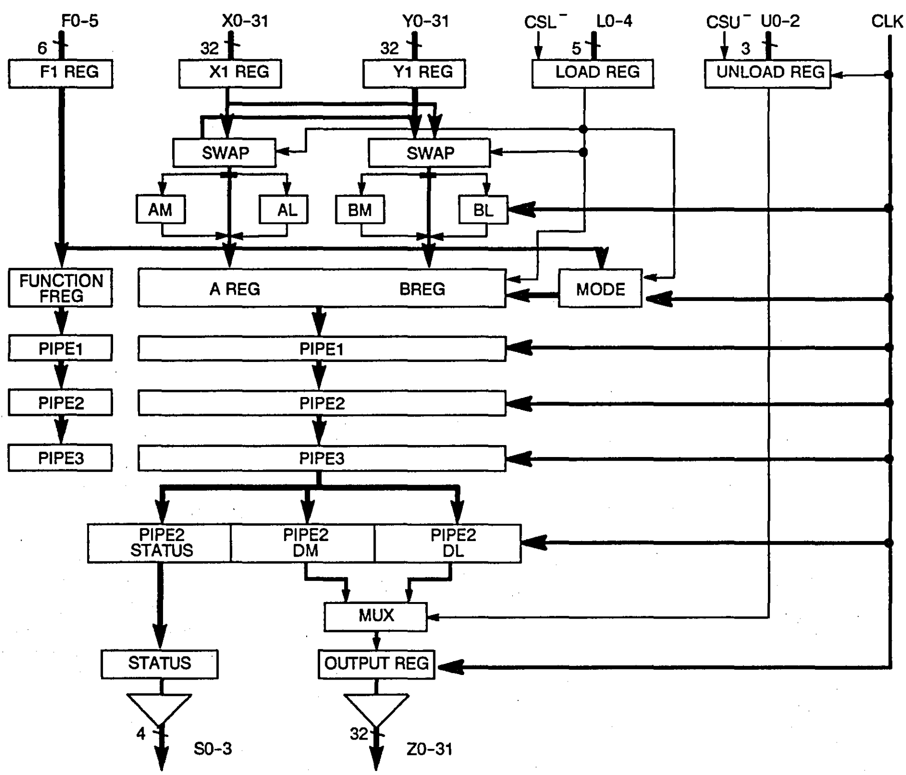


Figure 6. IDT721265 Floating-Point ALU

Flowthrough and Pipelining Modes

The IDT floating-point chips are architectured as pipelining devices which are well suited for pipelined signal processing applications such as FFT, FIR and Matrix multiplications. The IDT721264 floating-point multiplier consists of two pipeline stages which can be made transparent under control of two mode bits (MODE5 and MODE4) as follows:

MODE5	MODE4
Pipe1	STREG & DM, DL
0 -> Transparent	0 -> Transparent
1 -> Register	1 -> Register

In the single precision multiplication, the minimum pipeline clock is twice the system clock. However, the pipeline clock for the double precision multiplication is four times that of the system clock. To optimize the throughput in the pipeline mode, the multiplier also contains two timers: the accumulator advance control and pipeline advance control. For a given system clock, the accumulator timer control is used mainly to select the number of clocks required to perform the 24-bit-by-24-bit or 54-bit-by-54-bit fixed-point multiplication under control of the two mode bits MODE7 and MODE6:

MODE7	MODE6	Accumulate Rate
0	0	Clock/1
0	1	Clock/2
1	0	Clock/3
1	1	Clock/4

Under control of the four mode bits MODE11-8, the pipeline advance timer controls when the pipeline registers are clocked after the start of an operation. If all zeros are loaded into M11-8, the pipeline registers are latched only at the beginning of an operation. When M11-8 are loaded with a non-zero value N, the pipeline registers are clocked at the beginning of every operation and N clock cycles after the beginning of every operation. Both the accumulator advance timer and pipeline advance timer are reset at the beginning of each operation, namely every time the bit L0 is high. The example below illustrates two typical selections for two different system clocks :

Examples:

IDT721264 System Clock	Accumulator MODE7 & 6	Pipeline MODE11-8
Single 40ns	01 -- > 80ns	0010 (N=2) --> 80ns
Single 80ns	00 -- > 80ns	0001 (N=1) --> 80ns
Double 40ns	01 -- > 80ns	0100 (N=4) --> 160ns
Double 80ns	00 -- > 80ns	0010 (N=2) --> 160ns

The table below summarizes the performance of the IDT chip set:

Operation	IDT721264 Multiplier	IDT721265 ALU
Single-Precision Pipelined-Throughput	80ns	80ns
Single-Precision Latency	240ns	360ns
Double-Precision Pipelined-Throughput	160ns	80ns
Double-Precision Latency	360ns	360ns

Figure 7. IDT Floating-Point Chip Set Performance

Figure 8 shows the timing for the pipelined single precision multiplication. To achieve the maximum pipelined throughput in the single precision multiplication, the accumulator advance timer, pipeline advance timer and pipeline configuration control are selected as follows:

Clock	MODE5	MODE4	Accumulator MODE7-6	Pipeline MODE11-8
40ns	1	1	01 -> 80ns	0010 (N=2) -> 80ns

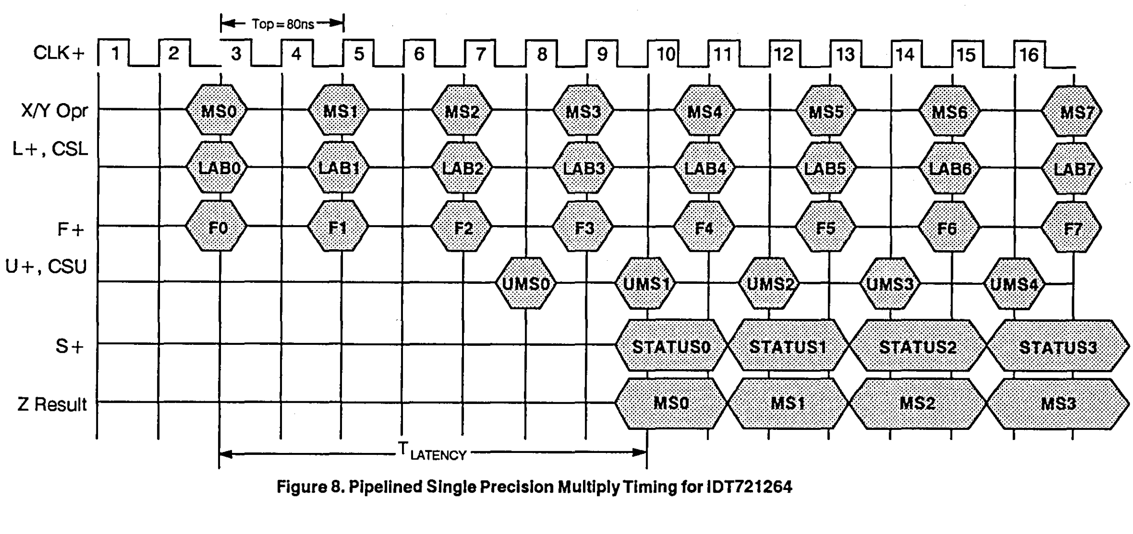


Figure 8. Pipelined Single Precision Multiply Timing for IDT721264

14

On the low-to-high transition of clock #3, the operands as well as the function are loaded into the AR, BR and F registers. In the next clock cycle (#4) the operation is started. It takes two clock cycles to finish the partial product of the 24-bit-by-24-bit multiplication. Then the partial product is loaded into pipe1. On the next two clock cycles (#6 and #7), the final result of the multiplication is generated and pipelined into the last pipe. On the low-to-high transition of clock #8, the unload-opcode can be loaded. The result, as well as status, can be read on clock #10 and remains for two clock cycles (pipeline clock). The $T_{LATENCY}$ specifies the initial total latency of the pipelined mode. After the pipe is full, the result can be read on the Z bus every two system clock cycles.

Figure 9 shows the timing for the pipeline double precision multiplication. In this mode, four clock cycles are required to perform the fixed-point multiplication. Therefore, the accumulator timer is set to clock/2 (two clock cycles) and the pipelined advance control is set to clock/4 which provides two passes required for the accumulations. To maximize the throughput, the DM and DL registers are made transparent, since the last pipe requires only two clock cycles (see table below).

Clock	MODE5	MODE4	Accumulator MODE7-6	Pipeline MODE11-8
40ns	0	0	01 -> 80ns	0100 (N=4) -> 160ns

Similar to pipelined single precision multiplication, the result and status can be read on the Z bus and S0-3 lines every four system clock cycles after the first initial pipeline delay is filled in.

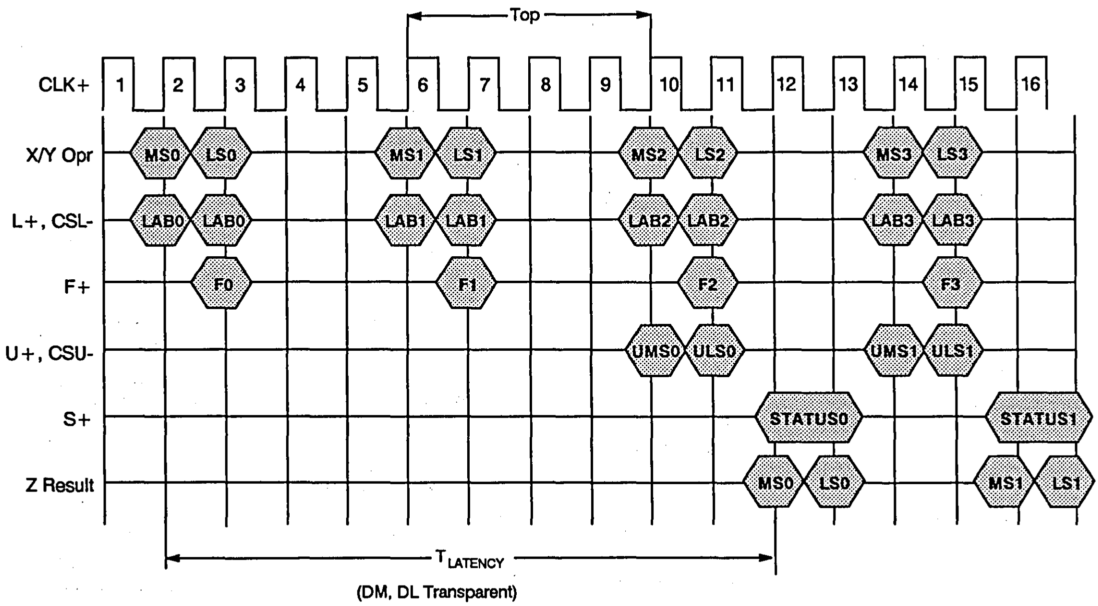


Figure 9. Pipelined Double Precision for IDT721264

Likewise, the floating-point ALU consists of four pipeline stages which can be made transparent under control of the four mode bits: MODE7, MODE6, MODE5 and MODE4 (see Figure 10). The IDT721265 ALU has only the pipeline advance control. The pipeline clock for the ALU operation is twice the system clock for both the single and double precision operations.

MODE7 Pipe1	MODE6 Pipe2	MODE5 Pipe3	MODE4 STREG & DM, DL
0 -> Transparent	0 -> Transparent	0 -> Transparent	0 -> Transparent
1 -> Register	1 -> Register	1 -> Register	1 -> Register

Figure 10. Pipeline Configuration for IDT721265

The IDT721265 ALU has the same throughput for the single and double precision operations. The pipeline clock must be twice the system clock. Therefore the pipeline advance control is set to two and all the pipelined stages are enabled (see Figure 11).

Clock	MODE7	MODE6	MODE5	MODE4	Pipeline MODE11-8
40ns	1	1	1	1	2 -> 80ns

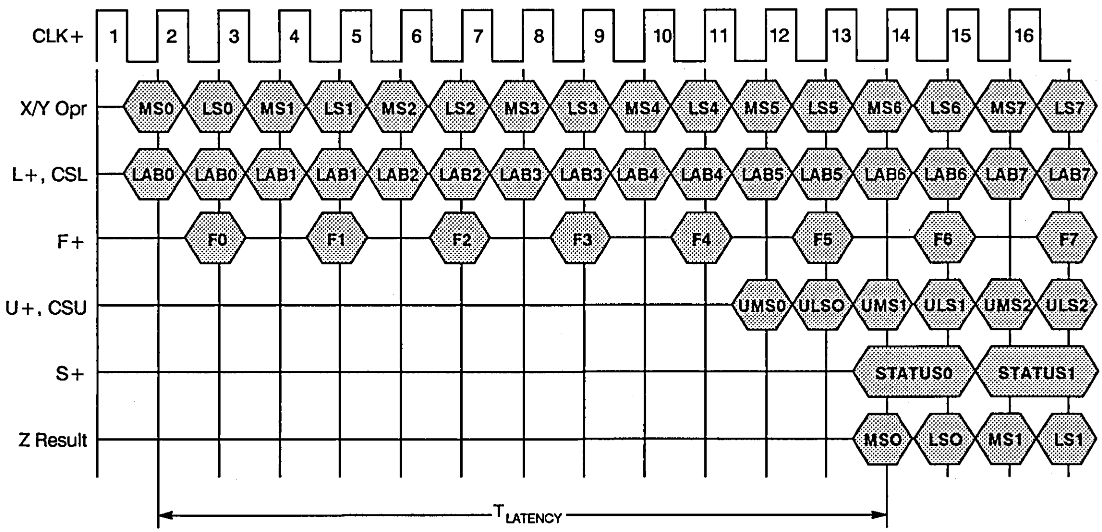


Figure 11. Pipelined Single and Double Precision ALU for IDT721265

For applications requiring a single clock execution time, such as in a general purpose computer, the pipelining stage can be made transparent to reduce the total latency using the four mode bits: MODE4, MODE5, MODE6 and MODE7.

In the flowthrough mode for single precision multiplication (Figure 12), the accumulative control is set to one, pipeline control is set to zero and the pipeline1 and DM, DL registers are made transparent in order to achieve the minimum total latency (see table below).

Clock	MODE5	MODE4	Accumulator MODE7-6	Pipeline MODE11-8
40ns	0	0	01 -> 80ns	0000

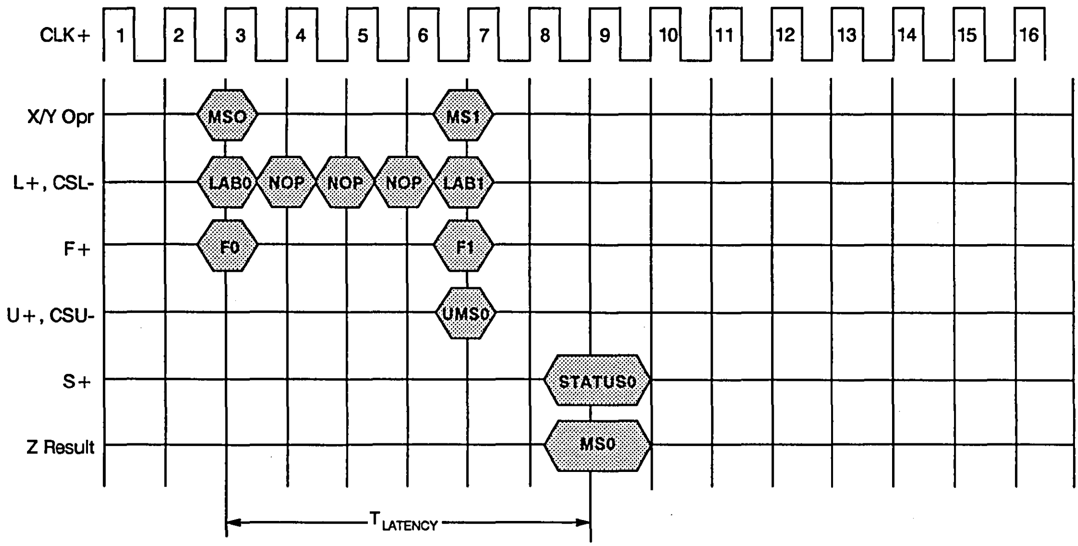


Figure 12. Flowthrough Single Precision Multiply for IDT721264

In the flowthrough mode for the double precision multiplication (Figure 13), the accumulator timer is set to clock/2, because two clock cycles are required to perform the partial product for each pass. To minimize the total latency, the pipeline advance control is set to zero and the DM, DL registers are made transparent.

Clock	MODE5	MODE4	Accumulator MODE7-6	Pipeline MODE11-8
40ns	0	0	01 -> 80ns	0000 (N=0)

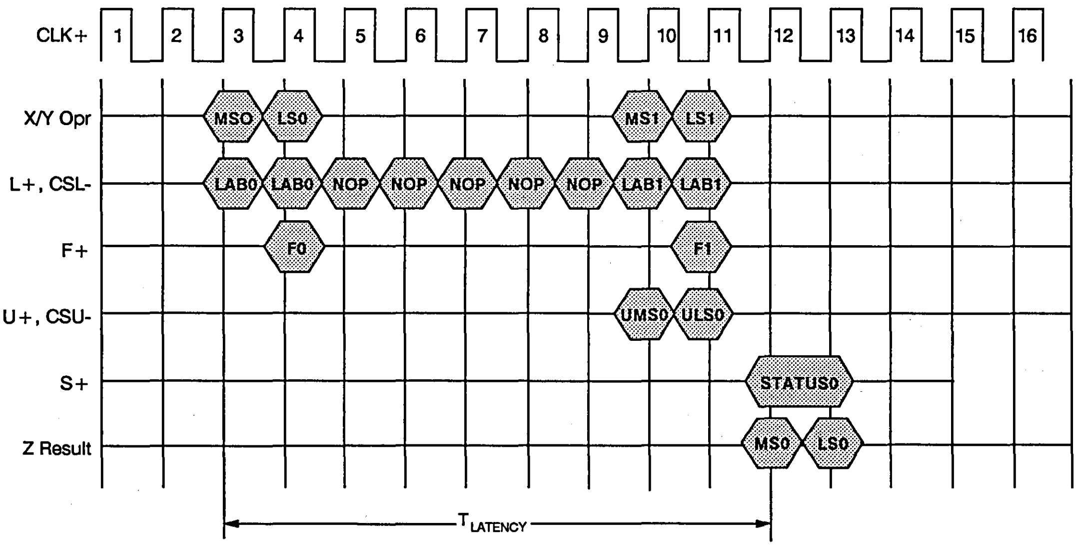


Figure 13. Flowthrough Double Precision Multiply for IDT721264

To minimize the total latency for the single and double precision ALU (Figure 14), the pipeline advance control is set to zero and all pipeline registers are made transparent.

Clock	MODE5	MODE4	Pipeline Register MODE 7-4	Pipeline Advance MODE 11-8
40ns	0	0	0000	0000 (N=0)

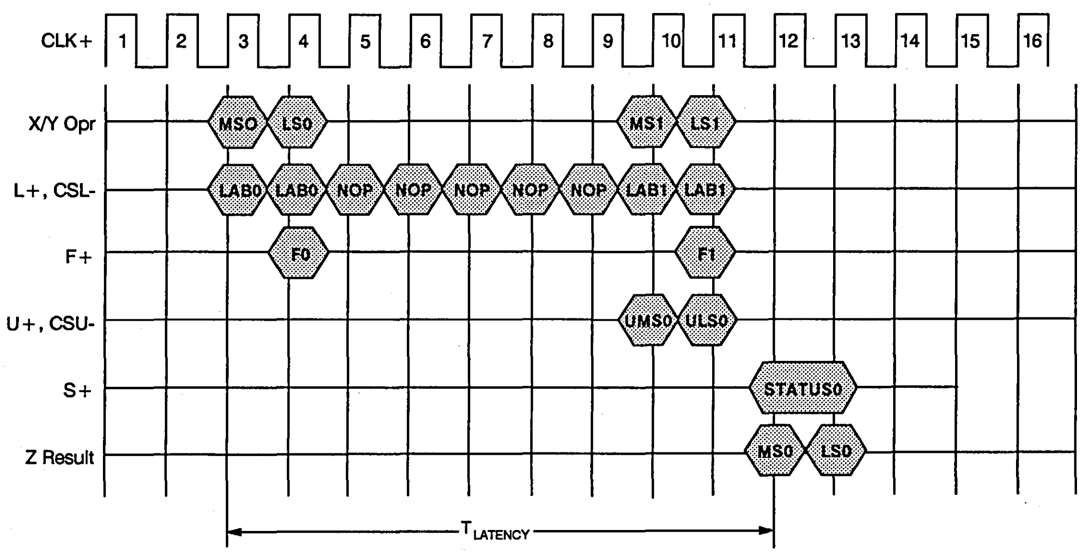


Figure 14. Flowthrough Double Precision ALU for IDT721265

Handling Denormalized Numbers

There are two ways to handle denormalized numbers in the IDT floating-point chip set: IEEE mode and Fast mode by programming mode bit MODE0. For applications requiring exact compliance with the IEEE standard (as in general purpose computers), it is necessary to treat the denormalized numbers exactly as specified by the IEEE standard. In this mode, the chip set contains the circuitry to detect the denormalized numbers and to generate the flag on the status bus S0-3. The IDT721264 multiplier cannot handle the denormalized number directly, but can detect it. The "denormalized number" exception is signaled on the status-bus S0-3. The operand is then moved to the floating-point ALU. The floating-point ALU provides a special instruction called "single wrap or double wrap" to convert a denormalized number into a normalized number called "wrap number". This wrapping process is done by shifting the fraction of a denormalized number toward the most significant bit until the hidden bit becomes one. At the same time, the exponent of the denormalized number (in this case is 0) is subtracted from the shift-number of the fraction in the two's complement format. Multiplication can be performed on the wrap number. The whole process consumes extra cycles because the software must detect the exception and call special routines to handle the exceptions.

However, the floating-point chip set provides a faster way to treat denormalized numbers for applications which do not require the IEEE standard compliance. In this particular mode, called FAST MODE, the denormalized number is treated as zero in order to shorten the processing delay.

Division

This section describes how to use the IDT721264/65 floating-point chip set to perform the convergence division of Q=A/B in the IEEE floating-point format. To achieve more accuracy, the non-restoring bit-wise algorithm is required; but it also consumes more time. The convergence method for binary division generates the reciprocal of the divisor by an iterative process and then obtains the quotient by multiplying the dividend by the divisor reciprocal. The operation A/B may be considered as A * 1/B. First, it is necessary to evaluate the term 1/B. A simple but effective iterative method called NEWTON-RAPHSON is used. Consider the graph of F(x) = 1/X (Figure 15) and assume that X_i is the first approximation of a root. If a tangent is drawn to the curve at $X=X_i$, then the tangent intersects with the X-axis at X_{i+1}, which is an improved approximation for the root of F(x) = 0.

The slope of the curve is defined as follows:

$$F(X)' = F(X_i)/X_i - X_{i+1}$$

Therefore:

$$X_{i+1} = X_i - F(X_i)/F'(X_i)$$

This method, based on the first order Taylor series expansion, is very useful for improving a first approximation to a root of an equation of the form f(x) = 0.

To find 1/B, we define f(x) = B -1/x, where B is the divisor. The root for this equation when f(x) = 0 corresponds to x = 1/B. Using the Newton-Raphson method, the iterative equation for the reciprocal of divisor 1/B is finalized as follows:

$$X_{n+1} = X_n(2-BX_n)$$

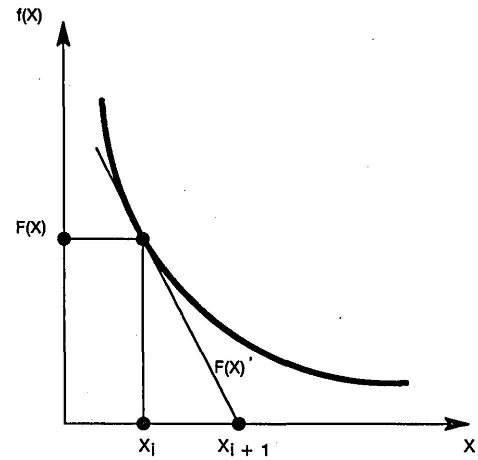


Figure 15. Graph of F(x) = 1/X

Here, B is the divisor and the X_n are successively closer approximations to the reciprocal 1/B. In order to use the Newton-Raphson method to obtain the quotient, the function must converge. When the function converges, the quotient is obtained. For this reason, this method does not provide an accurate remainder. The first approximation is very important for the success of this method. Since the equation for the reciprocal value is iterative, making the process converge requires that the first approximation X_0 of the divisor reciprocal must fall within the range:

$$0 < X_0 < 2/B \text{ if } B>0$$

$$2/B < X_0 < 0 \text{ if } <0$$

The error of X_i is reduced quadratically for every iteration. For example, computing the reciprocal of a 32-bit number can start by using a hardware lookup table to provide the 8 most significant bits. The next iteration will provide 15 bits and the third iteration provides 29 bits of accuracy. Depending on the application and accuracy desired, two or three iterations may be used. The example below illustrates the iterative equation and its quadratic convergence:

Example:

– To find the reciprocal of the number: B = 5.35

Because: B > 0: 0 < X_0 < 2/B= 0.373831775

1. Iteration: X_0 is chosen as 0.1 Error: 0.086915887
2. Iteration: X_1 = 0.1465 Error: 0.040415887
3. Iteration: X_2 = 0.178176962 Error: 0.008738925
4. Iteration: X_3 = 0.186507314 Error: 0.000408573

- To find the reciprocal of the number: B = 0.75

1. X_0 = 1 Error: 0.333334
2. X_1 = 1.25 Error: 0.083334
3. X_2 = 1.328125 Error: 0.005208
4. X_3 = 1.333313 Error: 0.000021

To implement the Newton-Raphson division algorithm, a hardware lookup-table which generates the reciprocal value of the first approximation (seed) is required. There are two lookup tables: one for the exponent and one for the fraction. The 8-bit exponent of a single precision floating-point number is used to address one of the 256 exponents in the lookup-table. Similarly, the fraction lookup table is addressed by the eight most significant bits of the fraction. Figure 16 illustrates how the divisor B is mapped into the first reciprocal value X_0 using lookup-tables. The sign-bit is unmodified. The exponent lookup table generates the exponent reciprocal values (H) using the 8-bit exponent as the address. H is calculated using the following equation:

H = 253 - E, where E is the 8-bit exponent of the divisor and ranges from 1 to 252.

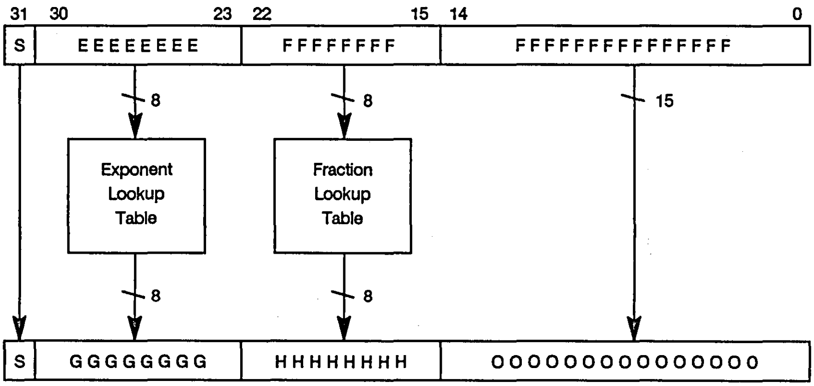


Figure 16. Division Look-up Table

Special Cases for E:

1. E=255 and F not zero: B is NaN. In this case, the quotient is NaN and signals the INF.
2. E=255 and F zero: B is INF. In this case, the RE can be set to zero.
3. E=254 : B is too large. In this case, the divisor and quotient are multiplied by the constant 1/2 and the operation is tried again.
4. E=253 : B is too large. In this case, the divisor and quotient are multiplied by the constant 1/4 and the operation is tried again.
5. E=0 : B is DNRM or zero. Depending on the value of the divident: DIV, the division results in different values as specified below:

–If DIV = NaN, DNRM, ZERO then Q = NaN status = INV
–If DIV = INF then Q = INF
–If DIV = NRM then Q = INF

The look-up table for the first reciprocal values of the fraction is generated using either eight or twelve most significant bits of the fraction. The other least significant bits of the first reciprocal fraction are filled in with the values zero. The output of the hardware lookup tables is generated as below:

1. Eight bits of the fraction:

   G= (256 x 512/257 + F) - 256

   where F ranges from 0 to 256
2. Twelve bits of the fraction:

The number of iterations can be reduced by using larger ROM look-up table:

G= (4096 x 8192/ 4097 + F) - 4096

where F and H range from 0 to 4095

With the hardware look-up implementation shown in Figure 17, the division can be calculated as follows:

1. Load divisor B into the input register DIN2 and DIN1.
2. Calculate the first reciprocal approximation of the divisor X_0 .
3. Perform the multiplication: B * X_i .
4. Select special instruction 2 - A to perform the 2 - BX_i . The IDT floating-point chip set provides special instructions to execute 2-A which saves the extra loading of the constant "2", as well as the external hardware to generate the constant.
5. If the accuracy is adequate, go to step 6; if not, go to step 3.
6. Perform the multiplication Q= A x 1/B.

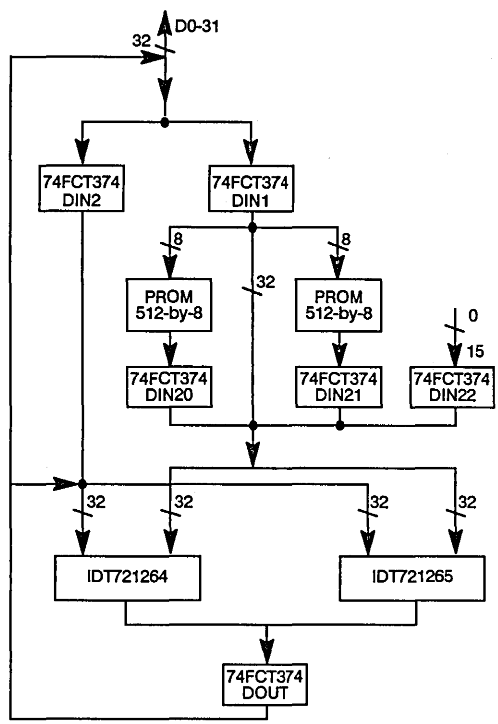


Figure 17. Configuration for Floating-Point Division

Applications

The IDT floating-point chip set is ideally suited for applications where large number crunching capability, high precision and very wide dynamic ranges are required. Typical examples of such applications are in high-speed signal processing, array processors, scientific engineering work stations and high-speed graphics accelerators. The data flow of such applications can be subdivided into either pipelined or flowthrough. Typical pipelined applications are FAST FOURIER TRANSFORM (FFT) and FINITE IMPULSE RESPONSE (FIR) which consist of n repetitive multiplications and additions. High-speed number crunching in a general purpose computer is a classic example of a flowthrough application where the operations happen at random intervals and require exact treatment of exceptions. Both architectures are implemented in the IDT floating-point chip set. Figures 18 and 19 illustrate some typical applications:

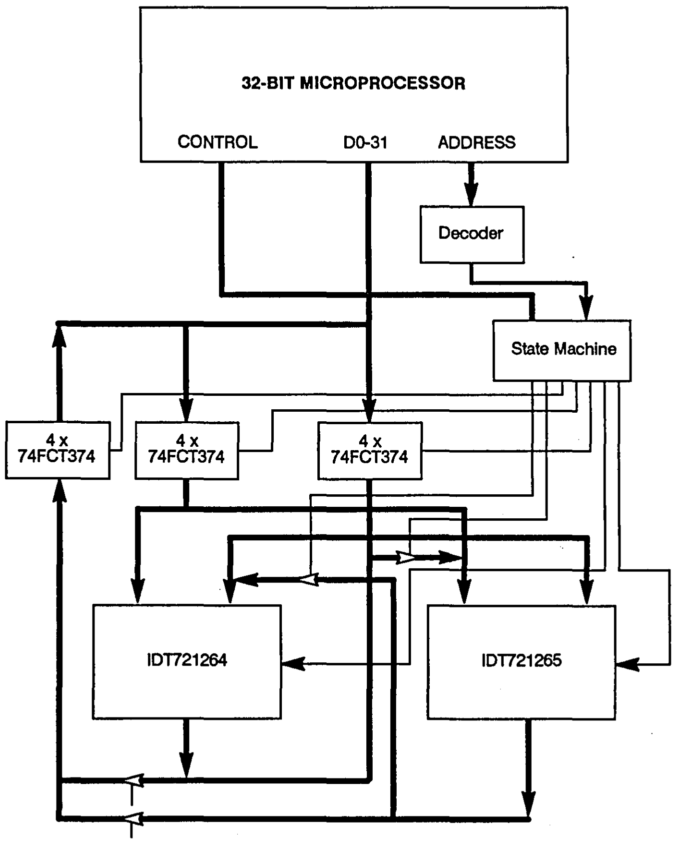


Figure 18. Floating-Point Interface with a 32-Bit Microprocessor

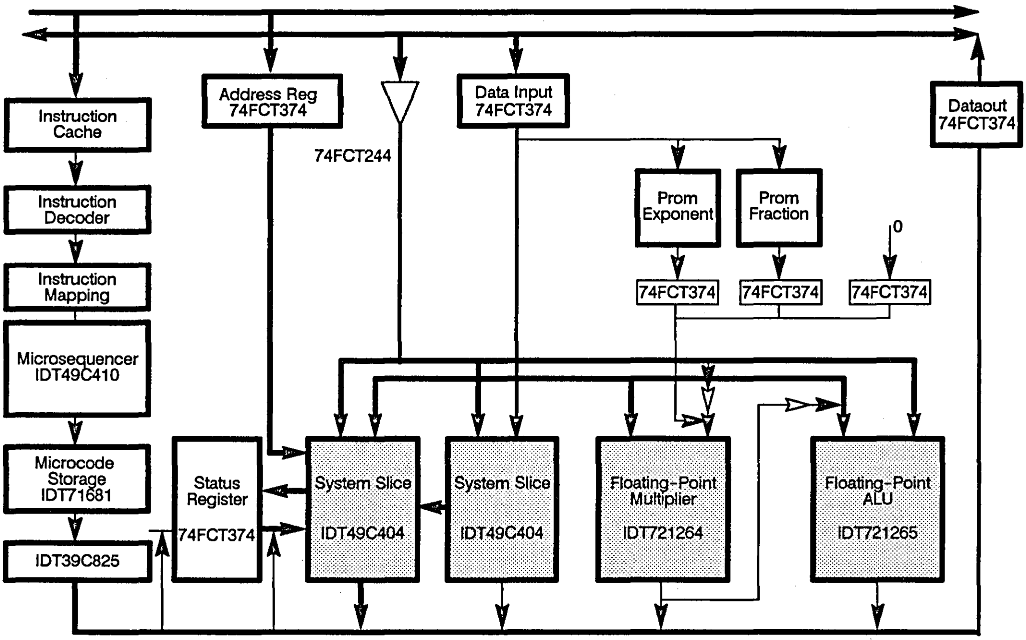


Figure 19. Typical 64-Bit CPU

FFT Processor

DSP applications such as radar, sonar, speech processing, imaging and seismic data processing require a real time spectrum analysis using the Fast Fourier Transformation. FFT is a high-speed algorithm for computing the Fourier transformation of a discrete time signal called the Discrete Fourier Transform (DFT). By taking advantage of the mathematical properties of periodic waveforms, the DFT algorithm provides a means to reduce the number of computations of the Fourier transform. The two well-known equations for the DFT are described below:

– Direct DFT:

$$X(k) = X(n)\, W^{nk,} \text{ where } k = \{0, N - 1\}$$

$$W = e^{-j(2\pi/N)}$$

– Inverse DFT:

$$x(n) = 1/N\, X(k)\, W^{-nk}$$

The simplest and most popular DFT for radix 2 can be rewritten in the two forms:

– Decimation in time:

The decimation-in-time algorithm consists of a butterfly in which two inputs (A and B) are combined to give two outputs (X and Y):

$$X = A + W_N{}^k \times B$$

$$Y = A - W_N{}^k \times B$$

Where $W_N{}^k = e^{-j(2\pi/N)} = e^{-\theta} = \cos\theta - \sin\theta$, and X and Y are complex numbers:

$$ReX = ReA + ReB \times \cos\theta + jImB \times \sin\theta$$

$$ImX = ImA + ImB \times \cos\theta - j\, ReB \times \sin\theta$$

$$ReY = ReA - ReB \times \cos\theta + ImB \times j\sin\theta$$

$$ImY = ImA - ImB \times \cos\theta - ReB \times \sin\theta$$

– Decimation in frequency:

The decimation in frequency algorithm also consists of a butterfly in which two inputs (A and B) are combined to give two outputs (X and Y):

$$X = A + B$$

$$Y = (A - B)\, W^k{}_N$$

The basic FFT calculation is the butterfly, which consists of four multiplications and six additions or subtractions. Figure 20 shows the basic butterfly calculation.

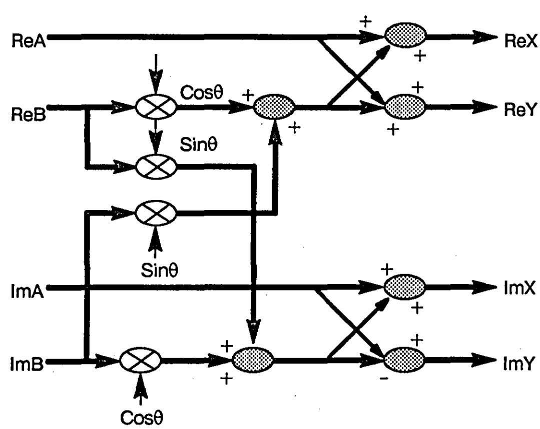


Figure 20. Butterfly Computational Diagram

Figure 22 illustrates an eight-point FFT; the butterflies occur in the group. Although the butterflies' spans and positions (as well as the twiddle factor W) vary from pass to pass, the signal flow through the butterfly is the same. The repetitive butterfly calculations are suitable for using the pipeline architecture of the floating-point IDT721264 and IDT721265.

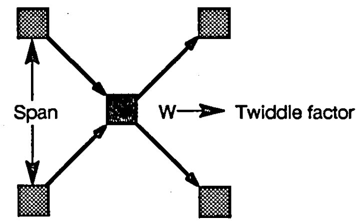


Figure 21. Butterfly

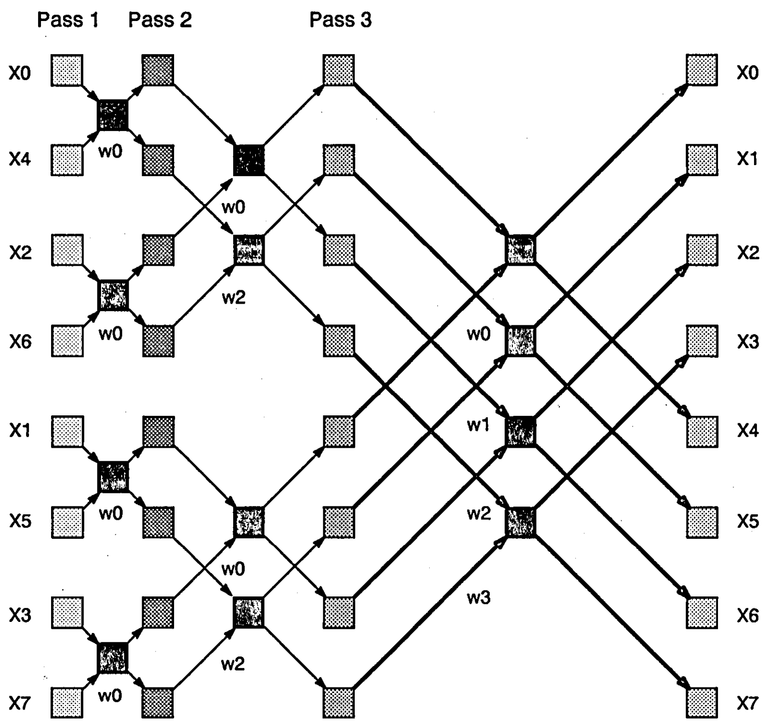


Figure 22. Eight-Point FFT Graph

Figure 23 illustrates the implementation for a single cycle radix 2 butterfly calculation. It consists of four building blocks: a control block, address generator, working RAM and execution unit. The control block contains the microsequencer (IDT49C410), a writeable control store using high-speed static RAM (IDT71681), pipelined registers (IDT49C818) and several MSI chips for condition code selection. The 16-bit-slice (IDT49C402) and some three-state buffers (IDT74FCT244) are used to generate the addresses for the working RAM, as well as for the FFT execution unit. The working RAM is configured from high-speed dual-port RAMs (IDT7132s) which are used as a buffer between the host processor and FFT processor. The execution block consists mainly of a single-clock butterfly network using the IDT floating-point chip set and several pipeline registers (IDT39C520). To accomplish a single clock cycle butterfly calculation, the butterfly network is highly pipelined. In the first stage of the butterfly network, four multiplications are performed in parallel. Then the products are pipelined into the second stage where the intermediate additions are executed. The last stage generates the final results for two complex numbers.

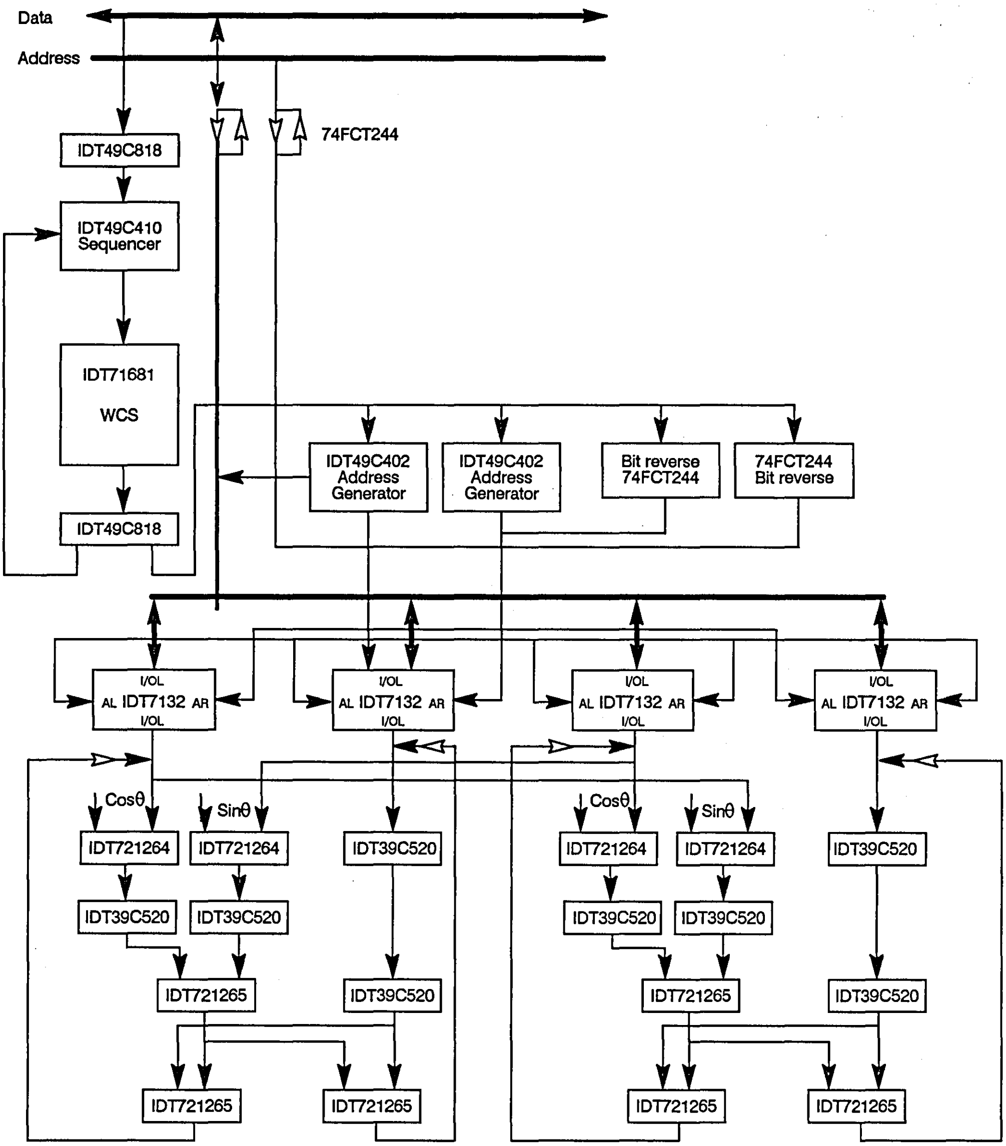


Figure 23. Pipelined FFT Processor

14

CONCLUSION

As the need for high-speed data computation with greater dynamic range and higher precision increases, so does the complexity of the hardware solution. The IDT721264 and IDT721265 provide an integrated high-performance CMOS solution for floating-point processors ideally suited for graphics accelerators and digital signal processing applications.

THE IDT49C404 32-BIT MICROPROGRAM MICROPROCESSOR

Integrated Device Technology, Inc.

APPLICATION NOTE AN-13

INTRODUCTION

IDT49C404 32-bit CMOS microprogram microprocessor's detailed functionality and operation is discussed in this User's Manual. This manual is subdivided into multiple sections each concentrating on a section of particular importance. These sections are: General Information – includes description, block diagram and pin definitions. Architectural Overview – explains the operation of the key functional blocks; seven port RAM, funnel shifter, ALU and mask/merge logic. Special Instruction definitions and Serial Protocol Channel diagnostics operation.

This manual is based on operating in the 32-bit mode; however, a section has been added within the Special Instructions category which defines the operating modes for 64-bit applications.

GENERAL DESCRIPTION

The IDT49C404 is an expandable, microprogrammable 32-bit ALU and register file designed in advanced high-speed, low-power CEMOS™. Highlighting the monolithic three-bus device is a powerful 7-port 64-word-by-32-bit working RAM, a 64-bits-in/32-bits-out cascadable funnel shifter, a high-speed multi-function ALU and the necessary Mask generation and Merge for field manipulation within a 32-bit word (see Figure 1).

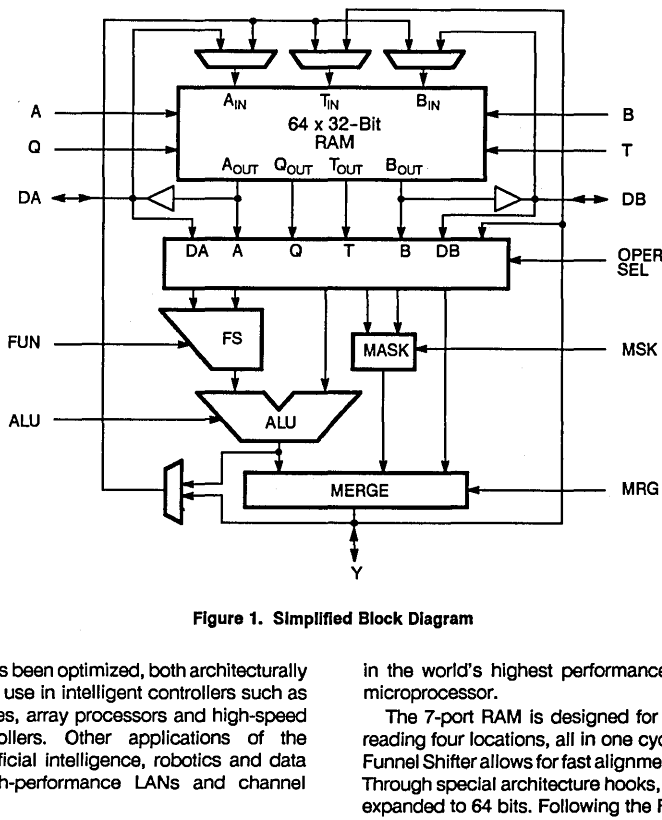


Figure 1. Simplified Block Diagram

This monolithic device has been optimized, both architecturally and instruction set-wise, for use in intelligent controllers such as high-speed graphics engines, array processors and high-speed communication/disk controllers. Other applications of the IDT49C404 range from artificial intelligence, robotics and data base manipulation to high-performance LANs and channel MUXes.

The IDT49C404 is the industry's only 32-bit microprocessor capable of performing the ALU, Shift and Merge operations in a single cycle. This feature, coupled with a highly orthogonal instruction set, fast 80ns cycle time and low CMOS power (1.5W), results in the world's highest performance microprogrammable 32-bit microprocessor.

The 7-port RAM is designed for writing three locations while reading four locations, all in one cycle. The 64-bits-in/32-bits-out Funnel Shifter allows for fast alignment of data to any bit boundary. Through special architecture hooks, the IDT49C404 can be easily expanded to 64 bits. Following the Funnel Shifter is a multi-function, streamlined 32-bit ALU which provides high-performance operations from any bit boundary while selecting status flags (carry, overflow and sign-bit). The 32-bit Merge Logic block, under

14

Printed in the U.S.A. 9/87

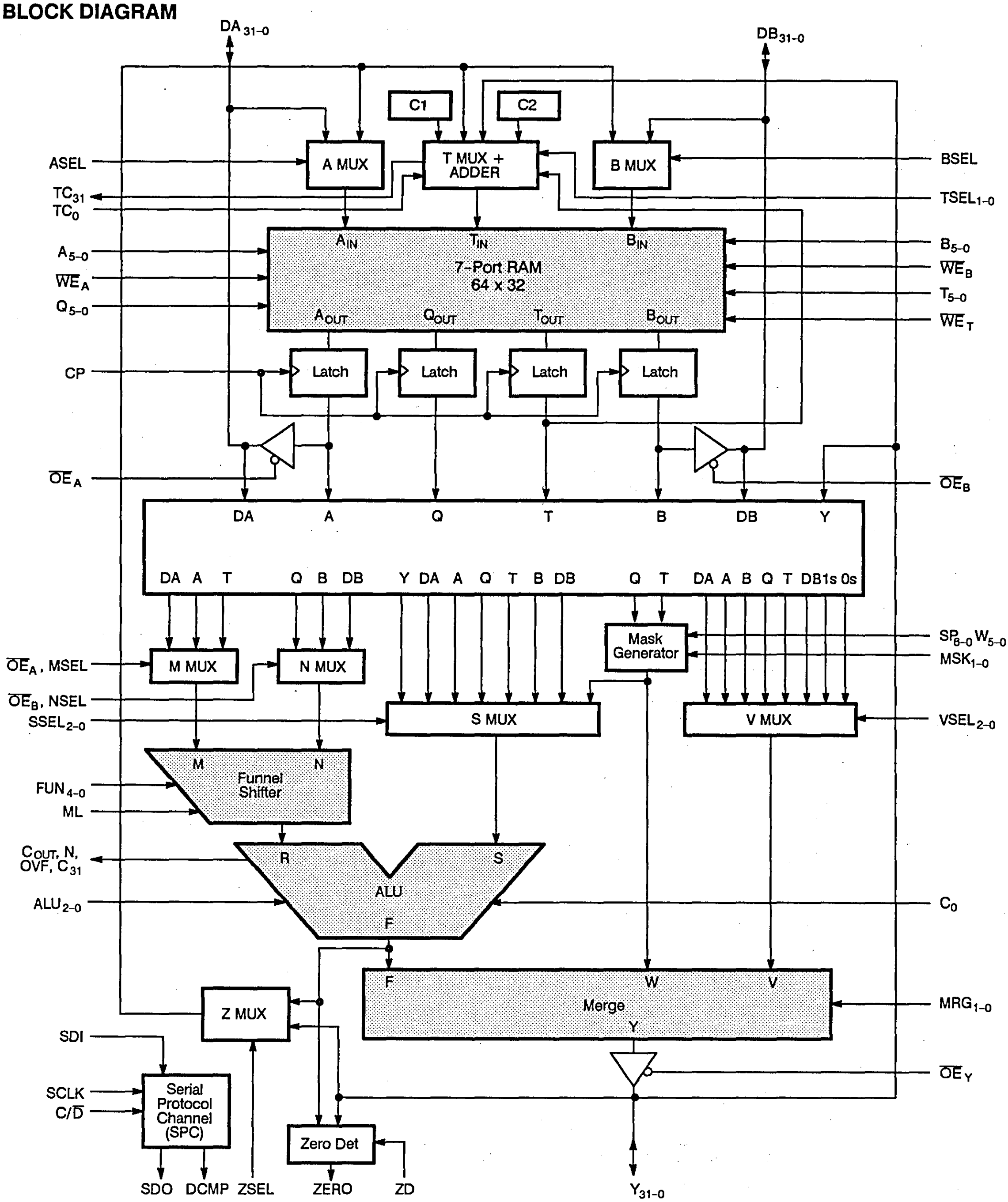
control of the 32-bit Mask Generator, enables the designer to select a subfield of any bit width on any bit boundary.

The IDT49C404's parallel architecture allows for large performance improvements in many applications. Often-used functions within graphics applications, such as block BLIT, line and curve drawing algorithms, take full advantage of the flexible 7-port RAM, Funnel Shift, Mask/Merge architecture. This same architectural approach also lends itself perfectly to high-speed disk and communication controller applications where extensive bit and subfield manipulation are needed.

The new IDT49C404 also features comprehensive on-chip diagnostics—Serial Protocol Channel (SPC)—which greatly simplifies the task of writing and debugging microcode, field maintenance debug and test, as well as system testing during manufacturing. Operation of this innovative IDT technique is performed by only four pins: Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Command/Data (C/$\overline{D}$).

Microcode for the device is developed by using the industry standard meta-assemblers and development systems for system level debugging available from Step Engineering, HILEVEL and Hewlett Packard.

BLOCK DIAGRAM



14

PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
DA_{31-0}	Thirty-two-bit data input/output port is under control of the signal $\overline{OE}_A$. When the $\overline{OE}_A$ is low, RAM output port A can be directly read on these lines. Data on these lines can be selected as the source for the ALU, funnel-shifter or loaded into port A of the working RAM.
DB_{31-0}	Thirty-two-bit data input/output port is under control of the signal $\overline{OE}_B$. When the $\overline{OE}_B$ is low, RAM output port B can be directly read on these lines. Data on these lines can be selected as the source for the ALU, funnel-shifter or loaded into port B of the working RAM.
Y_{31-0}	Thirty-two-bit data input/output port is under control of the signal $\overline{OE}_Y$. When $\overline{OE}_Y$ is low, the merge output can be directly read on these lines. Data on the lines can be loaded into port T of the working RAM or selected as the source for the ALU when $\overline{OE}_Y$ is high.
$\overline{OE}_Y$	A control input pin which, when low, enables the output of merge-logics on the lines Y_{31-0} and, when high, disables the Y_{31-0} three-state output buffers.
$\overline{WE}_A$	The write control signal for RAM input port A. If the signal $\overline{WE}_A$ is low, the data on the DA lines or Z bus is written into the RAM (input port A) when the clock signal is low.
$\overline{WE}_B$	The write control signal for RAM input port B. If the signal $\overline{WE}_B$ is low, the data on the DB lines or Z bus is written into the RAM (input port B) when the clock signal is low.
$\overline{WE}_T$	The write control signal for RAM input port T. If the signal $\overline{WE}_T$ is low, the data on the Z lines, Y lines, T + C1 or T + C2 is written into the RAM (input port T) when clock signal is low.
$\overline{OE}_A$	A control input for data input/output port DA. When $\overline{OE}_A$ is low, RAM output port A is read on the DA line. When $\overline{OE}_A$ is high, the data on the data lines can be selected as the source for the ALU or loaded into port A of the working RAM.
$\overline{OE}_B$	A control input for data input/output port DB. When $\overline{OE}_B$ is low, RAM output port B can be read on these lines. When is $\overline{OE}_B$ high, the data on the DB lines can be selected as the source for the ALU or loaded into port T of the working RAM.
CP	The clock input to the IDT49C404. When clock is low, data is written in the seven-port RAM.
TC_0	Used as carry input for the T counter.
TC_{31}	Used as carry output for the T counter.
ML	The input pin which can be used to load the external bit in order to fill in the vacant positions of a word in shift-linkage.
C_0	The carry input to the least significant bit of the ALU.
C_{OUT}	Indicates the carry-output.
N	Indicates the sign N of the ALU operation.
OVF	Indicates the conventional two's complement overflow.
C_{31}	The carry output pin which is used to ripple the carry in the expansion mode (64-bit).
ZERO	The open drain input/output pin which, when high, generally indicates that all outputs are low.
ALU_{2-0}	Instruction inputs are used to select the operations for the ALU.
A_{5-0}	Six RAM address inputs which contains the address of the RAM word appearing at RAM output port A and into which new data is written when $\overline{WE}_A$ is low.
B_{5-0}	Six RAM address inputs which contains the address of the RAM word appearing at RAM output port B and into which new data is written when $\overline{WE}_B$ is low.
T_{5-0}	Six RAM address inputs which contains the address of the RAM word appearing at output port T and into which new data is written under control of TSEL.
ASEL	Defines what data RAM port A receives, either DA or Z bus.
BSEL	Defines what data RAM port B receives, either DB or Z bus.
Q_{5-0}	Six RAM address inputs which contain the address of the RAM word appearing at output port Q.
SP_{6-0}	The seven pins are used to specify the start positions or the number of shift positions.
W_{5-0}	The six pins are used to specify the word width.
ZSEL	Selects the source of the Z bus between the output of the ALU (F) or the Y bus.
MSEL	Taken together with $\overline{OE}_A$, selects the source of the M input into the funnel shifter.
NSEL	Taken together with $\overline{OE}_B$, selects the source of the N input into the funnel shifter.
$VSEL_{2-0}$	Selects the source of the V bus used for merging with the output of the ALU.
ZD	Chooses zero detect of the ALU output (F) or the Y bus.
$SSEL_{2-0}$	Selects the source of the S operand input to the ALU.
FUN_{4-0}	Controls the operation of the funnel shifter.
MSK_{1-0}	Selects the function of the mask generator.
MRG_{1-0}	Controls the merge function.

PIN DESCRIPTIONS (Cont'd)

PIN NAME	DESCRIPTION
$TSEL_{1-0}$	Selects the source of the data to be written into the T port of the RAM.
SDI	Serial data input to the SPC command and data registers for diagnostics.
SDO	Serial data output from SPC command and data registers for diagnostics.
SCLK	SHIFT clock for loading the SPC command and data registers for diagnostics.
$C/\overline{D}$	Command/data control input for SPC operation.
DCMP	The open drain compare output for SPC diagnostics.
VCC_{7-0}	Eight pins for power supply 5 volt, all of which must be connected to 5 volts.
GND_{16-0}	Sixteen pins for ground, all of which must be connected to ground.

14

GENERAL ARCHITECTURAL OVERVIEW

The IDT49C404 is a high-speed 32-bit microprogrammable CMOS microprocessor slice which can be cascaded to 64 bits. It allows simple yet high-speed arithmetic and logic operations on Subfields, Shift, Rotate, Mask and Merge.

In general, the IDT49C404 can be viewed as a 7-port working RAM feeding into a funnel shifter, then into an ALU and then into Merge Logic. The control of each of these blocks is orthogonal, allowing the user to select data from registers, shift it, operate on it with the ALU and then merge it in only one cycle. Optionally, the Funnel Shifter or ALU can be bypassed, allowing the user additional flexibility. In this way, the designer may avoid paying a performance penalty when a particular algorithm requires only one or the other. Thus, the cycle time can be tailored to match the processing requirements.

The IDT49C404 can be divided into the following functional segments:

- Three 32-bit bidirectional I/O ports
- 7 port 64-word x 32-bit RAM
- 64-bits-in/32-bits-out cascadable Funnel Shifter
- 32-bit ALU
- Mask Generator
- Merge Logic
- Diagnostics circuitry

Three-Bus Architecture

The IDT49C404's 3-bus architecture consists of three bidirectional 32-bit ports (DA, DB and Y). The DA and DB bidirectional buses connect respectively to the A and B RAM outputs and A and B RAM inputs. Thus, data can be read out of the RAM on DA and DB or data can be brought in independently on DA and DB. This special feature allows for easy RAM expansion. Since data can be brought out on the DA and DB buses, other ALU elements can be connected externally which extend the overall ALU/Funnel Shifter/Mask-Merge capabilities.

The third 32-bit bus, Y, is the output of the Merge Logic and also the input back to the RAM ports A, B and T via the Z bus or internal Y bus. The Z MUX multiplexes between the ALU or the Y bus. By selecting the output of the ALU, the results of the ALU operation can be stored back into the RAM, while data may be brought out through the Merge path onto the Y bus. This results in an ALU operation in parallel with the extraction of data out of the register file. Additionally, there is an alternate data path which allows the Y bus to connect directly into the T MUX, such that data can be written from the ALU back into the RAM while data is being brought in, at the same time, through the Y bus to the RAM.

This three-bus approach allows for the easy data accessibility necessary when designing high-performance microprocessor-based systems.

Seven-Port RAM

The IDT49C404 incorporates a 64-word-by-32-bit RAM which has seven ports: four read ports and three write ports. The four read ports are A, B, Q and T. The A and B ports are considered the data path ports and can be used interchangeably. During most cycles they supply data to the Funnel Shifter, ALU and Merge Logic. These ports can be considered to be similar to the A and B ports of the IDT39C203 4-bit ALU. The Q and T output ports are used mainly for controlling the start and width for the Funnel Shifter and Mask generation for Merge operations. Since the Q and T ports are outputs of the RAM, the start positions may be computed on previous cycles using the ALU, providing extensive programmer flexibility.

There are three write ports: A, B and T. The A and B ports are typically used for results from the current cycle. The T port is used for incrementing counter values in the RAM, as well as loading data from the Y bus in parallel with ALU operations. There are four address buses controlling A, B, Q and T. In one cycle, the seven-port RAM is capable of writing to three locations while reading from four locations. This feature highlights the IDT49C404's highly parallel architecture.

64-Bit Funnel Shifter

The Funnel Shifter accepts two 32-bit operands (DA, A, DB, B,Q or T) which are operated on as a 64-bit word. The output of the Funnel Shifter is the result of selecting any consecutive 32-bit word within the 64-bit operand. The 32-bit word can start on any bit boundary between 0 and 31. The M and N input MUXes allow the user to swap the data, as well as duplicate it, allowing for barrel shifting. The Funnel Shifter also has the capability of taking any 32-bit word as an input and extending the sign, as well as providing zero fill. Through special hooks in the architecture, the Funnel Shifter can be expanded along with the ALU/Merge Logic to perform 64-bit operations in a single cycle.

ALU

The output of the Funnel Shifter feeds the 32-bit ALU. The ALU can perform conventional binary operations such as logic, addition and subtraction, as well as multiplication and division. Also, the sum of the start and the width information can be used to select the bit boundary from which the carry, sign and overflow flags will output as status. This allows for true arbitrary subfield operations. The other ALU inputs are selected from DA, DB, Y, A, B, Q, T or Mask Generator.

Mask Generation And Merge Logic

The mask generation and merge logic allows for field manipulation within the 32-bit resulting word. The mask generator, which determines how the bits will be merged between V and F, is controlled by start and width input pins. The start and width can also come from Q or T. T is used for start and Q is used for width, thus start/width can be calculated, stored in the register file and used in the mask generator. An alternate to the mask generator is a mask which comes directly from the Q or T outputs of the RAM, allowing for totally arbitrary masks.

The V input of the merge logic comes from a multiplexer which can select any output of the RAM, DA, DB, all 1s or all 0s. The F input is connected to the output of the ALU. The mask is used to merge the V and F input on a bit-by-bit basis, which results in the Y output.

Included in the merge logic is a priority detect circuit. It is used to produce a binary weighted code to indicate the location of the highest order one on its input.

DETAILED ARCHITECTURAL OVERVIEW

SEVEN-PORT RAM

As shown in Figure 3A, the 64-word-by-32-bit working RAM is a seven-port RAM. It has three dedicated input ports, A_{IN}, B_{IN} and T_{IN}, and four dedicated output ports, A_{OUT}, B_{OUT}, T_{OUT} and Q_{OUT}, with latches at the output ports. Any four RAM locations addressed at the address ports A, B, T and Q can be read simultaneously. Identical data appears at the four output ports when the same addresses are applied at address port A, address port B, address port T and address port Q. When the clock CP is high, latches at output ports A, B, T and Q are transparent and when the clock CP is low, the latches hold the data. A, B, T and Q can be selected as source for the ALU operation, Funnel Shifter and Merge Logic. A and B can be read out on the DA and DB lines. Q and T can be sources for the Mask Generator. When the addresses applied to address port A, B or T for writing data into RAM are matched, the data written into the matched RAM location is undefined.

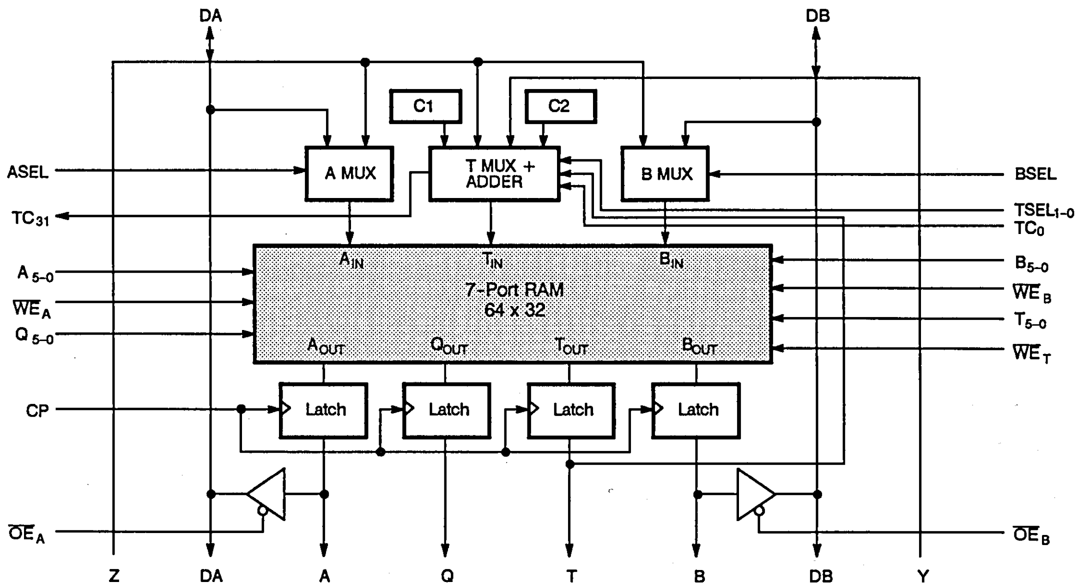


Figure 3A. Seven-Port RAM

The DA and DB buses are bidirectional 32-bit buses. As input buses they can provide data (as operands) into the Shifter/ALU/Merge block, as well as provide access to the seven-port RAM. As output buses they can be used to deliver data from the seven-port RAM to off-chip functions.

Under control of the select signals, ASEL and BSEL, data on the DA lines, DB lines or Z bus at the input ports A and B can be written into any two RAM locations whose addresses are applied at address port A or B. Writing occurs when the clock CP is low and the appropriate control signals, $\overline{WE}_A$ and $\overline{WE}_B$, are enabled low.

Data is written into the T_{IN} port under control of the $\overline{WE}_T$ and $TSEL_{1-0}$ signals. The $TSEL_{1-0}$ is used to select between the Y or Z bus, as well as increment a location identified by the T address lines. C_1 and C_2 are 32-bit registers that can be loaded with special instructions through the Z bus. The 32-bit increment can be performed with one of two values, C_1 or C_2. The 32-bit adder used for incrementing has carry-in and carry-out pins, TC_0 and TC_{31}, respectively. See Figure 3B.

14

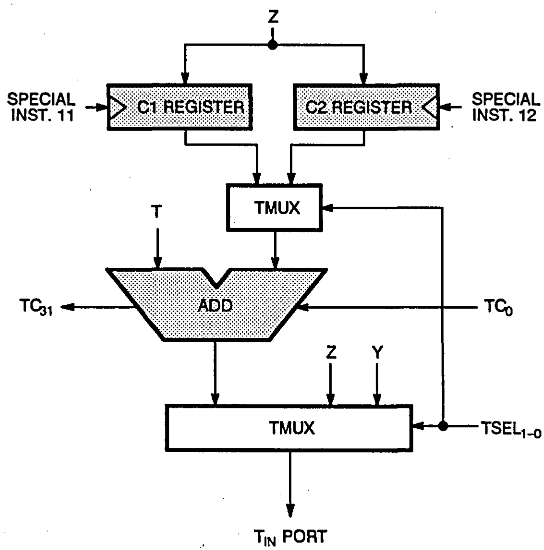


Figure 3B.

A RAM DEST		
Mnemonic	ASEL	Source
DA	0	DA Bus
Z	1	Z Bus

B RAM DEST		
Mnemonic	BSEL	Source
Z	0	Z Bus
DB	1	DB Bus

T Source		
Mnemonic	TSEL	Source
Z	0 0	Z Bus
Y	0 1	Y Bus
TC1	1 0	$T + C1 + TC_0$
TC2	1 1	$T + C2 + TC_0$

Figure 4A. T, A, B Instructions

Under control of the special instruction "load T, immediate", 16-bit immediate data can be loaded directly into the RAM location whose address is applied at the address port T. During the execution of the special instruction "multiply or divide", the contents of RAM T can be shifted up or down. In the adder mode, TC_0 is an input and TC_{31} is an output (see special instructions).

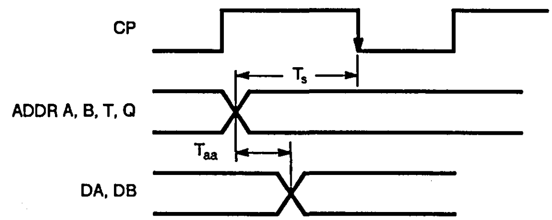


Figure 4B. Read Timing of the 7-Port RAM

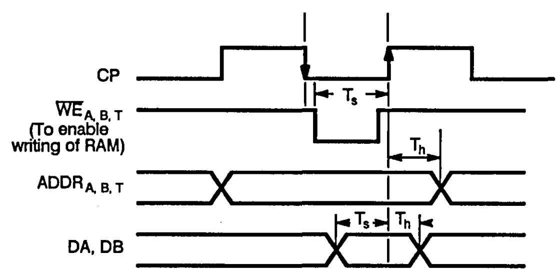


Figure 4C. Write Timing of the 7-Port RAM

EXECUTION BLOCK

The IDT49C404 can be divided into two functional blocks, the seven-port RAM and the execution block. The execution block (see Figure 5) processes the data on the IDT49C404. It includes the Funnel Shifter, ALU, Mask Generator and Merge Logic. The source for this block is a set of individual orthogonal control buses. Each of the individual functions has its own control signals. This block can select from nine possible operands: DA, A, Q, T, B, DB, 1s, 0s and Y. The results of this block can be written back into the RAM via the Y or Z buses or be sent outside the device via the Y bus.

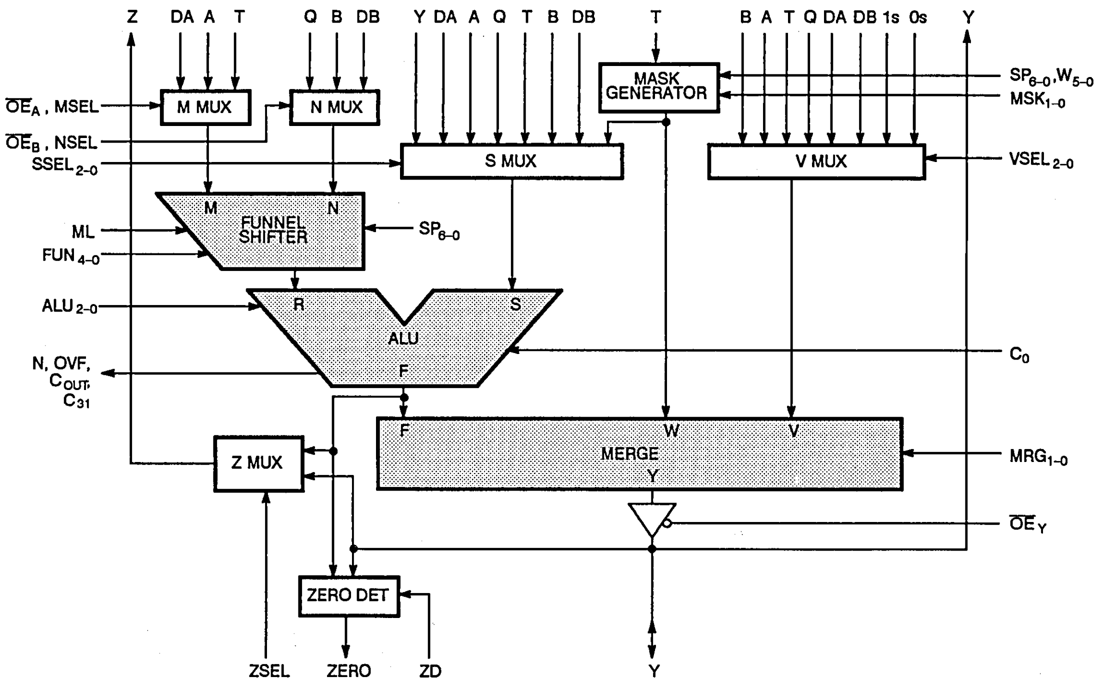


Figure 5. Block Diagram of Execution Circuitry

The organization of this block is the Funnel Shifter, which aligns data and inputs it to the ALU, and the output which can be merged into original operands as well as fields of all ones or zeros. With this organization, arbitrary fields of bits can be manipulated in one clock cycle. Performance tailoring, as defined in the Funnel Shift operations, can be accomplished by bypassing the Funnel Shifter or the ALU in any given cycle. In this way, a Shift/Merge or an ALU/Merge cycle can be achieved without paying a timing penalty for the unused function.

Manipulation of bit fields is accomplished by using all of the three functional elements in this block. Figure 6 shows how a 32-bit word with a subfield (B) can be modified with another word (A). First, the data in word A is aligned with B using the Funnel Shifter. The ALU can then combine the two words which will result in a 32-bit word where only the target subfield has correct data. Finally, the Merge unit merges the resulting partial field back into the original word (A).

The start (SP) and the width (W) information is used to tie together the different units in the execution block. The start information controls the Funnel Shifter for data alignment. The sum of the start and width is used to select the bit boundary to fetch flag information like sign, overflow and carry from the result of the ALU. Finally, the start and width information is used to generate a mask to control the Merge unit. In the 32-bit configuration, the most significant bit of SP and W should be tied low.

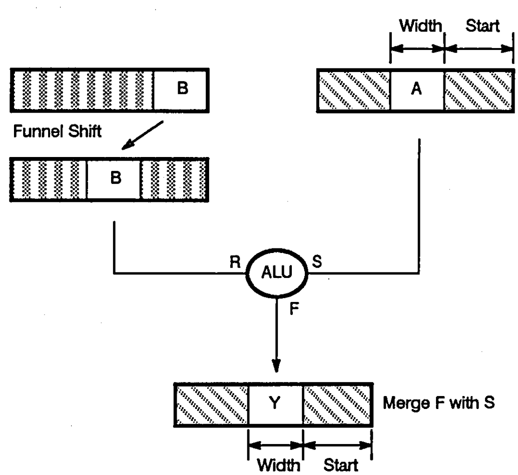


Figure 6. Alignment and Merge Operation

14

FUNNEL SHIFTER

The Funnel Shifter (Figure 7) is a block of logic which takes two 32-bit inputs, concatenates them into a 64-bit word and extracts out a 32-bit word starting on any bit boundary. Given the appropriate inputs, it can perform a variety of tasks such as barrel shift, arithmetic and logical linear shifts by any number of bits in a single cycle.

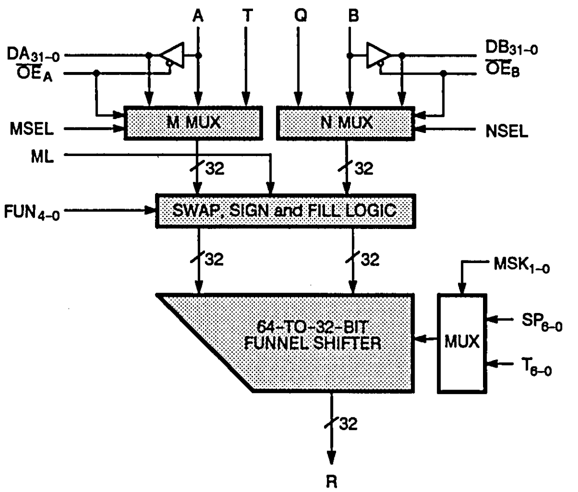


Figure 7. Detailed Funnel Shifter Diagram

The Funnel Shifter block can be segmented into three sections: operand select, SWAP and shifter. The operand selection is controlled by $\overline{OE}_A$, MSEL, $\overline{OE}_B$ and NSEL. The programmer can select from DA, A, Q, T, B and DB and route them to the M and N inputs of the shifter (Figure 8). The SWAP section is controlled by the FUN inputs which determine the fundamental operation of the total Funnel Shifter block. The SWAP logic swaps the M and N inputs, as well as performs fill operations on the M and N operands. The fill operations that are supported are sign, zero and fill with the value of the ML input pin. The fill operation is defined as replicating one bit across many.

M Source Selection			
Mnemonic	**$\overline{OE}_A$**	**MSEL**	**M Source**
AOE	0	0	A
T	0	1	T
A	1	0	A
DA	1	1	DA

N Source Selection			
Mnemonic	**$\overline{OE}_B$**	**NSEL**	**N Source**
BOE	0	0	B
Q	0	1	Q
B	1	0	B
DB	1	1	DB

Figure 8. M and N Source Selection

The shifter extracts a 32-bit word from the 64-bit word that is formed as a result of concatenating the two 32-bit inputs. The extensive list of Funnel Shift operations is shown in Figure 9. The start position is determined by a 6-bit two's complement number (seven pins are provided for cascading to 64 bits). The start position is determined either by the SP pins or the T output port of the RAM. The Mask Generator Source control (MSK) inputs determine whether SP or T will be used. The origin is at the boundary between the two 32-bit input words.

Mnemonic	FUN	Function	Operands[1]
SMLZ	00 000	Shift M and fill with 0	0, M
SNLZ	00 001	Shift N and fill with 0	0, N
SMLM	00 010	Shift M and fill with ML	ML, M
SNLM	00 011	Shift N and fill with ML	ML, N
XNM	00 100	Extract field from N, M	N, M
XMN	00 101	Extract field from M, N	M, N
SMAZ	00 110	Shift M arithmetic and fill 0	Sign, M, 0
SNAZ	00 111	Shift N arithmetic and fill 0	Sign, N, 0
SMAM	01 000	Shift M arithmetic and fill ML	Sign, M, ML
SNAM	01 001	Shift N arithmetic and fill ML	Sign, N, ML
BM	01 010	Barrel shift M	M
BN	01 011	Barrel shift N	N
PM	01 100	Pass M	M
PN	01 101	Pass N	N
PZ	01 110	Pass all 0s	0
PO	01 111	Pass all 1s	1
SMLZBA	10 000	Shift M and fill with 0, Bypass ALU	0, M
SNLZBA	10 001	Shift N and fill with 0, Bypass ALU	0, N
SMLMBA	10 010	Shift M and fill with ML, Bypass ALU	ML, M
SNLNBA	10 011	Shift N and fill with ML, Bypass ALU	ML, N
XNMBA	10 100	Extract field from N & M, Bypass ALU	N, M
XMNBA	10 101	Extract field from M & N, Bypass ALU	M, N
SMAZBA	10 110	Shift M arithmetic and fill 0, Bypass ALU	Sign, M, 0
SNAZBA	10 111	Shift N arithmetic and fill 0, Bypass ALU	Sign, N, 0
SMAMBA	11 000	Shift M arithmetic and fill ML, Bypass ALU	Sign, M, ML
SNAMBA	11 001	Shift N arithmetic and fill ML, Bypass ALU	Sign, N, ML
BMBA	11 010	Barrel shift M, Bypass ALU	M
BNBA	11 011	Barrel shift N, Bypass ALU	N
POCM	11 100	Pass 1s Complement of M	M
POCN	11 101	Pass 1s Complement of N	N
PMFM	11 110	Pass M and fill ML bit from Bit 0 to SP	M
PNFM	11 111	Pass N and fill ML bit from Bit 0 to SP	N

NOTE:

1. Operand order for negative start or shift down is shown. For positive start or shift up, swap operands (i.e. N, M → M, N). See Figure 11.

Figure 9. Funnel Shifter Operations

When performing shifts with fill, a positive start position results in shifting the word up and filling in from the least significant bit position. When using a negative start position, the word is shifted down and fill bits are inserted from the most significant end of the word. In the arithmetic shifts, the sign is propagated when shifting down and shifted around when shifting up (see Figure 10).

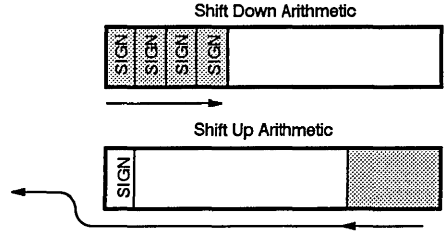


Figure 10. Shift Up/Down Arithmetic

14

The Extract operation extracts 32 consecutive bits to form a 64-bit word which is the concatenation of two 32-bit words. When extracting from M and N, where M is the most significant word, positive start positions select a 32-bit word starting in the N word and negative start positions starting in the M word (see Figure 11). When using negative start positions, the lower 32-bit word (N) is replicated above the upper 32-bit word (M).

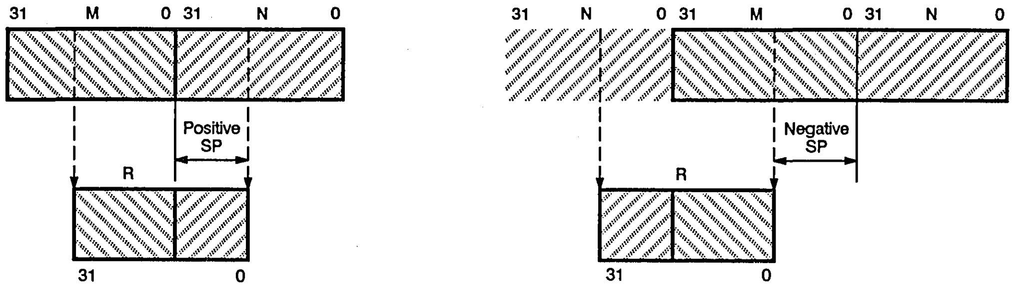


Figure 11. Positive/Negative Start Positions

When performing a rotation or barrel shift, a positive number indicates moving the bit in the least significant position towards the most significant end of the word.

When the Pass With Fill operation is performed, a 32-bit unshifted word is generated which is identical to the input word with the exception that the bit positions from zero to the position identified by SP are filled with the value of the ML input pin. This operation is used when two words, which contain a field that is already aligned, are operated on by the ALU. By filling the bit positions from zero to SP for one of the operands, the carry-in flag can be propagated to the embedded subfield (see Figure 12).

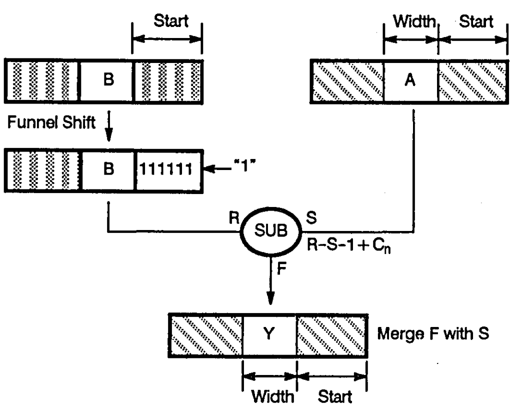


Figure 12. Aligned Bit Field Manipulation

ARITHMETIC LOGIC UNIT

The Arithmetic Logic Unit is a fully cascadable 32-bit ALU with full carry lookahead (Figure 13A). It performs addition and subtraction operations, as well as logical functions. The flags sign (N), overflow (OVF) and carry (C_{OUT}) are derived from the upper end of field identified by the sum of the start and width operands. When cascading (64-bit system), the flags are wire-ORed together between the two devices. The C_{31} line is the carry-out of the 32nd bit position of the ALU and is provided for ripple carry expansion (in the 64-bit application) into the C_0 input which is the carry input of the most significant device.

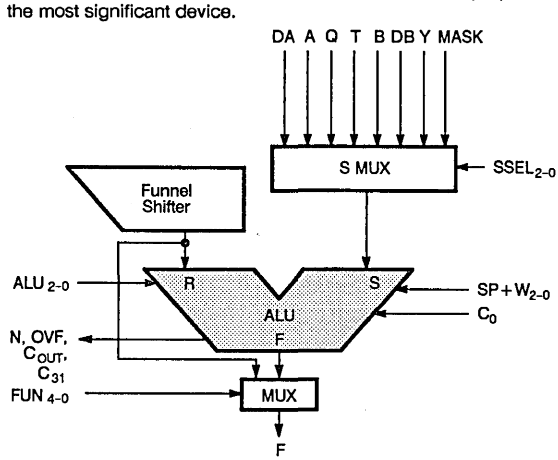


Figure 13A. ALU

The R operand is supplied by the Funnel Shifter while the S operand is supplied by the SMUX. For convenience and cycle time improvement, the Funnel Shifter can be placed in the pass mode. It can pass DA, A, DB, B, Q, T, all ones or all zeros. The SMUX is controlled by the SSEL inputs (Figure 13B). The possible operands via the SMUX are DA, A, Q, T, B, DB, Y or the output of the Mask Generator. The Mask Generator can be used as an operand for logical operations, as well as provide values for increments or decrements. The 4-bit Funnel shifter control is decoded in order to control a mux for bypassing the ALU. In this way, when the ALU is not required, it need not contribute to the delay through the device.

S Source				
Mnemonic	SSEL			Source
DA	0	0	0	DA
A	0	0	1	A
Q	0	1	0	Q
T	0	1	1	T
B	1	0	0	B
DB	1	0	1	DB
Y	1	1	0	Y
MASK	1	1	1	MASK

Figure 13B. S Source Instructions

The 3-bit instruction field which controls the ALU is shown in Figure 14. The opcode 101 is used to put the IDT49C404 into a special instruction mode where the VSEL and MRG control input pins determine what special instruction is executed. The special instructions are a group of operations which require special internal connections that cannot be controlled from the standard control input pins. Refer to the section on special instructions for more information.

ALU				
Mnemonic	ALU			Function
ADD	0	0	0	R + S + C_0
SUBR	0	0	1	S − R − 1 + C_0
SUBS	0	1	0	R − S − 1 + C_0
OR	0	1	1	R or S
AND	1	0	0	R and S
–	1	0	1	Special Instruction
EXOR	1	1	0	R exor S
EXNOR	1	1	1	R exnor S

Figure 14. ALU Instructions

MERGE LOGIC

The Merge Logic Unit combines two 32-bit words to form another 32-bit word under the control of a Mask. The Merge operation overlays a field of bits from one word onto another word. This is achieved by using the Mask to select which bits will be included in the result word. If the F Merge V function is selected, the F bus from the ALU provides the 32-bit word which is selected by the HIGH bits in the Mask. The word selected by the LOW bits in the mask is supplied by the VMUX which is controlled by the $VSEL_{2-0}$ input pins. The Mask is supplied by the Mask Generator and converts a start and a width input to a string of one bits in a word of zero bits.

The control lines for the Mask Generator are MSK_{1-0}. They select between the start and width as supplied from the SP_{6-0} and the W_{5-0} input pins or the RAM ports T and Q. These control lines are shown in Figure 15.

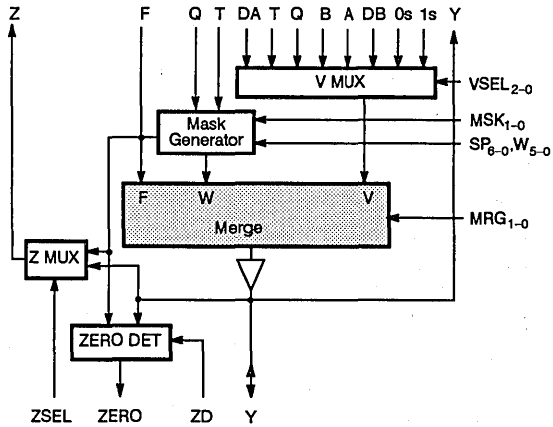


Figure 15. Merge Logic Unit

For example when F is merged with V, bit 0 of the output word receives bit zero of the word coming from the ALU (F) if bit 0 of the Mask is HIGH, or it receives bit 0 of the V bus if it is LOW. All of the bits in the result bus are processed in parallel at the same time. The Merge Unit can be characterized as thirty-two 1-bit MUXes which are controlled by the Mask (see Figure 16). If V Merge F is selected, operands F and V are swapped such that a 0 bit in W will select a bit in F.

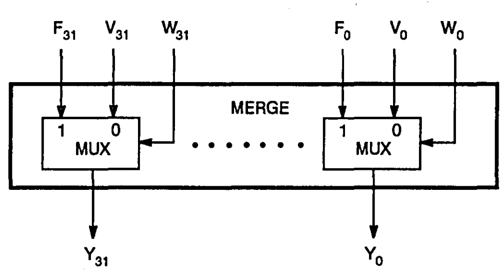


Figure 16. Detailed Diagram of Merge Function

The Merge Unit can combine various operands. It can directly pass the results of the ALU (F) as well as the Mask Generator. The output of the ALU (F) can be merged with the RAM ports Q and A, as well as the DB bus. The ALU results can also be merged into a word of all zeros or all ones (see Figure 17). These functions can be controlled by the VSEL inputs.

14

V Src				
Mnemonic	**VSEL**			**Source**
DA	0	0	0	DA
A	0	0	1	A
Q	0	1	0	Q
T	0	1	1	T
B	1	0	0	B
DB	1	0	1	DB
ZEROS	1	1	0	0's
ONEs	1	1	1	1's

Merge Control			
Mnemonic	**MRG**		**Function**
F	0	0	Pass F
V	0	1	Pass V
F to V	1	0	Merge F with V
V to F	1	1	Merge V with F

Figure 17. Merge Control Instruction

The Mask Generator produces a mask which is used by the Merge Unit. It can be used to select the RAM ports T or Q as a mask, or it can be used to generate a mask of a string of HIGH bits in a word of all LOW bits. There are seven SP pins to allow for control in the cascaded mode (64-bit operation of two devices). The width is provided by the W_{5-0} input pins. These operands can be used to select any width. The control lines MSK_{1-0} select which source is used for the Mask Generation (see Figure 18).

Mask Generator			
Mnemonic	**MSK**		**Source**
EXT	0	0	Start and Width from Instruction
INT	0	1	T & Q Supply Start and Width
T32	1	0	T as a 32-Bit Mask
Q32	1	1	Q as a 32-Bit Mask

Figure 18. Mask Generation Instructions

The Zero Detect can be performed on the output of the ALU or the Merge Unit. The ZD line determines the source for the Zero Detect. The ZSEL input steers the source of the Z bus between the output of the ALU or the Merge. When the output of the ALU is selected, data is allowed to be brought in through the Y bus pins and used in the ALU via the SMUX or written into the RAM via the T port. Alternatively, data could be passed through the Merge Unit by using an all zero mask to select the VMUX (see Figure 19).

Zero Detect Source		
Mnemonic	**ZD**	**Source**
F	0	F Bus
Y	1	Y Bus

Z BUS Source		
Mnemonic	**ZSEL**	**Source**
F	0	F Bus
Y	1	Y Bus

Figure 19. Zero/Z Bus Instructions

SPECIAL INSTRUCTIONS

The IDT49C404 supports a group of operations called Special Instructions (see Figure 20). These are instructions which require control over special internal connections beyond that provided by the standard set of control inputs. Special Instructions are achieved by setting the ALU control field to the binary value 101. The $VSEL_{2-0}$ and MRG_{1-0} inputs then select which Special Instruction is to be executed. The suggested layout of the microword is shown below, as well as a table of the Special Instructions and their opcodes.

Special Instructions (ALU = 101)				
Mnemonic	**MRG**	**VSEL**	**Function**	**Operands**
UMLT	0 0	0 0 0	Unsigned Multiply	A, B, T
TMLT	0 0	0 0 1	Two's Complement Multiply	A, B, T
TMLTL	0 0	0 1 0	Two's Complement Multiply Last Cycle	A, B, T
DIVF	0 0	0 1 1	First Divide	A, B, T
DIV	0 0	1 0 0	Second Divide	A, B, T
DIVL	0 0	1 0 1	Last Divide	A, B, T
PRF	0 0	1 1 0	Prioritize First Cycle (32 Bits)	S, Mask
PRS	0 0	1 1 1	Prioritize Second Cycle (64 Bits)	S
INC	0 1	0 0 0	S + Imm (7-Bit) + C_0	S, Imm
DEC	0 1	0 0 1	S – Imm (7-Bit) – 1 + C_0	S, Imm
LDI	0 1	0 1 0	Load T with Imm (16-Bit)	16-Bit Imm
LDC1	0 1	0 1 1	Load C1 from Z Bus	S
LDC2	0 1	1 0 0	Load C2 from Z Bus	S
EXCHG	0 1	1 0 1	Exchange RAM Locations	DA, DB
LDAB	0 1	1 1 0	Load DA into B Address	DA
LDBA	0 1	1 1 1	Load DB into A Address	DB
SMAGT	1 0	0 0 0	Sign Mag/Two's Comp Conversion	S
PROGS	1 0	0 0 1	Program Slice	–

Figure 20. Special Instructions

42	41 40	39 38	37 36	35 34	33	32 28	27 23	22 17	16 14	13 12	11 10	9 7	6 5	4 3	2 0
$\overline{OE}_Y$	$\overline{OE}_A$ $\overline{OE}_B$	MSEL NSEL	SSEL	MASK GEN	ML	FUNNEL SHIFTER	WIDTH	START	TSEL	ALU	MRG	VSEL	ZSEL ZD	ASEL BSEL	$\overline{WE}_A$ $\overline{WE}_B$ $\overline{WE}_T$
						16-BIT IMMEDIATE FIELD	16-BIT IMMEDIATE FIELD	16-BIT IMMEDIATE FIELD		SPECIAL INSTRUCTION FIELD	SPECIAL INSTRUCTION FIELD	SPECIAL INSTRUCTION FIELD			
							7-BIT IMMEDIATE FIELD	7-BIT IMMEDIATE FIELD							

NOTE:
SP6 and SP5 must be connected together and W5 must be connected to ground.

Figure 21A. Example of Instruction Field for a 32-bit System

44	43 42	41 40	39 38	37 36	35	34 30	29 24	23 17	16 14	13 12	11 10	9 7	6 5	4 3	2 0
$\overline{OE}_Y$	$\overline{OE}_A$ $\overline{OE}_B$	MSEL NSEL	SSEL	MASK GEN	ML	FUNNEL SHIFTER	WIDTH	START	TSEL	ALU	MRG	VSEL	ZSEL ZD	ASEL BSEL	$\overline{WE}_A$ $\overline{WE}_B$ $\overline{WE}_T$
							☒	☒		SPECIAL INSTRUCTION FIELD	SPECIAL INSTRUCTION FIELD	SPECIAL INSTRUCTION FIELD			
						16-BIT IMMEDIATE FIELD	16-BIT IMMEDIATE FIELD	16-BIT IMMEDIATE FIELD							
								7-BIT IMMEDIATE FIELD							

☒ Not used for 7 and 16-bit immediate

Figure 21B. Example of Instruction Field for a 64-bit System

Figures 21A & 21B show the Special Instruction field as well as two immediate fields. Several of the Special Instructions utilize immediate operands (7 bits or 1 bit) which are provided from microcode. The 7-bit immediate field is provided by the start position, while the 16-bit field is provided by the start, width and funnel control fields.

Some of the Special Instructions have special considerations when executed in the expanded 64-bit architecture. See the Expansion Mode section.

PROGRAM SLICE

The IDT49C404 can be expanded to a 64-bit system using two devices (see Figure 22). To configure a 64-bit system, there must be appropriate interconnect. Also, the "program slice" instruction must be executed to indicate two slices and their positions.

Programming slice number and position is done by executing the Special Instruction "program slice" (see Figure 20). The number of slices comes from the width pins (0 or 1) and the slice position from the C_0 input (slice 0 if C_0 is grounded and slice 1 if C_0 is high) because each slice raises its carry-out pin (C_{31}). For example, to program the 64-bit mode, ground the carry in line (C_0) and place the value "000001" on the width input pins.

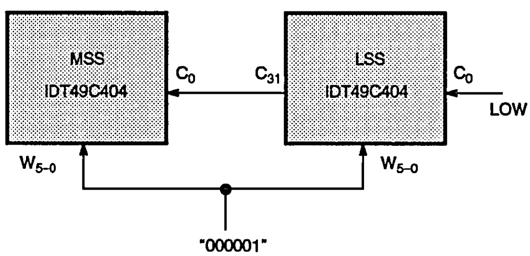


Figure 22. Programming 64-Bit Mode

Proper expansion interconnect will satisfy the requirements of device intercommunication for such things as a proper status flag generation, funnel shift cascade and special instructions like divide, multiply and prioritize. The status flag outputs (C_{OUT}, N, OVF) are tri-state outputs which turn on depending on which device has the appropriate information. During divide and multiply, the status flags provide the shift linkage for shifting one bit at a time. The carry-out of the 32nd bit of the ALU is connected to the carry-in of the first bit position of most significant slice. When RAM ports Q and T supply the start and width information, the SP and W pins are used to transmit the information from the least significant device to the most significant device. While this is happening, the pipeline register (which supplies external start and width) must be put in the Hi-Z state. During these operations, the 7 pins of the SP bus provide the start position, while the 6 pins of the W bus provide the width position.

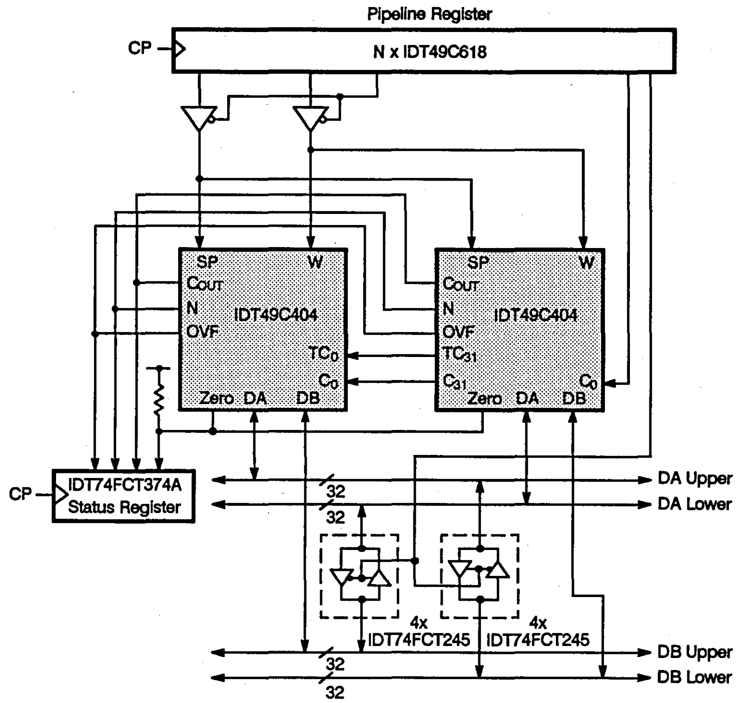


Figure 23. 64-Bit Configuration of Two Cascaded IDT49C404s

The 32-bit DA and DB buses of each device are taken in parallel to form two 64-bit buses. When the Funnel Shifter is being used, the DA and DB buses perform 32-bit swaps between the internal RAM of one device and the Funnel Shifter inputs of the other device. Therefore, two sets of transceivers must be provided to connect the lower 32 bits of the DA bus with the upper 32 bits of the DB and, conversely, for the other 32 bits of the upper DA and lower DB.

MULTIPLY

The IDT49C404 provides three Special Instructions to perform unsigned and signed two's complement multiply. These instructions work on a bit-by-bit basis. To use this instruction, the word addressed by the B port must be zero, the multiplier is addressed by the T address lines and the A address lines indicate the location of the multiplicand. After performing the multiplication operations several times, the resulting product will be stored in the locations addressed by the B and T ports. The word addressed by B is the 32 most significant bits and T is the 32 least significant bits of a 64-bit result (see Figure 24). There are no external connections required for 32-bit operations. For 64-bit configurations, external connections are required as shown in Figure 25.

To perform unsigned multiplication, the unsigned multiply instruction is executed 32 times. In order to perform signed multiplication the signed multiply instruction is executed 31 times, followed by one cycle of the "Two's Complement Multiply Last Cycle".

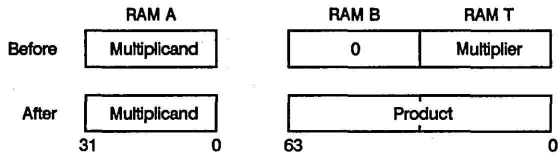


Figure 24. Multiply Operation

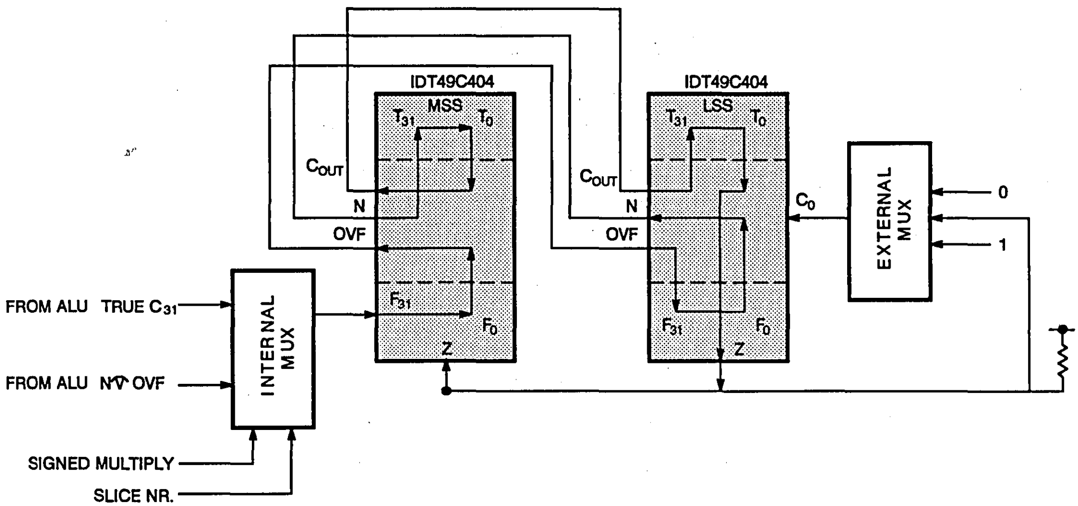


Figure 25. Multiply Operation in a 64-Bit System

TWO'S COMPLEMENT DIVISION

Three Special Instructions are provided for division which implement the non-restoring division algorithm. The B and T address inputs select the 64-bit dividend and the A address port identifies the 32-bit divisor. The quotient will end up in the location addressed by T, while the remainder is in the location addressed by B (see Figure 26). For 32-bit systems, no external connection is required. For 64-bit configurations, external connections are required. (see Figure 27).

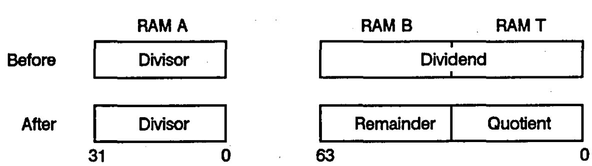


Figure 26. Two's Complement Division Operation

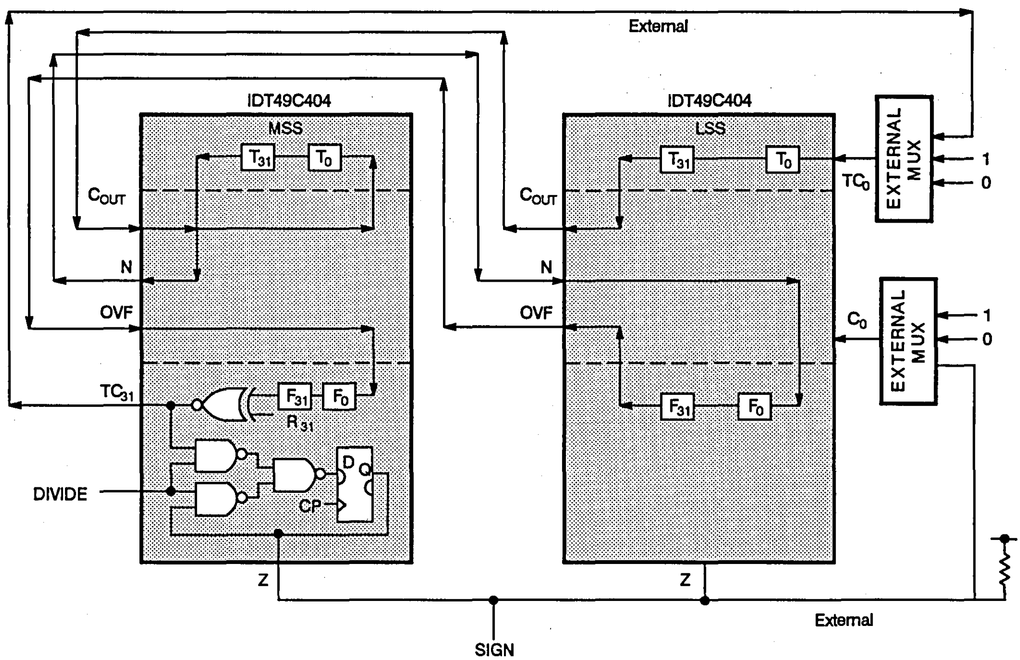


Figure 27. Divide Operation in a 64-Bit System

To perform 32-bit division, the "First Divide" instruction must be executed once followed by 30 cycles of the "Second Divide" instruction and, finally, one cycle of the "Third Divide" or last divide instruction.

PRIORITIZE

The IDT49C404 contains a 32-bit priority encoder. It is used to produce a binary-weighted code to indicate the location of the highest order one bit in a 32-bit word. The input to the priority encoder is from the SMUX. The Mask is used to determine which bit locations are eliminated from prioritization. The priority encoder generates a 6-bit binary output.

The IDT49C404 provides two Special Instructions for prioritizing. The first Prioritize instruction is used to perform the prioritizing on the operand provided by the SMUX. The result can be read on the Y lines or stored back in RAM simultaneous with the setting of the internal priority flag. The second Prioritize instruction is used to prioritize a 64-bit number in a 64-bit system. During the execution of the Special Instruction "Prioritize 1", the result of the most significant slice is moved to the least significant slice by reading out RAM A of the most significant slice which must be connected through bus tranceivers to the DA bus of the most significant device. At the same time, the internal priority flag of the most significant slice generated by the first Prioritize instruction is transferred to the least significant slice by using the ZF pin. When the ZF pin of the least significant slice is high, the data on the DB lines is loaded into RAM A of the least significant slice. When the ZF pin is low, RAM A of the least significant slice is unchanged. A zero is loaded into RAM A of the most significant slice.

INCREMENT/DECREMENT IMMEDIATE

There are two instructions provided for increment or decrement with an immediate value. The 7-bit immediate value is provided by the W_0, SP_{5-0} pins. The value to be operated on is supplied by the SMUX, controlled by the $SSEL_{2-0}$ input lines.

THE LOAD INSTRUCTION

The IDT49C404 provides a Special Instruction for loading data into the T_{IN} port. This instruction is used to load a 16-bit binary number into the least significant 16 bits of RAM location whose address is applied at the T address port. The most significant 16 bits are not affected by the execution of this instruction. The 16-bit immediate value is supplied by the FUN_{4-0}, W_{5-0} and SP_{6-0} pins. A 32-bit constant can be loaded by the Shift/Merge of two 16-bit loads.

LOAD C_1 AND C_2

Two instructions are supplied to load the registers C_1 and C_2 from the output of the ZMUX. When executing these instructions, a 32-bit word can be loaded through the Y pins via the ZMUX (with ZSEL = 1) or from the SMUX (controlled by $SSEL_{2-0}$) via the ZMUX (with ZSEL = 0).

LOAD DA TO B OR DB TO A

These two instructions route DA input into the B_{IN} port of the RAM and, conversely, the DB bus into the A_{IN} port. This allows for crossover of the DA and DB buses with respect to the A and B address.

SIGN/MAGNITUDE TWO'S COMPLEMENT

This instruction converts between sign magnitude or two's complement representation. The most significant bit is used to determine the operation. If the most significant bit is zero, the operand selected by the SMUX is passed unaltered. If it is a one, each bit in the operand is inverted and a one is added, resulting in a two's complement operation.

EXCHANGE

This instruction swaps the contents of the two RAM locations addressed by A and B.

SERIAL DIAGNOSTICS

As I.C.s become more complex and more integrated, additional consideration must be given to in-system testing and verification. IDT has addressed this increasingly important issue with Serial Protocol Channel.

The Serial Protocol Channel (SPC) is a flexible on-chip feature of the IDT49C404 which can be brought into use to monitor and control the operation of both the IDT49C404, as well as the interface hardware. It consists of four pins by which data can be entered into and extracted from a device through a serial data input and output port. Addresses and commands can be inserted into the device for stimulating and monitoring not only internal hardware, but the system bus and device I/O pins as well. SPC can be used at many points in the life of a product for diagnostic purposes such as system level design debug and development, system test during manufacturing and field maintenance debug and test.

The SPC has been optimized for a minimum number of pins with maximum flexibility. It consists of four pins:

- Serial Data Input pin (**SDI**) for inserting data and command strings
- Serial Data Output pin (**SDO**) for extracting information from the device
- Serial Clock pin (**SCLK**) for clocking the information
- Command/Data Mode pin (**C/$\overline{D}$**) to identify commands from data.

Figure 28 shows the internal architecture of the SPC on the IDT49C404. Its primary logic blocks consist of the Serial Command and Address/Data registers, the XFER strobe logic, the Command Decode logic and the I/O pads scan circuitry. The Command Register holds the command which controls the data paths and generates the signals necessary to exercise the hardware in the device.

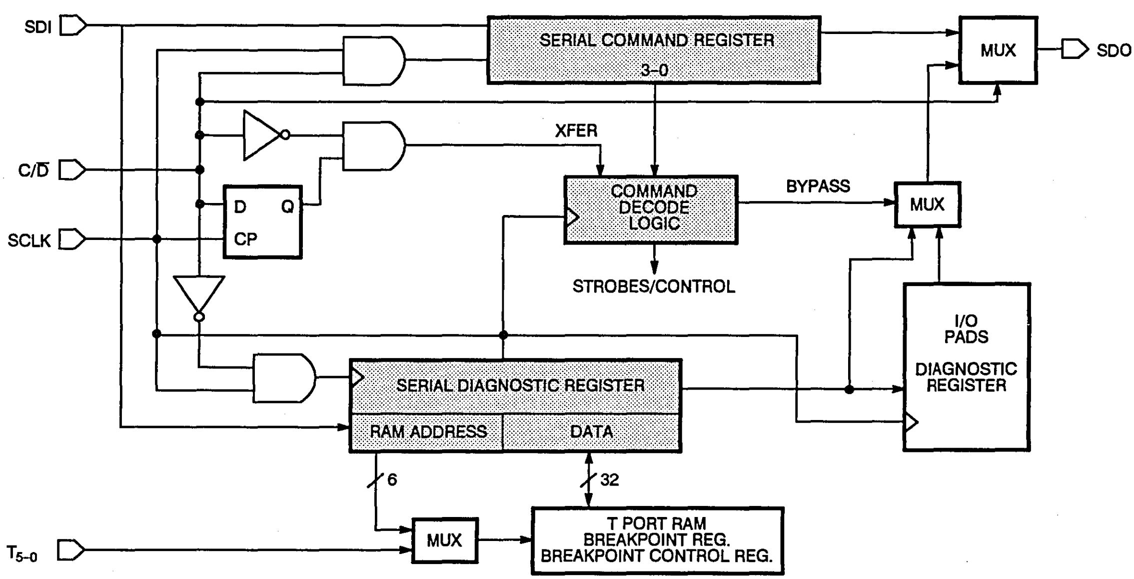


Figure 28. SPC Architecture on the IDT49C404

The Address/Data registers hold the RAM address/data and the data obtained after the diagnostic commands are executed. The I/O pad circuitry consists of scanning flip-flops that permit monitoring the state of the device pins, as well as simulating external conditions on these pins.

SHIFTING AND EXECUTION OF COMMAND AND DATA

An SPC operation is performed in four distinct phases:

1. data is shifted in,
2. command is shifted in,
3. command is executed, and
4. data is shifted out.

Information is shifted into the device under two phases of operation. In Phase 1, the C/$\overline{D}$ line is LOW and the data bits are shifted into the device. In Phase 2, the C/$\overline{D}$ line is HIGH and the command bits are shifted into the device.

During the Data Phase, data is simultaneously shifted into the serial data register, while the information from the data register is shifted out. During the Command Phase, opcode-type information is shifted through the serial ports. The command is executed when the last bit is shifted in and the C/$\overline{D}$ line is brought low. The execution phase is ended with the next serial clock edge. Figure 29 shows the sequence of events during a command execution.

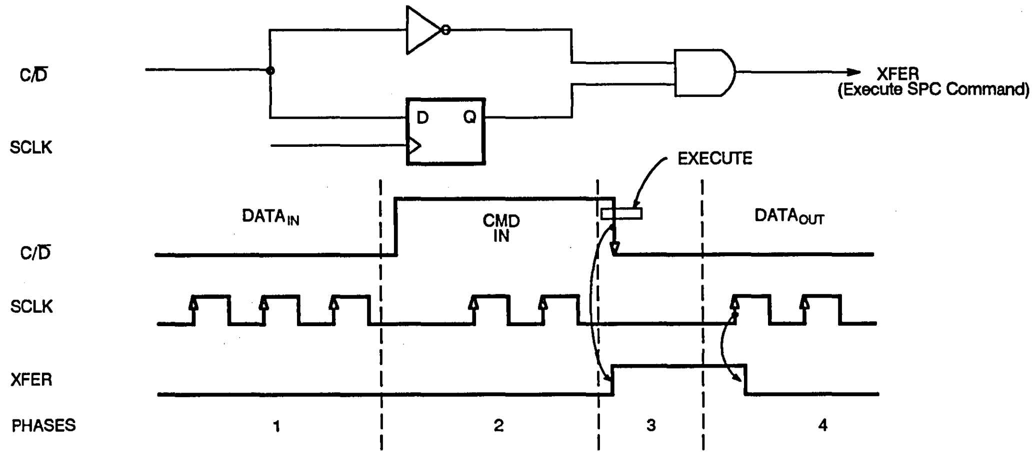


Figure 29. Phases of Executing SPC Commands

There is an internal signal called XFER which is generated from the SCLK and the C/$\overline{D}$ inputs. XFER is used both as an enable and a strobe. It begins with C/$\overline{D}$ transitioning from HIGH to LOW and ends with the next rising edge of SCLK. The strobe is then used to gate the decoded command register. The decode can be thought of as a one-of-N type decode. In this way, individual strobes and enables are generated which can be used to drive multiplexers and control registers/latches. In all devices there is a no-operation opcode (NOP) consisting of all command bits HIGH, which prevents the generation of any strobes.

With few exceptions, execution of the Serial Protocol commands can only be performed on devices which are currently in their standby mode. Each device has a unique standby mode. For MICROSLICE™ family devices, standby is when the system clock is stopped in the high state, guaranteeing that the RAM, latches and registers are not being accessed.

The above restriction does not apply to shifting command and data information through an active device into another device in its standby mode. The active device can be put in a NOP mode and this information shifted through without affecting its normal operation. When the commands (and data) reach their respective devices and execution is signaled by the lowering of the C/$\overline{D}$ line, those devices with a NOP opcode in their serial command registers will not generate internal strobes, thus leaving their current status undisturbed.

SPC permits a variety of diagnostic operations. It not only includes the ability to observe and modify the register files and key buses, but can also scan data out of the I/O pad cells which are connected to the pins of the device. In this way, by knowing the state of internal and external device connections, the state of the system surrounding the device can be monitored.

CASCADING SPC DEVICES

To the user, the SPC inside each device appears as two serial shift registers in parallel: one for command and the other for data, as shown in Figure 30. The serial clock shifts data while the command/data (C/$\overline{D}$) line selects which register is being accessed. The serial command register is used to control loading of data between the serial data register and other storage elements in the device.

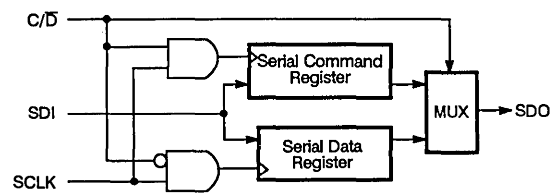


Figure 30. Basic SPC Structure

SPC also incorporates the feature of cascading an unlimited number of devices. By connecting the SDO pin of one device to the SDI pin of the next device, cascading of multiple devices with SPC becomes straightforward and simple. Figure 31 illustrates three cascaded devices.

In the Cascade Mode, the serial clock and the command/data line of each of device is connected in parallel. In this way, a minimal number of connections are made between successive SPC devices. To enter a command or data into the third device, the data must be shifted through the previous two devices. The data for each device must be entered in order of position in the ring through the first serial input. On the last shift clock, all of the data for each device will have reached its final destination.

The command registers for cascaded devices can be viewed as one long virtual microprogram command word, where each field corresponds to the individual command bits of each device. Similarly, the data register can be viewed as one continuous virtual data register, with each field corresponding to the data bits for each device.

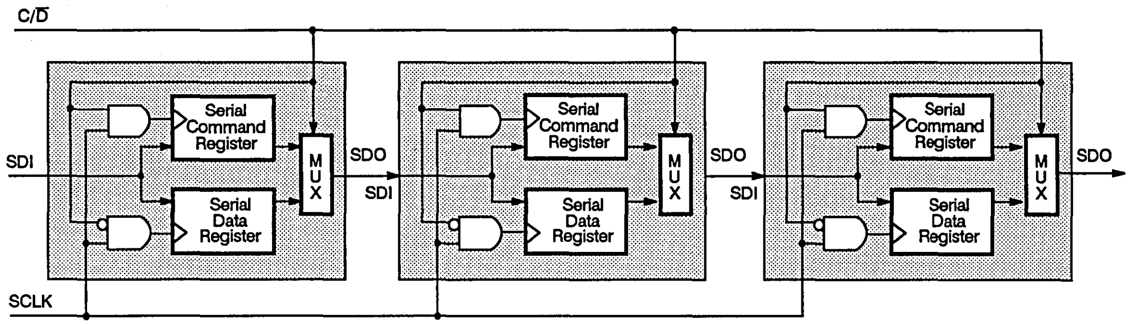


Figure 31. Cascaded Devices With SPC

SPC ON THE IDT49C404

The IDT49C404 accommodates a variety of diagnostic operations. It not only includes the standard Serial Protocol Channel, but also the ability to scan data out of the I/O pad cells which are connected to the pins of the device. In this way, the state of external connections can be observed, thus giving status information about the system surrounding the IDT49C404. The scan path through the I/O pad cells is in series with the serial data register.

Figure 32 illustrates the four pins (SDI, SDO, SCLK, and C/D̅) used to serially access the I/O pad cells, as well as the internal ALU registers and buses of the IDT49C404.

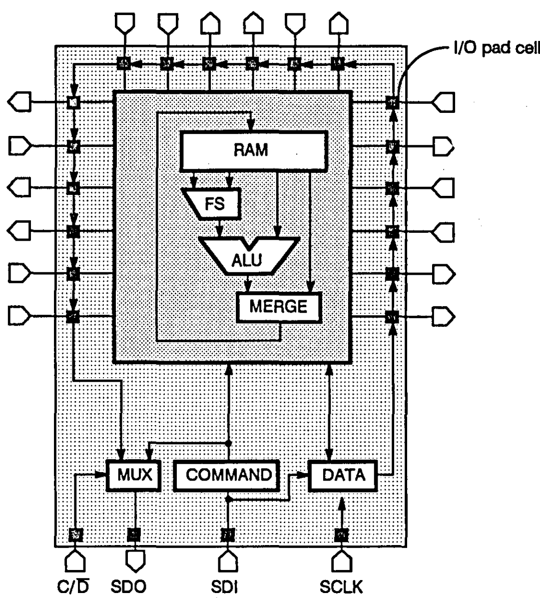


Figure 32. Conceptual Diagram of IDT49C404 Die Incorporating SPC Scan path

The block diagram in Figure 33 shows the detailed SPC architecture for the IDT49C404. It consists primarily of Serial Registers for Command, Data and Addresses and decode/control logic. The Serial Command Register consists of a 4-bit field (signals 3-0) which decodes 16 possible instructions. The 4-bit field coordinates the transfer of data between the RAM and the Serial Data Register, as well as controls an on-chip break detect mechanism.

In parallel to the path through the Command Register is a path going through a RAM Address Register, parallel-to-serial Data Register and the I/O pad scan. The Serial Data Register is connected to the internal bus to gain access to the RAM register file and the data break point circuitry.

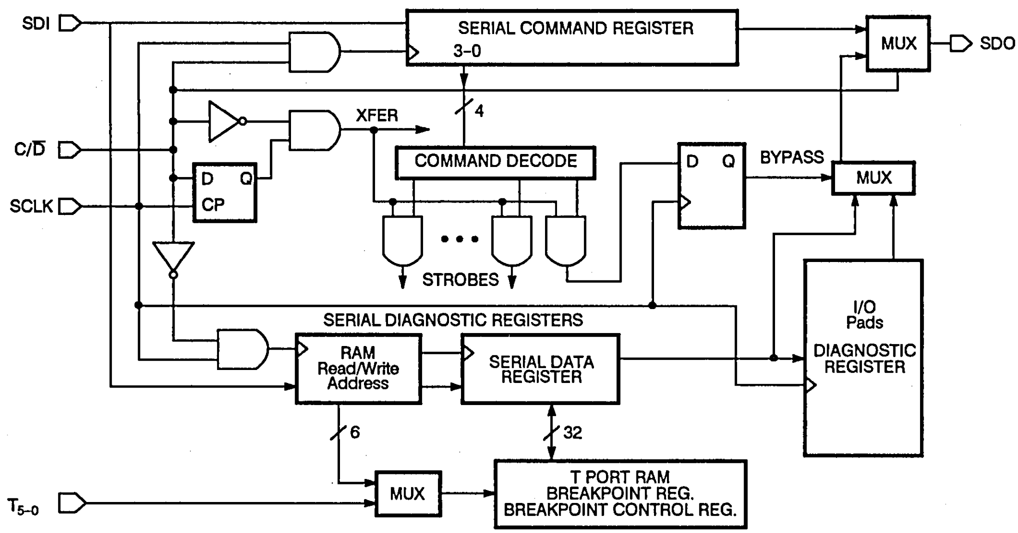


Figure 33. Internal Organization of the SPC

READING DATA

To read data from the IDT49C404's internal RAM or other logic circuitry into the Serial Data Register, the Address and Don't Care bits (for the Serial Data Register) are shifted in. The command is shifted into the Serial Command Register. The Command Register must be decoded to determine what data paths are to be steered in order to get data into the Serial Data Register. The read strobe generated by the strobe logic must then strobe this data (in parallel) into the Serial Data Register. The data can now be shifted out via the SDO pin and its contents disassembled and observed.

WRITING COMMAND/DATA

To perform the write operation, address and data must first be shifted into the Serial Data Register. The command is then entered into the Serial Command Register via the Command Phase. This register provides information as to what data paths are to be steered. The address is supplied by the Address Register in the data scan path. The write strobe is then generated between the time the C/D̄ line is lowered and the SCLK line is raised. This is the strobe which actually clocks the data into the RAM or register in the device.

I/O PAD SCAN PATH

Each I/O cell on the IDT49C404 contains a flip-flop which can be used to store the state of that cell and then be scanned out. Figure 34 shows the logic configuration. The flip-flop in the I/O cell is loaded each time an SPC command is executed via the XFER signal, thus loading the scan flip-flops in parallel. The SCLK is then used to scan the data out the SDO pin, in series with the Address and Serial Data Registers.

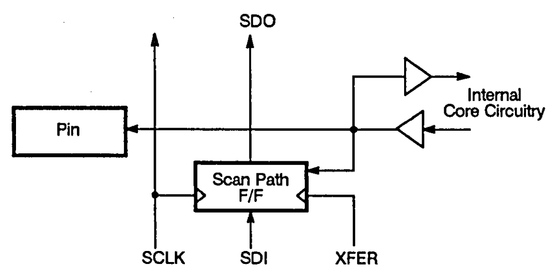


Figure 34. Serial Scan in the I/O Cell

The Set Bypass and Clear Bypass commands control a mode flip-flop which determines whether the I/O cell scan-path flip-flops are scanned out or not. The Clear Bypass command enables the scanning out of the RAM address, serial data and I/O cells. The Set Bypass command disables the scanning out of I/O cells such that only RAM address and serial data are shifted out.

SPC COMMAND OPCODES

The Serial Command Register consists of a 4-bit field as shown in Figure 35. The 4-bit command opcode field gives sixteen possible command opcodes. The first eight are reserved for writing data from the Serial Data Register into the registers and RAM on the device. The second eight opcodes are reserved for reading data from internal registers or RAM into the 32-bit Serial Data Register.

COMMAND OPCODES	
OP CODE	FUNCTION
0	Write RAM
1	Write Break Control
2	Write Break Data
3	Reserved
4	Reserved
5	Reserved
6	Set Bypass
7	Clear Bypass
8	Read RAM
9	Read Break Control
10	Read Break Data
11	View Z
12	Reserved
13	Reserved
14	Reserved
15	NOP

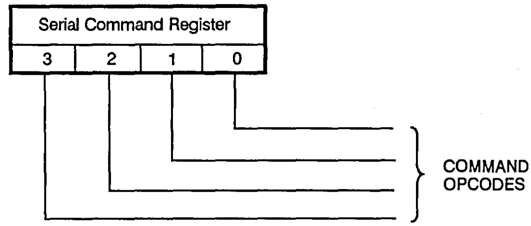


Figure 35. Serial Command Register and Opcodes

SPC COMMAND OPCODES

The Serial Command register consists of a 4-bit field shown in Figure 35. The four bit opcode gives 16 possible instructions. The first eight are for writing data from the Serial Diagnostic Register to the RAM or other register destinations. The second eight opcodes are for reading data from internal registers or the RAM into the Serial Data Register. The Serial Data Register is a 38 bit Register; 6 bits for RAM address and 32 bits for data.

Opcode 0 executes a write RAM operation. Opcode 1 is used to write to the Break Point Cmd registers. Opcodes 2 writes the Break Point Data register. Opcode 6 sets the bypass register, bypassing the I/O cells when shifting SPC data; and opcode 7 clears the bypass.

Opcode 8 reads the contents of the RAM. The RAM address is supplied by the Serial Diagnostic Register. Opcodes 9 and 10 are used for reading the Break Control Register and the Break Data Register, respectively. Opcode 11 is used to strobe data from the Z bus into the 32 bit diagnostics data register. Opcodes 12, 13 and 14 are reserved opcodes. The last opcode, 15, is a no-operation opcode. This opcode can be used to scan the data in and out of the I/O pad cells and use the device in a pass-through mode (in a cascaded application) without affecting normal device operation.

All the reserved opcodes if executed perform a no-operation, however they should not be relied upon to always perform NOPs as future upgrades may make use of reserved opcodes.

The command with Opcode 0 causes a write to the internal device RAM. Opcode 1 is used to write to the Q registers. Opcodes 2 and 3 are used to write data from the Serial Data Register into the Break Data Register and Break Control Registers, respectively. Opcodes 4 through 7 are reserved opcodes.

Opcode 8 is the first opcode used for reading data into the Diagnostics Register. It is called Read RAM. The RAM location address is supplied by the scan path in the input pad cells for the T port. The address, therefore, must be scanned in. Opcodes 9 and 10 are used for reading the Break Control Register and the Break Data Register, respectively. Opcode 11 is used to strobe data from the Z bus into the 32-bit diagnostics Data Register. Opcodes 12, 13 and 14 are reserved opcodes. The last opcode, 15, is a no-operation opcode. This opcode can be used to scan the data in and out of the I/O pad cells and use the device in a pass-through mode (in a cascaded application) without affecting normal device operation.

All the reserved opcodes if executed, perform a no-operation. However, they should not always be relied upon to perform NOPs as future upgrades may use reserved opcodes.

BREAKPOINT DETECTION CIRCUITRY

Figure 36 shows the diagnostics break point detection circuit on the IDT49C404. This circuit is designed to allow the user to monitor certain key data buses and detect the data patterns on the Z and S buses. When a data pattern is detected, a breakpoint compare signal is generated on the DCMP pin and is used to halt the system operation. The DCMP is an open drain signal and should be wire-ANDed with DCMP lines of other similar devices and monitored by the main sequencer in the system. Thus, the break point detection mechanism allows for an easier debug of microcode with regard to the data path.

BREAKPOINT DETECT MECHANISM

At the heart of the break point detection circuit is a comparator which compares data from the Break Data Register with data from either the Z bus or the S bus. The Break Control Register determines which of the two buses is selected for a comparison. The Break Control Register also steers a multiplexer at the output of the comparator. This multiplexer selects between the equal-to signal, latched-equal-to, V_{CC} or GND. The latched-equal-to input into the multiplexer gives the user the ability to pipeline the match signal, shortening the system cycle time in the diagnostics mode. The V_{CC} and GND inputs to the multiplexer allow the programmer to disable the break compare feature by forcing the DCMP pin either HIGH or LOW, respectively.

When a match is made the DCMP line goes HIGH. Thus, if any one slice in a cascade application does not match, the wire-ANDed DCMP will be LOW. Selecting GND via the multiplexer will disable matches altogether. Selecting V_{CC}, disables that particular slice from the comparison.

Figure 37 shows the format of the Break Data and Break Control Registers. The Break Data pattern is 32 bits wide, with bit 31 being the most significant bit and last to be shifted in. The Break Control Register contains three fields. Bits 0 and 1 control the DCMP output and bit 2 selects between the Z and the S bus to be compared with the Break Data Register. Bits 3 to 31 are reserved for future expansion.

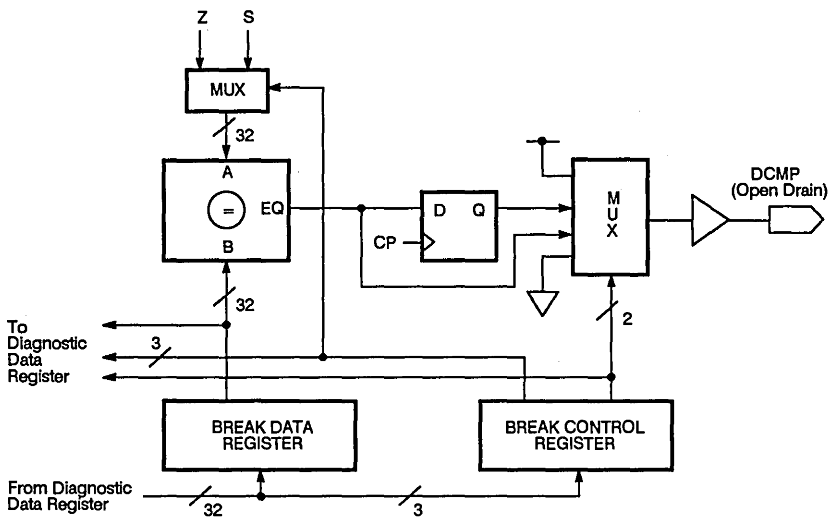
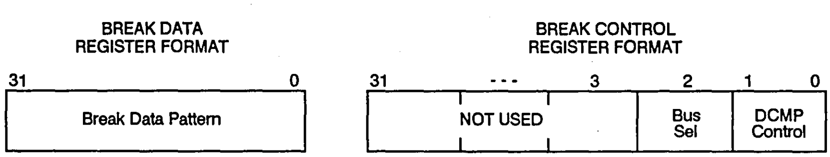


Figure 36. Breakpoint Detect Circuitry



BREAK POINT CONTROL CODES

Bus Sel	Bus
0	Z
1	S

DCMP Control		DCMP Status
0	0	LOW
0	1	Pipelined
1	0	Non-Pipelined
1	1	HIGH

Figure 37. Break-Point Control Registers and Opcodes

BASIC SPC APPLICATION

The block diagram in Figure 38 shows the Serial Protocol Channel being used with a writable control store in a microprogrammed design. The control store can be initialized through the SPC path. A register with SPC is used for the instruction register going into the IDT49C410 (16-bit microprogram sequencer), as well as data registers around the IDT49C404. In this way, the designer may use the Serial Protocol Channel to observe and modify the microcode read from the writable control store, and also observe and modify data and instructions in the system.

Access to the SPC on the user's system could be obtained using two possible approaches:

1. Interface the parallel I/O ports of a development system (such as an IBM PC or a PC-compatible) directly to the SPC lines.
2. Use a user-system processor to initiate and control the diagnostics via SPC.

When using the parallel port, the PC contains the monitor program required to generate the protocol for the SPC lines and supply the diagnostic information to the SPC hardware. This would allow the PC to be used not only as a development station, but also as a test and debugging tool. Figure 39 shows the set-up of a user's system. Microcode development is done on the host PC. The parallel interface connects the PC to the user's system via the four diagnostics pins, SDI, SDO, SCLK and C/$\overline{\text{D}}$. The monitor program would allow entering the data and addresses, exercising the commands and extracting and displaying the data from each device in the SPC ring.

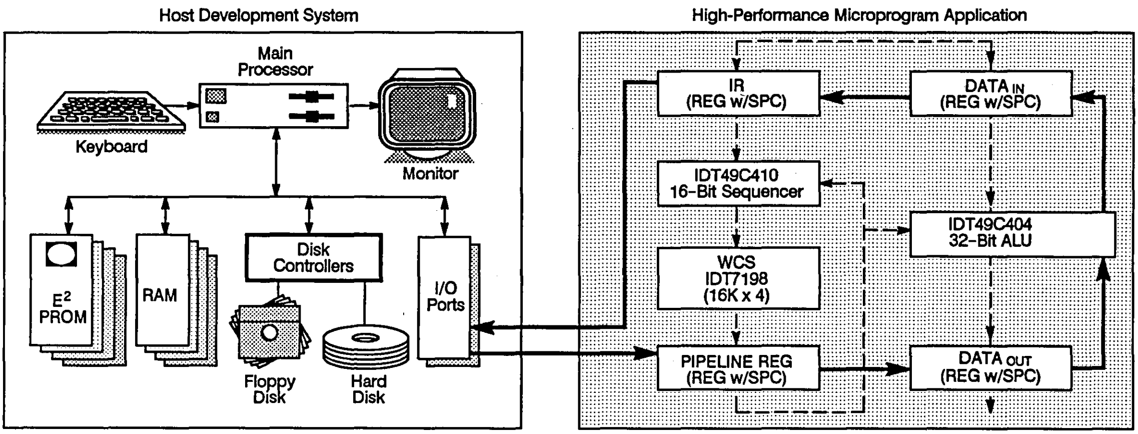


Figure 38. Typical Microprogram Application with SPC

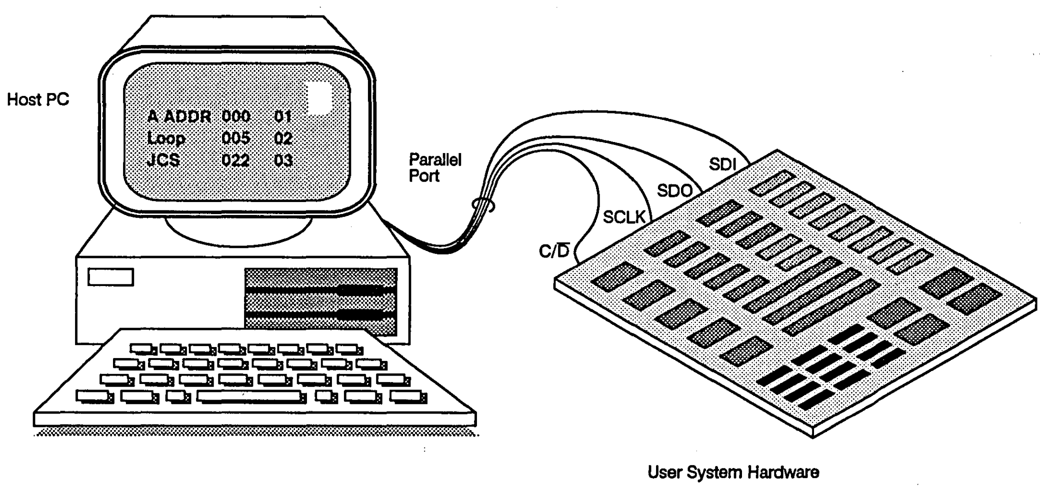


Figure 39. A PC-Based User System

Alternately, a processor on the user system could be used to generate the SPC signals and perform such functions as Writable Control Store initialize and power-up diagnostic operations. This could be the host processor or a dedicated control processor. Figure 40 shows a system where a dedicated processor is used to initialize and control the SPC diagnostic operations over the entire system.

Another method would be to use a diagnostics interface board to communicate with the SPC. To access the SPC through this interface board, the PC would serve as a host, transmitting diagnostic information directly to the user's hardware. The interface board generates the signals to operate the SPC in the user's system. The ability to be used, not only for system diagnostics but also as a debug tool, is the primary advantage of the SPC scheme.

TAKING ADVANTAGE OF DIAGNOSTICS

IDT's innovative Serial Protocol Channel has been architected in such a way that it can be easily implemented in many different applications. The cascading feature on the SPC not only allows a complete system debug and test, but specific blocks of logic can be tested by breaking the test program loop into multiple mini-loops, thus performing much tighter diagnostic checks.

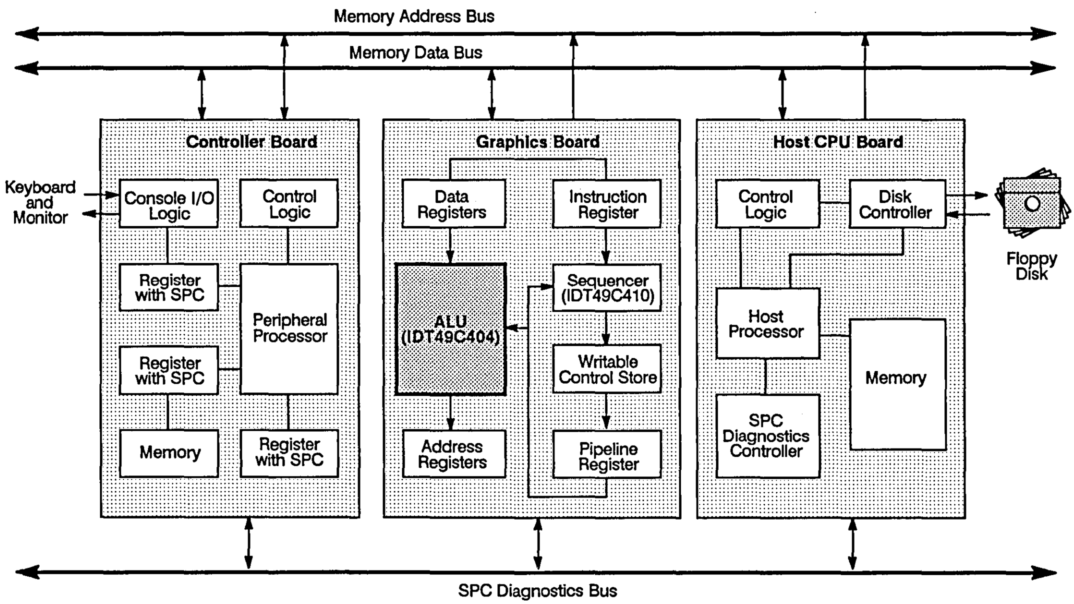


Figure 40. A Dedicated SPC Controller for a Complex Digital System

Finally, as chip technologies continue their push towards more heavily integrated VLSI architectures, IDT has responded with the right tool for enhancing and simplifying in-circuit testing and diagnostics—the **Serial Protocol Channel.**

Integrated Device Technology, Inc.

DUAL PORT RAMS WITH SEMAPHORE ARBITRATION

APPLICATION NOTE AN-14

by Michael J. Miller

INTRODUCTION

Due to their high bandwidth and message access flexibility, dual-port RAMs are used to link multiple high-performance processors and systems. Integrated Device Technology makes dual-port RAMs of many configurations, all of which consist of one RAM with two sets of address, data and control signals. This allows two processors to share the same block of physical memory in their respective address spaces. The two processors can access data in two memory locations simultaneously and asynchronously. This approach clearly outperforms a discrete parts design where two processors must synchronize through arbitration for access to a bus which is used to access one location at a time in a standard single-port RAM.

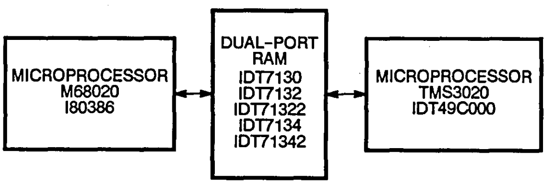


Figure 1. Dual-Port RAMs Link High-Performance Processors

IDT's dual-access approach removes synchronization requirements at the memory's bus access level. Nevertheless, synchronization must be performed at other levels to ensure data integrity and proper system operation. This application note addresses several approaches to solving the mutual exclusion problem and gives a detailed discussion of the semaphore capability provided by the IDT71322 and IDT71342.

Arbitration

Consider a multiple-processor system where each processor has access to the same data. Arbitration schemes are necessary to resolve the situation when multiple processors want the same piece of data at the same time. Different approaches to the arbitration issue have different tradeoffs and are best-suited for different applications. These solutions vary from no arbitration, hardware solutions, and software solutions, to combinations thereof.

Seemingly, the simplest solution is to employ no arbitration at all. This approach works if the application guarantees that two processors will not access the same location simultaneously or, if they do, then the indeterminate results are acceptable. Sometimes handshaking can be employed through I/O ports or interrupt mechanisms. This approach provides a high-performance, low-overhead design but is restricted to certain applications. If arbitration is not required, the IDT7134 can be used. It is a 4K x 8 dual-port RAM with no arbitration. This part can also be used in large dual-port designs where one hardware arbiter is used for a whole array composed of many IDT7134s. The interrupt handshake mechanism can be achieved by using the IDT7130/7140.

Most applications cannot sacrifice data integrity and utilize the dual-port memory as a collection of individual memory locations which require a finite access time. In this case, arbitration at memory location resolution is required. The IDT7130/7132 use an address comparison mechanism which provides a $\overline{\text{BUSY}}$ signal at both sides. When the two processors try to access the very same location, the arbitration asserts the $\overline{\text{BUSY}}$ signal to the processor which attempted access last. When access attempts are within 5ns of each other, a side is chosen arbitrarily. The $\overline{\text{BUSY}}$ outputs are suitable for attachment to the READY inputs of most microprocessors. This approach is very straightforward and flexible and has the benefit that a processor cannot be locked out of the RAM longer than the access period of the other processor.

The features of the IDT7130/7132 that make them a superb solution in many designs may create problems in other applications. The fact that $\overline{\text{BUSY}}$ lines are used and that arbitration resolution is at the level of individual locations can be a major limitation in some instances. Many significant controllers, such as the 8031 and 8051, are not equipped with READY input pins. Of those that are equipped, a penalty is often paid in the higher performance versions if they require "seeing" the $\overline{\text{BUSY}}$ signal faster than the IDT7130/7132 can supply it (16MHz 68020 requires 25ns $\overline{\text{AS}}$ to DSACK). In these cases, wasteful wait cycles are required. In other applications, software constraints may require mutual exclusion at the software data structure level rather than at the memory cell location level. For this reason, Integrated Device Technology developed the IDT71342 and IDT71322.

Instead of comparing addresses on every cycle, and occasionally asserting $\overline{\text{BUSY}}$ status, the IDT71342 and IDT71322 employ circuitry to support a software mechanism called semaphores. Here, every memory cycle is equally as short as the next and arbitration is handled at the software level.

The semaphore concept was pioneered by E.N. Dijkstra in 1968. He developed a test and set approach for single processor multi-tasking systems. The task tests a memory location (a semaphore) for a particular value and, on the next cycle, the task sets the same location a unique value. If the semaphore was already set, then the current task knows that another task has access. If the value was not present, then the task knows that it has permission to proceed and all other tasks are blocked because the semaphore is not set. Only one task at a time has permission via the semaphore. Semaphores are used like locks to resources such as disk buffers, message queues, critical code sections, shared access to communication controllers, etc.

Because the test and set operation requires that the two memory accesses are indivisible in time, the IDT7130/7132 will not support semaphores for many processors and systems. This occurs because one processor may test the semaphore and, before it can set it, the other processor might test it, too. In this case, both processors "believe" they have the semaphore. The IDT71342/71322 employs a twist by using set and test. The "set" corresponds to a request and the "test" checks to see if the request was granted. The indivisible double access requirement is avoided because, as soon as a request is made by one processor on one side, the grant

14

is blocked on the other side. Some processors support test and set operations through a read/modify/write operation, but the memory bus design must support the processor in such a way that the address and the chip select remain constant. When the test and set instruction is used, arbitration must take place. As will be seen, semaphore operation without hardware busy arbitration has many advantages.

The IDT semaphore scheme employs a software/hardware approach which provides a secure method of resource allocation with the flexibility of software configuration and control and the resolution of hardware. Since there is no hardware relationship between semaphores and dual-port memory locations, the block sizes, locations and semaphore association are defined by the software. The semaphores can also be used to allocate other resources such as I/O devices. This offers the system designer considerable flexibility.

As an example, dual-port RAM might be shared by a disk controller processor and a host processor. When the controller is accessing a buffer in memory (e.g. when writing a sector in a track), the main processor cannot be allowed to interrupt or delay the controller. By setting the semaphore, the controller has exclusive access to the disk buffer. When done,it releases the semaphore and therefore provides access to the disk buffer by the processor on the other side.

Because the processors must test and set a semaphore with multiple bus cycles, the semaphore arbitration scheme has a longer arbitration latency than the address comparison scheme. Since arbitration is most often used for access to multiple locations in memory the overhead can be amortized across multiple accesses. In systems that require mutual exclusion of access to data structures over a period longer than one memory cycle, this tradeoff is irrelevant.

Functional Description of the IDT71342/71322

The IDT71342 is a fast dual-port 4K x 8 CMOS static RAM with semaphore logic, packaged in a 52-pin PLCC and LCC. The IDT71322 is a 2K x 8 dual-port packaged in a 48-pin DIP and a 52-pin PLCC/LCC. The semaphore logic can be used to allocate portions of the dual-port RAM to one side or the other and is used in place of the address arbitration logic used in other dual-port designs. Semaphores are software-controlled. Therefore, this approach provides several advantages including allocation of multiple blocks of arbitrary size and no processor WAIT states or $\overline{BUSY}$ logic.

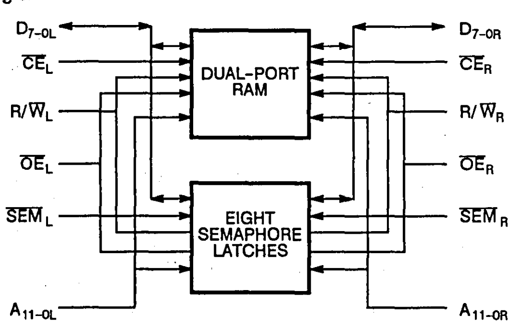


Figure 2. Functional Block Diagram of Dual-Port RAM with Semaphores

Like other IDT dual-port RAMs, the IDT71342/71322 allow access to a common set of RAM cells from two independent ports. Each port is functionally identical to that of a conventional static RAM. Both ports are completely independent and asynchronous in operation. Reading or writing on one port does not affect the operation or timing of read/write operations on the other port. Unlike the IDT7130/7132, the IDT71342/71322 do not employ hardware arbitration which blocks write access. If one port is writing to a location while the other port is reading that same location, the data will change during the read. If both ports attempt to write to the same location at the same time, the result will be some combination of the two data words being written. If both ports are reading, however, there is no interaction because the data does not change.

How the Semaphore Flags Work

The semaphore logic is provided by a set of eight latches. These latches can be used to pass a flag, or token, from one port to the other to indicate that a block of RAM is in use. The internal circuitry prevents the flag from being passed in both directions at the same time. The semaphores provide a hardware assist for a use-assignment method called "token passing allocation". In this method, the state of the semaphore latch is used as a token indicating that a block of RAM is in use. If the processor on the L port wants to use a block of RAM, it attempts to set the latch, requesting the token. The processor then checks the latch to see if it was successful in setting the semaphore. If it was, the processor proceeds to read and/or write in the block. If the processor was not successful in setting the latch, it means that the R port had set if first, has the token and is using the block. The L port then continues to test until it is successful, indicating that the R port has released the token and is no longer using the block.

The semaphore logic is independent of the dual-port RAM. These eight latches can be accessed from either port by enabling the semaphore chip enable ($\overline{SEM}$ = LOW), which is separate from the RAM chip enable. When the semaphore logic is enabled on a port, one of the eight latches can be read or written from that port. The latch is selected by the three least significant address pins for the port and the data for reading and writing uses the D_0 data pin.

A semaphore latch is read or written in the same manner as a RAM cell. The latch is written to a "1" or "0" by activating the semaphore logic enable, selecting the latch with the three least significant address bits, activating the write enable and putting a "1" or "0", respectively, on the D_0 data pin. The latch may be read by activating the semaphore enable, selecting the latch, holding the write enable high and reading the data on D_0. For the user's convenience, all eight of the data lines are set to the same value as D_0 during read. In other words, the data lines will contain all "1"s or all "0"s when D_0 is a "1" or a "0", respectively. In this way, branch zero testing can be employed.

The semaphore read logic latches the readout state of the semaphore flag during the read. This prevents the value seen by the reading port from changing during the read, even though the state of the latch may be changing internally due to write activity on the other port. The latch goes into the hold mode when both semaphore enable and output enable are active. In order to see the latch change, either the semaphore enable or output enable must be disabled, and then enabled. This means that read operations must be cyclic; it is not possible to enable the semaphore and output enable continuously and wait for the latch value being read to change.

The semaphore logic is active low. An access token is requested by writing a "0" to the semaphore latch and is released by writing a "1". To request a token, an attempt to write a "0" to the semaphore is made and the semaphore is read to determine if the "0" was successfully written. If a "0" is read, the token request was granted. If a "1" is read, the request was denied and the other port has the token.

The critical case of semaphore timing occurs when both ports request the token by writing a "0" at the same time. The semaphore logic is specially designed to resolve this problem – if requests are made simultaneously, the logic guarantees that only one side receives the token. In this case, the token assignment will be made arbitrarily to one port or the other.

Figure 2 shows the internal logic circuitry for one semaphore "latch" cell. It is composed of multiple latches and cross-coupled AND gates which serve as an arbiter to guarantee that only one side at a time receives a grant signal. A typical sequence of semaphore operations is listed in Table 1. The Do columns represent the logic value that would be read on that side. The "Request F/F"s are the internal flip-flops which store the state of requests.

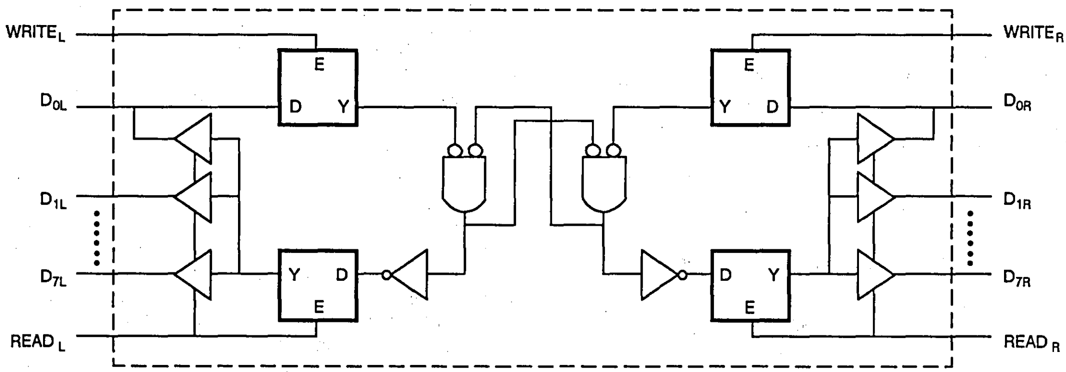


Figure 3. Simplified Diagram of One Semaphore Cell

Function	Left DO	Left Request F/F	Right Request F/F	Right DO	Status
No action	1	1	1	1	Semaphore free
L port writes 0	0	0	1	1	L port has token
R port writes 0	0	0	0	1	No change; L port keeps token
L port writes 1	1	1	0	0	Semaphore freed: R port gets it
R port writes 1	1	1	1	1	Semaphore free
L port writes 0	0	0	1	1	L port has token
L port writes 1	1	1	1	1	Semaphore free

Table 1. Semaphore Function Table

Use of Semaphores

Semaphores provide useful solutions for various problems at both the hardware and software levels. The following selections highlight a few of the semaphore benefits which range from increasing performance to providing functionality not available with other designs.

High-Performance Dual-Port Design

To gain a deeper understanding of the trade-offs between semaphore and non-semaphore dual-port RAM designs, the following example compares both approaches. Dual-port memory system design requires a key awareness of the microprocessor's memory access time requirements. Figure 3 is a read cycle timing diagram of a 20MHz 68020. Two timings are critical: A 45ns address to data size acknowledge ($\overline{DSACK}$) to guarantee no wait states and a 95ns address to data. It is also important to examine a typical design. Figure 4 shows the interface between a single processor and one side of the dual-port. For simplification, the other port interface was omitted from the drawing. This example shows the address bus which is decoded by a comparator (IDT74FCT521A) and an address decoder (IDT74FCT138A). The address interface chooses which dual-port RAM to enable. After the chip select is enabled, chip select address arbitration (only on the IDT7130/7132) and data access can begin.

14

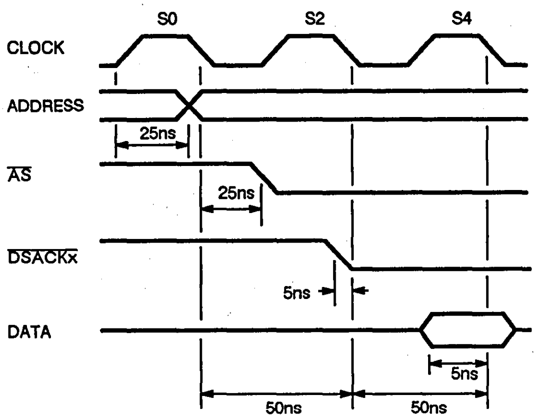
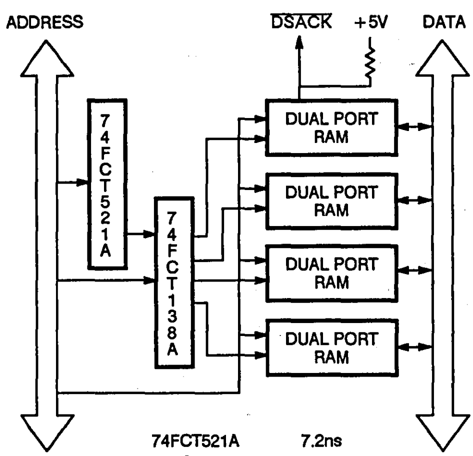


Figure 4. Read Cycle Timing for 20Mhz 68020



74FCT521A	7.2ns
74FCT138A	5.8ns
ADDRESS TO $\overline{CS}$ =	13ns

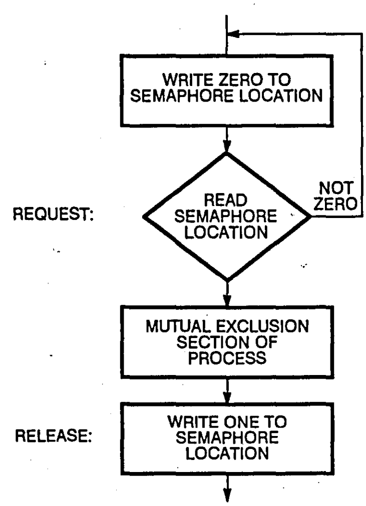
Figure 5. Memory Interface to One Port of a Dual-Port RAM System

In a tightly-coupled system (i.e., the 68020 processor and dual-port are on the same board), chip select can be generated from address in 13ns. In the best case, the data acknowledge is tied to the 68020 through a NAND gate (to include other acknowledges). The NAND gate will introduce another 5ns delay. This leaves 26.9ns to generate the acknowledge ($\overline{DSACK}$) and meet the 5ns setup time to guarantee that a wait state will not be inserted. In a less rigorous design where the dual-port and CPU are on separate boards, 10ns or more may be required for on/off board buffers and bus delay, etc. This leaves 16ns or less to generate acknowledge.

Considering the timing constraints, the designer can choose from several options. In applications which require arbitration resolution to the memory cell level, 26.9ns is not enough time to generate $\overline{DSACK}$ from $\overline{CS}$ using the IDT7130L55. One solution involves adding logic to the $\overline{BUSY}$/$\overline{DSACK}$ path so that a wait state is always inserted until the dual-port can respond with $\overline{BUSY}$. This will slow down the system whenever the dual-port is accessed. If block arbitration or higher memory cycle performance are required, the designer should utilize the IDT71342/71322. This configuration would only be constrained to the 95ns address to data access time, minus any address and data buffer time. The IDT71342/71322 provides high enough performance for use with the 25MHz 68020. Some software overhead is required for semaphore access but, given the fact that the semaphore arbitration is for a block of locations, the arbitration latency can be amortized across multiple higher speed accesses. Consequently, the semaphore approach provides a higher performance solution if block arbitration is desirable or acceptable.

A Software View of Semaphores

The dictionary defines semaphore as "signaling by flags." A semaphore is implemented as a specialized type of memory location which can be accessed by either processor in a dual-port design. Two different operations are performed on the semaphore: the request operation which attempts to gain access and the release operation which signals the termination of access. These operations are used to guarantee mutual exclusion, meaning that only one processor is accessing a resource at any given time. This occurs from the time a request is granted until the time that the semaphore is released.



Flow Chart 1. Sequence of Operations on Semaphore to Guarantee Mutual Exclusion

A semaphore is chosen which both processors associate with one resource. First the processor requests the semaphore by attempting to write a "0" to the semaphore location. Then it reads the location. If it receives a non-zero value (i.e. a "1"), it loops back and reads the semaphore location again. It will continue to read the location until it receives a "0". The software may be written in such a way that useful work may be performed while waiting. When a "0" is read, the processor can access the resource for as long, and as many times, as desired. The processor must release the semaphore when it is finished with the resource. This is achieved by writing a "1" to the semaphore location.

Using Semaphores at the Software Level

One example of where semaphores might be applied involves two processors working together to generate a video display for animated images. The "MASTER" processor generates a picture layout in the form of a display list. The "SLAVE" processor reads the display list, interprets it and generates an image in a display buffer. As the image is displayed, the video buffer is cleared. The displayed list is re-interpreted and displayed. If the display list is changed, the image appears as though it has moved, giving the illusion of animation.

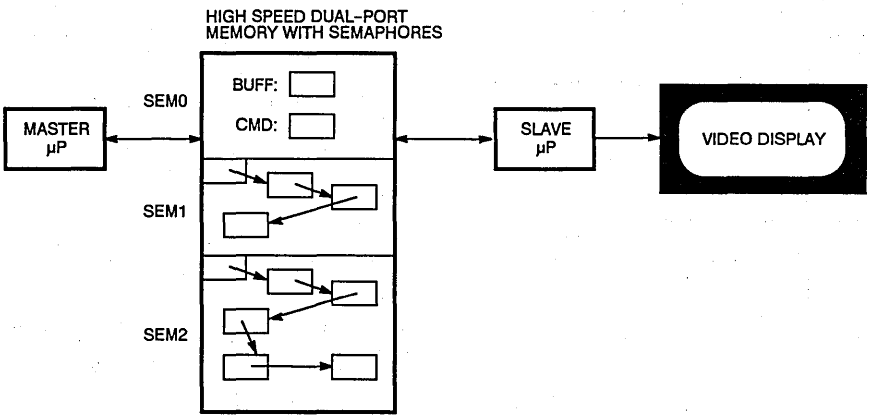


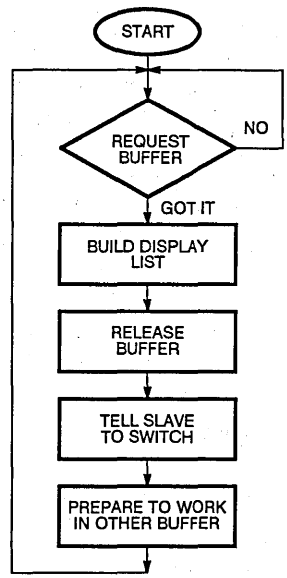
Figure 5. Software Block Diagram of Video Display System for Animation

A dual-port RAM is used to store the display list. The SLAVE interprets one display list repeatedly to generate the display buffer image, while the MASTER generates and updates another display list. The SLAVE processor continuously updates the video display buffer since the buffer is wiped clean when its contents are dumped to the video screen.

In this particular application, the dual-port RAM is broken up into three areas. The first area contains common information concerning which display list is being accessed and which one is being updated. It is locked with the semaphore SEM0. Two buffers comprise the other areas and are locked by semaphores SEM1 and SEM2. At any given time one buffer is used for the display list currently being interpreted and the other is used for the list being built. The common area stores the pointer which indicates which buffer is being updated.

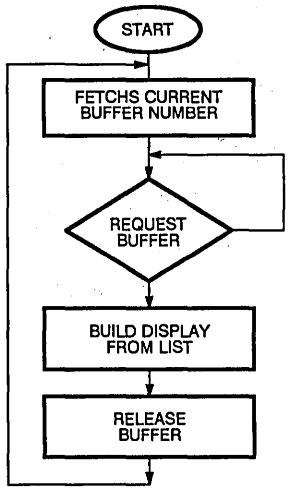
The key to the effectiveness of this approach lies at the software level. The flow chart for the master processor begins with a buffer request via a semaphore. Once granted, it builds a display list. Then it releases the buffer through the semaphore mechanism. Next it calls a routine to inform the SLAVE processor to switch over to the new buffer. It then loops back to request access to the other buffer.

The SLAVE processor functions by first fetching the current buffer/number. Then it requests the buffer via the semaphore mechanism (involving SEM1 or SEM2). Once the SLAVE gains access to the buffer, it builds the display from the list. After releasing the buffer, it goes back to fetching the current buffer/number. This is necessary because the MASTER processor may have switched buffers. Fetching the current buffer/number requires access to the common area which is achieved by obtaining the semaphore SEM0. After accessing the data, the SLAVE releases SEM0 which allows the MASTER to come in and update the common area.



Flow Chart 2. Sequence of Operations for Master Processor

14

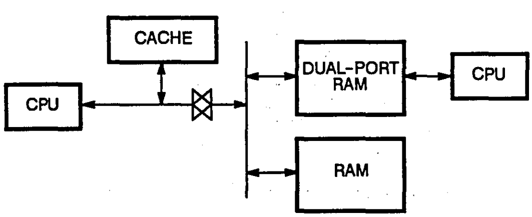


Flow Chart 3. Sequence of Operations for Slave Processor

The software code for the MASTER and SLAVE processors is listed on the following pages. It is in the form of a pseudo-"C" language-type program. The request for a semaphore is made by the WHILE statements accessing a variable called SEM. The semaphore is released by writing a "1" to that variable.

Semaphores and Caches

In high-performance dual-port systems, semaphores can be used with caches to achieve valid data synchronization. The use of caches is an established method of speeding up access between a processor and main memory. Main memory may be slower due to the use of lower cost, higher density DRAMs or system bus latency. The cache operates by monitoring data transfer between the processor and memory. When write operations are performed, the cache remembers the data and location. When a read is performed it compares the address of the request with a list of locations it has data for. If the address matches, the cache supplies the data and aborts the main memory access. If no match occurs, the cache allows the main memory access to proceed and notes the data and location.



Flow Chart 7. Dual-Port RAM in a Cached Memory Environment

One might first assume that the dual-port RAM can always be used with cached memory accesses. However, extra considerations must be made. When data is written to a memory location in dual-port RAM, the cache stores the acquired value and its associated location. The next time that location is read, the cache will register a "match" and bypass reading from the location in dual-port RAM. This might result in an error if a processor on the other port has written new data to the location.

One way to remedy the situation is to put the dual-port RAM into non-cached I/O address space and block data transfer between the dual-port RAM and cached address space where standard RAM exists. To make this approach work, semaphores must be employed to lock a buffer in the dual-port RAM while the data is in the cached RAM. In this way a "check out" procedure can be implemented to ensure data integrity. The semaphore latches must be addressed through non-cached I/O space in order for the request and release mechanism to function correctly.

CONCLUSION

There are a number of ways to handle dual-port RAM arbitration. Choice of the most efficient technique concerns what granularity of address arbitration is required, whether a processor must be locked out of a block of memory for multiple accesses from the other processor and what constraints are imposed by the memory access cycle timing. Semaphores provide an alternative which can result in higher performance systems and provide functions which are not otherwise achievable. The following is a quick summary.

No Busy Logic—Some applications guarantee by definition that the two processors will not access the same locations simultaneously or, if they do, it doesn't matter. The IDT7134 is also ideal for use in large dual-port designs where one arbiter is used for an array of dual-port devices.

Interrupt Logic—Interrupt logic provides a signaling method from one processor to the other to provide a mechanism for handshaking.

Hardware Busy Logic—Hardware busy logic provides the lowest latency overhead when accessing multiple individual unrelated memory locations. The **MASTER/SLAVE** concept was introduced over two years ago by IDT to provide a single arbiter—thus avoiding deadlocks encountered with multiple arbiters—when using more than one dual-port in wide bus applications.

Semaphore Logic—Semaphore logic provides the best overhead tradeoff when accessing a block of data comprised of multiple related locations. This facility may also be required in high-performance applications where one of the processors does not have a ready/busy input or the overhead of wait states cannot be tolerated.

Semaphores provide a mechanism for one processor to bar the other processor from seeing an incomplete update of a block of data. This is achieved through a software mechanism supported by on-chip circuitry which provides a test and set facility that arbitrates between simultaneous requests.

CODE FOR MASTER PROCESSOR

```
MAIN    ( )        {
          /*        code to initialize */

        FOREVER    {
              SEM (CUR_BUF):= 0
              UNTIL (SEM (CUR_BUF)  = 0);          /*request */
              BUILD_DISPLAY (CUR_BUFF);            /*Build new display list*/
              SEM (CUR_BUFF):= 1                   /*release */
              SWITCH_BUFF (CUR_BUFF);
              IF (CUR -= BUFF = 1)
                    CUR_BUFF:= 2;
              else  CUR_BUFF:= 1;
              }
        }                                          /*end MAIN*/

SWITCH_BUFF (NBUFF) {
        SEMO:= 0
        UNTIL (SEMO = 0);   /*request*/
        BUFF:= NBUFF;
        CMD:= NEW;
        SEM:= 1;                      /*release*/
        RETURN (  )
        }
```

CODE FOR SLAVE PROCESSOR

```
MAIN ( )    {
        FOREVER    {
              CUR_BUFF:= FETCH_BUFF ( );
              PROCESS (CUR_BUFF);
               }
        }

FETCH_BUFF ( )    {
        SEM 0:= 0;
        UNTIL (SEMO = 0);                   /*request*/
        A BUFF:= BUFF;
        CMD:= OLD;
        RETURN (ABUFF);
        SEMO:= 1;                           /*release*/
        }

PROCESS (BUFF)    {
        SEM (BUFF):= 0;
        UNTIL (SEM (BUFF)  = 0);            /*request*/
              REFRESH (BUFF):         /*code to refresh display*/
        SEM (BUFF):= 1;                     /*release*/
        }
```

14

Integrated Device Technology, Inc.

USING HIGH-SPEED SERIAL-PARALLEL FIFOS THE IDT72103/72104

APPLICATION NOTE AN-15

By Robert Stodieck

INTRODUCTION

FIFOs are a common hardware solution in designs where data must be transferred between two subsystems with different characteristic data generation, transfer or usage rates. A common case is the serialization and de-serialization of data. Serialization is required for a variety of applications such as communication, data storage and display. The IDT72103 and IDT72104 parallel-serial FIFOs have been designed to address these applications.

The IDT72103/4 FIFOs are a RAM-based design with self-incrementing internal read and write pointers. This design results in very low fall-through times compared to older FIFO designs that are based on ganged shift registers. The fall-through time of a FIFO is the time elapsing between the end of the first write to the FIFO and the time the first read may begin. The first byte of data written into the IDT72103/4 FIFOs is available as soon as the write is complete and the Empty Flag is consequently de-asserted.

Similarly, the serial registers are not shift registers but bit wide memory arrays with self-incrementing pointers. The serial output word and the serial input word transfer data starting from the least significant bit. If only a partial word is transferred into the serial input register, the bits will be in the correct bit location in the serial input register and not shifted right or left.

PARALLEL OPERATING CONSIDERATIONS

Regardless of how a FIFO is designed or used, FIFO full and empty boundary conditions require special consideration from the system designer. FIFO reads and writes may occur completely asynchronously from each other unless the FIFO is completely full or empty. What happens when excess reads or writes occur after the FIFO is full or empty depends on the design of the particular device. If a FIFO is empty, then reading the FIFO again will produce data which is out of sequence or invalid. If the FIFO is full, writing data overwrites previously written data or loses the data being written.

The design of the IDT72103/4 FIFOs gates out write pulses once the FIFO is full and gates out read pulses once the FIFO is empty. Excess writes are ignored and thus do not overwrite valid data. Excess reads produce invalid data since the outputs of the FIFO are tri-stated when the Empty Flag is active, but do not read data bytes out of sequence.

The Full and Empty Flags signal the full and empty boundary conditions. An internal read cycle cannot begin until the Empty Flag is de-asserted and a write cannot begin until the Full Flag is de-asserted (Figure 1).

If the read signal is low prior to the de-assertion of the Empty Flag or the write signal is low prior to the de-assertion of the Full Flag, they cannot be allowed to transit high again until an appropriate minimum read or write pulse time has elapsed.

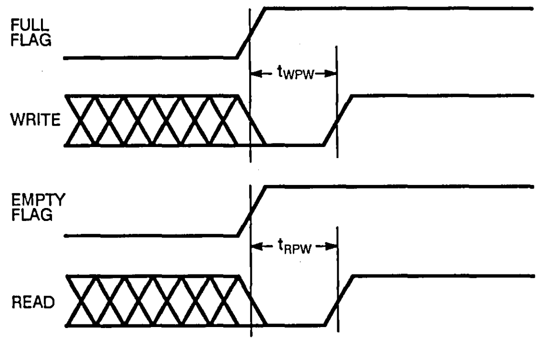


Figure 1. Parallel Read and Write Timing Following the De-Assertion of the Full and Empty Flags

Failure to observe this boundary condition timing produces internal read and write pulses of excessively short duration and may result in erratic operation.

The IDT72103/4 provide a full complement of flags which do not interact with the read and write signals. These provide the designer with flexible FIFO status indicators. They include, Empty + 1, Full - 1, Half-Full and Almost-Empty/Full. The Almost-Empty/Full Flag is asserted when the FIFO is less than 1/8th full and again when it is greater than 7/8th full.

The IDT72103/4 FIFOs can be expanded in depth to any level by cascading multiple devices. For depth expansion, the input and output buses are connected in parallel. The expansion output (XO) pin of the first part is connected to the expansion input (XI) pin of the next device in the cascade until all the parts are connected in a loop (Figure 2). The First-Load pin of one of the parts is tied to ground to identify it as the first device to be loaded in the cascade. All other parts have the First-Load pin tied to V_{CC}. The retransmit feature cannot be used in the depth expansion mode.

Empty Flag and Full Flag signals for the depth expanded cascade are derived from the individual FIFO Empty and Full Flag signals by logically ORing them together. The retransmit feature and the flags other than Empty and Full cannot be used in the depth expansion mode.

The IDT72103/4 FIFOs' retransmit feature allows data written to the FIFO one time to be read any number of times. The retransmit feature resets the read pointer to begin re-reading data from the first byte that was written after a reset pulse. This is particularly useful for applications such a video frame buffers which are written once and read many times.

Printed in the U.S.A. 8/87

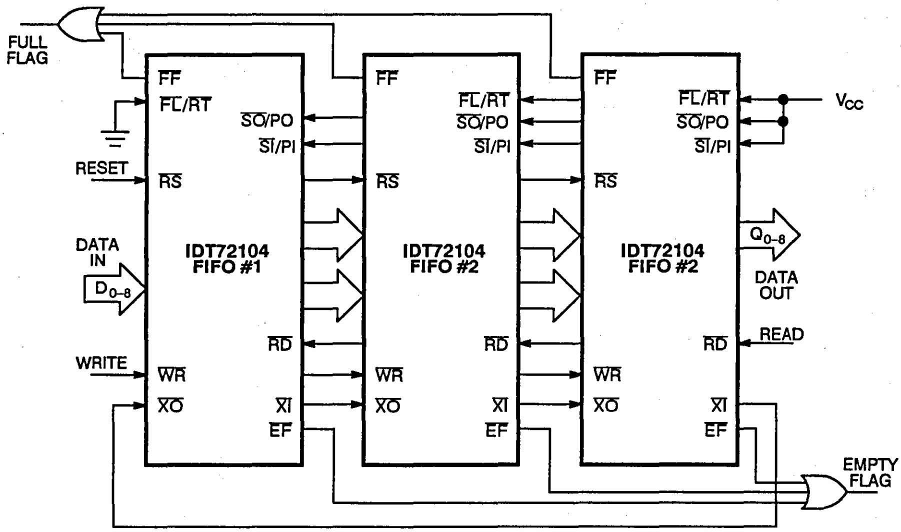


Figure 2. Parallel Depth Expansion to 12 Kilobytes

SERIAL TRANSFER AND EXPANSION – FLEXISHIFT™

The serial registers are bit wide memory arrays. Both serial width and serial depth expansion are facilitated by connecting the serial inputs and outputs in parallel. The serial output of an individual device is tri-stated when it is not active. Which serial input and serial output is active at a given moment is controlled through the expansion pins SOX (Serial Output Expansion), SIX (Serial Input Expansion), XO (Expansion Output) and XI (Expansion Input). Whether in an expansion mode or not, serial transfers always begin from the least significant bit.

The serial word width of the IDT72103/4 FIFOs may be programmed to be from four to any number of bits by using multiple parts (Figures 3 and 4). When used in the serial mode, the unused parallel input pins, D_0-D_8, and the unused parallel output pins, Q_0-Q_8, are used to output information on the status of the serial transfer (Figure 5).

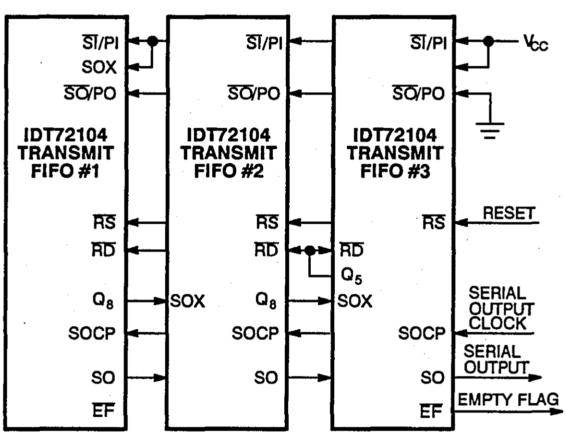


Figure 3. Serial Output Width Expansion to 24 Bits

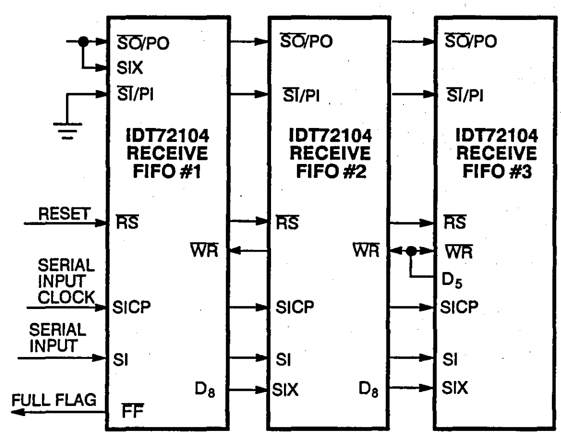


Figure 4. Serial Input Width Expansion to 24 Bits

14

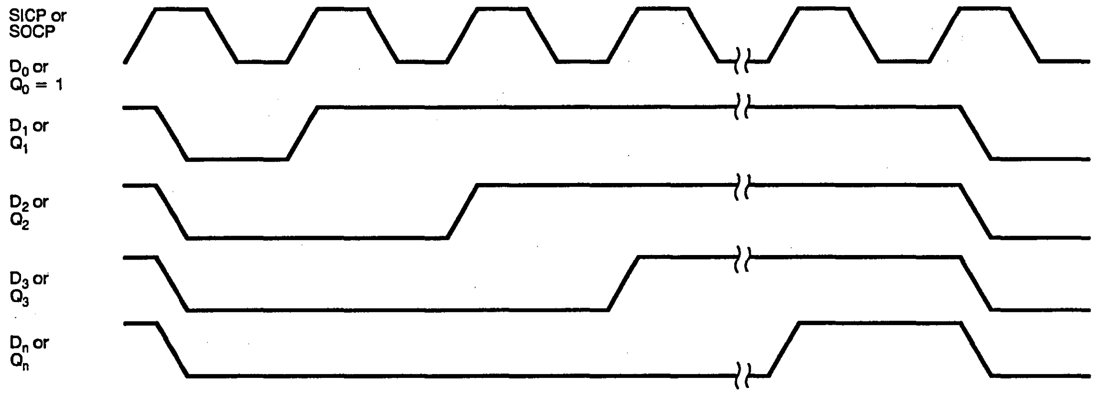


Figure 5. Parallel Pin Output Signals When In Serial Mode

These signals are used to trigger the reading and writing of data words to and from the FIFO registers and allow us to program the serial word width. These signals may also be used to drive related external logic. The minimum serial word width that may be programmed is 4 bits. Because D_0-D_8 and Q_0-Q_8 are simple outputs when the part is being used in the serial mode, they must not be bused together when in this mode.

The serial output word width is programmed by connecting the read line to the Q pin numbered one less than the word width required. The serial input word width is programmed by connecting the write line to the D pin numbered one less than the word width required. When multiple parts are used to expand the word width beyond 9 bits, this pattern continues over to the next part in sequence. In Figures 3 and 4, the word width has been programmed to nine plus nine plus six, or twenty-four bits.

On the serial input side, the SIX input of a FIFO that will sink higher order bits is tied to the D_8 pin of the FIFO which will sink lower order bits. The SIX input of the part to receive the lowest order bits is tied to V_{CC}. Likewise, on the serial output side, the SOX input of a FIFO that will source higher order bits is tied to the Q_8 pin of the FIFO which will source the lower order bits. The SOX input of the part to receive the lowest order bits is tied to V_{CC}. The serial expansion inputs SIX and SOX should not be used by external logic.

HARDWARE DESIGN

It is important to remember that FIFOs are state machines with internal logic being clocked by the read, write and expansion inputs. These control lines are high frequency clock lines and must be treated as such by the designer. It is important that these signals be clean, glitch free and reflection free.

With fast logic types and long traces it may be desirable to terminate the control signal lines to reduce ringing. A 20 to 50 Ohm series resistor placed close to the driving outputs may help balance the impedance of the output driver to the transmission impedance of the line and thus reduce ringing. Unused FIFO inputs must always be tied to V_{CC} or ground. When cascading the FIFO in depth or width, the expansion lines XI, XO, SIX and SOX should be as short as possible. If they are long, termination of these lines may also be required.

The designer must take care not to inadvertently design noise into these signals. For example, a designer may choose to strobe the read and write lines with a 74138 decoder. Since the inputs to the decoder never arrive at precisely the same time, the outputs may sequence through a number of transient states before settling. The result is a random number of very fine glitches (decoder glitches) on the outputs and, thus, the read and write signal lines. Since the logic is quite fast, the glitches may be very narrow and difficult or impossible to find with a logic analyzer.

HIGH-SPEED SERIAL LINK USING THE IDT72103/4

To minimize the CPU time associated with excessive task switching when transferring data, the ideal communications link appears to the processor as a range of memory addresses (dual-port memory) or an address that can be repeatedly read or written without corrupting data (FIFO).

If a serial link is required between two systems, a simple system using two parallel-serial FIFOs may provide a straightforward solution. If it is required, data word widths can be adjusted in the process. For example, data being transferred from a 32-bit processor can be folded to 16-bit words when moving through the FIFO serial link for use by a 16-bit CPU receiving the data. In this FIFO-serial link, data written to the transmitting FIFO is automatically transferred to the receiving FIFO as quickly as the hardware allows. The FIFO-serial link appears to the two systems as a virtual FIFO. The two communicating systems need only respond to the Empty or Full Flags of their respective local FIFOs.

In parallel I/O mode, the fall-through time of the IDT72103/4 is very small. The fall-through time of the FIFO-serial link is dedicated by the serial transfer rate and the serial word width. The serial data transfer rate may be limited by the characteristics of the serial channel or by the upper limit imposed by the FIFO logic.

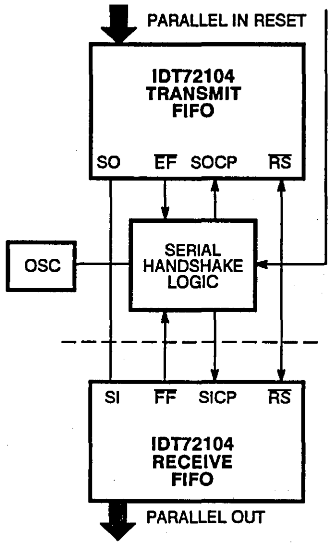


Figure 6. Serial Link Using Two IDT72104 FIFOs

SERIAL LINK OPERATION

For the purpose of illustration, a partial schematic of the serial handshake logic is shown in Figure 7. Operation of the serial link requires logic to pause the clock signals when the transmitting FIFO is empty or when the receiving FIFO is full and to restart the serial clock when the FIFOs are again ready for transfers.

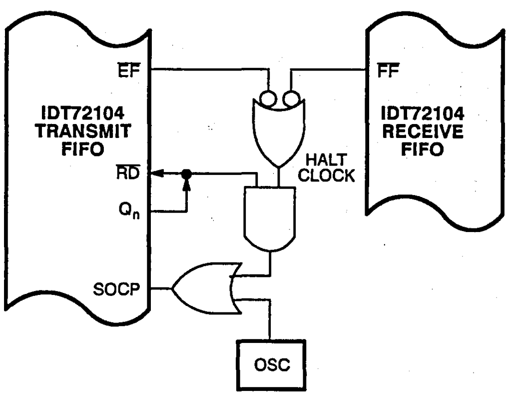


Figure 7. Partial Clock Enable Logic

The clock signals to the FIFOs are paused when the transmitter's Empty Flag or the receiver's Full Flag is asserted. The clock signals are re-started and serial transfer begins again when the Full and Empty flags are both de-asserted. Since the Empty and Full flags are both asserted after clocking the first bit of the last word to be transferred, the logic must also allow the last word to be transferred entirely before it de-asserts the clock enable signals. This is done by delaying the disabling of the clock signals until the read signal of the transmitting FIFO goes high. This signals to the handshake logic that the last bit of the serial transfer has been completed. The clock signal is then disabled in a high state. When both the transmitter's Empty Flag and the receiver's Full Flag are de-asserted, the serial clock signals are enabled again.

A complete schematic is shown in Figure 8. The logic is essentially the same as that in Figure 6, but includes provisions for synchronization to the serial clock and system reset. An IDT74FCT374A is used as array of clocked D-type flip-flops for synchronization of the handshake logic to the serial clock. Since the de-assertion of the Empty and Full flags is asynchronous to the serial transfer clock, logic is required to resolve metastability resulting from clock edge coincident transitions of the "HALT

14

CLOCK" signal. This is done by clocking the signal through stages of clocked D flip-flops.

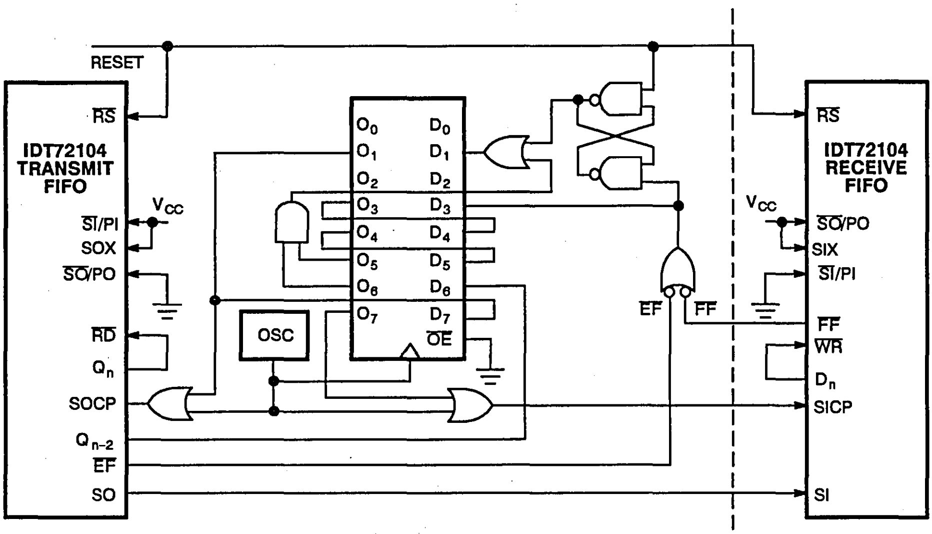


Figure 8. Serial Handshake Logic

The serial output clock must be one clock pulse ahead of the serial input clock. This is due to the fact that the FIFO serial output does not output the first bit until after the first positive output clock edge. Until this time, the output is in a high impedance state. On the other hand, the FIFO serial input inputs the first bit on the first serial input clock edge. To accomplish the necessary one clock cycle delay, the clock enable signal is clocked through one extra D flip-flop before it affects the serial input clock signal.

Reset of the serial handshake logic occurs automatically. The "HALT CLOCK" signal is asserted a few serial clock pulses after the transmitting FIFO's Empty Flag is asserted during reset. The cross coupled NAND gate flip-flop keeps the clocks disabled after reset until the transmitting FIFO de-asserts the Empty Flag and, thus, "HALT CLOCK" for the first time. This provides adequate time for the Q_{n-2} signal to return to logic high following reset, thus completing the reset sequence.

TIMING

The timings for the serial interface are based on the IDT72103/4 preliminary data sheet, dated April 1987, for a part with a 50ns address access time and for the schematic in Figure 8. Timing for other versions will follow this pattern. For operation at 40MHz, pipelining of logic delays is required for the handshake logic. The serial clock period is only 25ns. For operation at lower speeds, somewhat less complex circuitry can be used with fewer D flip-flops for pipelining.

The timings shown in Figures 9 and 10 assume the use of an IDT74FCT374A with CP-to-On delay of 6.5ns maximum and fast 74F00 series logic with propagation delays of 6ns. Minimum clock high time is dictated by the need to enable and disable the clock without glitching. Conservatively, this is 6ns OR gate delay + 6.5ns CP-to-On delay. Minimum clock period is dictated, in this case, by the fastest FIFO shift logic specification of 40MHz.

The "HALT CLOCK" signal may be de-asserted too close to the positive clock edge to avoid metastability in the D flip-flop associated with register input D3. To assure that the metastability does not cause glitches in the clock signal, the output O3 feeds the input D4. This would give the metastable flip-flop 25ns, the clock period minus 2ns, the set-up time for the next D input stage to settle out before affecting the clock logic. With this logic family, this time should be adequate to provide a very low probability that the metastable condition will not propagate further. Since timing is not critical here, another flip-flop stage has been added to ensure this (D5 and O5).

At 20ns maximum from clock high, the transmitter's read signal can be too late to safely de-assert the clock signals after one necessary gate delay (6ns) and still meet the set-up time for the IDT74FCT374A register (2ns). Instead, the output signal of a Q output tap two less than that used for the read signal is clocked in (Figure 9). The time from clock high to Q high is then 20ns maximum plus 2ns set-up. This safely fits into the 25ns window.

The AND gate shown in Figure 7 is present in Figure 8, but is the input to an additional OR gate not shown in Figure 7. The OR gate and a set-reset flip-flop are used to assure that the clocks are not active during reset. The flip-flop is set during system reset and cleared when the "HALT CLOCK" signal is de-asserted for the first time after reset. The flip-flop's clock-to-output time (6.5ns output 5 and 6), plus the two gate delays (6.5ns = 6ns), plus the set-up time (2ns), adds up to 20.5ns maximum and fits safely into the 25ns window provided.

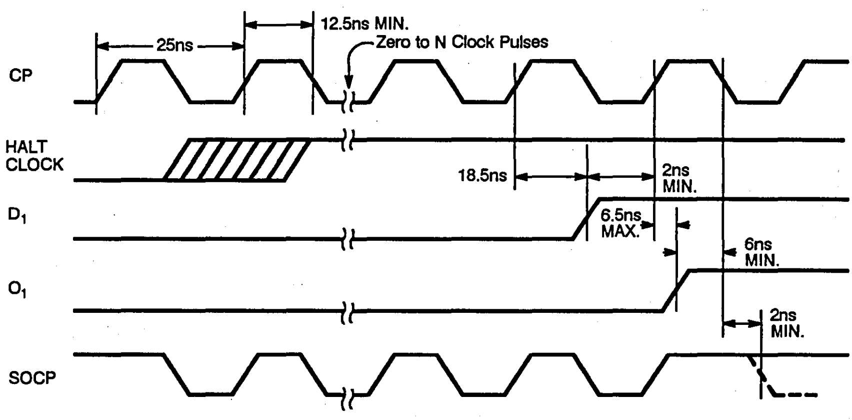


Figure 9. Serial Clock Disable Timing

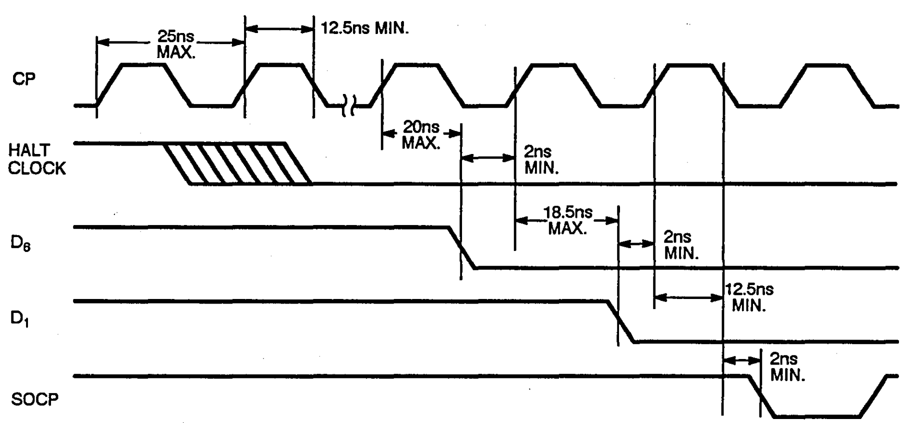


Figure 10. Serial Clock Enable Timing

14

The clock signals are disabled in the high state. In order to enable and disable them without glitches; the enable and disable operations must take place in the 12.5ns window provided by the clock high time. The register's clock-to-output delay is 6.5ns maximum; the gate delay is 6ns maximum.

The transmitter's serial clock must be one pulse ahead of the receiver's serial clock. This is accomplished by requiring the receiver's clock enable signal to pass through one additional D flip-flop before becoming effective (D_7 and O_7).

The reset pulse must be low for two serial clock pulses and the first write to the transmitting FIFO must not occur prior to RSQH (the time required for the FIFO Q outputs to return high after reset pulse—35ns for the part in question). Four additional serial clock pulses are required to ensure reset of the handshake logic without false clock pulses.

DATA WIDTH FOLDING DURING SERIAL TRANSFER

Data word widths may be multiplied or divided by integer quantities during transfer. Figure 11 shows an example where 16-bit data words are being folded into 8-bit words during serial transfer from a 16-bit processor to an 8-bit system. The folding operation is transparent to the processors on either side.

The folding operation is accomplished by programming the serial word width on each side of the serial link to multiples of each other. In Figure 11, the right hand serial word width has been programmed to be 16 bits. Nine bits of transmit FIFO #1 and 7 bits of transmit FIFO #2 are used. This is done by tying the SOX input of FIFO #1 to V_{CC} and triggering the read input for both FIFOs from the Q_4 output of transmit FIFO #2.

On the left hand side, the serial word width is programmed to 8 bits by tying the SIX input to V_{CC} and tying the write signal to the I/O pin D_7.

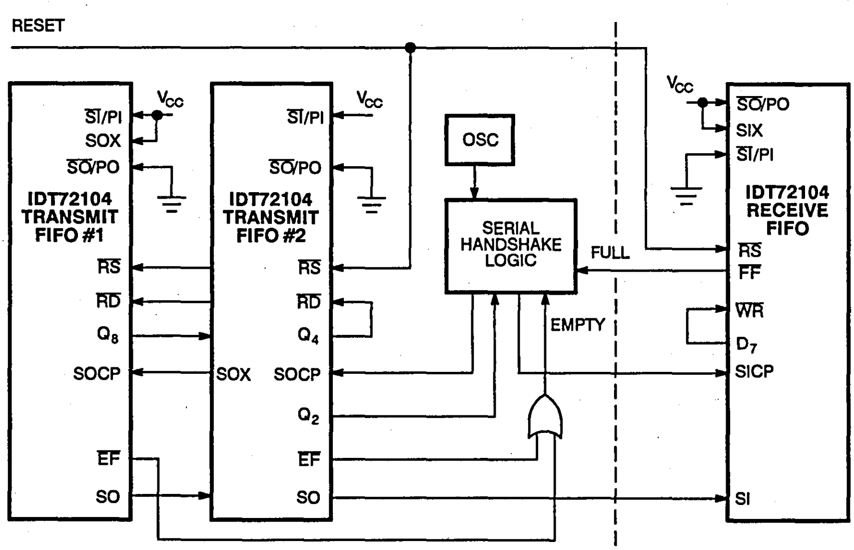


Figure 11. Schematic Facilitating 16-Bit to 8-Bit Data Folding During Serial Transfer

ONE-BIT VIRTUAL FIFO

In the serial-in/serial-out mode, the parallel-serial FIFO operates as a virtual 1 bit wide FIFO. The SICP input functions as a write input and the SOCP input functions as a read input. In this mode of operation the IDT72103/4 may be used to widen the word width of a parallel FIFO in 1-bit increments (Figure 12).

The 1-bit virtual FIFO has a latency of 4 to 9 bits, depending on the programmed serial word width. For example, if the FIFO is programmed for 9-bit words, 10 bits must be written into the FIFO before the Empty Flag is de-asserted and the first 9 bits can be read. The depth of the virtual FIFO in this mode is 9 x 4096 bits. If the word width is programmed to be 4, the latency is reduced to 4 bits and the depth is reduced to 4 x 4096 bits.

In applications where some latency is not a problem, the serial-in/serial-out FIFO can be used to extend the width of a parallel FIFO in increments of one. In general, the serial-serial FIFO depth should exceed the depth of the parallel FIFO to avoid empty and full boundary condition conflicts.

In Figure 12, an IDT74FCT861 latch is shown to maintain tri-state capability across all 10 output bits. This may not be required.

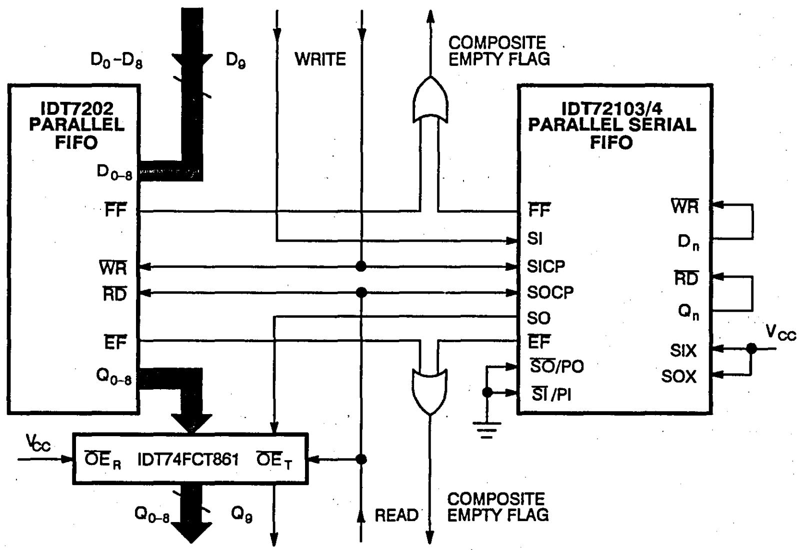


Figure 12. Serial-Serial FIFO Expanding the Width of a Parallel FIFO

CONCLUSION

The IDT72103/4 Parallel-Serial FIFO can be used to reduce parts count and lower power consumption in numerous applications which involve FIFOs and parallel/serial data conversion. Applications include video frame buffers, communications links, printer buffers and parallel-parallel FIFO bandwidth adjustment.

The numerous status flags, ample depth, speed and the presence of an independent output enable control make the FIFO highly flexible for use in parallel-to-parallel mode applications as well.

14

Integrated Device Technology, Inc.

SPC™ PROVIDES BOARD AND SYSTEM LEVEL TESTING THROUGH A SERIAL SCAN TECHNIQUE

APPLICATION NOTE AN-16

By Michael J. Miller and John R. Mick

INTRODUCTION

Advances in CMOS technology have resulted in the development of circuits that integrate the functions of multiple discrete devices onto a single chip. As companies continue to integrate more onto each device and put each device into smaller and smaller packages, board level densities have increased making the testing and debugging of systems more difficult. The desirable higher packaging density achieved with surface mounting (PLCC, SOIC) and tighter pin spacing has also contributed to the difficulties in testing at board and system levels. This is continuing at a time when the industry is also making an increased commitment to design and product quality which results in more testing and design verification. This quality commitment is not only manifested in the devices and systems but is also extending the quality of field maintenance support.

To address the situation, manufacturers of systems and ICs have used different techniques for diagnostic evaluation. Some of the first approaches were aimed at testing at the chip level and incorporated latches and registers which could, under diagnostics control, function as serial scan shift registers (LSSD pioneered by IBM). Other silicon manufacturers incorporated built-in test adhoc circuitry which performed an automatic self test. These techniques were successful at testing the chip level but did not address the board or system level. In the early 1980s, AMD introduced an octal register which included a shadow register to follow the operation of the main register. The contents of the shadow register can be serially accessed. By careful incorporation of this device throughout the board and system level, key data and control paths can be monitored. The shadow register technique is primarily limited to monitoring a single register.

While these methods provide basic testability, they are inflexible in that the system cannot be subjected to conditions other than those exercised by the BIT test logic, or be used conveniently as debug tools during the system design process. To overcome these limitations, IDT introduced the Serial Protocol Channel (SPC) in the fall of 1986. SPC allows the designer to observe and modify the contents of more complex and diverse structures such as register files, RAM, buses, I/O pads and logic. This simple on-chip technique allows observation of critical signals deep within the system and, when an error is observed, these signals may be easily modified in order to isolate and pinpoint the fault in the system.

A Wide Variety of Choices

As IDT expands their product line of fast VLSI CMOS devices we will continue to add devices to the family of parts with SPC. In the family today are:

- Registers:
  - IDT49FCT818—8-bits with output enable
  - IDT49FCT618—16-bits with byte output enables, clear, clock enable and read back
- ALUs:
  - IDT49C403—16-bit bit-slice microprocessor, quad 29203/03A, 64 registers, byte operation
  - IDT49C404—32-bit bit-slice microprocessor, funnel shifter/ALU/merge, 7-port RAM, bit field operation
- Sequencers:
  - IDT49C411—20-bit, interruptable, multi-way branch, status reg, counter stack
- Memory:
  - IDT78C18—Fast 2K x 8 EEPROM
  - IDT71502—Monolithic registered WCS RAM, break point detect, parity
- Subsystem Modules Built With SPC:
  - IDT7MB60XX—4K x 80 WCS with sequencer
  - IDT7MB6042—8K x 112 WCS
  - IDT7M6032—16K x 32 WCS
  - TBD—Several in design

The SPC Diagnostics Principle

In order to better understand SPC, consider a 16-bit register used in the data and control paths of a high-performance system. As shown in Figure 1, the main data path of the IDT49FCT618 lies in the section on the right and is from the D inputs down to the register and through the Y outputs.

This is the path that will be used most often during normal operation. The control signals provide the clocking and clearing of the data through the register. Provision is also made for reading the output from the register back onto the D bus. A latch ensures that the data captured in real-time settles down prior to being read by the processor on the D pins.

To enable monitoring of the system buses, a path should be established to access the register logic circuitry without affecting normal operation. The circuitry on the left is the added Serial Protocol Channel logic. It permits user-modification and observation of the D input pins, Data Register, Y output pins and the state of the Control inputs through the SPC Data and Control register. System memory can now be loaded by scanning in data through the SPC port and enabling it onto the D bus. The SPC Command and Data registers are easily accessed while the system is under normal operation.

SPC and MICROSLICE are trademarks of Integrated Device Technology, Inc.

Printed in the U.S.A. 11/87

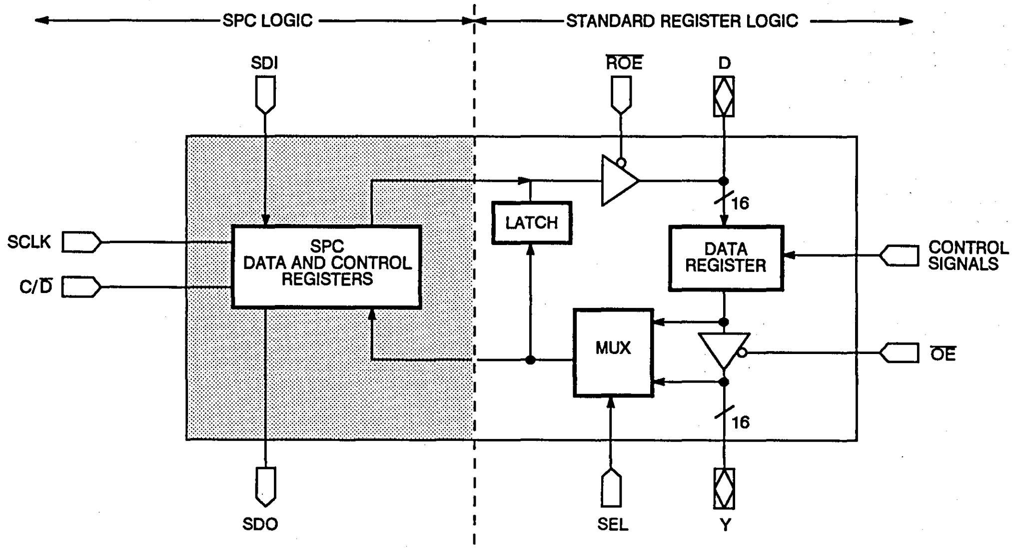


Figure 1. The Diagnostics Principle Using SPC on the IDT49C618

The SPC also allows for diagnostic operations to be performed synchronously with the system clock or in the "single step" mode. Thus, access to the system buses, via such special registers, enables the user to observe signals nested deep within the system and diagnose any system malfunction without the need for designing additional hardware logic. Such SPC logic, when implemented on ALUs and sequencers, simplifies the debug effort required for today's highly integrated complex circuitry.

The Serial Protocol Channel Defined

The Serial Protocol Channel (SPC) is a flexible on-chip feature which can be brought into use to monitor and control the operation of both the device and the interface hardware. It consists of four pins by which data can be entered into and extracted from a device through a serial data input and output port. Addresses and commands can be inserted into the device for stimulating and monitoring not only internal hardware but also the system buses and device I/O pins.

The SPC has been optimized for a minimum number of pins with maximum flexibility. It consists of four pins:

- Serial Data Input pin (SDI) for inserting data and command strings
- Serial Data Output pin (SDO) for extracting information from the device
- Serial Clock pin (SCLK) for clocking the information
- Command/Data mode pin ($C/\overline{D}$) to identify commands from data

The Broad Applications of SPC

SPC can be applied at multiple points in the life of a product in a variety of ways. It can be employed to debug and verify board designs. The code, vectors and SPC paths developed to verify the design can be carried on through to be the basis of manufacturing test and trouble shooting. Later on, SPC can be used for field maintenance test and trouble shooting. SPC is often incorporated for power on initialization of state machine and microprogram writable control stores. When E^2PROMs with SPC from IDT are deeply embedded into systems, factory floor and field configuration can be accomplished without the removal of boards or parts from the system.

SPC Aides Design Debug and Verification

Today, system debug and software development often incorporate a technique called In Circuit Emulation (ICE) to monitor the operation of complex VLSI devices such as microprocessors. ICE units often operate through the technique of employing a "captive" microprocessor device in a pod with buffers and cables that plug into the designers target socket.

14

Through SPC, a similar function can be achieved without slowing the system down with cables and buffers while simultaneously allowing for the observation of multiple devices throughout the system. Instead of "capturing" and isolating the devices under test, the SPC approach leaves the devices soldered into the board and accesses the contents of the device insitu.

Access to the SPC on the designer's system could be obtained using the parallel I/O ports of a development systems (such as an IBM-PC or a PC-compatible) directly to the SPC lines.

When using the parallel port, the PC contains the monitor program required to generate the protocol for the SPC lines and supply the diagnostic information to the SPC hardware. This would allow the PC to be used not only as a development station, but also as a test and debugging tool. Figure 3 shows a set-up of a user's system. Microcode development is done on the host PC. The parallel interface connects the PC to the user's system via the four diagnostics pins SDI, SDO, SCLK and C/$\overline{D}$. The monitor program would allow entering the data and addresses, exercising the commands and extracting and displaying the data from each device in the SPC ring.

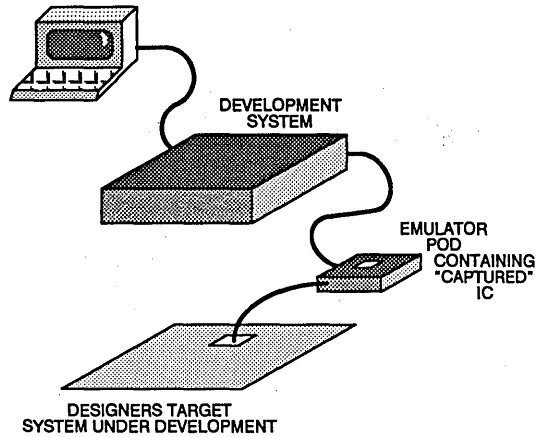


Figure 2. The ICE Environment

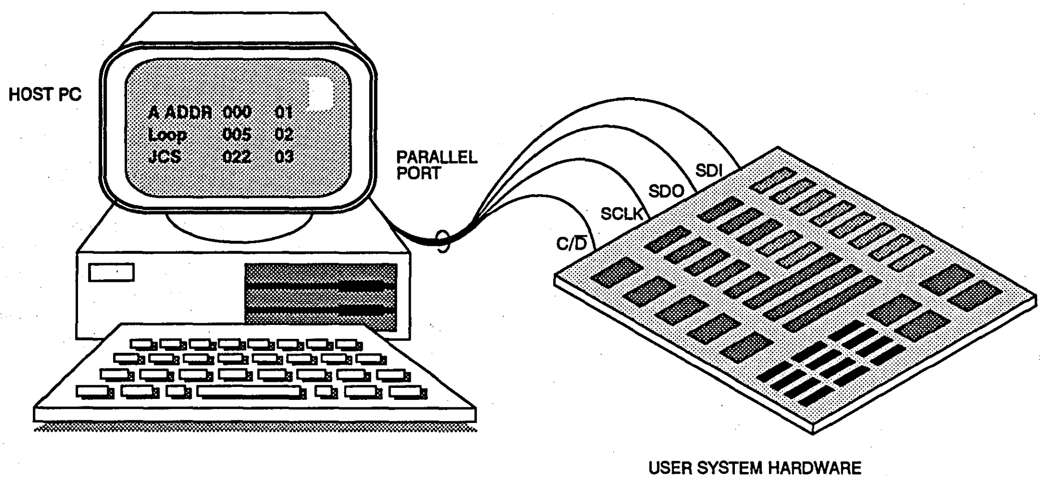


Figure 3. A PC-Based User-System

Figure 4 shows, in more detail, how the development system would attach to a target system such as a microprogrammable design. The development system might be any of the numerous systems such as IBM PC/XT, clone compatible, Apple computer, as well as a system designed by the user.

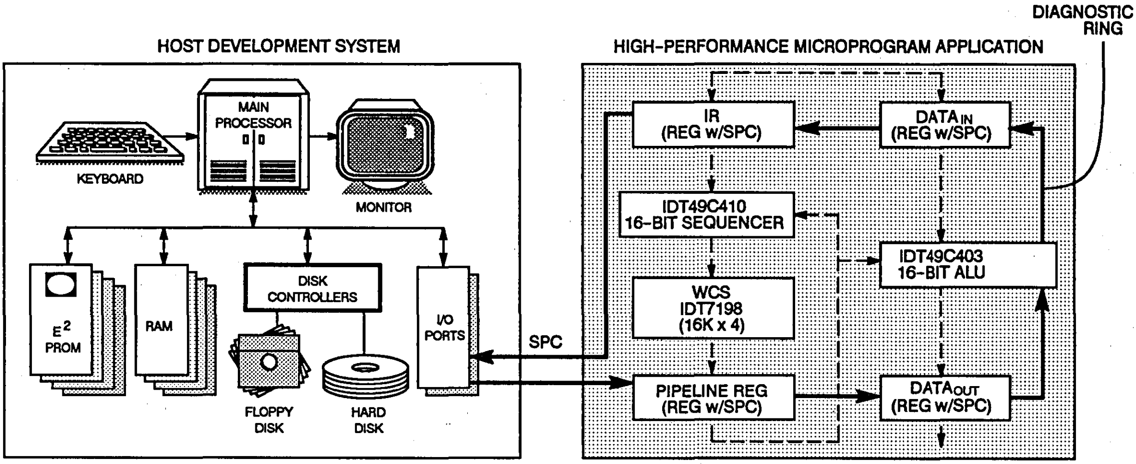


Figure 4. Typical Microprogram Application with SPC

SPC on the Manufacturing and Test Floor

When test philosophy is designed in and employed at development time through the use of SPC, the task of manufacturing test is made much easier. With the advent of surface mount devices such as PLCC, LCC and SOIC packages, dense double-sided boards can be constructed which seemingly defy such test techniques as bed of nails. SPC can be used in concert with such tried and true techniques such as board edge access. Through such combinations, test time can be cut by allowing for internal states of deeply embedded registers to be set up without having to go through a multitude of external stimulus vectors. The same development system that was used by the designer could be used on the manufacturing floor to drive the SPC channels. Alternatively, many ATE processors could be equipped to drive SPC.

A subset of the same vectors used for automatic test could be combined with others and loaded into portable systems such as clones and used in the field to diagnose and trouble-shoot. In larger systems which incorporate their own diagnostic processor to drive SPC, remote diagnostics is conceivable through the use of modems.

Initializing with SPC at Power Up Time

Some systems utilize writable control stores that must be loaded during power on. Such systems could utilize SPC as a mechanism to access the control store. The SPC channel could be driven by something as simple as a PAL state machine and load code out of slower dense EPROMs. Alternately, a processor on the user system could be used to generate the SPC signals and perform such functions as Writable Control Store initialize and power up diagnostic operations. This could be the host processor or a dedicated control processor. Figure 5 shows a system where the host processor is used to initialize and control the SPC diagnostics operations over the entire system. In larger systems, a dedicated processor could be utilized to both power up initialize the system, as well as do power on diagnostics or built-In Self Test (BIST).

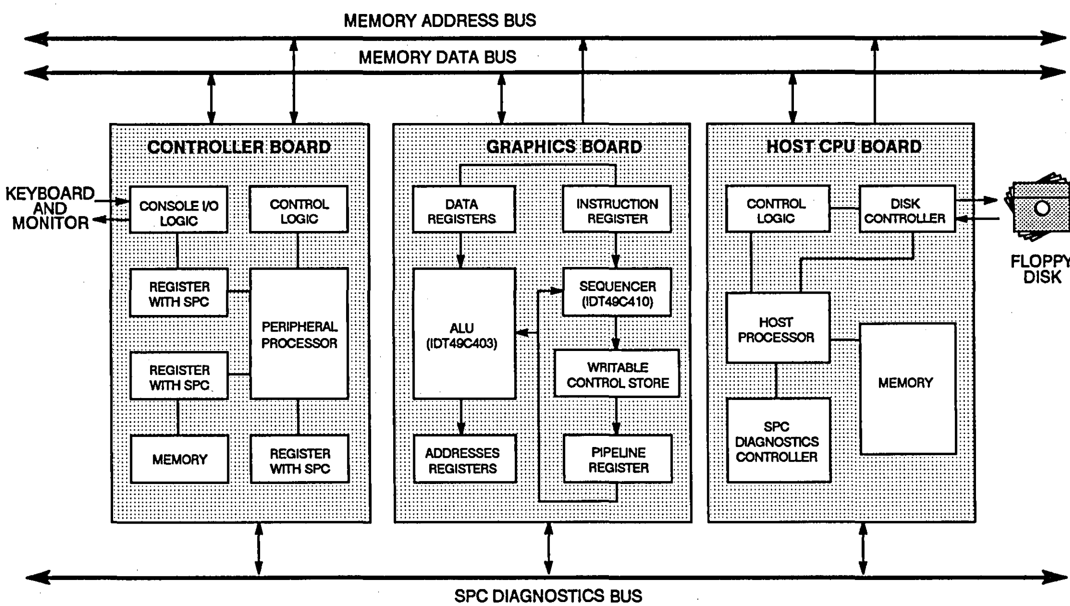


Figure 5. A Dedicated SPC Controller for a Complex Digital System

Another method would be to use a diagnostics interface board to communicate with the SPC. To access the SPC through this interface board, the PC would serve as a host, transmitting diagnostic information directly to the user's hardware. The interface board generates the signals to operate the SPC in the user's system. The ability to be used not only for system diagnostics but also as a debug tool is the primary advantage of the SPC scheme.

Factory and Field Configuration of Systems Through SPC

With devices that employ E^2PROM and SPC channels, factory and remote initialization can be contemplated. Traditionally, state machines and certain types of processors that cannot modify their code space have used non-volatile devices such as EPROMs and PROMs for their code stores. Today, E^2PROM with SPC can be used in place of, and deeply embedded within, such systems. Through the SPC channel, these devices can be initialized even though they may be soldered and bolted inside a cabinet. Such initialization might be employed just prior to shipment to configure a product or provide non-volatile field updates. One of the most simple approaches to programming these devices is to utilize a system such as an IBM PC/XT and its ubiquitous centronics parallel printer port to drive the SPC signals.

Understanding SPC Operation

To better understand how SPC functions, the following paragraphs describe SPC as it relates to the IDT78C18 fast 2K x 8 E^2PROM. The SPC channel on the IDT78C18 is a simple model of that which is included on other devices with SPC. The IDT78C18 incorporates a 2K x 8 memory array which has control and data signals that function in the same fashion as other E^2PROMs. In addition, an SPC channel is included on the silicon which allows for access to the memory array through the serial pins of the SPC channel. The Serial Data In (SDI) and Serial Data Out (SDO) pins allow for information to be shifted through the device under control of the serial Shift Clock (SCLK). The Command Data ($C/\overline{D}$) input indicates to the device when the information being shifted through is commands or data.

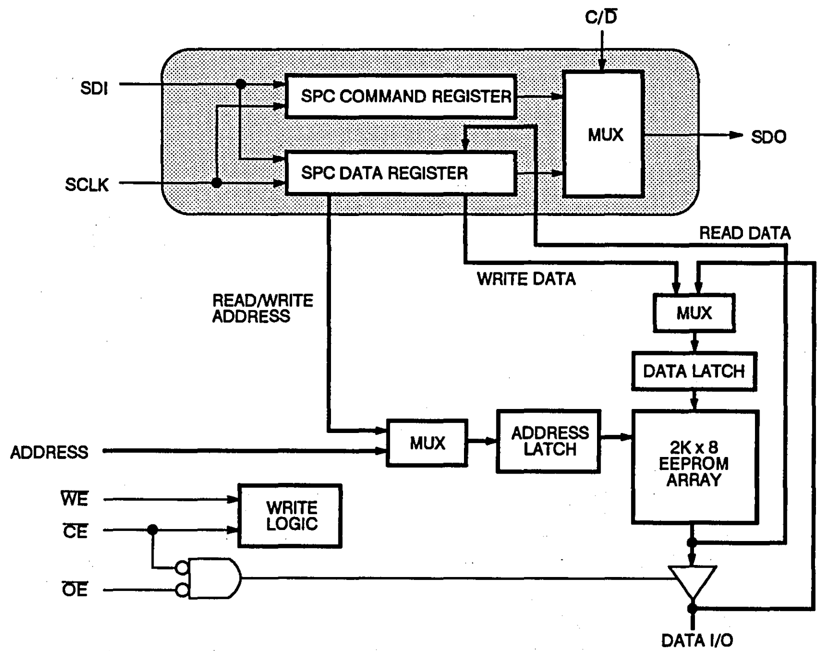


Figure 6. Block Diagram of the IDT78C18 Fast 2K x 8 E^{2}PROM with SPC

The SPC command set for accessing the IDT78C18 is straightforward and includes four commands: Read (0), Write (1), Erase (2) and NO-OP (F). The SPC command register is four bits long and commands are shifted in least significant bit first. The SPC data register is composed of the actual data transferred as well as the address in the memory array. The address and data are shifted in least significant bit first also. To accomodate for future expansion, the address register is implemented with 16-bit shift register of which the lower 11 bits are significant.

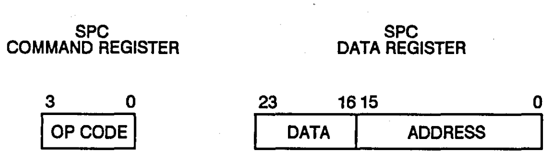


Figure 7. Format of SPC Command and Data Registers

An SPC operation is performed in up to four distinct phases:

(1) data is shifted in;

(2) command is shifted in;

(3) command is executed; and

(4) data is shifted out.

While some commands may not have phase (1) or (4), all SPC commands use at least phases (2) and (3).

Information is shifted into the device under two phases of operation. In phase 1, the C/$\overline{D}$ line is LOW and the data bits are shifted into the device. In phase 2, the C/$\overline{D}$ line is HIGH and the command bits are shifted into the device.

During the data phases (1 and 4), data is simultaneously shifted into the serial data register while the information from the data register is shifted out. During the command phase, opcode type information is shifted through the serial ports. The command is executed when the last bit is shifted in and the C/$\overline{D}$ line is brought low. The execution phase is ended with the next serial clock edge. Figure 8 shows the sequence of events during a command execution.

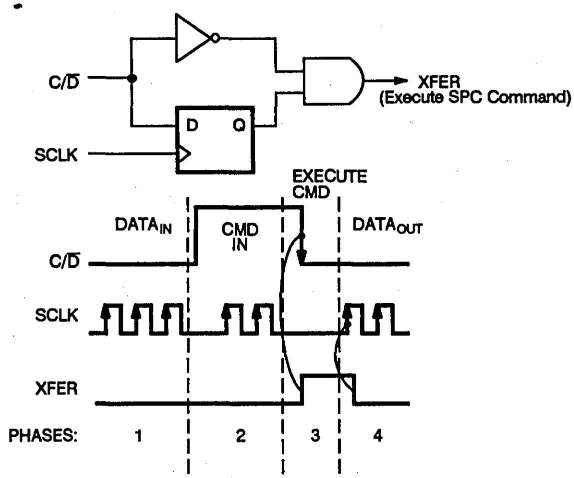


Figure 8. Phases of Executing SPC Commands

There is an internal signal called XFER which is generated from the SCLK and the C/D̄ inputs. XFER is used both as an enable as well as a strobe. It begins with C/D̄ transitioning from HIGH-to-LOW and ends with the next rising edge of SCLK. The strobe is then used to gate the decoded command register. The decode can be thought of as a one-of-N decode. In this way, individual strobes and enables are generated which can be used to drive multiplexers and control registers/latches. In all devices there is a No-Operation opcode (NOP) consisting of all command bits HIGH, which prevents the generation of any strobes.

Usually, execution of the Serial Protocol commands can only be performed on devices which are currently in their own normal system standby mode. Each device has a unique standby mode. For the IDT78C18, standby is when there is no current write or read operation under way. If a read operation is under progress, the recipient of the data must tolerate a period of undefined data. For the MICROSLICE™ family devices, standby is when the system clock is stopped in the HIGH state guaranteeing that the RAM, latches and registers are not being accessed.

The above restriction does not apply to shifting command and data information through an active device into another device in its standby mode. However, the user must make sure that when the commands (and data) reach their respective devices and execution is signaled by the lowering of the C/D̄ line, those devices which are active have a NOP opcode in their serial command registers and, therefore, will not generate internal strobes, thereby leaving their current operation undisturbed.

Figure 9 shows the general format of the execution of an SPC read command to observe the contents at any location in the memory array. The command sequence starts by shifting in the address of the location to be read, the opcode for the read command, followed by shifting out the contents of the desired location. When the C/D̄ line is brought LOW, the least significant address bit of the address register is already at the SDO pin.

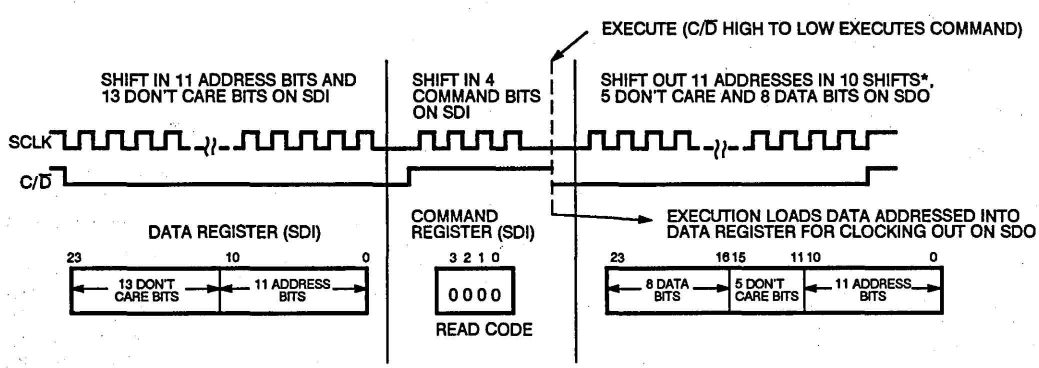


Figure 9. SPC Read Operation on IDT78C18 E^2PROM

While the read operation utilized all four phases of the general SPC operation, the following diagram demonstrates how the write command utilizes only three phases. The write operation on the IDT78C18 through SPC is started by shifting in the address and data to be written (see Figure 10). The SPC command for writing on the IDT78C18 is shifted in next, followed by the start of execution of the command with the lowering of the C/$\overline{D}$ input. The triggering of the write command must be terminated by raising the edge of SCLK such that another write operation is not retriggered.

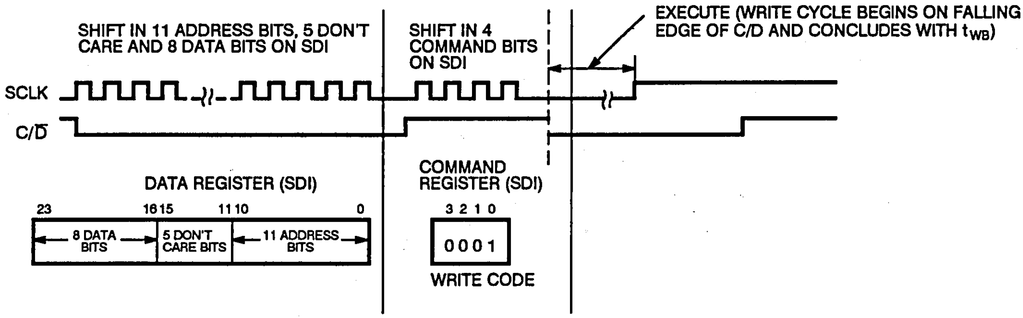


Figure 10. SPC Write Operation on IDT78C18 E²PROM

The SPC erase operation on the IDT78C18 can be done with only two phases: shift in command and execute. The diagram below shows the shifting in of the opcode for erase and the execution of the command.

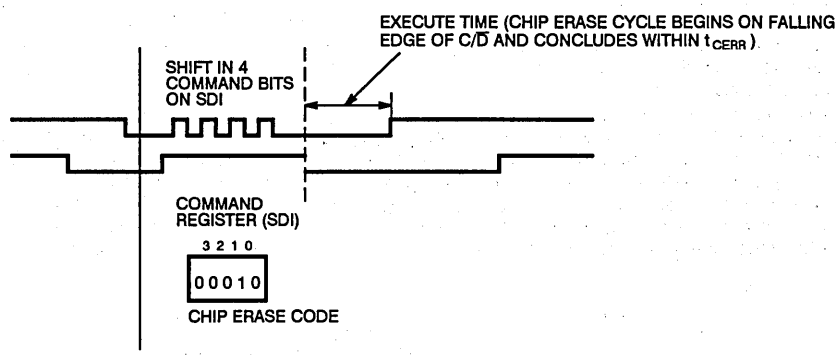


Figure 11. SPC Erase Operation on IDT78C18 E²PROM

Good Rules to Follow When Designing with SPC

There are several rules that make designs with SPC easier to implement and assure proper operation. When designing a system with many parts that incorporate SPC, the designer should divide the different parts into functional groups and employ at least one SPC scan loop for each group. If one scan loop is used for the entire design, it may become more difficult to coordinate the activity of each device. When there is only one scan loop, the observation of desired portions of the design is slowed down because of shifting bits that have no interest at the time.

Consistency must be exercised in the software to always leave the SPC signals in known states after each step in the debug/access software. In the design examples shown below, after executing a complete SPC command and extracting the data, the C/$\overline{D}$ signal is left in the HIGH state. This assures that each SPC channel in each device will be left in a non-execute state ready for the next SPC command or normal operation. The SCLK can be left HIGH of LOW, but should be the same after each command.

14

Serial Protocol Channel Design Example #1 Using the IBM PC/XT Centronics Port with SPC

The following example shows how the centronics printer port on a IBM PC/XT can be used to communicate via SPC with the IDT78C18 fast 2K x 8 E^2PROM. For designs which incorporate the IDT78C18 as a state machine or writable control store, this technique could be used in manufacturing as a method for configuring a product before test and shipment. In the field, this approach could be used for updating a product with the latest release of control code.

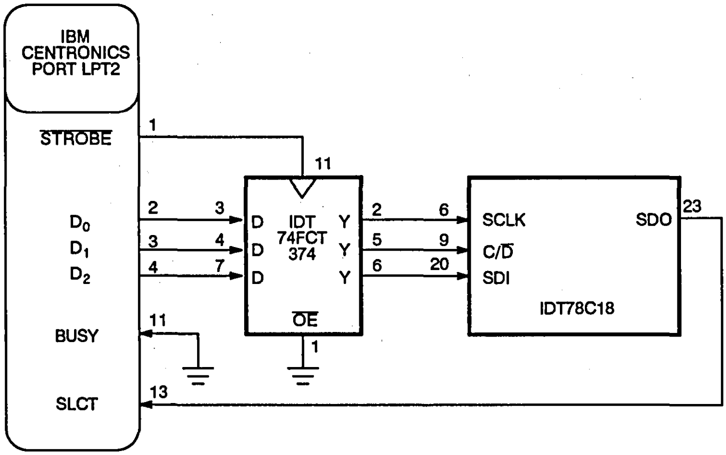


Figure 12. Centronics Interface to a SPC

The Hardware

The centronics port can be used as a parallel port to load an IDT74FCT374 to generate the required signals SDI, SCLK and C/D̄. The signal SDO, coming back from the IDT78C18, can be read in via the SLCT input on the centronics port. The block diagram in Figure 12 shows how the appropriate connections are made. The register is required due to glitches on the output port data pins.

The Software

The following program listing shows the subroutines in "C" which can be used to access the IDT78C18. In this example, the program was compiled in TURBO C from Borland International. This particular compiler has a library routine, named BIOSPRINT(), which can be used to access the centronics port on the IBM PC. When BIOSPRINT is called, it sets the values of the parallel bits on D_0, D_1 and D_2 and then pulses STROBE* HIGH-LOW-HIGH. It was used as the key routine to implement the SET_BIT() routine which sets the bit values in the IDT74FCT374. The routines SDI(), SCLK() and C_D() use SET_BIT() to set the corresponding signals of the IDT78C18. The last low level routine, SDO(), is used to return the value of the SDO pin on the IDT78C18.

The next level of code is composed of the two routines: SHIFT_OUT and SHIFT_IN. Both routines are responsible for shifting a specified number of bits out to the IDT78C18 or in from the IDT78C18. When these routines finish, the SCLK is left LOW.

The last level of code includes the routines READ_VALUE(), WRITE_VALUE() and ERASE(). As the names imply, they perform the appropriate operations to achieve the corresponding function through the SPC channel. When these routines finish, the SCLK and C/D̄ pins are left HIGH. In this way, the SPC is guaranteed to be left in a nonexecute state.

```
                    M O D U L E     S P C . C
                              (sp.c)

             Copyright 1987 by Integrated Device Technology Inc.
                          All rights reserved

    Programmer: Roy M. Johnson

    This module contains the routines to exercise SPC on the IDT78C18A EEPROM
    through the parallel output port lpt2

    This module contains the following routines:

    set_bit                         : interface to parallel port lpt2
    sdo                             : reads the sdo pin on the 78C18A
    sdi                             : sets the sdi pin on the 78C18A
    c_d                             : sets the cd pin on the 78C18A
    sclk                            : sets the sclk pin on the 78C18A
    shift_out                       : shifts data out to the 78C18A
    Shift_in                        : shifts data in from the 78C18A
    read_value                      : reads a value from a given address
    write_value                     : writes a value to a given address
    erase                           : erases the chip

    MODIFICATIONS

    RMJ - Tue Sept 5, 1987 09:30               : Created module
    MJM - Sat Sept 26, 1987 11:22:20           : Modified for appnote

    /*          Turboc libraries                                */

#include        <dos.h>
#include        <bios.h>
#include        <portab.h>        /* Initialize printer port settings */
MLOCAL          cur_status = 0;   /* Initialize printer port status */

                          FUNCTION SET_BIT

      Sets a bit (value) on the parallel output port LPT2. The bit is
      specified by (mask).

      Calling sequence: set_bit (value, mask)
             value: boolean value to be transmitted
             mask: specifies the sdi, sclk or cd pin
      Return values: pr_status
      BIOS functions invoked: biosprint

MLOCAL VOID     set_bit (value, mask)
BOOLEAN value;                          /* Value to be written */
UWORD   mask;                           /* Specifies pin to be */
                                        /* written: SDI, SCLCK or C/D */
{
        UWORD   pr_status;
        const   UWORD   cmd = 0 ;               /* biosprint          */
        const   UWORD   lpt2   = 1;             /* parameters         */

        if value == 1)                          /* mask in value to be */
                cur_status |=  mask;            /* written            */
        else
                cur_status &=  (~mask);
        pr_status = biosprint (cmd, cur_status, lpt2);
}
```

```
                         FUNCTION   SDO

    Reads and returns bit SDO (select line) on the parallel output port lpt2

    Calling sequence: sdo ()
    Return values: Bit value on busy line
    BIOS functions invoked: biosprint
```

```
GLOBAL BOOLEAN sdo ()
{
        UWORD value;
        const   UWORD cmd = 2;              /* biosprint            */
        const   UWORD lpt2 = 1;             /* parameters           */
        const   UWORD   select_mask = 0x10; /* select line mask     */
        UWORD    bits;

        bits = biosprint (cmd, cur_status, lpt2);

        value = bits & select_mask;         /* extract bit          */
        value >>= 4;
        return (value);
}
```

```
                         FUNCTION   SDI

    Transmits a bit value to the SDI pin on SPC

    Calling sequence: sdi (value)
            value: boolean value to be transmitted
    Return values: None
    Function invoked: set_bit
```

```
GLOBAL VOID          sdi (value)
BOOLEAN value;              /* Value to be transmitted            */

{
        const   UWORD   sdi_mask = 0x04;        /* sdi connected to  */
                                                /* D2 on port        */
        set_bit (value, sdi_mask);
}
```

```
                    FUNCTION    C_D

    Transmits a bit value to the C/D pin on SPC

    Calling sequence:  c_d (value)
         value: boolean value to be transmitted
    Return values: None
    Functions invoked: set_bit
```

```
GLOBAL VOID        c_d (value)
BOOLEAN value;
{
       const   UWORD   c_d_mask = 0x02;         /* C/D connected to  */
                                                /* D1 on port        */
       set_bit (value, c_d_mask);
}
```

```
                    FUNCTION   SCLK

    Transmits a bit value to the SCLK pin on SPC

    Calling sequence: sclk (value)
          value: boolean value to be transmitted
    Return values: None
    Functions invoked: set_bit
```

```
GLOBAL VOID        sclk (value)
BOOLEAN value;
{
          const   UWORD   sclk_mask = 0x01;             /* SCLK connected to   */
                                                        /* DO on port          */
          set_bit (value, sclk_mask);
}
```

```
                    FUNCTION   SHIFT_OUT

     Shifts data out serially, to the SPC registers

     Calling sequence: shift_out (data, num_shifts)
             data: data value to be shifted out
             num_shifts: number of shifts to be performed
     Return values: None
     Functions invoked: sdi, sclk
```

```
GLOBAL VOID         shift_out (data, num_shifts)
UWORD   data;                     /* Data value to be shifted               */
UWORD   num_shifts                /* Number of shifts to be performed       */
}
           const   UWORD   mask = 0x01;
           UWORD   i ;
           BOOLEAN bit;

           for (i = 0; i < num_shifts; i++) {
                      sclk (LOW);
                      bit = data & mask;
                     data >>= 1;
                      sdi (bit);
                      sclk (HIGH);
           }

           sclk (LOW);                     /* Set sclk low                  */
}
```

```
                    FUNCTION    SHIFT_IN

     Shifts data in serially, from the SPC data register

     Calling sequence: shift_in (num_shifts)
                num_shifts: number of shifts to be performed
     Return values: 16-bit word (data) with the value of the
                    8 MSB's of the data register
     Functions invoked: sdo, sclk
```

```
GLOBAL VOID         shift_in (num_shifts)
UWORD   num_shifts;               */Number of shifts to be performed */

{
           UWORD   data = 0;               */16-bit word for return value   */
           UWORD   i;
           UWORD   temp = 0;
           UWORD   mask = 0x8000;
           BOOLEAN bit;

           for (i = 0; i < num_shifts; i++) {
                      sclk (LOW);
                      temp >>= 1;
                      bit = sdo ();
                      if (bit) temp | = mask;
                      sclk (HIGH);
           }
           sclk (LOW);
           data = temp >> ((sizeof (UWORD) * 8) – num_shifts;
           return (data);

}
```

```
                         FUNCTION   READ_VALUE .
```

14

```
     Reads value in SPC serial data register

     Calling sequence: read_value (address)
            address: address of location to be read
     Return values: 16-bit word (data) with the value read
     Functions invoked: c_d, shift_out, shift_in

GLOBAL UWORD   read_write (address)
UWORD   address;                   /* Address of location to be read
{
          const   UWORD  read_opcode = 0x00;    /* Read opcode               */
          UWORD   data = 0;

          c_d (LOW);
          shift_out (address, 11);
          shift_out (0x00, 13);    /* don't cares      */
          c_d (HIGH);
          shift_out (read_opcode, 4);
          c_d (LOW);
          shift_in (16);                         /* don't cares         */
          data = shift_in (8);
          c_d (HIGH);
          return (data);
}

                         FUNCTION   WRITE_VALUE

     Writes a value in the SPC data registers. No
     data polling is performed and a 10ms write time is assumed

     Calling sequence: write_value (address, data)
             address: address of location to be written
             data: data value to be written
     Return values: None
     Functions invoked: c_d, shift_out

GLOBAL VOID write_value (address, data)
UWORD   address;                   /* Address of location to be read          */
UWORD   data;                      /* Data value to be written                */
{
          const   UWORD  Write_opcode = 0x01;   /* Write opcode          */

          c_d (LOW);
          shift_out (address, 11);
          shift_out (0x00, 5);
          shift_out (data, 8);
          c_d (HIGH);
          shift_out (write_opcode, 4);
          c_d (LOW);
          sclk (HIGH);                 /* sclk set high in 2ms
          c_d (HIGH);
}

                         FUNCTION    ERASE

      Erases the chip

      Calling sequence: erase ()
      Return values: None
      Functions invoked: c_d, shift_out

VOID erase ()
{
          const   UWORD   erase_opcode = 0x02;   /* Erase opcode              */

          c_d (HIGH);
          shift_out (erase_opcode, 4);
          c_d (LOW);
          sclk (HIGH);                      /* sclk set high in 2ms          */
          c_d (HIGH);
}
```

Serial Protocol Channel Design Example #2 Using SPC to Load and Debug a Microprogram Design

The key element of control in a microprogram design is the writable control store. It is the element which contains the control program code that coordinates the operation of each of the elements in the design. In the past the control store has been difficult to test. In a typical design, there are many registers which are utilized for such tasks as the instruction register (referred to as the pipeline register in most microprogram designs) and data path registers. The IDT49FCT818 and IDT49FCT618 are two types of registers which might be used in such a design. They include an 8-bit and 16-bit 74374 type internal register, respectively, and an SPC channel for observation and modification of the contents of the register and its buses. When these registers are used, complete control can be exercised over a microprogram design. The following section will describe these registers, an ALU (IDT49C403) with SPC, followed by a design example using these devices and how to access them using SPC.

Detailed Look at the IDT49FCT618

The IDT49FCT618 is a high-speed, general purpose 16-bit register with a Serial Protocol Channel. The D-to-Y path of the octal register provides a data path that is designed for normal system operation wherever a high-speed clock register is required. The SPC is used to communicate with a serial command and data registers.

The command and data registers are used to observe and control the operation of the 16-bit parallel data register for diagnostic purposes. The SPC command and data registers can be accessed while the system is performing normal system function. Diagnostic operations can then be performed "on the fly," synchronous with the system clock, or can be performed in the "single step" environment. The SPC port utilizes serial data in and out pins (a concept originated at IBM) which can participate in a serial scan loop throughout the system where normal data, address, status and control registers are replaced with the IDT49FCT618. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then, after a specified number of clock cycles, the data can be clocked out and compared with expected results. An "oscilloscope mode" can be achieved by loading data from the SPC data register into the octal data register synchronous to the system clock (PCLK) using a diagnostic command which transfers data synchronously. When repeated every Nth clock, the repeating states of the system can be observed on an oscilloscope. When used as a pipeline register, WCS loading can be accom-plished by scanning in data through the SPC port and enabling the data onto the D bus pins.

14

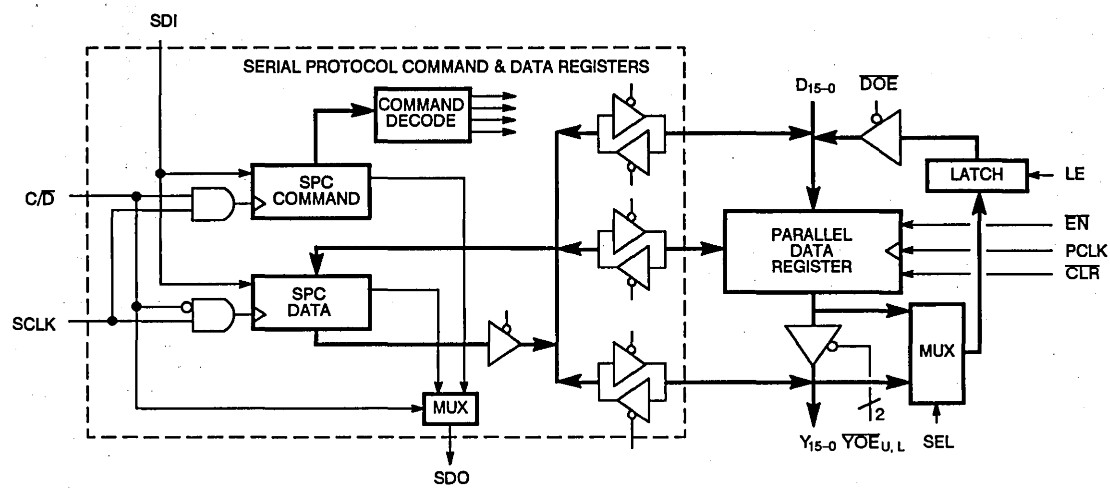


Figure 13. Detailed Functional Diagram of IDT49FCT618

Block Diagram

The block diagram consists of three main data paths and two logic blocks. The main data path is from the D inputs down to the register and through the Y outputs. This is the path that will be used most of the time in normal operation. For SPC operations there are data paths from the Y pins into the SPC data register and control block. Coming out of this block is the data path that allows data to be put back onto the D input pins or into the data register. The PCLK is used to clock the parallel data register. The EN signal is a clock enable for the 16-bit parallel data path. The $\overline{CLR}$ line offers an asynchronous 16-bit clear. $\overline{YOE}_{U,L}$ inputs are used to control the tri-state output of the Y pins. the other main data path is a read back path from the output of the 16-bit parallel register to the D bus. The SEL pin selects data from the output of the 16-bit parallel register to the D bus. The SEL pin selects data from the internal Q bus or the data output pins Y. The LE signal controls a latch in the read back path. In this way, data can be latched on the fly and allowed to settle before a processor reads it back on the D pins. The $\overline{ROE}$ input is a three-state control which selects whether the D bus is an input or an output.

The four standard pins for SPC are included on the IDT49FCT618 (SDI, SDO, SCLK and C/$\overline{D}$). Data is shifted through the IDT49FCT618 in the direction of LSB first. This means the first bit of information to be shifted in on SDI must be the least significant bit and the first bit to come out on SDO is the least significant. The least significant bit is always present at SDO. The C/$\overline{D}$ input determines whether it is the SPC command register or the SPC data register.

Cascading SPC Devices

When using SPC on a system level, the serial out of one device is connected to the serial in of the next device, thus cascading multiple devices with SPC capability together in one long serial shift register. The serial clock and the command/data mode line of each of these devices is connected in parallel. In this way, a minimal number of connections are made between each device for SPC. In the example of three cascaded devices shown below, to enter a command or data into the third device, the data must be shifted through the previous two devices. The data for each device must be entered, in order of position, in the ring through the first serial input. On the last shift clock, all of the data for each device will reach their final destination.

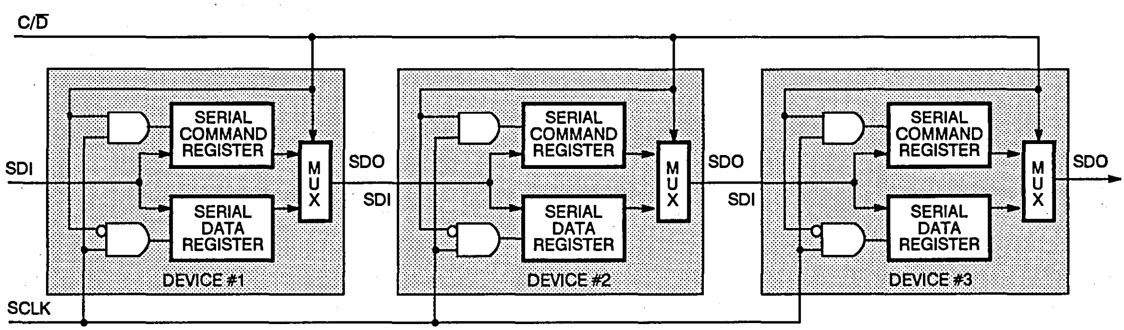


Figure 14. Example of Three Cascaded Devices

The SPC command registers can be viewed as one long virtual microprogram command word where each field corresponds to the individual command bits of each device. In the same way, the SPC data register can be viewed as one long virtual data register.

SPC Commands of the IDT49FCT618

There are 16 possible diagnostic opcodes. Ten of these are utilized; the other six are reserved and performed NO-OP functions. The top eight opcodes, 0 through 7, are reserved for transferring data into the SPC data register for shifting out. The lower eight opcodes, 8 through 15, are used for transferring data from the SPC data register to other parts of the device. Two of the commands are also used for connecting the data in and out pins.

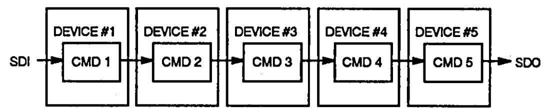
Opcode 0 is used for transferring data from the Y output pins into the SPC data register. Opcode 1 transfers data from the output of the register before the tri-state gate into the SPC data register. Opcode 2 transfers data which is on the data input pins D into the SPC data register. Opcode 3 transfers data on the Y pins to the SPC data register on the next PCLK, thus achieving a synchronous observation of the pipeline register in real time. This operation can be repeated without shifting in a new command by pulsing $C/\overline{D}$ LOW-HIGH-LOW after each PCLK. Opcode 4 is used for loading status into the SPC data register. Status consists of $\overline{YOE}_{U,L}$, PCLK, $\overline{ROE}$, LE, $\overline{EN}$, $\overline{CLR}$ and SEL.

OP Code	Diagnostic Command
0	Y to SPC Data Register
1	Parallel Data Register to SPC Data Register
2	D to SPC Data Register
3	Y to SPC Data Register Synchronous with PCLK
4	Status ($\overline{YOE}_{U,L}$, PCLK, etc.) to SPC Data Register
5-7	Reserved (NO-OP)
8	SPC Data to Y
9	SPC Data to D
10	SPC Data to Parallel Data Register
11	Select Serial Mode
12	Select Stub Mode
13	SPC Data to Y Synchronous with CLK/P
14	Connect D to Y
15	NO-OP

Figure 15. IDT49FCT618 SPC Commands

Opcode 8 is used for transferring data directly to the Y pins. Opcode 9 is used for transferring data in the SPC data register to the D pins. The operation of opcodes 8 and 9 can be temporarily suspended by raising the $C/\overline{D}$ input and resumed by lowering the $C/\overline{D}$ input. As soon as SCLK is transitioned from LOW-to-HIGH, the command is terminated.

Opcode 10 is used for transferring data from the SPC data register into the parallel data register. Opcodes 11 and 12 are used to select Serial and Stub Modes for shifting subsequent SPC commands. Once the mode is selected, the IDT49FCT618 SPC stays in that mode, regardless of how many commands are executed, until reprogrammed with either one of the Serial or Stub mode commands. The serial mode is the default mode that the IDT49FCT618 powers up in. In serial mode, commands are shifted through the command register and then to the SDO pin. This is the typical mode used when several varieties of devices that utilize the SPC access method are employed on one serial ring.



In Stub mode, SDI is connected directly to SDO. The serial input of the command register is connected to SDI. In this way the same diagnostic command can be loaded into multiple devices of like type. For example, in four clock cycles the same command could be loaded into eight IDT49FCT618s (128-bit pipeline register). Dislike devices must be segregated into serial scan loops of similar type as shown below. For example, all IDT49FCT618s must be in one loop, while two IDT49C403s might be in another loop.

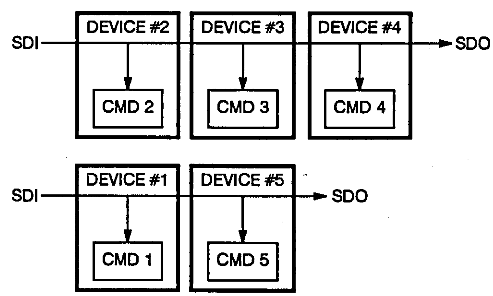


Figure 16. Example of Two Types of Devices in Stub Mode

Because there is an inherent delay through the device from SDI to SDO, the serial shift clock during the command phase must be slowed down to accommodate the delay. The slower clock is typically a small trade off compared to the reduced number of clock cycles.

Opcode 13 transfers data from the diagnostic data register to the pipeline register on the next PCLK. Opcode 14 connects the D bus to the Y. The operation of operation instruction 14 can be temporarily suspended, raising the $C/\overline{D}$ input and resumed by lowering the C/D input. As soon as SCLK is in transition, the command is terminated.

Except for the commands which transfer data from the SPC data register into the data register and set the Serial/Stub mode flip-flop, all of these commands are temporary and are only operational between the transition of HIGH-to-LOW of the $C/\overline{D}$ line and the LOW-to-HIGH of the SCLK clock.

Opcodes 3 and 13 transfer data synchronous to the PCLK which means that the HIGH-to-LOW on the $C/\overline{D}$ input is an arm signal. The data and command are shifted in while the PCLK is running. The $C/\overline{D}$ line is dropped previous to the desired PCLK edge and raised afterwards, before the next edge. These commands can be repeated over many times by leaving the $C/\overline{D}$ line LOW during multiple transitions of the PCLK, while not clocking SCLK. PCLK cycles can even be skipped by raising the C/$\overline{D}$ input during the desired clock periods.

The ability to execute a synchronous command repeatedly can provide major benefits. For example, the synchronous read instruction (instruction 3, Y to diag) could be clocked into the SPC command register. Then it could be continuously executed by pulsing the C/$\overline{D}$ line LOW-HIGH-LOW. When the whole system is stopped (PCLK quiescent), the SPC data register will contain the next to the last state of the parallel register. That value can be shifted out and the current state of the parallel register can then be observed, thus allowing for the observation of two states of the parallel register (the current and the previous).

In another example, an oscilloscope could be used to monitor the execution of a section of microcode. By loading into the SPC data register the pattern that forces a jump to a section of code and the synchronous write command (instruction 13, diag to Y) into the SPC command register, the system under test can be forced to repeat a segment of code repeatedly. When the C/$\overline{D}$ line is lowered, the system is forced to execute the state forced by what is in the SPC data register on the next PCLK. By raising the C/$\overline{D}$, the system is allowed to proceed normally until the C/$\overline{D}$ line is lowered often enough with small enough clock cycles. An oscilloscope can be used to observe the operation of the state machine.

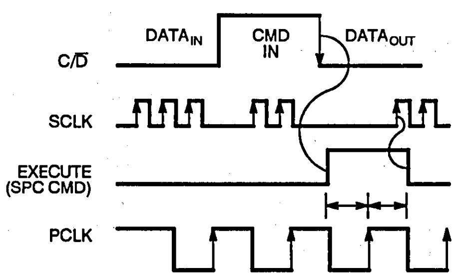


Figure 17. Timing of Synchronous Commands

Detailed SPC Architecture of the IDT49C403 Bit-Slice Microprocessor

The IDT49C403, a quad Am2903/29203 16-bit microprocessor slice, which includes an ALU and register file, is one of the devices on which IDT has incorporated the Serial Protocol Channel. The implementation of SPC on the IDT49C403 is shown in Figure 18.

Only four SPC pins (SDI, SDO, SCLK and C/$\overline{D}$) are used to serially access the I/O pad cells, as well as the internal ALU registers and buses. To control or monitor a section (such as the ALU), the appropriate command is loaded into the SPC command register. The desired function is then executed and the status information captured in the data register. The status information can then be serially shifted out and observed to verify proper system functionality.

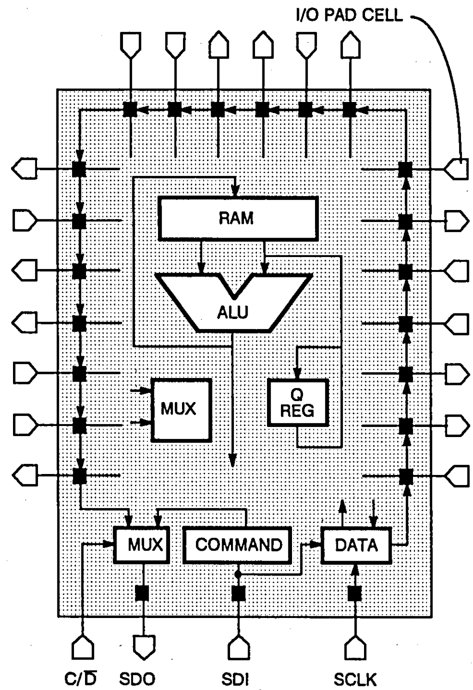


Figure 18. SPC on the IDT49C403 Die

The block diagram in Figure 19 shows the detailed SPC architecture for the IDT49C403. It primarily consists of serial registers for command, data, addresses and decode/control logic. The SPC command register consists of a four-bit field (signals 4-7) and four discrete control lines (signals 3, 2, 1, 0). The four-bit field coordinates the transfer of data between RAM and the SPC data register, as well as controls an on-chip break detect mechanism. The other discrete signals control the serial scan path through the I/O cells.

The SPC data register is in series with a RAM address register and I/O pad scan. The SPC data register is connected to the internal bus to gain access to the RAM register file as well as a data break point feature. The point of connection is the Y bus from the ALU back into the RAM.

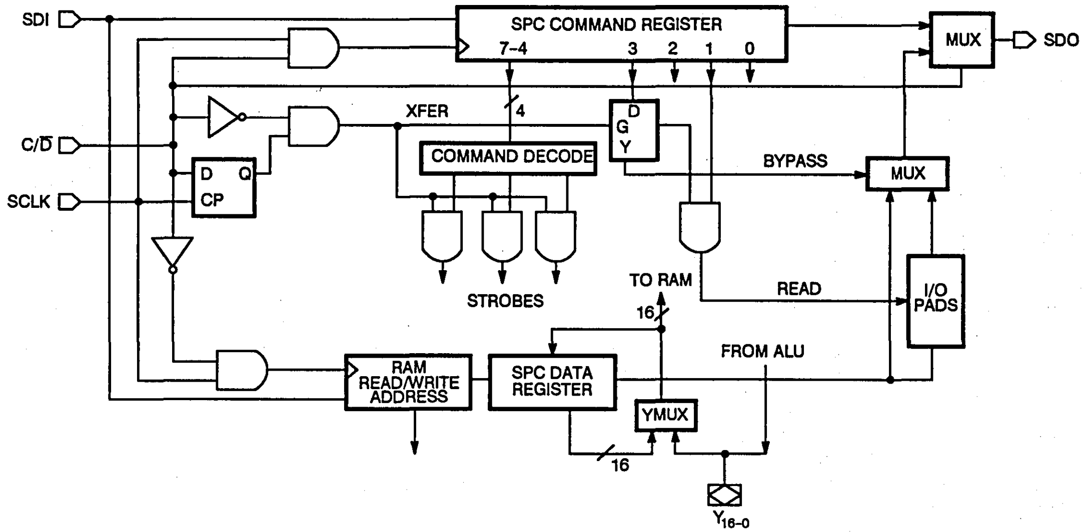


Figure 19. Internal Organization of the SPC

The multiplexer at the output transmits information via the SDO pin selecting data from either the SPC data register and the I/O pads or the command string from the SPC command register.

IDT49C403 SPC Command Opcodes

The SPC command register consists of an 8-bit field, as shown in Figure 13. Bit 1 enables the READ function of the I/O pad cells. Bit 3 enables the BYPASS function to bypass the I/O pad cells and scan out only the RAM address and data registers. Bits 0 and 2 are reserved. Bits 4 through 7 form the opcode field for reading and writing into the device.

The 4-bit command opcode field gives 16 possible command opcodes. The first 8 are reserved for writing data from the SPC data register into the registers and RAM on the device. The second 8 opcodes are reserved for reading data from registers and RAM into the 16-bit SPC data register.

COMMAND OPCODES	
OPCODE	FUNCTION
0	Write RAM
1	Write Q Registers
2	Write Break Control
3	Write Break Data
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Read RAM
9	Read Q Registers
10	Read Break Control
11	Read Break Data
12	View Y
13	Reserved
14	Reserved
15	NOP

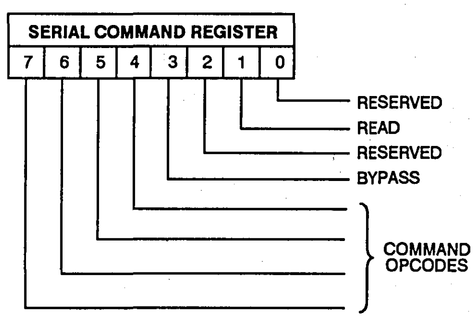


Figure 20. SPC Command Register and Opcodes for the IDT49C403

The command with opcode 0 causes a write to the internal device RAM. Opcode 1 is used to write to the Q registers. Opcodes 2 and 3 are used to write data from SPC data register into the break data register and break control registers, respectively. Opcodes 4 through 7 are reserved opcodes.

Opcode 8 is used for reading RAM data into the SPC data register. Opcode 9 is used to read a value out of the Q registers. (Here, also, the address register supplies the address of the Q register to be accessed). Opcodes 10 and 11 are used for reading the break control register and the break data register, respectively. Opcode 12 is used to strobe data from the Z bus into the 16-bit diagnostics data register. Opcodes 13 and 14 are reserved opcodes. The last opcode, 15, is a no-operation opcode. This opcode can be used to scan the data in and out of the I/O pad cells and use the device in a pass-through mode (in a cascaded application) without affecting normal device operation.

All the reserved opcodes, if executed, perform a no-operation; however, they should not be relied upon to always perform NOPs as future upgrades may make use of reserved opcodes.

Accessing the Contents of the IDT49C403 Register File

To read data from the device's internal RAM or other logic circuitry into the SPC data register, the address and don't care bits (for the SPC data register) are shifted in. The command is shifted into the SPC command register. The command register must be decoded to determine what data paths are to be steered in order to get data into the SPC data register. The read strobe, generated by the strobe logic, must then strobe this data (in parallel) into the SPC data register. The data can now be shifted out via the SDO pin and its contents disassembled and observed.

To perform the write operation, address and data must first be shifted into the SPC data register. The command is then shifted into the SPC command register via the command mode. This register provides information as to what data paths are to be steered. The address is supplied by the address register in the data scan path. The write strobe is then generated between the time the C/$\overline{D}$ line is lowered and the SCLK line is raised. This is the strobe which actually clocks the data into the RAM or register in the device.

Pad Cell Scan Path

Each I/O cell on the IDT49C403 contains a flip-flop which can be used to store the state of that cell and then be scanned out. Figure 11 shows the logic configuration. The READ line is enabled by a bit in the SPC command register and gated by the XFER signal, thus loading the scan flip-flops in parallel. The SCLK is then used to scan the data out of the SDO pin in series with the address and SPC data registers.

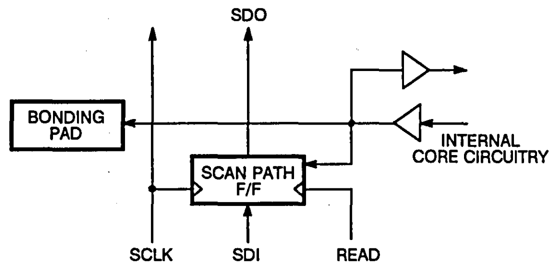


Figure 21. Serial Scan in the I/O Cell

0	Y15	25	$\overline{G}$/N	50	DB10	75	DA12
1	Y14	26	CN16	51	DB11	76	DA13
2	Y13	27	15	52	DB12	77	DA14
3	Y12	28	16	53	DB13	78	DA15
4	Y11	29	17	54	DB14	79	$\overline{LSS}$
5	Y10	30	18	55	DB15	80	CP
6	Y9	31	DCMP	56	$\overline{OEA}$	81	$\overline{WE}$
7	Y8	32	$\overline{MSS}$	57	DA0	82	B0
8	QIO15	33	DB0	58	DA1	83	B1
9	SIO15	34	DB1	59	DA2	84	B2
10	QIO0	35	DB2	60	DA3	85	B3
11	SIO0	36	DB3	61	DA4	86	B4
12	$\overline{OEY}$	37	DB4	62	DA5	87	B5
13	Z	38	DB5	63	DA6	88	Q0
14	W/$\overline{B}$	39	DB6	64	DA7	89	Q1
15	Y7	40	DB7	65	A0	90	$\overline{WRITE}$
16	Y6	41	$\overline{OEB}$	66	A1		
17	Y5	42	CN	67	A2		
18	Y4	43	I0	68	A3		
19	Y3	44	I1	69	A4		
20	Y2	45	I2	70	A5		
21	Y1	46	I3	71	DA8		
22	Y0	47	I4	72	DA9		
23	$\overline{IEN}$	48	DB8	73	DA10		
24	$\overline{P}$/N	49	DB9	74	DA11		

Figure 22. Shift Order of I/O Pad Cells

The BYPASS bit in the SPC command register selects whether the shifting of the I/O cells will be bypassed such that only the RAM address and data registers are scanned out. When the READ bit is HIGH, data is transferred from the pins to the scan register when SCLK transitions HIGH after C/D has transitioned LOW. The BYPASS bit in the command register is active HIGH so that a HIGH level bypasses scanning the I/O cells.

Figure 22 shows the order in which the I/O pad cells are scanned. The clocking will shift out the data on the Y_{15} pin first and continue in series until the WRITE pin is shifted out last.

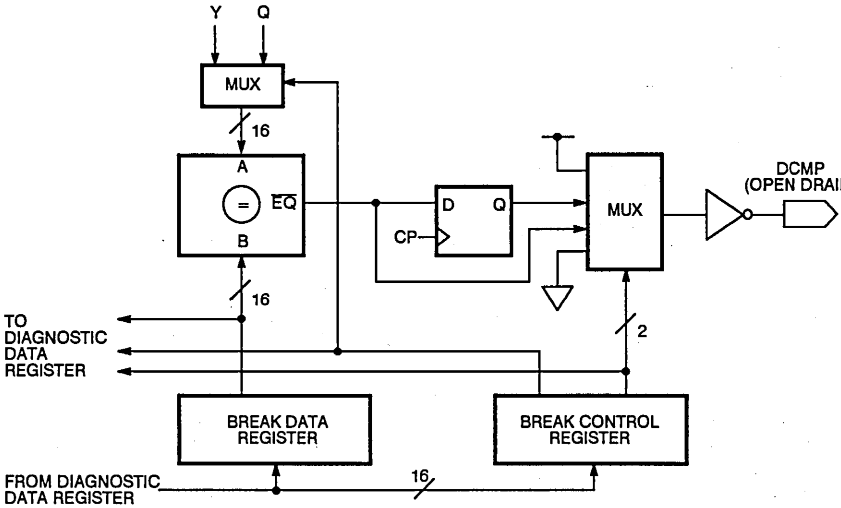


Figure 23. Breakpoint Detect Circuitry

Breakpoint Detection on the IDT49C403

Figure 23 shows the diagnostics breakpoint detection circuit on the IDT49C403. This circuit is designed to allow the user to monitor certain key data buses and detect the data patterns on the Y and Q buses. When a data pattern is detected, a breakpoint compare signal is generated on the DCMP pin and is used to halt the system operation. The DCMP is an open drain signal and should be wire-ORed with DCMP lines of other similar devices and monitored by the main sequencer in the system. The breakpoint detection mechanism thus allows for an easier debug of microcode with regard to the data path.

At the heart of the breakpoint detection circuit is a comparator which compares data from the break data register with data from either the Y bus or the Q bus. The break control register determines which of the two buses is selected for a comparison. The break control register also steers a multiplexer at the output of the comparator. This multiplexer selects between the equal-to signal, latched equal-to, V_{CC} or GND. The latched equal-to input into the multiplexer gives the user the ability to pipeline the match signal, thus shortening the system cycle time in the diagnostics mode. The V_{CC} and GND inputs to the multiplexer allow the programmer to disable the break compare feature by forcing the DCMP pin either LOW or HIGH, respectively.

When a match is made, the DCMP line goes HIGH. Thus, if any one slice in a cascade application does not match, the wire-ANDed DCMP will be low. Selecting V_{CC} via the multiplexer will disable matches altogether. To select GND, disable any one slice from the comparison.

Figure 24 shows the format of the break data and break control register. The break data pattern is 16 bits wide, with bit 16 being the most significant bit and last to be shifted in. The Break Control register contains three fields. Bits 0 and 1 control the DCMP output and bit 2 selects between the Y and the Q bus to be compared with the break data register. Bits 3 to 15 are reserved for future expansion.

14

BREAK DATA REGISTER FORMAT

15 ... 0
BREAK DATA PATTERN

BREAK CONTROL REGISTER FORMAT

15 ••• 3	2	1 0
•••	BUS SEL	DCMP CONTROL

BREAK POINT CONTROL ACCESS

BUS SEL	BUS
0	Y
1	Q

DCMP CONTROL		DCMP STATUS
0	0	LOW
0	1	PIPELINED
1	0	NON-PIPELINED
1	1	HIGH

Figure 24. Breakpoint Control Registers and Opcodes

Serial Protocol Channel Design Example #2

In order to fully understand the advantages and usage for the Serial Protocol Channel in debugging a typical set of hardware, a design example will now be presented. The design example chosen is a 16-bit computer design utilizing the IDT49C403 and the IDT49C410. This 16-bit ALU slice and 16-bit microprogrammed sequencer form the heart of an example 16-bit computer design that will be used to demonstrate the Serial Protocol Channel interface. Figure 25 shows a block diagram of the example design. The heart of the machine is an IDT49C403 containing 64 working registers and a high-performance arithmetic/logic unit. The IDT49C403 is a cascadable 16-bit microprocessor slice. In this example, it is used to hold all of the working registers, the program counter and stack pointer for this machine.

Example Machine

The bus structure for this computer design example consists of a 16-bit data bus, 16-bit address bus and 4-bit control bus. The control bus signals are memory request, I/O request, read/write and word/byte. Data from the 32K x 16 RAM main memory is received in the data-in (DI) register and the results to be sent to the main memory are output by means of a data-output (DO) register. Addresses are loaded into the Memory Address Register (MAR) and may come from either the Y bus or the DB bus of the IDT49C403. The right hand side of the block diagram of Figure 25 shows an instruction register organized as an 8-bit opcode, 4-bit source register (RS) select and 4-bit destination register (RD) select. These two 4-bit fields, as well as two 6-bit fields from the pipeline register, are multiplexed onto the destination address bus (403BSrc) and the source register select address bus (403ASrc). The microcoded portion of this example design consists of a IDT49C410, 16K x 96-bits of Writable Control Store (WCS) and 96-bit wide pipeline register. The IDT49C410 microprogram sequencer, WCS and pipeline register are connected in the normal state machine fashion, as shown in numerous available design examples. A 16-bit branch address field from the microprogram pipeline register feeds the D input to the IDT49C410 sequencer and also drives a mask register (MR) whose output is connected to the masks or 16-bit constants into the data path of the machine. Shift linkage and status control are provided by a 2904 and the design also includes an IDT7216, 16 x 16 multiplier connected to the DA, DB and Y buses of the IDT49C403.

The IDT49C410 sequencer, WCS and pipeline register are uniquely connected to an SPC load path. This load path utilizes two SPC channels and will be described in more detail later.

The example IDT49C403/IDT49C410 16-bit computer design uses a total of five Serial Protocol Channels. The five channels are depicted in Figure 26 and show the various registers connected in each channel. The exact partitioning used here was chosen out of convenience and as an attempt to learn as much as possible about controlling various types of four wire interfaces in an example design. As shown in Figure 26, Serial Protocol Channel 1 consisted of the 96-bit pipeline register and a 16-bit load WCS address register. All discrete registers in the example design are the IDT49FCT618. This is a 16-bit SPC register consisting of a 4-bit command, 96-bit pipeline register and 16-bit data register, as well as a 16-bit main data register. Since six of these IDT49FCT618 registers were used for the WCS pipeline register and one additional 16-bit IDT49FCT618 register was used for the load WCS address register, a total of 112 bits are required to load the serial data path and a total of 28 bits are required to load the serial command path for SPC Channel 1. The idea here is that, when loading the writable control store, the serial protocol processor will send first a 16-bit address followed by a 96-bit command word into the serial command path. It will follow this by sending a 28-bit command word into the serial command path. The appropriate control signals will then be toggled so as to execute a write of the WCS memory. This will be explained in more detail later and some example 68000 code will be shown for manipulating the various control lines. Channel 2 of the Serial Protocol Channel processor consists of three 16-bit IDT49FCT618 registers. These registers include the instruction register (IR), the MASK register (MR) and the data-in (DI) register. There is no particular design criteria for utilizing these three registers in series and the order in which they were connected was totally random. This path contains a 48-bit serial data channel and 12-bit serial command path.

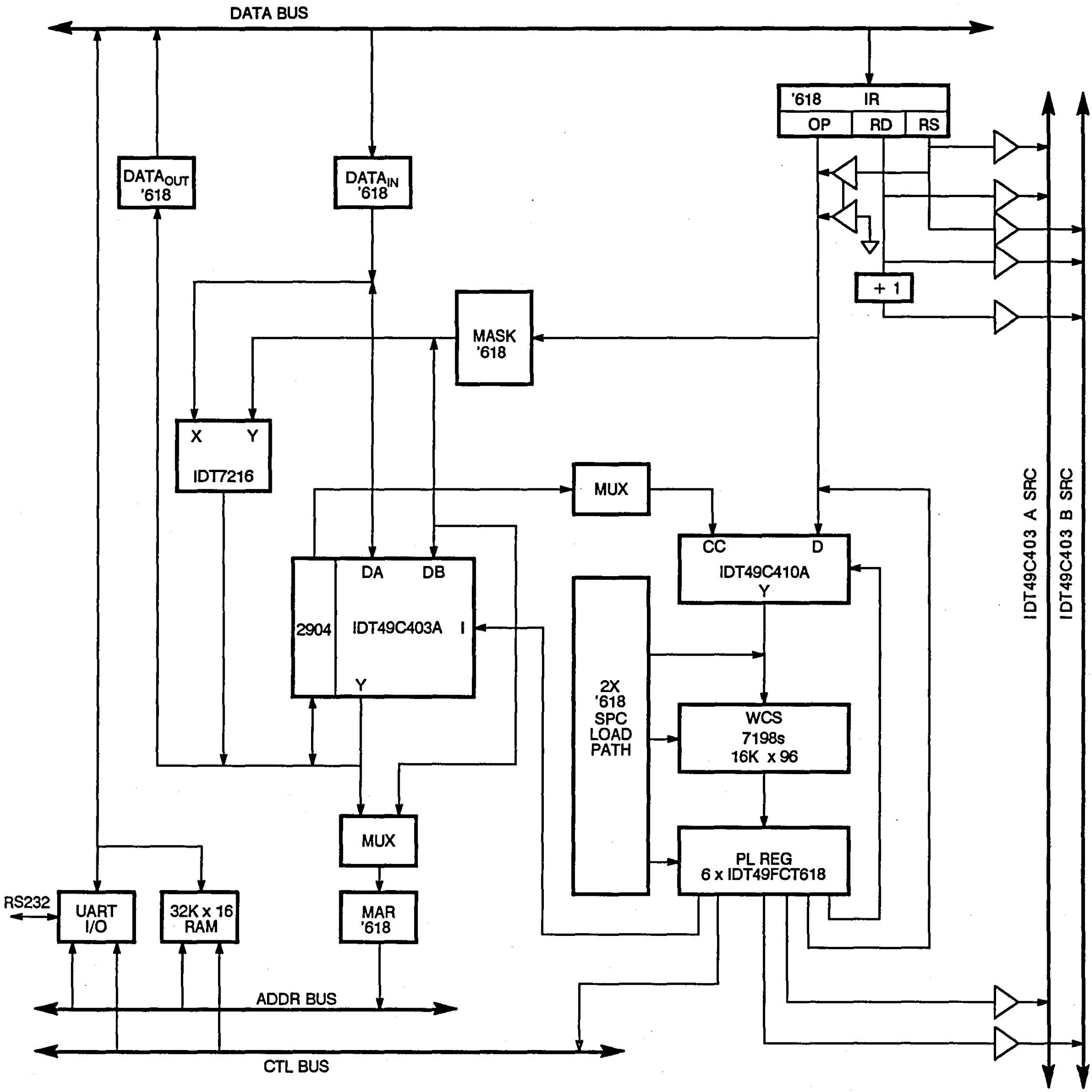


Figure 25. An Example of IDT49C403/IDT49C410 16-Bit Computer Design

14

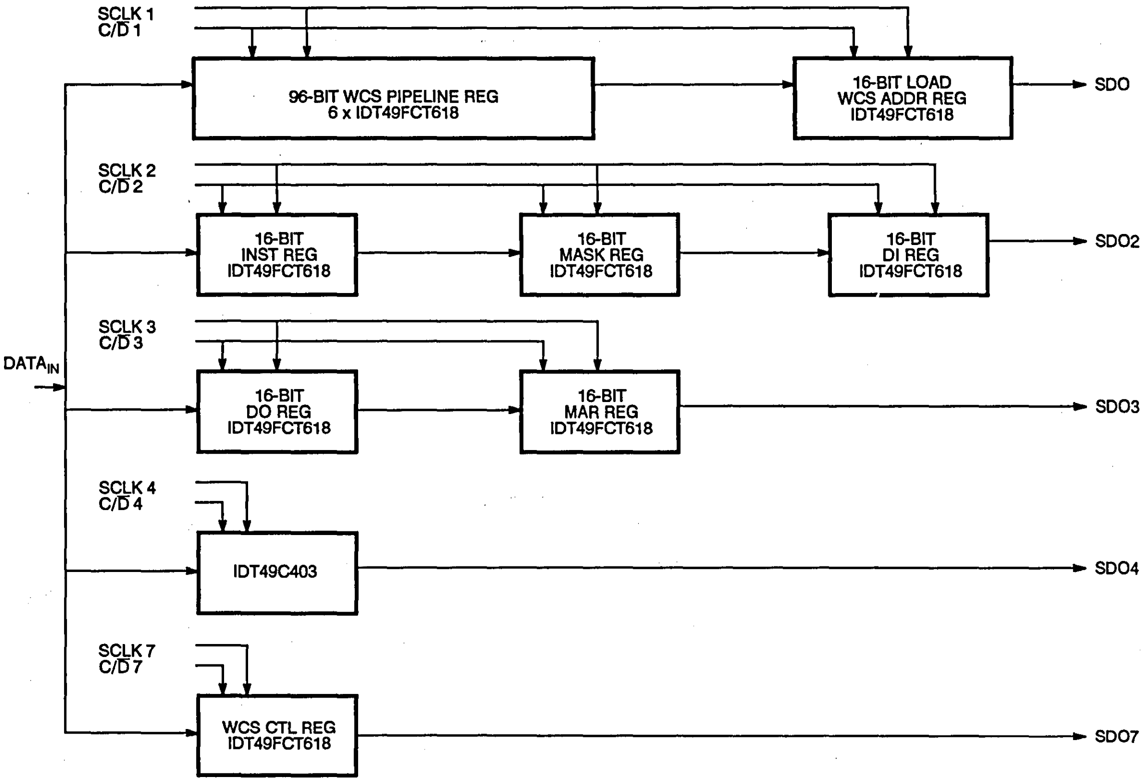


Figure 26. Five Serial Protocol Channels are Used In the Example Design

Channel 3 of the SPC connection (as shown in Figure 26) consists of a 16-bit data-out (DO) register and the 16-bit Memory Address Register (MAR). Two IDT49FCT618s are used for these registers and provide a total of 32 bits for the SPC data path and 8 bits for the SPC command path. This configuration was selected and placed on a separate SPC channel in an attempt to make the configuration look similar to the WCS channel. The reason for this can be seen by referring to the block diagram in Figure 25. The goal was to be able to write the 32K x 16 RAM from the SPC interface. By using the MAR register and the data-out (DO) register in the configuration shown in Figure 26, it was felt that much of the software for talking to this channel would be similar to the software required to talk to the WCS channel.

Channel 4 of the SPC interface consisted of the IDT49C403. This channel was kept as a separate channel in order to be able to conveniently interface to the data and command registers associated with the 16-bit slice. Since one of the goals of this design example was to build and test all of the theory behind serial protocol, we felt it would be desirable to be able to manipulate the command and data registers in the IDT49C403 independently. The IDT49C403 contains a 91-bit data channel and an 8-bit command channel.

The fifth channel of the SPC interface to the example 16-bit computer design is the WCS control register channel. This channel consists of one IDT49C618 register and is used to manipulate the output enable of the IDT49C410 and the output enable of the 16-bit load WCS address register of SPC Channel 1. It is also used to control the output enable and write enable of the 16K x 96 writable control store. This will be explained in more detail later.

From this description and by studying Figures 25 and 26, it should become obvious that a great number of registers in the 16-bit computer design example are available for reading, writing and examining by means of the SPC interface. In fact, all of the important registers associated with the design can be interrogated easily.

Next let's look at the actual hardware interface that was developed to provide the signals to the various SPC channels. A typical 68000 microprocessor design was utilized for the SPC interface. Figure 27 shows the 68000/SPC interface to the 16-bit IDT49C403/IDT49C410 computer design. A total of five SPC channels were used in the interface. The 68000 design contains EPROM, RAM and a UART connected to a standard CRT. A second UART was used to connect to an IBM PC in order to download assembled microcode and assembled machine code to be loaded into the example design by means of the SPC interface. The actual SPC interface consisted of some data output register bits for the command data lines, some output bits for the serial clock lines, one single data-out register bit and some data-in bits to be read from the serial interface channels. Figure 28 shows additional detail of the actual SPC interface. In actuality, a total of eight channels of SPC interface were designed, although only a total of five channels were used. Figure 28 shows that 74LS259 latches were used on the 68000 bus to provide the command data outputs for each of eight channels and a 74LS259 latch was used to provide the serial clock bit for each of the eight channels. Similarly, a 74LS251 eight input multiplexer was used for the data input path to the 68000 from the serial protocol channel and a 74FCT377 register was used to provide the data output bit. It is important to note here that only one data output bit was used and it is routed to the input of all the serial protocol channel data inputs. To date, no disadvantage has been found in doing this rather than utilizing eight separate data outputs. If the user so desires, he could use write separate data outputs. In summary, our serial protocol channel interface to the IDT49C403/IDT49C410 16-bit computer design example consists of five serial protocol channels utilizing five command data lines, five serial clock lines, five data-in lines and one data-out line. This means a total of sixteen active signals plus grounds.

It should be noted that the command data outputs, the serial clock outputs, the SPC data-out and SPC data-in signals are mapped vertically in the address space of the 68000 as opposed to horizontally across data bits of the 68000. This is not the way the design was started, but rather is the result of having written some example software. It seems that having a 16-bit word (register) used to control all of the serial clocks is a disadvantage. Thus, the hardware was redesigned so that all of the output bits utilized the 68000 data bit zero and are located at different addresses in the 68000 address space. This has turned out to be very convenient for the software and seems far superior to the original approach, although this could obviously be made to work. Note also that all of the data inputs are actually connected to data bit 15 of the 68000 design as opposed to data bit 0. This was done to cause the 68000 internal 16-bit data register to be conceptually connected in a serial loop with the protocol channel. Our approach to the software for SPC on the 68000 was basically to think and treat everything as 16-bit words in the 68000. This seems to work out quite nicely since the 68000 has a main memory that is 16 bits wide. Thus, we think of all words in memory as 16-bit entities and SPC channel words as strings of 68000 words in sequence. For example, the 112-bit writable control store and WCS address will be contained in a 68000 buffer consisting of a total of 7 words. The 28-bit command field of this same serial protocol channel will be contained in two 68000 words where the first word is 16-bits and the second word utilizes the 12 least significant bits. It turns out that 68000 software handles this quite conveniently and the bits can be shifted out quite conveniently through the serial hardware shown in Figure 28. We expect to have a single chip solution to the SPC interface in the near future.

When reading data in from the Serial Protocol Channel, we found it was most convenient to read the data in from the channel and begin loading in at data bit 15 and shifting the word down. Thus, after 16 read and shifts, a full 68000 16-bit word has been generated. This can now be stored in memory in a buffer and the next 16-bit field read in. We found it was most convenient to always read full 16-bit blocks from the Serial Protocol Channel even though a few of the last bits may actually be don't cares. This allowed all data words to always be aligned at the least significant bit boundaries and was the most convenient method for thinking of the Serial Protocol Channel command or data. We found that it was important to understand the mapping between the 68000 memory space and our various Serial Protocol Channels although it is not difficult to understand. We think of bit 0 and word 0 as being the first bit out and simply continue to output bits until the total number of BITSOUT is achieved. Each time a 16-bit increment is sent, we bump the address pointer to the next word boundary, read the word and then send out that data to SPC. Similarly, in reading in data, we read 16 bits at a time into an internal data register and then, at each 16-bit interval, output the word that has been received to the 68000 memory. Again, we bump the address pointer to the next word boundary and continue to receive input bits. These bits are loaded into the internal 16-bit register, starting at bit 15, and are then shifted down until a full 16-bit word has been generated. Thus, we always read in complete 16-bit words even though the last few more significant bits may be don't cares. This causes the words to be totally bit-aligned in 68000 memory and could be transmitted out without any additional 68000 manipulation.

While not shown in Figure 28, our hardware design actually includes the ability to read in the state of the command data bit and the SCLK bit from the 74LS273 latches. While we found this a convenient check in debugging our software, it is not required. However, our past experience has told us that it is always nice to be able to read a hardware register in a microprocessor system so we would probably continue to recommend that the path be provided to read these output bits back to the host processor.

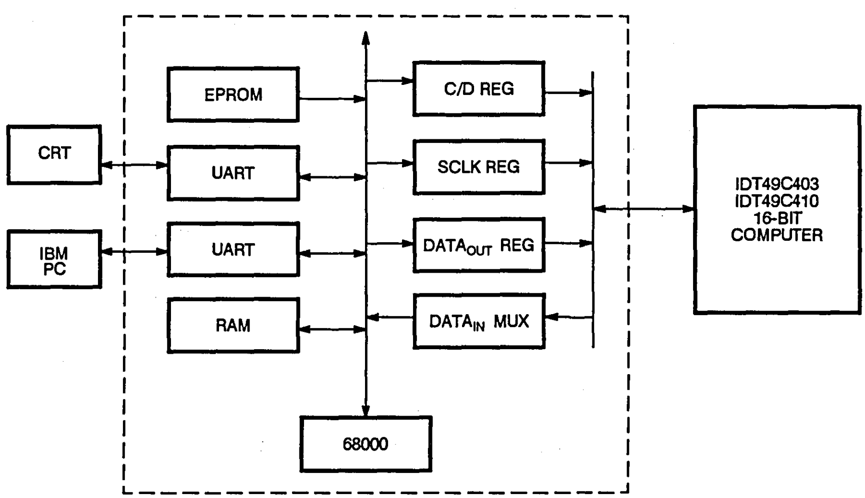


Figure 27. Example of a 68000/SPC Interface to a 16-bit IDT49C403/IDT49C410 Computer Design

14

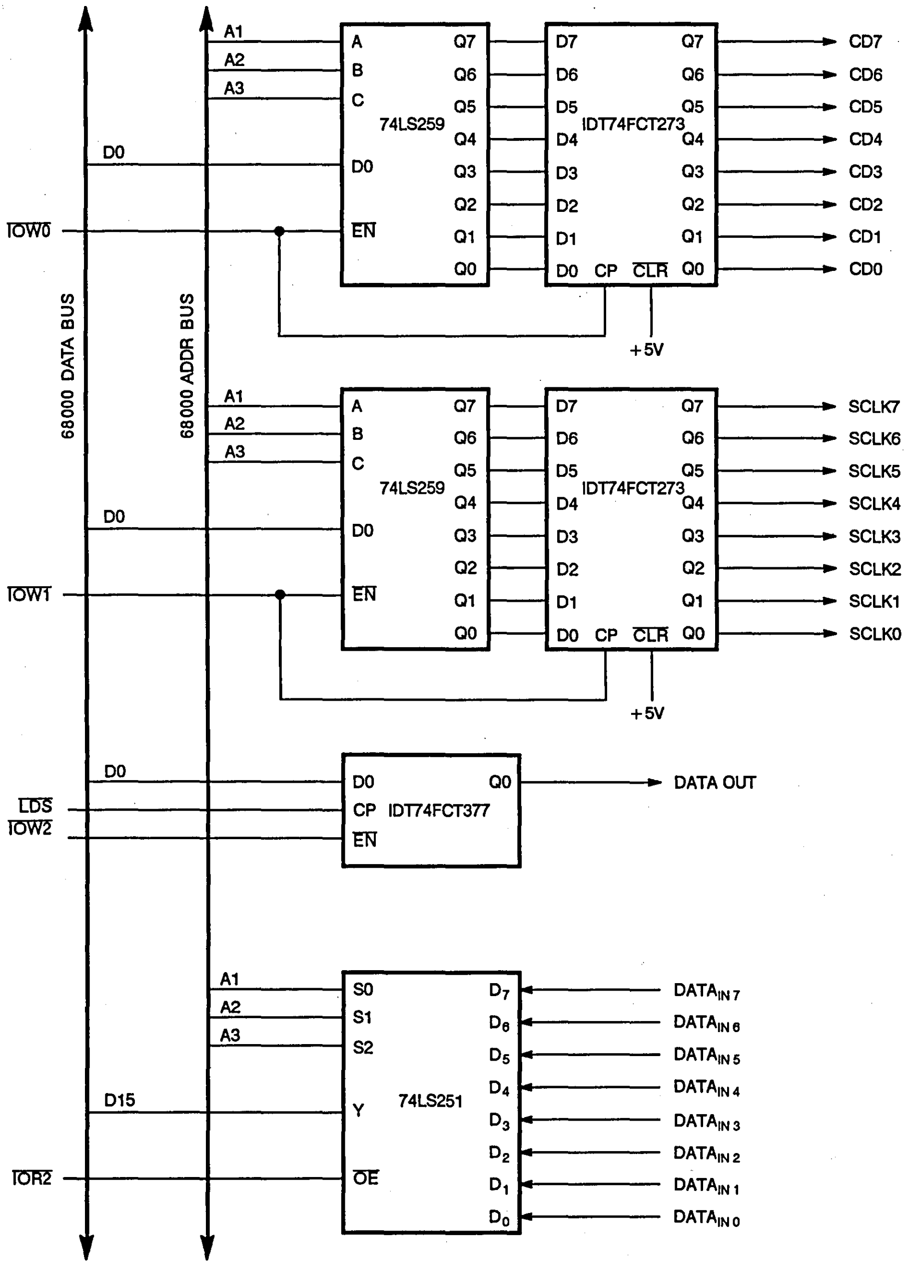


Figure 28. Detail 68000 to SPC Interface

Next, let's study the actual signals that we need to generate from the 68000 Serial Protocol Channel Interface. We will study this by simply looking at the SPC command/data, clock, data-out and data-in signals required for a single Serial Protocol Channel Interface. Referring to the waveforms in Figure 29, we see the required SPC signals. In our design, and we believe what should be one of the standard requirements for an SPC interface, the command/ data data line should always be kept HIGH when not in use and the serial clock line should always be kept LOW for consistency when not in use. If this rule is adhered to, we always know the starting input for a Serial Protocol Channel Interface and we can also guarantee that no command is currently being executed. Similarly, when we complete an instruction or a sequence of instructions, we should make sure that we always finalize the interface with an "execute" command so that no false executes will be initiated at the beginning of the next sequence. We believe this will be obvious after a future discussion about the Writable Control Store Interface.

Referring now to the signals in Figure 29, we see that if we had adhered to our rules of having C/$\overline{\text{D}}$ HIGH and SCLK LOW and we wish to send some data followed by a command to a Serial Protocol Channel, the following steps must be executed. First, we will bring the C/$\overline{\text{D}}$ line from HIGH-to-LOW to signal that data is going to be transmitted. Then we will output a data bit from the 68000 to the data-out flip-flop, as depicted in Figure 28. Then we will output a bit to set the SLCK HIGH and then the SLCK back LOW. Next we will change the data bit to a new value and again toggle the SLCK HIGH and back LOW. We will continue this sequence until the required number of data bits has been transmitted out the channel. In our design example in the case of Channel 1, we will output a total of 112 bits of data. Next, we will toggle the C/$\overline{\text{D}}$ line from the LOW state to the HIGH state. This will set the SPC to receive a command. Again, the data-out flip-flop will receive the first least significant command bit and then toggle the SCLK to HIGH and back LOW. This sequence of outputting a command bit and toggling SCLK will be repeated until all command bits have been transmitted. In the case of SPC Channel 1 in our example design, this would require a total of 28 command bits. At this point, if we wish to execute this command for this channel, we will bring the C/$\overline{\text{D}}$ line LOW, then cause the SCLK to go HIGH-to-LOW and then bring the C/$\overline{\text{D}}$ line back HIGH. This will complete the execution of the instruction just transmitted into this Serial Protocol Channel.

Similarly, Figure 29b shows the sequence for taking data out of a Serial Protocol Channel by means of executing a command that is input into the channel. The scheme here is similar to that described in Figure 29a. Remembering that we enter into the SPC frame with the C/$\overline{\text{D}}$ line HIGH and the SLCK LOW, we can begin by applying the first data output bit. Next we simply toggle SLCK HIGH and back LOW and continue this sequence until the correct number of command bits has been output into the port. After this has been completed, we bring the C/$\overline{\text{D}}$ line LOW which causes the device, such as the IDT49FCT618 register, to begin the execution of the command. This will result in the first data output bit being presented on the data-out line. At this point, we can do a 68000 read cycle of the data as depicted by the R in Figure 29b. What we are actually doing is executing the 68000 instructions required to read in this data bit from the Serial Protocol Channel and store it internally in a register in the 68000. After we have completed the read, we now toggle the SCLK HIGH and back LOW. This will have the effect of terminating the execute command inside of the IDT49FCT618. Since it is assumed we are executing some type of read command, the data will be loaded into the SPC data shift register inside of the device. Next, we read the second bit into the 68000 indicated by an R in Figure 29b. We follow this by toggling the serial clock line HIGH and back LOW, causing the internal SPC register to shift again. We repeat this sequence of instructions, reading the data bit into the 68000 and then toggling the SCLK, until all of the data is shifted into our 68000 processor system. If we were reading a word from the writable control store, this would require a total of 112 shifts to read the entire word. If we were reading a word from the IDT49C403, as connected to SPC Channel 4, it would require a total of 19 shifts. If we were reading a word from the data-out register and MAR register, as connected to Serial Protocol Channel 3, it would require a total of 32 shifts.

The Actual SPC Signals Generated by the 68000 Interface

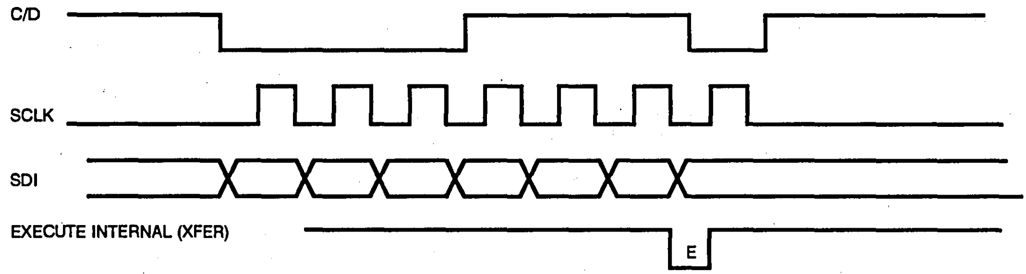


Figure 29A. Data Into SPC

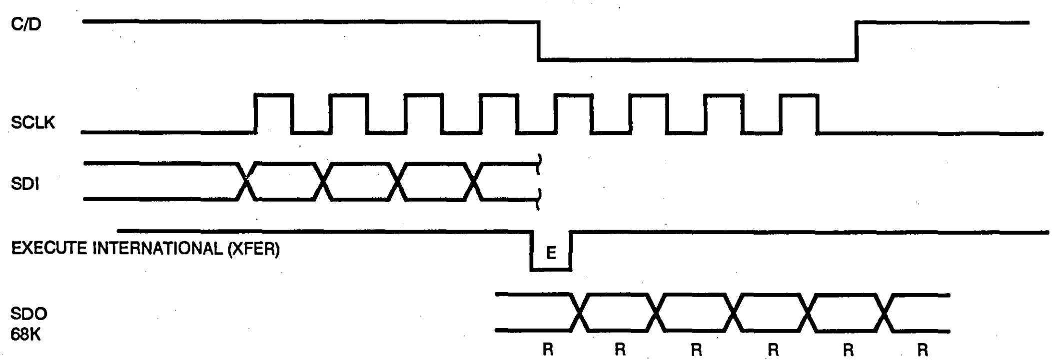


Figure 29B. Data Out of SPC

Example Software

Next, let's examine some of the actual 68000 code that we used to implement the Serial Protocol Channel Interface. First, let me explain that all of our software is stack oriented and we pass parameters and variables on a data stack that is pointed to by address register A6 in the 68000. Thus, we use register A7 as the normal return stack register and we use pointer A6 as a data stack pointer in our software. In addition, our software registers D0, D1, D2 and D3 are unprotected and are assumed to be destroyed by any subroutine call. Similarly, registers A0, A1 and A2 are unprotected and are also assumed to be destroyed by any subroutine call. This is always true except for a few very tightly coupled, very local subroutines that are part of a local larger routine or two special subroutine cases for A0 that we do not need to discuss at this time. Similarly, our software requires the user to protect registers D4, D5, D6 and D7, as well as address registers A3, A4 and A5, if they are to be used in the routine. Thus, these registers are always protected and can be assumed to remain correct after subroutine calls.

With this background, we can now examine a few of the key 68000 routines that we use to interface to the Serial Protocol Channel hardware. First, let's look at the routine we use for sending BITSOUT into the Serial Protocol Channel. The first software routine that we will examine is one that we call "BUFFOUT". This routine, Figure 30, will move the contents of a buffer pointed to by the address on the stack to the hardware port number that is on the stack. It will transmit the number of bits as contained in the word on the stack. Thus, our stack pointed to by register A6 contains three values. The first is a long word containing the hardware port number offset address; the second is a word containing the total number of bits to be transmitted; the third is a long word pointing to the buffer where the bits to be sent out are located. If we examine this routine, we will find that we always save and restore protected registers on the return stack. Thus, we enter a move multiple instruction as the first instruction and save the protected registers that we intend to use. Next, we see that we move the three passed parameters from the data stack into working registers inside the 68000. Since our goal is to send the "total number of bits", we need to figure out how many 16-bit words there are to be sent and then how many additional bits remain to be sent. This is achieved in our example code by taking the contents of register D5, moving it to register D6 and then rotating it down 4 bits. This will give the total number of 16-bit words in register D6 and will leave, after MASKING, the total number of remaining bits in register D5. Next, we hit an instruction sequence where we simply move the first word to the stack, as well as the number of bits to be sent, the hardware port number to the stack and call a routine called BITSOUT. This subroutine, (Figure 31), "BITSOUT", actually interfaces to the SPC hardware. If we study "Buff Loop" routine, we will find that we simply loop in this routine until we have sent all of the whole words to the BITSOUT subroutine. We then pass one more time in the routine called "Buff Words Done" to send out the remaining bits. Next, let us examine the routine called "BITSOUT".

```
This routine will move the buffer pointed to by the address on the stack
to the Hdw port number on the stack.

Registers Used: d4, d5, d6, a3
Stack: (Bufferaddr.l, TotalNumBits.w, HdwPortNum.l -- )
```

```
BuffOut:
        movem.l         d4-d6/a3,-(a7)    ;Save Reg

        move.l          (a6)+,d4        ;Hardware Port Number
        move.w          (a6)+,d5        ;Number Bits
        movea.l         (a6)+,a3        ;Buffer Pointer
        move.w          d5,d6           ;copy number of bits
        lsr.w           #4,d6           ;make d6 number of words
        andi.w          #$000F,d5       ;Upper part of bits = 0
BuffLoop:
        cmpi.w          #0,d6           ;count equal ?
        beq             BuffWordsDone
        move.w          (a3)+,-(a6)     ;Buff to stack
        move.w          #16,-(a6)       ;16 bits
        move.l          d4,-(a6)        ;Hardware Port number to stack
        jsr             BitsOut
        subq.w          #1,d6           ;bump count
        jmp             BuffLoop
BuffsWordsDone:
        cmpi.w          #0,d5
        beq             NoBits
        move.w          (a3)+,-(a6)     ;Buff to stack
        move.w          d5,-(a6)        ;Bits to stack
        move.l          d4,-(a6)        ;Hardware Port number to stack
        jsr             BitsOut
NoBits:
        movem.l         (a7)+,d4-d6/a3    ;Restore Reg
        rts
```

Figure 30. Routine to Send a Data Buffer Out to SDI

14

```
This routine will move the bits (or part-word) on the stack to the Hdw port
number on the stack.

Registers Used: d0, d1, d2, d4, d5, d6, a0, a3, a4
Stack: ( Data.w, NumBits.w, HdwPortNum.l -- )
```

```
BitsOut:
        movem.l     d4-d6/a3,-a4,-(a7)   ;Save Reg

        move.l      (a6)+,d4         ;Hardware Port Number
        move.w      (a6)+,d6         ;Number Bits
        andi.l      #$001f,d6        ;safety limit to 31, actual is 16 max
        move.w      (a6)+,d5         ;Data Word
        lea.l       BaseData,a3
        lea.l       BaseClk,a4
        move.w      d0,(a4,d4)       ;Set it LOW
BitsOutGo:
        move.w      #0,d0            ;Clock Low - use d0,d1 for
                                     ;speed,convenience
        move.w      #1,d1            ;Clock High
        clr.w       d2
BitsOutLoop:
        cmp.w       d2,d6            ;count equal ?
        beq         BitsOutDone
        move.w      d5, (a3,d4)      ;send character
        move.w      d1, (a4,d4)      ;SCLK - clock high
        move.w      d0, (a4,d4)      ;SCLK - clock low
        lsr.w       #1,d5            ;Next bit
        addq.w      #1,d2            ;bump count
        jmp         BitsOutLoop
BitsOutDone:
        movem.l     (a7)+,d4-d6/a3-a4   ;Restore Reg
        rts
```

Figure 31. Routine to Send a Data Word Out to SDI

This routine, "BITSOUT," will move the bits on the stack to the hardware port number on the stack. Again, three parameters are on our data stack when we enter this routine. They are the hardware port number address offset, the number of bits to be transmitted and the actual data word containing the bits. Once we have popped these parameters into 68000 registers D4, D5 and D6, we load our hardware BaseData and hardware BaseClock addresses into A3 and A4. After some other testing and initialization we finally arrive at the BITSOUT go loop. Here is where we actually transmit a data bit, contained in register D5, to the data-out flip-flop, then toggle the serial clock HIGH and then LOW at the appropriate channel. Finally, we shift the data word and then bump the bit count to see if we have completed the right number of BITSOUT. When we have transmitted the correct number of bits (note: the maximum should be 16 bits), we return from this subroutine. The return will actually be to the BuffOut loop where the next word will be set up in that loop.

The second key set of software for interfacing to our SPC hardware is the "Get SPC Data Subroutine." This routine will get data from the SPC hardware port and put it in a temporary buffer. Again, three parameters are passed to this routine on our operand stack. They include the hardware port number offset, the total number of bits to be input and the address of the temporary buffer in the 68000 address space. In studying this routine, as shown in Figure 32, we see we pop the parameters off the stack and set up our hardware base address registers. Then, we go to the "BitsIn Loop" where we actually get a bit and then toggle the serial clock HIGH and back LOW. Next, we MASK the most significant bit of the word we have just read because that is the actual data bit input from the SPC port.

We move it into the final destination register by first shifting this register and ORing in the actual data bit. We decrement the counter and branch to execute the loop again if we have not completed the entire total number of bits. Notice that, by means of the "MoreBits" external loop, we always read in full 16-bit words. Here, of course, the last few bits may actually be don't cares but the final word is indeed aligned on the least significant bit boundary for the useful bits.

While we're discussing software, let's review two additional useful small software routines. The first, depicted in Figure 32, is a routine called SPC Execute that will execute the command that has been transmitted to the C and D registers. It will use the hardware port number that it gets from the operand stack pointed to by A6. It will pulse the C/$\overline{D}$ and SLCK appropriately to cause a command to be executed. The timing is such that the C/$\overline{D}$ line will be brought from HIGH-to-LOW, then the SLCK will be toggled from LOW-to-HIGH-to-LOW and the C/$\overline{D}$ line will be brought back HIGH. This results in leaving the C/$\overline{D}$ line HIGH and the SLCK line LOW, as desired. The code simply consists of four moves to the hardware data ports on the 68000 and then returns to the calling routine. We call this little routine "SPC Execute." The other routine, shown in Figure 33, is even simpler. This routine will simply pulse a WCS control register to cause an actual write to the writable control store. The final details of this usage will be described later. What this routine does is simply pulse the Command/Data line (C/$\overline{D}$) on the SPC channel from HIGH-to-LOW and back to HIGH.

```
This routine will get data from the Spc Hdw port and put it in SpcBufl

Registers Used: d0, d1, d2, d4, d5, d6, a0, a3, a4
Stack: ( Bufferaddr.l, TotalNumBits.w, HdwPortNum.l -- )
```

```
GetSpcData:
        movem.l     d4-d5/a3-a4,-(a7)    ;Save Reg

        move.l      (a6)+,d4        ;Hardware Port Number
        move.w      (a6)+,d5        ;Number Bits
        movea.l     (a6)+,a3        ;Buffer Pointer
        lea.l       BaseCD,a0
        move.w      #0 (a0,d4)      ;set to data mode

        lea.l       BaseData, a4
        lea.l       BaseClk,a5
MoreBits:
        clr.w       d1              ;final word, set to 0
        move.w      #16,d2                  ;set for 16 bits
BitsInLoop:
        move.w      (a4,d4),d0      ;get a bit
        move.w      #1, (a5,d4)     ;SCLK - clock high
        move.w      #0, (a5,d4)     ;SCLK - clock low
        andi.w      #$8000,d0       ;mask to msb
        lsr.w       #1,d1           ;shift buffer down 1
        or.w        d0,d1           ;put in actual buffer
        subq.w      #1,d2           ;bump counter
        bne         BitsInLoop      ;16 bits yet?

        move.w      d1, (a3)+       ;put word in buffer
        move.w      #16,d0          ;16 bits done. Extra bits = don't care
        sub.w       d0,d5           ;Use d0 sub.w since subq.w is 8 max

        bpl         MoreBits        ;not done yet

        lea.l       BaseCD,a0
        move.w      #1, (a0,d4)     ;set to command mode

        movem.l     (a7)+,d4-d5/a3-a4    ;Restore Reg
        rts
```

Figure 32. Routine to Get Bits from SDO

14

```
This Routine will pulse the Wcs control register C/D H-L-H for writing. It will
use the hardware port number.

Registers Used: d0, a0
Stack: ( HdwPortNum.1 --- )
```

```
SpcWritePulse:
        move.1          (a6)+,d0        ;Hardware port number

        lea.1           BaseCD,a0       ;Base for CD hardware port

        move.w          #0, (a0, d0)    ;set to data mode
        move.w          #1, (a0,d0)     :set to command mode

        rts
```

```
This routine will execute the command in the C and D registers. It will use
Hdw port number from the stack. It will pulse the execute. CD = H-L-H,
Clk = L-H-L.

Timing is: C/D*     H H L L L H H
           Sclk     L L L H L L L

Registers Used: d0, a0, a1
Stack: ( HdwPortNum.1 --- )
```

```
SpcExecute:

        lea.1           BaseCD,a0       ;Base for CD hardware port
        lea.1           BaseClk,a1      ;Base for Clk hardware port
        move.1          (a6)+,d0        ;Hardware port number

        move.w          #0, (a0,d0)     ;set to data mode
        move.w          #1, (a1,d0)     ;clock high
        move.w          #0, (a1,d0)     ;clock low
        move.w          #1, (a0,d0)     ;set to command mode

        rts
```

Figure 33. Routines to Write Word to WCS

The Hardware

Next, let's examine the Writable Control Store (WCS) State Machine portion of our 16-bit example computer design. This is shown in more detail in Figure 34. What we see here is the IDT49C410 sequencer driving the address lines of the 16K x 96 writable control store. In this case, our actual design utilizes 16K x 4 IDT7198 RAMs. We use a total of 24 of these RAMs to achieve a 96-bit wide writable control store. We use six of the IDT49FCT618 registers to provide a total of 96-bits of pipeline register. A seventh IDT49FCT618 is used to provide an address to the writable control store when we are in the load or read Writable Control Store mode by means of the Serial Protocol Channel. We use an eighth IDT49FCT618 on a completely separate Serial Protocol Channel (Channel 7), to control the interface to the State Machine. This eighth IDT49FCT618 hooked to SPC Channel 7 is called the WCS control register. Let's examine its functions. First, bit Y2 is used to select the address source of the writable control store to be either the IDT49C410 sequencer or the IDT49FCT618 WCS address register. Thus, the Writable Control Store can get its source address from one of two points as controlled by this bit in the WCS control register. Bit Y0 is used to control the write enable line of the 16K x 96 writable control store, while bit Y1 is used to control the output enable of this WCS. Notice that we do not need or use the chip select on the RAMs in the writable control store so it is simply tied to ground. In normal execution for our 16-bit computer, we would expect that the write enable input to the writable control would be HIGH , the output enable to the writable control store would be LOW and the IDT49C410 sequencer would provide the address to the writable control store.

When we want to talk to the writable control store by means of the Serial Protocol Channel, the following events must take place. First, we will transmit a command by means of Channel 7 to the WCS control register where we will bring control of the address to the IDT49FCT618 WCS address register and deselect the ICT49C410 sequencer. However, we also need to know if this is going to be a read command for the WCS or a write command for the WCS. If it is a read command, we want to leave the WCS output enable LOW. If it is a write command, we want to bring the WCS output enable HIGH. Thus, it is obvious we need two types of WCS commands: a WCS read and a WCS write.

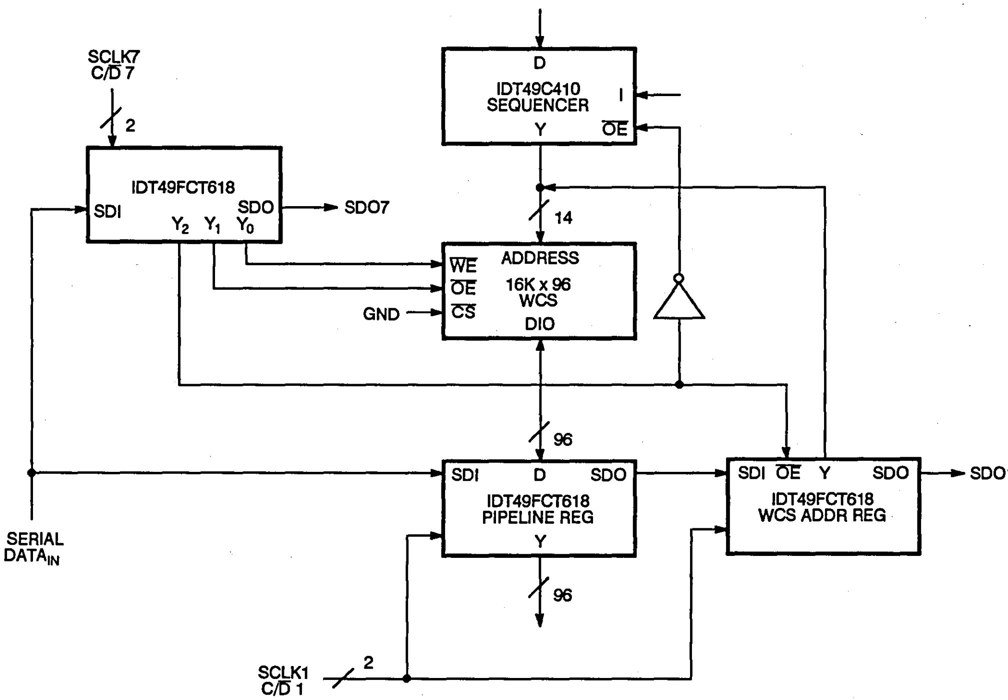


Figure 34. The WCS State Machine Portion of Our 16-Bit Example Computer

Writing WCS

Let's assume we wish to do a WCS write. We load the WCS command register with a bit to select the IDT49FCT618 address register and a bit to bring the output enable HIGH. The write enable should already have been HIGH. In this design, these bits are actually being stored in the main data register of the IDT49FCT618. A detailed diagram of the IDT49FCT618, for purposes of understanding the WCS control register, is shown in Figure 35. We will achieve this loading of the proper bits by first transmitting the data, then transmitting the command in the IDT49FCT618. The command we have entered into the IDT49FCT618 is command number 10 (HEX A) which will load the data into the main data register. Since our goal is to write data into the writable control store, we next need to send the appropriate address and data out Serial Protocol Channel 1 into the pipeline register and WCS address register. Without worrying about where the address and data actually come from, let's simply assume we transmit the data out the SPC Channel 1, switch to the command mode and transmit the command out Channel 1. Due to the method of interconnect of the WCS address register and pipeline register, the first 4-bit command will be opcode 8 while the next six 4-bit commands will be opcode 9. That is, we want to force the address data out the Y port on the WCS address register and the data out the D port on the pipeline register. Now we come to the tricky part. What must be accomplished at this time is the following. We need to bring the command data line of Channel 1 LOW to start executing the command that points the data and address toward the writable control store. After this, we must execute a command on SPC Channel 7 so to cause the write enable line on the WCS memory to toggle from HIGH-to-LOW and back to HIGH. This will write the data driving the WCS data and address lines into the memory. What we have found to be most beneficial is the following; when the original command that was loaded into the WCS control register selected the IDT49FCT618 and deselected the IDT49C410, we executed that command and loaded a HIGH,

14

HIGH, LOW into the main data register bits Y2, Y1 and Y0. Following that, we found it most beneficial to load the SPC data register (see Figure 35) with a LOW, HIGH, LOW for bits 2, 1, 0, respectively, and the 4-bit command register with command 8, the diagnostic register to Y command. This now puts us in the position of having the normal signals in the main data register and the write signals in the SPC data register, as shown in Figure 35. What we can do then is simply bring the command data line HIGH-LOW-HIGH and execute a write in the WCS. This will force the WCS write enable line from the HIGH state to the LOW state and back to the HIGH state. Then, we can complete the execution of the instruction of SPC Channel 1 by pulsing the serial clock HIGH, then back LOW and then bring the C/$\overline{D}$ line HIGH. An example of the 68000 code for executing this sequence is shown in Figure 33.

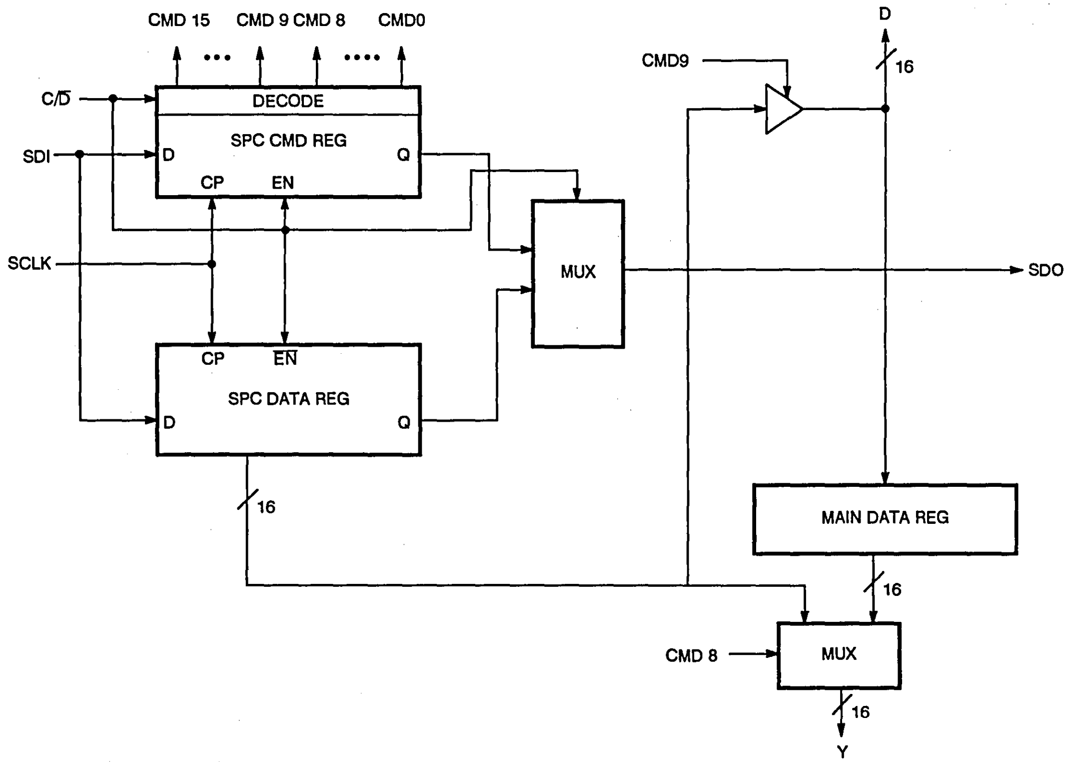


Figure 35. Detailed Diagram of IDT49FCT618 for Understanding WCS Control Register

Figure 36 shows the actual bit definitions for the 96 bits of microcode in this design example. If we study this bit definition and then review Figure 25, the block diagram of the design example, and Figure 26, the Serial Protocol Channel definition of the design example, we can arrive at an interesting conclusion. Channel 3 of our design utilizes the memory address register (MAR) and data-out register (DO) in a similar fashion to Channel 1. It turns out that the 96-bit pipeline register is the main control register to the 32K x 16 main memory. Thus, we have the same architecture for the 32K x 16 main memory RAM that we do for the writable control store. That is, we have both an address and data interface mechanism, as well as control bits that will control reading and writing. There are a couple of significant differences in that, in terms of the main memory control, we actually must be able to force a write without the use of the system clock. Thus, we have an architecture that will allow us to write main memory from SPC in much the same fashion that we write the WCS memory from SPC .

31 24	23 16	15 0
B SRC	A SRC	JUMP ADDRESS/MASK

63 62	61	60	59	58	57 56	55 54	53 52	51	50	49	48	47 46	45 44	43 42	41	40	39 36	35 32
410 SEQ D SRC	2904 CEM	7217 MULT				SYS BUS	MAR	LOAD REG			403 WD BY	Y BUS	Q REG	DB SEL	DA SEL	403 I_0	403 DEST $I_5 - I_8$	403 ALU $I_1 - I_4$
		MSPSEL	TWO'S	LD P	LD XY			DO	DI	MASK								

95 88	87 84	83 81	80	79 76	75 72	71 70	69 64
SPARE	MAIN BUS CYCLE	SPARE	IR REG	39C10 INST $I_0 - I_3$	2904 SHIFT $I_6 - I_9$	2904 CIN $I_{11} - I_{12}$	CC SEL

Figure 36. Definition of Microcode Bits

Serial Protocol Design Example #3

The following design example uses a 4K x 16 RAM identified as the IDT71502. The IDT71502 is a high-speed RAM with a pipeline register built into the output and includes an SPC channel for initialization and configuration. This design example shows how it is used and a simple circuit that can be constructed to initialize it from code stored in a slower access EPROM at system power up time.

General Description of IDT71502

The IDT71502 Registered RAM consists of a 4K x 16-bit RAM plus a 16-bit pipeline register and is designed for microcode writable control store use. A serial shift register system, the Serial Protocol Channel (SPC), is included on-chip for serial load and readback of the RAM data. A RAM address counter is also provided to speed up RAM load and readback. The SPC serial shift register is also configured to be used as a diagnostic register. The shift register can read all status conditions on the chip such as the RAM output, pipeline register output, data output pin state and RAM load/read counter value. A breakpoint comparator is included to support the diagnostic function. This breakpoint comparator can be used to detect a particular bit pattern in the RAM address or pipeline register outputs.

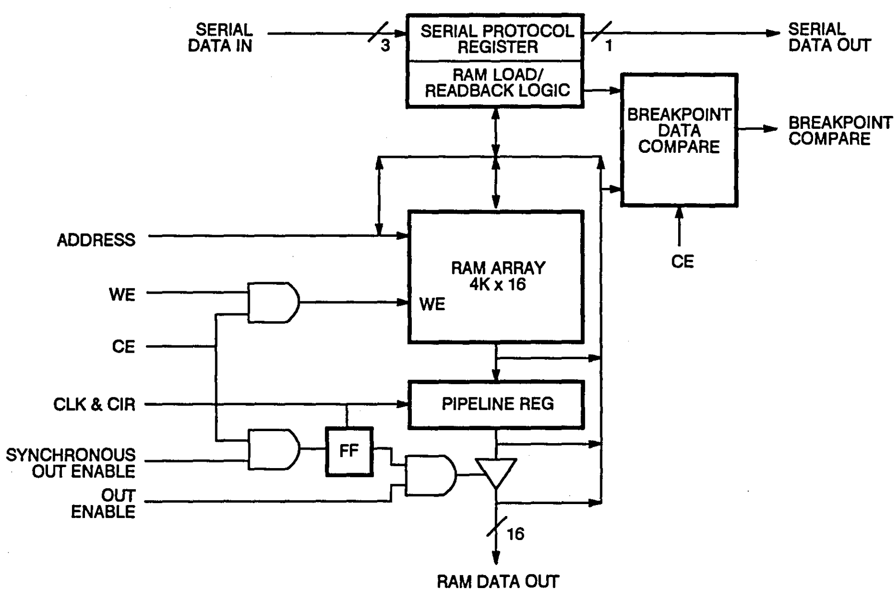


Figure 36. Block Diagram of IDT71502 4K x 16 Registered RAM

14

The IDT71502 Registered RAM includes features to support control store applications. These include synchronous output enable and an initialize register for selecting the initial value of the pipeline register. A parity output is provided which indicates the parity of the contents of the pipeline register. The parity output can be used to provide parity check control for high-reliability systems.

The IDT71502 RAM can also be used as a trace RAM for recording external data. In this mode, the data I/O pins are inputs and data is clocked into the RAM using the Initialize registers as the address counter. The trace mode, in combination with the breakpoint comparator, allows the IDT71502 RAM to be used as a one-chip logic analyzer.

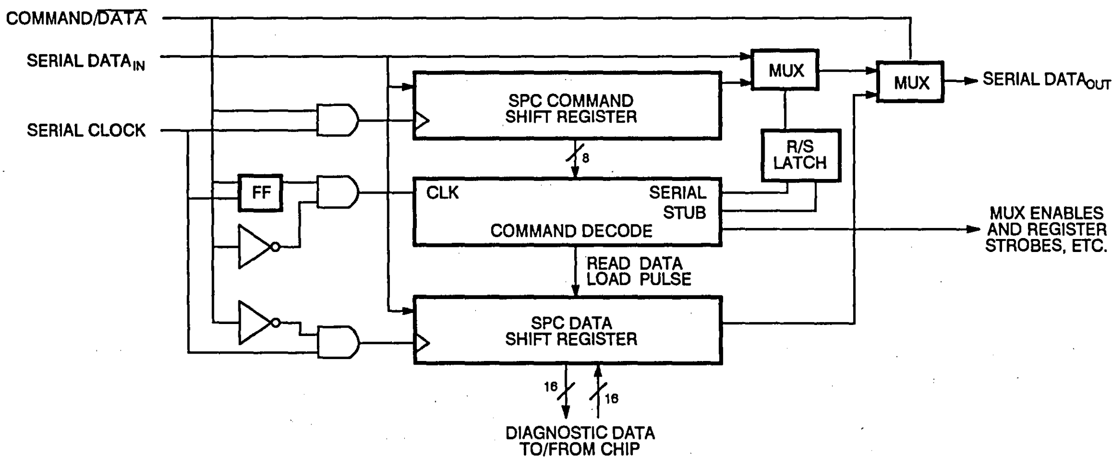


Figure 38. SPC Data and Command Registers for the IDT71502

The Serial Protocol Channel (SPC) logic consists of a 16-bit data shift register, an 8-bit command register and clock logic consisting of gates and a flip-flop. The command decode logic decodes and executes the command in the command shift register using the clock from the clock logic. The command is divided into two four-bit fields. The most significant four bits of the command register define the command to be executed: read, write, etc. The least significant four bits define the register to be read or written. (Note: The data to the SPC is shifted in LSB first.)

The block diagram shown below is a detailed schematic of the IDT71502 showing how the SPC channel connects to the various points in the device.

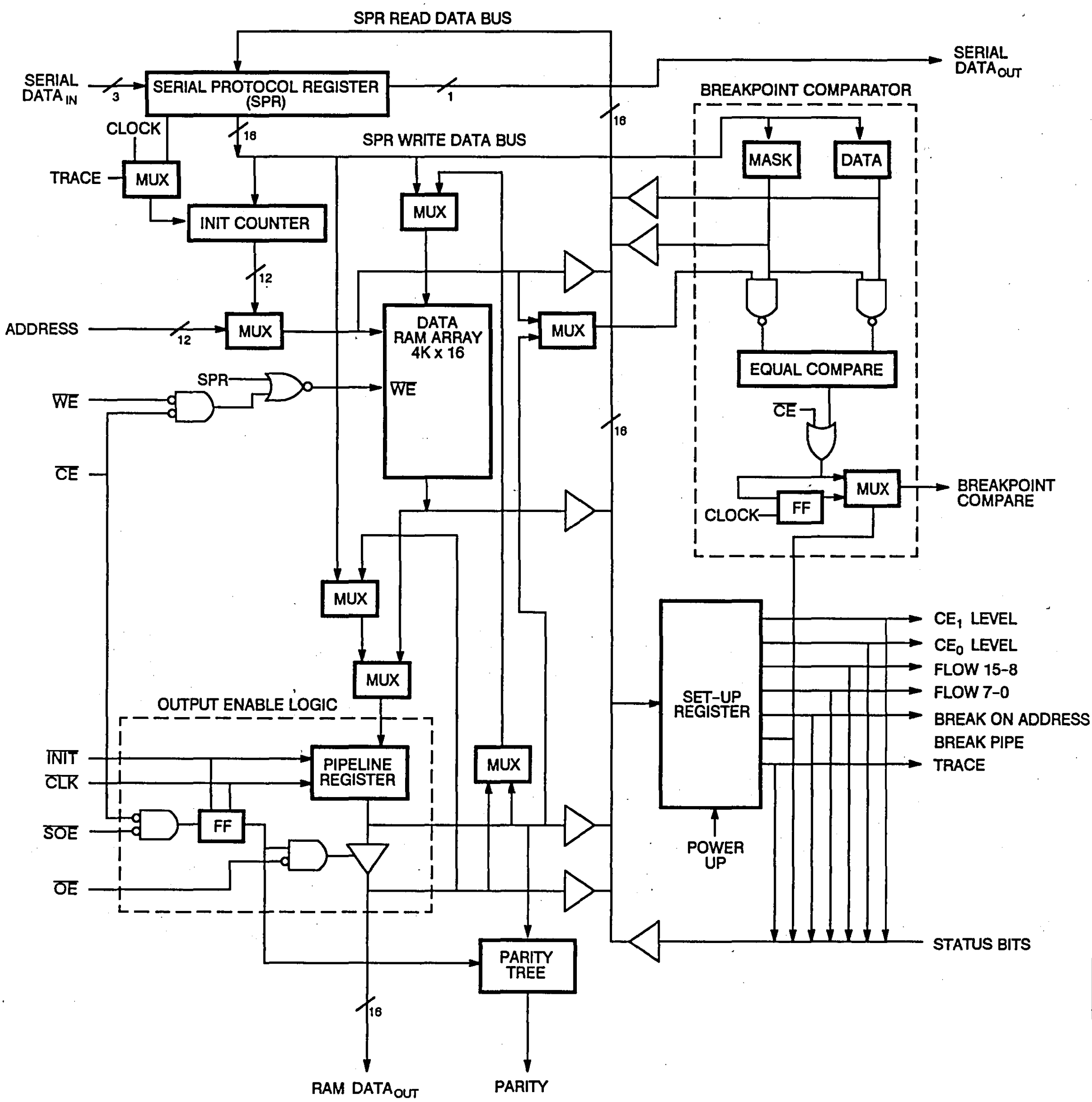


Figure 39. Detailed Block Diagram of IDT71502

Breakpoint Comparator Operation

The Breakpoint Comparator (BC) provides a masked 16-bit comparison of the various data paths that can be read by the SPC. It consists of an equal-comparator and the Break Data and Mask registers, as shown in the Breakpoint Comparator Logic Block Diagram. The BC compares the data from the chip against the data in the Break Data register and activates the Breakpoint Compare output if the two are equal. The Mask register enables comparison. If a bit in the Mask register is a one, comparison is enabled on the corresponding bit in the Data register; if zero, the comparison on that bit is disabled: i.e. forced to equal.

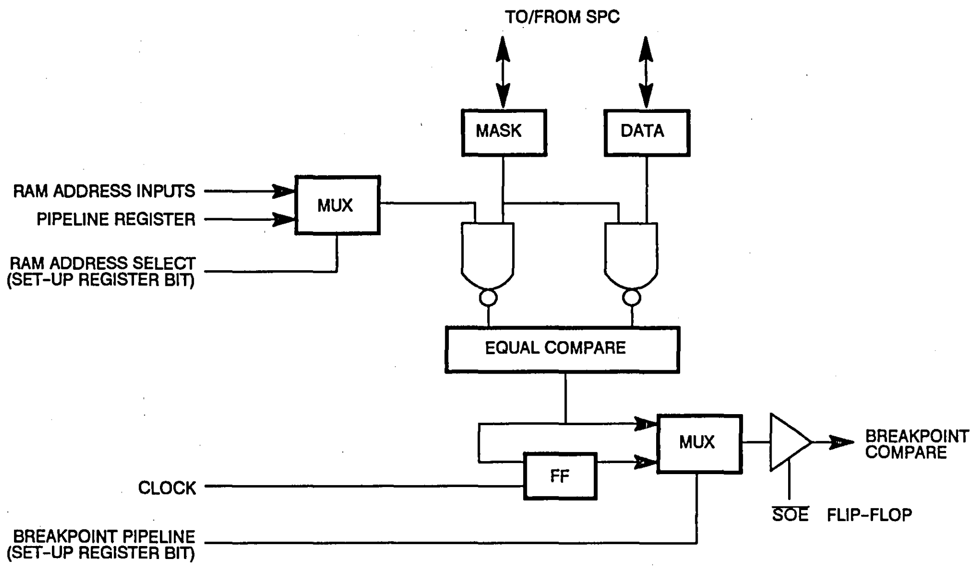


Figure 40. Breakpoint Comparator Logic Block Diagram

Trace Mode Operation

When the Trace bit in the Set-up register is set, the chip is in the Trace mode. In this mode, data from the chip data pins Y15-Y0 is written into sequential locations in the RAM. The address for the RAM comes from the Initialize counter, which is incremented after each RAM write. The Trace mode is used to record external data events in the same manner as a logic analyzer. The Trace mode recording sequence is as follows:

1. Data from the I/O pins is written into the pipeline register by the clock
2. Data in the pipeline register is written into the RAM by a one shot driven by the trailing edge of the clock.
3. The Initialize counter is incremented by the trailing edge of the RAM write pulse.

Using Trace Mode as a Logic Analyzer

The Trace mode allows the IDT71502 to be used as on on-board logic analyzer for system diagnostics. It is particularly powerful when used in conjunction with the breakpoint function. In the Trace mode, data is recorded in sequential locations in the RAM as controlled by the Trace counter. Since the incoming data is clocked into the pipeline register, the set-up and hold times are short and compatible with capturing changing bus data, for example. A block diagram of a system with an IDT71502 used in the Trace mode is shown in Figure 41.

The breakpoint outputs from the IDT71502 devices in a system can be used to control the Trace mode writing. The breakpoint outputs are open drain types which provide a wire-AND function when connected together to a single pull up resistor. By tying the breakpoint outputs for the writable control store RAMs and the trace RAM, a breakpoint comparison can be made over the full microcode word plus the data bus contents. This comparison can be used to enable the trace write so that only data which occurred at the breakpoint times is recorded. This allows recording the data that was on the bus during each instance of an I/O write, for example.

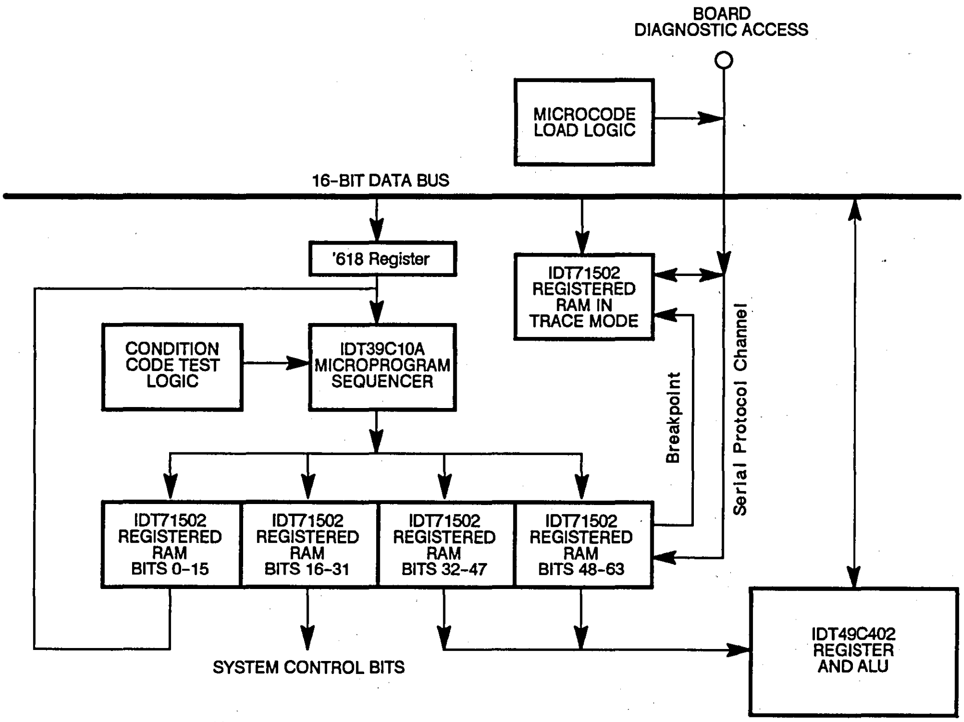


Figure 41. IDT71502 Used as WCS and Bus Trace

Using the Registered RAM in Writable Control Stores

The IDT71502 Registered RAM is designed expressly for efficient use in writable control stores. A simplified block diagram of a 16-bit microprogram controlled system using the IDT71502 is shown in Figure 41. The system shown uses four IDT71502 Registered RAM chips to provide 4K x 64 of microcode writable control store.

Serial Loading of the IDT71502 Using the SPC

In order to use the IDT71502 in writable control store applications, it must be loaded with the microprogram before use. This is done using the SPC. Loading the RAM over the SPC can be done in several ways. The microcode can be loaded from a central microprocessor which can perform both microcode load and system diagnostics at power up or it can be loaded using dedicated load logic.

An example of a design of this dedicated load logic is shown in Figure 42. The purpose of this example is to show how one goes about designing this logic. This example shows an approach which loads the RAMs with data from a single EPROM. The load logic gets its SPC command and data information from the EPROM. It is controlled by single byte instructions from the same EPROM. The format of these instructions is shown in Figure 43 and a map of the typical contents of the EPROM is shown in Figure 44.

The load logic consists of a 16-bit address counter, an 8-bit shift register, a 4-bit byte counter and a PAL containing a 2-bit instruction register. The logic in the PAL interprets the 2-bit load instructions to cause bytes of command or data information to be loaded into the IDT74FCT299 shift register and shifted to the SPC. The two IDT74FCT161 counters are used to count the bytes being sent and the 8 bits in each byte.

14

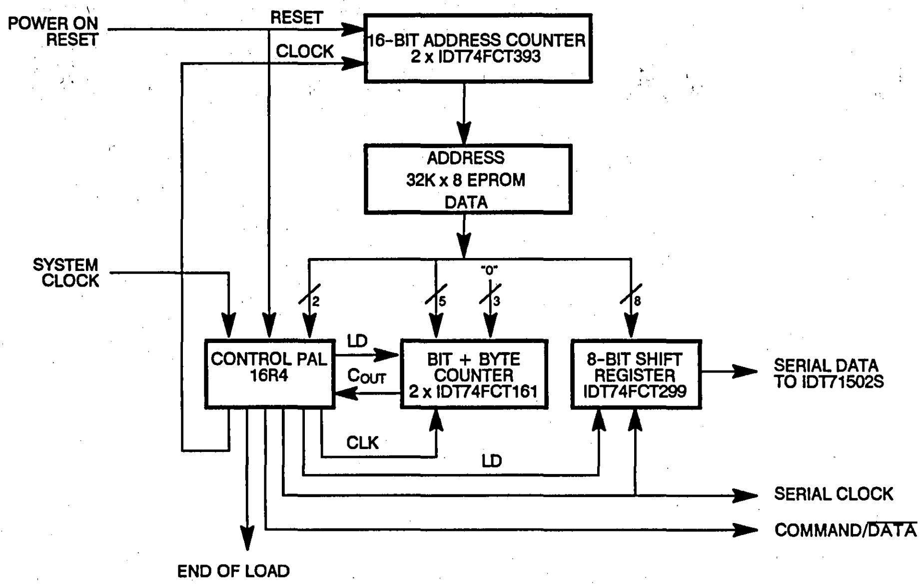


Figure 42. Microcode Load Logic Example

The format of the load logic instruction is shown in Figure 43. Each instruction consists of two bits of opcode and a byte count. The serial data that is shifted out of the automatic loader is always in multiples of 8-bits.

0	0	BYTE COUNT	LOAD COMMAND
0	1	BYTE COUNT	LOAD COMMAND USING SLOW CLOCK
1	0	BYTE COUNT	LOAD DATA
1	1	BYTE COUNT	STOP, END OF LOAD

Figure 43. Microcode Load Logic Instruction Formats

An example of some code is shown in Figure 44 in the form of a memory map. Each instruction to the loader logic is followed by data to be shifted out to the IDT71502. There is a block of commands followed by a block of data and so on.

EPROM ADDRS.	EPROM DATA			
0000	0	0	4	
0001	COMMAND BYTE 0			LOAD 4 COMMAND BYTES
0002	COMMAND BYTE 1			
0003	COMMAND BYTE 2			
0004	COMMAND BYTE 3			
0005	1	0	8	LOAD 8 DATA BYTES
0006	DATA BYTE 0			
0007	DATA BYTE 1			
	ETC.			
000B	DATA BYTE 7			
000C	0	0	4	LOAD 4 COMMAND BYTES
000D	COMMAND BYTE 0			
	ETC.			
XXXX	1	1	0	STOP, END OF LOAD

Figure 44. Microcode Load EPROM Memory Map

Summary

IDT's innovative Serial Protocol Channel has been architected in such a way that it can be easily implemented in many different applications. The cascading feature on the SPC not only allows a complete system debug and test, but specific blocks of logic can be tested by breaking the test program loop into multiple mini-loops, thus performing much tighter diagnostic checks.

Finally, as chip technologies continue their push towards more heavily integrated VLSI architectures, IDT has responded with the right tool for enhancing and simplifying in-circuit testing and diagnostics—the **Serial Protocol Channel.**

FIR FILTER IMPLEMENTATION USING FIFOs AND MACs

Integrated Device Technology, Inc.

APPLICATION NOTE AN-17

By Suneel Rajpal and Dave Wyland

INTRODUCTION

This application note shows a relatively simple method of implementing an N-tap finite duration impulse response (FIR) filter using FIFOs for the data and coefficient storage instead of space-consuming counters, RAMs and control logic. The multiply-accumulate operations can be performed by high-speed 16 x 16 multiply-accumulators (MACs) such as the IDT7210/7243.

Finite duration impulse response filters are popular in many DSP applications. FIRs have no feedback elements and no poles and they are unconditionally stable. Also, with FIRs one can have linear phase response that may be important for certain applications.

FIR filters are one of the basic building blocks of digital signal processing (DSP). The FIR filter uses digital components to perform the same function as analog filters. The FIR filter uses digital multipliers and accumulators to perform a series approximation of an analog filter. High-pass, low-pass and band-pass filters may be implemented. The digital FIR filter has several advantages over its analog counterpart. Its performance can be precisely specified and does not drift with time. Also, the filter type and performance can be changed with no change in hardware components and not introduce any amplifier noise. These features make the FIR filter popular in high-performance designs.

The FIR filter continuously processes (i.e. filters) the digital equivalent of the input analog signal. It does this by processing each input digital data word in a repetitive manner as a sum-of-products algorithm. In this algorithm, the current data word and some number of previous data words are each multiplied by a coefficient and the resulting products are summed. The filter type and performance are determined by the combination of the number of previous data words used and by the coefficients. The number of data words used is called the number of filter taps. An N-tap filter uses N data words and coefficients in the FIR calculation.

An FIR can be thought of as an average of incoming data values. Each of the successive data values is multiplied by its own coefficient and these values are totaled by an adder. A block diagram of this operation is shown in Figure 1. This sequence continues for each clock cycle as each data value advances one position and is multiplied by a new coefficient and a new sum is output. If one used a multiplier for every tap, a1 to a4, and an adder that added the four products (the multiplier outputs), a result can be obtained every cycle.

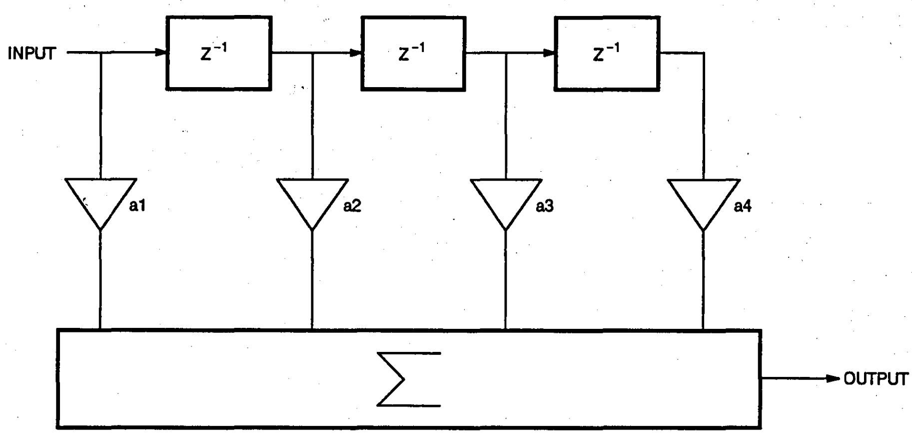


Figure 1. FIR Block Diagram

In many applications, only one MAC is used and the calculation is performed in 4 clock cycles for a four tap filter. If a single chip MAC is used, the appropriate data and coefficients are loaded to the MAC input registers. A new output results every four cycles, while a new input data value is loaded every four cycles. The hardware for loading the data and the coefficients is RAM with up/down counters and some logic. However, with the advent of FIFOs with asynchronous read and write capabilities and retransmit capability, one can have a better solution.

The IDT7201/7202 are high-speed 512 x 9 and 1K x 9 FIFOs that can be used to hold the data and coefficients for FIR filters. Higher density FIFOs such as the IDT7203/7204 (2K x 9/4K x 9) are also available. The IDT7201/7202, shown in Figure 2, are high-speed buffers that have an access time of 35ns and a cycle time of 45ns. These FIFOs support asynchronous and simultaneous read and write operations. On every falling edge of the write line, a new write cycle begins. The write pointer is incremented on every rising edge of the write line. On every falling read edge, a new read cycle begins and the read pointer is incremented on every rising read edge. The data is available after a delay of t_A (or 35ns for the highest speed part) after the falling read edge.

14

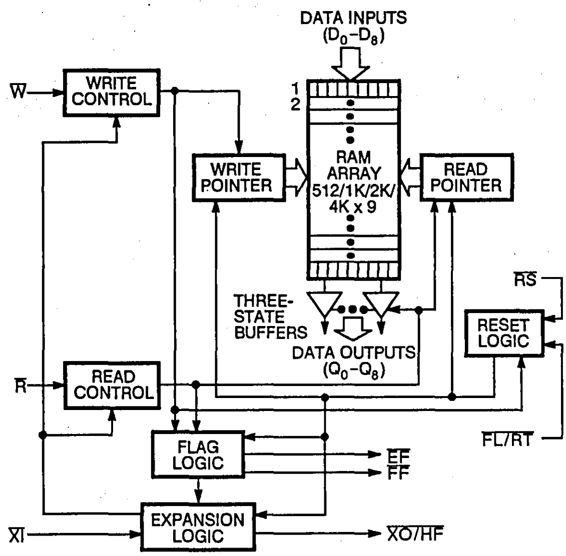


Figure 2. FIFO Block Diagram

The IDT7201/7202 FIFOs have a retransmit feature which is particularly useful in applications where the same data is repeatedly required. In a FIFO, N bytes can be written and then read. The retransmit feature allows the same N bytes to be read again without rewriting them. The retransmit feature resets the read pointer in the FIFO to zero, allowing a reread of the written information. If a FIFO is used to hold the filter coefficients, the retransmit feature can be used to reread the coefficients for each FIR calculation pass without having to reload them. Retransmit is performed by pulsing the retransmit input with the read and write clock lines high. This is shown in Figure 3 and, in greater detail, in Figure 7.

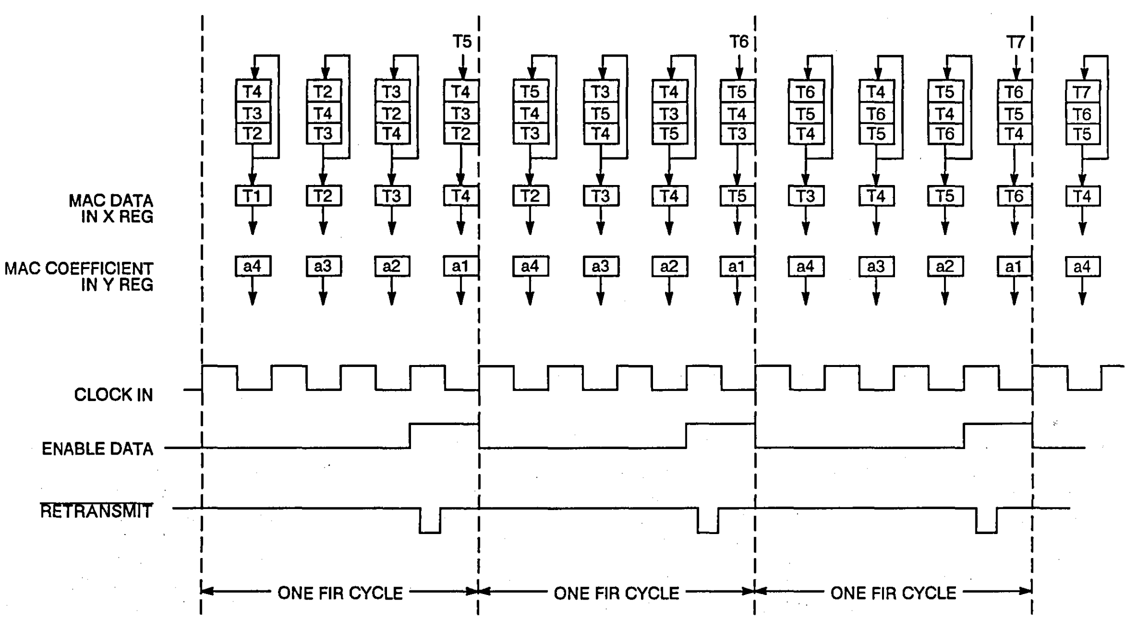


Figure 3. Sequence of Operations to Perform an FIR

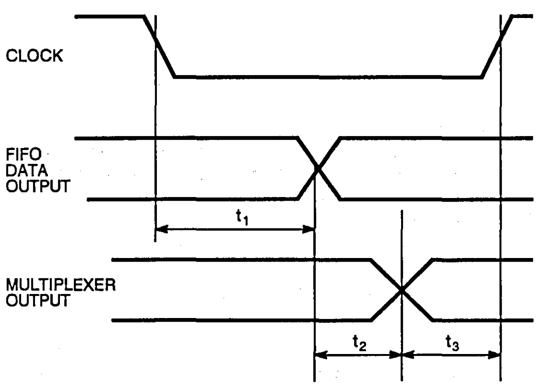
The clock cycle time can be at 120ns with a 50% duty cycle. For the data storage, the data is read from the FIFO, passes through the multiplexer and is then stored back in the FIFO. The delay path for the clock low time is as follows:

Read Going Low to Data on FIFO Output	35ns
FIFO Output to Multiplexer Output	5ns
Multiplexer Output to Write Going Low-to-High (Set-up)	18ns
Minimum Clock Low Time	58ns

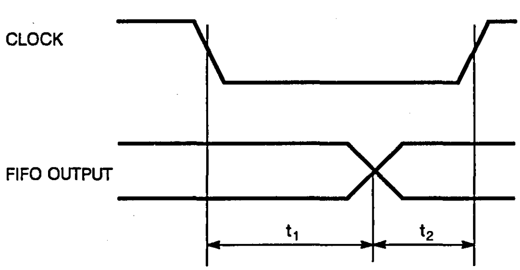
The delay path for the clock high time is as follows:

Control Circuit to Have RT Go From High-to-Low	10ns
Retransmit Minimum Low Time	35ns
Read and Write High Time After the RT Low-to-High	10ns
Minimum Clock High Time	55ns

Timing diagrams for these cases are shown in Figures 4 and 5.

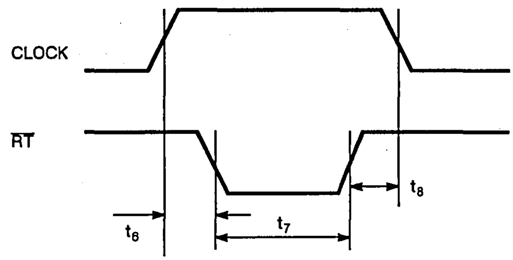


t_1 = FIFO Access Time, t_A = 35ns
t_2 = Multiplexer Delay = 5ns
t_3 = FIFO Input Set-up Time = 18ns



t_1 = FIFO Access Time = 35ns
t_4 = MAC Data Set-up Time = 25ns on 100ns (comm.) MAC

Figure 4. Clock Low Timings



t_6 = Time for External Circuit to Create $\overline{RT}$ Going From High-to-Low = 10ns
t_7 = Minimum Pulse Width for Retransmit Pulse = 35ns
t_8 = Read/Write High Time Requirement After the RT Goes From Low-to-High = 10ns

Figure 5. Clock High Timings

The MACs have input registers and an output accumulator. The MAC specification is based on the multiply-accumulate time or the time it takes for the input operands to be multiplied, the accumulator added or subtracted from this product and the result stored in the accumulator. The specification, called the multiply-accumulate time, is a register-to-register delay.

Another timing consideration for the data path is the set-up time for the MAC's input registers. In the case of the FIFO loading data to the MAC, the t_A of the FIFO plus the set-up of the MAC is 60ns (for the IDT7210/7243 100ns MACs) and this delay is equal to the suggested clock low time.

With the configuration shown in Figure 6, the clocked cycle time is 120ns at a 50% duty cycle using 35ns FIFOs (IDT7201/2) and 100ns multiplier-accumulators (IDT7210/7243). This system gives an output every 120Nns where N is the number of taps.

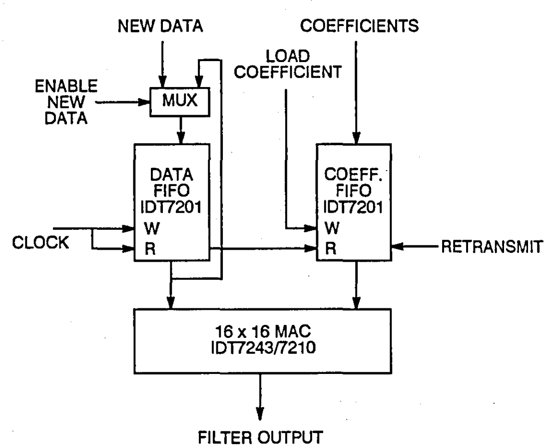


Figure 6. Logic Implementation of N-tap FIR

If the 120ns cycle time is considered slow for the user's application, a faster speed of 70ns cycle (60ns clock low and 10ns clock high) can be achieved. This is done by recirculating the coefficients through the FIFO using a multiplexer instead of using the retransmit feature, as shown in Figure 7. This is similar to the way the data is recirculated on the left side of Figure 6. The difference is that the coefficients are loaded into the FIFO initially from another source and, after loading, the FIFO output data becomes its input data (i.e., the input MUX selects the FIFO output to be the input after the initial loading of the coefficients). This configuration reduces the clock high minimum time requirement as the retransmit feature is not used. The clock low time does not change from the 60ns value.

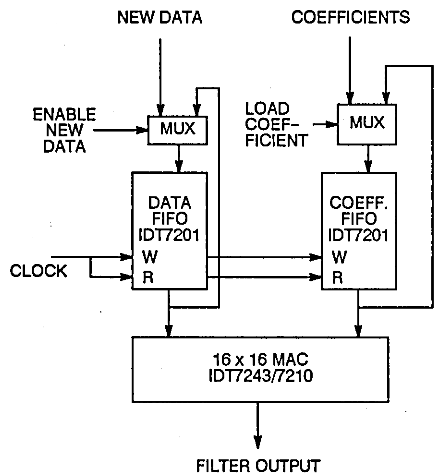


Figure 7. Logic Implementation of a Higher Speed N-tap FIR

The FIFOs used in this application have 35ns access times, but MACs faster than the 100ns used in the previous example have to be used. IDT has MACs that are as fast as 35ns clocked multiply-accumulate times and these would have to be used if the clock high time was only 10ns. The FIFO read and write minimum high times are also 10ns. This system yields a filter that gives an output every 70Nns where N is the number of taps.

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CONTROLLERS NEED MICROPROGRAMMING

APPLICATION NOTE AN-18

By Michael J. Miller

INTRODUCTION

Historically, mainframes and mini-computers were implemented using random logic for sequencing and control. In the course of improving performance, the instruction sets were enhanced which, in turn, made the random logic more complex. The more complex logic took longer to develop and was more difficult to debug and validate. Software came to the rescue in the form of microprogramming. The microcode replaced the random logic with the regular structure of ROM or Writable Control Store (WCS). This allowed for easier updates to the design which could even be performed in the field. Not surprisingly, the microprocessor community followed the same path of random logic for simpler processors to processors with complex instructions sets which are implemented through microprogramming.

The gains in microprocessor performance have slowed in pace and the implementation has again become very complex. Again, software has come to the rescue. There is a new trend today called RISC. Since programming techniques have made many recent advances more sophisticated, optimizing compilers are available. With these compilers the RISC community has opted to greatly reduce the complexity of the processor, eliminating microcode and relying upon the compiler to take advantage of using a much simpler but faster executing instruction set. Through this partitioning, it has been demonstrated that a much more efficient solution is realized for compiled languages such as C. This is shown through the numerous benchmarks circulating throughout the industry today.

Microprogramming has long since grown beyond being used just in CPUs. Today, microprogramming provides a technique to orchestrate the simultaneous parallel operations of multiple building blocks and the buses between them. In this way, algorithms that are implemented in a sequential fashion on a conventional CPU may be computed in parallel in multiple ALUs and buses. Today, these have been dubbed Very Large Instruction Word (VLIW) machines. Typically this technique is used in dedicated processors and controllers.

FAST, FLEXIBLE CONTROLLERS

Today's high-performance systems are composed of multiple processors and controllers working together. Several decades ago, in all but the most sophisticated designs, there was one processor doing everything. Now, the descendants of these systems are more like multicell organisms where each cell is interacting with other cells and performing a specialized task. For example, a work station today is composed of a central processor (CISC or RISC), a graphics/video controller, communications controller for ETHERNET or token ring, a mathematics accelerator and a disk controller (Figure 1). Except for the main CPU, all of the other elements are dedicated controllers. When performance counts, microprogram designs today can provide controller solutions that operate at more than 20 MIPS, which is an order of magnitude over what most fixed instruction set processors can provide today in controller-type applications. The fixed instruction CPU does the general purpose task at which it is good and coordinates the operations of multiple controllers which perform computation-intensive repetitive tasks.

The requirement for many of today's system designs to provide the highest performance possible means that there is a constant requirement for high-performance solutions such as microprogram architectures. The performance benefit, however, must always be traded off with the cost in terms of power consumed and number parts in design solution. The power and parts count for a solution provided by a given family of devices is directly related to the speed/power ratio of the technology used. The new wave of very-high-speed CMOS has entered the bit-slice world, thereby offering ever faster and denser functions. These new building blocks are, on the average, four to eight times as wide as 16- and 32-bit RALUs (ALUs with deep register files) and twice as fast at 1/4 the power of the previous generation of bipolar bit-slice. With the new ALUs and sequencers, the microprogram building block approach provides solutions that perform more than an order of magnitude faster at one to two times the parts count of a fixed instruction implementation.

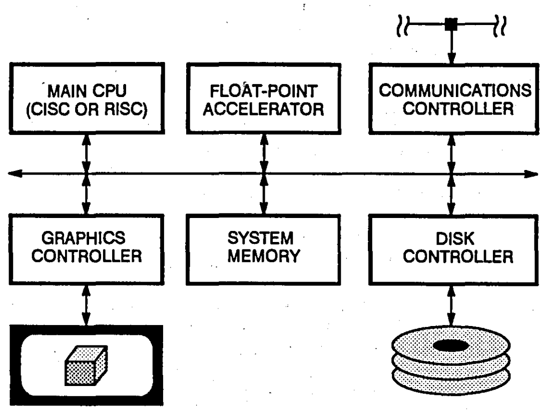
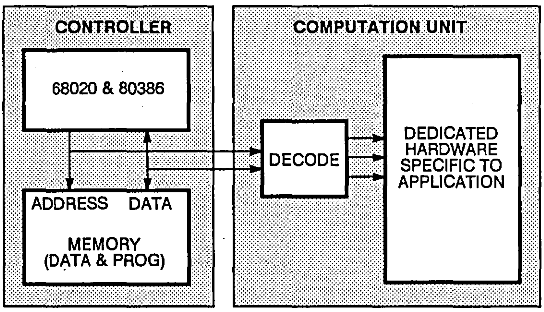


Figure 1. Typical Workstation Block Diagram

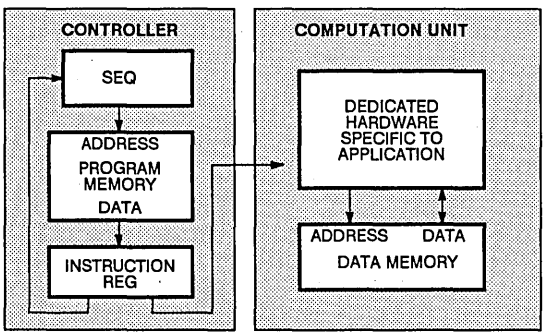
CONTROLLERS PROFIT FROM MICROPROGRAMMING

In order to understand why and where microprogramming is a very important solution for today's designer to use, one must compare the fixed instruction set processors (CISC and RISC) versus microprogram building block solutions. These two different approaches have major strengths in different areas. The fixed instruction set processors have mainly filled the niche of lower parts count solutions for general purpose computation. In the controller area they have serviced the low to medium performance solutions. Today, the microprogram bit-slice products have been utilized in very-high-performance control applications and emulation of specialized computer architectures. To see why, one must inspect the architectures (shown in Figure 2) more closely.

14



FIXED INSTRUCTION PROCESSOR SOLUTION



MICROPROGRAM SOLUTION
(HARVARD CLASS CONFIGURATION)

Figure 2. Comparisons of Microprocessors as Controllers

The fixed instruction set processors (like the 68000 family) fall into a class of machines referred to as the Von Neumann-type architecture which has an address bus and a data bus linking the processor and the memory together. These two buses are sometimes referred to as Von Neumann bottleneck because all data and program instructions must pass through the same address and data bus between the memory and processor, limiting the bandwidth because, at any given time, only data or program instructions can be fetched or written. The performance is therefore directly related to the bandwidth of this data path. For example, in a 25MHz 68020, for one memory access the clock must cycle three times, yielding 8 million data transfers in one second. To perform any instruction, the processor must fetch the opcode, source and destination designators and the data. This can be anywhere from two memory cycles to many and averages around 2 to 3 memory cycles. At a bus cycle rate of 8MHz, this results very simplistically in 2.75 to 4 MIPS. These theoretical numbers exceed actual benchmarks for the 68020. Through many years of optimizing the architecture and the instruction set, the fixed instruction microprocessors have become very good at performing general purpose type computations such as implementing operating systems, compilers, word processors and spread sheets. Because the instruction set is fixed and has been added to over the years, previous software written from these processors has been brought forward, making a very rich base of application software to solve all sorts of applications. Use of high level languages has made this process much easier.

The RISC approach is proceeding to take over large segments of these general purpose computing area. Major improvements have been made via various approaches, some of which include: 1) deeper pipelines, hence faster cycle times to match faster static RAMs; 2) separate instruction and data caches to allow the processor to fetch data and instructions simultaneously, improving on the Von Neumann bottleneck through an internal Harvard class-like architecture; and 3) large register files to avoid going off-chip for data. For a given level of technology, the RISC approach conservatively seems to provide two to three times the improvement current CISC. Not to be outdone, the newer CISC chips will start to incorporate many of these features on-chip.

The microprogram building block approach has many of the features that RISC has but with the flexibilty to fit into many different classes of bus architecture. In the simplest approach, one sequencer and ALU can be used with fast static RAM to form a Harvard class architecture similar to that used by the high-performance RISC designs. The microprogram approach allows instructions to be fetched at the same time that data is fetched. The ALUs incorporate such RISC features as simple orthogonal instruction sets, large expandable register files (32 and 64 locations) and single cycle operation.

The sole purpose of the sequencer is to generate a new address on every clock cycle. Thus, an instruction can be fetched on every clock cyle and placed in the instruction register. In the microprogramming world, the instruction register is referred to as the pipeline register. The pipeline register and memory can be from 32 bits up to 256 bits wide. The width of this register is tailored in each design in order to control multiple operations in parallel, tuning the performance to the required application. Unlike RISC, the microprogram approach does not use sophisticated MMUs, TLBs or caches. In real-time controllers, they only confuse the issue where precise cycle times are important.

Using today's technology, the IDT49C410 (16-bit microsequencer) can compute a next address in 16ns. Coupled with fast, 15ns static RAM (IDT6167) and high-speed registers (IDT74FCT374), sustained instruction fetch rates of 20 million times a second can be obtained. This sets a performance level for a simple bit-slice architecture at 20 MIPS. By using the VLIW approach, multiple operations can be performed in parallel and have a multiplying factor times the 20 MIPS. These very high rate instruction streams can be used in disk controllers, high-speed graphics engines, dedicated DSP architectures for radar/sonar, imaging devices, communications and robotics, to name a few.

The most economical, yet highest performance approach to utilize microprogramming in controller applications is to implement computation intensive and repetitive code with microprogram building blocks while relying on the host processor to provide all of the glue code. In this way, the tight inner loops are implemented in microcode. Since, in any given application the number of lines of code dedicated to tight inner loops is very small, the total amount of required microcode is reduced. The glue code which comprises the lions share of the code can be implemented in higher level languages.

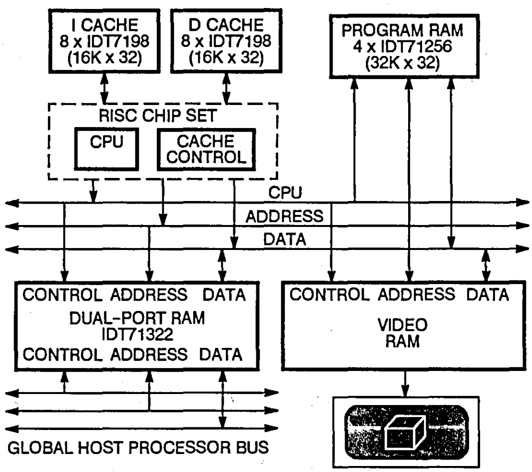


Figure 3. Graphics Applications Using RISC

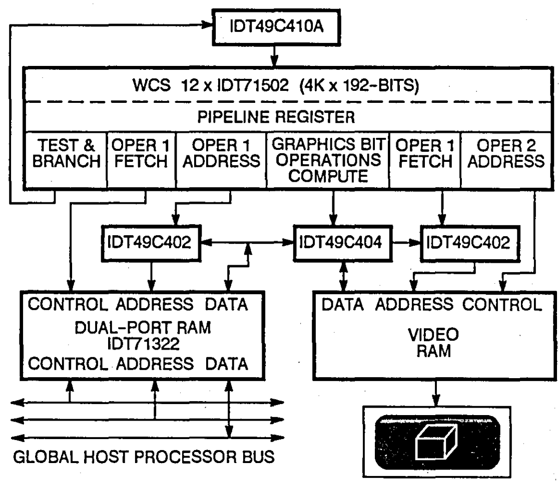


Figure 4. Graphics Applications Using Microprogram Building Blocks

BETTER GRAPHICS PERFORMANCE THROUGH MICROPROGRAMMING

A graphics controller provides a good example of a controller application for comparing the different approaches between RISC and microprogramming. One of the key tasks of a hypothetical graphics controller is to perform BitBlits to move ICONs in bit form out of the dual-port memory host system interface and into video memory at arbitrary bit offsets.

The block diagram shown in Figure 3 pictures a 32-bit RISC processor with instruction and data catches and program RAM for storing algorithms. When using a RISC solution, a program is written which performs the following loop of operations: 1) compute the address of a word of the ICON mask; 2) fetch a word of the ICON mask; 3) compute the address of the word in the video memory where the ICON mask will be merged; 4) fetch the word; 5) align the words; 6) merge the words; 7) store the result back into video memory; 8) test a loop variable and 9) branch. Optimistically, this loop might be performed in 10 instructions which, at 10 MIPS sustained, would yield 1 million loop iterations a second. Ten MIPS is used as an approximation because there is a maximum amount of data movement between locations in the dual-port and video RAM which cannot be cache. A more realistic approximation requires more instructions with the rate being half or a third of what is shown, thus yielding a rate 0.5 million iterations per second.

The same graphics application can be architected using IDT's CMOS microprogram building blocks as shown in Figure 4. It is comprised of a sequencer (IDT49C410A), registered writable control store RAMs (IDT71502 - 4K x 16), two 16-bit ALUs (IDT49C402A) to compute operand address and a 32-bit ALU (IDT49C404A) with register file, funnel shifter and merge unit to merge the graphics bits. In this solution the operands are computed, fetched, merged and stored in parallel. Although the fastest DRAMs (IMS2800-60) operate at a minimum cycle time of 120ns, two microprogram clock cycles of 60ns each can be utilized to form a DRAM read/modify/write operation in 120ns. This microprogram clock cycle equates to a 16.6MHz sustained instruction rate. Since two microprogram instructions are required to fetch, merge and store, the loop iteration rate is 8 million loops per second. This is an order of magnitude performance increase over the previously discussed RISC solution.

The architecture shown in Figure 4 would be very suitable in many graphics algorithms and could be considered a general purpose solution for high-performance controllers. The task would then be to microcode the graphics primitives such as vector, arc draw, shading and fill. The host processor would be used to compose the overall image through linking together the primitives.

Comparing part counts, the RISC solution requires on the average of two chips for the processor and two 32-bit blocks of fast static RAM (IDT7198, 16K x 4) for the cache. Both solutions use the same amount of dual-port and video RAM; therefore, the only differences would be in computation elements and static RAM. For the proposed microprogram solution, there are four VLSI chips plus 192 bits of static RAM for control store (12 x IDT71502, 4K x 16 registered RAM). As shown in Figure 5, chip count for the microprogram option is less than the RISC option. In this example, for the same number of devices, the microprogram building block solution offers a 10X performance improvement over the RISC alternative.

	COMPARISON	RISC	MICRO-PROGRAM
	Loop Interations	.5M	8M
PARTS COUNT	DRAM	EQUAL	
	DP RAM	EQUAL	
	Cache RAM	16	0
	Prog RAM	4	12
	VLSI	2	4
	Total of Non-common devices	22	16

Figure 5. Chip Count Comparision of RISC vs Microprogramming

14

Integrated Device Technology, Inc.

BUILD A 20 MIP DATA PROCESSING UNIT

TECHNICAL NOTE TN-02

by Michael J. Miller

INTRODUCTION

With the latest generation of CMOS devices from IDT, it is now possible for a user to design a data processing unit that will operate at 20 million instructions per second. The devices that make this possible are in the MICROSLICE™ family which provides such VLSI building blocks as sequencers and ALUs, a new generation of CMOS RAM devices which support 15ns access times and a memory interface family called FCT which is 20-50% faster than the equivalent functions in Fairchild FAST™. Putting these devices together, the designer can construct a microprogrammed machine which has a system clock speed of 20MHz. These microprogram designs can be used in a variety of application areas where high-speed processing and control sequences are required. Such application areas include dedicated graphics engines, digital signal processing, I/O controls for disk and tape, medical imaging, process control and special purpose computers.

BALANCED PATHS

For maximum performance and highest return on hardware investment, all critical paths should be as well-balanced as possible. Figure 1 shows a simplified block diagram of the basic structure of a microprogrammed machine. Microprogrammed machines are composed of static RAM, registers, latches and combinational logic. There are no dynamic elements involved. In the block diagram, there are three main elements: Next State Generator, Current State Register and Data Processing Element. The Next State Generator takes the current state information and generates the next state to be executed. The next state is stored into a Current State Register by the system clock on each clock cycle. Out of the Current State Register flow all control lines to the rest of the system. These control lines must control the next state generation as well as the Data Processing Elements. The Data Processing Elements might include such devices as fixed- and floating-point ALUs, register files and I/O devices. These Data Processing Elements can generate status information which also may be fed back into the Next State Generator such that the next state is determined by a combination of the current state and the current status.

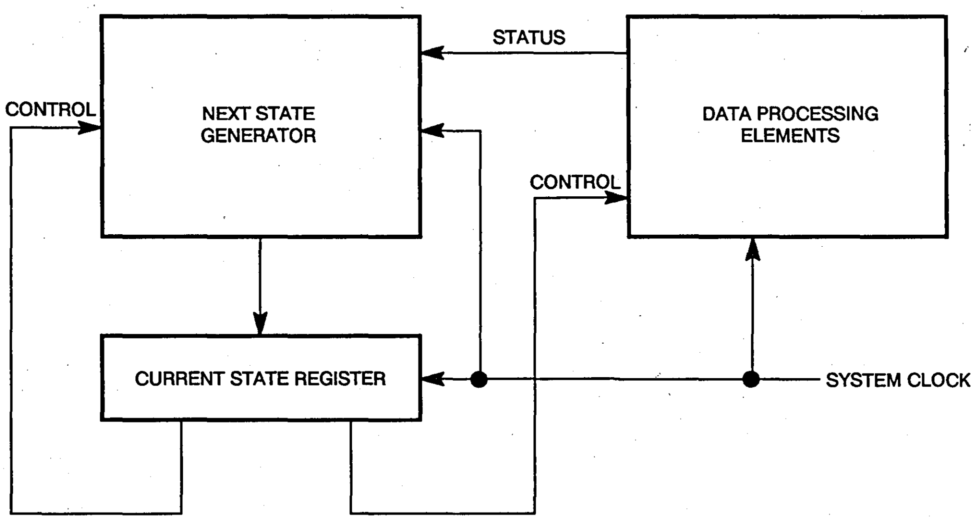


Figure 1. Simplified Block Diagram of a Microprogrammed Machine

MICROSLICE is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

Printed in the U.S.A. 9/87

Most designs generally have two critical paths. One path incorporates the time delay from the Current State Register, clocked by the system clock, through the Next State Generator and set up into the Current State Register. This is called the control path (Path B in Figure 2). The other path generally involved is from the system clock, through the current state output which controls the data processing elements to generate status and, in turn, effects the next state selected. This is called the data path (Path A in Figure 2). In order to break up the data path delay, the status can be put in a register rather than directly into the Next State Generator. For the highest performance designs, a status register is used. Therefore, when optimizing a microprogrammed design, these two paths must be taken into consideration and balanced for maximum performance.

CONTROL PATH

The control path can be designed using the IDT49C410A as the heart of the next state generation mechanism. Figure 2 shows the block diagram of a data processing unit using IDT devices. The IDT49C410A is used to generate the next address which is put into a RAM, referred to as a writable control store (WCS). Out of the WCS comes the next instruction to be executed and it is stored in a register built of IDT74FCT374A octal registers. This is the Current State Register and is often referred to as the pipeline register. The pipeline register can be viewed as containing several control fields: one for the IDT49C410A, another for the data processing elements, as well as additional fields for control of other elements in the system.

The field which controls the IDT49C410A contains instructions for the IDT49C410A as well as bits to control a multiplexer which selects status bits from a Current Status Register. The particular status bit which is selected out of the status register is used in combination with the instruction of the IDT49C410A to generate the next address. This latter path is the critical path. In the block diagram, the critical path in the control half is labeled as path B. All cycles start out with a system clock which generates a new instruction in 6.5ns using the IDT74FCT374A. This current instruction then controls the status MUX which can be constructed with a 74F151 using the Z bar output, which is the fastest output of the MUX. The propagation delay is 9ns. The condition code input on the IDT49C410A will then be combined with the instruction input and generate a new microprogram address in 16ns. This new address can then be used to access the next microprogram instruction in 15ns using the IDT6167A15 static RAMs. At this point in the cycle, the microprogram must be placed in the pipeline register with a 2.5ns set-up time. The total control loop then is 49ns, thus accommodating 20MHz operation in the control path.

THE DATA PATH

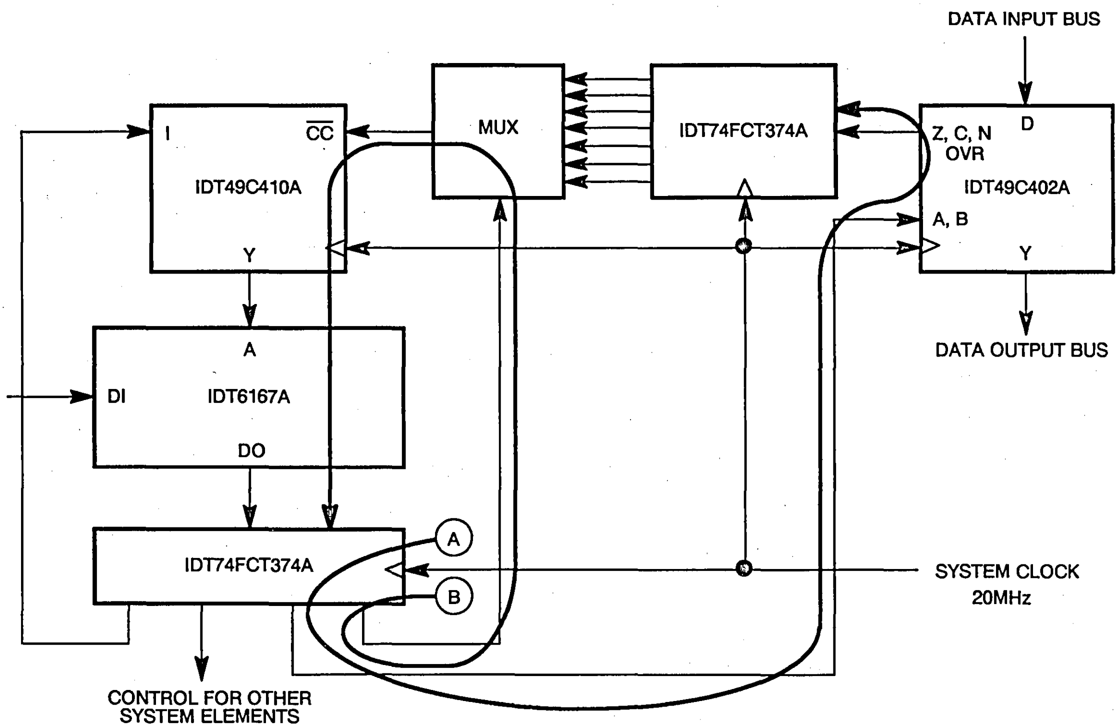
The other critical path in the data processing unit is the data path which includes elements for processing data. The data may, for example, be data coming off a disk controller, graphics information or DSP data, to name a few possibilities. Shown in the block diagram is an IDT49C402A which is a 16-bit cascadable binary ALU with 64 x 16 register file. The critical path starts with the system clock which generates a new instruction at the output of the pipeline register in 6.5ns. The field in the pipeline register is then fed into an IDT49C402A. This instruction controls the operation of the ALU unit as well as providing addresses to select operands out of the internal 64 word register file. As a consequence of the data coming out of the register file into the ALU and the ALU instruction inputs, a result is generated. The ALU result can be brought out on the Y-bus or stored back into the register file. Status flags which correspond to Zero, Sign and Overflow are also output. The instruction and A/B addresses delay to status flags and Y output is 37ns. The status flags require a 2.5ns set-up time into the status register. Therefore, this path totals 45ns (labeled Path A), matching the control path fairly well.

CONCLUSION

It can be seen that, by using the latest in CMOS devices from IDT, the designer is capable of creating a machine that can execute 20 million instructions per second. This type of performance is almost twice that achievable a year age using the 2900 family and corresponding devices. With the previous devices, the typical control path required 100ns to execute and the data path typically took 80ns to execute. This was using the fastest available devices implemented in bipolar TTL interface-type technology. Not only are the CMOS devices from IDT extremely fast, they also consume a minimum of power: 75 milliamperes for the IDT49C410A and125 milliamperes for the IDT49C402A. Each of the IDT74FCT374As typically consume 10 milliamperes. Therefore, it is not unreasonable to expect the designer to achieve a design which consumes about 1 watt for the ALU and sequencer shown in the simplified block diagram in Figure 2.

14

NOTE:
1. Times given are worst case maximum over commercial range.



Path (A)

CP -> Q	6.5ns
ABI -> Flags & Y	37.0ns
Set-up	2.5ns
Total	45.0ns

Path (B)

CP -> Q	6.5ns
MUX ('F151)	9.0ns
CC -> Y	16.0ns
RAM	15.0ns
Set-up	2.5ns
Total	49.0ns

Figure 2. More Detailed Diagram of a DPU Capable of 20 MIPS Using IDT MICROSLICE Parts

3232 Scott Blvd., Santa Clara, CA 95054-3090 • Telephone: (408) 727-6116 • TWX 9103382070

Integrated Device Technology, Inc.

USING THE IDT49C402A ALU

TECHNICAL NOTE TN-03

by Michael J. Miller

The MICROSLICE™ family consists of high-performance VLSI building blocks that provide such functions as ALUs, sequencers for building complex finite state machines, register files and support devices. The IDT49C402A is a member of this MICROSLICE family and is the first in a series of 16-bit ALUs from IDT. This high-speed ALU (shown in Figure 1) is capable of supporting 20MHz operations. This phenomenal speed is a result of CEMOS™, a single-poly double-metal structure using 1.2 micron gate lengths designed for high-performance and high-reliability.

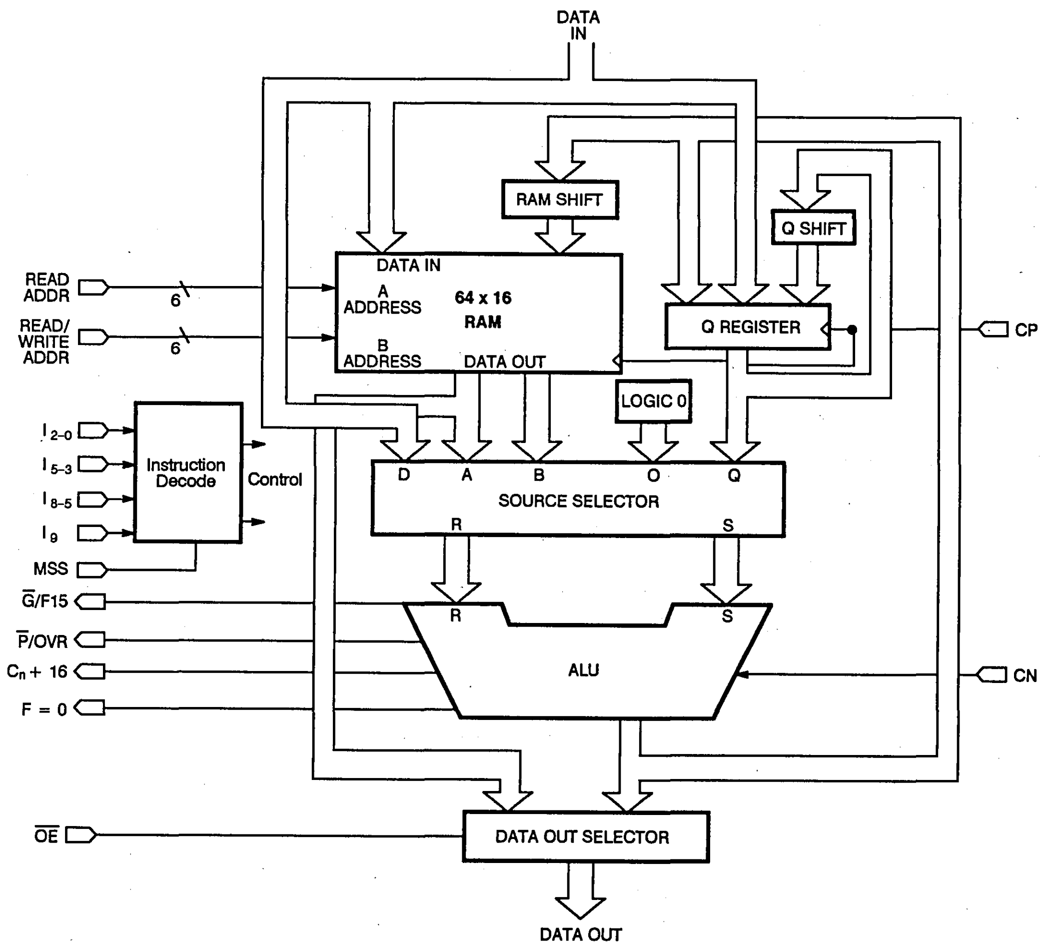


Figure 1. Block Diagram of the IDT49C402A

CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.

Printed in the U.S.A. 9/88

APPLICATIONS

The IDT49C402A can be thought of as a VLSI building block. This building block has a register file, an ALU and an accumulator. Since the IDT49C402A is designed out of static random logic, this device may be used in many different places. It can be used as a data path element in a general purpose computer or as an address generator to generate complex addresses for accessing data structures and linked lists. It might also be used as a complex accumulator with an ALU on its input to achieve sophisticated counter-type operations where constants may be in the register file in order CORDIC-type algorithms. Put simply, the IDT49C402A can be thought of and used as a very high-performance 16-bit version of the widely used 4-bit 7400 family (74181, 251, 381) ALUs.

FUNCTIONAL DESCRIPTION

The IDT49C402A is a high-speed, fully cascadable 16-bit CMOS ALU slice with 64-by-16-bit register file. It combines the standard functions of four 2901s (4-bit ALU) and a 2902 (carry lookahead), with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

Based on the normal control functions associated with a standard 2901 bit-slice operation, the IDT49C402A includes twice the destination codes. Its standard functions (Figures 2 and 3) include a 3-bit instruction field which controls the source operand select of the ALU (I_0, I_1, I_2), a 3-bit instruction field used to control the 8 possible functions of the ALU (I_3, I_4, I_5), and a 3-bit instruction field (I_6, I_7, I_8) for selecting the standard 8 destination control functions supported by the 2901. A 10th micro-instruction input, I_9, offers 8 additional destination control functions. This I_9 input, in conjunction with I_6 through I_8, allows many new functions to take place, like shifting of the Q register up and down independently, as well as loading the RAM or Q registers directly from the D inputs without going through the ALU. By tying the I_9 instruction input high, the I_8 through I_6 instruction lines exhibit the destination codes found in the 2901. With the I_9 line low, the new additional functions of the IDT49C402A can be accessed.

EXTRA DATA PATHS

The IDT49C402A, while using the same basic 2901-type architecture, incorporates a new data path aimed at increasing system parallelism. This data path goes directly from the D inputs into the register file and Q register. Normally, the loading of the register file and the Q register in the 2901 requires that the ALU work as a pass function in order to route the direct data input path through the ALU and then store the results in the register file or Q register. With the new data path, the data can be put directly into the register file in parallel with other ALU operations. For example, in one cycle the DFF destination instruction allows the A output port of the register file and the Q register to be combined together in the ALU with the results being stored into the Q register, while new data is brought into the register file and stored at the address selected by the B address port. One of the more sophisticated destination functions available in the IDT49C402A is DFA. This allows the RAM to be loaded directly from the D inputs, the Q register to receive the results of the ALU and the Y output bus to output data directly from the RAM. This extra data path allows full, complete utilization of all three major buses inside the IDT49C402A.

FUNCTION CONTROL

Mnemonic	Microcode				ALU Function
	I_5	I_4	I_3	Octal Code	
ADD	L	L	L	0	R Plus S
SUBR	L	L	H	1	S Minus R
SUBS	L	H	L	2	R Minus S
OR	L	H	H	3	R or S
AND	H	L	L	4	R and S
NOTRS	H	L	H	5	$\bar{R}$ and S
EXOR	H	H	L	6	R EX-OR S
EXNOR	H	H	H	7	R EX-NOR S

SOURCE CONTROL

Mnemonic	Microcode				ALU Source Operands	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Figure 2. Function and Source Codes

ALU DESTINATION CONTROL

Mnemonic	Microcode					Data to be Stored In RAM at B Address	Data to be Stored In Q Reg	Y Output	
	I_9	I_8	I_7	I_6	Hex Code				
OREG	H	L	L	L	8	–	F	F	
NOP	H	L	L	H	9	–	–	F	
RAMA	H	L	H	L	A	F	–	A	
RAMF	H	L	H	H	B	F	–	F	
RAMQD	H	H	L	L	C	F/2	Q/2	F	Original 2901 Functions
RAMD	H	H	L	H	D	F/2	–	F	
RAMQU	H	H	H	L	E	2F	2Q	F	
RAMU	H	H	H	H	F	2F	–	F	
DFF	L	L	L	L	0	D	F	F	
DFA	L	L	L	H	1	D	F	A	
FDF	L	L	H	L	2	F	D	F	
FDA	L	L	H	H	3	F	D	A	
XQDF	L	H	L	L	4	–	Q/2	F	New Added IDT49C402 Functions
DXF	L	H	L	H	5	D	–	F	
XQUF	L	H	H	L	6	–	2Q	F	
XDF	L	H	H	H	7	–	D	F	

Figure 3. Destination Codes

REGISTER FILE

The register file in the IDT49C402A is 64 addressable locations, each 16 bits wide. Being four times larger than most other 16-bit slices, this increased data space provides a larger cache of data which minimizes the traffic to bring in data from the outside world into the register file. From another perspective, the register file also can be viewed as 4 banks of 16 location register files. By using 2 of the address lines, a register file may be bank-selected, thus allowing the programmer to have 4 virtual 2901s operating inside the IDT49C402A. This enables the user to perform multi-tasking microcode. On each clock cycle a new task may be selected, thus having the minimal overhead for context switches.

INCREASED PERFORMANCE

The critical paths through the IDT49C402A are the address and instruction lines to the Y output and status flags (ABI to Y/Flags). For the A version of the IDT49C402 this is 37ns, the time required for the address input lines to select operands out of the RAM register file and be output as data is 37ns. This allows the user to construct a path well under 50ns. This would include the pipeline register instruction time with a clock-to-Q of 6.5ns (utilizing the IDT74FCT374A) and a set-up time of data and status (37ns) from the IDT49C402A into a status register with a set-up time of 2.5ns.

32-BIT APPLICATIONS

High-speed operation for most 32-bit applications is easily obtainable when using the IDT49C402A. In order to build a 32-bit ALU, two IDT49C402As can be cascaded by connecting the carry-out the ALU of one device into the carry-in of the next device (see Figure 4). In this 32-bit design, the critical path is through the ABI to carry-out ($C_n + 16$), which is 34ns, and then through the carry-in (C_n) of the most significant device as a set-up to the clock, which is 32ns. Using IDT's new FCT/A logic family, a cycle time of 75ns can be constructed.

CONCLUSION

The IDT49C402A can be used in a multitude of applications which previously incorporated discrete 2901s. Upgrading to this high-performance device allows the user to operate at a 20MHz level while reducing board space and overall power. It exemplifies its overall flexibility as a VLSI building block wherever an ALU function with register files is used.

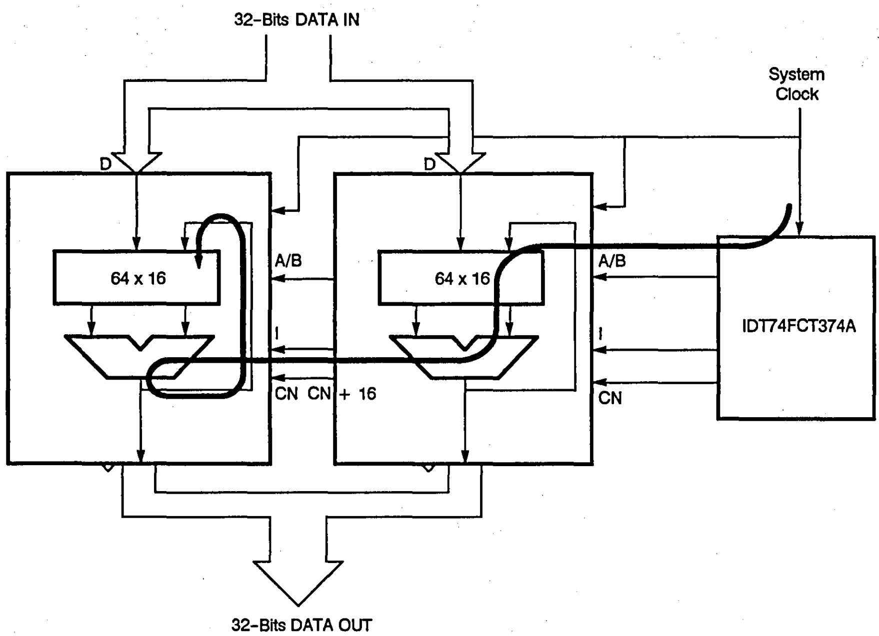


Figure 4. 32-Bit Configuration Showing Critical Delay Path

Integrated Device Technology, Inc.

USING HIGH-SPEED 8K x 8 RAMS

TECHNICAL NOTE TN-04

by Michael J. Miller

INTRODUCTION

Integrated Device Technology provides two high-speed CMOS 8K x 8 static RAMs for use in high-performance memory applications. These sophisticated static RAMs are suitable for incorporation in main memories and caches for the current generation of 25MHz 32-bit microprocessors, such as the Motorola 68020 and the Intel 80386. These two CMOS RAMs have an address-to-data access time of 30ns. Using these static RAMs together with the FCT family, which is a memory interface family provided by IDT, will result in very high-performance memory systems.

USING THE IDT7164

The IDT7164 is a 28-pin industry standard 8K x 8 CMOS static RAM. It has a chip select and address access time of 30ns. The block diagram in Figure 1 shows the IDT7164 in a typical application where the address bus is decoded to generate a chip select and the lower order address lines provide specific location selection inside the 8K x 8. The IDT74FCT521A is an 8-bit address comparator which generates an active low output signal whenever there is a match. The address-to-match output is 7.2ns commercial. The IDT74FCT138A is used as an address decoder. This is a one-of-eight selection device which can be used to take mid-range addresses and select one out of eight possible enables. The enable signals are then connected to eight 8K x 8 static RAMs. The address-to-enable-out time is 5.8ns. The sum total of the memory system shown is 43ns.

USING THE IDT7165

The IDT7165 is a more sophisticated version of the 8K x 8 static RAM. The No Connect pin in the industry standard is used as a bulk clear for this static RAM. By pulsing this control line low for 60ns, the entire contents of the 8K x 8 static RAM is cleared to a value of zero. This is an important function for systems which need to guarantee all locations are zero at power up time. For software, this can be very convenient because when the initial program is loaded in, it is guaranteed that all locations are zero without having to write them all, thus saving a lot of time. Clearing the memory at system reset also removes the nasty bug that some programs may run slightly differently each time the computer is powered on because the program inadvertently reads a location that has not been written to.

As today's static RAMs are utilizing ever decreasing transistor geometries, the probability of data still being intact when power is turned off and then turned back on increases. This effect is contrary to the requirements for data secure systems. Data security is not only important for military applications, but also commercial applications where data encryption or confidential data may be involved.

Incorporated on the IDT7165 8K x 8 static RAM are two chip selects just like the industry standard version. However, these two chip selects have slightly different operation. The active HIGH chip select is a chip select that, when disabled, puts the RAM into a low-power standby mode. This allows gating of the data bus so that, as the data bus floats in tri-state, the input buffers do not consume excessive power. The active LOW chip select, on the other hand, does not gate the data bus, providing a fast access path. This access path is 10ns faster than the active HIGH chip select, yielding a chip-select-bar-to-data-access time of 20ns. The block diagram in Figure 2 shows a configuration very similar to Figure 1. The difference, because of the fast chip select time, is that the delay time of the address comparator and decode selector are in parallel with part of the address access time. Therefore, the sum total access time from the address bus through the comparator decode selector is 33ns.

CONCLUSION

While the IDT7164 is an industry standard 8K x 8 with very high performance, the IDT7165 can provide increased performance with extra features such as bulk clear. Both of these devices are very suitable for inclusion into designs incorporating the current generation of 32-bit microprocessors.

Printed in the U.S.A. 7/86

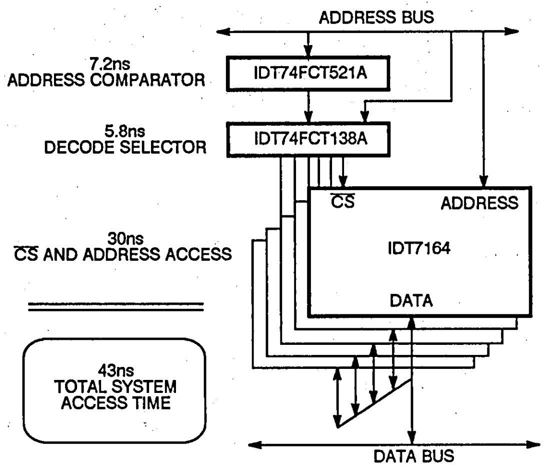


Figure 1. IDT7164 30ns Address and Chip Select Access

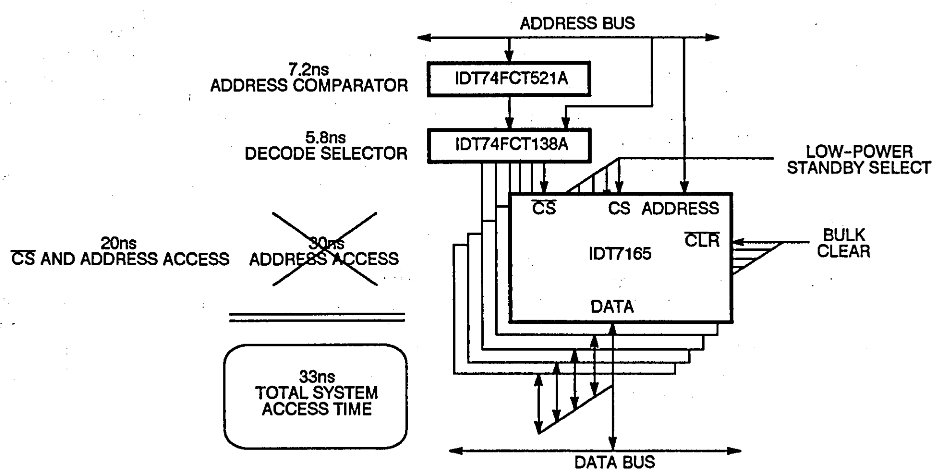


Figure 2. IDT7165 20ns Chip Select Access

Integrated Device Technology, Inc.

FCT—FAST, CMOS, TTL-COMPATIBLE LOGIC

TECHNICAL NOTE TN-05

INTRODUCTION

IDT developed FCT (Fast CMOS TTL-compatible Logic) to allow TTL designers and fast TTL systems to take advantage of CMOS' inherent low power and fast speed. We accomplished this by designing a family fully compatible with TTL levels and drive, with none of the disadvantages of input loading or power supply drain.

This Tech Note has been developed to assist design engineers, as well as component engineers, in more fully understanding and utilizing the performance advantages of IDT's FCT logic family. We have included in this document some of the common electrical characteristics published in the data book, but most of this information provides much more detail than could be adequately covered in a data sheet.

SECTIONS

Section 1
FCT DATA SHEET SPECIFICATIONS

By John R. Mick

INTRODUCTION

The goal of this Tech Note is to provide the design engineer with all of the technical information necessary to understand the advantages of the high-speed CMOS logic known as FCT. FCT stands for Fast CMOS TTL-compatible Logic.

This Tech Note contains the detailed electrical characteristics of the FCT devices. Particular emphasis has been placed on the unique characteristics that are inherent to CMOS, as well as the overall parameters of the family. We have tried to provide inter-family information, as we believe it is quite normal for designers to mix logic families in the same system. This allows the design engineer to use the appropriate elements in each aspect of the design. The most common example is to look at all of the various personal computers currently being manufactured. They typically contain CMOS, N-channel, Bipolar Schottky and EPROM technologies. Occasionally, some of these systems will include linear technology. Another example is that most fixed instruction set microprocessors have either been N-channel or CMOS. Typically, dynamic memories have been N-channel and static memories have either been N-channel or CMOS. Most logic has been Schottky or low-power Schottky-type devices and, more recently, oxide isolated Schottky devices have been used. This has been true of basic logic elements as well as bipolar PROMs and bipolar PALs™. More recently, we see people using CMOS PALs and N-channel or CMOS EPLDs.

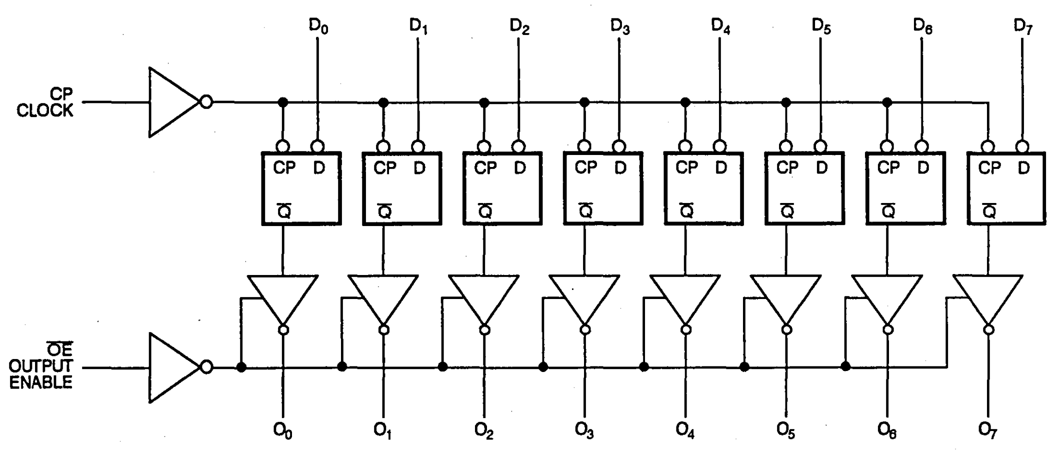
The major topics to be covered in this Tech Note are as follows:

- Input Characteristics
- Output Characteristics
- Transfer Characteristics
- Speed and Power Information
- Noise Margin
- Power Supply Considerations
- Power Calculations
- Interfacing FCT to CMOS Memories
- Good Design Practice
- Typical Examples

DC ELECTRICAL CHARACTERISTICS FOR FCT

Figure 1 shows the DC Electrical Characteristics over the full commercial and military operating range for the IDT54/74FCT374. This device has been chosen as an example for discussing the electrical characteristics because it is typical of all the devices in the FCT family. As shown in the figure, the input high level and input low level are identical to other TTL-compatible devices. The V_{IH} is specified at 2.0 volts and the V_{IL} is specified at 0.8 volts. This means that the input threshold characteristics of FCT are identical to Schottky, low-power Schottky, Fairchild F and other earlier forms of TTL logic. One of the significant differences of FCT is the input current. As seen in Figure 1, I_{IH} and I_{IL} are specified at ±5 microamps and this current may flow into or out of the input depending on whether the input is high or low. This means that I_{IH} (the input high current) is 5 microamps while I_{IL}(the input low current) is -5 microamps maximum.

FUNCTIONAL BLOCK DIAGRAM



Functional Block Diagram of IDT74FCT374

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following conditions apply unless otherwise specified:
T_A = 0°C to +70°C　V_{CC} = 5.0V ± 5%　Min. = 4.75V　Max. = 5.25V (Commercial)　V_{LC} = 0.2V
T_A = -55°C to +125°C　V_{CC} = 5.0V ± 10%　Min. = 4.50V　Max. = 5.50V (Military)　V_{HC} = V -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output Low Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	–	–	-40	µA
			V_O = 2.4V	–	–	40	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

Figure 1. The DC Electrical Characteristics of the IDT74FCT374

The output high voltage has been specified so as to exceed the requirements of Fairchild F. That is, a commercial temperature range device will have an I_{OH} of -15 milliamps at 2.4 volts while a military temperature range device will have an I_{OH} of -12 milliamps at 2.4 volts. Similarly, the output low voltage has been designed to exceed the requirements of the Fairchild F family. The IDT74FCT374 device is guaranteed to have an I_{OL} of 48 milliamps for the commercial temperature range, with V_{OL} equal to 0.5 volts, and I_{OL} is 32 milliamps for the military temperature range while meeting the V_{OL} of 0.5 volts. This is about twice the F374 specification. The short circuit current has been specified as -60 milliamps maximum to be compatible with Fairchild F. This means that the devices have good ability to drive capacitance in the low-to-high direction.

One of the advantages of the FCT logic family is its ability to drive CMOS memories to full CMOS levels. We have defined full CMOS levels to be V_{LC} equals 0.2 volts and V_{HC} equals V_{CC}-0.2 volts. The term V_{LC} stands for Low CMOS Voltage and the term V_{HC} stands for High CMOS Voltage. As can be seen in Figure 1, IDT74FCT374s can have an I_{OH} of -300 microamps while meeting the V_{HC} parameter and, similarly, IDT74FCT374s can have an I_{OL} of 300 microamps while meeting the V_{LC} parameter. These two parameters provide an indication of the drive capability of FCT in driving CMOS memories as well as other FCT devices.

The DC electrical characteristics of a typical CMOS static RAM are shown in Figure 2. The actual data shown in this figure is for the IDT7198 16K x 4 CMOS memory. First, the input current on a CMOS memory is normally specified as an input leakage current. Thus, the I_{IH} and I_{IL} specs of FCT are equivalent to an I_{LI} spec on a CMOS memory. It is also shown as an absolute value for this current. This means that the input current for a CMOS L power memory device is ±5 microamps military and ±2 microamps commercial. Similarly, the input current for the S power device is ±10 microamps military and ±5 microamps commercial. Recognizing that our FCT family of devices has a CMOS level drive of 300 microamps, it can be seen that we can drive anywhere from 60 to 150 RAM chips depending on the temperature range selected. Needless to say, this most likely is more capacitance than most designers would prefer to drive in a system.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7198S MIN.	IDT7198S TYP.[1]	IDT7198S MAX.	IDT7198L TYP.	IDT7198L MIN.[1]	IDT7198L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	
			COM'L.	–	–	5	–	–	2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	
			COM'L.	–	–	5	–	–	2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	7198S25 7198L25 COM'L.	7198S25 7198L25 MIL.	7198S30 7198L30 COM'L.	7198S30 7198L30 MIL.	7198S35 7198L35 COM'L.	7198S35 7198L35 MIL.	7198S45 7198L45 COM'L.	7198S45 7198L45 MIL.	7198S55 7198L55 COM'L.	7198S55 7198L55 MIL.	7198S70 7198L70 COM'L.	7198S70 7198L70 MIL.	7198S85 7198L85 COM'L.	7198S85 7198L85 MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = 0	S	100	–	100	110	100	110	100	110	100	110	100	110	–	110	mA
		L	85	–	85	95	85	95	85	95	85	95	85	95	–	95	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = f_{MAX}	S	135	–	125	140	125	140	125	140	125	140	125	140	–	140	mA
		L	125	–	115	125	105	115	100	110	100	110	95	110	–	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Output Open	S	55	–	50	55	45	50	45	50	45	50	45	50	–	50	mA
		L	45	–	40	45	35	40	30	35	30	35	30	35	–	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}	S	15	–	15	20	15	20	15	20	15	20	15	20	–	20	mA
		L	0.5	–	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	–	1.5	

NOTES:
1. All values are maximum guaranteed values.

FIGURE 2. The DC Electrical Characteristics of the IDT7198 16K x 4 Static RAM

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.[1] V_{CC} @ 2.0V	TYP.[1] V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	10	15	600	900	µA
			COM'L.	–	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\lvert I_{LI} \rvert$ (3)	Input Leakage Current			–	–		2		µA

NOTES:
1. $T_A = +25°C$
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

FIGURE 2. (Continued)

Another important parameter associated with CMOS static RAMs and their relation to FCT can be seen in Figure 2. This is the standby power supply current. There are two specifications for standby power supply current, I_{SB} and I_{SB1}. The I_{SB} standby power supply current is actually specified with the chip select at a TTL high (V_{IH}). The full power supply standby current (I_{SB1}) is a CMOS standby current and is specified with the chip select at V_{HC} and the inputs at V_{HC} or V_{LC}. Notice that on the low-power series device this can be anywhere from a 13-to-1 to almost a 40-to-1 savings in standby current for the deselected devices. This shows that the use of FCT to drive CMOS static RAMs can provide a significant power reduction with the use of no additional parts.

The offstate (high impedance) output current (I_{OZ}) shown in Figure 1 has been specified as ±40 microamps. This number was chosen to be lower than the Fairchild F specification of ±50 microamps for the following reason: both the low-power Schottky devices and the older, gold-doped TTL devices have an offstate high impedance output current of ±40 microamps. We felt that some design engineers may wish to replace those older devices with FCT in upgrading new systems. Since we meet this parameter quite handily, it is not necessary to compute new worst case leakage numbers if a system is being redesigned.Rather, the FCT devices will meet the three-state leakage requirements of all the high-speed bipolar Schottky processed logic elements.

Unfortunately, several of our IDT FCT data sheets went to print in the 1986-87 catalog with both the I_{OZ} and the input clamp diode parameter left off the data sheet. (This has been corrected in the new 1988 data book.) We apologize for this oversight and wish to indicate here in this Tech Note that these devices will meet the ±40 microamps of three-state leakage current, as well as the input clamp diodes specification of -1.2 volts at -18 milliamps. For historical purposes, it should be mentioned that the very first production runs of the FCT were built without input clamp diodes. The mask sets were soon changed and input clamp diodes added to all inputs of the FCT devices. Currently, the devices in production have input clamp diodes on all inputs.

UNDERSTANDING POWER CALCULATIONS

The most recent release of the power supply characteristics for the IDT74FCT374 is shown in Figure 3. It is IDT's goal to attempt to fully specify the power supply characteristics of these logic devices in a fashion most usable by the design engineer. As such, I_{CC} has been specified, as well as the three components which make it up; these are the quiescent power supply current (I_{CCQ}), the power supply current associated with TTL inputs high (I_{CCT}) and the dynamic power supply current (I_{CCD}). Again, it is necessary to look back in history to get a perspective of the reason for these parameters. First, several semiconductor manufacturers have been building devices known as HC and HCT for some years. In addition, the JEDEC JC-40.2 Committee has been very active in creating standards for these HC and HCT devices. The first standard published by the JC-40.2 Committee was known as Standard 7. It was revised in 1986 with a version known as Standard 7A. The purpose is to totally specify the HC and HCT devices so that a number of manufacturers can build them and provide second sources.

In the early days of the manufacture of HC and HCT, it was traditional for the manufacturers to specify I_{CC} with only 1-bit toggling. IDT believes that this is not representative of the total power supply current drawn by these devices and so has chosen to add additional specifications to the I_{CC} parameter. In order to remain comparable with the earlier specifications of 1-bit toggling, we have included these specifications at a 10MHz frequency. The new parameter of all 8 bits toggling is also included with a clock frequency of 10MHz and the data input frequency is chosen as 2.5MHz to provide a more realistic estimation of the power supply current. It is reasonable to ask why 5MHz was not chosen and the answer is that we felt this would not be realistic. If a toggle rate of 10MHz for the clock and 5MHz for the data is chosen, an 8-bit register can assume only two states: all highs on one cycle and all lows on the next cycle followed by all highs on the following cycle, and so forth. Obviously, any other checkerboard pattern is also possible but only two possible states would result. Thus, a 10MHz clock and a 2.5MHz data rate is most realistic.

Also, as can be seen in Figure 3, there are specifications for FCT being driven by other FCT devices as well as a specification for FCT being driven by a bipolar TTL device. The difference here is that an FCT device, when driven by another FCT device, will have its inputs pulled to V_{HC} or V_{LC}. When an FCT device is driven from a bipolar Schottky device, its inputs will be driven from a voltage very near V_{LC} to voltage typically around 3.4 or 3.5 volts. Thus, the high state will not be V_{HC}. This causes an increase in power dissipation that will be discussed later in this Tech Note.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current(4)	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_I = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	5.6	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_I = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	15.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

Figure 3. Power Supply Characteristics of the IDT74FCT374

As discussed earlier, the ICC power supply current consists of three components: the quiescent current, the current associated with inputs being driven from TTL levels and the current associated with the dynamic switching of the device. The equation in Note 4 of Figure 3 fully describes the relationship of this power supply current. For completeness here, let's review the full meaning of this equation. First, the quiescent current is taken directly from the data sheet and represents the maximum current that will flow at +125°C. The next term is that associated with the inputs being driven from TTL levels. If we view the typical CMOS input circuit shown in Figure 4, we see that the input comes in first to the input clamp diode, then goes through the ESD input protection resistor which is typically 120 ohms to 500 ohms. Next, this input connects to the gates of a CMOS inverter made up of a P-channel device and an N-channel device. This inverter operates in the normal fashion—if the input is at ground (or very nearly ground), the P-channel device will be on, the N-channel device will be off and no current will flow between VCC and Ground. Similarly, if the input is at 5 volts (or very nearly 5 volts), the N-channel device will be on, the P-channel device will be off and no current will flow between VCC and Ground. If however, the input is biased and a normal TTL high level (somewhere around 3.5 volts), the devices will be in the linear region and some current will flow between V_{CC} and Ground. This current is shown on the data sheet of Figure 3 as I_{CCT}–the power supply current for a TTL high input at 3.4 volts. The typical current is approximately 0.5 milliamps, but the maximum current per input can be as high as 1.4 milliamps.

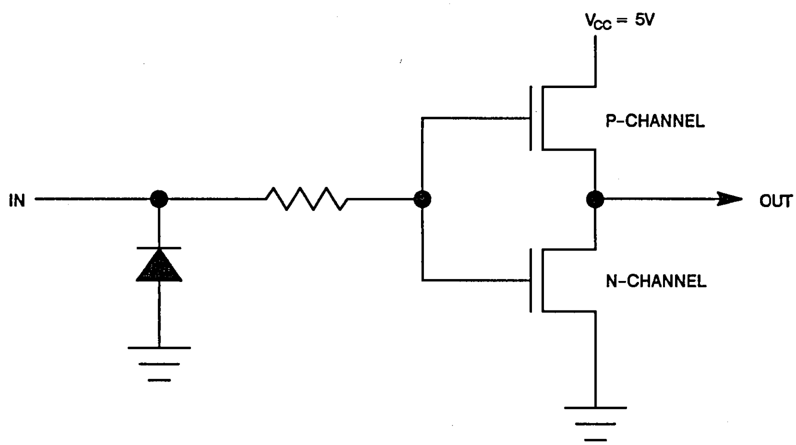


Figure 4. Typical CMOS Input Inverter for a Logic Device

Again, referring to the equation in Note 4 of Figure 3, the current associated with the inputs is calculated by considering each input. We must look at each input and consider its duty cycle high. This has been written in the equation as the I_{CCT} parameter times the duty cycle for the TTL input high (D_H) times the number of TTL inputs (N_T) at the D_H duty cycle. Another way of saying this would be simply to take the summation of the duty cycles times the I_{CCT} parameter. For example, if we had eight inputs at 50% duty cycle the result would be 4 x I_{CCT}. If we had eight inputs at 25% duty cycle the result would be 2 x I_{CCT}. If we had eight inputs at 75% duty cycle the result would be 6 x I_{CCT}. More importantly, if the inputs are swinging between V_{HC} and V_{LC} (or some voltage very near that value), the input current may be assumed to be zero. This parameter only applies when the input is being driven to a TTL high level in the vicinity of 3.4 volts. As the voltage goes higher, the current reduces and eventually becomes zero.

The final parameter in calculating I_{CC} is the dynamic current. We have chosen to describe this current as the current caused by an input transition pair (HLH or LHL). We did it this way because we couldn't think of any other way to describe this phenomena. Basically, we are talking about the power drawn from the V_{CC} input when charging a capacitor. When the transition is from a low to a high level, we draw current from the V_{CC} to charge an internal capacitance inside of the device. When that same capacitance is discharged, that is a transition from high-to-low; no current is drawn from V_{CC}, but rather the capacitance supplies the current which is discharged to Ground. Thus a high-low-high (HLH) or low-high-low (LHL) transition pair draws the same amount of average current from V_{CC}. We call this one cycle of the clock or one cycle of any data input. As the equation shows, for register devices we use a clock frequency divided by 2. For non-register devices, this parameter for f_{CP} should be set to 0. The next thing that is required is to take care of the second half of the equation–to consider the input frequency of each input. If, for example, all eight inputs of the IDT74FCT374 register are at 1MHz, we simply use 1 x 8 to account for this power. In other words, what is actually required is to perform a calculation of F_IN_I where I varies from 1-to-8 for the eight inputs of the IDT74FCT374. It should be repeated here that all currents are in milliamps and all frequencies are in megahertz.

For completeness, Figure 5 shows three example calculations for power supply current. The first example in Figure 5 (labeled Figure 5A) is for an IDT74FCT374 with a clock frequency of 1MHz. We also assume that all of the inputs are driven from other FCT devices, they are at a 50% duty cycle and that all eight inputs are at 250KHz. The second example is similar except the clock frequency has been raised to 10MHz. Again, the inputs are driven from other FCT devices, the inputs are at a 50% duty cycle and all eight inputs are at 2.5MHz. The final example is for a 10MHz clock where the inputs are driven from other TTL inputs such as Fairchild F or low-power Schottky. The inputs are assumed to be a 50% duty cycle and, again, all eight inputs are toggling at 2.5MHz. The reader should notice that the calculations in Figure 5B and 5C match the parameters on the data sheet shown in Figure 3.

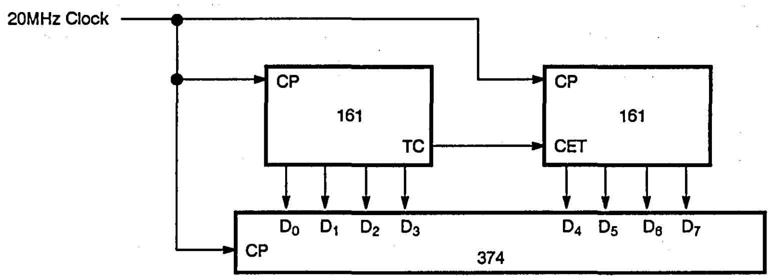
1MHz EXAMPLE	10MHz EXAMPLE	10MHz EXAMPLE
1) CMOS Driving Inputs	1) CMOS Driving Inputs	1) TTL Driving Inputs
2) 50% Duty Cycle	2) 50% Duty Cycle	2) 50% Duty Cycle
3) 8 Inputs at 250KHz	3) 8 Inputs at 2.5MHz	3) 8 Inputs at 2.5MHz
$I_{CC} = I_Q + I_D$ (Note: $I_I = 0$)	$I_{CC} = I_Q + I_D$	$I_{CC} = I_Q + I_I + I_D$
WORST CASE	WORST CASE	WORST CASE
= 1.5 + 0.25 (1/2 + 0.25 * 8)	= 1.5 + 0.25 (10/2 + 2.5 * 8)	= 1.5 + 1.6 * .5 * 9 + 0.25 (10/2 + 2.5 * 8)
= 1.5 + 0.625	= 1.5 + 6.25	= 1.5 + 7.2 + 6.25
= 2.125mA (10.6mW)	= 7.75mA (38.8mW)	= 14.95mA (75mW)
TYPICAL	TYPICAL	TYPICAL
= 0 + .15 (1/2 + 0.25 * 8)	= 0 + .15 (10/2 + 2.5 * 8)	= 0 + .5 * .5 * 9 + 0.15 (10/2 + 2.5 * 8)
= 0.375mA (1.875mW)	= 3.75mA (19mW)	= 2.25 + 3.75
		= 6mA (30mW)

Figure 5A. Example Power Calculations for IDT74FCT374 Driving IDT74FCT374 at 1MHz

Figure 5B. Example Power Calculations for IDT74FCT374 Driving IDT74FCT374 at 10MHz

Figure 5C. Example Power Calculations for Fairchild F374 Driving IDT74FCT374 at 10MHz

Figure 6 shows an example of an IDT74FCT374 being driven from a high-speed counter. The clock frequency to the IDT74FCT374 and the counter is 20MHz. Each of the data inputs is at 1/2 the frequency of the previous input—D_0 is at 10MHz, D_1 is at 5MHz, D_2 is at 2.5MHz and so forth. The table in Figure 6 shows the computation of the power for each input in both a typical and maximum column. From this we can see the total contribution of the current for each input as well as the clock. The total dynamic current, both typical and worst case, is then computed as 4.487 milliamps and 7.479 milliamps, respectively. If we wish to know the total worst case power supply current for the IDT74FCT374 in this configuration, we simply need to add the quiescent current of 1.5 milliamps. This would result in 8.979 milliamps as the worst case current. Since all of the inputs are at a 50% duty cycle, we can compute the worst case TTL input current for all the inputs and add this value to those previously calculated for the quiescent current and the dynamic current. This would result in a total I_{CC} for the IDT74FCT374 being driven in this configuration. The result would be 6.737 milliamps typical and 16.179 milliamps absolute worst case. From this example, it can be seen how to compute the frequency of each input and its contribution to the overall I_{CC}. It is normally good practice for the designer to compute both the typical and worst case currents for the design.



$$I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$$

			TYP.	MAX.
CLOCK	=	20MHz	1.500	2.500
D_0	=	10MHz	1.500	2.500
D_1	=	5MHz	.750	1.250
D_2	=	2.5	.375	.625
D_3	=	1.25	.187	.312
D_4	=	0.625	.093	.156
D_5	=	0.3125	.047	.078
D_6	=	0.15625	.023	.039
D_7	=	0.78125	.012	.019
TOTAL DYNAMIC CURRENT			4.487	7.479
QUIESCENT CURRENT			0	1.500
TTL INPUT CURRENT			2.25	7.2
TOTAL I_{CC} (mA)			6.737	16.179

Figure 6. Power In an IDT74FCT374 When Driven at 20MHz by a TTL Counter

A final example of power supply current contribution is shown in Figure 7. This example is simply a table of the IDT74FCT374 with TTL inputs and different frequencies and duty cycles on each of the inputs. The assumptions of frequency and duty cycle are shown in the last two columns at the left. In order to demonstrate the contribution of the TTL input current and the dynamic current, both a typical and maximum for each of the inputs has been shown. Then the table for total I_{CC} typical and device I_{CC} maximum has been computed for each input. The bottom line is a summation of the total currents for the input, the dynamic and, finally, on the right hand side, the total device. Incidentally, the actual method used to generate the frequencies on the left and the duty cycles associated with each of those frequencies is left as an exercise for the student. They were simply made up and do not represent any known example. The purpose here is to show the technique for computing the total power dissipation and helping the engineer understand the contribution of each input and each term. A fancy equation for the power supply current is:

$$I_{CC} = I_{CCQ} + I_{CCT} \sum_{i=1}^{N} D_i + I_{CCD} \left(f_{CP}/2 + \sum_{j=1}^{N} f_j\right)$$

Where:		
I_{CCQ}	=	Quiescent Current from data sheet
I_{CCT}	=	Current for a TTL input at 3.4V from data sheet
D_i	=	Duty Cycle for each input
i	=	The i-th input
N	=	Total number of inputs
I_{CCD}	=	Dynamic Current from data sheet
f_{CP}	=	Clock Frequency (0 if no clock)
fi	=	Frequency of input in MHz
j	=	The j-th input

14

Input Characteristics			Calculation Per Inch				Total Device	
Input	Frequency (MHz)	Duty Cycle	I_{INPUT}		$I_{DYNAMIC}$		I_{CC}	I_{CC}
			TYP.	MAX.	TYP.	MAX.	TYP.	MAX.
Quiescent	–	–	–	–	–	–	0.000	1.500
Clock	5.00	0.50	0.25	0.80	0.375	0.625	0.625	1.425
D_0	2.50	0.90	0.45	1.44	0.375	0.625	0.825	2.065
D_1	2.50	0.70	0.35	1.12	0.375	0.625	0.725	1.745
D_2	1.00	0.50	0.25	0.80	0.150	0.250	0.400	1.050
D_3	1.00	0.30	0.15	0.48	0.150	0.250	0.300	0.730
D_4	0.50	0.10	0.05	0.16	0.075	0.125	0.123	0.285
D_5	0.10	0.20	0.10	0.32	0.015	0.025	0.115	0.345
D_6	1.50	0.40	0.20	0.64	0.225	0.375	0.425	1.015
D_7	0.75	0.80	0.40	1.28	0.113	0.188	0.513	1.468
TOTALS			2.40	7.04	1.853	3.088	4.053	11.628

Figure 7. Inputs at Different Frequencies and Duty Cycles on Each Input

Section 2
ELECTRICAL CHARACTERISTICS OF FCT

By John R. Mick & Marcelo Martinez

This section details the electrical characteristics of FCT. It shows the typical characteristics as measured on the bench, on the automatic testers or both.

I_{IN} VERSUS V_{IN}

The typical characteristic of I_{IN} versus V_{IN} is shown in Figure 1. Basically, what we see here is that the input current is ±5 microamps from the range of 0 to about 14 volts; below 0 volts we see the effect of the input clamp diode. At about 0.7 volts, current begins to flow and we have a diode clamping effect where the voltage is held at the forward biased voltage of a clamp diode and the current increases. Similarly, we see the same type of effect at about 15 volts. That is an input breakdown effect where we get a clamping effect and the current increases in a current source mode with the voltage at 15 volts. The true effect at both 15 volts and about -0.7 volts is that of a diode. Because of the resolution of the scales, the curves do not look quite like a forward bias diode, but in actuality they are.

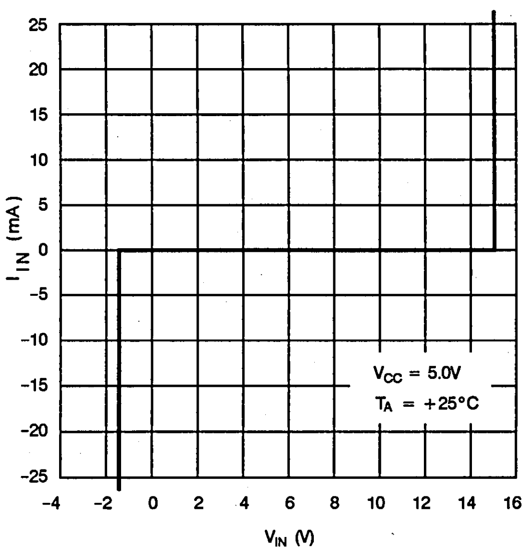


Figure 1. Input Characteristic for Input Voltage Versus Input Current

I_{CCT} VERSUS V_{IN}

The TTL input current in Figure 2 shows that I_{CCT} (the current between V_{CC} and Ground) for an input buffer begins to flow at about 1.1 volts. The current peaks at the actual switching threshold which is designated to be 1.5 volts. As the input is raised towards V_{CC}, the current reduces until, at about 4 volts, it is essentially in the nano-ampere range. Normally, a TTL output is about 3.4 to 3.5 volts. The typical current between V_{CC} and Ground at this voltage level is less than 0.5 milliamps.

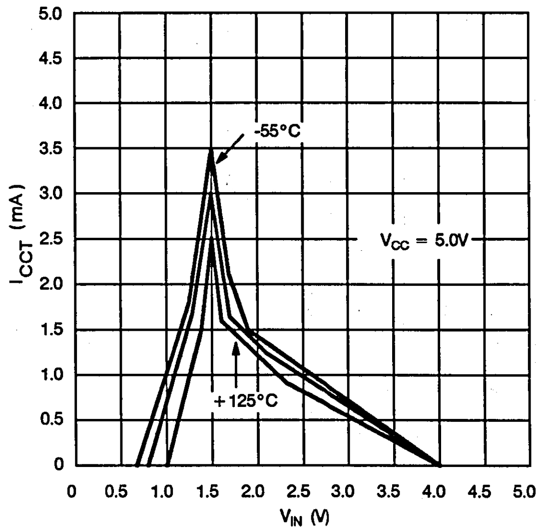
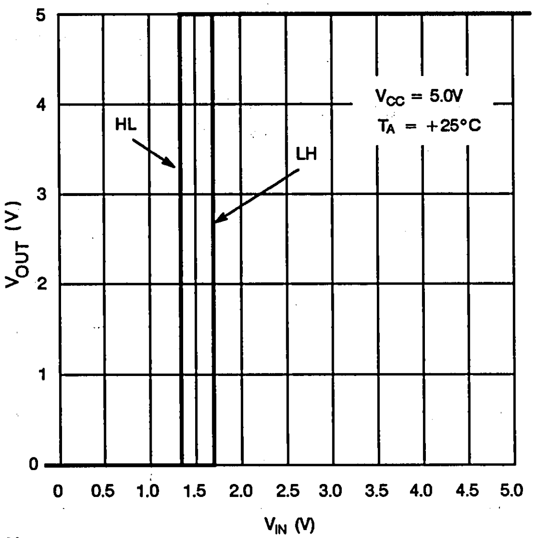


Figure 2. Input Current for a Typical FCT Input

The three lines in the curve shown in Figure 2 represent the currents for the temperatures of -55°C, +25°C and +125°C. The largest value of the current is at -55°C and the smallest value of the current is at +125°C. When we have FCT driving FCT, the DC power is zero and is accounted for in the dynamic power.

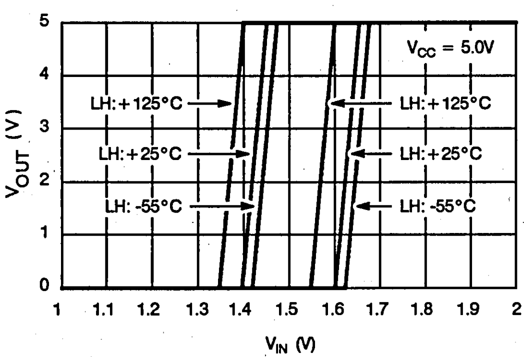
TRANSFER FUNCTION

Figure 3 shows the typical transfer function for an FCT input. This transfer characteristic assumes inputs with hysteresis. There are some FCT inputs that do not have hysteresis and these follow the curve labeled HL. What is depicted here is that the typical input characteristic has a switching point at 1.5 volts. There are about 200 millivolts of hysteresis on many of the FCT inputs. The curve in Figure 4 shows an expanded scale view around 1.5 volts. Here we see the effect of temperature on the actual threshold. What should be noted here is that the hysteresis remains at about 200 millivolts and the input threshold (or actual switching point) shifts about 80 millivolts over the full military temperature range, from -55°C to +125°C. Over the commercial temperature range, from 0°C to +70°C, the temperature input threshold shifts about 40 millivolts. This represents an extremely good temperature characteristic and demonstrates the stability of our FCT logic product.



Note:
1. Inputs without hysteresis follow HL curve.

Figure 3. The FCT Transfer Function Showing Hysteresis[1]



Note:
1. Inputs without hysteresis follow HL curves.

Figure 4. Detailed View of the FCT Transfer Function

IOLVERSUS VOL

Figure 5 shows the output load drive capabilities of a typical 32mA output buffer on a device such as the IDT74FCT374. At the full +125°C temperature we have over 40 milliamps of output drive. As the temperature gets colder, the output drive capability of FCT increases and comes very near doubling at the -55°C point. Notice also that the current sinking capability of FCT is relatively linear all the way up to about 0.8 volts. This means that, should a device be over loaded, the FCT output will sink the additional current without a significant increase in output voltage. This provides greater system reliability.

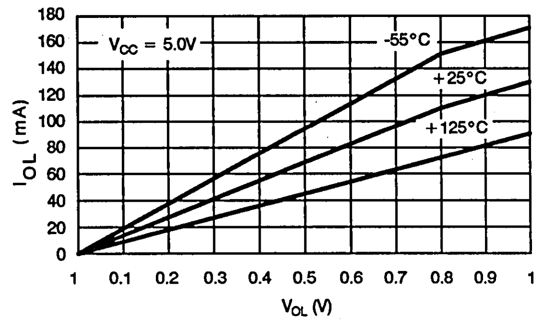


Figure 5. Plot of Output Low Voltage Versus Output Sink Current

I_{OH} VERSUS V_{OH}

The source current capability for the output in the high state is shown in Figure 6. At 2.4 volts we typically have in excess of 24 milliamps of output drive source current capability at +125°C. As the temperature gets colder, the output source current capability increases such that at -55°C we have over 40 milliamps of source current capability. Again, our FCT output structure provides TTL-like compatibility for maximum system reliability.

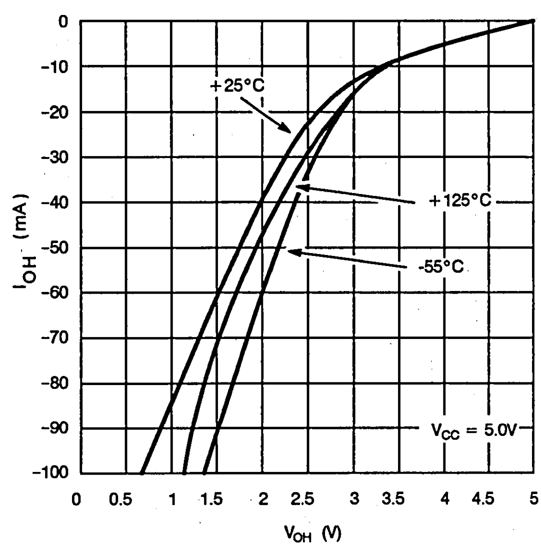


Figure 6. Plot of Output Source Current Versus High Voltage

T_F

Figure 7 shows the output rise output time versus capacitance for a typical high-to-low transition. The output fall time (T_F) is about 2.5 to 3ns into 50pF and 500 ohms as measured for the 10% to 90% points. If we measure the fall time from 4.5 to 0.5 volts, we find that the T_F is about 2.5ns.

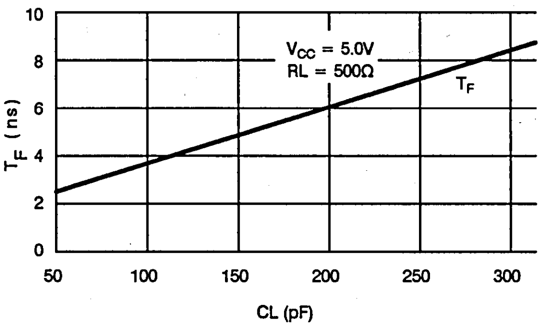


Figure 7. Output Fall Time Versus Capacitance (10% - 90%)

T_R

Due to the design of the output buffer, the output has one rise time from about 0.5 volts to 3.0 volts and a second rise time from about 3.0 volts to 4.5 volts (see Figure 8). The reason for this can be understood by studying the output buffer structure shown in Figure 8. Here we see that the fall time is controlled by an N-channel device between the output and Ground. When the output turns on (goes low), the N-channel device will sink the current and provide a single T_F time. Notice, however, the pull-up structure consists of an N-channel device, a P-channel device and a lateral NPN transistor with a resistor in series. As the device turns on, the lateral NPN transistor and the N-channel transistor cause an initial high-speed low-to-high transition until approximately the three to four volt level. At this point, the P-channel transistor takes over and pulls the output all the way to the rail. This device is slightly slower and this has a slightly different rise time (T_R) as the output pulls to the V_{CC} rail. Thus the rise time through the normal transition region from 0.8 volts to 2.0 volts is in the vicinity of 3ns.

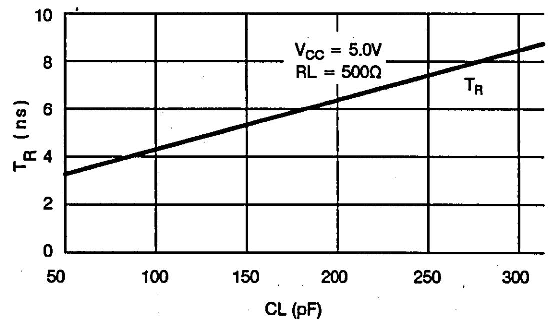


Figure 8. Output Rise Time Versus Capacitance for Voltage of Interest

A point to be noted while viewing Figure 9 is that, because of the N-channel device and P-channel device on the output structure, we have the equivalent of a clamp diode from Ground to the output and a clamp diode from the output to V_{CC}. The benefit of these two diodes is that both overshoot and undershoot at the output pin are minimized. This can provide significant system benefits in terms of noise reduction. The disadvantage of the clamp diode from the output to V_{CC} is that, if the V_{CC} voltage is reduced to 0 (the power is off), there is a clamp path between the output and the V_{CC} pin which will be at Ground. Thus, if the power is off and we have this output pin connected to a bus, the bus will not operate.

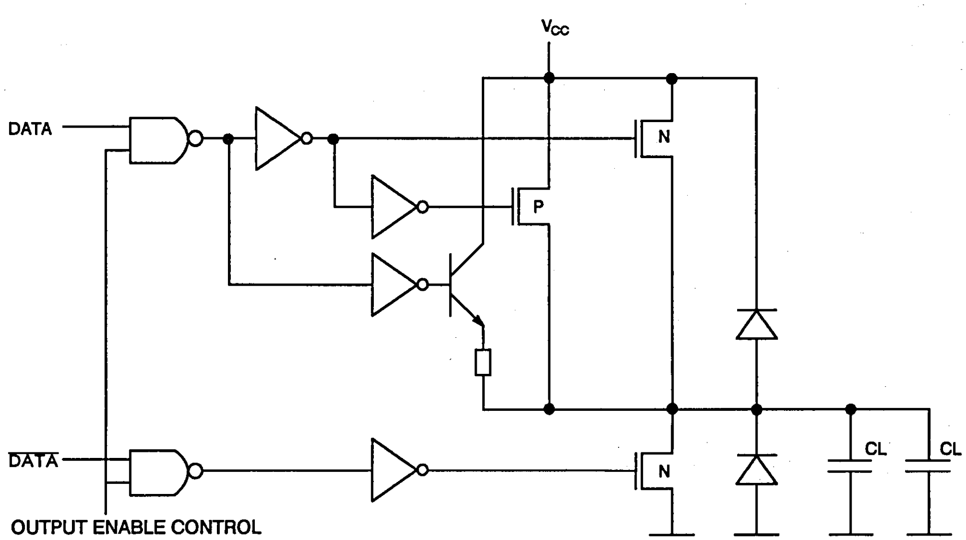


Figure 9. FCT Output Structure

14

ICCD VERSUS TA

The dynamic power dissipation for the IDT74FCT374 is shown in Figure 10. The purpose of this figure is to show that the dynamic power is flat with regard to temperature; the dynamic power is not a function of the ambient temperature. This is true whether the output enable is high or low.

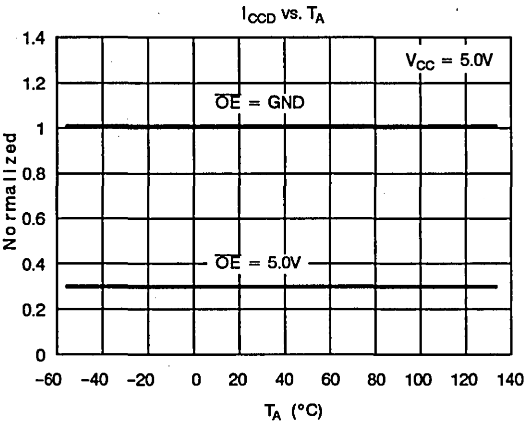


Figure 10. Relation for Dynamic Power Versus Temperature is Flat[1]

Note:
1. $\overline{OE}$ state corresponds to parts with output enable.

PROPAGATION DELAY VERSUS TEMPERATURE AND VCC

Figure 11 shows the typical propagation delay versus temperature characteristics of FCT devices. These measurements are made with an output load of 50pF and 500 ohms. If we normalize the propagation delay at +25°C, we see an increase in speed as the temperature gets colder. Similarly, as the device heats up, the propagation delay increases.

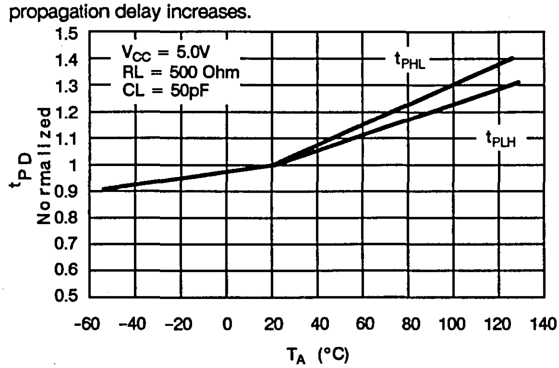


Figure 11. Plot of Normalized Propagation Delay Versus Temperature

Figure 12 shows the propagation delay versus VCC. Again, the measurements are made at 50pF and 500 ohms and the propagation delay has been normalized at 5 volts. What we see is that, as the voltage increases, the device gets faster and as the voltage decreases, the device gets slower. This is exactly as one would expect. Also shown in the curve of Figure 12 is that the device functions all the way down to a VCC of at least 2 volts. Although the propagation delay is considerably slower, the flip-flops will retain data and the outputs will remain in the proper state at VCCs of 2 volts and 3 volts. This is useful for memory systems with battery backup and so forth. One should not interpret from this that FCT devices will be specified at 2 volts or 3 volts, but rather that they will indeed function at these voltages.

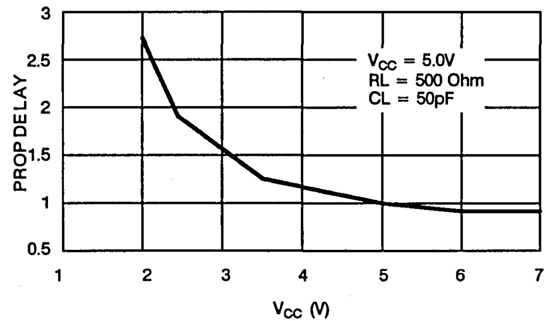


Figure 12. Plot of Normalized Propagation Delay Versus Supply Voltage

PROPAGATION DELAY VERSUS LOAD CAPACITANCE

The FCT devices have all AC parameters specified at 50pF load capacitance. As the load capacitance is increased, the propagation delay increases (see Figure 13). What this figure shows is the "delta" propagation delay that should be added to the data sheet specified propagation delay for these devices. The delta propagation delay at 50 picofarads is 0. If the load capacitance is increased to 150 picofarads, the delay that should be added to the data sheet specified delay is about 2ns, typical. If the capacitance is increased to 250 picofarads, about 4ns should be added to the output propagation delay. The data shown in this table is typical of FCT outputs. We recommend a worst case number of 3ns per 100 picofarads be used for worst case design. Another way to view this same parameter is to use 0.03ns per picofarad above 50pF. There are a number of FCT devices such as the IDT39CXX and the IDT54/74FCT8XX devices that are actually specified at 50 picofarads and 300 picofarads. Since the output structures in all FCT devices are similar or identical, it should be understood that FCT devices can be used to drive 300 picofarad loads with no degradation to the device. The only requirement is to add the appropriate propagation delay delta to the specification in the data sheet for worst case numbers.

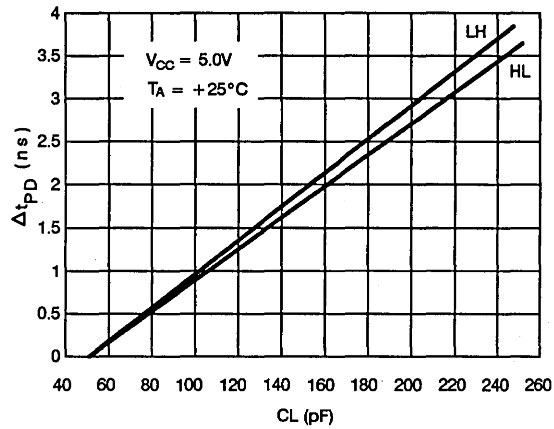


Figure 13. Plot Showing "Delta" Propagation Delay for Load Capacitance Over 50pF

FCT INPUT STRUCTURE

For completeness, a more detailed diagram of the FCT input structure is shown in Figure 14. Here we see the input ESD protection followed by two inverters. The second inverter contains a feedback circuit to provide the regeneration to give the hysteresis on inputs where it is provided.

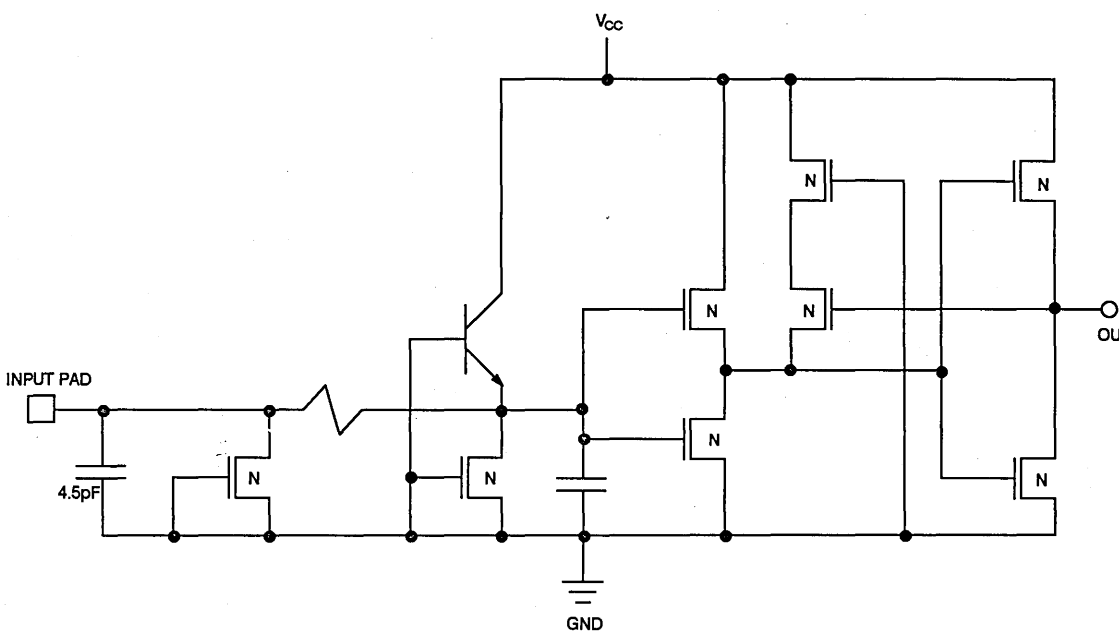


Figure 14. FCT Input Structure

14

Section 3
INTERFACING FCT

By Danh LeNgoc and Suneel Rajpal

Interface is the indispensable glue in digital systems. The popular low-power Schottky and Schottky families of interface logic dominated in the 70s. However, with the advent of advanced CMOS technologies and more sophisticated bipolar technologies, there is a definite shift to designing with other families such as FCT, ALS, 74F and AS in the '80s. FCT is the acronym for Fast CMOS TTL-compatible on the inputs and outputs and has the best ingredients—high speed, high drive and low power.

This section deals with interfacing FCT to other families and good board design techniques.

FCT—THE NEW LOGIC FAMILY

One of the most important graphs that summarizes performance characteristics is the speed/power curve. Figure 1 shows a comparison between the LS, S, HCT, AS, F and FCT families.

Figure 1 shows that FCT provides 74F-equivalent speeds at a fraction of the power. In addition, the FCT A family provides a 50% speed enhancement over the existing FCT speeds. This performance improvement can ensure reliable design where the margins were too tight and also provide better throughputs for new designs. The maximum clocked speeds shown in Figure 2 are also an important consideration.

SPEED/POWER PERFORMANCE CURVE

Speed/Power = Performance - Worst Case
(TTL inputs, frequency = 10MHz, 8 bits toggling)

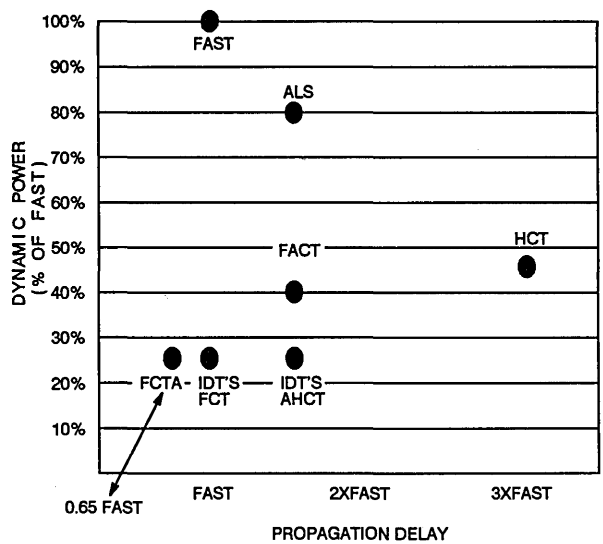
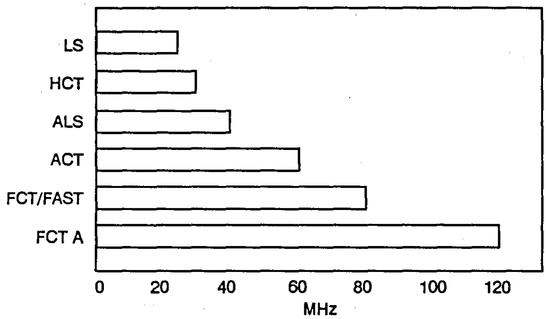


Figure 1. Logic Family Comparison



Maximum clock speeds for a 374 device
(Based on set-up time plus clock to output)

Figure 2. Maximum Clock Speeds

Yet, another important consideration is output drive. The output drive of the FCT family matches those provided by the 74F family. Currently, there is also an ACT family being discussed by semiconductor manufacturers. The drive of the ACT family is targeted to be 24mA, as opposed to 48mA/64mA provided by the FCT products. Figure 3 shows the output drive for different families. The high drive of the FCT parts makes them very useful as bus drivers as described in the applications section.

Family	I_{OL}/I_{OH}
FCT A/FCT	64/ -15mA
FAST	64/ -15mA
ACT	24/ -24mA
ALS	24/ -15mA
HCT	6/ -6mA
LS	24/ -15mA

Figure 3. Output Drive for Different Families

FCT INTERFACE TO OTHER FAMILIES

In deciding the interface capability to other logic families, there are two important factors. The first is the current and voltage compatibility and the second is the noise margin consideration. Voltage and Current parameters are listed in Table A for the FCT driving TTL only, FCT driving CMOS only, 74F and AS families. Note that the parameters for the FCT parts, such as low input current requirements, make for easier design. Also, the outputs of FCT parts can go to V_{CC}-0.2 volts for output currents of 300μA, enabling FCT to drive CMOS only circuits, a feature lacking in 74F and AS.

Parameter	FCT (Driving TTL)	FCT (Driving CMOS)	FAST (Driving TTL)	74HCMOS (Driving CMOS)
V_{IH} Min.	2V	2V	2V	3.15V
V_{IL} Max.	0.8V	0.8V	0.8V	0.9V
V_{OH} Min.	2.4V	4.8V	2.4V	3.7V
V_{OL} Max.	0.5V	0.2V	0.50V	0.4V
I_{IH} Max.	5μA	5μA	20μA	1μA
I_{IL} Max.	-5μA	-5μA	-0.6μA	-1μA
I_{OH} Max.	-15mA	-300μA	-1mA	-6.0mA
I_{OL} Max.	48mA	300μA	20mA	6mA

Table A. DC Parameters for FCT, Fairchild F, FACT and HC374 Devices

Note:

1. There are two noise margins. One is the low voltage noise margin, defined as V_{IL} max. (driven device) - V_{OL} max. (driver). The other is the high voltage noise margin, defined as V_{OH} min. (driver) - V_{IH} min. (driven device).

In driving FCT using 74F devices, a fairly good noise margin is achieved. The FCT input stage exhibits worst case V_{IL} of 0.8V and V_{IH} of 2.0V, the same as F4F TTL. Since the FCT devices are voltage-level sensitive, they draw a maximum input current of ±5μA. When the 74F TTL devices drive the FCT inputs, the 74F TTL output voltage will be close to their unloaded DC values: V_{OH} = 3.4V, V_{OL} = 0.2V. This gives a low noise margin = 0.6V and high noise margin = 1.4V. These noise margins are higher than the noise margins for 74F to 74F (about 0.3V and 0.4V respectively).

In driving FCT with CMOS, the output voltage of CMOS (V_{OL} = 0.2V, V_{OH} = V_{CC}-0.2V) are compatible with the input voltage requirement of FCT input stage. Therefore, CMOS devices can drive FCT inputs without additional external circuitry. This gives a low noise margin of 0.6V and a high noise margin of 1.65V. The best noise immunity is achieved when FCT devices are interfaced directly with FCT devices. Due to input/output compatibility, lower input leakage current and high drive of output stage, FCT outputs can drive FCT input up to the CMOS level (V_{CC}-0.2V, 0.2V). This provides a low noise margin of 0.6V and high noise margin of 2.8V.

FCT DRIVE 74F

The FCT output stage is designed to drive 74F inputs directly. The output stage of FCT devices is shown in Figure 9 of Section 2.

On the output high, the combination of NPN transistor (TTL drive) and N-channel devices of FCT output stage can source an output current I_{OH} = -15mA at V_{OH} = 2.4V. The high noise margin is 0.4V. On the output low, the FCT output stage can sink a current I_{OL} of 48mA at 0.5V (buffer devices can drive an I_{OL} of 64mA). The low noise margin is 0.3V, the same as 74F devices. The FCT output stage can be interfaced directly to CMOS inputs without any pull-up resistors or shift-level circuitries. In the output stage illustrated, the P-channel device at the output stage provides a CMOS-HIGH level of V_{CC} -0.2V and still sources a current I_{OH} of -300µA. This provides a high CMOS fanout, about 300 (CMOS leakage current = 1µA), which is then limited only to the capacitive loading. The low noise margin is 0.7V and the high noise margin is 1.65V. A noise immunity comparison of different 74F and FCT interfaces is shown in Figure 4.

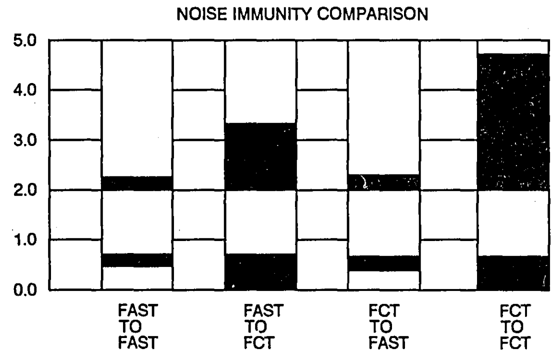


Figure 4. Noise Immunity Comparison

GOOD SYSTEM DESIGN PRACTICE

As digital systems become faster, so do clock and edge rates and this implies more consideration in the power distribution and the interconnect network. A power distribution element (PDE) or a ground plane should be used whenever possible. A ground plane maintains constant characteristic impedance for signal interconnections and maintains a low noise voltage plane for the V_{CC} supply. A ground plane can exist in single-sided boards, 2-sided boards or multi-layer boards.

A typical layout of ICs on a PC board is shown in Figure 5.

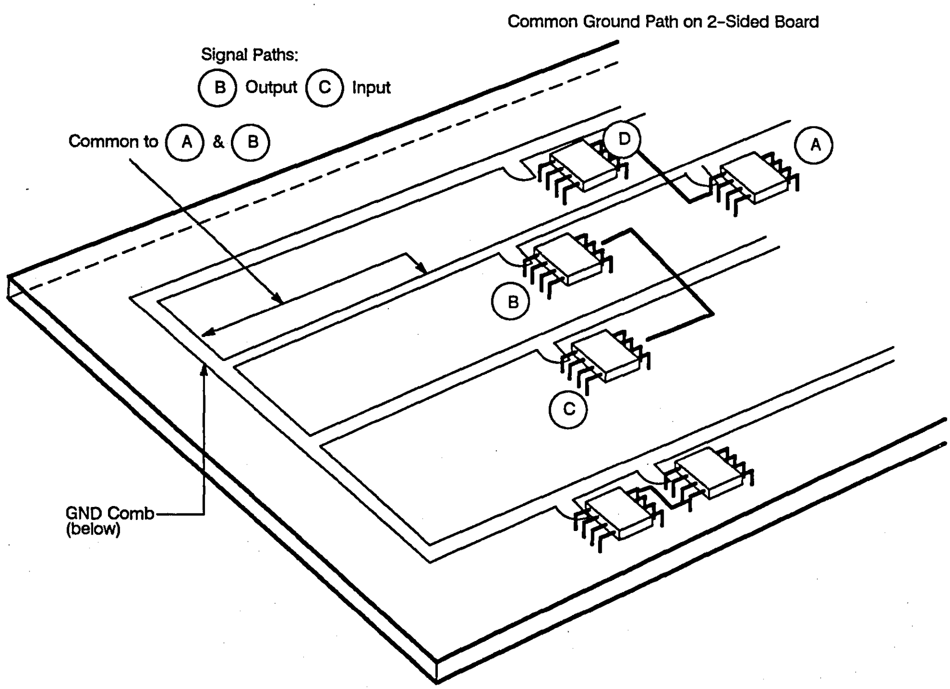


Figure 5. PC Board with ICs

Output Switching from high-to-low on device A can cause a voltage differential on the ground strip common to devices A and B. The transient ground current from device A can flow into device B. The transient ground passing through the inductive element between the two devices can cause the ground voltage on device B to spike. Since the output voltages of device B are referenced to the ground pin, the V_{OL} levels corresponding have a spike. If the output on a gate of device B was in a low state, the ground bounce would cause a spike (shown in Figure 6).

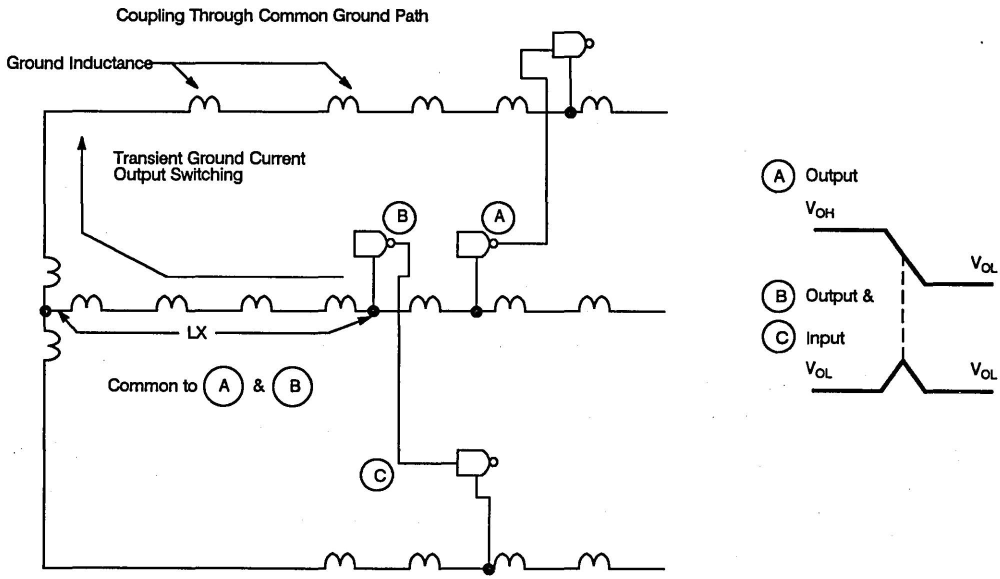


Figure 6. Ground Bounce Effect

This can cause false switching in the gate of device C if the spike were severe enough to drive it over its input threshold. One method of minimizing the ground spikes for two-sided boards is to periodically connect the ground distribution strips by narrow traces on top of the board (shown in Figure 7).

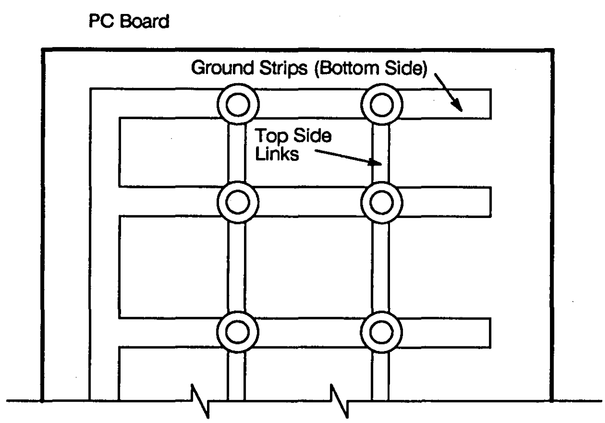


Figure 7. Ground Strips to Minimize Ground Spikes

Bus drivers, grouped on a common ground strip, can cause large spikes. Therefore, buffers that are driving backplanes should be grouped at the edge of the board and have their ground isolated and brought in from the backplane through a separate pin. Also,

14

jumper wires must not be used for ground connections. The preferred approach is to solder ground and supply pins.

Power Distribution Elements (PDE) are recommended for power distribution. A PDE, shown in Figure 8, consists of two flat conductors separated by dielectric.

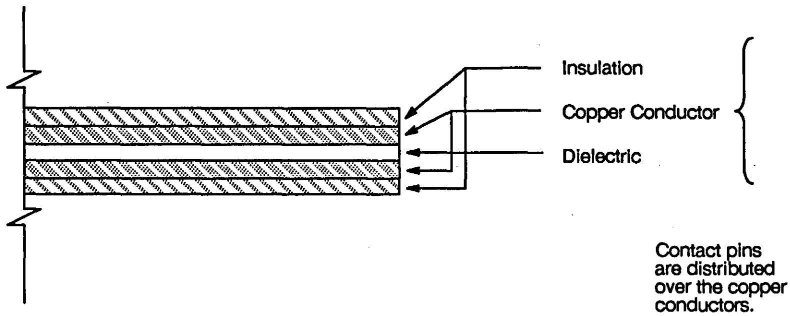


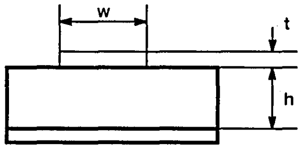
Figure 8. A Power Distribution Element (PDE)

This arrangement has a layer of insulation on the top and bottom. Contact pins are distributed over the conductors for easy access. The characteristic impedance of the PDE is about one-tenth the characteristic impedance of a two-sided printed board distribution (shown in Figure 5).

When using PDEs, it is best to arrange them so that each handles only one type of circuit function. Interface components that sink or source high currents should have a separate PDE. Also, by keeping the interface components at the edge of the board, noise due to high-current switching is isolated from other sections of the logic.

Buffers and logic gates need extra current when they switch. For example, if 8 outputs of a driver raise the voltage of the driven lines from 0.1 volts to 3.1 volts, then the current requirement can be computed. If the impedance of the driven line is 60 ohms, there is a sudden demand for 0.4A. A bypass capacitor can provide this current demand. The capacitor is computed by using the equation C dv/ct = I, where dv is the tolerable voltage drop, dt is the transition time (3ns in above example) and I is the current demand (0.4A in the above example).

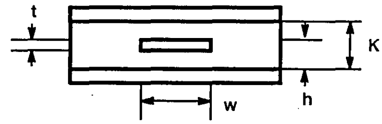
It is recommended that bypass capacitors be used for buffers and transceiver ICs. If PDEs are used, the bypass capacitors should be placed at the end of each PDE instead of each buffer and transceiver. The capacitors should be of low inductance and high-frequency quality. Where V_{CC} comes on the board decoupling capacitors of 0.1µf, a ceramic disk capacitor can be used in parallel with a 20 to 30µf tantalum capacitor.



$$Z_0 = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8w+t}\right)\Omega$$

$$t_{PD} = 1.017\sqrt{475e_r + .67}\ \text{ns/ft.}$$

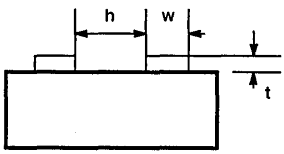
MICROSTRIP LINES



$$Z_0 = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4K}{0.67\pi\, w(0.8+\frac{t}{w})}\right)\Omega$$

$$t_{PD} = 1.017\sqrt{e_r}\ \text{ns/ft.}$$

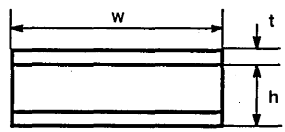
STRIP LINES



$$Z_0 = \frac{120}{\sqrt{e_r}} \ln\left(\frac{\pi h}{w+t}\right)\Omega$$

$$t_{PD} = 1.017\sqrt{475e_r + .67}\ \text{ns/ft.}$$

SIDE-BY-SIDE PL TRACES



$$Z_0 = \frac{377}{\sqrt{e_r}} \ln\left(\frac{h}{w}\right)\Omega$$

$$t_{PD} = 1.017\sqrt{475e_r + .67}\ \text{ns/ft.}$$

FLAT PARALLEL CONDUCTORS

e_r = The relative dieletric constant of one PC board's glass epoxy layer.

Figure 9. PCB Interconnects

CHARACTERISTIC IMPEDANCE SECTION

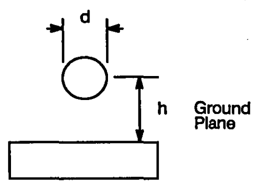
All forms of PCB interconnects are transmission lines. The point at which reflections need to be taken into account is when the transmission delay time is "long" with respect to the pulse rise time; the FCT family rise and fall times are 2-3ns. A "long" line is one whose round trip propagation delay is equal to or greater than the signal rise time. The line impedance Z_0 determines how much current must flow into the device output stage. Popular PCB interconnects are shown in Figure 9.

A microstripline is a signal trace over a ground plane; Z_0 and t_{PD} can be computed based on the geometry. For example, if $e_r = 5$ (for 910 glass epoxy) h = 30 mils, w = 15 mils, t = 3 mils, then $Z_0 = 85\Omega$ and $t_{PD} = 0.15$ns per inch.

A stripline is a microstripline encased between ground planes and has the lowest susceptibility to crosstalk. PC traces that are side by side also have impedance. The provided formula can be used in calculating power rail impedances or crosstalk.

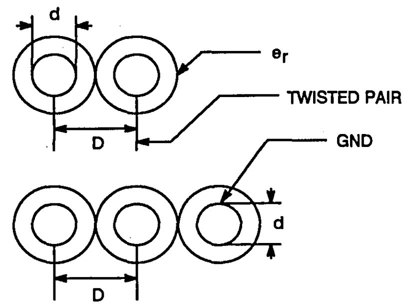
Flat parallel conductors, whose area is much greater than their thickness, tend to have very low impedances and thus make very good power distribution planes.

Wire interconnects are shown in Figure 10.



$$Z_0 = \sqrt{\frac{60}{e_r}}\ \ln\left(\frac{4h}{d}\right)\Omega$$

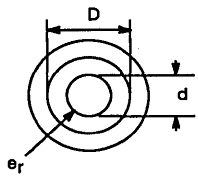
WIRE OVER GROUND PLANE



RIBBON

$$Z_0 = \sqrt{\frac{120}{e_r}}\ \ln\left(\frac{2D}{d}\right)\Omega$$

TWISTED PAIR OR RIBBON CABLE



e_r = The relative dielectric constant

$$Z_0 = \sqrt{\frac{60}{e_r}}\ \ln\left(\frac{D}{d}\right)$$

CO-AXIAL CABLE

Figure 10. Wired Interconnects

A wire over ground plane has the least stable of all impedances due to difficulties in keeping h constant. Propagation delay will vary with h and the insulation and is usually determined by measurement.

In a twisted pair of ribbon cables, impedance is stable and usually in the order of 70 to 100Ω. Coaxial cables have a very stable impedance, but this can be upset and reflections can be caused by sharp bends or crunching of the cable. Propagation delay and capacitance for twisted pair and coaxial cables is normally specified by the cable manufacturer.

The intrinsic impedance and propagation delay of the interconnect is only part of the impedance. The effective impedance has to be known as well. Adding gate inputs, outputs, connectors, etc. to a signal line reduces its impedance and increases its propagation delay. In the equations, C_L is the total of all additional loading and C_O is the intrinsic capacitance of the line. Figure 11 shows the effect of the impedance and propagation delays.

$$Z_0' = \frac{Z_0}{\sqrt{1+\left(\frac{C_L}{C_O}\right)}}\ \Omega$$

$$t_{PD} = \sqrt{L_O C_O}$$

$$t_{PD}' = t_{PD} = \sqrt{1+\left(\frac{C_L}{C_O}\right)}$$

Z_0' = New (lower) Impedance

t_{PD}' = Propagation delay with C_L

Where C_L is the Total of all Additional Loading

Figure 11. Effect of Impedance and Propagation Delays

When a source encounters an unmatched load on the line, that line will have reflections. Also, if the source has a fast rise and fall time and the propagation delay to the receiver is large then the reflections can occur. If propagation delay for the driver to the receiver is t_{PD}, and if t_{RISE} or $t_{FALL} < t_{PD}$, reflections will occur. Figure 12 shows the reflections on the low-to-high transition and Figure 13 shows the reflection on a high-to-low transition.

Gate Driving 100Ω Line Reflection Diagram
Low-to-High Transition

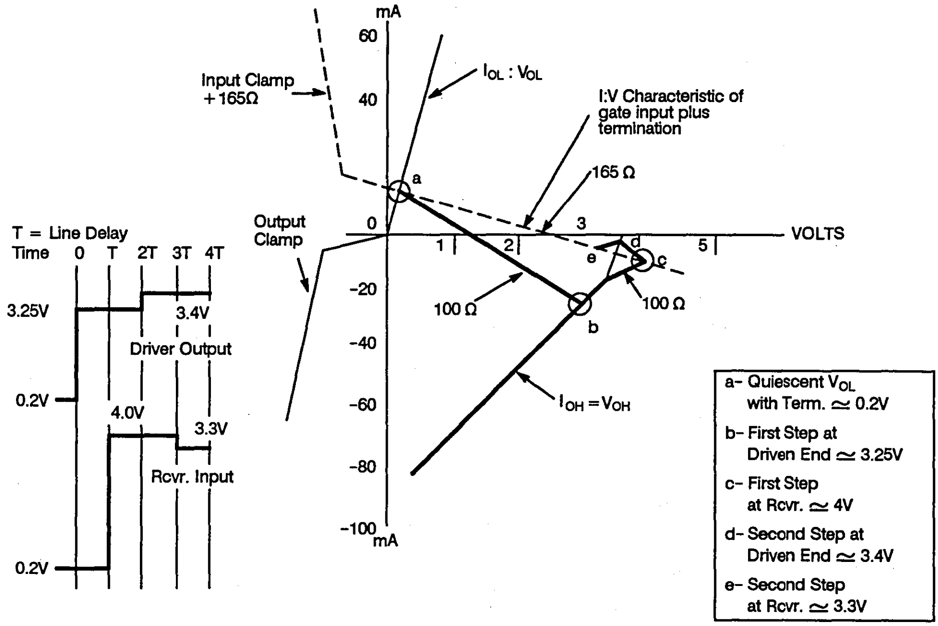


Figure 12. Reflections on a Low-to High Transition

14

Figure 13 shows the reflection on a high-to-low transition.

Gate Driving 100Ω Line Reflection Diagram
High-to-Low Transition

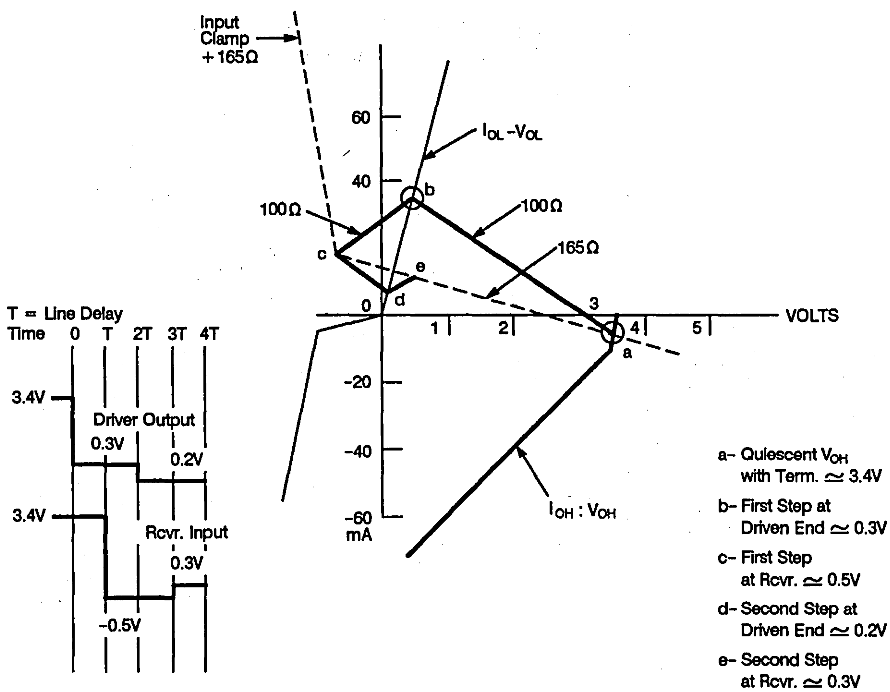


Figure 13. Reflections on a High-to-Low Transition

The points are generated by drawing load lines from the input and output characteristics of the devices. Reflections can be reduced by using short lead lengths and using appropriate terminations on the line.

The problems associated with reflections can be minimized by using appropriate terminations. In Figure 14, a step high-to-low voltage applied at the driver appears at the receiver.

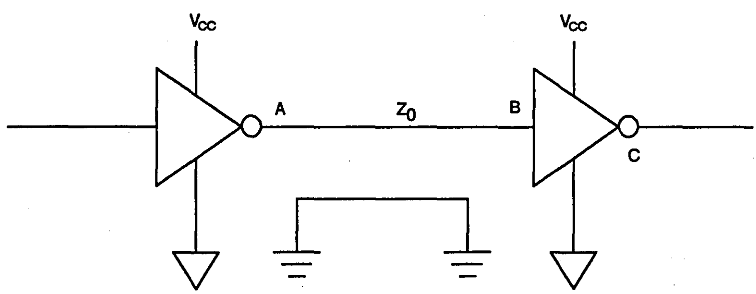
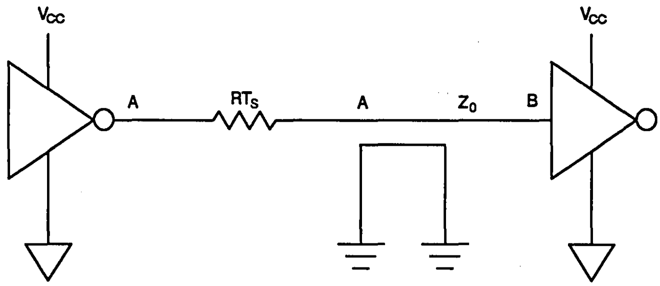


Figure 14.

Normally, there is no termination and the input step may try to double; however, due to the input clamp diode on the receiver, it settles to zero. FCT parts have a clamp diode only to ground and this helps negative-going excursions to clamp to a certain voltage. The FCT parts do not have a clamp diode to V_{CC} and this has other advantages when two systems having different V_{CC} levels are tied together, as explained under the System Advantages section. Another form of termination is series termination, as shown in Figure 15.



$RT_S = Z_0$

Figure 15. Series Termination

In this situation, the series value should be the effective impedance of the line less the output impedance of the driver. This matches the net source impedance with the line impedance, eliminating reflections from the source. Parallel terminations can be used as shown in Figure 16.

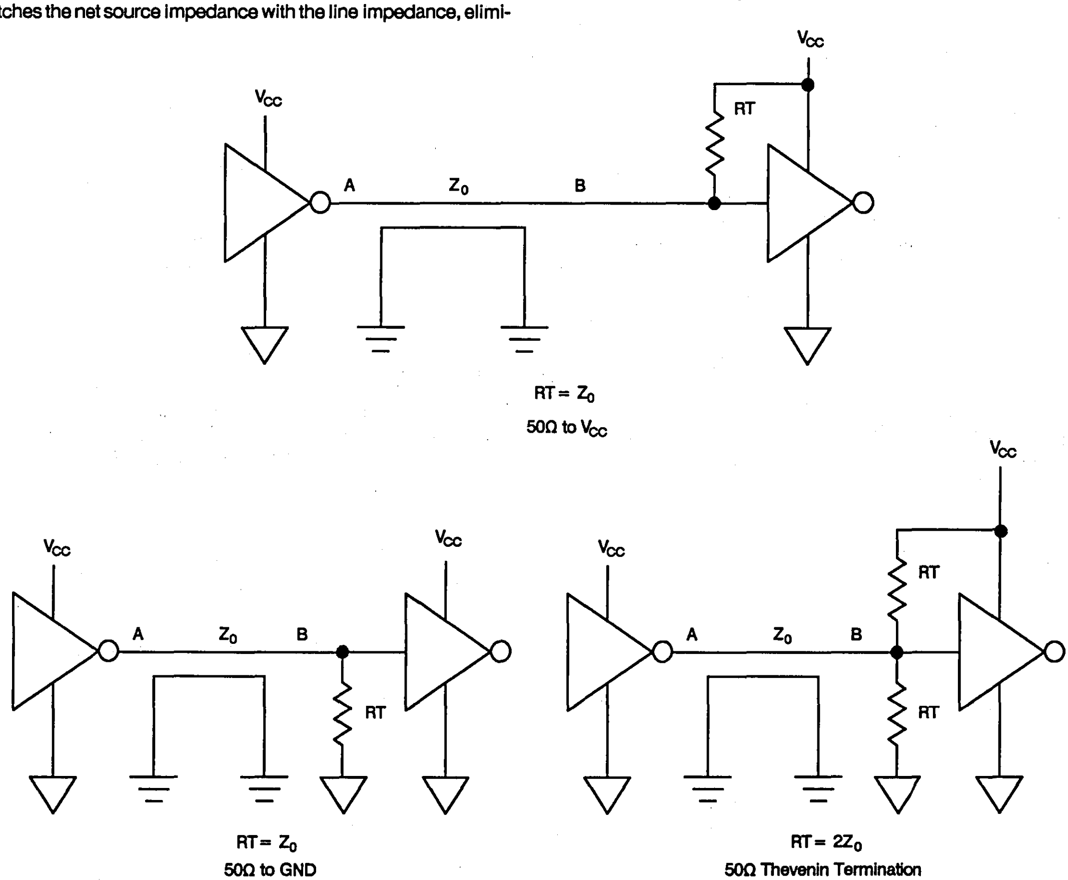


Figure 16. Parallel Terminations

14

These are resistive terminations to ground or V_{CC}, split resistor or Thevenin terminations. Resistive termination to ground or V_{CC} draws excessive DC current when the output is in the appropriate state due to the low value of the effective impedance. The Thevenin termination, which is popular with TTL circuits, does not work as well with CMOS-type circuits because, not only does one get DC resistive power in the termination, one also gets increased I_{CC} due to the resistive power in the termination due to the two transistors turning on in the input stage. Although the internal switching threshold of an FCT device is about 1.5 volts, there is more power consumed by the device with the inputs being at 2.5V than at 4.5V.

AC terminations, as shown in Figure 17, give no DC current drain and also terminate the line in the effective impedance.

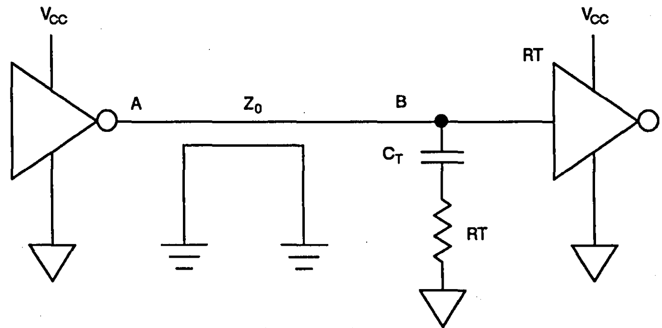


Figure 17. AC Termination

If used on a 3-state bus, the bus will remain in its last state for a few milliseconds. The capacitor should have an impedance XC at a value of less than 5% of the effective impedance and a frequency of $1/2t_{PD}$ of the line independent of the pulse repetition rate. A 10nF decoupling capacitor can be a good choice. The corresponding XC is about 100 milliohms and, therefore, RT should match the line impedance.

CROSSTALK

Crosstalk is caused by capacitive and inductive loading along parallel lines. Figure 18 shows transition on switching line A, B can affect another adjacent non-switching line, C, D.

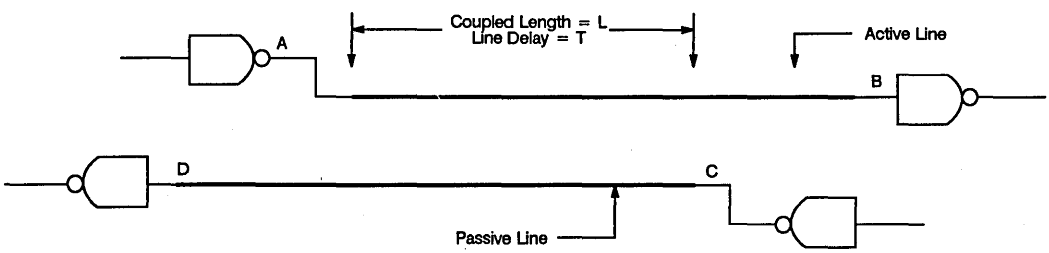


Figure 18.

The amplitude of the noise due to crosstalk is a function of the coupled length and the line delay. As shown in Figure 19, the line delay along the coupled length is compared to the rise time (t_R) and fall time (t_F)of the source.

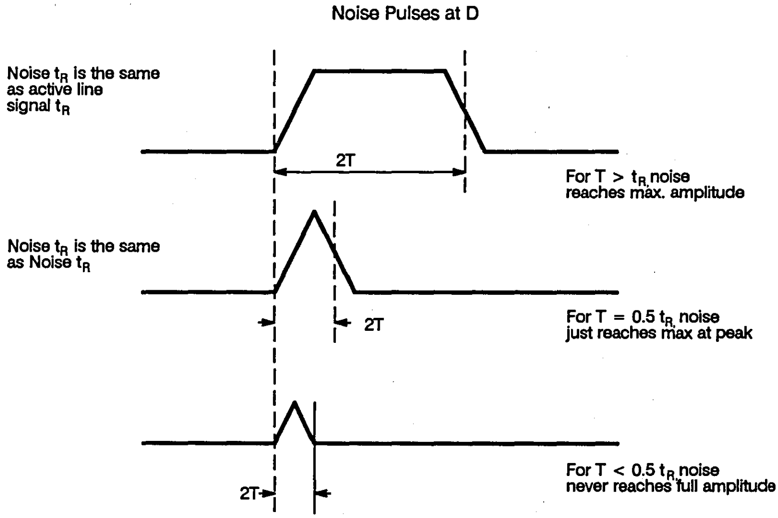


Figure 19. Crosstalk Amplitude for Different Line Delays

If T is long compared to t_R, the crosstalk pulse has time to develop to its full amplitude; if T is equal to 0.5 t_R , the reflection from the driven end of the passive line starts pulling the voltage down just as the noise pulse reaches full amplitude. Therefore, the noise in only a spike. When T< 0.5 t_R, the reflection arrives before the noise pulse and the noise amplitude is reduced even further.

The amplitude of the noise pulse can be reduced by using terminations. Figure 20 shows the noise amplitude when a terminating resistor is used.

Another way to reduce crosstalk in multi-layer configurations, is to place perpendicular signal lines in adjacent planes. Other general techniques for crosstalk reduction are to reduce spacing between signal lines, minimize spacing between signal lines and ground, run a ground trace alongside the cross-talker or cross-listener, use split-resistor terminations or make every other conductor in a flat cable a ground.

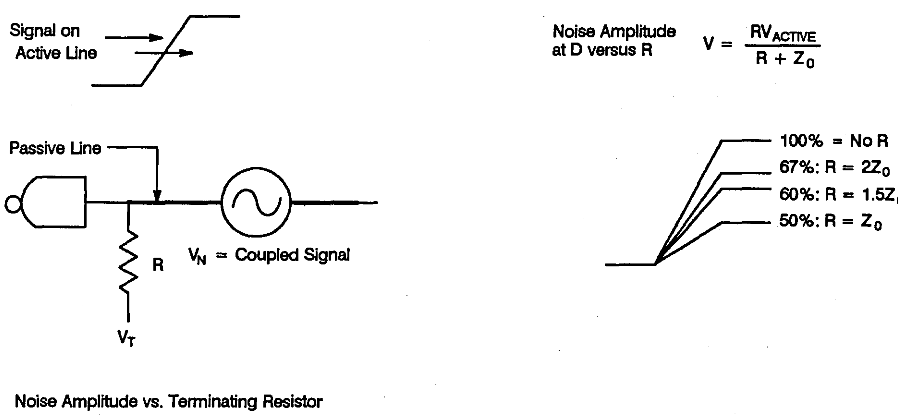


Figure 20.

14

SYSTEM ADVANTAGES

There are three significant advantages of using FCT devices besides high speed and low power. The typical input and output capacitance of FCT devices is 5pF and 8pF, respectively, measured at 1MHz and +25°C. Therefore, FCT loads the buses minimally.

Another advantage is the clamp diode on the input stage. Negative excursions on the input are clamped to -0.8 volts, thereby improving on reflected waves to the source.

A clamp diode for positive overshoots has intentionally not been added. The system advantage, compared to other CMOS-TTL families, is that one FCT device that has one V_{CC} level can drive another FCT device driven at another V_{CC} level without adding a series resistor. Currently, in other CMOS-TTL compatible families such as ACT, one had to add a series resistor of 100 ohms in the above application to limit the current flow from one voltage supply to the other when the second voltage supply was lower or not present. This is because ACT circuits have a clamp diode to V_{CC} in addition to clamp diodes to ground.

One design note on tying FCT outputs to buses when the device is powered down is that the output will clamp to 0.6 volts when some other bus driver is trying to pull it to an active high level. When the active driver pulls it low, there are no conflicting situations. A user must be aware of this in using FCT parts and powering them down to zero volts.

Section 4
Ground Bounce, ESD and Latch-Up

By Marcelo Martinez

GROUND BOUNCE

This noise effect is caused by large AC currents flowing in simultaneous switching outputs. It manifests itself as an instantaneous voltage drop on package and PCB ground inductances. This voltage can couple through a steady static output (worst case in the low state). This spike, riding on a normally low output, can be a concern in buffering edge triggered devices. Therefore, extra care is needed for this area.

Figure 1 illustrates the phenomenon for an octal buffer. LP and LB are the package and PCB ground inductances.

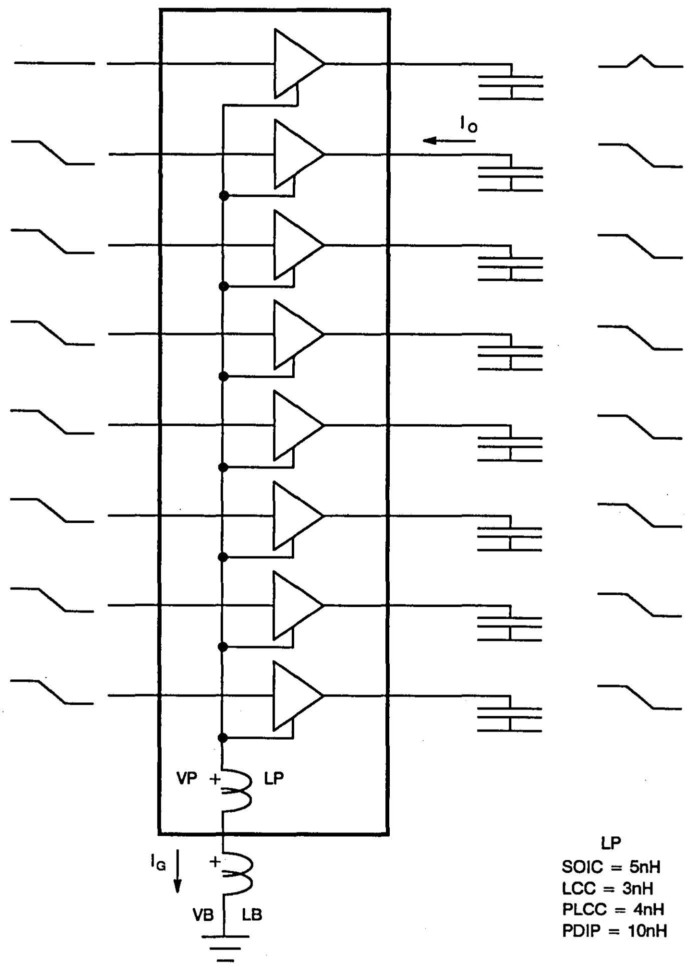


Figure 1.

The table shows the relative magnitudes of LP for different packages. In actual operation of the octal device shown, seven of the eight outputs switch high-low; the eighth one is held at ground by its input. Summation AC current I_G then flows through both inductances, causing the AC voltage drop VP and VB. The sum of VP and VB is then coupled to the output held at ground (it appears in the form of a spike in the top trace). VP + VB = (LP + LB) dI_G/dt $I_G = \Sigma IO$.

In most cases (octal buses, etc.), the spike is not a concern since it usually ends by the time the outputs switch (settling time). One must adhere to high-speed board design so that the spike doesn't propagate through the board's ground inductance (ground plane, for instance, and minimizing ground loop 0.5). Analyzing the effect of this spike further, it takes more than a V_{IL} (0.8V for TTL) amplitude to cause false triggering or pulse propagation for the driven device. Figure 2 illustrates this point.

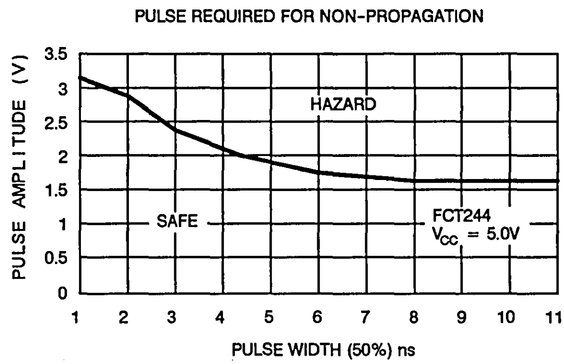


Figure 2.

Figure 2 shows an IDT74FCT244 being driven by various pulses varying in amplitude and duration. The graph shows the amplitude/pulse width combination necessary to cause the output of the IDT74FCT244 to violate a V_{OL}. Typically, the ground bounce spike 50% width is about 3ns; therefore, a 2.4V amplitude is needed for propagation, a number higher than typical spike amplitudes found in DIPs (worst case package). If additional immunity is needed in critical circuits, we can use surface mount packages which can decrease the spike amplitude by 40%. There are some vendors which have opted for bigger packages (multiple V_{CC}/V_{SS} pins); however, this approach has other inherent problems besides the obvious give-up in greater board space. By adding multiple grounds in the side of the package, the effective package ground inductances are substantially decreased. However, the edge rates will invariably be increased, causing additional crosstalk and ringing noise. Also, the dI_G/dt actually increases, causing a larger noise voltage across PCB inductances. Although the noise is decreased in the package, it increases in the board.

IDT has taken the correct approach to this noise concern in a new enhanced introduction of FCT logic. A new output structure has been developed which controls dI_G/dt rather than package inductances. The result is threefold: in DIPs, it reduces crosstalk and ringing and reduces the spike on PCB boards without sacrificing speed. FCT will be the easiest high-speed logic family to design in.

ELECTROSTATIC DISCHARGE PROTECTION

The input or output circuitry of all CMOS devices must be protected from high electrostatic discharges through special protection structures. This protection becomes increasingly important in state-of-the-art, high-speed CMOS where thinner oxides (lower gate voltage breakdown) and smaller geometries are used. IDT's 1 micron I/O structures meet MIL-STD-883's highest specification: Category B devices are not ESD sensitive below 2000V. Category B devices do not need special ESD handling procedures other than normal good practice.

The input protection circuit is designed to withstand large voltage and current spikes encountered in normal handling of devices.

The schematic for this structure, used in all FCT, is illustrated in Figure 3.

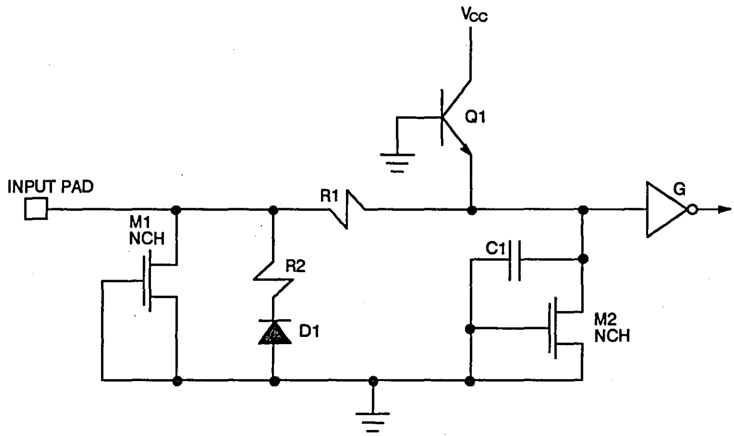


Figure 3.

The gate to be protected is shown as inverter G. Diode D1 and resistor R2 are really the drains of N-channel device M1 and act as a high current negative clamp to large negative voltage spikes. The area structure is large in order to handle the large currents. For large positive voltage spikes, device M1 breaks down at about 15V and diverts current from drain to source to ground. Again, this device is made large in area in order to handle large currents. The additional circuitry, composed of R1, Q1 and M2, is used to slow down fast ESD spikes at the pads in case D1 or M1 do not have enough time to act. Resistor R1 and capacitance C1 function as an RC delay circuit going into gate G. In addition, M2 clamps positive voltages at about 15V due to its breakdown and Q1 clamps negative voltages at about -0.6V.

Testing for ESD sensitivity is done according to MIL-STD-883C, Method 3015.2. The set-up is illustrated in Figure 4.

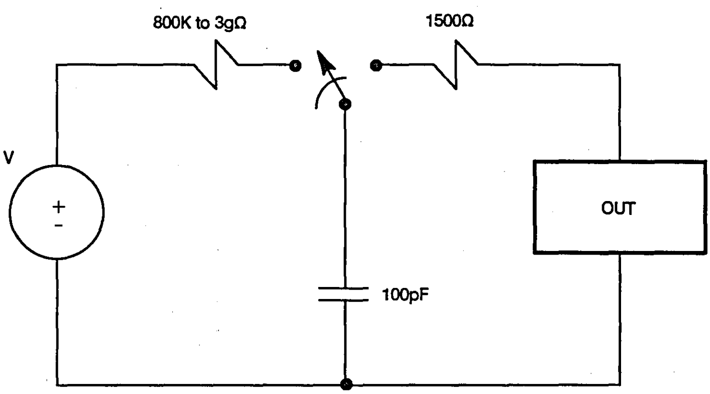


Figure 4.

The 1500Ω resistor and 100pF capacitor combination models the human. Essentially, the 100pF capacitor is charged to voltage V via the switch and then discharged through the device under test and the 1500Ω resistor. The part is then tested for damage. Usually an increase in input or output leakage is noted. The part is labeled "damaged" when the I/O leakages fail the data sheet specifications. This procedure is repeated 5 times at voltage V and -V. If the part passes, it is categorized as insensitive to voltage ±V.

Testing of FCT devices has shown typical protection up to 5000V. Even though the protection circuit provides good immunity to ESD damage, large ESD voltages can be generated by a person (more than 5000V); therefore, good handling practices still apply.

LATCH-UP

Latch-up has been a concern in the use of CMOS in the past. Much care has gone into eliminating this phenomenon under normal conditions. For example, minimum trigger currents are well above the maximum allowed current through any pin (120mA). However, the designer should be aware of latch-up, what causes it and how to prevent it.

The latch-up phenomenon can be easily explained by looking at a cross section of our CEMOS™ process illustrated in Figure 5.

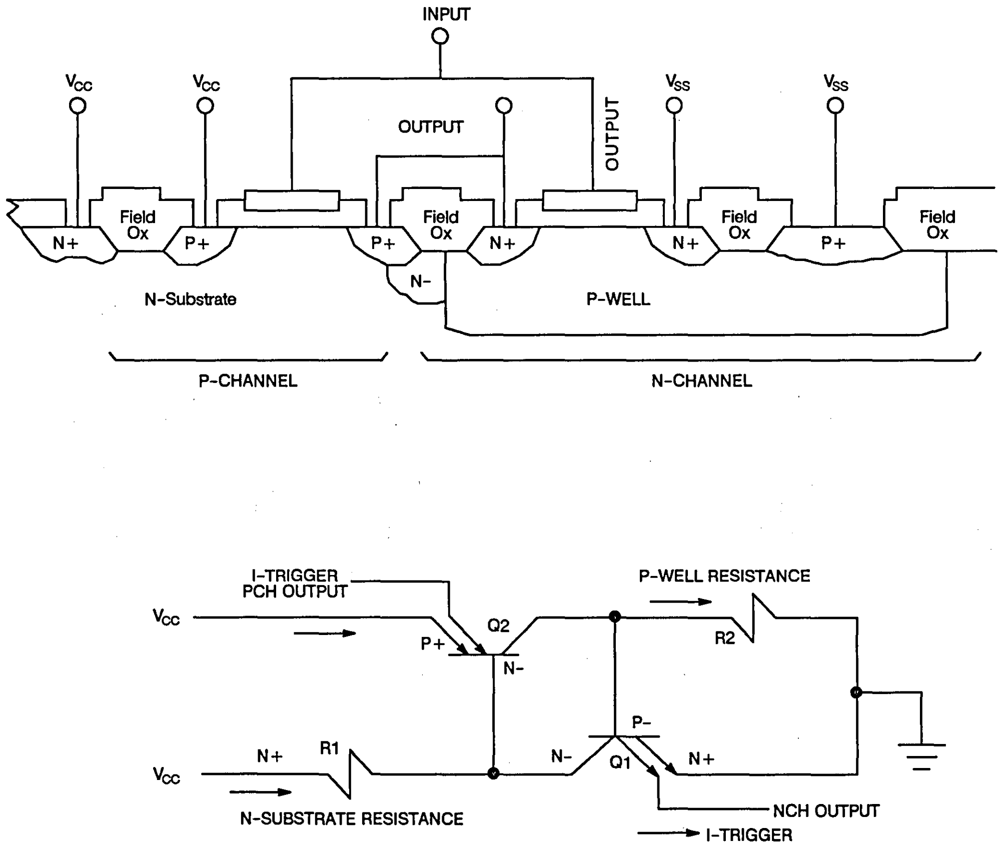


Figure 5. Process Profile and Schematic of Parasitic Bipolar Structures in CMOS Inverter

Figure 5 shows a typical output buffer and its parasitic bipolar equivalent schematic. The two emitters that trigger the SCR are connected to the output. Therefore, if the output is forced to be greater than V_{CC} by 0.5V, or below V_{SS} by 0.5V, the proper bipolar device is turned on. For example, if the output is forced below ground, collector current flows through R1 and Q1 causing a voltage drop across R1 which is the N-substrate. The voltage drop causes Q2 to be turned on if its base emitter magnitude is greater than a diode drop.

Q2 collector current then begins to flow which causes Q1 to turn on harder. At this point, latch-up has occurred since the collector currents flowing through V_{CC} and ground can be sustained even if the trigger current is removed. Since R1 and R2 are generally very low, the current flowing through V_{CC} can be > 1 A, which can blow the internal bond wires. Several steps were taken with FCT logic to substantially decrease latch-up susceptibility—among other things, decreasing R1 and R2, decreasing the betas of Q1 and Q2 and adding multiple collectors to divert current.

Another latch-up phenomenon is an internal one and can be triggered by V_{CC} overvoltage. In this case the SCR is triggered by internal MOS breakdowns. For the FCT logic line, the V_{CC} voltage needed for triggering is 10-12V, far above the normal operating range.

There are several methods and test circuits that can be employed to test for latch-up. The one primarily used to characterize the FCT logic family is shown in Figure 6.

Testing SCR Latch-Up of FCT

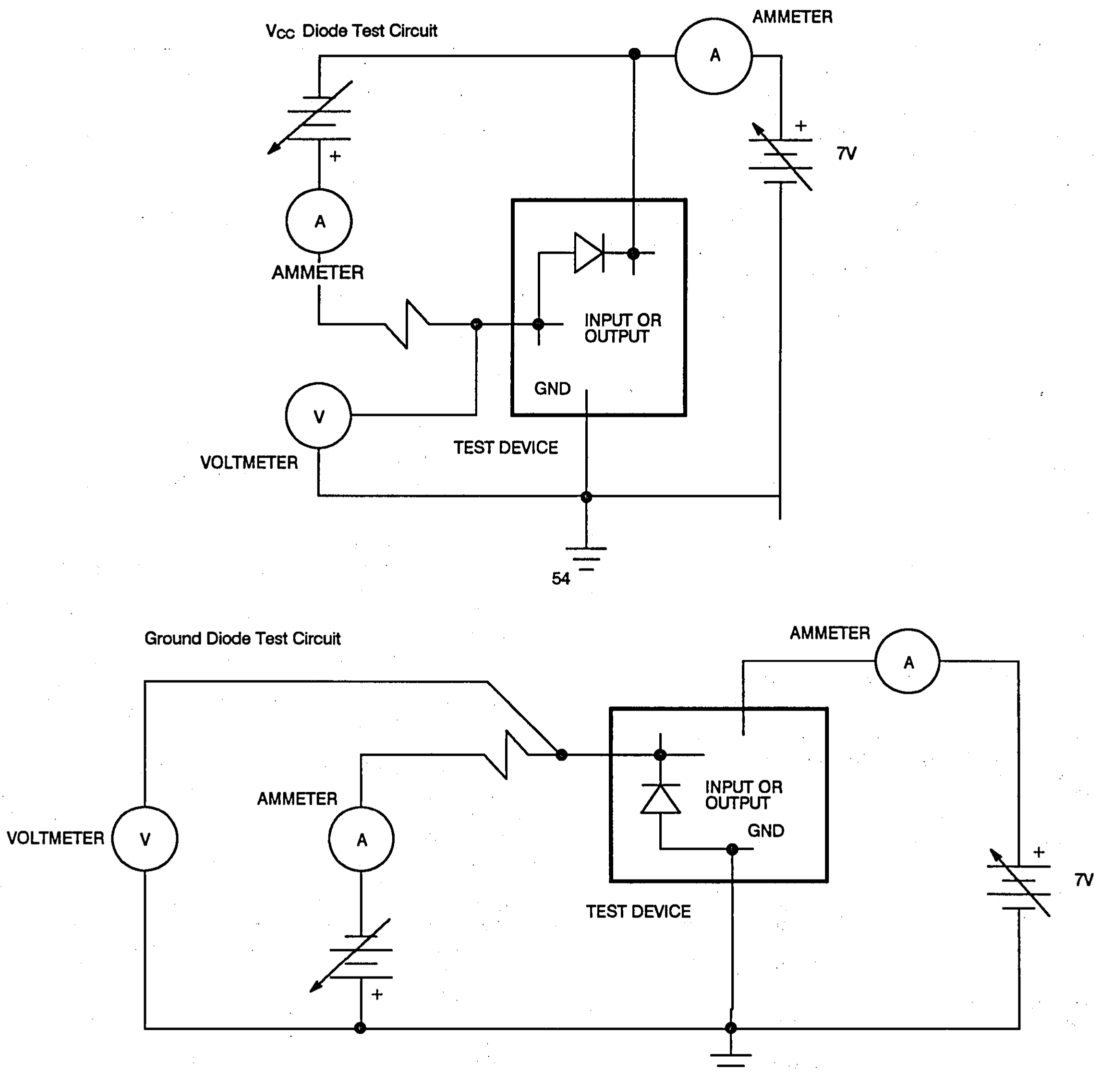


Figure 6.

This circuit utilizes several supplies and various meters to either force current into the Vcc diodes or force current out of the ground diodes. By controlling the input supply, a current is forced into or out of an input or output of the test device. As the input supply voltage is increased, the current into the diode increases. Internal transistor action may cause some supply current to flow, but this should not be considered latch-up. When latch-up occurs, the power supply current will jump and, if the input supply is reduced to zero, the power supply current should remain. The input trigger current is the input seen just prior to the supply current jumping.

Testing latch-up is a destructive test but, in order to test FCT devices without causing immediate damage, test limits for the amount of input or output currents and supply voltages should be observed. Even though immediate damage is avoided, the SCR latch-up test is destructive and the IC performance may be degraded when testing to these limits. Therefore, parts tested to these limits should not be used for design or production purposes. By not violating maximum electrical specifications, FCT logic is considered latch-up proof.

Section 5
Bus-Driving and Graphic Display Applications
By Suneel Rajpal

FCT devices have the basic functions register, latches, buffers, comparators, counters, decoders and, due to the inherent I/O capabilities, fit into many applications. In addition to 8-bit registers, buffers and latches, 8-bit, 9-bit and 10-bit versions are also available. FCT devices replace their equivalent 74F and 29800 devices, match or exceed the AC requirements and match the DC requirements, including I_{OL}.

Popular buses such as VME, Multibus and Multibus II have specific loading requirements. These are shown in tables MA to MC. FCT devices meet or exceed the requirements shown in these tables. In cases where 64mA drive is needed, drivers such as the IDT74FCT244 can be used.

Low State Sink Current	$I_{OL} \geq 48mA$
Low State Voltage	$I_{OL} \leq 0.6V$ @ I_{OL} = 48mA
High State Source Current	$I_{OH} \geq 3mA$
High State Voltage	$V_{OH} \geq 2.4$ @ I_{OH} -3mA
Drivers Off	
Current Sources by Board at 0.6V Including Leakage Current	$I_{OZL} = I_{IL} \leq 700\mu A$
Current Sunk by Board at 2.4V Including Leakage Current at 2.4V	$I_{OZH} = I_{IH} \leq 150\mu A$
Total Capacitive Load on Signal Including Signal Trade	$CT \leq 20pF$

Table A. VMEBUS Driving and Loading Requirements for Standard Three-State Lines (A_{01}-A_{31}, D_{00}-D_{31}, AM_0-AM_5, /IACK, /WRITE)

Low State Sink Current	$I_{OL} \geq$ = 48mA (BCLK/CCLK) I_{OL} = 32mA (Read/Write interrupt) $I_{OL} \geq$ 16mA (for address/data)
Low State Voltage	$V_{OL} \leq 0.5V$ @ I_{OL} = 48mA
Current Sourced by Board at 0.6V	$I_{IL} \leq$ 0.8mA (address, data) $I_{IL} \leq$ 2mA (read/write)
Current Sunk by Board at 2.4V	$I_{IH} \leq 125\mu A$ (address/data/read/write)
Total Capacitive Load On Signal	$CT \leq 18pF$

Table B. MULTIBUS Driving and Loading Requirements

Low State Sink Current Data and Address Requesting and Replying Agents	 $I_{OL} \geq 48mA$ $I_{OL} \geq 64mA$
Low State Voltage	$V_{OL} \leq 0.55V$ @ I_{OL} = max.
High State Source Current	$I_{OH} \geq$-3mA
High State Voltage	$V_{OH} \geq 2.4V$ @ I_{OH}= $-3\mu A$
Drivers Off Current Sourced by Board at 0.6V Including Leakage Current	$I_{OZL} + I_{IL} \leq 1000\mu A$
Current Sunk by Board at 2.4V, Including Leakage Current at 2.4V	$I_{OZH} + I_{IH}$ 100μA
Total Capacitive Load On Signal, Including Signal Trace	$CT \leq 20pF$

Table C. MULTIBUS II Driving and Loading Requirements for Standard Three-State Lines (AD31* -0*, PAR3*-PAR0, * SC9*-SC0*)

SERIALIZER FOR GRAPHIC DISPLAYS

Another more specific application for FCT devices is interface video RAMs. Pixel data is stored in memory and has to be read by the CRT. One popular storage device is Video RAMs or VRAMs. These devices consist of DRAMs that have a serial register on the outputs of the memory array. This architecture allows an entire DRAM row of data to be loaded in the serial register and to be displayed while the frame memory is updated/refreshed. The serial ports of the VRAM that output data may operate at a slower 25MHz rate. This may not be fast enough for the display refresh. One way to organize the data is shown in Figure 1. The frame buffer has 1K x 1K pixels. Each pixel may be 4 bits and therefore, can provide 16 different colors at a time. These pixels can be stored over 4 planes and each plane may be 16 64K x 1 DRAMs. In Figure 1 one plane is shown and the data may be disturbed so that P0 is in VRAM0, P1 is in VRAM1 (and so on), and P15 is in VRAM15.

Now P16 appears in VRAM0 again and the storage pattern is repeated. On displaying the data for one plane, all 16 VRAMs are accessed and a row of the DRAM memory (which is 256 bits wide) is stored in the serial register of the VRAM.

The 16 serial outputs of the VRAM can be fed directly to a RAM-DAC device that has serializing capability on board. The purpose of the RAM in the RAM-DAC is to select a particular color out of a palette of colors, thereby allowing a larger selection of displayable colors. The DAC portion is used to translate the digital value to the appropriate (red, green or blue) intensity level on the display. However, there are other possible configurations where the serializing capability has to be done before the data is sent to the RAM-DAC or even a DAC. In this case, an FCT299A allows a high-speed parallel-to-serial convert operation. These parts can be cascaded and the FCT299A allows a 70MHz operation in the cascaded mode. In the example shown in Figure 2, the data from four planes are loaded in parallel into four columns of FCT299As.

Each column consists of two cascaded FCT299As. Every 14ns a 4-bit parallel output is available that can be used as input to a DAC or a RAM-DAC.

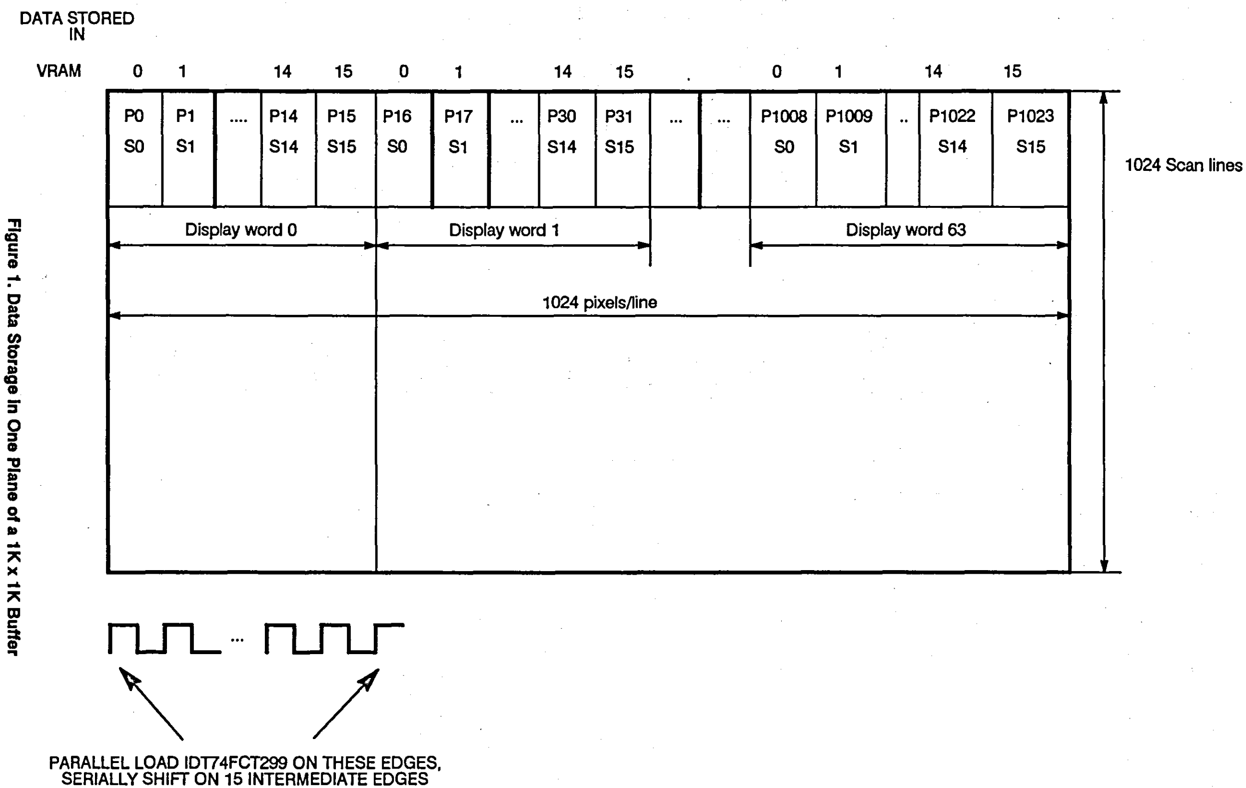


Figure 1. Data Storage in One Plane of a 1K x 1K Buffer

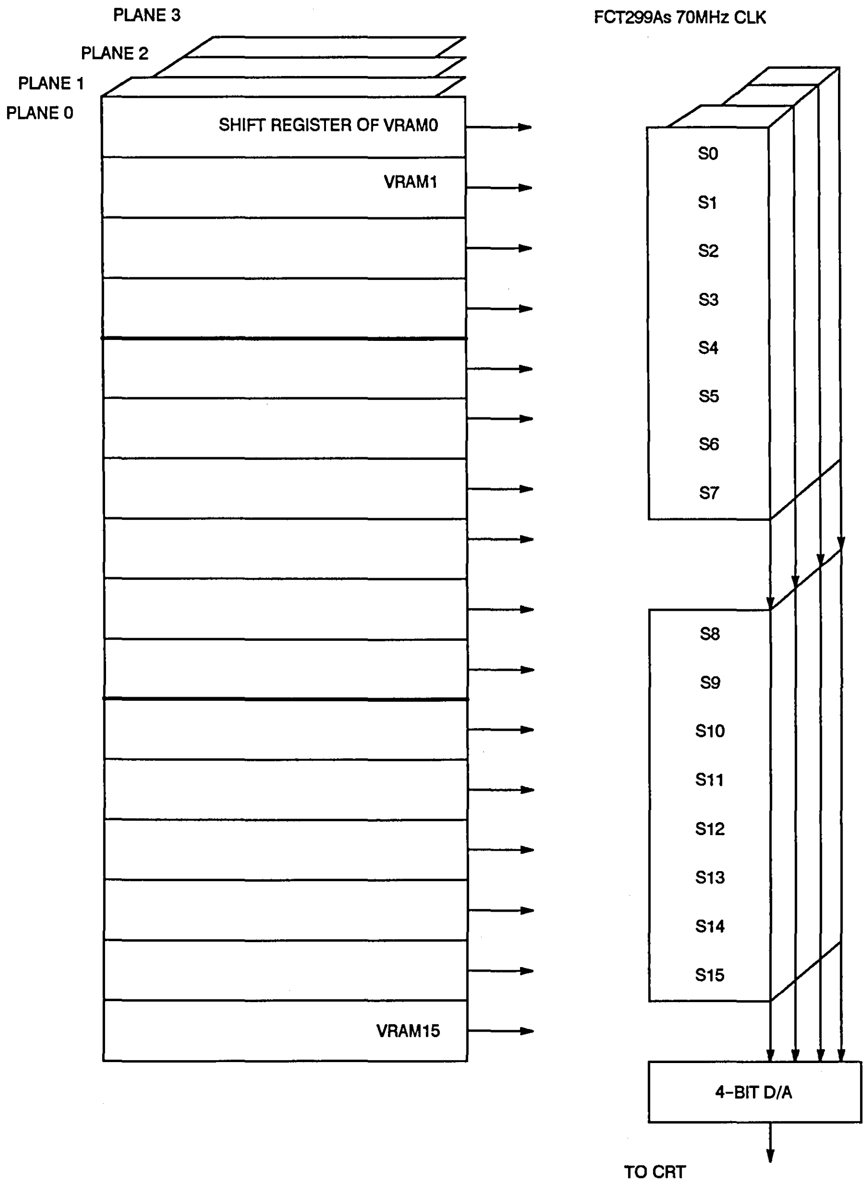


Figure 2. The Serializing Register IDT74FCT299A Interface to the VRAM

Section 6
Typical FCT Applications

The following are simple examples of using IDT's FCT devices in typical applications. They are intended to stimulate thinking of various other example applications of registers, latches, buffers, decoders, transceivers, comparators and counters.

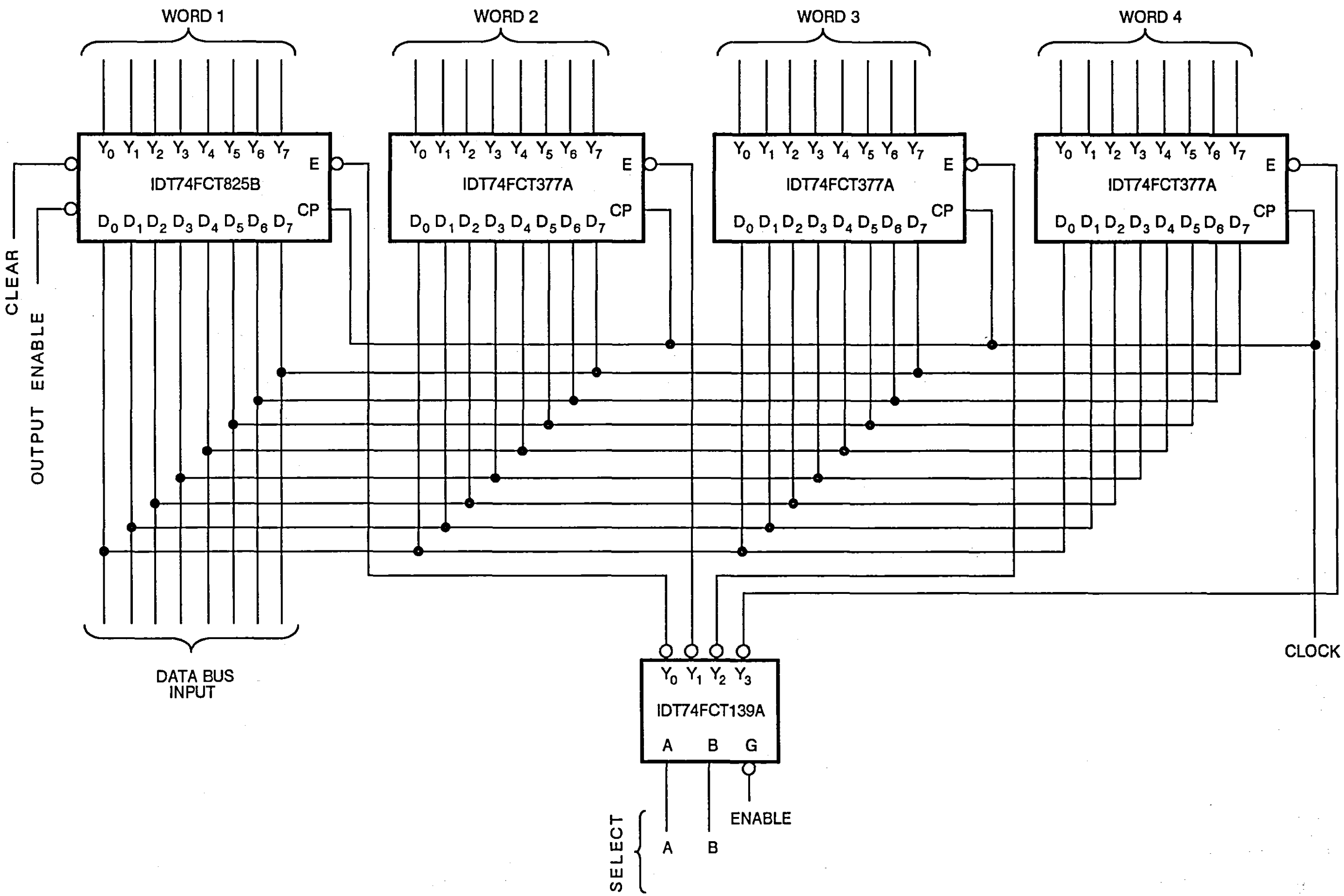


Figure 1. Selective Register Loading of Data on Synchronous Clock

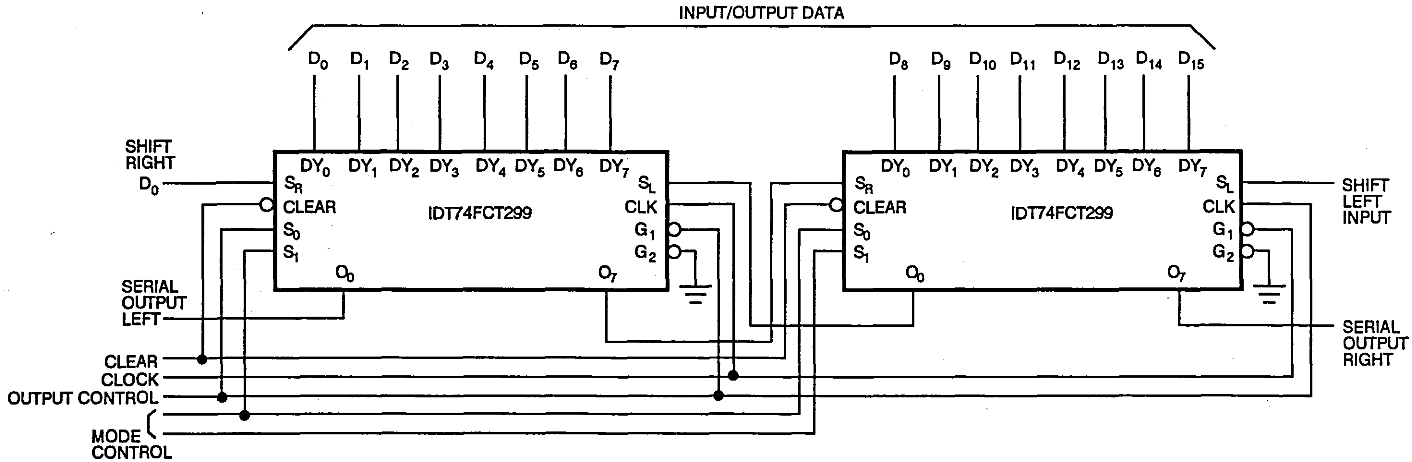


Figure 2. 16-Bit Cascaded Parallel Load/Unload Shift Right/Left Register Using IDT74FCT299s or IDT74FCT299As

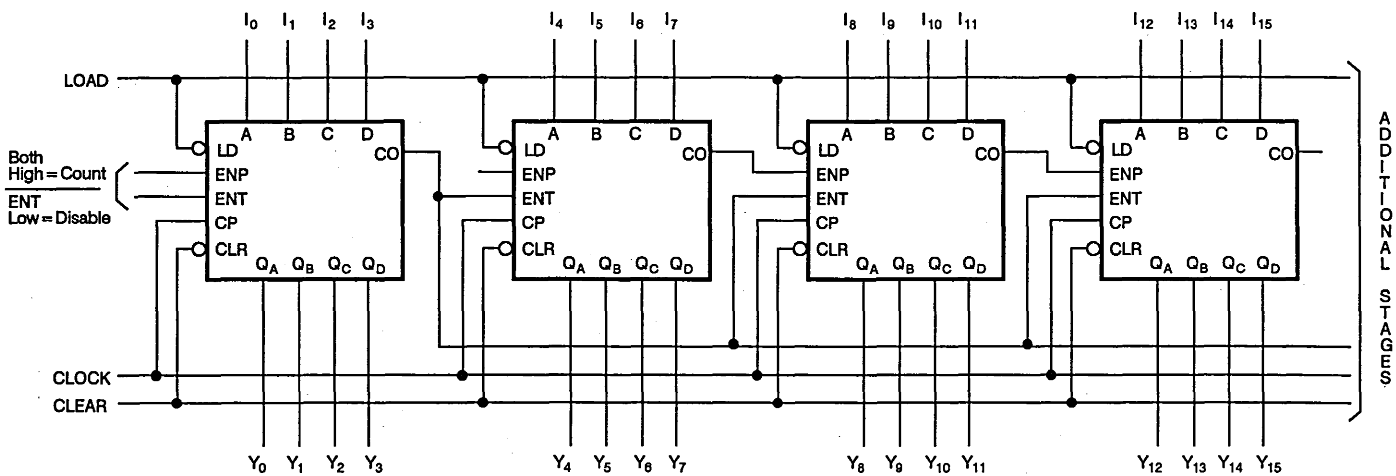


Figure 3. High-Speed Carry Lookahead Counter (IDT74FCT161A or IDT74FCT163A) — (Can count modulo N, N1-to-N_2 or N1-to-N maximum)

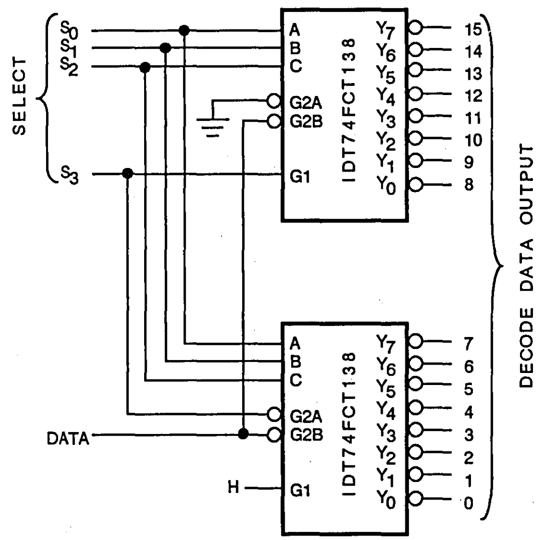


Figure 4. 1-of-16 Demultiplexer

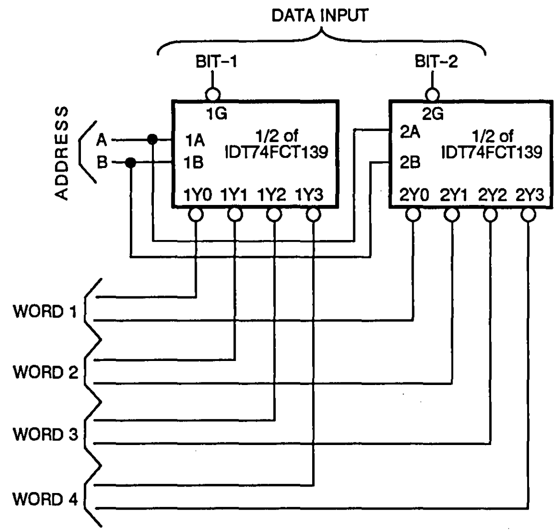


Figure 5. Data Routing Using One IDT74FCT139 as a Demultiplexer for Two Bits

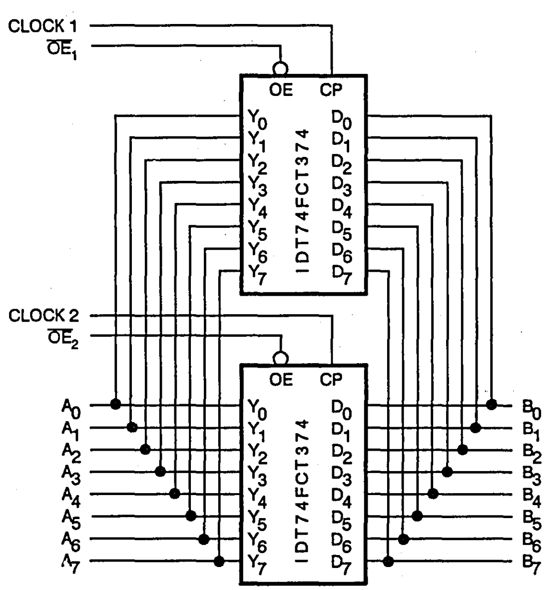


Figure 6. Two IDT74FCT374s Can Be Used as a Bidirectional Bus Driver/Register

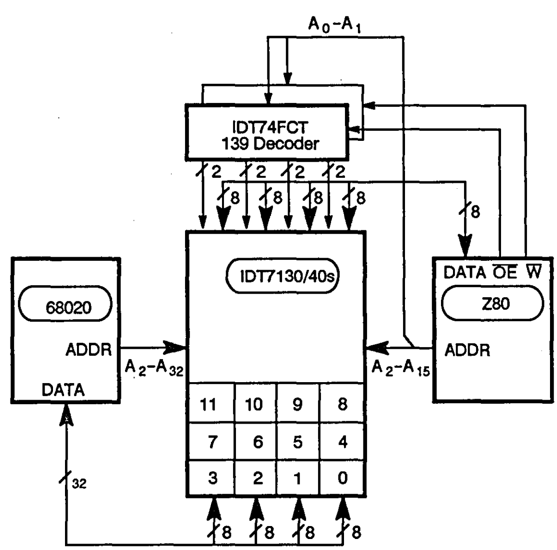


Figure 7. Interfacing 32/8-Bit Processors

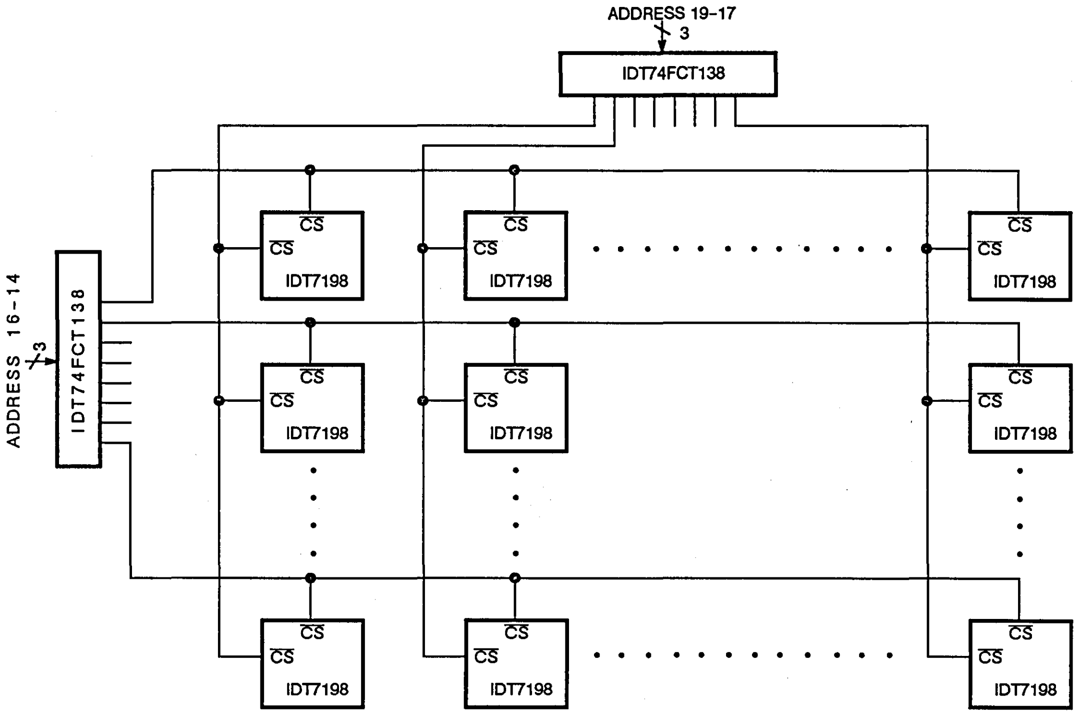
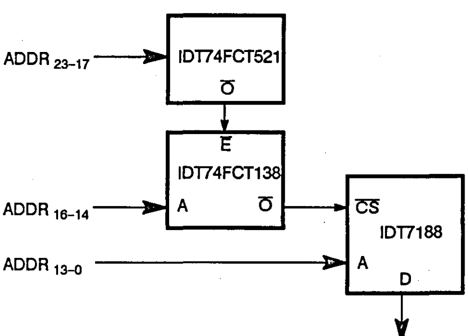
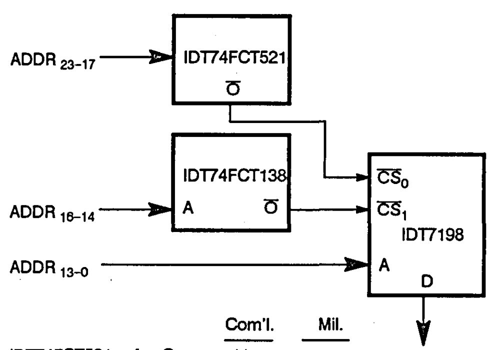


Figure 8. Memory Array Using Two $\overline{CS}$



		Com'l.	Mil.
IDT74FCT521	A - O	11ns	12.5ns
IDT74FCT138	E - O	9ns	14.0ns
IDT7188	CS - Data	35ns	45.0ns
		55ns	71.5ns

Figure 9. Standard Memory Design Using One $\overline{CS}$



		Com'l.	Mil.
IDT74FCT521	A - O	11ns	-
IDT74FCT138	E - O	-	14.0ns
IDT7188	CS - Data	35ns	45.0ns
		45ns	59ns

Speed Savings	9ns	12.5ns

Figure 10. Higher-Speed Memory Design Using Two $\overline{CS}$

14

Appendix A
Package Thermal Resistance
(In °C/Watt)

Package	θJC Junction-to-Case	θJA Junction-to-Ambient
Ceramic DIP		
16-pin (0.3)	35	90
20-pin (0.3)	28	75
24-pin (0.3)	26	65
Sidebraze DIP		
16-pin (0.3)	30	70
20-pin (0.3)	28	60
24-pin (0.3)	27	55
48-pin (0.4 x 70 mil)	21	38
48-pin (0.6 x 100 mil)	20	36
Plastic DIP		
16-pin (0.3)	45	74
20-pin (0.3)	40	70
24-pin (0.3)	35	65
LCC		
16-pin	45	–
20-pin	40	96
24-pin	35	90
28-pin	33	85
32-pin	31	83
48-pin	30	80
52-pin	30	80
PLCC/SOIC		
16-pin	40	90
20-pin	37	85
24-pin	34	80
28-pin	31	72
32-pin	30	68
48-pin	30	60
52-pin	30	58

Integrated Device Technology, Inc.

DESIGNING WITH FIFOs

TECHNICAL NOTE TN-06

by Suneel Rajpal and Frank Schapfel

FIFOs are First-In/First-Out buffers that act as elastic buffers between two synchronous or asynchronous systems. The IDT7201 (512 x 9), IDT7202 (1K x 9), IDT7203 (2K x 9) and IDT7204 (4K x 9) are high-speed FIFOs that can operate at frequencies greater than 20MHz. Here are a few tips on designing with these FIFOs.

A generic block diagram of the FIFOs is shown in Figure 1. After power up, the FIFO must be reset. The reset operation requires that the read and write lines be high for a time t_{RPW} or t_{WPW} (the read or write pulse width minimums) before the rising edge of $\overline{RS}$, and to be high for a time t_{RSR} after the rising edge of $\overline{RS}$. These operating conditions are shown in Figure 2. It is important to observe the stipulated requirements on $\overline{R}$ and $\overline{W}$ during reset because they increment the read and write pointers and both edges of the read and write also affect the empty and full counters. The Full and Empty Flag counters have to be appropriately set after a reset operation.

The read and write pointers are high-speed counters that are incremented on every rising edge of read and write lines. These lines must be noise-free as in other high-speed counters like F161s and AS161s. This poses a common interface issue that users often encounter. False clocks can be caused by transmission line effects or crosstalk. Some of the symptoms of false clocking are flags asserted when they should not be, missing data or scrambled data order.

The Read or Write signals may be generated by a part that is physically placed far away from the FIFO on a PC board. This implies a propagation delay to and from the driver to the receiver that is greater than the rise and fall time of the driver. This causes reflections on the line. Also the driver that has a low impedance on the high-to-low transition causes an impedance mismatch. The mismatch is apparent with an F-type device or a Schottky-TTL device as their high-to-low impedance is fairly small (typically under 15 Ohms for F-type or FCT and under 10 Ohms for Schottky-TTL). This translates to a signal that eventually settles near zero volts but, in the interim, has a "damping" effect; it may go through a -2.0 volt to + 1.5 volt to -1.0 volt to +.7 volt to zero volts. This is shown in Figure 3. The FIFO devices can handle a negative voltage level of 1.5V for less than 10ns. If a positive 1.1 voltage level persists for a pulse width greater than 5ns, the corresponding read or write pointer may increment. Data is either written or read twice, or garbage is written to or read from one or more locations. This can cause the FIFO to be "out of sync" where the read or write (or both pointers) are at wrong locations. This problem is solved by keeping the parts creating the $\overline{R}$ and $\overline{W}$ signal as close to the FIFO as possible. If FAST™ or Schottky devices are used, and if ringing occurs, add a series resistor of 20 to 50 Ohms so the impedance of the driver in the high-to-low transition, plus the series resistor, approximately equal the line impedance.

Read ($\overline{R}$) and Write ($\overline{W}$) should be high if read and write operations are not occurring. Crosstalk causes noise on the read and write lines that may be 1.1 volts or greater for more than 5ns. However, if read and write are high and noise appears on the line, the FIFO is more noise immune (as V_{OH} is higher on the driver when a CMOS device in being driven and the V_{CC} noise margin is greater than the ground noise margin). During a long clock low time of 150ns, for a clock cycle of 200ns, a spurious read or write can occur due to noise. If the system can handle it, a better recommended timing is a clock low time of 50ns and a clock high time of 150ns, giving better noise immunity.

Unused data inputs should be tied to ground or V_{CC}. In the standalone mode or width expansion mode, $\overline{XI}$ must be grounded and $\overline{FL}/\overline{RT}$ should be tied HIGH, given the retransmit feature is unused. Good board design techniques must be practiced and a ground plane or power distribution element are highly recommended. Decoupling capacitors of 0.1µf disk capacitors should be used to decouple V_{CC} and ground.

14

FAST is a trademark of Fairchild Semiconductor Co.

Printed in the U.S.A. 1/87

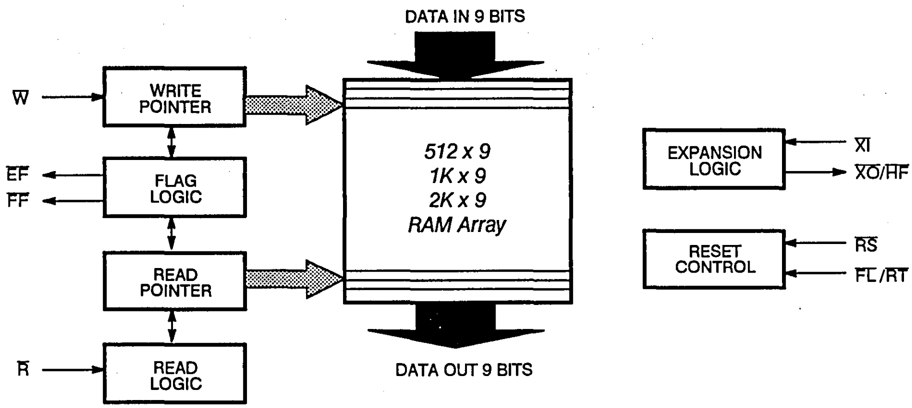


Figure 1. FIFO Block Diagram

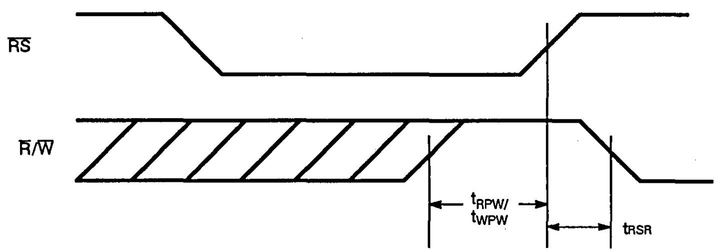


Figure 2. Reset Requirements

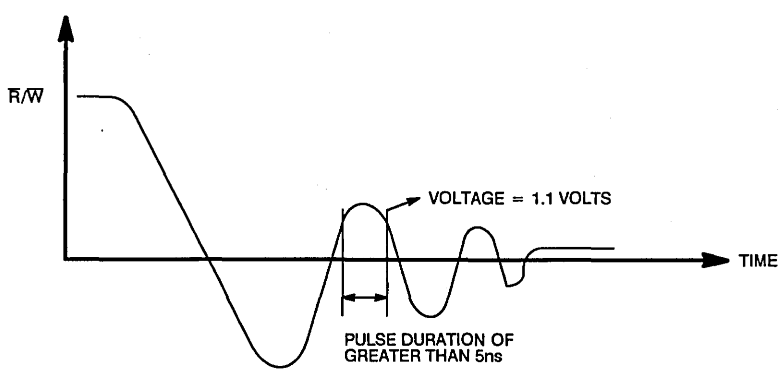


Figure 3. Reflections and Undershoot on the Read and Write lines that cause false increments on the Read and Write pointers

Integrated Device Technology, Inc.

FAST RAMs GIVE LOWEST POWER

TECHNICAL NOTE TN-07

by John R. Mick

INTRODUCTION

Many types of equipment such as airborne flight equipment and ground-based, battery operated equipment require the lowest possible power for their operation. Often, design engineers choose the slowest possible memories thinking that they are minimizing the power dissipation. In many applications, this does not necessarily represent the lowest power system.

UNDERSTANDING THE TRADEOFF

Most CMOS static RAMs have several different power supply specifications depending on their mode of operation. For example, the operating power supply current (I_{CC}) can be quite high. Many CMOS static RAMs have one or two different standby currents specified. The first of these is the TTL level standby current usually designated as I_{SB}. The second of these is the full CMOS standby power level usually designated as I_{SB1}. These two standby currents are usually considerably lower than the operating power supply current.

DESIGN EXAMPLE

Let us suppose that we have a microprocessor system that has a required bus cycle of 200ns. For the purpose of this design example, let us assume that if we select a slow static RAM (such as 120ns), we can design the system so that the chip select is low for 120ns and high for 80ns. This gives a total microprocessor bus cycle time of 200ns. The result of such a system is that, while the chip select is low, the operating power supply current is drawn. For the purpose of this example, let us assume that 90 milliamps is required. Similarly, while the chip select is high, the full CMOS standby power supply current is drawn and, in this example, let us assume it is 0.9 milliamps. The net result is that the average power dissipation to operate the RAM in this speed range is 275 milliwatts. This is shown in Figure 1.

A second design possibility exists in which we could select a very fast static RAM (such as 35ns). Let us assume the IDT7198L35 for the purpose of this example. In this design, a 200ns bus cycle is again required for the design, but now we will operate the RAM as fast as possible. This will result in the chip select being low for a total of 35ns and high for a total of 165ns. The net result is that, for the IDT7198L35, while the chip select is low, we draw an active power of 110 milliamps. While the chip select is high, we draw a CMOS standby power of 0.9 milliamps. This results in a total average power for the system of 100 milliwatts.

SUMMARY

As can be seen from the above example, and referring to Figure 1, utilizing the fastest static RAMs can result in the lowest overall operating power for this system. This takes advantage of the much higher speed of the RAM and the resulting low duty cycle for which we draw the high amount of power. Thus, we can see that one should not just choose a slow RAM for a low-power system, but rather the designer should consider the fastest possible static RAMs and utilize the low operating duty cycle when implementing the system.

FAST RAMs = LOWEST POWER

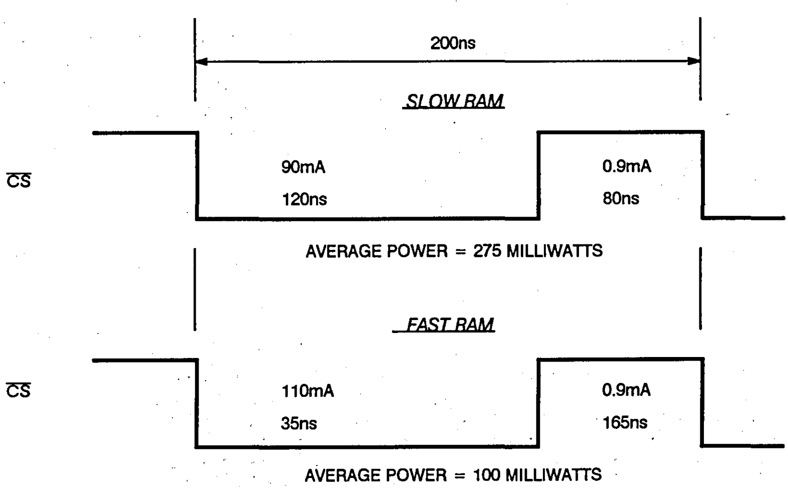


Figure 1. Active Chip Select Time for 200ns Cycle

14

Printed in the U.S.A. 1/87

Integrated Device Technology, Inc.

OPERATING FIFOs ON FULL AND EMPTY BOUNDARY CONDITIONS

TECHNICAL NOTE TN-08

by Suneel Rajpal and Frank Schapfel

The IDT7201, IDT7202, IDT7203 and IDT7204 (512 x 9, 1K x 9, 2K x 9 and 4K x 9) FIFOs have only four control lines: Read, Write, Reset, Retransmit. The focus of this tech note is the relation of the Read and Write lines to the FIFO's empty and full conditions.

These high-speed FIFOs can perform asynchronous and simultaneous read and write operations. Read and Write assert and deassert the Empty Flag and Full Flag. Therefore, special conditions exist when a full FIFO continues to be written to and a read operation takes place. Also, special timings occur when an empty FIFO continues to be read to and a write operation takes place. These operations are called the FIFO boundary conditions.

Read and Write increment the read and write pointers on their respective rising clock edges. The read and write pointers affect the Empty Flag and Full Flag counters. The Empty Flag timings are shown in Figure 1. When the FIFO has only one word in it, the falling edge of the Read causes the Empty Flag ($\overline{EF}$) to be asserted. After the clock cycle is completed (Read goes high again), $\overline{EF}$ will remain asserted and the internal read counter is not affected by subsequent read cycles. $\overline{EF}$ is deasserted by the next rising edge of Write, after which another read pulse can be applied to do a read operation. In asynchronous systems, read and write operations take place at any time; $\overline{EF}$ is set by one signal and deasserted by another asynchronous signal.

When Read is being clocked on an empty FIFO, the outputs will be in high-impedance. If a write operation is performed during asynchronous read cycles, a possible violation of the read pulse width minimum can occur, as shown in Figure 2. $\overline{EF}$ is deasserted, but there is an insufficient read pulse minimum width. To prevent the minimum read pulse width violation, initiate a read operation only after $\overline{EF}$ is high, or guarantee a long enough read pulse width minimum time. A violation of the timing causes an internal glitch on the FIFO Read which can cause the read pointer to be "out of sync." Then the data inside the FIFO may be scrambled or may be garbage. The Empty Flag and Full Flag counters may also be upset by the internal glitch, which upsets FIFO memory usage. The only way to recover from this violation is to do a master reset.

A similar situation arises at the full FIFO boundary condition. When the FIFO is one word from being full, the falling edge of Write causes the Full Flag ($\overline{FF}$) to be asserted. After the write cycle is completed (Write goes high again), $\overline{FF}$ will remain asserted and the internal write counter is not affected by subsequent write cycles. The $\overline{FF}$ flag is deasserted by the next rising edge of the Read, as shown in Figure 3, after which another write pulse can be applied to do a write operation.

When the FIFO is full and Write is being clocked, data sent to the FIFO will be ignored and the write pointer will not increment. Here, as in the earlier case, if these write cycles are asynchronous during a read operation, a possible violation of the write pulse width minimum can occur, as shown in Figure 4. Here, $\overline{FF}$ is deasserted but a sufficient write pulse minimum width is not met. To prevent the problem, initiate a write operation only after $\overline{FF}$ is high, or guarantee a long enough write pulse width minimum time. A violation of the timing causes an internal glitch on the FIFO write line. This can cause the write pointers to be "out of sync" where the data inside the FIFO may be scrambled or may be garbage. The Empty Flag and Full Flag counters may also be upset by the internal glitch. Again, the only way to recover from this condition is to do a master reset.

In summary, these FIFOs are designed to transfer only valid data from input to output. To ensure that valid data is written into and read from, empty and full FIFOs handshake through the flag mechanism. When there is no output data available, the reading side must wait until the end of a write. In a full FIFO, the writing side must wait for the reading side to create an "empty" location. Incomplete read and write cycles can not only invalidate data, but can cause the pointers to be out of synchronization, requiring a master reset to renew data transfer.

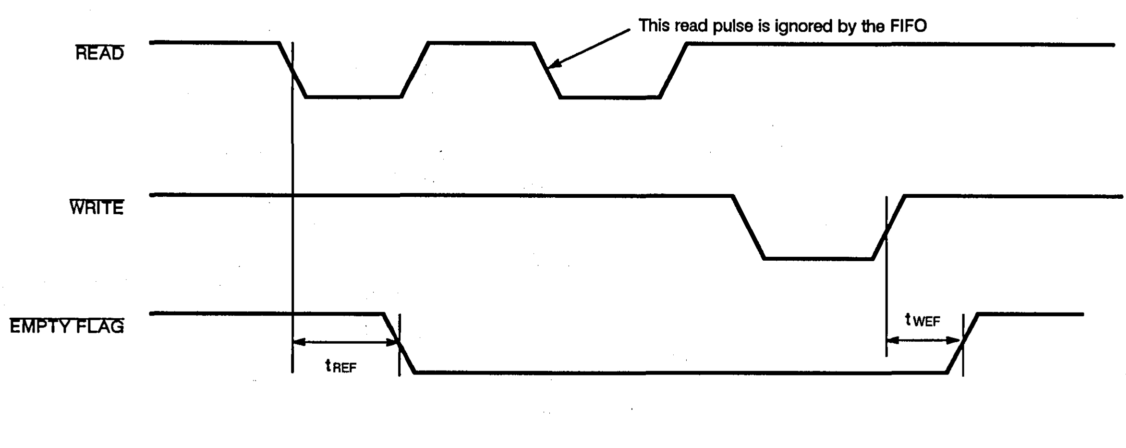


Figure 1. Empty Flag from Last Read to First Write

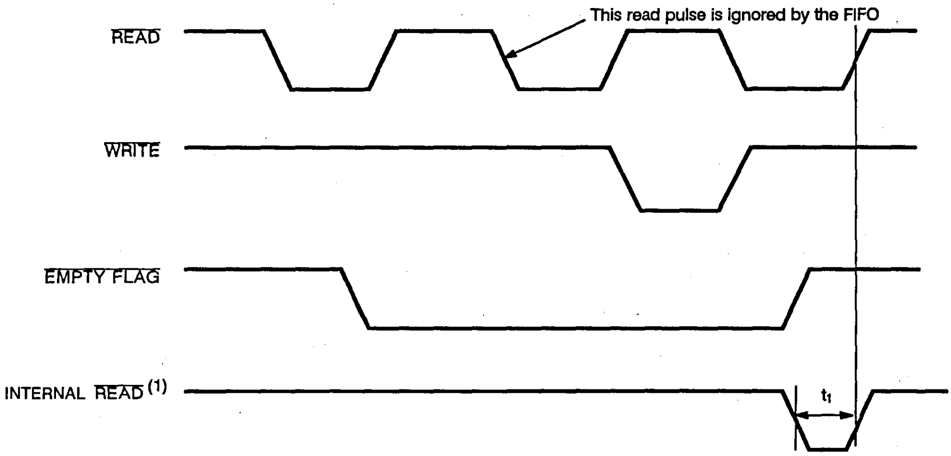
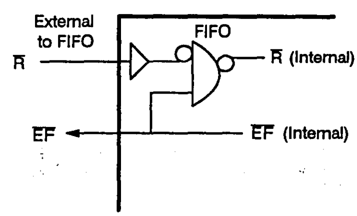


Figure 2. Violation of t_{RPW} During Boundary Conditions

Note:

1. Pulse within the FIFO used to clock the read pointer and the Empty and Full Flag counters.
2. If $t_1 < t_{RPW}$ (minimum read pulse width low), then the read pointer, Empty Flag and Full Flag counters may be out of sync. See Figure 15 of IDT7201/2SA data sheet.



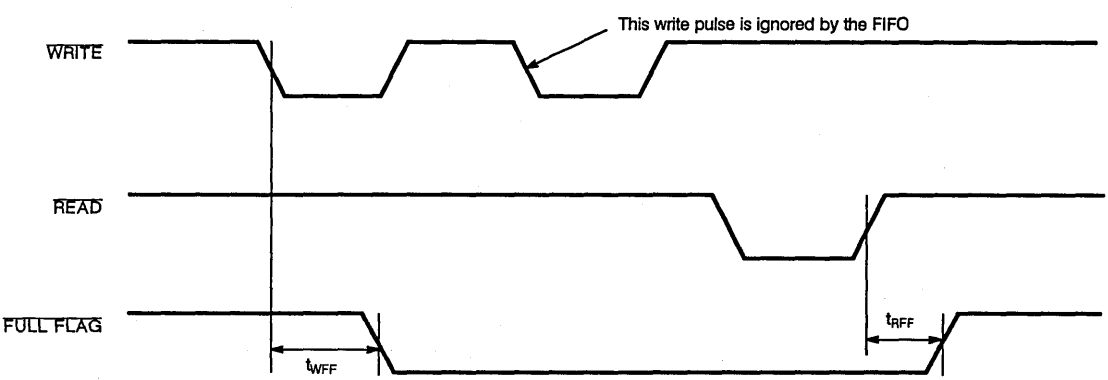


Figure 3. Full Flag from Last Write to First Read

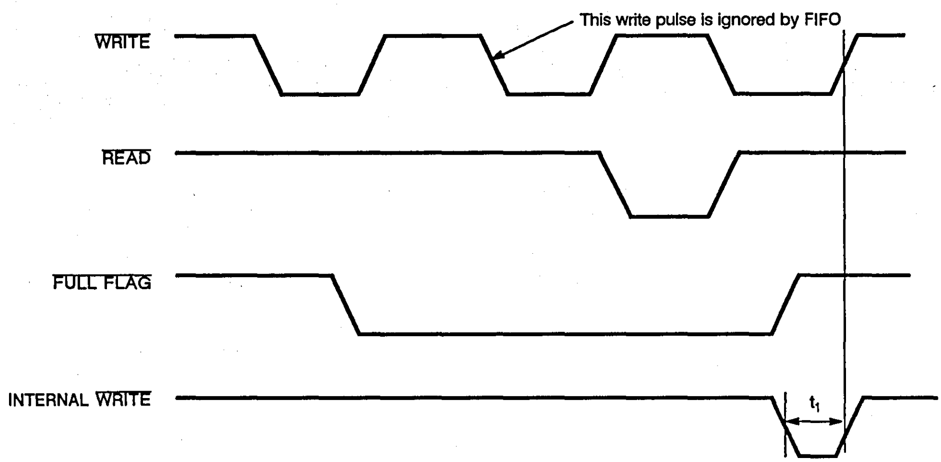
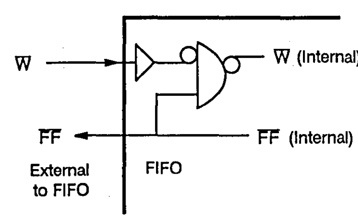


Figure 4. Violation of t_{WPW} During Boundary Conditions



Note:

1. Pulse within the FIFO used to clock the write pointer and the Empty and Full Flag counters.
2. If $t_1 < t_{WPW}$(minimum write pulse width low), then the write pointer, Empty Flag and Full Flag counters may be out of sync. See Figure 16 of IDT7201/2SA data sheet.

Integrated Device Technology, Inc.

CASCADING FIFOs or FIFO MODULES

TECHNICAL NOTE TN-09

by Suneel Rajpal and Frank Schapfel

The IDT7201, IDT7202, IDT7203 and IDT7204 are high-speed 512 x 9, 1K x 9, 2K x 9 and 4K x 9 FIFOs, respectively, that can be cascaded to form even deeper FIFOs. This tech note explains how these FIFOs are cascaded. The principles mentioned here also apply to the IDT7M203, IDT7M204, IDT7M205 and IDT7M206 high-speed 2K x 9, 4K x 9, 8K x 9 and 16K x 9 cascadable FIFO modules, respectively.

A cascaded FIFO configuration of 512 x 9 FIFOs is shown in Figure 1. The $\overline{FL}$ pin (First Load) of the first FIFO to be loaded after a reset is tied to ground. The other FIFOs have their $\overline{FL}$ pin tied to V_{CC}. After a reset operation, the first 512 writes occur in the first FIFO. During these write operations, the $\overline{XO}$ (Expansion Out) and $\overline{XI}$ (Expansion In) lines are high. On the 512th write, a pulse is created on the $\overline{XO}$ line following the $\overline{W}$ line. The pulse informs the second FIFO that it is going to receive the next word. It also informs the first FIFO that its write pointer will no longer increment due to an internal evaluation of the $\overline{XO}$ line. The $\overline{XO}$ line of the first FIFO is connected to the $\overline{XI}$ line of the second FIFO. The $\overline{XO}$ of the second FIFO is connected to the $\overline{XI}$ of the third, and so on. The $\overline{XO}$ of the last FIFO is connected to the $\overline{XI}$ of the first FIFO. A typical $\overline{XO}$ operation of 2048 writes after a reset is shown in Figure 2.

The same procedure holds true for read operations. During the 512th read operation after a reset, another pulse will be created on the $\overline{XO}$ line following the Read line. This pulse will inform the second FIFO that it will be read from on the next cycle (provided it isn't empty). Also the first FIFO's read pointer will not increment until it receives a second pulse on its $\overline{XI}$ line.

Figure 3 shows the $\overline{XO}$ and $\overline{XI}$ relationship to read and write. The $\overline{XO}$ pulses are transferred to the $\overline{XI}$ of the next level of FIFO. The first pulse transfers write pointer control and the second transfers read pointer control. There is an important advantage to this method expansion. A word written to the FIFO after a master reset is immediately available at the FIFO output. A read cycle can be initiated as soon as $\overline{EF}$ is unasserted. This is called zero fall-through time. Earlier shift register-based FIFOs have a fall-through time in the µsec range.

To take full advantage of this unique expansion feature, some design precautions must be observed. Since a pulse on $\overline{XI}$ activates read or write operations of the FIFO, they must be relatively free from cross-talk noise. A long trace from the $\overline{XO}$ of the last FIFO to the $\overline{XI}$ of the first FIFO is a potential source of cross-talk noise. To prevent noise spikes from altering the $\overline{XI}$ input on this and other $\overline{XO}$ to $\overline{XI}$ interconnects, a small capacitor in the 22pF to 47pF range should be inserted between the $\overline{XI}$ inputs and ground.

Another important point is how to handle flags in the expansion mode. To create the composite Full Flag, tie the four individual FIFO Full Flags to an OR gate. The composite Empty Flag is created similarly. This additional logic is shown in Figure 1.

To create intermediate flags using the individual Full and Empty flags is more tricky, but can be done. For example, an attempt to create a composite Half-Full Flag is described here. Let us define Flag f1 as when any two FIFOs are full and at least one other FIFO is not empty. Boolean Equation for f1:

$$
\begin{aligned}
f1 = {} & FF1.FF2(\overline{EF3}+\overline{EF4}) + \\
& FF2.FF3(\overline{EF1}+\overline{EF4}) + \\
& FF3.FF4(\overline{EF1}+\overline{EF2}) + \\
& FF4.FF1(\overline{EF2}+\overline{EF3})
\end{aligned}
$$

FFi = Full Flag of FIFOi

EFi = Empty Flag of FIFOi

In one extreme case, f1 is asserted when there is 1.5K-1 words in the FIFO array. The first two FIFOs are full, with 512 words in each, and the third FIFO has 511 words. Another extreme case is when two FIFOs are full and the third FIFO has only one word. Therefore, Flag f1 is only a range of words where the half-full condition exists, from 1K+1 to 1.5K-1 words in the array. It may not be used as a half-full indicator, because the FIFO array may be almost 3/4 full before Flag f1 is asserted.

As shown in Figure 4, an empty FIFO array has a word written to it and then read from it. Then, 1.5K-1 words are written to the FIFO array. The write pointer is on the last word of the third FIFO. Only at this time is Flag f1 asserted, while the FIFO array has 1.5K-1 words in it. Intermediate flags like f1, generated from Boolean Equations, can only provide a range of values when f1 is to be asserted. A precise position for f1 cannot be determined. If Boolean Equations are used to generate intermediate flags, consider all the different locations of the read and write pointers which may assert or deassert at a particular condition.

Printed in the U.S.A. 2/87

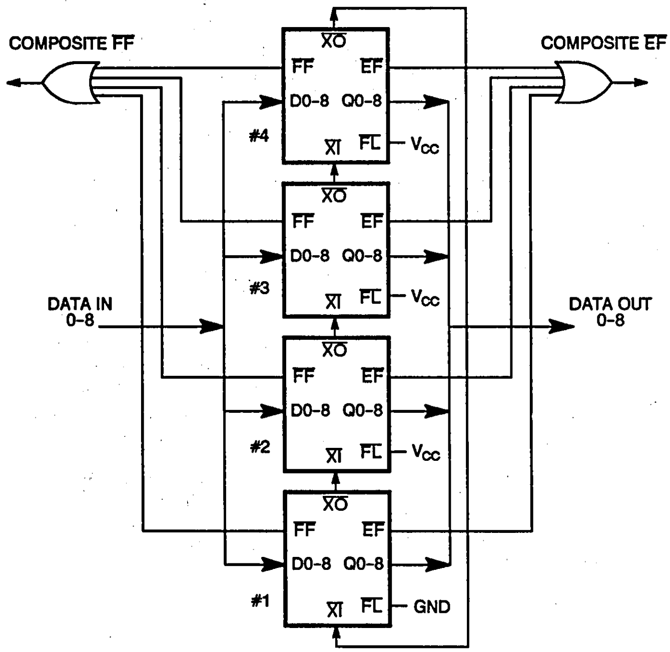


Figure 1. Four Cascaded 512 x 9 FIFOs

NOTE:
Read, Write and Reset controls go to all four FIFOs.

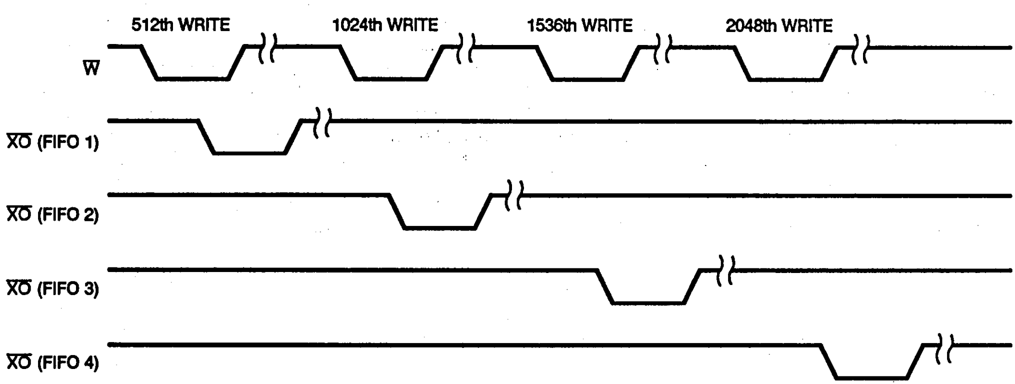


Figure 2. The XO/XI Timing Pulse for 2048 Writes and Zero Reads

NOTE:
Read line is assumed to be HIGH in this example.

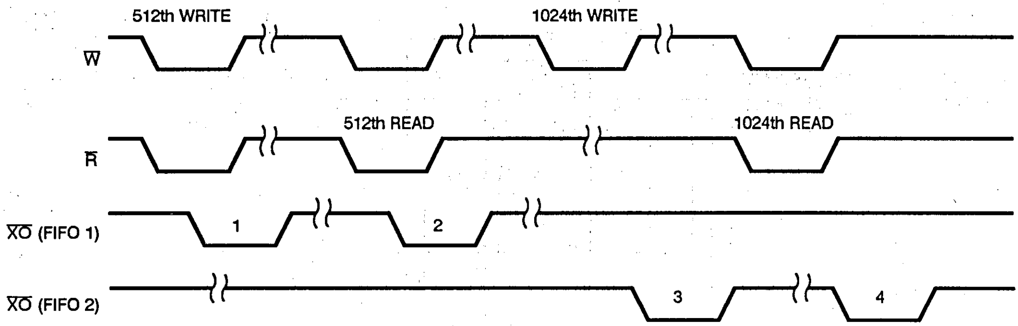


Figure 3. The $\overline{XO}$ and $\overline{XI}$ Pulse Timings

NOTES:

1. Pulse 1 is created by the 512th write pulse; it is a delayed write pulse.
2. Pulse 2 is created by the 512th read pulse.
3. Pulse 3 from FIFO 2 is created by the 1024th write pulse.
4. Pulse 4 is created by the 1024th read pulse.
5. $\overline{XO}$ (FIFO 3) and $\overline{XO}$ (FIFO 4) are not shown, but they follow the same pattern.
6. $\overline{XO}$ (FIFO 4) will be created by the 2048th write pulse and later by the 2048th read pulse, thereby transferring pointer control back to FIFO 1.

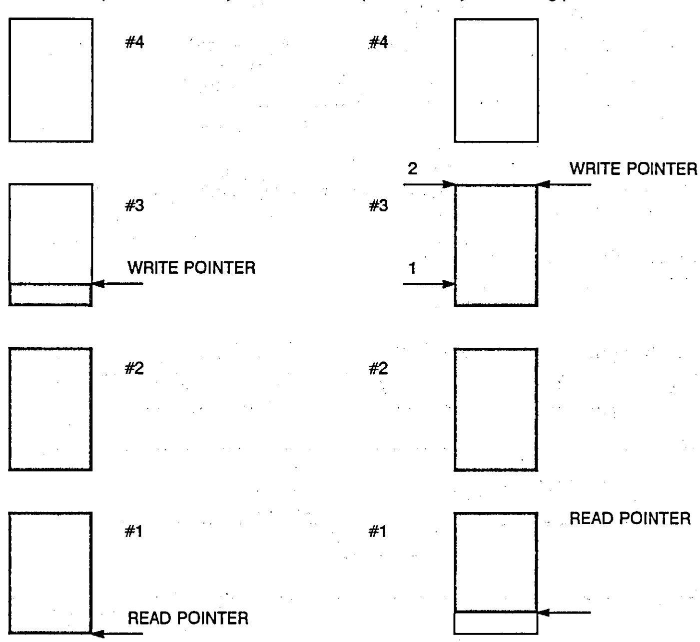


Figure 4. The Behavior of the f1 Flag for Different Cases

Case 1: In the cascaded FIFO arrangement, the write pointer has just written to FIFO #3 and the flag defined by the f1 equation would be asserted at the half-full point.

Case 2: The FIFO array is half-full at arrow at Note 1, but f1 will not be asserted until the last write into FIFO #3 or until the FIFO array is almost 3/4 full or at arrow 2.

Integrated Device Technology, Inc.

DUAL-PORT RAM ADDRESS ARBITRATION METASTABILITY TESTING

TECHNICAL NOTE TN-10

by David C. Wyland

SUMMARY

IDT has developed special testing methods for dual-port RAM address arbitration logic to ensure that their busy timing specifications are conservative and completely specified, even under the low probability conditions of metastability. This technical note discusses these special testing methods.

INTRODUCTION

Dual-port RAMs such as the IDT7130, IDT7132 and IDT7133 contain address arbitration logic which provides a busy signal to one of the two ports when both ports are accessing the same address at the same time. In many systems, the timing of these address signals is asynchronous. This allows a situation where both addresses arrive at the arbitration logic at exactly the same time and the logic must decide which side will receive the busy signal. When the signals arrive at the internal logic at exactly the same time, the settling time of the busy signal is longer than normal due to an effect known as metastability. Metastability time is included in the specifications of IDT dual-port RAM arbitration logic.

The additional settling time due to metastability is difficult to measure because the signals must arrive at exactly the same time for the metastability effect to be measurable. Because small amounts of on-chip and system noise will change the timing, metastability measurements are, by nature, statistical. As a result, the extra time for metastability cannot be directly tested. However, it can be estimated from parameters that can be tested.

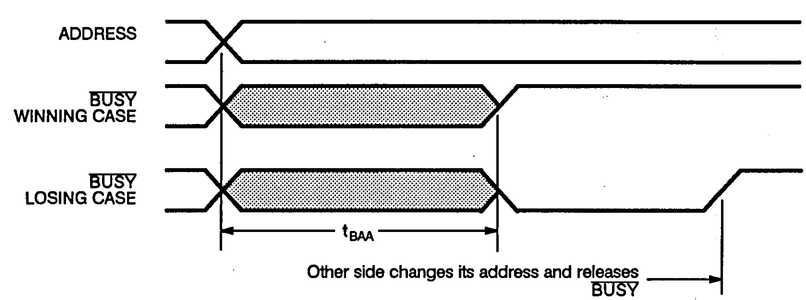
ARBITRATION PARAMETERS DEFINITION

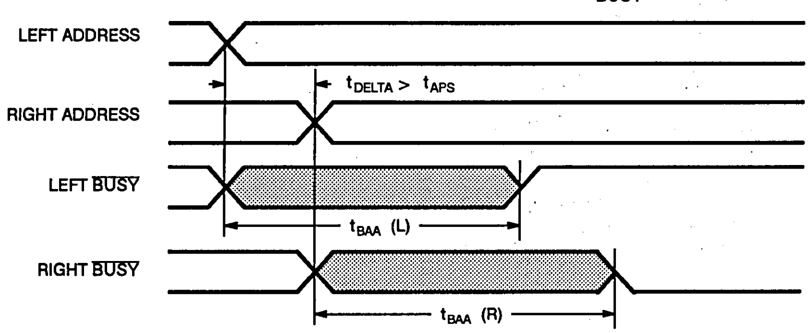
There are two major specifications for the dual-port arbitration circuit: the $\overline{\text{BUSY}}$ access time (t_{BAA}) and the arbitration priority set up time (t_{APS}). The $\overline{\text{BUSY}}$ access time specification is the most important. It defines the maximum time delay from the point that the address settles on one side to the time that the $\overline{\text{BUSY}}$ output will be stable on that side. This is shown below for both the case where $\overline{\text{BUSY}}$ is inactive (winning case) or active (losing case).

Several points should be noted about this specification:

- t_{BAA} is a maximum; it holds under all conditions, including metastability.
- $\overline{\text{BUSY}}$ can glitch high and low during t_{BAA}, similar to a RAM access time.
- If $\overline{\text{BUSY}}$ is high following t_{BAA}, it will not change until the address is changed.
- If $\overline{\text{BUSY}}$ is low following t_{BAA}, it will not change until the other side changes its address and releases the arbitration.

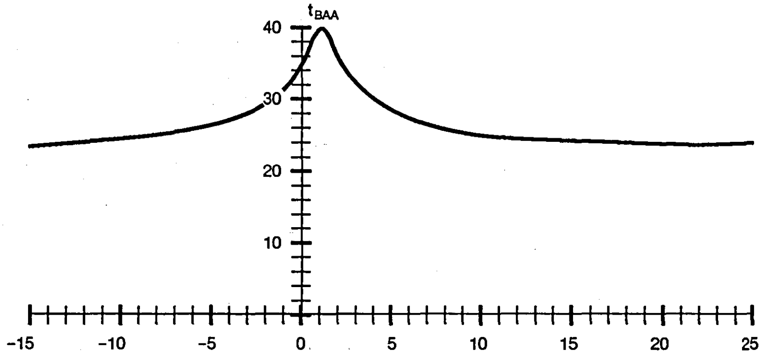
The arbitration logic determines when both sides are addressing the same location and it sends a $\overline{\text{BUSY}}$ signal to the side whose address settled last. This logic requires some time to work which leads to some ambiguity for simultaneous signals. For example, if the second address arrives too soon after the first, the logic will not be able to determine which was last and will arbitrarily pick one side or the other. The minimum time required between the two addresses to guarantee that the late one gets the $\overline{\text{BUSY}}$ signal is the arbitration priority set-up time, t_{APS}. If the late address arrives after t_{APS}, the late side will always get the $\overline{\text{BUSY}}$ signal; if it arrives earlier than t_{APS}, $\overline{\text{BUSY}}$ may be assigned to the early side. This is shown below for the case where the right side address arrives after the left side address ($\overline{\text{BUSY}}$ is active low). The delay between the addresses is called t_{DELTA} in this case.





METASTABILITY

The $\overline{BUSY}$ access time (t_{BAA}) varies with the delay between addresses (t_{DELTA}) in the figure on page 1. As t_{DELTA} approaches zero, the $\overline{BUSY}$ access time increases. This is shown in the sketch below. (Note: The curve shape is a rough estimate, although the values at the peak and at large t_{DELTA} are accurate.)



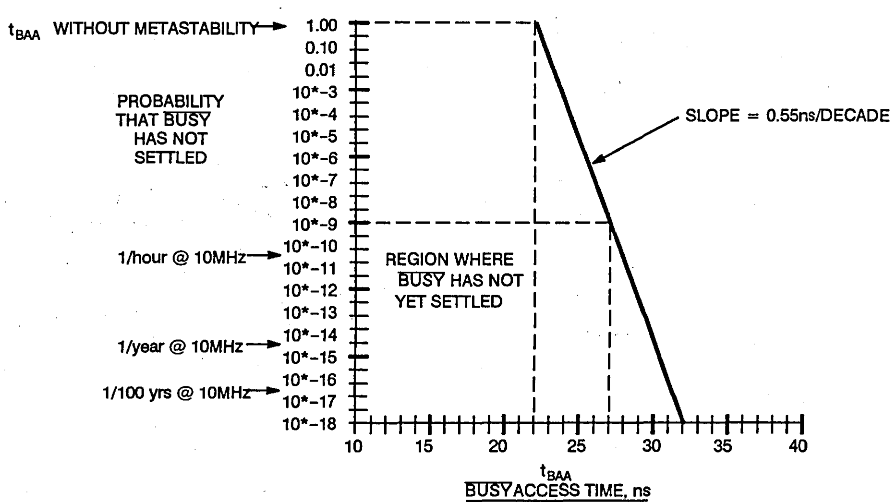
t_{DELTA}: Arrival Time of Right Address Relative to Left Address

The peak value corresponds to both address-compares arriving at the arbitration logic at the same time. In this condition, the arbitration latch is evenly balanced and must regenerate to one side or the other. This evenly balanced state is called the metastable state. If one address-compare arrives much earlier than the other, one side of the latch will be held off and the metastable state does not occur. It takes longer for the latch to settle to its final state from the metastable state than if the metastable state does not occur. This is shown on the graph. The metastable state does not occur at a t_{DELTA} of 50ns or more and the corresponding $\overline{BUSY}$ access time is 24ns. The peak value of 40ns corresponds to the settling time from the full metastable state.

Metastability is a theoretically unavoidable condition. Attempts to foil it by trying to bias the latch toward one side when the addresses arrive simultaneously only shifts the peak location to another value of t_{DELTA}. Also, in typical ICs, the peak does not occur at a t_{DELTA} of zero but is shifted one way or the other, depending on random delays in the particular chip.

The peak value shown in the t_{BAA} versus arrival time graph can only be measured statistically. The peak delay value corresponds to a perfectly balanced latch which must regenerate to one side or the other. This condition of perfect balance cannot be repeatedly achieved for a given set of input signal timings due to noise coupled into the latch from the input signals and internally from other parts of the chip.

The peak value is measured by repeatedly scanning the input signals through the arbitration window and measuring the delay time. The statistics of the measured delay times are used to generate a curve of probability as a function of the delay time. This is the origin of the notation of one failure per 100 years, etc. A plot of the data from a typical part is shown below. This plot shows the probability that the $\overline{BUSY}$ output has not yet settled as a function of the amount of time you wait for it to settle. Actual testing yields data for times between 1.0 and 10**-9ns; the lower probabilities for longer times are extrapolated from this data.



The plot on the previous page can be used to estimate the frequency of failure of $\overline{\text{BUSY}}$ to settle as a function of how long it takes to settle. The notes on the probability axis refer to these estimates. These notes assume that the system is repeatedly creating the metastable state at a 10MHz rate by applying the addresses at the same time. If you wait 27ns for $\overline{\text{BUSY}}$ to settle under these conditions, it will fail to settle by that time once in 10**9 times, or once every 100 seconds. If you wait approximately 31ns, it will fail to settle once per 100 years. Note that the 22ns time corresponding to probability 1.0 is also the time for the case where there is no metastability. This occurs when one address arrives a long time before the other. In the non-metastable case, $\overline{\text{BUSY}}$ will settle out in 22ns.

The 10MHz metastable inducement frequency is much higher than would be experienced in real systems. The actual metastable inducement frequency for a typical, high-performance system is less than once per second. This would increase the mean time to failure from once in 100 years to once in 10**9 years for the 31ns case mentioned above.

The reasoning for this is as follows. If both sides are accessing a 1024 word dual-port memory, the probability of access of a particular address by one side is on the order of one part per 1024. The probability of both sides simultaneously accessing the same address is the product of the probabilities for each side, or one part in 10**6, assuming a random use of the addresses by both sides.

If both sides are accessing the RAM, the probability that the addresses will arrive close enough in time to induce metastability is also small. If we use the t_{APS} time of 5ns as a conservative estimate of the metastability inducement window, the probability of the two sides accessing within this window is 5ns divided by the cycle time, i.e. 5/100 for a 100ns cycle time.

If we combine these results, we can estimate the actual frequency of metastability inducement as a function of the system cycle time:

Fmeta = Fcyc* (1/words per RAM)2 * (t_{APS}/t_{CYC})

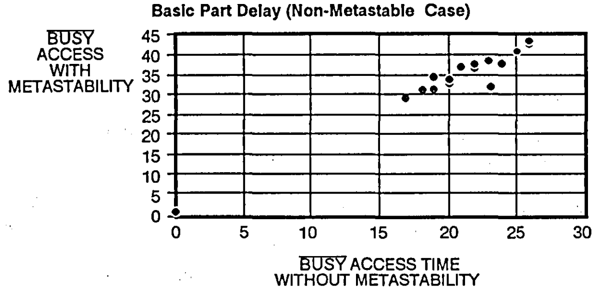
= Fcyc* (1/words per RAM)2 *(t_{APS}) *(Fcyc)

= (1/words per RAM)2* (t_{APS})* (Fcyc)2

= (10**-6)* (5.0*10**-9)* (10**7)2

= 5.0* 10**-1 = **0.5Hz**

$\overline{\text{BUSY}}$ Access Time for the Metastable Case
vs
Basic Part Delay (Non-Metastable Case)



Metastability settling time should be a function of the inherent speed of the part. This is because the regeneration time of the latch is determined by the gain-bandwidth of the devices. This has been verified experimentally. A plot of the $\overline{\text{BUSY}}$ access time for the metastable condition versus the non-metastable condition is shown below. This effectively plots the metastable settling time against the raw speed of the part, as indicated by the delay for the non-metastable case.

A linear estimate through these points allows $\overline{\text{BUSY}}$ access time with metastability to be calculated from the non-metastable time. This is given by:

$t_{BAA} = 1.33 * t_{BAANM} + 7\text{ns}$

Where: t_{BAANM} = $\overline{\text{BUSY}}$ access time without metastability

Alternatively, the maximum value of t_{BAANM} for a specified t_{BAA} is given by:

$t_{BAANM} = 0.75 * (t_{BAA} - 7)$

$= 0.75 * (45 - 7) = 28.5\text{ns}$

This means that the IDT7130 and IDT7132, 1K x 8 dual-port RAM devices, should have a $\overline{\text{BUSY}}$ access time of no more than 28.5ns in the non-metastable case to ensure a 45ns t_{BAA} spec for the metastable case.

$\overline{\text{BUSY}}$ ACCESS TIME TESTING ISSUES

Actual testing of the worst case t_{BAA} is difficult because the worst case value occurs at the metastable peak and is probabilistic in nature. The peak is probably much sharper than shown in the sketch and it occurs somewhere near, but not at, zero. Finding the peak value requires special equipment and a lot of test time. This type of special metastable testing has been performed on the IDT7130 and the data shown on the above graph is derived from these results.

The metastable access time is a calculated value based on probability. It is found by conducting many tests where the address delta is walked through the metastable region while recording the observed t_{BAA} times. This data is plotted on a semi-log probability graph and the graph is extrapolated to find the access time that must be allowed to reach a given level of probability that the $\overline{\text{BUSY}}$ output is valid. The access times shown on the metastable versus non-metastable graph are calculated to be large enough that they will be exceeded only once per 100 years at an arbitration rate of

10MHz. (Note: Reducing the time doesn't gain you much; reducing the time to once in 10 years only gains you .67ns in access time.)

$\overline{\text{BUSY}}$ ACCESS TIME TESTING METHODS

The following method can be used for testing t_{BAA}:

- Test the busy access time at 50+ns.
- Use the following table to relate the 50+ns value to the desired t_{BAA}:

t_{BAA} Spec	Test Limit, t_{BAANM}
60.0ns	39.75ns = .75*(t_{BAA} - 7)
50.0	32.25
45.0	28.50
40.0	24.75
35.0	21.00
20.0	17.25

- Check that correct assignment of $\overline{\text{BUSY}}$ occurs at t_{APS} (5.0ns) by testing with the left side earlier than the right, then later than the right by t_{APS}. Test for all address bit variations (wiggle each address bit).
- t_{BAC}, $\overline{\text{BUSY}}$ access from chip enable, is assumed to be 75% of t_{BAA} (we don't have any metastable data on t_{BAC}).
- t_{BAA} and t_{BAC} are, by nature, guaranteed but not (directly) tested.

14

CACHE-TAG RAM TIMING FOR THE 68020 USING THE IDT7174

Integrated Device Technology, Inc.

TECHNICAL NOTE TN-11

by David C. Wyland

A cache memory for the 68020 can be made using IDT7174 cache-tag RAMs in combination with cache-data RAMs such as the IDT7164. The access time requirements for the cache-tag and cache-data RAMs can be derived from the 68020 timing specifications.

The cache-tag RAMs must be fast because they must decide whether to use cache data or main memory data and this decision must be made at the beginning of the memory cycle. The critical path for the cache-tag RAMs is from the address outputs, through the cache-tag RAMs to their match outputs and through the DSACK drivers to the DSACK inputs to the 68020. This is shown in the 68020 Cache Interface drawing below.

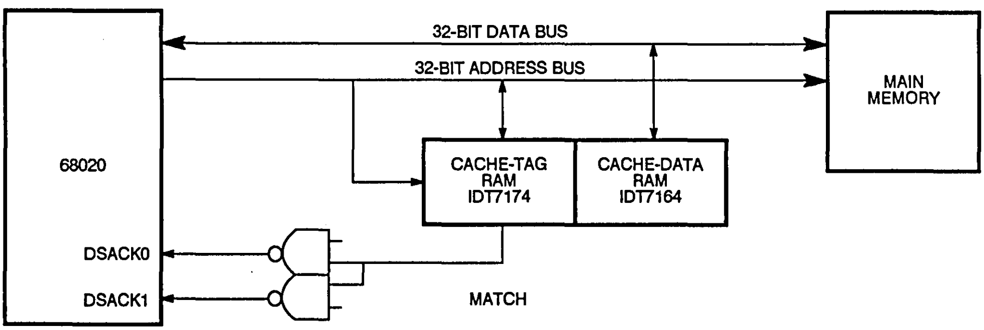


Figure 1. 68020 Cache Interface

The cache-tag and data RAM access time calculations and timing diagram are shown below for a 68020 running with a 20MHz clock.

Cache-Tag RAM Access Time Requirement			Cache-Data RAM Access Time Requirement		
Spec. No.	**Characteristic**	**Value @ 20 MHz (ns)**	**Spec. No.**	**Characteristic**	**Value @ 20 MHz (ns)**
-	3 Half-Clock Periods	75	-	5 Half-Clock Periods	125
6	Clock High to Address	-25	6	Clock High to Address	-25
-	DSACK Driver Delay	-5	27	$DATA_{IN}$ Valid to Clock Low	5
47A	DSACK Input Set-up Time	-5			
	Tag RAM Access Time	40		Data RAM Access Time	95

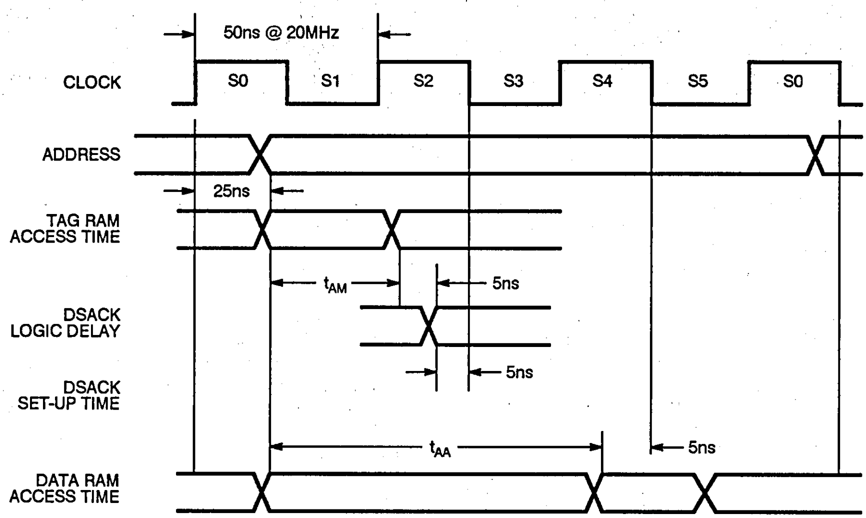


Figure 2. 68020 Cache Timing Diagram

Cache-tag and cache-data RAM access time requirements for various 68020 clock rates are shown in the table below. Note that a 5ns delay for the DSACK drive gates is assumed.

Speed (MHz)	Clock Period (ns)	Tag Access Time (ns)	Data Access Time (ns)
25	40	25	70
20	50	40	95
16	62.5	53	121
12.5	80	65	150

Figure 3. 68020 Cache Memory Access Time Requirements vs Clock Rate

Integrated Device Technology, Inc.

USING IDT'S VIDEO DACs IN 5V ONLY SYSTEMS

TECHNICAL NOTE TN-12

by John Hull

The IDT75C18 and IDT75C19 Video DACs were designed with ECL-compatible inputs because of the high data rates required for 1280 x 1024 pixel resolution CRT displays (110MHz). Normally, one would use a single -5.2V power supply (standard ECL) to power the DAC. There are a few reasons why this standard configuration would not be used, such as elimination of the minus supply and TTL compatibility.

POWER SUPPLY CONSIDERATIONS

The circuitry of the IDT75C18 and IDT75C19 have been partitioned on the chip into analog and digital functions to optimize the noise performance of the DAC. Both devices have analog and digital ground inputs, as well as analog and digital power connections.

Since the IDT75C18 and IDT75C19 have been designed for ECL systems, their A_{GND} and D_{GND} inputs are normally connected to 0V and their power supply pins, V_{EEA} and V_{EED}, connect to -5.2V.

As long as the correct polarity of the power supply inputs is maintained, the IDT75C18 and IDT75C19 can operate from a +5.0V as well as a -5.2V supply. The DAC is not affected by the polarity of its power supply. In the same manner, the ECL gates driving the DAC may be operated with a +5.0V power supply with no degradation of performance. This arrangement still provides a direct interface to the DAC; no level shifting is required. The advantage is that the minus power supply is eliminated. Care must be taken, however, that the +5.0V supply is high quality and correctly bypassed. Any noise on the +5.0V supply will couple directly into the ECL outputs, reducing input margins.

The following table summarizes the power and ground connections for the IDT75C18 and IDT75C19 for both positive and negative supplies.

Device Pin	Positive Supply	Negative Supply
A_{GND}	+5.0V	0V
D_{GND}	+5.0V	0V
V_{EEA}	0V	-5.2V
V_{EED}	0V	-5.2V

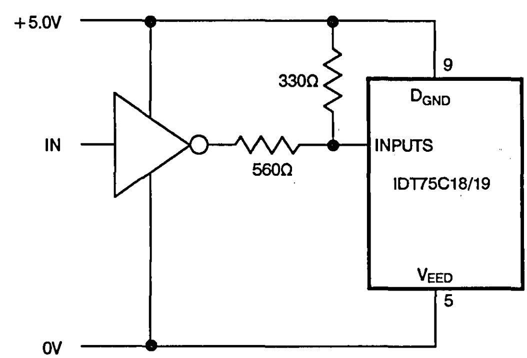
INPUT CONSIDERATIONS

Because the IDT75C18 and IDT75C19 were designed for ECL systems, all inputs were optimized for ECL logic levels. The important specification, however, is the threshold points, or at what voltage is a logic "1" and "0" guaranteed (V_{IH} & V_{IL}).

The V_{IH} specification may be restated as the minimum voltage which guarantees a logic "1" and V_{IL} as the maximum voltage guaranteeing a logic "0". In the minus supply case, any input voltage between 0V and -1.045V is a logic "1", while an input voltage between -1.49V and -5.2V (V_{EED}) is a logic "0". These voltages are referenced to 0V, D_{GND}. For the positive supply case, the input voltages are again referenced to 0V, but this time the pin is V_{EED}. To calculate the correct input voltage levels, simply subtract the specified V_{IH} and V_{IL} from the positive power supply (5.0V). The results are summarized in the following table.

Digital Input	Negative Supply	Positive Supply
Logic "1"	0V to -1.045V	+3.955V to 5.0V
Logic "0"	-1.49V to -5.2V	+3.51V to 0V

It is possible to directly drive the DAC inputs using IDT's FCT logic family. The guaranteed minimum output "high" level is 4.3V, easily exceeding the needed 3.955V. It is also possible to drive the DAC inputs using a normal TTL gate and an external resistor level shifter, as shown below. This circuit ensures proper input levels for the DAC if the TTL gate has a minimum V_{OH} of 2.4V and a maximum V_{OL} of 0.4V.



ANALOG OUTPUT CONSIDERATIONS

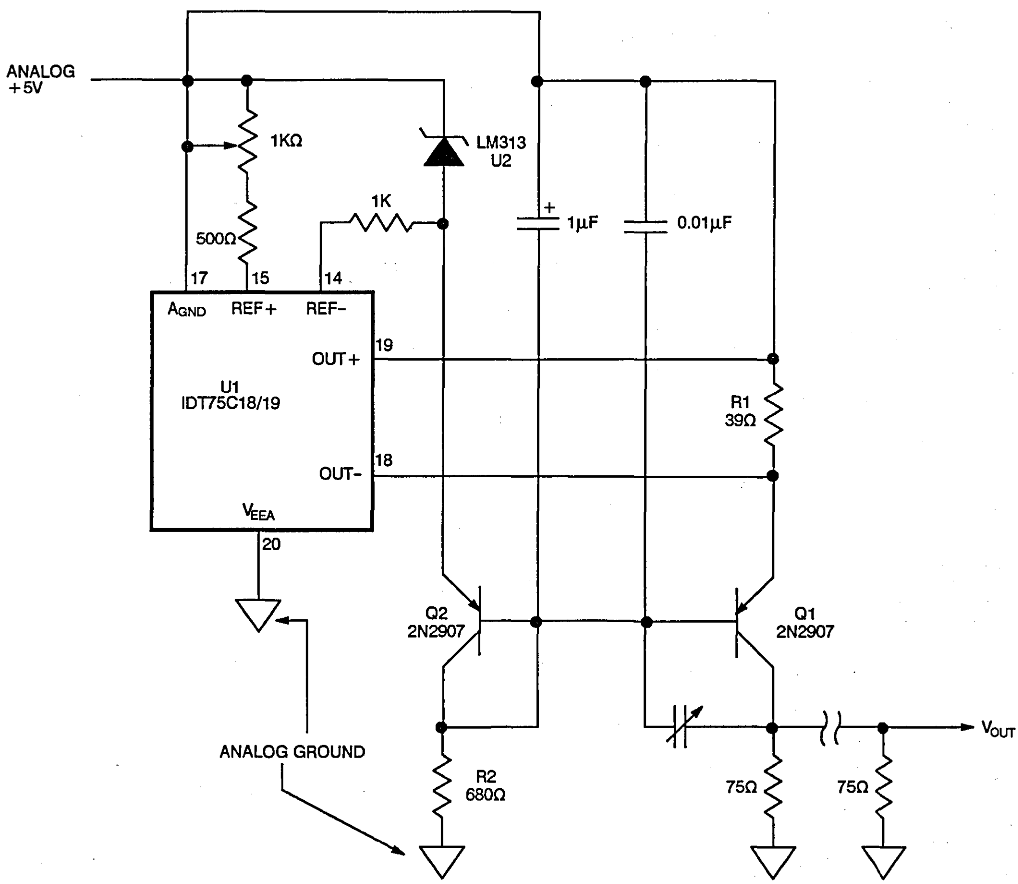
The output structure of the IDT75C18 and IDT75C19 is a high-impedance current sink which is capable of driving a doubly terminated 75Ω load to standard video levels. To convert the DAC output current into a voltage, a load resistor is connected between the output pin and the most positive supply. In the negative supply case, the output voltage swings between 0V and -1V, while in the positive supply case, the output swings between +5V and +4V. In many video applications, the output DC level is unimportant because the monitor is AC coupled. In other applications, this may be undesirable because of noise on the +5V supply.

The circuit below can be used to reference the output voltage to the most negative supply and provide some isolation from the +5V supply. PNP transistors Q1 and Q2 are biased to provide a nearly constant voltage on their bases. The current through Q1 is then essentially the DAC output current flowing into the OUT-pin. Q1 functions as a current source and the output voltage across the load resistors is now referenced to the most negative supply (in this case, 0V).

Printed in the U.S.A. 7/87

Resistor R2 and a reference voltage provided by U2, a band-gap diode, set the quiescent V_{BE} for Q1. Transistor Q2, connected as a diode, provides temperature compensation for the base-emitter voltage of Q1. Since a maximum of 30mA can flow through Q1, a monolithic dual is not recommended. Q1 and Q2 should, however, be placed in close thermal contact. The current through Q1 is, then, $(V+/39\Omega) - I_{VDAC}$. The output voltage corresponding to 10% White is 1.07V and to Sync is 0V.

A few practical points to note: The bases of Q1 and Q2 are biased with respect to +5V and, therefore, the bypass capacitors on the bases are connected to +5V and not to ground. The outputs of the DAC should share a current path to the most positive supply that is independent of the reference circuitry. The output current is proportional to the reference current and a feedback path into the DAC should be avoided. A small variable capacitor may be added between the base and collector of Q1 to optimize the output pulse response.



14

CACHE-TAG RAM TIMING FOR THE 80386 USING THE IDT7174

Integrated Device Technology, Inc.

TECHNICAL NOTE TN-13

by David C. Wyland

A cache memory for the 80386 can be made using IDT7174 cache-tag RAMs in combination with cache-data RAMs such as the IDT7164. The access time requirements for the cache-tag and cache-data RAMs can be derived from the 80386 timing specifications.

The cache-tag RAMs must be fast because they must decide whether to use cache data or main memory data and this decision must be made at the beginning of the memory cycle. The critical path for the cache-tag RAMs is from the address outputs, through the cache-tag RAMs to their match outputs and through the READY driver to the READY input to the 80386. This is shown in the 80386 Cache Interface drawing below.

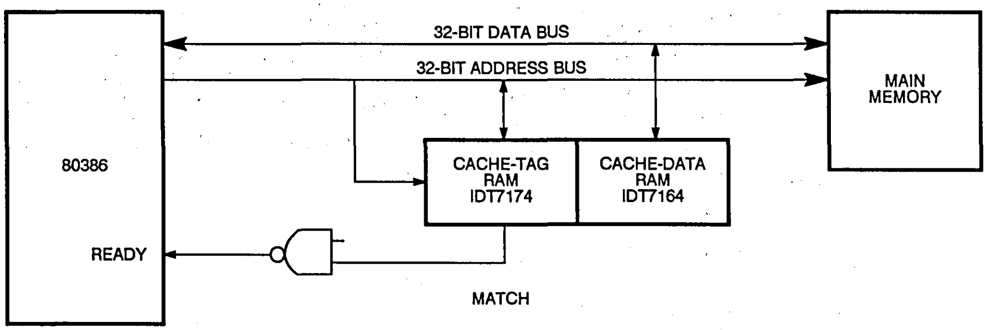


Figure 1. 80386 Cache Interface

The cache-tag and data RAM access time calculations and timing diagram are shown below for a 80386 running with a 16MHz clock.

Cache-Tag RAM Access Time Requirement			Cache-Data RAM Access Time Requirement		
Spec. No.	**Characteristic**	**Value @ 16 MHz (ns)**	**Spec. No.**	**Characteristic**	**Value @ 16 MHz (ns)**
–	2 Clock Periods	125	–	2 Clock Periods	125
T6	Clock High to Address	-40	T6	Clock High to Address	-40
–	READY Driver Delay	-5	T21	$DATA_{IN}$ Valid to Clock Low	-10
T19	READY Input Set-up Time	-20			
	Tag RAM Access Time	60		Data RAM Access Time	75

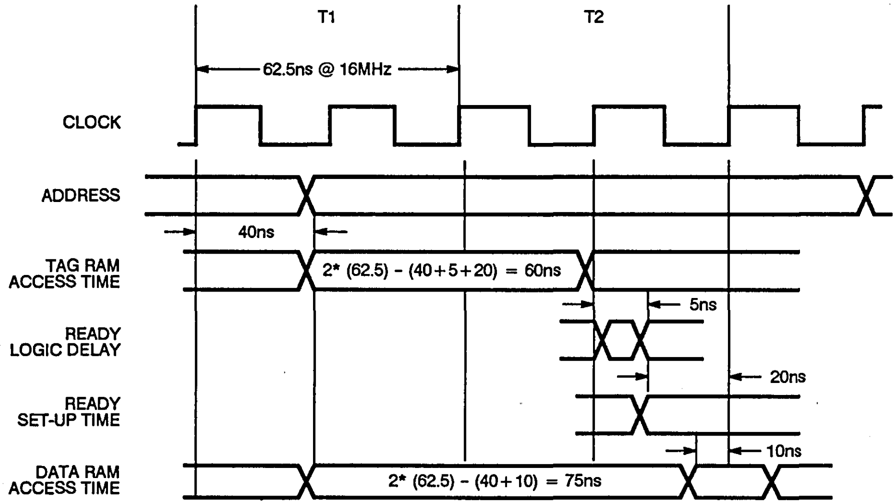


Figure 2. 80386 Cache Timing Diagram

Cache-tag and cache-data RAM access time requirements for various 80386 clock rates are shown in the table below. Note that a 5ns delay for the READY drive gate is assumed.

80386 Speed (MHz)	Clock Period (ns)	Tag Access Time (ns)	Data Access Time (ns)
20	50.0	52	58
16	62.5	60	75
12	83.3	95	110

Figure 3. 80386 Cache Memory Access Time Requirements vs Clock Rate

14

15

THERMAL PERFORMANCE CALCULATIONS FOR IDT'S PACKAGES

Since most of the electrical energy consumed by microelectronic devices eventually appears as heat, poor thermal performance of the device or lack of management of this thermal energy can cause a variety of deleterious effects. This device temperature increase can exhibit itself as one of the key variables in establishing device performance and long term reliability; on the other hand, effective dissipation of internally generated thermal energy can, if properly managed, reduce the deleterious effects and improve component reliability.

A few key benefits of IDT's enhanced CEMOS™ process are: low power dissipation, high speed, increased levels of integration, wider operating temperature ranges and lower quiescent power dissipation. Because the reliability of an integrated circuit is largely dependent on the maximum temperature the device attains during operation, and as the junction stability declines with increases in junction temperature (T_J), it becomes increasingly important to maintain a low (T_J).

CMOS devices stabilize more quickly and at greatly lower temperature than bipolar devices under normal operation. The accelerated aging of an integrated circuit can be expressed as an exponential function of the junction temperature as:

$$t_A = t_O \exp\left[\frac{Ea}{k}\left(\frac{1}{T_O} - \frac{1}{T_J}\right)\right]$$

where

t_A	=	lifetime at elevated junction (T_J) temperature
t_O	=	normal lifetime at normal junction (T_O) temperature
Ea	=	activation energy (ev)
k	=	Boltzmann's constant (8.617×10^{-5} ev/k)

i.e. the lifetime of a device could be decreased by a factor of 2 for every 10°C increase temperature.

To minimize the deleterious effects associated with this potential increase, IDT has:

1. Optimized our proprietary low-power CEMOS fabrication process to ensure the active junction temperature rise is minimal.
2. Selected only packaging materials that optimize heat dissipation, which encourages a cooler running device.
3. Physically designed all package components to enhance the inherent material properties and to take full advantage of heat transfer and radiation due to case geometries.
4. Tightly controlled the assembly procedures to meet or exceed the stringent criteria of MIL-STD-883C to ensure maximum heat transfer between die and packaging materials.

The following figures graphically illustrate the thermal values of IDT's current package families. Each envelope (shaded area) depicts a typical spread of values due to the influence of a number of factors which include: circuit size, package cavity size and die attach integrity. The following range of values are to be used as a comprehensive characterization of the major variables rather than single point of reference.

When calculating junction temperature (T_J), it is necessary to know the thermal resistance of the package (θ_{JA}) as measured in "degrees celsius per watt". With the accompanying data, the following equation can be used to establish thermal performance, enhance device reliability and ultimately provide you, the user, with a continuing series of high-speed, low-power CMOS solutions to your system design needs.

$$\theta_{JA} = [T_J - T_A]/P$$

$$T_J = T_A + P\,[\theta_{JA}] = T_A + P[\theta_{JA} + \theta_{CA}]$$

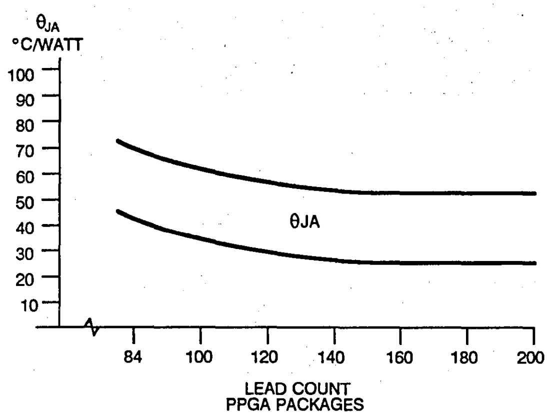
where

$$\theta_{JC} = \frac{T_J - T_C}{P} \qquad \theta_{CA} = \frac{T_C - T_A}{P}$$

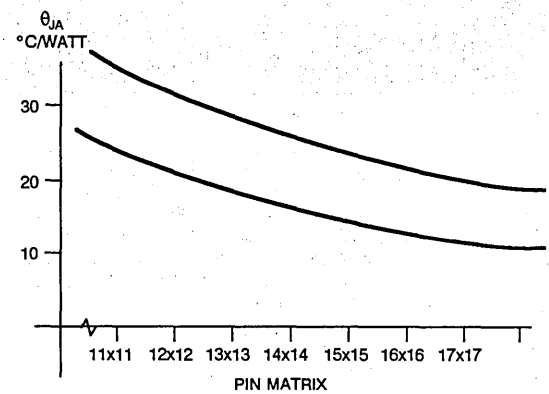
θ	=	Thermal resistance, junction to reference point
J	=	Junction
P	=	Operational power of device (dissipated)
T_A	=	Ambient temperature in degrees celsius (normally +70°C)
T_J	=	Junction temperature of integrated device
T_C	=	Temperature of case/package
θ_{CA}	=	**Case to Ambient,** thermal resistance—usually a measure of the heat dissipation due to natural or forced convection, radiation and mounting techniques.
θ_{JC}	=	**Junction to Case,** thermal resistance—usually measured with reference to the temperature at a specific point on the package (case) surface. (Dependent on package material properties and package geometry.)
θ_{JA}	=	**Junction to Ambient,** thermal resistance—usually measured with respect to the temperature of a specified volume of Still Air. (Dependent on $\theta_{JC} + \theta_{JA}$ which includes the influence of area and environmental condition.)

15

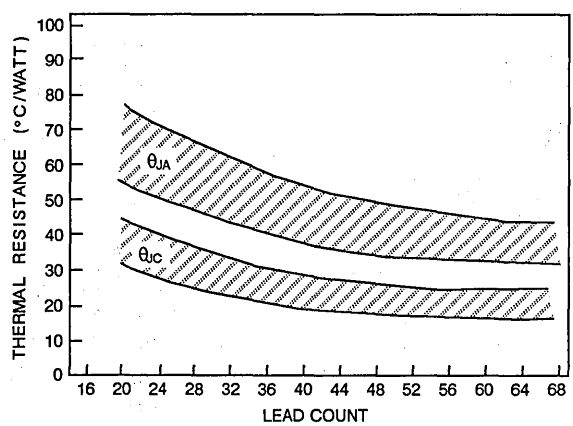
Ref. MIL-STD-883C, Method 1012.1
JEDEC ENG. Bulletin No. 20, January 1975
1986 Semi. Std., Vol. 4, Test Methods G30-86, G32-86.



PGA Thermal Resistance



Package Laminate Material: Hi Temp. Epoxy or Triazine (BT)



Thermal Resistance of Ceramic Leadless Chip Carrier (LCC) Packages

Integrated Device Technology, Inc.

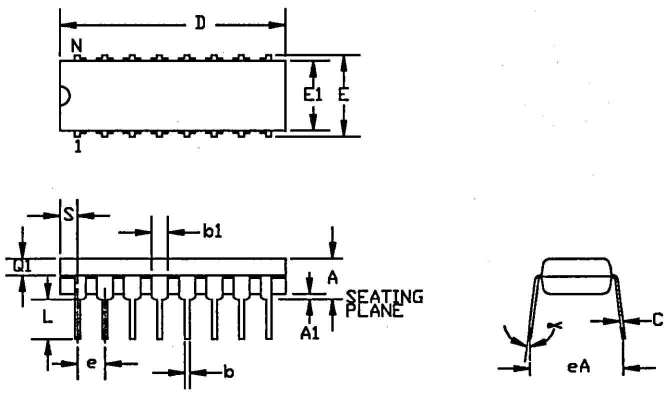
PACKAGE DIAGRAM OUTLINE INDEXES

Integrated Device Technology, Inc.

PACKAGE DIAGRAM OUTLINES

PLASTIC DUAL IN-LINE PACKAGES

16–24 PIN PLASTIC DIP (300 MIL)



NOTES:

[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.

[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

[3] D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG # / # OF PINS (N)	P16–1 16 (300 MIL)		P18–1 18 (300 MIL)		P20–1 20 (300 MIL)		P22–1 22 (300 MIL)		P24–1 24 (300 MIL)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.120	0.200	0.130	0.180	0.145	0.200	0.145	0.200	0.145	0.200
A1	0.015	0.070	0.015	0.060	0.015	0.060	0.015	0.060	0.015	0.060
b	0.015	0.020	0.015	0.020	0.015	0.020	0.015	0.020	0.015	0.020
b1	0.045	0.070	0.045	0.070	0.045	0.065	0.045	0.065	0.045	0.065
C	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
D	0.745	0.785	0.885	0.915	1.020	1.060	1.020	1.060	1.220	1.260
E	0.300	0.325	0.300	0.325	0.300	0.320	0.300	0.320	0.300	0.320
E1	0.245	0.270	0.245	0.270	0.240	0.280	0.240	0.270	0.240	0.280
e	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
eA	0.310	0.370	0.310	0.370	0.310	0.370	0.310	0.370	0.310	0.370
L	0.120	0.150	0.120	0.170	0.120	0.160	0.120	0.160	0.120	0.180
∝	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
S	0.015	0.060	0.030	0.070	0.025	0.070	0.005	0.030	0.045	0.075
Q1	0.050	0.080	0.050	0.080	0.055	0.075	0.055	0.075	0.055	0.075
N	16		18		20		22		24	

15

PLASTIC DUAL IN-LINE PACKAGES (Continued)

24–48 PIN PLASTIC DIP (600 MIL)

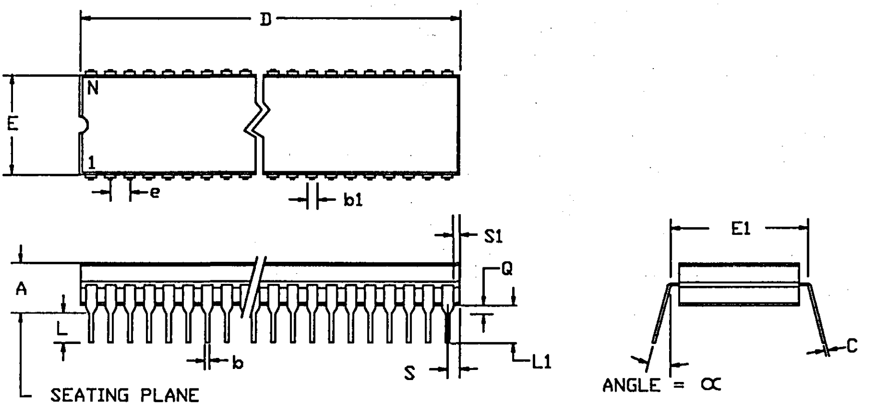
DWG # / # OF PINS (N)	P24–2 24 (600 MIL)		P28–1 28 (600 MIL)		P40–1 40 (600 MIL)		P48–1 48 (600 MIL)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.145	0.200	0.150	0.200	0.160	0.220	0.170	0.220
A1	0.015	0.060	0.015	0.060	0.015	0.070	0.015	0.060
b	0.015	0.020	0.015	0.020	0.015	0.020	0.015	0.020
b1	0.045	0.065	0.045	0.065	0.045	0.065	0.045	0.065
C	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
D	1.220	1.260	1.400	1.460	2.020	2.070	2.400	2.450
E	0.600	0.620	0.600	0.620	0.600	0.620	0.600	0.620
E1	0.530	0.560	0.500	0.550	0.500	.560	0.500	0.570
e	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
eA	0.610	0.670	0.610	0.670	0.610	0.700	0.610	0.700
L	0.120	0.180	0.120	0.180	0.100	0.160	0.120	0.180
α	0°	15°	0°	15°	0°	15°	0°	15°
S	0.045	0.080	0.025	0.080	0.065	0.085	0.050	0.075
Q1	0.060	0.080	0.060	0.080	0.060	0.080	0.060	0.080
N	24		28		40		48	

64 PIN PLASTIC DIP (900 MIL)

DWG # / # OF PINS (N)	P64–1 64 (900 MIL)	
	MIN	MAX
A	0.180	0.230
A1	0.015	0.060
b	0.015	0.020
b1	0.045	0.065
C	0.008	0.012
D	3.190	3.240
E	0.900	0.925
E1	0.800	0.870
e	0.090	0.110
eA	0.910	1.000
L	0.100	0.180
α	0°	15°
S	0.040	0.070
Q1	0.080	0.090
N	64	

DUAL IN-LINES PACKAGES

16–24 PIN CERDIP (300 MIL)



NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC - BASIC PIN SPACING BETWEEN CENTERS.

DWG # / # OF LEADS (N)	D16–1 16 (300 MIL)		D18–1 18 (300 MIL)		D20–1 20 (300 MIL)		D24–1 24 (300 MIL)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.090	.200	.140	.200	.140	.200
b	.016	.020	.014	.023	.014	.023	.014	.023
b1	.045	.070	.038	.065	.038	.065	.038	.065
C	.009	.013	.009	.014	.009	.014	.009	.014
D	.750	.830	.880	.940	.935	1.060	1.240	1.280
E	.240	.310	.220	.310	.220	.310	.220	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150		.150		.150		.150	
Q	.015	.060	.015	.060	.015	.060	.015	.060
S	.020	.080	.020	.080	.020	.080	.030	.080
S1	.005		.005		.005		.005	
ANGLE (DEG)	0°	15°	0°	15°	0°	15°	0°	15°

15

DUAL IN-LINE PACKAGES (Continued)

24–40 PIN CERDIP (600 MIL)

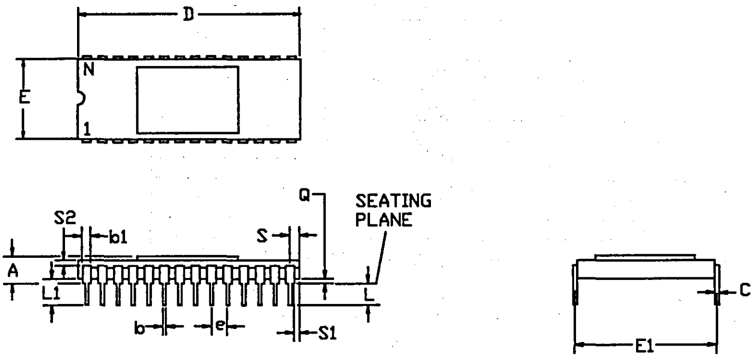
DWG # / # OF LEADS (N)	D24-2 24 (600 MIL)		D28-1 28 (600 MIL)		D40-1 40 (600 MIL)	
	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.090	.200	.160	.220
b	.014	.023	.015	.020	.015	.020
b1	.038	.065	.045	.060	.045	.060
C	.008	.015	.008	.013	.008	.012
D	1.230	1.290	1.440	1.490	2.020	2.070
E	.500	.560	.510	.545	.510	.545
E1	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.100	.180	.125	.200
L1	.150		.150		.150	
Q	.015	.060	.020	.065	.020	.060
S	.030	.080	.030	.080	.030	.080
S1	.005		.005		.005	
∝	0°	15°	0°	15°	0°	15°

28–40 PIN CERDIP (WIDE BODY)

DWG # / # OF LEADS (N)	D28-2 28 (WIDE BODY)		D32-1 32 (WIDE BODY)		D40-2 40 (WIDE BODY)	
	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.120	.210	.160	.220
b	.015	.020	.015	.020	.015	.020
b1	.045	.060	.038	.065	.045	.060
C	.008	.013	.008	.015	.008	.012
D	1.440	1.490	1.625	1.675	2.020	2.070
E	.570	.600	.570	.600	.570	.600
E1	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC	
L	.100	.180	.125	.200	.125	.200
L1	.150		.150		.150	
Q	.020	.065	.020	.060	.020	.060
S	.030	.080	.030	.080	.030	.080
S1	.005		.005		.005	
∝	0°	15°	0°	15°	0°	15°

DUAL IN-LINE PACKAGES (Continued)

20–28 PIN SIDEBRAZE (300 MIL)



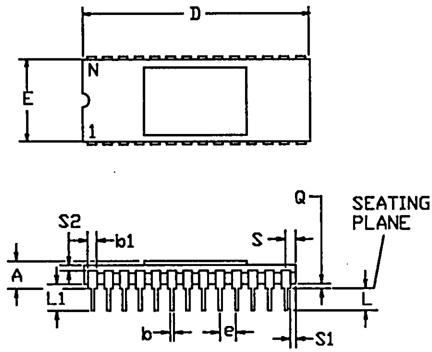
NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

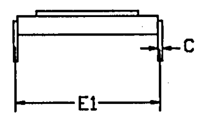
DWG # / # OF LEADS (N)	C20-1 20 (300 MIL)		C22-1 22 (300 MIL)		C24-1 24 (300 MIL)		C28-1 28 (300 MIL)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.100	.200	.090	.200	.090	.200
b	.014	.023	.014	.023	.014	.023	.014	.023
b1	.030	.060	.030	.060	.030	.060	.030	.060
C	.008	.015	.008	.015	.008	.015	.008	.015
D	.970	1.060	1.040	1.120	1.180	1.230	1.380	1.420
E	.220	.310	.260	.310	.220	.310	.220	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200	.125	.200
L1	.150		.150		.150		.150	
Q	.015	.060	.015	.060	.015	.060	.015	.060
S	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005		.005		.005		.005	
S2	.005		.005		.005		.005	

15

DUAL IN–LINE PACKAGES (Continued)

28–48 PIN SIDEBRAZE (400 MIL)



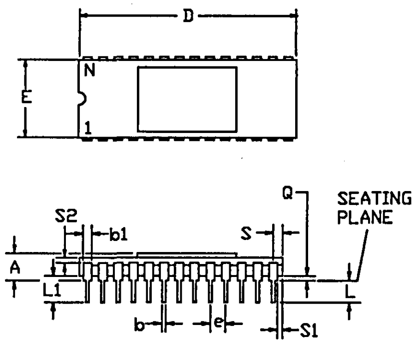


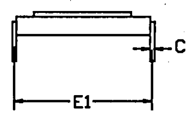
NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

DWG # # OF LEADS (N)	C28-2 28 (400 MIL)		C48-1 48 (400 MIL)	
	MIN	MAX	MIN	MAX
A	.090	.200	.085	.190
b	.014	.023	.014	.023
b1	.030	.060	.030	.060
C	.008	.014	.008	.014
D	1.380	1.420	1.690	1.730
E	.380	.420	.380	.410
E1	.390	.420	.390	.420
e	.100 BSC		.070 BSC	
L	.100	.175	.125	.175
L1	.150		.150	
Q	.030	.060	.020	.070
S	.030	.065	.030	.065
S1	.005		.005	
S2	.005		.005	

DUAL IN–LINE PACKAGES (Continued)

24–68 PIN SIDEBRAZE (600 MIL)



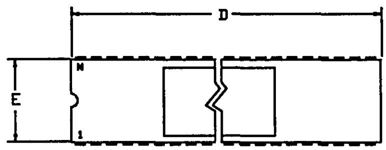


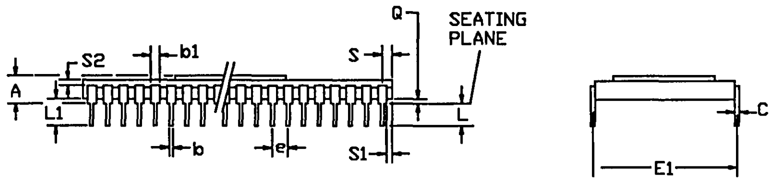
NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

DWG # / # OF LEADS (N)	C24–2 24 (600 MIL)		C28–3 28 (600 MIL)		C40–1 40 (600 MIL)		C48–2 48 (600 MIL)		C68–1 68 (600 MIL)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.190	.085	.190	.085	.190	.100	.190	.085	.190
b	.015	.023	.015	.022	.015	.023	.015	.023	.015	.023
b1	.040	.060	.038	.060	.038	.060	.040	.060	.030	.060
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	1.180	1.230	1.380	1.430	1.980	2.030	2.370	2.430	2.380	2.440
E	.575	.610	.580	.610	.580	.610	.550	.610	.580	.610
E1	.590	.620	.590	.620	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100	BSC	.100 BSC		.070 BSC	
L	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150		.150		.150		.150		.150	
Q	.020	.060	.020	.065	.020	.060	.020	.060	.020	.070
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005		.005		.005		.005		.005	
S2	.010		.010		.010		.005		.005	

DUAL IN–LINE PACKAGES (Continued)

64 PIN SIDEBRAZE (900 MIL)



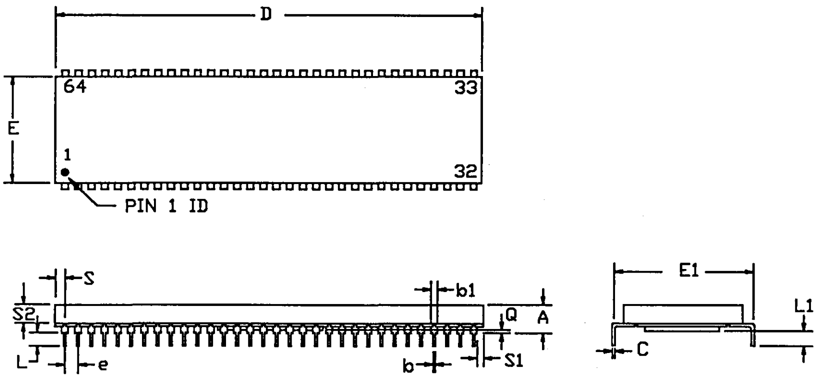


NOTES
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

DWG # / # OF LEADS (N)	C64-1 64 (900 MIL)	
	MIN	MAX
A	.110	.190
b	.014	.023
b1	.030	.060
C	.008	.015
D	3.160	3.240
E	.884	.915
E1	.890	.920
e	.100 BSC	
L	.125	.200
L1	.150	
Q	.015	.070
S	.030	.065
S1	.005	
S2	.005	

DUAL IN-LINE PACKAGES (Continued)

64 PIN TOPBRAZE (900 MIL)



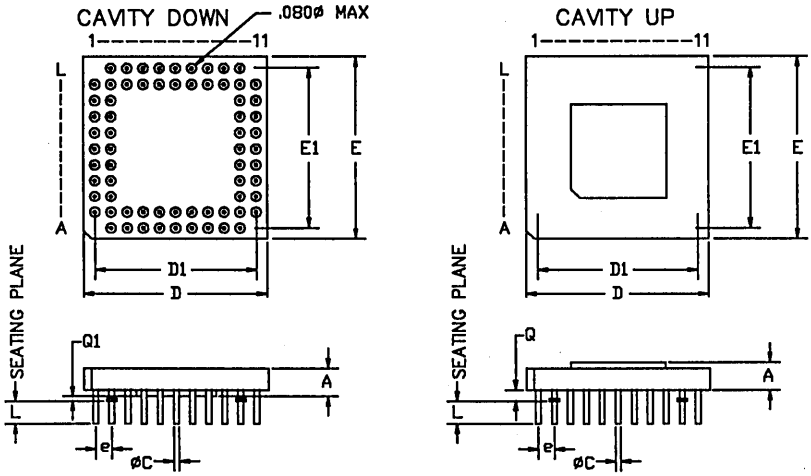
NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC - BASIC PIN SPACING BETWEEN CENTERS.

DWG # # OF LEADS (N)	C64-2 64 (900 MIL)	
	MIN	MAX
A	.120	.180
b	.015	.021
b1	.040	.060
C	.009	.012
D	3.165	3.235
E	.785	.815
E1	.885	.915
e	.100 BSC	
L	.125	.160
L1	.150	
Q	.020	.100
S	.030	.065
S1	.005	
S2	.005	

15

PLASTIC PIN GRID ARRAY

68 PIN PGA



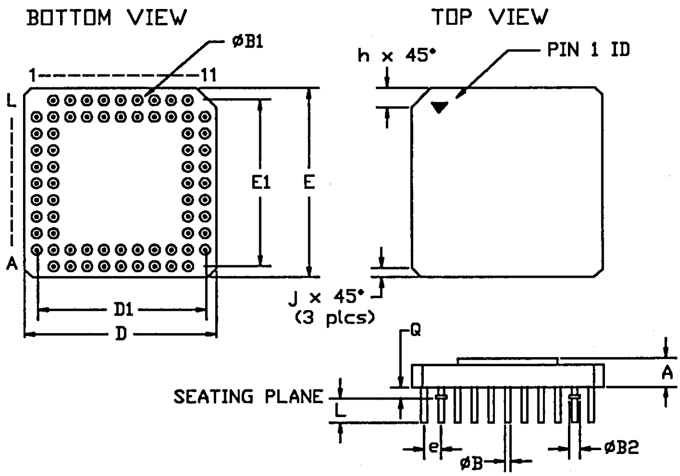
NOTES: UNLESS OTHERWISE SPECIFIED

1. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
2. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
3. DIM "A" INCLUDES BOTH THE PKG BODY & THE LID. IT DOES NOT INCLUDE HEATSINK OR OTHER ATTACHED FEATURES.
4. DIM "Q" APPLIES TO CAVITY UP CONFIGURATION AND "Q1" APPLIES TO CAVITY DOWN CONFIGURATION.
5. PIN DIAMETER "C" EXCLUDES SOLDER DIP OR OTHER LEAD FINISH.
6. PIN TIPS MAY HAVE RADIUS OR CHAMFER.

DWG No.	PG 68-1	
No. OF PIN	68 PIN	
SYMBOLS	MIN	MAX
A	.055	.145
C	.016	.020
D	1.140	1.180
D1	1.000 BSC	
E	1.140	1.180
E1	1.000 BSC	
e	.100	BSC
L	.100	.200
M	11	
N	68	
Q	.040	.070
Q1	.025	.070

PIN GRID ARRAY

68–108 PIN PGA (CAVITY UP)



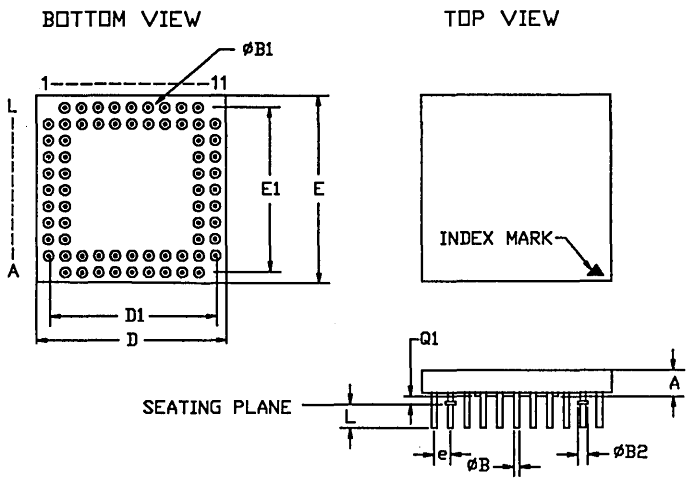
NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC - BASIC PIN SPACING BETWEEN CENTERS.

DWG # NO. OF LEADS	G68-1 68-LEADS		G84-1 84-LEADS		G108-1 108-LEADS	
	MIN	MAX	MIN	MAX	MIN	MAX
A	.070	.145	.070	.145	.070	.145
øB	.016	.020	.016	.020	.016	.020
øB1		.080	.060	.080		.080
øB2	.040	.060	.040	.060	.040	.060
D	1.140	1.180	1.180	1.235	1.188	1.212
D1	1.000 BSC		1.100 BSC		1.100 BSC	
E	1.140	1.180	1.180	1.235	1.188	1.212
E1	1.000 BSC		1.100 BSC		1.100 BSC	
e	.100 BSC		.100 BSC		.100 BSC	
h	.065	.085				
J	.015	.025				
L	.125	.200	.125	.200	.125	.200
N	68		84		108	
Q	.040	.060	.040	.060	.040	.060

15

PIN GRID ARRAY (Continued)

68–144 PIN PGA (CAVITY DOWN)

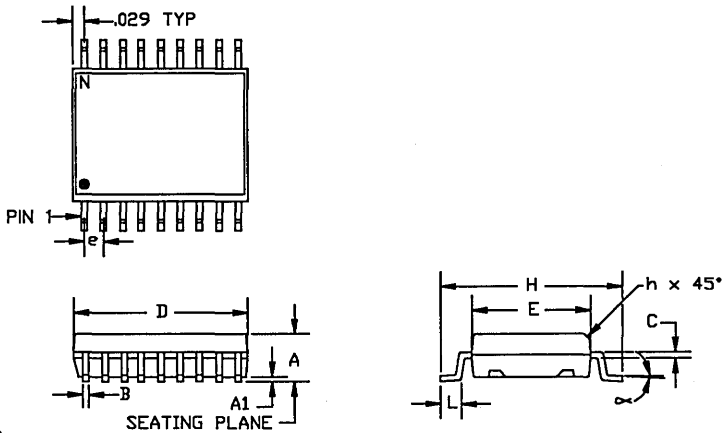


NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC - BASIC PIN SPACING BETWEEN CENTERS.

DWG # / NO. OF LEADS	G68-2 68-LEADS		G84-2 84-LEADS		G144-1 144-LEADS	
	MIN	MAX	MIN	MAX	MIN	MAX
A	.077	.095	.077	.095	.082	.100
ØB	.016	.020	.016	.020	.016	.022
ØB1	.060	.080	.060	.080	.060	.080
ØB2	.040	.060	.040	.060	.040	.060
D	1.098	1.122	1.180	1.235	1.559	1.590
D1	1.000 BSC		1.100 BSC		1.400 BSC	
E	1.098	1.122	1.180	1.235	1.559	1.590
E1	1.000 BSC		1.100 BSC		1.400 BSC	
e	.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200
N	68		84		144	
Q1	.025	.060	.025	.060	.025	.060

SMALL OUTLINE IC

16–28 PIN SMALL OUTLINE (GULL WING)



NOTES:

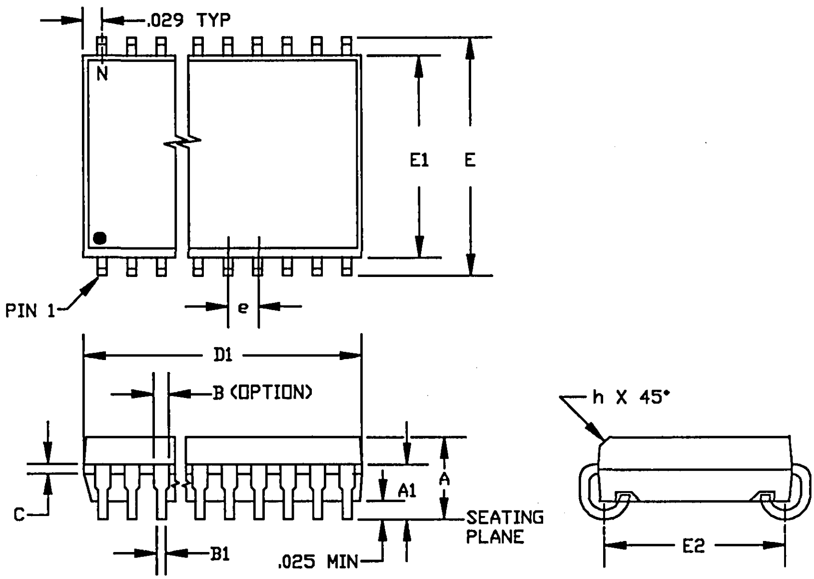
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC - BASIC PIN SPACING BETWEEN CENTERS.
[3] D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
[4] FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

DWG #	SO16-1		SO18-1		SO20-2		SO24-2		SO24-3		SO28-2		SO28-3	
NO. OF LD	16 LD		18 LD		20 LD		24 LD		24 LD		28 (.300")		28 (.330")	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.093	.1043	.093	.1043	.093	.1043	.093	.1043	.110	.120	.093	.1043	.108	.120
A1	.004	.0118	.004	.0118	.004	.0118	.004	.0118	.005	.0115	.004	.0118	.005	.014
B	.014	.020	.014	.020	.014	.020	.014	.020	.014	.018	.014	.020	.014	.019
C	.0091	.0125	.0091	.0125	.0091	.0125	.0091	.0125	.0091	.0125	.0091	.0125	.006	.010
D	.403	.413	.447	.462	.497	.511	.600	.614	.620	.630	.700	.712	.718	.728
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
E	.292	.2992	.292	.2992	.292	.2992	.292	.2992	.292	.2992	.292	.2992	.340	.350
h	.010	.029	.010	.029	.010	.029	.010	.029	.010	.029	.010	.029	.012	.025
H	.394	.419	.394	.419	.394	.419	.394	.419	.394	.419	.394	.419	.458	.478
L	.016	.050	.016	.050	.016	.050	.016	.050	.016	.050	.016	.050	.025	.045
∝	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°

15

SMALL OUTLINE IC (Continued)

24 PIN SMALL OUTLINE (J-BEND)

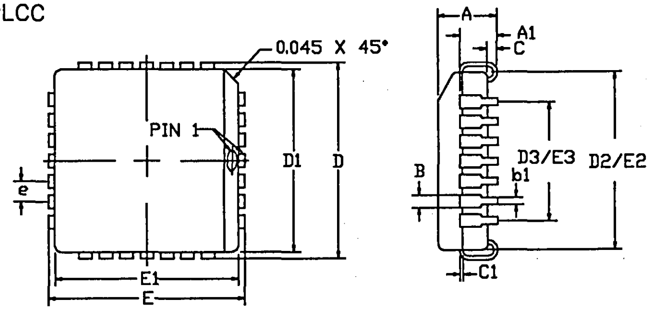


NOTES:
1. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
3. D1 & E1 INCLUDE MOLD MISMATCH & ARE DETERMINED AT THE PARTING LINE.

DWG #	Y24-1	
No. OF LD	24 LD (.300")	
SYMBOLS	MIN	MAX
A	.128	.148
A1	.082	.095
B	.026	.032
B1	.015	.020
C	.007	.011
D1	.620	.630
E	.335	.345
E1	.295	.305
E2	.260	.280
e	.050 BSC	
h	.010	.025

PLASTIC LEADED CHIP CARRIERS

20–84 PIN PLCC



NOTES:

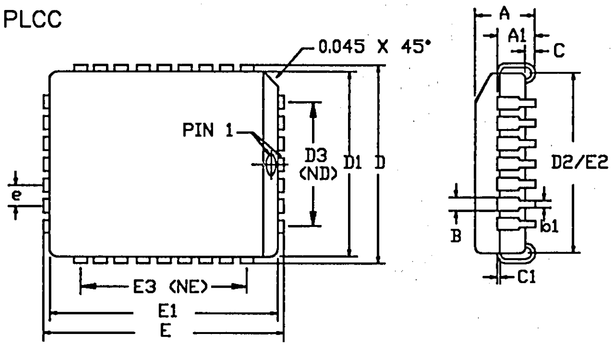
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC - BASIC PIN SPACING BETWEEN CENTERS.
[3] D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
[4] FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
[5] ND & NE = # LEADS IN D & E DIRECTIONS

DWG #	J20-1		J28-1		J44-1		J52-1		J68-1		J84-1	
NO. OF LD	20		28		44		52		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180
A1	.090	.120	.090	.120	.090	.120	.090	.120	.090	.120	.090	.120
B	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032
b1	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021
C	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040
C1	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
D1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
D2/E2	.290	.330	.390	.430	.590	.630	.690	.730	.890	.930	1.090	1.130
D3/E3	.200 REF		.300 REF		.500 REF		.600 REF		.800 REF		1.000 REF	
E	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
E1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
ND/NE	5		7		11		13		17		21	

15

PLASTIC LEADED CHIP CARRIER (Continued)

32 PIN PLCC



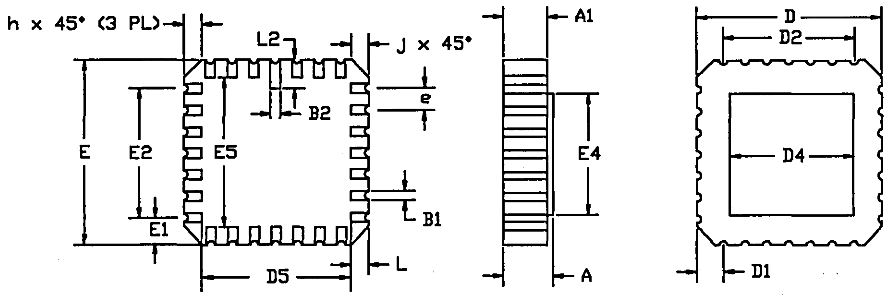
NOTES:

[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC - BASIC PIN SPACING BETWEEN CENTERS.
[3] D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
[4] FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
[5] ND & NE = # LEADS IN D & E DIRECTIONS RESPECTIVELY.

DWG #	J32-1	
NO. OF LEAD	32 LD	
SYMBOL	MIN	MAX
A	.120	.140
A1	.075	.095
B	.026	.032
b1	.013	.021
C	.015	.040
C1	.008	.012
D	.485	.495
D1	.449	.453
D2	.390	.430
D3	.150 REF	
E	.585	.595
E1	.549	.553
E2	.490	.530
E3	.400 REF	
e	.050 BSC	
ND/NE	7 / 9	

LEADLESS CHIP CARRIERS

20–44 PIN LCC (SQUARE)



NOTES:

[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.

[2] BSC - BASIC PIN SPACING BETWEEN CENTERS.

[3] ND=NE - NUMBER OF LEADS PER SIDE.

DWG # # OF PINS (N)	L20–2 20		L28–1 28		L44–1 44	
	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.100	.064	.100	.064	.120
A1	.054	.066	.054	.077	.054	.088
B1	.022	.028	.022	.028	.022	.028
B2	.022	.041	.022	.041	.022	.041
D	.342	.358	.442	.458	.640	.660
D1	.075 REF		.075 REF		.075 REF	
D2	.200 BSC		.300 BSC		.500 BSC	
D4		.358		.458		.560
D5	.250 REF		.350 REF		.550 REF	
E	.342	.358	.442	.458	.640	.660
E1	.075 REF		.075 REF		.075 REF	
E2	.200 BSC		.300 BSC		.500 BSC	
E4		.358		.458		.560
E5	.250 REF		.350 REF		.550 REF	
e	.050 BSC		.050 BSC		.050 BSC	
h	.040 REF		.040 REF		.040 REF	
j	.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055
L2	.077	.093	.077	.093	.077	.093
N	20		28		44	
ND	5		7		11	

15

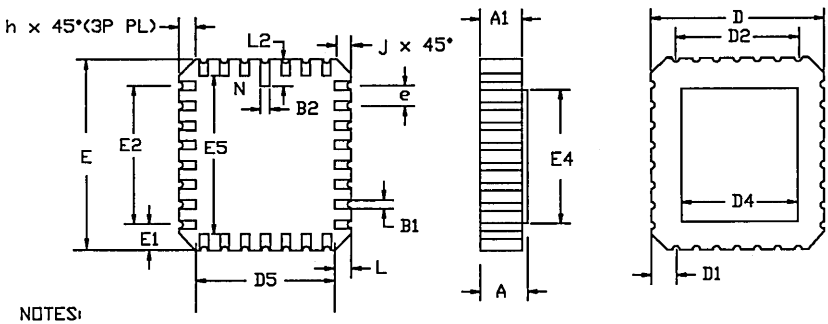
LEADLESS CHIP CARRIERS (Continued)

48–68 PIN LCC (SQUARE)

DWG # / # OF LEADS (N)	L48–1 48 (.040")		L52–1 52		L68–2 68		L68–1 68 (.025")	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.055	.120	.061	.087	.082	.120	.065	.120
A1	.045	.090	.051	.077	.072	.088	.055	.075
B1	.017	.023	.022	.028	.022	.028	.008	.014
B2	.017	.033	.022	.041	.022	.055	.008	.024
D	.554	.572	.739	.761	.938	.962	.554	.566
D1	.060 REF		.075 REF		.075 REF		.080 REF	
D2	.440 BSC		.600 BSC		.800 BSC		.400 BSC	
D4		.546		.661		.862		.535
D5	.480 REF		.650 REF		.850 REF		.430 REF	
E	.554	.572	.739	.761	.938	.962	.554	.566
E1	.060 REF		.075 REF		.075 REF		.080 REF	
E2	.440 BSC		.600 BSC		.800 BSC		.400 BSC	
E4		.546		.661		.862		.535
E5	.480 REF		.650 REF		.850 REF		.430 REF	
e	.040 BSC		.050 BSC		.050 BSC		.025 BSC	
h	.012 RADIUS		.040 REF		.040 REF		.040 REF	
j	.020 REF		.020 REF		.020 REF		.020 REF	
L	.033	.047	.045	.055	.045	.055	.045	.055
L2	.077	.093	.077	.093	.077	.093	.077	.093
N	48		52		68		68	
ND	12		13		17		17	

LEADLESS CHIP CARRIERS (Continued)

20–24 PIN LCC (RECTANGULAR)



NOTES:

[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.

[2] BSC - BASIC PIN SPACING BETWEEN CENTERS.

[3] ND = # LEADS ON 'D' SIDE

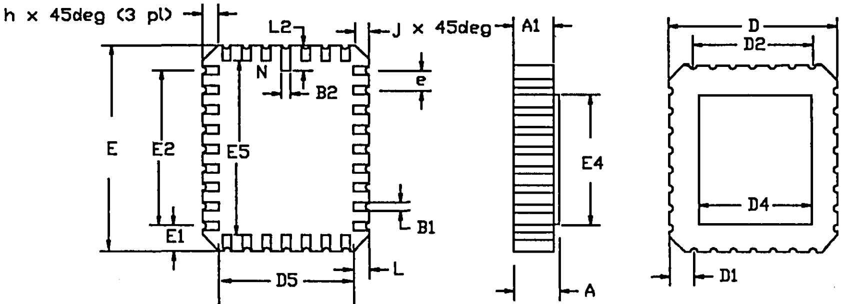
[4] NE = # LEADS ON 'E' SIDE

DWG # / # OF PINS (N)	L20-1 / 20		L22-1 / 22		L24-1 / 24	
	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.100	.064	.100	.064	.100
A1	.050	.066	.054	.063	.054	.066
B1	.022	.028	.022	.028	.022	.028
B2	.022	.041	.022	.041	.022	.041
D	.284	.296	.284	.296	.292	.308
D1	.070 REF		.070 REF		.050 REF	
D2	.150 BSC		.150 BSC		.200 BSC	
D4		.280		.280		.308
D5	.200 REF		.200 REF		.210 REF	
E	.419	.431	.480	.496	.392	.408
E1	.085 REF		.095 REF		.050 REF	
E2	.250 BSC		.300 BSC		.300 BSC	
E4		.410		.480		.408
E5	.335 REF		.400 REF		.310 REF	
e	.050 BSC		.050 BSC		.050 BSC	
h	.012 RADIUS		.012 RADIUS		.025 REF	
J	.012 RADIUS		.012 RADIUS		.015 REF	
L	.039	.051	.039	.051	.045	.055
L2	.083	.097	.083	.097	.077	.093
N	20		22		24	
ND	4		4		5	
NE	6		7		7	

15

LEADLESS CHIP CARRIERS (Continued)

28–32 PIN LCC (RECTANGULAR)



NOTES:

[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.

[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

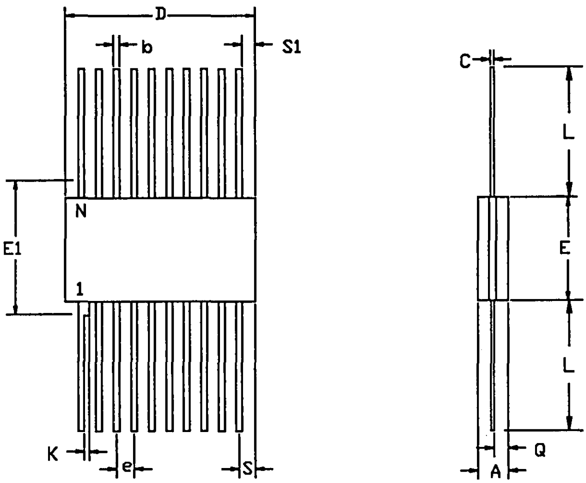
[3] ND = # LEADS ON 'D' SIDE

[4] NE = # LEADS ON 'E' SIDE

DWG # / # OF LEADS (N)	L28-2 / 28		L32-1 / 32	
	MIN	MAX	MIN	MAX
A	.060	.120	.060	.120
A1	.050	.088	.050	.088
B1	.022	.028	.022	.028
B2	.022	.041	.022	.041
D	.342	.358	.442	.458
D1	.075 REF		.075 REF	
D2	.200 BSC		.300 BSC	
D4		.358		.458
D5	.250 REF		.350 REF	
E	.540	.560	.540	.560
E1	.075 REF		.075 REF	
E2	.400 BSC		.400 BSC	
E4		.558		.558
E5	.450 REF		.450 REF	
e	.050 BSC		.050 BSC	
h	.040 REF		.040 REF	
J	.020 REF		.020 REF	
L	.045	.055	.045	.055
L2	.077	.093	.077	.093
N	28		32	
ND	5		7	
NE	9		9	

CERPACKS

16–24 LEAD CERPACK



NOTES:

[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.

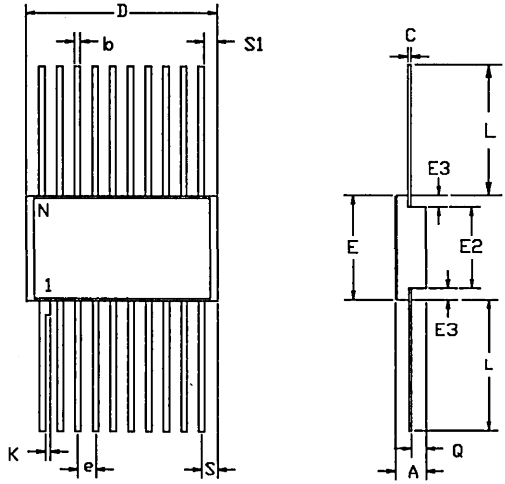
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

DWG # # OF LEADS (N)	E16–1 16 LEADS		E20–1 20–LEADS		E24–1 24–LEADS	
	MIN	MAX	MIN	MAX	MIN	MAX
A	.045	.085	.045	.092	.045	.090
b	.015	.019	.015	.019	.015	.019
C	.003	.006	.003	.006	.003	.006
D		.440		.540		.640
E	.245	.285	.245	.300	.260	.420
E1		.305		.305		.440
e	.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370
Q	.010	.040	.010	.040	.010	.040
S		.045		.045		.045
S1	.005		.005		.005	

15

FLATPACKS

20–28 LEAD FLATPACK



NOTES:

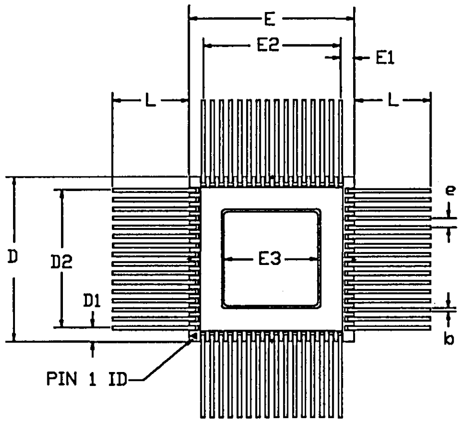
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.

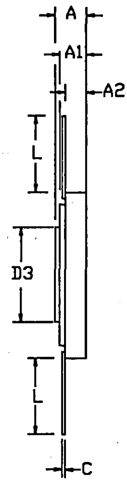
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

DWG # # OF LEADS (N)	F20–1 20–LEADS		F20–2 20–LEADS (.295 BODY)		F24–1 24–LEADS		F28–1 28–LEADS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.045	.092	.045	.092	.045	.090	.045	.090
b	.015	.019	.015	.019	.015	.019	.015	.019
c	.003	.007	.003	.006	.003	.007	.004	.007
D		.540		.540		.640	.710	.740
E	.340	.360	.245	.303	.360	.420	.480	.520
E2	.130		.130		.180		.180	
E3	.030		.030		.030		.040	
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.006	.015	.008	.015				
L	.250	.370	.250	.370	.250	.370	.250	.370
Q	.010	.040	.010	.040	.010	.040	.010	.040
S		.045		.045		.045		.045
S1	.005		.005		.005		.005	

FLATPACKS (Continued)

48–64 LEAD QUAD FLATPACK





NOTES:

[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.

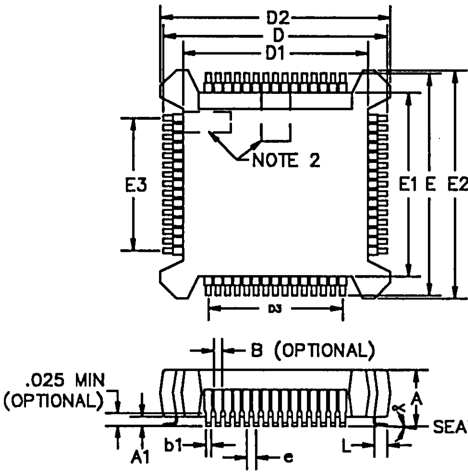
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

DWG # / # OF LEADS (N)	F48–1 48–LEADS		F64–1 64–LEADS	
	MIN	MAX	MIN	MAX
A	.089	.108	.070	.090
A1	.079	.096	.060	.078
A2	.058	.073	.030	.045
b	.018	.022	.016	.020
C	.008	.010	.009	.012
D		.750	.885	.915
D1	.100 REF		.075 REF	
D2	.550 BSC		.750 BSC	
D3		.630	.505	.535
e	.050 BSC		.050 BSC	
E		.750	.885	.915
E1	.100 REF		.075 REF	
E2	.550 BSC		.750 BSC	
E3		.630	.505	.535
L	.350	.450	.350	.450
ND	12		16	
NE	12		16	

15

PLASTIC FLATPACKS

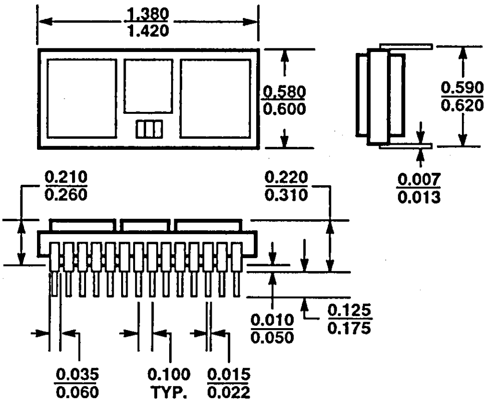
84-132 LEAD PLASTIC QUAD FLATPACK (GULL WING)



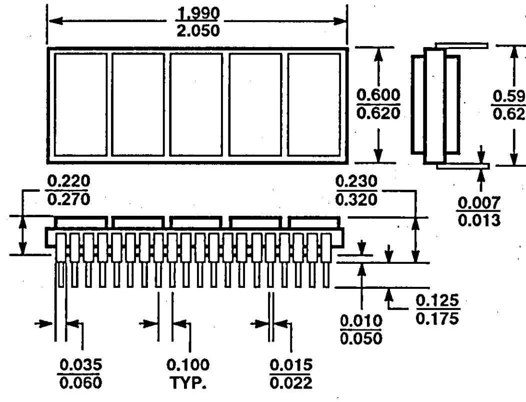
NOTES: UNLESS OTHERWISE SPECIFIED
1. DIMS D1,D2, E1 & E2 DO NOT INCLUDE MOLD PROTRUSION.
   ALLOWABLE MOLD PROTRUSIONS ARE AS FOLLOWS:
   D1 & E1= .010" MAX
   D2 & E2= .007" MAX
2. PIN 1 IDENTIFIER CAN BE POSITIONED AT EITHER ONE OF THESE TWO LOCATIONS.

DWG No.	PF84-1		PF100-1		PF132-1	
No OF LEAD	84 LD		100 LD		132 LD	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.160	.180	.160	.180	.160	.180
A1	.020	.040	.020	.040	.020	.040
B	.008	.016	.008	.016	.008	.016
b1	.008	.012	.008	.012	.008	.012
C	.0055	.008	.0055	.008	.0055	.008
D	.775	.785	.875	.885	1.075	1.085
D1	.647	.653	.747	.753	.947	.953
D2	.797	.803	.897	.903	1.097	1.103
D3	.500 REF		.600 REF		.800 REF	
e	.025 BSC		.025 BSC		.025 BSC	
E	.775	.785	.875	.885	1.075	1.085
E1	.647	.653	.747	.753	.947	.953
E2	.797	.803	.897	.903	1.097	1.103
E3	.500 REF		.600 REF		.800 REF	
L	.020	.030	.020	.030	.020	.030
∝	0°	8°	0°	8°	0°	8°
N	84		100		132	

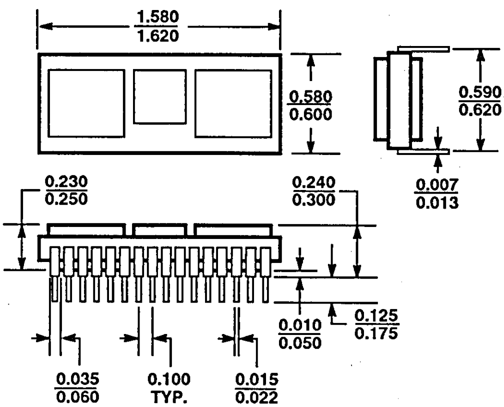
(M1) 28–PIN SIDEBRAZE DIP



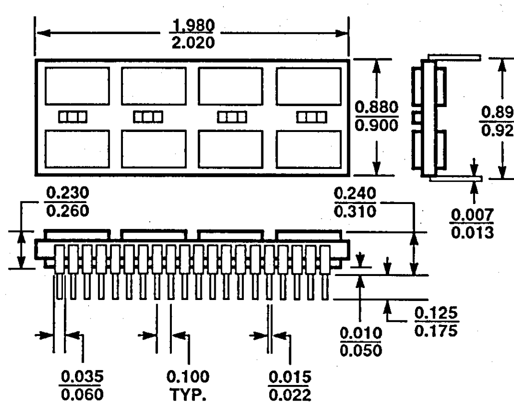
(M4) 40–PIN SIDEBRAZE DIP



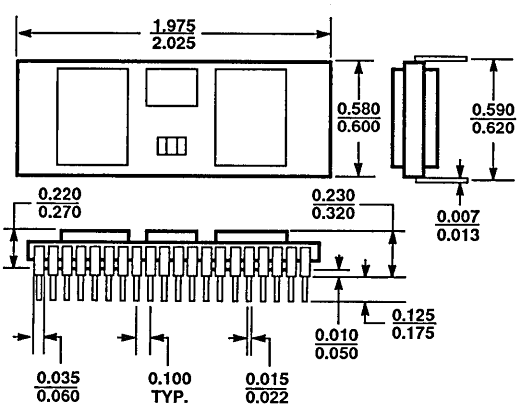
(M2) 32–PIN SIDEBRAZE DIP



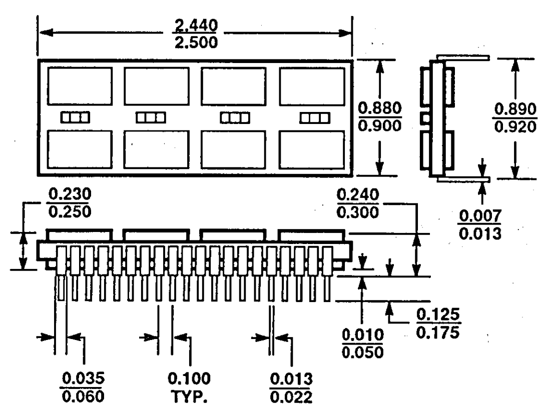
(M5) 40–PIN SIDEBRAZE DIP



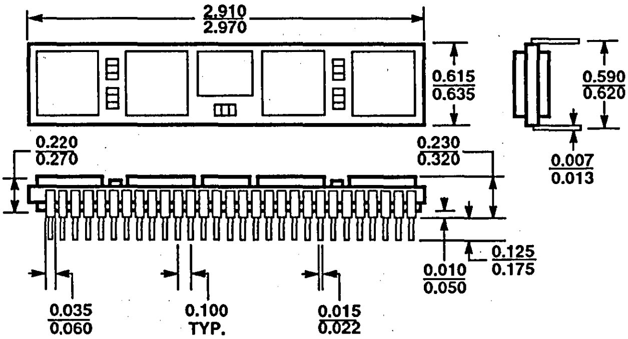
(M3) 40–PIN SIDEBRAZE DIP



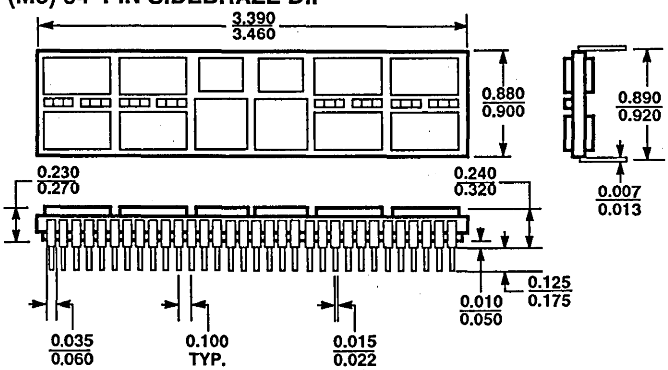
(M6) 40–PIN SIDEBRAZE DIP



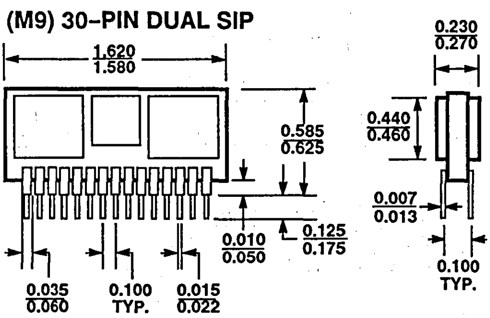
(M7) 58-PIN SIDEBRAZE DIP



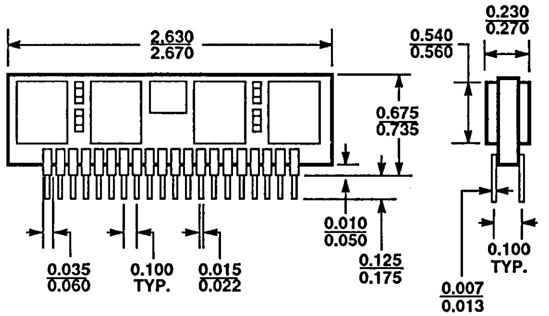
(M8) 64-PIN SIDEBRAZE DIP



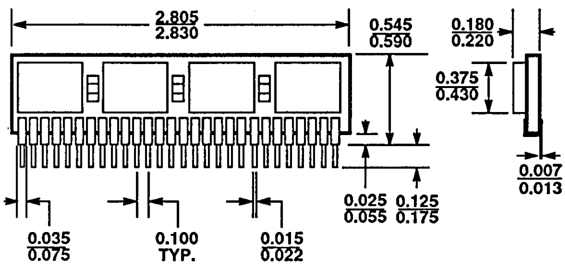
(M9) 30-PIN DUAL SIP



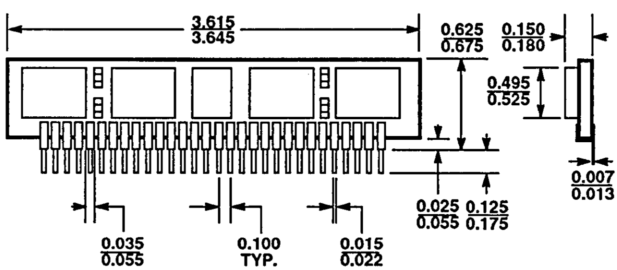
(M10) 40–PIN DUAL SIP



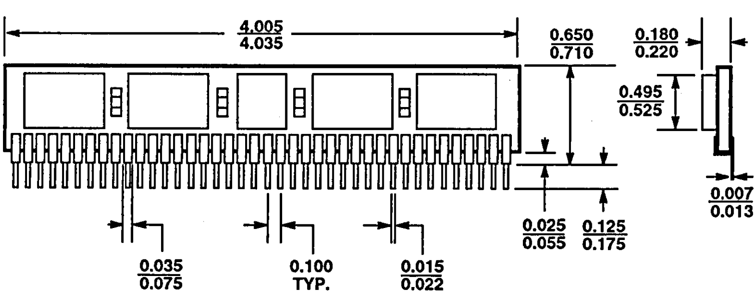
(M11) 28–PIN PLASTIC SIP



(M12) 30–PIN PLASTIC SIP

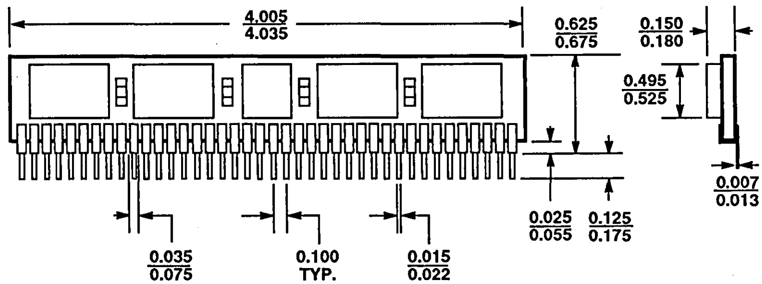


(M13) 40–PIN PLASTIC SIP

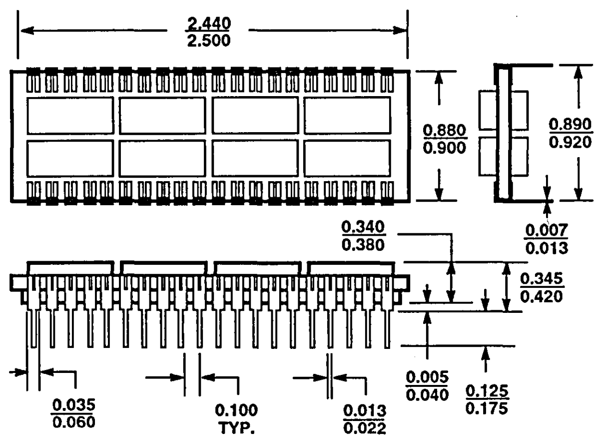


15

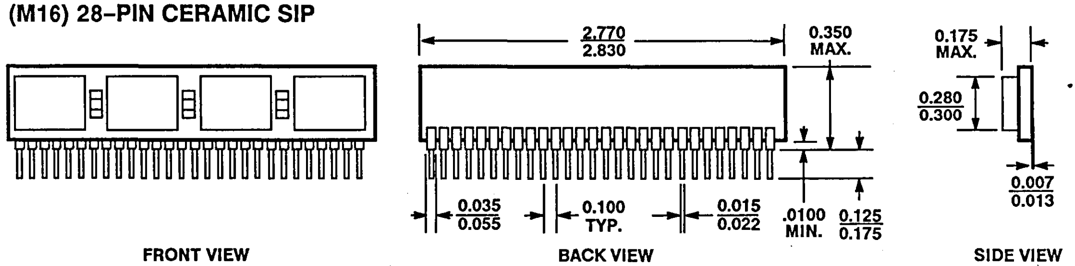
(M14) 40-PIN PLASTIC SIP



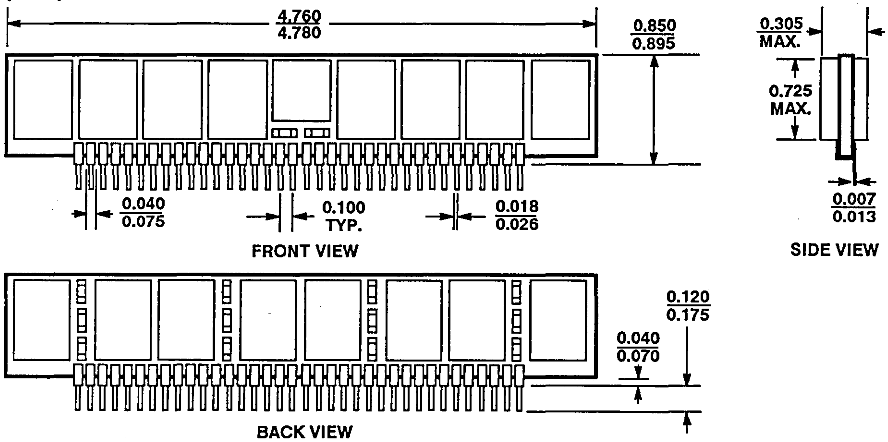
(M15) 40-PIN PLASTIC DIP



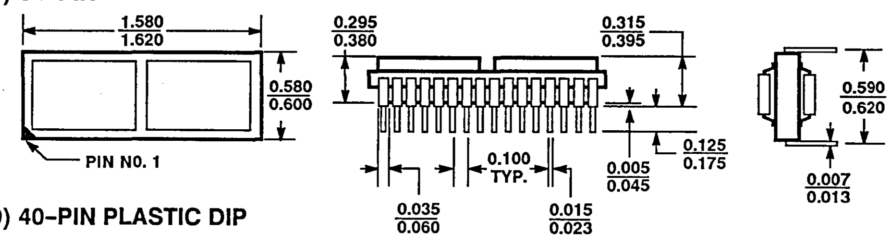
(M16) 28-PIN CERAMIC SIP



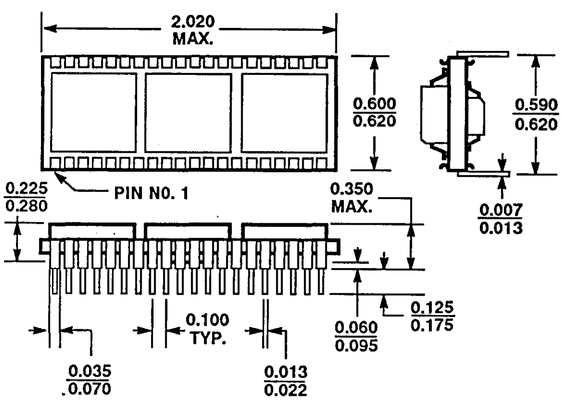
(M17) 36–PIN PLASTIC SIP



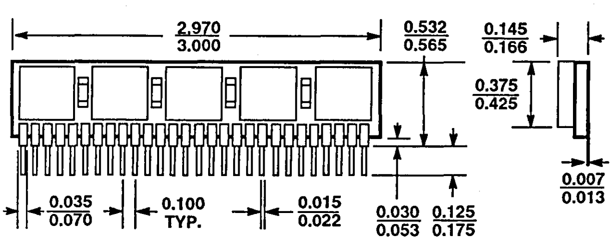
(M18) 32–PIN



(M19) 40–PIN PLASTIC DIP



(M20) 28–PIN PLASTIC SIP



15

Integrated Device Technology, Inc. has sales representatives and distributors covering each geographic area. Contact the nearest IDT Area Sales Office for the number of the local IDT sales office in your region.

Integrated Device Technology Area Sales Offices are located in:

BOSTON

15 Pleasant Street Connector
Suite 502
Framingham, MA 01701
Tel.: (617) 872-4900
TLX: 855249
FAX: (617) 872-4906

CHICAGO

1375 E. Woodfield Road
Suite 380
Schaumburg, IL 60173
Tel.: (312) 843-1262
TWX: (910) 651-1910
FAX: (312) 843-2430

LOS ANGELES

1570 Brookhollow Drive
Suite 208
Santa Ana, CA 92705
Tel: (714) 641-0601
EasyLink: 62909903
FAX: (714) 641-0855

SANTA CLARA

3001 Stender Way
Santa Clara, CA 95052
Tel.: (408) 492-8350
FAX: (408) 492-8358

IDT INTERNATIONAL LOCATIONS:

UNITED KINGDOM*

5 Bridge Street
Leatherhead
Surrey, UK KT228BL
Tel.: 011-44-372-377375
TWX: 851-94012233
FAX: 011-44-372-378851

GERMANY

Steinsdorfstrasse 19/1
8000 Munich 22
West Germany
Tel.: 011-49-89-228-5071
TLX: 5214056
FAX: 011-49-89-228-5491

JAPAN

U.S. Bldg. 201
1-6-15 Hirakawa-Cho, Chiyoda-Ku
Tokyo 102, Japan
Tel.: 011-81-3-221-9821
FAX: 011-81-3-221-9824

* European Headquarters

Integrated Device Technology
3236 Scott Boulevard, Santa Clara, CA 95054-3090
(408) 727-6116 FAX: (408) 727-3468

Suggested Resale: $9.95