ICT INC.

PEEL™ Products Data Book

Includes PLACE Software Manual

1994

Data Book

General Information

PEEL Arrays

PEEL Devices

Development Tools

Application Notes and Reports

Package Information

Sales Representatives and Distributors

PLACE Users Manual

Introduction to PLACE

PLACE Installation

Getting Started with PLACE

Operation Reference Guide

PLACE Design Language

Application Examples

Advanced Designation

The "Advanced" designation on an ICT data sheet indicates that the product is not yet ready for release. The specifications are subject to change, are based on design goals or preliminary part evaluation, and are not guaranteed. ICT or an authorized sales representative should be consulted for current information before using this product.

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The "Preliminary" designation on an ICT data sheet indicates that the product is not fully characterized. The specifications are subject to change, are based on design goals or preliminary part evaluation, and are not guaranteed. ICT or an authorized sales representative should be consulted for current information before using this product.

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©1993, Revised November 1993
ICT, Inc.
2123 Ringwood Avenue
San Jose, CA 95131
(408) 434-0678

Fax # (408) 434-0688
Marketing Fax # (408) 432-0815
BBS # (408) 434-0130 (2400bps, N, 8, 1)

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President's Message

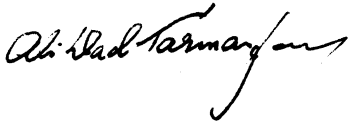
ICT Inc. is pleased to bring to you our 1993/1994 PEEL Products Data Book. Our dedicated staff continually strives to produce leading-edge programmable logic products with the features, performance, technology and development support needed by designers of electronic systems. Representative of our expanding product line and fast growing business, this years data book is larger than ever before.

Highlights from this years book include:

- Expanded PEEL Array section including the new 15ns PA7024.
- Industrial PEEL Devices and PEEL Arrays for extended operating voltage and temperature requirements.
- 5ns versions of the PEEL 18CV8, 20CG10A, and 22CV10A offering the fastest speeds available among low density CMOS PLDs.
- Low voltage and zero-power versions of the PEEL 22CV10A ideal for power sensitive portable applications.
- Advanced "Fitter" software for ABEL and CUPL, supporting PEEL Arrays.
- New application notes, characterization and reliability reports.
- The complete users manual for the powerful PLACE Development Software which is available free to PLD users.

Besides our product line expansion, ICT has enhanced its alliances with major semiconductor companies and fabrication facilities, ensuring high-volume manufacturing capability to support our future growth. ICT has also continued its serious commitment to customer satisfaction. At ICT, we understand that true product excellence is obtained by continuous effort in quality and customer service.

We thank you for your interest in ICT products and know you will find our 1993/1994 Data Book useful in your present and future programmable logic endeavors.



Alidad Farmanfarma
President, Chairman, CEO

ICT Product Overview

ICT Inc. designs, manufactures, and markets user-programmable integrated circuits. With expertise in technology and design, ICT specializes in Programmable Logic Devices (PLDs) based on the companies CMOS EEPROM technology. First introduced in 1986, ICT's Programmable Electrically Erasable Logic, PEEL™ Devices are among the first PLDs to utilize CMOS EEPROM technology, now the technology of choice among PLD users. ICT's product definition, design, and technology efforts have continued to improve and expand the PEEL product line.

Today there are two primary PEEL families: PEEL Devices for low-density standard PLD designs, and PEEL Arrays for medium-density complex PLD designs. Both families provide an attractive alternative to ordinary PLDs by offering the performance, flexibility, technology, and ease of design needed by programmable logic users. ICT's product line also includes development tools with everything required to ease the development of custom logic designs for PEEL Devices and PEEL Arrays. (see Figure 1)

PEEL Devices	PEEL Arrays	Development Tools
PEEL18CV8	PA7024	PLACE Advanced Development Software
PEEL20CG10A	PA7140	ABEL-to-PEEL Advanced Fitter
PEEL22CV10A	PA7128	CUPL-to-PEEL Advanced Fitter
		PDS-3 PEEL Development System

Figure 1. ICT Product Line

PEEL Devices

Programmable Electrically Erasable Logic (PEEL) Devices provide an attractive alternative to ordinary low-density PLDs. ICT's PEEL Device family is based on three main architectures; the PEEL 18CV8, 20CG10A and 22CV10A. PEEL Device products are distinguished by speed and offered in ranges from 5ns to 25ns tpd. Each product has a variety for power, package and operating-grade options. Power options for PEEL Devices are lower than most standard PLD families. Packaging comes in 20 and 24 pin DIP and SOIC and 20 and 28 pin PLCC. Operating temperature and voltage options include both commercial and industrial grade versions.

PEEL Device EE-technology provides the convenience of instant reprogramming for development and allows for a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability assuring the highest quality possible.

PEEL device architectures allow for super-set replacement of over 40 standard 20-pin and 24-pin PLDs (PAL, GAL, EPLD, etc.). They also offer additional architectural features so more logic can be put into every design. ICT's JEDEC file translation software instantly converts PEEL Devices to other PLDs without the need to rework the existing design. Development and programming support for the PEEL Devices is provided by ICT as well as manufactures of popular third-party programmers and development software.

For further information on PEEL Devices please refer to the selection guide and cross reference in Section 1 of this data book, as well as the individual data sheets in Section 3. Additional information on PEEL Devices is also included in the application notes and reports provided in Section 5.

PEEL Arrays

Programmable Electrically Erasable Logic (PEEL) Arrays are a family of Complex Programmable Logic Devices (CPLDs) based on ICT's CMOS EEPROM technology. PEEL Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and the speed needed for today's medium-density programmable logic designs.

The initial PEEL Array family consists of three parts the PA7024, PA7128 and PA7140. Packages range from 24 to 44 pins in plastic DIP, PLCC, and SOIC formats. ICT's CMOS EE technology allows reprogramability and high-speed performance. Wide-gate delays as fast as 9ns for internal (buried) and 15ns external (pin to pin) are possible with PEEL Arrays. Clock frequencies can be as fast as 76.9MHz for sequential functions. The PEEL Array architecture is based on a versatile multi-level logic array architecture rich in input latches, buried registers and sum-of-product logic functions. The basic logic array structure is similar to that of a PLA allowing true product term sharing. PEEL Arrays offer the most flexible logic and I/O cells of any CPLD available today. The unique PEEL Array logic cell incorporates multiple outputs allowing registers and combinatorial logic to be buried without limiting the use of I/O pins as with other CPLDs.

Logic cell registers are user-configurable to be true D, T and JK registers with independent or global clocks, resets, presets, clock polarity and other special features. Additionally, all registers and output enables allow full sum-of-products control. PEEL Arrays are ideal for implementing a wide variety of general purpose combinatorial, synchronous and asynchronous logic applications, including: buried counters, complex state-machines, comparitors, decoders, encoders, adders, address/data demux and other wide-gate logic. Because PEEL Arrays allow for multi-level buried logic, designs normally requiring multiple PLDs and/or random logic can be efficiently integrated. Development support for PEEL Arrays is provided by ICT and popular third party development tool manufacturers.

For further information on PEEL Arrays please refer to the selection guide in Section 1 of this data book as a well as the Introduction to PEEL Arrays and PEEL Array data sheets in Section 2.

Development Tools

Development and programming support for PEEL Arrays and PEEL Devices is provided by ICT and popular third party development tool manufacturers.

ICT's powerful PLACE Development Software (free to qualified PLD designers) provides everything a designer needs to develop custom logic designs for PEEL products. PLACE includes an architectural editor, logic compiler, waveform simulator, documentation utility, and a programmer interface. The PLACE editor graphically illustrates and controls the PEEL Arrays architecture, making the overall design easy to understand, while allowing the effectiveness of boolean logic equations, state machine design, and truth table entry. The PLACE compiler performs logic transformation and reduction making it possible to specify equations in almost any fashion and to fit the maximum logic into every design. PLACE also provides a multi-level logic simulator allowing external and internal signals to be fully simulated and analyzed via a waveform display.

Popular third-party development tools such as ABEL, CUPL, PLDesigner, and LOG/iC also support ICT PEEL products. PEEL Devices specifically are well supported as standard device types by all of these PLD software packages. Designers using PEEL Arrays can utilize ICT's ABEL-to-PEEL or CUPL-to-PEEL Advanced Fitters. The Fitters allow designer to use familiar tools, while making sure the logic description is properly mapped into the selected PEEL Array.

Programming for PEEL products is supported by many popular third-party programmers (see Programming Support list in Section 4.0 in this Data Book). ICT also offers the PEEL Development System (PDS-series) programmers with support for all PEEL Devices and PEEL Arrays.

For further information on PEEL Devices and Array Development Tools please refer to the Section 4 of this data book as well as the PLACE Users Manual included in the second half of this book.

ICT Quality and Reliability

ICT, Inc. is dedicated to providing its customers with integrated circuits designed, manufactured, tested, and serviced to the highest level of quality and reliability. From product definition through full production, ICT has developed and implemented a system designed to continually produce leading-edge CMOS products that meet, or exceed, all customer requirements.

"At ICT, we recognize that product excellence is obtained by a continuous commitment to quality and customer service."

Customer Service

ICT is committed to providing quality products and service to our customer's expectations. ICT is committed to providing quality products and service to our customer's expectations. At ICT, customer service plays an important role in quality assurance. All ICT employees are a part of the customer service team, whose goal is to provide complete customer satisfaction. ICT's commitment to this effort includes: expediting on-time deliveries, providing quick access to and action by our customer service department, keeping our sales marketing and applications organization well trained for product support, publishing accurate and informative product documentation, addressing customer concerns and processing corrective actions, and ensuring that customer quality, reliability and service is kept in mind from design through production.

Quality and Reliability by Design

ICT's design philosophy emphasizes quality and reliability during every part of the design cycle. Conservative design rules and extensive logic and circuit simulation are performed over extreme operating conditions. During circuit and process design, special attention is paid to problems such as CMOS latch-up and electrostatic discharge (ESD). For example, ICT's I/O pins are prevented from CMOS latch-up by a double guard-ring designed into all products. Also ICT designers have developed and implemented techniques to protect all products from electrostatic discharge (ESD) up to 2000V on all I/O pins.

Initial Device Qualification

Tests have been developed to observe the life expectancy of each new product. In order to qualify a new product, packaged parts from a minimum of three different lots must be scrutinized for electrical functionality and reliability over extreme temperature and voltage conditions. Tests include operating life, data retention, endurance, temperature cycling, 85/85, ESD, and latch-up. Pre-determined reliability goals must be met in order for a product to pass qualification. All procedures and results are carefully documented for future reference. This qualification validates the device, package, and supplier. When design rules are adjusted, a new foundry or assembly facility is used, or a new package type is introduced, a re-qualification of the product is addressed. (For more information see Reliability Report RR-1 in section 5.0 of the Data Book).

Ongoing Monitor Qualification

Although initial device qualification is an essential step to a product release, all products must be constantly monitored to ensure the reliability of the device. Production lots are sampled every quarter, and are subject to the same qualification tests. All results are again documented, and failures are carefully analyzed in order to find long term improvements to the product.

Quality and Reliability by Test

ICT has developed a test flow to ensure that all products shipped to customers are of the highest quality and reliability. Each device is erased, programmed, and read at Wafer Sort, Post-Bake Final Test, Package Test, and QA Test to guarantee electrical and functional characteristics of the part over the entire operating temperature range. Test programs are developed to screen out those devices which fail to meet data sheet specifications. Additionally since all of ICT's products are programmable, every unit shipped is subjected to a data retention bake which verifies the ability to retain data for at least ten years over the entire temperature range. This is the equivalent of over forty years of data retention at 55^{o}C.

PEEL Array Selection Guide

PART #	DESCRIPTION	SPEED[4]	Icc mA[3]	TEMP[1]	PACKAGE[2]	PAGE
PA7024P-15	20 I/Os, 2 I/CLKs, 40 registers/latches	10/15ns	140	C	P24	2-13
PA7024P-20 PA7024P-1	20 I/Os, 2 I/CLKs, 40 registers/latches	13/20ns	140	C	P24	2-13
PA7024P-25 PA7024P-2	20 I/Os, 2 I/CLKs, 40 registers/latches	17/25ns	140	C	P24	2-13
PA7024PI-25 PA7024PI-2	Industrial Temp. Range PA7024	17/25ns	155	I	P24	2-21
PA7024J-15	Surface Mount PA7024	10/15ns	140	C	J28	2-13
PA7024J-20 PA7024J-1	Surface Mount PA7024	13/20ns	140	C	J28	2-13
PA7024J-25 PA7024J-2	Surface Mount PA7024	17/25ns	140	C	J28	2-13
PA7024JI-25 PA7024JI-2	Industrial Temp. Range PA7024	17/25ns	155	I	J28	2-21
PA7024JN-15	Surface Mount - Alternate Pin Out	10/15ns	140	C	JN28	2-13
PA7024JN-20 PA7024JN-1	Surface Mount - Alternate Pin Out	13/20ns	140	C	JN28	2-13
PA7024JN-25 PA7024JN-2	Surface Mount - Alternate Pin Out	17/25ns	140	C	JN28	2-13
PA7024S-15	Surface Mount SOIC	10/15ns	140	C	S24	2-13
PA7024S-20 PA7024S-1	Surface Mount SOIC	13/20ns	140	C	S24	2-13
PA7024S-25 PA7024S-2	Surface Mount SOIC	17/25ns	140	C	S24	2-13
PA7024SI-25 PA7024SI-2	Industrial Temp. Range PA7024	17/25ns	155	I	S24	2-21
PA7128P-15 PA7128P-1	12 I/Os, 14 Inputs, 36 registers/latches	9/15ns	135	C	P28	2-27
PA7128P-20 PA7128P-2	20 I/Os, 14 Inputs, 40 registers/latches	12/20ns	135	C	P28	2-27
PA7128J-15 PA7128J-1	Surface Mount PA7128	9/15ns	135	C	J28	2-27
PA7128J-20 PA7128J-2	Surface Mount PA7128	12/20ns	135	C	J28	2-27
PA7128S-15 PA7128S-1	Surface Mount SOIC	9/15ns	135	C	S28	2-27
PA7128S-20 PA7128S-2	Surface Mount SOIC	12/20ns	135	C	S28	2-27

PEEL Array Selection Guide (continued)

PART #	DESCRIPTION	SPEED[4]	I_{CC} mA[3]	TEMP[1]	PACKAGE[2]	PAGE
PA7140T-20 PA7140T-1	24 I/Os, 14 Inputs, 60 registers/latches	13/20ns	150	C	T40	2-35
PA7140T-25 PA7140T-2	24 I/Os, 14 Inputs, 60 registers/latches	17/25ns	150	C	T40	2-35
PA7140J-20 PA7140J-1	Surface Mount PA7140	13/20ns	150	C	J44	2-35
PA7140J-25 PA7140J-2	Surface Mount PA7140	17/25ns	150	C	J44	2-35

[1] **Temperature range codes:**

C = Commercial 0°C to +70°C

I = Industrial -40°C to +85°C

[2] **Package Codes:** See section 6.0 for package drawings

J = PLCC

P = Plastic DIP (300 mil)

T = Plastic DIP (600 mil)

JN = PLCC (Alternate Pinout)

S = SOIC

[3]) **Icc** is specified at 25 MHz unless otherwise noted

[4] **Speed** designations refer to t_{PDI} / t_{PDX}

PEEL Device Selection Guide

PART #	DESCRIPTION	SPEED	Icc mA[3]	TEMP[1]	PACKAGE[2]	PAGE
PEEL18CV8P-7	PLD superset 12 config. I/O pins (8)	7.5ns	110	C	P20	3-3
PEEL18CV8P-10	PLD superset 12 config. I/O pins (8)	10ns	110	C	P20	3-3
PEEL18CV8P-15	PLD superset 12 config. I/O pins (8)	15ns	45	C	P20	3-3
PEEL18CV8P-25	PLD superset 12 config. I/O pins (8)	25ns	37	C	P20	3-3
PEEL18CV8PI-10	Industrial Temp. Range PEEL18CV8	10ns	115	I	P20	3-13
PEEL18CV8PI-15	Industrial Temp. Range PEEL18CV8	15ns	55	I	P20	3-13
PEEL18CV8PI-25	Industrial Temp. Range PEEL18CV8	25ns	50	I	P20	3-13
PEEL18CV8J-5	Surface mount PLCC PEEL18CV8	5ns	120	C	J20	3-10
PEEL18CV8J-7	Surface mount PLCC PEEL18CV8	7.5ns	110	C	J20	3-3
PEEL18CV8J-10	Surface mount PLCC PEEL18CV8	10ns	110	C	J20	3-3
PEEL18CV8J-15	Surface mount PLCC PEEL18CV8	15ns	45	C	J20	3-3
PEEL18CV8J-25	Surface mount PLCC PEEL18CV8	25ns	37	C	J20	3-3
PEEL18CV8JI-10	Industrial Temp. Range PEEL18CV8	10ns	115	I	J20	3-13
PEEL18CV8JI-15	Industrial Temp. Range PEEL18CV8	15ns	55	I	J20	3-13
PEEL18CV8JI-25	industrial Temp. Range PEEL18CV8	25ns	50	I	J20	3-13
PEEL18CV8S-7	Surface mount SOIC	7.5ns	110	C	S20	3-3
PEEL18CV8S-10	Surface mount SOIC	10ns	110	C	S20	3-3
PEEL18CV8S-15	Surface mount SOIC	15ns	45	C	S20	3-3
PEEL18CV8S-25	Surface mount SOIC	25ns	37	C	S20	3-3
PEEL18CV8SI-10	Industrial Temp. Range PEEL18CV8	10ns	115	I	S20	3-13
PEEL18CV8SI-15	Industrial Temp. Range PEEL18CV8	15ns	55	I	S20	3-13
PEEL18CV8SI-25	Industrial Temp. Range PEEL18CV8	25ns	50	I	S20	3-13
PEEL20CG10AP-7	PLD superset 12 config. I/O pins (10)	7.5ns	155	C	P24	3-16
PEEL20CG10AP-10	PLD superset 12 config. I/O pins (10)	10ns	135	C	P24	3-16
PEEL20CG10APL-15	PLD superset 12 config. I/O pins (10)	15ns	75	C	P24	3-16
PEEL20CG10AP-15	PLD superset 12 config. I/O pins (10)	15ns	135	C	P24	3-16
PEEL20CG10AP-25	PLD superset 12 config. I/O pins (10)	25ns	67	C	P24	3-16
PEEL20CG10API-10	Industrial Temp. Range PEEL20CG10A	10ns	145	I	P24	3-26
PEEL20CG10API-15	Industrial Temp. Range PEEL20CG10A	15ns	145	I	P24	3-26
PEEL20CG10API-25	Industrial Temp. Range PEEL20CG10A	25ns	75	I	P24	3-26
PEEL20CG10AJ-5	Surface mount PLCC PEEL20CG10A	5ns	140	C	J28	3-23
PEEL20CG10AJ-7	Surface mount PLCC PEEL20CG10A	7.5ns	155	C	J28	3-16

PEEL Device Selection Guide (continued)

PART #	DESCRIPTION	SPEED	Icc mA[3]	TEMP[1]	PACKAGE[2]	PAGE
PEEL20CG10AJ-10	Surface mount PLCC PEEL20CG10A	10ns	135	C	J28	3-16
PEEL20CG10AJL-15	Surface mount PLCC PEEL20CG10A	15ns	75	C	J28	3-16
PEEL20CG10AJ-15	Surface mount PLCC PEEL20CG10A	15ns	135	C	J28	3-16
PEEL20CG10AJ-25	Surface mount PLCC PEEL20CG10A	25ns	67	C	J28	3-16
PEEL20CG10AJI-10	Industrial Temp. Range PEEL20CG10A	10ns	145	I	J28	3-26
PEEL20CG10AJI-15	Industrial Temp. Range PEEL20CG10A	15ns	145	I	J28	3-26
PEEL20CG10AJI-25	Industrial Temp. Range PEEL20CG10A	25ns	75	I	J28	3-26
PEEL20CG10AS-7	Surface mount SOIC PEEL20CG10A	7.5ns	155	C	S24	3-16
PEEL20CG10AS-10	Surface mount SOIC PEEL20CG10A	10ns	135	C	S24	3-16
PEEL20CG10ASL-15	Surface mount SOIC PEEL20CG10A	15ns	75	C	S24	3-16
PEEL20CG10AS-15	Surface mount SOIC PEEL20CG10A	15ns	135	C	S24	3-16
PEEL20CG10AS-25	Surface mount SOIC PEEL20CG10A	25ns	67	C	S24	3-16
PEEL20CG10ASI-10	Industrial Temp. Range PEEL20CG10A	10ns	145	I	S24	3-26
PEEL20CG10ASI-15	Industrial Temp. Range PEEL20CG10A	15ns	145	I	S24	3-26
PEEL20CG10ASI-25	Industrial Temp. Range PEEL20CG10A	25ns	75	I	S24	3-26
PEEL22CV10AP-7	PLD superset 4/12 config, I/O pins (10)	7.5ns	155	C	P24	3-29
PEEL22CV10AP-10	PLD superset 4/12 config, I/O pins (10)	10ns	135	C	P24	3-29
PEEL22CV10AP-15	PLD superset 4/12 config, I/O pins (10)	15ns	135	C	P24	3-29
PEEL22CV10APL-15	PLD superset 4/12 config, I/O pins (10)	15ns	75	C	P24	3-29
PEEL22CV10AP-25	PLD superset 4/12 config. I/O pins (10)	25ns	67	C	P24	3-29
PEEL22CV10API-10	Industrial Temp. Range PEEL22CV10A	10ns	145	I	P24	3-40
PEEL22CV10API-15	Industrial Temp. Range PEEL22CV10A	15ns	145	I	P24	3-40
PEEL22CV10API-25	Industrial Temp. Range PEEL22CV10A	25ns	75	I	P24	3-40
PEEL22CV10AJ-5	Surface mount PLCC PEEL22CV10A	5ns	140	C	J28	3-37
PEEL22CV10AJ-7	Surface mount PLCC PEEL22CV10A	7.5ns	155	C	J28	3-29
PEEL22CV10AJ-10	Surface mount PLCC PEEL22CV10A	10ns	135	C	J28	3-29
PEEL22CV10AJ-15	Surface mount PLCC PEEL22CV10A	15ns	135	C	J28	3-29
PEEL22CV10AJL-15	Surface mount PLCC PEEL22CV10A	15ns	75	C	J28	3-29
PEEL22CV10AJ-25	Surface mount PLCC PEEL22CV10A	25ns	67	C	J28	3-29
PEEL22CV10AJI-10	Industrial Temp. Range PEEL22CV10A	10ns	145	I	J28	3-40
PEEL22CV10AJI-15	Industrial Temp. Range PEEL22CV10A	15ns	145	I	J28	3-40
PEEL22CV10AJI-25	Industrial Temp. Range PEEL22CV10A	25ns	67	I	J28	3-40

PEEL Device Selection Guide (continued)

PART #	DESCRIPTION	SPEED	Icc mA[3]	TEMP[1]	PACKAGE[2]	PAGE
PEEL22CV10AS-7	Surface mount SOIC PEEL22CV10A	7.5ns	155	C	S24	3-29
PEEL22CV10AS-10	Surface mount SOIC PEEL22CV10A	10ns	135	C	S24	3-29
PEEL22CV10AS-15	Surface mount SOIC PEEL22CV10A	15ns	135	C	S24	3-29
PEEL22CV10ASL-15	Surface mount SOIC PEEL22CV10A	15ns	75	C	S24	3-29
PEEL22CV10AS-25	Surface mount SOIC PEEL22CV10A	25ns	67	C	S24	3-29
PEEL22CV10ASI-10	Industrial Temp. Range PEEL22CV10A	10ns	135	I	S24	3-40
PEEL22CV10ASI-15	Industrial Temp. Range PEEL22CV10A	15ns	135	I	S24	3-40
PEEL22CV10ASI-25	Industrial Temp. Range PEEL22CV10A	25ns	67	I	S24	3-40
PEEL22V10AZ3P-15	3V Zero Power, I/O pins (10)	15ns	<10µA stby.	C	P24	3-43
PEEL22V10AZ3J-15	Surface mount PLCC PEEL22V10AZ3	15ns	<10µA stby.	C	J28	3-43
PEEL22V10AZ3S-15	Surface mount SOIC PEEL22V10AZ3	15ns	<10µA stby.	C	S24	3-43
PEEL22V10AZ3P-25	3V Zero Power, I/O pins (10)	25ns	<10µA stby.	C	P24	3-43
PEEL22V10AZ3J-25	Surface mount PLCC PEEL22V10AZ3	25ns	<10µA stby.	C	J28	3-43
PEEL22V10AZ3S-25	Surface mount SOIC PEEL22V10AZ3	25ns	<10µA stby.	C	S24	3-43
PEEL22V10AZP-15	5V Zero Power, I/O pins (10)	15ns	<10µA stby.	C	P24	3-43
PEEL22V10AZJ-15	Surface mount PLCC PEEL22V10AZ	15ns	<10µA stby.	C	J28	3-43
PEEL22V10AZS-15	Surface mount SOIC PEEL22V10AZ	15ns	<10µA stby.	C	S24	3-43
PEEL22V10AZP-25	5V Zero Power, I/O pins (10)	25ns	<10µA stby.	C	P24	3-43
PEEL22V10AZJ-25	Surface mount PLCC PEEL22V10AZ	25ns	<10µA stby.	C	J28	3-43
PEEL22V10AZS-25	Surface mount SOIC PEEL22V10AZ	25ns	<10µA stby.	C	S24	3-43

[1] **Temperature range codes:**
C = Commercial 0°C to +70°C
I = Industrial -40°C to +85°C

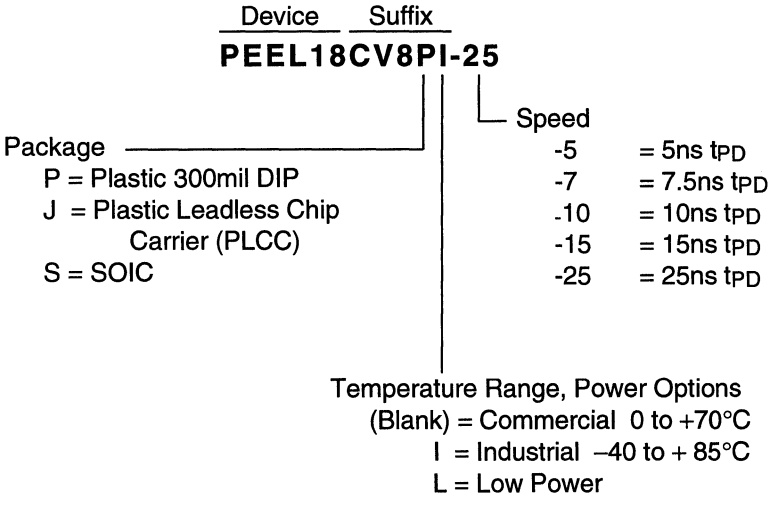
[2] **Package Codes:** See section 6.0 for package drawings
J = PLCC
P = Plastic DIP (300 mil)
T = Plastic DIP (600 mil)
JN = PLCC (Alternate Pinout)
S = SOIC

[3] **Icc** is specified at 25 MHz unless otherwise noted

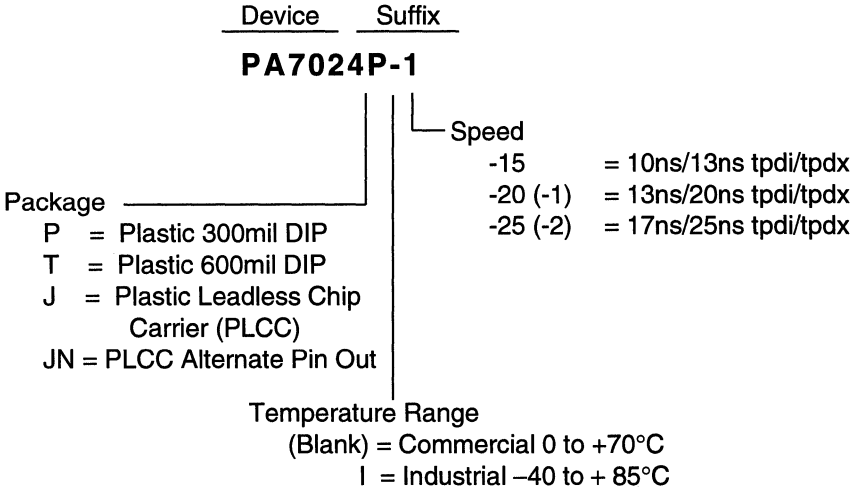
[4] **Speed** designations refer to t_{PDI} / t_{PDX}

Ordering Information

PEEL Devices



PEEL Arrays



PEEL Device Cross Reference ❖

Altera ☞ ICT	
EP310	PEEL18CV8
EP320	PEEL18CV8
EP330	PEEL18CV8

AMI ☞ ICT	
PEEL18CV8†	PEEL18CV8
PEEL20CG10†	PEEL20CG10A
PEEL22CV10A†	PEEL22CV10A

AMD ☞ ICT	
AmPAL16L8	PEEL18CV8
AmPAL16R4	PEEL18CV8
AmPAL16R6	PEEL18CV8
AmPAL16R8	PEEL18CV8
AmPAL18P8	PEEL18CV8
PALC16L8Q	PEEL18CV8
PALC16R4Q	PEEL18CV8
PALC16R6Q	PEEL18CV8
PALC16R8Q	PEEL18CV8
PALC18U8Q	PEEL18CV8
PALCE16V8	PEEL18CV8
PALCE20V8	PEEL20CG10A
PALCE22V10†	PEEL22CV10A
PAL10H8A	PEEL18CV8
PAL10L8A	PEEL18CV8
PAL12H6A	PEEL18CV8
PAL12L6A	PEEL18CV8
PAL14H4A	PEEL18CV8
PAL14L4A	PEEL18CV8
PAL16H2A	PEEL18CV8
PAL16HD8A	PEEL18CV8

AMD ☞ ICT	
PAL16L2	PEEL18CV8
PAL16L8	PEEL18CV8
PAL16R4	PEEL18CV8
PAL16R6	PEEL18CV8
PAL16R8	PEEL18CV8
PAL16RP4	PEEL18CV8
PAL16RP6	PEEL18CV8
PAL16RP8	PEEL18CV8
PALC16L8	PEEL18CV8
PALC16R4	PEEL18CV8
PALC16R6	PEEL18CV8
PALC16R8	PEEL18CV8
PALC18U8	PEEL18CV8
PALCE16V8	PEEL18CV8
PAL20L8A	PEEL20CG10A
PAL20R4A	PEEL20CG10A
PAL20R6A	PEEL20CG10A
PAL20R8A	PEEL20CG10A

Atmel ☞ ICT	
AT22V10†	PEEL22CV10A

Cypress ☞ ICT	
PALC16L8	PEEL18CV8
PALC16R4	PEEL18CV8
PALC16R6	PEEL18CV8
PALC16R8	PEEL18CV8
PLDC18G8	PEEL18CV8
PALC20G10	PEEL20CG10A
PLDC20G10	PEEL20CG10A
PALC22V10†	PEEL22CV10A
PAL22V10†	PEEL22CV10A

Harris ☞ ICT	
HPL16LC8	PEEL18CV8
HPL16RC8	PEEL18CV8
HPL16RC6	PEEL18CV8
HPL16RC4	PEEL18CV8

Intel ☞ ICT	
5C031	PEEL18CV8
5C032	PEEL18CV8
85C220	PEEL18CV8
85C224	PEEL22CV10A

Lattice ☞ ICT	
GAL16V8A	PEEL18CV8
GAL16V8B	PEEL18CV8
GAL20V8A	PEEL20CG10A
GAL20V8B	PEEL20CG10A
GAL22V10†	PEEL22CV10A
GAL22V10B†	PEEL22CV10A

National ☞ ICT	
PAL10H8	PEEL18CV8
PAL10L8	PEEL18CV8
PAL12H6	PEEL18CV8
PAL12L6	PEEL18CV8
PAL14H4	PEEL18CV8
PAL14L4	PEEL18CV8
PAL16L2	PEEL18CV8
PAL16L8	PEEL18CV8
PAL16R8	PEEL18CV8
PAL16R6	PEEL18CV8
PAL16R4	PEEL18CV8
GAL16V8	PEEL18CV8
GAL16V8A	PEEL18CV8

PEEL Device Cross Reference (cont.) ❖

National ☞ ICT		Samsung ☞ ICT		TI ☞ ICT	
PAL12L10	PEEL20CG10A	CPL16L8	PEEL18CV8	TIBPAL16L8	PEEL18CV8
PAL14L8	PEEL20CG10A	CPL16R8	PEEL18CV8	TIBPAL16R8	PEEL18CV8
PAL16L6	PEEL20CG10A	CPL16R6	PEEL18CV8	TIBPAL16R6	PEEL18CV8
PAL18L4	PEEL20CG10A	CPL16R4	PEEL18CV8	TIBPAL16R4	PEEL18CV8
PAL20L2	PEEL20CG10A	CPL20L10	PEEL20CG10A	TIBPAL16L8	PEEL18CV8
PAL20L8	PEEL20CG10A	CPL20L8	PEEL20CG10A	TIBPAL16R8	PEEL18CV8
PAL20L10	PEEL20CG10A	CPL20R8	PEEL20CG10A	TIBPAL16R6	PEEL18CV8
PAL20P8	PEEL20CG10A	CPL20R4	PEEL20CG10A	TIBPAL16R4	PEEL18CV8
PAL20R8	PEEL20CG10A	CPL22V10†	PEEL22CV10A	TIBPAD16N8	PEEL18CV8
PAL20R6	PEEL20CG10A			TIBPAD16N8	PEEL18CV8
PAL20R4	PEEL20CG10A	**SGS-Thompson ☞ ICT**		TIBPAD18N8	PEEL18CV8
PAL20RP8	PEEL20CG10A	GAL16V8B	PEEL18CV8	EP330	PEEL18CV8
PAL20RP6	PEEL20CG10A	GAL16V8L	PEEL18CV8	TIBPAL20L10	PEEL20CG10A
PAL20RP4	PEEL20CG10A	GAL16V8Q	PEEL18CV8	TIBPAL20L8	PEEL20CG10A
GAL22V10†	PEEL22CV10A	GAL20V8	PEEL20CG10A	TIBPAL20R8	PEEL20CG10A
				TIBPAL20R6	PEEL20CG10A
Philips ☞ ICT				TIBPAL20R4	PEEL20CG10A
PLHS18P8A	PEEL18CV8			TIBPAL22V10†	PEEL22CV10A
PLHS22CV10A†	PEEL22CV10A			TICPAL22V10†	PEEL22CV10A

❖ PEEL devices may be used as direct replacements for the PLDs indicated without modifying the original design. The original design can be translated to an equivalent PEEL design by using ICT's JEDEC file translator provided free with ICT's PLACE Development software and available from ICT sales representatives and ICT technical support bulleton board.

† Devices marked with this symbol are JEDEC-file compatible with the PEEL device referenced. No translation is required to use a PEEL device as a direct replacement.

PEEL Arrays

Introduction to PEEL Array. 2-3
PA7024 -15, -20, -25 2-13
PA7024I -25 2-21
PA7128 -15, -20 2-27
PA7140 -20, -25 2-35

Introduction to PEEL™ Arrays

Features

- **Programmable Electrically Erasable Logic Arrays**
  - Family of medium-density CPLDs
  - Reprógrammable CMOS EEPROM Technology
  - 24 to 44 pins in DIP, PLCC, and SOIC packages
- **Versatile Logic Array Architecture**
  - PLA structure with true product-term sharing
  - Logic, registers, latches can be I/O buried
  - 40 to 60 registers/latches
  - 40 to 72 logic cell output functions
- **Most Flexible Logic Cell of all CPLDs**
  - Multiple output functions per cell
  - D,T and JK registers with special features
  - Independent or global clocks, resets, presets, clock polarity, and output enables
  - All controls allow sum-of-products logic
- **High-Speed Wide-gate Performance**
  - tpd as fast as 9ns/15ns (internal/external)
  - fmax as fast as 76.9MHz
- **Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications**
  - Integration of multiple PLDs and random logic
  - Buried counters, complex state-machines
  - Comparitors, decoders, multiplexers and other wide-gate functions
- **Development and Programmer Support**
  - Familiar PLD development methodology
  - ICT PLACE Development Software (free to qualified PLD designers)
  - Fitters for ABEL and CUPL PLD Software
  - Programming support by ICT PDS-3 and other popular 3rd party programmers

Overview

Programmable Electrically Erasable Logic (PEEL) Arrays are a family of Complex Programmable Logic Devices (CPLDs) based on ICT's CMOS EEPROM technology. PEEL Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and the speed needed for today's programmable logic designs.

The initial PEEL Array family consists of three parts in packages ranging from 24 to 44 pins in plastic DIP, PLCC, and SOIC formats. ICT's CMOS EE technology allows reprogramability and high-speed performance. Wide-gate delays as fast as 9ns for internal (buried) and 15ns external (pin to pin) are possible with PEEL Arrays. Clock frequencies can be as fast as 76.9MHz for sequential functions.

The PEEL Array architecture is based on a versatile multi-level logic array architecture rich in input latches, buried registers and sum-of-product logic functions. The basic logic array structure is similar to that of a PLA (programmable AND, programmable OR) allowing true product term sharing.

PEEL Arrays offer the most flexible logic and I/O cells of any CPLD available today. The unique PEEL Array logic cell incorporates multiple outputs allowing registers and combinatorial logic to be buried without limiting the use of I/O pins as with other CPLDs. Logic cell registers are user-configurable to be true D, T and JK registers with independent or global clocks, resets, presets, clock polarity and other special features. Additionally, all registers and output enables allow full sum-of-products control.

PEEL Arrays are ideal for implementing a wide variety of general purpose combinatorial, synchronous and asynchronous logic applications, including: buried counters, complex state-machines, comparitors, decoders, encoders, adders, address/data demux and other wide-gate logic. Because PEEL Arrays allow for multi-level buried logic, designs normally requiring multiple PLDs and/or random logic can be efficiently integrated.

Development support for PEEL Arrays is provided by ICT and popular third party development tool manufacturers. ICT offers the powerful PLACE Development Software (free to qualified PLD designers) complete with architectural editor, logic compiler, and waveform simulator. Development with ABEL and CUPL is accommodated by PEEL Array fitters from ICT. Programming for PEEL Arrays is supported by ICT's PDS-3 and other popular third party programmers.

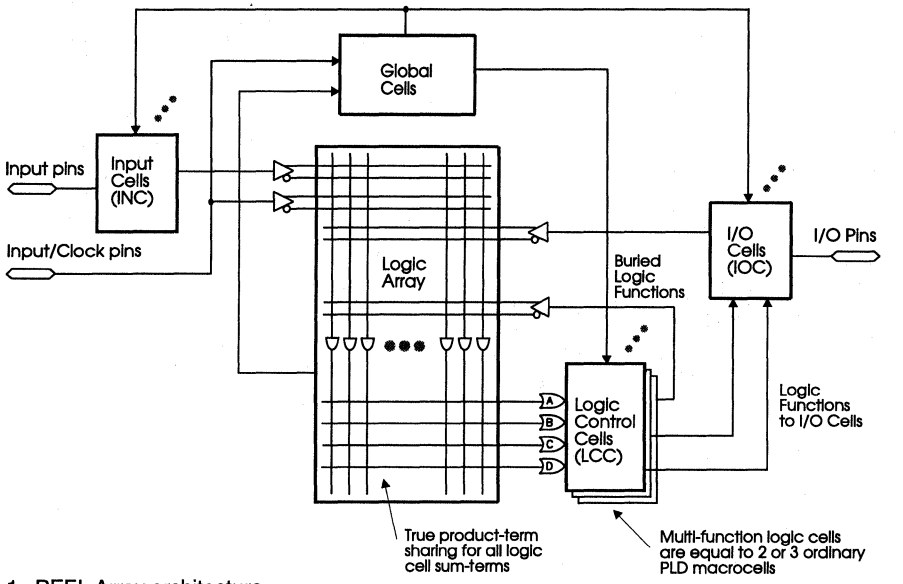


Figure 1. PEEL Array architecture

PEEL Array Architecture Overview

The primary elements of the PEEL Array architecture include I/O cells (IOCs), input cells (INCs), logic control cells (LCCs) and a logic array, as illustrated by the architecture diagram in figure 1.

Looking at the diagram, input signals to the PEEL Array are first fed through either I/O cells or inputs cells, each equipped with a user configured register/latch. The signals from the I/O and inputs cells, as well as feedbacks from the logic control cells are fed to the logic array with both true and compliments available. The logic array, which incorporates a PLA-like structure with true product term sharing, allows full sum-of-product logic functions to be fed (in groups of four) to each logic control cell.

The logic control cells allocate and control the sum-of-product functions to implement register and I/O cell functions like clocks, sets, presets and output enables as well as combinatorial and sequential output functions. PEEL Array logic cells provide multiple outputs (multi-function) that are equivalent to two or three macrocells of ordinary PLDs. The multiple outputs ensure that registers and logic functions can be buried and that I/Os can still be used for both inputs and outputs. Finally, the global cells allocate global clock signals and other register control functions for logic control cells and I/O cells.

The PEEL Array Family

The initial PEEL Array family includes three parts in packages ranging from 24 to 44 pins: the PA7024, PA7128, and PA7140. Although the basic architecture is similar, their resources vary relative to the number of inputs, I/Os, logic cells, and array size. The architectural variety of the family efficiently addresses a range of medium-density PLD applications.

The PA7024

Although smallest in pin count of the PEEL Arrays, the PA7024 is by far the most powerful 24-pin PLD today. With 20 I/O pins, 2 inputs/global-clock pins and 40 registers/latches, (20 LCC, 20 IOC) the PA7124 is suitable for a wide variety of applications, see figure 2. The PA7024's logic array provides 84 sum-of-product functions that share up to 80 product terms. It's multi-function logic cells have two outputs per cell for a total of 40 output functions (20 of which can be buried). To put this in perspective, the popular 22V10 has only 10 non-buried output functions. The PA7024 can implement designs that exceed the architectural capabilities of devices like the 22V10, 20RA10, EP610/630, ATV750, GAL6002, EPM5032. It is also a pin compatible super-set of most any 24-pin PLD. The PA7024 has propagation delays as fast as 10ns/15ns (internal/external) and synchronous clocking frequencies to 71.4MHz. Power consumption is 140mA max @ 25MHz (95mA typ.). PA7024 is available in 24 pin DIP, SOIC, and 28-pin PLCC.

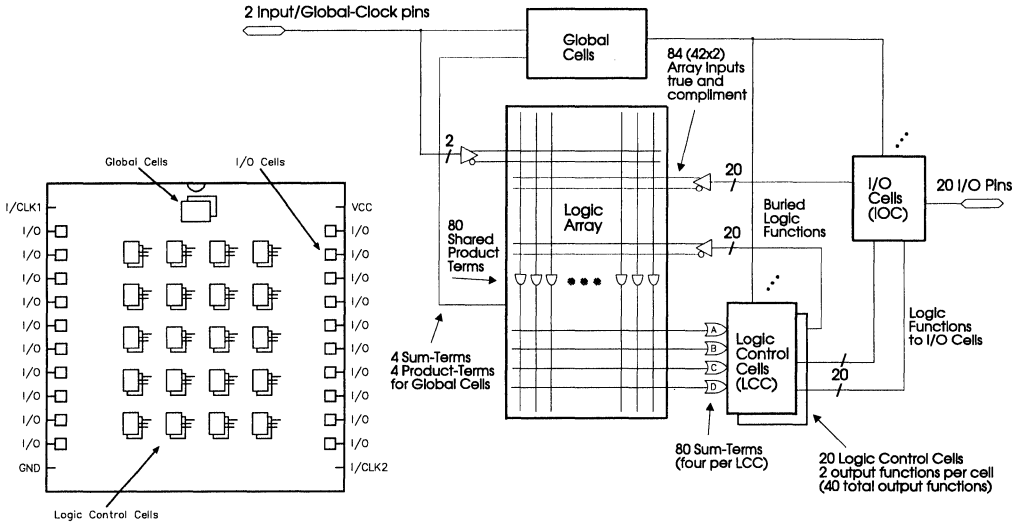


Figure 2. PA7024 block and architecture diagrams

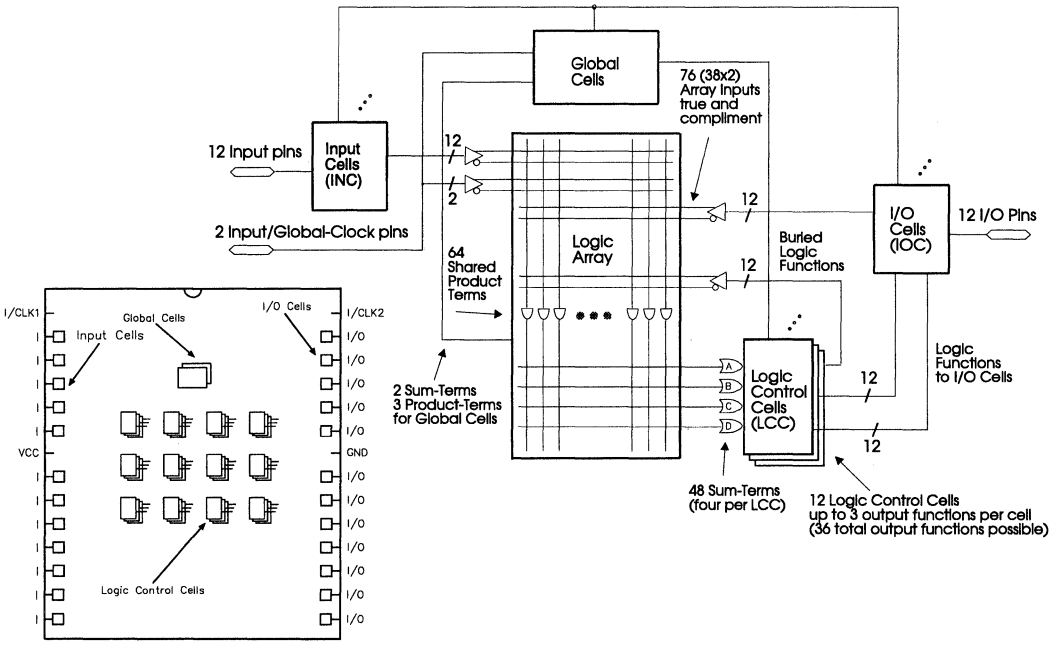


Figure 3. PA7128 block and architecture diagrams

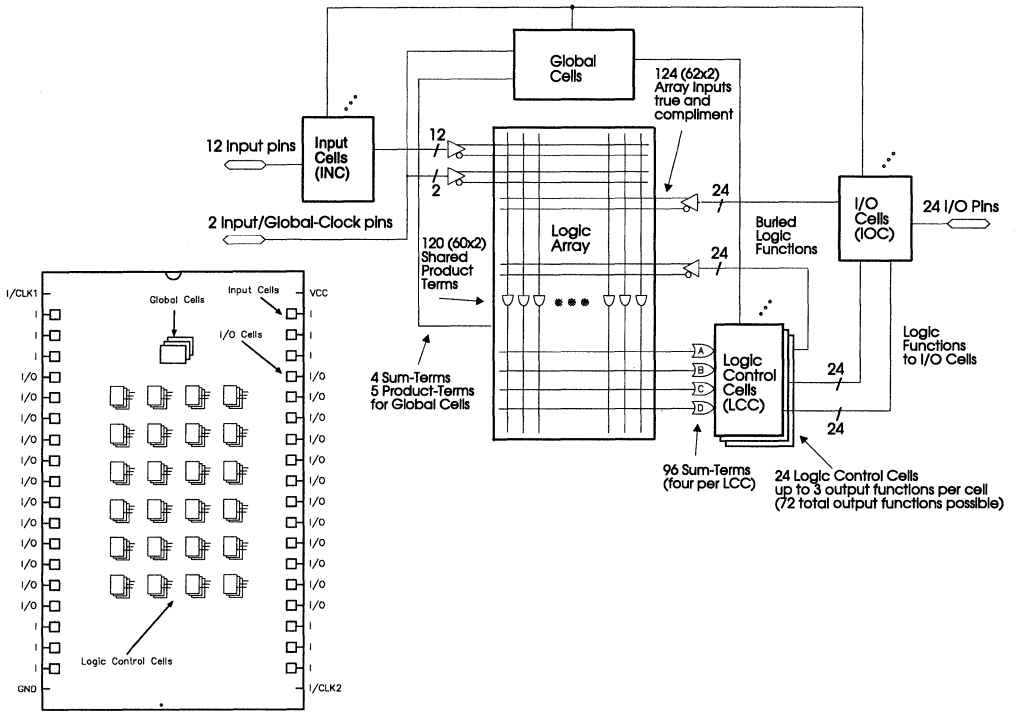


Figure 4. PA7140 architecture and block diagrams

The PA7128

With a slightly larger pin count and fewer logic cells than the PA7024, the PA7128 addresses applications requiring more inputs pins, fewer outputs pins and a lower cost. The PA7128 architecture consists of 12 I/O pins, 14 input pins and 36 registers/latches (12 LCC, 12 IOC, 12 INC), see figure 3.

The PA7128 logic array provides 50 sum-of-product logic functions that share 64 product terms. It's multi-function logic cells offer up to three outputs per cell for a total of 36 possible output functions (24 of which can be buried). An enhanced IOC cell allows for additional buried register capability. The PA7128 can implement designs that exceed the architectural capabilities of devices like the 26V12, 22V10, 20RA10, CY7C-330/331/332, ATV750, EPM5032 and EPM7032. It is also a pin compatible superset to several 28-pin PLDs. The PA7128 offers propagation delays as fast as 9ns/15ns (internal/external) and synchronous clocking frequencies to 76.9MHz. Power consumption is 135mA max @ 25MHz (90mA typ.). PA7128 is available in 28 pin DIP, PLCC and SOIC.

The PA7140

Offering more pin and logic density than the PA7024 or PA7128, the PA7140 architecture consists of 24 I/O pins, 14 input pins and 60 registers/latches (24 LCC, 24 IOC, 12 INC), see figure 4. The PA7140 logic array has 100 sum-of-product logic functions that can share up to 60 each of 120 product terms. The 24 LCC's are divided into two groups (group A and B) each with 12 LCC's. Each LCC group can fully share half (60) of the 120 product terms available for sum-of-product logic functions. As with the PA7128, the PA7140 multi-function logic cells offer up to three outputs per cell for a total of 72 possible output functions (48 of which can be buried). The PA7140 also has a special global cell feature to preload and unload buried registers for test purposes. The PA7140 can implement designs that exceed the architectural capabilities of devices like the Mach110/210, ATV2500, EPM7032, EPM5064 and EP910. The PA7140 offers propagation delays as fast as 13ns/20ns (internal/external) and synchronous clocking frequencies to 58.5MHz. Power consumption is 150mA max @ 25MHz (100mA typ.). The PA7140 is packaged in 40-pin DIP and 44-pin PLCC.

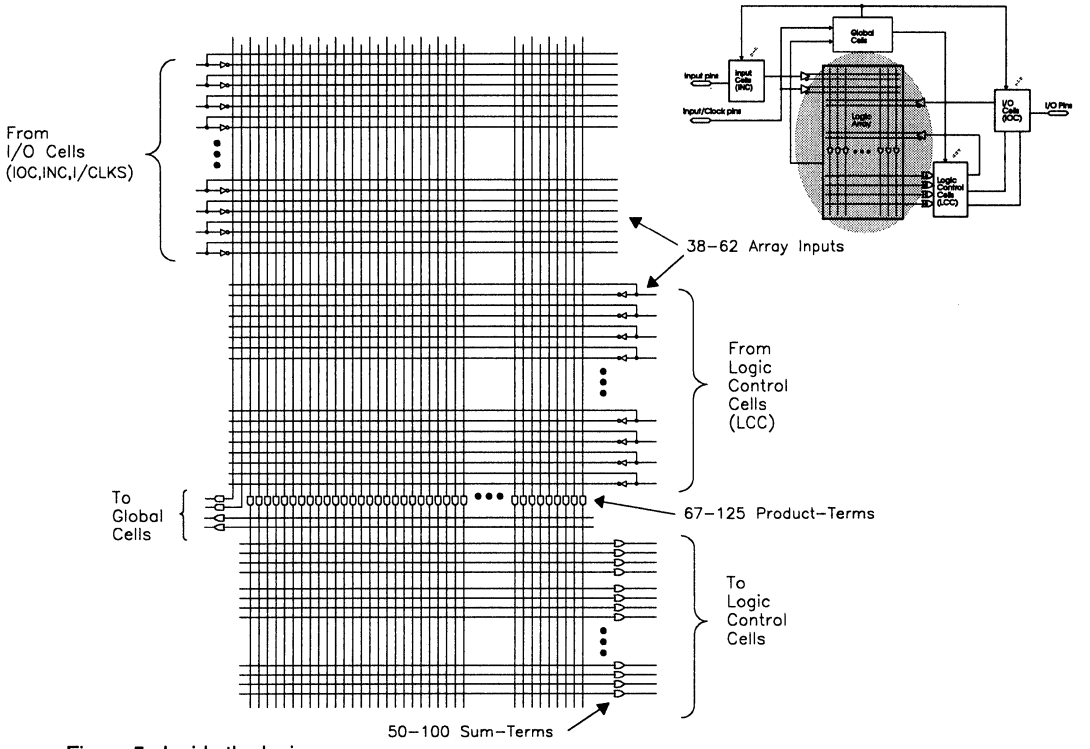


Figure 5. Inside the logic array

A Closer Look at the PEEL Array

Inside the Logic Array

The heart of the PEEL Array architecture is based on a logic array structure similar to that of a PLA (programmable AND, programmable OR). The logic array implements all logic functions and provides interconnection and control of the cells. Depending on the PEEL Array selected, a range of 38 to 62 inputs are available into the array from the I/O cells, inputs cells and input/global-clock pins.

All input signals provide both true and compliment signals and can be programmably connected to any product term in the array. The number of product-terms among PEEL Arrays range from 67 and 125. All product terms (with the exception of certain ones fed to the global cells) can be programmably connected to any of the sum-terms of the logic control cells (four sum-terms per logic control cell). Product-terms and sum-terms are also routed to the global cells for control purposes. Figure 5 shows a detailed view of the logic array structure.

True Product-Term Sharing

The PEEL logic array provides several advantages over common PLD logic arrays. First, it allows for true product-term sharing, not simply product-term steering, as commonly found in other CPLDs. Product term sharing ensures that product-terms, are used where they are needed and not left un-utilized or duplicated. Secondly, the sum-of-products functions provided to the logic cells can be used for clocks, resets, presets and output enables instead of just simple product-term control.

The PEEL logic array can also implement logic functions with many product terms with-in a single-level delay. For example a 16-bit comparitor needs 32 shared product terms to implement 16 exclusive-OR functions. The PEEL logic array easily handles this in a single level delay. Other PLDs/CPLDs either run out of product-terms or require expanders or additional logic levels that often slow performance and skew timing.

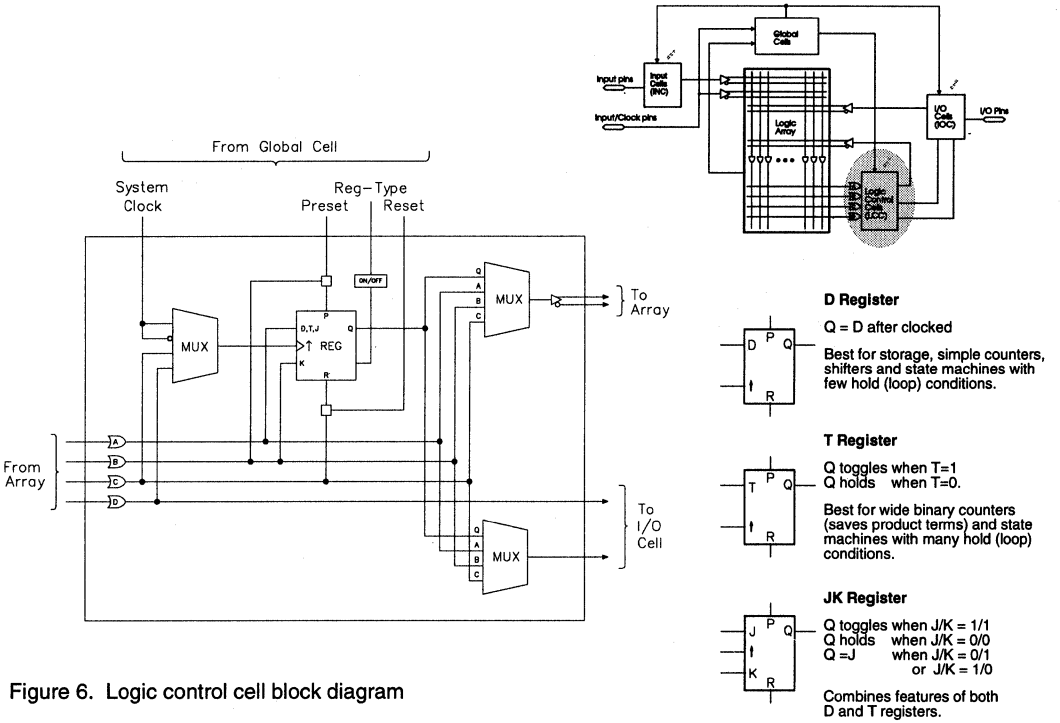


Figure 6. Logic control cell block diagram

Logic Control Cell (LCC)

Logic Control Cells (LCCs) are used to allocate and control the logic functions created in the logic array. Each LCC has four primary inputs and three outputs. The inputs to each LCC are complete sum-of-product logic functions from the array which can be used to implement combinatorial and sequential logic functions, and to control LCC registers and I/O cell output enables.

As shown in figure 6, the LCC is made up of three signal routing multiplexers and a versatile register with synchronous or asynchronous D, T, or JK registers (clocked-SR registers, which are a subset of JK, are also possible). EEPROM memory cells are used for programming the desired configuration. Four sum-of-product logic functions (SUM terms A, B, C and D) are fed into each LCC from the logic array. Each SUM term can be selectively used for multiple functions as listed below.

Sum-A = D, T, J or Sum-A
Sum-B = Preset, K or Sum-B
Sum-C = Reset, Clock, Sum-C
Sum-D = Clock, Output Enable, Sum-D

SUM-A can serve as the D, T, or J input of the register or a combinatorial path. SUM-B can serve as the K input, or the preset to the register, or a combinatorial path. SUM-C can be the clock, the reset to the register, or a combinatorial path. And, SUM-D can be the clock to the register, the output enable for the connected I/O cell, or an internal feedback node (7128, and 7140 only). Note that the sums controlling clocks, resets, presets and output enables are complete sum-of-product functions, not just product terms as with most other PLDs. This also means that any input or I/O pin can be used as a clock or other control function.

Several signals from the global cell are provided primarily for synchronous (global) registers control. The global cell signals are routed to all LCCs. These signals include a high speed clock of positive or negative polarity, global preset and reset, and a special register-type control that selectively allows dynamic switching of register type. This last feature is especially useful for saving product terms when implementing loadable counters and state machines by dynamically switching from D type register to load and T type register to count (see figure 9)

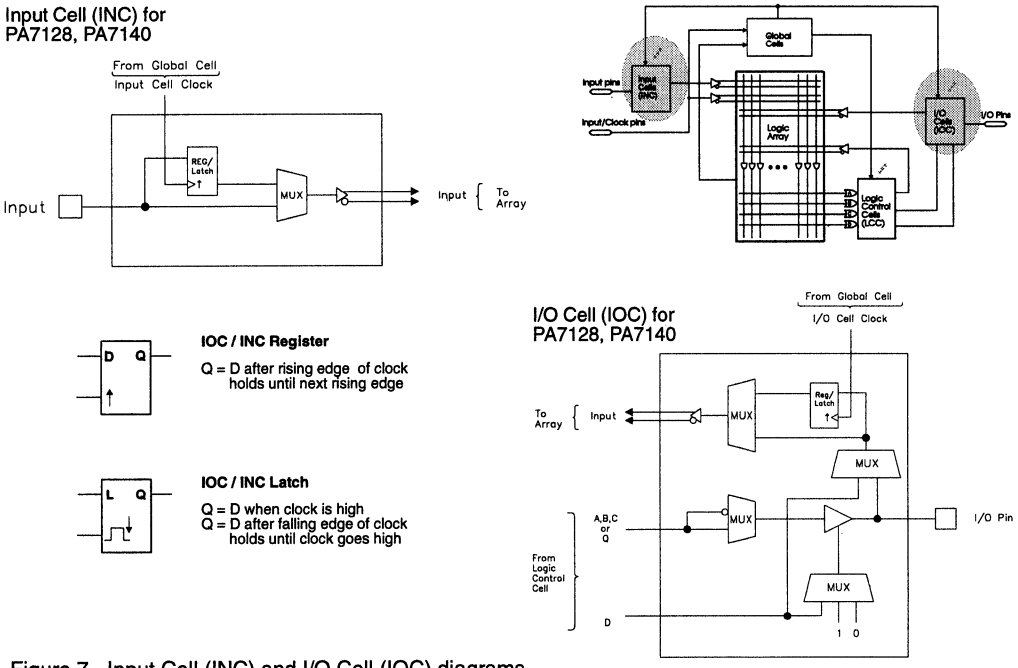


Figure 7. Input Cell (INC) and I/O Cell (IOC) diagrams

Multiple Outputs Per Logic Cell

An important feature of the logic control cell is its capability to have multiple outputs per cell each operating independently. As shown in figure 6, two of the three outputs can select the Q output from the register or the Sum A, B or C combinatorial paths. Thus, one LCC output can be registered, one combinatorial and the third, an output enable, or with the 7128 and 7140, an additional buried logic function. The multiple outputs make PEEL Array logic cells equivalent to two or three macrocells of other PLDs which have only one output per cell. It also allows registers to be truly buried from I/O pins without limiting them to input-only, (see figure 7 & 8)

Input Cells (INC)

Input cells (INCs) are included with the PA7128 and PA7140 only on dedicated inputs pins. The block diagram of the INC is shown in figure 7. Each INC consists of a multiplexer and a register/transparent latch which can be clocked from various sources selected by the global cell. The register is rising edge clocked. The latch is transparent when clock is high and latched on the clocks falling edge. The register/latch can also be bypassed for a non-registered input.

I/O Cell (IOC)

All PEEL Arrays have I/O cells (IOCs) as shown above in figure 7. Inputs to the IOCs can be fed from any of the LCCs in the array. Each IOC consists of routing and control multiplexers, an input register/ transparent latch, a three-state buffer and an output polarity control. The register/latch can be clocked from a variety of sources determined by the global cell. It can also be bypassed for a non-registered input. A feature of the 7128 and 7140 IOC is the use of SUM-D as a feed-back to the array when the I/O pin is a dedicated output. This allows for additional buried registers and logic paths. (see figure 7 & 8).

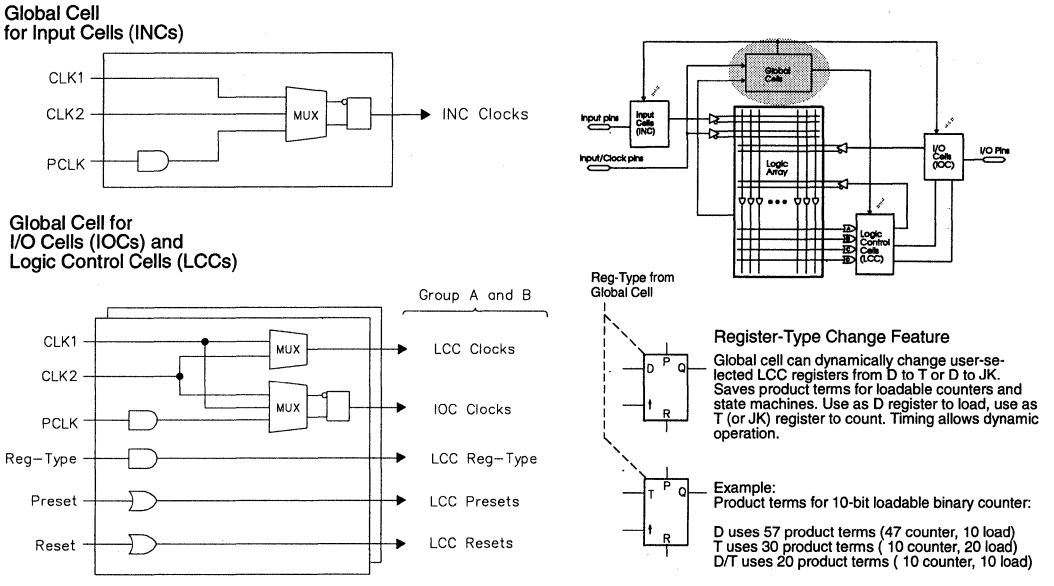
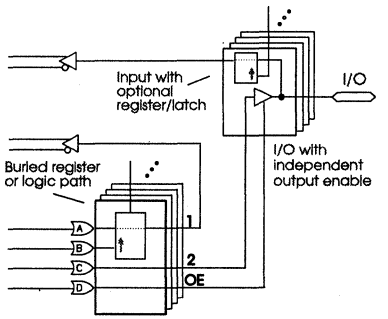
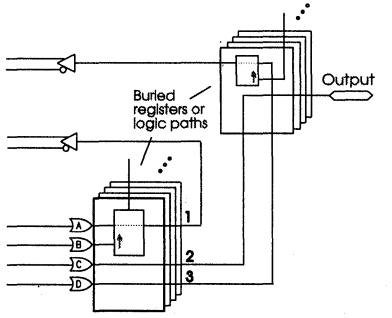


Figure 9. Global cell block diagrams



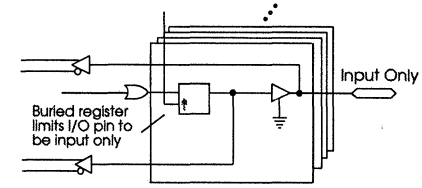
8a. PEEL Array LCC/IOC configured for two outputs/cell



8b. PEEL Array LCC/IOC configured for three outputs/cell

Global Cells

The global cells, shown in Figure 9, are used to direct global clock signals and/or control terms to the LCCs, IOCs and INCs. The global cells allow a clock to be selected from the CLK1 pin, CLK2 pin, or a product term from the logic array (PCLK). They also provide polarity control for INC and IOC clocks enabling rising or falling clock edges for input registers/latches. Note that each individual LCC clock has its own polarity control. The global cell for LCCs includes sum-of-products control terms for global reset and preset, and a fast product term control for LCC register-type, used to save product terms for loadable counters and state machines (see figure 8). If additional flexibility is needed, the PA7024 and PA7140 provides a second global cell that divides the LCC and IOCs into two groups, A and B. Half of the LCCs and IOCs use global cell A, half by global cell B. This means, for instance, two high speed global clocks can be used among the LCCs.



8c. Other PLDs with only one output per I/O macrocell

Figure 8a-c: PEEL Array multiple outputs/cell allow buried registers without limiting I/O to input only

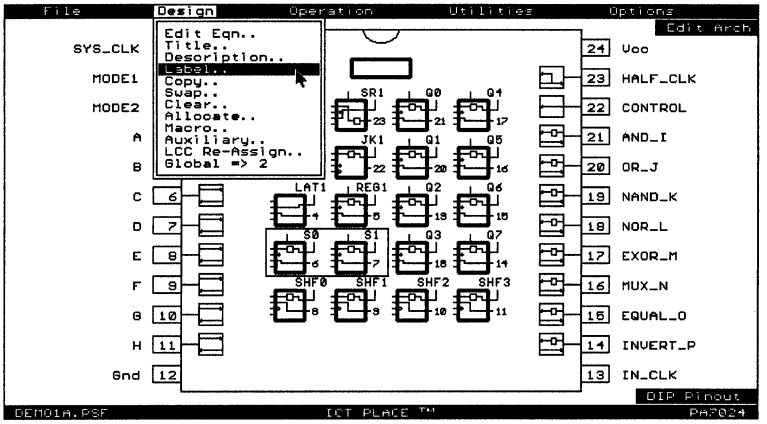


Figure 10a. PLACE Architectural Editor for PA7024

PEEL Array Development Support

Development support for PEEL Arrays is provided by ICT and manufacturers of popular development tools. ICT offers the powerful PLACE Development Software (free to qualified PLD designers).

The PLACE software includes an architectural editor, logic compiler, waveform simulator, documentation utility, and a programmer interface. The PLACE editor graphically illustrates and controls the PEEL Array's architecture, making the overall design easy to understand, while allowing the effectiveness of boolean logic equations, state machine design, and truth table entry. The PLACE compiler performs logic transformation and reduction making it possible to specify equations in most any fashion and fit the most logic possible in every design. PLACE also provides a multi-level logic simulator allowing external and internal signals to be simulated and analyzed via a waveform display. (see figure 10a-c)

PEEL Array development is also supported by popular development tools, such as ABEL and CUPL, via ICT's PEEL Array fitters. The fitters allow designers to use familiar tools, while making sure the description is properly mapped into the selected PEEL Array.

Programming

PEEL Arrays are EE-reprogrammable in all package types, plastic-DIP, PLCC, and SOIC. This makes them an ideal development vehicle for the lab. EE-reprogrammability is also useful for production, allowing unexpected changes to be made quickly and without waste. Programming of PEEL Arrays is supported by ICT's PDS-series programmers, as well as many other popular third party programmers.

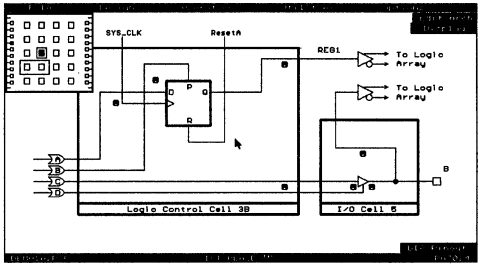


Figure 10b. PLACE LCC and IOC screen

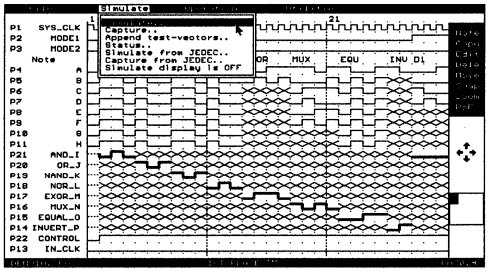
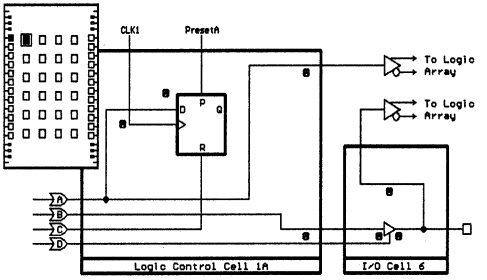


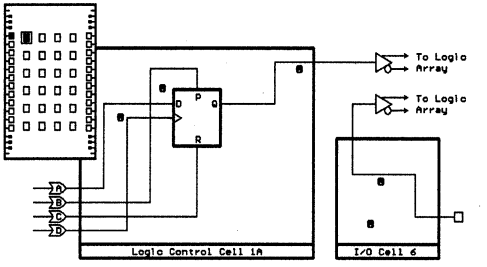
Figure 10c. PLACE waveform simulator screen

Design Security and Signature Word

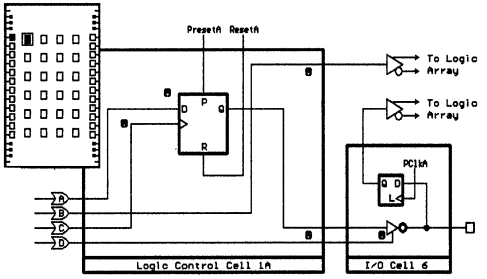
The PEEL Arrays provide a special EEPROM security bit that prevents unauthorized reading or copying of designs. Once set, the programmed bits of the PEEL Arrays can not be accessed until the entire chip has been electrically erased. Another programming feature, signature word, allows a user definable code to be programmed into the PEEL Array. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed in the device or to record the design revision.



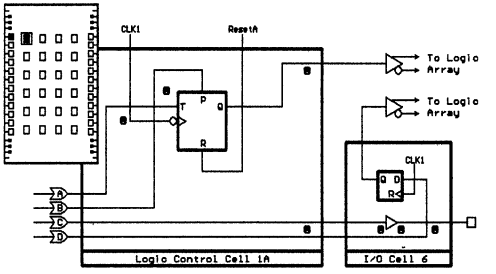
11a. Buried combinatorial and I/O



11b. D-Register (with clock, preset and reset) and input



11c. Buried combinatorial, D-registered I/O with latch



11d. 3 functions: buried T-reg., buried D-reg., and output

Figure 11. A few of over 8,000 possible LCC configurations

PEEL Array Applications

The unique combination of logic array speed and architectural flexibility let PEEL Arrays address a multitude of combinatorial, sequential and asynchronous applications. The versatile PEEL Array logic control cell is key to this flexibility offering over 8,000 possible user-selected configurations per cell (see figure 11).

Logic cells can be configured to support combinatorial functions like address decoders, encoders, multiplexers, comparitors, and adders. They also handle asynchronous random logic such as a D flip-flops (i.e., 7474) with independent clock reset and preset, SR latches and gated latches. Additionally, synchronous registered functions, like shifters, clock dividers, counters, and state machines are possible. Because PEEL Array registers have multiple outputs, buried counters and state machines with decode are easily supported (see figure 12).

Input latches add further flexibility allowing pipelined operation, direct demultiplexing and gated-strobing of address/data lines. Additionally, the number of registers and latches available for data storage, as well as tri-state I/Os, open many possibilities for bus interfaced sub-systems.

For more infomation on PEEL Array applications examples please refer to the PLACE Users Manual and the example design files provided with the PLACE software.

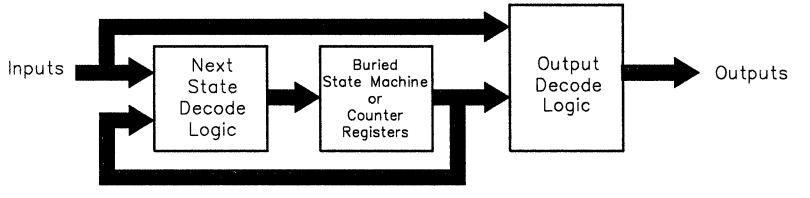


Figure 12. Buried counters and state machines

PA7024 PEEL™ Array
Programmable Electrically Erasable Logic Array

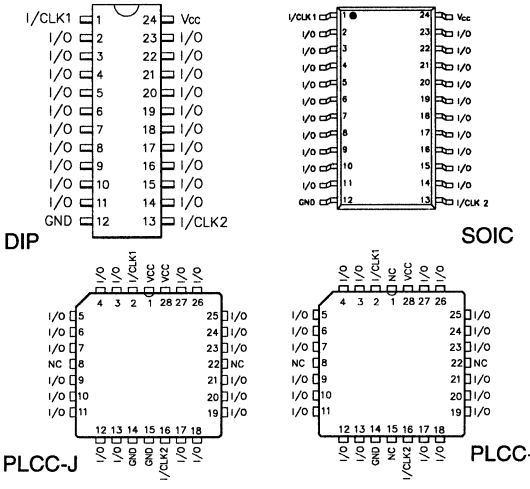
Features

- **CMOS Electrically Erasable Technology**
  - Reprogrammable in 24-pin DIP, SOIC, and 28-pin PLCC packages
- **Most Powerful 24-pin PLD Available**
  - 20 I/Os, 2 Inputs/clocks, 40 registers/latches
  - 40 logic cell output functions
  - PLA structure with true product-term sharing
  - Logic functions and registers can be I/O-buried
- **Flexible Logic Cell**
  - Multiple output functions per cell
  - D,T and JK registers with special features
  - Independent or global clocks, resets, presets, clock polarity, and output enables
  - Sum-of-products logic for output enables
- **High-Speed, Moderate Power Consumption**
  - As fast as 10ns/15ns (tpdi/tpdx), 71.4MHz fmax
  - ICC 140mA max, 95mA typical
- **Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications**
  - Integration of multiple PLDs and random logic
  - Buried counters, complex state-machines
  - Comparitors, decoders, multiplexers and other wide-gate functions
- **Development and Programmer Support**
  - ICT PLACE Development Software
  - Fitters for ABEL and CUPL design software
  - Programming support by ICT PDS-3 and other popular third-party programmers

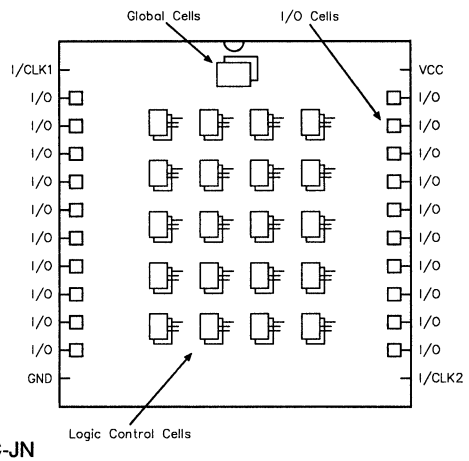
General Description

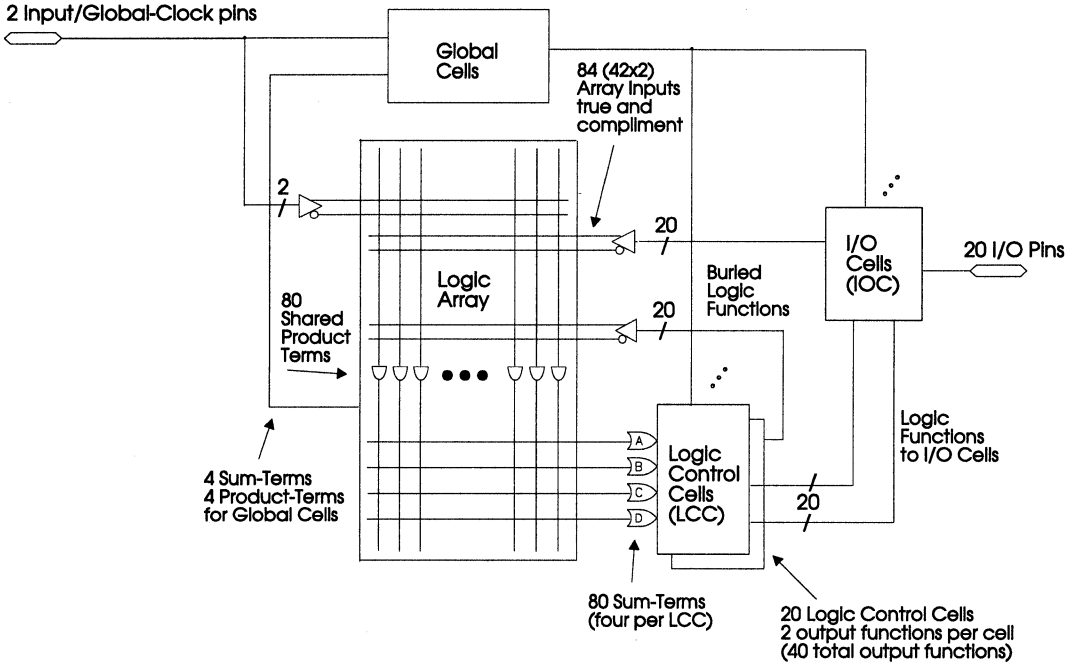
The PA7024 is a member of the Programmable Electrically Erasable Logic (PEEL) Array family based on ICT's CMOS EEPROM technology. PEEL Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and speed needed for today's programmable logic designs. The PA7024 is by far the most powerful 24-pin PLD available today with 20 I/O pins, 2 input/global-clocks, and 40 registers/latches (20 buried logic cells and 20 I/O reg/latches). Its logic array implements 84 sum-of-product logic functions that share 80 product terms. The PA7024s logic and I/O cells (LCCs, IOCs) are extremely flexible offering two output functions per logic cell (a total of 40 for all 20 logic cells). Logic cells are configurable as D, T and JK registers with independent or global clocks, resets, presets, clock polarity and other special features, making it suitable for a wide variety of combinatorial, synchronous and asynchronous logic applications. With pin compatibility and superset functionality to most 24-pin PLDs, (22V10, EP610/630, GAL6002), the PA7024 can implement designs that exceed the architectures of such devices. The PA7024 supports speeds as fast as 10ns/15ns (tpdi/tpdx) and 71.4MHz (fmax) at moderate power consumption 140mA (95mA typical). Packaging includes 24-pin DIP, SOIC, and 28-pin PLCC. Development and programming support for the PA7024 is provided by ICT and popular third-party development tool manufacturers.

Pin Configurations

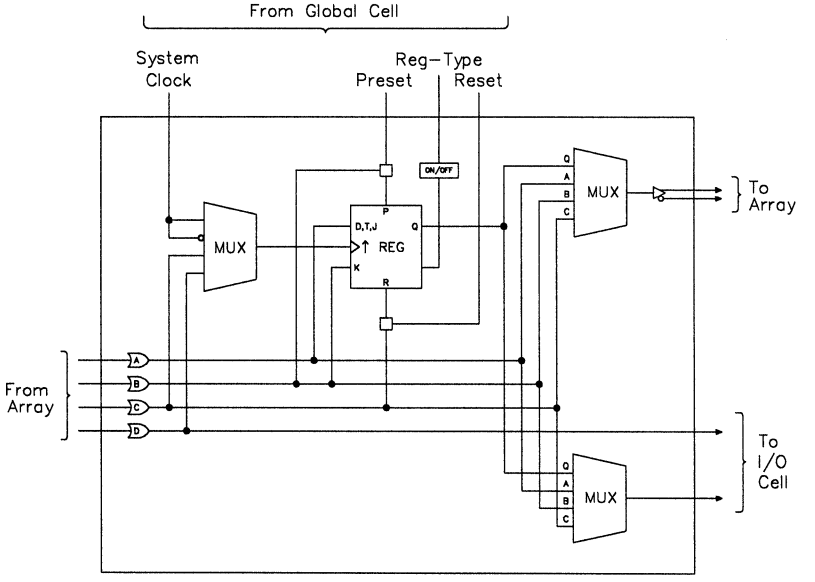


Block Diagram

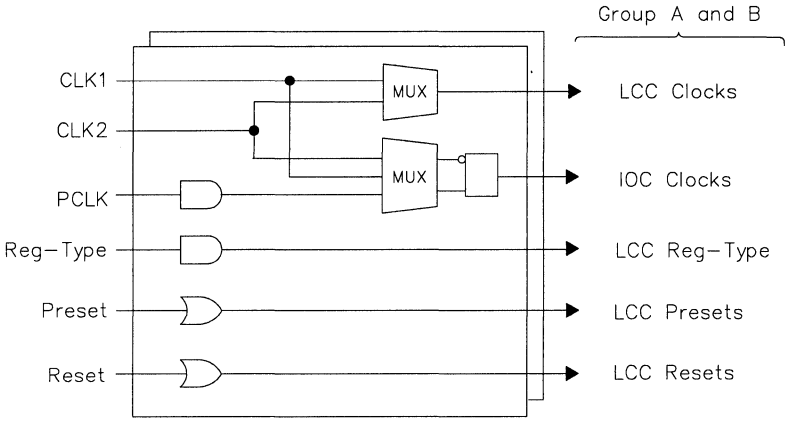




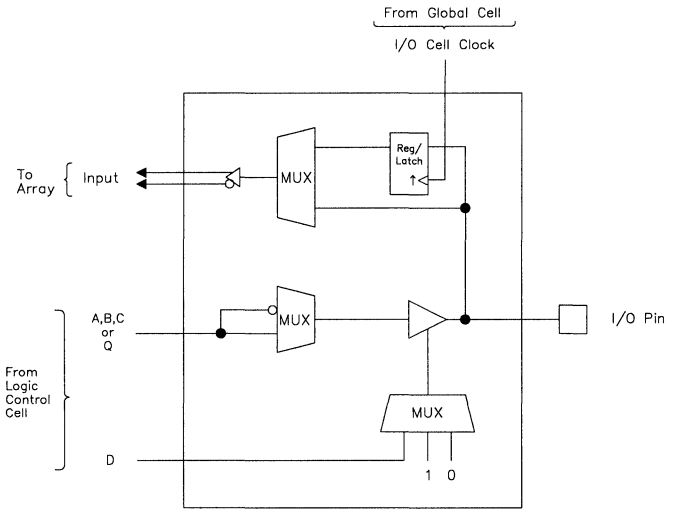
PA7024 Architecture Diagram



PA7024 Logic Control Cell



PA7024 Global Cell



PA7024 I/O Cell

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin	Relative to GND [1]	– 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		– 65 to + 150	°C
T_{LT}	Lead Temperature	(Soldering 10 seconds)	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+ 70	°C
T_R	Clock Rise Time	(Note 3)		20	ns
T_F	Clock Fall Time	(Note 3)		20	ns
T_{RVCC}	V_{CC} Rise Time	(Note 3)		250	ms

D.C. Electrical Characteristics

Over the operating range

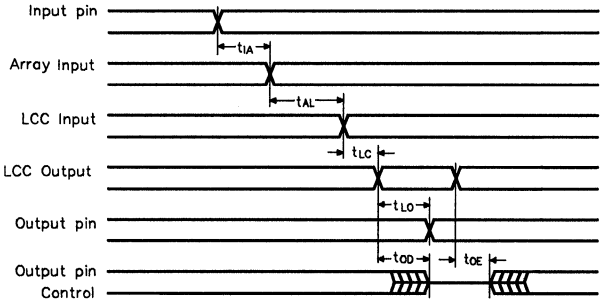
Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = – 4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = –10µA	V_{CC} – 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA		0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		– 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC}=Max, GND≤ V_{IN}≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O=High-Z, GND≤ V_O≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current[5]	V_{CC}=5V,V_O=0.5V, T_A=25°C	– 30	– 120	mA
I_{CC}	V_{CC} Current	V_{IN} = 0V or 3V [4, 12] f = 25MHz All outputs disabled		140 (typ.=95)[19]	mA
C_{IN}	Input Capacitance [6]	T_A=25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT}	Output Capacitance [6]			12	pF

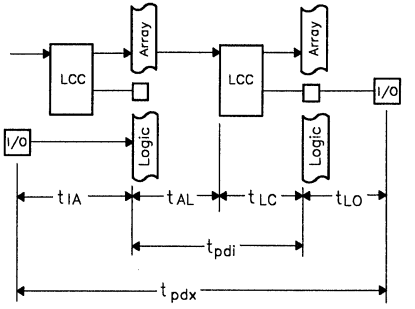
A.C. Electrical Characteristics Combinatorial

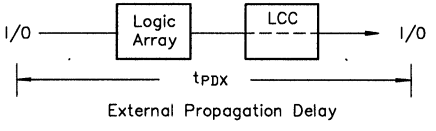
Over operating conditions

Symbol	Parameters [7, 13]	PA7024-15		PA7024-20 PA7024-1[18]		PA7024-25 PA7024-2[18]		Units
		Min	Max	Min	Max	Min	Max	
t_{PDI}	Propagation delay Internal (t_{AL}+ t_{LC})		10		13		17	ns
t_{PDX}	Propagation delay External (t_{IA}+ t_{AL}+ t_{LC}+ t_{LO})		15		20		25	ns
t_{IA}	Input or I/O pin to Array input		2		2		2	ns
t_{AL}	Array input to LCC		9		12		16	ns
t_{LC}	LCC input to LCC output [11]		1		1		1	ns
t_{LO}	LCC output to output pin		3		5		6	ns
t_{OD}, t_{OE}	Output Disable, Enable from LCC output [8]		3		5		6	ns
t_{OX}	Output Disable, Enable from input pin[8]		15		20		25	ns

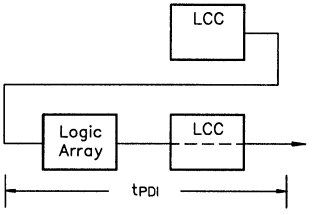
Combinatorial Timing - Waveforms and Block Diagram







External Propagation Delay



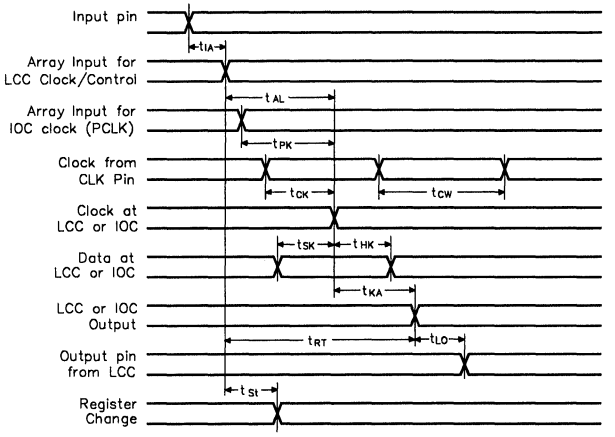
Internal Propagation Delay

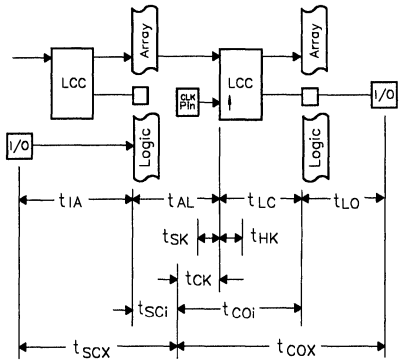
A.C. Electrical Characteristics Sequential

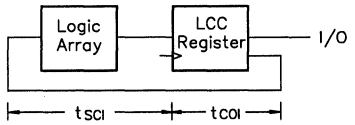
Over operating conditions

Symbol	Parameters [7, 13]	PA7024-15		PA7024-20 PA7024-1[18]		PA7024-25 PA7024-2[18]		Units
		Min	Max	Min	Max	Min	Max	
t_{SCI}	Internal set-up to system-clock[9] - LCC [15] (t_{AL}+ t_{SK}+ t_{LC} - t_{CK})	6		9		15		ns
t_{SCX}	Input [16] (Ext.) set-up to system-clock,-LCC(t_{IA}+ t_{SCI})	8		11		17		ns
t_{COI}	System-clock to Array Int. - LCC/IOC[15] (t_{CK} + t_{LC})		8		8		8	ns
t_{COX}	System-clock to Output Ext. - LCC (t_{COI}+ t_{LO})		12		13		13	ns
t_{HX}	Input hold time from system clock - LCC	0		0		0		ns
t_{SK}	LCC input set-up to async. clock [14] - LCC	3		3		4		ns
t_{AK}	Clock at LCC or IOC - LCC output	1		1		1		ns
t_{HK}	LCC input hold time from async. clock - LCC	4		4		4		ns
t_{SI}	Input set-up to system clock - IOC[15] (t_{SK} - t_{CK})	0		0		0		ns
t_{HI}	Input hold time from system clock - IOC (t_{CK} - t_{SK})	4		4		4		ns
t_{PK}	Array input to IOC PCLK clock		6		7		9	ns
t_{SPI}	Input set-up to PCLK clock - IOC (t_{SK} - t_{PK} - t_{IA}) [17]	0		0		0		ns
t_{HPI}	Input hold time from PCLK clock -IOC (t_{PK}+t_{IA}-t_{SK})[17]	5		6		7		ns
t_{CK}	System-clock delay to LCC and IOC		7		7		7	ns
t_{CW}	System-clock low or high pulse width	7		7		8		ns
f_{MAX1}	Max system-clock frequency Int/Int 1/(t_{SCI} + t_{COI})		71.4		58.8		43.5	MHz
f_{MAX2}	Max system-clock frequency Ext/Int 1/(t_{SCX} + t_{COI})		62.5		52.6		40.0	MHz
f_{MAX3}	Max system-clock frequency Int/Ext 1/(t_{SCI} + t_{COX})		55.5		45.5		35.7	MHz
f_{MAX4}	Max system-clock frequency Ext/Ext 1/(t_{SCX}+ t_{COX})		50.0		41.6		33.3	MHz
f_{TGL}	Max system-clock toggle frequency 1/(t_{CW} + t_{CW}) [10]		71.4		71.4		62.5	MHz
t_{PR}	LCC Preset/Reset to LCC output		1		1		2	ns
t_{ST}	Input to Global Cell preset/reset (t_{IA} + t_{AL} + t_{PR})		12		15		20	ns
t_{AW}	Asynch. preset/reset pulse width	8		8		8		ns
t_{RT}	Input to LCC Reg-Type (RT)		6		8		10	ns
t_{RTV}	LCC Reg-Type to LCC output register change		1		1		2	ns
t_{RTC}	Input to Global Cell register-type change (t_{RT} + t_{RTV})		7		9		12	ns
t_{RW}	Asynch. Reg-Type pulse width	10		10		10		ns
t_{RESET}	Power - on reset time for registers in clear state[3]		5		5		5	µs

Sequential Timing - Waveforms and Block Diagram

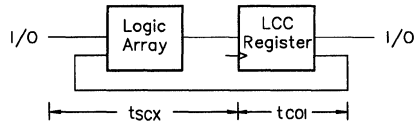






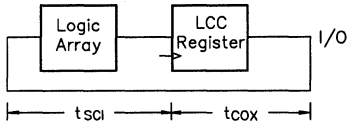
Internal Set–up, Internal Feedback (Int/Int)

$f_{MAX1} = 1/t_{SCI} + t_{COI}$



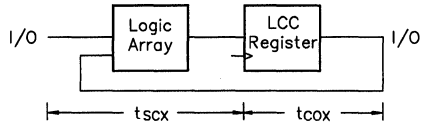
External Set–up, Internal Feedback (Ext/Int)

$f_{MAX2} = 1/t_{SCX} + t_{COI}$



Internal Set–up, External Feedback (Int/Ext)

$f_{MAX3} = 1/t_{SCI} + t_{COX}$



External Set–up, External Feedback (Ext/Ext)

$f_{MAX4} = 1/t_{SCX} + t_{COX}$

Notes:

1. Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
4. I/O pins are 0V or 3V.
5. Test one output at a time for a duration of less than 1 sec.
6. Capacitances are tested on a sample basis.
7. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
8. t_{OE} is measured from input transition to VREF ± 0.1V (See test loads at end of section 5 for VREF value). tOD is measured from input transition to VOH - 0.1V or VOL + 0.1V.
9. "System-clock" refers to pin 1 or pin 13 high speed clocks.
10. For T or JK registers in toggle (divide by 2) operation only.
11. For combinatorial and async-clock to LCC output delay.
12. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit D-type counter.
13. Test loads are specified at the end of section 3 in this data book.
14. "Async. clock" refers to the clock from the Sum term (OR gate).
15. The "LCC" term indicates that the timing parameter is applied to the LCC register.
    The "IOC" term indicates that the timing parameter is applied to the IOC register.
    The "LCC/IOC" term indicates that the timing parameter is applied to both the LCC and IOC registers.
16. The term "Input" without any reference to another term refers to an (external) input pin.
17. The parameter t_{SPI} indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of (t_{SK} - t_{PK} - t_{IA}). This means that no set-up time for the data from the pin or input is required, i.e. the external data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for t_{HPI} time, i.e. to wait for the PCLK signal to arrive at the IOC register.
18. PA7024-1 is an alternate number for PA7024-20.
    PA7024-2 is an alternate number for PA7024-25.
19. Typical (typ) ICC is measured at TA = 25°C, Freq = 25MHz, VCC = 5V.

PA7024I PEEL™ Array
Programmable Electrically Erasable Logic Array

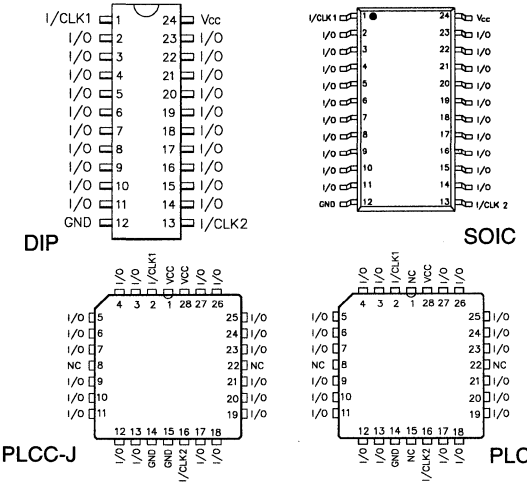
Features

- **Industrial Grade Specifications**
  - Vcc = 4.5V to 5.5V, TA = -40°C to +85°C
  - Reprogrammable 24-pin DIP, SOIC, and 28-pin PLCC packages
- **Most Powerful 24-pin PLD Available**
  - 20 I/Os, 2 Inputs/clocks, 40 registers/latches
  - 40 logic cell output functions
  - PLA structure with true product-term sharing
  - Logic functions and registers can be I/O-buried
- **Flexible Logic Cell**
  - Multiple output functions per cell
  - D,T and JK registers with special features
  - Independent or global clocks, resets, presets, clock polarity, and output enables
  - Sum-of-products logic for output enables
- **High-Speed, Moderate Power Consumption**
  - As fast as 17ns/25ns (tpdi/tpdx), 43.5MHz fmax
  - ICC 155mA max, 95mA typical
- **Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications**
  - Integration of multiple PLDs and random logic
  - Buried counters, complex state-machines
  - Comparitors, decoders, multiplexers and other wide-gate functions
- **Development and Programmer Support**
  - ICT PLACE Development Software
  - Fitters for ABEL and CUPL design software
  - Programming support by ICT PDS-3 and other popular third-party programmers

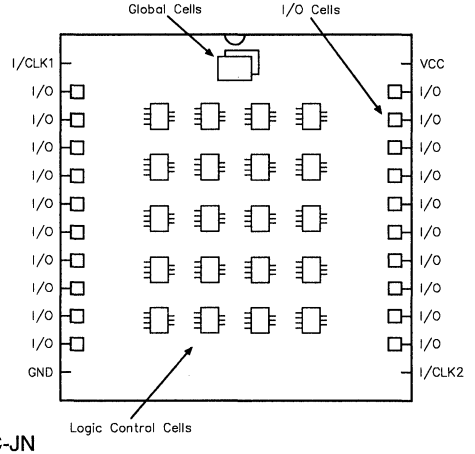
General Description

The PA7024I is an industrial grade version of the PA7024 Programmable Electrically Erasable Logic (PEEL) Array family based on ICT's 1-micron CMOS EEPROM technology. The PA7024 operates over the extended supply and temperature ranges needed for industrial applications. The PA7024I is functionally equivalent to the commercial grade PA7024 with 20 I/O pins, 2 input/global-clocks, and 40 registers/latches (20 buried logic cells and 20 I/O reg/latches). Its logic array implements 84 sum-of-product logic functions that share 80 product terms. The PA7024I logic and I/O cells (LCCs, IOCs) are extremely flexible offering two output functions per logic cell (a total of 40 for all 20 logic cells). Logic cells are configurable as D, T and JK registers with independent or global clocks, resets, presets, clock polarity and other special features, making it suitable for a wide variety of combinatorial, synchronous and asynchronous logic applications. With pin compatibility and super-set functionality to most 24-pin PLDs, (22V10, EP610/630, GAL6002) designs that exceed the architectures of such devices can be expanded upon. The PA7024I supports speeds as fast as 17ns/25ns (tpdi/tpdx) and 43.5MHz (fmax) at moderate power consumption 155mA (95mA typical). Packaging includes 24-pin DIP, SOIC, and 28-pin PLCC. Development and programming support for the PA7024I is provided by ICT and popular third-party development tool manufacturers.

Pin Configurations



Block Diagram



Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin	Relative to GND [1]	– 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		– 65 to + 150	°C
T_{LT}	Lead Temperature	(Soldering 10 seconds)	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Industrial [2]	4.5	5.5	V
T_A	Ambient Temperature	Industrial [2]	-40	+ 85	°C
T_R	Clock Rise Time	(Note 3)		20	ns
T_F	Clock Fall Time	(Note 3)		20	ns
T_{RVCC}	V_{CC} Rise Time	(Note 3)		250	ms

D.C. Electrical Characteristics

Over the operating range

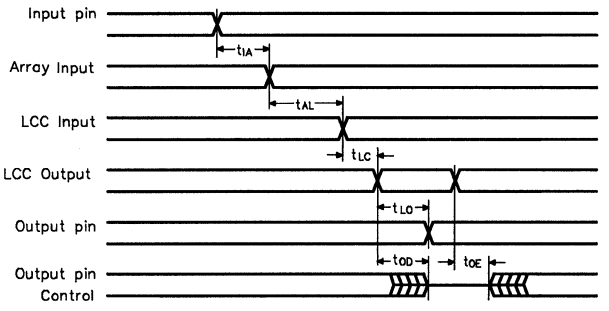
Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = – 4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = –10µA	V_{CC} – 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA		0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		– 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current [5]	V_{CC}=5V, V_O=0.5V, T_A=25°C	– 30	– 120	mA
I_{CC}	V_{CC} Current	V_{IN} = 0V or 3V [4, 12] f = 25MHz All outputs disabled		155 (typ=95) [19]	mA
C_{IN}	Input Capacitance [6]	T_A=25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT}	Output Capacitance [6]			12	pF

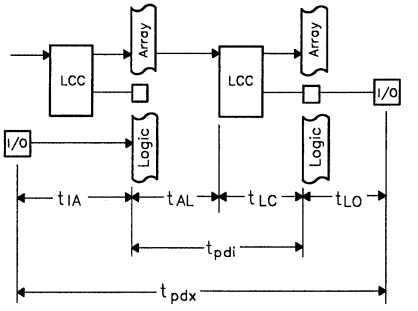
A.C. Electrical Characteristics Combinatorial

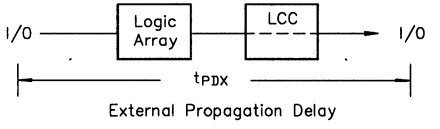
Over operating conditions

Symbol	Parameters[7, 13]	PA7024I-25 PA7024I-2[18]		Units
		Min	Max	
t_{PDI}	Propagation delay Internal (t_{AL}+ t_{LC})		17	ns
t_{PDX}	Propagation delay External (t_{IA}+ t_{AL}+ t_{LC}+ t_{LO})		25	ns
t_{IA}	Input or I/O pin to Array input		2	ns
t_{AL}	Array input to LCC		16	ns
t_{LC}	LCC input to LCC output [11]		1	ns
t_{LO}	LCC output to output pin		6	ns
t_{OD}, t_{OE}	Output Disable, Enable from LCC output [8]		6	ns
t_{OX}	Output Disable, Enable from input pin[8]		25	ns

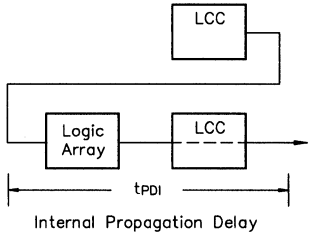
Combinatorial Timing - Waveforms and Block Diagram







External Propagation Delay



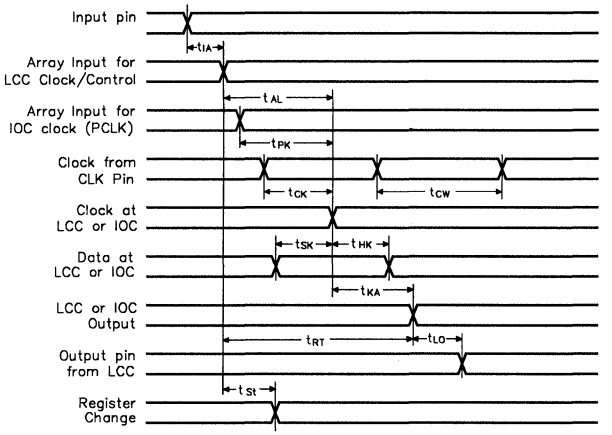
Internal Propagation Delay

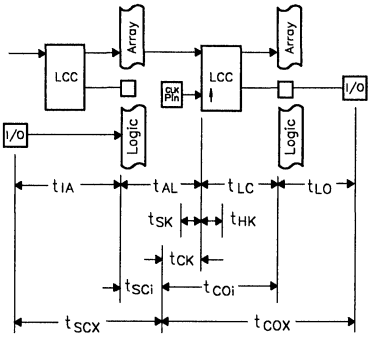
A.C. Electrical Characteristics Sequential

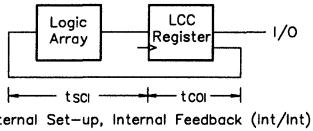
Over operating conditions

Symbol	Parameters [7, 13]	PA7024I-25 PA7024I-2[18]		Units
		Min	Max	
t_{SCI}	Internal set-up to system-clock[9] - LCC [15] (t_{AL}+ t_{SK}+ t_{LC} - t_{CK})	15		ns
t_{SCX}	Input [16] (Ext.) set-up to system-clock,-LCC(t_{IA}+ t_{SCI})	17		ns
t_{COI}	System-clock to Array Int. - LCC/IOC[15] (t_{CK} + t_{LC})		8	ns
t_{COX}	System-clock to Output Ext. - LCC (t_{COI}+ t_{LO})		13	ns
t_{HX}	Input hold time from system clock - LCC	0		ns
t_{SK}	LCC input set-up to async. clock [14] - LCC	4		ns
t_{AK}	Clock at LCC or IOC - LCC output	1		ns
t_{HK}	LCC input hold time from async. clock - LCC	4		ns
t_{SI}	Input set-up to system clock - IOC[15] (t_{SK} - t_{CK})	0		ns
t_{HI}	Input hold time from system clock - IOC (t_{CK} - t_{SK})	3		ns
t_{PK}	Array input to IOC PCLK clock		9	ns
t_{SPI}	Input set-up to PCLK clock - IOC (t_{SK} - t_{PK} - t_{IA}) [17]	0		ns
t_{HPI}	Input hold time from PCLK clock -IOC (t_{PK}+t_{IA}-t_{SK})[17]	7		ns
t_{CK}	System-clock delay to LCC and IOC		7	ns
t_{CW}	System-clock low or high pulse width	8		ns
f_{MAX1}	Max system-clock frequency Int/Int 1/(t_{SCI} + t_{COI})		43.5	MHz
f_{MAX2}	Max system-clock frequency Ext/Int 1/(t_{SCX} + t_{COI})		40.0	MHz
f_{MAX3}	Max system-clock frequency Int/Ext 1/(t_{SCI} + t_{COX})		35.7	MHz
f_{MAX4}	Max system-clock frequency Ext/Ext 1/(t_{SCX}+ t_{COX})		33.3	MHz
f_{TGL}	Max system-clock toggle frequency 1/(t_{CW} + t_{CW}) [10]		62.5	MHz
t_{PR}	LCC Preset/Reset to LCC output		2	ns
t_{ST}	Input to Global Cell preset/reset (t_{IA} + t_{AL} + t_{PR})		20	ns
t_{AW}	Asynch. preset/reset pulse width	8		ns
t_{RT}	Input to LCC Reg-Type (RT)		10	ns
t_{RTV}	LCC Reg-Type to LCC output register change		2	ns
t_{RTC}	Input to Global Cell register-type change (t_{RT} + t_{RTV})		12	ns
t_{RW}	Asynch. Reg-Type pulse width	10		ns
t_{RESET}	Power - on reset time for registers in clear state[3]		5	µs

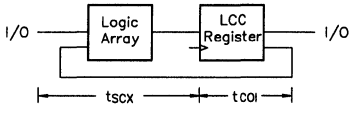
Sequential Timing - Waveforms and Block Diagram



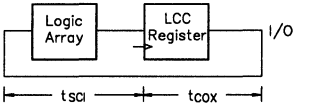




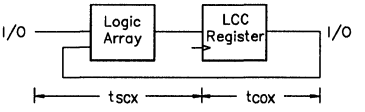
Internal Set–up, Internal Feedback (Int/Int)
$f_{MAX1} = 1/t_{SCI} + t_{COI}$



External Set–up, Internal Feedback (Ext/Int)
$f_{MAX2} = 1/t_{SCX} + t_{COI}$



Internal Set–up, External Feedback (Int/Ext)
$f_{MAX3} = 1/t_{SCI} + t_{COX}$



External Set–up, External Feedback (Ext/Ext)
$f_{MAX4} = 1/t_{SCX} + t_{COX}$

Notes:

1. Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
4. I/O pins are 0V or 3V.
5. Test one output at a time for a duration of less than 1 sec.
6. Capacitances are tested on a sample basis.
7. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
8. t_{OE} is measured from input transition to VREF ± 0.1V (See test loads at end of section 5 for VREF value). tOD is measured from input transition to VOH - 0.1V or VOL + 0.1V.
9. "System-clock" refers to pin 1 or pin 13 high speed clocks.
10. For T or JK registers in toggle (divide by 2) operation only.
11. For combinatorial and async-clock to LCC output delay.
12. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit D-type counter.
13. Test loads are specified at the end of section 3 in this data book.
14. "Async. clock" refers to the clock from the Sum term (OR gate).
15. The "LCC" term indicates that the timing parameter is applied to the LCC register.
    The "IOC" term indicates that the timing parameter is applied to the IOC register.
    The "LCC/IOC" term indicates that the timing parameter is applied to both the LCC and IOC registers.
16. The term "Input" without any reference to another term refers to an (external) input pin.
17. The parameter t_{SPI} indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of (t_{SK} - t_{PK} - t_{IA}). This means that no set-up time for the data from the pin or input is required, i.e. the external data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for t_{HPI} time, i.e. to wait for the PCLK signal to arrive at the IOC register.
18. PA7024-2 is an alternate number for PA7024I-20.
19. Typical (typ) ICC is measured at TA = 25°C, Freq = 25MHz, VCC = 5V.

PA7128 PEEL™ Array
Programmable Electrically Erasable Logic Array

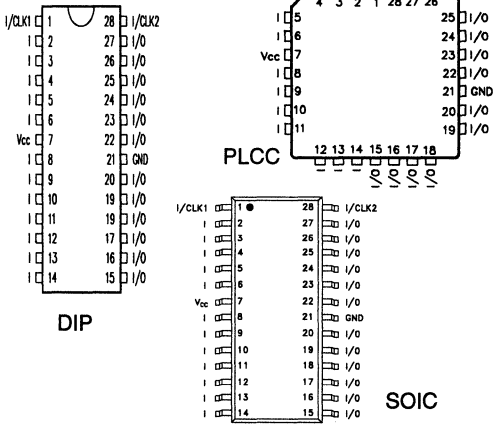
Features

- **CMOS Electrically Erasable Technology**
  - Reprogrammable in 28-pin DIP, SOIC, and PLCC packages
- **Versatile Logic Array Architecture**
  - 12 I/Os, 14 inputs, 36 registers/latches
  - Up to 36 logic cell output functions
  - PLA structure with true product-term sharing
  - Logic functions and registers can be I/O-buried
- **Flexible Logic Cell**
  - Up to 3 output functions per logic cell
  - D,T and JK registers with special features
  - Independent or global clocks, resets, presets, clock polarity, and output enables
  - Sum-of-products logic for output enables
- **High-Speed, Moderate Power Consumption**
  - As fast as 9ns/15ns (tpdi/tpdx), 76.9MHz fmax
  - ICC 135mA max, 90mA typical
- **Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications**
  - Integration of multiple PLDs and random logic
  - Buried counters, complex state-machines
  - Comparitors, decoders, multiplexers and other wide-gate functions
- **Development and Programmer Support**
  - ICT PLACE Development Software
  - Fitters for ABEL and CUPL design software
  - Programming support by ICT PDS-3 and other popular third-party programmers

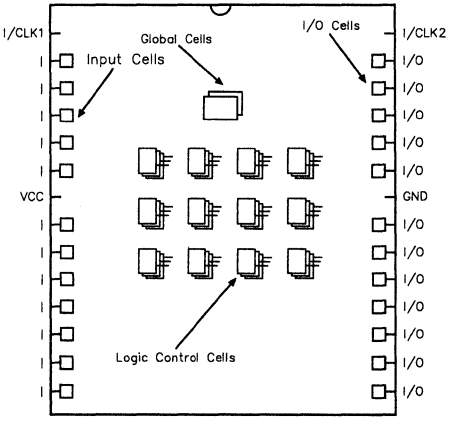
General Description

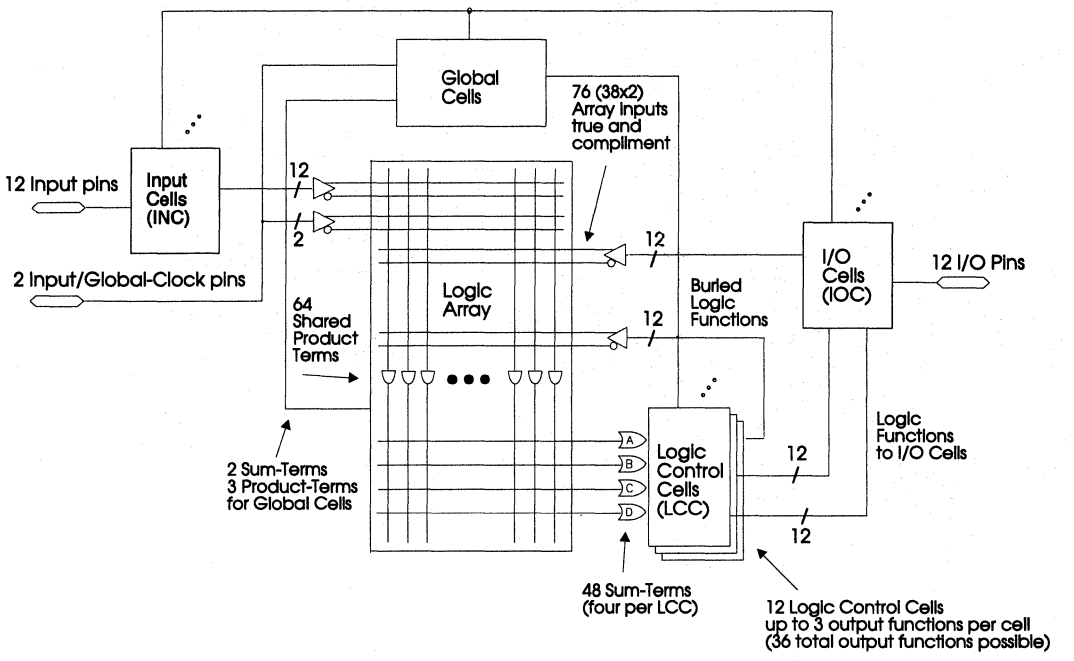
The PA7128 is a member of the Programmable Electrically Erasable Logic (PEEL) Array family based on ICT's 1-micron CMOS EEPROM technology. PEEL Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and speed needed for today's programmable logic designs. The PA7128 offers a versatile logic array architecture with 12 I/O pins, 14 inputs pins and 36 registers/latches (12 buried logic cells, 12 input reg/latches, 12 buried I/O reg/latches). Its logic array implements 50 sum-of-product logic functions that share 64 product terms. The PA7128's logic and I/O cells (LCCs, IOCs) are extremely flexible offering up to three output functions per cell (a total of 36 for all 12 logic cells). Cells are configurable as D, T and JK registers with independent or global clocks, resets, presets, clock polarity, and other special features, making the PA7128 suitable for a variety of combinatorial, synchronous and asynchronous logic applications. The PA7128 offers pin compatibility and super-set functionality to popular 28-pin PLDs, like the 26V12. Thus, designs that exceed the architectures of such devices can be expanded upon. The PA7128 supports speeds as fast as 9ns/15ns (tpdi/tpdx) and 76.9MHz (fmax) at moderate power consumption 135mA (90mA typical). Packaging includes 28-pin DIP, SOIC, and PLCC. Development and programming support for the PA7128 is provided by ICT and popular third party development tool manufacturers.

Pin Configurations

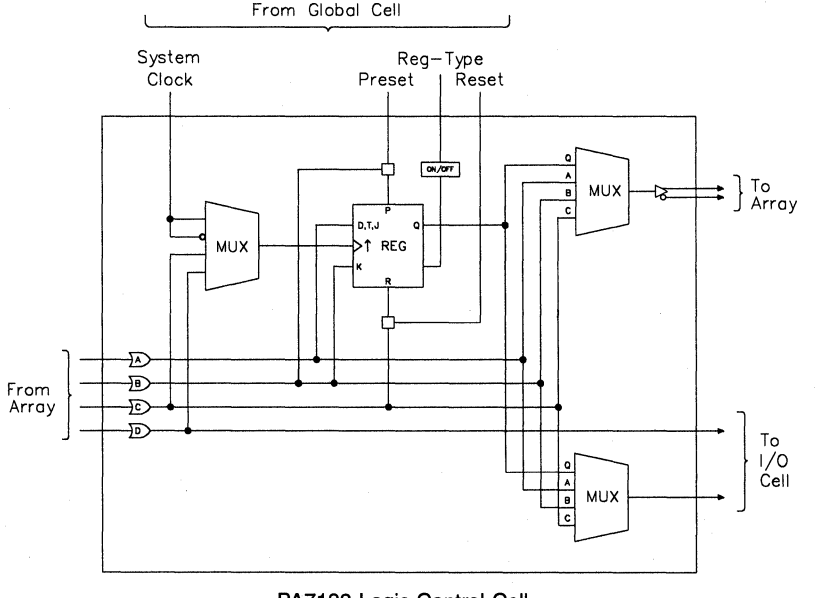


Block Diagram

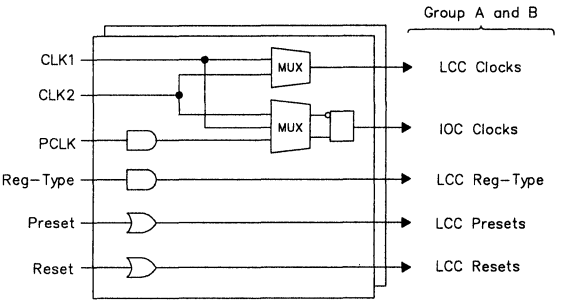




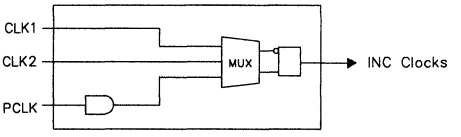
PA7128 Architecture Diagram



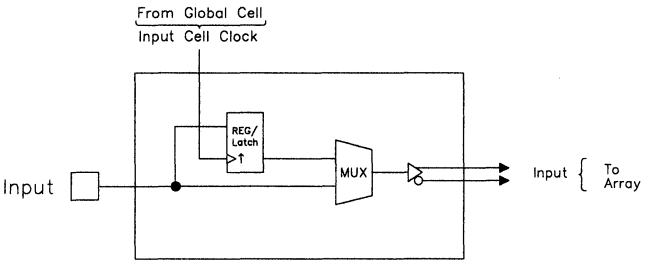
PA7128 Logic Control Cell



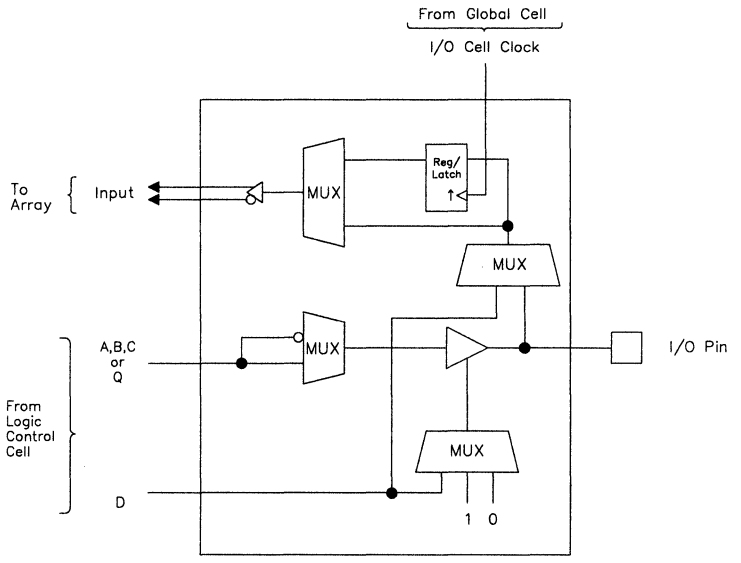
PA7128 Global Cell for LCCs and IOCs



PA7128 Global Cell for INCs



PA7128 Input Cell



PA7128 I/O Cell

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin	Relative to GND [1]	– 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		– 65 to + 150	°C
T_{LT}	Lead Temperature	(Soldering 10 seconds)	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+ 70	°C
T_R	Clock Rise Time	(Note 3)		20	ns
T_F	Clock Fall Time	(Note 3)		20	ns
T_{RVCC}	V_{CC} Rise Time	(Note 3)		250	ms

D.C. Electrical Characteristics

Over the operating range

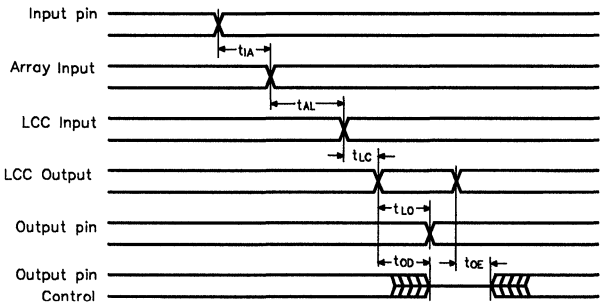
Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = – 4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = –10µA	V_{CC} – 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA		0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		– 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current [5]	V_{CC}=5V, V_O=0.5V, T_A=25°C	– 30	– 120	mA
I_{CC}	V_{CC} Current	V_{IN} = 0V or 3V f = 25MHz All outputs disabled		135 (typ=90) [20]	mA
C_{IN}	Input Capacitance [6]	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT}	Output Capacitance [6]			12	pF

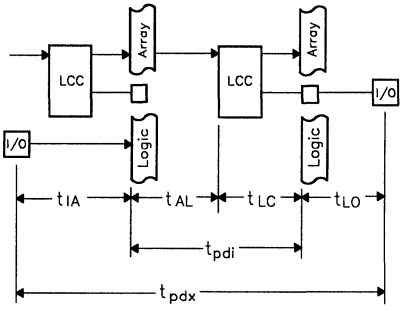
A.C. Electrical Characteristics Combinatorial

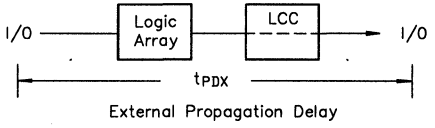
Over operating conditions

Symbol	Parameters [7, 13]	PA7128-15 PA7128-1[18]		PA7128-20 PA7128-2[18]		Units
		Min	Max	Min	Max	
t_{PDI}	Propagation delay Internal (t_{AL}+ t_{LC})		9		12	ns
t_{PDX}	Propagation delay External (t_{IA}+ t_{AL}+ t_{LC}+ t_{LO})		15		20	ns
t_{IA}	Input or I/O pin to Array input		2		3	ns
t_{AL}	Array input to LCC		8		10	ns
t_{LC}	LCC input to LCC output [11]		1		2	ns
t_{LO}	LCC output to output pin		4		5	ns
t_{OD}, t_{OE}	Output Disable, Enable from LCC output [8]		4		5	ns
t_{OX}	Output Disable, Enable from input pin[8]		15		20	ns

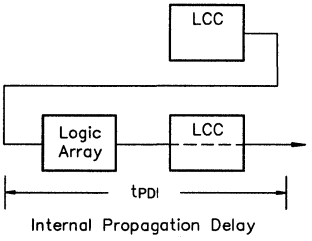
Combinatorial Timing - Waveforms and Block Diagram







External Propagation Delay



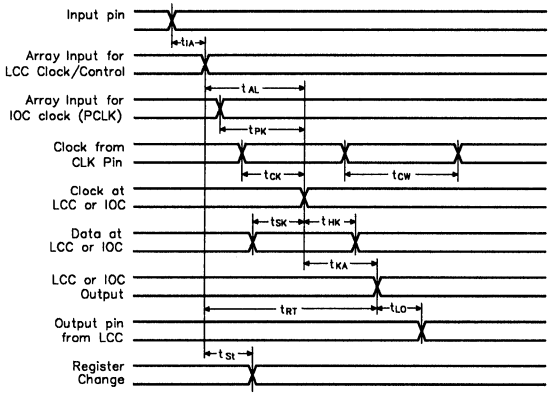
Internal Propagation Delay

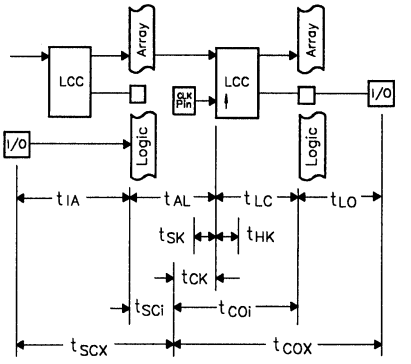
A.C. Electrical Characteristics Sequential

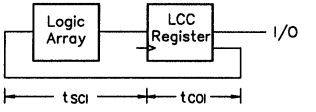
Over operating conditions

Symbol	Parameters [7, 13]	PA7128-15 PA7128-1[18]		PA7128-20 PA7128-2[18]		Units
		Min	Max	Min	Max	
t_{SCI}	Internal set-up to system-clock[9] , - LCC [15] (t_{AL}+ t_{SK}+ t_{LC} - t_{CK})	6		9		ns
t_{SCX}	Input [17] (Ext.) set-up to system-clock,-LCC(t_{IA}+ t_{SCI})	8		12		ns
t_{COI}	System-clock to Array Int.-LCC/IOC/INC[15] (t_{CK}+ t_{LC})		7		9	ns
t_{COX}	System-clock to Output Ext. - LCC (t_{COI}+ t_{LO})		11		14	ns
t_{HX}	Input hold time from system clock - LCC	0		0		ns
t_{SK}	LCC input set-up time to async. clock [14] - LCC	3		4		ns
t_{AK}	Clock at LCC or IOC - LCC output	1		1		ns
t_{HK}	LCC input hold time from async. clock - LCC	4		4		ns
t_{SI}	Input set-up to system clock -IOC/INC[15] (t_{SK} - t_{CK})	0		0		ns
t_{HI}	Input hold time from system clock -IOC/INC(t_{CK}-t_{SK})	3		3		ns
t_{PK}	Array input to IOC PCLK clock		6		7	ns
t_{SPI}	Input set-up to PCLK clock - IOC/INC (t_{SK}-t_{PK}-t_{IA})[19]	0		0		ns
t_{HPI}	Input hold PCLK clock [18]- IOC/INC (t_{PK} + t_{IA} - t_{SK})	5		7		ns
t_{SD}	Input set-up to system clock (t_{IA} + t_{AL} + t_{LC} + t_{SK} - t_{CK}) - IOC Sum-D [16]	8		12		ns
t_{HD}	Input hold time from system clock - IOC Sum-D	0		0		ns
t_{SDP}	Input set-up to PCLK clock (t_{IA} + t_{AL} + t_{LC} + t_{SK} - t_{PK}) - IOC Sum-D	4		5		ns
t_{HDP}	Input hold time from PCLK clock - IOC Sum-D	0		0		ns
t_{CK}	System-clock delay to LCC/IOC/INC		6		7	ns
t_{CW}	System-clock low or high pulse width	6		7		ns
f_{MAX1}	Max system-clock frequency Int/Int 1/(t_{SCI} + t_{COI})		76.9		55.6	MHz
f_{MAX2}	Max system-clock frequency Ext/Int 1/(t_{SCX} + t_{COI})		66.7		47.6	MHz
f_{MAX3}	Max system-clock frequency Int/Ext 1/(t_{SCI} + t_{COX})		58.8		43.5	MHz
f_{MAX4}	Max system-clock frequency Ext/Ext 1/(t_{SCX}+ t_{COX})		52.6		38.5	MHz
f_{TGL}	Max system-clock toggle frequency 1/(t_{CW} + t_{CW}) [10]		83.3		71.4	MHz
t_{PR}	LCC Preset/Reset to LCC output		1		2	ns
t_{ST}	Input to Global Cell preset/reset (t_{IA} + t_{AL} + t_{PR})		11		14	ns
t_{AW}	Asynch. preset/reset pulse width	8		8		ns
t_{RT}	Input to LCC Reg-Type (RT)		7		9	ns
t_{RTV}	LCC Reg-Type to LCC output register change		1		2	ns
t_{RTC}	Input to Global Cell reg.-type change (t_{RT} + t_{RTV})		8		11	ns
t_{RW}	Asynch. Reg-Type pulse width	10		10		ns
t_{reset}	Power-on reset time for register in clear state[3]		5		5	µs

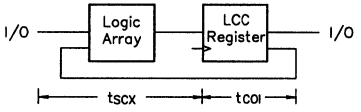
Sequential Timing - Waveforms and Block Diagram



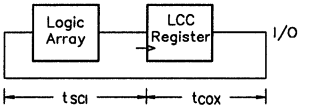




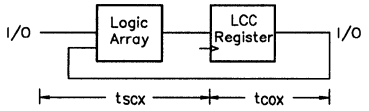
Internal Set–up, Internal Feedback (Int/Int)
$f_{MAX1} = 1/t_{SCI} + t_{COI}$



External Set–up, Internal Feedback (Ext/Int)
$f_{MAX2} = 1/t_{SCX} + t_{COI}$



Internal Set–up, External Feedback (Int/Ext)
$f_{MAX3} = 1/t_{SCI} + t_{COX}$



External Set–up, External Feedback (Ext/Ext)
$f_{MAX4} = 1/t_{SCX} + t_{COX}$

Notes:

1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
4. I/O pins are 0V or 3V.
5. Test one output at a time for a duration of less than 1 sec.
6. Capacitances are tested on a sample basis.
7. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
8. t_{OE} is measured from input transition to VREF ± 0.1V (See test loads at end of section 5 for VREF value). tOD is measured from input transition to VOH - 0.1V or VOL + 0.1V.
9. "System-clock" refers to pin 1 or pin 28 high speed clocks.
10. For T or JK registers in toggle (divide by 2) operation only.
11. For combinatorial and async-clock to LCC output delay.
12. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit D type Counter.
13. Test loads are specified at the end of section 3 in this data book.
14. "Async. clock" refers to the clock from the Sum term (OR gate)
15. The "LCC" term indicates that the timing parameter is applied to the LCC register.
    The "IOC" term indicates that the timing parameter is applied to the IOC register.
    The "INC" term indicates that the timing parameter is applied to the INC register.
    The "IOC/INC" term indicates that the timing parameter is applied to both the IOC and INC registers.
    The "LCC/IOC/INC" term indicates that the timing parameter is applied to the LCC, IOC and INC registers.
16. This refers to the Sum-D gate routed to the IOC register for an additional buried register.
17. The term "Input" without any reference to another term refers to an (external) input pin.
18. PA7128-1 is an alternate number for PA7128-15. PA7128-2 is an alternate number for PA7128-20.
19. The parameter t_{SPI} indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of (t_{SK} - t_{PK} - t_{IA}). This means that no set-up time for the data from the pin or input is required, i.e. the external data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for t_{HPI} time, i.e. to wait for the PCLK signal to arrive at the IOC register.
20. Typical (typ) ICC is measured at TA = 25°C, Freq = 25MHz, VCC = 5V.

PA7140 PEEL™ Array
Programmable Electrically Erasable Logic Array

Features

- **CMOS Electrically Erasable Technology**
  - Reprogrammable in 40-pin DIP and 44-pin PLCC packages
- **Versatile Logic Array Architecture**
  - 24 I/Os, 14 inputs, 60 registers/latches
  - Up to 72 logic cell output functions
  - PLA structure with true product-term sharing
  - Logic functions and registers can be I/O-buried
- **Flexible Logic Cell**
  - Up to 3 output functions per logic cell
  - D,T and JK registers with special features
  - Independent or global clocks, resets, presets, clock polarity, and output enables
  - Sum-of-products logic for output enables
- **High-Speed, Moderate Power Consumption**
  - As fast as 13ns/20ns (tpdi/tpd), 58.5MHz fmax
  - ICC 150mA max, 100mA typical
- **Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications**
  - Integration of multiple PLDs and random logic
  - Buried counters, complex state-machines
  - Comparitors, decoders, multiplexers and other wide-gate functions
- **Development and Programmer Support**
  - ICT PLACE Development Software
  - Fitters for ABEL and CUPL design software
  - Programming support by ICT PDS-3 and other popular 3rd party programmers

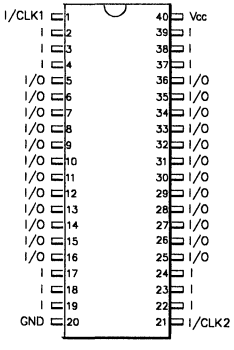
General Description

The PA7140 is a member of the Programmable Electrically Erasable Logic (PEEL) Array family based on ICT's 1-micron CMOS EEPROM technology. PEEL Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and speed needed for today's programmable logic designs. The PA7140 offers a versatile logic array architecture with 24 I/O pins, 14 inputs pins and 60 registers/latches (12 buried logic cells, 12 input reg/latches, 12 buried I/O reg/latches). Its logic array implements 100 sum-of-product logic functions divided into two groups each serving 12 logic cells. Each group shares half (60) of the 120 product-terms available for logic cells.

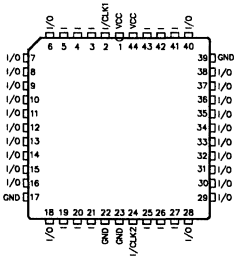
The PA7140's logic and I/O cells (LCCs, IOCs) are extremely flexible with up to three output functions per cell (a total of 72 for all 24 logic cells). Cells are configurable as D, T and JK registers with independent or global clocks, resets, presets, clock polarity, and other features, making the PA7140 suitable for a variety of combinatorial, synchronous, and asynchronous logic applications. The PA7140 supports speeds as fast as 13ns/20ns (tpdi/tpdx) and 58.5MHz (fmax) at moderate power consumption 150mA (100mA typical). Packaging includes 40-pin DIP, and 44-pin PLCC. Development and programming support for the PA7140 is provided by ICT and popular third party development tool manufacturers.

Pin Configurations

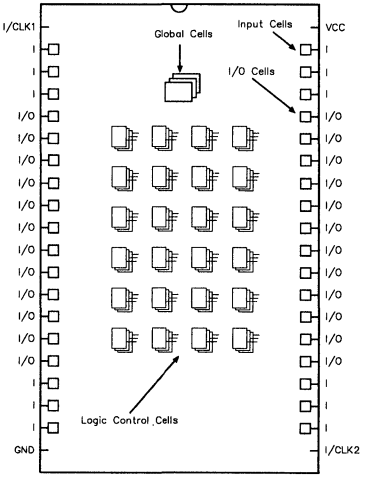
DIP (600 mil)

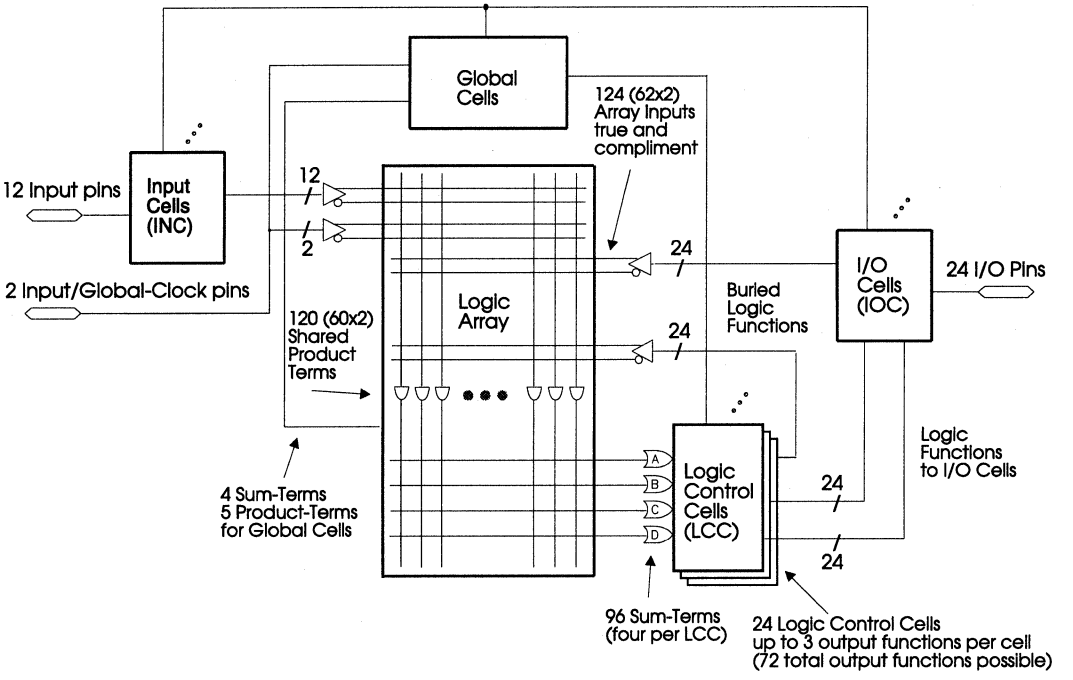


PLCC

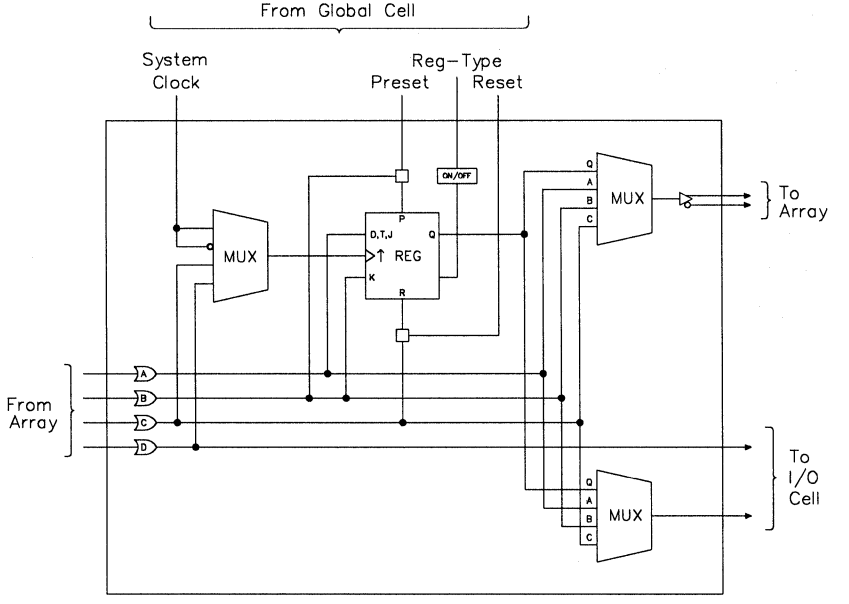


Block Diagram

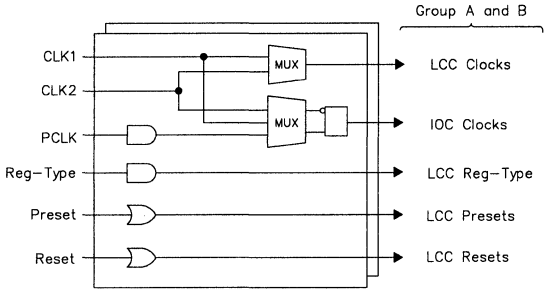




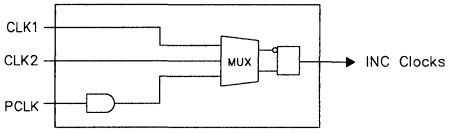
PA7140 Architecture Diagram



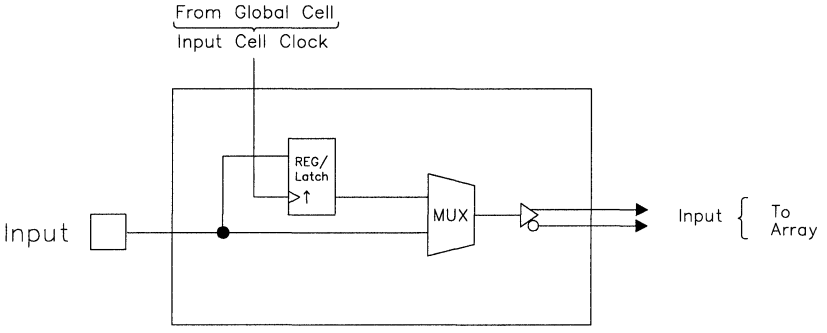
PA7140 Logic Control Cell



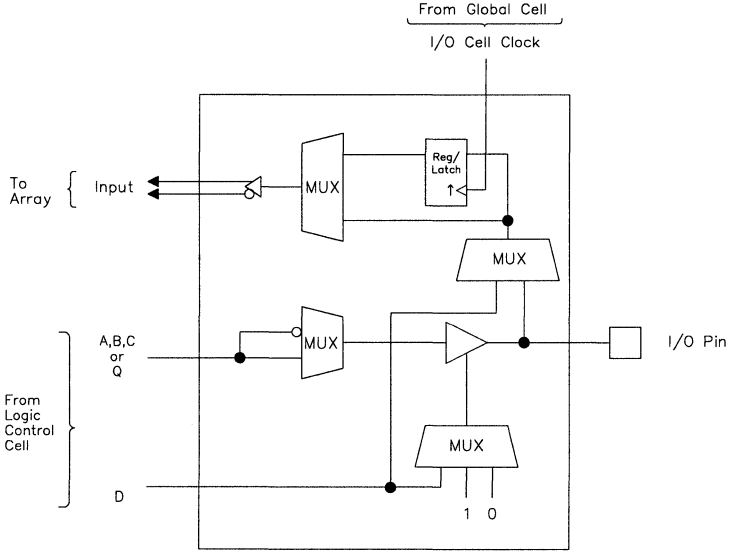
PA7140 Global Cell for LCCs and IOCs



PA7140 Global Cell for INCs



PA7140 Input Cell



PA7128 I/O Cell

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	(Soldering 10 seconds)	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+ 70	°C
T_R	Clock Rise Time	(Note 3)		20	ns
T_F	Clock Fall Time	(Note 3)		20	ns
T_{RVCC}	V_{CC} Rise Time	(Note 3)		250	ms

D.C. Electrical Characteristics

Over the operating range

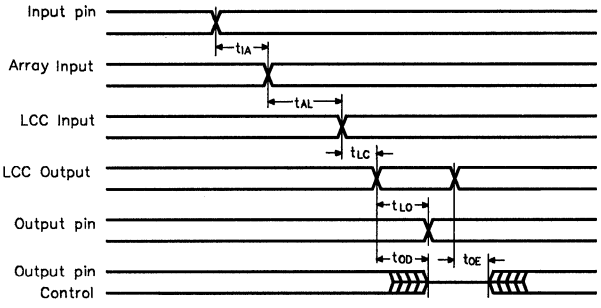
Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA		0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current [5]	V_{CC}=5V,V_O=0.5V,T_A=25°C	− 30	− 120	mA
I_{CC}	V_{CC} Current	V_{IN} = 0V or 3V [4,12] f = 25MHz All outputs disabled		150 (typ=100)[20]	mA
C_{IN}	Input Capacitance [6]	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT}	Output Capacitance [6]			12	pF

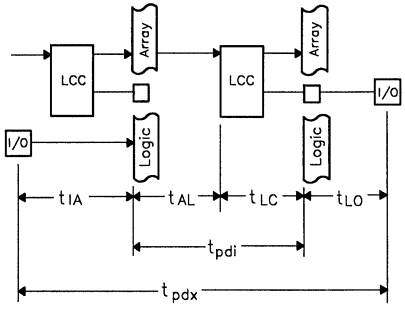
A.C. Electrical Characteristics Combinatorial

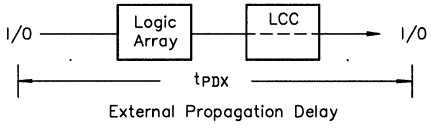
Over operating conditions

Symbol	Parameters [7, 13]	PA7140-20 PA7140-1[18]		PA7140-25 PA7140-2[18]		Units
		Min	Max	Min	Max	
t_{PDI}	Propagation delay Internal (t_{AL}+ t_{LC})		13		17	ns
t_{PDX}	Propagation delay External (t_{IA}+ t_{AL}+ t_{LC}+ t_{LO})		20		25	ns
t_{IA}	Input or I/O pin to array input		2		2	ns
t_{AL}	Array input to LCC		12		16	ns
t_{LC}	LCC input to LCC output [11]		1		1	ns
t_{LO}	LCC output to output pin		5		6	ns
t_{OD}, t_{OE}	Output Disable, Enable from LCC output [8]		5		6	ns
t_{OX}	Output Disable, Enable from input pin[8]		20		25	ns

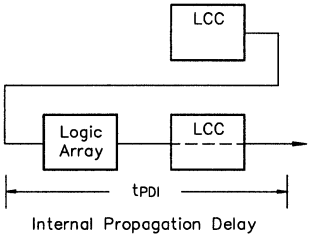
Combinatorial Timing - Waveforms and Block Diagram







External Propagation Delay



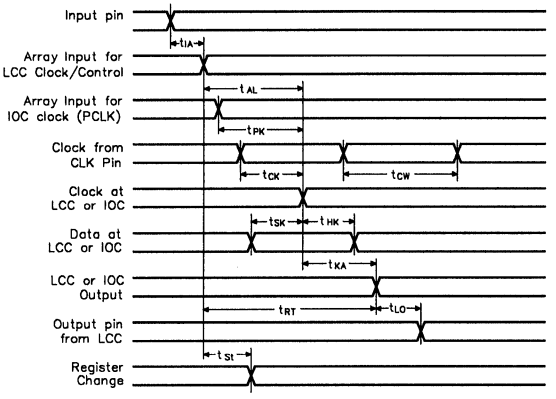
Internal Propagation Delay

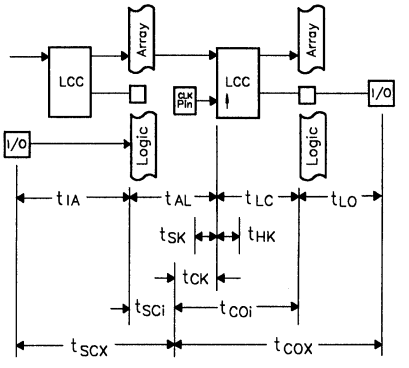
A.C. Electrical Characteristics Sequential

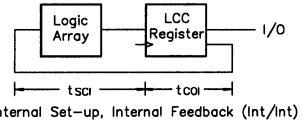
Over operating conditions

Symbol	Parameters [7, 13]	PA7140-20 PA7140-1[18]		PA7140-25 PA7140-2[18]		Units
		Min	Max	Min	Max	
t_{SCI}	Internal set-up to system-clock[9] , - LCC [15] (t_{AL}+ t_{SK}+ t_{LC} - t_{CK})	10		15		ns
t_{SCX}	Input [17] (Ext.) set-up to system-clock,-LCC(t_{IA}+ t_{SCI})	12		17		ns
t_{COI}	System-clock to Array Int.-LCC/IOC/INC[15](t_{CK}+ t_{LC})		7		8	ns
t_{COX}	System-clock to Output Ext.- LCC(t_{COI}+ t_{LO})		12		13	ns
t_{HX}	Input hold time from system clock - LCC	0		0		ns
t_{SK}	LCC input set-up to async. clock [14] - LCC	3		4		ns
t_{AK}	Clock at LCC or IOC - LCC output	1		1		ns
t_{HK}	LCC input hold time from async. clock - LCC	4		4		ns
t_{SI}	Input set-up to system clock -IOC/INC [15](t_{SK} - t_{CK})	0		0		ns
t_{HI}	Input hold time from system clock-IOC/INC (t_{CK}-t_{SK})	3		3		ns
t_{PK}	Array input to IOC PCLK clock		9		11	ns
t_{SPI}	Input set-up to PCLK clock -IOC/INC (t_{SK}-t_{PK}-t_{IA}) [19]	0		0		ns
t_{HPI}	Input hold PCLK clock [18] - IOC/INC (t_{PK} + t_{IA} - t_{SK})	6		7		ns
t_{SD}	Input set-up to system clock - IOC Sum-D [16] (t_{IA} + t_{AL} + t_{LC} + t_{SK} - t_{CK})	12		16		ns
t_{HD}	Input hold time from system clock - IOC Sum-D	0		0		ns
t_{SDP}	Input set-up to PCLK clock - IOC Sum-D (t_{IA} + t_{AL} + t_{LC} + t_{SK} - t_{PK})	9		12		ns
t_{HDP}	Input hold time from PCLK clock - IOC Sum-D	0		0		ns
t_{CK}	System-clock delay to LCC/IOC/INC		6		7	ns
t_{CW}	System-clock low or high pulse width	7		8		ns
f_{MAX1}	Max system-clock frequency Int/Int 1/(t_{SCI} + t_{COI})		58.8		43.5	MHz
f_{MAX2}	Max system-clock frequency Ext/Int 1/(t_{SCX} + t_{COI})		52.6		40.0	MHz
f_{MAX3}	Max system-clock frequency Int/Ext 1/(t_{SCI} + t_{COX})		45.7		35.7	MHz
f_{MAX4}	Max system-clock frequency Ext/Ext 1/(t_{SCX}+ t_{COX})		41.6		33.3	MHz
f_{TGL}	Max system-clock toggle frequency 1/(t_{CW} + t_{CW}) [10]		71.4		62.5	MHz
t_{PR}	LCC Preset/Reset to LCC output		1		2	ns
t_{ST}	Input to Global Cell preset/reset (t_{IA} + t_{AL} + t_{PR})		15		20	ns
t_{AW}	Asynch. preset/reset pulse width	8		8		ns
t_{RT}	Input to LCC Reg-Type (RT)		8		10	ns
t_{RTV}	LCC Reg-Type to LCC output register change		1		2	ns
t_{RTC}	Input to Global Cell reg.-type change (t_{RT} + t_{RTV})		9		12	ns
t_{RW}	Asynch. Reg-Type pulse width	10		10		ns
t_{reset}	Power-on reset time for register in clear state[3]		5		5	µs

Sequential Timing - Waveforms and Block Diagram

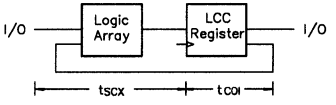






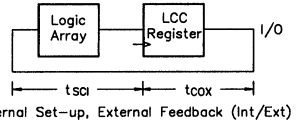
Internal Set–up, Internal Feedback (Int/Int)

$f_{MAX1} = 1/t_{SCI} + t_{COI}$



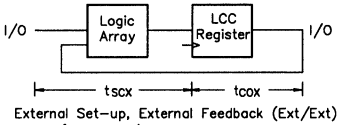
External Set–up, Internal Feedback (Ext/Int)

$f_{MAX2} = 1/t_{SCX} + t_{COI}$



Internal Set–up, External Feedback (Int/Ext)

$f_{MAX3} = 1/t_{SCI} + t_{COX}$



External Set–up, External Feedback (Ext/Ext)

$f_{MAX4} = 1/t_{SCX} + t_{COX}$

Notes:

1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
4. I/O pins are 0V or 3V.
5. Test one output at a time for a duration of less than 1 sec.
6. Capacitances are tested on a sample basis.
7. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
8. t_{OE} is measured from input transition to VREF ± 0.1V (See test loads at end of section 5 for VREF value). tOD is measured from input transition to VOH - 0.1V or VOL + 0.1V.
9. DIP: "System-clock" refers to pin 1/21 high speed clocks. PLCC: "System-clock" refers to pin 2/24 high speed clocks.
10. For T or JK registers in toggle (divide by 2) operation only.
11. For combinatorial and async-clock to LCC output delay.
12. ICC for a typical application: This parameter is tested with the device programmed as a 12-bit D type Counter.
13. Test loads are specified at the end of section 3 in this data book.
14. "Async. clock" refers to the clock from the Sum term (OR gate).
15. The "LCC" term indicates that the timing parameter is applied to the LCC register.
    The "IOC" term indicates that the timing parameter is applied to the IOC register.
    The "INC" term indicates that the timing parameter is applied to the INC register.
    The "IOC/INC" term indicates that the timing parameter is applied to both the IOC and INC registers.
    The "LCC/IOC/INC" term indicates that the timing parameter is applied to the LCC, IOC and INC registers.
16. This refers to the Sum-D gate routed to the IOC register for an additional buried register.
17. The term "Input" without any reference to another term refers to an (external) input pin.
18. PA7140-1 is an alternate number for PA7140-20.
    PA7140-2 is an alternate number for PA7140-25.
19. The parameter t_{SPI} indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of (t_{SK} - t_{PK} - t_{IA}). This means that no set-up time for the data from the pin or input is required, i.e. the external data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for t_{HPI} time, i.e. to wait for the PCLK signal to arrive at the IOC register.
20. Typical (typ) ICC is measured at TA = 25°C, Freq = 25MHz, VCC = 5V.

PEEL Devices

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PEEL™18CV8 -7/-10/-15/-25
CMOS Programmable Electrically Erasable Logic Device

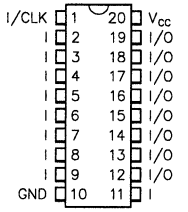
Features

- **High Speed/Low Power**
  - — Speeds ranging from 7ns to 25ns
  - — Power as low as 37mA at 25MHz
- **CMOS Electrically Erasable Technology**
  - — Superior factory testing
  - — Reprogrammable in plastic package
  - — Reduces retrofit and development costs
- **Development/Programmer Support**
  - — Third party software and programmers
  - — ICT PLACE Development Software and PDS-3 programmer
  - — PLD-to-PEEL JEDEC file translator
- **Architectural Flexibility**
  - — 74 product term x 36 input array
  - — Up to 18 inputs and 8 I/O pins
  - — Up to 12 configurations per macrocell
  - — Synchronous preset, asynchronous clear
  - — Independent output enables
  - — 20-pin DIP, PLCC, SOIC packages
- **Application Versatility**
  - — Replaces random logic
  - — Super-sets standard PLDs (PAL, GAL, EPLD)
  - — Enhanced architecture fits more logic than ordinary PLDs

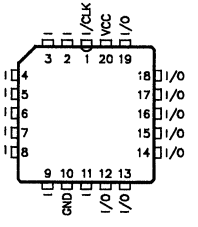
General Description

The PEEL18CV8 is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL18CV8 offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL18CV8 is available in 20-pin DIP, PLCC and SOIC packages with speeds ranging from 7ns to 25ns with power consumption as low as 37mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability thus, assuring the highest quality possible. The PEEL18CV8 architecture allows it to replace over 20 standard 20-pin PLDs (PAL, GAL, EPLD, etc.). It also provides additional architecture features so more logic can be put into every design. ICT's JEDEC file translator instantly converts to the PEEL18CV8 existing 20-pin PLDs without the need to rework the existing design. Development and programming support for the PEEL18CV8 is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

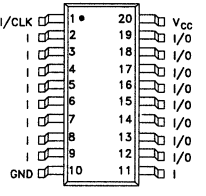
Pin Configuration (Figure 1)



DIP

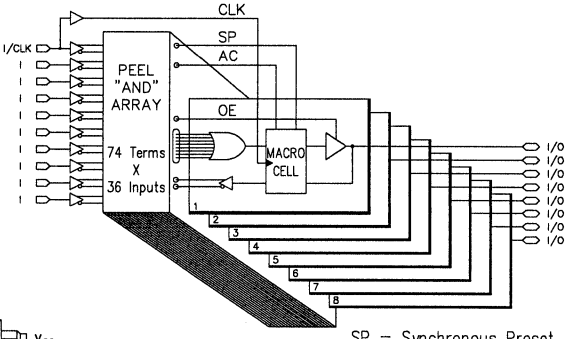


PLCC



SOIC

Block Diagram (Figure 2)



SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

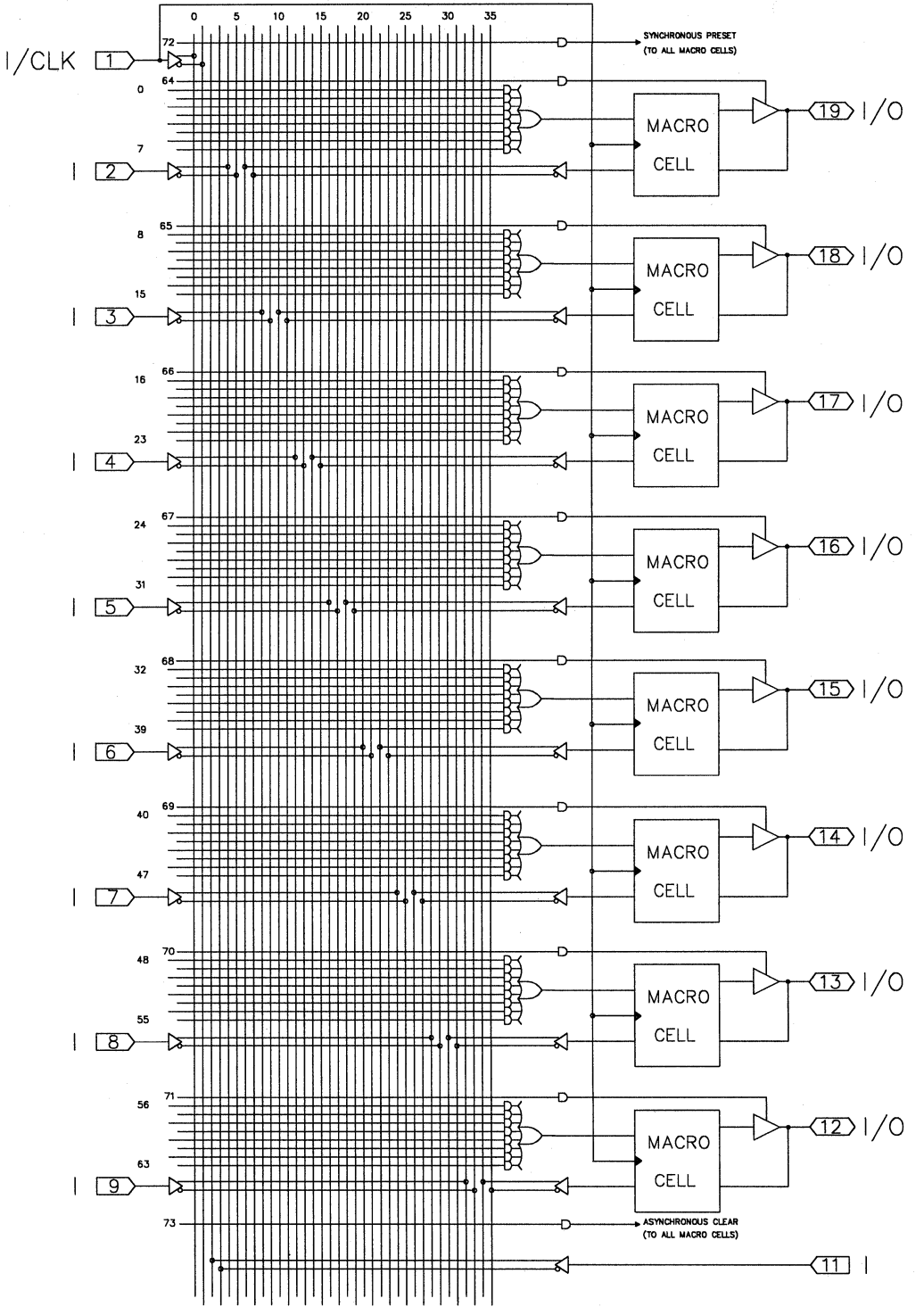


Figure 3. PEEL18CV8 Logic Array Diagram

Function Description

The PEEL18CV8 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL18CV8 architecture is illustrated in the block diagram of figure 2. Ten dedicated inputs and 8 I/Os provide up to 18 inputs and 8 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL18CV8 can implement up to 8 sum-of-products logic expressions.

Associated with each of the 8 OR functions is an I/O macrocell which can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL18CV8 (shown in figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

36 Input Lines:

- 20 input lines carry the true and compliment of the signals applied to the 10 input pins
- 16 additional lines carry the true and compliment values of feedback or input signals from the 8 I/Os

74 product terms:

- 64 product terms (arranged in groups of 8) used to form sum of product functions
- 8 output enable terms (one for each I/O)
- 1 global synchronous preset term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 36-input AND gate. A product term which is connected to both the true and compliment of an input signal will always be FALSE and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL18CV8, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function)

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL18CV8 to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine: output polarity; output type (registered or non-registered); and input/feedback path (bi-directional I/O, combinatorial feedback, or register feedback). Refer to table 1 for details.

Equivalent circuits for the twelve macrocell configurations are illustrated in figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10) the macrocell provides eight additional configurations. When creating a PEEL device design, the desired macrocell configuration generally is specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity
Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable
The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select
The PEEL18CV8 macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O); directly from the Q output of the flip-flop (registered feedback); or directly from the OR gate (combinatorial feedback).

Bi-directional I/O
The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback
The signal-select multiplexer gives the macrocell the ability to feedback the output of the OR gate, bypassing the output buffer, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in figure 5.)

Registered Feedback
Feedback also can be taken from the register, regardless of whether the output function is to be combinatorial or registered. When implementing combinatorial output function, registered feedback allows for the internal latching of states without giving up the use of the external output.

Design Security
The PEEL18CV8 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

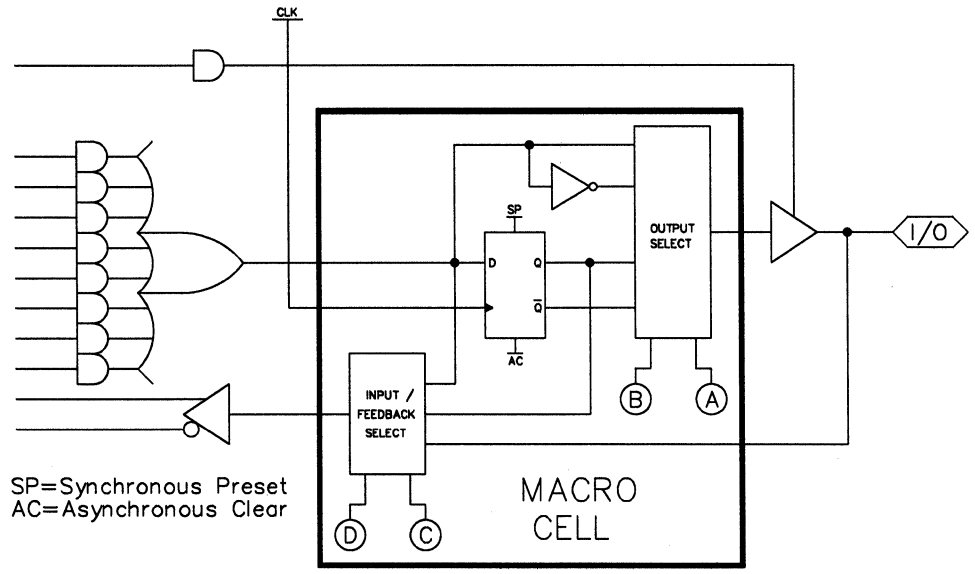


Figure 4. Block Diagram of The PEEL18CV8 I/O Macrocell

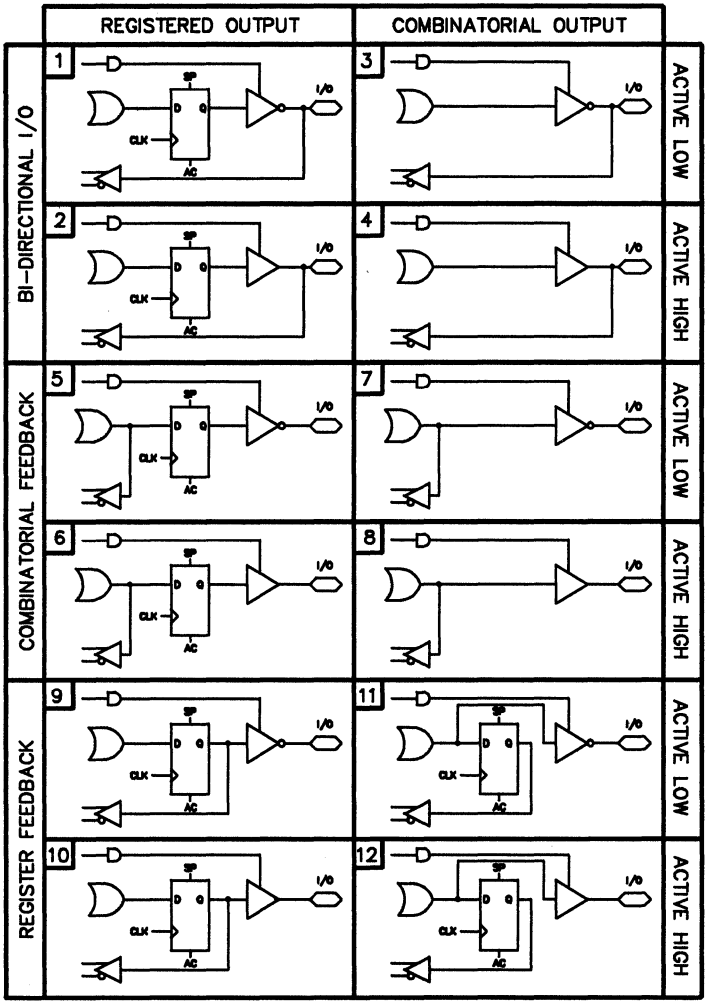


Figure 5. Equivalent Circuits for the Twelve Configurations of the PEEL18CV8 I/O Macorcell.

Configuration		Input/Feedback Select	Output Select	
#	A B C D			
1	1 1 1 1	Bi-Directional I/O	Register	Active Low
2	0 1 1 1	"	"	Active High
3	1 0 1 1	"	Combinatorial	Active Low
4	0 0 1 1	"	"	Active High
5	1 1 1 0	Combinatorial Feedback	Register	Active Low
6	0 1 1 0	"	"	Active High
7	1 0 1 0	"	Combinatorial	Active Low
8	0 0 1 0	"	"	Active High
9	1 1 0 0	Register Feedback	Register	Active Low
10	0 1 0 0	"	"	Active High
11	1 0 0 0	"	Combinatorial	Active Low
12	0 0 0 0	"	"	Active High

Table 1. PEEL18CV8 Macrocell Configuration Bits

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+ 70	°C
T_R	Clock Rise Time	See note 4		20	ns
T_F	Clock Fall Time	See note 4		20	ns
T_{RVCC}	V_{CC} Rise Time	See note 4		250	ms

D.C. Electrical Characteristics

Over the operating range

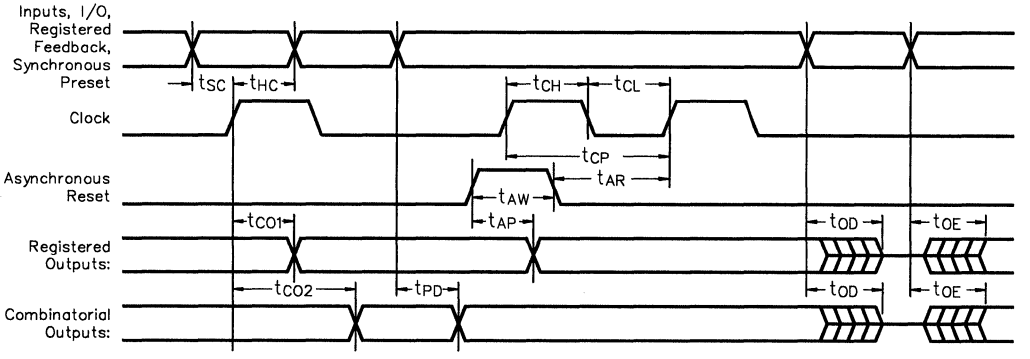
Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA		2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA		V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA			0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA			0.1	V
V_{IH}	Input HIGH Level			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level			− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}			±10	µA
I_{SC}	Output Short Circuit Current	V_{CC}=5V, V_O=0.5V[10], T_A = 25°C		− 30	−135	mA
I_{CC}[11]	V_{CC} Current (See CR-1 for typical I_{CC})	V_{IN} = 0V or 3V f = 25MHz All outputs disabled[5]	-7		110	mA
			-10		110	mA
			-15		45	mA
			-25		37	mA
C_{IN} [8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz			6	pF
C_{OUT} [8]	Output Capacitance				12	pF

A.C. Electrical Characteristics

Over the Operating Range [9,12]

Symbol	Parameter	-7		-10		-15		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input[6] to non-registered output		7.5		10		15		25	ns
t_{OE}	Input [6] to output enable [7]		7.5		10		15		25	ns
t_{OD}	Input [6] to output disable [7]		7.5		10		15		25	ns
t_{CO1}	Clock to output		7		7		12		15	ns
t_{CO2}	Clock to comb. output delay via internal registered feedback		10		12		25		35	ns
t_{CF}	Clock to Feedback		3.5		4		8		15	ns
t_{SC}	Input [6] or feedback setup to clock	5		5		12		20		ns
t_{HC}	Input [6] hold after clock	0		0		0		0		ns
t_{CL},t_{CH}	Clock low time, clock high time [9]	3.5		5		10		15		ns
t_{CP}	Min clock period Ext (t_{SC} + t_{CO1})	12		12		24		35		ns
f_{max1}	Internal Feedback ($1/t_{SC}+t_{CF}$)[13]	117.6		111		50		28.5		MHz
f_{max2}	External Feedback($1/t_{CP}$)[13]	83.3		83.3		41.6		28.5		MHz
f_{max3}	No Feedback ($1/t_{CL}+t_{CH}$)[13]	142.8		100		50		33.3		MHz
t_{AW}	Asynchronous Reset pulse width	7.5		10		15		25		ns
t_{AP}	Input [6] to Asynchronous Reset		7.5		10		15		25	ns
t_{AR}	Asynchronous Reset recovery time		7.5		10		15		25	ns
t_{RESET}	Power-on reset time for registers in clear state		5		5		5		5	µs

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
5. I/O pins are 0V or 3V.
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as an 8-bit Counter.
12. PEEL Device test loads are specified at the end of this section.
13. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

PEEL™18CV8 -5
CMOS Programmable Electrically Erasable Logic Device

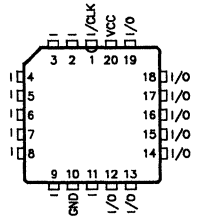
Features

- **CMOS .8μm EEPROM Technology**
- **High Speed**
  - tpd=5ns, fmax=166.7
- **Electrically Erasable Technology**
  - Superior factory testing
  - Reprogrammable in plastic package
  - Reduces retrofit and development costs
- **Development/Programmer Support**
  - Third party software and programmers
  - ICT PLACE Development Software and PDS-3 programmer
  - PLD-to-PEEL JEDEC file translator
- **Architectural Flexibility**
  - 74 product term x 36 input array
  - Up to 18 inputs and 8 I/O pins
  - Up to 12 configurations per macrocell
  - Synchronous preset, asynchronous clear
  - Independent output enables
  - 20-pin PLCC package
- **Application Versatility**
  - Replaces random logic
  - Super-sets standard PLDs (PAL, GAL, EPLD)
  - Enhanced Architecture fits more logic than ordinary PLDs

General Description

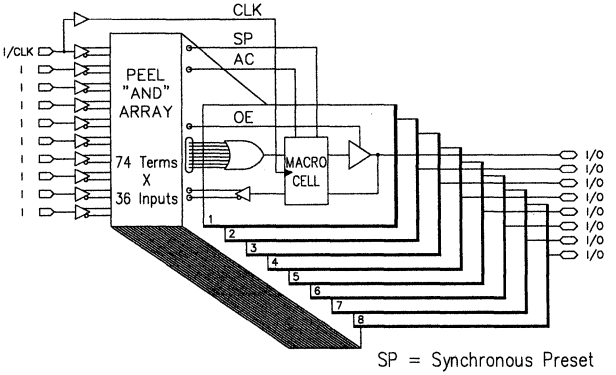
The PEEL18CV8-5 is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL18CV8-5 offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL18CV8-5 is available in a 20-pin PLCC package with power consumption of 120mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability thus, assuring the highest quality possible. The PEEL18CV8 architecture allows it to replace standard 20-pin PLDs (PAL, GAL, EPLD, etc.). It also provides additional architecture features so more logic can be put into every design. ICT's JEDEC file translator instantly converts to the PEEL18CV8 existing 20-pin PLDs without the need to rework the existing design. Development and programming support for the PEEL18CV8 is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

Pin Configuration (Figure 1)



PLCC

Block Diagram (Figure 2)



SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+ 70	°C
T_R	Clock Rise Time	See note 4		10	ns
T_F	Clock Fall Time	See note 4		10	ns
T_{RVCC}	V_{CC} Rise Time	See note 4		250	ms

D.C. Electrical Characteristics

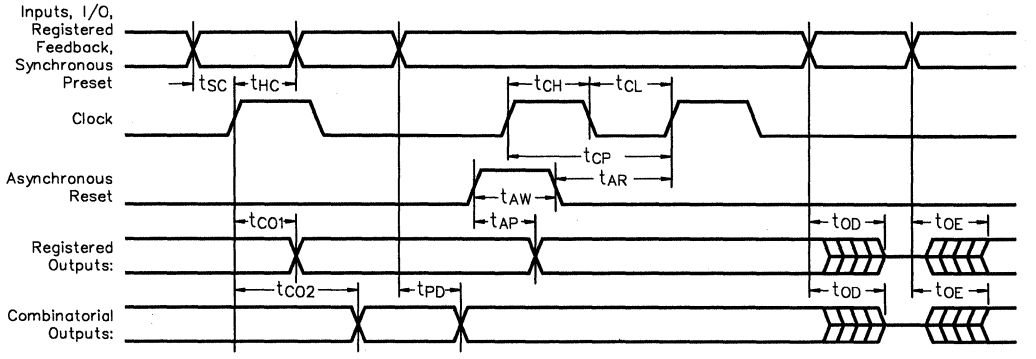
Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA		0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current	V_{CC}=5V, V_O=0.5V[10], T_A = 25°C	− 30	−135	mA
I_{CC}[11]	V_{CC} Current	V_{IN} = 0V or 3V f = 25MHz All outputs disabled [5]		120	mA
C_{IN} [8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT} [8]	Output Capacitance			12	pF

A.C. Electrical Characteristics Over the Operating Range [8,11]

Symbol	Parameter	18CV8-5		Unit
		Min	Max	
t_{PD}	Input or I/O to non-registered output		5	ns
t_{OE}	Input or I/O to output enable[6]		5	ns
t_{OD}	Input or I/O to output disable[6]		5	ns
t_{CO1}	Clock to output		4	ns
t_{CO2}	Clock to combinatorial output delay via internal registered feedback		7.5	ns
t_{CF}	Clock to Feedback		2.5	ns
t_{SC}	Input or feedback setup to clock	3.5		ns
t_{HC}	Input hold after clock	0		ns
t_{CL},t_{CH}	Clock width - clk low time, clk high time [4]	3		ns
t_{CP}	Min clock period External (t_{SC} + t_{CO1})	7		ns
f_{max1}	Max clock freq. Internal Feedback[12]	166.7		MHz
f_{max2}	Max clock freq. External (1/t_{CP})	133		MHz
f_{max3}	Max clock freq. No Feedback (1/(t_{CL}+t_{CH}))[12]	166.7		MHz
t_{AW}	Asynchronous clear pulse width	5		ns
t_{AP}	Input to asynchronous clear		5	ns
t_{AR}	Asynchronous Reset Recovery Time		5	ns
t_{RESET}	Power-on reset time for registers in clear state[4]		5	µs

Switching Waveforms



1. Minimum DC input is -0,5V, however inputs may undershoot to -2.0V for periods less than 20ns
2. Contact ICT for other operating ranges.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
5. I/O pins are 0V or 3V.
6. "Input" refers to an input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to V_{OH}-0.1V or V_{OL}+0.1V; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration less than 1 second.
11. ICC for a typical application: This parameter is tested with the device programmed as an 8-bit counter.
12. PEEL Device test loads are specified at the end of this section
13. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

PEEL™18CV8I -10/-15/-25
CMOS Programmable Electrically Erasable Logic Device

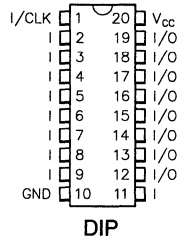
Features

- **Industrial Grade Specifications**
  - V_{CC} = 4.5V to 5.5V, TA = -40°C to +85°C
  - Reprogrammable 20-pin DIP, PLCC and SOIC packages
- **High Speed/Low Power**
  - Speeds ranging from 10ns to 25ns
  - Power as low as 50mA at 25MHz
- **Development/Programmer Support**
  - Third party software and programmers
  - ICT PLACE Development Software and PDS-3 programmer
  - PLD-to-PEEL JEDEC file translator
- **Architectural Flexibility**
  - 74 product term x 36 input array
  - Up to 18 inputs and 8 I/O pins
  - Up to 12 configurations per macrocell
  - Synchronous preset, asynchronous clear
  - Independent output enables
- **Application Versatility**
  - Replaces random logic
  - Super-sets standard PLDs (PAL, GAL, EPLD)
  - Enhanced architecture fits more logic than ordinary PLDs

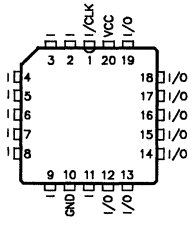
General Description

The PEEL18CV8I is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL18CV8I offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL18CV8I is available in 20-pin DIP, PLCC and SOIC packages with speeds ranging from 10ns to 25ns with power consumption as low as 50mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability thus, assuring the highest quality possible. The PEEL18CV8I architecture allows it to replace over 20 standard 20-pin PLDs (PAL, GAL, EPLD, etc.). It also provides additional architecture features so more logic can be put into every design. ICT's JEDEC file translator instantly converts to the PEEL18CV8I existing 20-pin PLDs without the need to rework the existing design. Development and programming support for the PEEL18CV8I is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

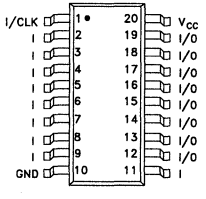
Pin Configuration (Figure 1)



DIP

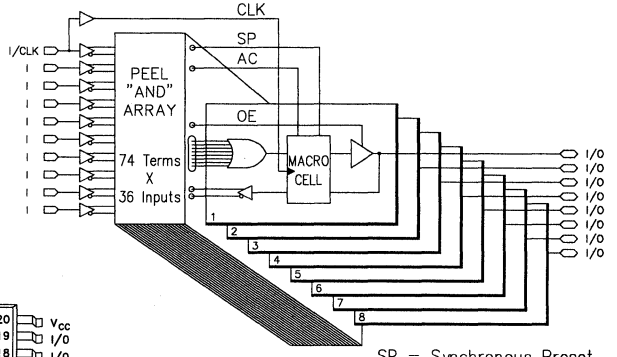


PLCC



SOIC

Block Diagram (Figure 2)



SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	– 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		– 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Industrial [2]	4.5	5.5	V
T_A	Ambient Temperature	Industrial [2]	-40	+ 85	°C
T_R	Clock Rise Time	See note 4		20	ns
T_F	Clock Fall Time	See note 4		20	ns
T_{RVCC}	V_{CC} Rise Time	See note 4		250	ms

D.C. Electrical Characteristics

Over the operating range

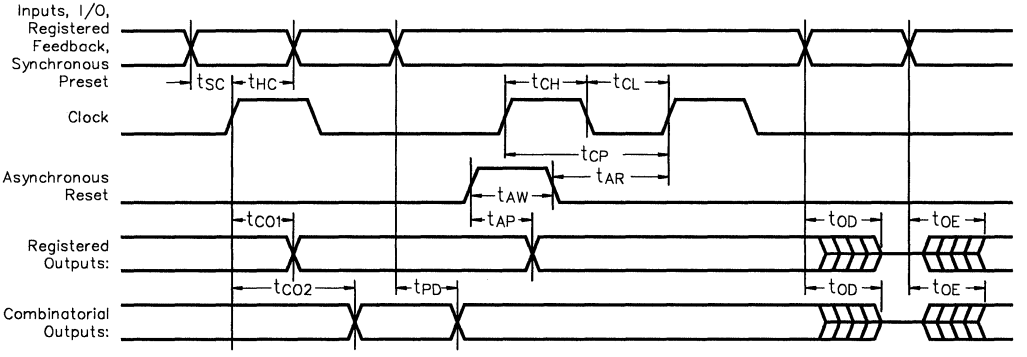
Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = – 4.0mA		2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = –10µA		V_{CC} – 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA			0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA			0.1	V
V_{IH}	Input HIGH Level			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level			– 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}			±10	µA
I_{SC}	Output Short Circuit Current	V_{CC}=5V, V_O=0.5V[10], T_A = 25°C		– 30	–135	mA
I_{CC}[11]	V_{CC} Current (See CR-1 for typical I_{CC})	V_{IN} = 0V or 3V, f = 25MHz, All outputs disabled[5]	I-10		115	mA
			I-15		55	mA
			I-25		50	mA
C_{IN} [8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz			6	pF
C_{OUT} [8]	Output Capacitance				12	pF

A.C. Electrical Characteristics

Over the Operating Range [9,12]

Symbol	Parameter	I-10		I-15		I-25		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input [6] to non-registered output		10		15		25	ns
t_{OE}	Input [6] to output enable [7]		10		15		25	ns
t_{OD}	Input [6] to output disable [7]		10		15		25	ns
t_{CO1}	Clock to output		7		12		15	ns
t_{CO2}	Clock to comb. output delay via internal registered feedback		12		25		35	ns
t_{CF}	Clock to Feedback		4		8		15	ns
t_{SC}	Input [6] or feedback setup to clock	5		12		20		ns
t_{HC}	Input [6] hold after clock	0		0		0		ns
t_{CL},t_{CH}	Clock low time, clock high time [9]	5		10		15		ns
t_{CP}	Min clock period Ext (t_{SC} + t_{CO1})	12		24		35		ns
f_{max1}	Internal Feedback ($1/t_{SC}+t_{CF}$) [13]	111		50		28.5		MHz
f_{max2}	External Feedback($1/t_{CP}$) [13]	83.3		41.6		28.5		MHz
f_{max3}	No Feedback ($1/t_{CL}+t_{CH}$) [13]	100		50		33.3		MHz
t_{AW}	Asynchronous Reset pulse width	10		15		25		ns
t_{AP}	Input [6] to Asynchronous Reset		10		15		25	ns
t_{AR}	Asynchronous Reset recovery time		10		15		25	ns
t_{RESET}	Power-on reset time for registers in clear state		5		5		5	µs

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
5. I/O pins are 0V or 3V.
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as an 8-bit Counter.
12. PEEL Device test loads are specified at the end of this section.
13. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

PEEL™20CG10A -7/-10/-15/L-15/-25
CMOS Programmable Electrically Erasable Logic Device

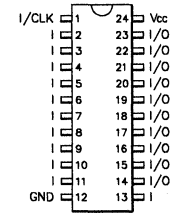
Features

- **High Speed/Low Power**
  - — Speeds ranging from 7ns to 25ns
  - — Power as low as 67mA at 25MHz
- **Electrically Erasable Technology**
  - — Superior factory testing
  - — Reprogrammable in plastic package
  - — Reduces retrofit and development costs
- **Development/Programmer Support**
  - — Third party software and programmers
  - — ICT Place Development Software and PDS-3 programmer
  - — PLD-to-PEEL JEDEC file translator
- **Architectural Flexibility**
  - — 92 product term X 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Up to 12 configurations per macrocell
  - — Synchronous preset, asynchronous clear
  - — Independent output enables
  - — 24-pin DIP, SOIC and 28-pin PLCC packages
- **Application Versatility**
  - — Replaces random logic
  - — Super-sets standard PLDs (PAL, GAL, EPLD)
  - — Enhanced Architecture fits more logic than ordinary PLDs

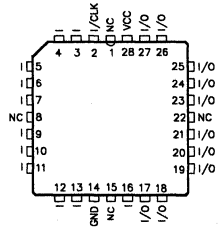
General Description

The PEEL20CG10A is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL20CG10A offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL20CG10A is available in 24-pin DIP, SOIC and 28-pin PLCC packages with speeds ranging from 7ns to 25ns with power consumption as low as 67mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability thus, assuring the highest quality possible. The PEEL20CG10A architecture allows it to replace over 20 standard 24-pin PLDs (PAL, GAL, EPLD etc.). It also provides additional architecture features so more logic can be put into every design. ICT's JEDEC file translator instantly converts to the PEEL20CG10A existing 24-pin PLDs without the need to rework the existing design. Development and programming support for the PEEL20CG10A is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

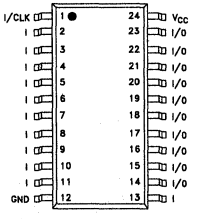
Pin Configuration (Figure 1)



DIP

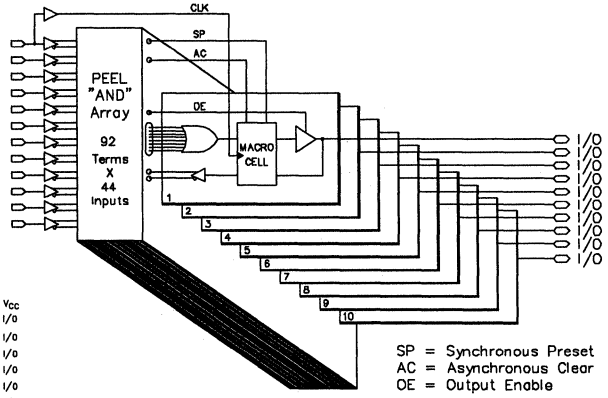


PLCC



SOIC

Block Diagram (Figure 2)



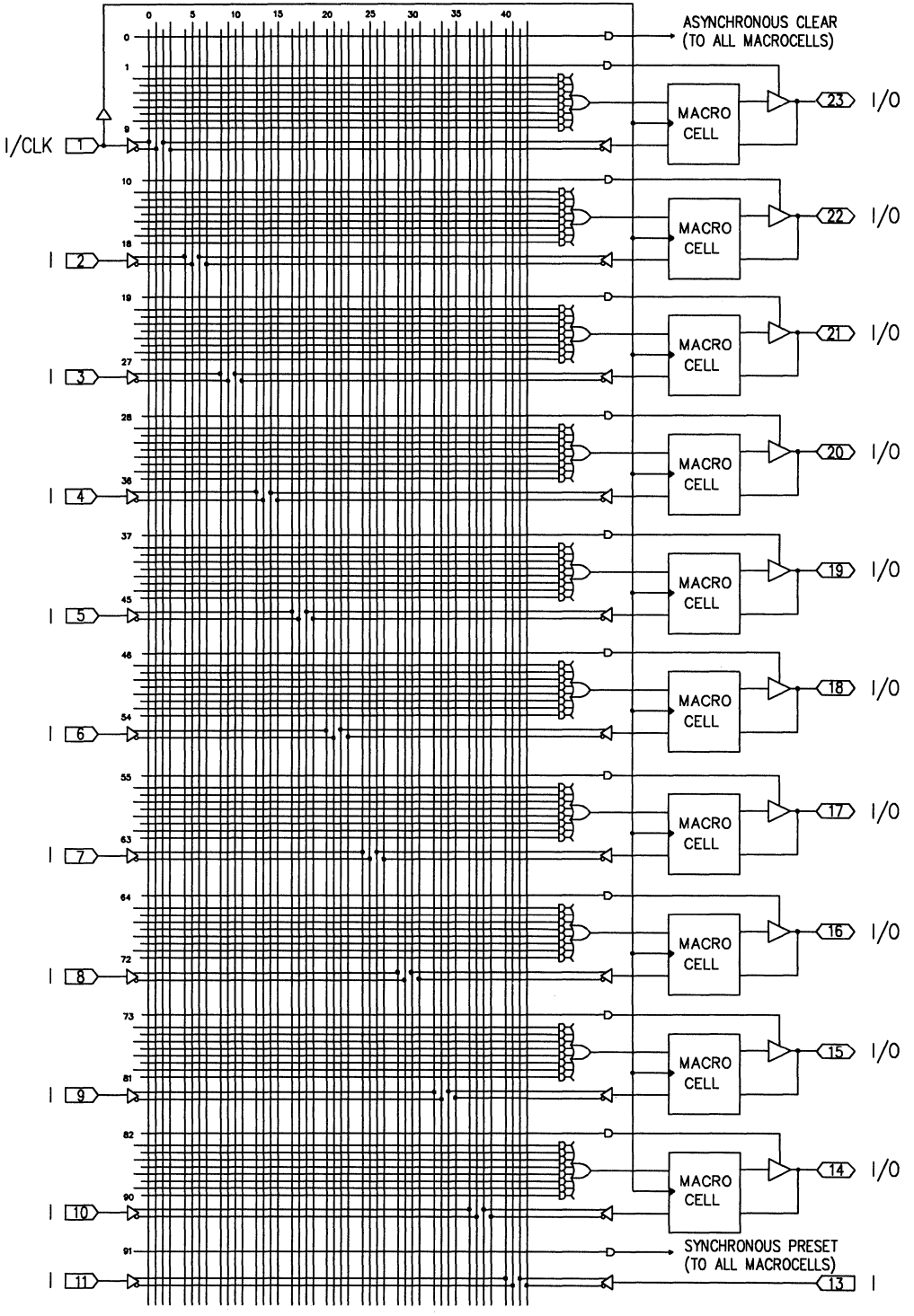


Figure 3. PEEL20CG10A Logic Array Diagram

Function Description

The PEEL20CG10A implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL20CG10A architecture is illustrated in the block diagram of figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL20CG10A can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL20CG10A (shown in figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

92 product terms:

- 80 product terms (8 per I/O)
- 10 output enable terms (one for each I/O)
- 1 global synchronous present term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL20CG10A, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program the connections on unused product terms so that they will have no effect on the output function)

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL20CG10A to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine: output polarity; output type (registered or non-registered); and input/feedback path (bi-directional I/O, combinatorial feedback, or register feedback). Table 1 shows the bit settings for each of the twelve macro-cell configurations.

Equivalent circuits for the twelve macrocell configurations are illustrated in figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10) the macrocell provides eight configurations that are unavailable in any PAL device.

Output Type

The signal from the OR array can be fed directly to the output pin or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity
Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable
The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select
The PEEL20CG10A macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O); directly from the Q output of the flip-flop (registered feedback); or directly from the OR gate (combinatorial feedback).

Bi-directional I/O
The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback
The signal-select multiplexer gives the macrocell the ability to feedback the output directly from the OR gate, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in figure 5.)

Registered Feedback
Feedback also can be taken from the register, regardless of whether the output function is to be combinatorial or registered. When implementing configurations 11 and 12 in figure 5, the register can be used for internal latching of data while leaving the external output free for combinatorial functions.

Design Security
The PEEL20CG10A provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word
The signature word feature allows a 24-bit code to be programmed into the PEEL20CG10A. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

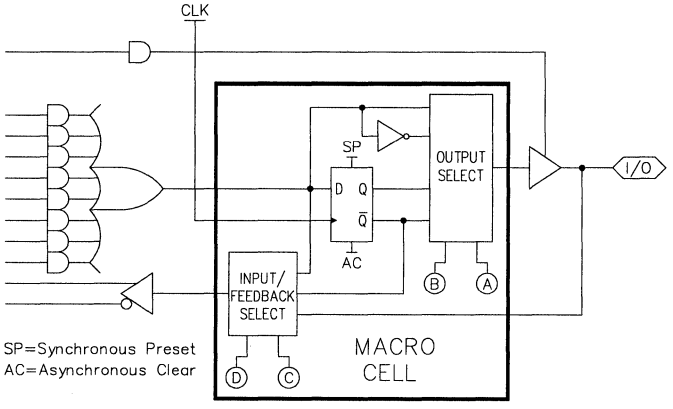


Figure 4. Block Diagram of the PEEL20CG10A I/O Macrocell

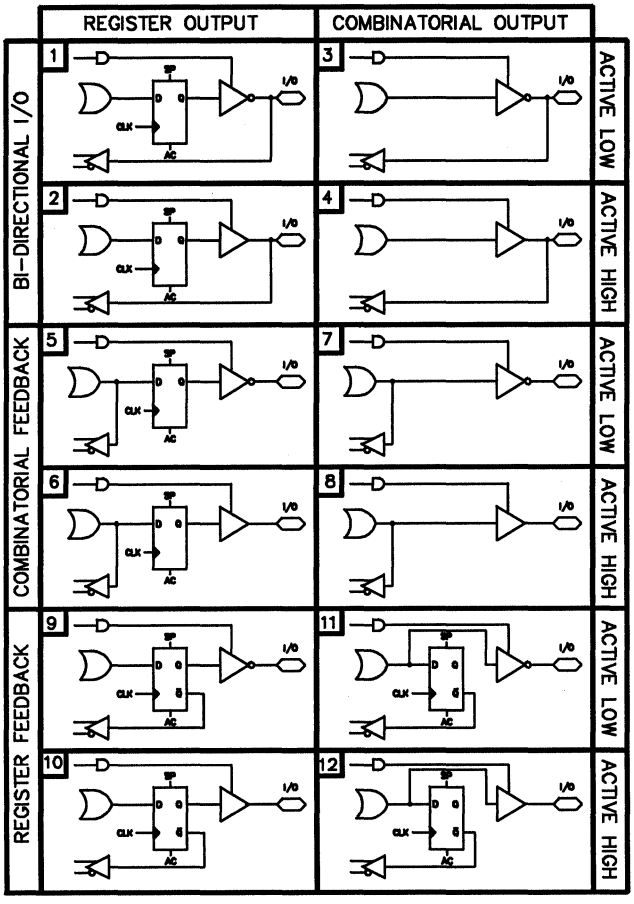


Figure 5. Equivalent Circuits for the Twelve Configurations of the PEEL20CG10A I/0 Macrocell.

Configuration #	A B C D	Input/Feedback Select	Output Select	
1	0 0 1 0	Bi-Directional I/O	Register	Active Low
2	1 0 1 0	"	"	Active High
3	0 1 0 0	"	Combinatorial	Active Low
4	1 1 0 0	"	"	Active High
5	0 0 1 1	Combinatorial Feedback	Register	Active Low
6	1 0 1 1	"	"	Active High
7	0 1 1 1	"	Combinatorial	Active Low
8	1 1 1 1	"	"	Active High
9	0 0 0 0	Register Feedback	Register	Active Low
10	1 0 0 0	"	"	Active High
11	0 1 1 0	"	Combinatorial	Active Low
12	1 1 1 0	"	"	Active High

Table 1. PEEL20CG10A Macrocell Configuration Bits

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+ 70	°C
T_R	Clock Rise Time	See note 4		20	ns
T_F	Clock Fall Time	See note 4		20	ns
T_{RVCC}	V_{CC} Rise Time	See note 4		250	ms

D.C. Electrical Characteristics

Over the operating range

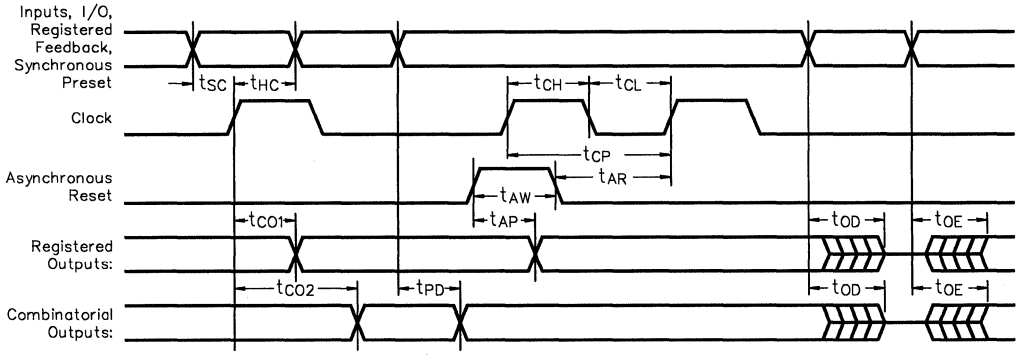
Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA		2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA		V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA			0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA			0.1	V
V_{IH}	Input HIGH Level			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level			− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}			±10	µA
I_{SC}	Output Short Circuit Current	V_{CC}=5V, V_O=0.5V[10], T_A = 25°C		− 30	−135	mA
I_{CC}[11]	V_{CC} Current (See CR-1 for typical I_{CC})	V_{IN} = 0V or 3V, f = 25MHz, All outputs disabled[5]	-7		155	mA
			-10		135	mA
			-15		135	mA
			L-15		75	mA
			-25		67	mA
C_{IN} [8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz			6	pF
C_{OUT} [8]	Output Capacitance				12	pF

A.C. Electrical Characteristics

Over the Operating Range [9,12]

Symbol	Parameter	-7		-10		-15		L-15		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input[6] to non-registered output		7.5		10		15		15		25	ns
t_{OE}	Input [6] to output enable [7]		7.5		10		15		15		25	ns
t_{OD}	Input [6] to output disable [7]		7.5		10		15		15		25	ns
t_{CO1}	Clock to output		5.5		6		8		10		15	ns
t_{CO2}	Clock to comb. output delay via internal registered feedback		10		12		17		19		35	ns
t_{CF}	Clock to Feedback		3.5		4		5		6		9	ns
t_{SC}	Input [6] or feedback setup to clock	3		4		8		10		15		ns
t_{HC}	Input [6] hold after clock	0		0		0		0		0		ns
t_{CL},t_{CH}	Clock low time, clock high time [9]	3		5		6		7.5		13		ns
t_{CP}	Min clock period Ext (t_{SC} + t_{CO1})	8.5		11		18		20		30		ns
f_{max1}	Internal Feedback ($1/t_{SC}+t_{CF}$)[13]	142		111		76.9		62.5		41.6		MHz
f_{max2}	External Feedback($1/t_{CP}$)[13]	117		90.9		62.5		50		33.3		MHz
f_{max3}	No Feedback ($1/t_{CL}+t_{CH}$)[13]	166		125		83.3		66.7		38.4		MHz
t_{AW}	Asynchronous Reset pulse width	7.5		10		15		15		25		ns
t_{AP}	Input [6] to Asynchronous Reset		7.5		10		15		18		25	ns
t_{AR}	Asynchronous Reset recovery time		7.5		10		15		18		25	ns
t_{RESET}	Power-on reset time for registers in clear state		5		5		5		5		5	µs

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
5. I/O pins are 0V or 3V.
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. PEEL Device test loads are specified at the end of this section.
13. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

PEEL™20CG10A -5
CMOS Programmable Electrically Erasable Logic Device

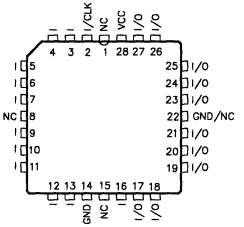
Features

- **.8μm CMOS EEPROM Technology**
- **High Speed**
  - — t_{PD} = 5ns, f_{max} = 181.8MHz
- **Electrically Erasable Technology**
  - — Superior factory testing
  - — Reprogrammable in plastic package
  - — Reduces retrofit and development costs
- **Development/Programmer Support**
  - — Third party software and programmers
  - — ICT PLACE Development Software and PDS-3 programmer
  - — PLD-to-PEEL JEDEC file translator
- **Architectural Flexibility**
  - — 92 product term X 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Up to 12 configurations per macrocell
  - — Synchronous preset, asynchronous clear
  - — Independent output enables
  - — 28-pin PLCC package
- **Application Versatility**
  - — Replaces random logic
  - — Super-sets standard PLDs (PAL, GAL, EPLD)
  - — Enhanced Architecture fits more logic than ordinary PLDs

General Description

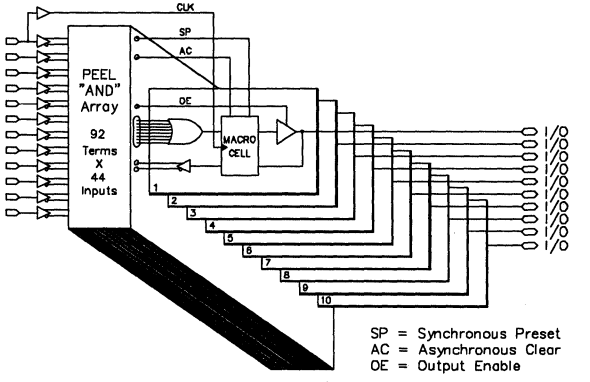
The PEEL20CG10A-5 is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The 20CG10A-5 offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL20CG10A-5 is available in a 28-pin PLCC package with power consumption of 140mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability thus, assuring the highest quality possible. The PEEL20CG10A architecture allows it to replace standard 24-pin PLDs (PAL, GAL, EPLD, etc.). It also provides additional architecture features so more logic can be put into every design. ICT's JEDEC file translator instantly converts to the PEEL20CG10A existing 24-pin PLDs without the need to rework the existing design. Development and programming support for the PEEL20CG10A is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

Pin Configuration (Figure 1)



PLCC

Block Diagram (Figure 2)



Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	70	°C
T_R	Clock Rise Time	See note 4		20	ns
T_F	Clock Fall Time	See note 4		20	ns
T_{RVCC}	VCC Rise Time	See note 4		250	ms

D.C. Electrical Characteristics

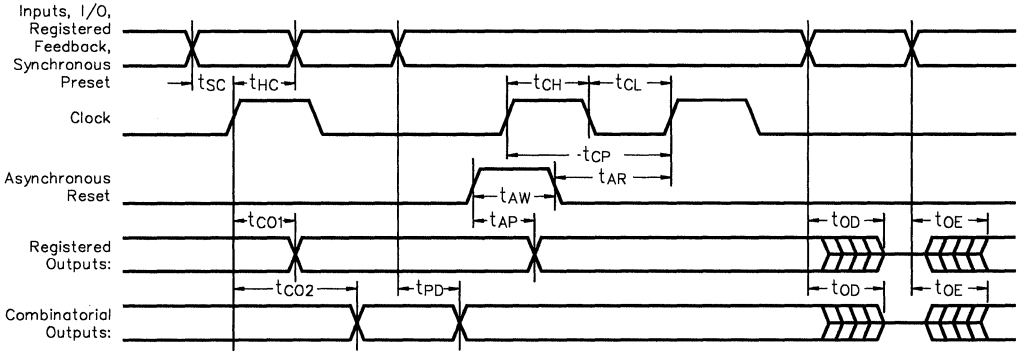
Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = −4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA		0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current	V_{CC}=5V, V_O = 0.5V [10], T_A = 25°C	− 30	−135	mA
I_{CC}	V_{CC} Current, Active	V_{IN} = 0V or 3V [5,11] f = 25MHz All outputs disabled		140	mA
C_{IN} [8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT} [8]	Output Capacitance			12	pF

A.C. Electrical Characteristics Over the Operating Range [9,12]

Symbol	Parameter	20CG10A-5		Unit
		Min	Max	
t_{PD}	Input[6] to non-registered output		5	ns
t_{OE}	Input [6] to output enable [7]		5	ns
t_{OD}	Input [6] to output disable [7]		5	ns
t_{CO1}	Clock to output		4	ns
t_{CO2}	Clock to combinatorial output delay via internal registered feedback		7.5	ns
t_{CF}	Clock to Feedback		2.5	ns
t_{SC}	Input [6] or feedback setup to clock	3		ns
t_{HC}	Input [6] hold after clock	0		ns
t_{CL},t_{CH}	Clock width - clock low time, clock high time [4]	2.5		ns
t_{CP}	Min clock period Extenal (t_{SC} + t_{CO1})	7		ns
f_{max1}	Max clock freq. Internal Feedback ($1/t_{SC}+t_{CF}$)[13]	181.8		MHz
f_{max2}	Max clock freq. External ($1/t_{CP}$)[13]	142.8		MHz
f_{max3}	Max clock freq. No Feedback ($1/t_{CL}+t_{CH}$)[13]	200		MHz
t_{AW}	Asynchronous Reset pulse width	5		ns
t_{AP}	Input [6] to Asynchronous Reset		5	ns
t_{AR}	Asynchronous Reset recovery time		5	ns
t_{RESET}	Power-on reset time for registers in clear state [4]		5	µs

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
5. I/O pins are 0V or 3V.
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. PEEL Device test loads are specified at the end of this section.
13. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

PEEL™20CG10AI -10/-15/-25
CMOS Programmable Electrically Erasable Logic Device

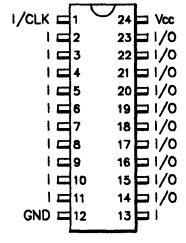
Features

- **Industrial Grade Specifications**
  - — V_{CC} = 4.5V to 5.5V, TA = -40°C to 85°C
  - — Reprogrammable 24-pin DIP, SOIC and 28-pin PLCC packages
- **High Speed/Low Power**
  - — Speeds ranging from 10ns to 25ns
  - — Power as low as 75mA at 25MHz
- **Development/Programmer Support**
  - — Third party software and programmers
  - — ICT Place Development Software and PDS-3 programmer
  - — PLD-to-PEEL JEDEC file translator
- **Architectural Flexibility**
  - — 92 product term X 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Up to 12 configurations per macrocell
  - — Synchronous preset, asynchronous clear
  - — Independent output enables
- **Application Versatility**
  - — Replaces random logic
  - — Emulates standard PLDs (PAL, GAL, EPLD)
  - — Enhanced Architecture fits more logic than ordinary PLDs

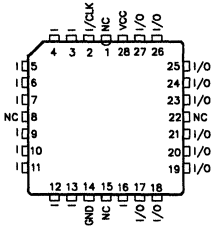
General Description

The PEEL20CG10AI is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The 20CG10AI offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL20CG10AI is available in 24-pin DIP, SOIC and 28-pin PLCC packages with speeds ranging from 10ns to 25ns with power consumption as low as 75mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability thus, assuring the highest quality possible. The PEEL20CG10AI architecture allows it to replace over 20 standard 24-pin PLDs (PAL, GAL, EPLD, etc.). It also provides additional architecture features so more logic can be put into every design. ICT's JEDEC file translator instantly converts to the PEEL20CG10AI existing 24-pin PLDs without the need to rework the existing design. Development and programming support for the PEEL20CG10AI is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

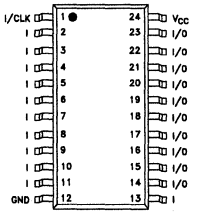
Pin Configuration (Figure 1)



DIP

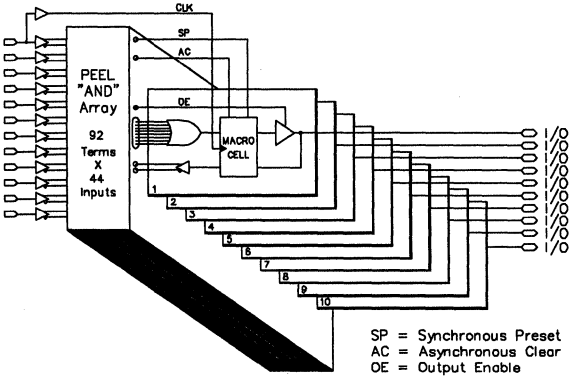


PLCC



SOIC

Block Diagram (Figure 2)



Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Industrial [2]	4.5	5.5	V
T_A	Ambient Temperature	Industrial [2]	-40	+ 85	°C
T_R	Clock Rise Time	See note 4		20	ns
T_F	Clock Fall Time	See note 4		20	ns
T_{RVCC}	V_{CC} Rise Time	See note 4		250	ms

D.C. Electrical Characteristics

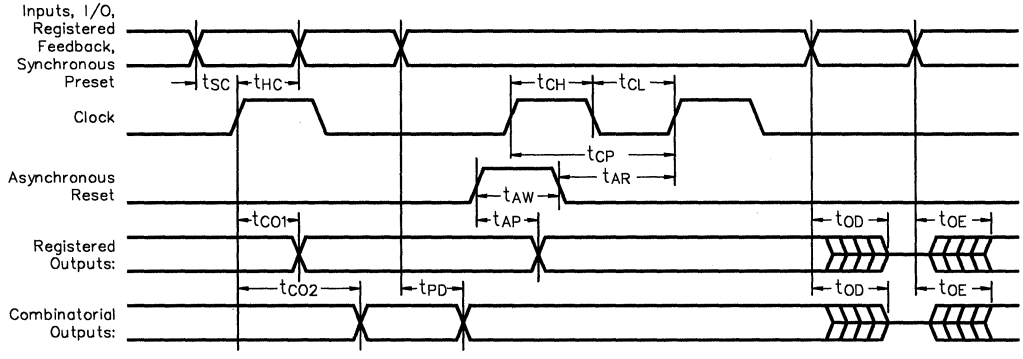
Over the operating range

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA		2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA		V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA			0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA			0.1	V
V_{IH}	Input HIGH Level			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level			− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}			±10	µA
I_{SC}	Output Short Circuit Current	V_{CC}=5V, V_O=0.5V[10], T_A = 25°C		− 30	−135	mA
I_{CC}[11]	V_{CC} Current (See CR-1 for typical I_{CC})	V_{IN} = 0V or 3V, f = 25MHz, All outputs disabled[5]	I-10		145	mA
			I-15		145	mA
			I-25		75	mA
C_{IN} [8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz			6	pF
C_{OUT} [8]	Output Capacitance				12	pF

A.C. Electrical Characteristics Over the Operating Range [9,12]

Symbol	Parameter	I-10		I-15		I-25		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input [6] to non-registered output		10		15		25	ns
t_{OE}	Input [6] to output enable [7]		10		15		25	ns
t_{OD}	Input [6] to output disable [7]		10		15		25	ns
t_{CO1}	Clock to output		6		8		15	ns
t_{CO2}	Clock to comb. output delay via internal registered feedback		12		17		35	ns
t_{CF}	Clock to Feedback		4		5		9	ns
t_{SC}	Input [6] or feedback setup to clock	5		8		15		ns
t_{HC}	Input [6] hold after clock	0		0		0		ns
t_{CL},t_{CH}	Clock low time, clock high time [9]	4		6		13		ns
t_{CP}	Min clock period Ext (t_{SC} + t_{CO1})	11		18		30		ns
f_{max1}	Internal Feedback ($1/t_{SC}+t_{CF}$) [13]	111		76.9		41.6		MHz
f_{max2}	External Feedback($1/t_{CP}$) [13]	90.9		62.5		33.3		MHz
f_{max3}	No Feedback ($1/t_{CL}+t_{CH}$) [13]	125		83.3		38.4		MHz
t_{AW}	Asynchronous Reset pulse width	10		15		25		ns
t_{AP}	Input [6] to Asynchronous Reset		10		15		25	ns
t_{AR}	Asynchronous Reset recovery time		10		15		25	ns
t_{RESET}	Power-on reset time for registers in clear state		5		5		5	µs

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
5. I/O pins are 0V or 3V.
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. PEEL Device test loads are specified at the end of this section.
13. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

PEEL™22CV10A -7/-10/-15/L-15/-25
CMOS Programmable Electrically Erasable Logic Device

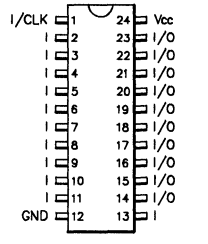
Features

- **High Speed/Low Power**
  - — Speeds ranging from 7ns to 25ns
  - — Power as low as 67mA at 25MHz
- **Electrically Erasable Technology**
  - — Superior factory testing
  - — Reprogrammable in plastic package
  - — Reduces retrofit and development costs
- **Development/Programmer Support**
  - — Third party software and programmers
  - — ICT PLACE Development Software and PDS-3 programmer
- **Architectural Flexibility**
  - — 132 product term X 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Up to 12 configurations per macrocell
  - — Synchronous preset, asynchronous clear
  - — Independent output enables
  - — 24-pin DIP, SOIC and 28-pin PLCC packages
- **Application Versatility**
  - — Replaces random logic
  - — Pin and JEDEC compatible with 22V10
  - — Enhanced Architecture fits more logic than ordinary PLDs

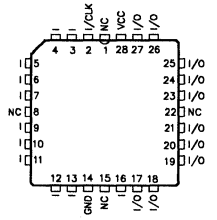
General Description

The PEEL22CV10A is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL22CV10A offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL22CV10A is available in 24-pin DIP, SOIC and 28-pin PLCC packages with speeds ranging from 7ns to 25ns with power consumption as low as 67mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability thus, assuring the highest quality possible. The PEEL22CV10A is JEDEC file compatible with standard 22V10 PLDs. Eight additional configurations per macrocell (a total of 12) are also available by using the "+" software/programming option (i.e, 22CV10A+). The additional macrocell configurations allow more logic to be put into every design. Development and programming support for the PEEL22CV10A is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

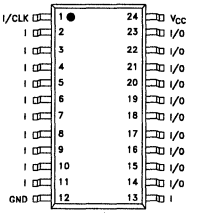
Pin Configuration (Figure 1)



DIP

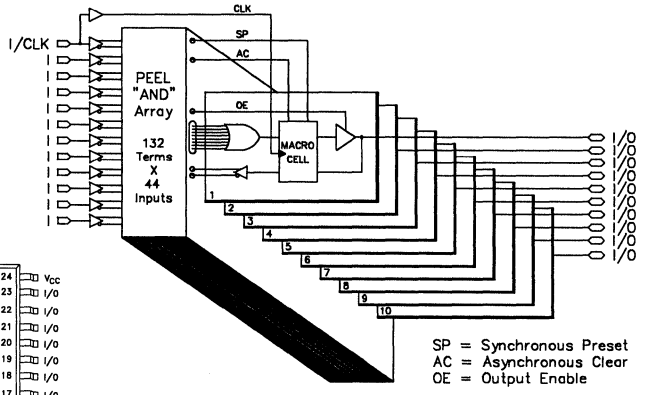


PLCC



SOIC

Block Diagram (Figure 2)



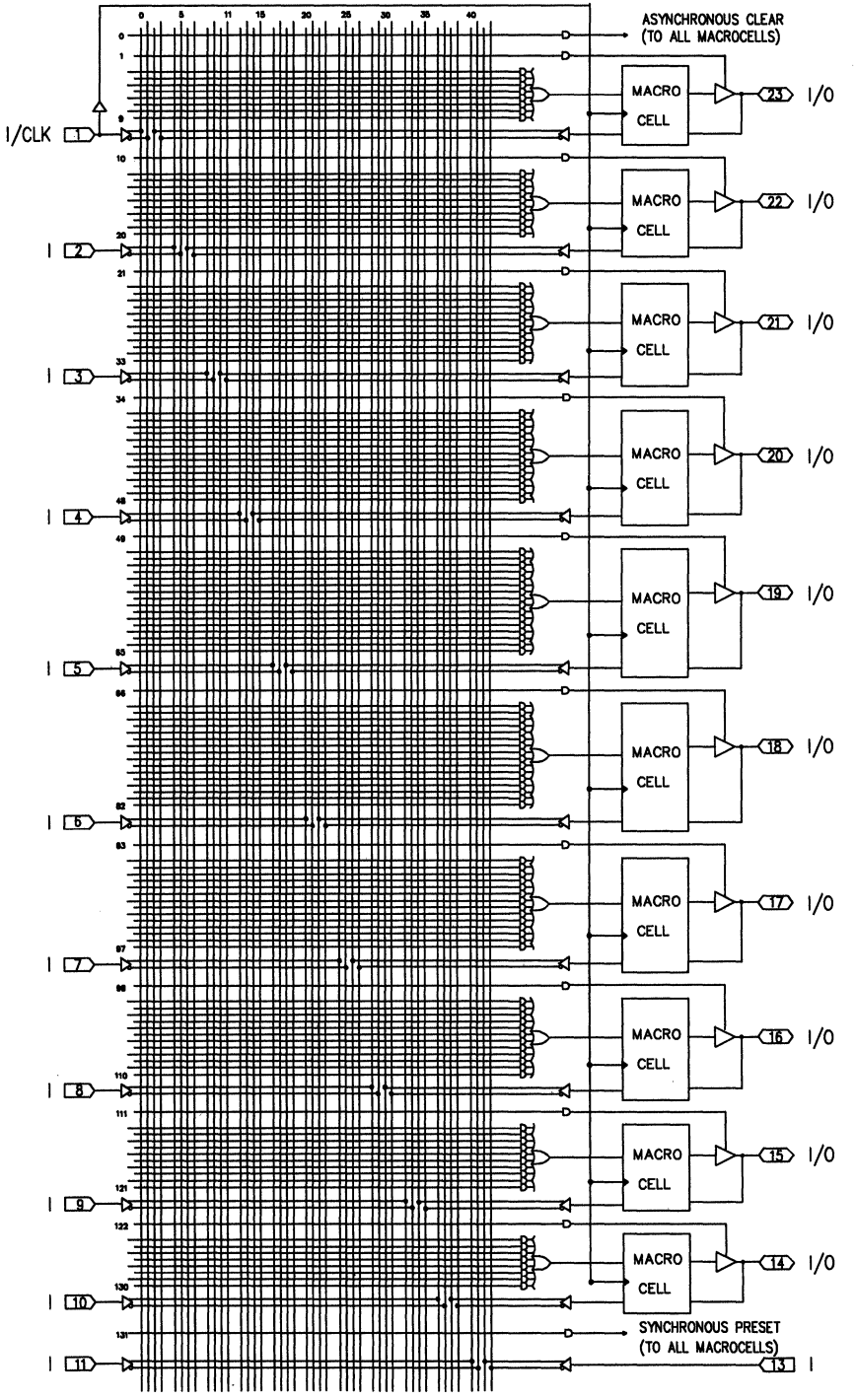


Figure 3. PEEL22CV10A Logic Array Diagram

Function Description
The PEEL22CV10A implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview
The PEEL22CV10A architecture is illustrated in the block diagram of figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure, the PEEL22CV10A can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 4 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions with either active-high or active-low polarity.

AND/OR Logic Array
The programmable AND array of the PEEL22CV10A (shown in figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

132 product terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12,14, and 16) used to form logical sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous present term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and compliment of an input signal will always be FALSE, and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL22CV10A, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is then configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program the connections on unused product terms so that they will have no effect on the output function)

Variable Product Term Distribution
The PEEL22CV10A provides 120 product terms to drive the 10 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see figure 3). This distribution allows optimum use of device resources.

Programmable I/O Macrocell
The output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL22CV10A to the precise requirements of their designs.

Macrocell Architecture
Each I/O macrocell, as shown in figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the two EEPROM bits controlling these multiplexers (refer to table 1). These bits determine output polarity and output type (registered or non-registered). Equivalent circuits for the four macrocell configurations are illustrated in figure 5.

Output Type
The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity
Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable
The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select
When configuring an I/O macrocell to implement a registered function (configurations 1 and 2 in Figure 5), the $\overline{Q}$ output of the flip-flop drives the feedback term. When configuring and I/O mcrocell to implement a combinatorial function (configurations 3 and 4 in Figure 5), the feedback signal is taken from the I/O pin. In this case, the pin can be used as a dedicated input or a bi-directionl I/O. (Refer also to Table 1)

Additional Macro Cell Configurations
Besides the standard four-configuration macro cell shown in figure 5, each PEEL22CV10A provides an additional eight configurations that can be used to increase design flexibility. The configurations are the same provided by the PEEL18CV8. However, to maintain JEDEC file compatibility with standard 22V10 PLDs the additional configurations can only be utilized by specifying the PEEL22CV10A+ for logic assembly and programming. To reference these additional configurations please refer to the PEEL22CV10A+ specifications at the end of this data sheet.

Design Security
The PEEL22CV10A provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word
The signature word feature allows a 24-bit code to be programmed into the PEEL22CV10A if the PEEL22CV10A+ software option is used. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

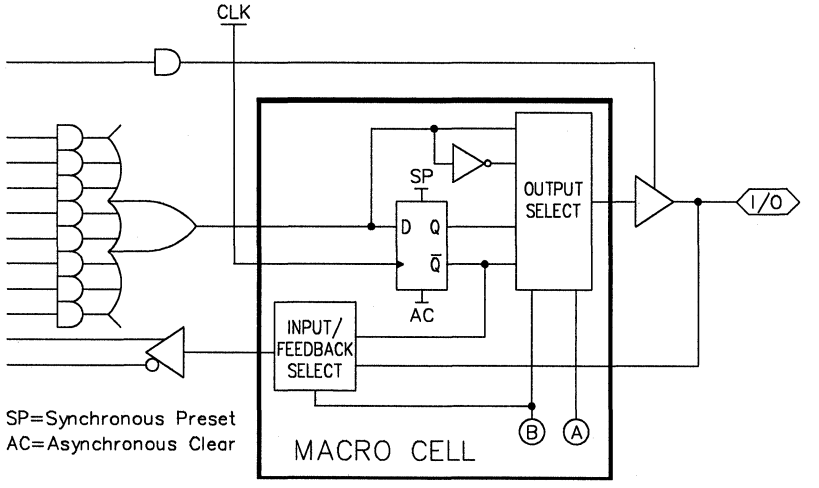


Figure 4. Block Diagram of the PEEL22CV10A I/O Macrocell

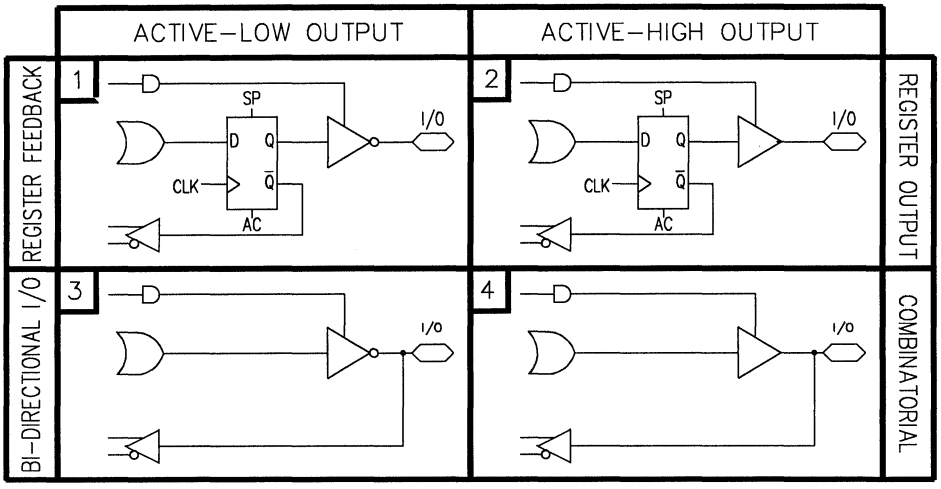


Figure 5. Equivalent Circuits for the Four Configurations of the PEEL22CV10A I/0 Macrocell.

Configuration			Input/Feedback Select	Output Select	
#	A	B			
1	0	0	Register Feedback	Register	Active Low
2	1	0			Active High
3	0	1	Bi-Directional I/O	Combinatorial	Active Low
4	1	1			Active High

Table 1. PEEL22CV10A Macrocell Configuration Bits

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+ 70	°C
T_R	Clock Rise Time	See note 4		20	ns
T_F	Clock Fall Time	See note 4		20	ns
T_{RVCC}	V_{CC} Rise Time	See note 4		250	ms

D.C. Electrical Characteristics

Over the operating range

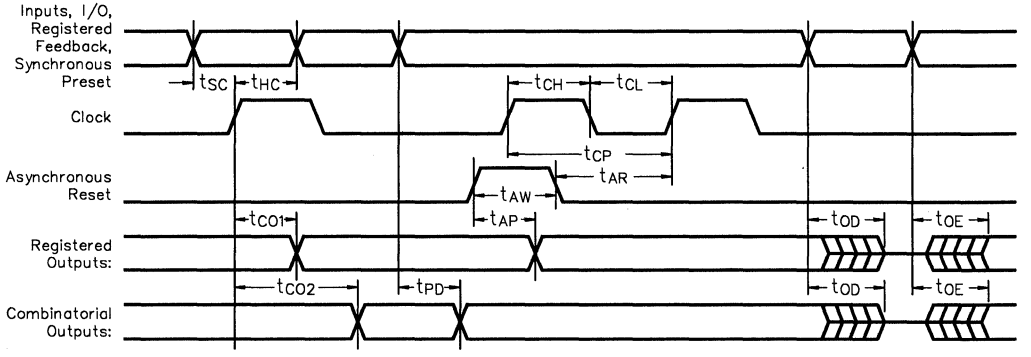
Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA		2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA		V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA			0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA			0.1	V
V_{IH}	Input HIGH Level			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level			− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}			±10	µA
I_{SC}	Output Short Circuit Current	V_{CC}=5V, V_O=0.5V[10], T_A = 25°C		− 30	− 135	mA
I_{CC}[11]	V_{CC} Current (See CR-1 for typical I_{CC})	V_{IN} = 0V or 3V f = 25MHz All outputs disabled[5]	-7		155	mA
			-10		135	mA
			-15		135	mA
			L-15		75	mA
			-25		67	mA
C_{IN} [8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz			6	pF
C_{OUT} [8]	Output Capacitance				12	pF

A.C. Electrical Characteristics

Over the Operating Range [9,12]

Symbol	Parameter	-7		-10		-15		L-15		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input [6] to non-registered output		7.5		10		15		15		25	ns
t_{OE}	Input [6] to output enable [7]		7.5		10		15		15		25	ns
t_{OD}	Input [6] to output disable [7]		7.5		10		15		15		25	ns
t_{CO1}	Clock to output		5.5		6		8		10		15	ns
t_{CO2}	Clock to comb. output delay via internal registered feedback		10		12		17		19		35	ns
t_{CF}	Clock to Feedback		3.5		4		5		6		9	ns
t_{SC}	Input [6] or feedback setup to clock	3		5		8		10		15		ns
t_{HC}	Input [6] hold after clock	0		0		0		0		0		ns
t_{CL},t_{CH}	Clock low time, clock high time [9]	3		4		6		7.5		13		ns
t_{CP}	Min clock period Ext (t_{SC} + t_{CO1})	8.5		11		18		20		30		ns
f_{max1}	Internal Feedback (1/t_{SC}+t_{CF}) [13]	142		111		76.9		62.5		41.6		MHz
f_{max2}	External Feedback(1/t_{CP}) [13]	117		90.9		62.5		50		33.3		MHz
f_{max3}	No Feedback (1/t_{CL}+t_{CH}) [13]	166		125		83.3		66.7		38.4		MHz
t_{AW}	Asynchronous Reset pulse width	7.5		10		15		15		25		ns
t_{AP}	Input [6] to Asynchronous Reset		7.5		10		15		18		25	ns
t_{AR}	Asynchronous Reset recovery time		7.5		10		15		18		25	ns
t_{RESET}	Power-on reset time for registers in clear state		5		5		5		5		5	µs

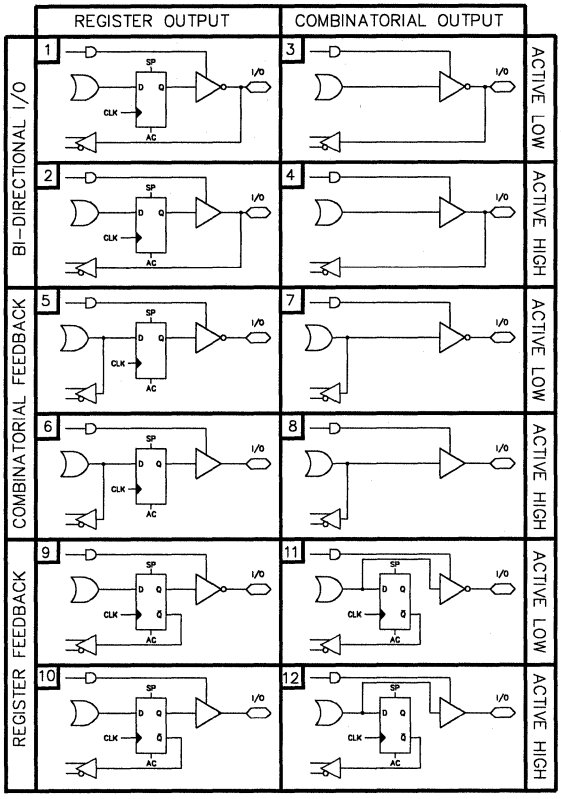
Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
5. I/O pins are 0V or 3V.
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. PEEL Device test loads are specified at the end of this section.
13. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

Additional Macro Cell Configurations

Besides the standard four-configuration macro cells, each PEEL22CV10A provides an additional eight configurations (twelve total) that can be used to increase design flexibility (see below). For logic assembly of all twelve configurations, specify PEEL22CV10A+, also select the PEEL22CV10A+ for programming.



Equivalent Circuits for the Twelve Configurations of the PEEL22CV10A+ I/0 Macrocell.

Configuration #	A B C D	Input/Feedback Select	Output Select	
1	0 0 1 0	Bi-Directional I/O	Register	Active Low
2	1 0 1 0	"	"	Active High
3	0 1 0 0	"	Combinatorial	Active Low
4	1 1 0 0	"	"	Active High
5	0 0 1 1	Combinatorial Feedback	Register	Active Low
6	1 0 1 1	"	"	Active High
7	0 1 1 1	"	Combinatorial	Active Low
8	1 1 1 1	"	"	Active High
9	0 0 0 0	Register Feedback	Register	Active Low
10	1 0 0 0	"	"	Active High
11	0 1 1 0	"	Combinatorial	Active Low
12	1 1 1 0	"	"	Active High

PEEL22CV10A+ Macrocell Configuration Bits

PEEL™22CV10A -5
CMOS Programmable Electrically Erasable Logic Device

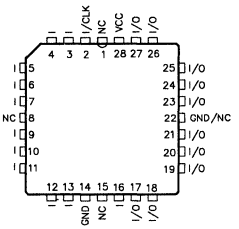
Features

- **0.8 µm CMOS EEPROM Technology**
- **High Speed**
  - — t_{PD} = 5ns, f_{max} = 181.8MHz
- **Electrically Erasable Technology**
  - — Superior factory testing
  - — Reprogrammable in plastic package
  - — Reduces retrofit and development costs
- **Development/Programmer Support**
  - — Third party software and programmers
  - — ICT PLACE Development Software and PDS-3 programmer
- **Architectural Flexibility**
  - — 132 product term X 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Up to 12 configurations per macrocell
  - — Synchronous preset, asynchronous clear
  - — Independent output enables
  - — 28-pin PLCC package
- **Application Versatility**
  - — Replaces random logic
  - — Pin and JEDEC compatible with 22V10
  - — Enhanced Architecture fits more logic than ordinary PLDs

General Description

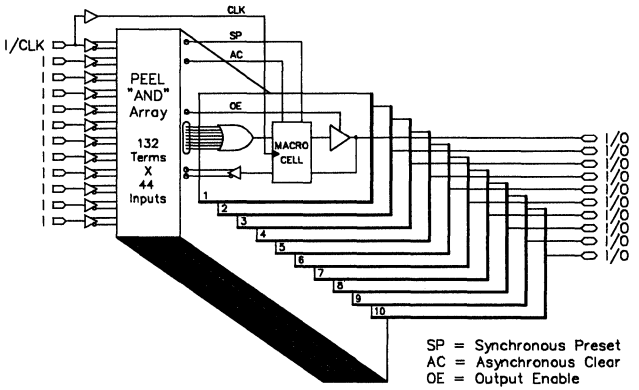
The PEEL22CV10A-5 is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL22CV10A-5 offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL22CV10A-5 is available in 28-pin PLCC package with power consumption of 140mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability thus, assuring the highest quality possible. The PEEL22CV10A-5 is JEDEC file compatible with standard 22V10 PLDs. Eight additional configurations per macrocell (a total of 12) are also available by using the "+" software/programming option (i.e, 22CV10A+). The additional macrocell configurations allow more logic to be put into every design. Development and programming support for the PEEL22CV10A is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

Pin Configuration (Figure 1)



PLCC

Block Diagram (Figure 2)



Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	– 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		– 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+70	°C
T_R	Clock Rise Time	See note 4		20	ns
T_F	Clock Fall Time	See note 4		20	ns
T_{RVCC}	V_{CC} Rise Time	See note 4		250	ms

D.C. Electrical Characteristics

Over the operating range

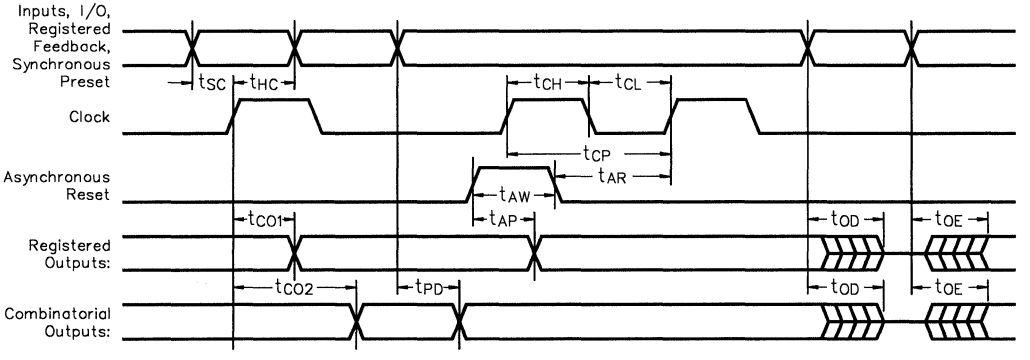
Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = –4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = –10µA	V_{CC} – 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 8mA		0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		– 0.3	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current	V_{CC}=5V, V_O = 0.5V [10], T_A = 25°C	– 30	–135	mA
I_{CC}	V_{CC} Current, Active	V_{IN} = 0V or 3V [5,11] f = 25MHz All outputs disabled		140	mA
C_{IN} [8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT} [8]	Output Capacitance			12	pF

A.C. Electrical Characteristics

Over the Operating Range [9,12]

Symbol	Parameter	22CV10A-5		Unit
		Min	Max	
t_{PD}	Input[6] to non-registered output		5	ns
t_{OE}	Input [6] to output enable [7]		5	ns
t_{OD}	Input [6] to output disable [7]		5	ns
t_{CO1}	Clock to output		4	ns
t_{CO2}	Clock to combinatorial output delay via internal registered feedback		7.5	ns
t_{CF}	Clock to Feedback		2.5	ns
t_{SC}	Input [6] or feedback setup to clock	3		ns
t_{HC}	Input [6] hold after clock	0		ns
t_{CL},t_{CH}	Clock width - clock low time, clock high time [4]	2.5		ns
t_{CP}	Min clock period Extenal (t_{SC} + t_{CO1})	7		ns
f_{max1}	Max clock freq. Internal Feedback ($1/t_{SC}+t_{CF}$)[13]	181.6		MHz
f_{max2}	Max clock freq. External ($1/t_{CP}$)[13]	142.8		MHz
f_{max3}	Max clock freq. No Feedback ($1/t_{CL}+t_{CH}$)[13]	200		MHz
t_{AW}	Asynchronous Reset pulse width	5		ns
t_{AP}	Input [6] to Asynchronous Reset		5	ns
t_{AR}	Asynchronous Reset recovery time		5	ns
t_{RESET}	Power-on reset time for registers in clear state [4]		5	µs

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
5. I/O pins are 0V or 3V.
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. PEEL Device test loads are specified at the end of this section.
13. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

PEEL™22CV10AI -10/-15/-25
CMOS Programmable Electrically Erasable Logic Device

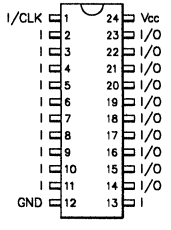
Features

- **Industrial Grade Specifications**
  - — V_{CC} = 4.5V to 5.5V, TA = -40°C to +85°C
  - — Reprogrammable 24-pin DIP, SOIC and 28-pin PLCC packages
- **High Speed/Low Power**
  - — Speeds ranging from 10ns to 25ns
  - — Power as low as 75mA at 25MHz
- **Development/Programmer Support**
  - — Third party software and programmers
  - — ICT PLACE Development Software and PDS-3 programmer
- **Architectural Flexibility**
  - — 132 product term X 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Up to 12 configurations per macrocell
  - — Synchronous preset, asynchronous clear
  - — Independent output enables
- **Application Versatility**
  - — Replaces random logic
  - — Pin and JEDEC compatible with 22V10
  - — Enhanced Architecture fits more logic than ordinary PLDs

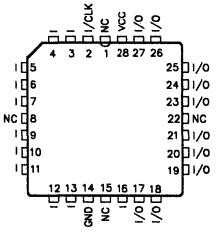
General Description

The PEEL22CV10AI is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL22CV10AI offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL22CV10AI is available in 24-pin DIP, SOIC and 28-pin PLCC packages with speeds ranging from 10ns to 25ns with power consumption as low as 75mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability thus, assuring the highest quality possible. The PEEL22CV10AI is JEDEC file compatible with standard 22V10 PLDs. Eight additional configurations per macrocell (a total of 12) are also available by using the "+" software/programming option (i.e, 22CV10A+). The additional macrocell configurations allow more logic to be put into every design. Development and programming support for the PEEL22CV10AI is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

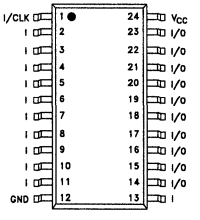
Pin Configuration (Figure 1)



DIP

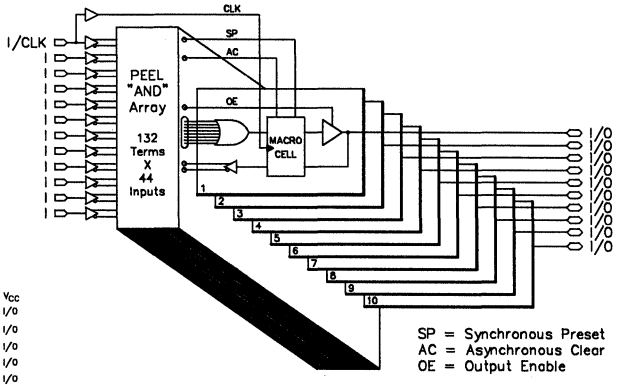


PLCC



SOIC

Block Diagram (Figure 2)



Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Industrial [2]	4.5	5.5	V
T_A	Ambient Temperature	Industrial [2]	-40	+ 85	°C
T_R	Clock Rise Time	See note 4		20	ns
T_F	Clock Fall Time	See note 4		20	ns
T_{RVCC}	V_{CC} Rise Time	See note 4		250	ms

D.C. Electrical Characteristics

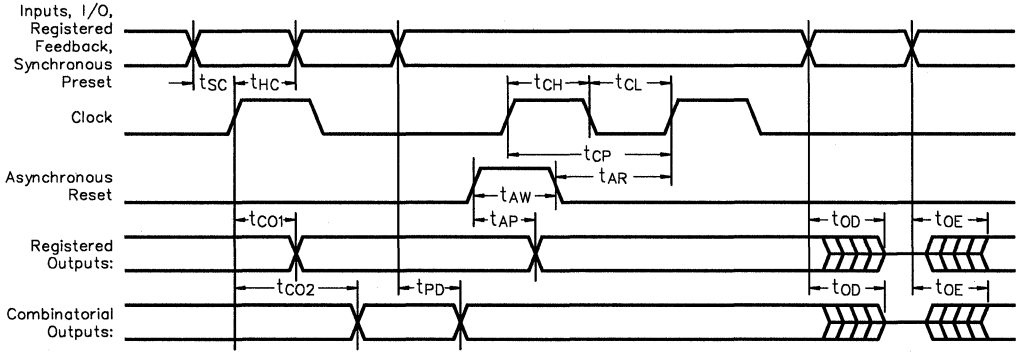
Over the operating range

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA		2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA		V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA			0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA			0.1	V
V_{IH}	Input HIGH Level			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level			− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}			±10	µA
I_{SC}	Output Short Circuit Current	V_{CC}=5V, V_O=0.5V[10], T_A = 25°C		− 30	-135	mA
I_{CC}[11]	V_{CC} Current (See CR-1 for typical I_{CC})	V_{IN} = 0V or 3V, f = 25MHz, All outputs disabled[5]	I-10		145	mA
			I-15		145	mA
			I-25		75	mA
C_{IN} [8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz			6	pF
C_{OUT} [8]	Output Capacitance				12	pF

A.C. Electrical Characteristics Over the Operating Range [9,12]

Symbol	Parameter	I-10		I-15		I-25		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input [6] to non-registered output		10		15		25	ns
t_{OE}	Input [6] to output enable [7]		10		15		25	ns
t_{OD}	Input [6] to output disable [7]		10		15		25	ns
t_{CO1}	Clock to output		6		8		15	ns
t_{CO2}	Clock to comb. output delay via internal registered feedback		12		17		35	ns
t_{CF}	Clock to Feedback		4		5		9	ns
t_{SC}	Input [6] or feedback setup to clock	5		8		15		ns
t_{HC}	Input [6] hold after clock	0		0		0		ns
t_{CL},t_{CH}	Clock low time, clock high time [9]	4		6		13		ns
t_{CP}	Min clock period Ext (t_{SC} + t_{CO1})	11		18		30		ns
f_{max1}	Internal Feedback ($1/t_{SC}+t_{CF}$) [13]	111		76.9		41.6		MHz
f_{max2}	External Feedback($1/t_{CP}$) [13]	90.9		62.5		33.3		MHz
f_{max3}	No Feedback ($1/t_{CL}+t_{CH}$) [13]	125		83.3		38.4		MHz
t_{AW}	Asynchronous Reset pulse width	10		15		25		ns
t_{AP}	Input [6] to Asynchronous Reset		10		15		25	ns
t_{AR}	Asynchronous Reset recovery time		10		15		25	ns
t_{RESET}	Power-on reset time for registers in clear state		5		5		5	µs

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
5. I/O pins are 0V or 3V.
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. PEEL Device test loads are specified at the end of this section.
13. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

PEEL™ 22V10AZ (5V), 22V10AZ3 (3V) Zero Power CMOS Programmable Electrically Erasable Logic Device

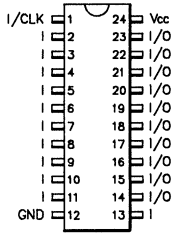
Features

- **Low Power, Low Voltage**
  - — I_{CC} = 10µA standby
  - — V_{CC} = 4.75V - 5.25V for 22V10AZ
    V_{CC} = 2.70V - 3.60V for 22V10AZ3
  - — t_{PD} = 15ns and 25ns versions
- **Electrically Erasable Technology**
  - — Superior factory testing
  - — Reprogrammable in plastic package
  - — Reduces retrofit and development costs
- **Development/Programmer Support**
  - — Third party software and programmers
  - — ICT PLACE Development Software and PDS-3 programmer
- **Architectural Flexibility**
  - — 132 product term X 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Up to 12 configurations per macrocell
  - — Synchronous preset, asynchronous clear
  - — Independent output enables
  - — 24-pin DIP, SOIC and 28-pin PLCC packages
- **Application Versatility**
  - — Replaces random logic
  - — Pin compatible with standard 22V10
  - — Ideal for power-sensitive systems
  - — Enhanced architecture options

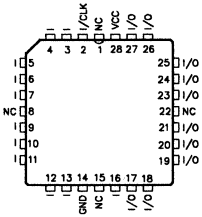
General Description

The PEEL22V10AZ and PEEL22V10AZ3 are Programmable Electrically Erasable Logic (PEEL) devices providing low power and low voltage alternatives to ordinary PLDs. The PEEL22V10AZ and PEEL22V10AZ3 are available in 24-pin DIP, SOIC, and 28-pin PLCC packages. A "zero-power" standby mode, makes the PEEL22V10AZ and PEEL22V10AZ3 ideal for power sensitive applications such as hand held meters, portable communication equipment and laptop computer/peripherals. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability thus, assuring the highest quality possible. The PEEL22V10AZ and PEEL22V10AZ3 are JEDEC file compatible with standard 22V10 PLDs. Eight additional configurations per macrocell (a total of 12) are also available by using the "+" software/programming option (i.e, 22V10AZ+). The additional macro cell configurations allow more logic to be put into every design. Development and programming support for the PEEL22V10AZ and PEEL22V10AZ3 is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

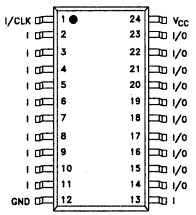
Pin Configuration (Figure 1)



DIP

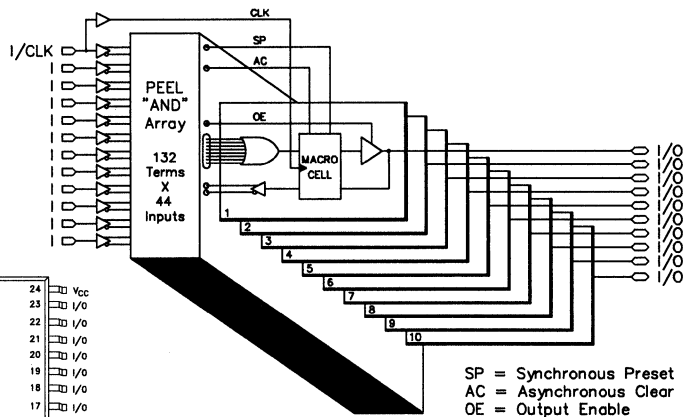


PLCC

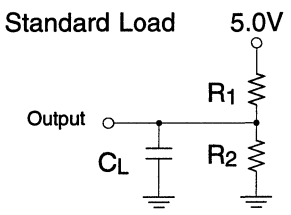


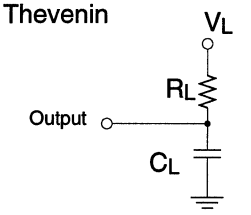
SOIC

Block Diagram (Figure 2)



PEEL Device and PEEL Array Test Loads





Part Number	Standard Loads				
	CMOS Interface		TTL Interface		
	R1	R2	R1	R2	C_L
PEEL18CV8	480KΩ	480KΩ	235Ω	159Ω	50pF
PEEL20CG10A	480KΩ	480KΩ	235Ω	159Ω	50pF
PEEL22CV10A	480KΩ	480KΩ	235Ω	159Ω	50pF
PA7024	480KΩ	480KΩ	235Ω	159Ω	50pF
PA7128	480KΩ	480KΩ	235Ω	159Ω	50pF
PA7140	480KΩ	480KΩ	235Ω	159Ω	50pF

Part Number	Thevenin Equivalent				
	CMOS Interface		TTL Interface		
	R_L	V_L	R_L	V_L	C_L
PEEL18CV8	228KΩ	2.375V	95Ω	2.02V	50pF
PEEL20CG10A	228KΩ	2.375V	95Ω	2.02V	50pF
PEEL22CV10A	228KΩ	2.375V	95Ω	2.02V	50pF
PA7024	228KΩ	2.375V	95Ω	2.02V	50pF
PA7128	228KΩ	2.375V	95Ω	2.02V	50pF
PA7140	228KΩ	2.375V	95Ω	2.02V	50pF

Development Tools

PLACE Advanced Development Software. 4-3
ABEL-to-PEEL Array Advanced Device Fitter 4-6
CUPL-to-PEEL Array Advanced Device Fitter. 4-7
PDS-3 PEEL Development System 4-8
Programming and Software Development Support List. . . 4-9

INC.

PLACE™ Advanced Development Software for PEEL Arrays and PEEL Devices

Features

- **PEEL Architectural Compiler and Editor**
  - — Advanced development support for PEEL Arrays and PEEL Devices
  - — Runs on IBM compatible system
  - — Fast and efficient design environment
- **Architectural Editing**
  - — Graphic display and control of architecture
  - — Equation and state machine entry
- **Logic Compilation**
  - — Auto-transformation to sum-of-products
  - — Five levels of logic reduction
- **Multi-level Logic Simulation**
  - — Simulates internal and external signals
  - — Interactive waveform editor and display
- **Translates Standard PLDs to PEEL Devices**
  - — Reads PLD (PAL, GAL, EPLD) JEDEC file then automatically translates to PEEL Devices
- **Programmer Interface**
  - — Interfaces to ICT's PDS and popular third party programmers

General Description

PLACE is an advanced development software package offering complete support for ICT's family of PEEL (Programmable Electrically Erasable Logic) Arrays and Devices. The innovative PLACE architectural editor graphically controls the architecture, logic equations, truth tables, and state machine entry, making the overall design easy to understand. The PLACE compiler performs logic transformation so equations can be defined in most any fashion. The compiler also features five levels of user-selectable logic reduction, including auto-demorganization, making it possible to fit more logic into every design. PLACE also provides a multi-level logic simulator that lets the external and internal signals be fully simulated, analyzed and edited via a special waveform display. Documentation of PLACE designs is accomplished through batch printing of equations, architecture and waveform displays. System requirements for PLACE are: IBM PC compatible system with DOS version 3.0 or greater, 512K memory, EGA or VGA graphics and mouse. PLACE also supports expanded memory systems with EMS drivers conforming to the 3.2 or greater LIM EMS specification.

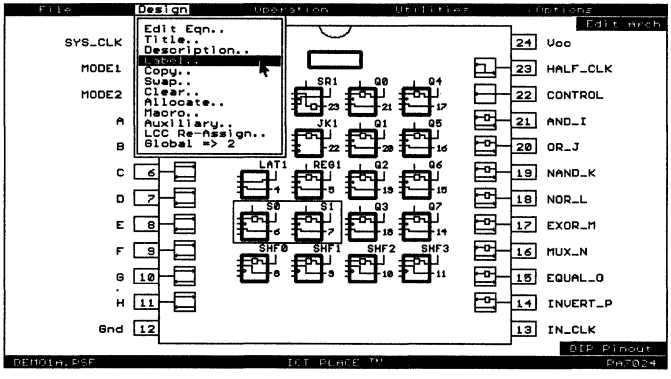


Figure 1. The PLACE architectural editors "chip display" provides a global view of design allowing quick access to I/Os, registers, cells and equations.

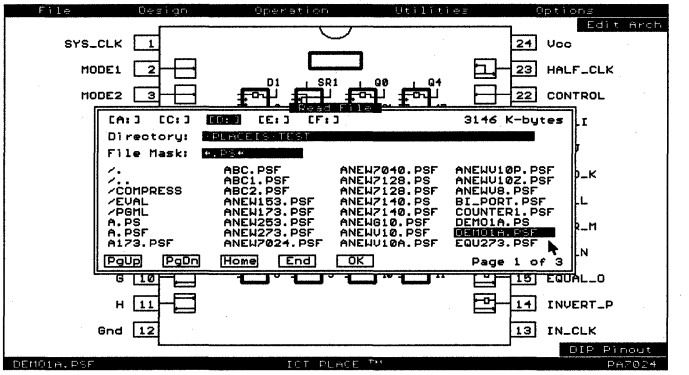


Figure 2, The PLACE software functions in a mouse driven windows environment allowing easy access and control of all operations. Shown here is the file selection window.

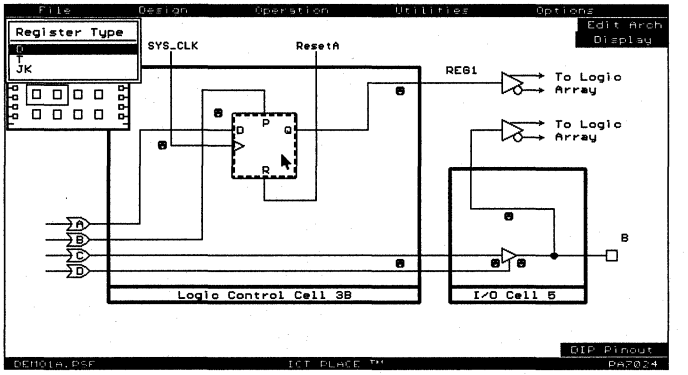


Figure 3, The architecture of each cell can be specified by selecting the desired architectural element with the mouse and then "clicking" through all possible configurations graphically on the screen. Shown here is the PA7024s register selection of D, T or JK flip-flops.

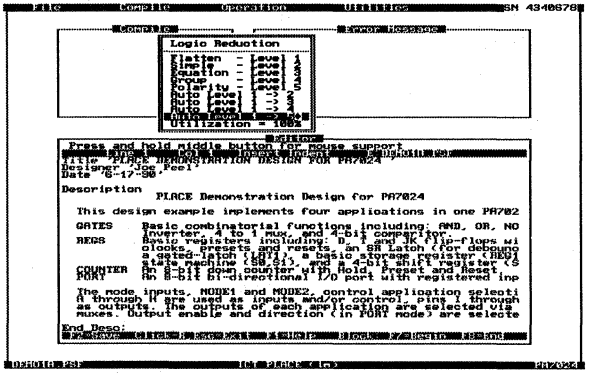


Figure 4, The PLACE compiler performs logic transformation, and hence allowing designs to be specified in any fashion (i.e. equation, state-diagram or truth-table). The compiler also features five levels of user-selectable logic reduction, making it possible to fit more logic into every design.

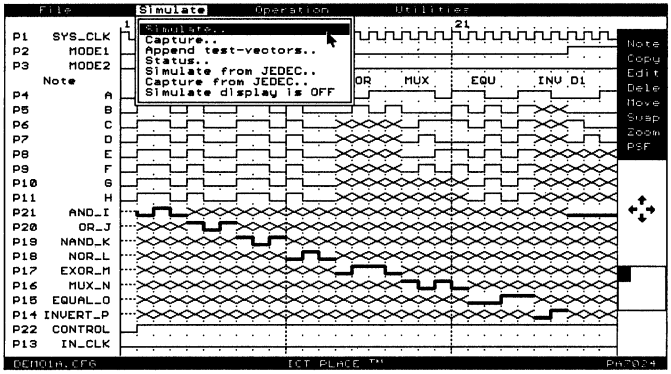


Figure 5, The PLACE logic simulator lets external and internal signals be fully simulated, analyzed and edited via a special waveform display. Output signals can be "captured" or simulated. Simulation errors are marked on the display for quick analysis.

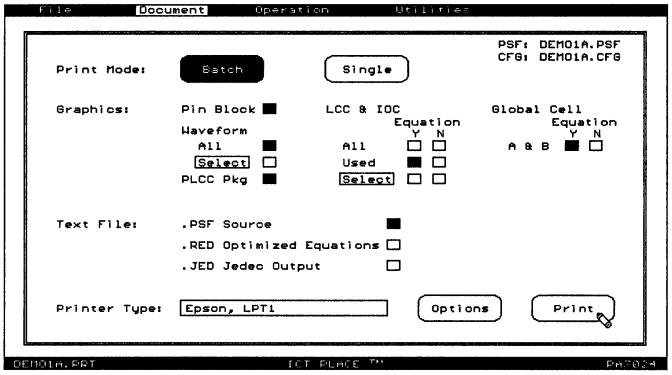


Figure 6, PLACE designs can be documented through batch or single printing of architectures, waveform displays and logic description such as equations, state-diagram and truth-table syntax.

INC.

ABEL-to-PEEL™ Advanced Device Fitter

Features

- **PEEL Array Support for ABEL Software**
  - — Supports PA7024, 7128 and 7140
  - — Operates with ABEL 4.0 or greater
- **Maintains ABEL Design Methodology**
  - — Design, compile, simulate with ABEL
  - — Fitter creates JEDEC programming files
  - — Operates on "Berkeley Espresso" PLA files
- **True Device Independent Design Entry**
  - — I/O pin and node numbers need not be specified
  - — Optimizes cell and I/O placement for best fit
  - — Eases conversion from other PLD designs
- **Translation to PLACE Source File**
  - — Optionally creates PLACE ".psf" source file
  - — Allows architectural viewing of design
  - — Alternate compiler for complex designs
  - — JEDEC file waveform simulator
- **PEEL Array ABEL Design Examples**
  - — Numerous examples provided for reference
  - — Combinatorial, synchronous, asynchronous applications
- **System Requirements**
  - — PC compatibles (DOS 3.0 or greater)
  - — Sun SPARCstations (Sun OS 4.0.3 or greater)

General Description

ABEL-to-PEEL (v2.0) Advanced Device Fitter allows designers to create programming files for ICT's PEEL Array family (PA7024, PA7128, PA7140) using ABEL 4.0 (or greater) high-level design language from Data I/O. The ABEL development methodology is fully maintained through design entry, compilation and functional simulation. The fitter operates on "Berkeley Espresso" PLA files, that are produced by the ABEL compiler, and creates PEEL Array JEDEC programming files. ABEL-to-PEEL Advanced Device Fitter provides true independent design entry, therefore, it is not necessary to specify pin numbers, node numbers, global clock, reset or preset nodes. The fitter automatically optimizes the placement of logic cells and I/Os for the best fit. This feature eases the conversion from other PLD designs. A detailed description of the configuration selected by the fitters is stored in a ".log" file. The fitter also allows use of the PLACE software by optionally creating a ".psf" extension file which allows for architectural viewing of the design in PLACE software. This makes it possible to simulate test vectors stored in the JEDEC file while using the PLACE software. Numerous PEEL Array ABEL design examples using combinatorial, synchronous and asynchronous designs are provided for reference. The ABEL-to-PEEL Fitter operates on PC compatibles with DOS 3.0 or Sun SPARCstations with Sun OS 4.0.3 or greater.

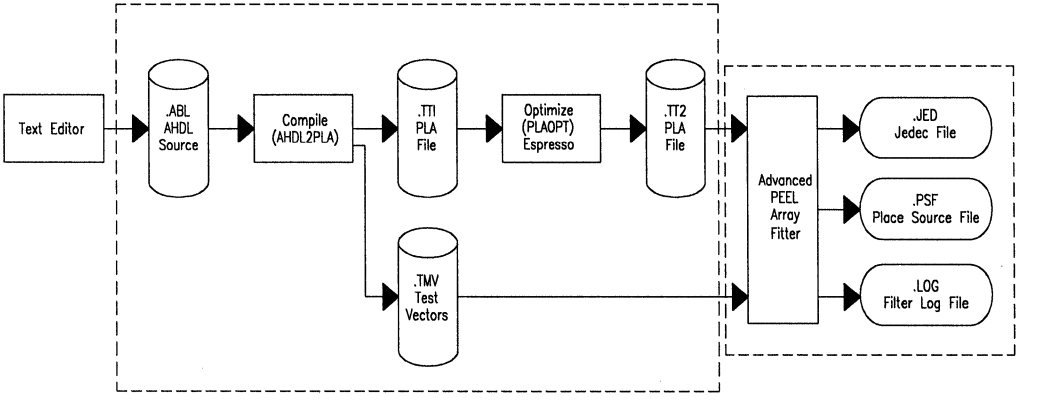


Figure 1. Design flow with ABEL-to-PEEL Advanced Fitter

INC.

CUPL-to-PEEL™ Advanced Device Fitter

Features

- **PEEL Array Support for CUPL Software**
  - — Supports PA7024, 7128 and 7140
  - — Operates with CUPL 4.4 or greater
- **Maintains CUPL Design Methodology**
  - — Design, compile, simulate with CUPL
  - — Fitter creates JEDEC programming files
  - — Operates on "Berkeley Espresso" PLA files
- **True Device Independent Design Entry**
  - — I/O pin and node numbers need not be specified
  - — Optimizes cell and I/O placement for best fit
  - — Eases conversion from other PLD designs
- **Translation to PLACE Source File**
  - — Optionally creates PLACE ".psf" source file
  - — Allows architectural viewing of design
  - — Alternate compiler for complex designs
  - — JEDEC file waveform simulator
- **PEEL Array CUPL Design Examples**
  - — Numerous examples provided for reference
  - — Combinatorial, synchronous and asynchronous applications
- **System Requirements**
  - — PC compatibles (DOS 3.0 or greater)
  - — Sun SPARCstations (Sun OS 4.0.3 or greater)

General Description

CUPL-to-PEEL (v2.0) Advanced Device Fitter allows designers to create programming files for ICT's PEEL Array family (PA7024, PA7128, PA7140) using CUPL 4.4 (or greater) high-level design language from Logical Devices. The CUPL development methodology is fully maintained through design entry, compilation and functional simulation. The fitter operates on "Berkeley Espresso" PLA files, that are produced by the CUPL compiler, and creates PEEL Array JEDEC programming files. CUPL-to-PEEL Advanced Device Fitter provides true independent design entry, therefore, it is not necessary to specify pin numbers, node numbers, global clock, reset or preset nodes. The fitter automatically optimizes the placement of logic cells and I/Os for the best fit. This feature eases the conversion from other PLD designs. A detailed description of the configuration selected by the fitters is stored in a ".log" file. The fitter also allows use of the PLACE software by optionally creating a ".psf" extension file which allows for architectural viewing of the design in PLACE software. This makes it possible to simulate test vectors stored in the JEDEC file while using the PLACE software. Numerous PEEL Array CUPL design examples using combinatorial, synchronous and asynchronous designs are provided for reference. CUPL-to-PEEL Fitter operates on PC compatibles with DOS 3.0 or greater or Sun SPARCstations with Sun OS 4.0.3 or greater.

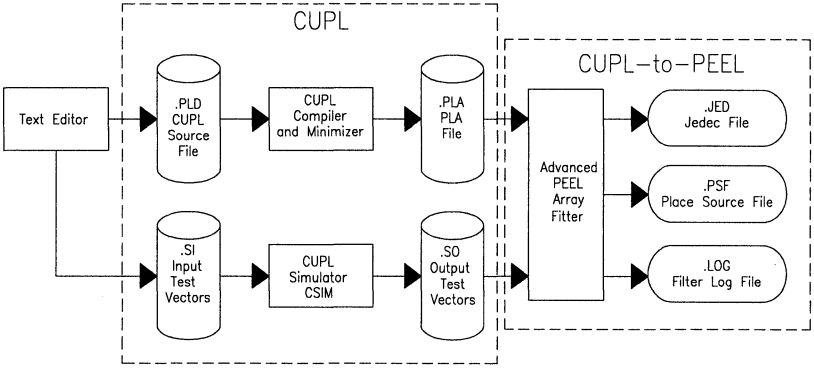


Figure 1. Design Flow for CUPL-to-PEEL Advanced Fitter

INC.

PDS-3 PEEL™ Development System

Features

- **Development System for PEEL Products**
  - PLACE Advanced Development Software
  - PDS-3 Programmer
- **Design from Concept to Silicon**
  - Editor, logic compiler, simulator, translator, programmer, tester in one system
- **Supports PEEL Devices and PEEL Arrays**
  - PEEL 18CV8, 20CG10A, 22CV10A
  - PA7024, PA7128, and PA7140
- **Handles DIP, PLCC, and SOIC Packages**
  - Standard 40-pin 300-600mil DIP ZIF socket
  - Optional PLCC and SOIC adapters
- **Programmer Functions**
  - Program, read, verify, secure
  - Functional test via JEDEC file vectors
  - Checksum, position and continuity check, blank check, illegal-bit check, auto-sense
- **Translate Standard PLDs to PEEL Devices**
  - Reads most PLDs (e.g., PAL GAL EPLD)
  - PLACE translator automatically converts design for programming PEEL Devices
- **System Requirements**
  - IBM PC compatible with DOS 3.0 or greater
  - 640K bytes RAM minimum
  - Serial port for programmer upload/download

General Description

The PEEL Development System (PDS-3) is a powerful, yet inexpensive, PC-based system for designing with Programmable Electrically Erasable Logic (PEEL) products. Equipped with ICT's PLACE Development Software (see PLACE data sheet), the PDS-3 programmer has everything needed to create PEEL Device/Array designs from concept to silicon. The standard 40-pin DIP zero-insertion-force socket handles DIP packages from 20 to 40 pins, as well as PLCC and SOIC packages using optional adapters. All standard programming functions are supported including: program, read, verify and secure. Test vectors from the JEDEC file can be applied to the device for functional verification. Built-in features ensure device integrity and reliable programming including: checksum, position/continuity check, blank check, and illegal-bit check. The auto-sense features automatically activates the PDS-3 in response to the socket without any key presses. The PDS-3 can read most any PLD (e.g., PAL, GAL, EPLD) for conversion to a PEEL Device using the PLACE translator. System requirements include IBM PC compatibility with DOS 3.0 or greater, 640K RAM and serial port. Note: the PDS-3 can be upgraded to a universal PLD and memory programmer, contact ICT for more information.

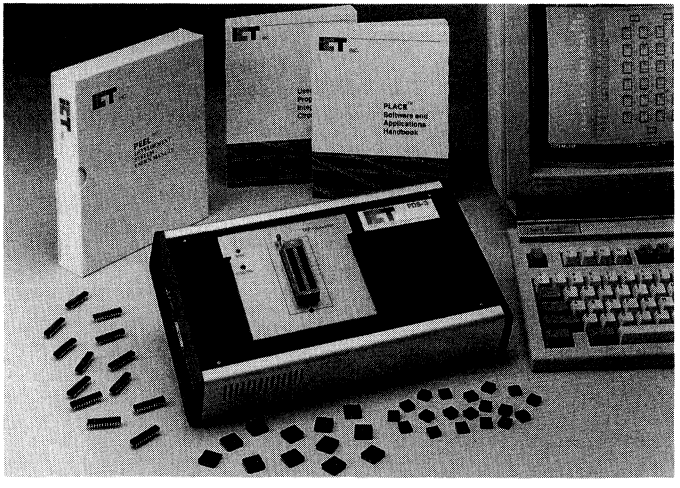


Figure 1. PDS-3 Development System

Programming Support (as of August 1993)

ICT, INC. (408) 434-0678*

	PDS-1 PEEL™ Development System	
ICT Part Number	**Software**	**Adapter**
PEEL18CV8	PDS-1 V3.60, PLACE V2.01	PLCC PDA-20, SOIC 20SO30A
PEEL22CV10	PDS-1 V3.20, PLACE V2.01	PLCC PDA-24, SOIC 24SO30
PEEL22CV10Z		
PEEL20CG10		
PA7024	PLACE V1.08B	
PEEL22CV10A	PDS-1 V3.56, PLACE V2.01	
PEEL22CV10A+	PDS-1 V3.57, PLACE V2.01	

ICT, INC. (408) 434-0678*

	PDS-2 PEEL™ Development System	
ICT Part Number	**Software**	**Adapter**
PEEL18CV8	PLACE V2.10	PLCC PDA-20, SOIC 20SO30A
PEEL22CV10		PLCC PDA-24, SOIC 24SO30
PEEL22CV10Z		
PEEL20CG10		
PA7024		
PEEL22CV10A		
PEEL22CV10A+		

ICT, INC. (408) 434-0678*

	PDS-3 PEEL™ Development System	
ICT Part Number	**Software**	**Adapter**
PEEL18CV8	PLACE V2.30 and PDS-3 V1.00	PLCC PDA-20, SOIC 20SO30A
PEEL22CV10		PLCC PDA-24, SOIC 24SO30
PEEL22CV10Z		
PEEL20CG10		
PEEL22CV10A		
PEEL22CV10A+		
PEEL20CG10A		
PA7024		
PA7128	PLACE V2.30 and PDS-3 V1.01	PLCC P28D28, SOIC 28SO30A
PA7140	PLACE V2.40 and PDS-3 V1.01	PLCC P44D40

* BBS # for ICT is (408) 434-0130 (2400bps, N, 8, 1)

Advantech (408) 245-6678

	PC-UPROG
ICT Part Number	**Software**
PEEL18CV8	V1.2
PEEL22CV10	
PEEL22CV10Z	
PEEL20CG10	
PEEL22CV10A	
PEEL22CV10A+	
PEEL20CG10A	V1.7
PA7024	V1.8
PA7128	V1.9
PA7140	

Advin Systems (408) 243-7000

	Pilot-U40
ICT Part Number	**Software**
PEEL18CV8	V8.0
PEEL22CV10	V9.4
PEEL22CV10Z	V9.5
PEEL20CG10	
PEEL22CV10A	V9.94
PEEL22CV10A+	
PEEL20CG10A	V10.50
PA7024	V10.03
PA7128	Contact Advin
PA7140	

Aval Data Corp. Japan (033) 344-2001 Ireland 353-1-892136

	PKW-1100	
ICT Part Number	**Adapter**	**Firmware**
PEEL18CV8	Contact	V1.0
PEEL22CV10	Aval	V1.2
PEEL22CV10Z		
PEEL20CG10	Contact Aval	
PEEL22CV10A		
PEEL22CV10A+		
PEEL20CG10A		
PA7024		
PA7128		
PA7140		

BP Microsystems (800) 225-2102*

	PLD 1100 /CP 1128/CP1200
ICT Part Number	**Software**
PEEL18CV8	V1.07
PEEL22CV10	V1.53
PEEL22CV10Z	
PEEL20CG10	
PEEL22CV10A	
PEEL22CV10A+	
PEEL20CG10A	V2.19
PA7024	V1.53
PA7128	V2.24
PA7140	

Bytek Corp. (407) 994-3520

	U135H - U/A
ICT Part Number	**Software**
PEEL18CV8	V15
PEEL22CV10	
PEEL22CV10Z	
PEEL20CG10	
PEEL22CV10A	
PEEL22CV10A+	
PEEL20CG10A	Contact Bytek
PA7024	V15
PA7128	Contact Bytek
PA7140	

Owen Electronics US (415) 324-1094 Germany (06381) 4202-0 **

	AP-II+/AP-III+
ICT Part Number	**Software**
PEEL18CV8	V1.8B/V1.8B /V3.0
PEEL22CV10	V2.01/V2.02B/V3.0
PEEL20CG10	
PEEL22CV10Z	
PEEL22CV10A	
PEEL22CV10A+	
PEEL20CG10A	
PA7024	V3.2
PA7128	
PA7140	

* BBS # for BP Microsystems is (713) 688-9283
**BBS # for Owens Electronics is 49-6381-4202-22

DATA I/O (800) 426-1045 *

	Unisite with Site 40/48 Adapter		
ICT Part Number	**Software**	**Family**	**Pinout**
PEEL18CV8	V1.4	8D	3A
PEEL22CV10	V2.3		28
PEEL22CV10Z			A3
PEEL20CG10	V2.2		56
PEEL22CV10A	V3.4	A6	28
PEEL22CV10A+			A3
PEEL20CG10A	V4.0		
PA7024	V3.2	141	027
PA7128	Contact Data I/O		
PA7140			

Unisite Chipsite/Pinsite Adapter **		
Software	**Family**	**Pinout**
V2.5	8D	3A
V2.6		28
V2.7		A3
Contact Data I/O		
V3.6	A6	28
		A3
V4.0		
V3.2	141	027
Contact Data I/O		

	*2900 /3900***		
ICT Part Number	**Software**	**Family**	**Pinout**
PEEL18CV8	V1.0/V1.0	8D	3A
PEEL22CV10			28
PEEL20CG10			56
PEEL22CV10Z			A3
PEEL22CV10A	V1.7/V1.1	A6	28
PEEL22CV10A+			A3
PEEL20CG10A	V3.0		
PA7024	V1.6/V1.0	141	027
PA7128	Contact Data I/O		
PA7140			

** These programmers or adapters are qualified via the Unisite programmer.

	Model 60A		*Model 60H*		
ICT Part Number	**Adapter**	**Firmware**	**Firmware**	**Family**	**Pinout**
PEEL18CV8	360A-001	V11	V12	8D	3A
PEEL22CV10		V14	V14		28
PEEL22CV10Z					A3
PEEL20CG10		V16	V16		56
PEEL22CV10A	360A-006	V14	V14		3A
PEEL22CV10A+					28

	Model 29B Programmer			
ICT Part Number	**Module**	**Adapter / Firmware**	**Family**	**Pinout**
PEEL18CV8	LogicPak™ V04	303A-011A / V02	8D	3A
PEEL22CV10		303A-011A / V09		28
PEEL22CV10Z		303A-011A / V06		A3
PEEL20CG10				56
PEEL22CV10A		303A-011B / V14	A6	28
PEEL22CV10A+				A3

* Keep-Current-Express BBS
USA (206) 881-3465
UK 44-734-4448913
Germany 49-89-858-5880
Japan 81-33-436-0205

Logical Devices (305) 974-0967

	ALLPRO 40 / 88
ICT Part Number	**Software**
PEEL18CV8	V1.44
PEEL22CV10	V1.47
PEEL22CV10Z	V2.1
PEEL20CG10	
PEEL22CV10A	V2.2
PEEL22CV10A+	
PEEL20CG10A	V2.3
PA7024	V2.1
PA7128	V2.4
PA7140	

	ALLPRO-88 XR
ICT Part Number	**Software**
PEEL18CV8	V1.0
PEEL22CV10	
PEEL22CV10Z	
PEEL20CG10	
PEEL22CV10A	
PEEL22CV10A+	
PEEL20CG10A	V1.2.8
PA7024	V1.0
PA7128	Contact Logic Devices
PA7140	

	PALPRO-2X Programmer
ICT Part Number	**Firmware**
PEEL18CV8	V5.2

	PROMPRO-8X Programmer
ICT Part Number	**Firmware**
PEEL18CV8	V5.2

SMS Microcomputer Systems (206) 883-8447, Germany 7522-5018

	Sprint Expert/Plus
ICT Part Number	**Software**
PEEL18CV8	#1/92
PEEL22CV10	
PEEL22CV10Z	#3/92
PEEL20CG10	
PEEL22CV10A	
PEEL22CV10A+	
PEEL20CG10A	
PA7024	
PA7128	Contact SMS
PA7140	

Stag Microsystems (408) 988-1118

	PPZ	
ICT Part Number	**Module**	**Firmware**
PEEL18CV8	ZM2200	V34
PEEL22CV10	ZM3000	V11.0
PEEL22CV10Z		
PEEL20CG10	Contact Stag	
PEEL22CV10A		
PEEL22CV10A+		
PEEL20CG10A		
PA7024		
PA7128		
PA7140		

ZL-30A	
Module	**Firmware**
30A800 A	V30A26
	V30A36
	V30A41
	V30A45
	V30A41
Contact Stag	

System 3000
Firmware
N/A
V11.0
V10.0
Contact Stag

System General

USA (408) 263-6667
Taiwan 2-917-3005

ICT Part Number	*TURPRO-1* Software
PEEL18CV8	V1.0
PEEL22CV10	
PEEL20CG10	
PEEL22CV10Z	V1.68
PEEL22CV10A	
PEEL22CV10A+	
PEEL20CG10A	
PA7024	
PA7128	1.68K
PA7140	

Xeltek (408) 524-1929

ICT Part Number	*SuperPro* ❖/II Software
PEEL18CV8	V1.0
PEEL22CV10	
PEEL22CV10Z	
PEEL20CG10	
PEEL22CV10A	
PEEL22CV10A+	
PEEL20CG10A	V1.7A
PA7024	V1.0
PA7128	V1.7B
PA7140	V1.7C

PEEL Development Software Support

ICT Part Number (*1)	ICT PLACE™	Data I/O ABEL™	Logical Dev. CUPL™	Isdata LOG/iC™	Minc PLDesigner™
PEEL18CV8	V 2.01	V 2.1	V 2.15	V3.2	V 2.0
PEEL22CV10					V 1.5
PEEL20CG10		V 3.0	V 3.00		V 2.0
PEEL22CV10Z					V 2.2
PEEL22CV10A (*4)		V 2.1	V 2.15		V 1.5
PEEL22CV10A+ (*4)		V 3.0	V 3.00		V 2.2
PEEL20CG10A	V2.20				V 2.0
PA7024	V1.08B	V 4.0 (*2)	V 4.2 (*2)	*3	*3
PA7128	V2.30				
PA7140	V2.40				

*1 Version numbers equal to, or greater than, will support the specified ICT device according to manufacturers claims.

*2 For PEEL Array support by ABEL or CUPL the ABEL-to-PEEL fitter software or CUPL-to-PEEL fitter software from ICT is required. Please contact an ICT representative for more information.

*3 Support in progress. Contact third-party software manufacturer or ICT for updated information.

*4 Use the PEEL22CV10 device types when designing with the PEEL22CV10A and PEEL22CV10A+ devices. The PEEL22CV10A is JEDEC compatible with PEEL22CV10, and the PEEL22CV10A+ is compatible with PEEL22CV10Z.

For updated information on software support, please contact ICT (408) 434-0678, Data I/O (800) 426-1045, Logical Devices (305) 974-0697, Isdata (408) 373-7359, and Minc, Inc. (719) 590-1155.

Application Notes and Reports

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CR-1 PEEL Device Characterization Report 5-17
RR-1 1 μm CMOS PEEL Product Reliability Report 5-21

Logical Design Techniques for PEEL™ Devices

Introduction

Logic designers are confronted with a variety of new programmable logic device (PLD) architectures and technologies. Even after sorting through a multitude of PLD data sheets, selecting the right PLD for a given application can often become a trial and error process. Understanding the design techniques associated with PLD architectures can greatly minimize design effort and maximize logic utilization.

This application note addresses techniques used to design with PEEL™ (Programmable Electrically Erasable Logic) devices. The examples provided will demonstrate how architecturally enhanced PEEL devices can achieve higher logic integration and flexibility than ordinary PLDs.

PEEL Device Overview

PEEL devices (Programmable Electrically Erasable Logic devices) provide an attractive alternative by offering the performance, flexibility, ease of design, and production practicality needed by logic designers today. Key features of PEEL devices include:

PEEL Performance provides speeds as fast as 5ns t_{pd} with power as low as 37mA at 25 MHz.

PEEL Architectural Flexibility allows PEEL devices to functionally replace over 40 PLD architectures (i.e. PAL, GAL, EPLD), reducing the number of different parts needed in inventory. Additionally, PEEL enhanced architectures make it possible to put more logic into every package.

PEEL Ease of Design is provided by free PLACE Development Software, a low cost PEEL Development System and support from popular third party programmers and development software.

PEEL EE-Reprogrammability provides the convenience of instant reprogramming for development, no waste as with one-time-programmable PLDs, and no wait as with UV EPLDs. It also allows for a risk-free re-usable production inventory minimizing the impacts of programming changes or errors. EE-Reprogrammability also improves factory testability thus, assuring the highest quality possible.

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Independent Output Enables
Bi-Directional Registered I/O
Buried Combinatorial Feedback
Buried Combinatorial Feedback with Register
Buried Register with Combinatorial Output
Application Examples
Bus-Programmable Multiplexer
Input Synchronizer
8-Bit Counter with Function Controls
Change-0f-State Detection Port
Conclusion

PEEL Device Family

The PEEL device family includes three primary devices architectures, the PEEL 18CV8, 20CG10A, and 22CV10A. The basic architectures of the 18CV8, 20CG10A and 22CV10A are similar. Both implement sum-of-products logic with a programmable-AND/fixed-OR structure. Depending on the device, between 18 to 22 inputs and 8 to 10 macrocell outputs are available (see figure 1).

The core of each device is a programmable, electrically-erasable AND array consisting of input lines running perpendicular to product terms. The input lines are derived from the true and compliment of each potential input pin. The product terms include: one global synchronous preset term; one global asynchronous clear term; one output enable term per I/O; and groups of 8 logic product terms per sum for PEEL18CV8 and 20CG10A, or a distribution of 8-16 terms per sum for the 22CV10A.

I/O Macrocell Configurability

Each logical sum is directly associated with an I/O macrocell and I/O pin. The macrocell consists of a D-type flip-flop, an output mux, and a feedback mux. Four EE memory cells per macro-cell can program

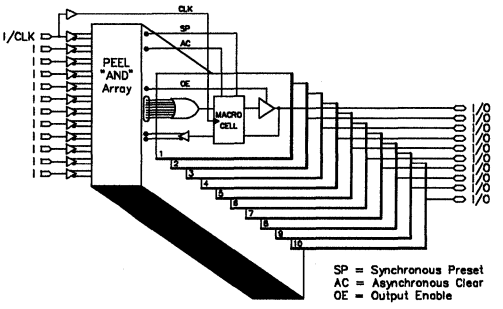


Figure 1. PEEL Device Block Diagram

the configuration of each macro cell twelve different ways. The twelve possible I/O macrocell configurations are illustrated in figure 2. The twelve-configurations provide control of output polarity, feedback path and output type (registered or combinatorial, dedicated input, output, or bidirectional I/O).

Most other PLD macrocells are fixed configurations having four or fewer possible configurations. The flexibility of the I/O macrocell not only makes these devices ideal for sequential or combinatorial applications, but also allows implementation of functions that might require multiple conventional PLDs. To take advantage of the extra macrocells in the 22CV10A the 22CV10A+ software option must be selected when compiling, designing, and programming parts.

PEEL Design Techniques

Designing with PEEL devices is much like designing with 20 and 24 pin PLDs. However, PEEL architectures give designers additional flexibility, making it possible to fit more logic into a single package.

Standard Macrocell Configurations

Macrocell configurations number 3, 4, 9 and 10 (in figure 2) are four of the twelve PEEL device macrocell configurations that are most similar to the fixed I/O configurations used among standard PLD architectures such as the 16R8, 16L8, 18P8, 16V8 and 22V10. PEEL devices allow for each I/O pin to be independently configured as an input, output or I/O. Additionally, any output function can be independently configured as combinatorial, registered, active high or active low. Independent configurable I/Os make it possible to customize the PLD to your design rather than modifying your design to fit the PLD. These four standard macrocell configurations, can be used to implement a variety of logic functions such as random gates, encoders, decoders, multiplexers, latches, counters and shifters.

Independent Output Enables

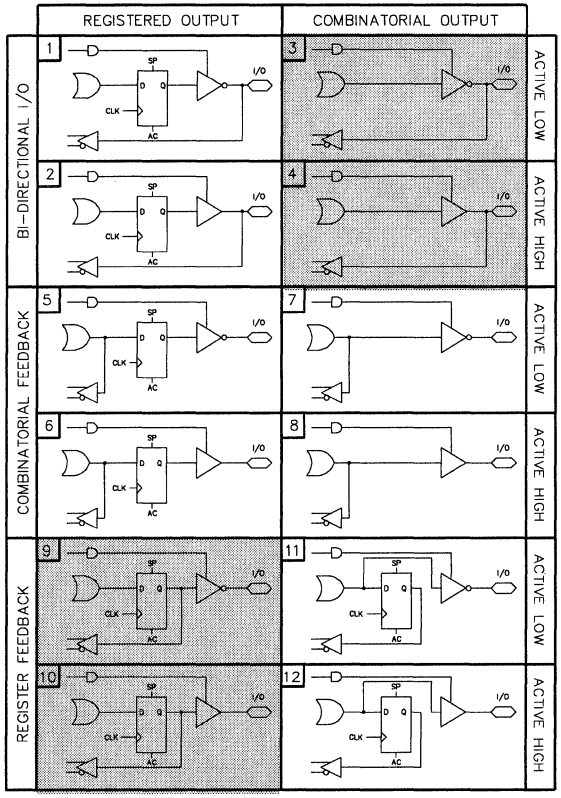
Each I/O also has independent programmable output enables for both combinatorial or registered outputs. The output enables are helpful for bus interfacing as well as "wire-ORing" of signals. Each I/O can be enabled or disabled via individual product terms, even on registered outputs where most standard PLDs offer only a single output enable control pin.

Bi-Directional Registered I/O

Two of the additional PEEL macrocell configurations include bi-directional registered I/O both active-high and active-low, (#1 and #2 in figure 2) The difference between this configuration and the registered output of standard PLD (i.e.,16R8) is that the feedback is from the pin rather than the register. This makes it possible to use a registered output as an input also. Some possible applications for this include: synchronous-read/writable I/O, bus interfaced code conversion, and the wired-OR "Busy" function for bus arbitration circuits.

Buried Combinatorial Feedback

Two additional macro cell configurations found in PEEL devices allow for buried combinatorial feedback before the output enable (#7 and #8 in figure 2). This configuration is very useful for creating latches or logic paths that must be used internally, but only appear externally when accessed by the processor (i.e., as when interfaced to a bus). Furthermore, this configuration is useful in reducing propagation delays when feeding an output signal back into the device for another logic function. This is because the signal is routed directly into the array rather than delayed through the I/O buffer at the pin. An example of how buried combinatorial feedback can be used is shown in the "Change-of-State Detector" application in the following section.



Bi-directional registered I/O (1 & 2)

Standard GAL, PAL, and 22V10 combinatorial configurations (3 & 4)

Buried combinatorial feedback with register (5 & 6)

Buried combinatorial feedback (7 & 8)

Standard GAL*, PAL*, and 22V10 register configurations (9 & 10)

Buried register with combinatorial output (11 & 12)

* GAL/PALdevices do not have indepent output enables as shown

Figure 2. PEEL Device Twelve-Configuration Macrocell

Buried Combinatorial Feedback with Register

Two other PEEL macrocell configurations provide buried combinatorial feedback with a registered output (#5 and #6 in figure 2). This configuration lends itself towards clock synchronization applications. In such applications the buried combinatorial feedback can create an asynchronous latch, the output of which will be stable for clocking into the register. This circuit can be used for interfacing data between two systems operating from different clocks or for simply synchronizing asynchronous signals.

Buried Register with Combinatorial Output

Another useful macrocell configuration is the pseudo-buried register with combinatorial output (#11 and #12 in figure 2). This configuration allows the register output to be fed back into the array while the combinatorial function is routed to the pin. This configuration makes it possible to use the registers as programmable buried storage nodes while the outputs can be selectively addressed for reading onto a bus. Possible functions or applications for this configuration include; or programmable comparitor, programmable dip-switch, buried control register, programmable mask register. An example of how this configuration is used can be seen in the "Change-of-State Detector" application in the following section.

Global Preset and Clear

The PEEL18CV8, 20CG10A and 22CV10A each have a synchronous preset (SP) and asynchronous clear (AC) product term that control all the registers. Although these functions are fairly straight forward, there are some unique ways to take advantage of functions especially for counters and state machines. An example of this is shown in the 8-bit Counter with Function Controls application example in the application section of this application note.

Application Examples

The following pages include a few application examples that demonstrate ways to take advantage of some of the PEEL device architectural enhancements. All of the examples were designed using the PLACE logic compiler.

Bus-Programmable Multiplexer

This application (shown in figure 3) implements an 8 to 1 multiplexer that can be interfaced to a uP bus. Any one of the 8 Inputs (I0-7) can be selectively routed to the output (OUT) by writing (/WR and /CS=0) a 3-bit binary value to the data inputs (DI0-2). The value is stored into a 3-bit latch that controls the multiplexer selection. Because the latch utilizes internal asynchronous feedback (macro configuration #8), the value can also be enabled onto the data outputs (DO0-2). The DI and SO (0-2) pins should be tied together for write/read bus operation. See figure 4.

Input Synchronizer (PEEL18CV8)

Quite often systems need to synchronize an asynchronous input in order to avoid potential metastability conditions that can be caused by set-up time violations. A common method for doing this uses two rippled D-type flip-flops (i.e., 74LS74) as shown in figure 5. In this circuit the asynchronous input is feed into the D of the first flip-flop and the Q of the first is feed into the D of the second. The resulting Q output of the second flip-flop will be synchronized to the clock.

PEEL devices can implement the same type of circuit requiring only one input pin, one output pin and a system clock. This is accomplished by using the internal feedback with-register macrocell configuration (#5 or 6 in figure 2) and the clock signal which is provided in the AND array. The PEEL circuit , shown in figure 5, is comprised of a gated-latch that internally latches the asynchronous input on the falling edge of the clock. This holds the input stable to adequately meet the set-up time of the register which is clocked on the rising edge. If by chance the input violates the set-up time of the gated latch, the clock low time will encounter any possible metastability stabilizing in time for the high-going register clock.

If multiple input synchronizers are needed for a system, the PEEL device solution becomes even more elegant. This is because only two pins per synchronizer are needed. Thus, a PEEL18CV8 could implement eight such synchronizer circuits in a single 20 pin package.

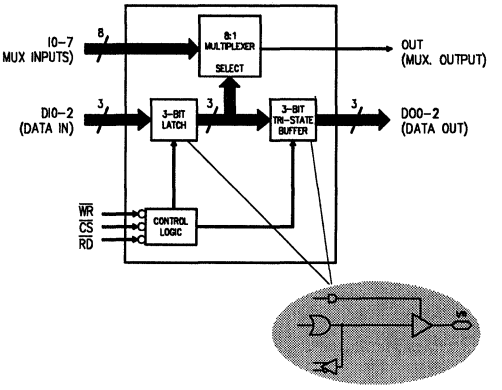


Figure 4. Buried Latches in Bus-Programmable Multiplexer

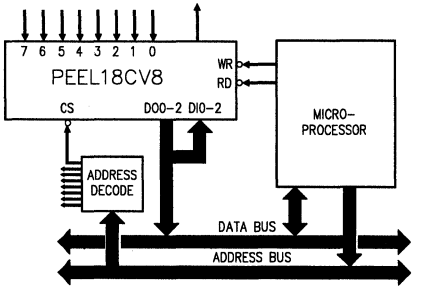


Figure 3. Programmable Multiplexer System Diagram

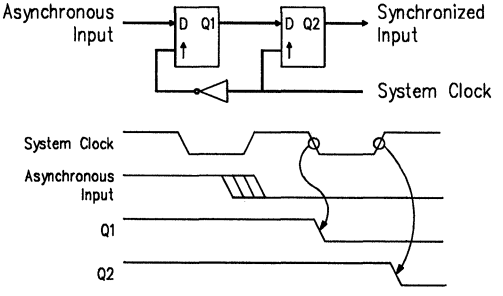


Figure 5. Input synchronization using standard logic

The equations for this circuit are shown below. Although using the clock signal in the equations may look like a possible race condition, this is not the case because of the zero hold time allowed for PEEL device registers. A possible logic hazard is removed (a high-low-high glich) by ANDing the input (IN) and the internal feedback signal (Q2). Note, the Q2 signal used on the right side of the equation actually represents the internal combinatorial feedback labeled as Q1 in figure 6.

```
Q2 :=  CLK &  IN #  "when CLK=1 allow input to set-up
      !CLK & Q2 #  "when CLK=0 latch input internally
        IN  & Q2   "prevent hazard condition
```

8-Bit Counter with Function Controls (PEEL18CV8)

A free-running re-setable 8-bit counter is a fairly common function for a conventional 20-pin registered PLD like the 16R8. However, try adding control functions such as load or hold and you will quickly realize that it is not possible. This is because the number of product terms used per bit for a binary D register counter is N, that is, bit 1 uses one product term, bit 2 uses two and bit 8 uses eight. Since there are only eight product terms per SUM (as is the case for most every 20-pin registered PLD), all the product terms for bit-8 are used for counting.

In order to implement the load or the hold function of a counter, an additional product term is needed per bit. Because of this, most 8-bit load or hold counters are designed using a 24 pin device like the 22V10 which has additional product terms. The 20-pin PEEL18CV8 however, can implement a loadable or holdable 8-bit counter plus more, by taking advantage of its synchronous preset and asynchronous clear terms. The synchronous preset term specifically, can be used to free up a product term of eigth bit. The product term function is the last count before all bits are set to one as shown in the equation below. Freeing this product term from the eigth bit now makes it possible to add either the load or hold condition for all eight bits.

```
SP := Q7 & Q6 & Q5 & Q4 & Q3 & Q2 & Q1 & !Q0
```

An example of the type of multi-function 8-bit counter that can be designed with the 18CV8 is shown in figure 7. In this application the PEEL18CV8 implements an 8 bit counter with four control functions: hold, reset, repeat and output enable. The operation of each control is listed below.

SYNCHRONOUS RESET - When set high, the outputs (Q0-7) will go low after the next clock. When set low, the counter will start counting up with each clock.

HOLD COUNT - When set high, the count will hold the present state. When low, the count will resume.

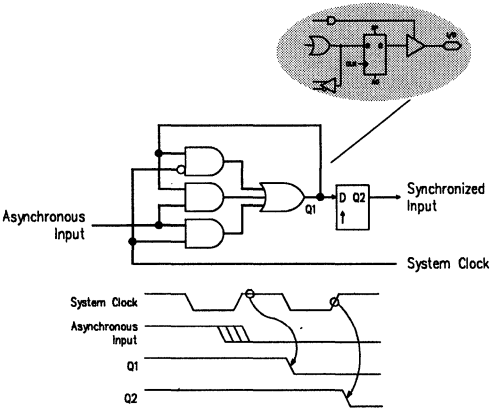


Figure 6. Input synchronization using a PEEL18CV8

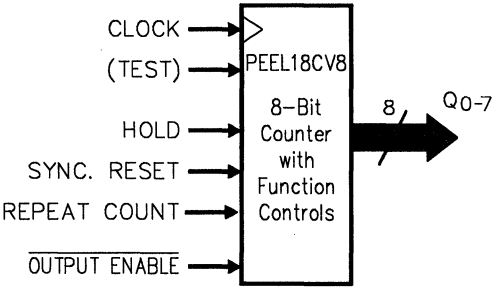


Figure 7. PEEL18CV8 8-bit Counter with Hold and other function controls.

REPEAT COUNT - When set high, the counter will repeat the count after reaching FF HEX. When set low, the counter will stop after one complete count. The asynchronous clear product term is used for this function.

OUTPUT ENABLE - When high, the outputs will be disabled and will enter a high impedance state. When low, the outputs are enabled.

Change-of-State Detection Port (22CV10A+)

The application shown in figure 8 uses the PEEL22CV10A (with the "+" option) as a intelligent input port that off-loads the µP from having to perform software polling. The change-of-state port incorporates eight inputs that are monitored for a change-of-state (low or high). If a change occurs an interrupt will be sent to the µP. The µP can then read either the eight pseudo buried registers holding the change-of-state or read inputs directly. Uses for such an application include; sensor monitoring, "glitch" detection, communication handshaking and clock synchronization. Figure 9 shows a block diagram of the functions implemented.

The operation of the Change-of-State Detection Port is as follows: Any change on the inputs (low-to-high or high-to-low) can be detected via an 8-bit non-equality comparitor (NEQ). When detected, the INTR latch output is set for interrupting a µP. The INTR output is also used to clock the 22CV10A+ which latches the input state into eight pseudo-buried registers. The µP can then read the registers on D0-D7 when CS, RD, and A0 = 0. Once read (unless another change has occurred) the INTR latch will be reset . The I0-I7 pins can be read directly by properly addressing the A0 input (A0 = 1).

All preceding applications were created using the PEEL Development System with PLACE™ logic complier. For more detailed information on these and other applications refer to the ICT PLACE Software and Users Manual.

Conclusion

Flexible and architecturally enhanced PEEL devices, along with easy-to-use PEEL development tools, help PLD designers get more logic into every package. Additionally, PEEL Devices provides a low power, reprogrammable and higher quality alternative to conventional PLDs.

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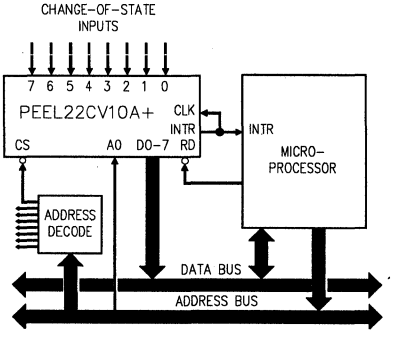

Figure 8. PEEL22CV10A+ Change-of-State Detector

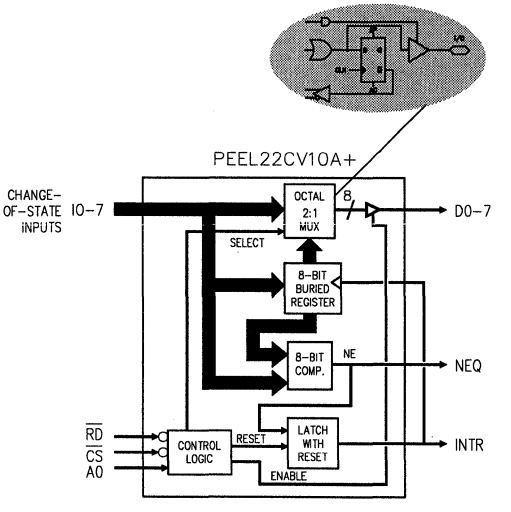

Figure 9. PEEL22CV10A+ Change-of-State Detector functional block diagram

Using Internal Timing of PEEL Devices

Introduction

The ICT PEEL devices are CMOS Programmable Electrically Erasable Logic (PEEL) device with external speed performance as fast as 5ns t_{PD}. In addition to the high performance, PEEL devices provide low-power, reprogrammablility and additional macro cell configurations. The additional macro cell configurations not only add functionality but also further enhance performance.

The unique internal feedback macro cell configuration offers fast internal propagation delays. For example a 22CV10A-10 has an internal t_{PDI} of 7ns. This makes it possible to achieve internal multi-level logic functions over 3ns faster per level than any other 10ns 22V10. The same applies for other PEEL devices as well. Internal timing for all PEEL devices is provided at the end of this application note. The PEEL 22CV10A-10 will be used as an example throughout this application note.

Internal Combinatorial Timing

System designers using programmable logic devices to implement functions such as range decoders, adders, arithmetic logic and parity generator/checkers, etc., often encounter limitations due to the number of product terms available per sum. For example, the carry-out function alone for a four-bit, carry-look-ahead adder requires over 36 product terms, while the most significant bit requires 28 product terms. An n-bit parity generator/checker requires 2^{n-1} product terms. Such logic applications are almost impossible to directly map into standard sum-of-product PLDs.

A common solution for fitting these applications into a standard PLD is to use multi-level logic design. The penalties with this method are the use of additional I/Os and the added propagation delay of a second level of logic. Most standard PLD specifications provide an external propagation delay specification called t_{PD}. To obtain the total propagation delay of a multi-level logic circuit, simply multiply the device t_{PD} by the number of logic levels used. Thus a device with 10ns t_{PD} would require 20ns for two levels, 30ns for three levels, and so on.

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PEEL Macrocells for Multi-level Logic

ICT's PEEL22CV10A provides additional macrocell configurations which allow designers to achieve faster propagation delay for multi-level logic by using internal t_{PD} timing (configurations 5-8 in figure 1). Notice that these four macrocell configurations allow for feedback immediately after the sum instead of at the pin as with the standard combinatorial 22V10 configurations 3 and 4 if figure 1. The additional

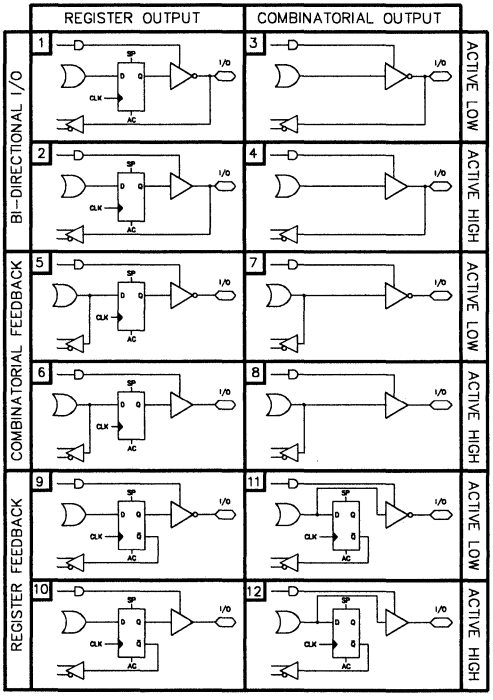
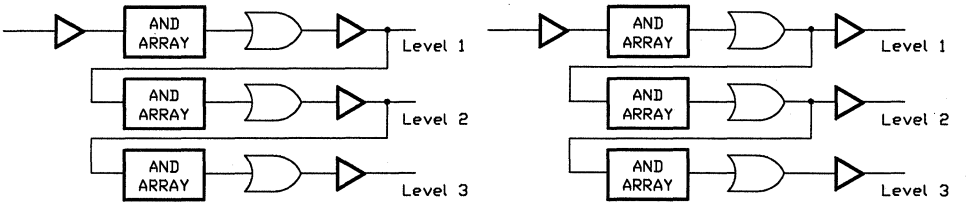


Figure 1. PEEL22CV10A Macrocell Configurations



Standard 22V10 - External Feedback Path

PEEL22CV10A - Internal Feedback Path

	Standard 22V10-10	Propagation Delay
level 1	t_{PD}	10 ns
level 2	$2x(t_{PD})$	20 ns
level 3	$3x(t_{PD})$	30 ns

	PEEL 22CV10A-10	Propagation Delay
level 1	t_{PD}	10 ns
level 2	$t_{PD}+t_{PDI}$*	17 ns
level 3	$t_{PD}+2x(t_{PDI})$*	24 ns

*t_{PDI}=Internal propagation delay = 7

Figure 2. Multi-level Logic in Standard 22V10-10 vs PEEL22CV10A-10 with Internal t_{PDI}

macrocells can be used by specifying the 22CV10A+ as the device type in the design source file. Programming is accomplished also by specifying the 22CV10A+.

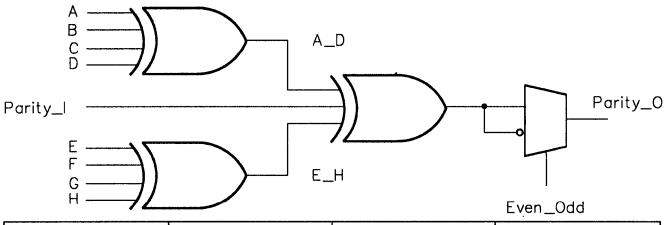
Figure 2 shows the circuit and timing differences for external and internal timing of the 22CV10A-10. With its 7ns internal timing "t_{PDI}", the PEEL22CV10A removes the additional delay caused by the output buffer making it the best candidate for high speed multi-level logic design.

Multi-level Logic Application

This application uses the PEEL22CV10A as a 9-bit even/odd parity generator/checker. The application takes advantage of the PEEL22CV10A's internal timing and saves at least 3ns in comparison to an implementation in a standard 22V10 device. A functional diagram of a 9-bit parity even/odd generator/checker is shown in figure 3 and the corresponding table lists its functional operation.

The parity function is commonly implemented via the utilization of the exclusive-OR operation. To build a N-bit parity generator/checker, the number of 2-input exclusive-OR gates required is N-1. A N-bit parity function can also be implemented via the AND-OR logic operation but it requires 2^{N-1} product terms. For instance, a 9-bit parity function will require 256 product terms. Though the PEEL22CV10A device has only 132 product terms, a 9-bit parity function can still be implemented by using two macro cells to implement two 4-bit parity generators. Both outputs of the macro cells are fed back and XORed with the 9th bit (Parity_In). With this method, there is an additional delay due to the feedback of the 4-bit parity generator outputs. If it is implemented in the PEEL22CV10A device, then the delay would be about 3ns less than if it was implemented in a standard 22V10 device. This is because the outputs in the 22V10 device are fed back from the pin, whereas in the PEEL22CV10A the outputs can be configured to feedback directly from the OR gate (before the output buffer).

The design file implementation of the PEEL22CV10A as a 9-bit parity generater/checker is included with ICT's PLACE Development Software.



No. of high inputs A-H	Parity In	Even/Odd	Parity Out
Even	1	0	H
Odd	1	0	L
Even	0	0	L
Odd	0	0	H
Even	1	1	L
Odd	1	1	H
Even	0	1	H
Odd	0	1	L

Figure 3. 9-Bit Parity Even/Odd Generator/Checker

Internal Sequential Timing

The maximum frequency for sequential logic functions such as counters and state-machines, is typically calculated for 22CV10A-10 as follows

$f_{MAX} = 1/(t_{SC}+t_{CO})$

$f_{MAX} = 1/(7ns+7ns) = 71.4MHz$

Where t_{SC} is the input set-up-to-clock and t_{CO} is clock-to-output. This timing parameter assumes that the feedback could possibly be coming from an input pin (see Figure 4). In reality many designs only use the internal feedback from the register and not any inputs (as shown in Figure 5). The ICT PEEL devices specify internal feedback from the register allowing a high frequency of operation as shown below.

$f_{MAX} = 1/(t_{SC}+t_{CF})$

$f_{MAX} = 1/(7ns+4ns) = 90.9MHz$

Even faster clocking can be accomplished with "pipelined" designs where feedback is not used at all. The timing in this configuration is just limited to the clock high and low time, providing proper set-up time is maintained (see figure 6).

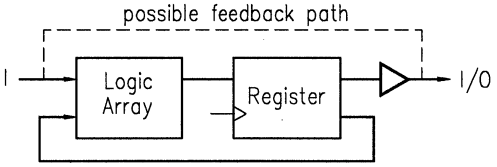


Figure 4. External feedback $f_{MAX} = 1/(t_{SC}+t_{CO})$

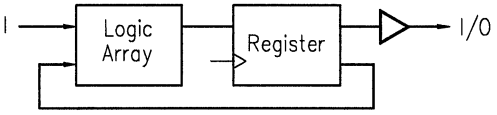


Figure 5. Internal Feedback $f_{MAX} = 1(/t_{SC}+t_{CF})$

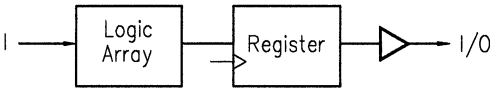
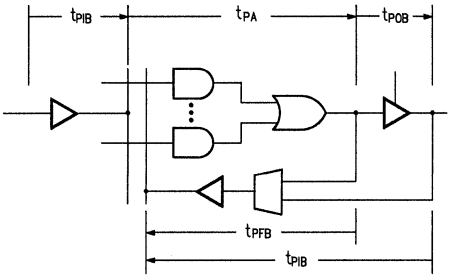


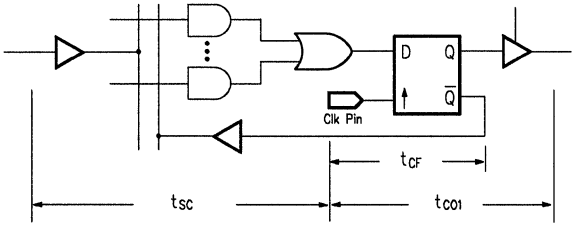
Figure 6. No feedback $F_{MAX} = 1/(t_{CL}+t_{CH})$

PEEL20CG10A and 22CV10A Internal Timing Specification



PEEL20CG10A 22CV10A Internal Combinatorial Timing[4,13]

Symbol	Parameter	-7	-10	-15	-25	Unit
		Max	Max	Max	Max	
t_{PIB}	Input or I/O pin to Input of Array	2	2.5	4	7	ns
t_{PFB}	Feedback to Input of Array	2	2.5	4	7	ns
t_{POB}	Output of Array to Output pin	3	3	5	5	ns
t_{PA}	Input of Array to Output of Array	2.5	4.5	6	13	ns
t_{PDI}	Internal propagation delay (t_{PA}+t_{PFB})	4.5	7	10	20	ns

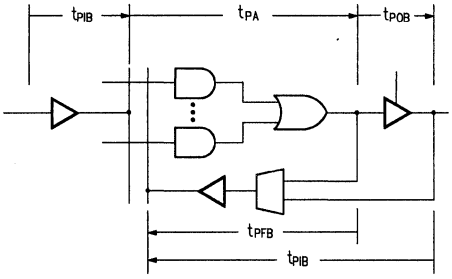


PEEL20CG10A 22CV10A Internal Sequential Timing[4,13]

Symbol	Parameter	-7		-10		-15		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SC}	Input or feedback setup to clock	4.5		7		8		15		ns
t_{CO1}	Clock to output		5.5		7		8		15	ns
t_{CO2}	Clock to combinatorial output delay via internal registered feedback		10		12		17		35	ns
t_{CF}	Clock to feedback		3.5		4		5		9	ns
t_{CL},t_{CH}	Clock low time, clock high time	3.5	3.5	5		6			15	ns
f_{MAX1}	Max clock freq. Int feedback(1/(t_{SC}+t_{CF}))	12.5		90.9		76.9			41.6	MHz
f_{MAX3}	Max clock freq. No feedback(1/(t_{CL}+t_{CH}))	142.8		100		83.3			38.4	MHz

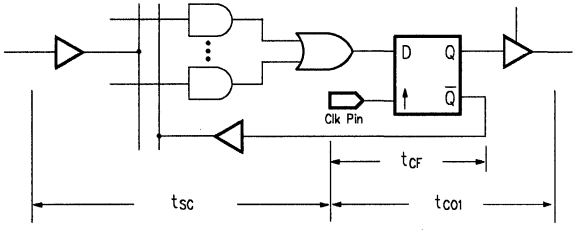
*Refer to the specific data sheets for description of footnotes

PEEL18CV8 Internal Timing Specification



PEEL18CV8 Internal Combinatorial Timing[4,13]

Symbol	Parameter	-7	-10	-15	-25	Unit
		Max	Max	Max	Max	
t_{PIB}	Input or I/O pin to Input of Array	2	2.5	4	7	ns
t_{PFB}	Feedback to Input of Array	2	2.5	4	7	ns
t_{POB}	Output of Array to Output pin	3	3	5	5	ns
t_{PA}	Input of Array to Output of Array	2.5	4.5	6	13	ns
t_{PDI}	Internal propagation delay (t_{PA}+t_{PFB})	4.5	7	10	20	ns



PEEL18CV8 Internal Sequential Timing[4,13]

Symbol	Parameter	-7		-10		-15		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SC}	Input or feedback setup to clock	5		5		12		20		ns
t_{CO1}	Clock to output		7		7		12		15	ns
t_{CO2}	Clock to combinatorial output delay via internal registered feedback		10		12		25		35	ns
t_{CF}	Clock to feedback		3.5		4		8		15	ns
t_{CL},t_{CH}	Clock low time, clock high time	3.5		5		10		15		ns
f_{MAX1}	Max clock freq. Int feedback(1/(t_{SC}+t_{CF}))	117.6		111		50		28.5		MHz
f_{MAX3}	Max clock freq. No feedback(1/(t_{CL}+t_{CH}))	142.8		100		50		33.3		MHz

*Refer to the specific data sheets for description of footnotes

PEEL Device Metastability

Introduction to Metastability

Metastability is a type of failure that can occur when digital circuits attempt to synchronize asynchronous digital data. Whenever a clocked flip-flop synchronizes an asynchronous input (Figure 1), there is a small but finite probability that the output will exhibit an unpredictable delay. This happens when the input transition violates the setup and hold time specification. In other words it actually occurs within the small timing window where the flip-flop decides to accept the new input. Under these circumstances the flip-flop enters an unstable equilibrium state called metastable. A slight deviation from perfect balance will eventually cause the outputs to revert to one of the two stable states. But the delay depends not only on the gain-bandwidth product of the circuit, but also on the original balance and the noise level of the circuit. Therefore, it can only be described in statistical terms.

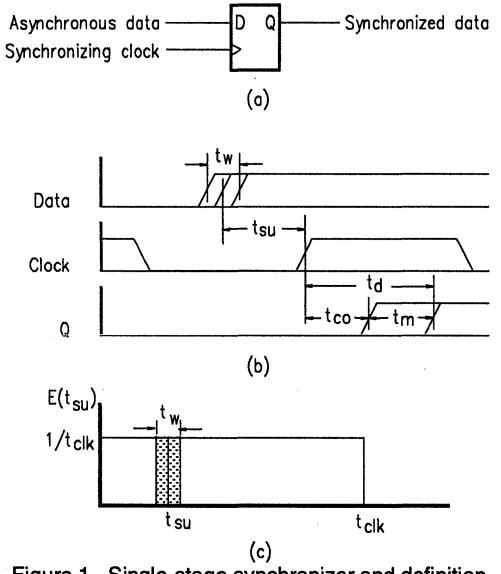


Figure 1. Single-stage synchronizer and definition of critical trigger window t_W

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As shown in Figure 1, a critical trigger window t_W is defined. If a flip-flop timing constraint is violated during the time window t_W, the output Q is still unresolved within a decision time t_{COM}. It is referenced to the beginning of the trigger event which is the positive clock edge for the sample circuit in Figure 1, t_d thus includes the normal propagation delay t_{CO} and extra delay due to metastability t_{MET}. The relation $t_W=f(t_d)$ can be used for defining metastable behavior of flip-flops. The exponential function was found to be asymptotically valid for the relation:

$$t_W=f(t_d)=a*\exp(b*t_d)$$

The probability density function for actual setup time $E(t_{SU})$ is unity for one clock period t_{CLK} (Figure 1). The probability for one data event to hit the critical window t_W is thus equivalent to the indicated area t_W/t_{CLK}. With given $t_W(t_d)$ the reliability (mean time between failures, MTBF) of a synchronizer can be calculated to be:

$$MTBF(t_d)=1/(t_W(t_d)*f_{CLK}*f_{DATA})$$

We can rewrite the equation with the exponential relation:

$$MTBF=\exp(t_d/k2)/(k1*f_{CLK}*f_{DATA})$$

k1 and k2 are the constant we can get from experimental results to calculate MTBF with relative t_d, clock frequency f_{CLK} and data frequency f_{DATA}.

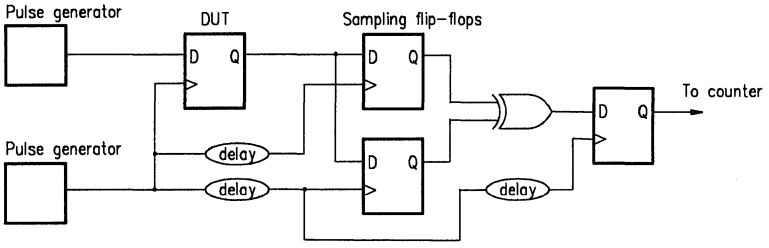

Figure 2. Metastability measurement setup

Measurement Setup and Parameters

Figure 2 shows a test circuit to measure metastable parameters of a synchronizer. A device under test (e.g. DUT) is triggered on its D and CLK inputs by two asynchronous free-running clocks. In here, we use two different pulse generators to provide a data rate of 1 MHz and a clock rate of 2 MHz. The data transitions are randomly and evenly distributed over the entire clock period of about one transition per clock cycle. Under these circumstances, we may assume that the data transitions are also evenly distributed within the failure time window t_W.

On the output of the DUT, there are two well characterized sampling flip-flops (the difference delay time via pin to D input and pin to CLK are characterized to prevent violation of setup time). These two flip-flops use the same clock signal used by the DUT; the first sampling clock is delayed by t_d (time delay for metastable output resolved t_d, and the second sampling clock is delayed by approximately 120 ns later. It is clocked so late that the probability that the output did not resolve at that time can be neglected.) Because this probability decreases exponentially with time, this condition can easily be satisfied.

The outputs of both sampling flip-flops are exclusive-ORed and the result sampled after another flip-flop with fixed time delay. When the first two sample states differ, there must be a transition after t_{COM}, revealing a late transition metastable condition on the DUT. Accumulating these pulses for some known time interval yields the MTBF of the DUT for a given t_{COM}.

To run the test, t_{CO} is used as a base delay (e.g. t_M=0). We get different MTBF with increasing t_M until MTBF greater then 60 sec. When the MTBF results are plotted on semi-log paper for t_d yields a best-fit straight line with slope - 1/k2. k1 then can be calculated by inserting a k2 value into the MTBF equation. With k1 and k2, the designer can easily find t_{COM} for a chosen MTBF, f_{CLK} and f_{DATA}.

Metastability Data for PEEL22CV10A-10

ICT PEELs are based upon fast, CMOS EEPROM process technologies which make them exhibit superior recovery ability against metastability. Figure 3 shows the experimental metastable characteristics of PEEL22CV10A-10. **Other 1μm PEEL devices have similar or better characteristics.** k1 is related on the Y-axis intercept point and k2 is the inverse of slope of the straight line. The following table is the k1 and k2 values for PEEL22CV10A-10:

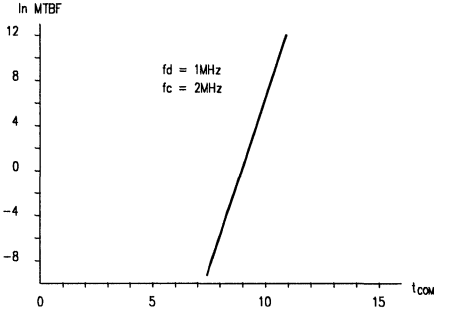

Figure 3. K2 plot of 22CV10A

Device	k1	k2
PEEL22CV10A-103x10110.16ns	$3x10^{11}$	0.16ns

For example, to determine the MTBF for PEEL22CV10A-10 that is used as a synchronizer in a system with 33 MHz clock frequency, 25 MHz data rate, t_{MET} is calculated with the following equation:

$t_{MET}=1/f_{CLK}-t_{SU}-t_{CO}=1/33$ MHz-6-8=16ns

enter these values into the MTBF equation

$MTBF=\exp(t_d/k2)/(k1*f_{CLK}*f_{DATA})=1.7x10^{31}$years

To determine the maximum clock rate(e.g. $f_{CLK}=1/(t_{SU}+t_d)$ that a device will allow in an asynchronous environment for expected MTBF, the following equation then can be used:

$MTBF=\exp((1/f_{CLK}-t_{SU})/k2)/(k1*f_{CLK}*f_{DATA})$

Solving the equation for a 25 MHz data stream and 10 years MTBF expected for PEEL22CV10A-10, get the maximum clock rate f_{CLK}=52 MHz and t_{MET}=5ns.

Synchronizer Circuit Improves MTBF

Although PEELs show extremely quick metastable settling time, we still can improve the MTBF by using its unique internal feedback configuration. In Figure 4, a gated-latch internally latches the asynchronous input on the falling edge of the system clock, generating the signal Q1. ANDing the input with Q1 through the internal feedback path, eliminates a possible hazard condition during the clock's high-to-low transiting time. The latch then holds Q1 stable to ensure meeting the setup-time requirement of the subsequent D flip-flop, which registered on the next rising system clock edge.

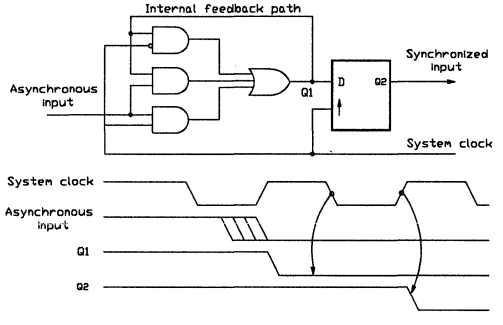

Figure 4. PEEL22CV10A Synchronizer

Just like a two stage synchronizer, the probability that a data goes metastable is the multiplication of the two probabilities of each synchronizer as they go metastable. Therefore since the probability of failure becomes so small, the MTBF of PEEL devices dramatically improves.

When using the same measurement setup above, we get $k1=3x10^{46}$ and k2=0.05ns for the same PEEL22CV10A-10 with gated latch. With the same 25 MHz data rate and 10 years MTBF, the maximum clock frequency 70 MHz can be reached. As a result almost no extra delay is needed for the synchronizer.

References

1. Horstmann, Jens U, "Metastability Behavior of CMOS ASIC Flip-Flops in Theory and Test"

IEEE Journal of Solid State Circuits, Vol 24, No. 1, February 1989, page 146.

2. Rubin, Kim, "Metastability Testing in PALs"

Electronics Conventions Management, Inc. ELECTRO 1987 Professional Program Papers.

3. Tavana, Danesh M, "A Study of the anomalous behavior of synchronizer circuits"

Monolithic Memories Inc. Applications book, 1984, page 11-13.

4. Masteller, Steven R, "Design a digital synchronizer with a low metastable-failure rate" EDN, April 25, 1991. page 169.

PEEL™ Device Characterization Report

Introduction

The following data provides typical and worst case measurements for several key AC and DC parameters 1-micron PEEL 18CV8, 20CG10A, and 22CV10A products. Normalized characterization graphs are included.

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Introduction

DC Characterization Data

Supply Current vs Temperature and Vcc

Package Thermal

Output Sink/Source Current vs Output Voltage

AC Characterization Data

Speed vs Capacitive output Loading

Output Slew Rates and Ground Bounce

Speed vs Temperature and Vcc

DC Characterization Data

Supply Current vs Ambient Temperature and Vcc

The effects of power supply current (ICC) vs Vcc voltage and ambient temperature are provided on normalized graphs. Typical ICC measurements may be used in conjunction with the normalized graphs to ascertain additional data concerning variations over temperature or Vcc. Figure 1a shows variations in temperature at Vcc=5.0V. Figure 1b shows variations in Vcc at Temp.=25°C.

Product	ICC(m A)	
	Typical	Data Sheet
22CV10A/20CG10A-7	100	155
22CV10A/20CG10A-10	80	135
22CV10A/20CG10A-15	70	135
22CV10AL/20CG10AL-15	55	75
22CV10A/20CG10A-25	40	67
18CV8-7	75	110
18CV8-10	65	110
18CV8-15	28	45
18CV8-25	18	37

Note: Typical ICC at Temp=25°C, Vcc=5.0V, Freq=25MHz;
Data sheet at Temp=0-70°C, Vcc=5.25V, Freq=25MHz

Package Thermal

The PEEL Devices and PEEL Arrays are available in plastic DIP, plastic LCC and SOIC packages. Thermal characteristics of these packages are specified by the thermal (junction to ambient) resistance value "θJA". Used in conjunction with the PEEL Devices and PEEL Arrays power dissipation and a reference operating temperature, the thermal resistance can determine junction temperature (T junction = T reference + Power × θJA). For example, the θJA for ICT's 24 pin plastic DIP package is approximately 60°C/Watt and the θJA for ICT's 28 pin plastic LCC (PLCC) package is approximately 58°C/Watt. Contact ICT for additional package thermal characteristics.

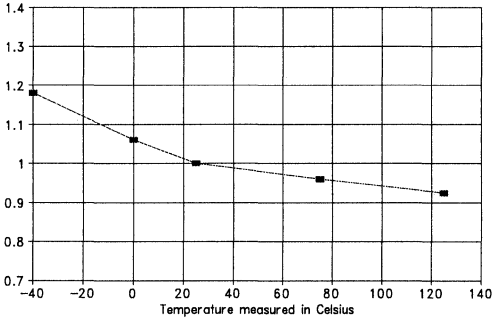

Figure 1a. Normalized ICC vs Temperature

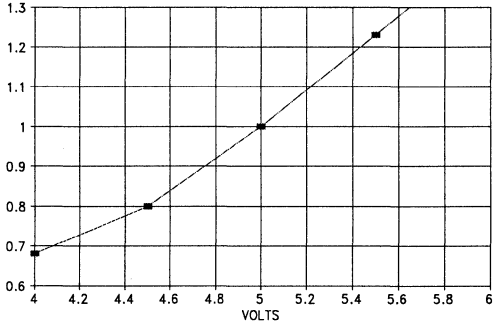

Figure 1b. Normalized ICC vs VCC

Output Sink and Source Current vs Output Voltage

Two graphs (Figures 2a and 2b) plotting the relative effects of output current vs voltage are provided: Output sink current (IOL) vs Output voltage low (VOL) and Output source current (IOH) vs Output voltage high (VOH). Data for both graphs use Vcc=5.0V and Temp=25°C.

	Typical	Data Sheet Limit
IOL @ VOL .5V	32mA	16mA
VOL @ IOL 16mA	0.22V	0.5V
IOH @ VOL 2.4V	-33mA	-4mA
VOH @ IOL -4mA	3.8V	2.4V

Note: Typical measurement at Temp=25°C, Vcc=4.75V

Table 2. Output Drive

AC Characterization Data

Speed vs Capacitive Output Loading

The effects of capacitive output loading on Tpd are provided on a normalized graph in Figure 3. Typical Tpd measurements can be used in conjunction with the normalized graph to ascertain additional data concerning loading variations. All measurements were taken with Vcc=5.0 and Temp.=25°C.

Output Slew Rates and Ground Bounce

Output buffers of the PEEL devices have a nominal slew rate of 1V/ns for both low-to-high and high-to-low transmissions between 0 and 3V. The slew rate is fast enough to meet 22CV10A speed requirements but slow enough to minimize bounce and transmission line effects.

Ground bounce testing of the PEEL devices is implemented in a fashion similar to the March 2, 1989 EDN report on Ground Bounce Measurements with the addition of full TTL loading on all outputs. The set-up has nine out of ten outputs simultaneously switching while the tenth attempts to maintain a steady low level. The switching outputs are approximately 10 MHz. Testing was performed with Vcc=5V and Temp=25°C. The worst case results are shown in the following example using the PEEL22CV10AP.

22CV10AP

9 Switched Outputs	Unswitched Outputs Voltage Peak (TTL load)
Low-High	0.42V
High-Low	0.83V

Table 4 Ground Bounce

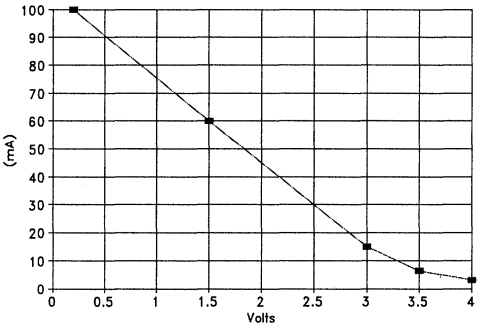

Figure 2a. IOH vs VOH

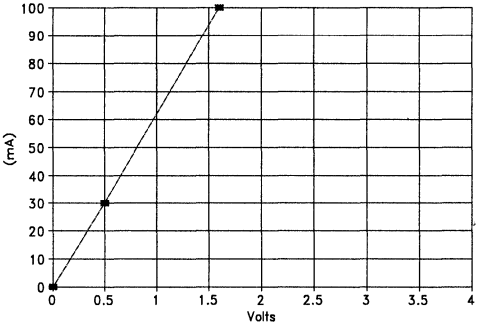

Figure 2b. IOL vs VOL

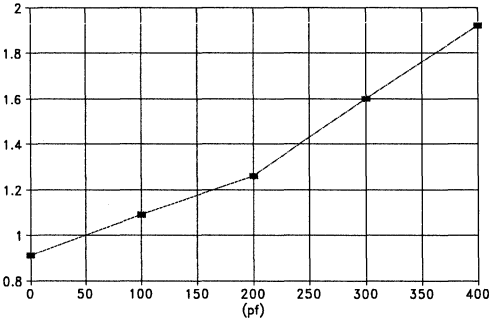

Figure 3. Normalized TPD vs Output Loading

Product	Tpd (ns)		Tco (ns)		Tsc (ns)	
	Typical	Data Sheet	Typical	Data Sheet	Typical	Data Sheet
22CV10A/20CG10A-7	5.5	7.5	4	5.5	2.5	3
22CV10A/20CG10A-10	8	10	4.5	6	3.5	5
22CV10A/20CG10A-15	12	15	6	8	6	8
22CV10AL/20CG10AL-15	13	15	7	10	7	10
22CV10A/20CG10A-25	16	25	10	15	10	15
18CV8-7	5.5	7.5	5	7	3	5
18CV8-10	8	10	5	7	3.5	5
18CV8-15	12	15	8	12	8	12
18CV8-25	18	25	10	15	10	20

Note: Typical at Temp=25°C, Vcc=5.0V, Freq=25MHz; Data sheet at Temp=0-70°C, Vcc=4.75-5.25V, Freq=25MHz

Table 3 Characterization Data

Speed vs Temperature and Vcc

The effects of ambient temperature and Vcc voltage vs speed (Tpd, Tco and Tsc) are provided on normalized graphs in figures 4a-4f. Typical speed measurements may be used in conjunction with the normalized graphs to ascertain additional data concerning variations over temperature or Vcc. Graphs showing variations in temperature uses Vcc=5.0V. Graphs showing variations in Vcc uses Temp=25°C. Standard data sheet test loads are used.

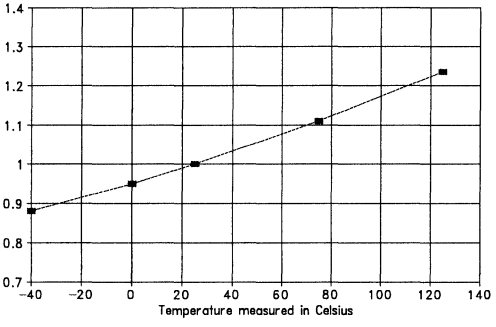

Figure 4a. Normalized TPD vs Temperature

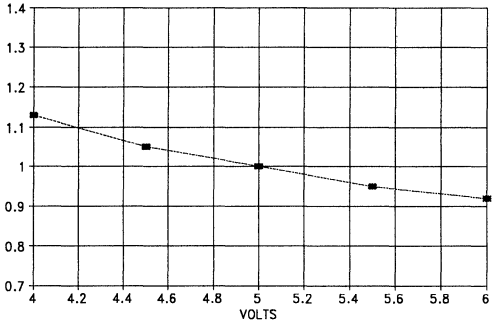

Figure 4b. Normalized TPD vs VCC

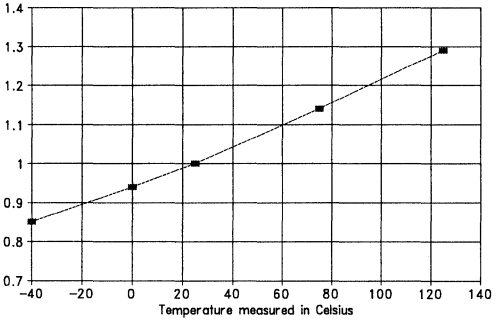

Figure 4c. Normalized TCO vs Temperature

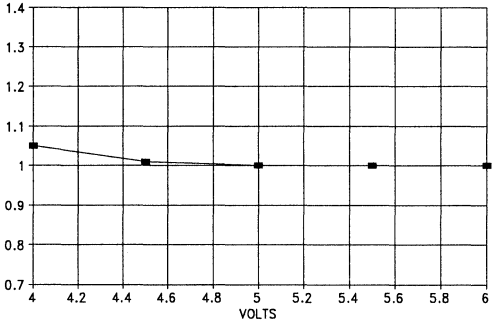

Figure 4d. Normalized TCO vs VCC

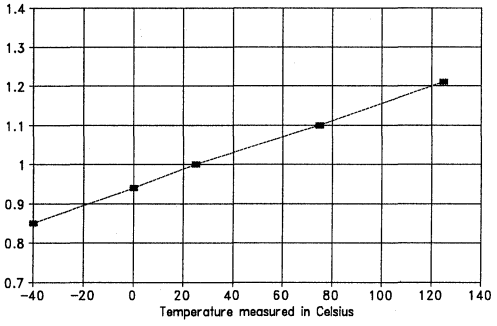

Figure 4e. Normalized TSC vs Temperature

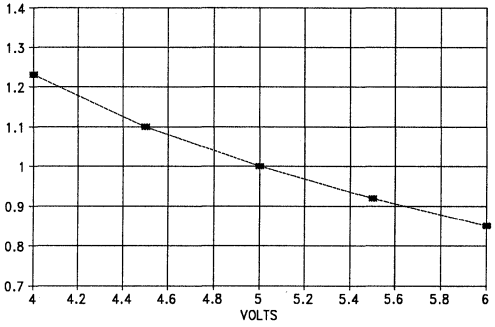

Figure 4f. Normalized TSC vs VCC

1μm CMOS PEEL Products Reliability Report

Introduction

ICT Inc. is dedicated to providing its customers with integrated circuits that are designed, manufactured, tested, and serviced to the highest level of Quality and Reliability. This reliability report provides a summary of ICT's 1.0um CMOS EEPROM process for PEEL devices and Arrays. It also documents the reliability tests performed and the data collected to ensure our reliability and quality standards. Additionally an overview of ICT's standard production test flow is included.

1.0μm EEPROM Process Overview

ICT's 1.0um process is an N-well based CMOS process. The N-well approach is chosen for optimal low power consumption while balancing the performance of both N-Channel transistors and memory cells. Two layers of polysilicon for the memory cell allows the first poly layer to be used as the floating gate, while the second poly layer is used for the control gate and peripheral transistor gate.

The transistors have a high quality 225 Å gate oxide, with 0.8um effective channel length. The EEPROM memory cell has 100 Å tunnel oxide between the floating gate and the drain side. Charge injection into and out from the floating gate are accomplished by the Fowler Nordheim tunneling mechanism. This process utilizes double metal layers to minimize the signal delay time and reduce chip size. High breakdown voltages are achieved by graded drain/source junction.

To simplify the design and process of ICT's EEPROM technology, unlike that of other EEPROM manufactures, EPI materials or substrate bias generators are not required. This reduces the number of mask steps to 15, improving reliability and yield. High CMOS latchup immunity and High ESD protection are achieved by double guard band design in the chip layout.

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Endurance
Temperature Cycling
Pressure Pot
Temperature Humidity Bias Stress
Latch-up
Electro static discharge (ESD)
Production Test Flow

Reliability Tests

Reliability test for ICT's initial device qualification include: operating life, data retention, endurance, temperature cycling, pressure pot, temperature humidity bias stress, latch-up and electro-static discharge (ESD). Reliability related tests, such as data retention, are also incorporated into ICTs standard production test flow.

After initial device qualification, all products are carefully monitored to ensure the reliability of the device. Production lots are periodically sampled, and are subject to the same qualification tests; all results are documented, and failures are carefully analyzed in order to find long term improvements to the product.

PEEL Devices and Arrays developed with ICT's 1.0μm CMOS EEPROM process share extensive design commonalty and more significantly, they share the same memory cell structure. Furthermore, these devices are manufactured using similar molding compounds, test flows, and advanced screening techniques. These similarities make the reliability data of each device relevant to the others.

Test data provided in this report is applicable to the following PEEL Device and PEEL Array products:

PEEL18CV8	**PA7024**
PEEL20CG10A	**PA7128**
PEEL22CV10A	**PA7140**

Device	Lot #	168 hrs	500 hrs	1000 hrs	Failure Mode
22CV10A	E980329ES	0/100	0/100	0/100	
22CV10A	EA30727	0/101	0/101	0/101	
22CV10A	E980330	0/101	0/101	0/101	
22CV10A	992129	0/101	0/101	1/100	ILH1 on Pin 11
22CV10A	RAB1523	0/105	0/105	0/105	
22CV10A	TL10042W	0/105	0/105	0/105	
22CV10A	TL10042	0/105	0/105	0/105	
22CV10A	TL11056	0/105	0/105	0/105	
22CV10A	TL11057	0/105	0/105	0/105	
22CV10A	EL16020	0/105	0/105	0/105	
22CV10A	TL37075	0/105	0/105	0/105	
18CV8	TL38110	0/105	0/105	0/105	
18CV8	TL41140	1/105	0/104	0/104	Output stuck high
18CV8	TL41139	0/105	0/105	0/105	
18CV8	TL38109	0/105	0/105	0/105	
18CV8	TL41141	0/105	1/105	0/104	Leakage recovered after bake
PA7024	9004360	0/121	0/121	0/121	
PA7024	9016905	0/101	0/101	0/101	
PA7024	9014205	0/53	0/53	0/53	
PA7024	EAB2224	0/105	0/105	0/105	
PA7024	TL10058	1/105	0/104	0/104	Functional Pin 19 stuck
PA7024	TL10059	0/105	0/105	0/105	
PA7024	TL16020	0/105	0/105	0/105	
Total		2/2358	1/2356	1/2355	

Continuous operation. Bias voltage=5.25V, amb. temp=125°C, Duration=1000 hours

Table 1. Dynamic High-Temperature Operating Life Test Data

Device Hrs @ 125°C	Activation Energy	Equivalent Hrs at:		# of Failures	Predicted Fail Rate at:	
		70°C	55°C		70°C	55°C
2,355,836	1.0eV	2.52E8	1.19E9	4	20FITS	5FITS

ICT takes a conservative approach to calculate FIT rates. Five failures are assumed for worst case calculations.

Table 2 Failure Rate Predictions at 60 % U.C.L.

Operating Life

A Dynamic High-Temperature Operating Life (DHTOL) test is a standard approach used to evaluate the reliability of a product under accelerated conditions. Endpoint data is gathered at the rated ambient temperature and the devices are biased as they would be in actual operation. The devices are exercised by constantly switching the inputs. This DHTOL test is set for a continuous operation typically at an ambient temperature of 125°C and a duration equal to 1,000 hours.

The results of the DHTOL test are recorded in a datalog and made available for future reference, see Table 1. Failures in this reliability report are expressed in FITS. Since integrated circuits exhibit very low failure rates, it is convenient to refer to failures in a population during a period of 10^9 devices hours; one failure in 10^9 device hours is defined as one FIT, see Table 2.

Device	Lot #	57 Hrs.	168 Hrs.	336 Hrs.	500 hrs.	Failure Mode
22CV10A	TL25052	0/210	0/210	0/210	0/210	
22CV10A	TL21110	0/210	0/210	0/210	0/210	
18CV8	TL38109	0/210	0/210	0/210	0/210	
18CV8	TL41139	0/210	0/210	0/210	0/210	
18CV8	TL41140	1/210	0/209	0/209	0/209	Bit Failure

Total Hours = 524,500

Using activation energy of 1.0 eV, 500 hours at 165°C is equivalent to 87.7 years at 70°C or 420 years at 55°C of data retention on floating gate.

Table 3. Data Retention

Device	Lot #	100 Cycles	500 Cycles	1000 Cycles
22CV10A	TL10042	0/30	0/30	0/30
22CV10A	TL11056	0/30	0/30	0/30
22CV10A	TL11057	0/30	0/30	0/30

MIL STD 883C Condition B (-55°C to 125°C)

Table 4a. Temperature Cycling Air To Air (-55°C to 125°C)

Device	Lot #	100 Cycles	500 Cycles	1000 Cycles
22CV10A	TL10042	0/30	0/30	0/30
22CV10A	TL11056	0/30	0/30	0/30
22CV10A	TL11057	0/30	0/30	0/30
18CV8	TL41139	0/105	0/105	0/105
18CV8	TL41140	0/105	0/105	0/105
18CV8	TL41141	0/105	0/105	0/105

MIL STD 883C Condition C (-65°C to 150°C)

Table 4b. Temperature Cycling Air To Air (-65°C to 150°C)

Data Retention

At the cell level, data retention is a function of the floating gate's ability to retain charge over extended periods of time without an applied gate bias. Data retention failures in a floating gate structure are commonly caused by dielectric defects; these failures can be accelerated by high-temperature bake stress. The purpose of this test was to determine the reliability of the floating gates ability to retain charge beyond the normal 10 years of operation. Production devices are subjected to a non-biased bake of 165°C with a duration of 57 hours for commercial and 228 hours for industrial. See Table 3.

Endurance

An ICT EEPROM endurance specification means that for any lot of devices shipped, fewer than 5% of the units will cease to cycle properly before the specified limit. Endurance refers to the maximum number of erase and write operations through which each memory cell can be reliably cycled. ICT samples all production lots to assure that this criterion is met. Standard specified limits for both PEEL Devices and PEEL Arrays are 1,000 cycles. However, due to the highly reliable 100 Å tunnel oxide, the actual endurance characteristics are typically significantly better. ICT incorporates into the standard production test flow, a proprietary endurance procedure that allows monitoring of endurance characteristics to endurance specifications.

Temperature Cycling Air to Air

The device is cycled at temperature extremes in Nitrogen environment without power. The normal temperature extremes are -65°C to +150°C with a minimum dwell time of 10 minutes at each of the temperatures with 5 minutes transfer time according to mil STD 883C method 1010.5 condition C. This test measures die stress to the mechanical condition of the package because the thermal coefficient of die are not the same as those of the encapsulation mold compound or the leadframe. See Tables 4a and 4b.

Device	Lot #	72hrs	168hrs.
22CV10A	TL10042	0/100	0/100
22CV10A	TL11057	0/100	0/100
18CV8	TL41139	0/105	0/105
18CV8	TL41140	0/105	0/105
18CV8	TL41141	0/105	0/105

Saturated steam @127°C, 20 PSIG

Table 5 Pressure pot

Device	Lot #	100 Hrs.	500 Hrs.	1000 Hrs.
18CV8	TL41138	0/105	0/105	0/105
18CV8	TL41140	0/105	0/105	0/105
18CV8	TL41141	0/105	0/105	0/105

MIL STD 883C Condition C (-65°C to 150°C)

Table 6 Temperature Humidity Bias Stress

Pressure Pot

The device is exposed to saturated steam at high temperature and pressure. The normal condition is 20 PSI at 127°C. The corrosion resistance of the die in a moist ambient is a key package reliability issue. The plastic encapsulate is not a moisture barrier and will saturate within 72 hours. Since the die is not powered, its temperature and relative humidity will be the same as autoclave once equilibrium is reached. The environmental conditions are now such that it has an ample supply of steam and temperature to start thermally activated events. Autoclave is a good test to detect cracks and holes in the encapsulating plastic and contamination induced leakage problems inadvertently added during the assembly operation. See Table 5.

Temperature Humidity Bias Stress

This accelerated temperature and humidity bias stress is normally performed at 85°C and 85% relative humidity. To maximize metal corrosion conditions, the worst-case bias is the one which has least power dissipation and maximum voltage applied. Higher power dissipation tends to lower humidity at the chip surface and hence lower corrosion susceptibility. This test was performed with alternate pins biased to +5 volts or 0 volts. See Table 6.

Latch-Up

To prevent latch-up a double guard-ring is used on all I/O pins of PEEL Devices and PEEL Arrays. The double guard-ring consists of a dummy N-well ring around the P transistor and a P+ ring around the N transistor.

Positive bias latch-up: All pins show no latch-up for positive bias of up to +16V. Above +16V, gate assisted breakdown may occur destroying the device.

Negative bias latch-up: Negative bias latch-up tests show that all pins on PEEL Devices and PEEL Arrays will withstand 100mA and most pins will exceed 250mA. The reliability data listed in Table 7 shows actual worse case trigger current measurements for negative bias latch-up (Vcc=5V, Vss=0).

Device Type	Current
PEEL18CV8	160mA
PEEL22CV10A	160mA
PEEL20CG10A	160mA
PA7024	250mA
PA7128	270mA
PA7140	270mA

Table 7. Negative Bias Latch-up

Electro-static Discharge (ESD)

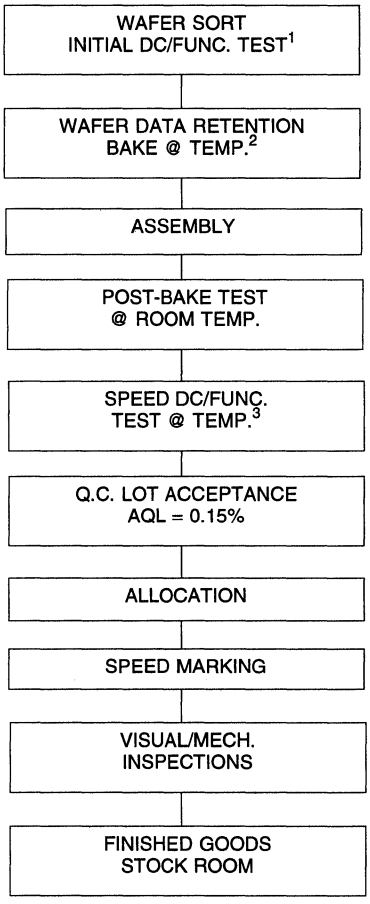
Electrostatic discharge (ESD) is evaluated per MIL-STD-883 Method 3015. The procedure implements a destructive test in which device pins are subjected to multiple ESD pulses at progressively increased voltages. Leakage current is monitored until a leakage current of greater than 1uA is measured at the pin. Electrostatic Discharge (ESD) testing on PEEL Devices and PEEL Arrays shows that all pins can withstand greater than 2000V.

Production Test Flow

ICT has developed a test flow to ensure that all products shipped to customers are of the highest quality and reliability. Each device is erased, programmed, and read at Wafer Sort, Package Test, and QA Test to guarantee electrical characteristics over the entire operating temperature range and functionality of the part. Test programs are developed to screen out those devices which fail to meet data sheet specifications.

Rather than relying exclusively on lot sample based reliability data, ICT has also incorporated 100% data retention verification into its standard production test flow. The test programs are developed to screen out those devices which fail to meet data sheet specifications. This is accomplished by subjecting all devices to a wafer-level data retention bake which verifies the ability to retain data for at least ten years over the entire temperature range (0 to 70°C for Commercial and -40 to 85°C for Industrial).

Figure 1 shows the general test flow for ICT's 1.0 micron CMOS EEPROM-based product.



Notes :

1. All functional and parametric parameters are tested at room temperature. Proper Program/Verify operation is tested via multiple erase, write, and read tests.

2. A proprietary procedure determines the time and temperature of the Data Retention Bake which verifies that the device will hold data for greater than ten years of operation at the maximum rated operation temperature.

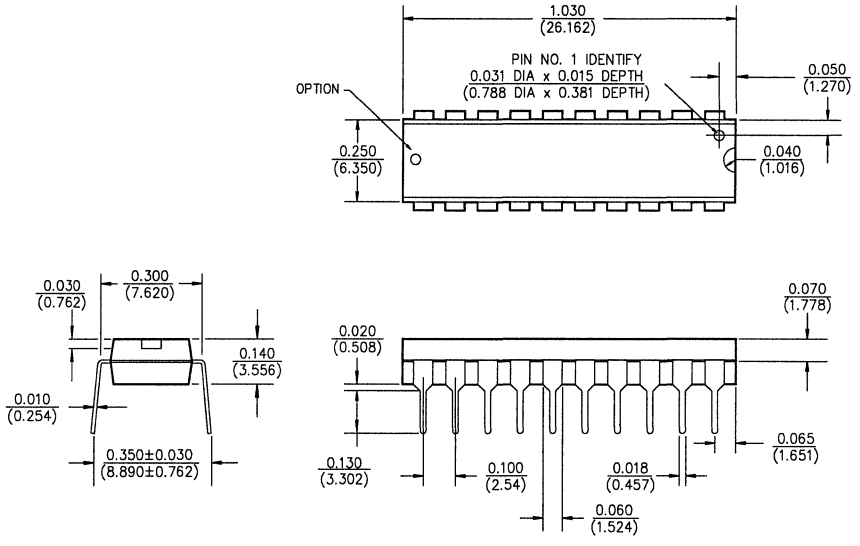
3. Devices are tested at data sheet specifications.
Commercial Temp.=0°C to 70°C
Industrial Temp.= -40°C to 85°C

Figure 1. Test Flow for 1.0 Micron Products

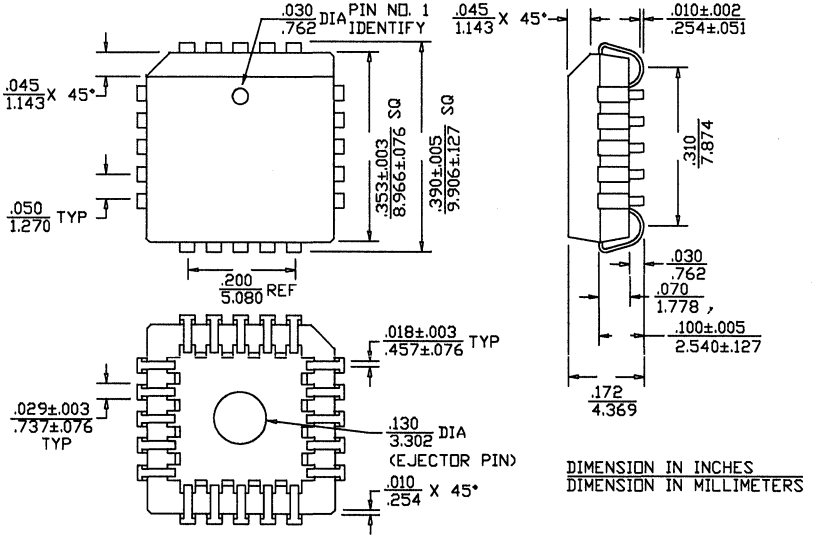
Package Information

Package Diagrams 6-3

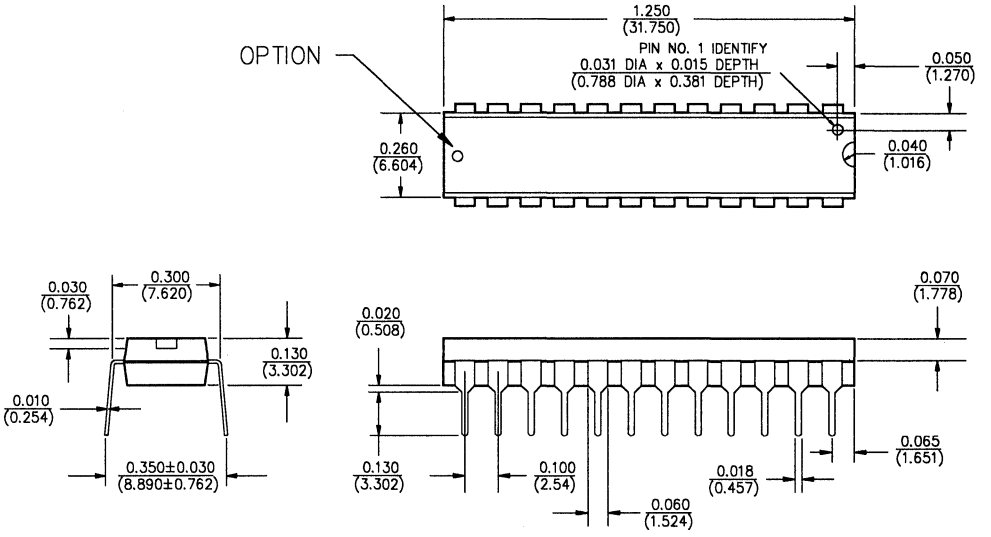
Package Diagrams



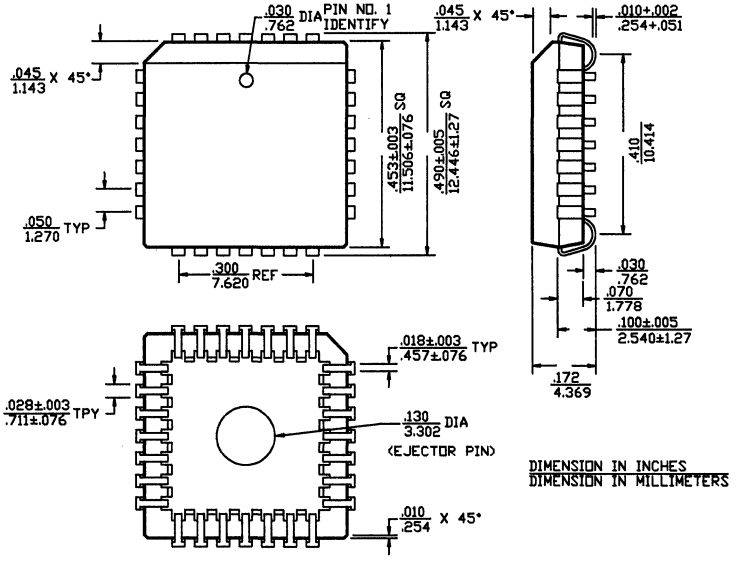
20-Pin Plastic DIP (P20)



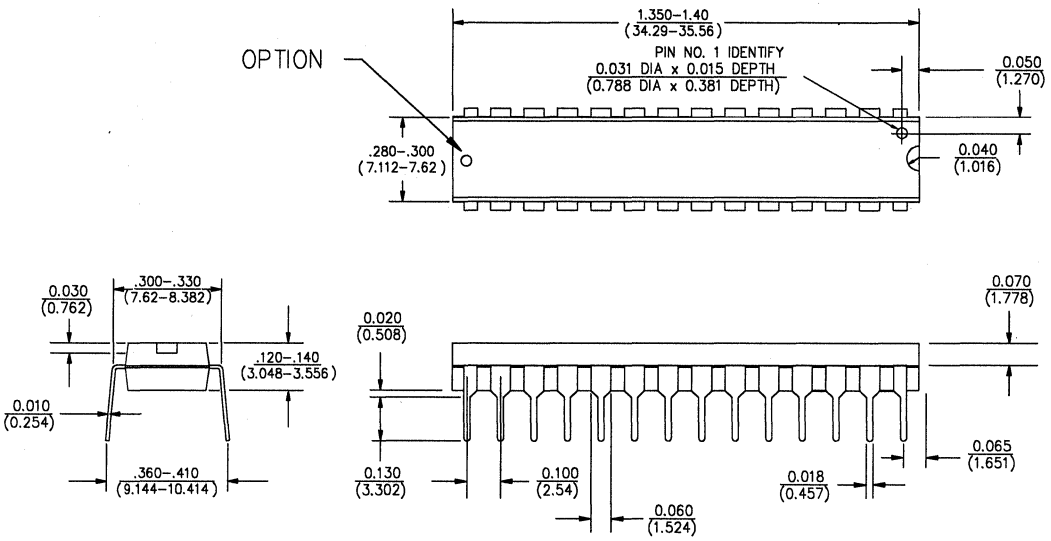
20-Pin PLCC (J20)



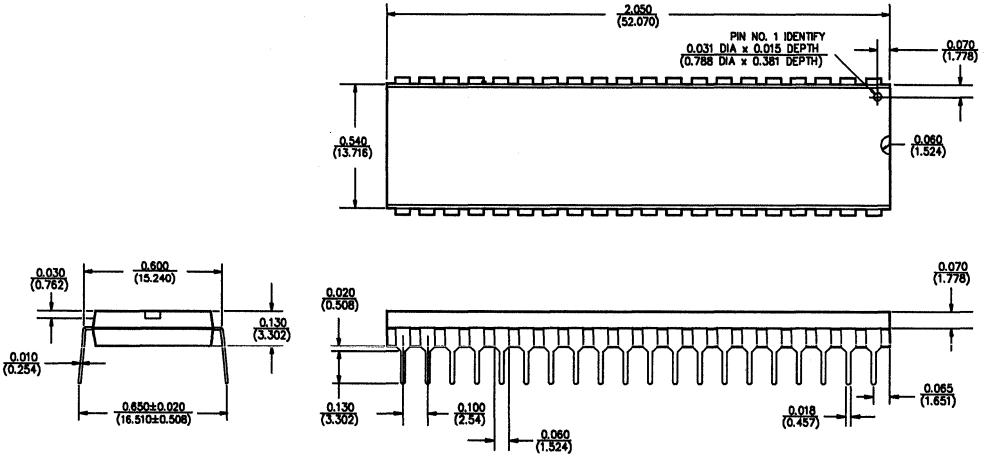
24-Pin Plastic DIP (P24)



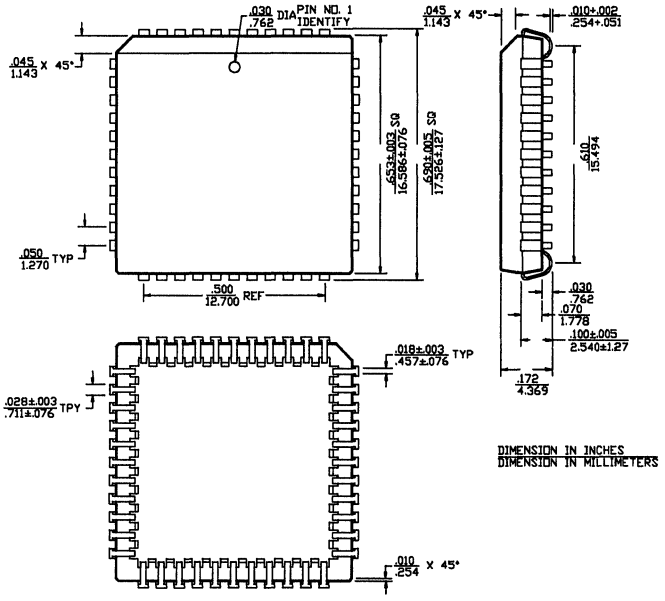
28- Pin PLCC (J28)



28-Pin Plastic Dip (P28)



40-Pin Plastic DIP (T40)



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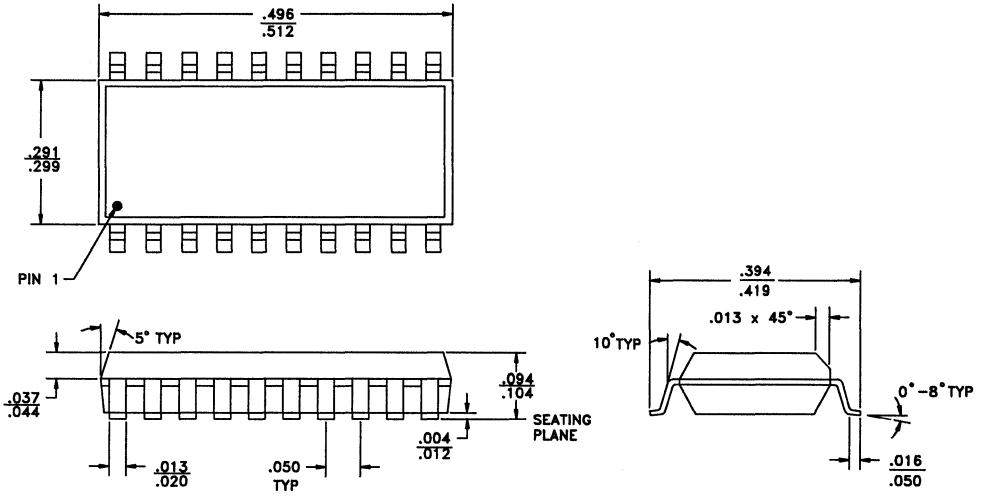
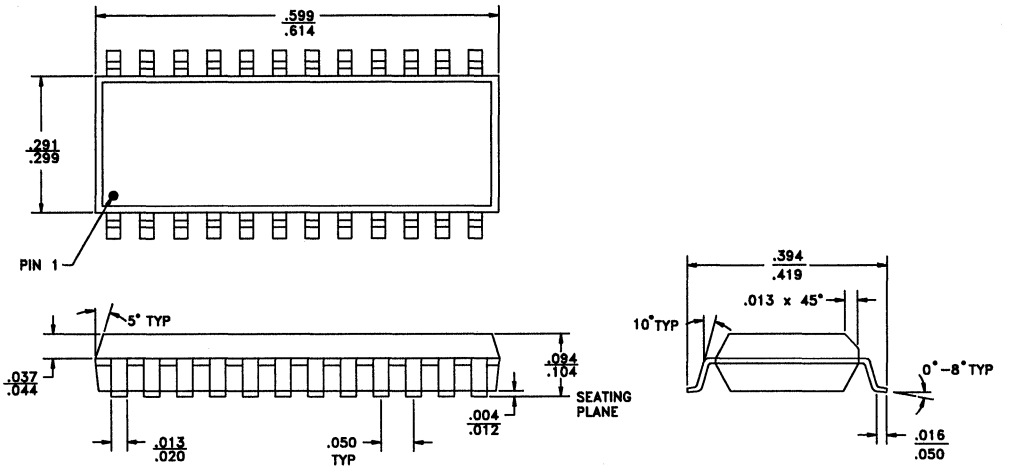
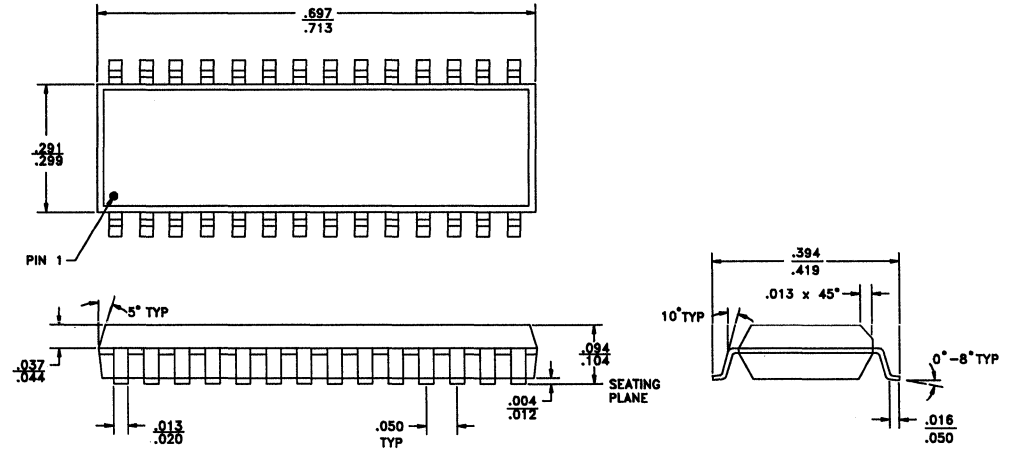


20-Pin SOIC (S20)



24-Pin SOIC (S24)



28-Pin SOIC (S28)

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San Jose, California 95131
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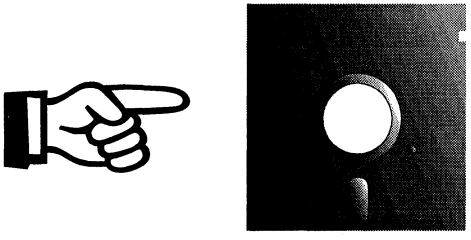
ICT's PLACE Development Software is available free to qualified PLD users!



For more infomation contact your local ICT representative as listed in Section A on the previous pages

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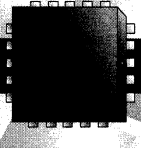
PLACE™ Software Users Manual

For PEEL Arrays and Devices



1993 / 1994

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Introduction to PLACE

7.0 Introduction to PLACE™

7.1 PLACE Advanced Development Software

Welcome to the PLACE Advanced Development Software from ICT, Inc. PLACE (PEEL Logic Architectural Compiler and Editor) is an enhanced development package that offers complete support for ICT's family of PEEL (Programmable Electrically Erasable Logic) Arrays and Devices.

The PLACE Advanced Development Software is free to qualified PLD users. To obtain a copy of PLACE please contact your local ICT representative (see Section A).

PLACE Features

Architectural Editor

PLACE incorporates an innovative architectural editor which graphically illustrates and controls the architectures, logic equations, state-diagram and truth-table entries, hence making the overall design easy to understand while allowing for optimum utilization.

Logic Compiler

The PLACE compiler performs logic transformation allowing equations to be specified in most any fashion. The compiler also features five levels of user-selectable logic reduction (including "auto-demorganization") making it possible to fit more logic into every design.

Logic Simulator

PLACE provides a multi-level logic simulator that lets the external and internal signals be fully simulated, analyzed and edited via a graphically illustrated waveform display.

Documentation

PLACE designs can be documented through batch printing of the logic design description, architecture and waveform displays.

Programmer Interface

Programming is supported by a direct interface to the ICT PEEL Development System programmers: PDS-1, PDS-2 and PDS-3, and by other popular programmers via the serial communication port or by automatically executing the third-party programming software from within PLACE.

7.2 PLACE Introduction

The PLACE Software portion of this description is organized in six sections. Before trying to design with the PLACE software, make sure you read through the three sections: "Introduction", "Installation" and "Getting Started". By doing so you will save yourself time.

After you have completed installing the PLACE software and have become familiar with the basic operations, you can refer to sections 8 and 9 on "Operation Reference Guide" and "PLACE Design Language Reference Guide" as you implement your first design. Documentation describing several application examples are provided in chapter 10. These examples are also included on diskette and will automatically be loaded during installation.

While using this manual and the software you may need to reference the product specifications in the data book.

The software operations and features described in this manual are referenced to PLACE Version 2.50. For additional information on new features and manual corrections, please refer to the README.DOC file on the PLACE disk.

7.3 PEEL Device and PEEL Array support

The devices supported in the PLACE software include:

PEEL Arrays

PA7024	PA7140	PA7128

PEEL Devices

PEEL18CV8	PEEL22CV10A
PEEL20CG10A	PEEL22CV10A+

Additional devices will be supported in future software versions.

7.4 Converting APEEL File ".APL" to PLACE File ".PSF"

ICT has discontinued further development of its original PEEL software named APEEL. All products are now supported by PLACE. If you still use APEEL for development your designs can be converted to the PLACE design language format by using the APL2PSF (APL2PSF.EXE) utility. This allows the PLACE enhanced features available for the PEEL Arrays to be used to implement designs for the lower density PEEL devices.
The format for the APL2PSF utiltiy is:

APL2PSF *filename*

The extension of the *filename* defaults to ".APL" if not specified.

7.5 JEDEC Translation

JEDEC-file translation utility of the PLACE Software translates JEDEC files created for programming other PLD's (PALs, GALs, EPLDs etc.,) to JEDEC files used for programming PEEL devices. The translated JEDEC file will program a PEEL device to be a pin-for-pin replacement for the original PLD. The utility translates JEDEC files that have been written on a disk. If a disk file is not available, the pattern may be read from a master device with ICT's PEEL Development System or a third-party programmer. When a third-party programmer is used, the software will allow the file to be up loaded through a serial port and written to a file.

The translated PEEL JEDEC file is given the name of the original file with the ".JED" extension modified to ".JEX". The ".JEX" file can then be used to program your PEEL devices. The translator can be accessed directly from DOS or through the PLACE Utilities menu.

Using the JEDEC File Translator from DOS

The PEEL device translator program is contained in a file called PEELXLT.EXE on the program diskette. When using PEELXLT.EXE, you must specify a PLD source file name, a source PLD type, and a target PEEL device type. Type: "PEELXLT source_filename source_PLDtarget_PEEL_device". An example is given below:

```
PEELXLT B:\R8CNTR 16R8 18CV8
```

In the above example, the JEDEC file "R8CNTR.JED" (which is included on the disk as an example) is translated from a PAL16R8 to a PEEL18CV8 device. Process creates the PEEL device JEDEC file "R8CNTR.JEX". You need not specify the extension for the PLD source file name because it is assumed to have a ".JED" extension. Do not specify device family (eg. PAL, PEEL, etc...) or manufacturer (eg. AMD, Lattice, etc.) for source PLD and target PEEL device number.

Using the JEDEC File Translator from the PLACE Utilities Menu

After PLACE has been fully installed, the translator can be accessed from the "Translate" selection in the PLACE Utilities menu. Accessing the translator from PLACE, a sequence of menus are provided to aid in the translation process. From the first file menu, select Read/Translate and the file to be translated, then follow the menu driven commands. Note that the translator is not mouse driven, all commands must be selected from the keyboard.

These devices can be translated to the PEEL18CV8

PAL16L8	PAL16R8	PAL16R6	PAL16R4
PAL16P8	PAL16RP8	PAL16RP6	PAL16RP4
PAL10L8	PAL12L6	PAL14L4	PAL16L2
PAL10H8	PAL12H6	PAL14H4	PAL16H2
PAL16H8	PAL16LD8	PAL16HD8	PAL18P8
PAL18V8	GAL16V8	EP310	EP320
5C031	5C032		

These devices can be translated to the PEEL20CG10A, PEEL22CV10A/A+

PAL20L8	PAL20R8	PAL20R6	PAL20R4
PAL20L10	PAL20L2	PAL18L4	PAL16L6
PAL14L8	PAL12L10	PAL22V10	PAL20G10
PAL20AP10	PAL20RP8	PAL20RPG	PAL20RP4
PAL20ARP4	PAL20ARP6	PAL20ARP8	PAL20ARP10
GAL20V8			

PLACE Installation

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PLACE Installation

8.0 PLACE Installation

8.1 System Requirements

- ☐ IBM PC, XT, AT, 386, 486 or compatible
- ☐ Minimum 560K RAM memory for all designs.
- ☐ EGA, VGA, SVGA or Hercules Graphics.
- ☐ A hard disk with at least 4.0 MB free space.
- ☐ Microsoft mouse or compatible with driver
- ☐ DOS version 3.0 or greater
- ☐ (Optional) Expanded Memory with LIM specification version 3.2 or higher.
- ☐ If using PDS-2 or PDS-3 programmer, one communication port (serial port).

8.2 Hard Disk Installation Procedure

- Turn the computer on.
- Boot-up DOS 3.0 or higher.
- Install your mouse driver, otherwise PLACE will not boot-up.
- Insert the PLACE original disk into drive A. Do not write-protect this disk.
- At the A> prompt, type "INSTALL" followed by the [ENTER] key. Note that you can abort the installation any time by pressing Ctrl-Break.
- Type in your company name and address, installation date, and your name.
- Select your options. Enter the directory you want PLACE to be installed to. Default drive and directory is C:\ICTPLACE.
- Once installation is completed, type "INIT" to initialize the PLACE software. For subsequent use of the PLACE software, type "PLACE" followed by the [ENTER] key.

☐ (Optional) If you wish to run PLACE from any directory, you can do this by adding the following to your AUTOEXEC.BAT file. Assuming "C:\ICTPLACE" is the installed directory, you would add "C:\ICTPLACE" to your DOS path and insert "SET ICTPLACE=C:\ICTPLACE".

☐ ICT recommends using the Logitech or Microsoft mouse for proper operation of the PLACE Software.

- It is recommended that MS Dos 5.0 (or greater) users minimize the usage of the TSR programs (i.e. PC pop-up calculator program), so that the computer has enough memory to run the PLACE software. The command for loading TSR programs into upper memory is:

  LOADHIGH(LH) PC-CALC.EXE (to load PC-CALC.EXE into upper memory).

  Dos will not tell you if the procedure is successful or not. If the procedure was not successful the program will occupy the conventional memory. To check if the program was loaded into upper memory enter the command MEM /C and note the programs location in memory

- For Dr. Dos 6.0 users please read the file DRDOS6.DOC before installing the PLACE software.

8.3 Initializing the PLACE Software using "INIT"

After each PLACE installation, it is recommended to initialize the PLACE software by typing "INIT" followed by the [ENTER] key in the PLACE directory. The initialization procedure erases the "PLACE.SAV" file which stores the set-up configurations of the PLACE software. Once this file is erased, the PLACE software during boot-up (i.e., by typing "PLACE" followed by the [ENTER] key) sets all of the configuration variables except for the color, graphic adapter (VGA only) and mouse type variables to the default conditions.

You can re-initialize PLACE any time you run into problems with the software, or if you want to change the set-up configuration variables.

VGA Graphic Adapter Option

If a VGA monitor is being used, the PLACE software can be set to operate using the 640X350 (EGA) or 640X480 (VGA) resolution. In most cases, the VGA resolution is preferred because the graphics are much cleaner and distinct. The EGA resolution option is provided in case a problem is encountered using the VGA resolution. If you are running PLACE for the first time, you may want to experiment with both options before starting your designs.

Color Type Option

This option allows the PLACE software to be displayed in 2 (monochrome) or 16-color mode. For Hercules monitors, always select the 2-color mode, i.e. answer "N" for No when prompted for the color option.

Mouse Type Option

The PLACE software allows multiple mouse cursor types to be displayed depending on the mode selected (e.g. Edit Eqn, Edit Arch, Label, and etc.) in the Design operation. For instance, a left-pointing arrow ("<-") mouse cursor indicates the current mode is the "Edit Eqn" mode. Figure 8-1 illustrates the different mouse cursor types found in the Design operation. In addition, each of the PLACE operations has its own unique mouse cursor.

Programmer Type Option

The Place Software allows initialization of PDS series programmers (PDS-1, PDS-2, PDS-3).

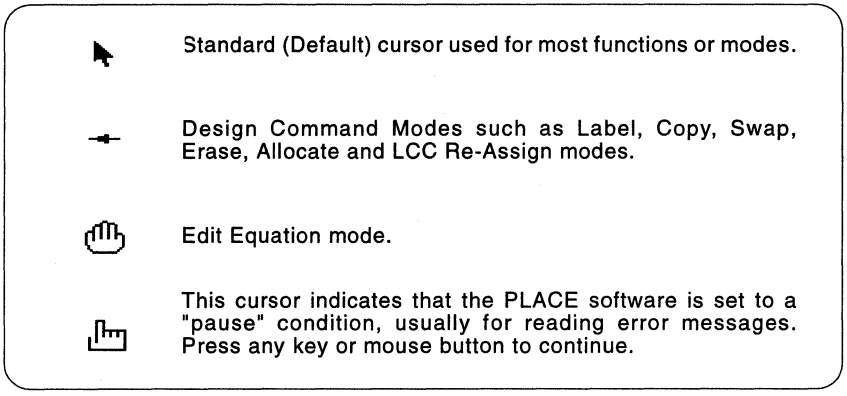

Figure 8-1, Multiple Mouse Cursor Types

If you are experiencing mouse problems with the multiple cursor mode, it is recommended to select the single cursor type in the initialization procedure.

Getting Started with PLACE

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Getting Started with PLACE

9.0 Getting Started with PLACE

9.1 Entering the PLACE software

Once PLACE is properly installed (i.e. PLACE was initialized by using "INIT"), it can be entered by typing "PLACE" while in the ICTPLACE directory. Pressing the ENTER key twice after typing "PLACE" will bypass the boot-up messages. If you wish to enter PLACE from any directory, see section 8.2 or 8.3 on "Hard Disk Installation Procedure". Before using the PLACE software, please read through the following sections on "Using the Mouse" and "Getting HELP".

9.2 Using the Mouse

The PLACE software and manual will commonly refer to several mouse actions using the nomenclatures specified in Table 9-1.

Term	Mouse Action
Click	press/release the left button of mouse.
Click-R	press/release the right button of mouse.
Click-LH	press/hold the left button of the mouse while moving the mouse.
Click-RH	press/hold the right button of the mouse while moving the mouse.
Click-MH	press/hold the middle button of the mouse while moving the mouse(3-button mouse only).

Table 9-1, Nomenclatures for PLACE mouse actions

Note that the default mouse cursor is a North-West pointing Arrow. However, several cursor types (Figure 8-1) may appear depending on whether option #1 of the mouse cursor types was selected during the PLACE initialization procedure (section 8.4), or on the type of mode or function that was selected in the PLACE software.

"Click" - press/release left button

"Click" is used in all operations and modes to make a selection. A selection can be made by moving the mouse cursor to the desired item, and press/release the left button of the mouse. In many cases this selected item will be highlighted. Items that can be selected include pop-down and pop-up menu windows, architectural elements in the design operation such as Logic

Control Cells (LCC), I/O Cells (IOC), Input Cells (INC), Global Cells (GBC), test vector waveforms (Simulate operation) and etc.

"Click-R" press/release right button

"Click-R" in most cases is used to exit, complete or return from the current function being performed. **In the Design operation, Click-R is also used to toggle back and forth from the default "Edit Architecture" mode to the "Edit Equation" mode.**

"Click-LH" or press/hold the left button while moving the mouse

Click-LH is used in both the Design and Simulate operations. In the Design operation, it is used to scroll from one LCC/IOC to another in the LCC/IOC screen. In the Simulate operation, it is used for panning in the waveform screen as well as block selection for the copy, move, and delete functions in the "Edit" mode.

"Click-RH" and "Click-MH" or press/hold the left and right button respectively while moving the mouse

For 3-button mouse systems, click-MH (click-RH for 2-button mouse) is used to display the menu options in the PLACE text editor utilized in the Design or Program operation. While holding the middle mouse button down (right button for 2-button mouse), move the mouse cursor and click at the menu option. Once the option is selected, the middle button can be released.

Mouse support in the PLACE Text Editor

Mouse is supported in the PLACE Text Editors which are used within the Design, Compile and Program operations. To initiate the mouse support, press the middle button (3-button mouse) or right button (2 button mouse) of the mouse but don't release the button. Move the mouse cursor to the top of the screen to select the functions. Table 9-2 lists the mouse actions in the text editor.

Re-initializing the mouse in PLACE

In the event a mouse problem is encountered, press the [ESC] key as many times as needed to exit the current mode or function to return to the main screen of the operation (Design, Compile, Simulate, Document and Program). Then, press the [Alt]-M keys (simultaneously press the [Alternate] and character "M" keys) to re-initialize the mouse.

Mouse Action	Function
Click within the text area	Move the text cursor to the mouse cursor
Click at the top border area	Scroll 6 lines up
Click at the bottom border area	Scroll 6 lines down
Click at the first line of the text	Scroll 1 line up
Click at the last line of the text	Scroll 1 line down
Click-R (right button)	Exit editor (3-button) Access mouse menu (2-button)
Click-M (middle button)	Access mouse menu (3-button only)

Table 9-2, PLACE Text Editor Mouse Actions

9.3 Getting HELP

The PLACE software incorporates an on-line HELP feature which provides information and procedures for most PLACE functions and modes. To get HELP information, just point the mouse to the menu function or mode and simultaneously press the [F1] key. Besides this on-line command HELP, a general HELP menu is provided in the Utilities pop-down menu.

9.4 A Guided Tour through the PLACE software

To quicken the learning process, this section discusses some basic procedures commonly used in the PLACE software. The device used in this guided tour is the PA7024. So, some of the terms used in this section may only be applicable to the PA7024 device (or the PEEL Array family of devices). For instance, terms such as LCC (Logic Control Cell) and GBC (Global Cell) pertain only to devices in the PEEL Array family.

If you are a first-time PLACE user, it is recommended that you run the PLACE software while reading this section. By actually performing the instructions (specified in *italics*), you will be able to get a more complete understanding of the features, modes or functions found in the PLACE software.

There are five main operations that can be performed with PLACE; Design, Compile, Simulate, Document and Program. When first entering PLACE, it will default to the Design Operation in the edit architecture mode ("Edit Arch"). The display will show the PA7024 PEEL Array pin block diagram (Figure 9-1).

Note that PLACE automatically loads the ANEW template file upon initial boot-up. In Figure 9-1, the PLACE software has loaded the ANEW file (ANEW7024.PSF) for the PA7024 device. There is an ANEW template file for each device supported by the PLACE software. For instance, the

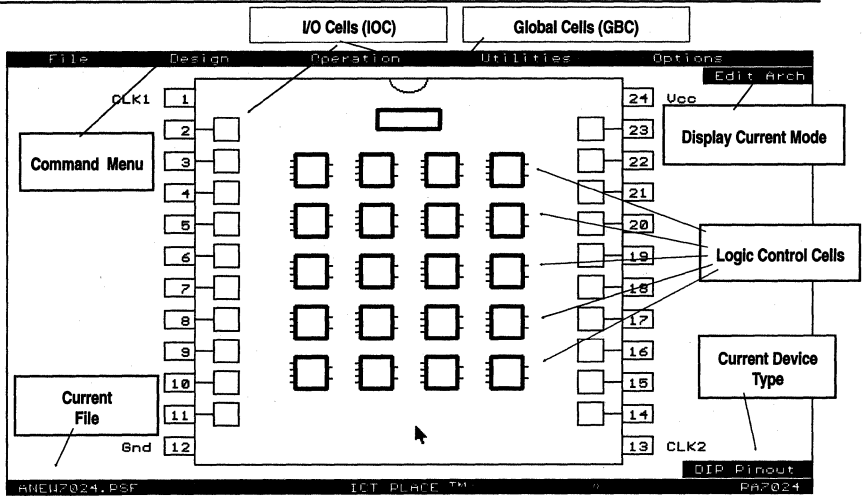

Figure 9-1, The PA7024 Pin Block Diagram screen in the Design Operation

ANEW7140.PSF file is the template file for the PA7140 device. Each ANEW file contains the device's default cell configurations.

At the top of the screen, there are five pop-down menu options: File, Design, Operations, Utilities and Options (available only in the Design operation). *Move the mouse cursor to the "Operation" menu.* A pop down window will appear showing the five main operations (Figure 9-2). Note the menu option titled "Design" to the left of the operation menu. This menu is called the "command" menu. Each time a new operation is selected, this command menu will change to allow the selection of commands specific for that operation. The command menu is also used as an indicator for the current operation.

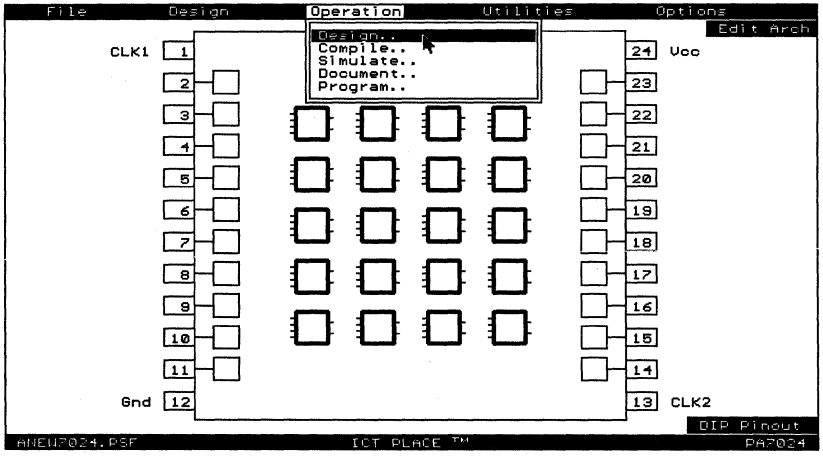

Figure 9-2, The Operations pop-down menu

Move the mouse cursor to the "File" menu option and Click the "Read" command. A list of the PLACE Source Files (.PSF) will appear (Figure 9-3). The design examples provided with the PLACE software include:

- ❑ Multiple-Application Design Example (PA7024, DEMO1A.PSF)
- ❑ Basic Gates (PA7024, GATES1.PSF)
- ❑ Basic Registers and Latches (PA7024, REG1.PSF)
- ❑ 8-Bit Counter with Hold, Reset and Preset (PA7024, COUNTER1.PSF)
- ❑ Bi-Directional I/O Port (PA7024, BI_PORT1.PSF)
- ❑ Bus Programmable Clock Generator/Timer (PA7024, TIMER.PSF)
- ❑ Blackjack Machine Example (PA7024, JACK7024.PSF)
- ❑ Timer/Counter (PA7140, TC7140)
- ❑ 4-Bit State Machine with 8-Bit Counter Application (ST7128, PA7128)
- ❑ Basic Gates (18CV8, V8GATES.PSF)
- ❑ Basic Registers and Latches (18CV8, V8REGS.PSF)
- ❑ Clock Divider and Address Decoder (18CV8, V8CLKADD.PSF)
- ❑ Bus Programmable 8-to-1 Multiplexer (18CV8, V8BUSMUX.PSF)
- ❑ 8-Bit Counter with Function Controls (18CV8, V8FCNTR.PSF)
- ❑ Change-of-state Input Port with Interrupt (18CV8, V8CPORT.PSF)
- ❑ Octal Synchronization Circuits (18CV8, V8SYNC.PSF)
- ❑ 8-Bit Up/Down Loadable Counter with Carry-out or Borrow-in (PEEL22CV10A, V10CNT8.PSF)
- ❑ 9-Bit Even/Odd Parity Generator/Checker (PEEL22CV10A, PARV10A.PSF)
- ❑ 8-Bit Change-of-State Input Port with Interrupt (PEEL22CV10A+, V10PORT.PSF)

As shown in Figure 9-3, there are two methods of making a selection from the file menu window.

1. Click to highlight a file or directory, and then click at the [OK] selector.
2. "Double Click" at the file or directory. The first click highlights the selection, and the second click makes selection.

Click the DEMO1A.PSF file. The PLACE Design operation will once again be displayed, but this time with the DEMO1A demonstration design file. For more detail information on the demonstration example files refer to chapter 12 of this manual.

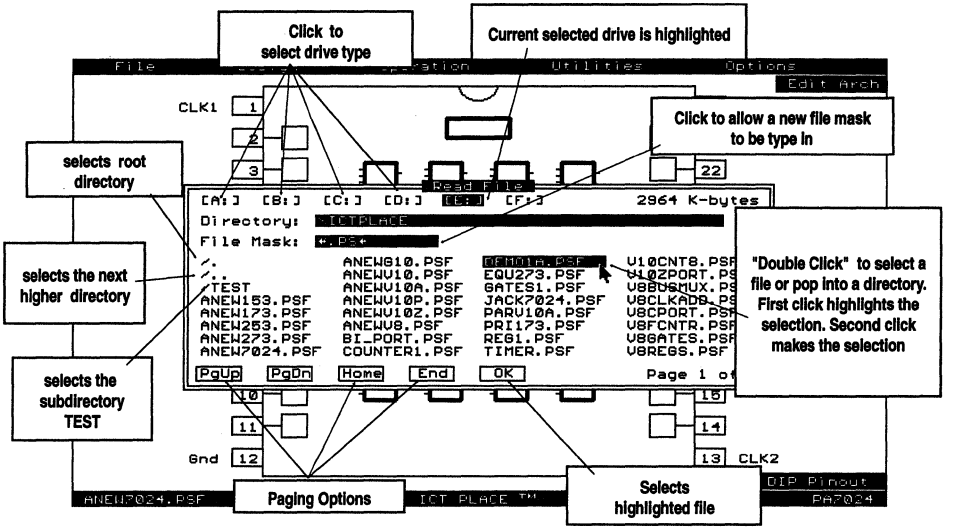

Figure 9-3, Reading a demonstration file from the File menu

Once the file is loaded, *move the mouse to the "Design" menu option at the top of the screen* (Figure 9-4). *Click at the "Title" command.* A window will appear on the screen displaying the title, designer and date of the design. The title of the design can now be entered by typing in the characters from the keyboard. *Click or press the [ENTER] key to move the cursor to the next Title field. Click-R or press the [ESC] key to exit this mode.*

Move the mouse cursor back to the "Design" menu option and click the command listed as "Description". The screen will now display the description of the design (Figure 9-5). *Move the mouse cursor into the displayed window and click the mouse button.* This procedure allows the design description to be entered or modified by having the PLACE software automatically open the text editor and highlight the text. *Press [ESC] to exit the text editor.*

With a 3-button mouse, click-R exits the text editor and returns to the previous screen. For the 2-button mouse system, click-RH (press and hold the mouse right button) to allow selection of the text editor menu at the top of the screen. Then while the right button is still held down, click at the "ESC" menu option to exit the editor. Please refer to section 10-14 on "Text Editor Commands" for more information.

From the pin block diagram screen move the mouse cursor to the "Design" menu option and click the "Label" command. Notice that the mouse cursor changes from a North-west pointing Arrow to a Hand cursor (the Hand cursor is available only if option #1 of the mouse cursor type was selected during the PLACE initialization procedure). *Now move the cursor to one of the Logic Control Cells (LCCs), Input/Output Cells (IOCs), or Input Cells (INCs - PA7140 only) and click the mouse button.* A window will appear displaying the current label (or name). Figure 9-6 shows the I/O cell #2 was selected in

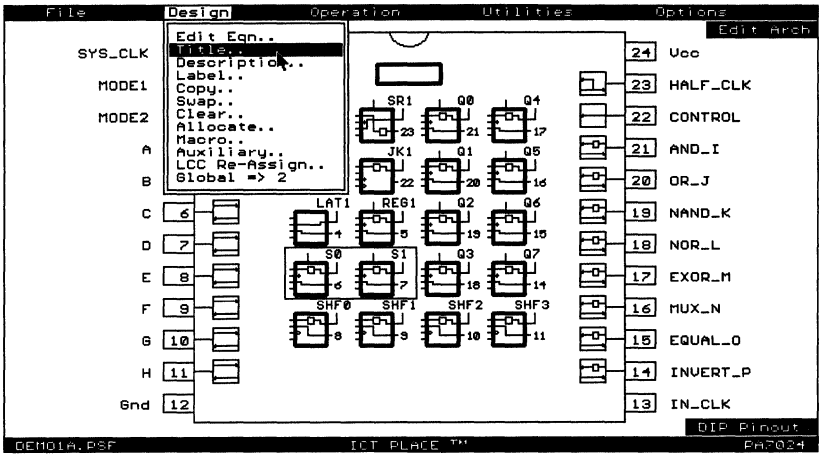

Figure 9-4, The "Design" command menu

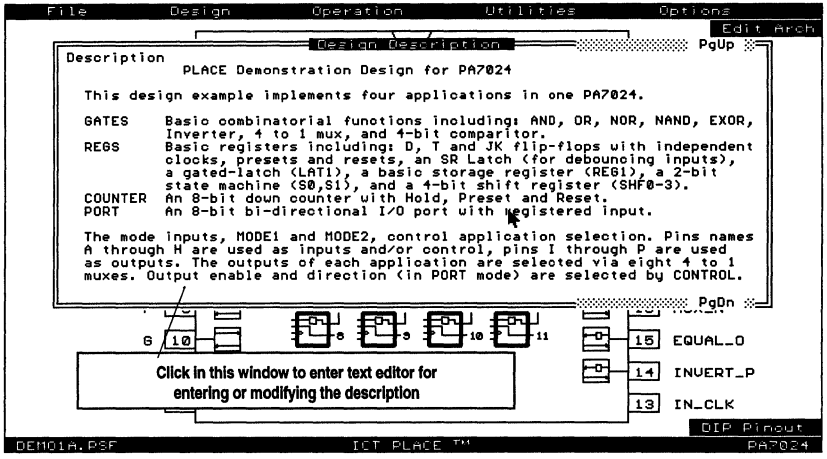

Figure 9-5, The "Description" window

the Label mode. To change the label use the [BACKSPACE] key and type in the new label followed by the [ENTER] key. The Label command is used to define all IOCs, INCs and LCCs that are used in a design.

The architecture of the LCCs, IOCs or INCs can be configured prior to labelling. However, labels must be specified before the equations, state-diagrams or truth-tables can be entered. Please refer to Chapter 10 "Operation Reference Guide" for options on the "Label" command.

Click-R to exit the "Label" mode and return to the "Edit Arch" mode. Now, move the cursor to one of the LCCs. Note that both the LCC and its interconnected IOC will be highlighted. *Click the mouse to bring up the*

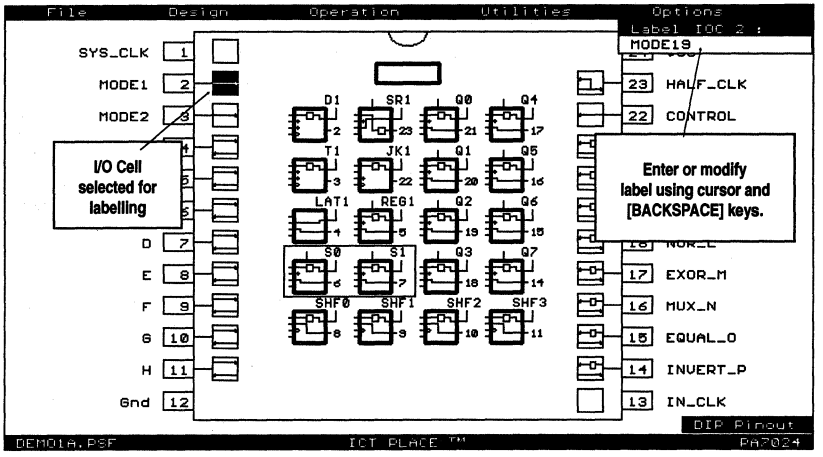

Figure 9-6, The "Label" command for Pin, INC, IOC and LCC

associated "LCC and IOC Screen". This screen displays a close-up view of the selected LCC and its associated IOC configuration.

Select the configuration of the cells by clicking at any of the "select indicators" (Figure 9-7). With the PA7024 device, over 4000 configurations can be selected by clicking at each of the select indicators. Any time the mouse cursor is moved away from a select indicator, the pop-up window is cleared. *Click-LH (press/hold left mouse button) and move the cursor left and right or up and down.* This allows panning from one cell to another without returning to the pin block screen. Notice that the miniature pin block diagram in the upper left corner displays the current LCC/IOC location.

Move the cursor into the "D" OR or Sum-D gate (shown in Figure 9-7) and click the mouse button. A window displaying the equation for the selected OR gate will be opened. This window will be referred to as PSF Text Display Window. The size of the window can be increased or decreased by pressing the [Up] or [Down] cursor key, and followed by the [ENTER] key (refer to Chapter 10 "Operation Reference Guide" for more information on the PSF Text Display window). *Click-R to close the display window. To return to the pin block diagram screen, click-R once again or press the [ESC] key.*

The Global Cell (GBC) configuration can be selected by the same process, i.e. by clicking the select indicators in the cell (Figure 9-8).

There are multiple global cells in all PEEL Arrays. For instance, the PA7024 device has two global cells which are called Global Cell A and B. The default condition for the PA7024 (and all PEEL Arrays) is the one global cell mode. The two global cell mode can be selected by clicking at the "Global = 2" command found in the "Design" menu window. With two global cells, Global Cells A and B control global signals for all LCCs connected to the IOCs located on the left (pins 2 to 11) and right side (pins 14 to 23) of the pin block diagram respectively. Please refer to the PEEL Array data sheet for more information on the global cells.

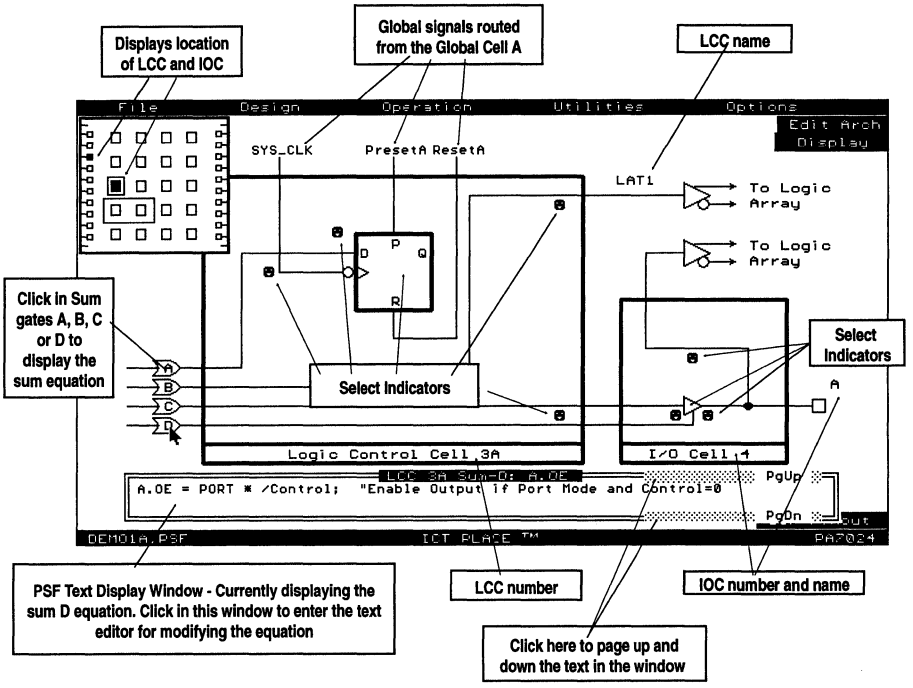

Figure 9-7, Configuring the LCC and IOC Architecture

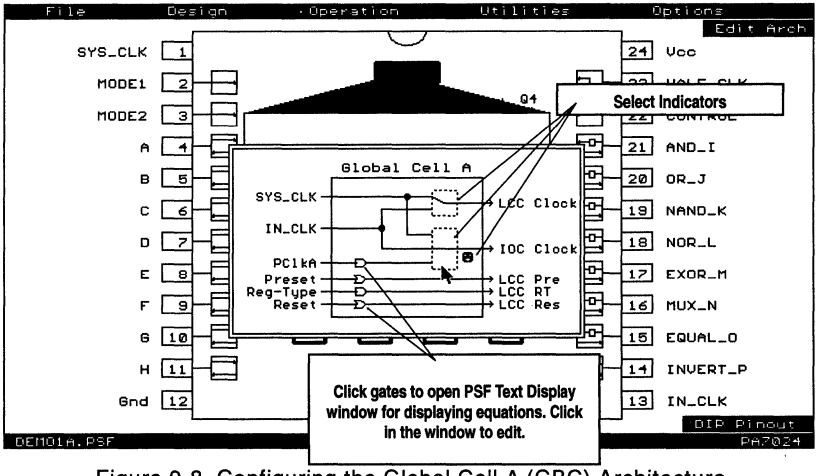

Figure 9-8, Configuring the Global Cell A (GBC) Architecture

In the pin block screen, move the mouse cursor to the "Design" Command pop-down menu again. Click the command listed as "Edit Eqn" for edit equation. Notice that the mouse cursor has changed to a "<-" (arrow) which is the Edit Equation cursor. *Move the cursor to one of the four inputs of any*

LCC and the input will be highlighted. Click to select the input equation. In Figure 9-9, the PSF Text Display window displaying the sum-C equation was selected from the third input of the LCC "QO".

Move the mouse cursor to the "Display" option located in the upper right corner of the screen and click the mouse button. This opens a window listing the options for opening an additional PSF Text Display window. *Move the cursor to highlight the "Macro Definition" option and click the mouse button.* The PSF Text Display window showing the macro definitions specified in the design will appear (Figure 9-10).

Move the cursor to the inside of the PSF Text Display window and click the mouse button. This enters the text editor which is used for editing boolean equations, state diagram and truth table syntax. The selected equation will be highlighted (Figure 9-11). Note that equations can also be selected for the LCC/IOC screen by moving the cursor to the one of the four "Sum" inputs and clicking the mouse button (Figure 9-7). Equations for the Global Cell can also be selected this way (Figure 9-8). Once inside the editor, most of the standard Wordstar™ commands can be used (see Chapter 10 for the command reference information on the text editor). *Click-R or press the [ESC] key to return to the pin block diagram screen again.*

After returning from the text editor, the "Edit Eqn" mode is still selected (indicated by the "<-" mouse cursor). *Click-R and the cursor will change back to the default "Edit Architecture" cursor.* Click-R will toggle back and forth between Edit Equation and Edit Architecture for quick access to both modes.

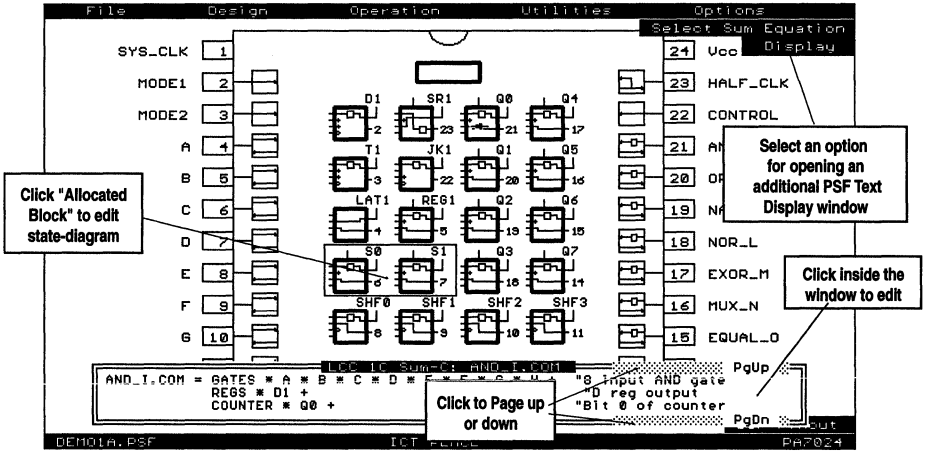

Figure 9-9, Selecting equations from the block diagram screen

If you have followed the instructions up to this point you have now familiarized yourself with the basic functions of the Design operation in the PLACE software. *Now, move the cursor to the "File" menu option and click the*

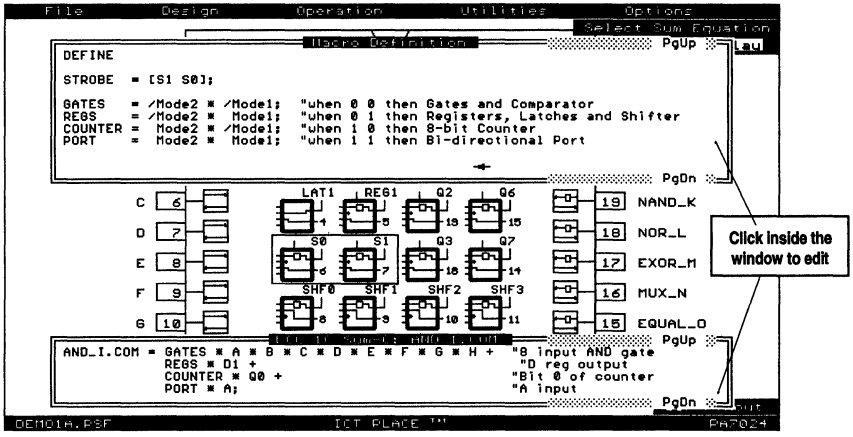

Figure 9-10, Selecting equations from the block diagram screen

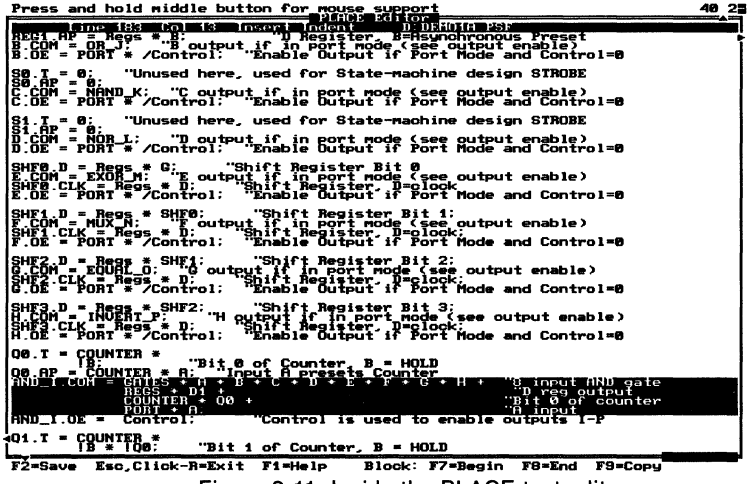

Figure 9-11, Inside the PLACE text editor

"SaveAs" command. The file window will appear (figure 7-12). *Move the cursor to the box named "NEW" and click the mouse button. Type in the name "TEMP" or any other new name to save your modified file.* If the file extension is omitted, then it will be defaulted to ".PSF".

Once your Design file is saved, select the File pop-down window again and read in the "GATES1.PSF" design example. Move the mouse cursor to the Operations pop-down window and try selecting the other operations starting with Compile, Simulate, Document, Program and back to Design. The screens should look as displayed in Figures 9-13 through 9-16. For more information on the commands and functions in the five main operation, please refer to the "Operation Reference Guide" in Chapter 10.

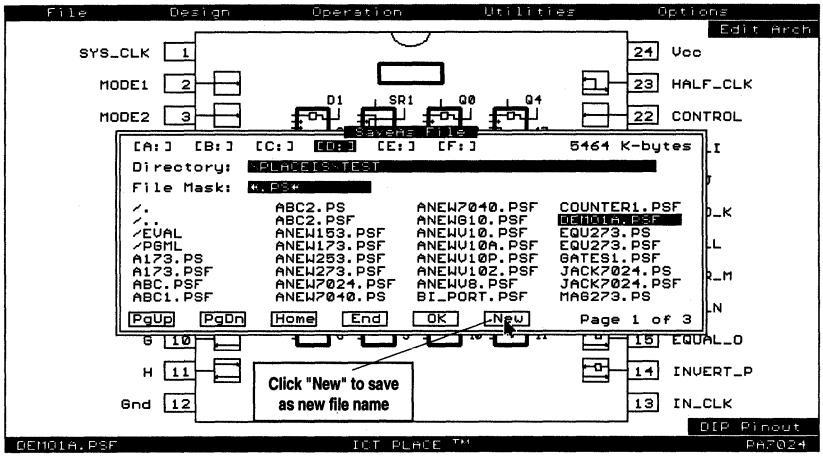

Figure 9-12, Using "SaveAs" to save a new PLACE source file

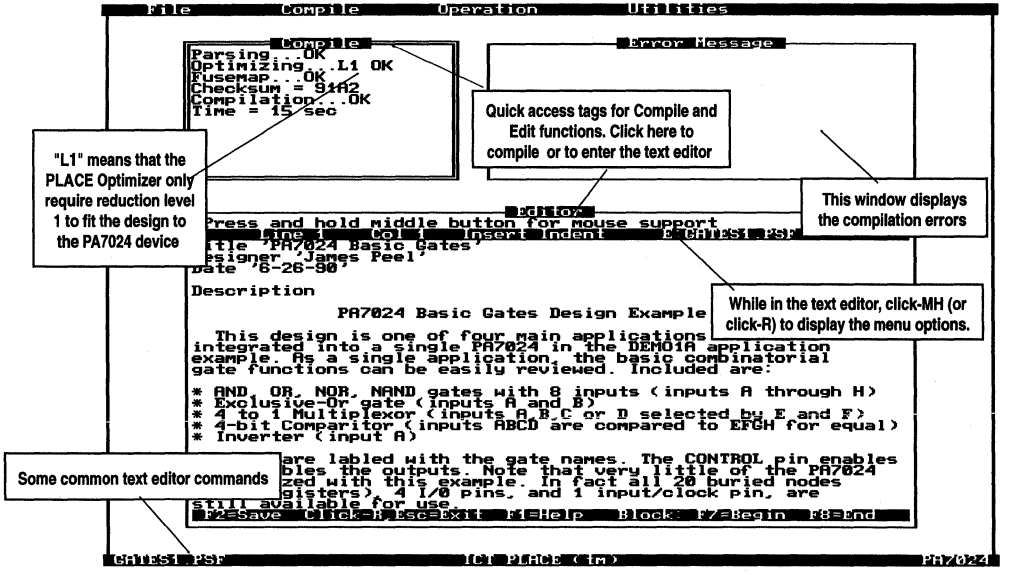

Figure 9-13, The Compile Operation Screen (Standard version only)

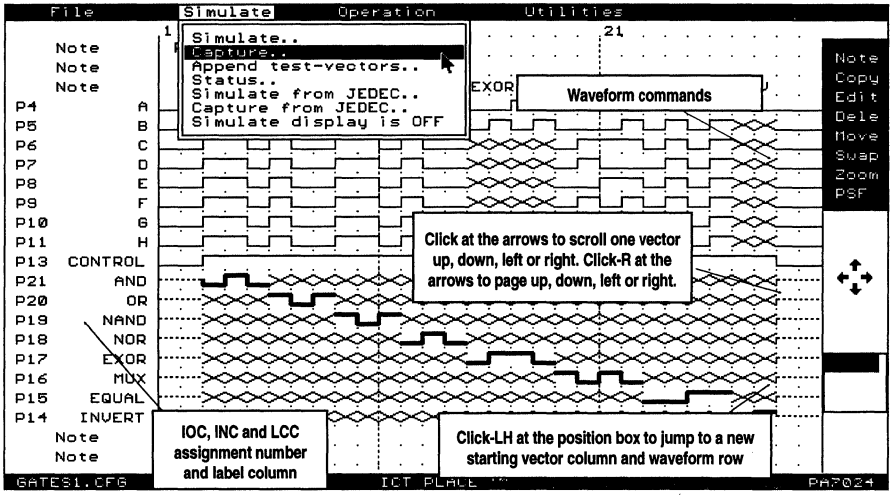

Figure 9-14, The Simulate Operation Main Screen

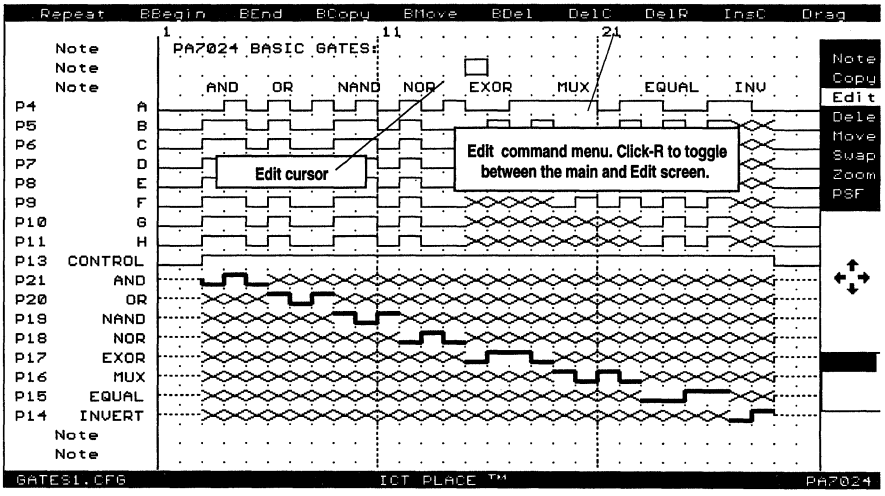

Figure 9-15, The Simulate Operation "Edit" Screen

9.5 The PLACE Design Process

Starting a new design can be accomplished by selecting the "New" command in the "File" menu option while in the Design Operation. This command loads the ANEW file which clears all of the pin and cell (INC, IOC and LCC) names. Note that when a cell is cleared, it will be set to its default configuration. Once this is done a new design can be entered. The following chart lists the typical procedure for implementing a design using PLACE. Please use this as a "road map" for implementing your PLACE designs while referring to the Operation and Language Reference Guides in Chapters 10 and 11 of this manual.

Design

1. Select "New" from the "File" menu option.
2. Enter "Title"

and "Description" from the "Design" menu option.

3. Label all the pins (IOCs and INCs) and LCC (node) names to be used in the design by using the "Label" command.
4. Configure the architectures of the INCs, IOCs and LCCs for the design. Use the "Copy" command to copy or duplicate the INC, IOC or LCC configurations if needed. Use the "Swap" command to move pins, INCs, IOCs and LCCs for desired positioning.
5. For state-diagrams and truth-tables, use the "Allocate" command to allocate the labeled IOCs and/or LCCs for the state machine and truth-table designs.
6. For boolean equation design entry, select the Edit Equation ("Edit Eqn") mode and enter the equations for each LCC input. The equation entry can be done via the pin block or LCC and IOC screen.
7. Edit or modify the architectures and equations until ready to compile. Make sure to save the design through the "File" menu option or by pressing ^S (Ctrl-S).
8. If desired, use the "Swap" command again to reposition the pin and cell locations.
9. Pull down the "Operation" menu and select the Compile operation.

Through out the design process, it is a good practice to periodically save your design. You can do this with the "Save" function in the "File" pop-down menu or hold the [Ctrl] key down and press "S" (^S).

Compile

1. If coming directly from the Design operation (i.e., with the design file loaded), select the "Compile" command menu and click the "Run" command. If the design file was not loaded prior to entering the Compile operation, then "Read" the appropriate source (.PSF) file from the "File" menu window.
2. If a compile error occurs, the compiler will indicate the error with a message and locate the error in the displayed source file. You may ana-

lyze the error and correct it with-in the compile operation (by clicking the "Editor" title bar to enter the editor). You may also return to the Design operation to correct the error. If the compilation is ok, proceed to the Simulate operation.

Simulate

1. Enter the input pin waveforms using the "Edit" command.
2. Enter expected output wavforms for test verification or use the "Capture" command in the "Simulate" menu window to automatically generate the output waveforms.
3. After simulation, click at the "Status" command to check if there are any simulation failures. Correct all simulation failures either by changing the vectors, or by returning to the Design operation and modifying the design.
4. Once properly simulated, append the vectors to the JEDEC file using the "Append test vectors" command from the "Simulate" menu window.
5. Save the ".CFG" simulation file using the "File" menu window. Like the design operation, periodically save your simulation (.CFG) files by pressing "^S". It is recommended to save your first simulation vector file with the ".CFG" file extension. Any vector file can be saved with the extension ".CFx", where x is an alphanumeric character.

Document

1. In the Document operation, select the printer type and interface if you are running the PLACE Document operation for the first-time.
2. Select the Batch or Single option.
3. Click in all the desired print options, such as pin block diagram, PLCC package pinout, cell architectures, simulated waveforms and design texts (such as equations, state-diagrams or truth-tables).
4. Once the options are selected, click the "Print" command to send the documents to the printer.
4. Save your selections onto your hard disk. The filename will consists of the root filename with extension ".PRT".

Program

If using a PDS series programmer (PDS-1, PDS-2, PDS-3) refer to your PDS user's manual for the "program" operation. The "PC Com" (Serial Communication Port Window) Interface window is automatically displayed if the PDS Series Programmers are installed in your computer. The commands in the window allow the JEDEC file to be transmitted or received via the com port to or from a third-party programmer which has a serial communication file transfer utility.

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Operation Reference Guide

10.0 Operation Reference Guide

In this section, the features in the PLACE software are discussed in more detail. Sections 10.1 to 10.3 detail the features or functions that are similar in all PLACE operations. Features specific to each operation are discussed in the following sections.

10.1 File Menu

The "File" menu option shown in Figure 10-1 provides options for file maintenance, system information and screen dump to IBM/Epson printer (additional printer support in Document operation) via the parallel port. This file menu is similar in all operations (i.e. Design, Compile, Simulate, Document and Program operations) with the exception of the type of file (see Table 10-1 for PLACE file types) that is read or saved.

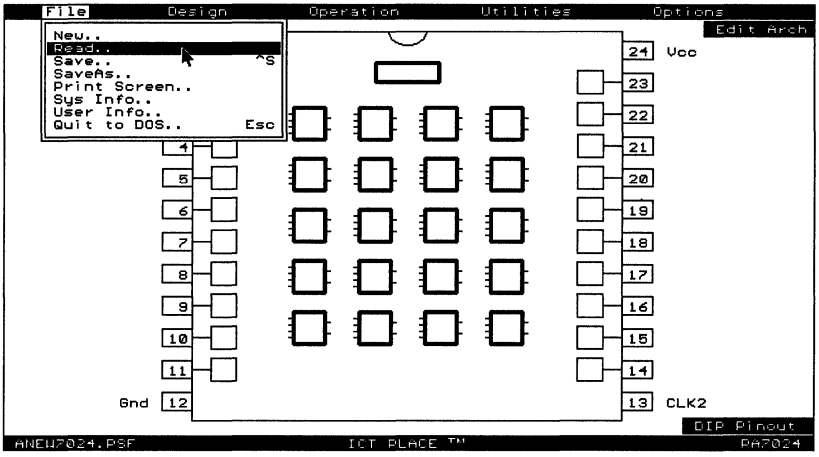

Figure 10-1, File Menu Option

New ..... When in Design operation "New" clears the file in memory and allows device selection for starting a new design. Loads "ANEWxxxx.PSF" (xxxx = device number) as a template file. The PLACE software automatically prevents your edited ANEW file from overwriting the original file by prompting for a new file name during the "Save" command.

Read ..... Allows a PSF source, simulation, documentation or JEDEC file to be loaded from the current directory in the current operation (e.g. loads PSF file in Design operation, CFG in Simulate operation, and etc. - refer to the Table 10-1).

When selected, the File selection window will appear (Figure 10-2):

- A file can be read by clicking the desired file name and clicking the [OK] selector. For quick selection, you can do a "double click", i.e. click twice on the same file name (first click highlights the file, and the second click selects the file).
- New drive is selected by clicking the drive letter at the top of the directory window.
- New directory is selected by clicking the directory name preceded by a "/", or clicking the "/.." (next higher directory) or "/." (root directory). The selection action is similar to selecting a file, i.e., click the [OK] selector or "double click" the selection.
- New file mask can be changed by clicking the file mask highlighted area and typing in the file mask. Use the [Backspace] key, cursor keys or the mouse to move the text cursor. Press the [ENTER] key or click the mouse when completed. Default is "*.PS*". After the file is read, the name will appear in the lower left corner of the pin block screen.

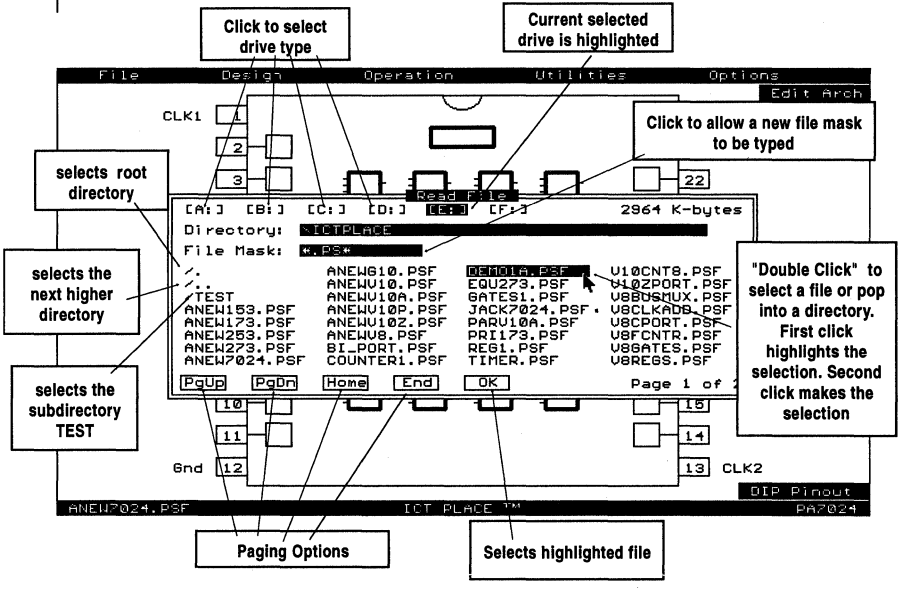

Figure 10-2, "Read" file selection screen

Save..... Saves the current file to disk. If the file is a new design (i.e. an ANEW file), then a new file name will be prompted for.

SaveAs ..... Allows a new file to be saved to the current directory and disk. Click an existing file to over-write or click [New] selector to enter a new file name (the "SaveAs" file selection screen is similar to that of the "Read" screen in Figure 10-2 with the exception of the [New] function).
Note that in the Simulate operation if the root name of the CFG simulation file is not changed, then the file will still reference the same PSF design file. An example is shown below.
DEMO1A.CFG saved as DEMO1A.CF1 - both files reference the DEMO1A.PSF design during simulation.
DEMO1A.CFG saved as DEMO1B.CFG - these files reference DEMO1A.PSF and DEMO1B.PSF design respectively during simulation.

Print Screen .... Sends current screen to the IBM or Epson graphic printer. For more printer support such as HP Laserjet and Postscript printers, please refer to the Document operation.

Sys Info..... Displays system information such as file name, current directory, memory usage and etc.

User Info..... Displays information about the user, such as company name and address, user's name and date of installation.

Quit to DOS .... Quits PLACE program to DOS.

File Extension	Function
PSF	PLACE Source File (PSF) is the design source file used by the Design and Compile operations.
PS	Back-up file for the PSF design file.
MAP	Output file from the PLACE Compiler. This file provides detailed information of how the design equations are mapped into the JEDEC file. This information may be useful for design debugging.
RED	Output file from the PLACE Optimizer (prior to fuse mapping) in the Compile operation. This file contains the reduced or optimized equations in the sum-of-product form. It maintains the PLACE design format so that it can read into the Design operation for design verification and debug, or into the Documant operation for documentation purposes. Note that the unused equations are omitted, so you will get "Equations not found" errors in the Design operation.
JED	Output JEDEC file from the PLACE Compiler and is used by the Simulate and Program operations.
JE	Back-up for the JED file.

Table 10-1, PLACE File Types

INT	Output file from the PLACE Compiler. This file contains the IOC and LCC interconnects which are used for the waveform display in the Simulate operation.
CFG	Primary vector source file for the Simulate operation. This file contains the data for vector simulation and waveform display. The PLACE Simulator simulates the vector in the CFG file with reference to the PSF design file with the same root file name. Hence, other file extensions may be used for the vector source file instead of CFG. However, we recommend using the CFG extension for your primary source file because all PLACE operations automatically reference to the CFG file during the operation switching process.
CF(n)	(Recommended) Alternate vector source file for the Simulate operation. The character "n" can be any alphanumeric character except of course "G". This file extension method is used for the convenience of displaying all the vector files in the directory pop-up window, i.e. with the file mask *.CF*. Remember that the vector source files with the same root file name reference the same PSF design file. Example, the DEMO1A.CFG and DEMO1A.CF1 are vector files for the DEMO1A.PSF design file.
PRT	Input file for the Document operation. This file contains print selection tags for documenting the design.
PR	Back-up for the PRT file.
PN1	Default file extension for the output file from the PLACE Document operation (any file extension can be used with the exception of those that are specified in this table). The Document operation has a "Print to file" option which directs the screen capture data to this file. This file can then be sent to the printer using the DOS Copy command.

Table 10-1, PLACE File Types (Continued)

10.2 Operation Menu

When an operation is selected from the "Operation" menu (Figure 10-3), the PLACE software automatically loads the proper input file for the selected operation. For instance, the PSF file is loaded for the Design and Compile operations, the CFG file for the Simulate operation, the PRT file for the Document operation, and JED (JEDEC) file for the Program operation.

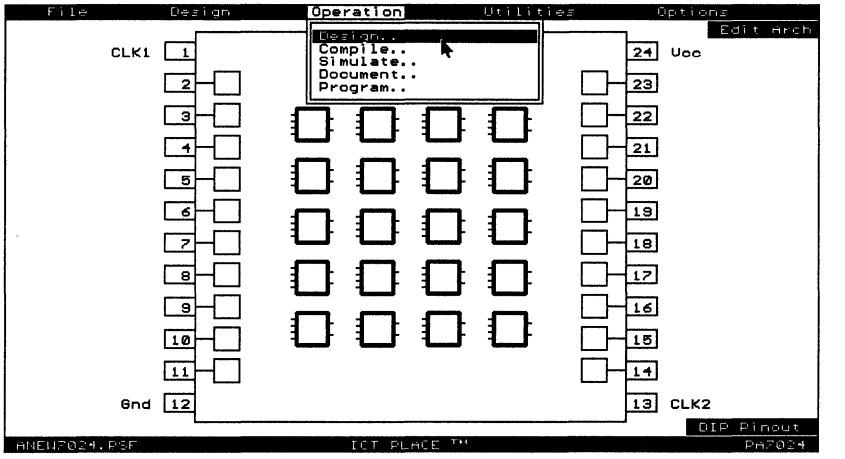

Figure 10-3, Operation Menu Option

Design..... Selects Design operation for creating a PSF design source file. The PSF file (if exists) will automatically be loaded.

Compile..... Selects Compile operation for compiling the PSF design source file to create a JED (JEDEC) file for simulation and programming use. The PSF file (if it exists) will automatically be loaded upon entering the Compile operation.

Simulate ..... Selects Simulate operation for creating a CFG vector source file which can be edited and simulated to the JED file. The CFG file (if it exists) will automatically be loaded.

Document..... Selects Document operation for documenting the design via printing the graphic screens and text files. If it exists, the PRT file will automatically be loaded. If the PRT file does not exist, then the print selection tags will be set to the default settings.

Program ..... Selects Program operation for programming a PEEL Array or PEEL Device with the JED (JEDEC) file. The JED file (if it exists) will automatically be loaded.

10.3 Utilities Menu

Help ..... Provides general information on the Help instruction. For individual Help per command, move the mouse to the command in the menu window and press the [F1] key. See Figure 10-4 for additional Help locations.

File Editor ..... Enter the file or text editor. To exit the editor press the [Esc] key or click-R if using a 3-button mouse. Refer to the "PLACE Text Editor" section in this chapter for more information on the editor commands.

DOS Shell ..... Enters a DOS shell. This feature temporarily exits the PLACE software. Type "EXIT" in the DOS shell to return to the PLACE software. Upon returning from the DOS shell, the previous set-up conditions will be restored. This means that the previous settings and the edited file is saved to disk and will be loaded automatically into the PLACE software. If EMS is available, it will be used to save the settings and file.

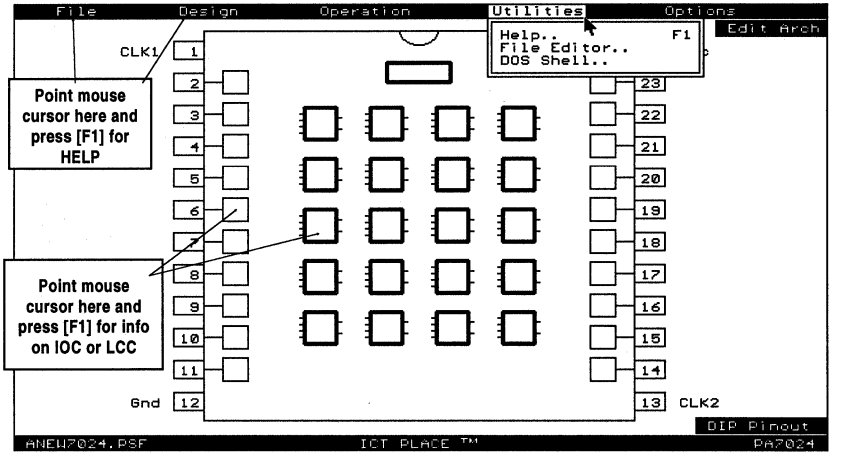

Figure 10-4, Utilities Menu Option

10.4 Design Operation - Design Menu

The "Design" menu contains commands used for implementing PEEL Array and PEEL Device designs. Note that some design commands such as "LCC Re-assign" and "Global => 2" commands are only applicable to the PEEL Array designs. The two cursor types used by some of the commands in the "Design" menu are the "Left Arrow" and "Hand" cursors.

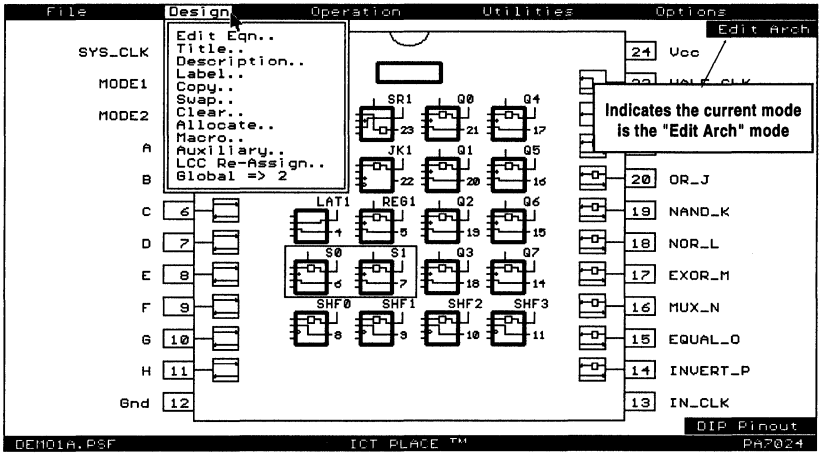

Figure 10-5, Design Menu Option

In the PLACE software, all commands that are not applicable to the selected device will be disabled.

Edit Eqn ..... Selects Edit Eqn mode (also selected by clicking-R in the Edit Arch mode). This mode is identified by the left arrow mouse cursor (<-) if a 3-button mouse is used. In the "Edit Eqn" mode (also refer as "Select Sum Equation" mode), there are three ways of entering a logic description.

1. **Equation:** Move the cursor to highlight the OR (Sum) gate, and click to bring the sum equation out. Note that the equations for each cell are created by the label command. Hence, all cells must be labeled prior to selecting their OR gates.
2. **State diagram:** Move the cursor into the state diagram box without highlighting any of the OR gates in the LCC selected for the state diagram design. Then, click to open the window with the state diagram syntax. The requirement for designing with the state diagram syntax is that the cells (LCCs and IOCs) must be allocated by using the "Allocate" command.

3. **Truth table:** Click at the T(n) labels located at the bottom of the LCC or IOC to open the window for displaying the truth table design syntax. Like the state diagram design, cells used in the truth table design must first be allocated.

After opening the window to display the design syntax (this window will be referred to as **PSF Display window**), move the cursor into the window and click to open the text editor for entering and editing the design syntax. Press the [Esc] key or click-R to exit editor. Refer to section 10.29 for the text editor commands.

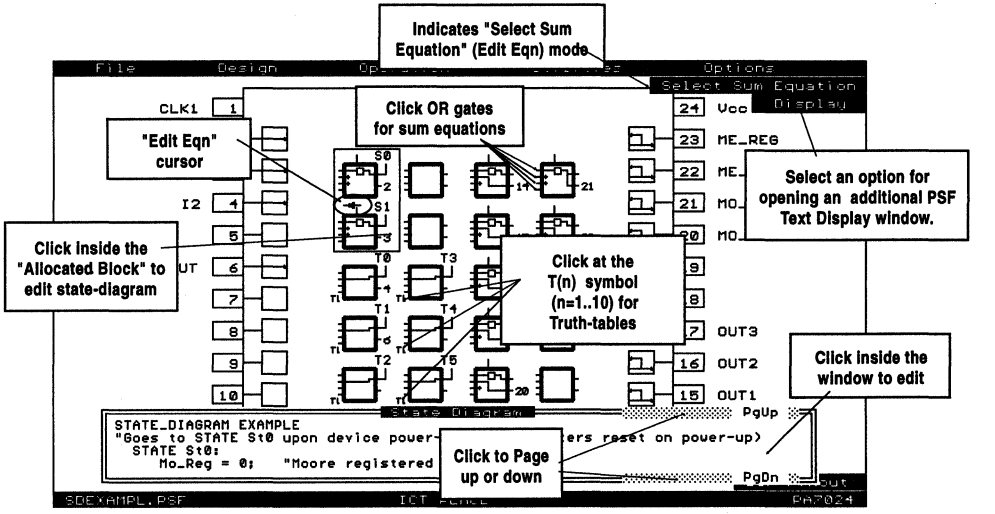

Figure 10-6, Edit Equation Mode

Title ..... Allows a title, designer's name and date to be entered into the source file.

Description ..... Opens a window to display the design description. The window size can be adjusted by pressing the Up or Down cursor keys followed by the ENTER key, or using the "**Display**" menu (see section 10-6). Paging can be accomplished by clicking at the PgUp or PgDn markers, or using the PgUp or PgDn keys. To enter the PLACE text editor for editing, click inside the displayed window. There is no limitation in terms of the type of characters you can use for describing your design, just as long as your description is specified within the reserved words "DESCRIPTION" and "END_DESC". Note you can use the reserved word "DESCRIPTION" but not the word "END_DESC".

Label ..... Enters the "Label" mode so that any LCC, IOC, INC or pin can be labeled. After a LCC or IOC is labeled, the equations related to the labeled cell are automatically generated in the source file (all equations equate to 0) . The number and type (sum or product equations) of equations generated depends on the device type and the configuration of the cell (Table 10-2). **In PEEL Arrays, note that the equations are generated only if both the LCC and its associated IOC are previously unused or unlabeled.**

If the label for the LCC or IOC is deleted and its associated cell (IOC or LCC) is unused, then all the equations are automatically deleted.

Below is an example of the four equations generated for a labeled PA7024 LCC (assume the label is "!TEST").

Example:

Configuration	Equations generated
D-type flip-flop	!TEST.D = 0;
Async. Preset	!TEST.AP = 0;
Async. Reset	!TEST.AR = 0;
Assigned IOC is an I/O type	!TEST.OE = 0;

Assume that the flip-flop's output of the LCC is connected to the IOC.

PEEL Device	Number of equations per IOC
18CV8,	1 sum equation, 1 product equation
22CV10A/A+,	

PEEL Array	Number of equations per LCC/IOC pair
PA7024, PA7140	4 sum equations
PA7128	

Table 10-2, Number of Equations per IOC or LCC/IOC pair

Labelling Methods

Below are the three methods of labelling cells and pins.

1) **Click and Type method:**
This is the normal method of labelling the cells or pins. Move the mouse cursor and click the mouse button to select the cell or pin. Type in the label and press the ENTER key or right button of the mouse to complete the label procedure. Repeat this procedure for all cells and pins.

2) **Group (Set) method:**
The group or set method is designed for labelling a group of cells or pins with names that differ by a single alphabet character or a set of numbers. Some examples of the group names are: ModeA, ModeB, ModeC; AD0, AD1, .., AD15; and A0, A1, .., A12.

The first step in implementing this method is to click at a cell (IOC, INC, LCC or pin) which will be the starting cell, i.e. the first label in the group will be assigned to this cell. If the starting cell is an IOC, INC or pin, then the labels will be assigned to the next cell or pin **in ascending order**. For PEEL Arrays, if the starting cell is a LCC, then the labels will be assigned to the subsequent LCCs in ascending order (i.e. 1A, 2A, .., 1B, 2B, ..,5D). After the starting cell has been selected, type the *group name* in the label window.

Format of the group name is:

prefix name + [A..Z] + suffix name
+ [Z..A] +
+ [1..n] +
+ [n..1] + (where n > 1)

Some examples are:

Group Name	Assigned Labels
Q[0..3]	Q0, Q1, Q2, Q3
ADDR[9..13]	ADDR9, ADDR10, ADDR11, ADDR12, ADDR13
D[99..102]_IN	D99_IN, D100_IN, D101_IN, D102_IN
OUT[1000..998]	OUT1000, OUT999, OUT998
IN[51..49]DATA	IN51DATA, IN50DATA, IN49DATA, IN48DATA
[A..C]10	A10, B10, C10
![Z..X]1	!Z1, !Y1, !X1

3) **Keyboard method:**
Like the Group method, the keyboard method also allows labels to be assigned quickly. However, this method is more suitable for assigning labels which are significantly different from each other, i.e. they differ by more than two alphabet characters. Some of the label examples are INPUT, OUTPUT, ADDRAA, ADDRBB, OE, READ, !WRITE and etc. Normally to assign these labels you would need to implement the "Click and Type" method. But, performing this click and type task repeatedly for

twenty cells is a very tedious job. The "Keyboard" method shortcuts this task by bypassing the mouse click procedure.

In this method, you should first click on a cell (or pin) which you want the label to start from (defaults to the first pin if no pin or cell is selected). After typing in the label, press the [ENTER] key to implement the assignment (like in the "Click and Type" method). If the [ENTER] key is pressed the second time, the hand mouse cursor automatically advances to the next cell **in ascending order**. You can now type in the label for the current selected cell, and then press the [ENTER] key twice to advance to the next cell. Repeat the procedure until all the cells are labeled. **Please note that if you move your mouse cursor at any time during this mode, the "Keyboard" labelling will be aborted.**

Note that all three methods of labelling cells and pins can be used in conjunction with each other. The "Click and Type" method can be used to select a new starting cell for the "Group" and "Keyboard" methods.

Renaming labels

The Label function can also be used for renaming the pins, IOCs, INCs or LCCs. During the renaming process, the previous labels used in the IOC, INC and LCC configuration, DEFINE, STATE_DIAGRAM, TRUTH_TABLE and EQUATIONS sections will automatically be replaced by the new label. This replacement process allows the user to change the pin or cell labels with ease so that the labels that are used throughout the PSF file need not be manually changed. An example of the label replacement is:

	Before Change	**After Change**
Pin Label	TEST	/TEST1
Equations	OUT.COM = A & TEST	OUT.COM = A & TEST1
	OUT.OE = /TEST	OUT.OE = /TEST1

As seen in the previous example, the replacement process only replaces the label. Even though the input signal active level is changed, the logic of the equation remains unchanged. For instance, the OUT output which is controlled by the OUT.OE equation is enabled on a FALSE or OFF condition. With the TEST input the FALSE condition is a HIGH signal. On the other hand, the FALSE condition for the /TEST1 input is a LOW signal.

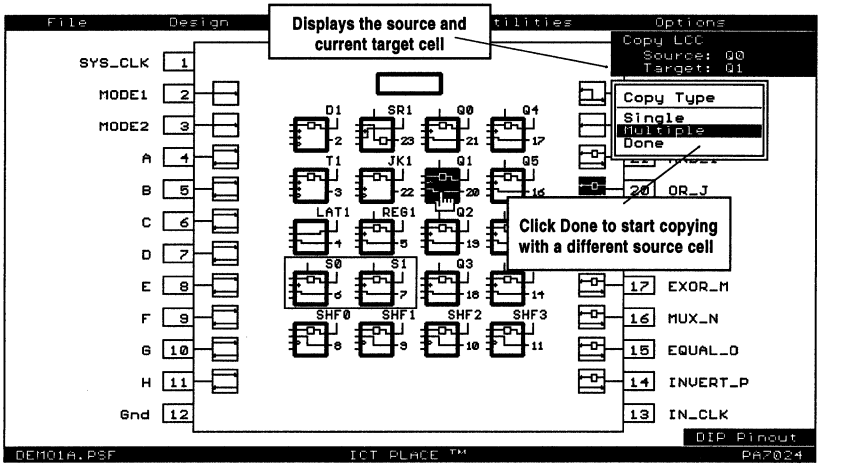

Figure 10-7, Copy Mode

Copy..... Copies the selected LCC's, IOC's or INC's configuration into another cell. This will not copy the equations. Select the "Multiple" option in the Copy Type window for doing multiple copying (Figure 10-7), i.e. copying from one cell into many cells. Select "Done" to complete the current "Multiple" copying set and to start another. The only restriction in the "Copy" mode is that the source and target cells must be of the same type, i.e. LCC to LCC, IOC to IOC and INC to INC.

Swap ..... This mode allows swapping of LCCs, IOCs, INCs or pins to reorganize your design. The functions of the cells do not change. There are two restrictions when swapping the two cells.

1. Both the source and target cells must be of the same type, i.e. LCC with another LCC, IOC with another IOC, and INC with another INC.
2. For PEEL Arrays, the swapping of IOCs or LCCs are not permitted if the two global cell mode is used and if one of the following is true: a) the cells that are being swapped are IOCs which are located on the opposite sides of the pin block diagram; or b) the cells that are being swapped are LCCs which are connected to IOCs that are located on the opposite sides of the pin block diagram.

Clear ..... Clears the LCC, IOC or INC. This sets a default configuration to the cells and re-name the sum output names to the new configuration. After clearing both the LCC and its assigned IOC, then all the sum equations associated with this cell are deleted.

Allocate..... Allocates the LCC or IOC for state-machine or truth table design. Before the cell can be used for allocation, it must first be labeled. This mode also allows a state-machine or truth table design to be created, deleted or modified. For state-machine design, the allocated cells will be surrounded by a border. For truth table design, the allocated cells will be indicated by "In" and "Tn" (inputs and outputs respectively), where n ranges from 1 to 10. Note that only the outputs of the truth table ("Tn") will be marked after exiting the "Allocate" mode. See sections 10.10 and 10.11 for detailed descriptions of the state diagram and truth table designs.

Macro ..... Displays the macro definitions in the PSF design file. Macro definitions are text statements which succeed the keyword "DEFINE" but precede one of the following reserved words: STATE_DIAGRAM; TRUTH_TABLE; or EQUATIONS.

Auxiliary ..... Additional functions such as Security Bit, Signature and Zero-Power options which are found in the Peel Arrays and in some PEEL Devices. Below is a brief description of each function but you should refer to the ICT data book for more information.

Security Bit - Setting this feature ON enables the security bit to be programmed on the device (inserts the "G1" field in the JEDEC file). Once the security bit has been programmed, the design programmed into the device cannot be read back (except for the Signature Word). All PEEL products provide the security bit feature.

Signature Word - The Signature Word of the device allows a user ID to be stored in the device so that it can be read back for design verification even after the security bit has been programmed. Devices with the Signature Word (number of 8-bit bytes in parenthesis) are PA7024 (8 bytes), PA7140 (2 bytes), PA7128 (1 byte), PEEL22CV10A+ (3 bytes).

Example: Signature = ABC [ENTER]
(converts the characters A, B, C to the ASCII values 65, 66 and 67 respectively. Each character requires an 8-bit byte)

LCC Re-Assign.. (PEEL Arrays only) Allows the two internal and external outputs of the LCC to be separated and re-assigned. Below lists the requirements for re-assigning the LCC.

1) The IOCs and LCCs of both source and target cells must be labeled.
2) The internal and external LCC outputs must not be sharing the same sum term, i.e they must be from separate sum terms.
3) All sum terms must be used, i.e. the output equation extensions must not contain the ".SUMx" extension where x = A..D for sums A through D.
4) The source and target LCCs must have the same configurations prior to the re-assignment. Use the "Copy" function to copy the configurations of the LCC (and possibly the IOC too) from the source to the target cell. All LCCs and IOCs can be reconfigured later for your specific application requirements.

Example:

Figure 10-8 illustrates a typical example which requires the LCC re-assignment feature. In this example, a design modification is required to make the output "TESTOUT" synchronous with the clock "CK1". Currently, the output "TESTOUT" is a combinatorial output. This output would need to become a registered output in order to be synchronous with the clock "CK1". The problem is that the register in the LCC associated with this output is already being used for another function. The internal output "IN" for the LCC 3C can be duplicated by copying the configuration of the LCC 3C into an empty LCC and retyping the equations. However, a faster method is to use the "LCC Re-Assign" command which separates the output "IN" from the LCC 3C and re-assigns it to another IOC with an unused LCC (LCC 4C or 5B).

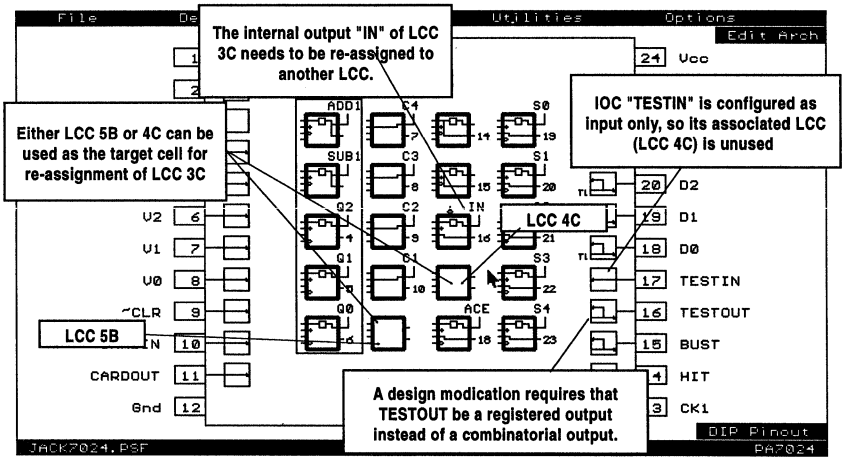

Figure 10-8, A typical example for re-assigning the LCC

The procedure for re-assigning the internal output "IN" in LCC 3C is as follows:

1) Change the configuration of the LCC 3C and IOC "TESTIN" so that all the sum terms are used. In this example, set the IOC "TESTIN" to an I/O type instead of input only.
2) Label the LCC 4C which will be the target cell.
3) Copy the cell configurations, using the LCC 3C "IN" and IOC "TESTIN" as the source cells. The target cells will be the newly labeled LCC 4C and the IOC "TESTOUT".
4) Select the "LCC Re-Assign" command and click the source and target LCC (LCC 3C and 4C respectively).
5) Reconfigure all the cells (both source and target LCCs and IOCs) for their specific application requirements, i.e. IOC "TESTIN" to input only, IOC "TESTOUT" to output only, and etc.

Global ..... Toggles between the one or two global cell mode. If two global cells are used, swapping is not allowed with IOCs that are located on the left and right sides of the device, or with LCCs which are associated with IOCs that are located on the left and right sides of the device. This feature allows the device to be separated into two parts with each part containing its own high speed clock. Please refer to the ICT data book for more information on the benefits of the one and two global cell modes.

10.5 Design Operation - Pin Block Diagram Screen

The default function for the pin block diagram screen is the Edit Architecture mode (Edit Arch). This mode is automatically set when the PLACE software is initially entered. It allows selection of the Logic Control Cells (LCCs), I/O Cells (IOCs), Input Cells (INCs) or Global Cells (GBCs) for controlling cell configurations.

The PA7140 pin block diagram shown in Figure 10-11 illustrates the PLCC pinout configuration. For the PA7140 device, the PLCC pinout is the default configuration. As for devices with availability in both the DIP and PLCC packages, the DIP (default configuration) or PLCC pinout configuration can be set in the "Options" menu. Refer to section 10-13 for more information on the "Options" menu.

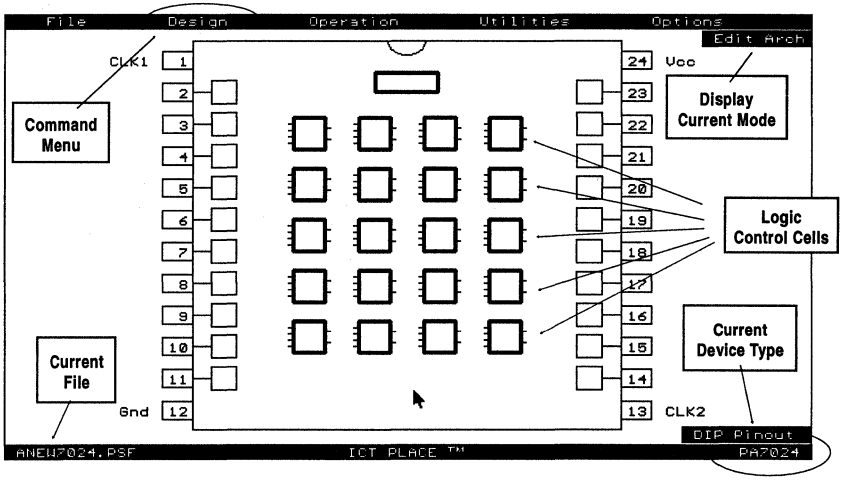

Figure 10-9, Pin Block Diagram of the PA7024

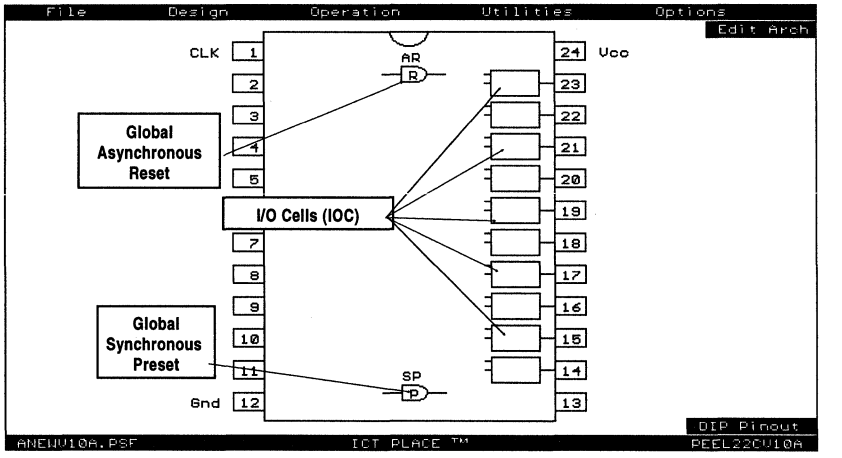

Figure 10-10, Pin Block Diagram of the PEEL22CV10A

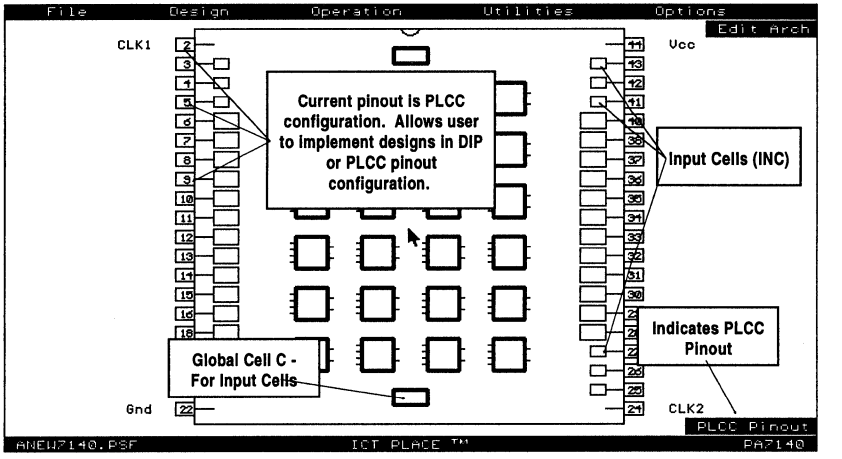

Figure 10-11, Pin Block Diagram of the PA7140

10.6 Design Operation - LCC and IOC Screen

If a Logic Control Cell (LCC) or I/O Cell (IOC) is selected from the pin block diagram screen, the screen zooms into the selected cell for a close-up view of the cell configurations (Figure 10-12). Note that both the LCC and its currently connected IOC are displayed. In this screen, selections can be accomplished by moving the mouse cursor to the "selectors" such as the registers "rectangle", polarity "bubble", OR gates, or the "Smile Face" selectors. Except for the OR gate, all of the above selectors are highlighted when selected and are used for controlling the cell configurations.

Selecting any of the four OR gates will display its associated equation. Move the cursor inside the equation window and click to enter text editor. Click-R to return from editor, to complete the selected mode or function, or to return to the block diagram screen.

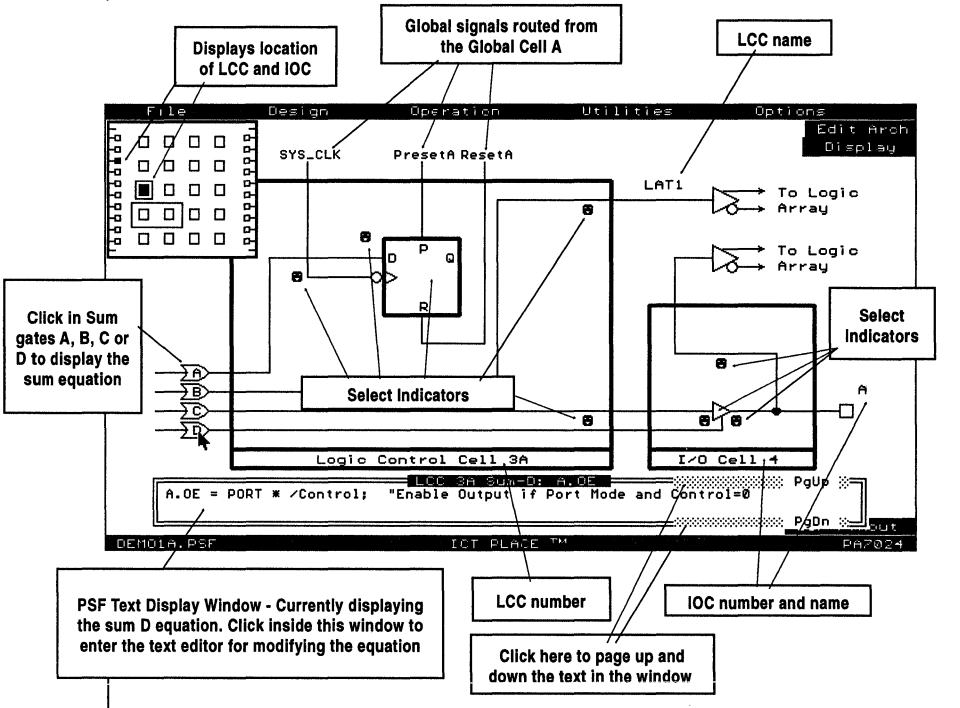

Figure 10-12, LCC and IOC screen of the PA7024

Select Indicators in PEEL Arrays (PA7024, PA7140 and PA7128)

Below are the descriptions of the "select indicators" found in all PEEL Arrays. Unless specified otherwise, all "select indicators" are applicable for all the PEEL Array devices.

Clk (Clock) Select

/Global	Inverted clock signal from the Global Cell A or B. If the two global cell mode is used, then LCCs connected to IOCs on the left and right sides of the pin block diagram are controlled by Global Cells A and B respectively. For one global cell mode, all global signals are routed from Global Cell A.
Global	**Default configuration.** Non-inverted clock signal from the Global Cell A or B.
Sum-C	Clock signal from the Sum-C gate. The Reset signal for the LCC register will automatically be routed from the Global Cell A or B if it was originally connected to the Sum-C gate.
Sum-D	Clock signal from the Sum-D gate. If the IOC connected to the LCC is an I/O type, then the output will be disabled. If the IOC is an output type, then it will remain as an output type with only combinatorial feedback from the pin.

RT (Register Type) Control

Off	**Default configuration.** Sets the dynamic register control to Off. This means that any signal on the RT line (RTA or RTB equation in the PSF file) will not implement a dynamic register change.
On	Sets the dynamic register control to On. A TRUE logic on the RTA or RTB equation (in the PSF file) changes the type of register in the LCC during normal operation. For instance, if RT is "On" and Register Type is "D -> T", then the D-type register will be changed to a T-type register when the logic on the RTA equation is TRUE. For the one global cell mode, the RTA equation controls the RT signals in all LCCs. For the two global cell mode, the RTA and RTB equations control the RT signals of the LCCs which are connected to IOCs on the left and right sides of the pin block diagram respectively.

Register Type

If RT is Off:

D	**Default configuration.** D-type register. Reset and preset of the register can be locally (through the sum B or C gate) or globally (ResetA or PresetA equation) controlled.
T	T-type register. Reset and preset of the register can be locally (through the sum B or C gate) or globally (ResetA or PresetA equation) controlled.
JK	JK register. Sum-A for the J-input, and Sum-B for the K-input. Reset can be controlled locally or globally, but the preset will automatically be set to global preset.

IF RT is On:

D -> T	**Default configuration.** D-type register when the RT signal is FALSE, and T-type register when it is TRUE. Reset and preset can be locally or globally controlled.
D -> JK	D-type register when the RT signal is FALSE, and JK-type register when it is TRUE. For the JK-type register, Sum-A is used for the J-input, and Sum-B for the K-input. Reset can be controlled locally or globally, but the preset will automatically be set to global preset.
T -> D	T-type register when the RT signal is FALSE, and D-type register when it is TRUE. Reset and preset can be locally or globally controlled.
JK -> D	JK-type register when the RT signal is FALSE, and D-type register when it is TRUE. For the JK-type register, Sum-A is used for the J-input, and Sum-B for the K-input. Reset can be controlled locally or globally, but the preset will automatically be set to global preset.

Note that the Sum-B gate cannot be used for both K-input and preset for the register.

Preset and Reset for the LCC Register

The output of the LCC register is set to a HIGH signal when the preset signal is TRUE. On the other hand, the output of the register goes LOW if the reset signal is TRUE. **If both the preset and reset signals are TRUE, then the preset signal takes precedence over the reset signal.**

There is no dedicated MUX for controlling the preset or reset of the LCC register. Both of these signals are indirectly controlled by the "Clk Select", "Register Type", "Buried Output" and "Ext Output" selections. **The same Sum (OR) gate allocated for any of the above configurations cannot be used for presetting or resetting the LCC register.** So, the PLACE software automatically switches the preset or reset to the global signal when the local sum gate is used.

Buried Output (Internal Output of the LCC)

Reg-Q	**Default configuration** Connects the output of the LCC register to the internal or buried output of the LCC.
Sum-A	Connects the Sum-A gate to the internal or buried output of the LCC.
Sum-B	Connects the Sum-B gate to the internal or buried output of the LCC. If the preset of the register is locally controlled (through Sum-B), it will automatically be set to global preset.
Sum-C	Connects the Sum-C gate to the internal or buried output of the LCC. If the reset of the register is locally controlled (through Sum-C), it will automatically be set to global preset.

Ext Output (External Output of the LCC to the IOC)

Reg-Q	**Default configuration.** Connects the output of the LCC register to the external output of the LCC.
Sum-A	Connects the Sum-A gate to the external output of the LCC.

Sum-B Connects the Sum-B gate to the external output of the LCC. If the preset of the register is locally controlled (through Sum-B), it will automatically be set to global preset.

Sum-C Connects the Sum-C gate to the external output of the LCC. If the reset of the register is locally controlled (through Sum-C), it will automatically be set to global preset.

OE (Output Enable) Select

I/O **Default configuration.** Sets the IOC to I/O type. Sum-D is used for the output enable control. If the LCC Clk Select is set to Sum-D, the IOC changes from the I/O to input type automatically.

Input Sets the IOC to input type. If Sum-D is not used for the LCC clock, then it will be disabled.

Output Sets the IOC to output type. If Sum-D is used for the LCC clock, then the Feedback Type will automatically be set to combinational.

Feedback Type

In the normal configuration, whether the IOC is an I/O, input or output type, this multiplexer controls the path from the pin. However, in the PA7140 and PA7128 devices, the option "FB Mux" allows the path to come from the Sum-D gate.

Com **Default configuration.** Combinatorial path from the pin or Sum-D.

Reg Registered path from the pin or Sum-D. The clock for the register can be directly from the CLK1 or CLK2 pin, or PCLK product term.

Lat Latched path from the pin or Sum-D. The latch trigger can be directly from the CLK1 or CLK2 pin, or PCLK product term.

Out (Output) Polarity

Invert Inverts the output to the pin for active Low output.

Non-invert **Default configuration.** Non-inverted output for active High output.

FB Mux (PA7140 and PA7128 only)

Pin **Default configuration.** Sets the feedback path to come from the pin.

Sum-D Sets the feedback path to come from the Sum-D gate. With this configuration, the IOC automatically becomes an output pin with no feedback from the pin. This means that the Sum-D signal will be buried. See Figure 10-13.

Select Indicators in the PEEL Devices

Output Select	
Com	**Default configuration.** Sets the IOC to combinatorial output. In the 22CV10A devices, the feedback path is automatically set to come from the pin with this configuration. For other devices such as PEEL18CV8, the feedback path is controlled by the "Feedback Type" MUX.
Reg	Sets the IOC to registered output. In the and 22CV10A devices, the feedback path is automatically set to come from the $\overline{Q}$ of the register with this configuration. The register is triggered on the rising-edge of the clock.

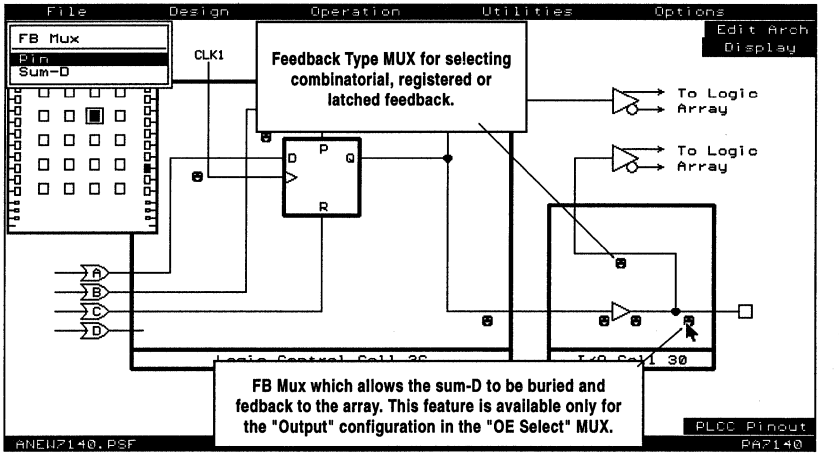

Figure 10-13, LCC and IOC screen of the PA7140

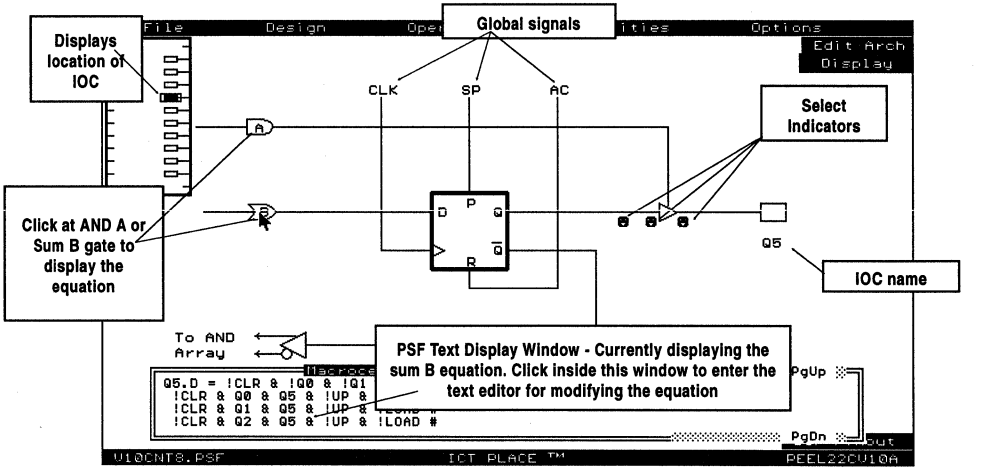

Figure 10-14, IOC screen of the PEEL22CV10A

OE (Output Enable) Select

I/O	**Default configuration.** Sets the IOC to I/O type. Depending on the device, a sum or product term controls the output enable term.
Output Enabled	Enables the output in the IOC.
Output Disabled	Disables the output in the IOC.

Out (Output) Polarity

Invert	**Default configuration.** Inverts the output to get an active Low output.
Non-invert	Buffers the active High output.

Feedback Select (18CV8, 20CG10A, and 22CV10A+)

Pin	Feedback path from the pin.
Reg	Feedback path from the Q (PEEL18CV8 only) or $\overline{Q}$ (all other devices) of the register.
Or	Feedback from the OR gate, i.e. prior to the register and output buffer.

Global Asynchronous Reset and Synchronous Preset in PEEL Devices

In all registered PEEL devices, the IOC (or macro cell) register can be reset or preset using an internal reset or preset product term. The PLACE software automatically assigns node numbers for both product terms.

When the reset product term is TRUE, the output of the register in the IOC (or Macrocell) is set to a LOW signal asynchronously. **For 20-pin devices, the asynchronous reset node number is 21, and for 24-pin devices the node number is 25.**

When the preset product term is TRUE, the output of the register in the IOC changes to a HIGH signal (synchronously) with the rising-edge of the clock signal. **The node number for the preset product term is 22 and 26 for the 20 and 24-pin devices respectively.**

When both the reset and preset signals are TRUE, then the reset signal takes precedence over the preset signal.

10.7 Design Operation - Input Cell (INC) for PA7140 and PA7128

In addition to the IOCs and LCCs, the PA7140 and PA7128 have Input Cells (INCs). Each INC allows the input to be configured as combinational, registered or latched input (Figure 10-15).

Input Type

Com	**Default configuration.** Sets the input to be combinational.
Reg	Sets the input to be registered. The clock for the register is controlled by the Global Cell C.
Lat	Sets the input to be latched. The trigger for the latch is controlled by the Global Cell C.

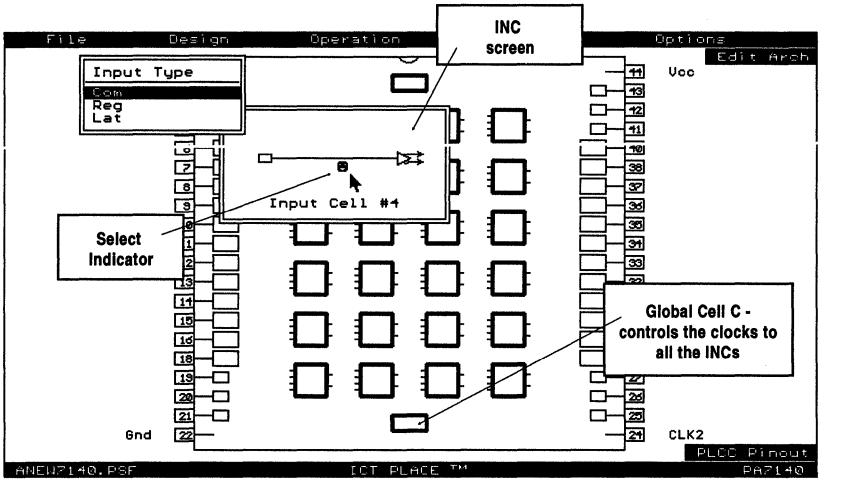

Figure 10-15, INC screen of the PA7140

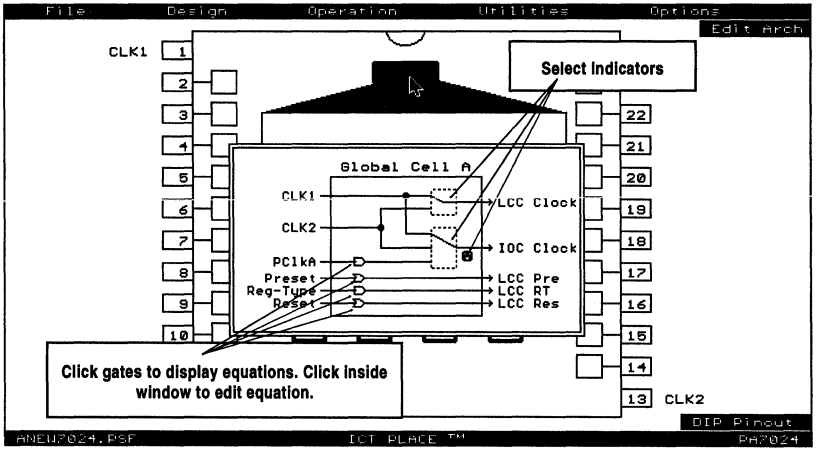

Figure 10-16, Global Cell A screen of the PA7024

10.8 Design Operation - Global Cell (GBC) for PEEL Arrays

Global Cells A and B

In PEEL Arrays, the Global Cells (GBCs) A and B which are located at the top of the pin block diagram are used to control the global signals for the LCC and IOC. These global signals include the clock for the LCC and IOC, and preset, reset and register type control for the LCC.

After clicking the GBC to bring the Global Cell window up for selection, click at the MUX "rectangle" to set the desired clock selection for the LCCs and IOCs. The IOC clock polarity is controlled by the "Clock Polarity" select indicator. Click at the AND or OR (Sum) gates to display the global equations for register-type, PCLK, global reset or preset. Move the cursor inside the equation window and click the mouse to enter the text editor. In the text editor, press the [Esc] key or click-R to return to the global cell window. The same procedure can be used in the one or two global cell mode.

In the one global cell mode, the Global Cell A controls the global signals to all the LCCs and IOCs in the device (Global Cell B is ignored). In the two global cell mode, Global Cell A controls the global signals to the LCCs and its associated IOCs that are located on the left side of the pin block diagram. Global Cell B controls the global signals to the remaining LCCs and IOCs which are located on the right side of the pin block diagram.

Global Signals

LCC Clock	This signal clocks the register in the LCCs. The signal comes from one of the two dedicated clock pins, CLK1 or CLK2.
IOC Clock	This signal clocks the register in the IOCs. In addition to the two dedicated clock pins CLK1 and CLK2, the signal can come from a product term PCLKA (GBC A) or PCLKB (GBC B). The select indicator "Clock Polarity" allows the IOC clock polarity to be changed. The default configuration is "Pos" which means that the IOC register or latch is triggered on the rising-edge or HIGH signal. If the configuration is set to "Neg", then the register or latch is triggered on the falling-edge or LOW signal.
LCC Pre	This sum (OR) term is the global preset for the LCC register. The LCC register is preset to a HIGH signal when this sum term is TRUE. **This term takes precedence over the reset term for the LCC register.**
LCC RT	This product term is the global register-type change for the LCC. Each LCC has the option ("RT Control") of enabling the dynamic register-type change when this term is TRUE.
LCC Res	This sum (OR) term is the global reset for the LCC register. The LCC register is reset to a LOW signal when this sum term is TRUE.
LCC PLD	This sum (OR) term is the global preload for the LCC register. The LCC registers controlled by this global cell are loaded from the associated IOC pin when this sum term is true and the registers is clocked.

LCC ULD This sum (OR) term is the global unload for the LCC register. The content of the LCC registers controlled by the global cell will be unloaded to the IOC pin when true.

Global Cell C (PA7140 and PA7128 only)

In addition to Global Cells A and B, the PA7140 and PA7128 have Global Cell C. This cell which is located at the bottom of the pin block diagram controls the global clock signal for the Input Cells (INCs).

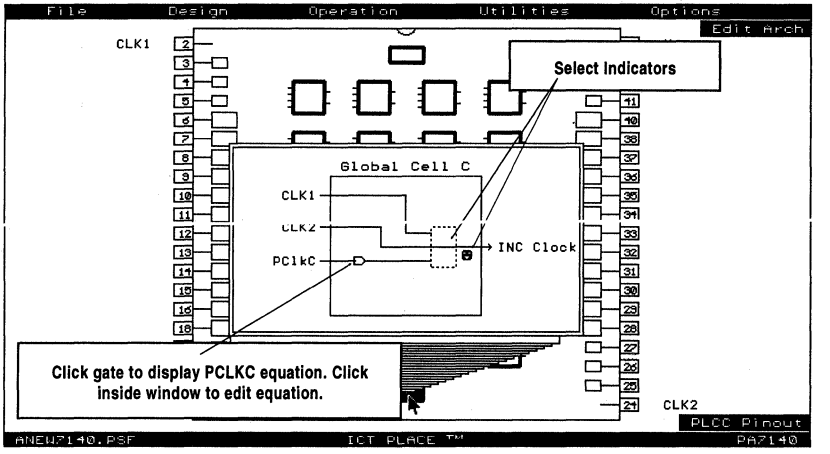

Figure 10-17, Global Cell C screen of the PA7140

10.9 Design Operation - Entering Equations

One of the primary methods of entering the design equations is via the "Edit Eqn" mode which was discussed in section 10.4. Figures 10-18 and 10-19 shows the "Edit Eqn" mode for the PA7024 and PEEL22CV10A devices respectively.In addition to the "Edit Eqn" mode, equations can also be edited via the LCC and IOC screen (or just IOC screen for the PEEL devices). Refer to Figures 10-20 and 10-21.

For editing equations for the global signals in the PEEL Arrays, please refer to section 10.8 on "Global Cells for PEEL Arrays".

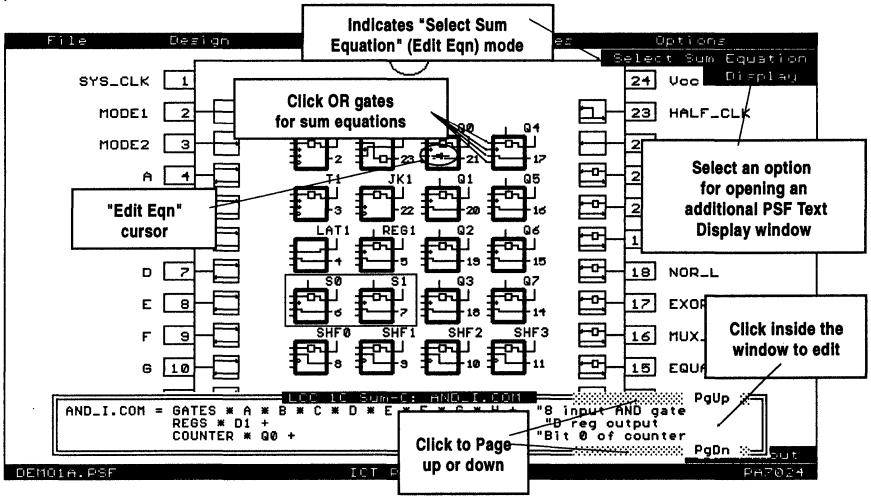

Figure 10-18, "Edit Eqn" mode of the PA7024

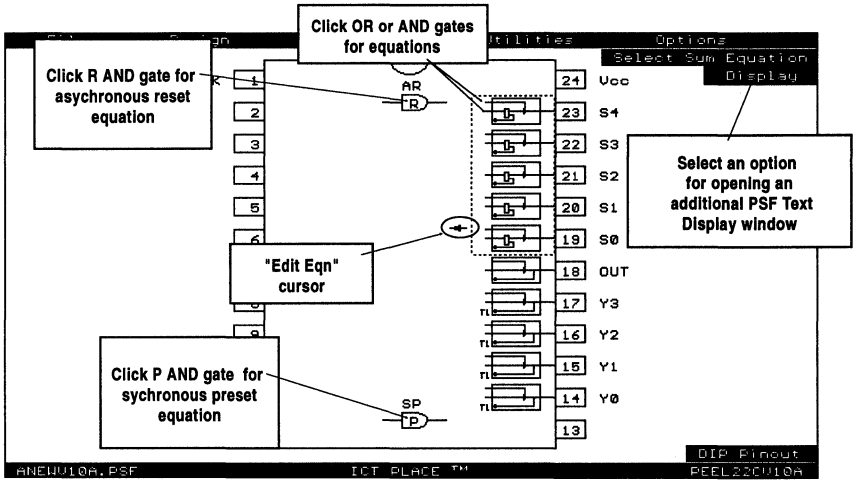

Figure 10-19, "Edit Eqn" mode of the PEEL22CV10A

After the cell (LCC or IOC) is labeled using the "Label" command in the "Design" menu window, the PLACE software automatically generates the equations. To edit or modify these equations, first, click at the desired OR (sum) or AND (product) gate to bring the equations out in PSF Text Display window (section 10.12). Then, click inside the window to enter the text editor. When you are done editing the equations, press the [Esc] key or click-R to return to the previous screen. Whether the device is a PA7024, PEEL22CV10A or any other device, the procedure for entering the design equations remains the same.

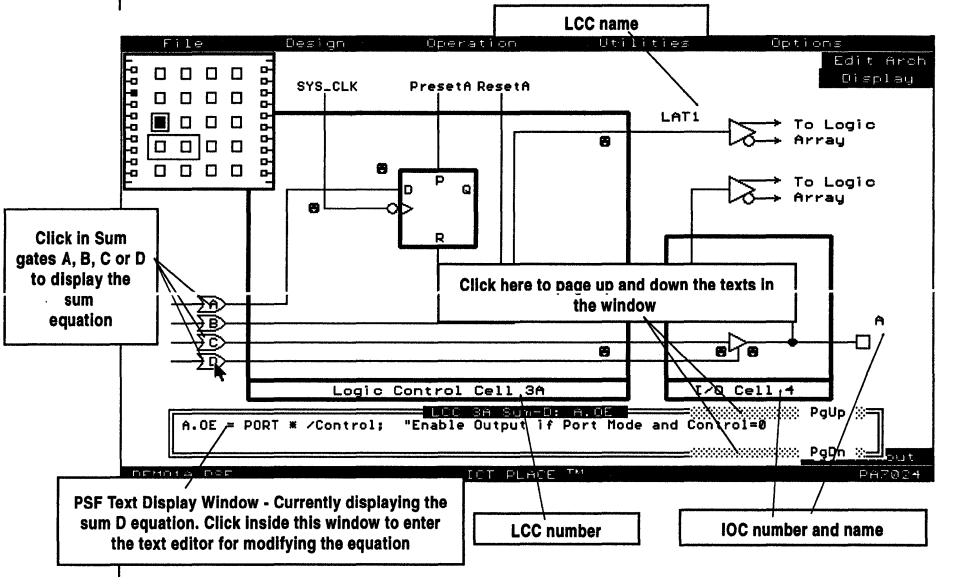

Figure 10-20, Editing equations in the LCC and IOC screen of the PA7024

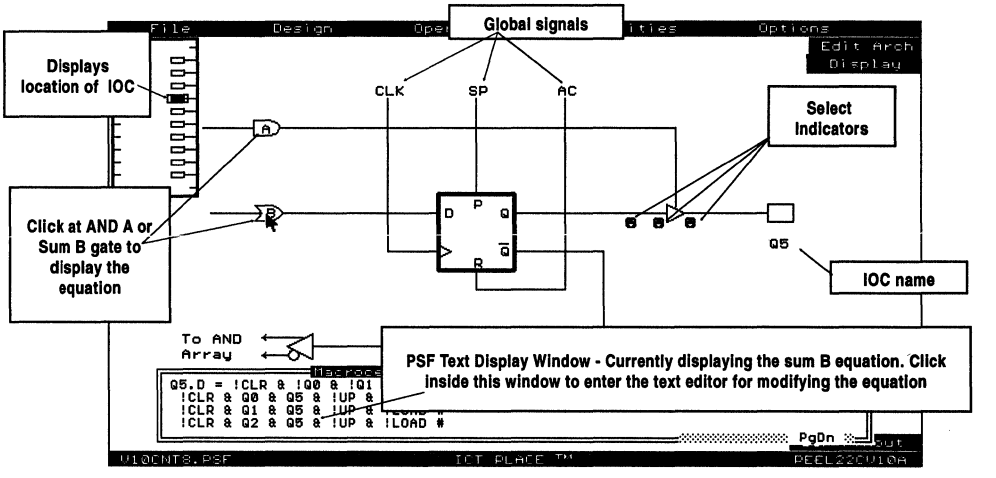

Figure 10-21, Editing equations in the IOC screen of the PEEL22CV10A

10.10 Design Operation - State Diagram Designs

An alternate method of describing a logic design is the state diagram design implementation. In this section, the procedure to implement the state diagram designs is discussed. The syntax for these state diagram designs are discussed in detail in chapter 11 on "PLACE Design Language".

The first step in the state diagram design is to label the cells to be used as state variables for the state diagram. These cells will be referred to as "State Cells". Then, configure each state cell and use the "Copy" command to duplicate the configurations to other state cells. Next, select the "Allocate" command (section 10.4) in the "Design" menu window to implement the state cell assignments. Choose the "State Diagram" option in the "Design Type" window. A window pops up allowing the options of adding or erasing state diagrams (Figure 10-22).

Note that the PEEL22CV10A device is used in the example described in this section. The procedure of implementing the state diagram design remains the same for all devices. In addition to the IOCs, LCCs in the PEEL Arrays can also be allocated as state cells.

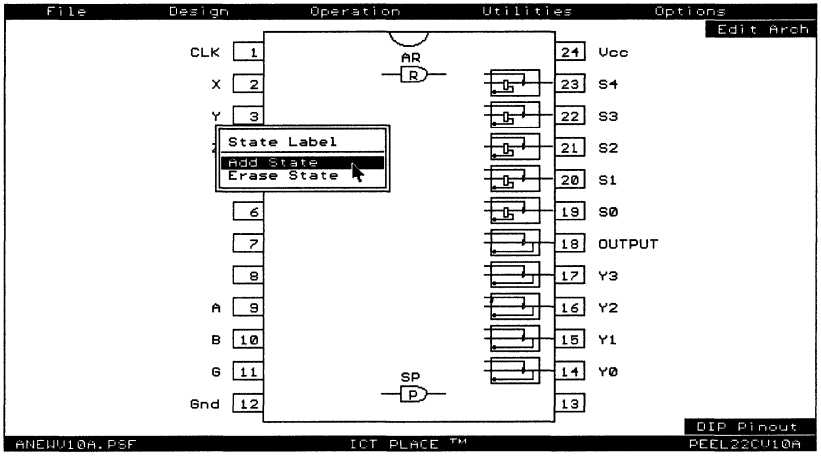

Figure 10-22, Adding a state diagram design

Type in the label for the new state diagram. The syntax of the label is similar to those used for labelling pins or cells (refer to chapter 11 on "PLACE Design Language"). The next step is to allocate the state cells as illustrated in Figure 10-23.

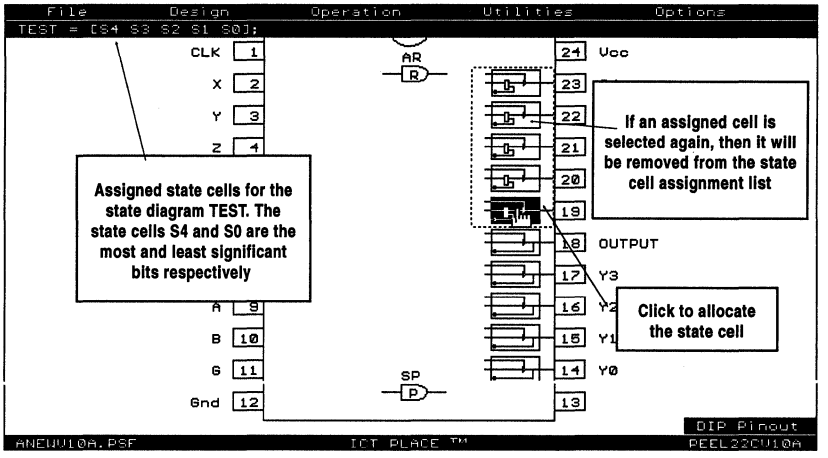

Figure 10-23, Allocating state cells for a state-diagram design

After completing the state cell assignments (by pressing the [Esc] key or click-R), a border surrounds the assigned state cells to indicate the state diagram. Additional state diagrams are differentiated by the line types in the borders.

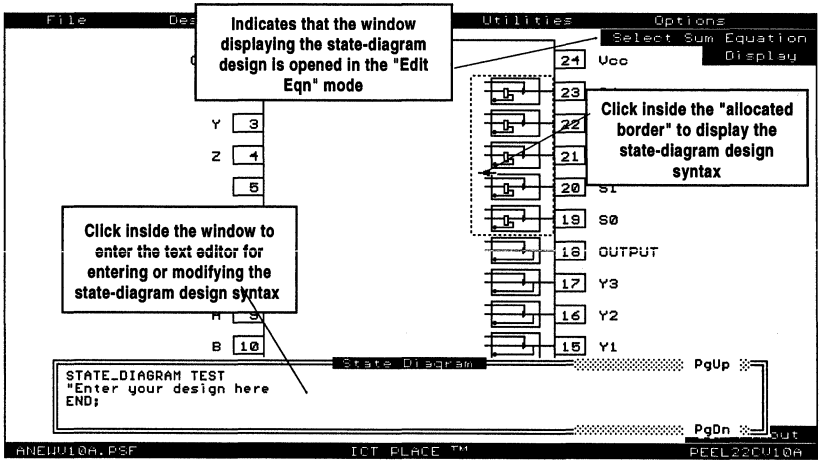

Figure 10-24, Entering design description for the state-diagram

10.11 Design Operation - Truth Table Designs

In truth table designs, the description of the logic design is in the form of a truth table. This design method is most suitable for random combinatorial logic applications.

Like the state diagram design procedure discussed in the previous section, the truth table design begins with allocating labeled pins and cells. Figure 10-25 shows a new truth table being labeled "DECODE" at the beginning of the truth table "Allocate" command.

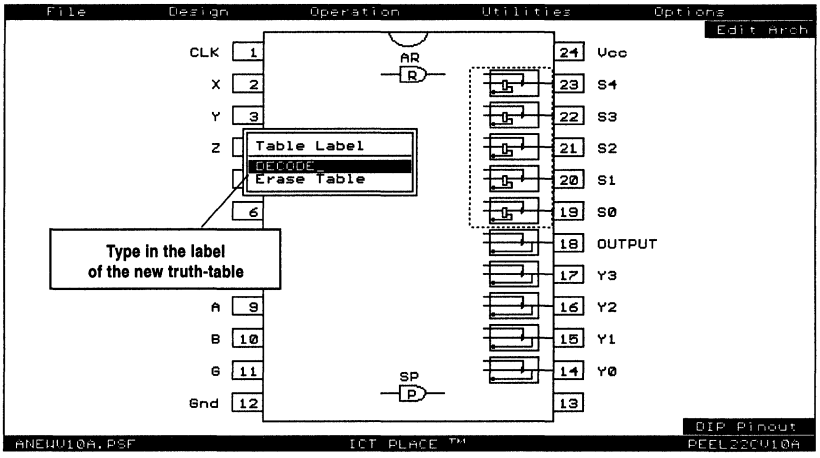

Figure 10-25, Entering the label for a new truth-table design

After typing in the label, the next step is to select the inputs of the truth table (Figure 10-26). A truth table input can be a pin, INC, IOC, or LCC. Click at the "Output" option in the pop-up window to complete the input selection and to start the output selection. Press the [Esc] key or click-R to complete the output selection.

Note that during the input or output selection process, if you click on a selected pin or cell, then it will be removed from the input or output selection list.

Press the [Esc] key or click-R during the input or output selection process to abort or complete the "Allocate" command. A window will pop up to confirm implementing the changes made. Pressing the [Esc] key or clicking-R when the "Implement changes?" window is popped up will return you to the previous mode (input or output selection).

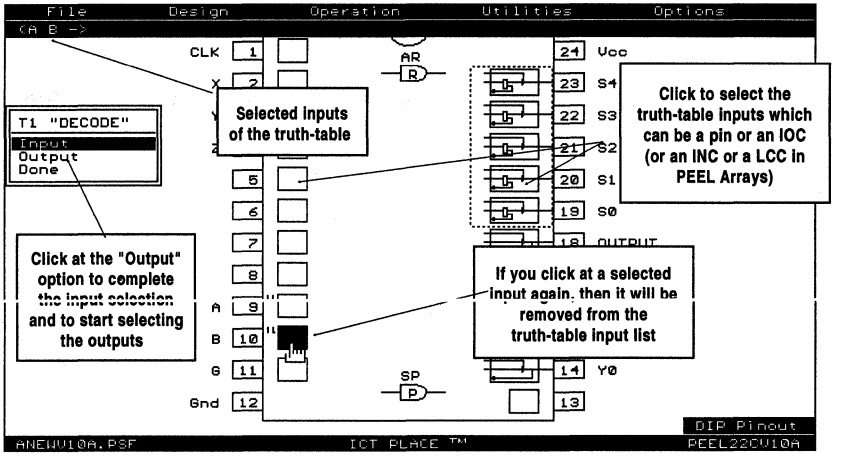

Figure 10-26, Selecting truth-table inputs

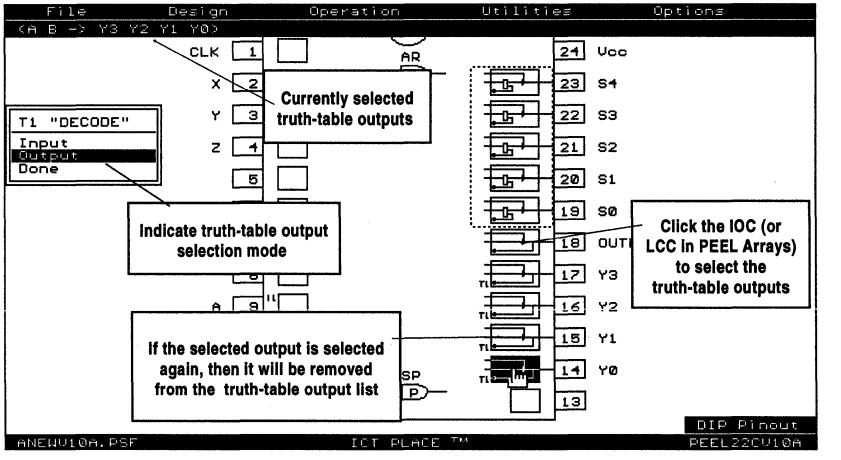

Figure 10-27, Selecting truth-table outputs

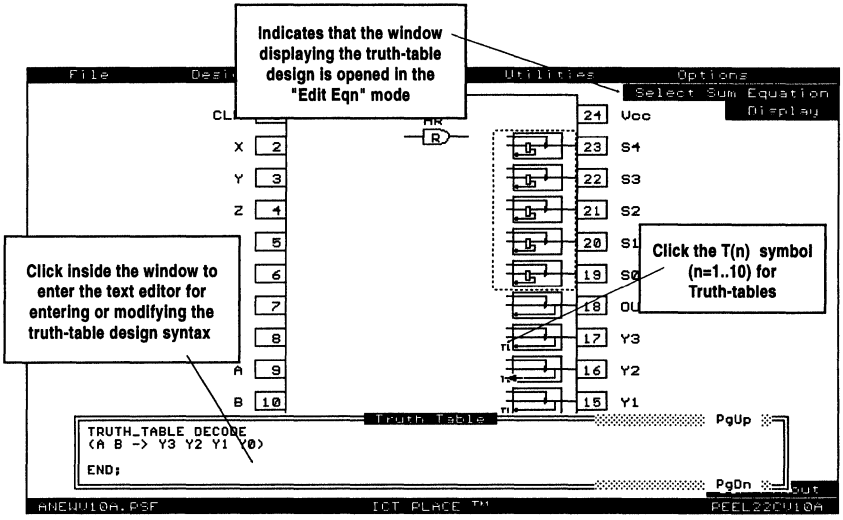

Figure 10-28, To enter the truth-table design description

For more information on the syntax of the truth table design description, please refer to chapter 11 on "PLACE Design Language".

10.12 Design Operation - PSF Text Display Window

The PSF Text Display Windows are the windows which can be opened to display the logic description of the current design, such as equations, state diagrams, truth tables, macro definitions, and etc. The two types of windows in the PLACE software are the Equation and Option Display windows. An Equation Display window is opened by clicking the left mouse button on any SUM or AND node (gate), state diagram block and truth table marker (indicated by Tn where n = 1 to 10). This window is always located at the bottom of the screen. Refer to Figures 10-29 through 10-31. On the other hand, the Option Display window is located at the top of the screen and is opened from the "Display" menu. The "Display" menu is selectable in the "Edit Eqn" mode, LCC/IOC screen for the PEEL Arrays, and IOC screen for PEEL Devices. See Figures 10-29 and 10-30.

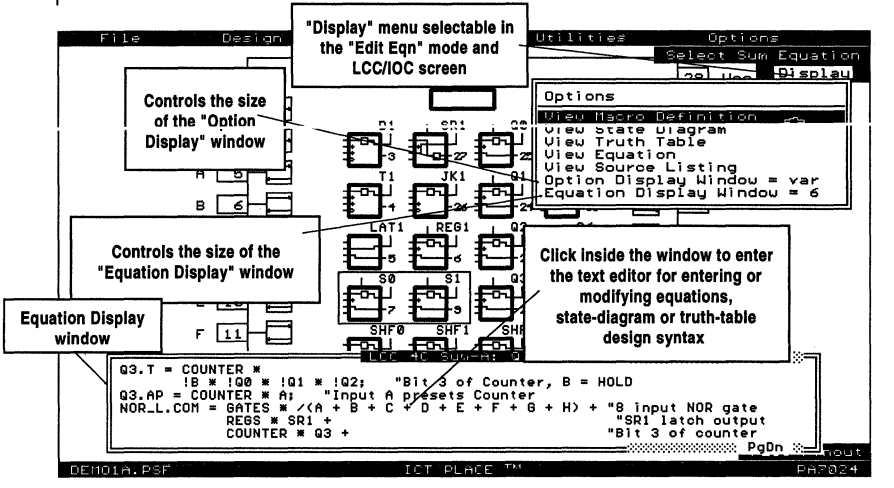

Figure 10-29, "Display" menu in "Edit Eqn" mode

Display Options

In the "Display" menu, there are several categories of the PSF design file in which it can be selected for viewing. The list includes Macro Definition, State Diagram, Truth table, Equation and Source File. With or without the Equation Display window opened, you can open this additional window by clicking at the selected category (Figure 10-32).

If the "Equation" or "Source File" option is selected, the window opens by displaying the most recently displayed page. This means that if you have previously opened the "Equation" or "Source File" window and have paged up or down, then the next time you select the same option the previous page will be displayed.

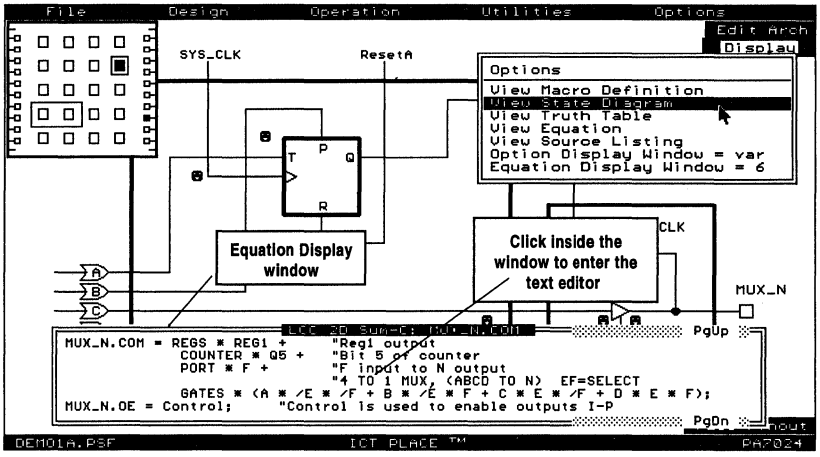

Figure 10-30, "Display" menu in the LCC/IOC screen

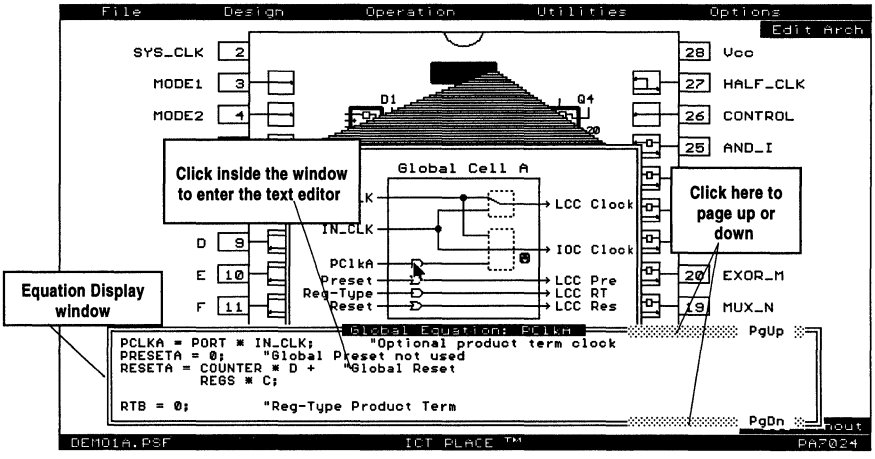

Figure 10-31, Equation Display window of the Global Cell A

Sizing the Display Windows

There are two ways which you can size the display windows:

- The first method is by pressing the Up and Down cursor keys followed by the [ENTER] key when the window is displayed. The first cursor key pressed enters the sizing mode by outlining the current window. Each subsequent cursor key moves the window border up or down. Then, press the [ENTER] key to accept the selected size. The maximum number of lines for each window is 19.

- The second method is to use the last two options in the "Display" menu (Figure 10-29). Click at either option to advance the number of lines for the window. This number will be used the next time the window is opened. In addition, the selection "var" ("variable") is available for both these options. This selection (illustrated by "Option Display Window = var" or "Equation Display Window = var") allows the size of the window to be dependent on the type of design syntax selected. The criteria for setting the "var" window size are:
  - **Equations (Equation Display Window only):** A set of equation will be displayed. This equation starts from the selected SUM or AND gate label (e.g. Q1.D) and ends with any of the following characters (in prioritized order): ";", "=", "TEST_VECTORS" or ASCII# 26 (End-of-File) character.
  - **State Diagrams:** A state diagram design group which begins and ends with the keywords "STATE_DIAGRAM *statename*" and "END;" respectively.
  - **Truth Tables:** A truth table design group which begins and ends with the keywords "TRUTH_TABLE" and "END;" respectively.
  - **Macro Definitions:** The displayed text will succeed the keyword "DEFINE" but precede "STATE_DIAGRAM *statename*", "TRUTH_TABLE" or "EQUATIONS".

For the "Equations" and "Source File" options in the Options menu, the "var" selection sets the window size to 19 lines (maximum number).

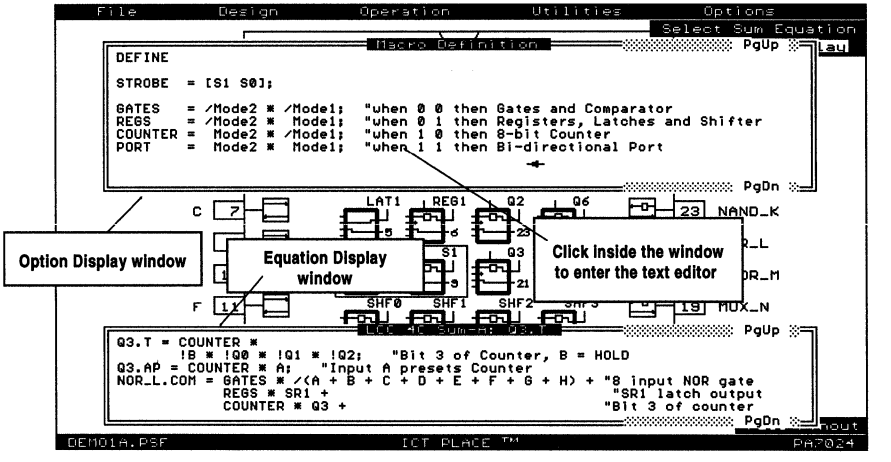

Figure 10-32, Both Equation and Option Display windows opened

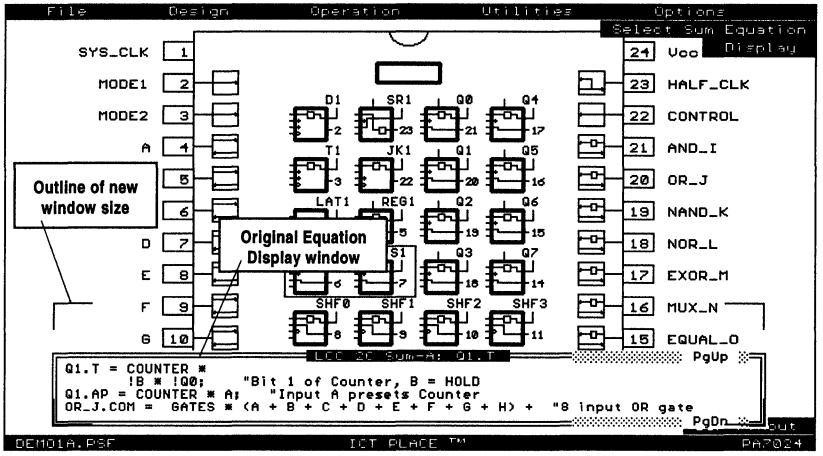

Figure 10-33, Sizing the Equation Display window

Paging Up and Down

The contents of the window can be paged up and down by pressing the PgUp and PgDn keys respectively. It can also be accomplished by clicking at the PgUp and PgDn markers in the upper and lower right corner of the window (Figure 10-31).

Entering the PLACE Text Editor via the Display Window

Clicking the left button of the mouse within the Equation or Option Display window opens the PLACE text editor for entering or modifying the design syntax. In addition, the PLACE text editor highlights the selected block and moves the text cursor to the top of the block. The block that is highlighted depends on which Display Window the text editor was opened from. If the editor was opened via the Equation Display Window, then the equation, state diagram or truth table block will be highlighted depending on which design type was selected. If the Option Display Window was used instead, then the block displayed on the window will be highlighted in the text editor. To return to the previous screen, press the ESC key.

10.13 Design Operation - Options Menu

Set Pinout to DIP/PLCC ..... Allows the pin numbers in the pin block diagram and LCC/IOC screen to show the pinout of DIP or PLCC package type. Figures 10-34 and 10-35 show the pinouts for DIP and PLCC packages respectively. **The default is the DIP pinout for all devices with the exception for the PA7140 device which defaults to PLCC pinout configuration.** Pinout for the SOIC package is the same as the DIP package.

PLCC Configuration ..... Displays the design in the actual PLCC package form (Figure 10-36). Press the [Esc] key or click-R to return to the previous screen.

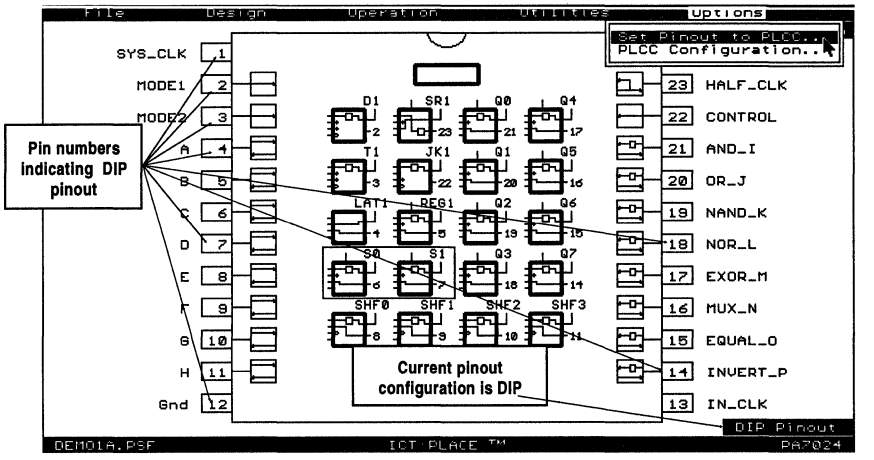

Figure 10-34, "Options" menu and DIP pinout for the PA7024

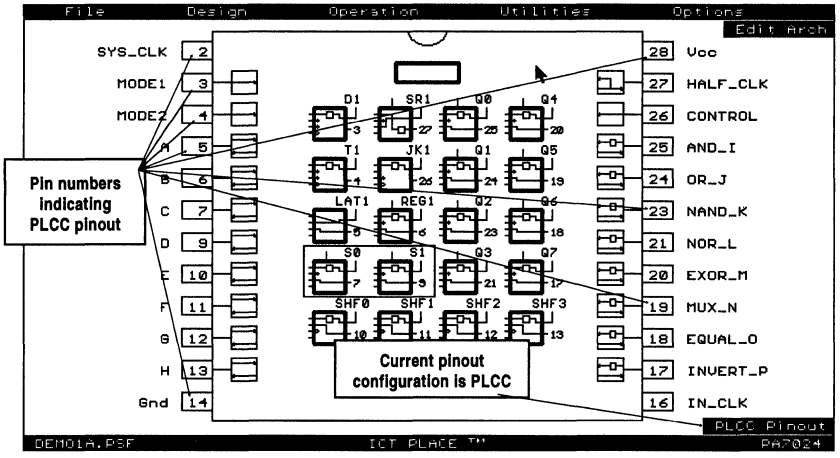

Figure 10-35, PLCC pinout for the PA7024

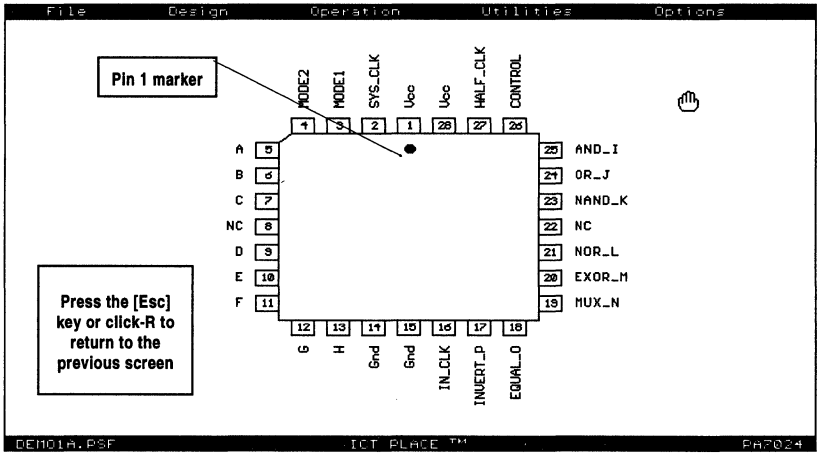

Figure 10-36, PLCC package configuration for the PA7024

10.14 Compile Operation - Main Screen

There are three windows in the main screen of the Compile Operation (Figure 10-37). Each of these windows provides a specific function in regards to the compilation process of the PLACE Source File (PSF).

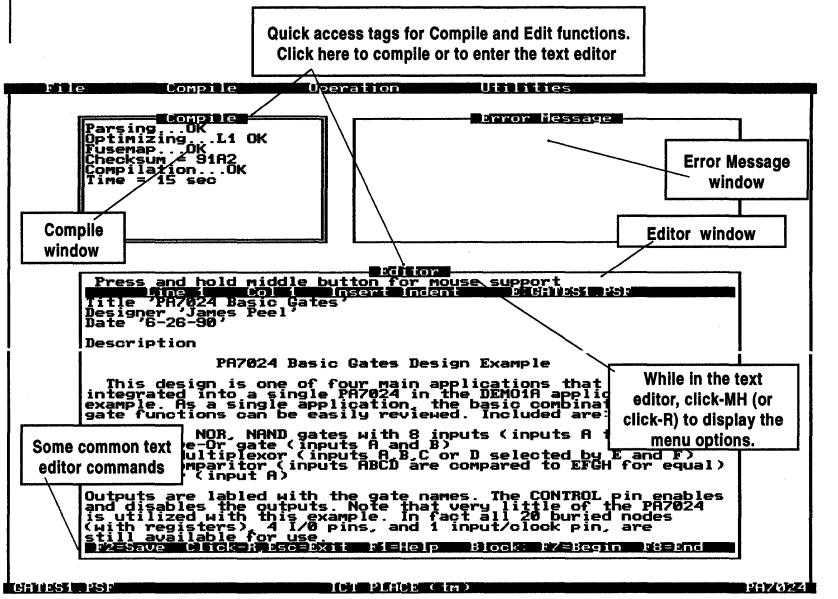

Figure 10-37, Compile Operation screen

Compile . . . . . This window displays the information regarding the status of the compilation. The compilation of a PSF file is a three step process: Parsing; Optimization; and Fuse-mapping.

Parsing - Checks the syntax of the PSF file and displays the error in the Error Message window.
Optimization - Implements logic transformation (complex equations into sum-of-product form conversion) and reduction to the parsed PSF file, and outputs the results to a file with extension ".RED". The RED file is in the PSF format, hence it can be read into the Design Operation for analysis of the reduced equations. After optimization is completed, the reduction level implemented is displayed. For instance in Figure 10-37, the "L1" term in "Optimizing ...L1 OK" indicates that the reduction level L1 was used for the GATES1.PSF design, and the optimization process was successful (as indicated by OK).
Fuse-mapping - This is the final step of the compilation process. After successful optimizations, the reduced equations are mapped into the device by outputing a

JEDEC file. In addition, the fuse-mapper outputs a ".MAP" file which contains the information on how each equation is mapped in the JEDEC file.

Once the compilation is completed and successful, the check sum of the JEDEC file and compilation time will be displayed.

Error Message . . This window displays any error encountered during the compilation process. Figure 10-38 shows an example of a syntax error in which an unknown signal "MØDE2" was encountered in the macro definition (the correct signal is "Mode2"). Once an error is encountered the compilation is aborted, and the text editor is opened automatically to allow the highlighted error to be investigated or analyzed. Note that the highlighted line sometimes does not contain the error. This may be due to an incorrect format for comments in previous lines. Please refer to chapter 11 for more information on the Comment format.

Editor. . . . . The Editor window allows the text editor to be opened for design edits or modifications. If a syntax error is found during the compiling process, the editor opens and highlights the error line automatically. A full screen editor is available via the "Utilities" menu.

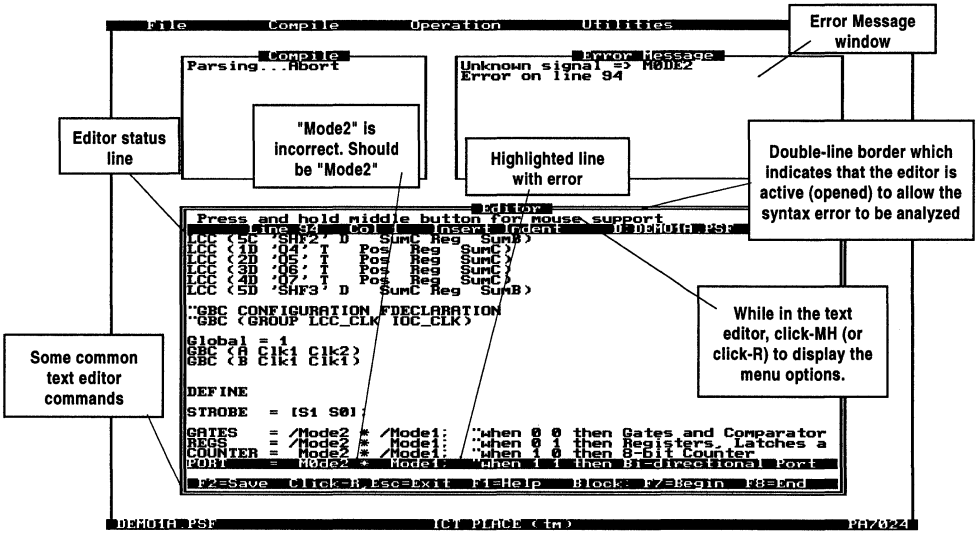

Figure 10-38, Encountering a compilation syntax error

10.15 Compiler Operation - Compile Menu

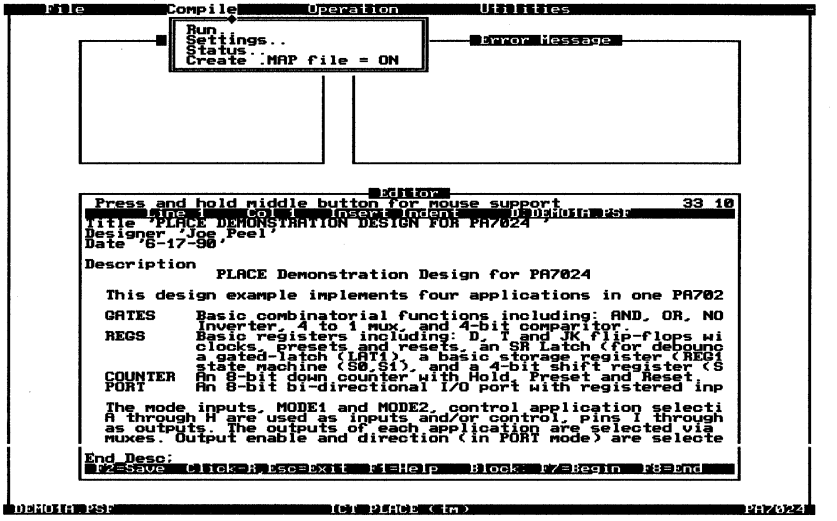

Figure 10-39, Compile menu

Run..... Compiles currently selected PSF design file. If the compilation process is successful, then a JEDEC ".JED" file will be created. If a compilation error occurs, an error message will be displayed in the Error Message window. In addition, the editor will be opened and the line containing the error highlighted automatically. You can then make the edits here or go back to the Design operation to correct the source file. Please refer back to section 10.14 for more information on the compilation process. **Note: The compiler can be executed by clicking at the "Compile" window heading.**

Settings..... Allows the selection of logic optimization level and product term utilization as listed in Table 10-3.

- **The default option for the reduction level selection is "Auto 1-5".** The "Auto" reduction levels refer to the automatic increments of the reduction levels. For instance, the "Auto 1-5" means that the optimization process starts with reduction level 1. If the design does not fit the device after the completion of level 1, then it proceeds to level 2. If the design still does not fit the device, it proceeds to level 3 and so on until a fit occurs. Once the design achieves a device fit, the reduction level will be displayed in the Compile window (Figure 10-37).
- There are five reduction levels, ranging from no logic reduction to group reduction with deMorganization of

outputs. The higher the level the better the utilization but the optimization time will also be longer. When compiling a design for the first time, it is recommended to use the "Auto 1-5" option. Note the level needed (displayed in the Compile window) to successfully compile the design. For subsequent compilations, select the single reduction level.

- **"Utilization":** This command allows the maximum number of product terms (in percentage) used during the logic optimization process to be set. For instance in the PA7024 device, if the product utilization is set as "Utilization = 60 %", then 60% of 80 product terms (80 product terms is the maximum for the PA7024) will be used during logic optimization. Hence, this command allows you to estimate whether additional logic can be implemented into the selected device. **The default product term utilization is "Utilization = 100 %".**

Optimization Function Level	
Level 1	No reduction. Transforms equations to sum-of-products.
Level 2	Simple reduction. Combines duplicate product terms.
Level 3	Pin reduction. Optimizes terms per individual equation.
Level 4	Group reduction. Optimizes terms over all equations which can be shared.
Level 5	Group with output polarity inversion reduction. deMorganizes Outputs (automatically inverts polarity) to achieve best optimization of terms.
Auto 1-2	Optimizes from Level 1 to 2 until logic fits.
Auto 1-3	Optimizes from Level 1 to 3 until logic fits.
Auto 1-4	Optimizes from Level 1 to 4 until logic fits.
Auto 1-5	Optimizes from Level 1 to 5 until logic fits.
Utilization	Sets the maximum product terms which can be shared to be used in the logic reduction or optimization process. The number set is in percentage.

Table 10-3, "Settings" menu in the Compile menu window

Status ..... Displays the device utilization and use of architecture after the design is compiled.

Create .MAP file During the fuse-mapping process, a ".MAP" file can be created in addition to the JEDEC file. This MAP file contains the detailed information regarding how each equation is mapped in the JEDEC file. **The default condition is ON.**

10.16 Simulate Operation - Waveform Screen

After successful compilation of a PSF design file, test-vectors may be necessary to verify the design. In the Simulate operation, these test-vectors are displayed as waveform signals (Figure 10-40). The vectors are created using the "Edit" command. The vectors are then used to simulate (logically only) the function of the design by retrieving the design's logic from the JEDEC file which was created in the Compile operation. These vectors can also be appended to the JEDEC file so that they can be used to exercise the device after programming.

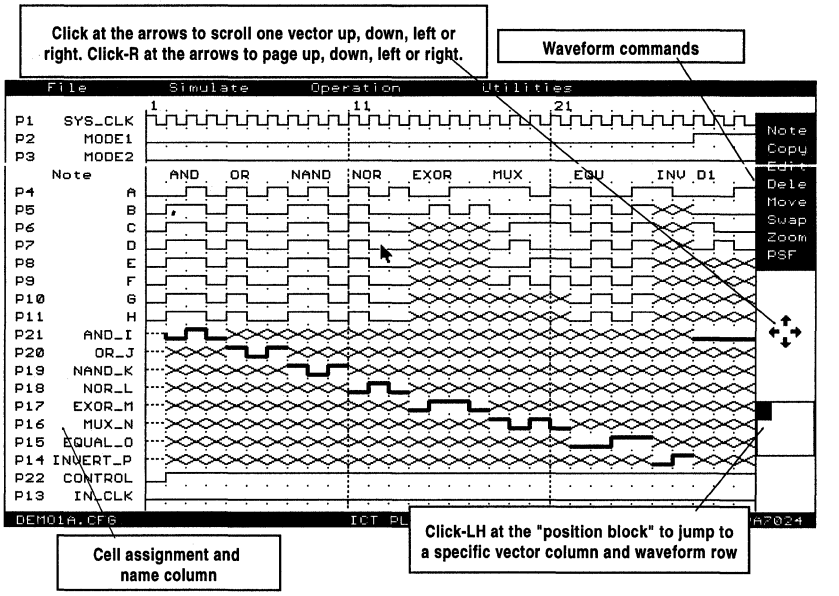

Figure 10-40, Simulate waveform screen

In the waveform display, each waveform row represents a signal from a pin or an internal node (e.g. a LCC, IOC or INC). The external pins are indicated by "P" followed by the pin number. LCC internal output is indicated by "L" with the cell assignment coordinates. The prefix for the IOC or INC node (i.e. the output of the IOC or INC register) is an "I" followed by the assigned pin number. The IOC and INC nodes are differentiated by the assigned pin numbers. For instance in the PA7140 device, pins 3-5, 19-21, 25-27 and 41-43 are assigned to INCs. The rest of the pins except pins 2 and 24 (CLK pins) are assigned to IOCs. For more information, please refer to the ICT data book.

Examples of the waveform pin and cell assignments, and labels found in the TC7140.PSF design file of the PA7140 (the PA7140 device has all the cells, i.e. LCCs, IOCs and INCs) are:

P2	CLK	=> pin 2 with label CLK
L3A	P2	=> LCC 3A with label P2
I15	C2	=> IOC 15 with label C2
I4	SELECT	=> INC 4 with label SELECT

Scrolling and paging in the waveform display

As illustrated in Figure 10-40, scrolling and paging can be accomplished by clicking and clicking-R at the arrow markers located on the right side of the screen. An additional method of scrolling and paging is to use the left, right, up and down cursor keys, and the [PgUp] and [PgDn] keys respectively.

Alternately, you can click-LH (click and hold the left mouse button) at the "position block" to jump to another waveform display section. Once you have selected the location, release the left button to return to the normal screen mode.

Functions of the waveform signals

In the Simulate operation, the graphical image of each waveform signal represents a specific function. For instance, the waveform signal image ⎍ which is represented by the test-vector C in the JEDEC file indicates a Low-High-Low input pulse. This signal functions as a clock for triggering a register on the rising or falling edge of the signal. Please refer to Tables 10-4 and 10-5 for additional information on other waveform signals.

Symbol	Color	Function	JEDEC Vector Symbol
	Blue	System Clock	C
	Blue	Input High	1
	Blue	Input Low	0
	Blue	High Voltage Preload	P
	Blue	Input or Output Don't Care	X
	Yellow	Output High	H
	Yellow	Output Low	L
	Yellow	Output High Impedance	Z
	Red	Buried or Internal Signals which cannot be modified	N/A

Table 10-4, Waveform signal symbol table for a color monitor

Figures 10-40 through 10-55 illustrated in this section were captured via a monochrome monitor. Refer to Table 10-5 for the functions of the waveform signals in these figures.

Symbol	Linewidth	Function	JEDEC Vector Symbol
	Normal	System Clock	C
	Normal	Input High	1
	Normal	Input Low	0
	Normal	High Voltage Preload	P
	Normal	Input or Output Don't Care	X
	Thick	Output High	H
	Thick	Output Low	L
	Dotted	Output High Impedance	Z
	Center	Buried or Internal Signals which cannot be modified	N/A

Table 10-5, Waveform signal symbol table for a monochrome monitor

10.17 Simulate Operation - Simulate Menu

Simulate ..... Performs logic simulation of waveform vectors on external signals, i.e. on the "P" waveform rows only. The simulator compares the simulated signals with the current signals on the pins, and then mark the locations with signals that do not match. These marked locations are vector simulation errors (Figure 10-42). The special symbols used indicate the type of simulation errors (Table 10-6). On the other hand, the signals for all internal nodes are not checked but are automatically captured during logic simulation.

During simulation, the design's logic is retrieved from the JEDEC file that has the same root name. For example, the JEDEC file DEMO1A.JED will be used during the vector simulation of DEMO1A.CFG.

Capture ..... Unlike the "Simulate" command, this command "captures" the signal on all external outputs. With this command, signals on the output pins need not be generated be-

cause the simulated signals are automatically inserted by the simulator. In addition, the simulated signals are also inserted into vector locations which contain the output Low "L", output High "H" and Don't Care "X" signals. This means that if you have simulation errors on any of these vector locations, they will be replaced by the simulated signals. See Figure 10-42.

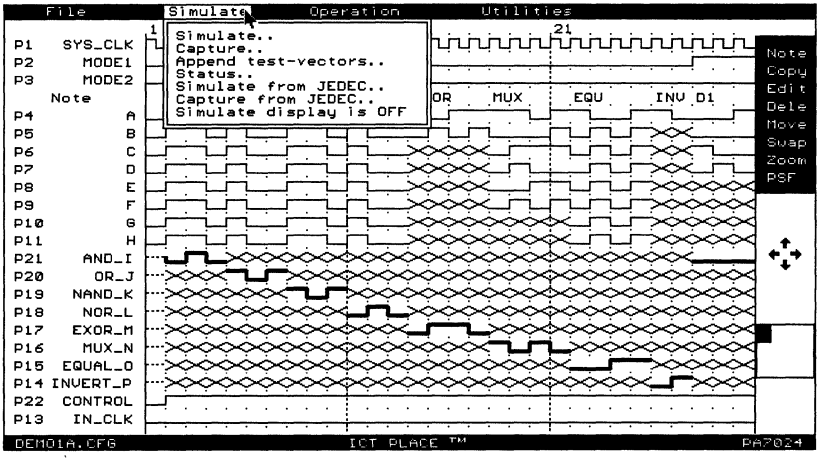

Figure 10-41, Simulate waveform screen

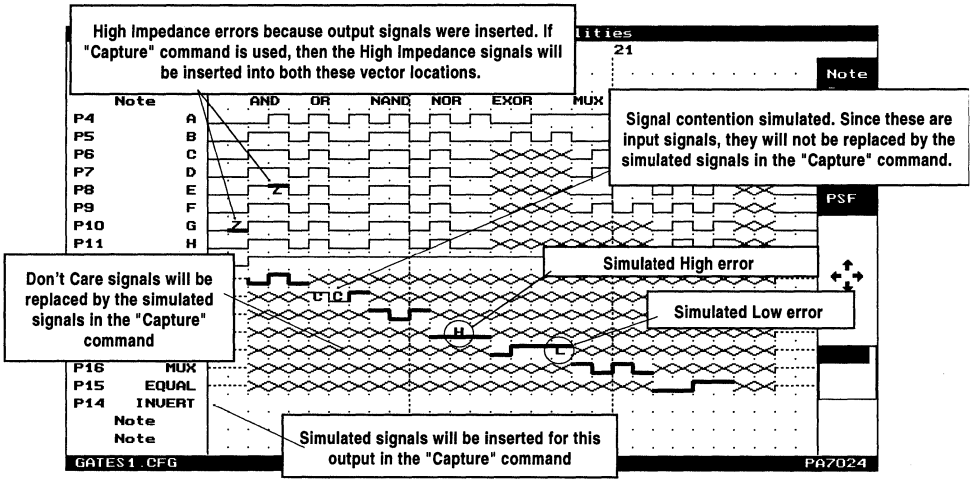

Figure 10-42, Vector simulate errors

Error Symbol	Function
L	Indicates that a LOW signal is simulated on the pin at the current vector location.
H	Indicates that a HIGH signal is simulated on the pin at the current vector location.
Z	Indicates that the pin is in a High Impedance condition at the current vector location. An example is the insertion of output signals ("L" or "H") on inputs.
C	Indicates that a signal contention condition exists at the current vector location. An example is the insertion of input signals ("0" or "1") on outputs.
U	Indicates that the signal at the current vector location is unstable or in an indeterminate state. An example of an application which causes this error is an oscillator. When an unstable error occurs, the simulation process is aborted and the pin number(s) reported. Note that the PLACE Simulator will not flag an error if the unstable output has a Don't Care symbol.

Table 10-6, Simulation error symbols for pins

Please refer to Figure 10-43 for information on the "Simulate" and "Capture" commands for asynchronous clock designs.

Append test vectors..... This command converts the waveform vectors into the JEDEC file test-vectors and appends them to the ".JED" file. This allows the vectors to exercise the device on a PLD programmer.

Status ..... Provides status information such as the maximum vector columns available with the current system configuration (more system RAM memory, more vector columns available), number of total vectors used, number of simulation errors, and the previous simulation time.

Simulate from JEDEC..... With this function, the PLACE Simulate waveforms can be generated from the test vectors specified in the JEDEC file. If an ICT PDS-1 programmer is present, this function together with the "Capture" function in the "Test" menu of the Program operation allow viewing of device vector results via the waveform screen.

Capture from JEDEC..... This command is similar to that of the "Simulate from JEDEC" command except that the output signal levels will be replaced by the simulated signal levels.

Test Vectors for Asynchronous Clock Applications

Asynchronous clock refers to the triggering of the LCC or IOC register via a sum or product term. Devices with the asynchronous clock capability include PA7024, PA7140 and PA7128. If the simulated waveform vectors are appended to the JEDEC file for exercising the device, then special attention for the asynchronous clock designs is needed. This is because of possible data set-up time violations due to how the input signals are applied on the PLD programmer.

Note: Some programmer, the input signals are applied serially starting from pin 1 after the device has been powered-up (set the Vcc pin to 5V). First, input signals "0" and "1" are applied, then preset signals "P" (this is high voltage preset which is not supported in many PEEL devices), then clock signals ("C"), and then the output pins are sensed and compared with the vectors from the JEDEC file. With this method, data set-up time violations for asynchronous clock designs are very possible, especially if the input signals "0" and "1" are used to emulate the clock signals.

There are two methods to ensure the proper test vectors for testing the asynchronous clock designs.

1. The first method is to use the dedicated clock signal ⎍ (JEDEC "C") in the sum or product term equation. Since this signal exhibits a Low-High-Low voltage level in a given vector period, the standard logic operation of the AND and OR operators may be applied, but with some modifications.

Clock	Operator	Input	Result
C	& (AND)	1	C
C	&	0	0
C	# (OR)	1	C
C	#	0	C

   By using the dedicated clock signal, the programmer applies the signal to the clock only after all input signals are applied. Note that if the result "C" is routed to an external output, then a signal contention error will be flagged.

2. The second method is to add dummy or Wait states prior to all clock edges which are generated by the "0" and "1" input signals. The advantage with this method is that the same clock signal can be routed to an external output without encountering a signal contention simulation error as in the preceding method. However, the disadvantage is that a minimum of two vectors are required to generate a clock cycle, "0" and "1" signals on successive vectors.

Figure 10-43, Test Vectors for asynchronous clock applications - Sum or Product term clock

Preloading the LCC registers (in logic simulation only)

In the Simulate operation for the PA7024, PA7140 and PA7128 devices, all the LCC registers can be preloaded with the user-specified data. Note that this feature is only a software feature and does not exist in the device physically. If the preload vectors are applied to the device on a PLD programmer, these vectors will fail.

In Figure 10-44, the PA7024 application example has two sets of registered output pins P0..P7. At the preload vector column 11 and 22, the LCC registers for these outputs are preloaded with data 0 and FF HEX respectively. The preload condition is activated by the waveform symbol \ (JEDEC "P") on the dedicated preload pin 13 (each device type has a specific pin dedicated for the preload function). The clock symbol ⌐¯ on pin 1 is not necessary because the preload symbol automatically loads the data in asynchronously.

Below is a list of the preload pins and the assigned pins for the LCC registers for the PA7024, PA7140 and PA7128 devices.

Device	Preload Pin	Preload Data Pins	LCC Registers
PA7024	13	2 - 6	LCC 1A - 5A
		7 - 11	LCC 1B - 5B
		14 - 18	LCC 1C - 5C
		19 - 23	LCC 1D - 5D
PA7140	24	6 - 11	LCC 1A - 6A
		12 - 16, 18	LCC 1B - 6B
		28 - 33	LCC 1C - 6C
		34 - 38, 40	LCC 1D - 6D
PA7128	1	15 - 17	LCC 1A - 3A
		18 - 20	LCC 1B - 3B
		21 - 23	LCC 1C - 3C
		24 - 27	LCC 1D - 3D

By adding the preload condition at the beginning of each CFG file (except for the first one), then up to 36 CFG files (CFA, CFB, .., CFZ and CF0, CF2, .., CF9) can be linked together for simulating a large PEEL Array design. With approximately 700 vectors per CFG file for a 512K system, about 25,000 "continuous" vectors can be simulated for a design.

Figure 10-45, LCC Register Preload function

Simulate display ..... When the Simulate display is set to the ON condition, the waveform vectors are displayed during the simulation or capture process. If this command is set to the OFF condition, the waveform vectors will not be displayed during simulation. Instead, each vector will be illustrated by a "." for a vector which passes simulation, and a "*" for a failed vector.

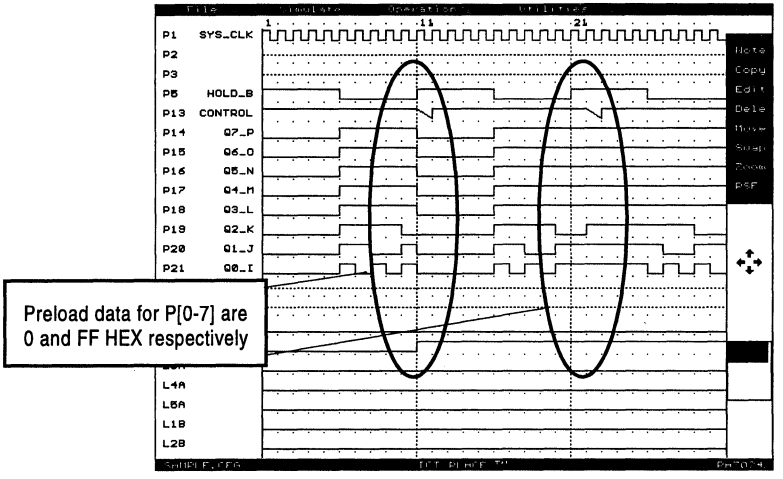

Figure 10-44, PA7024 LCC Register Preload, and Product or Sum Clock application

10.18 Simulation Operation - Entering or Editing Waveforms

In the Simulate operation, the test vectors are entered or modified via the "Edit" command. All other commands on the right side of the screen (such as Note, Copy, and etc.) are merely used for organizing the waveform screen. This means that these commands do not affect the results of the vector simulation. Please refer to section 10.19 for more information on the waveform organization commands.

Note that only waveform signals for the external pins (inputs or outputs) can be entered or edited. All internal node signals are captured by the simulator and displayed for analysis.

Edit ..... Edits input or output vectors, or inserts the text into the rows generated by the Note command. There are three methods of entering or editing the waveform vectors.

1. Move the edit "box" cursor to a vector location and click the mouse button. Continue clicking until the desired waveform signal is displayed. Since there are eight different signals possible, each vector is selected again after every eight clicks.
2. Move the edit cursor to a vector location and press the vector symbol keys such as C, 1, 0, P, H, L, X or Z to select the type of waveform signal. For instance, pressing the key "C" will select the clock signal for the current vector location. Refer to

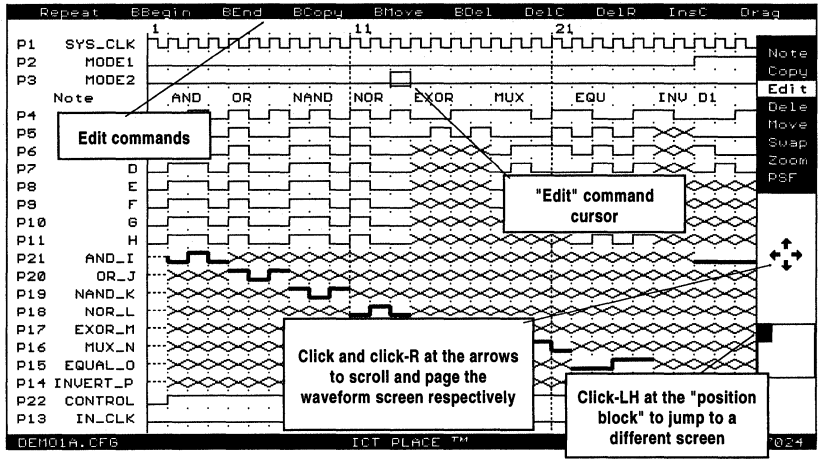

Figure 10-46, "Edit" command in the Simulate operation

Table 10-4 or 10-5 for the description of each waveform signal. Note that the vector symbols are actually the standard symbols used in the test vector section of the JEDEC file.

3. Use the "Drag" command which will be described later in this section.

Once the "Edit" command is selected, the advanced commands for editing test vectors will appear at the top of the screen and can be selected with the mouse. In addition, the previous block of vectors selected via the BBegin and BEnd commands will be displayed. **Click-R to exit the "Edit" command.**

Repeat..... Repeat allows a single vector to be repeated by a specified number. Click "Repeat" then move the edit cursor to a vector location and click. This vector location will be the starting location. Then, enter the number of vectors to repeat and press Enter. All existing vectors following the starting vector will be overwritten.

The commands which begin with the letter "B" indicate that they are block commands. Block commands are commands which manipulate a block of test vectors referred to as a "vector block" (Figure 10-48).

BBegin..... This command allows a vector location to be selected as the beginning vector of the "vector block". If no current block exists, then the PLACE software automatically enters the "BEnd" command immediately after the selection of the beginning vector. If a block exists, then a new beginning vector can be selected. The previous ending vector will remain unchanged.

BEnd . . . . . Allows the selection of an ending vector for the "vector block". Like the "BBegin" command, a new ending vector can be selected for a current "vector block". If a block does not exist, then the selected ending vector is still applicable the next time a beginning vector is selected.

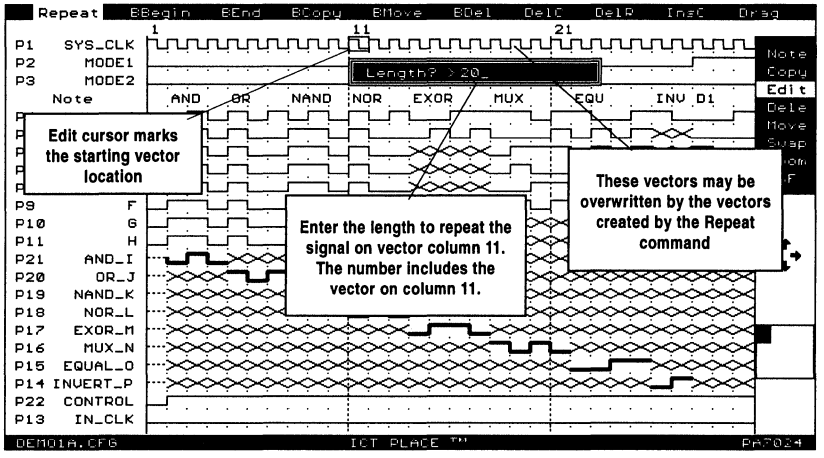

Figure 10-47, "Repeat" command

The beginning and ending vectors of the "vector block" must always be located on the upper-left and lower-right of the block respectively. A block can have a single row or column. In this case, the beginning vectors are the most-left or top vectors, and the ending vectors are the most-right or bottom vectors. In addition, beginning and ending vectors can be located on separate waveform screens.

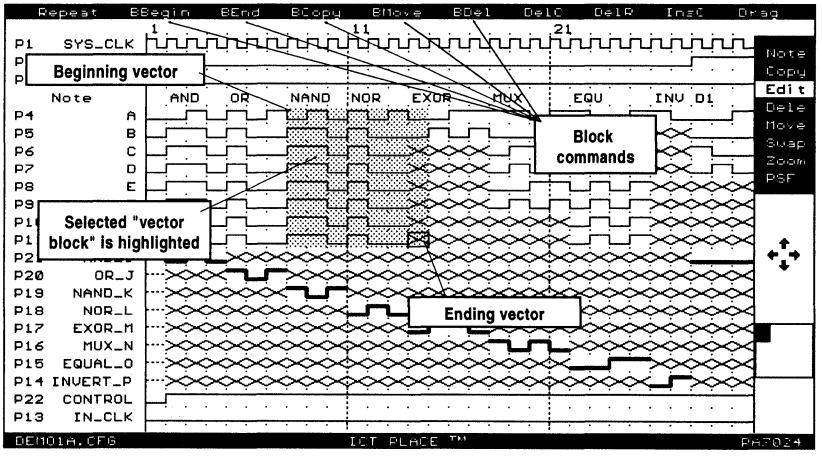

Figure 10-48, Vector block selected

BCopy ..... Copies the currently selected block into another waveform area after the selection of a starting vector location.

BMove ..... Moves the currently selected block into another waveform area after the selection of a starting vector location.

BDel ..... Deletes the currently selected block of vectors. A pop-up window to confirm the deletion will appear.

The following lists the row or column commands.

DelC ..... Enters a mode which allows the current waveform vector column to be deleted. Additional clicks will continue to delete the next vector column. Click-R to exit this mode.

DelR ..... Enters a mode which allows all the vectors on the selected waveform vector row to be deleted. Click-R to exit.

InsC ..... Enters a mode to allow vector columns to be inserted. The vector column is inserted prior to the selected vector column (Figure 10-49). Additionally, the signals on the new column follow the selected vector column.

Drag ..... Enters a mode which allows input or output signals to be entered or edited. Only four signals are available in the drag mode: input "0"; input "1"; output "L"; and output "H".

Select the waveform vector row and column after you have entered the "Drag" command. The drag edits will start from this location. Move the cursor horizontally across from left to right and click at the selected vector location to end the current signal. Click again to select

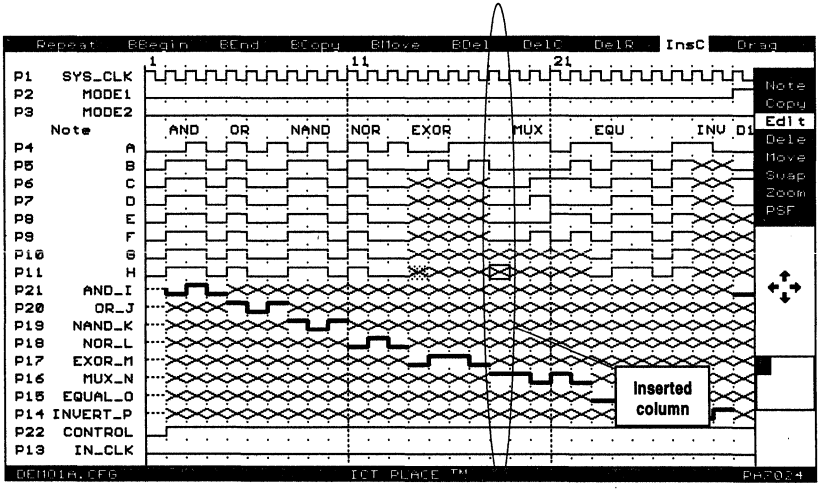

Figure 10-49, Inserting a vector column

another vector location. To exit the drag mode, click-R or press the [Esc] key. **Note that the drag edits will overwrite the previous vectors.**

Selecting the input or output signal

The input signal (blue or normal width) is selected when the "Drag" command is first selected. **To "drag" an output signal, press ^X or [Ctrl]-X during the "dragging" process, i.e. the input signal is currently being dragged. Pressing [Ctrl]-X during the drag process toggles between dragging an input or an output signal.** The output signal is indicated by a yellow or thick line.

10.19 Simulation Operation - Organizing Waveforms

All the commands in this section are used to organize the display of the waveform screen for a better understanding of the PLACE designs. This means that these commands do not affect the results of the simulation or the actual generation of the test-vectors for the JEDEC file. In each CFG Simulate file, a maximum of 99 waveform rows are allowed.

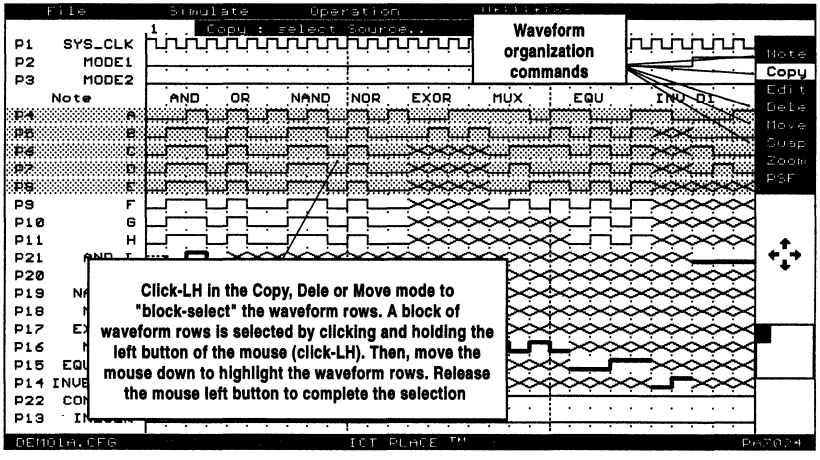

Figure 10-50, Commands for organizing the waveform screen

Note..... Allows a "Note" row to be inserted for adding comments to the waveform display. Add the note line by clicking at the desired line, click-R to exit note command then select the "Edit" mode. Move the edit cursor to the note line and click to enter text for the comments.

Copy..... Copies a waveform vector row or a "block" of selected waveform rows to another location. This command will prompt for a source and target selection. Click-R to exit this mode.

Dele ..... Removes a waveform vector row or a "block" of selected waveform rows from the current waveform screen. Note that the unduplicated waveform rows for external pins and internal nodes will be appended to the bottom of the CFG file (last screen of the waveform display). All other waveform rows such as Notes and duplicated rows (i.e. rows that were copied using the "Copy" command) can be removed from the CFG file. The CFG file has a minimum number of waveform rows allocated for each device type that cannot be removed. For instance, the PA7024 device has 62 waveform signals (22 inputs/outputs + 20 LCC internal outputs + 20 IOC registered nodes) that are always present in the CFG file.e. Click-R to exit.

Move ..... Allows a waveform vector row or a "block" of selected waveform rows to be moved from one location into another location. This command will prompt for a source and target selection. Click-R to exit.

Swap ..... Allows a waveform vector row to be swapped with another vector row. This command will prompt for a source and target selection. Click-R to exit. No "block" swapping is available.

10.20 Simulate Operation - Zoom Command

When the **"Zoom"** command is selected, the waveform screen displays 170% more vectors than the normal screen. Normally, the waveform screen is 22 rows by 30 columns. But in the zoom mode, the screen is 30 rows by 60 columns. With more vectors being displayed, more waveform vectors can be viewed on a single screen, which may lead to a better understanding of the overall design.

Within the Zoom mode, there are actually two separate modes which will be referred to as Zoom Modes A and B. A typical procedure of using the Zoom mode is:

- From the normal waveform screen mode, click at the **"Zoom"** menu on the right side of the screen to enter Zoom Mode A. The screen in this mode consists of 30 rows of waveforms and 60 columns of vectors.
- In Mode A, almost all commands in the Simulate operation can be executed. These commands include file read and save, simulate, capture, or the PSF command (section 10.21). Some of the commands not executable in Mode A are the Note, Edit, Erase, Copy, Move and Swap commands. If you click-R in Mode A, you will be returned to the normal waveform screen mode.

➤ To enter Mode B, click at the **"Zoom"** menu once again but this time don't release the left button of the mouse. A rectangular box depicting a window view of the current selected waveform screen is displayed (Figure 10-52). This rectangular "view" window can be moved to another location by moving the mouse. If you wish to return to Mode A at this time, press the right button of the mouse while the left button is being pressed. Otherwise, releasing the left button of the mouse will return you to the normal waveform screen selected via the rectangular "view" window.

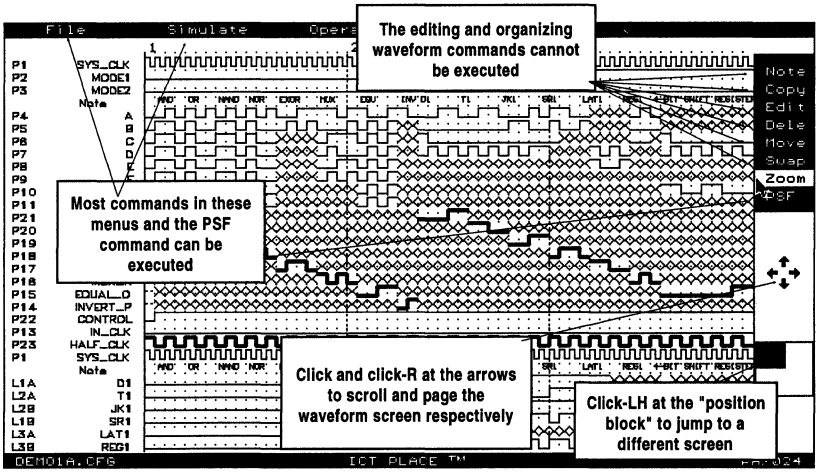

Figure 10-51, Mode A of the "Zoom" waveform screen

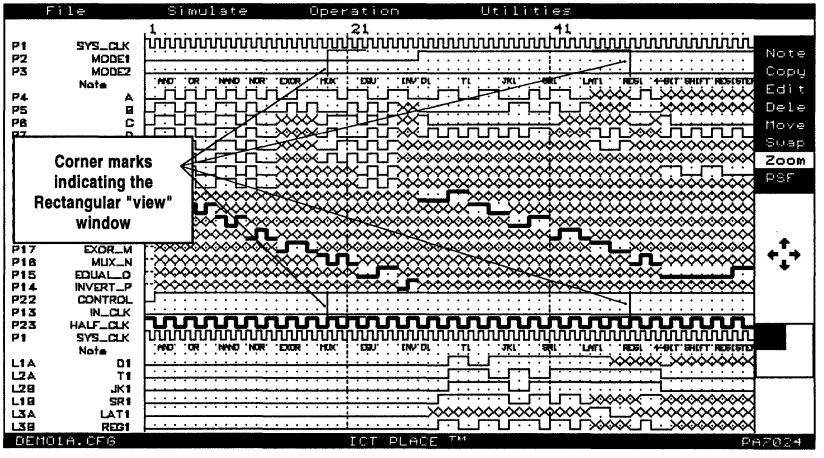

Figure 10-52, Mode B of the "Zoom" waveform screen

10.21 Simulate Operation - PSF Command

The PSF design file can be displayed on the waveform screen by selecting the **"PSF"** command located on the right side of the screen. With the PLACE design source file displayed, you can compare the simulation results with the design logic. If a simulation waveform vector error is detected, then the modification can be done using the "Edit" command. If the error is in the design logic, then return to Design operation to correct the error and recompile the PSF file.

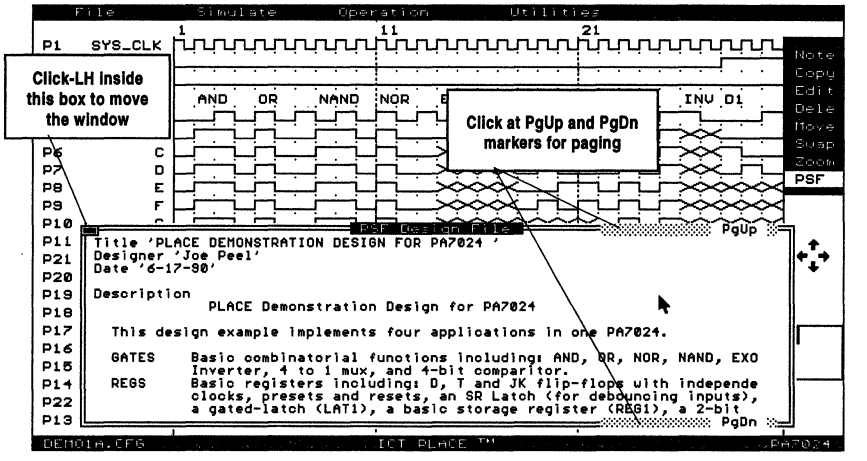

Figure 10-53, Mode B of the "Zoom" waveform screen

As shown in Figure 10-53, a window will pop-up displaying the PLACE design source file. The features of this window are similar to those available for the PSF Text Display windows found in the Design operation. These features include paging up and down the display screen and window sizing. An additional feature not available in the Design operation is the moving of the display window to another location (Figure 10-55). **To close the PSF window, press the [Esc] key or click-R.**

Paging Up and Down

Like in the Design operation, paging within the PSF window is accomplished by clicking at the PgUp or PgDn markers located at the top and bottom of the window, or by pressing the PgUp and PgDn keys. See Figure 10-53.

Sizing the Display Window

The size of the window can be adjusted by pressing the Up and Down cursor keys followed by the ENTER key. The Up cursor key increases the window size while the Down cursor key decreases the size. A maximum of 19 lines of text can be displayed on the window.

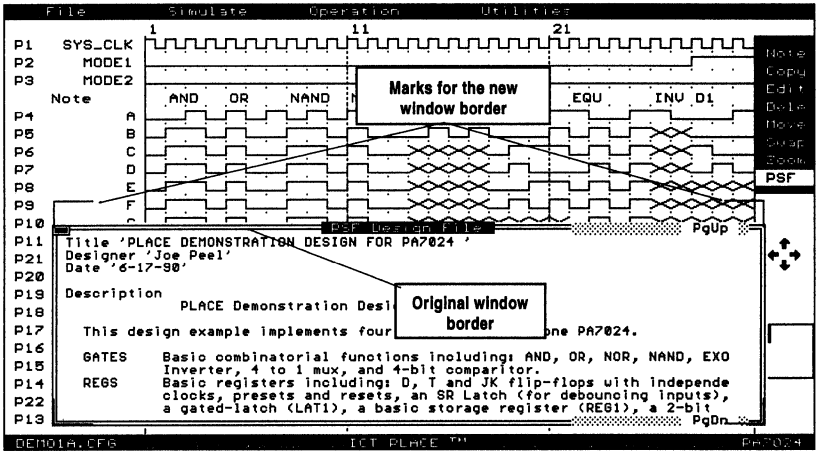

Figure 10-54, Sizing the PSF display window

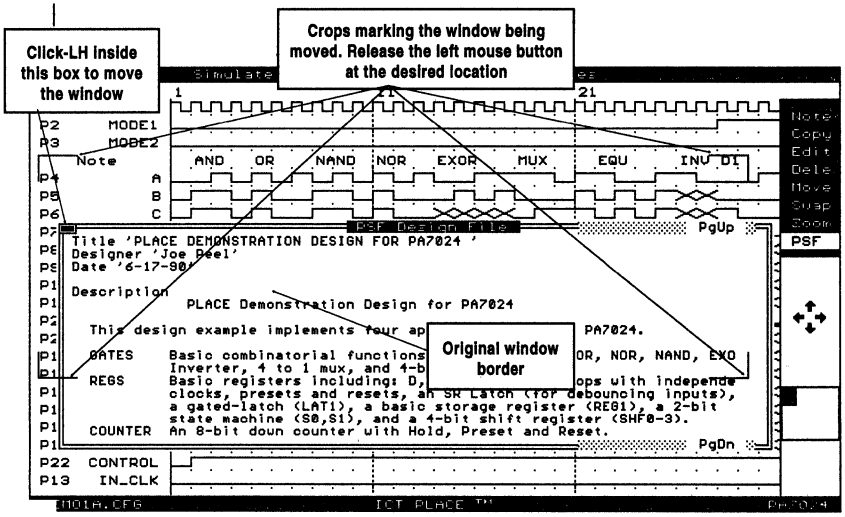

Figure 10-55, Moving the PSF display window

10.22 Document Operation - Document Window

In the Document operation, the documents relating to a PLACE design can be printed via some of the most popular printers, such as IBM and Epson graphic printers, HP Laserjet II and postscript laser printers. In addition, the printing of these documents (including the design configuration and simulate waveform screen images, PSF design file, compiled outputs and etc.) can be set up in a queue or batch mode.

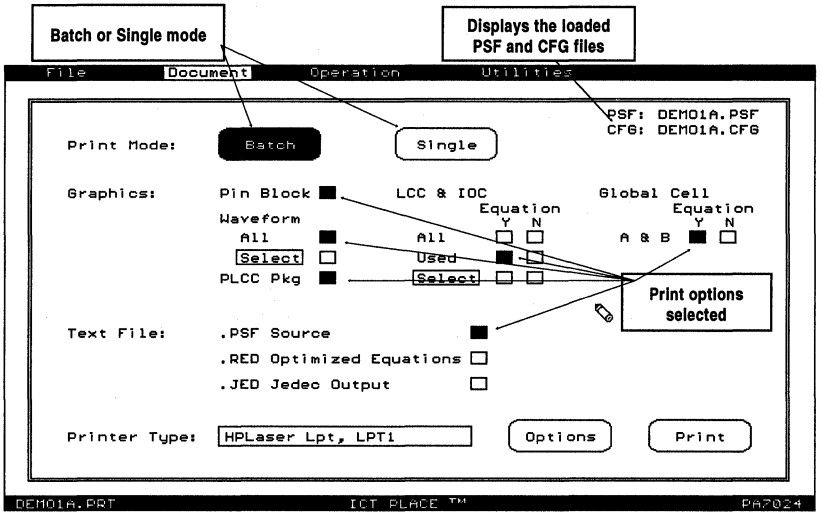

Figure 10-56, Document window for PA7024

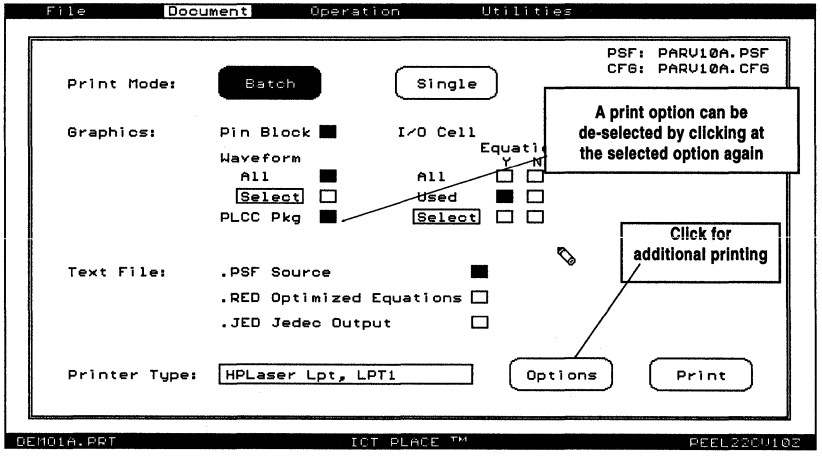

Figure 10-57, Document window for PEEL22CV10A

As shown in the Figures 10-56 and 10-57, the current PSF and CFG files loaded are displayed at the upper-right corner of the window. If these files exist, they will be loaded automatically upon boot-up of the Document operation. However a different PSF design file or simulation waveform CFG file can be read from the "File" menu.

After making the print option selections, the printing is initiated by clicking at the "Print" command located at the lower-right corner of the window. **Remember that a print option can be de-selected by clicking at the selected (highlighted) option again.** Note that all selected print options can be saved via the "Save" or "saveAs" command (as a ".PRT" file) in the "File" menu window.

Print Mode ..... Allows the selection of "Batch" or "Single" printing.
- Single printing allows one graphic screen or text file to be selected and printed at a time.
- Batch printing allows several screens or text files to be selected, each printed out sequentially.

Graphics ..... This option is used to select the graphics screens to be printed, including: Block Diagram Screen "Pin-Block", PLCC package configuration (if applicable), LCC/IOC and GBC graphic screens for PEEL Arrays or IOC graphic screens for PEEL Devices and the CFG waveform screens. In addition, the logic equations for the LCC or IOC may be appended to each printed design configuration graphic screen .

To select a graphic screen, click at the print option box until it is highlighted. The equation (Y/N) selection includes or excludes the equations for each LCC/IOC or IOC screen.

- **Pin Block:** Selects the pin block diagram for printing. The pinout will be in DIP configuration for all devices except for the PA7140 device which will be in PLCC configuration.
- **Waveform:** Allows waveform screens to be selected for printing.
  - All: Selecting "All" will print all waveforms.
  - Select: Selecting the "Select" option allows specific waveform screen to be chosen for printing. See to section 10.23 for more information.
- **LCC / IOC (PEEL Arrays) or IOC (PEEL Devices):** Allows the design cell configuration screens to be selected for printing. For PEEL Arrays, the LCC/IOC screens will be printed. If it is a PEEL device, then the IOC screens will be selected for printing.
  - All: Selects all cells (LCC/IOC for PEEL Arrays and IOC for PEEL Devices) for printing.
  - Used: Selects only used or labeled cells for printing.

Select: Allows specific cells to be selected for printing. Refer to section 10.24 for more information.

- **Global Cell (PEEL Arrays only):** Selects all global cells for printing. The equation (Y/N) selection includes or excludes the equations for each Global Cell screen.

Text File..... Selects the PSF design source file, the RED compiled reduction file which contains the reduced equations from the PLACE optimizer, and the JEDEC file for printing.

Printer Type .... Selects printer type and set-up. Refer to section 10.25.

Options ..... Selects additional printing options (Figure 10-58).

- **Waveform Zoom:** Sets whether the waveform screens to be printed are in the normal or zoom screen mode.
- **Print to file:** Redirects all printer outputs to a file. The file name will be prompted for immediately after selecting this option.
- **COM Rdy Handshake (Postscript printer only):** If sets to the ON condition, the PLACE software waits for an end-of-job character (ASCII# 4) from the printer after sending each graphic screen. If set to the OFF condition, the PLACE software continues to the next print job without waiting for an answer from the printer. The PLACE software utilizes the XON/XOFF handshake signals when communicating with the postscript via the COM port. **It is recommended to set to the OFF condition if a printer buffer or spooler is used.**

Print..... Initiates the printing with the currently selected options.

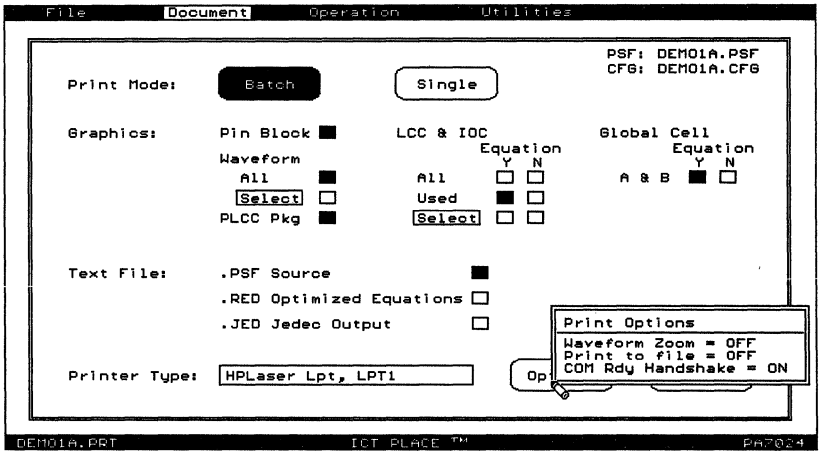

Figure 10-58, "Options" command

10.23 Document Operation - Waveform "Select" Print Option

The waveform "Select" option allows specific waveform screens to be selected for printing. Figure 10-59 shows the waveform "Select" screen.

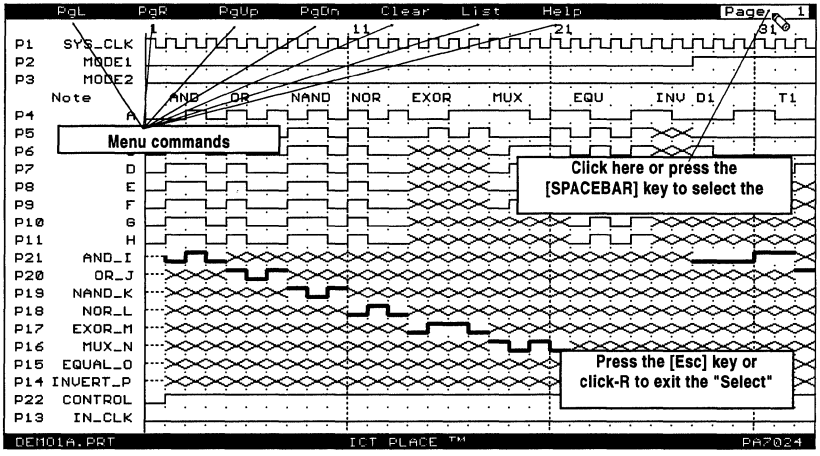

Figure 10-59, Waveform "Select" screen

Selecting a screen ..... A waveform screen can be selected by pressing the [SPACEBAR] key or clicking at the page number located at the upper-right corner of the screen. Once selected, the page number of the screen will be highlighted. For a list of selected waveform screen, click at the "List" command.

PgL or
Left cursor key.... Pages the screen to the left.

PgR
Right cursor key .. Pages the screen to the right.

PgUp or
Up cursor key or
[PgUp] key ..... Pages the screen up.

PgDn or
Down cursor key or
[PgDN] key ..... Pages the screen down.

List..... Lists all the selected waveform page numbers.

Help..... Displays the Help screen.

10.24 Document Operation - LCC/IOC or IOC "Select" Option

In PEEL Arrays, the LCC and IOC "Select" screen allows specific LCC/IOC pairs to be selected for printing. The selection is made by clicking at the LCCs or IOCs and the LCC/IOC pairs will be highlighted. In PEEL devices, the IOCs are selected with the similar method, i.e. clicking at the IOCs until highlighted.

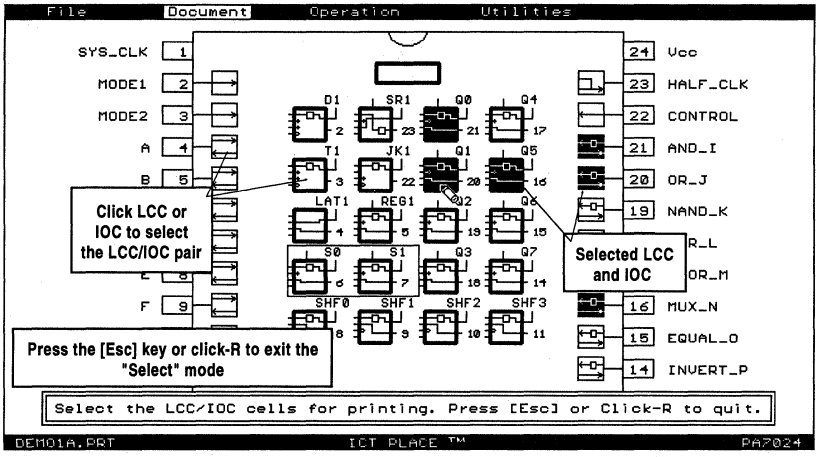

Figure 10-60, LCC/IOC "Select" screen for PA7024

10.25 Document Operation - Printer Type Selection

Unlike the "Print" command in the "File" menu window of the Design, Compile, Simulate and Program operations (in which only the IBM and Epson graphic printers are supported), several popular printers are supported in the Document operation. These printers include IBM, Epson, HP Laserjet II and Postscript laser printers.

If you are setting up the Document operation for the first time, then you will need to configure the printer type and set-up. Once configured, the printer type and its set-up will automatically be loaded each time the Document operation is selected.

After opening the "Print" window as shown in Figure 10-61, select the "Type" option to choose your printer type. Note that the printer type selection also sets the type of interface (parallel or COM) used. The "Set-up" option sets the parameters of the selected printer interface.

Type..... Printer with the type of interface (parallel or COM) used.

- **IBM:** Sends the printer outputs in IBM printer command format via the parallel port.
- **Epson:** Sends the printer outputs in Epson printer command format via the parallel port. Both IBM's and Epson's command format are very similar to each other.
- **HPLaser Lpt:** Sends the printer outputs in HP Laserjet II printer command language via the parallel port.
- **HPLaser Ser:** Sends the printer outputs in HP Laserjet II printer command language via the serial communication port (COM port).
- **Postscript:** Sends the printer outputs in Postscript printer command language via the serial communication port (COM port). Uses the XON/XOFF handshake signals. For more information, refer to section 10.22 for the description of the "Options" menu.

Set-up ..... Allows the printer interface to be configured. To make the set-up selections, click at the options in the "Printer Setup" window until the desired selection appears. Then, press the [Esc] key or click-R to return to the "Print" pop-up window.

- **Parallel port (LPT):** Allows the port number LPT1, LPT2 or LPT3 to be selected.
- **COM:** Allows the port number COM1 or COM2, baud rate, data size, stop bits and parity to be selected.

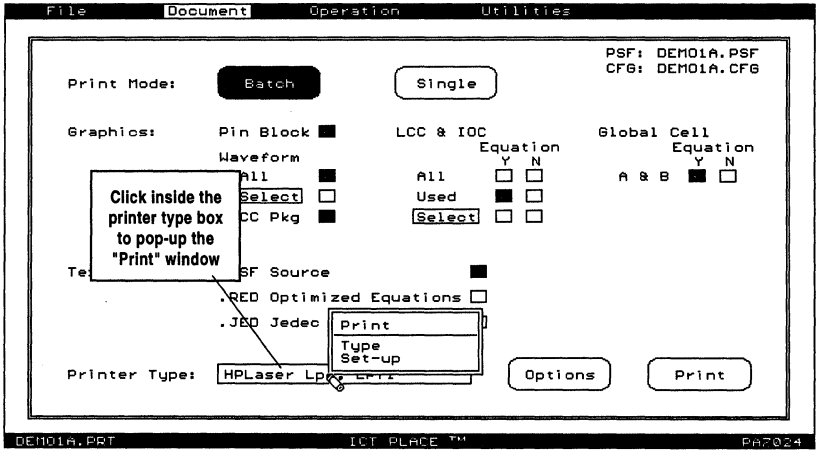

Figure 10-61, Setting the printer type and set-up

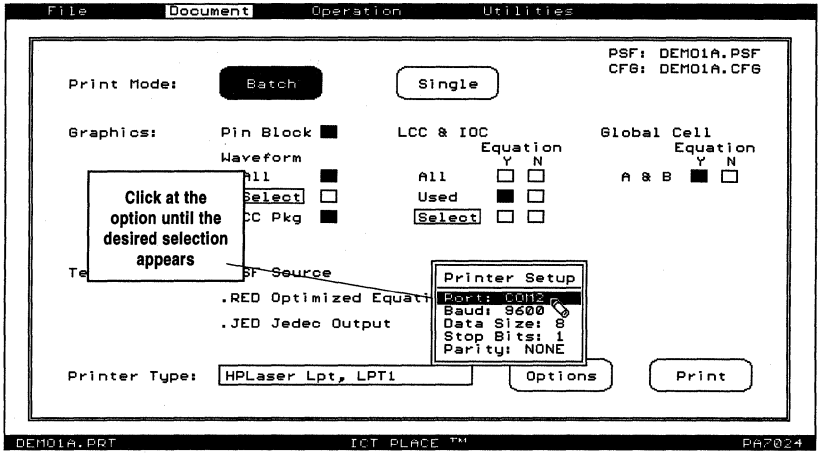

Figure 10-62, "Printer Setup" window

10.26 Program Operation

If using a PDS series programmer (PDS-1, PDS-2, PDS-3) refer to the PDS user's Manual for information on program operation

10.27 Program Operation - Serial Communication Window

The "PC Com" Interface window is automatically displayed if the ICT PDS series programmer is not installed in your computer. The commands in this window allow the JEDEC file to be transmitted or received via the COM port to or from a third-party programmer which has a serial communication file transfer utility.

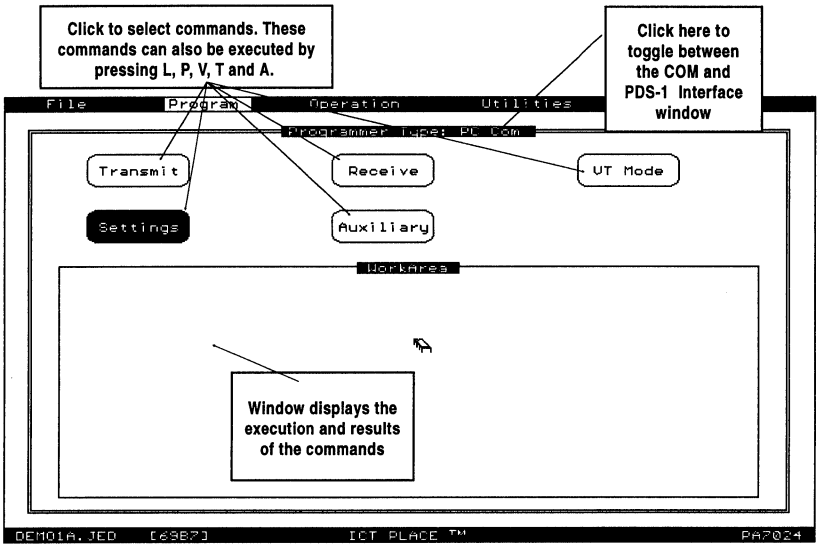

Figure 10-65, "PC Com" Interface window

If the JEDEC file with extension ".JED" exists (i.e. successful compilation of the PSF design file), then it will be loaded into the memory automatically upon boot-up of the Program operation. Otherwise, the JEDEC file can be read via the "File" menu.

Programmer Type..... The "Programmer Type" box allows selecting between two programmer interfaces, the PDS-1 or COM port. This feature is activated only if a PDS-1 programmer is installed in the computer.

Upload..... Sets computer to receive JEDEC file from the serial communication (COM) port.

Download ..... Sends currently loaded JEDEC file to the serial communication (COM) port.

VT Mode ..... Sets video terminal emulation mode with current settings. See "Settings" below.

Settings..... Allows communication port parameters such as baud rate, data bits, parity, stop bits, and serial COM port number to be selected.

Auxiliary..... Selects Auxiliary functions such as

- **Space Bar:** If set to ON, the last command will be executed in the main window. For instance, if the last command was the Program command, then pressing the [SPACEBAR] key will repeat this command.
- **Auto-secure:** If set to ON, the JEDEC field "G1" is added to the JEDEC file in the memory. This field enables the security bit programming in the PLD programmer. Note that some programmers will override this option and require you to turn the security bit programming manually.
- **Read Signature:** Reads the Signature word of the JEDEC file in memory.
- **Write Signature:** Allows the Signature word to be added into the JEDEC file in the memory.
- **Compute Checksum**: Computes the check sum of the JEDEC file in memory.

To view the current JEDEC file

The current JEDEC file in the memory can be analyzed using the "Editor" command in the "Utilities" menu window. Once in the editor, all the features and functions available in the editor of the Design or Compile operation are applicable here. Refer to section 10.28. **Press the [Esc] key or click-R to return to the previous screen.**

10.28 PLACE Text Editor

Figure 10-66 shows the PLACE text editor (a Wordstar™-like editor) that is used in the Design, Compile and Document operations. In the Design operation, the text editor is primarily used for entering or modifying the logic descriptions of the design. In the Compile operation, the editor is interfaced closely with the PLACE compiler. If a compilation syntax error is encountered, the editor opens automatically and displays the line with the error. If possible, this error can then be analyzed and modified without returning to the Design operation. In the Document operation, the editor is mainly used for displaying the JEDEC file.

Using mouse in the editor

The PLACE text editor supports some of the editor commands via the mouse. As shown in Figure 10-66, press and hold the middle or right button of the mouse (the button depends on whether a 2 or 3-button mouse is used) to enter the mouse mode. Once in the mouse mode, no text editing can be done. Instead, only screen paging and scrolling, and cursor movement can be performed (Figure 10-67). To exit the mouse mode, release the left button of the mouse. The best application of the mouse is to quickly move the editor cursor to another location.

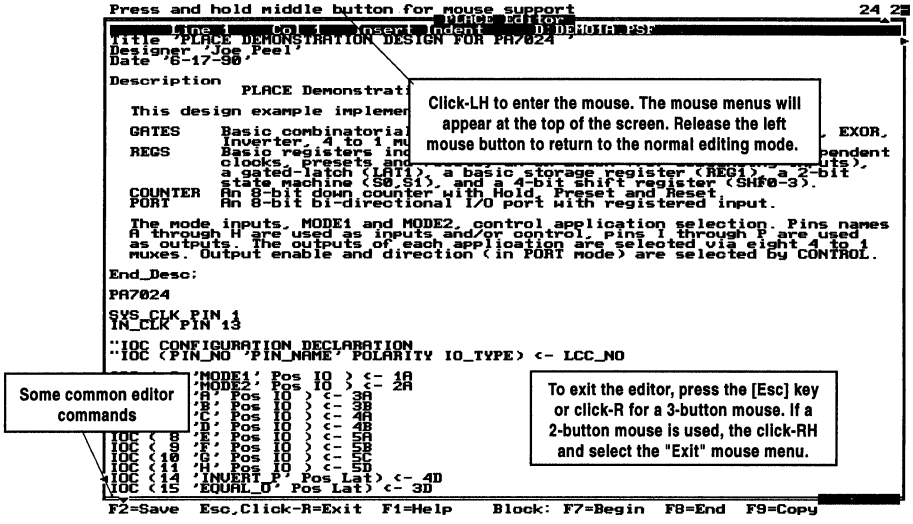

Figure 10-66, PLACE text editor

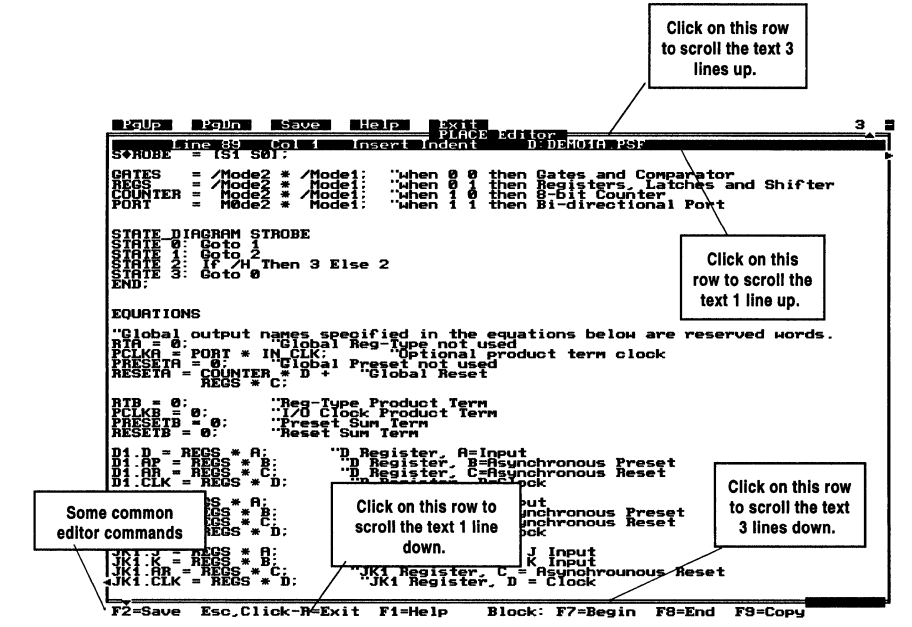

Figure 10-67, Mouse mode in the PLACE Text Editor

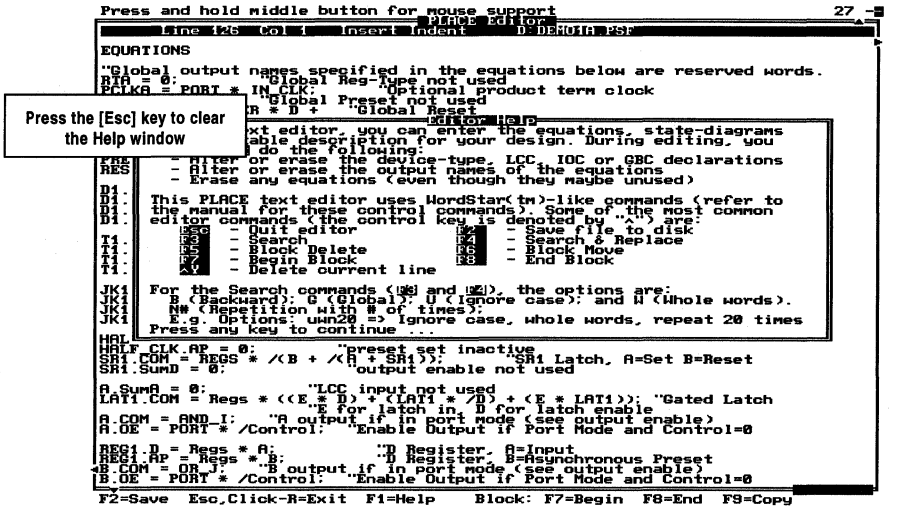

Figure 10-69, Help screen in the editor

Text Editor Keyboard Commands

Screen and cursor movement

Functions	Commands
Character left	^S or Left arrow key
Character right	^D or Right arrow key
Word left	^A or ^-Left-arrow key
Word right	^F or ^-Right arrow key
Line up	^E or Up arrow key
Line down	^X or Down arrow key
Scroll up	^W or ^-Up-arrow key
Scroll down	^Z or ^-Down-arrow key
Page up	^R or [PgUp] key
Page down	^C or [PgDn] key
Top of file	^QR or ^-[PgUp] key
End of file	^QC or ^-[PgDn] key
Begin of line	^QS or [Home] key
End of line	^QD or [End] key
Top of screen	^QE or ^-[Home] key
Bottom of screen	^QX or ^-[End] key
Top of block	^QB
Bottom of block	^QK
Previous cursor	^QP
Jump marker 0..3	^Q0..^Q3
Set marker 0..3	^K0..^K3

Insert and delete

Functions	Commands
New line	^M or [Enter] key
Insert line	^N
Tab	^I or [Tab] key
Delete current character	^G or [Del] key
Delete character left	^H or [Backspace] key
Delete word	^T
Delete to end of line	^QY
Delete line	^Y

Block Functions

In the Design operation, the PLACE software selects and highlights a block of text automatically when the editor is opened via the PSF Text Display windows. If desired, specific text can be manually "blocked" via the [F7] and [F8] function keys. This is done by first moving the editor cursor to the location which marks the beginning of the block and then press the [F7] key. Then, move the cursor to the "end" location of the block and press the [F8] key. A block is selected if it is highlighted.

Functions	Commands
Begin block	^KB or [F7] key
End Block	^KK or [F8] key
Copy block	^KC
Move block	^KV
Delete block	^KY
Hide block	^KH
Mark single word	^KT
Read block from file	^KR
Write block to file	^KW
Print block	^KP

Miscellaneous

Functions	Commands
Exit editor	^KQ or [Esc] key
Save and Open new file	^KD
Toggle insert mode	^V or [Ins] key
Toggle autoindent	^OI
Toggle fixed tabs/smart tabs	^OF
Restore line	^QL
Search string	^QF
Search and replace string	^QA
Repeat last search operation	^L

PLACE Design Language

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PLACE Design Language

11

11.0 PLACE Design Language

11.1 Introduction

To simplify the design entry process, the PLACE software allows control of the architectures graphically. This capability allows the user to better utilize his or her time on the actual design implementation and not on architectural syntax found in most other PLD software tools. Underneath the graphics however, the PLACE software incorporates a powerful design language that provides standard behavioral design methods such as State Diagrams, Truth Tables and Equations.

PLACE Source File Format

Figure 11-1 shows the format of the PLACE Source File (PSF). Figures 11-2 and 11-3 illustrate the differences between the PSF formats for the PA7024 and PEEL18CV8 devices. **Note: All format categories in figure 11-1 that are shaded are automatically set-up via the PLACE architectural editor.**

Design Description:	*Title of the design, name of designer, date and detailed description of the design.*
Device type:	*PA7024, PEEL18CV8, PEEL22CV10A, and etc.*
Special features:	*Sets Security-bit, Zero-Power or Signature Word.*
Input or Clock Pins:	*Assigns names to the clock and dedicated input pins.*
Cell Configurations:	*PEEL Arrays: IOC and LCC Configurations.* *PEEL Devices: IOC (Macro Cell) Configurations.*
Global Configurations:	*PEEL Array: Group A and B Global Cell Configurations.* *PEEL Devices: Asynchronous and Synchronous node definitions for registered PEEL Devices (e.g. PEEL18CV8, PEEL22CV10A, etc.).*
Comments	Details the description of the design.
Macro Definitons:	State assignments, equation and constant declarations.
State-diagrams **Truth-tables** **Equations**	

Figure 11-1, PLACE Source File Format

While reading the PSF file, the PLACE software checks the file format for incompatibilities. If any format incompatibilites are found for the selected device type, the PLACE software will display error messages.

```
TITLE ' '
Designer ' '
Date ' '

Description
      Enter description here ...
End_Desc;

PA7024                          "Device type

"Optional Special Features Identifiers
AUTO_SECURE                     "Programs the security bit. If unspecified,
                                "defaults to  Security-bit OFF
SIGNATURE 'ABCDEFGH'            "Programs Signature Word  'ABCDEFGH'

CLK1 PIN 1                      "Input or Clock pin declaration
CLK2 PIN 13

IOC ( 2 "POS IO ) <- 1A         "IOC Declaration
IOC ( 3 " POS IO ) <- 2A
IOC ( 4 " POS IO ) <- 3A
IOC ( 5 " POS IO ) <- 4A
IOC ( 6 " POS IO ) <- 5A
IOC ( 7 " POS IO ) <- 1B
IOC ( 8 " POS IO ) <- 2B
IOC ( 9 " POS IO ) <- 3B
IOC (10 " POS IO ) <- 4B
IOC (11 " POS IO ) <- 5B
IOC (14 " POS IO ) <- 1C
IOC (15 " POS IO ) <- 2C
IOC (16 " POS IO ) <- 3C
IOC (17 " POS IO ) <- 4C
IOC (18 " POS IO ) <- 5C
IOC (19 " POS IO ) <- 1D
IOC (20 " POS IO ) <- 2D
IOC (21 " POS IO ) <- 3D
IOC (22 " POS IO ) <- 4D
IOC (23 " POS IO ) <- 5D
```

Figure 11-2, PA7024 "ANEW7024.PSF" File Template

```
LCC (1A " D  POS  REG  REG )    "LCC Declaration
LCC (2A " D  POS  REG  REG )
LCC (3A " D  POS  REG  REG )
LCC (4A " D  POS  REG  REG )
LCC (5A " D  POS  REG  REG )
LCC (1B " D  POS  REG  REG )
LCC (2B " D  POS  REG  REG )
LCC (3B " D  POS  REG  REG )
LCC (4B " D  POS  REG  REG )
LCC (5B " D  POS  REG  REG )
LCC (1C " D  POS  REG  REG )
LCC (2C " D  POS  REG  REG )
LCC (3C " D  POS  REG  REG )
LCC (4C " D  POS  REG  REG )
LCC (5C " D  POS  REG  REG )
LCC (1D " D  POS  REG  REG )
LCC (2D " D  POS  REG  REG )
LCC (3D " D  POS  REG  REG )
LCC (4D " D  POS  REG  REG )
LCC (5D " D  POS  REG  REG )

Global = 1                      "Number of global cells used
GBC (A Clk1 Clk1)               "Global Cell A configuration
GBC (B Clk1 Clk1)               "Global Cell B configuration

DEFINE                          "Macro Definitions

STATE_DIAGRAM SD_name           "State diagram design syntax
END;                            "Ends current State diagram syntax

TRUTH TABLE TT_name             "Truth table design syntax
END;                            "Ends current State diagram syntax

EQUATIONS                       "Logic equation syntax

"Equations for the Global Cell A
RTA = 0;                        "Reg-Type Product Term
PCLKA = 0;                      "IOC Clock Product Term
PRESETA = 0;                    "Preset Sum Term
RESETA = 0;                     "Reset Sum Term

"Equations for the Global Cell B
RTB = 0;                        "Reg-Type Product Term
PCLKB = 0;                      "IOC Clock Product Term
PRESETB = 0;                    "Preset Sum Term
PESETB = 0;                     "Reset Sum Term
```

Figure 11-2, PA7024 "ANEW7024.PSF" File Template (Continued)

```
TITLE ' '
DESIGNER ' '
DATE ' '

Description
     Enter description here ...
End_Desc;

PEEL18CV8                          "Device type

"Optional Special Features Identifiers
AUTO_SECURE                        "Programs Security-bit. If unspecified,
                                   " defaults to security-bit OFF

CLK pin 1                          "Input or Clock pin declaration

IOC (12 " POS COM FEED_PIN )       "I/O  or Macro Cell Configuration
IOC (13 " POS COM FEED_PIN )
IOC (14 " POS COM FEED_PIN )
IOC (15 " POS COM FEED_PIN )
IOC (16 " POS COM FEED_PIN )
IOC (17 " POS COM FEED_PIN )
IOC (18 " POS COM FEED_PIN )
IOC (19 " POS COM FEED_PIN )

AR NODE 21                         "Global Asynchronous Reset  Node
SP NODE 22                         "Global Synchronous Preset Node

DEFINE                             "Macro Definitions

STATE_DIAGRAM  SD_name             "State diagram design syntax
END;                               "Ends current State diagram syntax

TRUTH TABLE  TT_name               "Truth table design syntax
END;                               "Ends current State diagram syntax

EQUATIONS                          "Logic equation syntax

"Equations for the global nodes
AR = 0;                            "Global Asynchronous Reset Equation
SP = 0;                            "Global Synchronous Preset Equation
```

Figure 11-3, PEEL18CV8 "ANEWV8.PSF" Template File

11.2 Design Description

The design description section of the PSF format is made up of four fields. The fields include: Title of the design; Designer's name; Date of the design; and a detailed description of the design.

☞ In describing the PSF formats for the following sections (including this one), *italics* will be used to identify fields in which the user would enter identifiers, such as title and date of the design, name of the designer, pin names, and etc. The reserved identifiers will be specified in **bold**. Most of the examples used for illustrating the formats (except for the PEEL device formats) are taken from the Blackjack Machine Application Example (JACK7024.PSF) illustrated in section 12.7. **All reserved identifiers and labels are not case sensitive.**

Title

Format: **Title** *'title of design'*

Example: Title 'Blackjack Machine Example'

Only the characters between the ASCII 32 and 127 can be used in specifying the title of the design. The maximum length of the title is 69 characters.

☞ The characters between the ASCII 32 and 127 are normal characters. These characters include A..Z, a..z, 0..9, space, !, ", $, %, &, ', (,), *, +, ,, -, ., /, :, ;, <, =, >, ?, @, [, \,], ^, _, ‘, {, |, }, and ~.

Designer

Format: **Designer** *'name of the designer'*

Example: Designer 'Joe Peel'

Like the Title identifier, only characters between the ASCII 32 and 127 can be used. The maximum length of the designer's string is 47 characters.

Date

Format: **Date** *'date of design'*

Example: Date 'May 10th, 1991'

Characters valid in the date string are between ASCII 32 and 127. The maximum string length is 47 characters.

Description

The Description identifier allows the user to specify in detail the description of the design. The user specifies his or her description within the reserved identifiers **"Description"** and **"End_Desc;"**. These identifiers are automatically inserted by the PLACE software.

Format: **Description**
enter description of design here ...
End_Desc;

Example:
```
Description
        Blackjack Machine Example

        This design example was based on C.R. Clare's design
        in Designing Logic Systems Using State Machines
        (McGraw Hill, 1972). The blackjack machine plays ....

        All ASCII characters can be used here.

        End_Desc;
```

All PLACE reserved words except "End_Desc" can be used within the "Description" and "End_Desc" identifiers. Each line does not need to begin with a double quotation mark, as required in the Comments field (section 11.9).

11.3 Device Type

The target device of the design is declared by simply entering the ICT PEEL device name.

Format: *device_type*

The following are the device types supported in Version 2.4 of the PLACE software.

PA7024	**PEEL22CV10A**	**PEEL18CV8**
PA7140	**PEEL22CV10A+**	
PA7128		

11.4 Special Features

The special features such as enabling the Security Bit, programming the Signature Word, and setting the Zero Power Bit are available for some of the PEEL devices. These features are optional, meaning that they are not required to be specified in the PSF file. If not specified, the default conditions will be implemented. Refer to the description of each of these features for their default conditions.

Security Bit

Once the security bit feature is enabled, the programmed data in the device (except for the Signature Word) is prevented from being loaded or read, and hence prevents any unauthorized copying of the design in the PEEL device.

The security bit feature is available for the following devices.

PA7024 **PEEL18CV8**
PA7140 **PEEL22CV10A+**
PA7128 **PEEL22CV10A**

Format: **AUTO_SECURE**

The security bit of the device is enabled via the reserved identifier **AUTO_SECURE**. If this identifier is specified in the PSF file, the PLACE Compiler will create a JEDEC file with the security bit enabled (sets the "G1" field). In most PLD programmers, the "G1" field automatically enables the security bit programming.

Default condition: AUTO_SECURE identifier is unspecified. The JEDEC file generated will not have the "G1" field. In most PLD programmers, the user can enable or disable the security bit programming.

Signature Word

The signature word of the device allows a user to enter a design revision number so that the design can be identifed after the security bit of the PEEL device is enabled. Hence, the signature word data can still be loaded even after the security bit of the device is enabled.

The signature word feature is supported in the following devices. Note that the number of 8-bit bytes in the signature word is specified within the parenthesis.

PA7024 (8 bytes) **PA7140 (2 bytes)**
PA7128 (1 byte)
PEEL22CV10A+ (3 bytes)

Format: **SIGNATURE** *'signature str'*

Example: Signature 'REV. A'

Default condition: SIGNATURE identifier is unspecified, which means that the signature word in the device JEDEC file is unused. Note that if the ICT PDS-1 programmer is present, this signature word can be programmed in the Program operation.

11.5 Clock and Input Pins

After labelling a clock or a dedicated input pin (pin that is not associated to an Input Cell or INC) of the device using the "**Label**" command in the Design operation, the PLACE software automatically creates the pin assignment statement.

Format: *pin_label* **PIN** pin_number

Example: CLK1 pin 13

Please refer to section 11.6 for the pin label format.

Default condition: Unlabeled pin (no pin assignment statement) signifies that the pin is unused.

11.6 Pin and Cell Labels

Format: First character: **A..Z, a..z, ~, /, !**
Body of the label: **A..Z, a..z, 0..9, ~, _**

Examples: Valid labels: Addr10, ~10, /OUT
Invalid labels: _Add, 25MHz, /15IN

The label is not case sensitive. The maximum length of the label is 8 characters (including the / or ! character). **When a / or ! character is added at the beginning of the label, the pin, cell or node becomes an active Low signal path.** Hence, a TRUE logic (logic "1") is resulted when a Low signal is applied.

Example:

```
/A pin 1          "Active Low Input
B pin 2           "Active High Input

IOC (12 'C' Pos COM Feed_pin)      "Output Polarity = Pos
IOC (13 'D' Neg COM Feed_pin)      "Output Polarity = Neg
IOC (14 '/E' Pos COM Feed_pin)     "Output Polarity = Pos
IOC (15 '/F' Neg COM Feed_pin)     "Output Polarity = Neg

EQUATIONS
C.COM = A;        "C=TRUE or 1 when A=LOW
D.COM = B;        "D=TRUE or 1 when B=HIGH
```

The / or ! on the pin or cell labels only affect the active level of the inputs or feedback paths (i.e. variables on the right side of the equal sign in the equations). The polarity of the outputs (i.e. outputs routed to the external pins) are not affected because they are controlled by the IOC configuration statements. In the above example, the feedback active levels and output polarities of cells C, D, E, and F are:

Cell	Feedback Active Level	Output Polarity
C	High	High
D	High	Low
/E	Low	High
/F	Low	Low

11.7 Cell Configurations

The cell configuration format statements are used to specify the type of configuration of each cell in the selected device. In most cases, knowledge of the cell configuration formats is not necessary because the configurations of the IOC and LCC are automatically modified by the PLACE architectural software.

Note that all the configuration statements are necessary for the operation of the PLACE software. This means that **you should not delete any of these configuration statements** including the configuration statements for unused cells.

Format:

Input Cell in PA7140 and PA7128:

INC (pin_number *'pin_label'* input_type)

Example: INC (3 'A1' Reg)

I/O Cell in PEEL Arrays:

IOC (pin_number *'pin_label'* output_pol pin_type) <- Assigned_LCC

Example: IOC (4 'V4' Pos IO) <- 3A

Logic Control Cell in PEEL Arrays only:

LCC (cell_number *'cell_label'* flip-flop_type clock buried_out ext_out)

Example: LCC (1A 'ADD10' D SumC Reg Reg)

I/O Cell (or Macro Cell) in PEEL devices:

IOC (pin_number *'pin_label'* output_pol pin_type feedback_type)

Example: IOC (12 'OUT' POS COM FEED_PIN)

Default condition: The default cell configurations are set by the cell configuration statements in the "ANEWxxxx.PSF" files. If the "**New**" function under the File menu command in the Design operation is selected, the PLACE software reads the ANEW file for the selected device (see Table 11-1) and sets the default configurations found in the file.

ANEW File	Device
ANEW7024.PSF	PA7024
ANEW7140.PSF	PA7140
ANEW7128.PSF	PA7128
ANEWV8.PSF	PEEL18CV8
ANEWV10A.PSF	PEEL22CV10A
ANEWV10P.PSF	PEEL22CV10A+

Table 11-1, PLACE ANEW Template Files

Parameters for the INC Format (PA7140 and PA7128 only)

Pin_Number — The pin number that is assigned to the current Input cell.

Device	INC Pin Numbers
PA7140 (PLCC)	3-5, 19-21, 25-27, 41-43
PA7128	2-6, 8-14

Pin_Label — See section 11.6 for the format of the pin label.

Input_type — The identifiers for the pin type parameter are:

Identifier	Function
COM	Combinatorial input
REG	D-type registered input
LAT	D-type latched input

Parameters for the IOC Format (PEEL Arrays only)

Pin_Number — The pin number that is assigned to the current I/O cell.

Device	IOC Pin Numbers
PA7024	2-11, 14-23
PA7140 (PLCC)	6-16, 18, 28-38, 40
PA7128	15-20, 22-27

Pin_Label — See section 11.6 for the format of the pin label.

Output_pol

This parameter which refers to the output polarity of the pin is controlled by the following identifiers:

Identifier	Function
POS	Positive Polarity for the Output
NEG	Negative Polarity for the Output

The output polarity "bubble" in the Design operation of the PLACE software controls this parameter. **Inserting the / or ! character in the pin_label does not affect the output (section 11.6).**

Pin_type

The identifiers for the pin type parameter are:

Identifier	Function
IO	I/O
REG	I/O with D-type registered input
LAT	I/O with D-type latched input
OUT	Output only
INCOM	Input only
INREG	Input only with D-type register
INLAT	Input only with D-type latch
OUTREG	Output only with D-type registered feedback
OUTLAT	Output only with D-type latched feedback
DCOM	Output only with feedback from Sum-D
DREG	Output only with D-type registered feedback from Sum-D
DLAT	Output only with D-type latched feedback from Sum-D

The parameters DCOM, DREG and DLAT are only applicable for PA7140 and PA7128 devices.

Assigned_LCC

The LCC that is connected to the current IOC.

Parameters for the LCC Format (PEEL Arrays only)

Cell_number

The cell number that is assigned to the current Logic Control cell. It ranges from 1A-6A, 1B-6B, 1C-6C and 1D-6D. Figure 11-4 illustrates the cell number organization for the PA7024 device.

Device	LCC Assignments
PA7024	1A-5A, 1B-5B, 1C-5C, 1D-5D
PA7140 (PLCC)	1A-6A, 1B-6B, 1C-6C, 1D-6D
PA7128	1A-3A, 1B-3B, 1C-3C, 1D-3D

Refer to the IOC statement described in the previous section for the assigned IOC for each LCC.

Cell_label

Refer to section 11.6 for the cell label format.

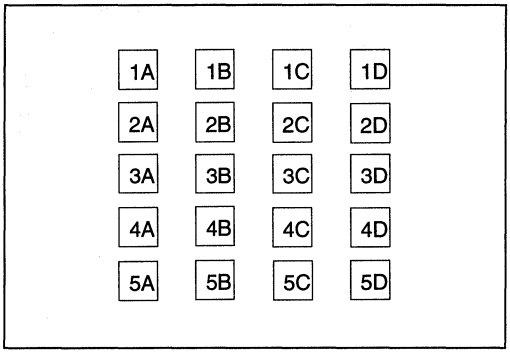

Figure 11-4, LCC numbering syustem in PA7024

Flip-flop type

Specifies the type of register in the LCC. The dynamic register type setting (RT signal) is also specified in this parameter. The RT signal which comes from the Global Cell dynamically changes the register type in the LCC during normal (5V) operation.

Identifier	Function
D	D-type register (RT mode is disabled)
T	T-type register (RT mode is disabled)
JK	JK-type register (RT mode is disabled)
DT	D-type register when RT= FALSE, T-type register when RT = TRUE
DJK	D-type register when RT = FALSE, JK-type register when RT = TRUE
TD	T-type register when RT = FALSE, D-type register when RT = TRUE
JKD	JK-type register when RT = FALSE, D-type register when RT = TRUE

Clock

Controls the type of clock for the current LCC.

Identifier	Function
POS	High speed (system) clock from pin 1 or 13 that triggers the register on the rising edge. Note: Global cell controls which pin to use for system clock
NEG	Register is triggered on the falling edge of the system clock
SumC	Local clock coming from the Sum C term. Register is triggered on the rising edge of the clock signal
SumD	Local clock coming from the Sum D term. Register is triggered on the falling edge of the clock signal

Buried_Out — Output of the LCC that is fed back internally to the array.

Identifier	Function
Reg	Internal output from the output of the register
SumA	Internal output from the Sum A term (i.e. the input of the register)
SumB	Internal output from the Sum B term
SumC	Internal output from the Sum C term

Ext_Out — Output of the LCC which is connected to the I/O cell. This output sends the signal of the device to the outside world. The final output signal depends on the output polarity of its assigned IOC.

Parameters for the IOC Format (PEEL Devices)

Pin_Number — The pin number that is assigned to the current I/O cell. Below lists the PEEL I/O pin numbers.

Device	I/O Pin Numbers
PEEL18CV8 PEEL22CV10A, PEEL22CV10A+,	12 - 19

Pin_Label — See section 11.6 for the format of the I/O pin label.

Output_pol — This parameter which refers to the output polarity of the pin is controlled by the following identifiers:

Identifier	Function
POS	Positive Polarity for the Output
NEG	Negative Polarity for the Output

The output polarity "bubble" in the PLACE architectural software controls this parameter. Inserting the / or ! character in the pin_label does not affect the output (section 11.6). Hence, only this parameter controls the polarity of the output.

Pin_type — The identifiers for the pin type parameter are:

Identifier	Function
COM	I/O with combinatorial output
REG	I/O with D-type registered output
OUTCOM	Combinatorial output only
OUTREG	Registered output only
IN	Output disabled (May or may not be an input depending on the feedback type)

Note that only the PEEL18CV8, 22CV10A and 22CV10A+ have output registers.

Feedback_type — Specifies the type of feedback for the selected device. This parameter is only applicable for devices such as PEEL18CV8 and 22CV10A+. The feedback types of the 22CV10A are automatically set to FEED_PIN and FEED_REG for COM and REG output types respectively.

Identifier	Function
FEED_PIN	Feedback from the pin
FEED_REG	Feedback from the output of the register
FEED_OR	Feedback directly from sum term (i.e. prior to the register)

11.8 Global Configurations

PEEL Arrays

The global configurations for PEEL Arrays are used to set up the global signals for the LCCs, IOCs and INCs.

Format:

```
Global = n                          "n = 1 or 2 cells
GBC (A  LCC_clock  IOC_clock)       "Global Cell A
GBC (B  LCC_clock  IOC_clock)       "Global Cell B
GBC (C  ___  INC_clock)             "Global Cell C
                                    "(PA7140 and
                                    "PA7128 only)
```

Example:

```
Global = 1
GBC (A  Clk1  Clk2)
GBC (B  Clk1  Clk2)
GBC(C  ___  Clk1)
```

Table 11-2 shows the definitions of the Clk1, Clk2 and PClk terms used in the GBC configuration statements.

Clk1 and Clk2 terms - specify the system clock pin to use.

Device	Clk1 pin	Clk2 pin
PA7024	1	13
PA7140	2	24
PA7128	1	28

PClk terms - specify to use the product term for the global clock.

Device	IOCs by PClkA	IOCs by PClkB	INCs by PClkC
PA7024	2 - 11	14 - 23	none
PA7140	6 - 16, 18	28 - 38, 40	3-4, 19-21, 25-27, 41-44
PA7128	15 - 20, 22 - 27		2-6, 8-16

Table 11-2, Definitions of global clock terms

Global = n — The **n** parameter equals 1 or 2. This paramter sets the number of global cells to be used for the LCCs and IOCs. If one global cell is used, then global cell A controls the global signals for all LCCs and IOCs in the device and global cell B configuration statement is ignored . If "Global = 2" is specified, then Global Cell A controls the global signals for the IOCs and LCCs in which the IOCs are on the left side of the device. Global Cell B then controls the global signals for the IOCs and LCCs in which the IOCs are on the right side of the device. See Table 11-2.

Below are the descriptions of each parameter in the GBC (GBC A, B or C) configuration statements.

LCC_clock — Sets the system clock pin for the LCC global clock. The two options available are the **Clk1** and **Clk2** pins. Refer to Table 11-2 for the Clk1 and Clk2 pin numbers for each PEEL Array.

IOC_clock — Sets the system clock pin or product term for the IOC global clock. The options available are **Clk1, Clk2**, and **PCLKA or PCLKB.** See Table 11-2.

INC_clock — Sets the system clock pin or product term for the INC global clock. The options available are **Clk1, Clk2** and **PCLKC**. See Table 11-2.

PEEL Devices

In the registered PEEL devices such as PEEL18CV8, 22CV10A, and 22CV10A+, the global configurations are represented by the global node assignments. These global nodes control the asynchronous reset and synchronous preset product terms.

Format: *node_label* **NODE** node_number

Example: AC node 21 "For PEEL18CV8 device

node_label — Please refer to section 11.6 for the node label format.

node_number — The node assignment numbers for the selected device are:

Device	Node Number	Function
PEEL18CV8	21	Asynchronous Reset
	22	Synchronouse Preset
PEEL22CV10A, PEEL22CV10A+,	25	Asynchronous Reset
	26	Synchronouse Preset

11.9 Comments

In the PLACE software, comments are available so that each component of the design which may not be readily apparent from the source file is explained. Comments do not affect the design itself. Liberal use of comments can make a PSF design file easy to understand.

Format: " *Insert comments here ...*

Example: "Enable security bit programming

A comment begins with a double quotation mark (") and ends with the end of line. A comment can be specified anywhere in the PSF design file.

Note that the double quotation marks are not required if the comments are specified within the **"DESCRIPTION"** and **"END_DESC"** reserved identifiers.

11.10 Macro Definitions

The macro definitions are used for:

- declaring constants so to make the design easier to understand.
- declaring commonly used equations so that they need not be repeated throughout the design file.
- assigning the state cells and set variables for state diagram designs.
- assigning the pins or cells for truth table designs.

The macro definitions in the PSF design file are located after the reserved identifier **DEFINE** but prior to one of the following reserved identifiers: **STATE_DIAGRAMS**; **TRUTH_TABLE**; or **EQUATIONS** (whichever is specified first). Macro definitions that are specified via the "Macro" function in the Design operation are automatically inserted into this location.

Format: **DEFINE**
specify macro definitons here...

STATE_DIAGRAMS, TRUTH_TABLE or **EQUATIONS**

Example:

```
DEFINE
QSTATE = [ADD10 SUB10 Q2 Q1 Q0]      "State_Diagram Assignment
Clear          = ^B00000             "Constant Declaration
ShowHit        = ^B00001
AddCard        = ^B11011
Add_10         = ^B10010
Wait           = ^B00010
Test_17        = ^B00110
Test_22        = ^B00111
```

```
ShowStand     = ^B00101
ShowBust      = ^B00100

is_Ace = !V4 & !V3 & !V2 & !V1 & V0;          "Equation Declaration

SCORE = [S4 S3 S2 S1 S0]                      "Truth table input assignment
BCD2  = [D5 D4]                               "Truth table ouput assignment
BCD1  = [D3 D2 D1 D0]                         "Truth table output assignment

STATE_DIAGRAM  QSTATE      "Ends the Macro Definitions
```

Macro Constants

Format: *Const_label = constant*

Examples:
```
Clear  = ^B00000
ShowHit = ^B00001
```

Const_label — The format for the label of the constant is similar to that of the pin or cell label (see section 11.6) with two exceptions, and they are:

1. The length of the label can be up to 20 characters long instead of 8.
2. The / or ! character cannot be used at the beginning of the label.

Constant — Specifies the value of the constant in decimal, hexadecimal, octal or binary numbering system.

The format for the constant is:

symbol + number

The symbols for the numbering systems are:

Numbering system	Symbol
Decimal	none (default)
Hexadecimal	^H or ^h
Octal	^O or ^o
Binary	^B or ^b

Examples:		
	15	(decimal)
	^HF	(hexadecimal)
	^O17	(octal)
	^B1111	(binary)

Macro Equations

Format: *Eqn_label = complex_eqn*

Example:
```
ls_ACS  =  !V4 & !V3 & !V2 & !V1 & !V0;
```

Eqn_label — The label for the equation macro is similar to that for the label for the macro constant. See previous section.

Complex_eqn Macro equation can be specified using the logic operators (), !, &, # and $ (refer to section 11.13).

The input side of a macro equation (i.e. the right side of the "=" symbol) is made up of pin or cell labels, or labels from other macro equations. Below is an example of a macro equation which is a function of other macro equations.

```
DEFINE
  Mac1 = A & B;                "Macro  level 1
  Mac2 = C # D;                "Macro level 1
  Mac3 = Mac1 $ Mac2; "Macro level 2
```

If the macro equation uses only pin and/or cell labels, then it has one macro level. If it uses **previously defined** macro equation labels in addition to the pin and cell labels, then it has multiple macro levels. The number of macro levels depends on whether the macro equation labels used in the equation are functions of more macro equation labels themselves.

The number of macro levels is limited by the total number of characters (**maximum of 1024 characters**) in the "flattened" macro equation, i.e. the input side of a flattened macro equation consists of only pin and/or cell labels. Note that the additional spaces between the input variables in the macro equation are automatically deleted by the PLACE Compiler. Example: A maximum of 5 macro levels can be used if each (unflattened) equation level has less than 200 characters. **Typically, the maximum macro level is about ten.**

Macro State Cell Assignments for STATE DIAGRAMS

The state cell assignment defines the pin or cell labels to be used by the state diagram design syntax.

☞ The "**Allocate**" command in the "Design" menu window of the Design operation automatically generates the state cell assignment definition and STATE_DIAGRAM design syntax. An example is shown below.

```
DEFINE
QSTATE = [ADD10  SUB10  Q2  Q1  Q0]

STATE_DIAGRAM  QSTATE
  "enter design here ...
END;
```

Format: *state_label* = [Cell1 Cell2 Cell3 ... Celln]

Example: QSTATE = [ADD10 SUB10 Q2 Q1 Q0]

State_label The state label format is similar to that of the pin or cell label (section 11.6). The only exception is that the state

label does not allow the use of the / or ! character at the beginning of the label.

Cell(n) Specifies the cell labels to be used as state cells by the state diagram. A maximum of 24 cells can be allocated as state cells. Each state cell label must be separated by a space. The most and least significant bit of the state cells are the first and last allocated cells respectively in the cell assignment definition, i.e. Cell1 is the Most Significant Bit and Celln is the Least Significant Bit.

Macro Set Variables in State Diagrams

Outputs in a state diagram can be assigned to a set variable so that the logic of these outputs can be specified with a numeric constant. The constant can be specified in a binary, octal, hexadecimal or decimal (default) numbering system.

Format: *set_var = [Cell1 Cell2 Cell3 ... Celln]*

Example:

```
DEFINE
TEST = [T2 T1] "State cell assignment
OUT = [Y3 Y2 Y1 Y0]          "Set variable assignment

STATE_DIAGRAM TEST
 State 0:    OUT = 0;        "Macro Set variable OUT
                             "Y3-0 = 0000
             Goto 1;
 State 1:    OUT = ^HB;                  "Y3-0 = 1011
             Goto 2;
 State 2:    OUT = ^B1100;  "Y3-0 = 1100
             Goto 3;
 State 3:    Goto 0
END;
```

Set_var The format is similar to the state label format used for the state cell assignments.

Celln Specifies the assigned pin or cell label.

The macro set variable equation feature is only available within the state diagram design syntax. Also, **only one macro level is available in the macro set variable assignment**.

Macro Cell Allocation for Truth Tables

The **"Allocate"** command in the PLACE Design operation can also be used to allocate the pins and cells for the truth table design. The pins and cells can be allocated as truth table inputs, truth table outputs or both. If a cell or pin is allocated as the truth table input and output, then it is an I/O. The output of the I/O is then enabled or disabled via the .OE equation.

The following example shows the allocation of the pins and cells for the truth table design "TABLE1".

Example:
```
TRUTH_TABLE  TABLE1
(I4 I3 I2 I1 I0 -> Y5 Y4 Y3 Y2 Y1 Y0)
END;
```

Another method of allocating the pins and cells is through the macro set variable method. The inputs and outputs of the truth table can be assigned to the macro set variables in the DEFINE section. The labels of these macro set variables are then used in the truth table design syntax instead of the pin and cell labels.

Format: *table_label = [Cell1 Cell2 Cell3 ... Celln]*

Example:
```
DEFINE
Input = [I4 I3 I2 I1 I0];
Y_HiBit = [Y5 Y4];
Y_LoBit = [Y3 Y2 Y1 Y0];

TRUTH_TABLE TABLE1
(Input -> Y_HiBit Y_LoBit)
^H15 ->   1     ^HA      "I4-0 = 10101, Y5-0 = 011010
^H16 ->   1     ^HB      "I4-0 = 10110, Y5-0 = 011011
END;
```

Table_label — The format is similar to the state label used for the state cell assignments.

Celln — Specifies the assigned pin or cell label.

Please refer to section 11.12 on "Truth Table Design Syntax" for more information.

Macro Counter Function

COUNTERF is the macro function for designing an up-down, loadable counter. It must be specified in the DEFINE section.

Format: COUNTERF*(Load, Updown, cBits, Type, iBits)*

Example:

```
DEFINE

UPDN_BITS = [Q4 Q3 Q2 Q1 Q0]; "Counting Bits. Q[4-0] can be pin or cell
                               labels.

LOAD_EN = A & B;          "Load Control Equation. Loads when A = TRUE
                          and "B=True.

LOAD_BITS = [L4 L3 L2 L1 L0] "Load Inputs, either pin or cell labels
```

```
UPDN_CON = C & !D;        "Updown Control. If C=TRUE, D=FALSE, it is DOWN
                          "Counter else, it is Up Counter.

COUNTERF(LOAD_EN, UPDN_CON, UPDN_BITS, T, LOAD_BITS);
.
.
.
```

EQUATIONS

Load: 0 = No load function
Pin_Name, Node_Name (Cell_Names),
Macro_defined_label = load control

Updown: 0 = Up Ccount
1 = Down Count
Pin_Name, Node_Name (Cell_Names),
Macro_defined_label = updown control
(True logic for Up Count)

cBits: A Macro-Set-Variable (page 9-22) with at least 2 elements.
This set contains the counting bits which include Pin_Names or Node_Names (Cell_Names).

Type: D = D-type counter
T = T-type counter (uses fewest # of product terms)
(The pins or cells assigned to the macro label in the "cBits" parameter must have the same register type)

iBits: 0 = Non-loadable counter
Macro-Set_Variable = Data bits for loading the counter. This set must have the same number of elments as the cBits. The elements include Pin_Names or Node_Names (Cell_Names). If load=0, then iBits=0.

11.11 State Diagrams

The state diagram language is used to implement state machine designs. In the PLACE software, the state machine design is specified between the "**STATE_DIAGRAM *state_label***" and "**END**" identifiers. These identifiers together with the state cell allocation definition (refer to section 11.10) are automatically created when the LCCs or IOCs are allocated for the state machine via the "**Allocate**" command in the Design operation.

Format:

```
DEFINE
State_label = [Cell1 Cell2 ... Celln]

STATE_DIAGRAM State_label
  STATE state_0: "usually Reset state
  STATE state_1:
     .
     .
  STATE state_n: "last state
END;
```

State_label The state label format is similar to that of the pin or cell label (see section 11.6). The only exception is that the state label does not allow the use of the / or ! character at the beginning of the label.

CellN Specifies the cell labels to be used as state cells by the state diagram. A maximum of 24 cells can be allocated as state cells. Each state cell label must be separated by a space. **The most and least significant bit of the state cells are the first and last allocated cells respectively, i.e. Cell0 and CellN are MSB and LSB respectively.**

State_n Specifies the state number which can be in the form of a numeric value or a constant label defined in the DEFINE section. Refer to "Macro Constants" in section 11.10.

The PLACE state diagram syntax includes:

- **GOTO**
- **IF-THEN-ELSE**
- **CASE-ELSE-ENDCASE**
- **WITH-ENDWITH;**
  (used in conjunction with GOTO, IF-THEN-ELSE and CASE-ELSE-ENDCASE)

GOTO

Format: **GOTO** *state_num;*

Examples: GOTO ShowHit; or
GOTO ^B00001;

State_num Specifies the state number for the unconditional jump. A numeric representation of the state or a constant label defining the numeric value in the macro definition section can be used to indicate the state number.

The GOTO statement is used to unconditionally jump to a different state on the next clock edge.

IF-THEN-ELSE

Unlike the GOTO statement, the IF statement provides a conditional jump to the next state. If the condition is satisfied, the logic jumps to the state specified after the THEN identifier. If the condition is not satisfied, the ELSE state will be the next state.

Format: **IF** *condition* **THEN** *state_num1*
ELSE *state_num2;*

Example: if (!CARDIN) then AddCard
else ShowHit; "^B00001 can be used
"instead of ShowHit.

Condition A boolean expression condition which can be in the form of a macro equation label (see "Macro Equations" in section 11.10).

State_num1 If condition is satisfied, then jump to this state on the next clock edge.

State_num2 If condition is not satisfied, then jump to the alternate state.

CASE-ELSE-ENDCASE

Format:

```
CASE
        condition_1: state_num;
        condition_2: state_num;
        .
        .
        condition_N: state_num;
ELSE                    "ELSE is optional
        state_num;
END_CASE;
```

Example:

```
case
  !Bust: ShowStand;
  Bust & !Ace: ShowBust;
  Bust & Ace: Sub_10;        "^B01111 can be used
endcase;                     "instead of the constant label
                             "Sub_10.
```

Condition_N The condition must be a boolean expression. It can also be in the form of an equation label defined in the macro definition section (see "Equation Declaration" in Macro Definitions).

State_num The number represents the state for the conditional jump.

The CASE statement is simply an IF statement with multiple conditions. It lists a sequence of mutually-exclusive conditions and their corresponding state numbers. If a condition in the list is satisfied, the logic jumps to the corresponding state on the next clock edge. If no conditions are satisfied, then it jumps to the state number specified after the ELSE reserved identifier.

Note that the ELSE identifier is optional. If it is not specified and the conditions in the CASE list are not satisfied, then the next state is dependent on the type of flip-flop that is set up in the state cells. For instance, if the state cells have D-type registers, then the next state will reset to state 0. If the state cells have T-type registers, then it will hold at the current state.

WITH-ENDWITH

The WITH statement is used in conjunction with the GOTO, CASE-ELSE-ENDCASE or IF-THEN-ELSE statements. It allows outputs to be specified so that they use the same clock edge(rising or falling clock edge dependent on the configuration) that triggers the next state. **It is recommended to use only registered outputs with the WITH statement.**

Format: **WITH**
registered output equations ...
ENDWITH;

Example:
```
if (A & B) then 1 with
                C = IN; "C is a D-type registered output
                D = 1;  "D is a T-type registered output
                endwith;
        else 2;
```

In the above example, when the expression (A & B) is true jump to state 1 on the next clock edge. Using the same clock edge, the output C latches the data from the input IN. Also, output D will toggle (since it is a T-type register) on same clock edge. If the condition (A & B) is not satisfied, the logic jumps to state 2 without changing the signals on outputs C and D.

Register Types of the "allocated" state cells

Prior to entering your state diagram design syntax, the outputs of the allocated LCCs and IOCs must be configured as registered outputs. The type of registers used, whether they are D, T or JK type registers, affect the behavior of the state diagram. An example is shown in Figure 11-5.

Outputs of the State Diagram

The two types of outputs in the PLACE state diagram are the synchronous and asynchronous outputs.

- **Synchronous Outputs:** These are registered outputs which use the same clock as the state machine. The outputs follow the input data on the next clock edge.
- **Asynchronous Outputs:** These are combinatorial outputs. The outputs follow the input data immediately.

Note that the state diagram outputs must first be configured using the PLACE architectural software. For instance if a registered output is required, the type of flip-flop (D,T or JK) and clock (pin or sum term) must be configured in the LCC/IOC or IOC screen in the Design operation.

The two classes of state machine designs that can be created using the PLACE software are the Mealy and Moore machines. Both of these state machine designs can utilize the synchronous and asynchronous outputs.

```
DEFINE
ST_TEST = [S2 S1 S0]

STATE_DIAGRAM  ST_TEST
  state 0: goto 1;
  state 1: case
             A&B&C: 0;
             A&B&/C: 3;
             /A&/B&/C: 4;
           end;
  state 2: goto 5;
    .
    .
  state 7: goto 0;
END:
```

All conditions in the case statement of state 1 failed. Hence, the equations for the state cells S0, S1 and S2 are:

S0 = 0; S1 = 0; S2 = 0;

Question:
What is the next state?

If D-type registers are used for S0, S1 and S3 state cells:	**If T-type registers are used for S0, S1 and S3 state cells:**
Answer: Output of a D-type register follows the input on the next clock edge. Hence after clocking the S0, S1 and S2 registers, the outputs equate to 0 which is the condition of state 0. **So, the state 0 is the next state.**	Answer: Output of a T-type register follows the previous state on the next clock edge if the input is FALSE or "0". Hence after clocking the S0, S1 and S2 registers, the outputs follow the previous state of each register. **So, the state 1 is the next state.**

Figure 11-5, State diagrams with D and T type registers

Mealy Machine

A Mealy state machine is defined as having outputs which are a function of two sets of variables:

- the present input conditions
- the present state of the machine

```
Examples:   Me_Reg = INPUT;      "Registered output
            Me_Com = INPUT;      "Combinatorial output
```

Moore machine

A Moore state machine is defined as having outputs which are strictly a function of the state of the machine.

```
Examples:   Mo_Reg = 0;          "Registered output
            Mo_Com = 0;          "Combinatorial output
```

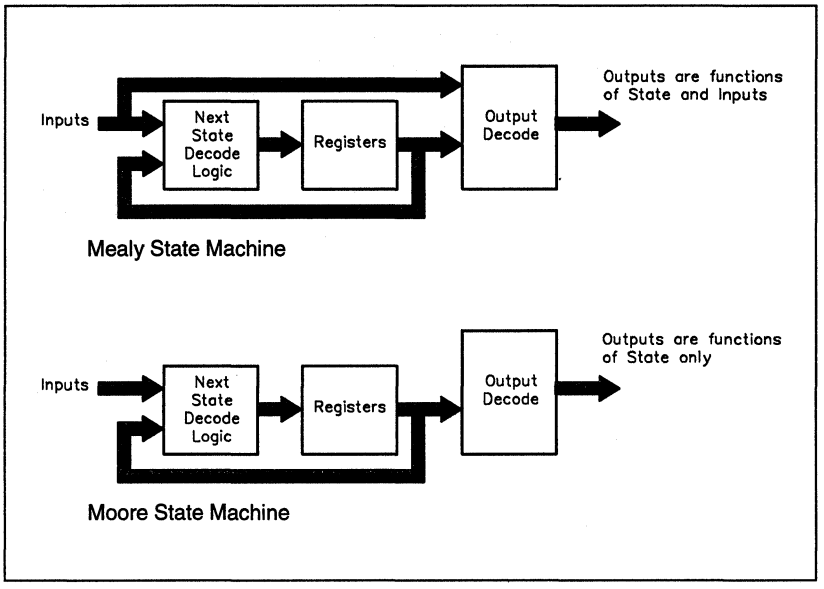

Figure 11-6, Mealy and Moore State Machines

How the PLACE State Diagram works

Figure 11-7 shows a state diagram example (SDEXAMPL.PSF) using the PLACE state diagram language. This example does not implement any specific application except to illustrate the usage of the state diagram language. The features that are illustrated in the example are:

- GOTO, CASE-ELSE-ENDCASE, IF-THEN-ELSE and WITH-END-WITH syntax.
- Synchronous and asychronous outputs in Mealy and Moore state machines
- Set Equations for Moore Machine Applications (refer to section 11.10 on "Macro Definitions")

The PLACE Simulate waveforms for the example are shown in Figure 11-8.

```
DEFINE

EXAMPLE = [S1 S0]                    "State cell assignment definition
Grp_Out = [OUT3 OUT2 OUT1 OUT0]      "Group outputs assignment

St0 = 0;                             "default - Decimal
St1 = ^H1;                           " ^H   - Hexadecimal
St2 = ^O2;                           " ^O   - Octal
St3 = ^B11;                          " ^B   - Binary

In0 = /I2 & /I1 & /I0                "Input conditions for the State Diagram
In1 = /I2 & /I1 &  I0
In2 = /I2 &  I1 & /I0
In3 = /I2 &  I1 &  I0
In4 =  I2 & /I1 & /I0
In5 =  I2 & /I1 &  I0
In6 =  I2 &  I1 & /I0
In7 =  I2 &  I1 &  I0
In4T06 = In4 # In5 # In6


STATE_DIAGRAM  EXAMPLE
"Goes to STATE St0 upon device power-up (all registers reset on power-up)

   STATE St0:
      Mo_Reg = 0;        "Moore registered output
      Mo_Com = 0;        "Moore combinatorial output
      Grp_Out = 0;       "Moore group combinatorial output, Out3-0 = 0000
      Me_Reg = INPUT;    "Mealy register output
      Me_Com = INPUT;    "Mealy combinatorial output

      IF In1 THEN St1    "If In1=true, then go to STATE St1,
           ELSE St0      "             else remain at STATE St0.

   STATE St1:
      Grp_Out = ^B0110;  "Out3-0 = 0110. These combinational outputs will be valid after the
                         "present state occurs with a single propagation delay (tpd).
      Me_Reg = INPUT;    "This registered output will be valid on the next clock edge,
                         " i.e. clock edge for the NEXT STATE (St0, St1 or St2 depending
                         "on which CASE condition is satisfied).
```

Figure 11-7 PLACE State Diagram Language for SDEXAMPL Design Example

```
    Me_Com = INPUT;   "This combinational output will be valid after the present
                      "state occurs with a single propagation delay (tpd).

    CASE
        /I2 & I1 & /I0: St0          "Go to St0 if (/I2&I1&/I0)=In2=true
                        WITH
                          Mo_Reg = 1; "This output equals to 1 on the next clock edge
                                      "only if the NEXT STATE is St0.
                        ENDWITH;
        In3:            ST2;         "Go to St2 if In3=true
    ELSE
        St1             "If no condition in the CASE list is satisfied, remain at STATE St1.
    ENDCASE;
STATE St2:
    Grp_Out = ^HA;    "Out3-0 = 1010. These combinational outputs will be valid after the
                      "present state occurs with a single propagation delay (tpd).

    IF (In4To6)       THEN St3   "If (In4To6)=true, then go to STATE St3,
        WITH
          Me_Reg = INPUT;        "This registered output will be valid on the next
                                 "clock edge only if the NEXT STATE is St3.
        ENDWITH;
    ELSE
        St2;                     "If (In4To6)=false, then remain at STATE St2.

STATE St3:
    Mo_Reg = 1;       "This output equals to 1 on the next clock edge.
    Mo_Com = 1;       "This combinational output will be valid after the present state
                      "occurs with a single propagation delay (tpd).
    Grp_Out = 0;      "Out3-0 = 0000.
    Me_Reg = 0;       "Reset all Mealy outputs
    Me_Com = 0;

    GOTO St0;         "Go to STATE St0 unconditionally.

END;                  "End of STATE DIAGRAM EXAMPLE
```

Figure 11-7 PLACE State Diagram Language for SDEXAMPL Design Example (Continued)

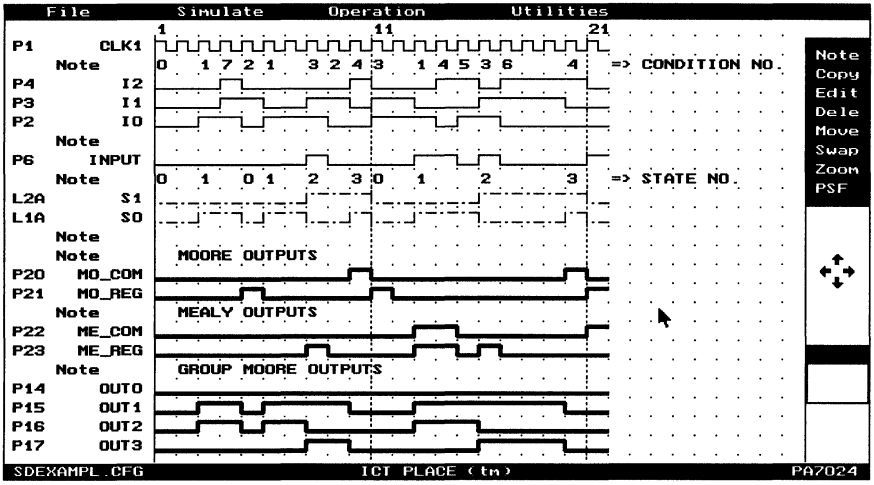

Figure 11-8 Simulate Waveforms for the SDEXAMPL Design Example

11.12 Truth Tables

In addition to state diagrams and equations, truth tables can be used to describe the logic designs.

Format 1: **TRUTH_TABLE** *table_label*
(*In1 In2 ... InN* **->** *Out1 Out2 ... OutN***)** or

END;

Format 2: **TRUTH_TABLE** *table_label*
(*Input* **->** *Output***)**

END;

Example 1:

```
TRUTH_TABLE DECODE "3-to-8 Decoder
(C B A -> Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7)
 0 0 0 ->  1  0  0  0  0  0  0  0
 0 0 1 ->  0  1  0  0  0  0  0  0
 0 1 0 ->  0  0  1  0  0  0  0  0
    .
    .
END;
```

Example 2:

```
DEFINE
SCORE = [S4 S3 S2 S1 S0]
BCD2 = [D5 D4]                    "
BCD1 = [D3 D2 D1 D0]

TRUTH_TABLE BIN2BCD "From JACK7024.PSF
( SCORE -> BCD2 BCD1)
    0   ->   0    0;
    1   ->   0    1;
    2   ->   0    2;
    .
    .
END;
```

Table_label — The format for the label is similar to that for the pin or cell label (section 11.6) with one exception, and that is the / or ! character is not allowed at the beginning of the label.

InN (Format 1) — Specifies the pin or cell labels to be used as truth table inputs. The inputs can be either registered or combinatorial. **Input data must be in binary (0 or 1) format.**

OutN (Format 1) — Specifies the pin or cell labels to be used as truth table outputs. Like the inputs, truth table outputs can be either registered or combinatorial. **Output data must be in binary (0 or 1) format.**

Inputs (Format 2) — Specifies a macro defined group of registered or combinatorial pins or cells to be used as truth table inputs. Input data can be in decimal (default), hexadecimal (^H or ^h), octal (^O or ^o) or binary (^B or ^b) numbering system. Only one macro level is available for the macro input set.

Outputs (Format 2) — Specifies a macro define group of registered or combinatorial pins or cells to be used as truth table outputs. Input data can be in a decimal (default), hexadecimal (^H or ^h), octal (^O or ^o) or binary (^B or ^b) numbering system. Only one macro level is available for the macro output set.

An additional feature is that both the truth table formats can be used in a single truth table design.

Alternate truth table description which uses both formats for Example 2 is:

```
TRUTH_TABLE  BIN2BCD
( SCORE -> D5 D4 BCD1)
    0   ->  0  0   0;
    1   ->  0  0   1;
    2   ->  0  0   2;
    .
    .
END;
```

11.13 Equations

The boolean logic equations are the primary methods for specifying logic functions in the PLACE software.

The PLACE architectural software automatically creates the equation for each sum or product term in the cell when it is labeled via the **"Label"** command in the "Design" menu of the Design operation. An example of a newly labeled LCC is shown below.

```
A.D = 0;
A.AP = 0;
A.AR = 0;
A.CLK = 0;
```

Format: *Output_label.EXT = logic_equation ;*

(The semicolon at the end of the equation is used by the PLACE software to mark the end of the equation when displaying the equation in the Equation Display window. Refer to "PSF Text Display Windows" in section 11.12)

Examples:
```
C1.COM = (V0 & Add10 & Sub10 & S0);
S0.T = (V0 & Add10 & Sub10);
XOR1.COM = A $ B;
XOR2.COM = (!A & B) + (A & !B);
```

Output_label — This is the pin or cell label that has been entered via the **"Label"** command. Refer to section 11.6 for the format of the label.

.EXT — The dot extension of the output is automatically appended to the output label by the PLACE software. The type of extension that is appended on each output label depends on the configuration of the pin or cell, the specific function of the product or sum term, and the device type. Refer to Figure 11-9.

Logic_equation — A boolean logic expression that consists of inputs, feedbacks and logic operators. Table 11-3 shows the functions and priorities of the logic operators available in the PLACE software.

Operator	Logic Function	Priority
( )	Logical organization	1
! or /	NOT	2
& or *	AND	3
# or +	OR	4
$	Exclusive-OR	5

Table 11-3, Priorities of logic operators in PLACE

The output equations can be moved to other locations of the PSF design file as long as they are specified after the reserved identifier **EQUATIONS**. However, the PLACE software operation will be affected if the unused or any other equations generated by the PLACE software are deleted. This means that all equations, whether they are used or unused, are continuously referenced by the PLACE software.

Functions of the Dot Extensions in the equation labels

In the PLACE source file, each of the Dot extensions represents a specific function. Figure 11-9 details the functions of all Dot extensions.

PEEL Array

Sum Term	Dot Extension	LCC Function (unless stated otherwise)
Sum A	.COM	Combinatorial Internal/External Output
	.D	D Input of the Register
	.T	T Input of the Register
	.J	J Input of the Register
	.SumA	Sum A term is unused
Sum B	.COM	Combinatorial Internal/External Output
	.K	K Input of the Register
	.AP	Asynchronous Preset for Register
	.SumB	Sum B term is unused
Sum C	.COM	Combinatorial Internal/External Output
	.CLK	Asynchronous Clock for Register
	.AR	Asynchronous Reset for Register
	.SumC	Sum C term is unused
Sum D	.CLK	Asynchronous Clock for Register
	.OE	External Output Enable Control (IOC)
	.FB	Buried feedback (PA7140 and PA7128)
	.SumD	Sum D term is unused

PEEL18CV8/PEEL22CV10A/22CV10A+ Devices

Prod Term	Dot Extension	Function
And A	.OE	External Output Enable Control
	.AndA or .And	Product (And) A term is unused
Sum B	.COM	Combinatorial External Output
	.D	D Input of the Register
	.SumB or .Sum	SumB term is unused

Figure 11-9, Functions of the Dot Extension in the Equations Labels

Logic Reduction Compiler Directive (For Equations Only)

A compiler directive is available to prevent redundant terms in the equations from being removed during the logic optimization process. Sometimes redundant terms are intentionally added to avoid race or hazard conditions, especially in asynchronous applications.

Format: **@REDUCE ON** or **@R+**

@REDUCE OFF or **@R-**

Example:
```
@R-                          "same as @Reduce Off
G_Latch.COM =          "Gated Latch Application
    LAT_EN & LAT_IN
    !LAT_EN & G_Latch
    LAT_IN & G_Latch;  "redundant term to fix hazard
@R+                          "same as @Reduce On
```

@Reduce On — Equations succeeding this directive will be optimized. Redundant terms will be removed from the equations. This is the default condition.

@Reduce Off — All equations specified after this directive will be flattened (i.e. converted to Sum-of-Product equations from complex equations) but not optimized. Redundant terms will be left in the equations.

Equations of the Outputs used for State Diagrams or Truth Tables

Boolean equations are generated for all pins and cells that are labeled via the **"Label"** command, including those that are specifically used for state diagram or truth table designs. **These equations if they are unmodified do not affect the logic of the state diagrams or truth tables because they always equate to zero.** However, if the equations are modified and they do not equate to zero, then they will be logically ORed with the boolean equations that are transformed from the state diagram or truth table design syntax by the PLACE compiler.

PLACE Application Examples

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12.0 PLACE Application Examples

12.1 Overview

There are several PLACE application examples provided with the PLACE software. All application files included with the PLACE software are listed in Table 12-1. The following pages provide descriptions and block diagrams for the design example included with the PLACE software. The design source (PSF) files with equations state machine and truth table descriptions are not shown. Please use the PLACE software to review the design source files. The PLACE document operation can also be useful for printing out the PSF design file or other applicable graphics and text files.

File Name	Device	Description
DEMO1A.PSF	PA7024	Demonstration design for PA7024 which includes Basic Gates and Registers, 8-bit Down Counter, 2-bit State Machine, 4-bit Shift Register and 8-bit Bidirectional I/O Port
GATES1.PSF	PA7024	Basic Gates (part of DEMO1A).
REG1.PSF	PA7024	Basic Registers, 8-bit Down Counter, 2-bit State Machine and 4-bit Shift Register (all are part of the DEMO1A)
BI_PORT.PSF	PA7024	8-bit Bidirectional I/O Port (part of DEMO1A)
COUNTER1.PSF	PA7024	8-bit Down Counter with Preset, Reset and Hold (part of DEMO1A)
TIMER.PSF	PA7024	16-Bit Programmable Clock Generator/Timer
JACK7024.PSF	PA7024	Blackjack Machine Example
TC7140.PSF	PA7140	8-bit Time/Counter
ST7128.PSF	PA7128	4-Bit State-Machine and 8-Bit Counter
V8GATES.PSF	18CV8	Basic Logic Gates
V8REGS.PSF	18CV8	Basic Registers and Latches
V8CLKADD.PSF	18CV8	Clock Divider Address Decoder
V8BUSMUX.PSF	18CV8	Bus Programmable 8-to-1 Multiplexer
V8FCNTR.PSF	18CV8	8-bit Counter with Function Controls
V8CPORT.PSF	18CV8	Change-of-State Input Port with Interrupt
V8SYNC.PSF	18CV8	Synchronization Circuit.
V10CNT8.PSF	22CV10	8-bit Up/Down Loadable Counter with Carry-out or Borrow-in
PARV10A	22CV10A	9-bit Even/Odd Parity Generator/Checker
V10ZPORT	22CV10A+	Change-of-State Input Port with Interrupt

Table 12-1, PLACE application examples

12.2 DEMO1A.PSF - PA7024

The PLACE design file DEMO1A.PSF incorporates several applications within one design, including: Basic Gates, Basic Registers and Latches, 8-bit Counter, Bi-Directional I/O Port and a Divide-by-2 Clock design. Figures 12-1 and 12-2 show the PLACE pin block and equivalent schematic diagrams.

- **GATES** Basic combinatorial functions including AND, OR, NOR, NAND, EXOR, Inverter, 4-to-1 mux, and 4-bit comparator.
- **REGS** Basic registers including D, T and JK flip-flops with independent clocks, presets and resets, an SR Latch (for debouncing inputs), a gated-latch (LAT1), a basic storage register (REG1), a 2-bit state machine (S0,S1), and a 4-bit shift register (SHF0-3).
- **COUNTER** An 8-bit down counter with Hold, Preset and Reset.
- **PORT** An 8-bit bi-directional I/O port with registered input.

The mode inputs, MODE1 and MODE2, control application selection. Pins names A through H are used as inputs and/or control, pins I through P are used as outputs. The outputs of each application are selected via eight 4-to-1 muxes. Output enable and direction (in PORT mode) are selected by CONTROL. Each of the four applications are also provided with the PLACE software as individual design examples.

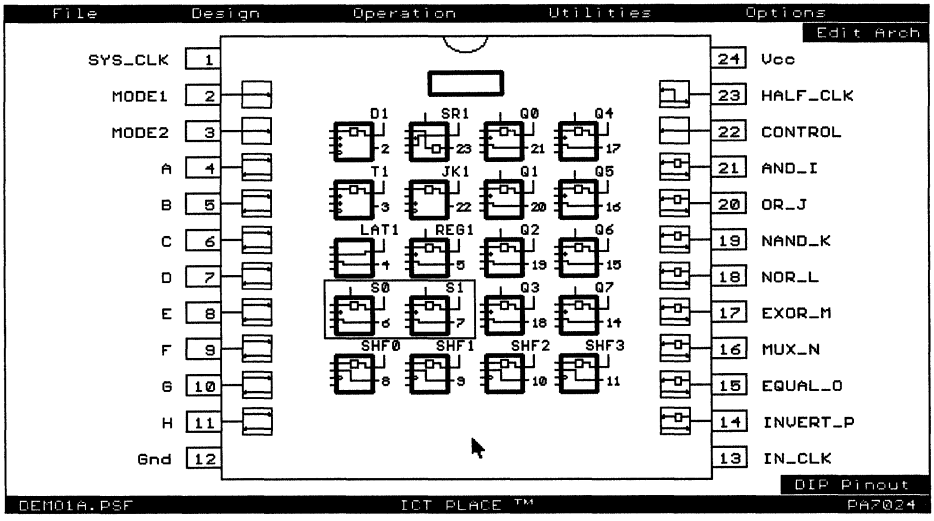

Figure 12-1, PLACE pin block diagram of DEMO1A.PSF

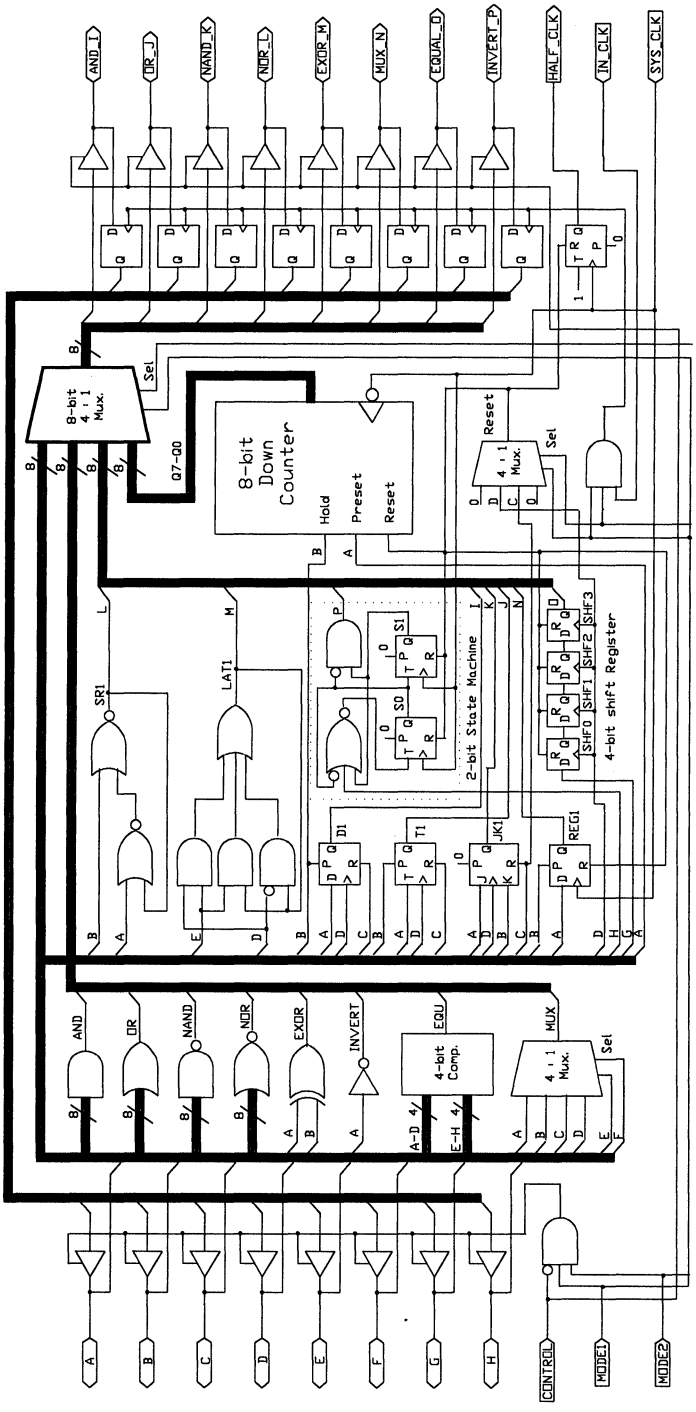

Figure 12-2, Logic schematic of DEMO1A.PSF

12.3 TIMER.PSF - PA7024

This application uses the PA7024 to implement a 16-bit programmable clock-generator/interrupt-timer that can be interfaced to a 16-bit microprocessor bus. A buried 16-bit reloadable down counter is used to divide the high speed input clock.

Upon power-up the counter is disabled. To program the counter, a value must be written into a 16-bit count register from the D0-D15 I/O pins and the counter must be enabled (see Table 12-2 for control). The value in the count register will be loaded into the counter which will count down to 0000 Hex. After reaching 0000 Hex, it will automatically reload the value from the count register. This allows the counter to be free running for clock generation if the value in the count register is maintained. **Note that the "register-type change" feature of the PA7024 global cell is used to dynamically switch the T registers to D registers for loading when the counter reaches the count 0000 Hex.**

If the count register is changed, the new count will be loaded after the count reaches 0000 Hex. One-shot operation for timer controlled interrupts can be implemented by setting the count register to 0000 Hex after the count has been loaded. When this is done, the counter will stop and hold at 0000 Hex. The OUT pin will toggle (initially low then high and so on) each time the counter reaches 0000 Hex. The counter and OUT pin can be reset, disabled or enabled via a bus command (see table). The count can be read "on the fly" via the D0-D15 pins, temporarily held stable until the read is completed.

/CS	/RD	/WR	/A0	Function
1	X	X	X	Not selected (Don't Care)
0	1	0	0	Write Count Register from D0-D15
0	0	1	0	Read Count Register onto D0-D15
0	1	0	1	Reset/Stop Counter and OUT
0	0	1	1	Enable and Read Counter onto D0-D15

Table 12-2, Command table for TIMER.PSF

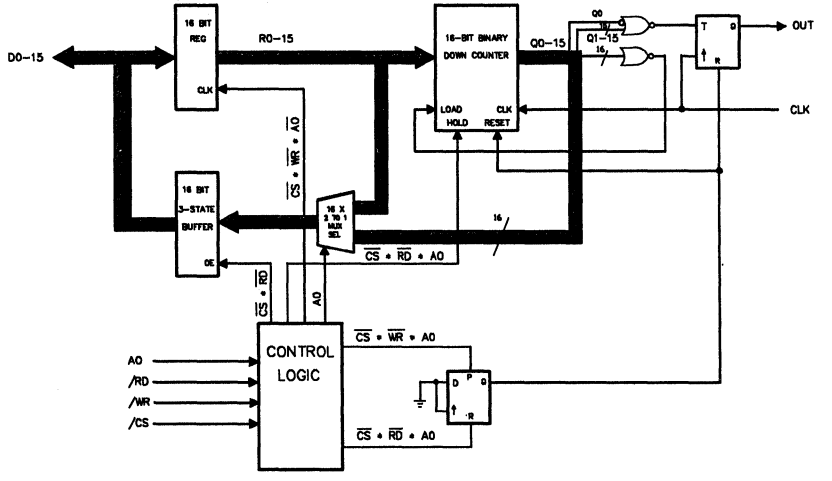

Figure 12- 3, Logic schematic of TIMER.PSF

12.4 JACK7024.PSF - PA7024

This design example is based on C.R. Clare's design in Designing Logic Systems Using State Machines (McGraw Hill, 1972). The blackjack machine plays the dealer's hand, using typical dealer strategies to decide whether to draw another card (hit) or stand after each round.

The example contains the following logic designs:

- A state machine that controls the game logic which includes:
  - checking the status of the card reader.
  - making the decision of what action to take for a hit, stand or a bust. An example is to draw a card if the hit signal is true.
  - making the decision of when to use the value 1 or 11 for an ace card.
- A Multiplexer/Comparator which compares the point total and sends the hit, stand or bust signal to the state machine. If the point total is greater than 21, it's a bust. If it is equal or less than 16, then hit else stand.
- A 5-Bit Adder that adds the value of the drawn card.
- A Binary-to-BCD converter for converting the 5-bit binary score and converts it to 2-digit BCD for the digital display.

This design example can also be implemented by using three PLDs which include a PAL22V10 for the Multiplexer, Comparator and Adder, a PAL16L8 for the Binary-to-BCD converter, and a PAL16R6 for the state machine.

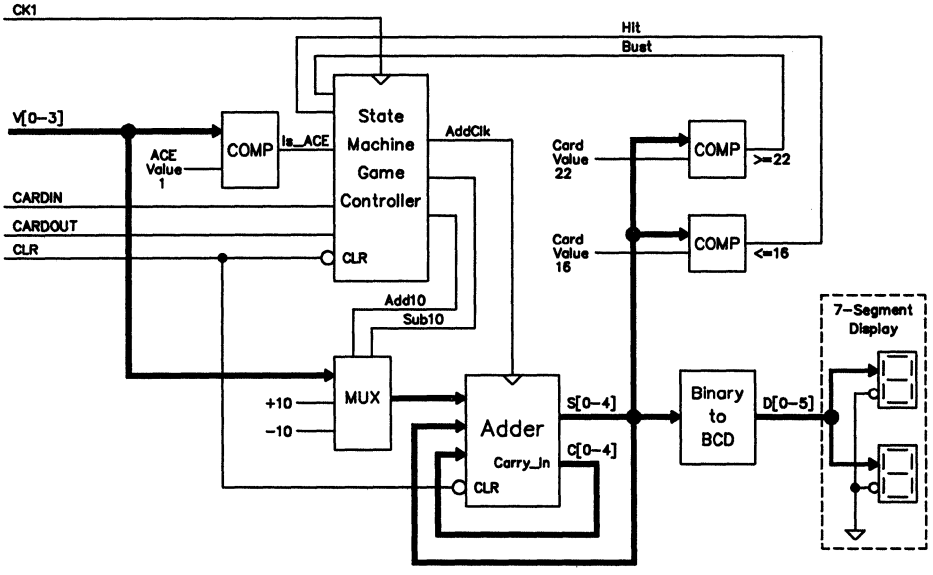

Figure 12-4, Logic diagram of JACK7024.PSF

12.5 TC7140.PSF - PA7140

This example uses a PA7140 device to implement a timer/counter application which is typically used in a microprocessor-based computer system. The circuit employs a multiplexer to allow either the imcoming or latched data to be loaded into the counter. The desired data is then loaded into the counter either by reseting the counter and the compare register, or by a match between the counter's state and the value in the compare register.

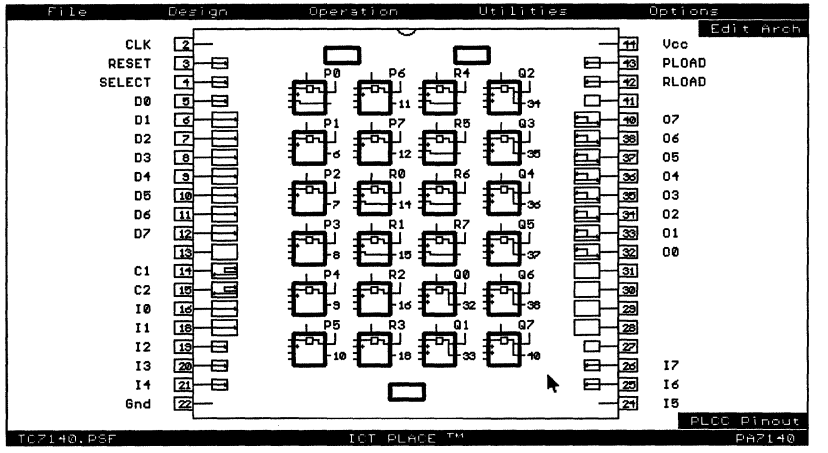

Figure 12-5, PLACE block diagram of TC7140.PSF

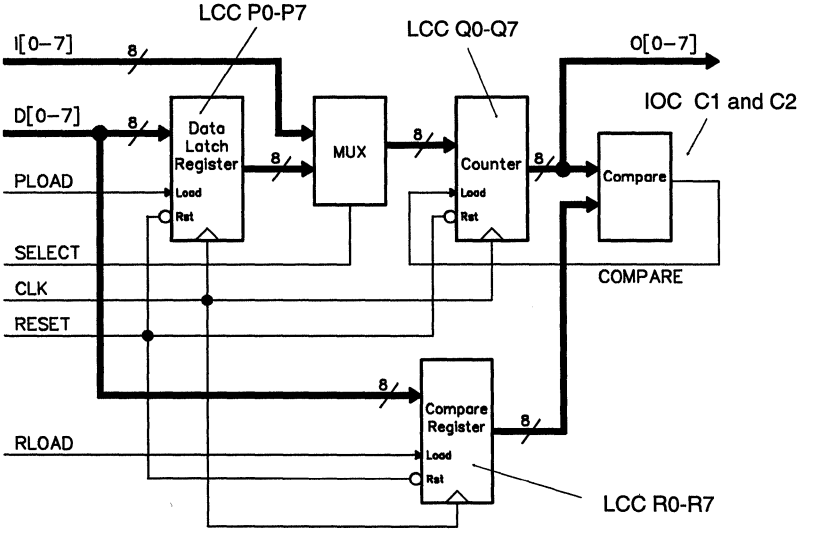

Figure 12-6, Logic diagram of TC7140.PSF

12.6 ST7128.PSF - PA7128

This example implements an 8-bit buried counter, an 8-bit buried register, and a 4-bit buried state machine. The counter uses 8 LCC registers and the the 8-bit register and 4-bit state machine uses 12 IOC register/latches. IOC registers can be buried by using the feature of the 7128 that allows the output enables to be fed back into the array.

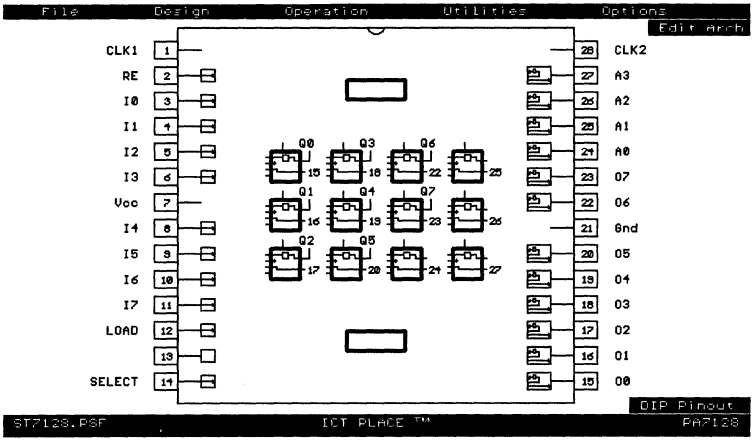

Figure 12-7, PLACE pin block diagram of TC7140.PSF

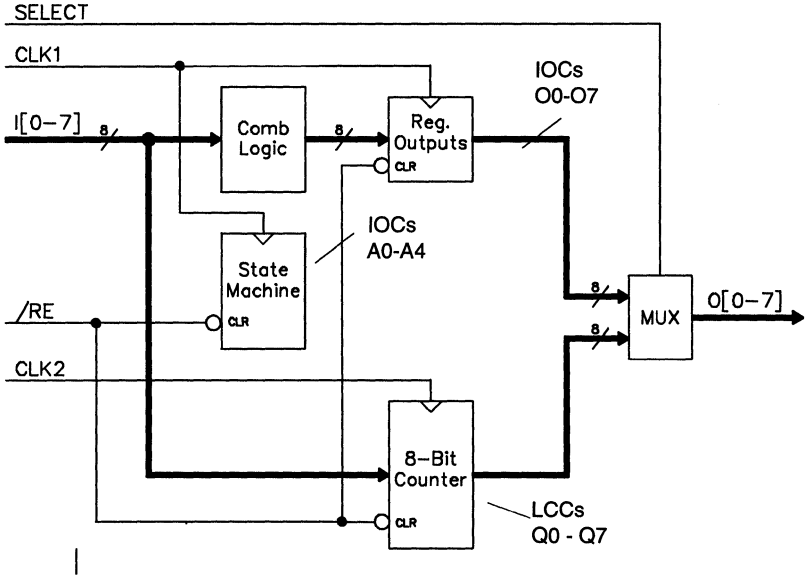

Figure 12-8, PLACE logic diagram of TC7140.PSF

12.7 V8GATES.PSF - PEEL18CV8

This PEEL18CV8 application example implements several basic logic gates. The logic gates include:

- an inverter
- four-input AND, OR, NAND, and NOR gates
- a four-input AND-OR- INVERT gate
- a two- input XOR gate
- a high-impedance buffer.

Each gate uses one or more of the (A,B,C and D) inputs. Additionally, the high-impedance buffer uses the /HZ input for impedance control. The truth table for these gates can be examined in the test vectors. Note, the remaining unused input pins can be used as additional inputs into the gates.

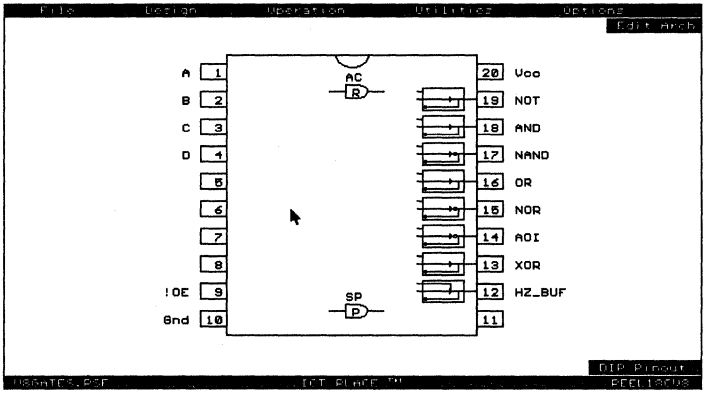

Figure 12-9, PLACE block diagram of V8GATES.PSF

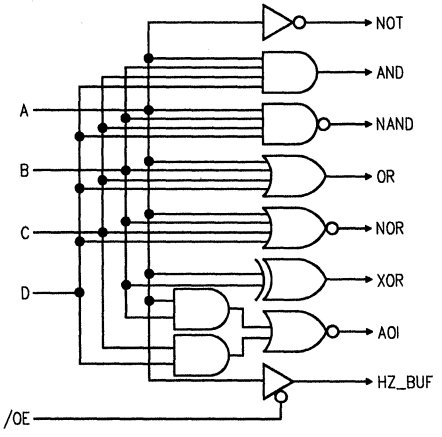

Figure 12-10, Logic schematic of V8GATES.PSF

12.8 V8REGS - PEEL18CV8

This application example demonstrates the implementation of several basic registers and latches within a PEEL18CV8. Four register types included are the D, T, JK, and SR, all of which are clocked by the CLK input. All registers can be synchronously reset, set,and asynchronously reset using the SRES, SSET and ARES inputs respectively. Besides the registers, an SR latch and a Gated Latch circuit show how independent asynchronous storage elements can be implemented. Only the Q outputs of these registers and latches are provided at the output pins. The /Q outputs could easily be accessed by inverting the macro cell output polarity. Truth table operation can be referenced via the test vectors.

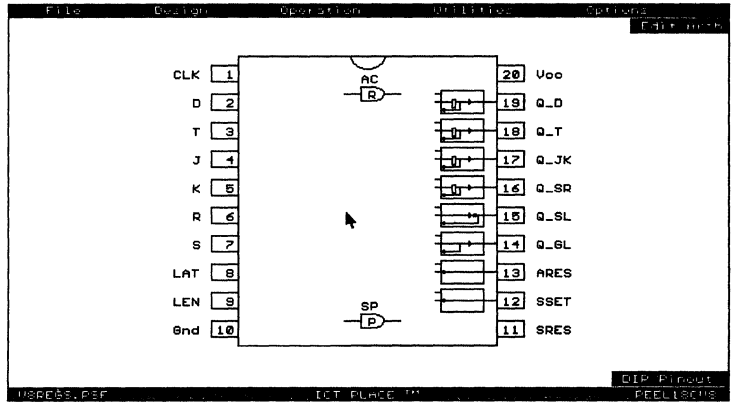

Figure 12-11, PLACE block diagram of V8REGS.PSF

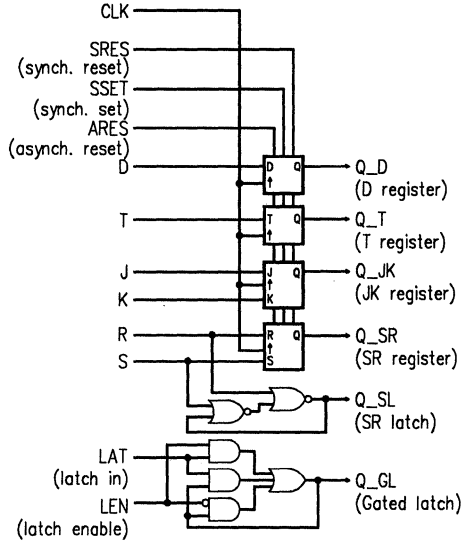

Figure 12-12, Logic schematic of V8REGS.PSF

12.9 V8CLKADD.PSF - PEEL18CV8

This application uses the PEEL18CV8 for two common microprocessor system functions: a clock divider and a memory mapped address decoder. The clock divider provides a ÷2, ÷4 and ÷8 clock outputs. The SET input sets all clock outputs high. The address decoder decodes the processor address lines to select one of five memory or I/O devices. The chip select for these devices are active low. The memory map over a 64K boundary is shown below.

Memory Map for Address Decoder

Function	Address
EPROM (32K X 8)	8000-FFFF Hex
EEPROM (2K X 8)	5000-5FFF Hex
UART	4100-41FF Hex
PORT	4000-40FF Hex
SRAM (8K X 8)	0000-1FFF Hex

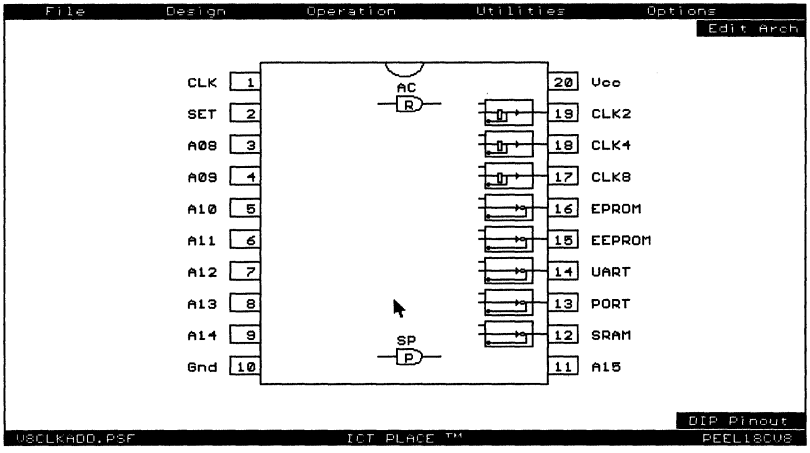

Figure 12-13, PLACE block diagram of V8CLKADD.PSF

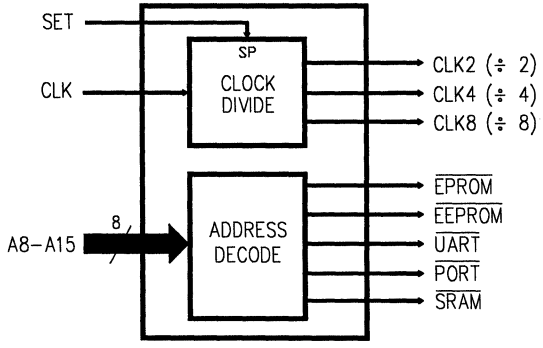

Figure 12-14, Block diagram of V8CLKADD.PSF

12.10 V8BUSMUX.PSF - PEEL18CV8

This application implements an 8 to 1 multiplexer that can be interfaced to a µP bus. Any one of the 8 inputs (I0-7) can be selectively routed to the output (OUT) by writing (/WR and /CS =0) a 3-bit binary value to the data inputs (DI0-2). The value is stored into a 3-bit latch that controls the multiplexer selection. Because the latch utilizes internal asynchronous feedback (configuration #8 of the macro cell), the value can also be enabled onto the data outputs DO[0-2]. The DI and DO[0-2] pins should be tied together for write/read bus operation.

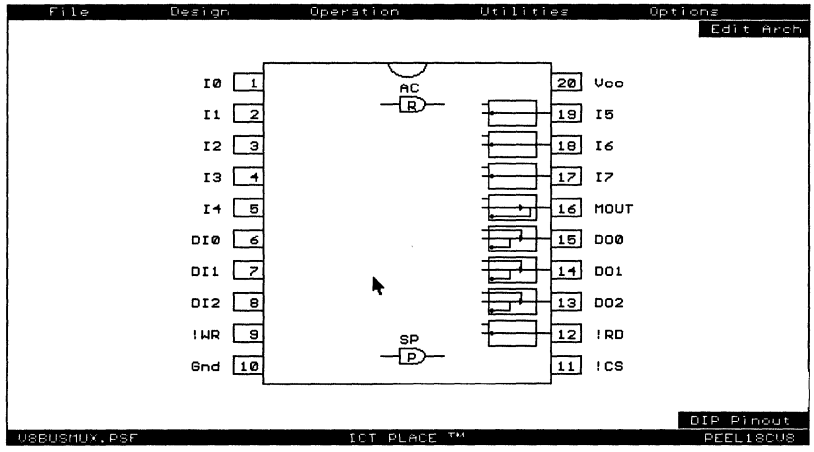

Figure 12-15, PLACE block diagram of V8BUSMUX.PSF

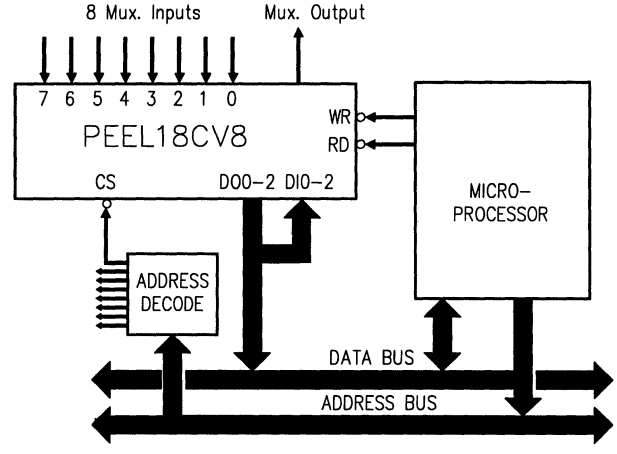

Figure 12-16, Logic schematic of V8BUSMUX.PSF

12.11 V8FCNTR.PSF - PEEL18CV8

This application uses the PEEL18CV8 as an 8 bit counter with four control functions: hold, reset, repeat and output enable. The Synchronous Preset term was utilized to free-up a product term from the eighth bit of the counter. This allows the hold function to be implemented.

- SRES (Synchronous Reset): When SRES is set High, the outputs (Q0-7) will go Low after the next clock. When SRES is Low, the counter will start counting up with each clock.
- HOLD (Hold Count): When HOLD is set High the count will hold the present state. When HOLD is Low the counter will resume.
- REP (Repeat Count): When REP is set High, the counter repeats the count after reaching FF Hex. When REP is Low, the counter will stop after one complete count.
- OE (Output Enable): When OE is High, the outputs are disabled (High-Z). When Low, the outputs are enabled.
- (TEST): This input is used to preload the registers to simplify test vector operation.

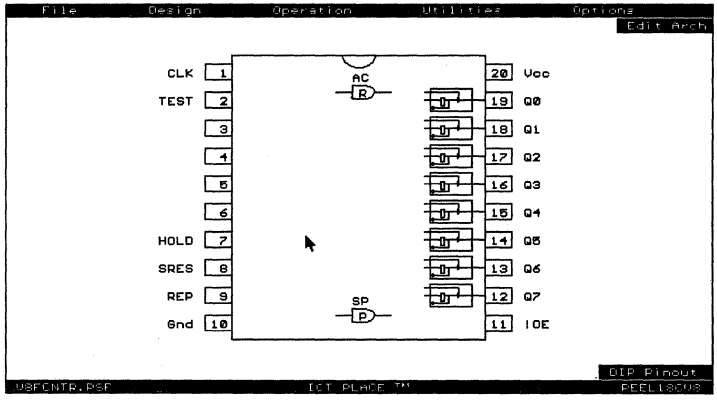

Figure 12-17, PLACE block diagram of V8FCNTR.PSF

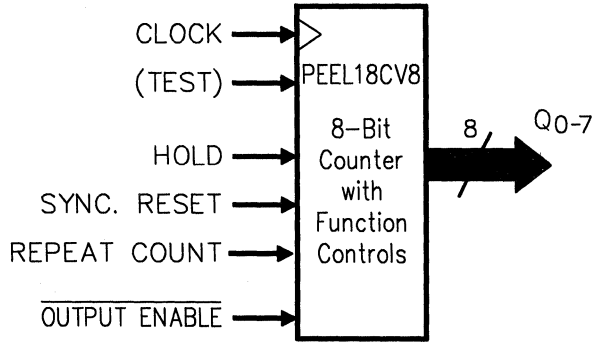

Figure 12-18. Block diagram of V8FCNTR.PSF

12.12 V8SYNC.PSF - PEEL18CV8

Digital systems often require synchronization of asynchronous inputs to avoid the potential metastability problems caused by set-up time violation. A common synchronization method uses two rippled 74LS74-type flip-flops (Figure 12-19).

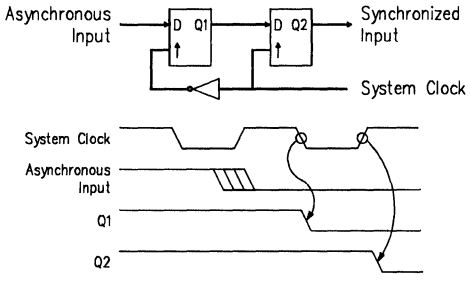

Figure 12-19, A common synchronizer circuit

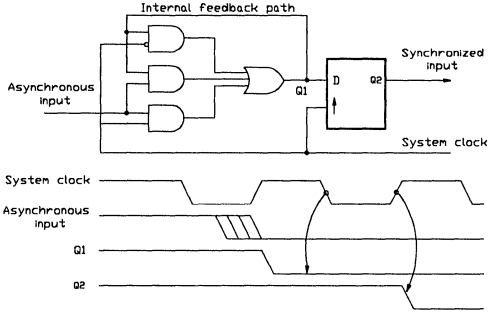

Figure 12-20, Synchronizer circuit in V8SYNC.PSF design

In this PLACE design example, the PEEL18CV8 utilizes the macro cell configuration #6 (configuration #5 can also be used instead) to implement eight synchronizer circuits as shown in Figure 12-20. In each synchronizer circuit, the gated-latch internally latches the asynchronous input on the falling edge of the clock, generating the signal Q1. ANDing the input Q1 through the internal feedback path eliminates a possible hazard condition during the clock's High-to-Low transition time. The latch then holds Q1 stable to ensure meeting the set-up time requirement of the subsequent D flip-flop which, as before, registers the signal on the next rising edge of the system clock edge. If by chance the input pulse width violates the set-up time of the gated-latch, the clock's Low time will give more time for settling. See Application Note AN-1 for more information on this design.

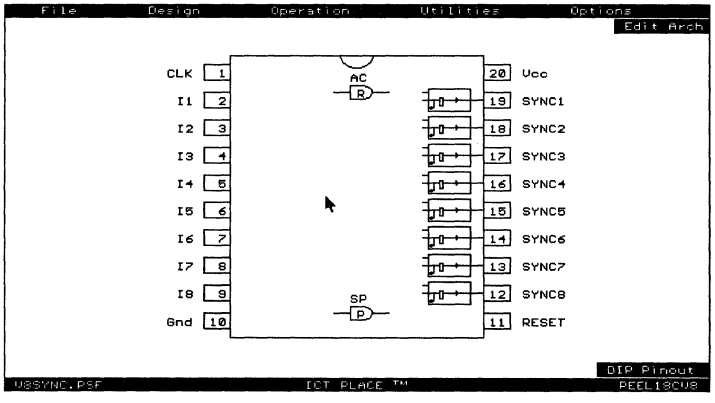

Figure 12-21, PLACE pin block diagram of V8SYNC.PSF

12.13 V10CNT8.PSF - PEEL22CV10

This application uses the PEEL22CV10 as an 8-bit Up/Down Loadable counter. The four controls are:

- CLR (Synchronous Clear)—When CLR is set to High, all outputs (Q7-Q0 and CO_BI) will be set to Low on next clock.
- UP (Up/Down control)—When UP is set to High, outputs Q7-Q0 will count up on each clock. When UP is set to Low, outputs Q7-Q0 will count down.
- LOAD (Load data)—When LOAD is set High, outputs Q7-Q0 will follow the data of D7-D0 on next clock and the output CO_BI will be set to Low.
- !OE (Output Enable)—When OE is set to High, all outputs (Q7-Q0 and CO_BI) will be High Impedance. When OE is set Low, all outputs will be enabled.

Note: After counting up 255, the count will go to 0 and the CO_BI will be set High on next clock. The High will remain on the CO_BI pin until LOAD or CLR goes High.

Operation Table

CLK	CLR	UP	LOAD	!OE	D[7-0]	Q[7-0]	CO_BI
C	1	X	X	0	X	LOW	0
C	0	1	0	0	X	Count up	0
C	0	1	0	0	X	255 - 0	1 carry-out
C	0	0	0	0	X	Count down	0
C	0	0	0	0	X	0 - 255	1 borrow-in
C	0	X	1	0	DATA IN	DATA IN	0
X	X	X	X	1	X	3-STATE	0

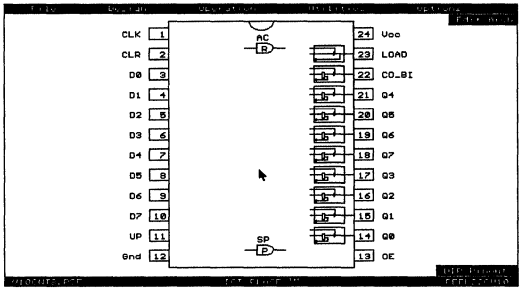

Figure 12-22, PLACE pin block diagram of V10CNT8.PSF

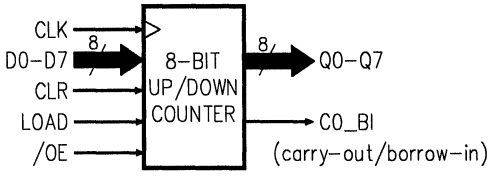

Figure 12-23. Block diagram of V10CNT8.PSF

12.14 PARV10A.PSF - PEEL22CV10A

This application uses the PEEL22CV10A as a 9-bit even/odd parity generator/checker.

Operation Table

Number of high inputs A - H	Parity_I	Even_Odd	Parity_O
Even	1	0	H
Odd	1	0	L
Even	0	0	L
Odd	0	0	H
Even	1	1	L
Odd	1	1	H
Even	0	1	H
Odd	0	1	L

The parity function is commonly implemented via the utilization of the exclusive-OR operation. To build a N-bit parity generator/checker, the number of 2-input exclusive-OR gates required is N-1. A N-bit parity function can also be implemented via the AND-OR logic operation but it requires 2^{N-1} product terms. For instance, a 9-bit parity function will require 256 product terms. Though the PEEL22CV10A device has only 132 product terms, a 9-bit parity function can still be implemented by using two macro cells to implement two 4-bit parity generators. Then, both the outputs of the macro cells are fed back and XORed with the 9th bit (Parity_In). With this method, there is an additional delay due to the feedback of the 4-bit parity generator outputs. If it is implemented in the PEEL22CV10A device, then the delay would be about 3 ns less than if it was implemented in a standard 22V10 device. This is because the outputs in the 22V10 device are fed back from the pin, whereas in the PEEL22CV10A the outputs can be configured to feedback directly from the OR gate (before the output buffer).

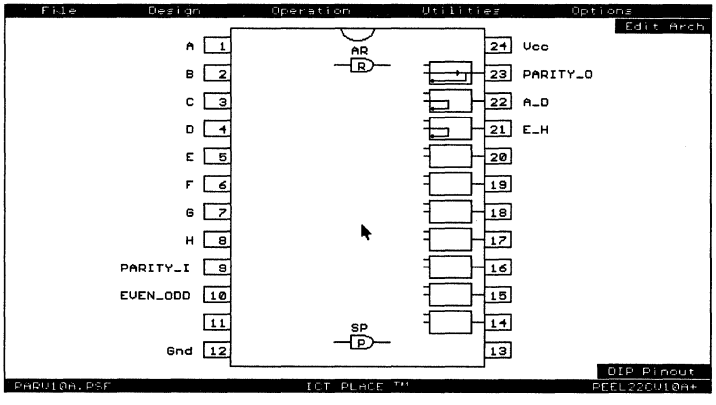

Figure 12-24, PLACE pin block diagram of PARV10A.PSF

12.15 V10PORT.PSF - PEEL22CV10

This application uses the PEEL22CV10A (with the + software/programming option) as an 8-bit input port of which all of its inputs can detect a change-of-state. When detected, the INTR output is set for interrupting a CPU. The state change is latched by eight pseudo-buried registers which can be read by the CPU on D0-D7 as listed in the address table below. Once read, unless another change has occurred, the INTR will be reset. The NEQ output can be used for status polling of any remaining state change. See Application Note AN-1 for more information.

Address			Data Outputs	
A0	**CS**	**RD**	**D0-7**	**NEQ**
X	1	X	Hi-Z	Hi-Z
X	X	1	Hi-Z	Hi-Z
0	0	0	Read I0-I7 Change	I0-I7 Pending Change Status

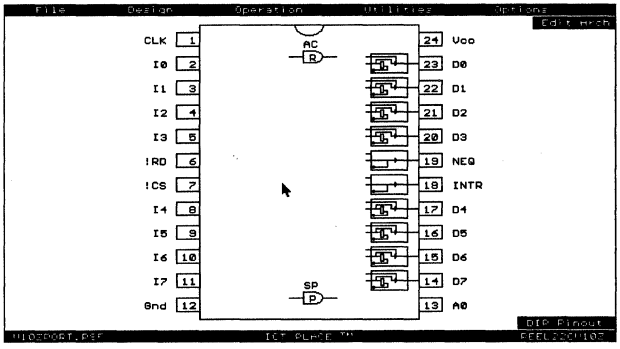

Figure 12-25, PLACE pin block diagram of V10ZPORT.PSF

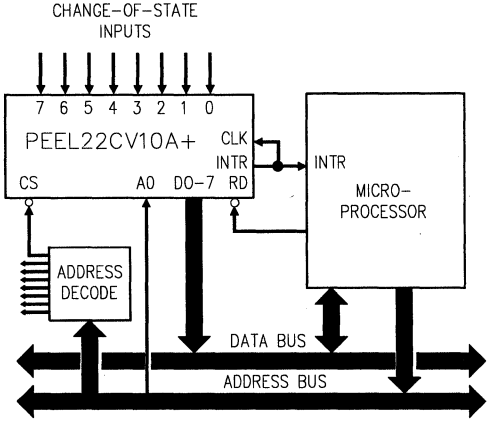

Figure 12-26, System interface block diagram of V10ZPORT.PSF

ICT Inc. 2123 Ringwood Avenue, San Jose, CA 95131 Phone: (408)434-0678 FAX: (408)432-0815