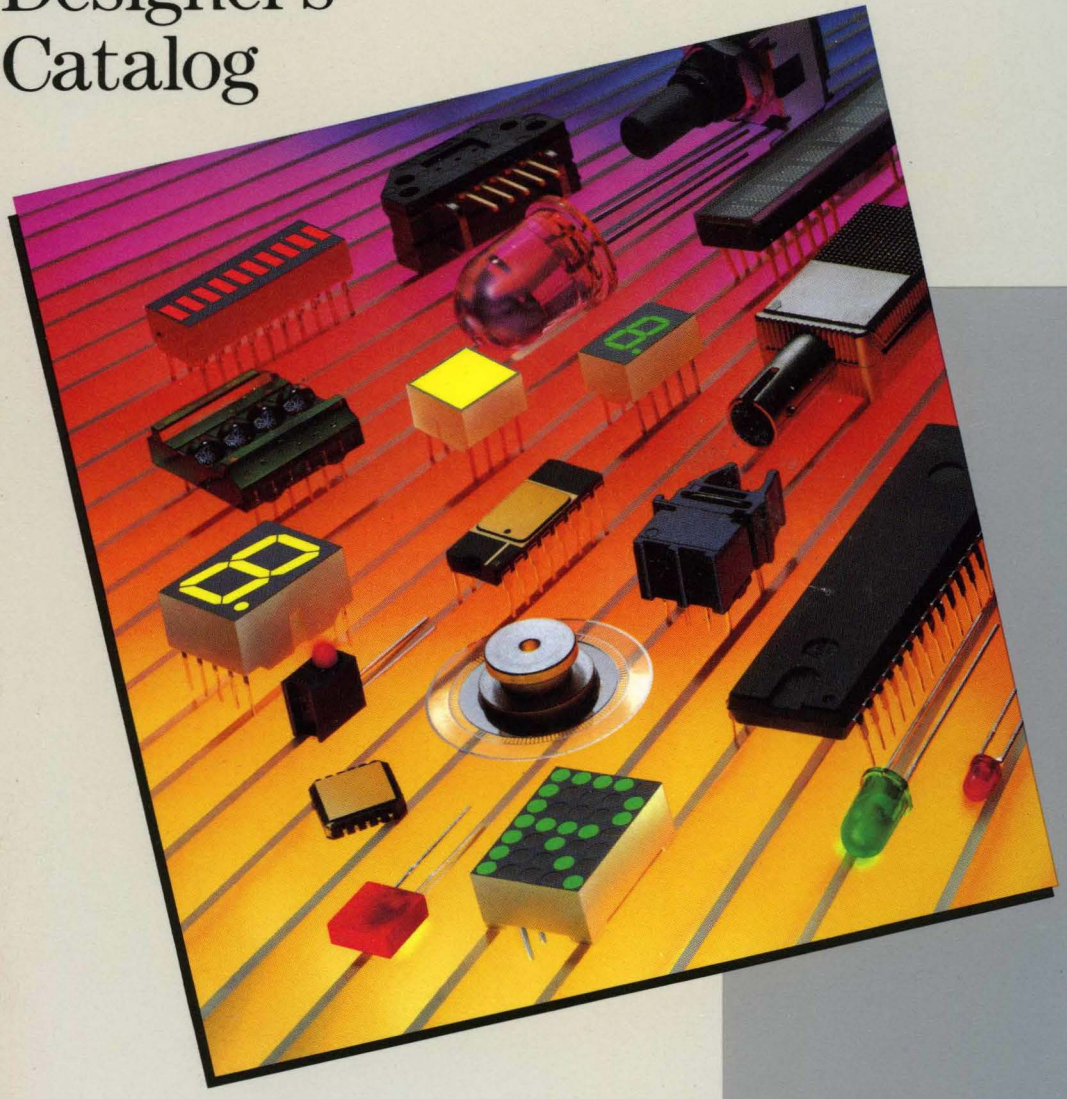
1991-92

Optoelectronics
Designer's Catalog

HEWLETT
PACKARD

Optoelectronics Designer's Catalog



1991-1992

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Hewlett-Packard: A Leader in Components

A Brief Sketch

For over 25 years, Hewlett-Packard's Components Group has developed reliable, high performance optoelectronic and microwave components. Recognized for technological advances, setting world standards, and providing high-quality products, the Components Group has become a leader in the markets it serves, such as the computer, telecommunication, automotive and military/aerospace markets.

The products of the Components Group are vertically integrated, from the growing of LED crystals, to the development of the various on-board integrated circuits, to package design. Vertical integration ensures that HP quality is maintained throughout product development and manufacturing.

Over 5000 employees are dedicated to HP Components, including a worldwide sales force. Manufacturing facilities are located in Malaysia and Singapore with factory and marketing support in San Jose, California. Marketing operations are also located in Germany, Singapore, and Japan.

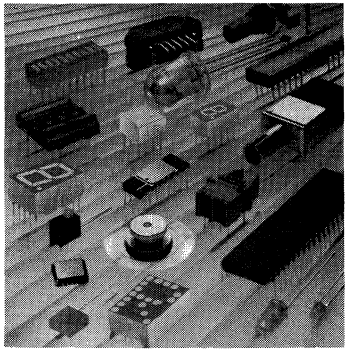
Each field sales office is staffed with engineers trained to provide technical assistance. An extensive communications network links field with factory to assure that each customer can quickly obtain the information and help needed.

Quality and Reliability

Quality and reliability are very important concepts to Hewlett-Packard in maintaining the commitment to product performance.

At Hewlett-Packard, quality is integral to product development, manufacturing, and final introduction. "Parts per million" (PPM), as a measure of quality, is used in HP's definition of product assurance. And HP's commitment to quality means that there is a continuous process of improvement and tightening of quality standards. Manufacturing quality circles and quality testing programs are important ingredients in HP products.

Reliability testing is also required for the introduction of new HP components. Lifespan calculations in "mean-time-between-failure" (MTBF) terms are published and available as reliability data sheets. HP's stringent reliability testing assures long component lifetimes and consistent product performance.



About This Catalog

To help you choose and design with Hewlett-Packard optoelectronic components, this catalog includes detailed specifications for HP component products. The catalog is divided into nine sections:

1. Motion Sensing and Encoder Products
2. LED Light Bars and Bar Graph Arrays
3. LED Lamps
4. LED Displays
5. Fiber Optics
6. Optocouplers
7. Electrophotographic Products
8. Applications
9. Appendix

How to Find the Right Information

- The Table of Contents (p. iii) helps you to locate the product sections as well as the selection guides for each of the product sections.
- An alphanumeric index (p. iv) lists every component represented in this catalog.
- Selection guides at the beginning of each of the seven product sections, contain basic product specifications which allows you to quickly select products most suitable for your application.

Following the product sections is a complete listing of application bulletins and notes which are frequently useful as design aids. The final section is an appendix containing HP sales, service, and authorized distributor locations.

How to Order

To order any component in this catalog or additional applications information, call the HP office nearest you and ask for a Components representative. A complete listing of the U.S. sales offices is on page 9-7; offices located outside of the U.S. are listed on page 9-8.

A world-wide listing of HP authorized distributors is on page 9-3. These distributors can offer off-the-shelf delivery for most HP components.

If you need technical assistance, please call our Customer Information Center at 1-800-752-0900.

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Bold = New Product

*Not recommended for new design; contact your local Sales Representative for further information (see Section 9).

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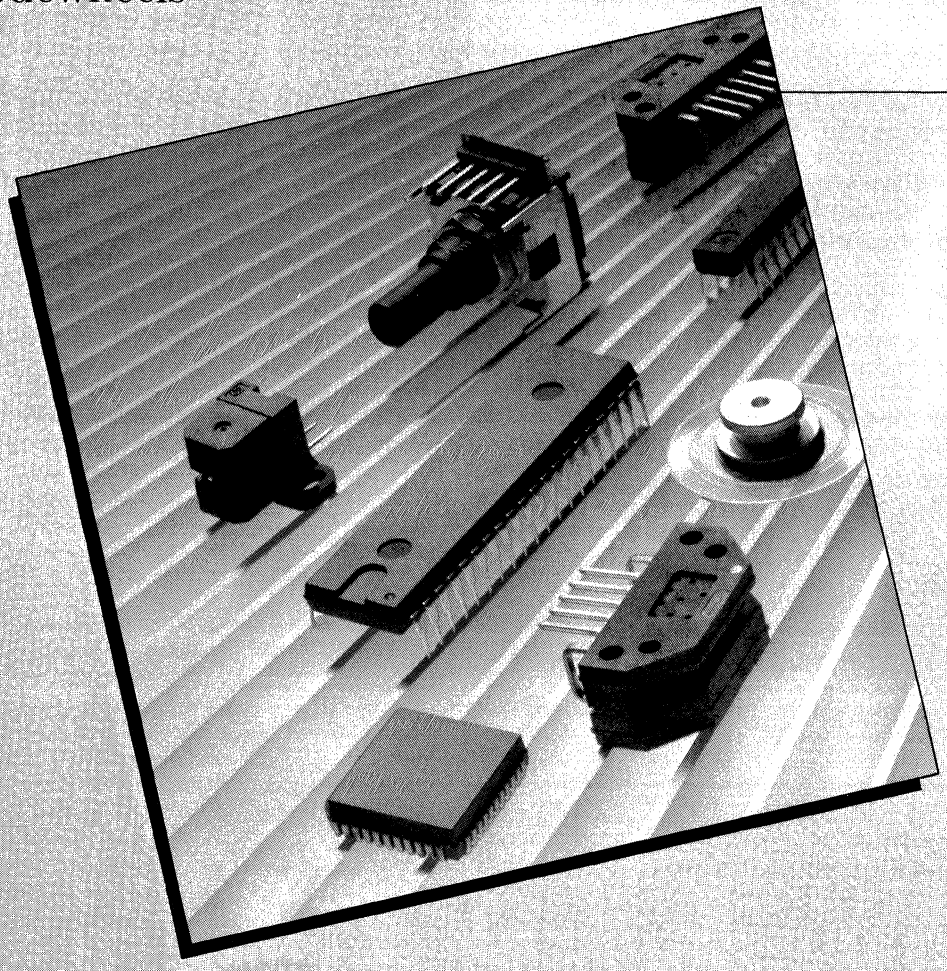
Bold = New Product

HEWLETT PACKARD

Motion Sensing and Control

- Optical Encoder Modules
- Optical Encoders
- Rotary Pulse Generators
- Motion Control ICs
- Codewheels



Motion Sensing and Control

Motion Sensing and Control

Hewlett-Packard's growing family of motion sensing and control products developed as an extension of our emitter/detector systems capabilities. Motion sensing products include optical shaft encoders and optical encoder modules for closed-loop servo applications, and rotary pulse generators for manual input applications. HP's optical products provide a digital link converting mechanical shaft rotation into TTL logic level signals. HP's motion control ICs complement the optical products and greatly simplify the design of digital motion control systems.

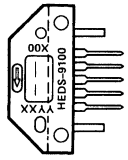
Our HEDS-9000, HEDS-9100, HEDS-9200, and HEDS-9700 series optical encoder modules provide sophisticated motion detection at a low price, making them ideal for high volume applications such as printer, plotters, and industrial automation equipment. The HEDS-9000 and HEDS-9100 are now available in three channel versions, the HEDS-9040 and 9140, which provide a third channel index pulse in addition to the standard two channel outputs. The HEDS-9200 series linear encoder module uses the same emitter/detector technology as the HEDS-9000 to sense linear position. The HEDS-9700 comes in a super small, wave solderable package with a variety of mounting options.

The HEDS-5500 and HEDS-5600 series are complete, quick assembly, low cost optical shaft encoders. No adhesives or last minute adjustments are necessary for assembly. In addition, the HEDS-5540 and HEDS-5640 provide a third channel index pulse for home position sensing. The HEDS-5500 and 5600 series encoders offer a complete solution in industrial, medical, and office automation equipment.

Hewlett-Packard's new HRPG series of low cost miniature rotary pulse generators (RPGs) use reflective optics technology for superior reliability and consistent rotational feel for more than 1 million revolutions. The HRPG is ideal for front panel applications such as test and measurement equipment, medical equipment, CAD/CAM systems, and audio/video equipment. The HRPG is available in a variety of configurations including smooth or detented turning, multiple terminations and mounting options, and a wide selection of shaft configurations.

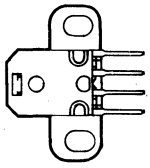
To complement the motion sensing products, HP has released two motion control IC families. The HCTL-1100 CMOS general purpose motion control IC performs all of the time-intensive tasks of digital motion control. The HCTL-1100 controls position or velocity while using an incremental encoder for feedback information. The HCTL-1100 is also available in a surface mount package. The HCTL-2000, HCTL-2016, and HCTL-2020 Quadrature Decoder/Counter ICs provide a one chip, easy to implement solution to interfacing the quadrature output of an encoder or RPG to a microprocessor. These CMOS ICs include a quadrature decoder, a 12 or 16 bit up/down counter, and an 8 bit bus interface. In addition, the HCTL-2020 has cascade output signals as well as quadrature decoder output signals.

Optical Encoder Modules

Package Outline Drawing	Part No.	Channels	Resolution	Page No.
	HEDS-9000 OPT☐ 00	A, B	☐ A 500 CPR B 1000 CPR	1-12
	HEDS-9040 OPT☐ 00	A, B, I	☐ B 1000 CPR J 1024 CPR	1-22
	HEDS-9100 OPT☐ 00	A, B	☐ K 96 CPR C 100 CPR D 192 CPR E 200 CPR F 256 CPR G 360 CPR H 400 CPR A 500 CPR I 512 CPR	1-12
	HEDS-9140 OPT☐ 00	A, B, I	☐ F 256 CPR G 360 CPR A 500 CPR I 512 CPR	1-22
	HEDS-9200 OPT☐ 00	A, B	☐ L 120 LPI M 127 LPI P 150 LPI Q 180 LPI R 200 LPI	1-18

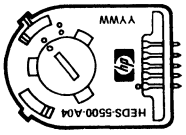
Bold Type – New Product

Small Optical Encoder Modules – HEDS-9700 Series

Package Outline Drawing	Part No.	Lead Bend	Channels	Resolution	Mounting Options	Page No.
	**HEDS-9700** OPT [1][2][2]	Straight	A, B	[1] K 96 CPR C 100 CPR D 192 CPR E 200 CPR F 256 CPR G 360 CPR H 400 CPR	[2][2] 50 – Standard 51 – Rounded Outline 52 – Backplane 53 – Standard w/Posts 54 – Tabless 55 – Backplane w/Posts	1-31
	HEDS-9701 OPT [1][2][2]	Bent	A, B			
	HEDS-9720 OPT [3][2][2]	Straight	A, B	[3] L 120 LPI M 127 LPI P 150 LPI		
	HEDS-9721 OPT [3][2][2]	Bent	A, B			

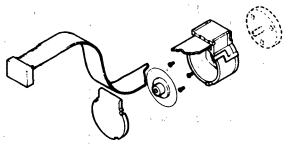
Bold Type – New Product

Quick Assembly Encoder – HEDS-5500 Series

Package Outline Drawing	Part No.	Channels	Mounting Type	Through Hole	Resolution	Shaft Size	Page No.
	HEDS-5500 OPT [1][2][2]	A, B	Standard	None	[1] K 96 CPR C 100 CPR	[2][2] 01 2 mm 02 3 mm	1-41
	HEDS-5505 OPT [1][2][2]	A, B	Standard	8.9 mm (0.35 in.)	D 192 CPR E 200 CPR	03 1/8 in. 04 5/32 in.	
	HEDS-5600 OPT [1][2][2]	A, B	External Mounting Ears	None	F 256 CPR G 360 CPR	05 3/16 in. 06 1/4 in.	
	HEDS-5605 OPT [1][2][2]	A, B	External Mounting Ears	8.9 mm (0.35 in.)	H 400 CPR A 500 CPR I 512 CPR	11 4mm 14 5 mm 12 6 mm	
	HEDS-5540 OPT [3][2][2]	A, B, I	Standard	None	[3] F 256 CPR G 360 CPR	13 8 mm	
	HEDS-5545 OPT [3][2][2]	A, B, I	Standard	8.9 mm (0.35 in.)	A 500 CPR I 512 CPR		
	HEDS-5640 OPT [3][2][2]	A, B, I	External Mounting Ears	None			
	HEDS-5645 OPT [3][2][2]	A, B, I	External Mounting Ears	8.9 mm (0.35 in.)			

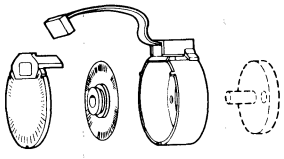
Bold Type – New Product

28 mm Encoders – HEDS-5000 Series

Package Outline Drawing	Part No.	Channels	Option Code		Page No.
			Resolution	Shaft Size	
	HEDS-5000 OPT. [1][2][2]	A, B	[1] C 100 CPR D 192 CPR E 200 CPR	[2][2] 01 2 mm 02 3 mm 03 1/8 in.	*
	HEDS-5010 OPT [1][2][2]	A, B, I	F 256 CPR G 360 CPR H 400 CPR A 500 CPR I 512 CPR	04 5/32 in. 05 3/16 in. 06 1/4 in. 11 4 mm 14 5 mm 12 6 mm	

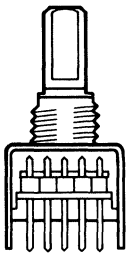
*Contact your local Sales Representative for information regarding this product. (See Section 9.)

56 mm Encoders – HEDS-6000 Series

Package Outline Drawing	Part No.	Channels	Option Code		Page No.
			Resolution	Shaft Size	
	HEDS-6000 OPT. [1][2][2]	A, B	[1] D 192 CPR E 200 CPR H 400 CPR A 500 CPR	[2][2] 05 3/16 in. 06 1/4 in. 07 5/16 in.	*
	HEDS-6010 OPT [1][2][2]	A, B, I	I 512 CPR B 1000 CPR J 1024 CPR	08 3/8 in. 09 1/2 in. 10 5/8 in. 11 4 mm 12 6 mm 13 8 mm	

*Contact your local Sales Representative for information regarding this product. (See Section 9.)

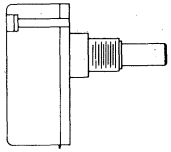
Rotary Pulse Generator – HRPG Series

Package Outline Drawing	Part No.	Shaft Feel/ Resolution*	Mechanical Configuration	Termination	Page No.
	HRPG- A[1][1][1] OPT [2][2][3]	[1][1][1] S16 – Smooth 16 CPR D16 – Detented 16 CPR S 32 – Smooth 32 CPR D32 – Detented 32 CPR S64 – Smooth 64 CPR SCA – Smooth 120 CPR	[2][2] 11 – 0.3" x 0.25" 13 – 0.3" x 0.25" D-cut 14 – 0.5" 0.25" 16 – 0.5" x 0.25" D-cut 17 – 0.8" x 0.25" 19 – 0.8" x 0.25" D-cut 51 – 7.6 mm x 6 mm 53 – 7.6 mm x 6 mm D-cut 54 – 12.7 mm x 6 mm 56 – 12.7 mm x 6 mm D-cut 57 – 20.3 mm x 6 mm 59 – 20.3 mm x 6 mm D-cut	[3] F – Pins Front with Bracket R – Pins Rear with Bracket C – Cable Connector with Strain Relief	1-51

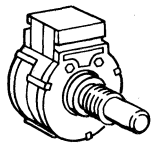
*When ordering detented versions, a D-cut shaft is recommended.

Bold Type – New Product

Rotary Pulse Generator – HEDS-5700

Package Outline Drawing	Part No.	Termination	Resolution	Shaft Configuration	Drag Option	Page No.
			[1]	[2]	[3]	1-59
	HEDS-5700	Pins	K 96 CPR	0 – 0.25" dia	0 – free spinning	
	OPT [1][2][3]		C 100 CPR	1 – 6 mm dia	1 – static drag	
	HEDS-5701	6" Color Coded Leads	D 192 CPR	2 – 0.25" dia D-cut		
	OPT [1][2][3]		E 200 CPR			
			F 256 CPR			
			G 360 CPR			
			H 400 CPR			
			A 500 CPR			
			I 512 CPR			

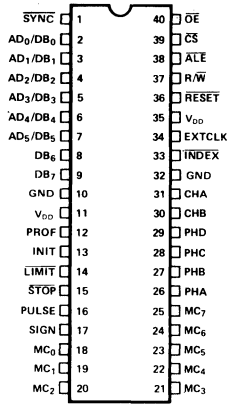
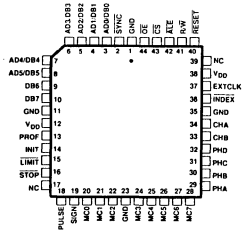
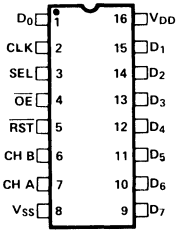
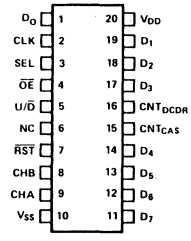
Rotary Pulse Generator – HEDS-7500

Package Outline Drawing	Part No.	Resolution	Channels	Termination	Page No.
	HEDS-7500	256 CPR	A, B	Color Coded Wire	*
	HEDS-7501	256 CPR	A, B	Ribbon Cable	
	HEDS-7502	256 CPR	A, B, I	Color Coded Wire	
	HEDS-7503	256 CPR	A, B, I	Ribbon Cable	

Bold Type – New Product

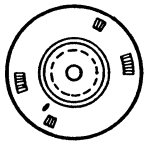
*Contact your local Sales Representative for information regarding this product. (See Section 9.)

Motion Control ICS – HCTL-XXXX Series

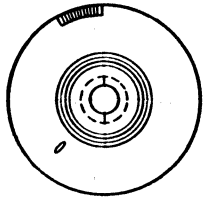
Package Outline Drawing	Part No.	Package	Description	Page No.
	**HCTL-1100**	PDIP	CMOS General Purpose Motion Control IC	1-77
	**HCTL-1100** OPT PLC	PLCC	CMOS General Purpose Motion Control IC	
	HCTL-2000	PDIP	CMOS Quadrature Decoder/Counter IC, 12-bit Counter	1-61
	HCTL-2016	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	
	**HCTL-2020**	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	

Bold Type – New Product

Codewheels – 11.00 mm (0.433 in) Optical Radius

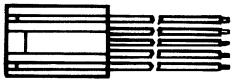
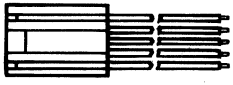
Package Outline Drawing	Part No.	Matching Encoder Module	Channels	Resolution	Shaft Size	Page No.
	**HEDS-5120** OPT [1][2][2]	HEDS-9100 HEDS-9700	A, B	[1] K 96 CPR C 100 CPR D 192 CPR E 200 CPR F 256 CPR G 360 CPR H 400 CPR A 500 CPR I 512 CPR	[2][2] 01 2 mm 02 3 mm 03 1/8 in. 04 5/32 in. 05 3/16 in. 06 1/4 in. 11 4 mm 14 5 mm 12 6 mm 13 8 mm	1-12 1-31
	HEDS-5140 OPT [3][2][2]	HEDS-9140	A, B, I	[2] F 256 CPR G 360 CPR A 500 CPR I 512 CPR		1-22

Codewheels – 23.36 mm (0.920 in) Optical Radius

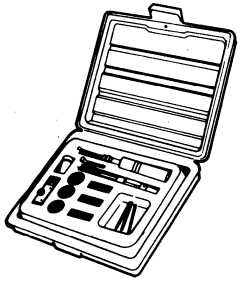
Package Outline Drawing	Part No.	Matching Encoder Module	Channels	Resolution	Shaft Size	Page No.
	HEDS-6100 OPT [1][2][2]	HEDS-9000	A, B	[1] D 192 CPR E 200 CPR H 400 CPR A 500 CPR I 512 CPR B 1000 CPR J 1024 CPR	[2][2] 05 3/16 in. 06 1/4 in. 07 5/16 in. 08 3/8 in. 09 1/2 in. 10 5/8 in. 11 4 mm 12 6 mm 13 8 mm	1-12
	HEDS-6140 OPT [3][2][2]	HEDS-9140	A, B, I	[3] B 1000 CPR J 1024 CPR		1-22

Bold Type – New Product

Accessories for Encoders and Encoder Modules

Package Outline Drawing	Part No.	Description	Page No.
	**HEDS-8902**	4-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5500 and HEDS-5600 2 channel encoders. Also fits HEDS-9000, HEDS-9100, and HEDS-9200 2 channel encoder modules.	1-41 1-12 1-18
	**HEDS-8903**	5-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5540 and HEDS-5640 three channel encoders. Also fits HEDS-9040 and HEDS-9140 three channel encoder modules.	1-41 1-22
	HEDS-8905	Alignment Tool for HEDS-9140	1-22
	HEDS-8906	Alignment Tool for HEDS-9040	1-22
	HEDS-8910 OPT 0 □□	Alignment Tool for HEDS-5540/5545 and HEDS-5640/5645. Order in appropriate shaft size.	1-41

Convenience Assembly Tools for 28 mm Diameter Encoders – Not Required

Package Outline Drawing	Part No.	Description	Page No.
	HEDS-8930	HEDS-5000 Series Tool Kit • Holding Screwdriver • Torque Limiting Screwdriver • HEDS-8920 Hub Puller • HEDS-8922 Gap Setter	*
	HEDS-892X	Centering Cones • Aid in High Volume Assembly • Order in Appropriate Shaft Size	

Bold Type – New Product

*Contact your local Sales Representative for information regarding this product. (See Section 9.)

HEWLETT PACKARD

Two Channel Optical Incremental Encoder Module

Technical Data

HEDS-9000
HEDS-9100

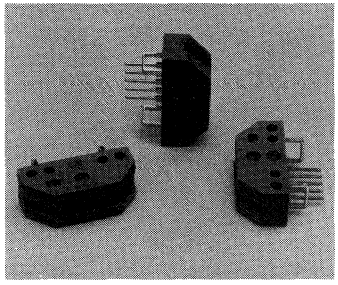
Features

- **High Performance**
- **High Resolution**
- **Low Cost**
- **Easy to Mount**
- **No Signal Adjustment Required**
- **Insensitive to Radial and Axial Play**
- **Small Size**
- **-40°C to 100°C Operating Temperature**
- **Two Channel Quadrature Output**
- **TTL Compatible**
- **Single 5 V Supply**

Description

The HEDS-9000 and HEDS-9100 series are high performance, low cost, optical incremental encoder modules. When used with a codewheel, these modules detect rotary position. The modules consist of a lensed LED source and a detector IC enclosed in a small C-shaped plastic package. Due to a highly collimated light source and a unique photo-detector array, the modules are extremely tolerant to mounting misalignment.

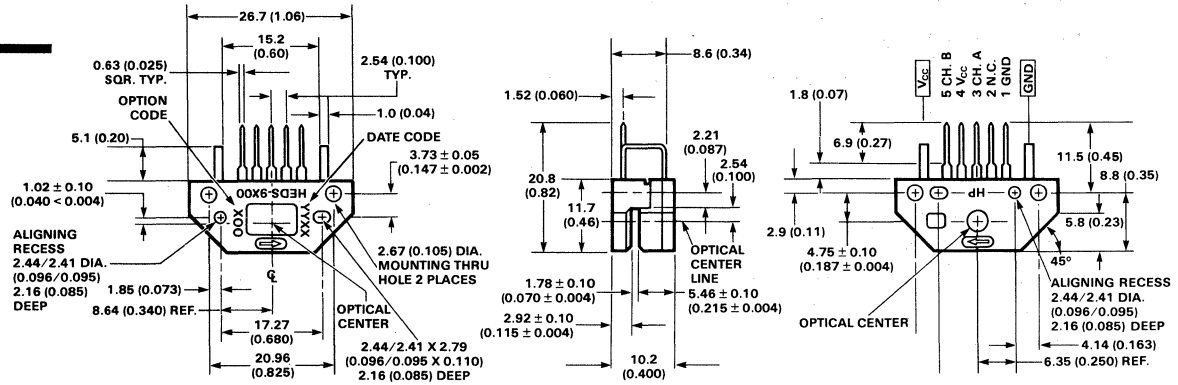
The two channel digital outputs and the single 5 V supply input



are accessed through five 0.025 inch square pins located on 0.1 inch centers.

Standard resolutions for the HEDS-9000 are 500 CPR and 1000 CPR for use with a HEDS-

Package Dimensions



ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

6100 codewheel or equivalent. For the HEDS-9100, standard resolutions between 96 CPR and 512 CPR are available for use with a HEDS-5120 codewheel or equivalent.

Applications

The HEDS-9000 and 9100 provide sophisticated motion detection at a low cost, making them ideal for high volume applications. Typical applications include printers, plotters, tape drives, and factory automation equipment.

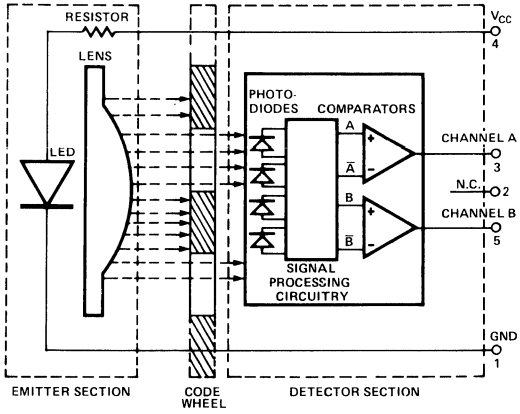
Theory of Operation

The HEDS-9000 and 9100 are C-shaped emitter/detector modules. Coupled with a codewheel, they translate the rotary motion of a shaft into a two-channel digital output.

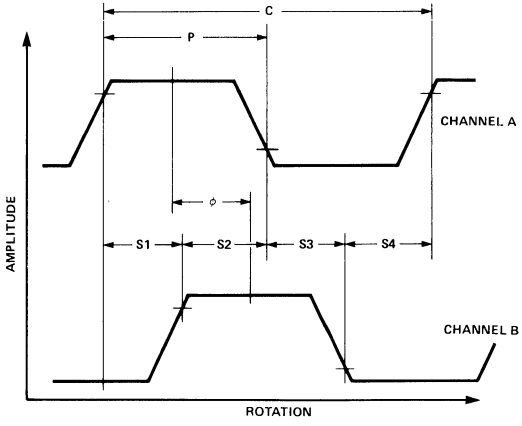
As seen in the block diagram, each module contains a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single polycarbonate lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel rotates between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and design of the codewheel. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\overline{A}$, B, and $\overline{B}$. Two comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

Block Diagram



Output Waveforms



Definitions

Count (N) = The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

1 Shaft Rotation = 360 mechanical degrees
= N cycles
1 cycle (c) = 360 electrical degrees (°e)
= 1 bar and window pair

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Absolute Maximum Ratings

Storage Temperature, T_S ..... -40°C to 100°C
Operating Temperature, T_A ..... -40°C to 100°C
Supply Voltage, V_{CC} ..... -0.5 V to 7 V
Output Voltage, V_O ..... -0.5 V to V_{CC}
Output Current per Channel, I_O ..... -1.0 mA to 5 mA

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error (Δϕ): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates in the direction of the arrow on top of the module, channel A will lead channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (R_{OP}): The distance from the codewheel's center of rotation to the optical center (O.C.) of the encoder module.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T	–40		100	°C	
Supply Voltage	V_{CC}	4.5		5.5	Volts	Ripple < 100 mV_{p-p}
Load Capacitance	C_L			100	pF	3.2 kΩ pull-up resistor
Count Frequency	f			100	kHz	$\frac{\text{Velocity (rpm) x N}}{60}$

Note: The module performance is guaranteed to 100 kHz but can operate at higher frequencies.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances. These characteristics do not include codewheel contributions.

Parameter	Sym.	Typ.	Case 1 Max.	Case 2 Max.	Units	Notes
Pulse Width Error	ΔP	7	30	40	°e	
Logic State Width Error	ΔS	5	30	40	°e	
Phase Error	Δϕ	2	10	15	°e	

Case 1: Modules mounted on tolerances of ±0.13 mm (0.005").
Case 2: HEDS-9000 mounted on tolerances of ±0.50 mm (0.020").
HEDS-9100 mounted on tolerances of ±0.38 mm (0.015").

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, typical at 25°C.

Parameter	Symbol	Min.	Typical	Max.	Units	Notes
Supply Current	I_{CC}		17	40	mA	
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40 µA max.
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA
Rise Time	t_r		200		ns	C_L = 25 pF
Fall Time	t_f		50		ns	R_L = 11 kΩ pull-up

Recommended Codewheel Characteristics

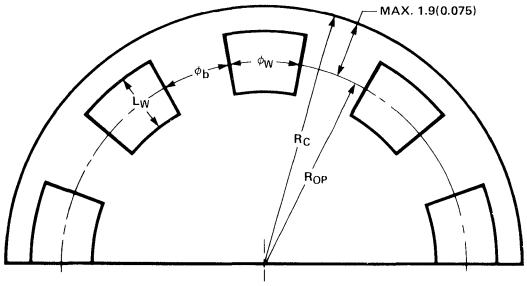


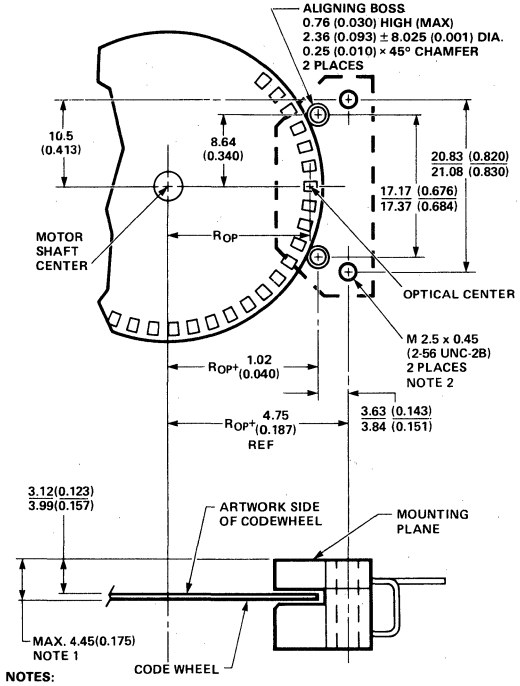
Figure 1. Codewheel Design.

Codewheel Options

HEDS Series	CPR (N)	Option	Optical Radius mm (in.)
5120	96	K	11.00 (0.433)
5120	100	C	11.00 (0.433)
5120	192	D	11.00 (0.433)
5120	200	E	11.00 (0.433)
5120	256	F	11.00 (0.433)
5120	360	G	11.00 (0.433)
5120	400	H	11.00 (0.433)
5120	500	A	11.00 (0.433)
5120	512	I	11.00 (0.433)
6100	500	A	23.36 (0.920)
6100	1000	B	23.36 (0.920)

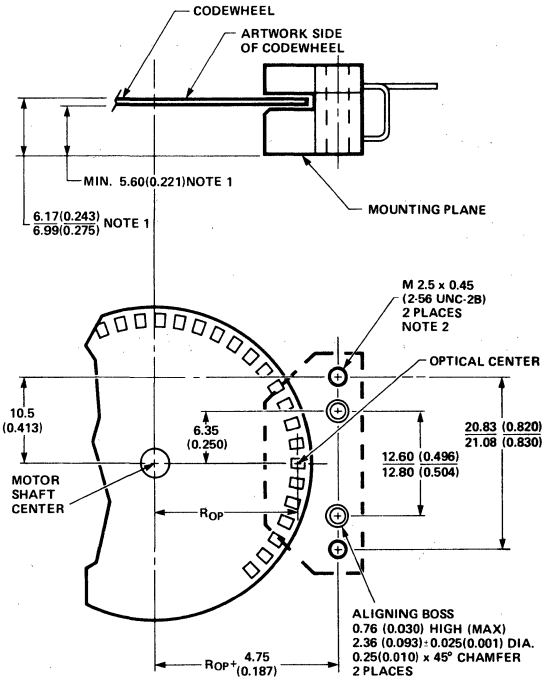
Parameter	Symbol	Minimum	Maximum	Units	Notes
Window/Bar Ratio	ϕ_w/ϕ_b	0.7	1.4		
Window Length	L_w	1.8 (0.07)	2.3 (0.09)	mm (inch)	
Absolute Maximum Codewheel Radius	R_C		R_{OP} + 1.9 (0.075)	mm (inch)	Includes eccentricity errors

Mounting Considerations



NOTES:
1. THESE DIMENSIONS INCLUDE SHAFT END PLAY, AND CODEWHEEL WARP.
2. MAXIMUM RECOMMENDED MOUNTING SCREW TORQUE IS 4 kg-cm (3.5 in-lbs).

Figure 2. Mounting Plane Side A.



NOTES:
1. THESE DIMENSIONS INCLUDE SHAFT END PLAY, AND CODEWHEEL WARP.
2. MAXIMUM RECOMMENDED MOUNTING SCREW TORQUE IS 4 kg-cm (3.5 in-lbs).

Figure 3. Mounting Plane Side B.

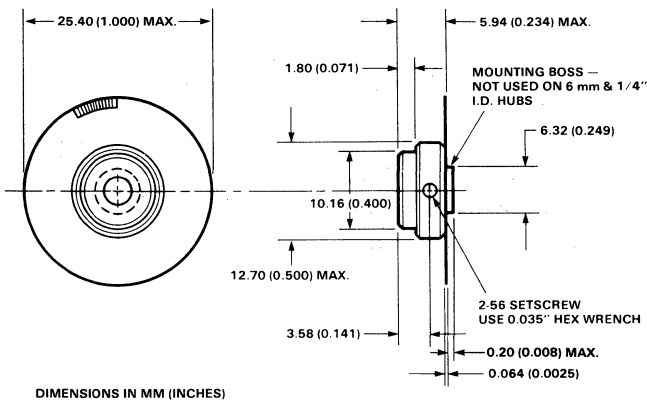


Figure 4. HEDS-5120 Codewheel.

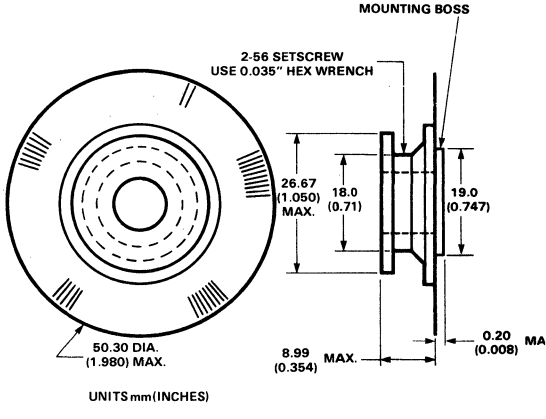


Figure 5. HEDS-6100 Codewheel.

Connectors

Manufacturer	Part Number	Mounting Surface
AMP	103686-4 640442-5	Both Side B
DuPont	65039-032 with 4825X-000 term.	Both
HP	HEDS-8902 with 4-wire leads	Side B (see Fig. 6)
Molex	2695 series with 2759 series term.	Side B

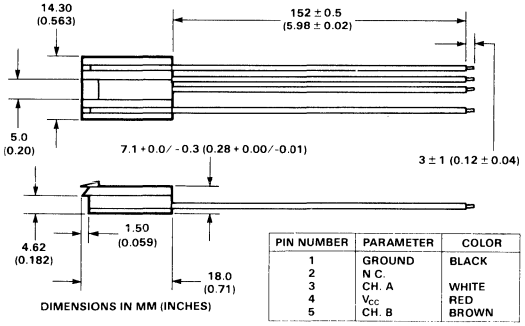


Figure 6. HEDS-8902 Connector.

Ordering Information

HEDS-9000 Option ☐ 0 0 **HEDS-6100 Option** ☐ ☐ ☐

Resolution (Cycles/Rev)
A - 500 CPR
B - 1000 CPR

Shaft Diameter	
05 - 3/16 in.	10 - 5/8 in.
06 - 1/4 in.	11 - 4 mm
07 - 5/16 in.	12 - 6 mm
08 - 3/8 in.	13 - 8 mm
09 - 1/2 in.	

HEDS-9100 Option ☐ 0 0 **HEDS-5120 Option** ☐ ☐ ☐

Resolution (Cycles/Rev)	
K - 96 CPR	G - 360 CPR
C - 100 CPR	H - 400 CPR
D - 192 CPR	A - 500 CPR
E - 200 CPR	I - 512 CPR
F - 256 CPR	

Shaft Diameter	
01 - 2 mm	11 - 4 mm
02 - 3 mm	14 - 5 mm
03 - 1/8 in.	12 - 6 mm
04 - 5/32 in.	13 - 8 mm
05 - 3/16 in.	
06 - 1/4 in.	

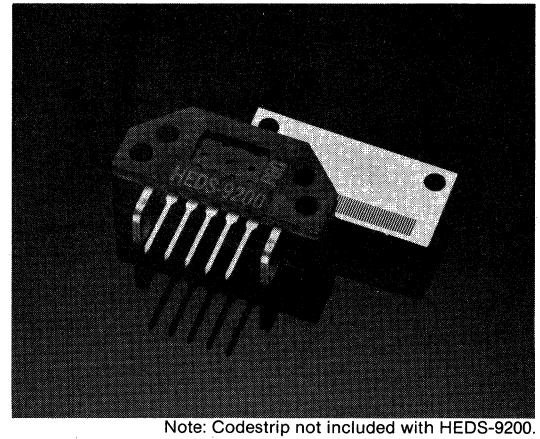
HEWLETT PACKARD

LINEAR OPTICAL INCREMENTAL ENCODER MODULE

HEDS-9200 SERIES

Features

- **HIGH PERFORMANCE**
- **HIGH RESOLUTION**
- **LOW COST**
- **EASY TO MOUNT**
- **NO SIGNAL ADJUSTMENT REQUIRED**
- **INSENSITIVE TO MECHANICAL DISTURBANCES**
- **SMALL SIZE**
- **-40° C TO 100° C OPERATING TEMPERATURE**
- **TWO CHANNEL QUADRATURE OUTPUT**
- **TTL COMPATIBLE**
- **SINGLE 5 V SUPPLY**



Note: Codestrip not included with HEDS-9200.

Description

The HEDS-9200 series is a high performance, low cost, optical incremental encoder module. When operated in conjunction with a codestrip, this module detects linear position. The module consists of a lensed LED source and a detector IC enclosed in a small C-shaped plastic package. Due to a highly collimated light source and a unique photo-detector array, the module is extremely tolerant to mounting misalignment.

The two channel digital outputs and the single 5 V supply input are accessed through four 0.025 inch square pins located on 0.1 inch centers.

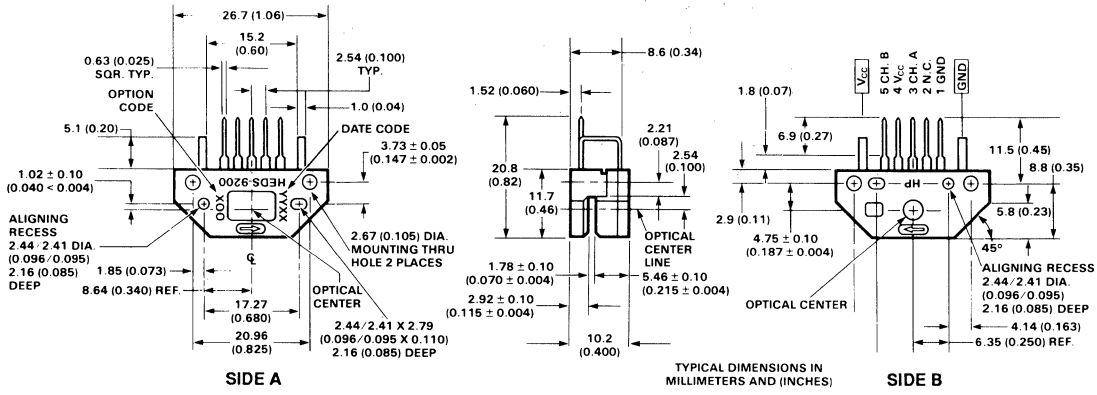
Five standard resolutions between 4.72 counts per mm (120 counts per inch) and 7.87 counts per mm (200 counts per inch) are available. Consult local Hewlett-Packard sales representatives for other resolutions ranging from 1.5 to 7.87 counts per mm (40 to 200 counts per inch).

Applications

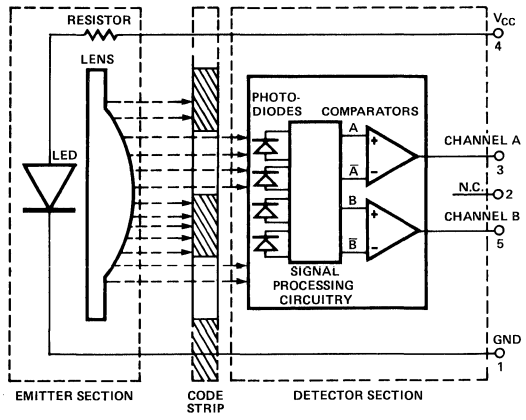
The HEDS-9200 provides sophisticated motion detection at a low cost, making it ideal for high volume applications. Typical applications include printers, plotters, tape drives, and factory automation equipment.

ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

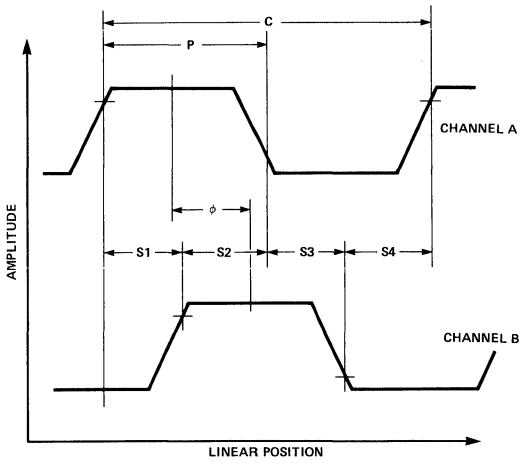
Package Dimensions



Block Diagram



Output Waveforms



Theory of Operation

The HEDS-9200 is a C-shaped emitter/detector module. Coupled with a codestrip it translates linear motion into a two-channel digital output.

As seen in the block diagram, the module contains a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single polycarbonate lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codestrip moves between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codestrip. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the count density of the codestrip. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\overline{A}$, B and $\overline{B}$. Two comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

Definitions

Count density (D): The number of bar and window pairs per unit length of the codestrip.

Pitch: 1/D, The unit length per count.

Electrical degree (° e): Pitch/360, The dimension of one bar and window pair divided by 360.

1 cycle (C): 360 electrical degrees, 1 bar and window pair.

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180° e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180° e.

State Width(S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90° e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90° e.

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90° e for quadrature output.

Phase Error ($\Delta\phi$): The deviation of the phase from its ideal value of 90° e.

Direction of Movement: When the codestrip moves, relative to the module, in the direction of the arrow on top of the module, channel A will lead channel B. If the codestrip moves in the opposite direction, channel B will lead channel A.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Storage Temperature	T_S	-40		100	°C	
Operating Temperature	T_A	-40		100	°C	
Supply Voltage	V_{CC}	-0.5		7	Volts	
Output Voltage	V_O	-0.6		V_{CC}	Volts	
Output Current per Channel	I_O	-1.0		5	mA	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T	-40		100	°C	
Supply Voltage	V_{CC}	4.5		5.5	Volts	Ripple < 100 m Vp-p
Load Capacitance	C_L			100	pF	3.2 KΩ pull-up resistor
Count Frequency	f			100	kHz	Velocity X D

Note:
The module performance is guaranteed to 100 kHz but can operate at higher frequencies.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances. These characteristics do not include codestrip defects.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Pulse Width Error	ΔP		7	35	elec. deg.	
Logic State Width Error	ΔS		5	35	elec. deg.	
Phase Error	$\Delta\phi$		2	13	elec. deg.	

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, typical at 25° C

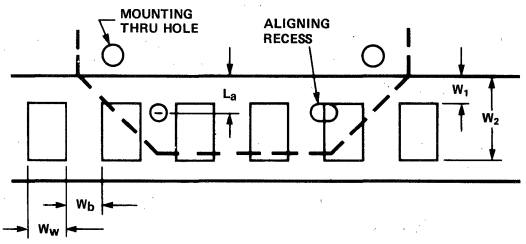
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		17	40	mA	
High Level Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -40 μA Max.
Low Level Output Voltage	V_{OL}			0.4	Volts	I_{OL} = 3.2 mA
Rise Time	t_r		200		ns	C_L = 25 pF
Fall Time	t_f		50		ns	R_L = 11 KΩ pull-up

Note:
1. For improved performance in noisy environments or high speed applications, a 3.3 kΩ pull-up resistor is recommended.

Recommended Codestrip Characteristics

Codestrip design must take into consideration mounting as referenced to either side A *or* side B (See figure 1).

MOUNTING AS REFERENCED TO SIDE A



MOUNTING AS REFERENCED TO SIDE B

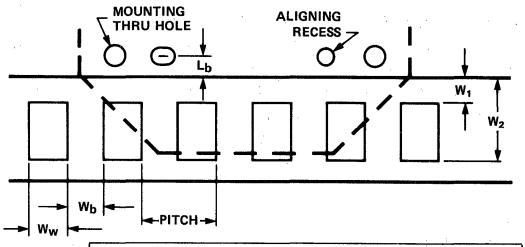


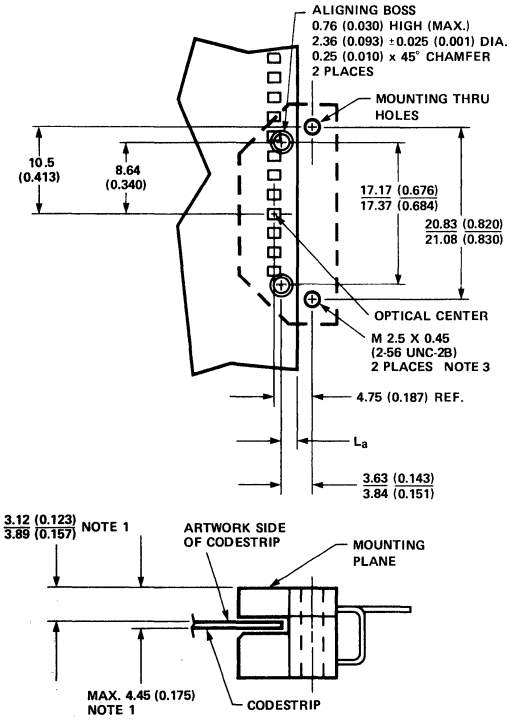
Figure 1. Codestrip Design

STATIC CHARGE WARNING: LARGE STATIC CHARGE ON CODESTRIP MAY HARM MODULE. PREVENT ACCUMULATION OF CHARGE.

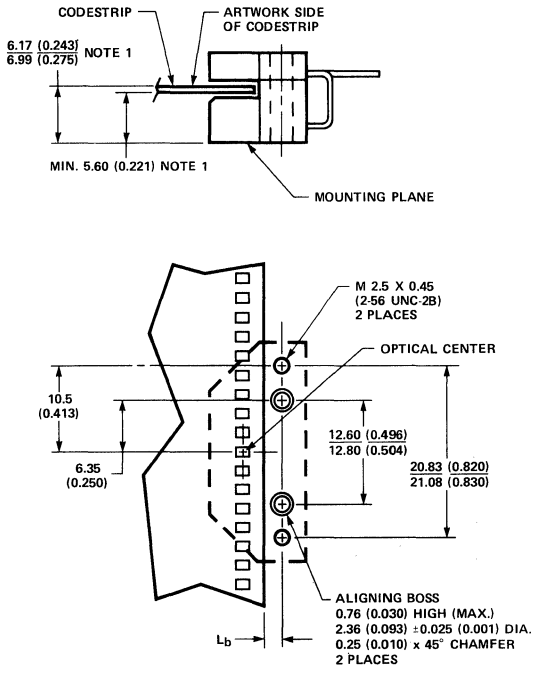
Parameter	Symbol	Mounting Ref. Side A	Mounting Ref. Side B	Units
Window/Bar Ratio	W_w/W_b	0.7 Min. 1.4 Max.	0.7 Min. 1.4 Max.	
Mounting Distance	L	$L_a \leq 0.51$ (0.020)	$L_b \geq 3.23$ (0.127)	mm (inch)
Codestrip edge to inside window edge	W_1	$W_1 \leq 0.53$ (0.021) + L_a	$W_1 \leq 4.27$ (0.168) - L_b	mm (inch)
Codestrip edge to outside window edge	W_2	$W_2 \geq 1.50$ (0.059) + L_a	$W_2 \geq 5.23$ (0.206) - L_b	mm (inch)

Note:
All parameters and equations must be satisfied over the full length of codestrip travel including maximum codestrip runout.

Mounting Considerations



MOUNTING PLANE SIDE A



MOUNTING PLANE SIDE B

Notes:
1. These dimensions include codestrip warp.
2. Reference definitions of L_a and L_b on page 3.
3. Maximum recommended mounting screw torque is 4 kg-cm (3.5 in-lbs).

Connectors

Manufacturer	Part Number	Mounting Surface
AMP	103686-4	Both
	640442-5	Side B
DuPont	65039-032 with 4825X-000 term.	Both
HP	HEDS-8902 with 4-wire leads	Side B
Molex	2695 series with 2759 series term.	Side B

Ordering Information

HEDS-9200 Option [ ] [0] [0]

RESOLUTION Counts per mm (inch)	PITCH mm (inch) per count
L - 4.72 (120)	0.212 (0.0083)
M - 5.00 (127)	0.200 (0.0079)
P - 5.91 (150)	0.169 (0.0067)
Q - 7.09 (180)	0.141 (0.0056)
R - 7.87 (200)	0.127 (0.0050)

Consult local Hewlett-Packard sales representatives for other resolutions.

HEWLETT PACKARD

Three Channel Optical Incremental Encoder Modules

Technical Data

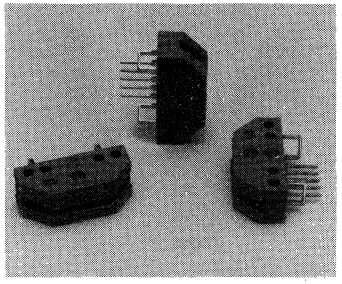
HEDS-9040
HEDS-9140

Features

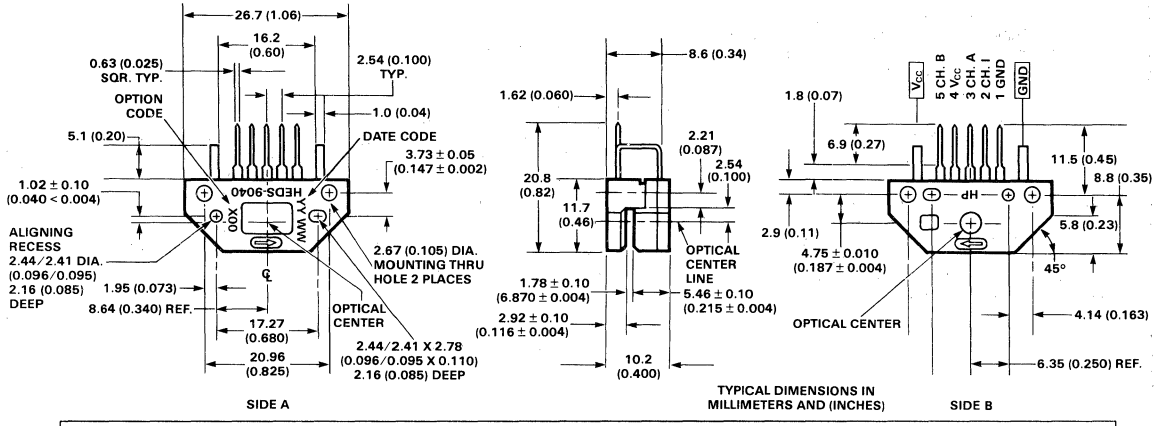
- **Two Channel Quadrature Output with Index Pulse**
- **Resolution Up to 1024 Counts Per Revolution**
- **Low Cost**
- **Easy to Mount**
- **No Signal Adjustment Required**
- **Small Size**
- **-40°C to100°C Operating Temperature**
- **TTL Compatible**
- **Single 5 V Supply**

Description

The HEDS-9040 and HEDS-9140 series are three channel optical incremental encoder modules. When used with a codewheel, these low cost modules detect rotary position. Each module consists of a lensed LED source and a detector IC enclosed in a small plastic package. Due to a highly collimated light source and a unique photodetector array, these modules provide the same high performance found in the HEDS-9000/9100 two channel encoder family.



Package Dimensions



ESD WARNING; NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

The HEDS-9040 and 9140 have two channel quadrature outputs plus a third channel index output. This index output is a 90 electrical degree high true index pulse which is generated once for each full rotation of the codewheel.

The HEDS-9040 is designed for use with a HEDS-6140 codewheel which has an optical radius of 23.36 mm (0.920 inch). The HEDS-9140 is designed for use with a HEDS-5140 codewheel which has an optical radius of 11.00 mm (0.433 inch).

The quadrature signals and the index pulse are accessed through five 0.025 inch square pins located on 0.1 inch centers.

Standard resolutions between 256 and 1024 counts per revolution are available. Consult local Hewlett-Packard sales representatives for other resolutions.

Applications

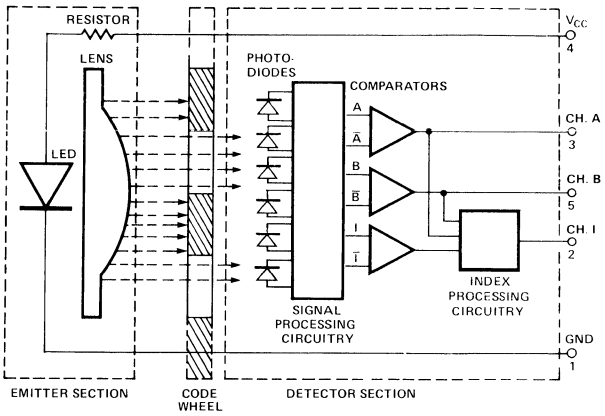
The HEDS-9040 and 9140 provide sophisticated motion control detection at a low cost, making then ideal for high volume applications. Typical applications include printers, plotters, tape drives, and industrial and factory automation equipment.

Theory of Operation

The HEDS-9040 and 9140 are emitter/detector modules. Coupled with a codewheel, these modules translate the rotary motion of a shaft into a three-channel digital output.

As seen in the block diagram, the modules contain a single

Block Diagram

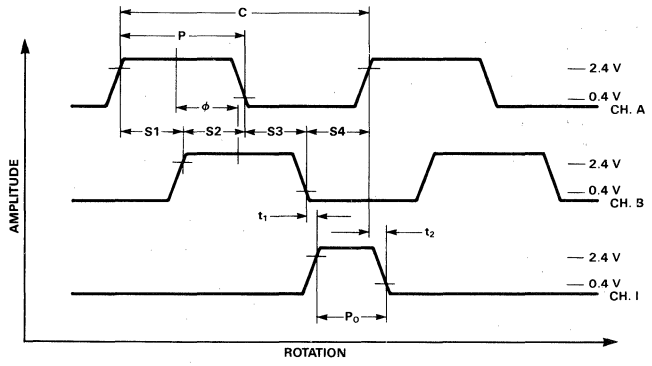


Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single polycarbonate lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel rotates between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and design of the codewheel. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\overline{A}$, B, $\overline{B}$, I and $\overline{I}$. Comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

The output of the comparator for I and $\overline{I}$ is sent to the index processing circuitry along with the outputs of channels A and B. The final output of channel I is an index pulse P_0 which is generated once for each full rotation of the codewheel. This output P_0 is a one state width (nominally 90 electrical degrees), high true index pulse which is coincident with the low states of channels A and B.

Output Waveforms



Definitions

Count (N): The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

One Cycle (C): 360 electrical degrees (°e), 1 bar and window pair.

One Shaft Rotation: 360 mechanical degrees, N cycles.

Position Error ($\Delta\Theta$): The normalized angular difference between the actual shaft position and the position indicated by the encoder cycle count.

Cycle Error (ΔC): An indication of cycle uniformity. The difference between an observed shaft angle which gives rise to one electrical cycle, and the nominal angular increment of 1/N of a revolution.

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error ($\Delta\phi$): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates in the direction of the arrow on top of the module, channel A will lead channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (R_{OP}): The distance from the codewheel's center of rotation to the optical center (O.C.) of the encoder module.

Index Pulse Width (P_O): The number of electrical degrees that an index is high during one full shaft rotation. This value is nominally 90°e or 1/4 cycle.

Absolute Maximum Ratings

Storage Temperature, T_S	-40°C to 100°C
Operating Temperature, T_A	-40°C to 100°C
Supply Voltage, V_{CC}	-0.5 V to 7 V
Output Voltage, V_O	-0.5 V to V_{CC}
Output Current per Channel, I_{OUT}	-1.0 mA to 5 mA
Shaft Axial Play	±0.25 mm (±0.010 in.)
Shaft Eccentricity Plus Radial Play	0.1 mm (0.004 in.) TIR
Velocity	30,000 RPM[1]
Acceleration	250,000 rad/sec²[1]

Note:
1. Absolute maximums for HEDS-5140/6140 codewheels only.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T_A	-40		100	°C	
Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts	Ripple < 100 mV_{P-P}
Load Capacitance	C_L			100	pF	2.7 kΩ pull-up
Count Frequency	f			100	kHz	Velocity (rpm) x N/60
Shaft Perpendicularity Plus Axial Play				±0.25 (±0.010)	mm (in.)	6.9 mm (0.27 in.) from mounting surface
Shaft Eccentricity Plus Radial Play				0.04 (0.0015)	mm (in.) TIR	6.9 mm (0.27 in.) from mounting surface

Note: The module performance is guaranteed to 100 kHz but can operate at higher frequencies.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances unless otherwise specified. Values are for the worst error over the full rotation of HEDS-5140 and HEDS-6140 codewheels.

Parameter		Symbol	Min.	Typ.*	Max.	Units
Cycle Error		ΔC		3	5.5	°e
Pulse Width Error		ΔP		7	30	°e
Logic State Width Error		ΔS		5	30	°e
Phase Error		Δϕ		2	15	°e
Position Error		ΔΘ		10	40	min. of arc
Index Pulse Width		P_O	60	90	120	°e
CH. I rise after CH. B or CH. A fall	-25°C to +100°C	t_1	10	100	250	ns
	-40°C to +100°C	t_1	-300	100	250	ns
CH. I fall after CH. A or CH. B rise	-25°C to +100°C	t_2	70	150	300	ns
	-40°C to +100°C	t_2	70	150	1000	ns

Note: Module mounted on tolerance circle of ±0.13 mm (±0.005 in.) radius referenced from module Side A aligning recess centers. 2.7 kΩ pull-up resistors used on all encoder module outputs.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Notes
Supply Current	I_{CC}	30	57	85	mA	
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -200 μA max.
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.86 mA
Rise Time	t_r		180		ns	C_L = 25 pF R_L = 2.7 kΩ pull-up
Fall Time	t_f		40		ns	

* Typical values specified at V_{cc} = 5.0 V and 25°C.

Mechanical Characteristics

Part No.	Parameter	Dimension	Tolerance	Units
HEDS-6140 23.36 mm optical radius codewheel	Codewheel Available to Fit These Standard Shaft Diameters	4 6 8	+0.000 -0.015	mm
		3/16 1/4 5/16 3/8 1/2 5/8	+0.000 -0.0007	in
	Moment of Inertia	7.7 (110 x 10^{-6})		g-cm^2 (oz-in-s^2)
HEDS-5140 11.00 mm optical radius codewheel	Codewheel Available to Fit These Standard Shaft Diameters	2 3 4 5 6 8	+0.000 -0.015	mm
		5/32 1/8 3/16 1/4	+0.000 -0.0007	in
	Moment of Inertia	0.6 (8.0 x 10^{-6})		g-cm^2 (oz-in-s^2)

Note: The tolerance requirements are on the mating shaft, not on the codewheel.

Electrical Interface

To insure reliable encoding performance, the HEDS-9040 and 9140 three channel encoder modules require 2.7 kΩ (±10%) pull-up resistors on output pins 2, 3, and 5 (Channels I, A and B) as shown in Figure 1. These pull-up resistors should be located as close to the encoder module as possible (within 4 feet). Each of the three encoder module outputs can drive a single TTL load in this configuration.

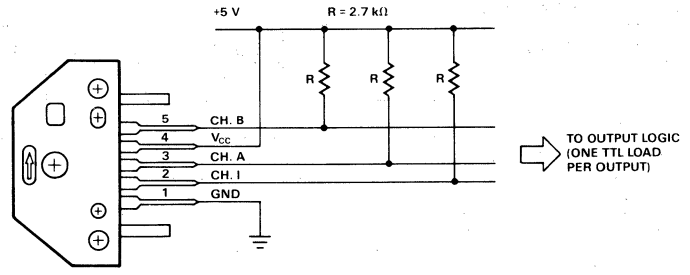


Figure 1. Pull-up Resistors on HEDS-9X40 Encoder Module Outputs.

Mounting Considerations

Figure 2 shows a mounting tolerance *requirement* for proper operation of the HEDS-9040 and HEDS-9140. The Aligning Recess Centers must be located within a tolerance circle of 0.005 in. radius from the nominal locations. This tolerance must be maintained whether the module is mounted with side A as the mounting plane using aligning pins (see Figure 5), or mounted with Side B as the mounting plane using an alignment tool (see Figures 3 and 4).

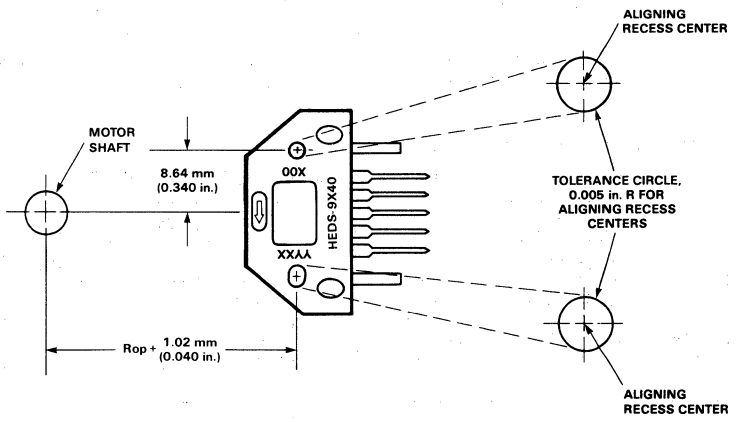


Figure 2. HEDS-9X40 Mounting Tolerance.

Mounting with an Alignment Tool

The HEDS-8905 and HEDS-8906 alignment tools are recommended for mounting the modules with Side B as the mounting plane. The HEDS-8905 is used to mount the HEDS-9140, and the HEDS-8906 is used to mount the HEDS-9040. These tools fix the module position using the codewheel hub as a reference. They will not work if Side A is used as the mounting plane.

The following assembly procedure uses the HEDS-8905/8906 alignment tool to mount a HEDS-9140/9040 module and a HEDS-5140/6140 codewheel:

Instructions:

1. Place codewheel on shaft.

2. Set codewheel height: (a) place alignment tool on motor base (pins facing up) flush up against the motor shaft as shown in Figure 3. (b) Push codewheel down against alignment tool. The codewheel is now at the proper height. (c) Tighten codewheel setscrew and remove alignment tool.

Some motors have a boss around the shaft that extends above the mounting plane. In this case, the alignment tool cannot be used as a gage block to set the codewheel height as described in 2(a), (b), and (c).
If boss is above mounting plane: Slide module onto motor base, adjusting height of codewheel so that it sits approximately in the middle of module slot. Lightly tighten setscrew. The codewheel height will be more precisely set in step 5.

3. Insert mounting screws through module and thread into the motor base. Do not tighten screws.

4. Slide alignment tool over codewheel hub and onto module as shown in Figure 4. The pins of the alignment tool should fit snugly inside the alignment recesses of the module.

If boss is above mounting plane: The pins of the tool may not mate properly because the codewheel is too high on the shaft. Loosen codewheel setscrew and lower codewheel slightly. Retighten setscrew lightly and attempt this step again.

5. While holding alignment tool in place, tighten screws down to secure module.

If boss is above mounting plane: Push codewheel up flush against alignment tool to set codewheel height. Tighten codewheel setscrew.

6. Remove alignment tool.

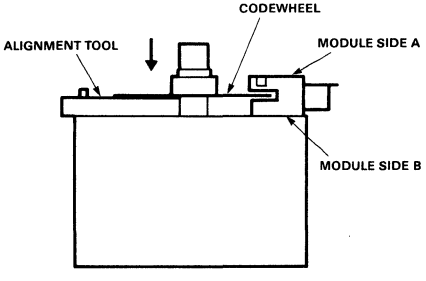


Figure 3. Alignment Tool is Used to Set Height of Codewheel.

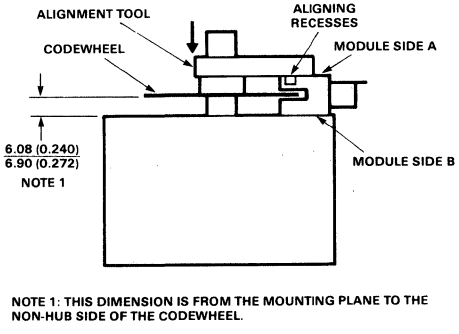


Figure 4. Alignment Tool is Placed over Shaft and onto Codewheel Hub. Alignment Tool Pins Mate with Aligning Recesses on Module.

Mounting with Aligning Pins

The HEDS-9040 and HEDS-9140 can also be mounted using aligning pins on the motor base. (Hewlett-Packard does not provide aligning pins.) For this configuration, Side A *must* be used as the mounting plane. The aligning recess centers must be located within the 0.005 in. Radius Tolerance Circle as explained in "Mounting Considerations." Figure 5 shows the necessary dimensions.

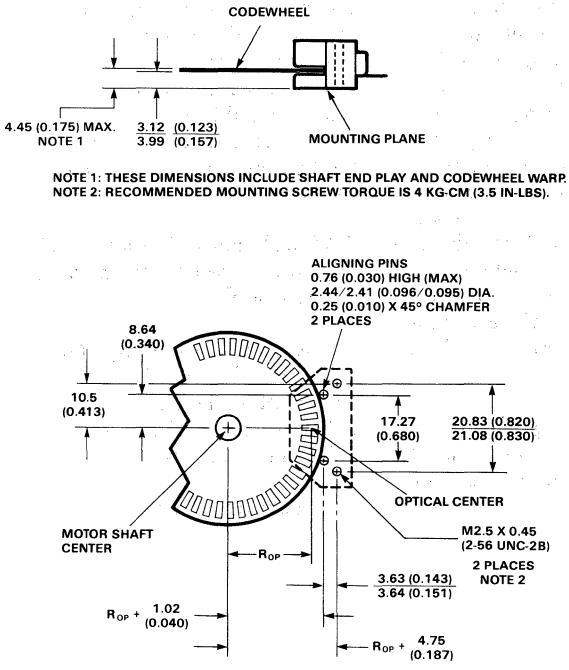


Figure 5. Mounting Plane Side A.

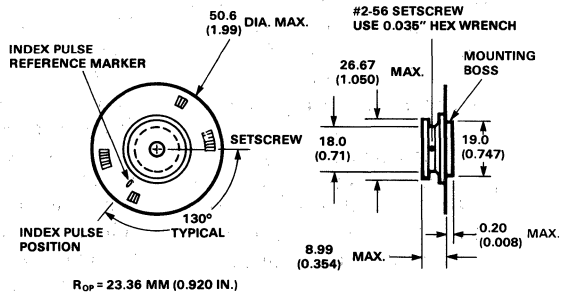


Figure 6. HEDS-6140 Codewheel Used with HEDS-9040.

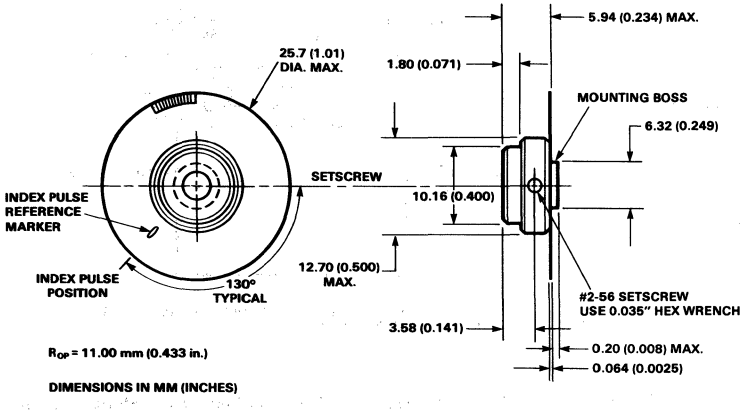
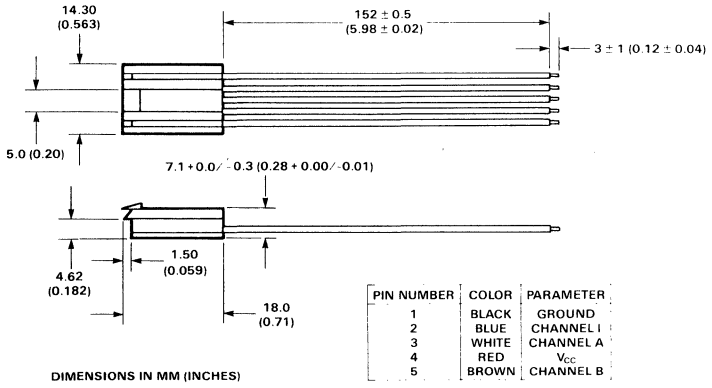


Figure 7. HEDS-5140 Codewheel Used with HEDS-9140.

Connectors

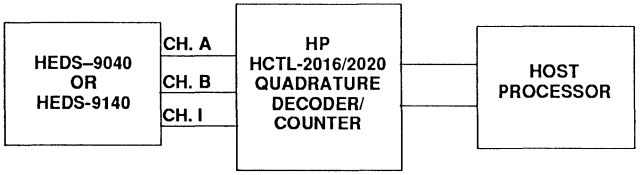
Manufacturer	Part Number	Mounting Surface
AMP	103686-4	Both
	640442-5	Side B
DuPont	65039-032 with 4825X-000 term.	Both
HP	HEDS-8903 with 5-wire leads	Side B (see Figure 8)
Molex	2695 series with 2759 series term.	Side B

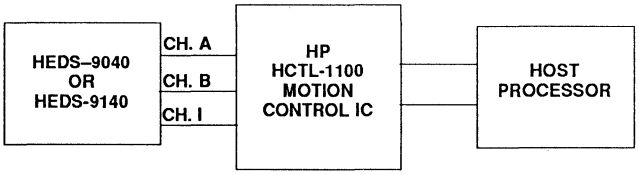


PIN NUMBER	COLOR	PARAMETER
1	BLACK	GROUND
2	BLUE	CHANNEL I
3	WHITE	CHANNEL A
4	RED	V_{CC}
5	BROWN	CHANNEL B

Figure 8. HEDS-8903 Connector.

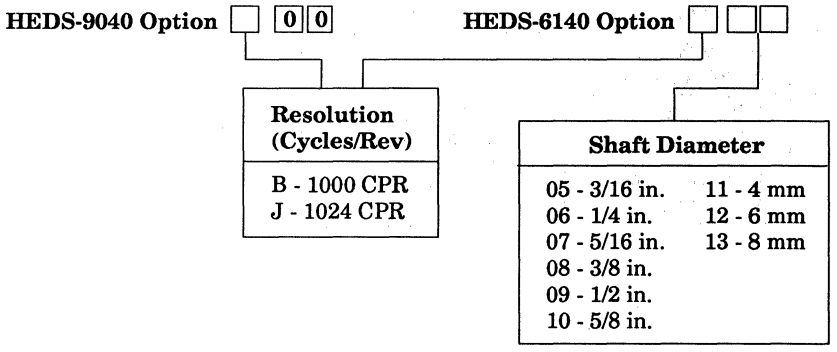
Typical Interfaces



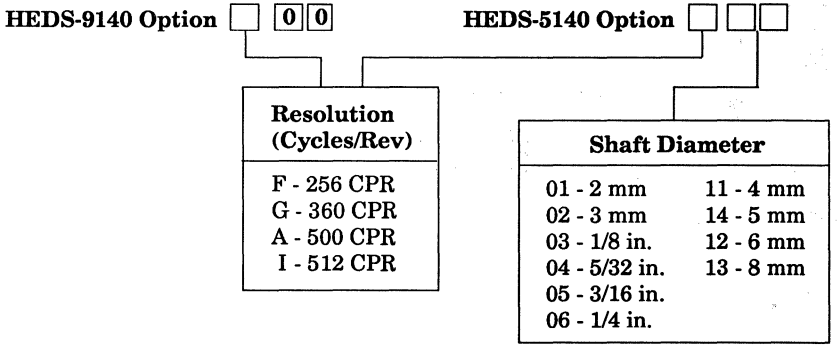


Ordering Information

Three Channel Encoder Modules and Codewheels, 23.36 mm Optical Radius



Three Channel Encoder Modules and Codewheels, 11.00 mm Optical Radius



Accessories

HEDS-8905
Alignment Tool for mounting the HEDS-9140.

HEDS-8906
Alignment Tool for Mounting the HEDS-9040.

HEWLETT PACKARD

Small Optical Encoder Module

Technical Data

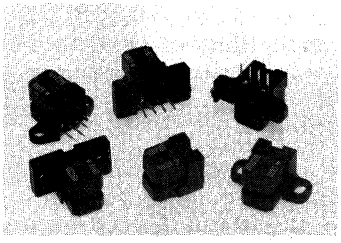
HEDS-9700 Series

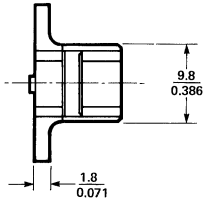
Features

- **Small Size**
- **Low Cost**
- **Multiple Mounting Options**
- **Wide Resolution Range**
- **Linear and Rotary Options Available**
- **No Signal Adjustment Required**
- **Insensitive to Radial and Axial Play**
- **-40°C to +85°C Operating Temperature**
- **Two Channel Quadrature Output**
- **TTL Compatible**
- **Single 5V Supply**
- **Wave Solderable**

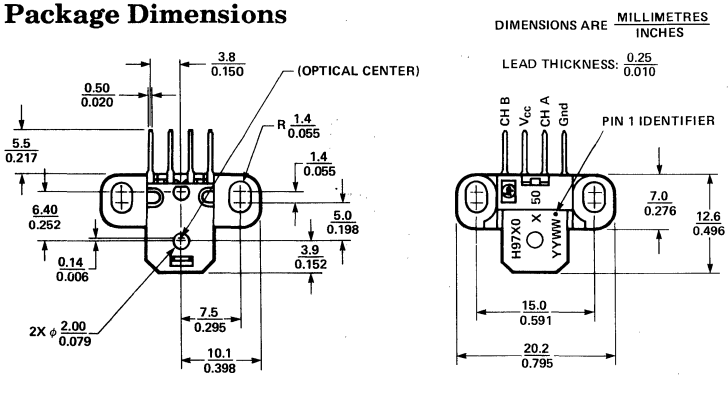
Description

The HEDS-9700 series is a high performance, low cost, optical incremental encoder module. When operated in conjunction with either a codewheel or codestrip, this module detects rotary or linear position. The





Package Dimensions



Mounting Option #50 - Standard

Contact Factory for Detailed Package Dimensions

ESD WARNING; NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

module consists of a lensed LED source and a detector IC enclosed in a small C-shaped plastic package. Due to a highly collimated light source and a unique photodetector array, the module is extremely tolerant to mounting misalignment.

The two channel digital outputs and 5V supply input are accessed through four solder-plated leads located on 2.54 mm (0.1 inch) centers.

The standard HEDS-9700 is designed for use with an 11 mm optical radius codewheel, or linear codestrip. Other options are available. Please contact factory for more information.

Applications

The HEDS-9700 provides sophisticated motion detection at a low cost, making closed-loop control very cost-competitive! Typical applications include printers, plotters, copiers, and office automation equipment.

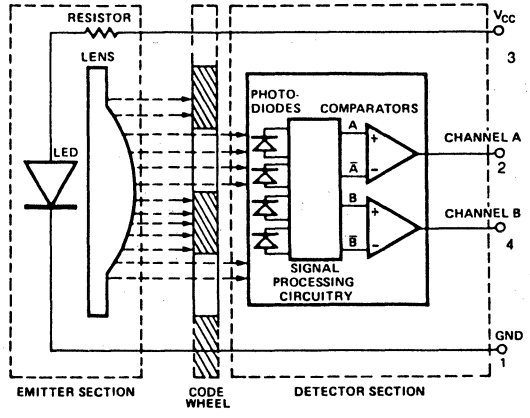
Theory of Operation

The HEDS-9700 is a C-shaped emitter/detector module. Coupled with a codewheel, it translates rotary motion into a two-channel digital output. Coupled with a codestrip, it translates linear motion into a digital output.

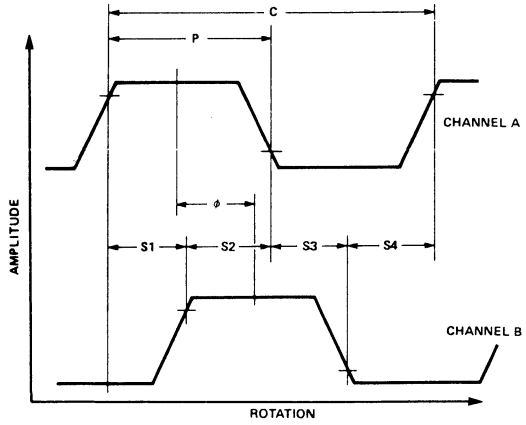
As seen in the block diagram, the module contains a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel/codestrip moves between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel/codestrip. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and count density of the codewheel/codestrip. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are fed through the signal processing circuitry. Two comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with channel B (90 degrees out of phase).

Block Diagram



Output Waveforms



Definitions

Count (N) = The number of bar and window pairs or counts per revolution (CPR) of the codewheel, or the number of lines per inch of the codestrip (LPI).

1 Shaft Rotation = 360 mechanical degrees
= N cycles

1 cycle (c) = 360 electrical degrees (°e)
= 1 bar and window pair

Pulse Width (P): The number of electrical degrees that an output is high during one cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error (Δϕ): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates counterclockwise, as viewed looking down on the module (so the marking is visible), channel A will lead channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (Rop): The distance from the codewheel's center of rotation to the optical center (O.C.) of the encoder module.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	85	°C	See Note
Operating Temperature	T_A	-40	85	°C	See Note
Supply Voltage	V_{CC}	-0.5	7	V	
Output Voltage	V_O	-0.5	V_{CC}	V	
Output Current per Channel	I_O	-1.0	5	mA	
Soldering Temperature			260	°C	t ≤ 5 sec.

Note: Higher operating ranges available, contact factory for more information.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	–40	85	°C	
Supply Voltage	V_{CC}	4.5	5.5	V	Ripple < 100 mV_{p-p}
Load Capacitance	C_L		100	pF	3.2 kΩ pull-up
Count Frequency			20	kHz	(Velocity (rpm) x N)/60

Note: The module performance is guaranteed to 20 kHz but can operate at higher frequencies. Contact factory for more information.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances. These characteristics do not include codewheel/codestrip contributions.

Parameter	Symbol	Typ.	Case 1 Max.	Case 2 Max.	Units	Notes
Pulse Width Error	ΔP	7	30	40	°e	
Logic State Width Error	ΔS	5	30	40	°e	
Phase Error	Δϕ	2	10	15	°e	

Case 1: Module mounted on tolerances of ±0.13 mm (0.005"). Case 2: Module mounted on tolerances of ±0.25 mm (0.010")

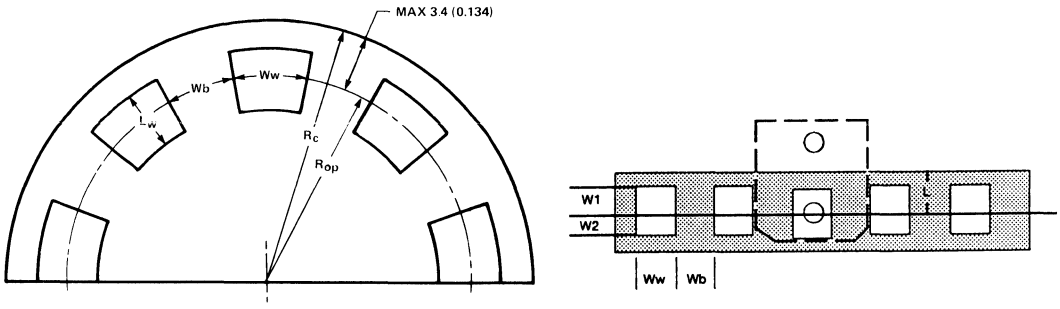
Note: See Figures in Mounting Considerations for details on Case 1 and Case 2 mounting tolerances.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, Typical at 25°C.

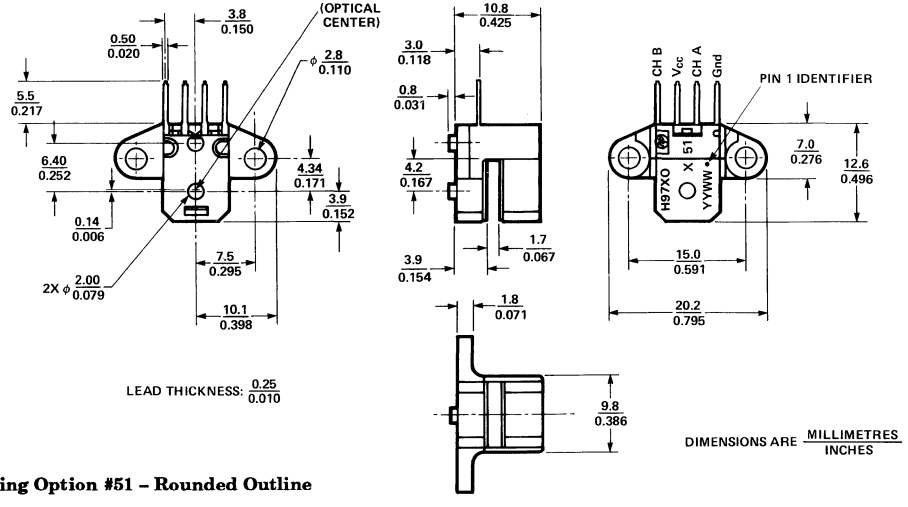
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		17	40	mA	
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40 μA
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA
Rise Time	t_r		200		ns	C_L = 25 pF, R_L = 11 kΩ
Fall Time	t_f		50		ns	C_L = 25 pF, R_L = 11 kΩ

Recommended Codewheel and Codestrip Characteristics



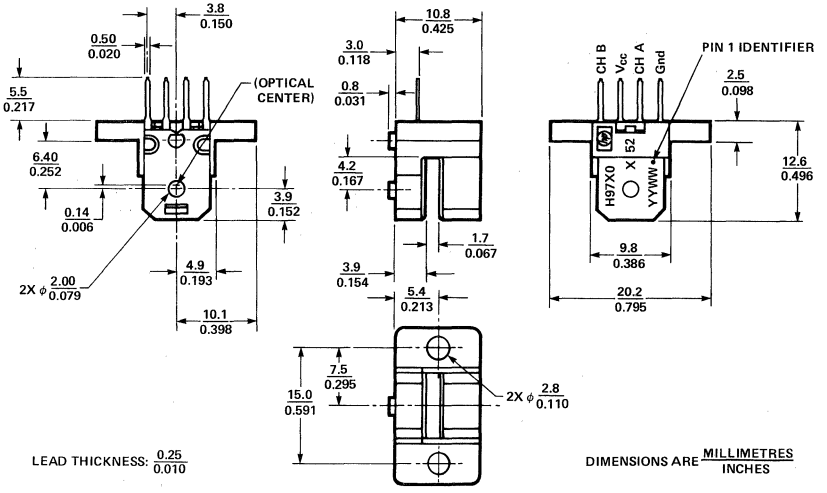
Parameter	Symbol	Min.	Max.	Units	Notes
Window/Bar Ratio	Ww/Wb	0.7	1.4		
Window Length (Rotary)	Lw	1.80 (0.071)	2.30 (0.091)	mm (inch)	
Absolute Maximum Codewheel Radius (Rotary)	Rc		Rop + 3.40 (Rop + 0.134)	mm (inch)	Includes eccentricity errors
Center of Post to Inside Edge of Window	W1	1.04 (0.041)		mm (inch)	
Center of Post to Outside Edge of Window	W2	0.76 (0.030)		mm (inch)	
Center of Post to Inside Edge of Codestrip	L		3.60 (0.142)	mm (inch)	

Optional Packages Available

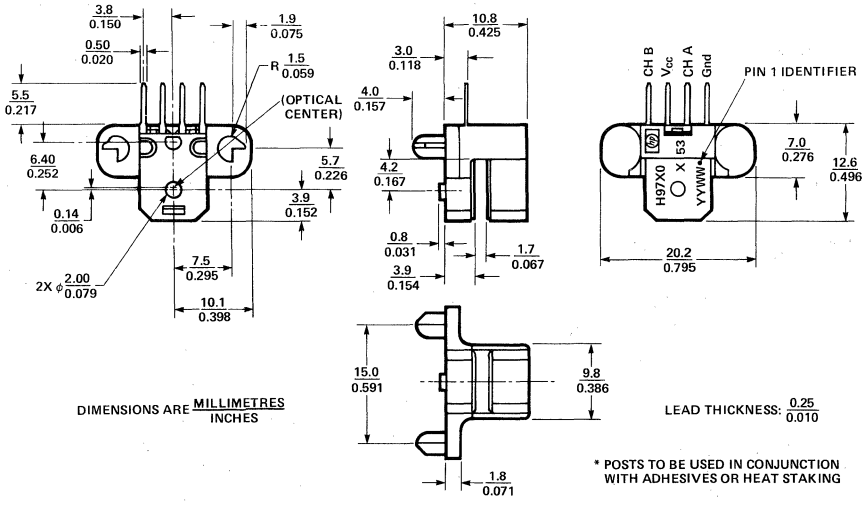


Mounting Option #51 – Rounded Outline

Optional Packages Available (cont'd.)

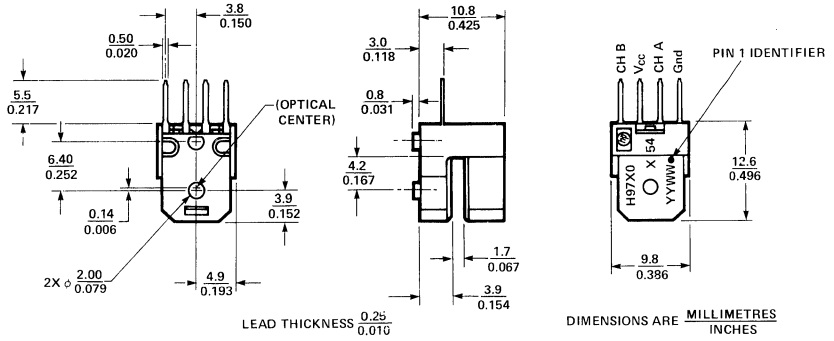


Mounting Option #52 - Backplane

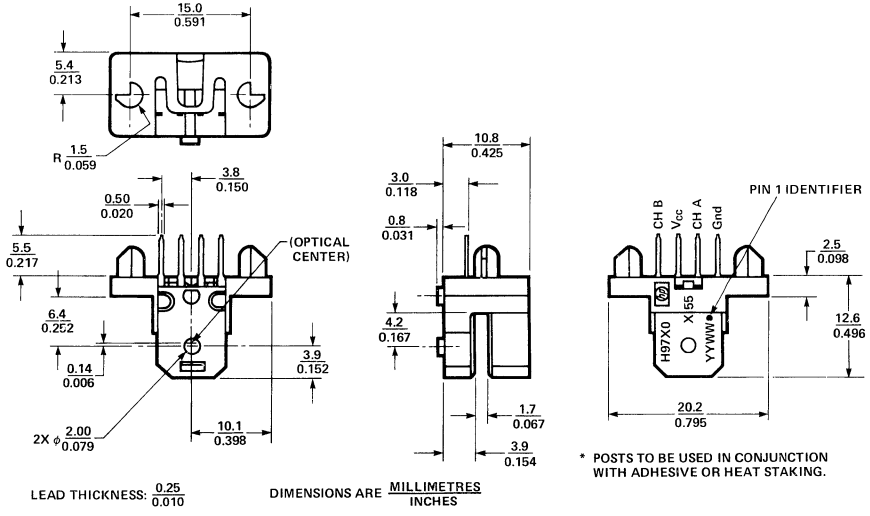


Mounting Option #53 - Standard with Posts

Optional Packages Available (cont'd.)

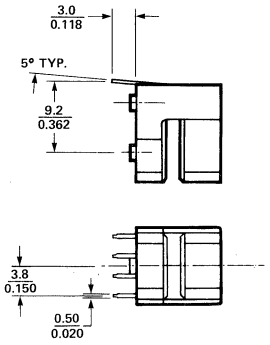


Mounting Option #54 – Tabless

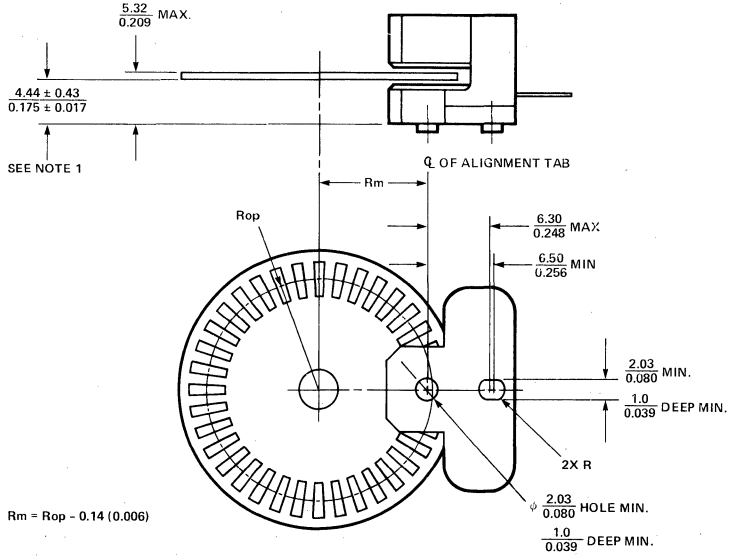


Mounting Option #55 – Backplane with Posts

Bent Lead Option



Mounting Considerations



Note: These dimensions include shaft end play and codewheel warp.

All dimensions for mounting the module and codewheel/codestrip should be measured with respect to the two mounting posts, shown above.

Mounting Tolerances

Case 1 and Case 2 specify the mounting tolerances required on Rm in order to achieve the respective encoding characteristics shown on page 4. The mounting tolerances are as follows:

Case 1: Rm ± 0.13 mm (.005 inches)
Case 2: Rm ± 0.25 mm (.010 inches)

Recommended Screw Size: M2.5 x 0.45 or 2-56

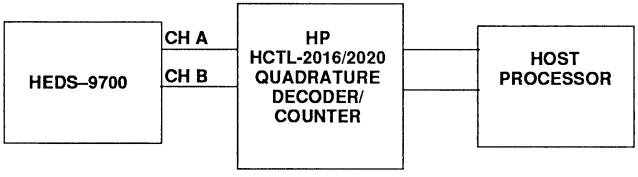
Wave Solder Conditions

Flux – RMA Water Soluble (per MIL-F-14256D)

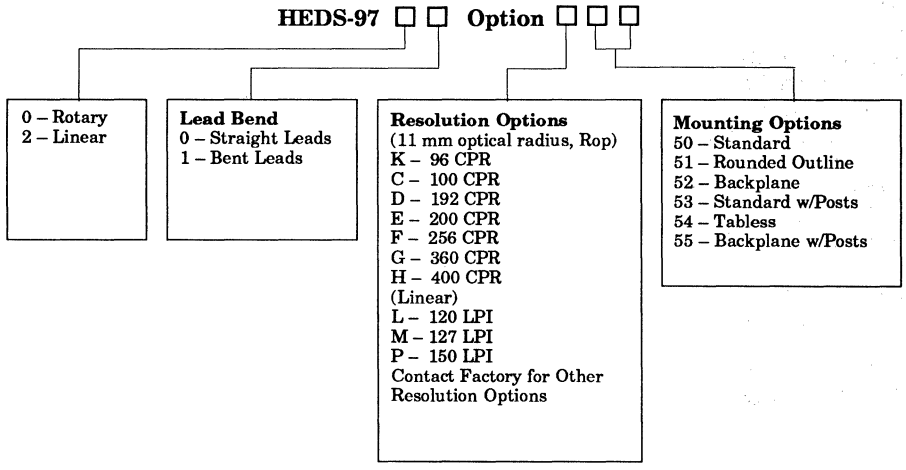
Process Parameters

1. Flux
2. Pre-heat 60 seconds total
   PCB top side @ 230°C
   PCB bottom side @ 260°C
3. Wave solder 255°C, 1.2 meters/min line speed
4. Hot Water Wash
   1st: 30°C 45 seconds
   2nd: 70°C 90 seconds
5. Rinse
   1st: 23°C 45 seconds
   2nd: 23°C 45 seconds
6. Dry
   1st: 80°C 105 seconds
   2nd: 95°C 105 seconds

Typical Interface



Ordering Information



Note: Please contact factory for codewheel and codestrip information.

Quick Assembly Two and Three Channel Optical Encoders

Technical Data

HEDS-5500/5540
HEDS-5600/5640

Features

- **Two Channel Quadrature Output with Optional Index Pulse**
- **Quick and Easy Assembly**
- **No Signal Adjustment Required**
- **External Mounting Ears Available**
- **Low Cost**
- **Resolutions Up to 512 Counts Per Revolution**
- **Small Size**
- **-40°C to 100°C Operating Temperature**
- **TTL Compatible**
- **Single 5 V Supply**

Description

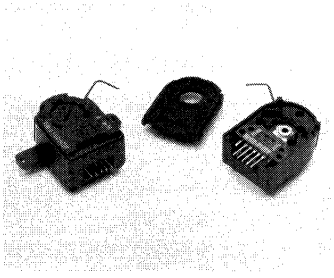
The HEDS-5500/5540 and 5600/5640 are high performance, low cost, two and three channel optical incremental encoders. These encoders emphasize high reliability, high resolution, and easy assembly.

Each encoder contains a lensed LED source, an integrated circuit with detectors and output circuitry, and a codewheel which rotates between the emitter and detector IC. The outputs of the HEDS-5500 and 5600 are two square waves in quadrature. The HEDS-5540 and 5640 also have a third channel index output in addition to the two channel quadrature. This index output is a 90 electrical degree, high true index pulse which is generated once for each full rotation of the codewheel.

These encoders may be quickly and easily mounted to a motor. For larger diameter motors, the HEDS-5600/5640 feature external mounting ears.

The quadrature signals and the index pulse are accessed through five 0.025 inch square pins located on 0.1 inch centers.

Standard resolutions between 96 and 512 counts per revolution are presently available. Consult local Hewlett-Packard sales representatives for other resolutions.



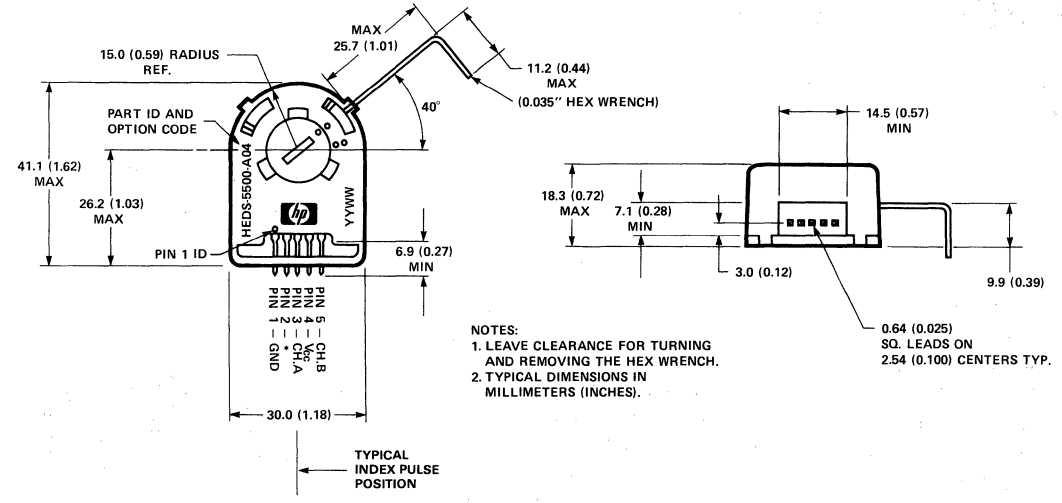
Applications

The HEDS-5500, 5540, 5600, and 5640 provide motion detection at a low cost, making them ideal for high volume applications. Typical applications include printers, plotters, tape drives, positioning tables, and automatic handlers.

ESD WARNING; NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

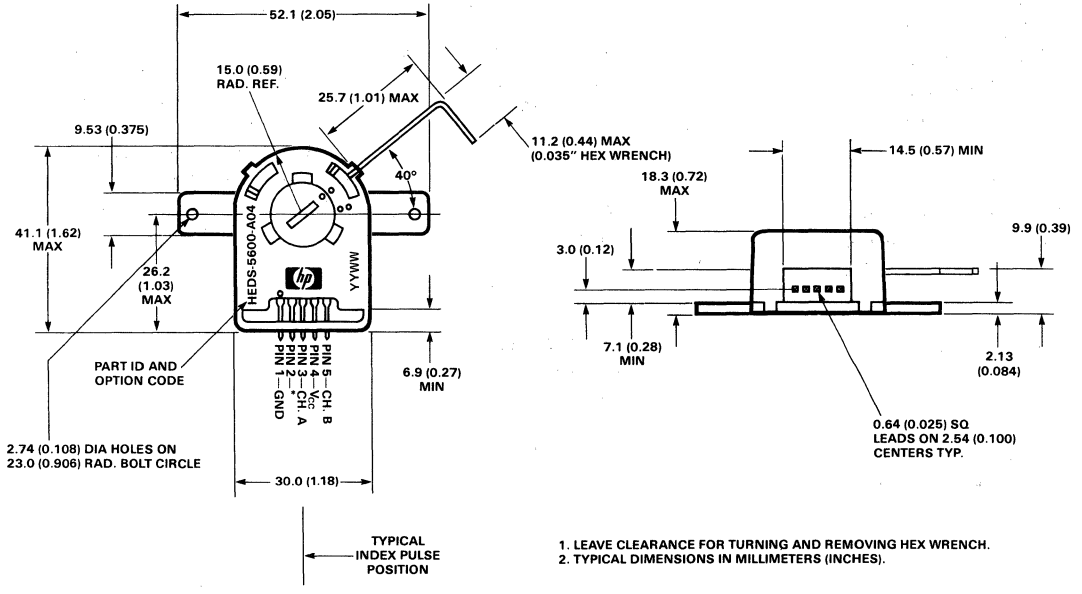
Package Dimensions

HEDS-5500/5540



***Note:** For the HEDS-5500, Pin #2 is a No Connect. For the HEDS-5540, Pin #2 is CH. I, the index output.*

HEDS-5600/5640



***Note:** For the HEDS-5600, Pin #2 is a No Connect. For the HEDS-5640, Pin #2 is CH. I, the index output.*

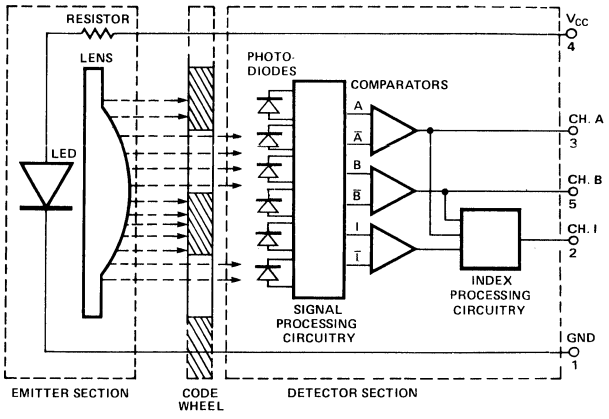
Theory of Operation

The HEDS-5500, 5540, 5600, and 5640 translate the rotary motion of a shaft into either a two- or a three-channel digital output.

As seen in the block diagram, these encoders contain a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single polycarbonate lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel rotates between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and design of the codewheel. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\overline{A}$, B and $\overline{B}$ (also I and $\overline{I}$ in the HEDS-5540 and 5640). Comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

Block Diagram



NOTE: CIRCUITRY FOR CH. I IS ONLY IN HEDS-5540 AND 5640 THREE CHANNEL ENCODERS.

In the HEDS-5540 and 5640, the output of the comparator for I and $\overline{I}$ is sent to the index processing circuitry along with the outputs of channels A and B. The final output of channel I is an index pulse P_0 which is generated once for each full rotation of the codewheel. This output P_0 is a one state width (nominally 90 electrical degrees), high true index pulse which is coincident with the low states of channels A and B.

Definitions

Count (N): The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

One Cycle (C): 360 electrical degrees (°e), 1 bar and window pair.

One Shaft Rotation: 360 mechanical degrees, N cycles.

Position Error ($\Delta\Theta$): The normalized angular difference between the actual shaft position and the position indicated by the encoder cycle count.

Cycle Error (ΔC): An indication of cycle uniformity. The difference between an observed shaft angle which gives rise to one electrical cycle, and the nominal angular increment of 1/N of a revolution.

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error ($\Delta\phi$): The deviation of the phase from its ideal value of 90°e.

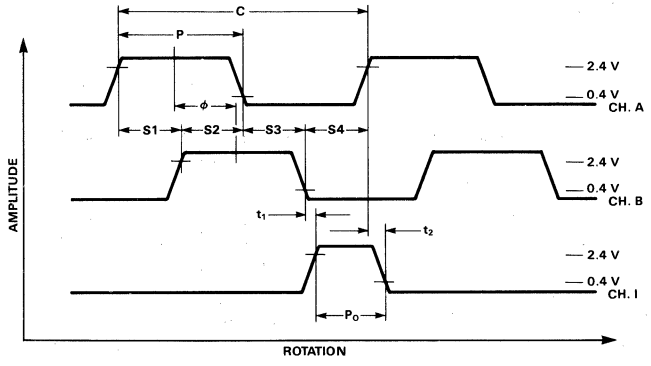
Direction of Rotation: When the codewheel rotates in the counterclockwise direction (as viewed from the encoder end of the motor), channel A will lead channel B. If the codewheel rotates in the clockwise direction, channel B will lead channel A.

Index Pulse Width (P_O): The number of electrical degrees that an index output is high during one full shaft rotation. This value is nominally 90°e or 1/4 cycle.

Absolute Maximum Ratings

Storage Temperature, T_S	-40°C to 100°C
Operating Temperature, T_A	-40°C to 100°C
Supply Voltage, V_{CC}	-0.5 V to 7 V
Output Voltage, V_O	-0.5 V to V_{CC}
Output Current per Channel, I_{OUT}	-1.0 mA to 5 mA
Vibration	20 g, 5 to 1000 Hz
Shaft Axial Play	±0.25 mm (±0.010 in.)
Shaft Eccentricity Plus Radial Play	0.1 mm (0.004 in.) TIR
Velocity	30,000 RPM
Acceleration	250,000 rad/sec^2

Output Waveforms



Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T_A	-40		100	°C	
Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts	Ripple < 100 mV_{p-p}
Load Capacitance	C_L			100	pF	2.7 kΩ pull-up
Count Frequency	f			100	kHz	Velocity (rpm) x N/60
Shaft Perpendicularity Plus Axial Play				±0.25 (±0.010)	mm (in.)	6.9 mm (0.27 in.) from mounting surface
Shaft Eccentricity Plus Radial Play				0.04 (0.0015)	mm (in.) TIR	6.9 mm (0.27 in.) from mounting surface

Note: The module performance is guaranteed to 100 kHz but can operate at higher frequencies. 2.7 kΩ pull-up resistors required for HEDS-5540 and 5640.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances unless otherwise specified. Values are for the worst error over the full rotation.

Part No.	Description		Sym.	Min.	Typ.*	Max.	Units
HEDS-5500 HEDS-5600 (Two Channel)	Pulse Width Error		ΔP		7	45	°e
	Logic State Width Error		ΔS		5	45	°e
	Phase Error		$\Delta\phi$		2	20	°e
	Position Error		$\Delta\Theta$		10	40	min. of arc
	Cycle Error		ΔC		3	5.5	°e
HEDS-5540 HEDS-5640 (Three Channel)	Pulse Width Error		ΔP		5	35	°e
	Logic State Width Error		ΔS		5	35	°e
	Phase Error		$\Delta\phi$		2	15	°e
	Position Error		$\Delta\Theta$		10	40	min. of arc
	Cycle Error		ΔC		3	5.5	°e
	Index Pulse Width		P_O	55	90	125	°e
	CH. I rise after	-25°C to +100°C	t_1	10	100	250	ns
	CH. A or CH. B fall	-40°C to +100°C	t_1	-300	100	250	ns
	CH. I fall after	-25°C to +100°C	t_2	70	150	300	ns
	CH. B or CH. A rise	-40°C to +100°C	t_2	70	150	1000	ns

Note: See Mechanical Characteristics for mounting tolerances.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range.

Part No.	Parameter	Sym.	Min.	Typ.*	Max.	Units	Notes
HEDS-5500 HEDS-5600	Supply Current	I_{CC}		17	40	mA	
	High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40 µA max.
	Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA
	Rise Time	t_r		200		ns	C_L = 25 pF
	Fall Time	t_f		50		ns	R_L = 11 kΩ pull-up
HEDS-5540 HEDS-5640	Supply Current	I_{CC}	30	57	85	mA	
	High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -200 µA max.
	Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.86 mA
	Rise Time	t_r		180		ns	C_L = 25 pF
	Fall Time	t_f		40		ns	R_L = 2.7 kΩ pull-up

*Typical values specified at V_{cc} = 5.0 V and 25°C.

Mechanical Characteristics

Parameter	Symbol	Dimension	Tolerance[1] HEDS-5X00	Tolerance[1] HEDS-5X40	Units
Codewheel Fits These Standard Shaft Diameters		2 3 4 5 6 8	+0.000 -0.015	+0.000 -0.015	mm
		5/32 1/8 3/16 1/4	+0.0000 -0.0007	+0.0000 -0.0007	in
Moment of Inertia	J	0.6 (8.0 x 10^{-6})			g-cm^2 (oz-in-s^2)
Required Shaft Length[2]		14.0 (0.55)	±0.5 (±0.02)	±0.5 (±0.02)	mm (in.)
Bolt Circle[3]	2 screw mounting	19.05 (0.750)	±0.13 (±0.005)	±0.13 (±0.005)	mm (in.)
	3 screw mounting	20.90 (0.823)	±0.13 (±0.005)	±0.13 (±0.005)	mm (in.)
	ext. mtg. ears	46.0 (1.811)	±0.13 (±0.005)	±0.13 (±0.005)	mm (in.)
Mounting Screw Size[4]	2 screw mounting	M 2.5 or (2-56)			mm (in.)
	3 screw mounting	M 1.6 or (0-80)			mm (in.)
	ext. mtg. ears	M 2.5 or (2-56)			mm (in.)
Encoder Base Plate Thickness		0.33 (0.130)			mm (in.)
Hub Set Screw		(2-56)			(in.)

Notes:
1. These are tolerances required of the user.
2. The HEDS-55X5 and 56X5 provide an 8.9 mm (0.35 inch) diameter hole through the housing for longer motor shafts. See Ordering Information.
3. The HEDS-5540 and 5640 must be aligned using the aligning pins as specified in Figure 3, or using the alignment tool as shown in "Encoder Mounting and Assembly". See also "Mounting Considerations."
4. The recommended mounting screw torque for 2 screw and external ear mounting is 1.0 kg-cm (0.88 in-lbs). The recommended mounting screw torque for 3 screw mounting is 0.50 kg-cm (0.43 in-lbs).

Electrical Interface

To insure reliable encoding performance, the HEDS-5540 and 5640 three channel encoders require 2.7 kΩ (±10%) pull-up resistors on output pins 2, 3, and 5 (Channels I, A, and B) as shown in Figure 1. These pull-up resistors should be located as close to the encoder as possible (within 4 feet). Each of the three encoder outputs can drive a single TTL load in this configuration.

The HEDS-5500 and 5600 two channel encoders do not normally require pull-up resistors. However, pull-up resistors on output pins 3 and 5 (Channels A and B) are recommended to improve rise times.

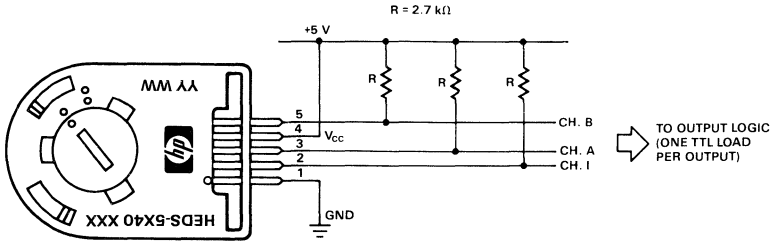


Figure 1. Pull-up Resistors on HEDS-5X40 Encoder Outputs.

Mounting Considerations

The HEDS-5540 and 5640 three channel encoders must be aligned using the aligning pins as specified in Figure 3, or using the HEDS-8910 Alignment Tool as shown in Encoder Mounting and Assembly.

The use of aligning pins or alignment tool is recommended but not required to mount the HEDS-5500 and 5600. If these two channel encoders are attached to a motor with the screw sizes and mounting tolerances specified in the mechanical characteristics section without any additional mounting bosses, the encoder output errors will be within the maximums specified in the encoding characteristics section.

The HEDS-5500 and 5540 can be mounted to a motor using either the two screw or three screw mounting option as shown in Figure 2. The optional aligning pins shown in Figure 3 can be used with either mounting option.

The HEDS-5600 and 5640 have external mounting ears which may be used for mounting to larger motor base plates. Figure 4 shows the necessary mounting holes with optional aligning pins and motor boss.

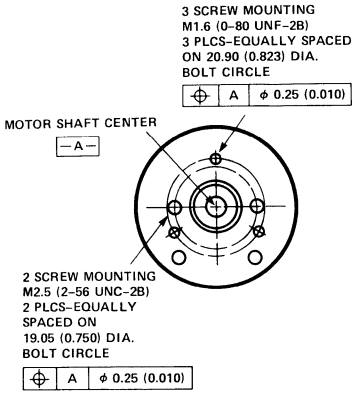


Figure 2. Mounting Holes.

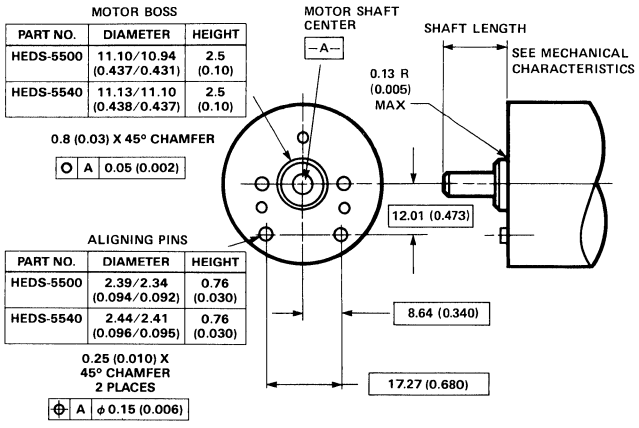


Figure 3. Optional Mounting Aids.

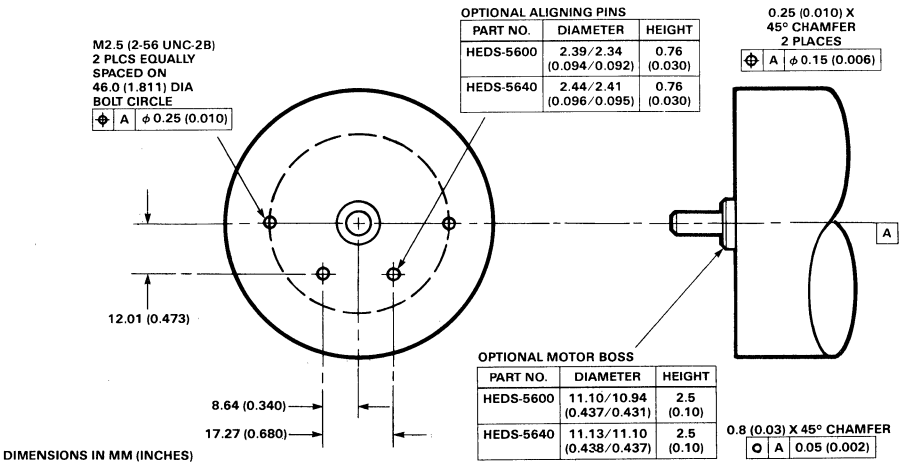
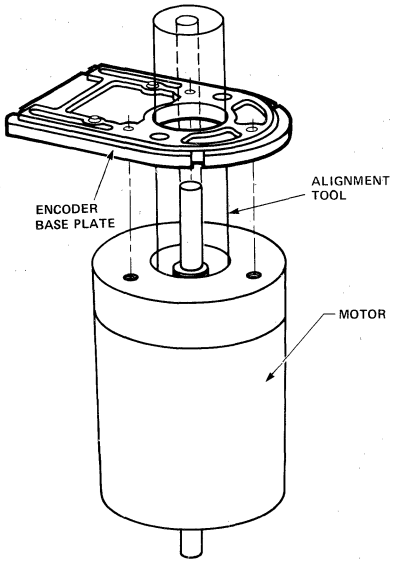


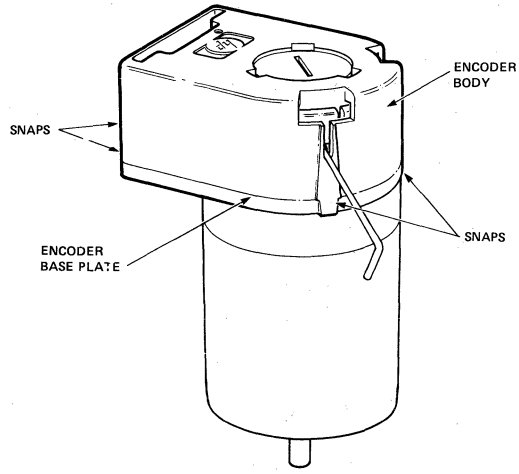
Figure 4. Mounting with External Ears.

Encoder Mounting and Assembly

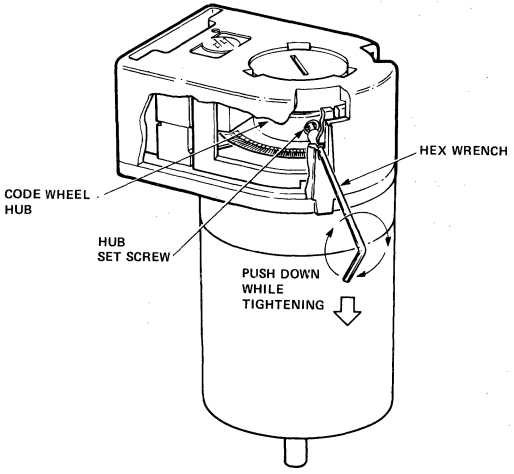


1. For HEDS-5500 and 5600: Mount encoder base plate onto motor. Tighten screws. Go on to step 2.

1a. For HEDS-5540 and 5640: Slip alignment tool onto motor shaft. With alignment tool in place, mount encoder baseplate onto motor as shown above. Tighten screws. Remove alignment tool.



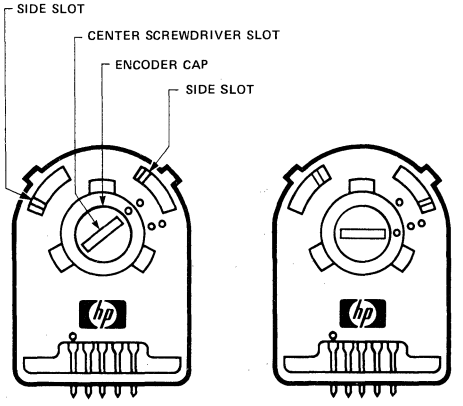
2. Snap encoder body onto base plate locking all 4 snaps.



3a. Push the hex wrench into the body of the encoder to ensure that it is properly seated into the code wheel hub set screws. Then apply a downward force on the end of the hex wrench. This sets the code wheel gap by levering the code wheel hub to its upper position.

3b. While continuing to apply a downward force, rotate the hex wrench in the clockwise direction until the hub set screw is tight against the motor shaft. The hub set screw attaches the code wheel to the motor's shaft.

3c. Remove the hex wrench by pulling it straight out of the encoder body.

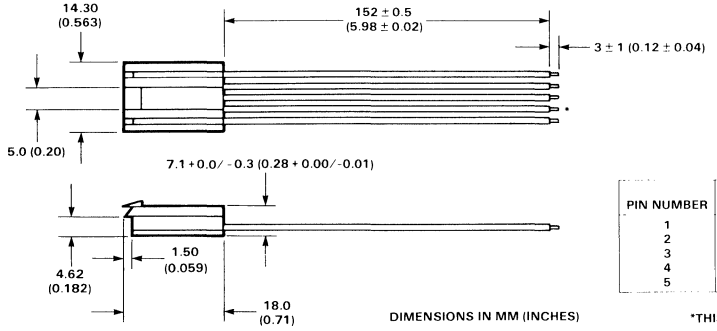


4. Use the center screwdriver slot, or either of the two side slots, to rotate the encoder cap dot clockwise from the one dot position to the two dot position. Do not rotate the encoder cap counterclockwise beyond the one dot position.

The encoder is ready for use!

Connectors

Manufacturer	Part Number
AMP	103686-4 640442-5
Berg	65039-032 with 4825X-000 term.
HP	HEDS-8902 (2 ch.) with 4-wire leads
	HEDS-8903 (3 ch.) with 5-wire leads
Molex	2695 series with 2759 series term.

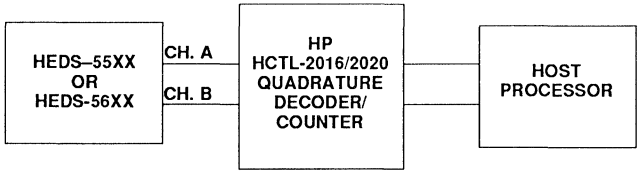


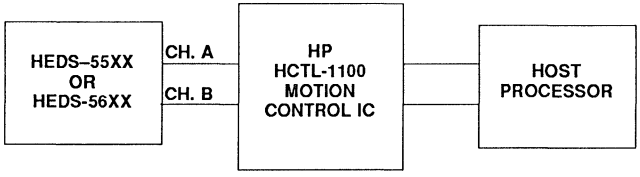
PIN NUMBER	PARAMETER	HEDS-8902 COLORS	HEDS-8903 COLORS
1	GROUND	BLACK	BLACK
2	CH. I	N/A*	BLUE
3	CH. A	WHITE	WHITE
4	V_{CC}	RED	RED
5	CH. B	BROWN	BROWN

*THIS WIRE IS NOT ON HEDS-8902.

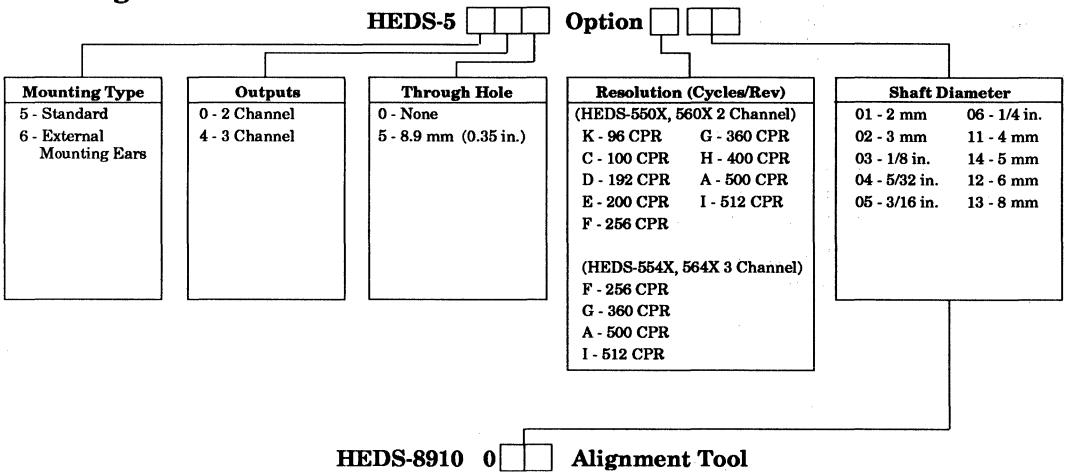
Figure 5. HEDS-8902 and 8903 Connectors.

Typical Interfaces





Ordering Information



(Included with each order of HEDS-554X/564X three channel encoders)

Miniature Panel Mount Optical Encoder

Technical Data

HRPG Series

Features

- **Miniature Size**
- **Smooth Turning and Detented Options**
- **Multiple Mounting Bracket Options**
- **Uses Optical Reflective Technology**
- **Quadrature Digital Output**
- **Small Footprint for Versatile Mounting**
- **TTL Compatible**

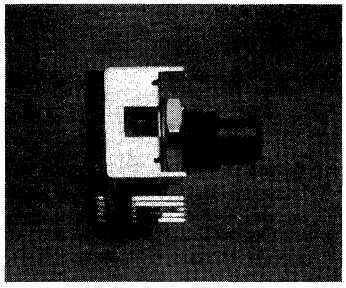
Description

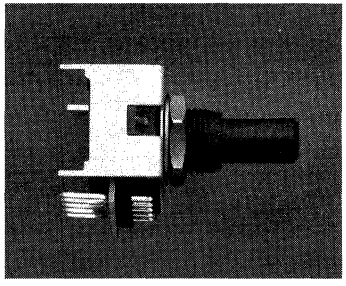
The HRPG series is a family of miniature panel mount optical encoders, also known as Rotary Pulse Generators (RPG) and digital potentiometers. The HRPG is designed to be mounted on a front panel and used as a rotary, data-entry device. The HRPG is very flexible for numerous applications due to the many configuration options available. These options include detents or smooth, multiple terminations, versatile mounting capabilities, and different shaft configurations.

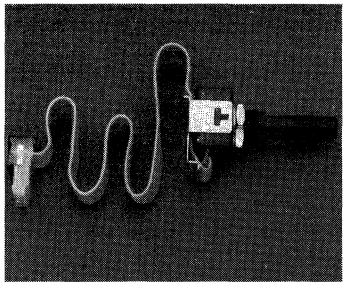
The HRPG uses optical reflective technology providing accuracy and reliability to the encoder. An LED emits a beam of light onto the specular codewheel surface. When the light strikes the surface, it projects the image of the codewheel back on the photo-detector, causing the output to change. The entire detector circuit is on one IC, thus the part is less sensitive to temperature and other environmental variations.

Applications

Typical applications for the Rotary Pulse Generator include front panel instruments, audio/visual boards, and other devices requiring digital output from a turning knob.







Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	+85	°C	
Operating Temperature	T_A	0	+70	°C	
Vibration			20	g	20 Hz to 2 kHz
Supply Voltage	V_{CC}	-0.5	7	V	
Output Voltage	V_O	-0.5	V_{CC}	V	
Output Current Per Channel	I_O	-1	5	mA	
Shaft Load – Axial			4.0	N	10^6 Revolutions
Shaft Load – Radial			0.1	Nm	10^6 Revolutions
Revolution Life		10^6		Rev	At Maximum Loads

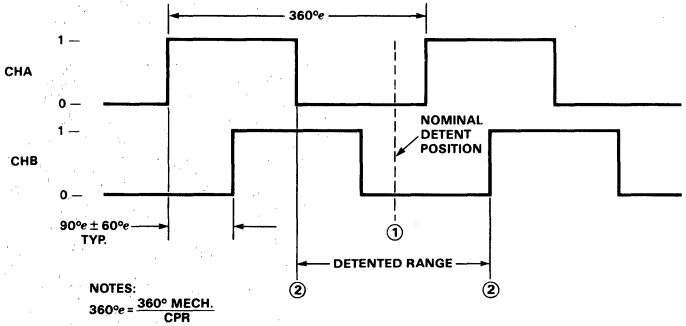
Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	0	+70	°C	Non Condensing Atmosphere
Supply Voltage	V_{CC}	4.5	5.5	V	Ripple < 100 mV_{P-P}
Rotation Speed – Detented			200	RPM	
– Smooth			300	RPM	

Electrical Characteristics
Over Recommended Operating Range

Parameter	Symbol	Min.	Max.	Units	Notes
Supply Current	I_{CC}		40	mA	
High Level Output Voltage	V_{OH}	2.4		V	I_{OH} = - 40 µA Max.
Low Level Output Voltage	V_{OL}		0.4	V	I_{OL} = 3.2 mA

Output Waveforms



NOTES:

$360°e = \frac{360° \text{ MECH.}}{CPR}$

CHANNEL A LEADS CHANNEL B FOR CLOCKWISE ROTATION
CHANNEL B LEADS CHANNEL A FOR COUNTERCLOCKWISE ROTATION

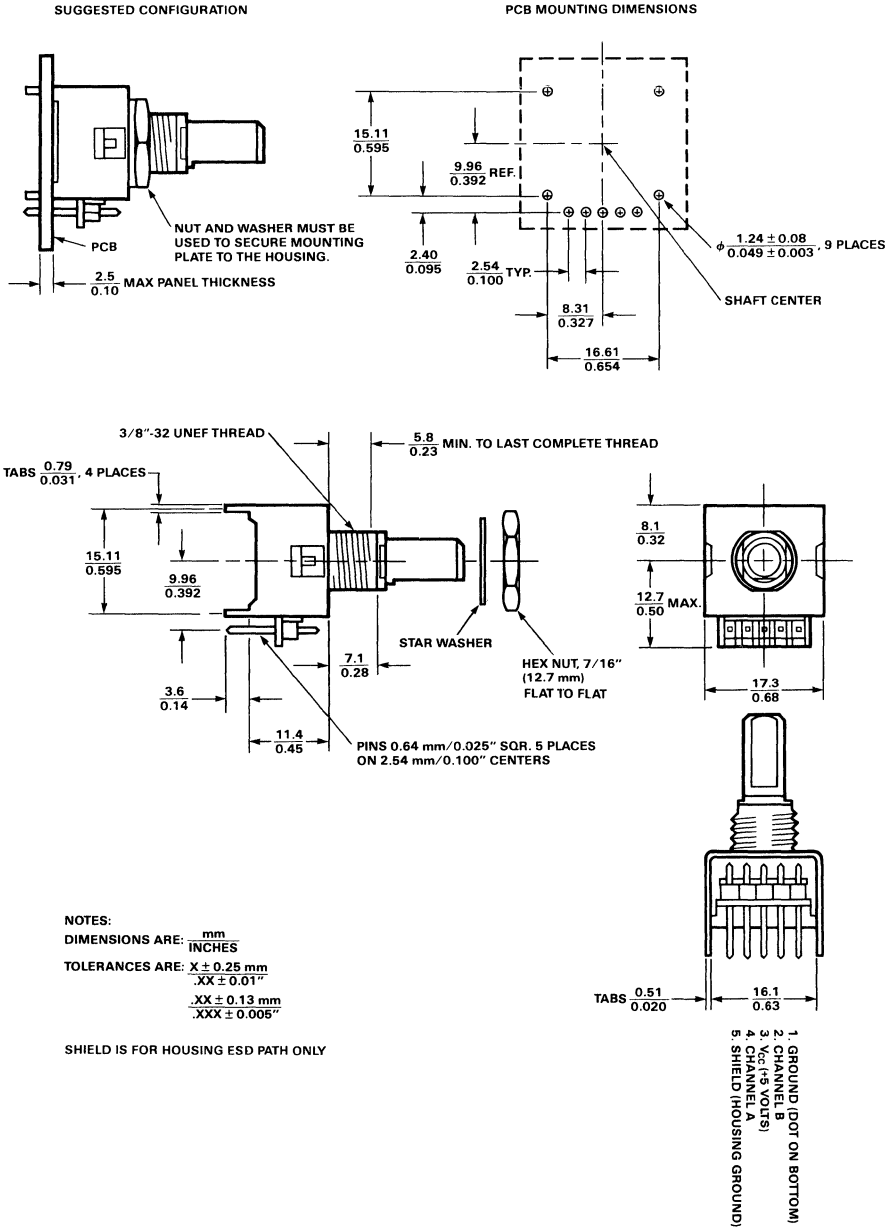
1. FOR HRPG-ADXX #XXX THE NOMINAL DETENT POSITION IS CENTERED AROUND LOW-LOW STATE (CHA = 0, CHB = 0).
2. DETENT POSITION WILL LIE WITHIN THESE BOUNDARIES, NEVER IN HIGH-HIGH STATE (CHA = 1, CHB = 1).

Mechanical Configurations

Termination Options

Option R – Pins Rear with Bracket

HRPG-AXXX#XXR



NOTES:

DIMENSIONS ARE: mm / INCHES

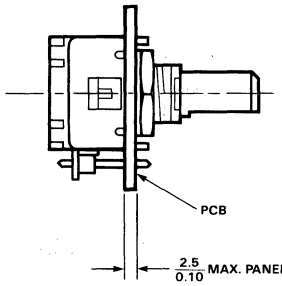
TOLERANCES ARE: X ± 0.25 mm / .XX ± 0.01"

.XX ± 0.13 mm / .XXX ± 0.005"

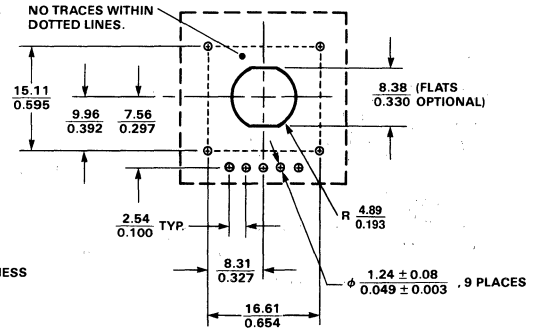
SHIELD IS FOR HOUSING ESD PATH ONLY

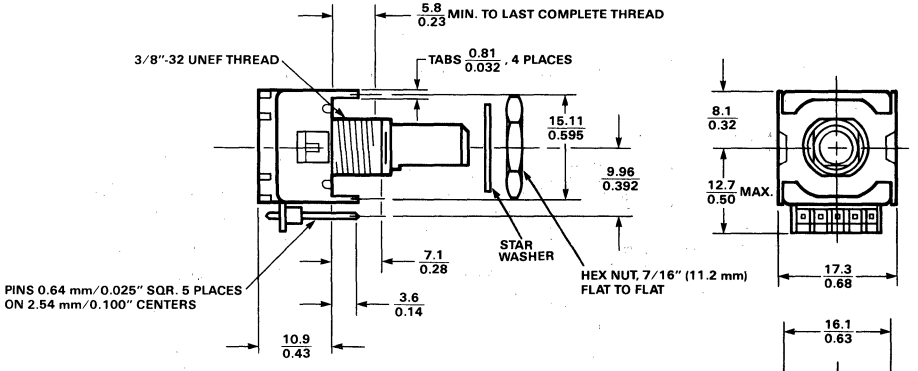
Option F – Pins Front with Bracket
HRPG-AXXX#XXF

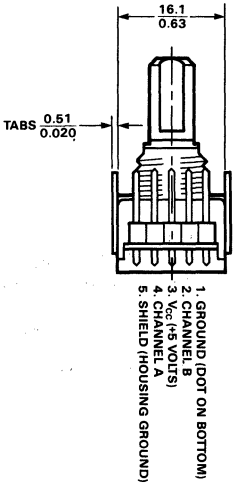
SUGGESTED CONFIGURATION



PCB MOUNTING DIMENSIONS



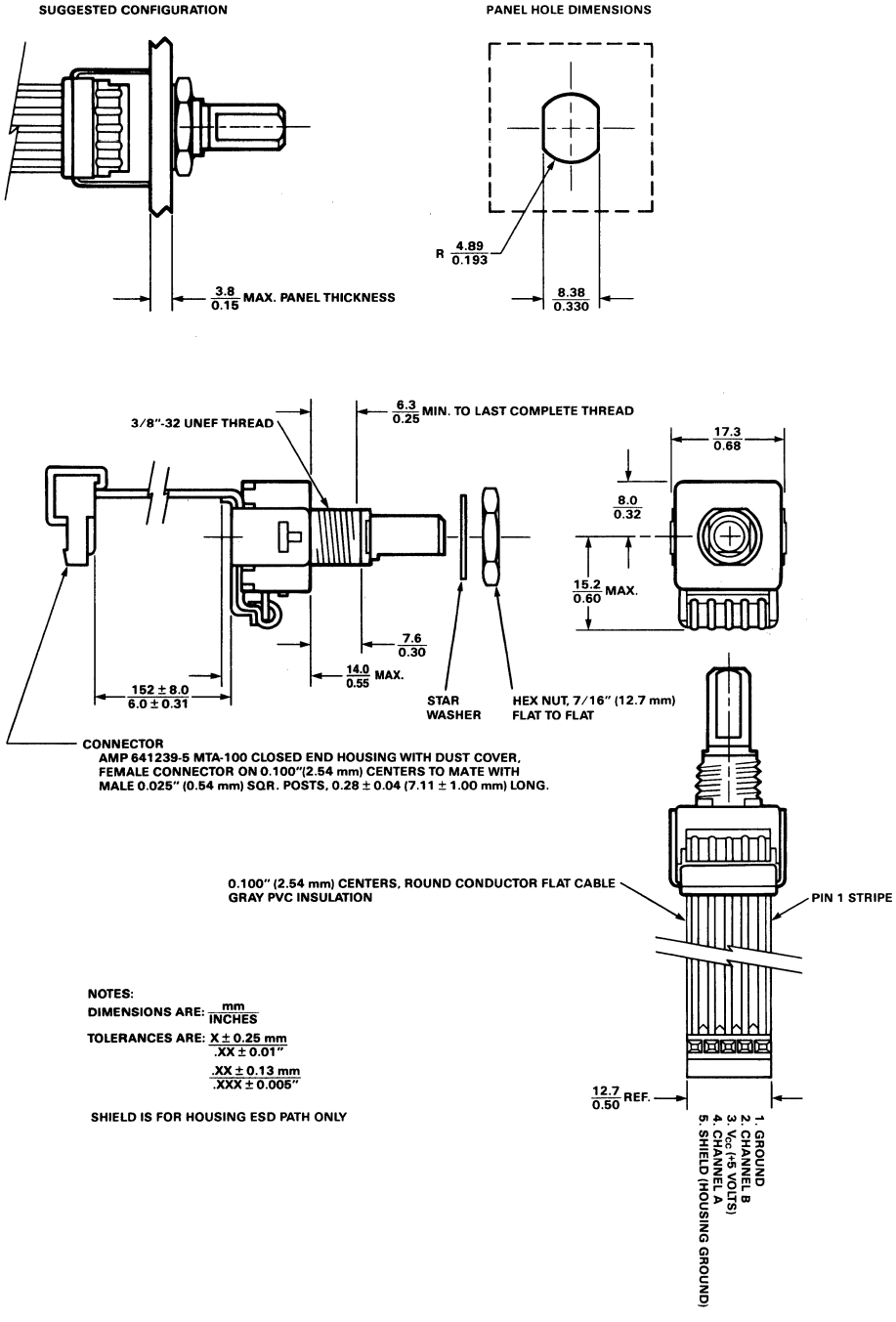




NOTES:
DIMENSIONS ARE: mm / INCHES
TOLERANCES ARE: X ± 0.25 mm / .XX ± 0.01" / .XX ± 0.13 mm / .XXX ± 0.005"

SHIELD IS FOR HOUSING ESD PATH ONLY

Option C – Cable Connector with Strain Relief
HRPG-AXXX#XXC

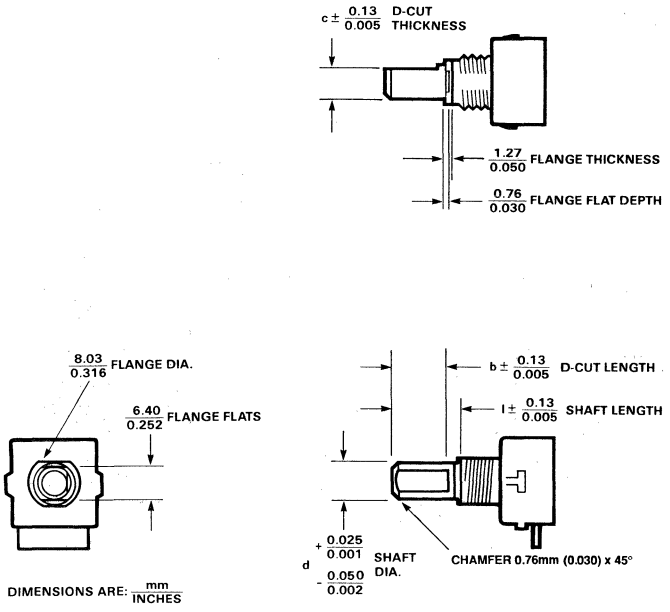


NOTES:
DIMENSIONS ARE: mm / INCHES
TOLERANCES ARE: X ± 0.25 mm / .XX ± 0.01"
.XX ± 0.13 mm / .XXX ± 0.005"

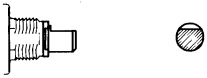
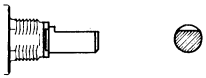
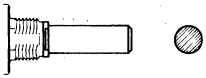
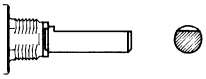
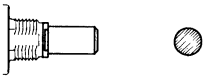
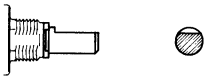
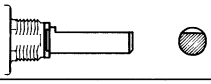
SHIELD IS FOR HOUSING ESD PATH ONLY

Shaft Configurations

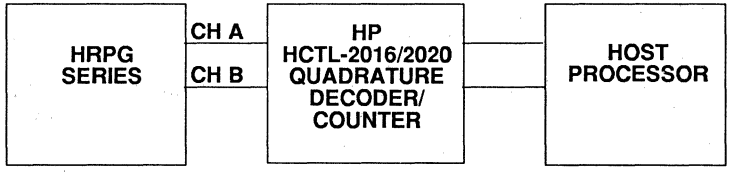
Shaft Dimensions (D-cut shown also)



Shaft Options Available

Option #	Shaft Length (l)	Shaft Diameter (d)	D-Cut Thickness (c)	D-Cut Length (b)	Sketch (not to scale)
11	0.30"	0.251"	–	–	
13	0.30"	0.250"	0.225"	0.230"	
14	0.50"	0.251"	–	–	
16	0.50"	0.250"	0.225"	0.400"	
17	0.80"	0.251"	–	–	
19	0.80"	0.250"	0.225"	0.700"	
51	7.6 mm	6.02 mm	–	–	
53	7.6 mm	6.00 mm	5.33 mm	5.84 mm	
54	12.7 mm	6.02 mm	–	–	
56	12.7 mm	6.00 mm	5.33 mm	10.16 mm	
57	20.32 mm	6.02 mm	–	–	
59	20.32 mm	6.00 mm	5.33 mm	17.78 mm	

Typical Interface



Ordering Information

HRPG - A □□□ # □□□

Shaft Feel / Resolution

S16 – Smooth 16CPR
D16 – Detented 16CPR*
S32 – Smooth 32CPR
D32 – Detented 32CPR*
S64 – Smooth 64CPR
SCA – Smooth 120CPR

Mechanical Configuration

11 – 0.3" long, 0.25" dia.
13 – 0.3" long, 0.25" dia. D-cut
14 – 0.5" long, 0.25" dia.
16 – 0.5" long, 0.25" dia. D-cut
17 – 0.8" long, 0.25" dia.
19 – 0.8" long, 0.25" dia. D-cut
51 – 7.6 mm long, 6 mm dia.
53 – 7.6 mm long, 6 mm dia. D-cut
54 – 12.7 mm long, 6 mm dia.
56 – 12.7 mm long, 6 mm dia. D-cut
57 – 20.3 mm long, 6 mm dia.
59 – 20.3 mm long, 6 mm dia. D-cut

Termination

F – Pins Front with Bracket
R – Pins Rear with Bracket
C – Cable Connector with Strain Relief

*Note: When ordering detented versions, a D-cut shaft is recommended.

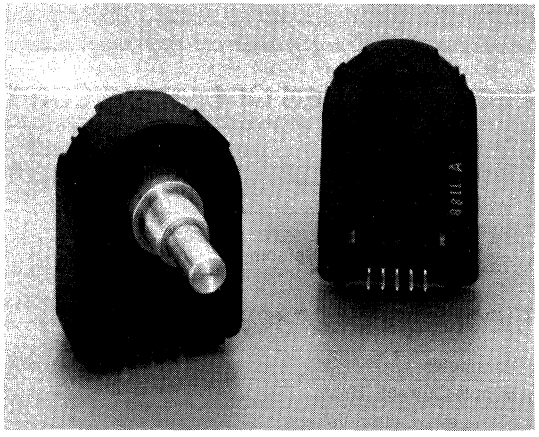
HEWLETT PACKARD

PANEL MOUNT OPTICAL ENCODER

HEDS-5700 SERIES

Features

- **AVAILABLE WITH OR WITHOUT STATIC DRAG FOR MANUAL OR MECHANIZED OPERATION**
- **HIGH RESOLUTION - UP TO 512 CPR**
- **LONG ROTATIONAL LIFE, >1 MILLION REVS**
- **-20 TO 85 °C OPERATING TEMPERATURE RANGE**
- **TTL QUADRATURE OUTPUT**
- **SINGLE 5V SUPPLY**
- **AVAILABLE WITH COLOR CODED LEADS**



Description

The HEDS-5700 series is a family of low cost, high performance, optical incremental encoders with mounted shafts and bushings. The HEDS-5700 is available with tactile feedback for hand operated panel mount applications, or with a free spinning shaft for applications requiring a pre-assembled encoder for position sensing.

The encoder contains a collimated LED light source and special detector circuit which allows for high resolution, excellent encoding performance, long rotational life, and increased reliability. The unit outputs two digital waveforms which are 90 degrees out of phase to provide position and direction information.

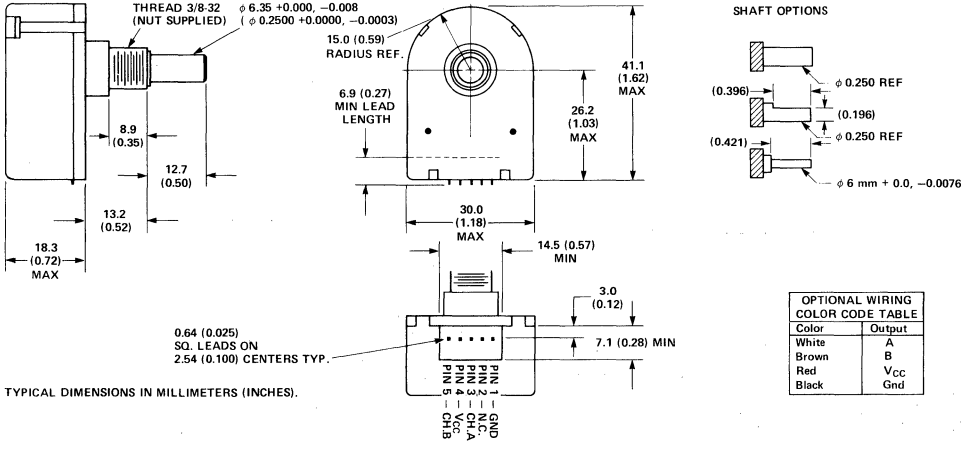
The HEDS-5700 is quickly and easily mounted to a front panel using the threaded bushing, or it can be directly coupled to a motor shaft (or gear train) for position sensing applications.

Applications

The HEDS-5700 with the static drag option is best suited for applications requiring digital information from a manually operated knob. Typical front panel applications include instruments, CAD/CAM systems, and audio/video control boards.

The HEDS-5700 without static drag (free spinning) is best suited for low speed, mechanized operations. Typical applications are copiers, X-Y tables, and assembly line equipment.

Package Dimensions



TYPICAL DIMENSIONS IN MILLIMETERS (INCHES).

OPTIONAL WIRING COLOR CODE TABLE	
Color	Output
White	A
Brown	B
Red	V_{CC}
Black	Gnd

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	+85	°C	
Operating Temperature	T_a	-20	+85	°C	
Vibration			20	g	20Hz - 2kHz
Supply Voltage	V_{CC}	-0.5	7	V	
Output Voltage	V_O	-0.5	V_{CC}	V	
Output Current Per Channel	I_O	-1	5	mA	
Shaft Load - Axial			1	lb	
- Radial			1	lb	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	-20	+85	°C	Non Condensing Atmosphere
Suppy Voltage	V_{CC}	4.5	5.5	V	Ripple <100mV_{p-p}
Rotation Speed - Drag			300	RPM	
- Free Spinning			2000	RPM	

Electrical Characteristics Over Recommended Operating Range, Typical at 25°C

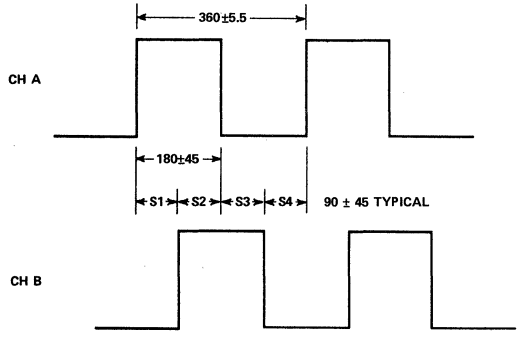
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		17	40	mA	
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40μA Max.
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2mA

Note: If more source current is required, use a 3.2K pullup resistor on each output.

Mechanical Characteristics

Parameter	Min.	Typ.	Max.	Units	Notes
Starting Torque - Static Drag		0.47		oz in	
- Free Spinning			0.14	oz in	
Dynamic Drag - Static Drag		1.1		oz in	100 RPM
- Free Spinning		0.70		oz in	2000 RPM
Rotational Life - Static Drag	1 x 10^6			Revolutions	1 lb Load
- Free Spinning	12 x 10^6			Revolutions	4 oz Radial Load
Mounting Torque of Nut			13	lb in	

Output Waveforms



NOTE: All values are in electrical degrees, where 360°e=1 cycle of resolution.
Errors are worst case over one revolution.
CH B leads CH A for counterclockwise rotation.
CH A leads CH B for clockwise rotation.

Ordering Information

HEDS-570□-□□□

Mechanical Configuration
0 - Pins
1 - 6" Color Coded Leads

Shaft Configuration
0 - 1/4" dia. with no flat
1 - 6mm dia. with no flat
2 - 1/4" dia. with flat

Resolutions (Cycles Per Revolution)
K=96 CPR G=360 CPR
C=100 CPR H=400 CPR
D=192 CPR A=500 CPR
E=200 CPR I=512 CPR
F=256 CPR

Drag Option
0 - Free Spinning
1 - Static Drag

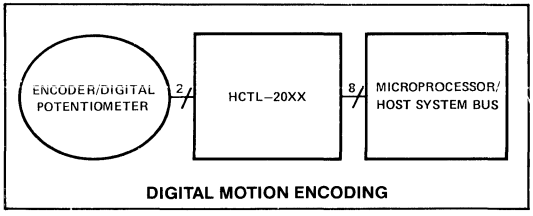
HEWLETT PACKARD

QUADRATURE DECODER/ COUNTER INTERFACE IC

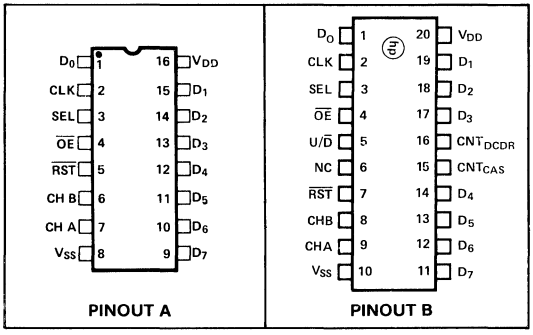
HCTL-2000
HCTL-2016
HCTL-2020

Features

- **INTERFACES ENCODER TO MICROPROCESSOR**
- **14 MHz CLOCK OPERATION**
- **FULL 4X DECODE**
- **HIGH NOISE IMMUNITY:**
  SCHMITT TRIGGER INPUTS
  DIGITAL NOISE FILTER
- **12 OR 16-BIT BINARY UP/DOWN COUNTER**
- **LATCHED OUTPUTS**
- **8-BIT TRISTATE INTERFACE**
- **8, 12, OR 16-BIT OPERATING MODES**
- **QUADRATURE DECODER OUTPUT SIGNALS, UP/DOWN AND COUNT**
- **CASCADE OUTPUT SIGNALS, UP/DOWN AND COUNT**
- **SUBSTANTIALLY REDUCED SYSTEM SOFTWARE**



DIGITAL MOTION ENCODING



PINOUT A PINOUT B

Description

The HCTL-2000, 2016, 2020 are CMOS ICs that perform the quadrature decoder, counter, and bus interface function. The HCTL-20XX family is designed to improve system performance in digital closed loop motion control systems and digital data input systems. It does this by shifting time intensive quadrature decoder functions to a cost effective hardware solution. The entire HCTL-20XX family consists of a 4x quadrature decoder, a binary up/down state counter, and an 8-bit bus interface. The use of Schmitt-triggered CMOS inputs and input noise filters allows reliable operation in noisy environments. The HCTL-2000 contains a 12-bit counter. The HCTL-2016 and 2020 contain a 16-bit counter. The HCTL-2020 also contains quadrature decoder output signals and cascade signals for use with many standard counter ICs. The HCTL-20XX family provides LSTTL compatible tri-state output buffers. Operation is specified for a temperature range from -40 to +85°C at clock frequencies up to 14 MHz.

Applications

- **INTERFACE QUADRATURE INCREMENTAL ENCODERS TO MICROPROCESSORS**
- **INTERFACE DIGITAL POTENTIOMETERS TO DIGITAL DATA INPUT BUSES**

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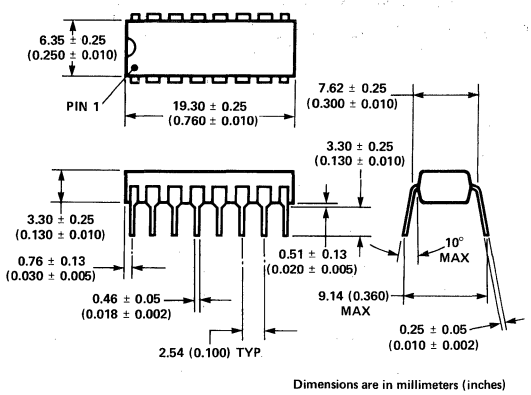
- MOTOROLA 6802/8, 24-BIT CASCADE 12
- INTEL 8748 15

ESD WARNING: Standard CMOS handling precautions should be observed with the HCTL-20XX family ICs.

Devices

Part Number	Description	Package Drawing
HCTL-2000	12-bit counter. 14 MHz clock operation.	A
HCTL-2016	All features of the HCTL-2000. 16-bit counter.	A
HCTL-2020	All features of the HCTL-2016. Quadrature decoder output signals. Cascade output signals.	B

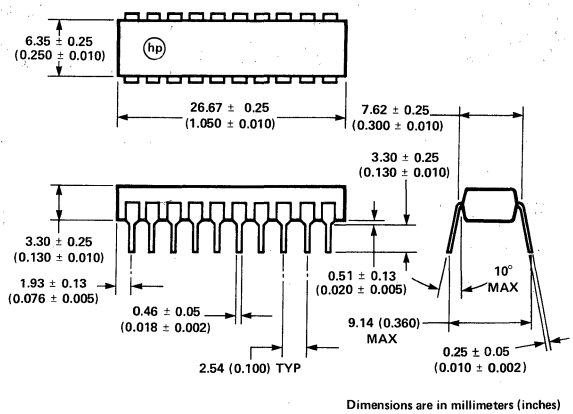
Package Dimensions



Dimensions are in millimeters (inches)

PACKAGE A LEAD FINISH: SOLDER DIPPED

PACKAGE A



Dimensions are in millimeters (inches)

PACKAGE B LEAD FINISH: SOLDER DIPPED

PACKAGE B

Operating Characteristics

Table 1. Absolute Maximum Ratings (All voltages below are referenced to V_{SS})

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	-0.3 to +5.5	V
Input Voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Storage Temperature	T_S	-40 to +125	°C
Operating Temperature	T_A[1]	-40 to +85	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	+4.5 to +5.5	V
Ambient Temperature	T_A[1]	-40 to +85	°C

Table 3. DC Characteristics V_{DD} = 5 V ± 5%; T_A = -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}[2]	Low-Level Input Voltage				1.5	V
V_{IH}[2]	High-Level Input Voltage		3.5			V
V_{T+}	Schmitt-Trigger Positive-Going Threshold			3.5	4.0	V
V_{T-}	Schmitt-Trigger Negative-Going Threshold		1.0	1.5		V
V_H	Schmitt-Trigger Hysteresis		1.0	2.0		V
I_{IN}	Input Current	V_{IN} = V_{SS} or V_{DD}	-10	1	+10	μA
V_{OH}[2]	High-Level Output Voltage	I_{OH} -1.6 mA	2.4	4.5		V
V_{OL}[2]	Low-Level Output Voltage	I_{OL} = +4.8 mA		0.2	0.4	V
I_{OZ}	High-Z Output Leakage Current	V_O = V_{SS} or V_{DD}	-10	1	+10	μA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{SS} or V_{DD}, V_O = HiZ		1	5	μA
C_{IN}	Input Capacitance	Any Input[3]		5		pF
C_{OUT}	Output Capacitance	Any Output[3]		6		pF

Notes:
1. Free Air
2. In general, for any V_{DD} between the allowable limits (+4.5 V to +5.5 V), V_{IL} = 0.3 V_{DD} and V_{IH} = 0.7 V_{DD}; typical values are V_{OH} = V_{DD} - 0.5 V @ I_{OH} = -40 μA and V_{OL} = V_{SS} + 0.2 V @ I_{OL} = 1.6 mA.
3. Including package capacitance.

Functional Pin Description

Table 4. Functional Pin Descriptions

Symbol	Pin 2000/2016	Pin 2020	Description
V_{DD}	16	20	Power Supply
V_{SS}	8	10	Ground
CLK	2	2	CLK is a Schmitt-trigger input for the external clock signal.
CHA CHB	7 6	9 8	CHA and CHB are Schmitt-trigger inputs which accept the outputs from a quadrature encoded source, such as incremental optical shaft encoder. Two channels, A and B, nominally 90 degrees out of phase, are required.
$\overline{RST}$	5	7	This active low Schmitt-trigger input clears the internal position counter and the position latch. It also resets the inhibit logic. $\overline{RST}$ is asynchronous with respect to any other input signals.
$\overline{OE}$	4	4	This CMOS active low input enables the tri-state output buffers. The $\overline{OE}$ and SEL inputs are sampled by the internal inhibit logic on the falling edge of the clock to control the loading of the internal position data latch.
SEL	3	3	This CMOS input directly controls which data byte from the position latch is enabled into the 8-bit tri-state output buffer. As in $\overline{OE}$ above, SEL also controls the internal inhibit logic. SEL = 0: High byte selected SEL = 1: Low byte selected
CNT_{DCDR}		16	A pulse is presented on this LSTTL-compatible output when the quadrature decoder has detected a state transition.
U/$\overline{D}$		5	This LSTTL-compatible output allows the user to determine whether the IC is counting up or down and is intended to be used with the CNT_{DCDR} and CNT_{CAS} outputs. The proper signal U (high level) or $\overline{D}$ (low level) will be present before the rising edge of the CNT_{DCDR} and CNT_{CAS} outputs.
CNT_{CAS}		15	A pulse is presented on this LSTTL-compatible output when the HCTL-2020 internal counter overflows or underflows. The rising edge on this waveform may be used to trigger an external counter.
D0	1	1	These LSTTL-compatible tri-state outputs form an 8-bit output port through which the contents of the 12/16-bit position latch may be read in 2 sequential bytes. The high byte, containing bits 8-15, is read first (on the HCTL-2000, the most significant 4 bits of this byte are set to 0 internally). The lower byte, bits 0-7, is read second.
D1	15	19	
D2	14	18	
D3	13	17	
D4	12	14	
D5	11	13	
D6	10	12	
D7	9	11	
NC		6	Not connected — this pin should be left floating.

Switching Characteristics

Table 5. Switching Characteristics Min/Max specifications at V_{DD} = 5.0 ± 5%, T_A = -40 to + 85°C

	Symbol	Description	Min.	Max.	Units
1	t_{CLK}	Clock period	70		ns
2	t_{CHH}	Pulse width, clock high	28		ns
3	t_{CD}[1]	Delay time, rising edge of clock to valid, updated count information on D0-7		65	ns
4	t_{ODE}	Delay time, $\overline{OE}$ fall to valid data		65	ns
5	t_{ODZ}	Delay time, $\overline{OE}$ rise to Hi-Z state on D0-7		40	ns
6	t_{SDV}	Delay time, SEL valid to stable, selected data byte (delay to High Byte = delay to Low Byte)		65	ns
7	t_{CLH}	Pulse width, clock low	28		ns
8	t_{SS}[2]	Setup time, SEL before clock fall	20		ns
9	t_{OS}[2]	Setup time, $\overline{OE}$ before clock fall	20		ns
10	t_{SH}[2]	Hold time, SEL after clock fall	0		ns
11	t_{OH}[2]	Hold time, $\overline{OE}$ after clock fall	0		ns
12	t_{RST}	Pulse width, $\overline{RST}$ low	28		ns
13	t_{DCD}	Hold time, last position count stable on D0-7 after clock rise	10		ns
14	t_{DSD}	Hold time, last data byte stable after next SEL state change	5		ns
15	t_{DOD}	Hold time, data byte stable after $\overline{OE}$ rise	5		ns
16	t_{UDD}	Delay time, U/$\overline{D}$ valid after clock rise		45	ns
17	t_{CHD}	Delay time, CNT_{DCDR} or CNT_{CAS} high after clock rise		45	ns
18	t_{CLD}	Delay time, CNT_{DCDR} or CNT_{CAS} low after clock fall		45	ns
19	t_{UDH}	Hold time, U/$\overline{D}$ stable after clock rise	10		ns
20	t_{UDCS}	Setup time, U/$\overline{D}$ valid before CNT_{DCDR} or CNT_{CAS} rise	t_{CLK}-45		ns
21	t_{UDCH}	Hold time, U/$\overline{D}$ stable after CNT_{DCDR} or CNT_{CAS} rise	t_{CLK}-45		ns

Notes:

1. t_{CD} specification and waveform assume latch not inhibited.
2. t_{SS}, t_{OS}, t_{SH}, t_{OH} only pertain to proper operation of the inhibit logic. In other cases, such as 8 bit read operations, these setup and hold times do not need to be observed.

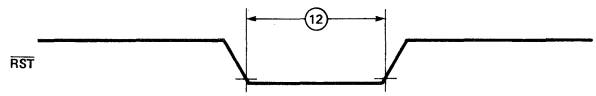


Figure 1. Reset Waveform

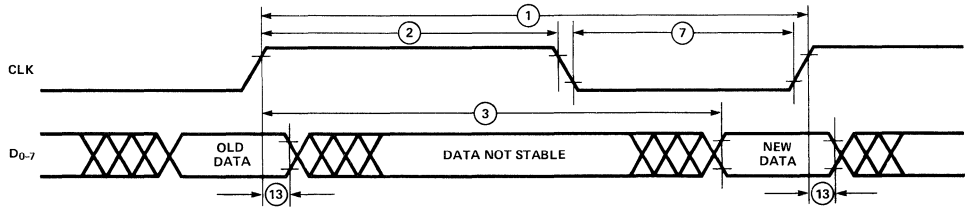


Figure 2. Waveform for Positive Clock Related Delays

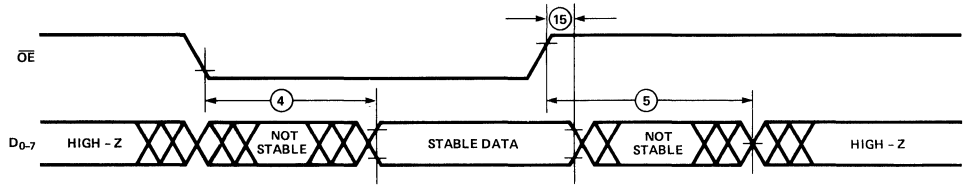


Figure 3. Tri-State Output Timing

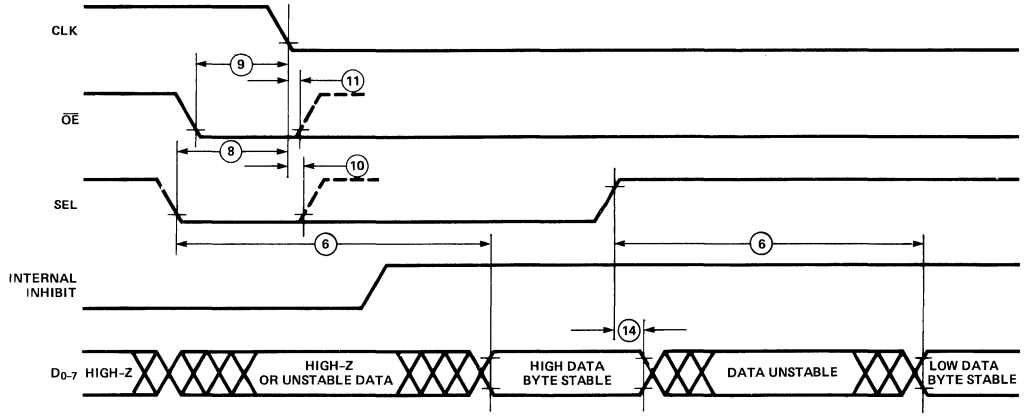


Figure 4. Bus Control Timing

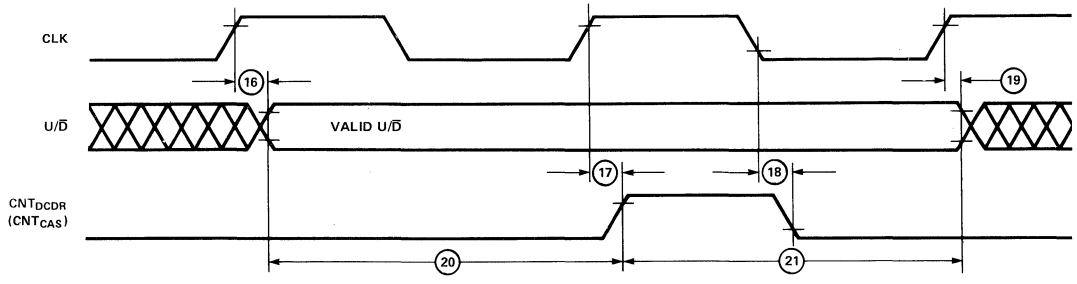


Figure 5. Decoder, Cascade Output Timing (HCTL-2020 only)

Operation

A block diagram of the HCTL-20XX family is shown in Figure 6. The operation of each major function is described in the following sections.

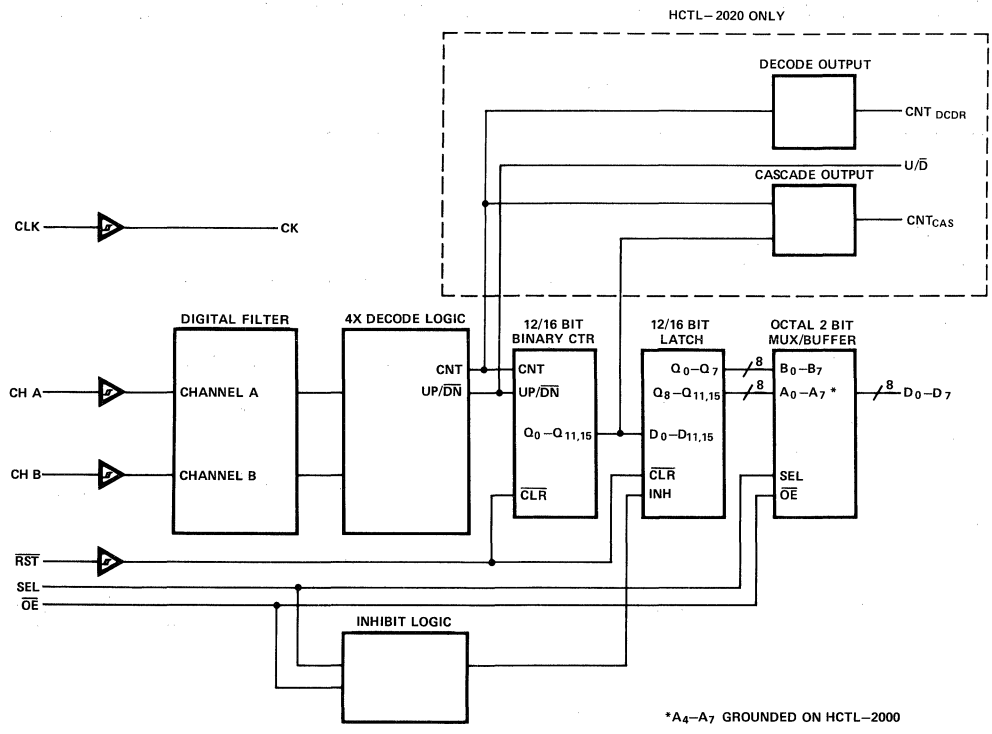


Figure 6. Simplified Logic Diagram

DIGITAL NOISE FILTER

The digital noise filter section is responsible for rejecting noise on the incoming quadrature signals. The input section uses two techniques to implement improved noise rejection. Schmitt-trigger inputs and a three-clock-cycle delay filter combine to reject low level noise and large, short duration noise spikes that typically occur in motor system applications. Both common mode and differential mode noise are rejected. The user benefits from these techniques by improved integrity of the data in the counter. False counts triggered by noise are avoided.

Figure 7 shows the simplified schematic of the input section. The signals are first passed through a Schmitt trigger buffer to address the problem of input signals with slow rise times and low level noise (approximately < 1 V). The cleaned up signals are then passed to a four-bit delay filter. The signals on each channel are sampled on rising clock edges. A time history of the signals is stored in the four-bit shift register. Any change on the input is tested for a stable level being present for three consecutive rising clock edges. Therefore, the filtered output waveforms can change only after an input level has the same value for three consecutive rising clock edges. Refer to Figure 8 which shows the timing diagram. The result of this circuitry is that short noise spikes between rising clock edges are ignored and pulses shorter than two clock periods are rejected.

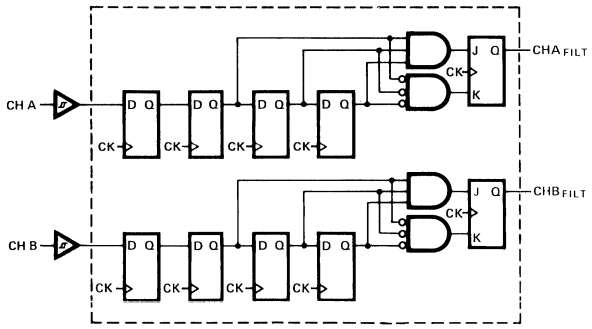


Figure 7. Simplified Digital Noise Filter Logic

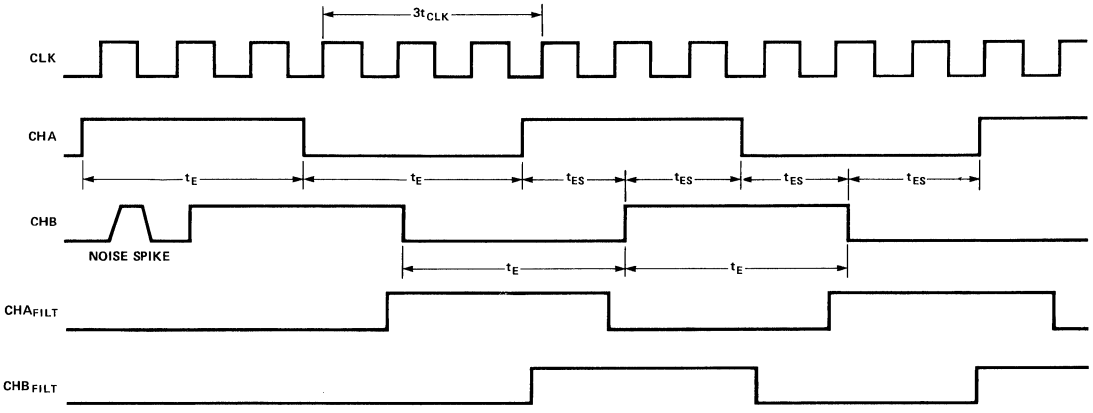


Figure 8. Signal Propagation Through Digital Noise Filter

QUADRATURE DECODER

The quadrature decoder decodes the incoming filtered signals into count information. This circuitry multiplies the resolution of the input signals by a factor of four (4X decoding). When using an encoder for motion sensing, the user benefits from the increased resolution by being able to provide better system control.

The quadrature decoder samples the outputs of the CHA and CHB filters. Based on the past binary state of the two signals and the present state, it outputs a count signal and a direction signal to the internal position counter. In the case of the HCTL-2020, the signals also go to external pins 5 and 16 respectively.

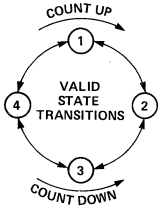
Figure 9 shows the quadrature states and the valid state transitions. Channel A leading channel B results in counting up. Channel B leading channel A results in counting down. Illegal state transitions, caused by faulty encoders or noise severe enough to pass through the filter, will produce an erroneous count.

DESIGN CONSIDERATIONS

The designer should be aware that the operation of the digital filter places a timing constraint on the relationship between incoming quadrature signals and the external clock. Figure 8 shows the timing waveform with an incremental encoder input. Since an input has to be stable for three rising clock edges, the encoder pulse width (t_E - low or high), has to be greater than three clock periods ($3t_{CLK}$). This guarantees that the asynchronous input will be stable during three consecutive rising clock edges. A realistic design also has to take into account finite rise times of the waveforms, asymmetry of the waveforms, and noise. In the presence of large amounts of noise, t_E should be much

greater than $3t_{CLK}$ to allow for the interruption of the consecutive level sampling by the three-bit delay filter. It should be noted that a change on the inputs that is qualified by the filter will internally propagate in a maximum of seven clock periods.

The quadrature decoder circuitry imposes a second timing constraint between the external clock and the input signals. There must be at least one clock period between consecutive quadrature states. As shown in Figure 9, a quadrature state is defined by consecutive edges on both channels. Therefore, t_{ES} (encoder state period) > t_{CLK}. The designer must account for deviations from the nominal 90 degree phasing of input signals to guarantee that t_{ES} > t_{CLK}.



CHA	CHB	STATE
1	0	1
1	1	2
0	1	3
0	0	4

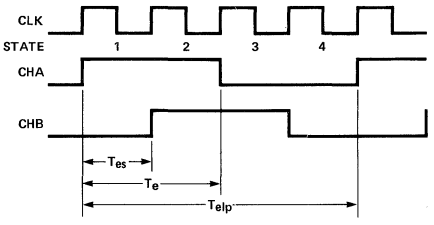


Figure 9. 4x Quadrature Decoding

POSITION COUNTER

This section consists of a 12-bit (HCTL-2000) or 16-bit (HCTL-2016/2020) binary up/down counter which counts on rising clock edges as explained in the Quadrature Decoder Section. All 12 or 16 bits of data are passed to the position data latch. The system can use this count data in several ways:

A. System total range is ≤ 12 or 16 bits, so the count represents "absolute" position.

B. The system is cyclic with ≤ 12 or 16 bits of count per cycle. $\overline{RST}$ is used to reset the counter every cycle and the system uses the data to interpolate within the cycle.

C. System count is > 8, 12 or 16 bits, so the count data is used as a relative or incremental position input for a system software computation of absolute position. In this case counter rollover occurs. In order to prevent loss of position information, the processor must read the outputs of the IC before the count increments one-half of the maximum count capability (i.e. 127, 2047, or 32,767 quadrature counts). Two's-complement arithmetic is normally used to compute position from these periodic position updates. Three modes can be used:

1. The IC can be put in 8-bit mode by tying the SEL line high, thus simplifying IC interface. The outputs must then be read at least once every 127 quadrature counts.
2. The HCTL-2000 can be used in 12-bit mode and sampled at least once every 2047 quadrature counts.
3. The HCTL-2016 or 2020 can be used in 16-bit mode and sampled at least once every 32,767 quadrature counts.

D. The system count is > 16 bits so the HCTL-2020 can be cascaded with other standard counter IC's to give absolute position.

POSITION DATA LATCH

The position data latch is a 12/16-bit latch which captures the position counter output data on each rising clock edge, except when its inputs are disabled by the inhibit logic section during two-byte read operations. The output data is passed to the bus interface section. When active, a signal from the inhibit logic section prevents new data from being captured by the latch, keeping the data stable while successive reads are made through the bus section. The latch is automatically reenabled at the end of these reads. The latch is cleared to 0 asynchronously by the $\overline{RST}$ signal.

INHIBIT LOGIC

The Inhibit Logic Section samples the $\overline{OE}$ and SEL signals on the falling edge of the clock and, in response to certain conditions (see Figure 10 below), inhibits the position data latch. The $\overline{RST}$ signal asynchronously clears the inhibit logic, enabling the latch. A simplified logic diagram of the inhibit circuitry is illustrated in Figure 11.

STEP	SEL	$\overline{OE}$	CLK	INHIBIT SIGNAL	ACTION
1	L	L	⌊	1	SET INHIBIT; READ HIGH BYTE
2	H	L	⌊	1	READ LOW BYTE; STARTS RESET
3	X	H	⌊	0	COMPLETES INHIBIT LOGIC RESET

Figure 10. Two Byte Read Sequence

BUS INTERFACE

The bus interface section consists of a 16 to 8 line multiplexer and an 8-bit, three-state output buffer. The multiplexer allows independent access to the low and high bytes of the position data latch. The SEL and $\overline{OE}$ signals determine which byte is output and whether or not the output bus is in the high-Z state. In the case of the HCTL-2000 the data latch is only 12 bits wide and the upper four bits of the high byte are internally set to zero.

QUADRATURE DECODER OUTPUT (HCTL-2020 ONLY)

The quadrature decoder output section consists of count and up/down outputs derived from the 4X decode logic of the HCTL-2020. When the decoder has detected a count, a pulse, one-half clock cycle long, will be output on the CNT_{DCDR} pin. This output will occur during the clock cycle in which the internal counter is updated. The U/$\overline{D}$ pin will be set to the proper voltage level one clock cycle before the rising edge of the CNT_{DCDR} pulse, and held one clock cycle after the rising edge of the CNT_{DCDR} pulse. These outputs are not affected by the inhibit logic. See Figures 5 and 12 for detailed timing.

CASCADE OUTPUT (HCTL-2020 ONLY)

The cascade output also consists of count and up/down outputs. When the HCTL-2020 internal counter overflows or underflows, a pulse, one-half clock cycle long, will be output on the CNT_{CAS} pin. This output will occur during the clock cycle in which the internal counter is updated. The U/$\overline{D}$ pin will be set to the proper voltage level one clock cycle before the rising edge of the CNT_{CAS} pulse, and held one clock cycle after the rising edge of the CNT_{CAS} pulse. These outputs are not affected by the inhibit logic. See Figures 5 and 12 for detailed timing.

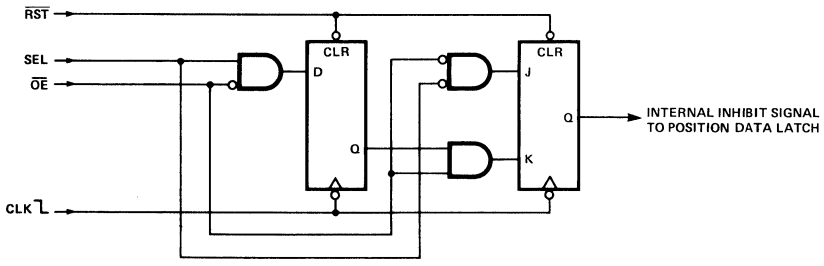
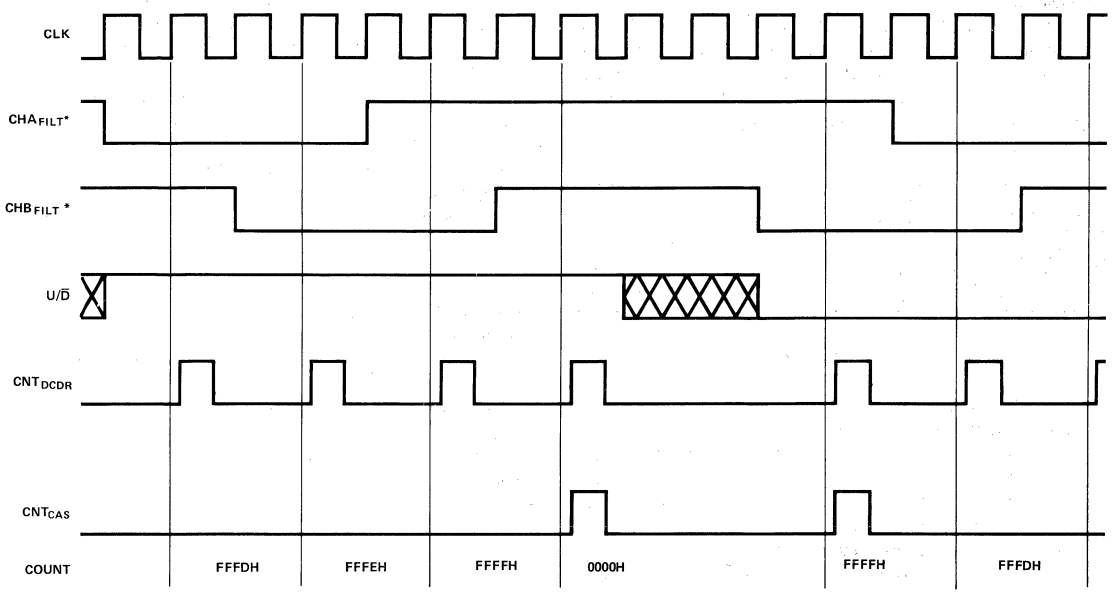


Figure 11. Simplified Inhibit Logic



*CHA_{FILT} and CHB_{FILT} are the outputs of the digital noise filter (see figures 7 and 8).

Figure 12. Decode and Cascade Output Diagram

CASCADE CONSIDERATIONS (HCTL-2020 ONLY)

The HCTL-2020's cascading system allows for position reads of more than two bytes. These reads can be accomplished by latching all of the bytes and then reading the bytes sequentially over the 8-bit bus. Care must be taken to latch all of the bytes such that they represent the count as it actually is, despite propagation delays through the counters.

A good understanding of the mechanics of count propagation is important in designing a proper interface. Consider the sequence of events for a read cycle that starts as the HCTL-2020's internal counter rolls over. On the rising clock edge, count data is updated in the internal counter, rolling it over. A count-cascade pulse (CNT_{CAS}) will be generated with some delay after the rising clock edge (t_{CHD}). There will be additional propagation delays through the external counters and registers. Meanwhile, with $\overline{OE}$ and SEL low to start the read, this new count on the HCTL-2020 will be latched in on the falling clock edge of this cycle. If the external registers are latched too soon, before the CNT_{CAS} pulse has toggled the external counters and registers, a major count error will occur.

Valid data can be ensured by latching the external counter data on the first rising clock edge following the falling edge on which the internal count on the HCTL-2020 is latched (provided that all the delays are less than one clock cycle). This will ensure that a cascade pulse that occurs during the clock cycle when the read begins has adequate time to propagate. This also guarantees that a cascade pulse occurring on the clock cycle after the read is initiated will not be erroneously latched.

For example, suppose the HCTL-2020 count is at FFFFH and an external counter is at F0H, with the count going up. A count occurring in the HCTL-2020 will cause the counter to roll over and a cascade pulse will be generated. A read starting on this clock cycle will show 0000H from the HCTL-2020. The external counter should read F1H, but if the host latches the count before the cascade signal propagates through, the external counter will still read F0H.

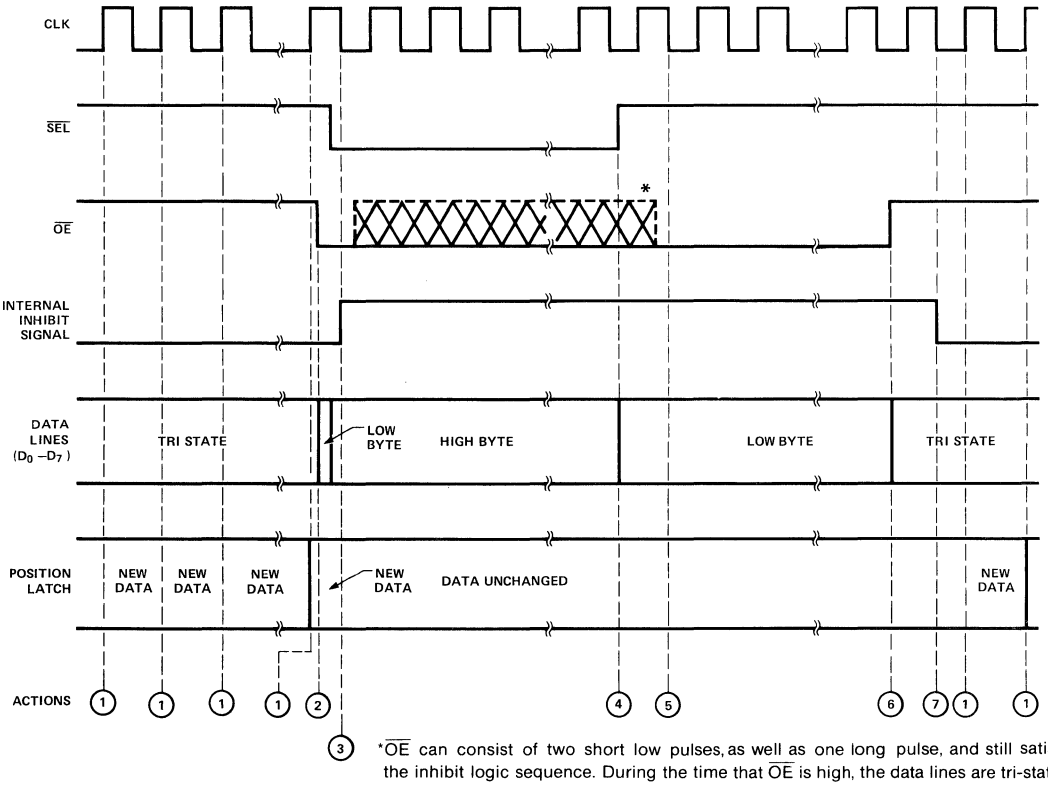
General Interfacing

The 12-bit (HCTL-2000) or 16-bit (HCTL-2016/2020) latch and inhibit logic allows access to 12 or 16 bits of count with an 8-bit bus. When only 8-bits of count are required, a simple 8-bit (1-byte) mode is available by holding SEL high continuously. This disables the inhibit logic. $\overline{OE}$ provides control of the tri-state bus, and read timing is shown in Figures 2 and 3.

For proper operation of the inhibit logic during a two-byte read, $\overline{OE}$ and SEL must be synchronous with CLK due to the falling edge sampling of $\overline{OE}$ and SEL.

The internal inhibit logic on the HCTL-20XX family inhibits the transfer of data from the counter to the position data latch during the time that the latch outputs are being read. The inhibit logic allows the microprocessor to first read the high order 4 or 8 bits from the latch and then read the low order 8 bits from the latch. Meanwhile, the counter can continue to keep track of the quadrature states from the CHA and CHB input signals.

Figure 11 shows the simplified inhibit logic circuit. The operation of the circuitry is illustrated in the read timing shown in Figure 13.



*$\overline{OE}$ can consist of two short low pulses, as well as one long pulse, and still satisfy the inhibit logic sequence. During the time that $\overline{OE}$ is high, the data lines are tri-stated.

Figure 13. Typical Interface Timing

ACTIONS

1. On the rising edge of the clock, counter data is transferred to the position data latch, provided the inhibit signal is low.

2. When $\overline{OE}$ goes low, the outputs of the multiplexer are enabled onto the data lines. If SEL is low, then the high order data bytes are enabled onto the data lines. If SEL is high, then the low order data bytes are enabled onto the data lines.

3. When the IC detects a low on $\overline{OE}$ and SEL during a falling clock edge, the internal inhibit signal is activated. This blocks new data from being transferred from the counter to the position data latch.

4. When SEL goes high, the data outputs change from the high byte to the low byte.

5. The first of two reset conditions for the inhibit logic is met when the IC detects a logic high on SEL and a logic low on $\overline{OE}$ during a falling clock edge.

6. When $\overline{OE}$ goes high, the data lines change to a high impedance state.

7. The IC detects a logic high on $\overline{OE}$ during a falling clock edge. This satisfies the second reset condition for the inhibit logic.

Interfacing the HCTL-2020 to a Motorola 6802/8 and Cascading the Counter for 24 Bits

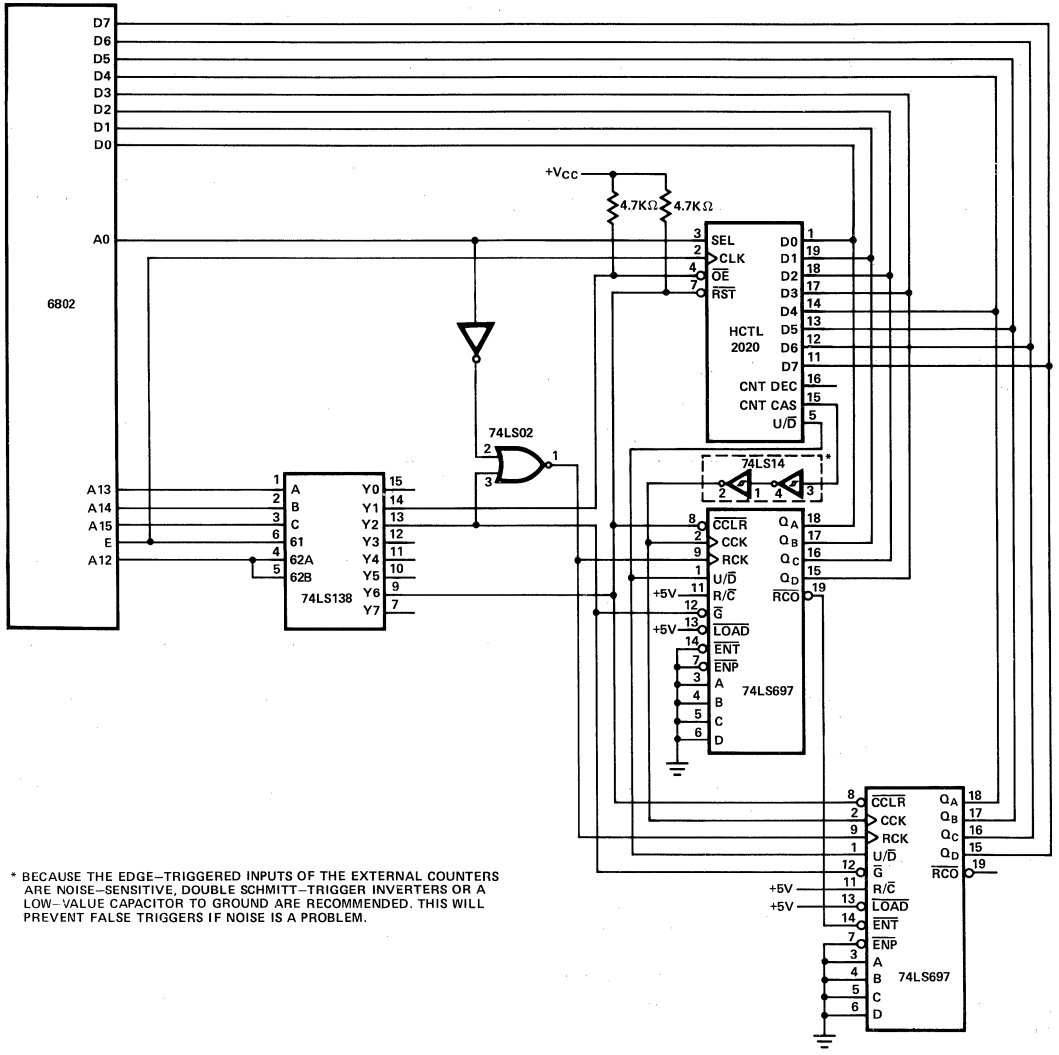


Figure 14. A Circuit to Interface to the 6802/8

In this circuit an interface to a Motorola 6802/8 and a cascading scheme for a 24-bit counter are shown. This circuit provides a minimum part count by: 1) using two 74LS697 Up/Down counters with output registers and tri-state outputs and 2) using a Motorola 6802/8 LDX instruction which stores 16 bits of data into the index registers in two consecutive clock cycles.

The HCTL-2020 $\overline{OE}$ and the 74LS697 $\overline{G}$ lines are decoded from Address lines A15-A13. This results in counter data being enabled onto the bus whenever an external memory access is made to locations 4XXX or 2XXX. Address line A12 and processor clock E enable the 74LS138. The processor clock E is also used to clock the HCTL-2020. Address A0 is connected directly to the SEL pin on the HCTL-2020. This line selects the low or high byte of data from the HCTL-2020.

Cascading is accomplished by connecting the CNT_{CAS} output on the HCTL-2020 with the counter clock (CCK) input on both 74LS697's. The U/$\overline{D}$ pin on the HCTL-2020 and the U/$\overline{D}$ pin on both 74LS697's are also directly connected for easy expansion. The $\overline{RCO}$ of the first 4-bit 74LS697 is connected to the $\overline{ENT}$ pin of the second 74LS697. This enables the second counter only when there is a $\overline{RCO}$ signal on the first counter.

This configuration allows the 6802 to read both data bytes with a single double-byte fetch instruction (LDX 2XX0). This instruction is a five cycle instruction which reads external memory location 2XX0 and stores the high order byte into the high byte of the index register. Memory location 2XX1 is next read and stored in the low order byte of the index register. The high byte of counter data is clocked into the 74LS697 registers when SEL is high and $\overline{OE}$ goes low. This upper byte can be read at any time by pulling the 74LS697 $\overline{G}$ low when reading address 4XXX. Figure 15 shows memory addresses and gives an example of reading the HCTL-2020. Figure 16 shows the interface timing for the circuit.

Address	Function
CXXX	Reset Counters
4XXX	Enable High Byte on Data Lines
2XX0	Enable Low Byte on Data Lines
2XX1	Enable Mid Byte on Data Lines

Read Example	
LDX 2000 STX 0100	Loads mid byte and then low byte into memory locations 0100 and 0101
LDAA 4000 STAA 0102	Loads the high byte into memory location 0102

Figure 15. Memory Addresses and Read Example

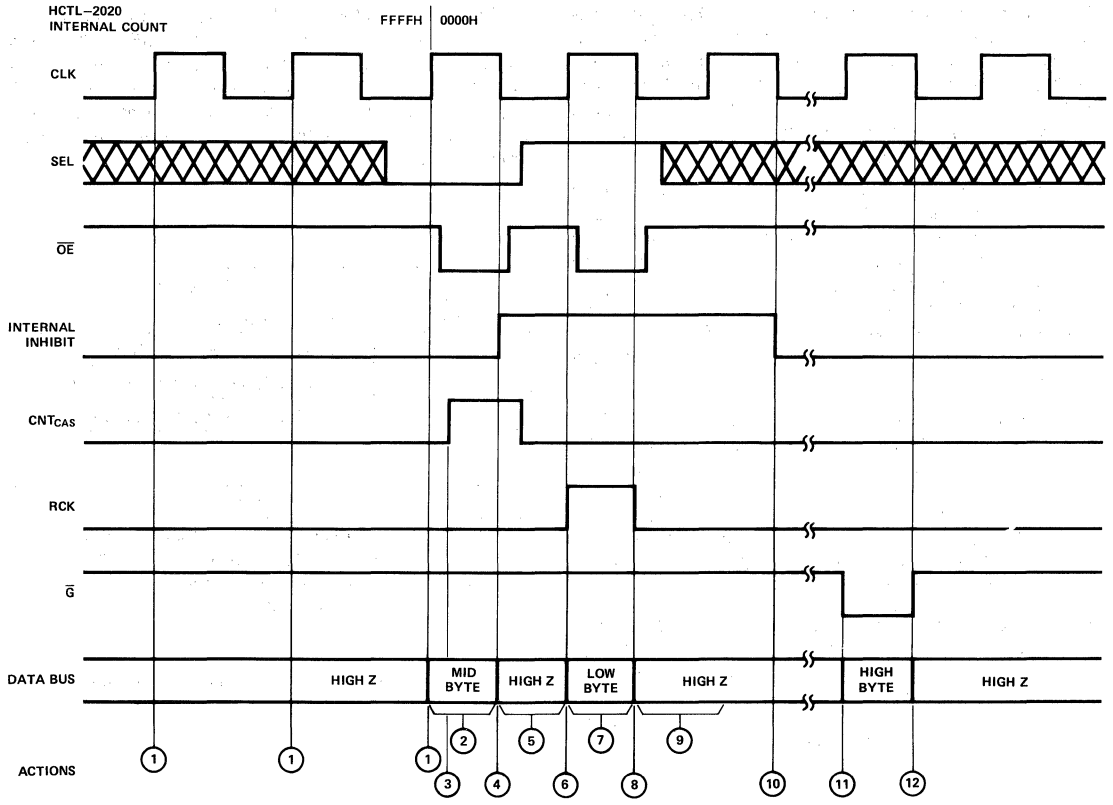


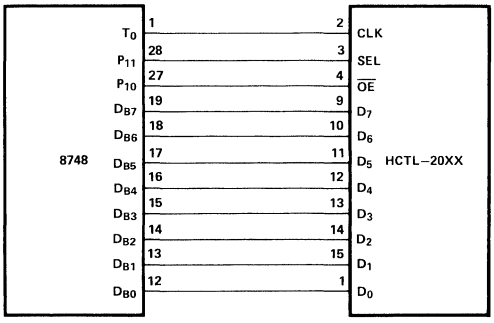
Figure 16. Interface Timing for the 6802/8

ACTIONS

1. The microprocessor clock output is E. If the internal HCTL-2020 inhibit is not active, new data is transferred from the internal counter to the position data latch.
2. An even address output from the 6802 causes SEL to go low. When E goes high, the address decoder output for the HCTL-2020 $\overline{OE}$ signal goes low. This causes the HCTL-2020 to output the middle byte of the system counter (high byte of the HCTL-2020 counter).
3. In this case, the HCTL-2020 counter has overflowed and there is an output on the CNT_{CAS} line. This pulse is counted by the 74LS697 but not loaded into the output register of the 74LS697 at this time.
4. The 6802 reads the data bus on the falling edge of E, storing the high order 2020 data byte (middle system byte) into the high byte of the index register. The chip detects that $\overline{OE}$ and SEL are low on the falling edge of E and activates the internal inhibit signal. The position data latch is inhibited and data cannot be transferred from the internal counter to the latch.
5. When E goes low, the address decoder output is disabled and $\overline{OE}$ goes high. The 6802 increments the address, causing SEL to go high. The position data latch is still inhibited.
6. When SEL is high and $\overline{OE}$ is low the 74LS697 register clock (RCK) goes high. The rising edge of RCK loads the 74LS697 count into the 74LS697 register. Delaying the RCK signal until the second $\overline{OE}$ allows for delays on the CNT_{CAS} signal.
7. The address decoder is enabled after E goes high. The $\overline{OE}$ line goes low and the low data byte is enabled onto the bus.
8. The 6802 reads the data bus on the falling edge of E, storing the low order data byte into the low byte of the index register. The HCTL-2020 detects that $\overline{OE}$ is low and SEL is high on the falling edge of E, thus meeting the first inhibit reset condition.
9. When E goes low, the address decoder is disabled, causing $\overline{OE}$ to go high and the data lines to go to the high impedance state. The 6802 continues its instruction execution, and the state of SEL is indeterminate.
10. The HCTL-2020 detects $\overline{OE}$ is high on the next falling edge of E. This satisfies the second inhibit reset condition and the inhibit signal is reset.
11. When E goes high, a new address causes the $\overline{G}$ line on the 74LS697 to go low and enables the high byte onto the data bus.
12. When E goes low, the high byte is read into the 6802. The data bus returns to tri-state.

Interfacing the HCTL-20XX to an Intel 8748

The circuit shown in Figure 17 shows the connections between an HCTL-20XX and an 8748. Data lines D0-D7 are connected to the 8748 bus port. Bits 0 and 1 of port 1 are used to control the SEL and $\overline{OE}$ inputs of the HCTL-20XX respectively. T0 is used to provide a clock signal to the HCTL-20XX. The frequency of T0 is the crystal frequency divided by 3. T0 must be enabled by executing the ENT0 CLK instruction after each system reset, but prior to the first encoder position change. An 8748 program which interfaces to the circuit in Figure 17 is given in Figure 18. The resulting interface timing is shown in Figure 19.



* NOTE: PIN NUMBERS ARE DIFFERENT FOR THE HCTL-2020

Figure 17. An HCTL-20XX-to-Intel 8748 Interface

LOC	Object Code	Source Statements	Comments
000	99 00	ANL P1, 00H	Enable output and higher order bits
002	08	INS A, BUS	Load higher order bits into ACC
003	A8	MOVE R0 A	Move data to register 0
004	89 03	ORL P1, 01H	Change data from high order to low order bits
006	08	INS A, BUS	Load order bits into AC
008	A9	MOV R1, A	Move data to register 1
009	89 03	ORL P1, 03H	Disable outputs
00B	93	RETR	Return

Figure 18. A Typical Program for Reading HCTL-20XX with an 8748

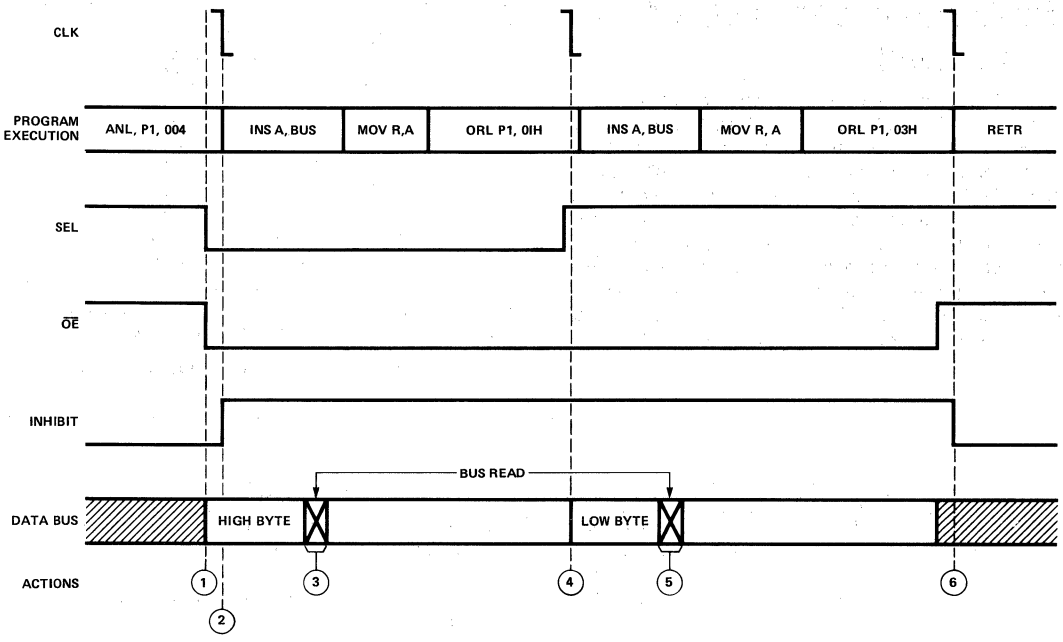


Figure 19. 8748 READ Cycle from Figure 18.

ACTIONS

1. ANL P1, 00H has just been executed. The output of bits 0 and 1 of Port 1 cause SEL and $\overline{OE}$ to be logic low. The data lines output the higher order byte.
2. The HCTL-20XX detects that $\overline{OE}$ and SEL are low on the next falling edge of the CLK and asserts the internal inhibit signal. Data can be read without regard for the phase of the CLK.
3. INS A, BUS has just been executed. Data is read into the 8748.
4. ORL PORT 1, 01H has just been executed. The program sets SEL high and leaves $\overline{OE}$ low by writing the correct values to port 1. The HCTL-20XX detects $\overline{OE}$ is low and SEL is high on the next falling edge of the CLK, and thus the first inhibit reset condition is met.
5. INS A, BUS has just been executed. Lower order data bits are read into the 8748.
6. ORL P1, 03H has just been executed. The HCTL-20XX detects $\overline{OE}$ high on the next falling edge of CLK. The program sets $\overline{OE}$ and SEL high by writing the correct values to port 1. This causes the data lines to be tri-stated. This satisfies the second inhibit and reset condition. On the next rising CLK edge new data is transferred from the counter to the position data latch.

HEWLETT PACKARD

General Purpose Motion Control IC

Technical Data

HCTL-1100 Series

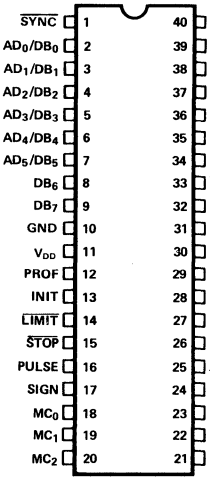
Features

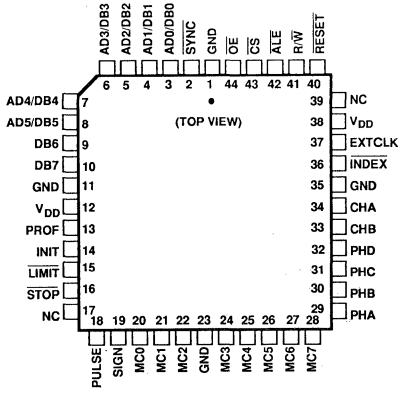
- **Low Power CMOS**
- **PDIP and PLCC Versions Available**
- **Enhanced Version of the HCTL-1000**
- **DC, DC Brushless, and Step Motor Control**
- **Position and Velocity Control**
- **Programmable Digital Filter and Commutator**
- **8-Bit Parallel, and PWM Motor Command Ports**
- **TTL Compatible**
- **SYNC Pin for Coordinating Multiple HCTL-1100 ICs**
- **100 kHz to 2 MHz Operation**
- **Encoder Input Port**

Description

The HCTL-1100 series is a high performance, general purpose motion control IC, fabricated in HP CMOS technology. It frees the host processor for other tasks by performing all the time-intensive functions of digital motion control. The programmability of all control parameters provides maximum flexibility and quick design of control systems with a minimum number of components. In addition to the HCTL-1100, the complete control system consists of a host processor to specify commands, an amplifier, and a motor with an incremental encoder (such as the HP HEDS-5XXX, -6XXX, -9XXX series). No analog compensation or velocity feedback is necessary.

Pinouts





ESD WARNING; NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

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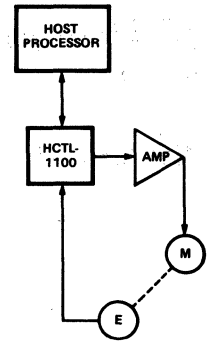
Applications

Typical applications for the HCTL-1100 include printers, medical instruments, material handling machines, and industrial automation.



System Block Diagram

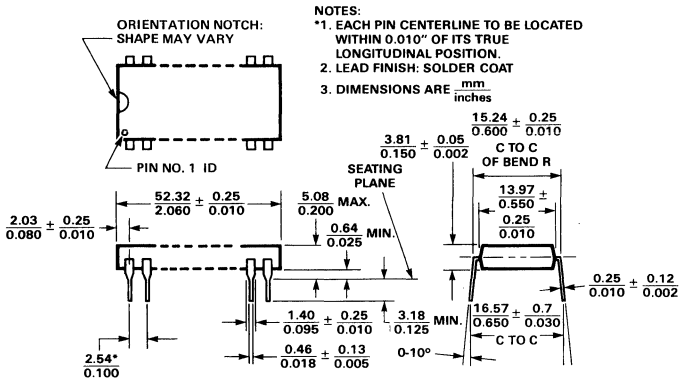
HCTL-1100 vs. HCTL-1000

The HCTL-1100 is designed to replace the HCTL-1000. Some differences exist, and some enhancements have been added.

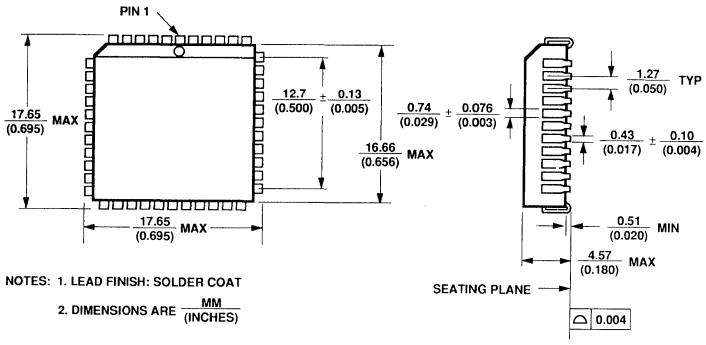
Comparison of HCTL-1100 and HCTL-1000

Description	HCTL-1100	HCTL-1000
Max. Supply Current	30 mA	180 mA
Max. Power Dissipation	165 mW	950 mW
Max. Tri-State Output Leakage Current	150 nA	10 µA
Operating Frequency	100 kHz-2 MHz	1 MHz-2 MHz
Operating Temperature Range	-20°C to +85°C	0°C to 70°C
Storage Temperature Range	-55°C to +125°C	-40°C to +125°C
Synchronize 2 or More ICs	Yes	–
Preset Actual Position Registers	Yes	–
Read Flag Register	Yes	–
Limit and Stop Pins	Must be pulled up to V_{DD} if not used.	Can be left floating if not used.
Hard Reset	Required	Recommended
PLCC Package Available	Yes	–

Package Dimensions



40-PIN PLASTIC DUAL INLINE PACKAGE



44 PIN PLASTIC LEADED CHIP CARRIER PACKAGE

Theory of Operation

The HCTL-1100 is a general purpose motor controller which provides position and velocity control for DC, DC brushless and stepper motors. The internal block diagram of the HCTL-1100 is shown in Figure 1. The HCTL-1100 receives its input commands from a host processor and position feedback from an incremental encoder with quadrature output. An 8-bit bi-directional multiplexed address/data bus interfaces the HCTL-1100 to the host processor. The encoder feedback is decoded into quadrature counts and a 24-bit counter keeps track of position. The HCTL-1100 executes any one of four control algorithms selected by the user. The four control modes are:

- Position Control
- Proportional Velocity Control
- Trapezoidal Profile Control for point to point moves
- Integral Velocity Control with continuous velocity profiling using linear acceleration

The resident Position Profile Generator calculates the necessary profiles for Trapezoidal Profile Control and Integral Velocity Control. The HCTL-1100 compares the desired position (or velocity) to the actual position (or velocity) to compute compensated motor commands using a programmable digital filter D(z). The motor command is externally available at the Motor Command port as an 8-bit byte and at the PWM port as a Pulse Width Modulated (PWM) signal.

The HCTL-1100 has the capability of providing electronic commutation for DC brushless and stepper motors. Using the encoder position information, the motor phases are enabled in the correct sequence. The commutator is fully programmable to encompass most motor/encoder combinations. In addition, phase overlap and phase advance can be programmed to improve torque ripple and high speed performance. The HCTL-1100 contains a number of flags including two externally available flags, Profile and Initialization, which allow the user to see or check the status of the controller. It also has two emergency inputs, $\overline{\text{Limit}}$ and $\overline{\text{Stop}}$, which allow operation of the HCTL-1100 to be interrupted under emergency conditions.

The HCTL-1100 controller is a digitally sampled data system. While information from the host processor is accepted asynchronously with respect to the control functions, the motor command is computed on a discrete sample time basis. The sample timer is programmable.

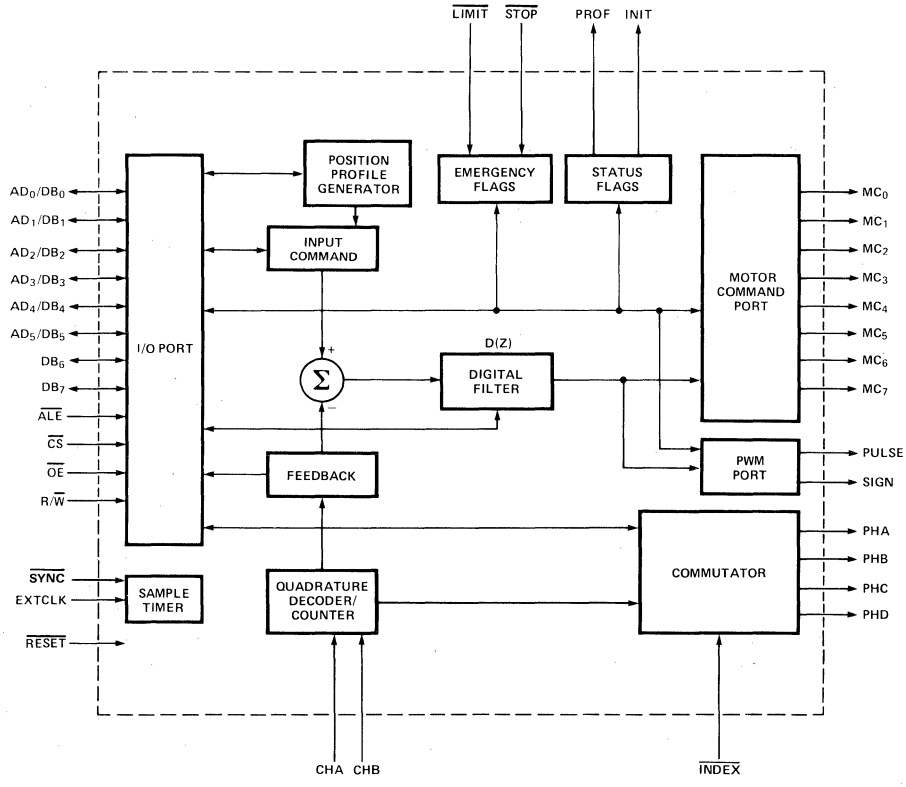


Figure 1. Internal Block Diagram.

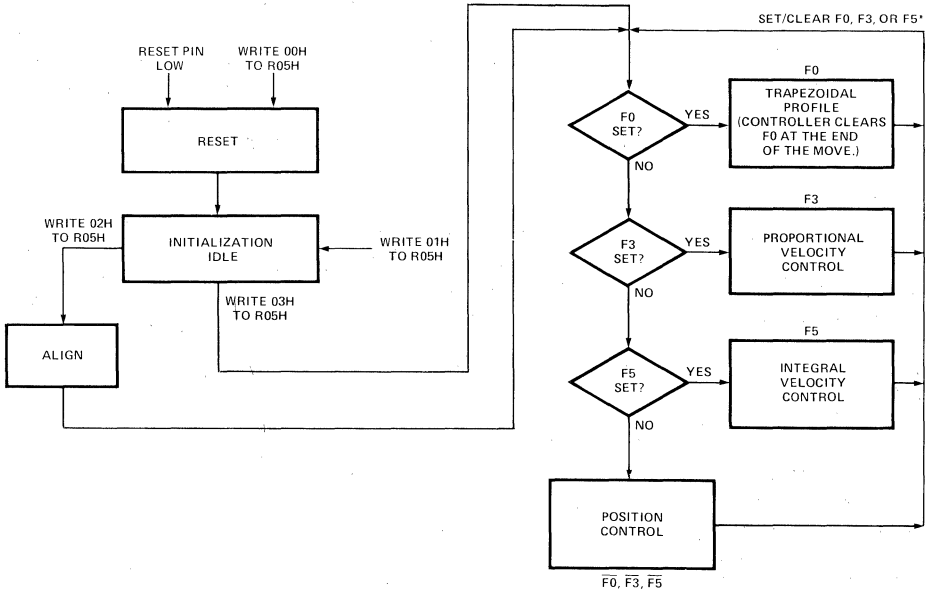


Figure 2. Operating Mode Flowchart

Electrical Specifications

Absolute Maximum Ratings

Operating Temperature, T_A ..... -20°C to 85°C
Storage Temperature, T_S ..... -55°C to 125°C
Supply Voltage, V_{DD} ..... -0.3 V to 7 V
Input Voltage, V_{IN} ..... -0.3 V to V_{DD} +0.3 V
Maximum Operating Clock Frequency, f_{CLK} ..... 2 MHz

DC Electrical Characteristics

V_{DD} = 5 V ± 5%; T_A = -20°C to +85°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Voltage	V_{DD}	4.75	5.00	5.25	V	
Supply Current	I_{DD}		15	30	mA	
Input Leakage Current	I_{IN}		10	100	nA	V_{IN} = 0.00 and 5.25 V
Input Pull-Up Current SYNC PIN	I_{PU}		-40	-100	µA	V_{IN} = 0.00 V
Tristate Output Leakage Current	I_{OZ}		10	150	nA	V_{OUT} = -0.3 to 5.25 V
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{DD}	V	
Output Low Voltage	V_{OL}	-0.3		0.4	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4		V_{DD}	V	I_{OH} = -200 µA
Power Dissipation	P_D		75	165	mW	
Input Capacitance	C_{IN}			20	pF	
Output Capacitance	C_{OUT}		100		pF	

AC Electrical Characteristics

V_{DD} = 5 V ± 5%; T_A = -20°C to +85°C; Units = nsec

ID #	Signal	Symbol	Clock Frequency				Formula*	
			2 MHz		1 MHz			
			Min.	Max.	Min.	Max.	Min.	Max.
1	Clock Period (clk)	t_{CPER}	500		1000			
2	Pulse Width, Clock High	t_{CPWH}	230		300			
3	Pulse Width, Clock Low	t_{CPWL}	200		200		200	
4	Clock Rise and Fall Time	t_{CR}		50		50		50
5	Input Pulse Width $\overline{\text{Reset}}$	t_{IRST}	2500		5000		5 clk	
6	Input Pulse Width $\overline{\text{Stop}}$, $\overline{\text{Limit}}$	t_{IP}	600		1100		1 clk + 100 ns	
7	Input Pulse Width $\overline{\text{Index}}$, Index	t_{IX}	1600		3100		3 clk + 100 ns	
8	Input Pulse Width CHA, CHB	t_{IAB}	1600		3100		3 clk + 100 ns	
9	Delay CHA to CHB Transition	t_{AB}	600		1100		1 clk + 100 ns	
10	Input Rise/Fall Time CHA, CHB, Index	t_{IABR}		450		900		900 (clk < 1 MHz)
11	Input Rise/Fall Time $\overline{\text{Reset}}$, $\overline{\text{ALE}}$, $\overline{\text{CS}}$, $\overline{\text{OE}}$, $\overline{\text{Stop}}$, $\overline{\text{Limit}}$	t_{IR}		50		50		50
12	Input Pulse Width $\overline{\text{ALE}}$, $\overline{\text{CS}}$	t_{IPW}	80		80		80	
13	Delay Time, $\overline{\text{ALE}}$ Fall to $\overline{\text{CS}}$ Fall	t_{AC}	50		50		50	
14	Delay Time, $\overline{\text{ALE}}$ Rise to $\overline{\text{CS}}$ Rise	t_{CA}	50		50		50	
15	Address Setup Time Before $\overline{\text{ALE}}$ Rise	t_{ASR1}	20		20		20	
16	Address Setup Time Before $\overline{\text{CS}}$ Fall	t_{ASR}	20		20		20	
17	Write Data Setup Time Before $\overline{\text{CS}}$ Rise	t_{DSR}	20		20		20	
18	Address/Data Hold Time	t_H	20		20		20	
19	Setup Time, R/$\overline{\text{W}}$ Before $\overline{\text{CS}}$ Rise	t_{WCS}	20		20		20	
20	Hold Time, R/$\overline{\text{W}}$ After $\overline{\text{CS}}$ Rise	t_{WH}	20		20		20	
21	Delay Time, Write Cycle, $\overline{\text{CS}}$ Rise to $\overline{\text{ALE}}$ Fall	t_{CSAL}	1700		3400		3.4 clk	
22	Delay Time, Read/Write, $\overline{\text{CS}}$ Rise to $\overline{\text{CS}}$ Fall	t_{CSCS}	1500		3000		3 clk	
23	Write Cycle, $\overline{\text{ALE}}$ Fall to $\overline{\text{ALE}}$ Fall For Next Write	t_{WC}	1830		3530		3.7 clk	

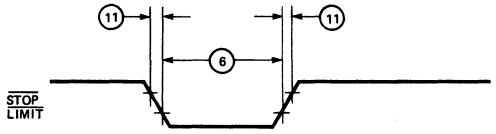
AC Electrical Characteristics, continued

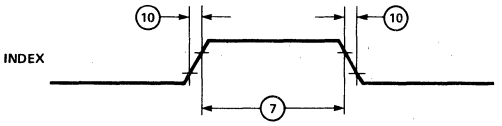
ID #	Signal	Symbol	Clock Frequency				Formula*	
			2 MHz		1 MHz			
			Min.	Max.	Min.	Max.	Min.	Max.
24	Delay Time, $\overline{CS}$ Rise to $\overline{OE}$ Fall	t_{CSOE}	1700		3200		3 clk + 200 ns	
25	Delay Time, $\overline{OE}$ Fall to Data Bus Valid	t_{OEDB}	100		100		100	
26	Delay Time, $\overline{CS}$ Rise to Data Bus Valid	t_{CSDB}	1800		3300		3 clk + 300 ns	
27	Input Pulse Width $\overline{OE}$	t_{IPWOE}	100		100		100	
28	Hold Time, Data Held After $\overline{OE}$ Rise	t_{DOEH}	20		20		20	
29	Delay Time, Read Cycle, $\overline{CS}$ Rise to $\overline{ALE}$ Fall	t_{CSALR}	1820		3320		3 clk + 320 ns	
30	Read Cycle, $\overline{ALE}$ Fall to $\overline{ALE}$ Fall For Next Read	t_{RC}	1950		3450		3 clk + 450 ns	
31	Output Pulse Width, PROF, INIT, Pulse, Sign, PHA-PHD, MC Port	t_{OF}	500		1000		1 clk	
32	Output Rise/Fall Time, PROF, INIT, Pulse, Sign, PHA-PHD, MC Port	t_{OR}	20	150	20	150	20	150
33	Delay Time, Clock Rise to Output Rise	t_{EP}	20	300	20	300	20	300
34	Delay Time, $\overline{CS}$ Rising to MC Port Valid	t_{CSMC}		1600		3200		3.2 clk
35	Hold Time, $\overline{ALE}$ High After $\overline{CS}$ Rise	t_{ALH}	100		100		100	
36	Pulse Width, $\overline{ALE}$ High	t_{ALPWH}	100		100		100	
37	Pulse Width, $\overline{SYNC}$ Low	t_{SYNC}	9000		18000		18 clk	

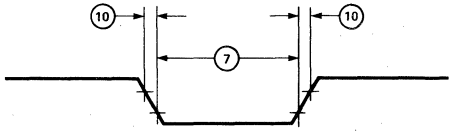
*General formula for determining AC characteristics for other clock frequencies (clk), between 100 kHz and 2 MHz.

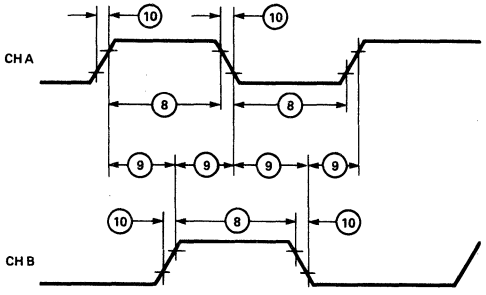
HCTL-1100 I/O Timing Diagrams

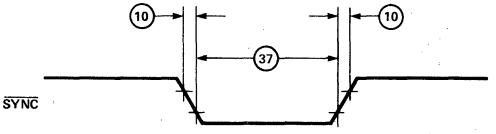
Input logic level values are the TTL Logic levels V_{IL} = 0.8 V and V_{IH} = 2.0 V. Output logic levels are V_{OL} = 0.4 V and V_{OH} = 2.4 V.

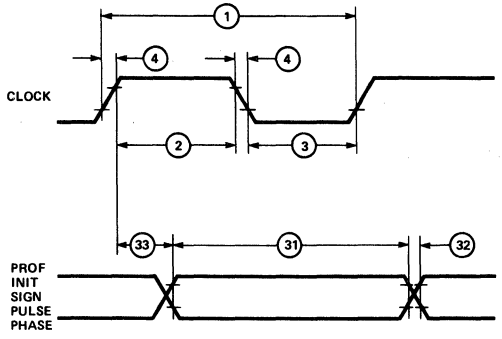


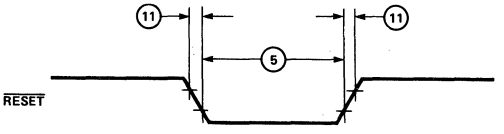










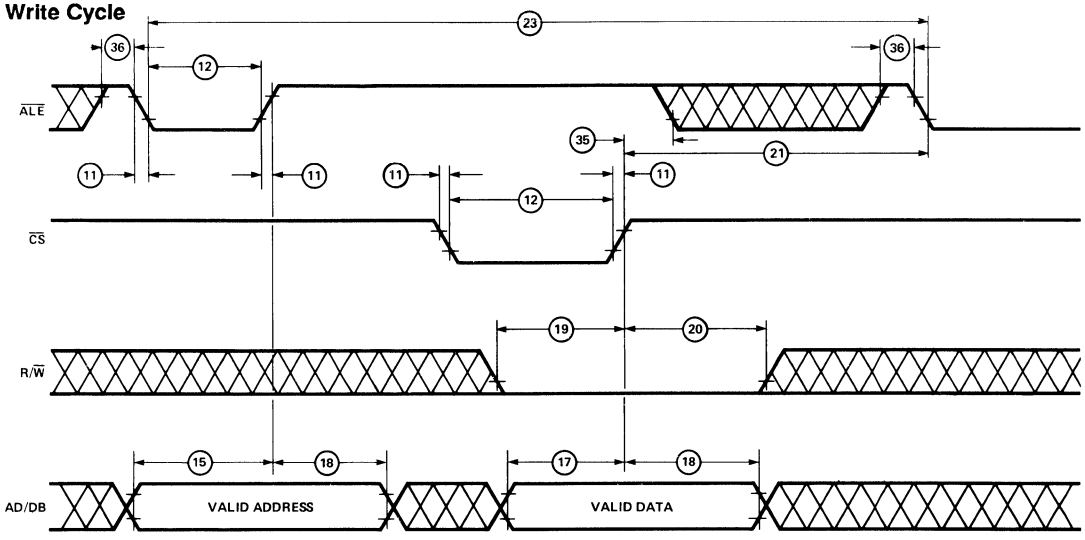


HCTL-1100 I/O Timing Diagrams

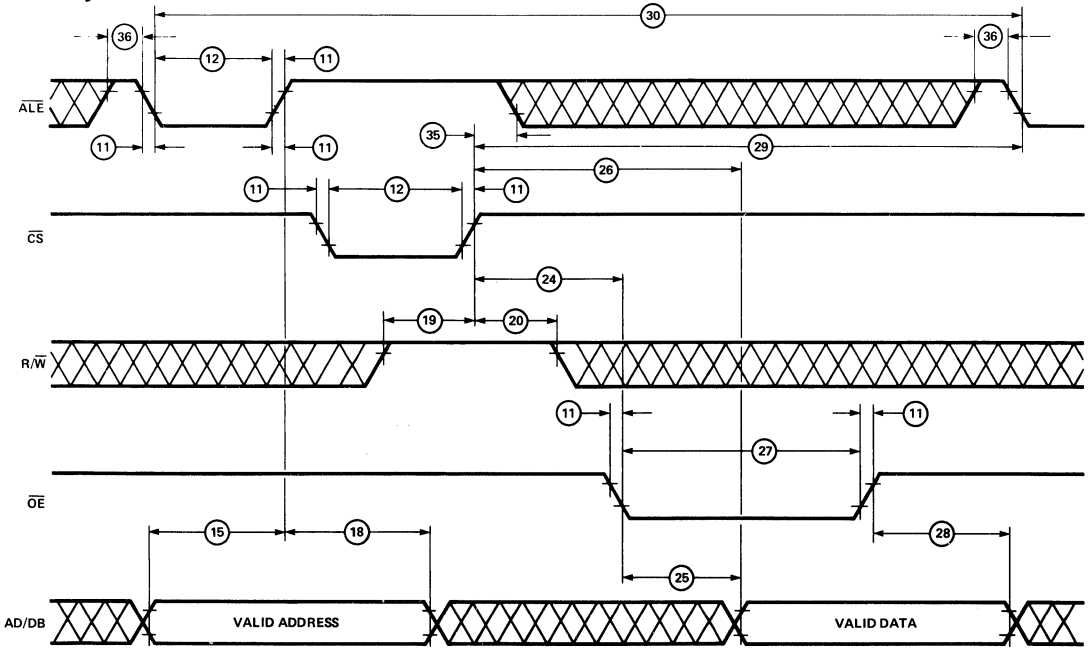
There are three different timing configurations which can be used to give the user flexibility to interface the HCTL-1100 to most microprocessors. See the I/O interface section for more details.

$\overline{ALE}/\overline{CS}$ NON OVERLAPPED

Write Cycle



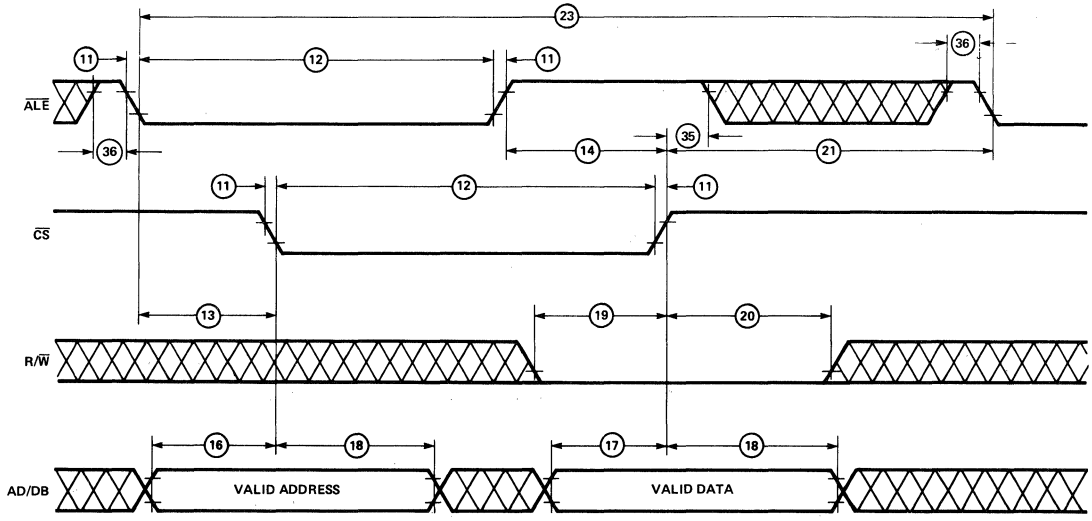
Read Cycle



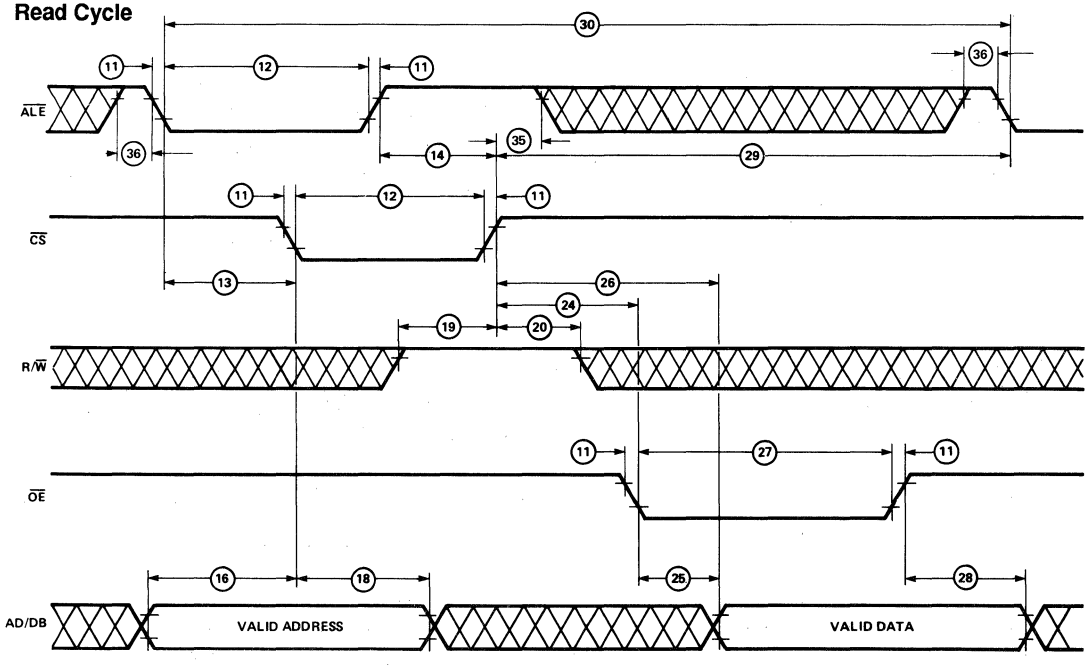
HCTL-1100 I/O Timing Diagrams

$\overline{ALE}/\overline{CS}$ OVERLAPPED

Write Cycle



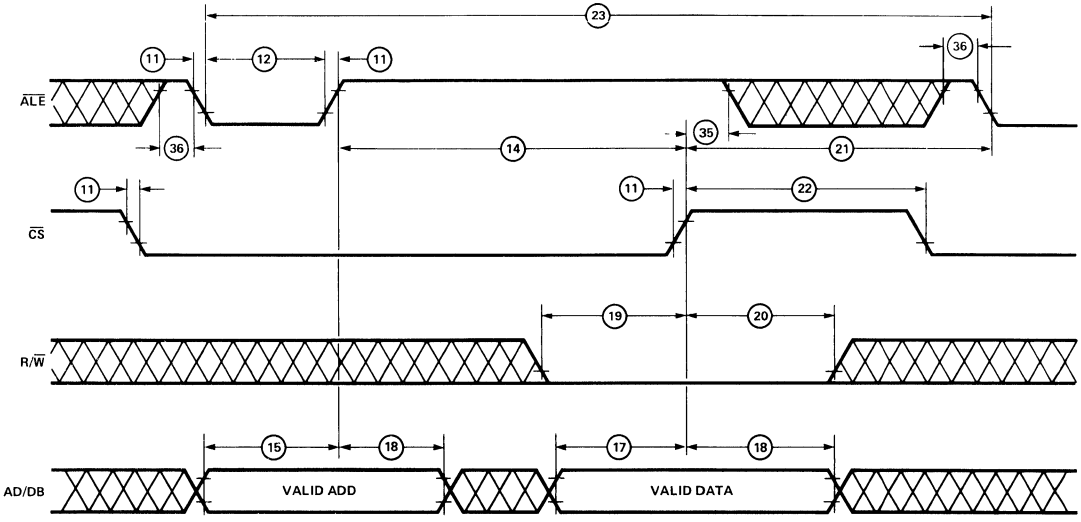
Read Cycle



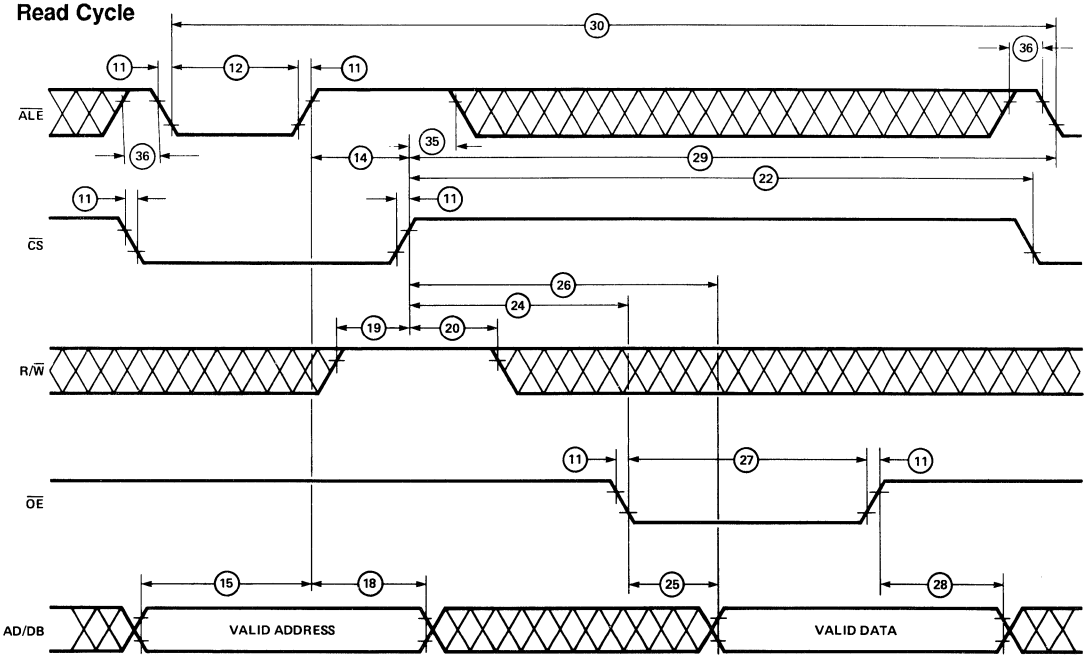
HCTL-1100 I/O Timing Diagrams

$\overline{ALE}$ WITHIN $\overline{CS}$

Write Cycle



Read Cycle



Pin Descriptions and Functions

Input/Output Pins

Symbol	Pin Number		Description
	PDIP	PLCC	
AD0/DB0-AD5/DB5	2-7	3-8	Address/Data Bus – Lower 6 bits of 8-bit I/O port which are multiplexed between address and data.
DB6, DB7	8, 9	9, 10	Data bus – Upper 2 bits of 8-bit I/O port used for data only.

Input Signals

Symbol	Pin Number		Description
	PDIP	PLCC	
CHA/CHB	31, 30	34, 33	Channel A, B – Input pins for position feedback from an incremental shaft encoder. Two channels, A and B, 90 degrees out of phase are required.
$\overline{\text{Index}}$	33	36	Index Pulse – Input from the reference or index pulse of an incremental encoder. Used only in conjunction with the Commutator. Either a low or high true signal can be used with the Index pin. See Timing Diagrams and Encoder Interface section for more detail.
R/$\overline{\text{W}}$	37	41	Read/Write – Determines direction of data exchange for the I/O port.
$\overline{\text{ALE}}$	38	42	Address Latch Enable – Enables lower 6 bits of external data bus into internal address latch.
$\overline{\text{CS}}$	39	43	Chip Select – Performs I/O operation dependent on status of R/$\overline{\text{W}}$ line. For a Write, the external bus data is written into the internal addressed location. For Read, data is read from an internal location into an internal output latch.
$\overline{\text{OE}}$	40	44	Output Enable – Enables the data in the internal output latch onto the external data bus to complete a Read operation.
$\overline{\text{Limit}}$	14	15	Limit Switch – An internal flag which when externally set, triggers an unconditional branch to the Initialization/Idle mode before the next control sample is executed. Motor Command is set to zero. Status of the Limit flag is monitored in the Status register.
$\overline{\text{Stop}}$	15	16	Stop Flag – An internal flag that is externally set. When flag is set during Integral Velocity Control mode, the Motor Command is decelerated to a stop.
$\overline{\text{Reset}}$	36	40	Reset – A hard reset of internal circuitry and a branch to Reset mode.
ExtClk	34	37	External Clock
V_{DD}	11, 35	12, 38	Voltage Supply – Both V_{DD} pins must be connected to a 5.0 volt supply.
GND	10, 32	1, 11, 23, 35	Circuit Ground
$\overline{\text{SYNC}}$	1	2	Used to synchronize multiple HCTL-1100 sample timers.
NC	–	17, 39	Not connected. These pins should be left floating.

Output Pins

Symbol	Pin Number		Description
	PDIP	PLCC	
MC0-MC7	18-25	20-22, 24-28	Motor Command Port – 8-bit output port which contains the digital motor command adjusted for easy bipolar DAC interfacing. MC7 is the most significant bit (MSB).
Pulse	16	18	Pulse – Pulse width modulated signal whose duty cycle is proportional to the Motor Command magnitude. The frequency of the signal is External Clock/100 and pulse width is resolved into 100 external clocks.
Sign	17	19	Sign – Gives the sign/direction of the pulse signal.
PHA-PHD	26-29	29-32	Phase A, B, C, D – Phase Enable outputs of the Commutator.
Prof	12	13	Profile Flag – Status flag which indicates that the controller is executing a profiled position move in the Trapezoidal Profile Control mode.
Init	13	14	Initialization/Idle Flag – Status flag which indicates that the controller is in the Initialization/Idle mode.

Pin Functionality

$\overline{\text{SYNC}}$ Pin

The $\overline{\text{SYNC}}$ pin is used to synchronize two or more ICs. It is only valid in the INIT/IDLE mode (see Operating the HCTL-1100). When this pin is pulled low, the internal sample timer is cleared and held to zero. When the level on the pin is returned to high, the internal sample timer instantly starts counting down from the programmed value.

Connecting all $\overline{\text{SYNC}}$ pins together in the system and pulsing the $\overline{\text{SYNC}}$ signal from the host processor will synchronize all controllers.

$\overline{\text{Limit}}$ Pin

This emergency-flag input is used to disable the control modes of the HCTL-1100. A low level on this input pin causes the internal Limit flag to be set. If this pin is NOT used, it must be pulled up to V_{DD}. If it is not connected, the pin could float low, and possibly trigger a false emergency condition.

The Limit flag, when set in any control mode, causes the HCTL-1100 to go into the Initialization/Idle mode, clearing the Motor Command and causing an immediate motor shutdown. When the Limit flag is set, none of the three control mode flags (F0, F3, or F5) are cleared as the HCTL-1100 enters the Initialization/Idle mode. The user should be aware that these flags are still set before commanding the HCTL-1100 to re-enter one of the four control modes from Initialization/Idle mode.

In general, the user should clear all control mode flags after the $\overline{\text{limit}}$ pin has been pulled low, then proceed.

$\overline{\text{Stop}}$ Pin

The Stop flag affects the HCTL-1100 only in the Integral Velocity Mode.

When a low level is present on this emergency-flag input, the internal stop flag is set. If this pin is NOT used, it must be pulled up to V_{DD}. If it is not connected, the pin could float low, and possibly trigger a false emergency condition.

When the STOP flag is set, the system will come to a decelerated stop and stay in this mode with a command velocity of zero until the Stop flag is cleared and a new command velocity is specified.

Notes on Limit and Stop Flags

Stop and Limit flags are set by a low level input at their respective pins. The flags can only be cleared when the input to the corresponding pin goes high, signifying that the emergency condition has been corrected, AND a write to the Status register (R07H) is executed. That is, after the emergency pin has been set and cleared, the flag also must be cleared by writing to R07H. Any word that is written to R07H after the emergency pin is set and cleared will clear the emergency flag. The lower four bits of that word will also reconfigure the Status register.

Encoder Input Pins (CHA, CHB, $\overline{\text{INDEX}}$)
The HCTL-1100 accepts TTL compatible outputs from 2 and 3 channel incremental encoders such as the HEDS-5XXX, 6XXX, and 9XXX series encoders. Channels A and B are internally decoded into quadrature counts which increment or decrement the 24-bit position counter. For example, a 500-count encoder is decoded into 2000 quadrature counts per revolution. The position counter will be incremented when Channel B leads Channel A. The Index channel is used only for the Commutator and its function is to serve as a reference point for the internal Ring Counter.

The HCTL-1100 employs an internal 3-bit state delay filter to remove any noise spikes from the encoder inputs to the HCTL-1100. This 3-bit state delay filter requires the encoder inputs to remain stable for three consecutive clock rising edges for an encoder pulse to be considered valid by the HCTL-1100's actual position counter (i.e., an encoder pulse must remain at a logic level high or low for three consecutive clock rising edges for the HCTL-1100's actual position counter to be incremented or decremented.) The designer should therefore generally avoid creating the encoder pulses of less than 3 clock cycles.

The index signal of an encoder is used in conjunction with the Commutator. It resets the internal ring counter which keeps track of the rotor position so that no cumulative errors are generated.

The $\overline{\text{Index}}$ pin of the HCTL-1100 also has a 3-bit filter on its input. The $\overline{\text{Index}}$ pin is *active low and level transition sensitive*. It detects a valid high-to-low transition and qualifies the low input level through the 3-bit filter. At this point, the Index signal is internally detected by the commutator logic. This type of configuraiton allows an Index or $\overline{\text{Index}}$ signal to be used to generate the reference mark for commutator operation as long as the AC specifications for the Index signal are met.

Motor Command Port (MC0-MC7)
The 8-bit Motor Command port consists of register R08H whose data goes directly to external pins MC0-MC7. MC7 is the most significant bit. R08H can be read and written to, however, it should be written to only during the Initialization/Idle mode. During any of the four Control modes, the controller writes the motor command into R08H.

This topic is further discussed in the "Register Section" under "Motor Command Register R08H".

Pulse Width Modulation (PWM) Output Port (Pulse, Sign)
The PWM port consists of the Pulse and Sign pins. The PWM port outputs the motor command as a pulse width modulated signal with the correct polarity. This topic is further discussed in the "Register Section" under "PWM Motor Command Register R09H".

Trapezoid Profile Pin (Prof)
The Trapezoid Profile Pin is internally connected to software flag bit 4 in the Status Register. This flag is also represented by bit 0 in the Flag Register (R00H). See the "Register Section" for more information. Both the Pin and the Flag indicate the status of a trapezoid profile move. When the HCTL-1100 begins a trapezoid move, this flag is set by the controller (a high level appears on the pin), indicating the move is in progress. When the HCTL-1100 finishes the move, this flag is cleared by the controller.

Note that the instant the flag is cleared may not be the same instant the motor stops. The flag indicates the completion of the command profile, not the actual profile. If the motor is stalled during the move, or cannot physically keep up with the move, the flag will be cleared before the move is finished.

INIT/IDLE Pin (INIT)
This pin indicates that the HCTL-1100 is in the INIT/IDLE mode, waiting to begin control. This pin is internally connected to the software flag bit 5 in the Status Register R07H. This flag is also represented by bit 1 in the Flag Register (R00H) (See the "Register Section" for more information).

Commutator Pins (PHA-PHD)
These pins are connected only when using the commutator of the HCTL-1100 to drive a brushless motor or step motor. The four pins can be programmed to energize each winding on a multiphase motor.

Operation of the HCTL-1100

Registers

The HCTL-1100 operation is controlled by a bank of 64 8-bit registers, 35 of which are user accessible. These registers contain command and configuration information necessary to properly run the controller chip. The 35 user-accessible registers are listed in Tables 1 and 2. The register number is also the address. A functional block diagram of the HCTL-1100 which shows the role of the user-accessible registers is also included in Figure 3. The other 29 registers are used by the internal CPU as scratch registers and should not be accessed by the user.

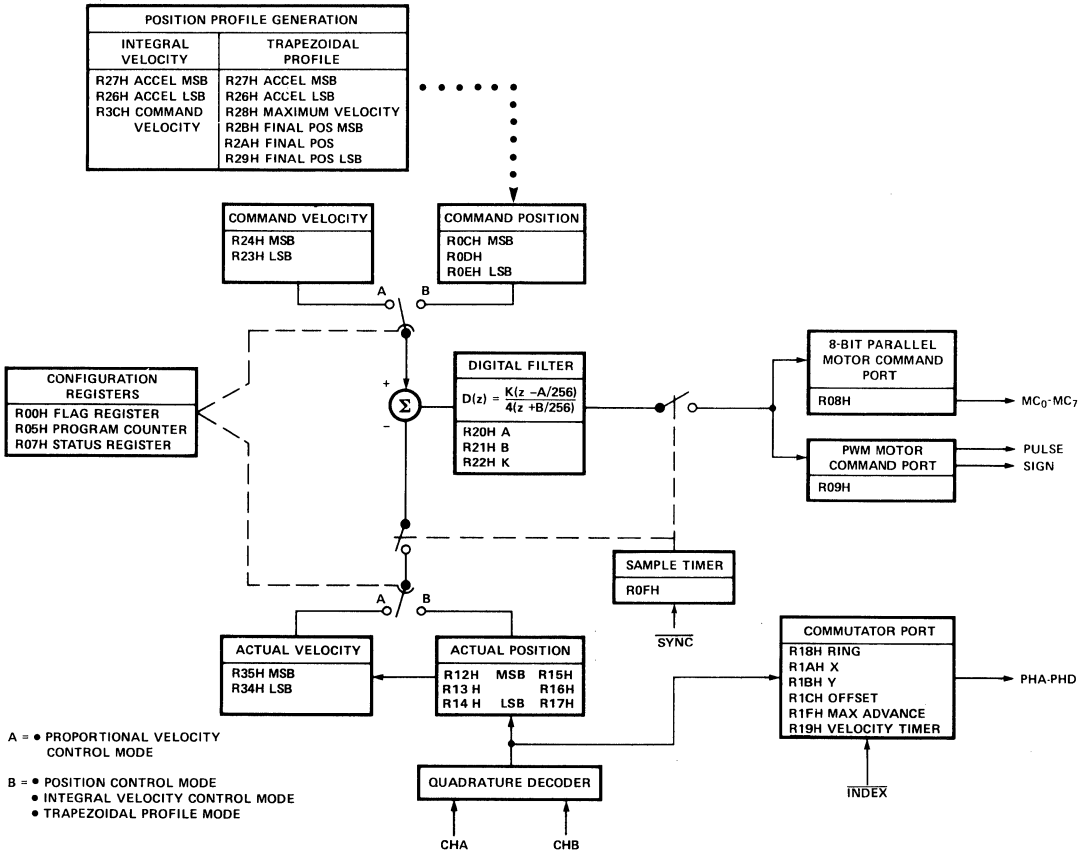


Figure 3. Register Block Diagram

Table 1. Register Reference By Mode

Register		Function	Data Type[1]	User Access
Hex	Dec.			
General Control				
R00H	R00D	Flag Register		r/w
R05H	R05D	Program Counter	scalar	r/w
R07H	R07D	Status Register	-	r/w[2]
R0FH	R15D	Sample Timer	scalar	r/w
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R15H	R21D	Preset Actual Position MSB	2's Complement	w[8]
R16H	R22D	Preset Actual Position	2's Complement	w[8]
R17H	R23D	Preset Actual Position LSB	2's Complement	w[8]
Output Registers				
R07H	R07D	Sign Reversal Inhibit	-	r/w[2]
R08H	R08D	8 bit Motor Command	2's Complement+80H	r/w
R09H	R09D	PWM Motor Command	2's Complement	r/w
Filter Registers				
R20H	R32D	Filter Zero, A	scalar	r/w
R21H	R33D	Filter Pole, B	scalar	r/w
R22H	R34D	Gain, K	scalar	r/w
Commutator Registers				
R07H	R07D	Status Register	-	r/w[2]
R18H	R24D	Commutator Ring	scalar[6,7]	r/w
R19H	R25D	Velocity Timer	scalar	w
R1AH	R26D	X	scalar[6,7]	r/w
R1BH	R27D	Y Phase Overlap	scalar[6,7]	r/w
R1CH	R28D	Offset	2's Complement[7]	r/w
R1FH	R31D	Max. Phase Advance	scalar[6,7]	r/w
Position Control Mode				
R00H	R00D	Flag Register	-	r/w
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R0CH	R12D	Command Position MSB	2's Complement	r/w[3]
R0DH	R13D	Command Position	2's Complement	r/w[3]
R0EH	R14D	Command Position LSB	2's Complement	r/w[3]

Table 1. Continued

Register Hex	Register Dec.	Function	Data Type	User Access
Trapezoid Profile Control Mode				
R00H	R00D	Flag Register	-	r/w
R07H	R07D	Status Register	-	r/w[2]
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R29H	R41D	Final Position LSB	2's Complement	r/w
R2AH	R42D	Final Position	2's Complement	r/w
R2BH	R43D	Final Position MSB	2's Complement	r/w
R26H	R38D	Acceleration LSB	scalar	r/w
R27H	R39D	Acceleration MSB	scalar[6]	r/w
R28H	R40D	Maximum Velocity	scalar[6]	r/w
Integral Velocity Mode				
R00H	R00D	Flag Register	-	r/w
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R26H	R38D	Acceleration LSB	scalar	r/w
R27H	R39D	Acceleration MSB	scalar[6]	r/w
R3CH	R60D	Command Velocity	2's Complement	r/w
Proportional Velocity Mode				
R00H	R00D	Flag Register	-	r/w
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R23H	R35D	Command Velocity LSB	2's Complement	r/w
R24H	R36D	Command Velocity MSB	2's Complement	r/w
R34H	R52D	Actual Velocity LSB	2's Complement	r
R35H	R53D	Actual Velocity MSB	2's Complement	r

Notes:
1. Consult appropriate section for data format and use.
2. Upper 4 bits are read only.
3. Writing to R0EH (LSB) latches all 24 bits.
4. Reading R14H (LSB) latches data in R12H and R13H.
5. Writing to R13H clears Actual Position Counter to zero.
6. The scalar data is limited to positive numbers (00H to 7FH).
7. The commutator registers (R18H, R1CH, R1FH) have further limits which are discussed in the Commutator section of this data sheet.
8. Writing to R17H (R23D) latches all 24 bits (only in INIT/IDLE mode).

Table 2. Register Reference Table by Register Number

Register		Function	Mode Used	Data Type	User Access
Hex	Dec.				
R00H	R00D	Flag Register	All	–	r/w
R05H	R05D	Program Counter	All	scalar	w
R07H	R07D	Status Register	All	–	r/w[2]
R08H	R08D	8 bit Motor Command Port	All	2's complement + 80H	r/w
R09H	R09D	PWM Motor Command Port	All	2's complement	r/w
R0CH	R12D	Command Position (MSB)	All except Proportional Velocity	2's complement	r/w[3]
R0DH	R13D	Command Position	All except Proportional Velocity	2's complement	r/w[3]
R0EH	R14D	Command Position (LSB)	All except Proportional Velocity	2's complement	r/w[3]
R0FH	R15D	Sample Timer	All	scalar	r/w
R12H	R18D	Read Actual Position (MSB)	All	2's complement	r[4]
R13H	R19D	Read Actual Position	All	2's complement	r[4]/w[5]
R14H	R20D	Read Actual Position (LSB)	All	2's complement	r[4]
R15H	R21D	Preset Actual Position (MSB)	INIT/IDLE	2's complement	w[8]
R16H	R22D	Preset Actual Position	INIT/IDLE	2's complement	w[8]
R17H	R23D	Preset Actual Position (LSB)	INIT/IDLE	2's complement	w[8]
R18H	R24D	Commutator Ring	All	scalar[6,7]	r/w
R19H	R25D	Commutator Velocity Timer	All	scalar	w
R1AH	R26D	X	All	scalar[6]	r/w
R1BH	R27D	Y Phase Overlap	All	scalar[6]	r/w
R1CH	R28D	Offset	All	2's complement[7]	r/w
R1FH	R31D	Maximum Phase Advance	All	scalar[6,7]	r/w
R20H	R32D	Filter Zero, A	All except Proportional Velocity	scalar	r/w
R21H	R33D	Filter Pole, B	All except Proportional Velocity	scalar	r/w
R22H	R34D	Gain, K	All	scalar	r/w
R23H	R35D	Command Velocity (LSB)	Proportional Velocity	2's complement	r/w
R24H	R36D	Command Velocity (MSB)	Proportional Velocity	2's complement	r/w
R26H	R38D	Acceleration (LSB)	Integral Velocity and Trapezoidal Profile	scalar	r/w
R27H	R39D	Acceleration (MSB)	Integral Velocity and Trapezoidal Profile	scalar[6]	r/w
R28H	R40D	Maximum Velocity	Trapezoidal Profile	scalar[6]	r/w
R29H	R41D	Final Position (LSB)	Trapezoidal Profile	2's complement	r/w
R2AH	R42D	Final Position	Trapezoidal Profile	2's complement	r/w
R2BH	R43D	Final Position (MSB)	Trapezoidal Profile	2's complement	r/w
R34H	R52D	Actual Velocity (LSB)	Proportional Velocity	2's complement	r
R35H	R53D	Actual Velocity (MSB)	Proportional Velocity	2's complement	r
R3CH	R60D	Command Velocity	Integral Velocity	2's complement	r/w

Notes:
1. Consult appropriate section for data format and use.
2. Upper 4 bits are read only.
3. Writing to R0EH (LSB) latches all 24 bits.
4. Reading R14H (LSB) latches data in R12H and R13H.
5. Writing to R13H clears Actual Position Counter to zero.
6. The scalar data is limited to positive numbers (00H to 7FH).
7. The commutator registers (R18H, R1CH, R1FH) have further limits which are discussed in the Commutator section of this data sheet.
8. Writing to R17H (R23D) latches all 24 bits (only in INIT/IDLE mode).

Register Descriptions – General Control, Output, Filter, and Commutator

Flag Register (R00H)

The Flag register contains flags F0 through F5. This register is a read/write register. Each flag is set and cleared by writing an 8-bit data word to R00H. When writing to R00H, the upper four bits are ignored by the HCTL-1100, bits 0,1,2 specify the flag address, and bit 3 specifies whether to set (bit=1) or clear (bit=0) the addressed flag.

Flag Descriptions

F0–Trapezoidal Profile Flag – set by the user to execute Trapezoidal Profile Control. The flag is reset by the controller when the move is completed. The status of F0 can be monitored at the Profile pin and in Status register R07H bit 4.

F1–Initialization/Idle Flag – set/cleared by the HCTL-1100 to indicate execution of the Initialization/Idle mode. The status of F1 can be monitored at the Initialization/Idle pin and in bit 5 of the Status register (R07H). The user should not attempt to set or clear F1.

F2–Unipolar Flag – set/cleared by the user to specify Bipolar (clear) or Unipolar (set) mode for the Motor Command port.

F3–Proportional Velocity Control Flag – set by the user to specify Proportional Velocity control.

F4–Hold Commutator flag – set/cleared by the user or automatically by the Align mode. When set, this flag inhibits the internal commutator counters to allow open loop stepping of a motor by using the commutator. (See "Offset register" description in the "Commutator section.")

F5–Integral Velocity Control – set by the user to specify Integral Velocity Control. Also set and cleared by the HCTL-1100 during execution of the Trapezoidal Profile mode. This is transparent to the user except when the Limit flag is set (see "Emergency Flags" section).

Writing to the Flag Register

When writing to the flag register, only the lower four bits are used. Bit 3 indicates whether to set or clear a certain flag, and bits 0,1,and 2 indicate the desired flag. The following table shows the bit map of the Flag register:

Bit Number	Function
7-4	Don't Care
3	1 = set 0 = clear
2	AD2
1	AD1
0	AD0

The following table outlines the possible writes to the Flag Register:

Flag	SET	CLEAR
F0	08H	00H
F1	-	-
F2	0AH	02H
F3	0BH	03H
F4	0CH	04H
F5	0DH	05H

Reading the Flag Register

Reading register R00H returns the status of the flags in bits 0 to 5. For example, if bit 0 is set (logic 1), then flag F0 is set. If bit 4 is set, then flag F4 is set. If bits 0 and 5 are set, then both flags F0 and F5 are set.

The following table outlines the Flag Register Read:

Bit Number	Flag (1 = set) (0 = clear)
8-6	Don't Care
5	F5
4	F4
3	F3
2	F2
1	F1
0	F0

Notes:

1. A soft reset (writing 00H to R05H) will not reset the flags in the flag register. A hard reset ($\overline{\text{RESET}}$ pin low) is required to reset all the flags. The flags can also be reset by writing the proper word to the Flag register as explained above.
2. While in Trapezoid Profile Mode, Flag F0 will be set, and Flag F5 may be set. F5 is used for internal purposes. Both flags will be cleared at the end of the profile.

Program Counter Register (R05H)

The Program Counter, which is a write-only register, executes the preprogrammed functions of the controller. The program counter is used along with the control flags F0, F3, and F5 in the Flag register (R00H) to change control modes. The user can write any of the following four commands to the Program Counter.

Value written to R05H	Action
00H	Software Reset
01H	Enter Init/Idle Mode
02H	Enter Align Mode (only from INIT/IDLE Mode)
03H	Enter Control Mode (only from INIT/IDLE Mode)

These Commands are discussed in more detail in the "Operating Modes" section.

Status Register (R07H)
The Status register indicates the status of the HCTL-1100. Each bit decodes into one signal. All 8 bits are user readable and are decoded as shown below. Only the lower 4 bits can be written to by the user to configure the HCTL-1100. To set or clear any of the lower 4 bits, the user writes an 8-bit word to R07H. The upper 4 bits are ignored. Each of the lower 4 bits directly sets/clears the corresponding bit of the Status register as shown below. For example, writing XXXX0101 to R07H sets the PWM Sign Reversal Inhibit, sets the Commutator Phase Configuration to "3 Phase", and sets the Commutator Count Configuration to "full".

Motor Command Register (R08H)
The 8-bit Motor Command Port consists of register R08H. The register is connected to external pins MC0-MC7. MC7 is the most significant bit. R08H can be read and written to; however, it should be written to only in the Initialization/Idle mode. During any of the four control modes, the HCTL-1100 writes values to register R08H.

The Motor Command Port operates in two modes, bipolar and unipolar, when under control of internal software. Bipolar mode allows the full range of values in R08H (-128D to +127D). The data written to the Motor Command Port by the control algorithms is the internally computed 2's-complement motor command with an 80H offset added. This allows direct interfacing to a DAC. Connecting the Motor Command Port to a DAC, Bipolar mode allows the full voltage swing (positive and negative).

Unipolar mode functions such that with the same DAC circuit, the motor command output is restricted to positive values (80H to FFH) when in a control mode. Unipolar mode is used with multi-phase motors when the commutator controls the direction of movement. (If needed, the Sign pin could be used to indicate direction). In Unipolar mode, the user can still write a negative value to R08H in INIT/IDLE mode.

Unipolar mode or Bipolar mode is programmed by setting or clearing flag F2 in the Flag Register R00H.

Internally, the HCTL-1100 operates on data of 24, 16 and 8-bit lengths to produce the 8-bit motor command, available externally. Many times the computed motor command will be greater than 8 bits. At this point, the motor command is saturated by the controller. The saturated value output by the controller is not the full scale value 00H (00D), or FFH

Table 3. Status Register

Status Bit	Function
0	PWM Sign Reversal Inhibit 0 = off 1 = on
1	Commutator Phase Configuration 0 = 3 phase 1 = 4 phase
2	Commutator Count Configuration 0 = quadrature 1 = full
3	Should always be set to 0
4	Trapezoidal Profile Flag F0 1 = in Profile Control
5	Initialization/Idle Flag F1 1 = in Initialization/Idle Mode
6	Stop Flag 0 = set (Stop triggered) 1 = cleared (no Stop)
7	Limit Flag 0 = set (Limit triggered) 1 = cleared (no Limit)

(255D). The saturated value is adjusted to 0FH (15D) (negative saturation) and F0H (240D) (positive saturation). Saturation levels for the Motor Command port are in Figure 4.

PWM Motor Command Register (R09H)

The PWM port outputs the motor command as a pulse width modulated signal with the correct sign of polarity. The PWM port consists of the Pulse and Sign pins and R09H.

The PWM signal at the Pulse pin has a frequency of External Clock/100 and the duty cycle is resolved into the 100 clocks. (For example, a 2 MHz clock gives a 20 KHz PWM frequency).

The Sign pin gives the polarity of the command. Low output on Sign pin is positive polarity.

The 2's-complement contents of R09H determine the duty cycle and polarity of the PWM command. For example, D8H (–40D) gives a 40% duty cycle signal at the Pulse pin and forces the Sign pin high. Data outside the 64H (+100D) to 9CH (–100D) linear range gives 100% duty cycle. R09H can be read and written to. However, the user should only write to R09H when the controller is in the Initialization/Idle mode. Figure 5 shows the PWM output versus the internal motor command.

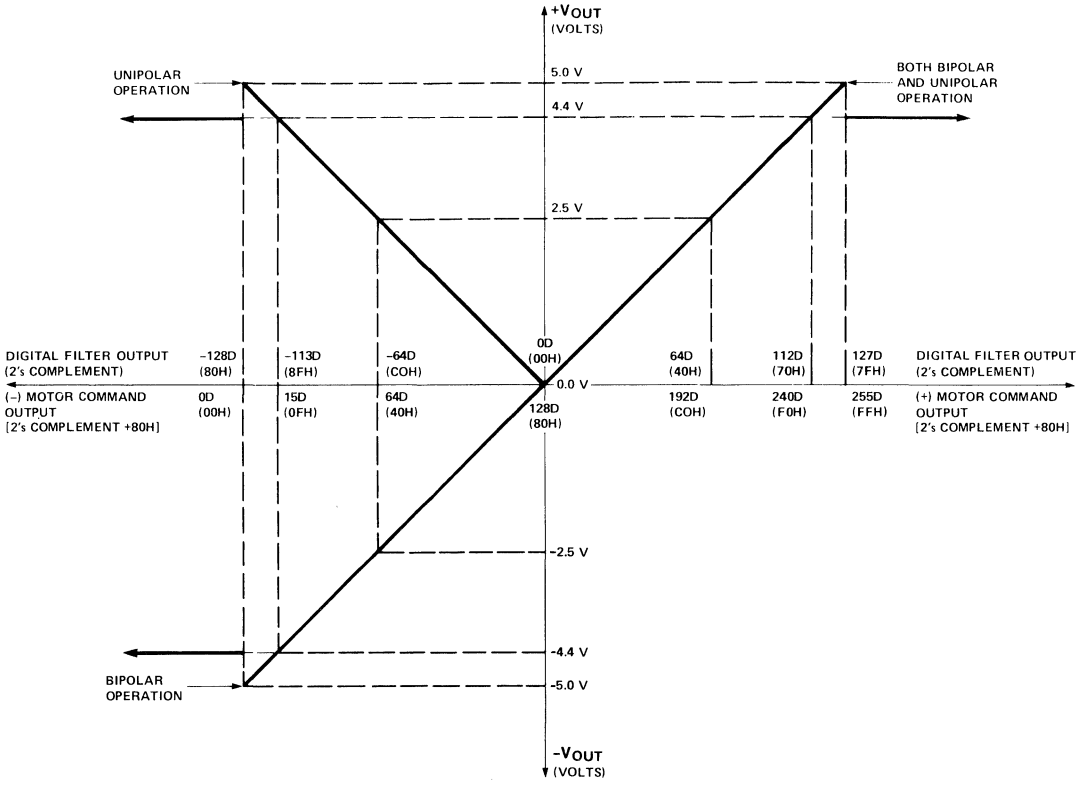


Figure 4. Motor Command Port Output

When any Control mode is being executed, the unadjusted internal 2's-complement motor command is written to R09H. Because of the hardware limit on the linear range (64H to 9CH, ±100D), the PWM port saturates sooner than the 8-bit Motor Command port (00H to FFH, +127D to –128D). When the internal motor command saturates above 8 bits, the PWM port is saturated to the full ±100% duty cycle level. Figure 5 shows the actual values inside the PWM port. Note that the Unipolar flag, F2, does *not* affect the PWM port.

For commutation of brushless motors with the PWM port, only use the Pulse pin from the PWM port as the commutator already contains sign information. (See Figure 9.)

The PWM port has an option that can be used with H-bridge type amplifiers. The option is Sign Reversal Inhibit, which inhibits the Pulse output for one PWM period after a sign polarity reversal. This allows one pair of transistors to turn off before others are turned on and thereby avoids a short across the power supply. Bit 0 in the Status register (R07H) controls the Sign Reversal Inhibit option. Figure 6 shows the output of the PWM port when Bit 0 is set.

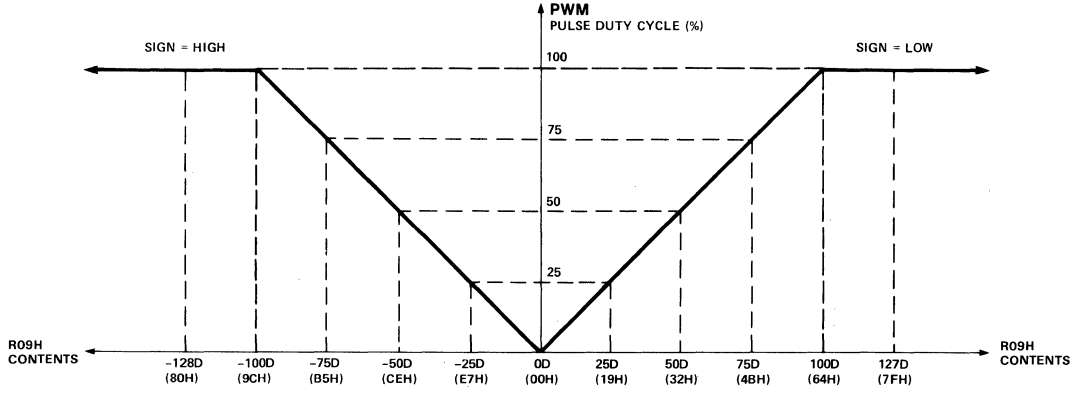


Figure 5. PWM Port Output

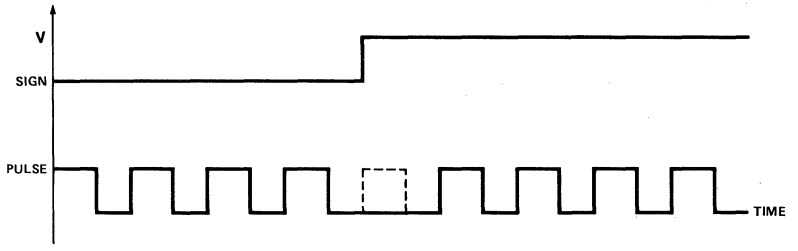


Figure 6. Sign Reversal Inhibit

Actual Position Registers
Read, Clear: R12H,R13H,R14H
Preset : R15H,R16H,R17H

The Actual Position Register is accessed by two sets of registers in the HCTL-1100. When reading the Actual Position from the HCTL-1100, the host processor will read Registers R12H(MSB), R13H, and R14H(LSB). When presetting the Actual Position Register, the processor will write to Registers R15H(MSB), R16H, and R17H(LSB).

When reading the Actual Position registers, the order should be R14H, R13H, R12H. These registers are latched, such that, when reading Register R14H, all three bytes will be latched so that count data does not change while reading three separate bytes.

When presetting the Actual Position Register, write to R15H and R16H first. When R17H is written to, all three bytes are simultaneously loaded into the Actual Position Register.

Note that presetting the Actual Position Registers is only allowed while the HCTL-1100 is in INIT/IDLE mode.

The Actual Position Registers can be simultaneously cleared at any time by writing any value to R13H.

Digital Filter Registers

Zero (A)	R20H
Pole (B)	R21H
Gain (K)	R22H

All control modes use some part of the programmable digital filter D(z) to compensate for closed loop system stability. The compensation D(z) has the form:

$$D(z) = \frac{K\left(z - \frac{A}{256}\right)}{4\left(z + \frac{B}{256}\right)} \qquad [1]$$

where:
z = the digital domain operator
K = digital filter gain (R22H)
A = digital filter zero (R20H)
B = digital filter pole (R21H)

The compensation is a first-order lead filter which in combination with the Sample Timer T (R0FH) affects the dynamic step response and stability of the control system. The Sample Timer, T, determines the rate at which the control algorithm gets executed. All parameters, A, B, K, and T, are 8-bit scalars that can be changed by the user any time.

As shown in equations [2] and [3], the digital filter uses previously sampled data to calculate D(z). This old internally sampled data is cleared when the Initialization/ Idle mode is executed.

In Position Control, Integral Velocity Control, and Trapezoidal Profile Control the digital filter is implemented in the time domain as shown below:

$$MC_n = (K/4)(X_n) - [(A/256)(K/4)(X_{n-1}) + (B/256)(MC_{n-1})] \qquad [2]$$

where:
n = current sample time
n-1 = previous sample time
MC_n = Motor Command Output at n
MC_{n-1} = Motor Command Output at n-1
X_n = (Command Position – Actual Position) at n
X_{n-1} = (Command Position – Actual Position) at n-1

In Proportional Velocity control the digital compensation filter is implemented in the time domain as:

$$MC_n = (K/4)(Y_n) \qquad [3]$$

where:

Y_n = (Command Velocity – Actual Velocity) at n

For more information on system sampling times, bandwidth, and stability, please consult Hewlett-Packard Application Note 1032, *Design of the HCTL-1000's Digital Filter Parameters by the Combination Method.*

Sample Timer Register (R0FH)

The contents of this register set the sampling period of the HCTL-1100. The sampling period is:

$$t = 16(T+1)(1/\text{frequency of the external clock}) \quad [4]$$

where:

T = contents of register R0FH

The Sample Timer has a limit on the minimum allowable sample time depending on the control mode being executed. The limits are given in Table 4 below.

The minimum value limits are to make sure the internal programs have enough time to complete proper execution.

The maximum value of T (R0FH) is FFH (255D). With a 2 MHz clock, the sample time can vary from 64 µsec to 2048 µsec. With a 1 MHz clock, the sample time can vary from 128 µsec to 4096 µsec.

Digital closed-loop systems with slow sampling times have lower stability and a lower bandwidth than similar systems with faster sampling times. To keep the system stability and bandwidth as high as possible the HCTL-1100 should typically be programmed with the fastest sampling time possible. This rule of thumb must be balanced by the needs of the velocity range to be controlled. Velocities are specified to the HCTL-1100 in terms of quadrature encoder counts per sample time. The faster the sampling time, the higher the slowest possible speed.

Hardware Description

The Sample Timer consists of a buffer and a decrement counter. Each time the counter reaches 00H, the Sampler Timer Value T (value written to R0FH) is loaded from the buffer into the counter, which immediately begins to decrement from T.

Writing to the Sample Timer Register

Data written to R0FH will be latched into the internal buffer and used by the counter after it completes the present sample time cycle by decrementing to 00H. The next sample time will use the newly written data.

Reading the Sample Timer Register

Reading R0FH gives the values directly from the decrementing counter. Therefore, the data read from R0FH will have a value anywhere between T and 00H, depending where in the sample time cycle the counter is.

Example –

1. On reset, the value of the timer is pre-set to 40H.
2. Reading R0FH shows 3EH . . . 2BH . . . 08H . . . 3CH . . .

Synchronizing Multiple Axes

Synchronizing multiple axes with HCTL-1100s can be achieved by using the $\overline{\text{SYNC}}$ pin as explained in the Pin Discussion section. Some users may not only want to synchronize several HCTL-1100s but also follow custom profiles for each axis. To do this, the user may need to write a new command position or command velocity during each sample time for the duration of the profile. In this case, data written to the HCTL-1100 has to be coordinated with the Sample Timer. This is so that only one command position or velocity is received during any one sample period, and that it is written at the proper time within a sample period.

At the beginning of each sample period, the HCTL-1100 is performing calculations and executions. New command positions and velocities should not be written to the HCTL-1100 during this time. If they are, the calculations may be thrown off and cause unpredictable control.

The user can read the Sample Timer Register to avoid writing too early during a sample period. Since the Sample Timer Register continuously counts down from its programmed value, the user can check if enough time has passed in the sample period to insure the completion of the internal calculations. The length of time needed by the HCTL-1100 to do

Table 4.

Control Mode	R0FH Contents Minimum Limit
Position Control	07H(07D)
Proportional Velocity Control	07H(07D)
Trapezoidal Profile Control	0FH(15D)
Integral Velocity Control	0FH(15D)

its calculations is given by the Minimum Limits of R0FH (Sample Timer Register) as shown in Table 4. For Position Control Mode, the user should wait for the Sample Timer to count down 07H from its programmed value before writing the next command position or velocity. If the programmed sample timer value is 39H, wait until the Sample Timer Register reads 32H. Writing between 32H and 00H will make the command information available for the next sample period.

Commutator

Status Register	(R07H)
Commutator Ring	(R18H)
X Register	(R1AH)
Y Phase Overlap	(R1BH)
Offset	(R1CH)
Max. Phase Advance	(R1FH)
Velocity Timer	(R19H)

The commutator is a digital state machine that is configured by the user to properly select the phase sequence for electronic commutation of multiphase motors. The Commutator is designed to work with 2, 3, and 4-phase motors of various winding configurations and with various encoder counts. Along with providing the correct phase enable sequence, the Commutator provides programmable phase overlap, phase advance, and phase offset.

Phase overlap is used for better torque ripple control. It can also be used to generate unique state sequences which can be further decoded externally to drive more complex amplifiers and motors.

Phase advance allows the user to compensate for the frequency characteristics of the motor/amplifier combination. By advancing the phase enable command (in position), the delay in reaction of the motor/amplifier combination can be offset and higher performance can be achieved.

Phase offset is used to adjust the alignment of the commutator output with the motor torque curves. By correctly aligning the HCTL-1100's commutator output with the motor's torque curves, maximum motor output torque can be achieved.

The inputs to the Commutator are the three encoder signals, Channel A, Channel B, and Index, and the configuration data stored in registers.

The Commutator uses both channels and the index pulse of an incremental encoder. The index pulse of the encoder must be physically aligned to a known torque curve location because it is used as the reference point of the rotor position with respect to the Commutator phase enables.

The index pulse should be permanently aligned during motor encoder assembly to the last motor phase. This is done by energizing the last phase of the motor during assembly and permanently attaching the encoder codewheel to the motor shaft such that the index pulse is active as shown in Figures 7 and 8. Fine tuning of alignment for commutation purposes is done electronically by the Offset register (R1CH) once the complete control system is set up.

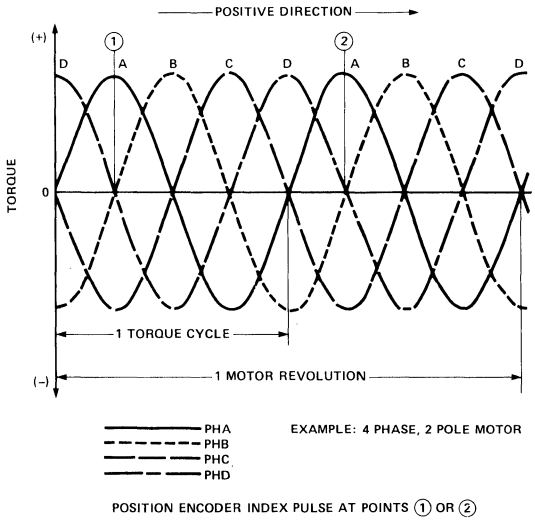


Figure 7. Index Pulse Alignment to Motor Torque Curves.

Each time an index pulse occurs, the internal commutator ring counter is reset to 0. The ring counter keeps track of the current position of the rotor based on the encoder feedback. When the ring counter is reset to 0, the Commutator is reset to its origin (last phase going low, Phase A going high) as shown in Figure 10.

The output of the Commutator is available as PHA, PHB, PHC, and PHD. The HCTL-1100's commutator acts as the electrical equivalent of the mechanical brushes in a motor. Therefore, the outputs of the commutator provide only proper phase sequencing for bidirectional operation. The magnitude information is provided to the motor via the Motor Command and PWM ports. The outputs of the commutator must be combined with the outputs of one of the motor ports to provide proper DC brushless and stepper motor control. Figure 9 shows an example of circuitry which uses the outputs of the commutator with the Pulse output of the PWM port to control a DC brushless or stepper motor. A similar procedure could be used to combine the commutator outputs PHA-PHD with a linear amplifier interface output (Figure 16) to create a linear amplifier system.

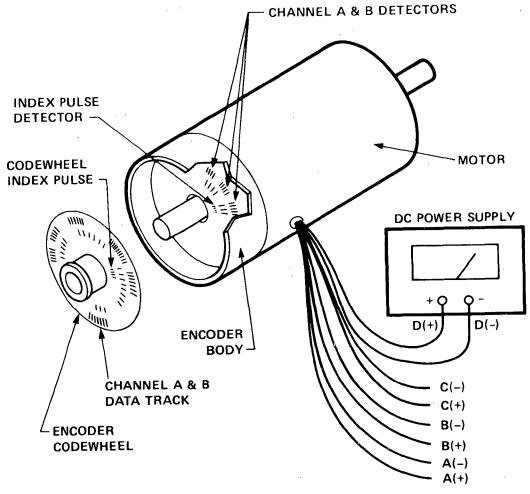


Figure 8. Codewheel Index Pulse Alignment.

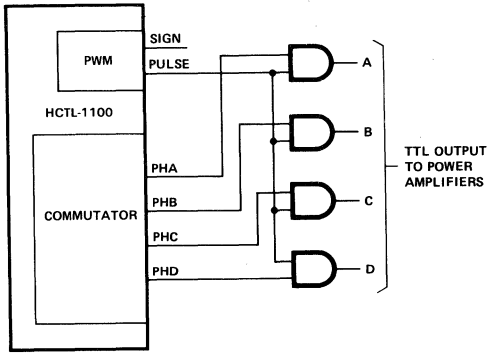


Figure 9. PWM Interface to Brushless DC Motors.

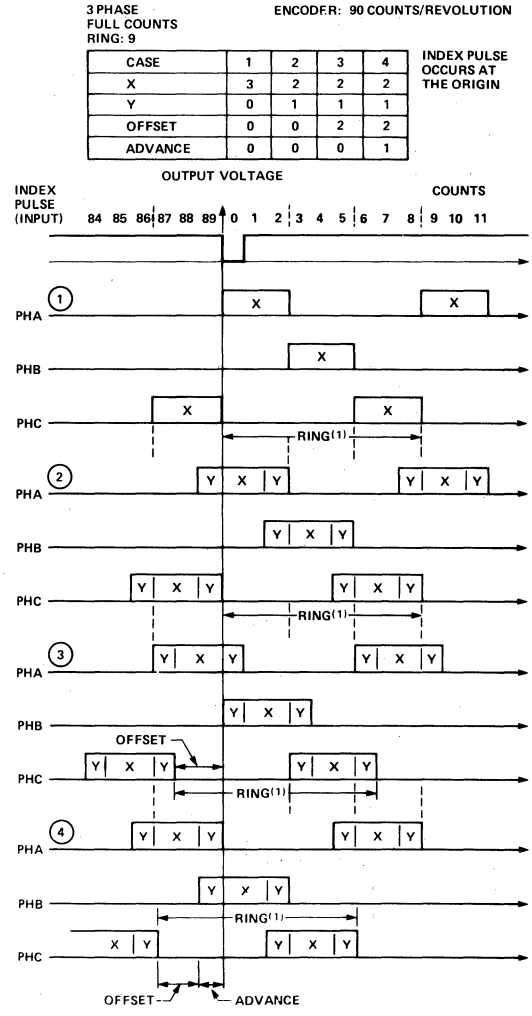


Figure 10. Commutator Configuration.

The Commutator is programmed by the data in the following registers. Figure 10 shows an example of the relationship between all the parameters.

Status Register (R07H)

Bit #1- 0 = 3-phase configuration, PHA, PHB, and PHC are active outputs.
1 = 4-phase configuration, PHA – PHD are active outputs.

Bit #2- 0 = Rotor position measured in quadrature counts (4x decoding).
1 = Rotor position measured in full counts (1 count = 1 codewheel bar and space.)

Bit #2 only affects the commutator's counting method. This includes the Ring register (R18H), the X and Y registers (R1AH & R1BH), the Offset register (R1CH), the Velocity Timer register (R19H), and the Maximum Advance register (R1FH).

Quadrature counts (4x decoding) are always used by the HCTL-1100 as a basis for position, velocity, and acceleration control.

Ring Register (R18H)

The Ring register is defined as 1 electrical cycle of the commutator which corresponds to 1 torque cycle of the motor. The Ring register is scalar and determines the length of the commutation cycle measured in full or quadrature counts as set by bit #2 in the Status register (R07H). The value of the ring must be limited to the range of 0 to 7FH.

X Register (R1AH)

This register contains scalar data which sets the interval during which only one phase is active.

Y Register (R1BH)

This register contains scalar data which set the interval during which two sequential phases are both active. Y is phase overlap. X and Y must be specified such that:

$$X + Y = \text{Ring}/(\#\text{ of phases}) \quad [5]$$

These three parameters define the basic electrical commutation cycle.

Offset Register (R1CH)

The Offset register contains two's-complement data which determines the relative start of the commutation cycle with respect to the index pulse. Since the index pulse must be physically referenced to the rotor, offset performs fine alignment between the electrical and mechanical torque cycles.

The Hold Commutator flag (F4) in the Status register (R07H) is used to decouple the internal commutator counters from the encoder input. Flag (F4) can be used in conjunction with the Offset register to allow the user to advance the commutator phases open loop. This technique may be used to create a custom commutator alignment procedure. For example, in Figure 10, case 1, for a three-phase motor where the ring = 9, X = 3, and Y = 0, the phases can be made to advance open loop by setting the Hold Commutator flag (F4) in the Flag register (R07H). When the values 0, 1, or 2 are written to the Offset register, phase A will be enabled. When the values 3, 4 or 5 are written to the Offset register, phase B will be enabled. And, when the values 6, 7, or 8 are written to the Offset register, phase C will be enabled. No values larger than the value programmed into the Ring register should be programmed into the Offset register.

Phase Advance Registers (R19H, R1FH)

The Velocity Timer register and Maximum Advance register linearly increment the phase advance according to the measured speed for rotation up to a set maximum.

The Velocity Timer register (R19H) contains scalar data which determines the amount of phase advance at a given velocity. The phase advance is interpreted in the units set for the Ring counter by bit #2 in R07H. The velocity is measured in revolutions per second.

$$\text{Advance} = N_f v \Delta t \quad [6]$$

$$\text{where: } \Delta t = \frac{16\,(\text{R19H} + 1)}{\text{f external clk}} \quad [7]$$

N_f = full encoder counts/revolution.
v = velocity (revolutions/second)

The Maximum Advance register (R1FH) contains scalar data which sets the upper limit for phase advance regardless of rotor speed.

Figure 11 shows the relationship between the Phase Advance registers. Note: If the phase advance feature is not used, set both R19H and R1FH to 0.

Commutator Constraints and Use

When choosing a three-channel encoder to use with a DC brushless or stepper motor, the user should keep in mind that the number of quadrature encoder counts (4x the number of slots in the encoder's codewheel) must be an integer multiple (1x, 2x, 3x, 4x, 5x, etc.) of the number of pole pairs in the DC brushless motor or steps in a stepper motor. To take full advantage of the commutator's overlap feature, the number of quadrature counts should be at least 3 times the number of pole pairs in the DC brushless motor or steps in the stepper motor. For example, a 1.8°, (200 step/revolution) stepper motor should employ at least a 150 slot codewheel = 600 quadrature counts/revolution = 3 x 200 steps/revolution).

There are several numerical constraints the user should be aware of to use the Commutator.

The parameters of Ring, X, Y, and Max Advance must be positive numbers (00H to 7FH). Additionally, the following equation must be satisfied:

$$(-128D)\ 80H \le 3/2\ \text{Ring} + \text{Offset} \pm \text{Max Advance} \le 7FH\ (127D) \quad [8]$$

In order to utilize the greatest flexibility of the Commutator, it must be realized that the Commutator works on a circular ring counter principle, whose range is defined by the Ring register (R18H). This means that for a ring of 96 counts and a needed offset of 10 counts, numerically the Offset register can be programmed as 0AH (10D) or AAH (-86D), the latter satisfying Equation 8.

If bit #2 in the Status register is set to allow the commutator to count in full counts, a higher resolution codewheel may be chosen for precise motor control without violating the commutator constraints equation (Equation 8).

Example: Suppose you want to commutate a 3-phase 15 deg/step Variable Reluctance Motor attached to a 192 count encoder.

1. Select 3-phase and quadrature mode for commutator by writing 0 to R07H.
2. With a 3-phase 15 degree/step Variable Reluctance motor the torque cycle repeats every 45 degrees or 8 times/revolution.
3. Ring register
$$= \frac{(4)(192)\ \text{counts/revolution}}{8/\text{revolution}}$$
$$= 96\ \text{quadrature counts}$$
$$= 1\ \text{commutation cycle}$$
4. By measuring the motor torque curve in both directions, it is determined that an offset of 3 mechanical degrees, and a phase overlap of 2 mechanical degrees is needed.
$$\text{Offset} = 3° \frac{(4)\ (192)}{360°}$$
$$\cong 6\ \text{quadrature counts}$$

To create the 3 mechanical degree offset, the Offset

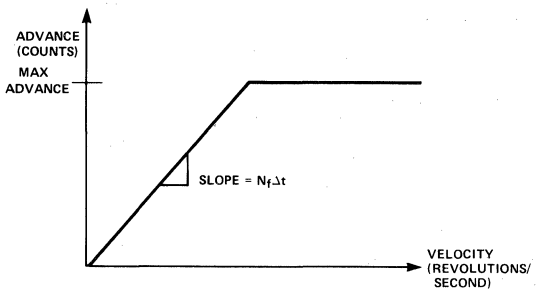


Figure 11. Phase Advance vs. Motor Velocity.

register (R1CH) could be programmed with either A6H (-90D) or 06H (+06D). However, because 06H (+06D) would violate the commutator constraints Equation 8, A6H (-90D) is used.

$$Y = \text{overlap} = \frac{(2°)(4)(192)}{360°} \cong 4$$

$$X + Y = 96/3$$

Therefore, X = 28
Y = 4

For the purposes of this example, the Velocity Timer and Maximum Advance are set to 0.

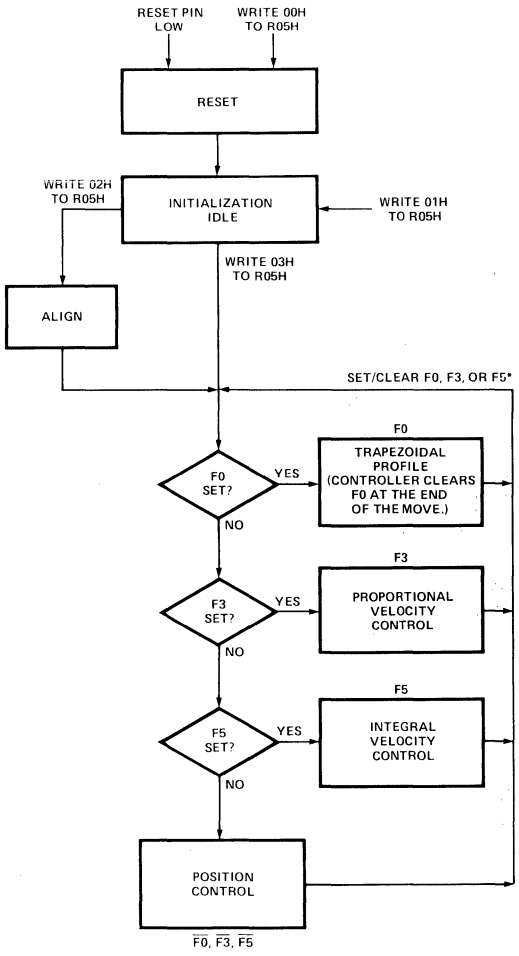
Operation Flowchart

The HCTL-1100 executes any one of three setup routines or four control modes selected by the user. The three setup routines include:
- Reset
- Initialization/Idle
- Align.

The four control modes available to the user include:
- Position Control
- Proportional Velocity Control
- Trapezoidal Profile Control
- Integral Velocity Control

The HCTL-1100 switches from one mode to another as a result of one of the following three mechanisms:
1. The user writes to the Program Counter.
2. The user sets/clears flags F0, F3, or F5 by writing to the Flag register (R00H).
3. The controller switches automatically when certain initial conditions are provided by the user.

This section describes the function of each setup routine and control mode and the initial conditions which must be provided by the user to switch from one mode to another. Figure 12 shows a flowchart of the setup routines and control modes, and shows the commands required to switch from one mode to another.



*Only one flag should be set at a time.

Figure 12. Operation Flowchart.

Setup Modes

Hard Reset

Executed by:
-Pulling the RESET pin low (required at power up)

When a hard reset is executed (RESET pin goes low), the following conditions occur:
- All output signal pins are held low except Sign, Data bus, and Motor Command.
- All flags (F0 to F5) are cleared.
- The Pulse pin of the PWM port is set low while the Reset pin is held low. After the Reset pin is released (goes high) the Pulse pin goes high for one cycle of the external clock driving the HCTL-1100. The Pulse pin then returns to a low output.
- The Motor Command port (R08H) is preset to 80H (128D).
- The Commutator logic is cleared.
- The I/O control logic is cleared.
- A soft reset is automatically executed.

Soft Reset

Executed by:
- Writing 00H to R05H, or
- Automatically called after a hard reset

When a soft reset is executed, the following conditions occur:
- The digital filter parameters are preset to
  A (R20H) = E5H (229D)
  B (R21H) = K (R22H) = 40H (64D)
- The Sample Timer (R0FH) is preset to 40H (64D).
- The Status register (R07H) is cleared.
- The Actual Position Counters (R12H, R13H, R14H) are cleared to 0.

From Reset mode, the HCTL-1100 goes automatically to Initialization/Idle mode.

Initialization/Idle

Executed by:
- Writing 01H to R05H, or
- Automatically executed after a hard reset, soft reset, or
- Limit pin goes low.

The Initialization/Idle mode is entered either automatically from Reset, by writing 01H to the Program Counter (R05H) under any conditions, or pulling the Limit pin low.

In the Initialization/Idle mode, the following occur:
- The Initialization/Idle flag (F1) is set.
- The PWM port R09H is set to 00H (zero command).
- The Motor Command port (R08H) is set to 80H (128D) (zero command).
- Previously sampled data stored in the digital filter is cleared.

It is at this point that the user should pre-program all the necessary registers needed to execute the desired control mode. The HCTL-1100 stays in this mode (idling) until a new mode command is given.

Align

Executed by:
- Writing 02H to R05H

The Align mode is executed only when using the commutator feature of the HCTL-1100. This mode automatically aligns multiphase motors to the HCTL-1100's internal Commutator.

The Align mode can be entered only from the Initialization/Idle mode by writing 02H to the Program Counter register (R05H).

Before attempting to enter the Align mode, the user should clear all control mode flags and set both the Command Position registers (R0CH, R0DH, and R0EH) and the Actual Position registers (R12H, R13H, and R14H) to zero. After the Align mode has been executed, the HCTL-1100 will automatically enter the Position Control mode and go to position zero. By following this procedure, the largest movement in the Align mode will be one torque cycle of the motor.

The Align mode assumes: the encoder index pulse has been physically aligned to the last motor phase during encoder/motor assembly, the Commutator parameters have been correctly preprogrammed (see the section called Commutator for details), and a hard reset has been executed while the motor is stationary.

The Align mode first disables the Commutator and with open loop control enables the first phase (PHA) and then the last phase (PHC or PHD) to orient the motor on the last phase torque detent. Each phase is energized for 2048 system sampling periods (t). For proper operation, the motor must come to a complete stop during the last phase enable. At this point the Commutator is enabled and commutation is closed loop.

The HCTL-1100 then automatically switches from the Align mode to Position Control mode.

Control Modes

Control flags F0, F3, and F5 in the Flag register (R00H) determine which control mode is executed. Only one control flag can be set at a time. After one of

these control flags is set, the control modes are entered either automatically from Align or from the Initialization/Idle mode by writing 03H to the Program Counter (R05H).

Position Control Mode

Flags: F0 Cleared
F3 Cleared
F5 Cleared

Registers Used:

Register		Function
R00H	R00D	Flag Register
R12H	R18D	Read Actual Position MSB
R13H	R19D	Read Actual Position
R14H	R20D	Read Actual Position LSB
R0CH	R12D	Command Position MSB
R0DH	R13D	Command Position
R0EH	R14D	Command Position LSB

Position Control performs point-to-point position moves with no velocity profiling. The user specifies a 24-bit position command, which the controller compares to the 24-bit actual position. The position error is calculated, the full digital lead compensation is applied and the motor command is output.

The controller will remain position-locked at a destination until a new position command is given.

The actual and command position data is 24-bit two's-complement data stored in six 8-bit registers. Position is measured in encoder quadrature counts.

The command position resides in R0CH (MSB), R0DH, R0EH (LSB). Writing to R0EH latches all 24 bits at once for the control algorithm. Therefore, the command position is written in the sequence R0CH, R0DH and R0EH. The command registers can be read in any desired order.

The actual position resides in R12H (MSB), R13H, and R14H (LSB). Reading R14H latches the upper two bytes into an internal buffer. Therefore, Actual Position registers are read in the order of R14H, R13H, and R12H for correct instantaneous position data.

The largest position move possible in Position Control mode is 7FFFFFH (8,388,607D) quadrature encoder counts.

Proportional Velocity Mode

Flags: F0 Cleared
F3 Set
F5 Cleared

Registers Used:

Register		Function
R00H	R00D	Flag Register
R23H	R35D	Command Velocity LSB
R24H	R36D	Command Velocity MSB
R34H	R52D	Actual Velocity LSB
R35H	R53D	Actual Velocity MSB

Proportional Velocity Control performs control of motor speed using only the gain factor, K, for compensation. The dynamic pole and zero lead compensation are not used. (See the "Digital Filter" section of this data sheet.)

```
Example Code to Program Position Moves

   { Begin }
        Hard Reset { HCTL-1100 goes into INIT/IDLE Mode }

        Initialize Filter, Timer, Command Position Registers

        Write 03H to Register R05H
             { HCTL-1100 is now in Position Mode }

        Write Desired Command Position to Command Position Registers
             { Controller Moves to new position }

        Continue writing in new Command Positions
   { end }
```

The command and actual velocity are 16-bit two's-complement words.

The command velocity resides in registers R24H (MSB) and R23H (LSB). These registers are unlatched which means that the command velocity will change to a new velocity as soon as the value in either R23H or R24H is changed. The registers can be read or written to in any order.

R24H	R23H
IIII IIII	IIII FFFF

COMMAND VELOCITY FORMAT

The units of velocity are quadrature counts/sample time. To convert from rpm to quadrature counts/sample time, use the formula shown below:

$$Vq = (Vr)(N)(t)(0.01667/rpm\text{-}sec) \quad [9]$$

Where:
Vq = velocity in quadrature counts/sample time
Vr = velocity in rpm
N = 4 times the number of slots in the codewheel (i.e., quadrature counts).
t = The HCTL-1100 sample time in seconds. (See the section on the HCTL-1100's Sample Timer register).

Because the Command Velocity registers (R24H and R23H) are internally interpreted by the HCTL-1100 as 12 bits of integer and 4 bits of fraction, the host processor must multiply the desired command velocity (in quadrature counts/sample time) by 16 before programming it into the HCTL-1100's Command Velocity registers.

The actual velocity is computed only in this algorithm and stored in scratch registers R35H (MSB) and R34H (LSB). There is no fractional component in the actual velocity registers and they can be read in any order.

The controller tracks the command velocity continuously until new mode command is given. The system behavior after a new velocity command is governed only by the system dynamics until a steady state velocity is reached.

Integral Velocity Mode
Flags: F0 Cleared
F3 Cleared
F5 Set to begin move

Registers Used:

Register		Function
R00H	R00D	Flag Register
R26H	R38D	Acceleration LSB
R27H	R39D	Acceleration MSB
R3CH	R60D	Command Velocity

Integral Velocity Control performs continuous velocity profiling which is specified by a command velocity and command acceleration. Figure 13 shows the capability of this control algorithm.

The user can change velocity and acceleration any time to continuously profile velocity in time. Once the specified velocity is reached, the HCTL-1100 will maintain that velocity until a new command is specified. Changes between actual velocities occur at the presently specified linear acceleration.

The command velocity is an 8-bit two's-complement word

```
Example Code for Programming Proportional Velocity Mode

    { Begin }
        Hard Reset { HCTL-1100 goes into INIT/IDLE Mode }

        Initialize Filter, Timer, Command Position Registers

        Write 03H to Register R05H
            { HCTL-1100 is now in Position Mode }

        Write Desired Command Velocity (if needed)

        Set Flag F3 {Proportional Velocity Move Begins}

        { System ramps to Command Velocity }

        Continue writing new Command Velocities
    {end}
```

stored in R3CH. The units of velocity are quadrature counts/ sample time.

The conversion from rpm tc quadrature counts/sample time is shown in equation 9. The Command Velocity register (R3CH) contains only integer data and has no fractional component.

While the overall range of the velocity command is 8 bits, two's-complement, the difference between any two sequential commands cannot be greater than 7 bits in magnitude (i.e., 127 decimal). For example, when the HCTL-1100 is executing a command velocity of 40H (+64D), the next velocity command must fall in the range of 7FH (+127D), the maximum command range, C1H (-63D), the largest allowed difference.

The command acceleration is a 16-bit scalar word stored in R27H and R26H. The upper byte (R27H) is the integer part and the lower byte (R26H) is the fractional part provided for resolution. The integer part has

R27H	R26H
0IIIIIII	FFFFFFFF/256

Command Acceleration Format

a range of 00H to 7FH. The contents of R26H are internally divided by 256 to produce the fractional resolution.

The units of acceleration are quadrature counts/sample time squared.

To convert from rpm/sec to quadrature counts/[sample time]^2, use the formula shown below:

$$Aq = (Ar)(N)(t^2)(0.01667/rpm\text{-}sec) \quad [10]$$

Where:

Aq = Acceleration in quadrature counts/[sample time]^2

Ar = Acceleration in rpm/sec

N = 4 times the number of slots in the codewheel (i.e., quadrature counts)

t = The HCTL-1100 sample time in seconds. (See the section on the HCTL-1100's Sample Timer register).

Because the Command Acceleration registers (R27H and R26H) are internally interpreted by the HCTL-1100 as 8 bits of integer and 8 bits of fraction, the host processor must multiply the desired command acceleration (in quadrature counts/[sample time]^2) by 256 before programming it into the HCTL-1100's Command Acceleration registers.

Internally, the controller performs velocity profiling through position control.

Each sample time, the internal profile generator uses the information which the user has programmed into the Command Velocity register (R3CH) and the Command Acceleration registers (R27H and R26H) to determine the value which will be automatically loaded into the Command Position registers (R0CH, R0DH, and R0EH). After the new command position has been generated, the difference between the value in the Actual Position registers (R12-R13H, and R14H) and the new value in the Command Position registers is calculated as the new position error. This new position error is used by the full digital compensation filter to compute a new motor command output by this sample time. The register block in Figure 3 further shows how the internal profile generator works in Integral Velocity mode. In control theory terms, integral compensation has been added and therefore, this system has zero steady-state error.

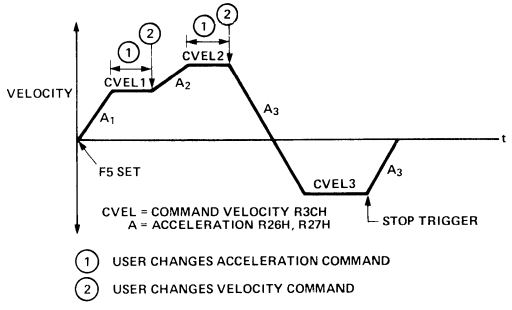


Figure 13. Integral Velocity Modes.

Although Integral Velocity Control mode has the advantage over Proportional Velocity mode of zero steady state velocity error, its disadvantage is that the closed loop stability is more difficult to achieve. In Integral Velocity Control mode the system is actually a position control system and therefore the complete dynamic compensation D(z) is used.

If the external Stop flag F6 is set during this mode signalling an emergency situation, the controller automatically decelerates to zero velocity at the presently specified acceleration factor and stays in this condition until the flag is cleared. The user then can specify new velocity profiling data.

Trapezoid Profile Mode

Flags: F0 Set to begin move
F3 Cleared
F5 Cleared

Registers Used:

Register		Function
R00H	R00D	Flag Register
R07H	R07D	Status Register
R12H	R18D	Read Actual Position MSB
R13H	R19D	Read Actual Position
R14H	R20D	Read Actual Position LSB
R29H	R41D	Final Position LSB
R2AH	R42D	Final Position
R2BH	R43D	Final Position MSB
R26H	R38D	Acceleration LSB
R27H	R39D	Acceleration MSB
R28H	R40D	Maximum Velocity

Trapezoid Profile Control performs point-to-point position moves and profiles the velocity trajectory to a trapezoid or triangle. The user specifies only the desired final position, acceleration and maximum velocity. The controller computes the necessary profile to conform to the command data. If maximum velocity is reached before the distance halfway point, the profile will be trapezoidal, otherwise the profile will be triangular. Figure 14 shows the possible trajectories with Trapezoidal Profile Control.

The command data for Trapezoidal Profile Control mode consists of a final position, a command acceleration, and a

```
Example Code for Programming Integral Velocity Mode

     (Begin)
          Hard Reset {HCTL-1100 goes into INIT/IDLE Mode}

          Initialize Filter, Timer, Command Position Registers

          Write 03H to Register R05H
               {HCTL-1100 is now in Position Mode}

          Write Desired Acceleration (if needed)

          Write Desired Maximum Velocity (if needed)

          Set Flag F5 {Integral Velocity Move Begins}

          {System ramps to Maximum Velocity}

          Continue writing new Accelerations and Velocities
     { end }
```

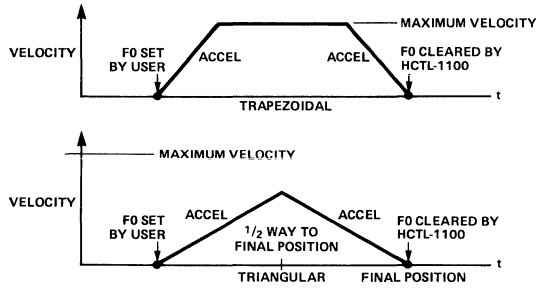


Figure 14. Trapezoidal Profile Mode.

maximum velocity. The 24-bit, two's-complement final position is written to registers R2BH, (MSB), R2AH, and R29H (LSB). The 16-bit command acceleration resides in registers R27H (MSB) and R26H (LSB). The command acceleration has the same integer and fraction format as discussed in the Integral Velocity Control mode section. The 7-bit maximum velocity is a scalar value with the range of 00H to 7FH (0D to 127D). The maximum velocity has the units of quadrature counts per sample time, and resides in register R28H. The command data registers may be read or written to in any order.

The internal profile generator produces a position profile using the present Command Position (R0CH-R0EH) as the starting point and the Final Position (R2BH-R29H) as the end point.

Once the desired data is entered, the user sets flag F0 in the Flag register (R00H) to commence motion (if the HCTL-1100 is already in Position Control mode).

When the profile generator sends the last position command to the Command Position registers to complete the trapezoidal move, the controller clears flag F0. The HCTL-1100 then automatically goes to Position Control mode with the final position of the trapezoidal move as the command position.

When the HCTL-1100 clears flag F0 it does NOT indicate that the motor and encoder are at the final position NOR that the motor and encoder have stopped. The flag indicates that the command profile has finished. The motor and encoder's true position can only be determined by reading the Actual Position registers. The only way to determine if the motor and encoder have stopped is to read the Actual Position registers at successive intervals.

The status of the Profile flag can be monitored both in the Status register (R07) and at the external Profile pin at any time. While the Profile flag is high NO new command data should be sent to the controller.

Each sample time, the internal profile generator uses the information which the user has programmed into the Maximum Velocity register (R28H), the Command Acceleration registers (R27H and R26H), and the Final Position registers (R2BH, R2AH, and R29H) to determine the value which will be automatically loaded into the Command Position registers (R0EH, R0DH, and R0CH). After the new command position has been generated, the difference between the value in the Actual Position registers (R12H, R13H, and R14H) and the new value in the Command Position registers is calculated as the new position error. This new position error is used by the full digital compensation filter to compute a new motor command output for the sample time. (The register block diagram in Figure 3 further shows how the internal profile generator works in Trapezoidal Profile mode.)

Example Code for Programming Trapezoid Moves

```
{ Begin }
     Hard Reset { HCTL-1100 goes into INIT/IDLE Mode }

     Inititalize Filter, Timer, Command Position Registers

     Write 03H to Register R05H
        { HCTL-1100 is now in Position Mode }

     { Profile #1}

     Write Desired Acceleration

     Write Desired Maximum Velocity

     Write Final Position

     Set Flag F0 {Trapezoid Move Begins, PROF pin goes high}

     Poll PROF pin until it goes low (Move is complete)

     { Profile #2}

     Write Desired Acceleration

     Write Desired Maximum Velocity

     Write Final Position

     Set Flag F0 {Trapezoid Move Begins, PROF pin goes high}

     Poll PROF pin until it goes low (Move is complete)

     { Repeat }
     .
     .
     .
     .
{ end }
```

Applications of the HCTL-1100

Interfacing the HCTL-1100 to Host Processors

The HCTL-1100 looks to the host microprocessor like a bank of 8-bit registers to which the host processor can read and write (i.e., the host processor treats the HCTL-1100 like RAM). The data in these registers controls the operation of the HCTL-1100. The host processor communicates to the HCTL-1100 over a bidirectional multiplexed 8-bit data bus. The four I/O control lines. $\overline{ALE}$, $\overline{CS}$, $\overline{OE}$, and R/$\overline{W}$ execute the data transfers (see Figure 15).

There are three different timing configurations which can be used to give the user greater flexibility to interface the

HCTL-1100 to most microprocessors (see Timing diagrams). They are differentiated from one another by the arrangement of the $\overline{ALE}$ signal with respect to the $\overline{CS}$ signal. The three timing configurations are listed below.

1. $\overline{ALE}$, $\overline{CS}$ non-overlapped
2. $\overline{ALE}$, $\overline{CS}$ overlapped
3. $\overline{ALE}$ within $\overline{CS}$

Any I/O operation starts by asserting the $\overline{ALE}$ signal which starts sampling the external bus into an internal address latch. Rising $\overline{ALE}$ or falling $\overline{CS}$ during $\overline{ALE}$ stops the sampling into the address latch.

$\overline{CS}$ low after rising $\overline{ALE}$ samples the external bus into the data latch. Rising $\overline{CS}$ stops the sampling into the data latch, and starts the internal synchronous process.

In the case of a write, the data in the data latch is written into the addressed location. In the case of a read, the addressed location is written into an internal output latch. $\overline{OE}$ low enables the internal output latch onto the external bus. The $\overline{OE}$ signal and the internal output latch allow the I/O port to be flexible and avoid bus conflicts during read operations.

It is important that the host microprocessor does not attempt to perform too many I/O operations in a single sample time of the HCTL-1100. Each I/O operation interrupts the execution of the HCTL-1100's internal code for 1 clock cycle. Although extra clock cycles have been allotted in each sample time for I/O operations, the number of extra cycles is reduced as the value programmed into the Sample Timer register (R0FH) is reduced.

Table 5 shows the maximum number of I/O operations allowed under the given conditions.

The number of external clock cycles available for I/O operations in any of the four control modes can be increased by increasing the value in the Sample Timer register (R0FH).

For every unit increase in the Sample Timer register (R0FH) above the minimums shown in Table 5 the user may perform 16 additional I/O operations per sample time.

Interfacing the HCTL-1100 to Amplifiers and Motors

The Motor Command port is the ideal interface to an 8-bit DAC, configured for bipolar output. The data written to the 8-bit Motor Command port by the control algorithms is the internally computed 2's-complement motor command with an 80H offset added. This allows direct interfacing to a DAC. Figure 16 shows a typical DAC interface to the HCTL-1100. An inexpensive DAC, such as MC1408 or equivalent, has its digital inputs directly connected to the Motor Command port. The DAC produces an output current which is converted to a voltage by an operational amplifier. R_O and R_G control the analog offset and gain. The circuit is easily adjusted for +5 V to –5 V operation by first writing 80H to R08H and adjusting R_O for 0 V output. Then FFH is written to R08H and R_G is adjusted until the output is 5 V. Note that 00H in R08H corresponds to –5 V out.

Figure 17 shows an example of how to interface the HCTL-1100 to an H-bridge amplifier. An H-bridge amplifier allows bipolar motor operation with a unipolar power supply. The Sign Reversal Inhibit feature prevents all transistors from being on at the same time when the direction of motion is reversed.

Table 5. Maximum Number of I/O Allowed

Sample Timer Register Value	Operating Mode	Maximum Number of I/O Operations Allowed per Sample
07H (07D)	Position Control or Prop. Vel. Control	5
OFH (15D)	Position Control or Prop. Vel. Control	133
	Trapezoidal Prof. or Integral Vel. Control	6

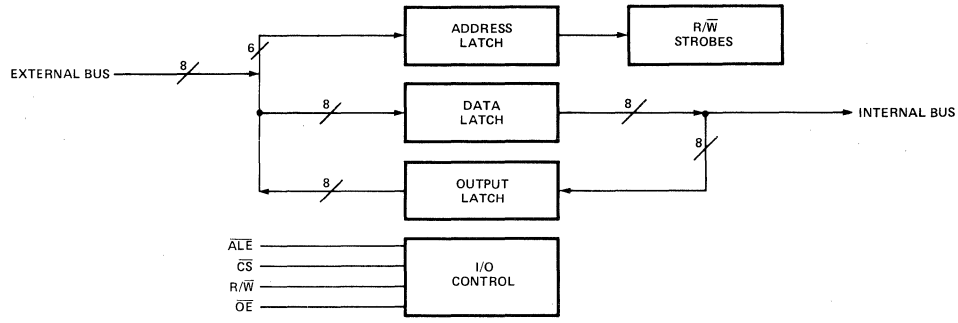


Figure 15. I/O Port Block Diagram.

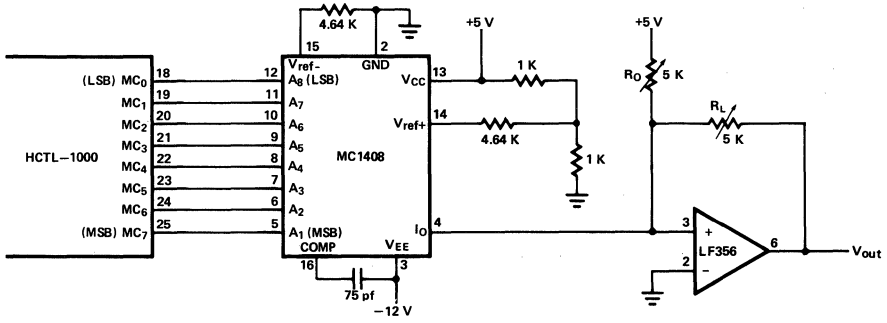


Figure 16. Linear Amplifier Interface.

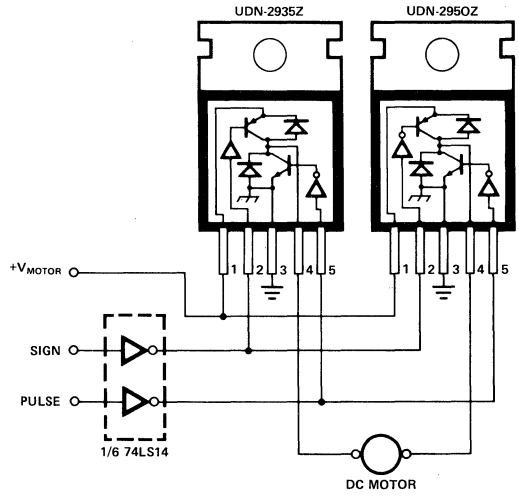


Figure 17. H-Bridge Amplifier Interface.

Additional Information From Hewlett-Packard

Additional information regarding the HCTL-1100 is available from the Hewlett-Packard Motion Control Factory. Please contact your local HP sales representative for more information.

1. Application Note 1032: "Design of the HCTL-1000's Digital Filter Parameters by the Combination Method"
2. Intel 8051 interface to the HCTL-1100
3. Zilog Z80 interface to the HCTL-1100
4. Motorola 6803-1 interface to the HCTL-1100
5. HCTL-1100 Sample Timer and Digital Filter (Seminar Slides)
6. DC Brush Motor Interfaces (Seminar Slides)
7. DC Brushless Motor Interfaces (Seminar Slides)
8. Step Motor Interfaces– including half-step mode (Seminar Slides)
9. List of Board Level Vendors using the HCTL-1000/ HCTL-1100. Many companies provide board level products using the HCTL-1000 and HCTL-1100 compatible with numerous busses.
10. HCTL-1000/HCTL-1100 Troubleshooting Guide. An answer guide to the most often asked questions about the operation of the HCTL-1000 and HCTL-1100.

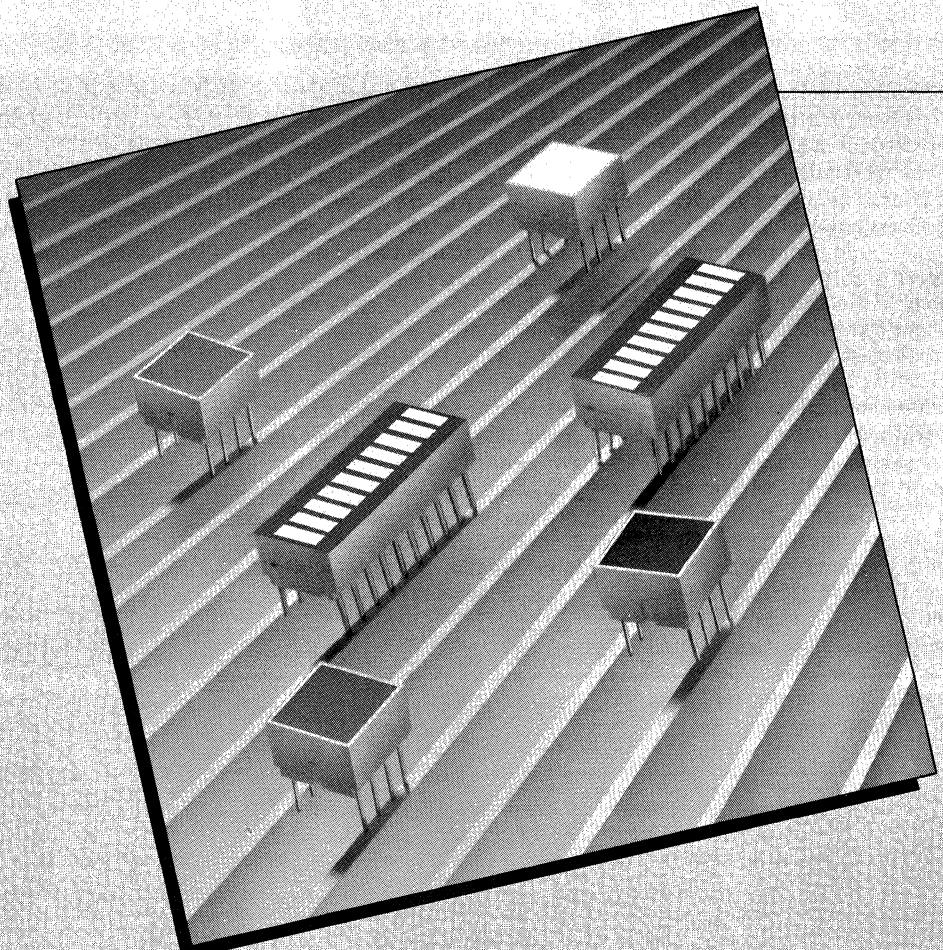
Ordering Information

HCTL-1100: 40 Pin DIP Package
HCTL-1100#PLC: 44 Pin PLCC Package

HEWLETT PACKARD

Light Bars and Bar Graph Arrays

- Light Bars
- Bar Graph Arrays

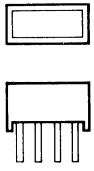
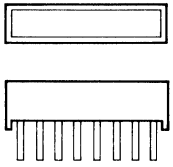
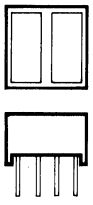
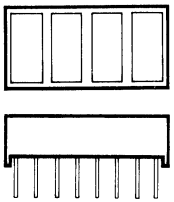
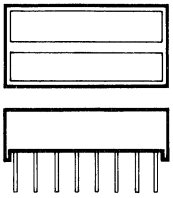


Light Bars and Bar Graph Arrays

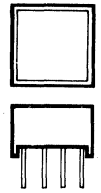
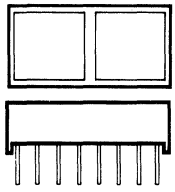
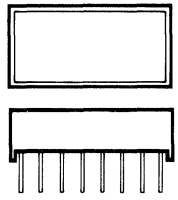
LED Light Bars are Hewlett-Packard's innovative solution to fixed message annunciation. The large, uniformly illuminated light emitting surface may be used for backlighting legends or simple indicators. Four distinct colors are offered: AlGaAs red, high efficiency red, yellow, and high performance green with two bicolor combinations. The AlGaAs Red Light Bars provide exceptional brightness at very low drive currents for those applications where portability and battery backup are important considerations. Each of the eight X-Y stackable package styles offers one, two, or four light emitting surfaces. Along with this family of stackable light bars, HP also provides a single chip light bar for high brightness indication of small areas. Panel Mounts are also available for all devices.

In addition to light bars, HP offers effective analog message annunciation with the 10-element LED Bar Graph Arrays. These bar graph arrays eliminate the matching and alignment problems commonly associated with arrays of discrete LED indicators. Each device offers easy to handle packages that are compatible with standard DIP sockets. The 10-element Bar Graph Array is available in standard red, AlGaAs red, high efficiency red, yellow, and high performance green. The multicolor 10-element arrays have high efficiency red, yellow, and green LEDs in one package. The package is X-Y stackable, with a unique interlock allowing easy end-to-end alignment.

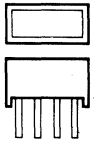
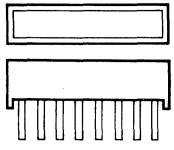
LED Light Bars

Device		Description			Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLMP-2300	High Efficiency Red	4 Pin In-Line; 0.100" Centers; 0.400"L x 0.195"W x 0.245"H	Diffused	23 mcd	2.0 V	2-8
	HLMP-2400	Yellow		Diffused	20 mcd	2.1 V	
	HLMP-2500	Green		Green Diffused	25 mcd	2.2 V	
	HLMP-2350	High Efficiency Red	8 Pin In-Line; 0.100" Centers; 0.800"L x 0.195"W x 0.245"H	Diffused	45 mcd	2.0 V	
	HLMP-2450	Yellow		Diffused	38 mcd	2.1 V	
	HLMP-2550	Green		Green Diffused	50 mcd	2.2 V	
	HLMP-2600	High Efficiency Red	8 Pin DIP; 0.100" Centers; 0.400"L x 0.400"W x 0.245"H Dual Arrangement	Diffused	22 mcd	2.0 V	
	HLMP-2700	Yellow		Diffused	18 mcd	2.1 V	
	HLMP-2800	Green		Green Diffused	25 mcd	2.2 V	
	HLMP-2620	High Efficiency Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Quad Arrangement	Diffused	25 mcd	2.0 V	
	HLMP-2720	Yellow		Diffused	18 mcd	2.1 V	
	HLMP-2820	Green		Green Diffused	25 mcd	2.2 V	
	HLMP-2635	High Efficiency Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Dual Bar Arrangement	Diffused	45 mcd	2.0 V	
	HLMP-2735	Yellow		Diffused	35 mcd	2.1 V	
	HLMP-2835	Green		Green Diffused	50 mcd	2.2 V	

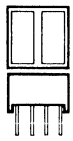
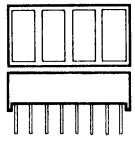
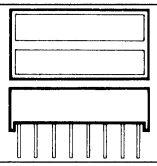
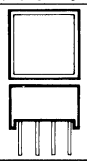
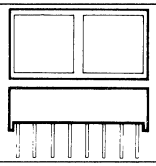
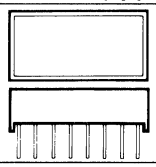
LED Light Bars (Continued)

Device		Description			Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLMP-2655	High Efficiency Red	8 Pin DIP; 0.100" Centers; 0.400"L x 0.400"W x 0.245"H Square Arrangement	Diffused	43 mcd	2.0 V	2-8
	HLMP-2755	Yellow		Diffused	35 mcd	2.1 V	
	HLMP-2855	Green		Green Diffused	50 mcd	2.2 V	
	HLMP-2670	High Efficiency Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Dual Square Arrangement	Diffused	45 mcd	2.0 V	
	HLMP-2770	Yellow		Diffused	35 mcd	2.1 V	
	HLMP-2870	Green		Green Diffused	50 mcd	2.2 V	
	HLMP-2685	High Efficiency Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Single Bar Arrangement	Diffused	80 mcd	2.0 V	
	HLMP-2785	Yellow		Diffused	70 mcd	2.1 V	
	HLMP-2885	Green		Green Diffused	100 mcd	2.2 V	

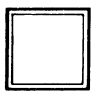
DH AlGaAs Low Current LED Light Bars

Device		Description			Typical Luminous Intensity @ 3 mA	Typical Forward Voltage @ 3mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLCP-A100	AlGaAs Red	4 Pin In-Line; 0.100" Centers; 0.400"L x 0.195"W x 0.245"H	Diffused	7.5 mcd	1.6 V	2-8
	HLCP-B100	AlGaAs Red	8 Pin In-Line; 0.100" Centers; 0.800"L x 0.195"W x 0.245"H	Diffused	15.0 mcd		

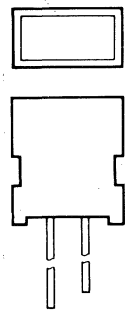
DH AlGaAs Low Current LED Light Bars (Continued)

Device		Description			Typical Luminous Intensity @ 3 mA	Typical Forward Voltage @ 3 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLCP-D100	AlGaAs Red	8 Pin DIP; 0.100" Centers; 0.400"L x 0.400"W x 0.245"H Dual Arrangement	Diffused	7.5 mcd	1.6 V	2-8
	HLCP-E100	AlGaAs Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Quad Arrangement	Diffused	7.5 mcd		
	HLCP-F100	AlGaAs Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Dual Bar Arrangement	Diffused	15.0 mcd		
	HLCP-C100	AlGaAs Red	8 pin DIP; 0.100" Centers; 0.400"L x 0.400"W x 0.245"H Square Arrangement	Diffused	15.0 mcd		
	HLCP-G100	AlGaAs Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Dual Square Arrangement	Diffused	15.0 mcd		
	HLCP-H100	AlGaAs Red	16 Pin DIP; 0.100" Centers; 0.800"L x 0.400"W x 0.245"H Single Bar Arrangement	Diffused	30.0 mcd		

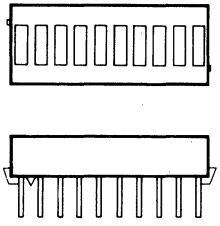
LED Bicolor Light Bars

Device		Description			Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLMP-2950	High Efficiency Red/ Yellow	8 Pin DIP; 0.100" Centers; 0.400"L x 0.400"W x 0.245"H Square Arrangement	Diffused	HER: 20 mcd Yellow: 12 mcd	HER: 2.0 V Yellow: 2.1 V	2-8
	HLMP-2965	High Efficiency Red/ Green		Diffused	HER: 20 mcd Green: 20 mcd	HER: 2.0 V Green: 2.2 V	

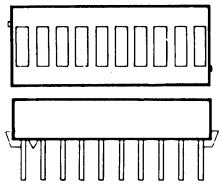
Single Chip LED Light Bar

Device		Description			Tyical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-T200	High Efficiency Red (626 nm)	One Chip LED Light Bar	Tinted Diffused	4.8 mcd @ 20 mA	100°	2.2 V @ 20 mA	2-19
	HLMP-T300	Yellow (585 nm)			6.0 mcd @ 20 mA		2.2 V @ 20 mA	
	HLMP-T400	Orange (608 nm)			4.8 mcd @ 20 mA		2.2 V @ 20 mA	
	HLMP-T500	Green (569 nm)			6.0 mcd @ 20 mA		2.3 V @ 20 mA	

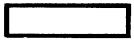
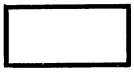
LED Bar Graph Arrays

Device		Description			Typical Luminous Intensity	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HDSP-4820	Standard Red	20 Pin DIP; 0.100" Centers;1.0"L x 0.400"W x 0.200"	Diffused	1250 µcd @ 20 mA DC	1.6 V @ 20 mA DC	2-23
	HDSP-4830	High Efficiency Red		Diffused	3500 µcd @ 10 mA DC	2.1 V @ 20 mA DC	
	HDSP-4840	Yellow		Diffused	1900 µcd @ 10 mA DC	2.2 V @ 20 mA DC	
	HDSP-4850	High Performance Green		Green Diffused	1900 µcd @ 10 mA DC	2.1 V @ 10 mA DC	
	HDSP-4832	Multicolor		Diffused	1900 µcd @ 10 mA DC		
	HDSP-4836	Multicolor		Diffused	1900 µcd @ 10 mA DC		

DH AlGaAs Low Current 10-Element Bar Graph Arrays

Device		Description			Typical Luminous Intensity	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLCP-J100	AlGaAs Red	20 Pin DIP; 0.100" Centers;1.0"L x 0.400"W x 0.200"H	Diffused	1000 µcd @ 1 mA	1.6 V @ 1 mA	2-23

Panel Mounts for LED Light Bars

Device		Corresponding Light Bar Module Part Number	Page No.
Package Outline Drawing	Part No.		
	HLMP-2598	HLMP-2350, -2450, -2550, HLCP-B100	2-30
	HLMP-2599	HLMP-2300, -2400, -2500, HLCP-A100	
	HLMP-2898	HLMP-2600, -2700, -2800 -2655, -2755, -2855 -2950, -2965, HLCP-C100, -D100	
	HLMP-2899	HLMP-2620, -2720, -2820, -2635, -2735, -2835 -2670, -2770, -2870 -2685, -2785, -2885 HLCP-E100, -F100, -G100, -H100	

Intensity Selected Light Bars

Description	Option Code	Applicable Part Number HLMP-	Page No.
	S02	This option provides the selection of light bars from two adjacent luminous intensity categories.	*

*Contact your local Sales Representative for information regarding this product. (See Section 9.)

HEWLETT PACKARD

LED Light Bars

Technical Data

HLCP-A100, -B100, -C100, -D100, -E100, -F100, -G100, -H100
HLMP-2300, -2350, -2400, -2450, -2500, -2550, -2600, -2620, -2635, -2655, -2670, -2685, -2700, -2720, -2735, -2755, -2770, -2785, -2800, -2820, -2835, -2855, -2870, -2885, -2950, -2965

Features

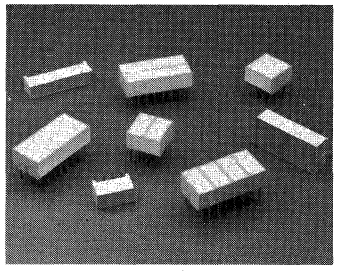
- **Large Bright, Uniform Light Emitting Areas**
- **Choice of Colors**
- **Categorized for Light Output**
- **Yellow and Green Categorized for Dominant Wavelength**
- **Excellent ON-OFF Contrast**
- **X-Y Stackable**
- **Flush Mountable**
- **Can be Used with Panel and Legend Mounts**
- **Light Emitting Surface Suitable for Legend Attachment per Application Note 1012**
- **HLCP-X100 Series Designed for Low Current Operation**
- **Bicolor Devices Available**

Applications

- **Business Machine Message Annunciators**
- **Telecommunications Indicators**
- **Front Panel Process Status Indicators**
- **PC Board Identifiers**
- **Bar Graphs**

Description

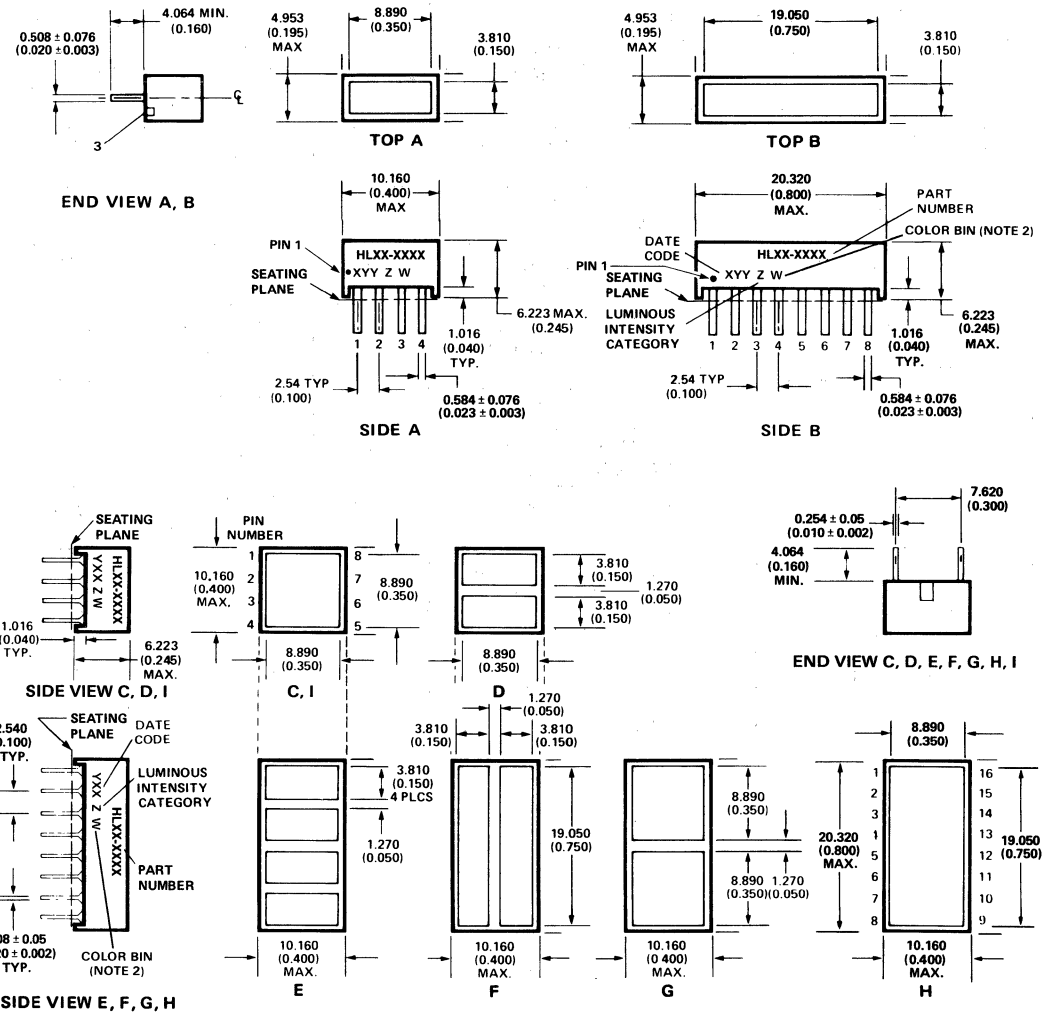
The HLCP-X100 and HLMP-2XXX series light bars are rectangular light sources designed for a variety of applications where a large bright source of light is required. These light bars are configured in single-in-line and dual-in-line packages that contain either single or segmented light emitting areas. The AlGaAs Red HLCP-X100 series LEDs use double heterojunction AlGaAs on a GaAs substrate. The HER HLMP-2300/2400 and Yellow HLMP-2400/2700 series LEDs have their p-n junctions diffused into a GaAsP epitaxial layer on a GaP substrate. The Green HLMP-2500/2800 series LEDs use a liquid phase GaP epitaxial layer on a GaP substrate. The bicolor HLMP-2900 series use a combination of HER/Yellow or HER/Green LEDs.



Selection Guide

Light Bar Part Number				Size of Light Emitting Areas	Number of Light Emitting Areas	Package Outline		Corresponding Panel and Legend Mount Part No. HLMP-
HLCP-	HLMP-							
AlGaAs	HER	Yellow	Green					
A100	2300	2400	2500	8.89 mm x 3.81 mm (.350 in. x .150 in.)	1	A		2599
B100	2350	2450	2550	19.05 mm x 3.81 mm (.750 in. x .150 in.)	1	B		2598
D100	2600	2700	2800	8.89 mm x 3.81 mm (.350 in. x .150 in.)	2	D		2898
E100	2620	2720	2820	8.89 mm x 3.81 mm (.350 in. x .150 in.)	4	E		2899
F100	2635	2735	2835	3.81 mm x 19.05 mm (.150 in. x .750 in.)	2	F		2899
C100	2655	2755	2855	8.89 mm x 8.89 mm (.350 in. x .350 in.)	1	C		2898
G100	2670	2770	2870	8.89 mm x 8.89 mm (.350 in. x .350 in.)	2	G		2899
H100	2685	2785	2885	8.89 mm x 19.05 mm (.350 in. x .750 in.)	1	H		2899
	2950	2950		8.89 mm x 8.89 mm (.350 in. x .350 in.)	Bicolor	I		2898
	2965		2965	8.89 mm x 8.89 mm (.350 in. x .350 in.)	Bicolor	I		2898

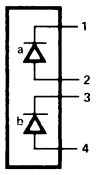
Package Dimensions



NOTES:

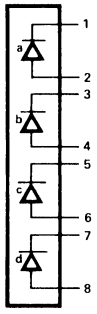
1. **DIMENSIONS IN MILLIMETRES (INCHES). TOLERANCES ±0.25 mm (±0.010 IN.) UNLESS OTHERWISE INDICATED.**
2. **FOR YELLOW AND GREEN DEVICES ONLY.**
3. **CATHODE NOTCH IS IN PROCESS OF BEING REPLACED BY A CATHODE DOT ON THE UNIT MARKING SIDE OF THE DEVICE. PROPOSED EFFECTIVE DATE FOR THIS CONVERSION IS JANUARY 1ST, 1991.**

Internal Circuit Diagrams

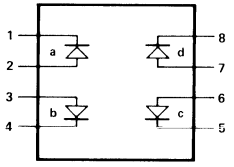


A

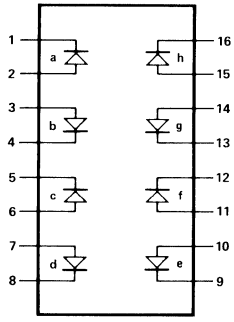
PIN	PIN FUNCTION A -2300/-2400 -2500	PIN FUNCTION B -2350/-2450 -2550
1	Cathode — a	Cathode — a
2	Anode — a	Anode — a
3	Cathode — b	Cathode — b
4	Anode — b	Anode — b
5		Cathode — c
6		Anode — c
7		Cathode — d
8		Anode — d



B

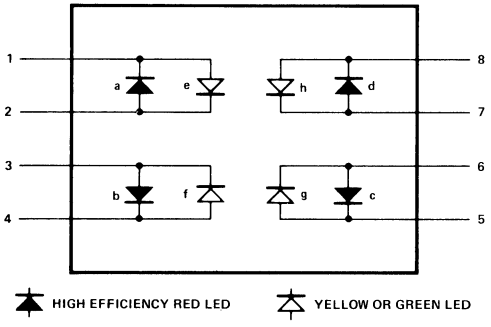


C,D



E,F,G,H

PIN	PIN FUNCTION C, D	PIN FUNCTION E, F, G, H
1	CATHODE a	CATHODE a
2	ANODE a	ANODE a
3	ANODE b	ANODE b
4	CATHODE b	CATHODE b
5	CATHODE c	CATHODE c
6	ANODE c	ANODE c
7	ANODE d	ANODE d
8	CATHODE d	CATHODE d
9		CATHODE e
10		ANODE e
11		ANODE f
12		CATHODE f
13		CATHODE g
14		ANODE g
15		ANODE h
16		CATHODE h



I

PIN	PIN FUNCTION HER	PIN FUNCTION YELLOW/ GREEN
1	CATHODE a	ANODE e
2	ANODE a	CATHODE e
3	ANODE b	CATHODE f
4	CATHODE b	ANODE f
5	CATHODE c	ANODE g
6	ANODE c	CATHODE g
7	ANODE d	CATHODE h
8	CATHODE d	ANODE h

Absolute Maximum Ratings

Parameter	AlGaAs Red HLCP-X100 Series	HER HLMP-2300/ 2600/29XX Series	Yellow HLMP-2400/ 2700/2950 Series	Green HLMP-2500/ 2800/2965 Series
Average Power Dissipated per LED chip	37 mW[1]	135 mW[2]	85 mW[3]	135 mW[2]
Peak Forward Current per LED chip	45 mA[4]	90 mA[5]	60 mA[5]	90 mA[5]
Average Forward Current per LED chip	15 mA	25 mA	20 mA	25 mA
DC Forward Current per LED chip	15 mA[1]	30 mA[2]	25 mA[3]	30 mA[2]
Reverse Voltage per LED chip	5 V	6 V[6]		
Operating Temperature Range	–20°C to +100°C[7]	–40°C to +85°C		–20°C to +85°C
Storage Temperature Range	–55°C to +100°C	–40°C to +85°C		
Lead Soldering Temperature 1.6 mm (1/16 inch) Below Seating Plane	260°C for seconds[8]			

Notes:
1. Derate above 87°C at 1.7 mW/°C per LED chip. For DC operation, derate above 91°C at 0.8 mA/°C.
2. Derate above 25°C at 1.8 mW/°C per LED chip. For DC operation, derate above 50°C at 0.5 mA/°C.
3. Derate above 50°C at 1.8 mW/°C per LED chip. For DC operation, derate above 60°C at 0.5 mA/°C.
4. See Figure 1 to establish pulsed operation. Maximum pulse width is 1.5 mS.
5. See Figure 6 to establish pulsed operation. Maximum pulse width is 2 mS.
6. Does not apply to bicolor parts.
7. For operation below –20°C, contact your local HP sales representative.
8. Maximum component side temperature is 140°C during solder process.

Electrical/Optical Characteristics at T_A = 25°C
AlGaAs Red HLCP-X100 Series

Parameter	HLCP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity per Lighting Emitting Area[1]	A100/D100/E100	I_V	3	7.5		mcd	I_F = 3 mA
	B100/C100/F100/G100		6	15		mcd	
	H100		12	30		mcd	
Peak Wavelength		λ_{PEAK}		645		nm	
Dominant Wavelength[2]		λ_d		637		nm	
Forward Voltage per LED		V_F		1.8	2.2	V	I_F = 20 mA
Reverse Breakdown Voltage per LED		V_R	5	15		V	I_R = 100 µA
Thermal Resistance LED Junction-to-Pin		$R\theta_{J\text{-}PIN}$		250		°C/W/ LED	

High Efficiency Red HLMP-2300/2600/2900 Series

Parameter	HLMP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity per Lighting Emitting Area[1]	2300/2600/2620	I_V	6	23		mcd	I_F = 20 mA
	2350/2635/2655/2670/2950[3]		13	45		mcd	
	2965[4]		19	45		mcd	
	2685		22	80		mcd	
Peak Wavelength		λ_{PEAK}		635		nm	
Dominant Wavelength[2]		λ_d		626		nm	
Forward Voltage per LED		V_F		2.0	2.6	V	I_F = 20 mA
Reverse Breakdown Voltage per LED[5]		V_R	6	15		V	I_R = 100 μA
Thermal Resistance LED Junction-to-Pin		$R\theta_{J\text{-}PIN}$		150		°C/W/ LED	

Yellow HLMP-2400/2700/2950 Series

Parameter	HLMP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity per Lighting Emitting Area[1]	2400/2700/2720	I_V	6	20		mcd	I_F = 20 mA
	2450/2735/2755/2770/2950[3]		13	38		mcd	
	2785		26	70		mcd	
Peak Wavelength		λ_{PEAK}		583		nm	
Dominant Wavelength[2]		λ_d	579.0	585	595.0	nm	
Forward Voltage per LED		V_F		2.1	2.6	V	I_F = 20 mA
Reverse Breakdown Voltage per LED[5]		V_R	6	15		V	I_R = 100 μA
Thermal Resistance LED Junction-to-Pin		$R\theta_{J\text{-}PIN}$		150		°C/W/ LED	

High Performance Green HLMP-2500/2800/2965 Series

Parameter	HLMP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity per Lighting Emitting Area[1]	2500/2800/2820	I_V	5	25		mcd	I_F = 20 mA
	2550/2835/2855/2870		11	50		mcd	
	2965[4]		25	50		mcd	
	2885		22	100		mcd	
Peak Wavelength		λ_{PEAK}		565		nm	
Dominant Wavelength[2]		λ_d		572	577	nm	
Forward Voltage per LED		V_F		2.2	2.6	V	I_F = 20 mA
Reverse Breakdown Voltage per LED[5]		V_R	6	15		V	I_R = 100 µA
Thermal Resistance LED Junction-to-Pin		$R\theta_{J\text{-}PIN}$		150		°C/W/ LED	

Notes:

1. These devices are categorized for luminous intensity. The intensity category is designated by a letter code on the side of the package.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is the single wavelength which defines the color of the device. Yellow and Green devices are categorized for dominant wavelength with the color bin designated by a number code on the side of the package.
3. This is an HER/Yellow bicolor light bar. HER electrical/optical characteristics are shown in the HER table. Yellow electrical/ optical characteristics are shown in the Yellow table.
4. This is an HER/Green bicolor light bar. HER electrical/optical characteristics are shown in the HER table. Green electrical/ optical characteristics are shown in the Green table.
5. Does not apply to HLMP-2950 or HLMP-2965.

AlGaAs Red

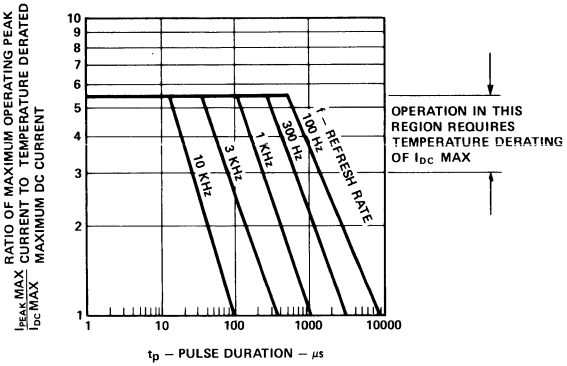


Figure 1. Maximum Allowable Peak Current vs. Pulse Duration

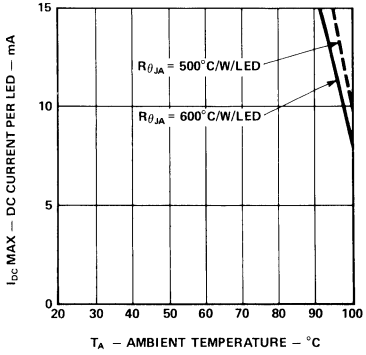


Figure 2. Maximum Allowed DC Current per LED vs. Ambient Temperature, T_JMAX = 110°C

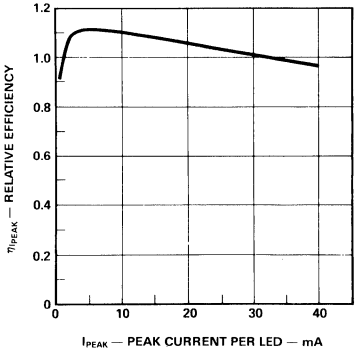


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current

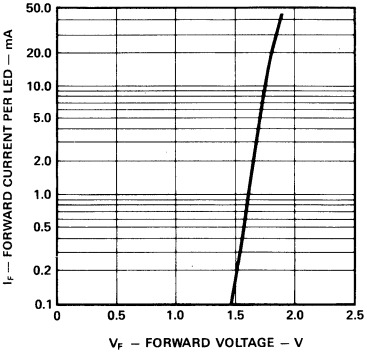


Figure 4. Forward Current vs. Forward Voltage

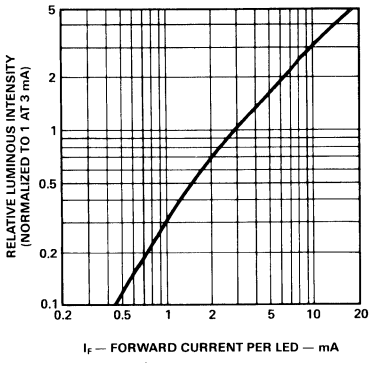


Figure 5. Relative Luminous Intensity vs. DC Forward Current

HER, Yellow, Green

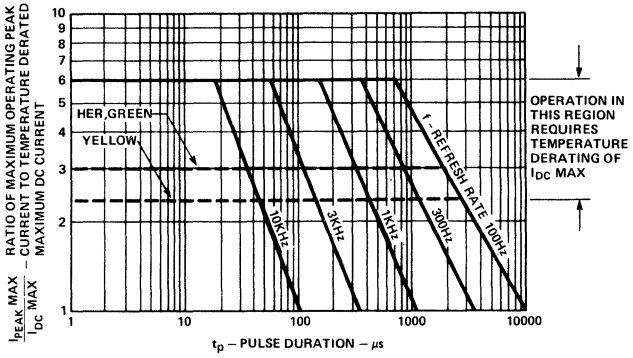


Figure 6. Maximum Allowed Peak Current vs. Pulse Duration

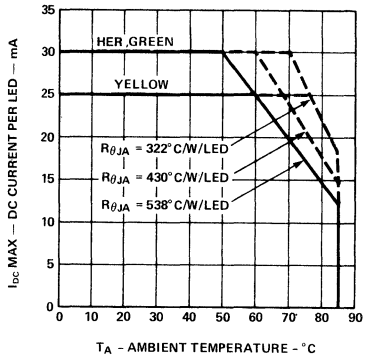


Figure 7. Maximum Allowable DC Current per LED vs. Ambient Temperature, T_J MAX = 100°C

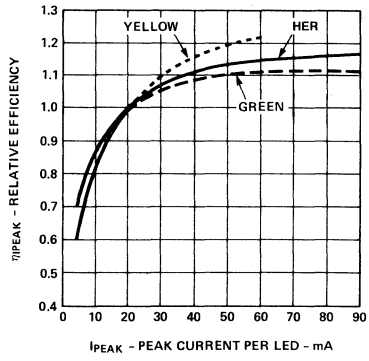


Figure 8. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak PED Current

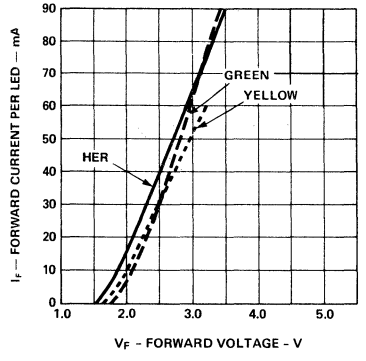


Figure 9. Forward Current vs. Forward Voltage Characteristics

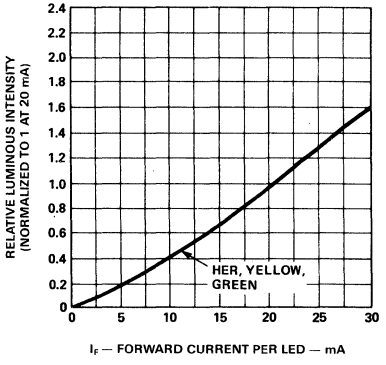


Figure 10. Relative Luminous Intensity vs. DC Forward Current

For a detailed explanation on the use of data sheet information and recommended soldering procedures, see Application Notes 1005, 1027, and 1031.

Electrical

These light bars are composed of two, four, or eight light emitting diodes, with the light from each LED optically scattered to form an evenly illuminated light emitting surface.

The anode and cathode of each LED is brought out by separate pins. This universal pinout arrangement allows the LEDs to be connected in three possible configurations: parallel, series, or series parallel. The typical forward voltage values can be scaled from Figures 4 and 9. These values should be used to calculate the current limiting resistor value and typical power consumption. Expected maximum V_F values for driver circuit design and maximum power dissipation, may be calculated using the following V_FMAX models:

AlGaAs Red HLCP-X100 series

$V_F MAX = 1.8\ V + I_{Peak}\ (20\Omega)$
For: $I_{Peak} \leq 20$ mA
$V_F MAX = 2.0\ V + I_{Peak}\ (10\Omega)$
For: $20\ mA \leq I_{Peak} \leq 45$ mA

HER (HDSP-2300/2600/2900), Yellow (HDSP-2400/2700/2900) and Green (HDSP-2500/2800/2900) series

$V_F MAX = 1.6 + I_{Peak}\ (50\Omega)$
For: $5\ mA \leq I_{Peak} \leq 20$ mA
$V_F MAX = 1.8 + I_{Peak}\ (40\Omega)$
For: $I_{Peak} \geq 20$ mA

The maximum power dissipation can be calculated for any pulsed or DC drive condition. For DC operation, the maximum power dissipation is the product of the maximum forward voltage and the maximum forward current. For pulsed operation, the maximum power dissipation is the product of the maximum forward voltage at the peak forward current times the maximum average forward current. Maximum allowable power dissipation for any given ambient temperature and thermal resistance ($R\theta_{J\text{-}A}$) can be determined by using Figure 2 or 7. The solid line in Figure 2 or 7 ($R\theta_{J\text{-}A}$ of 600/538 C/W) represents a typical thermal resistance of a device socketed in a printed circuit board. The dashed lines represent achievable thermal resistances that can be obtained through improved thermal design. Once the maximum allowable power dissipation is determined, the maximum pulsed or DC forward current can be calculated.

Optical

Size of Light Emitting Area	Surface Area	
	Sq. Metres	Sq. Feet
8.89 mm x 8.89 mm	67.74×10^{-6}	729.16×10^{-6}
8.89 mm x 3.81 mm	33.87×10^{-6}	364.58×10^{-6}
8.89 mm x 19.05 mm	135.48×10^{-6}	1458.32×10^{-6}
3.81 mm x 19.05 mm	72.85×10^{-6}	781.25×10^{-6}

The radiation pattern for these light bar devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas:

$$L_v\ (cd/m^2) = \frac{I_v\ (cd)}{A\ (m^2)}$$

$$L_v\ (\text{footlamberts}) = \frac{\pi I_v\ (cd)}{A\ (ft^2)}$$

Refresh rates of 1 kHz or faster provide the most efficient operation resulting in the maximum possible time average luminous intensity.

The time average luminous intensity may be calculated using the relative efficiency characteristic of Figure 3 or 8, ηI_{PEAK}, and adjusted for operating ambient temperature. The time average luminous intensity at $T_A = 25°C$ is calculated as follows:

$$I_{v\ TIME\ AVG} = \left[\frac{I_{AVG}}{I_{TEST}}\right](\eta I_{PEAK})\ (I_v\ \text{Data Sheet})$$

where:

I_{TEST} = 3 mA for AlGaAs Red (HLMP-X000 series)
20 mA for HER, Yellow and Green (HLMP-2XXX series)

Example:
For HLMP-2735 series

$\eta I_{PEAK} = 1.18$ at $I_{PEAK} = 48$ mA

$$I_{v\ TIME\ AVG} = \left[\frac{12\ mA}{20\ mA}\right](1.18)\ (35\ mcd)$$

$$= 25\ mcd$$

The time average luminous intensity may be adjusted for operating ambient temperature by the following exponential equation:

$$I_v(T_A) = I_V(25°C)e^{[K(T_A - 25°C)]}$$

Color	K
AlGaAs Red	–0.0095/°C
HER	–0.0131/°C
Yellow	–0.0112/°C
Green	–0.0104/°C

Example:

I_v (80°C) = (25 mcd)$e^{[-0.0112(80-25)]}$
= 14 mcd.

Mechanical

These light bar devices may be operated in ambient temperatures above +60°C without derating when installed in a PC board configuration that provides a thermal resistance pin to ambient value less than 280°C/W/LED. See Figure 2 or 7 to determine the maximum allowed thermal resistance for the PC board, $R\theta_{PC\text{-}A}$, which will permit nonderated operation in a given ambient temperature.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DES, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

For further information on soldering LEDs please refer to Application Note 1027.

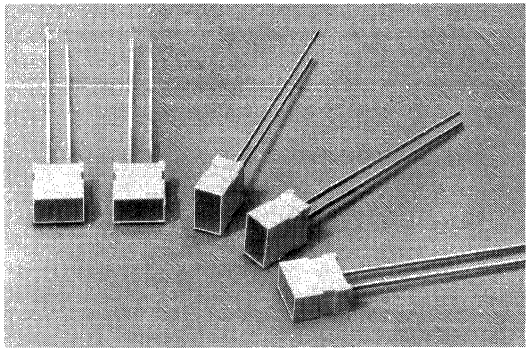
HEWLETT PACKARD

SINGLE CHIP LED LIGHT BAR

HIGH EFFICIENCY RED HLMP-T200 SERIES
YELLOW HLMP-T300 SERIES
ORANGE HLMP-T400 SERIES
HIGH PERFORMANCE GREEN HLMP-T500 SERIES

Features

- **FLAT RECTANGULAR LIGHT EMITTING SURFACE**
- **CHOICE OF 4 BRIGHT COLORS**
- **EXCELLENT ON/OFF CONTRAST**
- **IDEAL AS FLUSH MOUNTED PANEL INDICATORS**
- **LONG LIFE: SOLID STATE RELIABILITY**
- **SOLDER COATED LEADS**



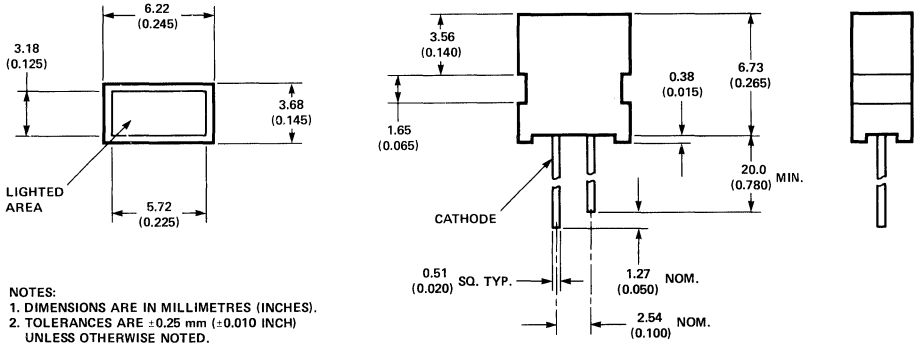
Description

The HLMP-T200/-T300/-T400/-T500 light bars are rectangular light sources designed for a variety of applications where this shape and a high sterance are desired. These light bars consist of a rectangular plastic case around an epoxy encapsulated LED lamp. The encapsulant is tinted to match the color of the emitted light. The flat top surface is exceptionally uniform in light emission and the plastic case eliminates light leakage from the sides of the device.

Applications

- **BAR GRAPHS**
- **FRONT PANEL STATUS INDICATORS**
- **TELECOMMUNICATIONS INDICATORS**
- **PUSH BUTTON ILLUMINATION**
- **PC BOARD IDENTIFIERS**
- **BUSINESS MACHINE MESSAGE ANNUNCIATORS**

Package Dimensions



NOTES:
1. DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. TOLERANCES ARE ±0.25 mm (±0.010 INCH) UNLESS OTHERWISE NOTED.

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	High Efficiency Red T200	3.0	4.8		mcd	I_F = 20 mA
		Orange T400	3.0	4.8			
		Yellow T300	3.0	6.0			
		Green T500	3.0	6.0			
$2\Theta 1/2$	Included Angle Between Half Luminous Intensity Points	All		100		Deg.	I_F = 20 mA See Note 1
λ_{PEAK}	Peak Wavelength	High Efficiency Red		635		nm	Measurement at Peak
		Orange		612			
		Yellow		583			
		Green		565			
λ_d	Dominant Wavelength	High Efficiency Red		626		nm	See Note 2
		Orange		608			
		Yellow		585			
		Green		569			
τ_S	Speed of Response	High Efficiency Red		350		ns	
		Orange		350			
		Yellow		390			
		Green		870			
C	Capacitance	High Efficiency Red		4		pF	V_F = 0; f = 1 MHz
		Orange		4			
		Yellow		8			
		Green		11			
$R\theta_{JC}$	Thermal Resistance	All		120		°C/W	Junction to Cathode Lead at Seating Plane
V_F	Forward Voltage	HER/Orange	1.5	2.2	2.6	V	I_F = 20 mA
		Yellow	1.5	2.2	2.6		
		Green	1.6	2.3	2.6		
V_R	Reverse Breakdown Volt.	All	5.0			V	I_R = 100 μA
η_V	Luminous Efficacy	High Efficiency Red		145		$\frac{\text{lumens}}{\text{Watt}}$	See Note 3
		Orange		262			
		Yellow		500			
		Green		595			

Notes:
1. $\Theta 1/2$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Characteristics at $T_A = 25°C$

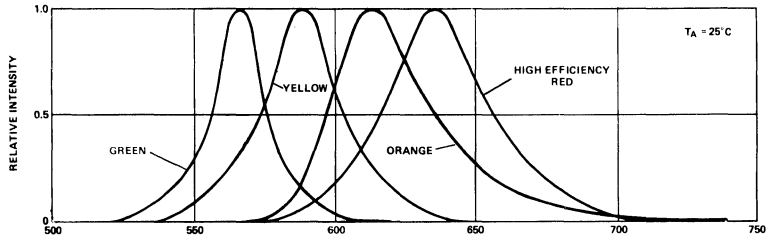


Figure 1. Relative Intensity vs. Wavelength.

High Efficiency Red, Orange, Yellow, and Green Light Bars

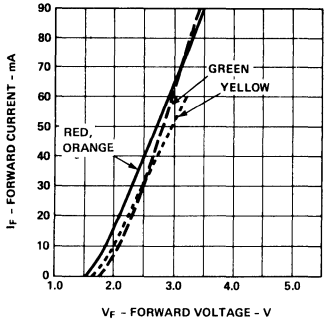


Figure 2. Forward Current vs. Forward Voltage Characteristics.

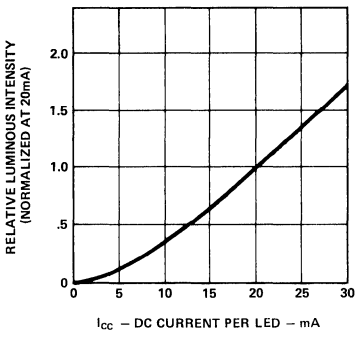


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

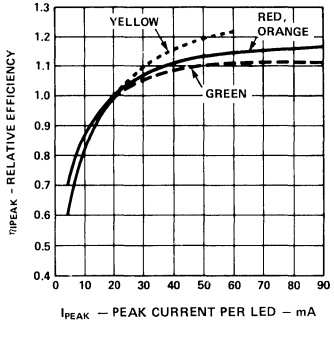


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. LED Peak Current.

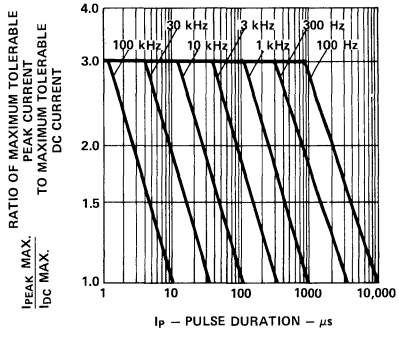


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

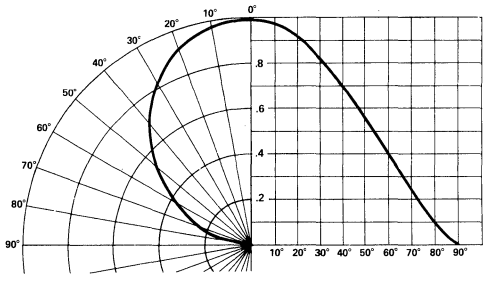


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	High Efficiency Red/ Orange	Yellow	Green	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Operating Temperature Range	-40 to +85	-40 to +85	-20 to +85	°C
Storage Temperature Range	-55 to +100	-55 to +100	-55 to +100	
Reverse Voltage (I_R = 100 μA)	5			V
Transient Forward Current[4] (10 μsec Pulse)	500			mA
Lead Soldering Temperature [1.6 mm (0.063 in.) below seating plane]	260° C for 3 seconds			

Notes:
1. See Figure 5 to establish pulsed operating conditions.
2. For Red, Orange, and Green derate linearly from 50° C at 0.5 mA/° C. For Yellow derate linearly from 50° C at 0.34 mA/° C.
3. For Red, Orange, and Green derate power linearly from 25° C at 1.6 mW/° C. For Yellow derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

Electrical

The typical forward voltage values, scaled from Figure 2, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design and maximum power dissipation may be calculated using the following V_F models:

$$V_F = 1.8V + I_{PEAK}(40\Omega)$$
For $I_{PEAK} \geq 20$ mA

$$V_F = 1.6V + I_{DC}(50\Omega)$$
For 5 mA $\leq I_{DC} \leq$ 20 mA

Optical

The radiation pattern for these light bar devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas:

$$L_V\ (cd/m^2) = \frac{I_V\ (cd)}{A\ (m^2)}$$

$$L_V\ (footlamberts) = \frac{\pi I_V\ (cd)}{A\ (ft^2)}$$

Size of light emitting area (A)= 3.18 mm x 5.72 mm
$= 18.19 \times 10^{-6}\ m^2$
$= 195.8 \times 10^{-6}\ ft^2$

Mechanical

These light bar devices may be operated in ambient temperatures above +50° C without derating when installed in a PC board configuration that provides a thermal resistance (junction to ambient) value less than 625° C/W.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60° C (140° F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

10-Element Bar Graph Array

Technical Data

HDSP-4820
HLCP-J100
HDSP-4830
HDSP-4840
HDSP-4850
HDSP-4832
HDSP-4836

Features

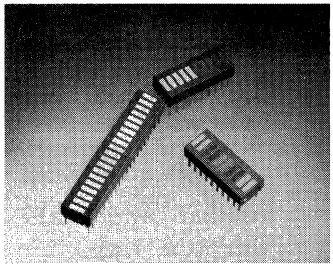
- **Custom Multicolor Array Capability**
- **Matched LEDs for Uniform Appearance**
- **End Stackable**
- **Package Interlock Ensures Correct Alignment**
- **Low Profile Package**
- **Rugged Construction**
- **Large, Easily Recognizable Segments**
- **High ON-OFF Contrast, Segment to Segment**
- **Wide Viewing Angle**
- **Categorized for Luminous Intensity**
- **HDSP-4832/4836/4840/4850 Categorized for Dominant Wavelength**
- **HLCP-J100 Operates at Low Current**
  Typical Intensity of 1.0 mcd at 1 mA Drive Current

Applications

- **Industrial Controls**
- **Instrumentation**
- **Office Equipment**
- **Computer Peripherals**
- **Consumer Products**

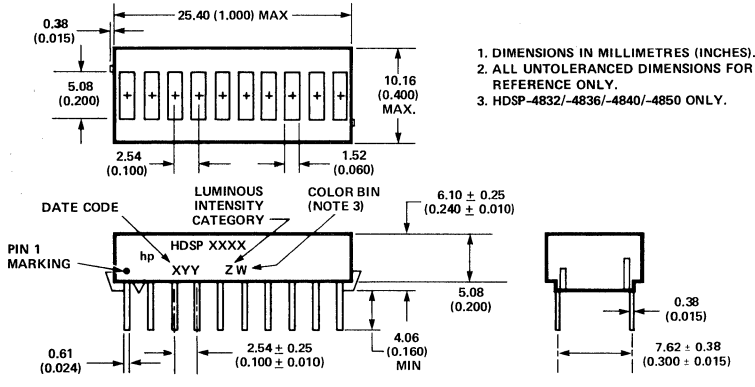
Description

These 10-element LED arrays are designed to display information in easily recognizable bar graph form. The packages are end stackable and therefore capable of displaying long strings of information. Use of these bar graph arrays eliminates the alignment, intensity, and color matching problems associated with discrete LEDs. The HDSP-4820/4830/4840/4850 and HLCP-J100 each contain LEDs of one color. The HDSP-4832/4836 are multicolor arrays with High Efficiency Red, Yellow, and High Performance Green LEDs in a single package.



CUSTOM MULTICOLOR ARRAYS ARE AVAILABLE WITH MINIMUM DELIVERY REQUIREMENTS. CONTACT YOUR LOCAL DISTRIBUTOR OR HP SALES OFFICE FOR DETAILS.

Package Dimensions



1. DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS FOR REFERENCE ONLY.
3. HDSP-4832/-4836/-4840/-4850 ONLY.

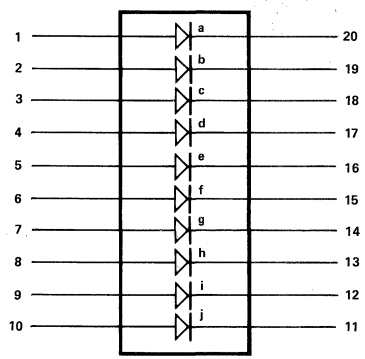
Absolute Maximum Ratings[7]

Parameter	Red HDSP-4820	AlGaAs Red HLCP-J100	HER HDSP-4830	Yellow HDSP-4840	Green HDSP-4850
Average Power Dissipation per LED (T_A = 25°C)	63 mW	37 mW	87 mW	50 mW	105 mW
Peak Forward Current per LED	150 mA[1]	45 mA[2]	90 mA[3]	60 mA[3]	90 mA[3]
DC Forward Current per LED	30 mA[4]	15 mA[4]	30 mA[5]	20 mA[5]	30 mA[5]
Operating Temperature Range	–40°C to +85°C	–20°C to +100°C	–40°C to +85°C		–20°C to +85°C
Storage Temperature Range	–40°C to +85°C	–55°C to +100°C	–40°C to +85°C		
Reverse Voltage per LED	3.0 V	5.0 V	3.0 V		
Lead Soldering Temperature (1.59 mm (1/16 inch) below seating plane)[6]	260°C for 3 seconds[8]				

Notes:

1. See Figure 1 to establish pulsed operating conditions. Maximum pulse width is 1.5 ms.
2. See Figure 2 to establish pulsed operating conditions. Maximum pulse width is 1.5 ms.
3. See Figure 8 to establish pulsed operating conditions. Maximum pulse width is 2 ms.
4. Derate maximum DC current for Red above T_A = 62°C at 0.79 mA/°C, and AlGaAs Red above T_A = 91°C at 0.8 mA°C. See Figure 3.
5. Derate maximum DC current for HER above T_A = 48°C at 0.58 mA/°C, Yellow above T_A = 70°C at 0.66 mA/°C, and Green above T_A = 37°C at 0.48 mA/°C. See Figure 9.
6. Clean only in water, isopropanol, ethanol, Freon TF or TE (or equivalent), or Genesolve DI-15 (or equivalent).
7. Absolute maximum ratings for HER, Yellow, and Green elements of the multicolor arrays are identical to the HDSP-4830/4840/4850 maximum ratings.
8. Maximum component side temperature is 140°C during solder process.

Internal Circuit Diagram



Pin	Function	Pin	Function
1	Anode a	11	Cathode j
2	Anode b	12	Cathode i
3	Anode c	13	Cathode h
4	Anode d	14	Cathode g
5	Anode e	15	Cathode f
6	Anode f	16	Cathode e
7	Anode g	17	Cathode d
8	Anode h	18	Cathode c
9	Anode i	19	Cathode b
10	Anode j	20	Cathode a

Multicolor Array Segment Colors

Segment	HDSP-4832 Segment Color	HDSP-4836 Segment Color
a	HER	HER
b	HER	HER
c	HER	Yellow
d	Yellow	Yellow
e	Yellow	Green
f	Yellow	Green
g	Yellow	Yellow
h	Green	Yellow
i	Green	HER
j	Green	HER

Electrical/Optical Characteristics at $T_A = 25°C$[4]

Red HDSP-4820

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1]	I_F	I_F = 20 mA	610	1250		µcd
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[2]	λ_d			645		nm
Forward Voltage per LED	V_F	I_F = 20 mA		1.6	2.0	V
Reverse Voltage per LED[5]	V_R	I_R = 100 µA	3	12		V
Temperature Coefficient V_F per LED	$\Delta V_F/°C$			–2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			300		°C/W/ LED

AlGaAs Red HLCP-J100

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1]	I_V	I_F = 1 mA	600	1000		µcd
		I_F = 20 mA Pk; 1 of 4 Duty Factor		5200		
Peak Wavelength	λ_{PEAK}			645		nm
Dominant Wavelength[2]	λ_d			637		nm
Forward Voltage per LED	V_F	I_F = 1 mA		1.6		V
		I_F = 20 mA		1.8	2.2	
Reverse Voltage per LED[5]	V_R	I_R = 100 µA	5	15		V
Temperature Coefficient V_F per LED	$\Delta V_F/°C$			–2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			300		°C/W/ LED

High-Efficiency Red HDSP-4830

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1,4]	I_V	I_F = 10 mA	900	3500		µcd
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[2]	λ_d			626		nm
Forward Voltage per LED	V_F	I_F = 20 mA		2.1	2.5	V
Reverse Voltage per LED[5]	V_R	I_R = 100 µA	3	30		V
Temperature Coefficient V_F per LED	ΔV_F/°C			–2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			300		°C/W/ LED

Yellow HDSP-4840

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1,4]	I_V	I_F = 10 mA	600	1900		µcd
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[2,3]	λ_d		581	585	592	nm
Forward Voltage per LED	V_F	I_F = 20 mA		2.2	2.5	V
Reverse Voltage per LED[5]	V_R	I_R = 100 µA	3	40		V
Temperature Coefficient V_F per LED	ΔV_F/°C			–2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			300		°C/W/ LED

Green HDSP-4850

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1,4]	I_V	I_F = 10 mA	600	1900		µcd
Peak Wavelength	λ_{PEAK}			566		nm
Dominant Wavelength[2,3]	λ_d			571	577	nm
Forward Voltage per LED	V_F	I_F = 10 mA		2.1	2.5	V
Reverse Voltage per LED[5]	V_R	I_R = 100 µA	3	50		V
Temperature Coefficient V_F per LED	ΔV_F/°C			–2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			300		°C/W/ LED

Notes:

1. The bar graph arrays are categorized for luminous intensity. The category is designated by a letter located on the side of the package.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
3. The HDSP-4832/-4836/-4840/-4850 bar graph arrays are categorized by dominant wavelength with the category designated by a number adjacent to the intensity category letter. Only the yellow elements of the HDSP-4832/-4836 are categorized for color.
4. Electrical/optical characteristics of the High-Efficiency Red elements of the HDSP-4832/-4836 are identical to the HDSP-4830 characteristics. Characteristics of Yellow elements of the HDSP-4832/-4836 are identical to the HDSP-4840. Characteristics of Green elements of the HDSP-4832/-4836 are identical to the HDSP-4850.
5. Reverse voltage per LED should be limited to 3.0 V max. for the HDSP-4820/4830/4840/4850/4832/4836 and 5.0 V max. for the HLCP-J100.

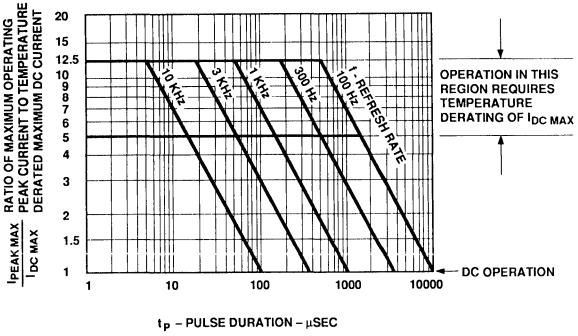


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration – Red.

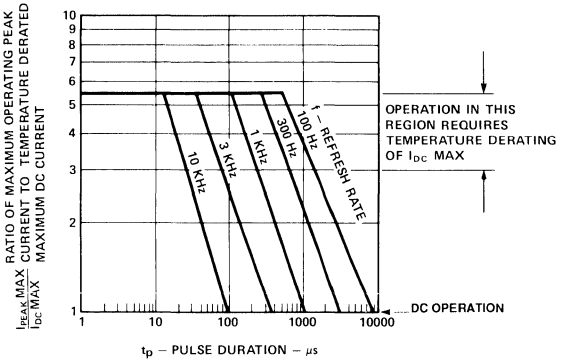


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration – AlGaAs Red.

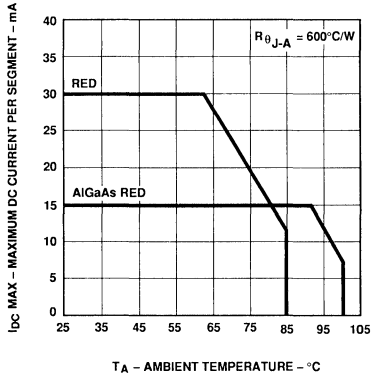


Figure 3. Maximum Allowable DC Current vs. Ambient Temperature. T_{JMAX} = 100°C for Red and T_{JMAX} = 110°C for AlGaAs Red.

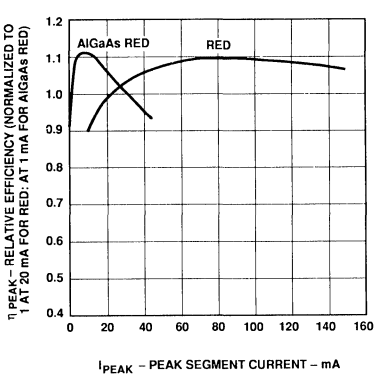


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

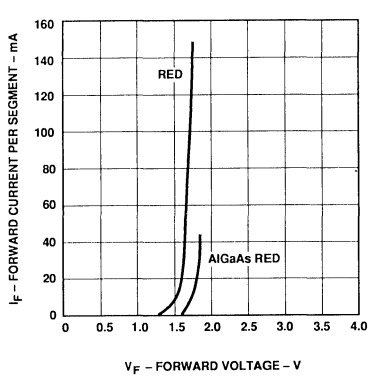


Figure 5. Forward Current vs. Forward Voltage.

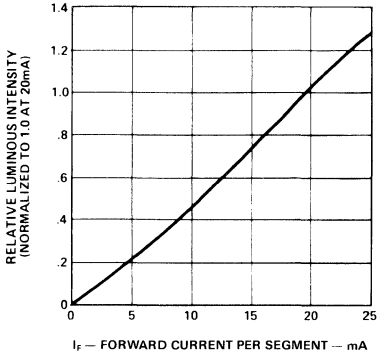


Figure 6. Relative Luminous Intensity vs. DC Forward Current – Red.

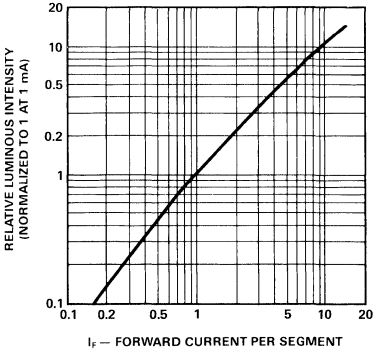


Figure 7. Relative Luminous Intensity vs. DC Forward Current – AlGaAs.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

HER, Yellow, Green

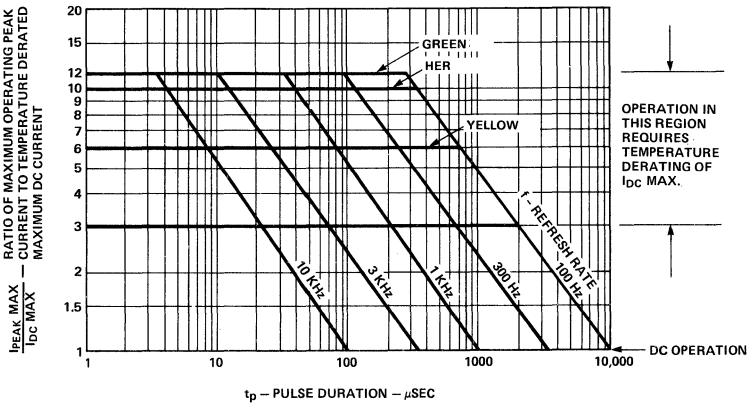


Figure 8. Maximum Tolerable Peak Current vs. Pulse Duration – HER/Yellow/Green.

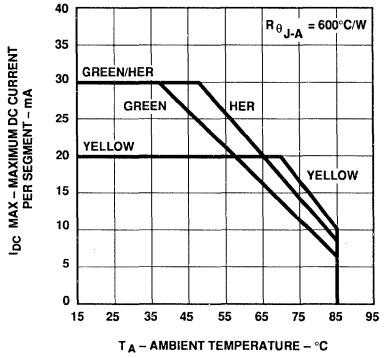


Figure 9. Maximum Allowable DC Current vs. Ambient Temperature. T_{JMAX} = 100°C.

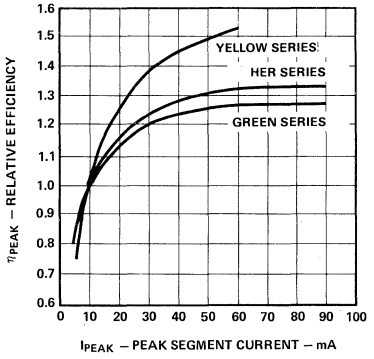


Figure 10. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

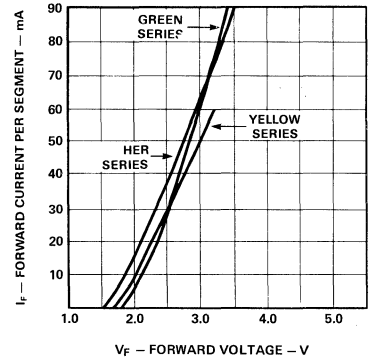


Figure 11. Forward Current vs. Forward Voltage.

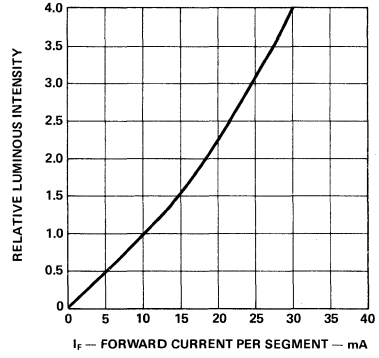


Figure 12. Relative Luminous Intensity vs. DC Forward Current.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

Electrical/Optical

These versatile bar graph arrays are composed of ten light emitting diodes. The light from each LED is optically stretched to form individual elements. The Red (HDSP-4820) bar graph array LEDs use a p-n junction diffused into a GaAsP epitaxial layer on a GaAs substrate. The AlGaAs Red (HLCP-J100) bar graph array LEDs use double heterojunction AlGaAs on a GaAs substrate. HER (HDSP-4830) and Yellow (HDSP-4840) bar graph array LEDs use a GaAsP epitaxial layer on a GaP substrate. Green (HDSP-4850) bar graph array LEDs use liquid phase GaP epitaxial layer on a GaP substrate. The multicolor bar graph arrays (HDSP-4832/4836) have HER, Yellow, and Green LEDs in one package.

These displays are designed for strobed operation. The typical forward voltage values can be scaled from Figures 5 and 11. These values should be used to calculate the current limiting resistor value and typical power consumption. Expected maximum V_F values for driver circuit design and maximum power dissipation may be calculated using the following V_FMAX models:

Standard Red HDSP-4820 series

$V_F MAX = 1.8\ V + I_{Peak}\ (10\ \Omega)$
For: $I_{Peak} \geq 5$ mA

AlGaAs Red HDSP-J100 series

$V_F MAX = 1.8\ V + I_{Peak}\ (20\ \Omega)$
For: $I_{Peak} \leq 20$ mA
$V_F MAX = 2.0\ V + I_{Peak}\ (10\ \Omega)$
For: $I_{Peak} \geq 20$ mA

HER (HDSP-4830) and Yellow (HDSP-4840) series

$V_F MAX = 1.6 + I_{Peak}\ (45\ \Omega)$
For: $5\ mA \leq I_{Peak} \leq 20$ mA
$V_F MAX = 1.75 + I_{Peak}\ (38\ \Omega)$
For: $I_{Peak} \geq 20$ mA

Green (HDSP-4850) series

$V_F MAX = 2.0 + I_{Peak}\ (50\ \Omega)$
For: $I_{Peak} > 5$ mA

Figures 4 and 10 allow the designer to calculate the luminous intensity at different peak and average currents. The following equation calculates intensity at different peak and average currents:

$$I_V AVG = (I_F AVG / I_F AVG\ DATA\ SHEET)(\eta_{peak})(I_V DATA\ SHEET)$$

Where:

I_VAVG is the calculated time averaged luminous intensity resulting from I_FAVG.

I_FAVG is the desired time averaged LED current.

I_FAVG DATA SHEET is the data sheet test current for I_VDATA SHEET.

η_{peak} is the relative efficiency at the peak current, scaled from Figure 4 or 10.

I_V DATA SHEET is the data sheet luminous intensity, resulting from I_FAVG DATA SHEET.

For example, what is the luminous intensity of an HDSP-4830 driven at 50 mA peak 1/5 duty factor?

I_FAVG = (50 mA)(0.2) = 10 mA
I_FAVG DATA SHEET = 10 mA
$\eta_{Peak} = 1.3$
I_V DATA SHEET = 3500 µcd

Therefore

I_VAVG = (10 mA/10 mA) (1.3)(3500 µcd) = 4550 µcd

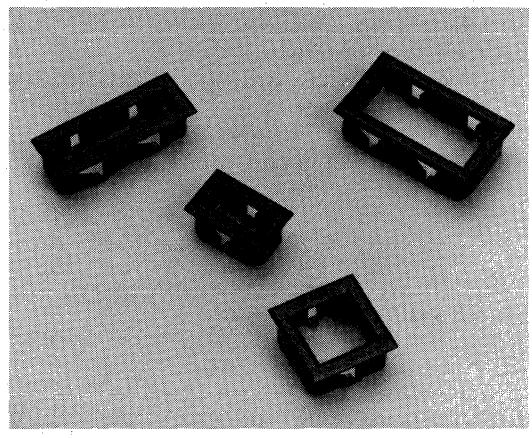
HEWLETT PACKARD

PANEL AND LEGEND MOUNTS FOR LED LIGHT BARS

HLMP-2598
HLMP-2599
HLMP-2898
HLMP-2899

Features

- **FIRMLY MOUNTS LIGHT BARS IN PANELS**
- **HOLDS LEGENDS FOR FRONT PANEL OR PC BOARD APPLICATIONS[1]**
- **ONE PIECE, SNAP-IN ASSEMBLY**
- **MATTE BLACK BEZEL DESIGN ENHANCES PANEL APPEARANCE**
- **FOUR SIZES AVAILABLE**
- **MAY BE INSTALLED IN A WIDE RANGE OF PANEL THICKNESSES**
- **PANEL HOLE EASILY PUNCHED OR MILLED**



Description

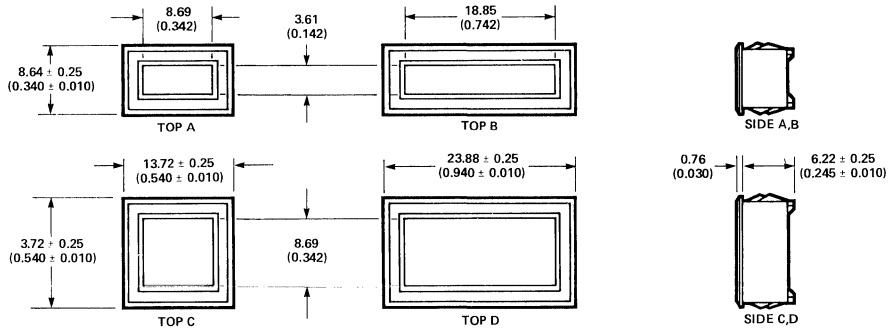
This series of black plastic bezel mounts is designed to install Hewlett-Packard Light Bars in instrument panels ranging in thickness from 1.52 mm (0.060 inch) to 3.18 mm (0.125 inch). A space has been provided for holding a 0.13 mm (0.005 inch) film legend over the light emitting surface of the light bar module.

Selection Guide

Panel and Legend Mount Part No. HLMP-	Corresponding Light Bar Module Part No. HLCP-	HLMP-	Panel Hole Installation Dimensions[2]	Package Outline	
2598	B100	2350, 2450, 2550	7.62 mm (0.300 inch) x 22.86 mm (0.900 inch)		B
2599	A100	2300, 2400, 2500	7.62 mm (0.300 inch) x 12.70 mm (0.500 inch)		A
2898	D100 C100	2600, 2700, 2800 2655, 2755, 2855 2950, 2965, 2980	12.70 mm (0.500 inch) x 12.70 mm (0.500 inch)		C
2899	E100 F100 G100 H100	2620, 2720, 2820 2635, 2735, 2835 2670, 2770, 2870 2685, 2785, 2885	12.70 mm (0.500 inch) x 22.86 mm (0.900 inch)		D

Notes:
1. Application Note 1012 addresses legend fabrication options.
2. Allowed hole tolerance: +0.00 mm, -0.13 mm (+0.000 inch, -0.005 inch). Permitted radius: 1.60 mm (0.063 inch).

Package Dimensions



NOTES: 1. DIMENSIONS IN MILLIMETRES (INCHES)
2. UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.

Mounting Instructions

1. Mill[3] or punch a hole in the panel. Deburr, but do not chamfer, the edges of the hole.
2. Place the front of the mount against a solid, flat surface. A film legend with outside dimensions equal to the outside dimensions of the light bar may be placed in the mount or on the light bar light emitting surface. Press the light bar into the mount until the tabs snap over the back of the light bar[4]. When inserting the HLMP-2898, align the notched sides of the light bar with the mount sides which do not have the tabs). (See Figure 1)
3. Applying even pressure to the top of the mount, press the entire assembly into the hole from the front of the panel[5]. (See Figure 2)

NOTE: For thinner panels, the mount may be pressed into the panel first, then the light bar may be pressed into the mount from the back side of the panel.

Notes:
3. A 3.18 mm (0.125 inch) diameter mill may be used.
4. Repetitve insertion of the light bar into mount may cause damage to the mount.
5. Repetitive insertion of the mount into the panel will degrade the retention force of the mount.

Suggested Punch Sources

Hole punches may be ordered from one of the following sources:

Danly Machine Corporation
Punchrite Division
15400 Brookpark Road
Cleveland, OH 44135
(216) 267-1444

Ring Division
The Producto Machine Company
Jamestown, NY 14701
(800) 828-2216

Porter Precision Products Company
12522 Lakeland Road
Santa Fe Springs, CA 90670
(213) 946-1531

Di-Acro Division
Houdaille Industries
800 Jefferson Street
Lake City, MN 55041
(612) 345-4571

Installation Sketches

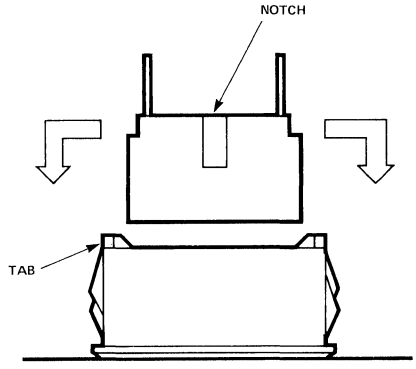


Figure 1. Installation of a Light Bar into a Panel Mount

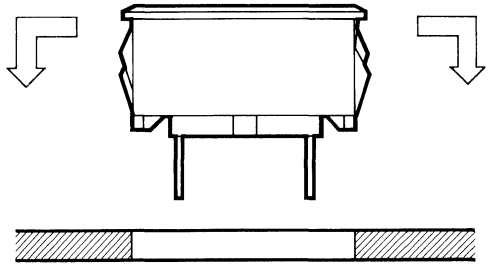
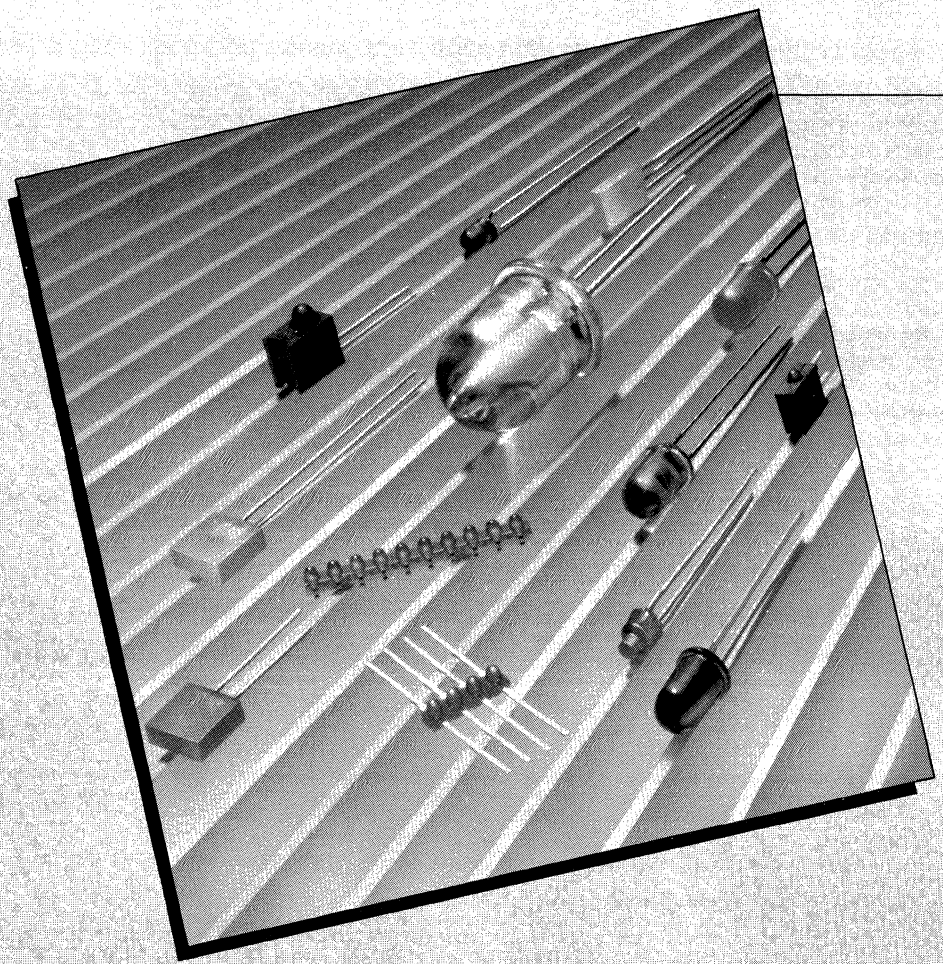


Figure 2. Installation of the Light Bar/Panel Mount Assembly into a Front Panel

HEWLETT PACKARD

Solid State Lamps

- AlGaAs Lamps
- General Purpose Lamps
- Special Purpose Lamps
- Lead Bend Options
- JAN Qualified Hermetic Lamps (pg 3-129)



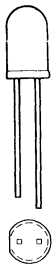
Solid State Lamps

From General to Special Purpose Lamps, Hewlett-Packard continues to grow its LED lamp product offering. This year, HP expanded the AS AlGaAs product family with the introduction of new rectangular, T1, T-1 3/4, and subminiature lamps.

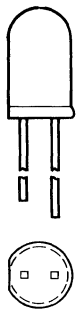
HP always strives to supply products with greater performance each year. To this effect, HP has introduced a new series of transparent substrate AlGaAs products, including the world's brightest LED, the HLMP-8150.

New packages are always an area of growth and importance to designers and Hewlett-Packard. Now, applications that require a high brightness light source can be addressed with HP's high power LED family. These LEDs have a superior optical performance due to the high tech package design. In addition, these parts are capable of being driven by higher currents than traditional LEDs and this results in more light output. Finally, designers will have a high reliability alternative to applications which traditionally required the brightness supplied by incandescent bulbs.

High Power TS AlGaAs Lamps

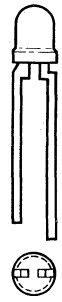
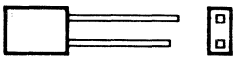
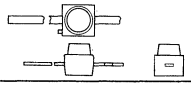
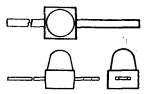
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	**HLMP-8150**	Red (637 nm)	T-4	Untinted Nondiffused	15.0 mcd @ 20 mA	4°	1.85 V @ 20 mA	3-30
	**HLMP-8104**	Red (637nm)	T-1 3/4	Untinted Nondiffused	4.0 mcd @ 20 mA	7°	1.85 V @ 20 mA	3-34
	HLMP-8103				3.0 mcd @ 20 mA			
	HLMP-8102				2.0 mcd @ 20 mA			
	HLMP-8100				0.7 mcd @ 20 mA	24°		

High Intensity DH AlGaAs Lamps

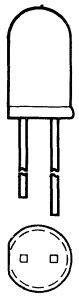
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-D101	AlGaAs Red (637 nm)	T-1 3/4	Tinted Diffused	70.0 mcd @ 20 mA	65°	1.8 V @ 20 mA	3-38
	HLMP-D105			Untinted Nondiffused	240.0 mcd @ 20 mA	24°		

Bold Type – New Product

High Intensity DH AlGaAs Lamps (Continued)

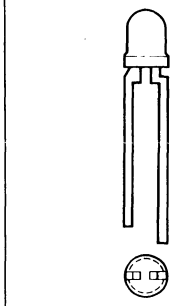
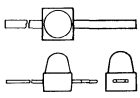
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-K101	AlGaAs Red (637 nm)	T-1	Tinted Diffused	45.0 mcd @ 20 mA	60°	1.8 V @ 20 mA	3-38
	HLMP-K105			Untinted Nondiffused	65.0 mcd @ 20 mA	45°		
	**HLMP-R100**		Rectangular	Tinted Diffused	7.5 mcd @ 20 mA	100°		3-83
	**HLMP-S100**		2 mm x 5 mm Rectangular		7.5 mcd @ 20 mA	110°		3-87
	**HLMP-P105**		Flat Top Subminiature	Untinted Nondiffused	10.0 mcd @ 10 mA	125°	1.7 V @ 10 mA	3-91
	HLMP-Q101		Subminiature	Tinted Diffused	45.0 mcd @ 20 mA	70°	1.8 V @ 20 mA	
	HLMP-Q105			Untinted Nondiffused	55.0 mcd @ 10 mA	28°	1.7 V @ 10 mA	

Low Current DH AlGaAs Lamps

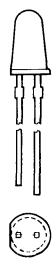
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-D150	AlGaAs Red (637 nm)	T-1 3/4	Tinted Diffused	3.0 mcd @ 1 mA	65°	1.6 V @ 1 mA	3-42
	HLMP-D155			Untinted Nondiffused	10.0 mcd @ 1 mA	24°		

Bold Type – New Product

Low Current DH AlGaAs Lamps (Continued)

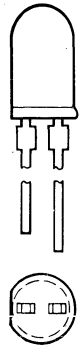
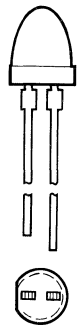
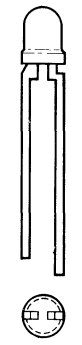
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-K150	AlGaAs Red (637 nm)	T-1	Tinted Diffused	2.0 mcd @ 1 mA	60°	1.6 V @ 1 mA	3-42
	HLMP-K155			Untinted Nondiffused	3.0 mcd @ 1 mA	45°		
	HLMP-Q150		Subminiature	Tinted Diffused	1.8 mcd @ 1 mA	70°	1.6 V @ 1 mA	3-91
	HLMP-Q155			Untinted Nondiffused	4.0 mcd @ 1.0 mA	28°		

Very High Intensity AlGaAs Lamps

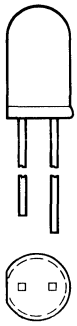
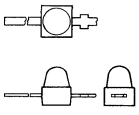
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-4100	AlGaAs Red (637 nm)	T-1 3/4	Untinted Nondiffused	750.0 mcd @ 20 mA	8°	1.8 V @ 20 mA	3-46
	HLMP-4101				1000.0 mcd @ 20 mA			

Bold Type – New Product

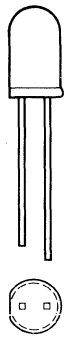
Ultrabright Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-3750	High Efficiency Red (626 nm)	T-1 3/4	Untinted Non-diffused	125.0 mcd @ 20 mA	24°	2.2 V @ 20 mA	3-50
	HLMP-3850	Yellow (585 nm)			140.0 mcd @ 20 mA		2.2 V @ 20 mA	
	HLMP-3950	Green (569 nm)			120.0 mcd @ 20 mA		2.3 V @ 20 mA	
	HLMP-3390	High Efficiency Red (626 nm)	T-1 3/4 Low Profile	Untinted Non-diffused	55.0 mcd @ 20 mA	32°	2.2 V @ 20 mA	
	HLMP-3490	Yellow (585 nm)					2.2 V @ 20 mA	
	HLMP-3590	Green (569 nm)					2.3 V @ 20 mA	
	HLMP-1340	High Efficiency Red (626 nm)	T-1	Untinted Non-diffused	45.0 mcd @ 20 mA	45°	2.2 V @ 20 mA	
	HLMP-1440	Yellow (585 nm)					2.2 V @ 20 mA	
	HLMP-1540	Green (569 nm)					2.3 V @ 20 mA	

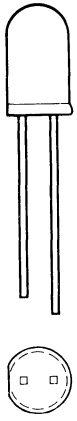
Low Current Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-4700	High Efficiency Red (626 nm)	T-1 3/4	Tinted Diffused	2.0 mcd @ 2 mA	50°	1.8 V @ 2 mA	3-54
	HLMP-4719	Yellow (585 nm)			1.8 mcd @ 2 mA		1.9 V @ 2 mA	
	HLMP-4740	Green (569 nm)			1.8 mcd @ 2 mA		1.8 V @ 2 mA	
	HLMP-1700	High Efficiency Red (626 nm)	T-1	Tinted Diffused	1.8 mcd @ 2 mA	50°	1.8 V @ 2 mA	
	HLMP-1719	Yellow (585 nm)			1.6 mcd @ 2 mA		1.9 V @ 2 mA	
	HLMP-1790	Green (569 nm)			1.6 mcd @ 2 mA		1.8 V @ 2 mA	
	HLMP-7000	High Efficiency Red (626 nm)	Subminiature	Tinted Diffused	0.8 mcd @ 2 mA	90°	1.8 V @ 2 mA	3-91
	HLMP-7019	Yellow (585 nm)			0.6 mcd @ 2 mA		1.9 V @ 2 mA	
	HLMP-7040	Green (569 nm)			0.6 mcd @ 2 mA		1.8 V @ 2 mA	

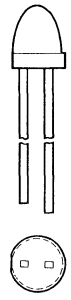
High Intensity T-1 3/4 Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-3315	High Efficiency Red (626 nm)	T-1 3/4	Tinted Nondiffused	40.0 mcd @ 10 mA	35°	2.2 V @ 10 mA	3-58
	HLMP-3316				60.0 mcd @ 10 mA			
	HLMP-3415	Yellow (585 nm)			40.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-3416				50.0 mcd @ 10 mA			
	HLMP-3517	Green (569 nm)			50.0 mcd @ 10 mA	24°	2.3 V @ 10 mA	
	HLMP-3519				70.0 mcd @ 10 mA			

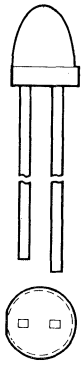
Diffused (Wide Angle) T-1 3/4 Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-3300	High Efficiency Red (626 nm)	T-1 3/4		3.5 mcd @ 10 mA	60°	2.2 V @ 10 mA	3-62
	HLMP-3301				7.0 mcd @ 10 mA			
	HLMP-3762				12.0 mcd @ 10 mA			
	HLMP-D400	Orange (602 nm)			3.5 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-D401				7.0 mcd @ 10 mA			
	HLMP-3400	Yellow (585 nm)			4.0 mcd @ 10 mA	60°	2.2 V @ 10 mA	
	HLMP-3401				8.0 mcd @ 10 mA			
	HLMP-3862				12.0 mcd @ 10 mA			
	HLMP-3502	Green (569 nm)			2.4 mcd @ 10 mA	60°	2.3 V @ 10 mA	
	HLMP-3507				5.2 mcd @ 10 mA			
	HLMP-3962				11.0 mcd @ 10 mA			

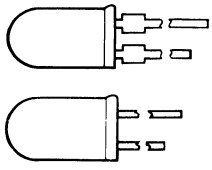
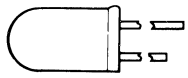
High Intensity T-1 3/4 Low Profile Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-3365	High Efficiency Red (626 nm)	T-1 3/4 Low Profile	Tinted Non-Diffused	10.0 mcd @ 10 mA	45°	2.2 V @ 10 mA	3-66
	HLMP-3366				18.0 mcd @ 10 mA			
	HLMP-3465	Yellow (585 nm)			12.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-3466				18.0 mcd @ 10 mA			
	HLMP-3567	Green (569 nm)			7.0 mcd @ 10 mA	40°	2.3 V @ 10 mA	
	HLMP-3568				15.0 mcd @ 10 mA			

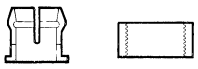
Diffused (Wide Angle) T-1 3/4 Low Profile Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-3200	Red (640 nm)	T-1 3/4 Low Profile	Tinted Diffused	2.0 mcd @ 20 mA	60°	1.6 V @ 20 mA	3-66
	HLMP-3201				4.0 mcd @ 20 mA			
	HLMP-3350	High Efficiency Red (626 nm)			3.5 mcd @ 10 mA	50°	2.2 V @ 10 mA	
	HLMP-3351				7.0 mcd @ 10 mA			
	HLMP-3450	Yellow (585 nm)			4.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-3451				10.0 mcd @ 10 mA			
	HLMP-3553	Green (569 nm)			3.2 mcd @ 10 mA		2.3 V @ 10 mA	
	HLMP-3554				10.0 mcd @ 10 mA			

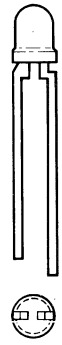
Standard Red T-1 3/4 Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-3000	Red (648 nm)	T-1 3/4	Tinted Diffused	2.0 mcd @ 20 mA	60°	1.6 V @ 20 mA	3-71
	HLMP-3001				4.0 mcd @ 20 mA			
	HLMP-3002				2.0 mcd @ 20 mA			
	HLMP-3003				4.0 mcd @ 20 mA			
	HLMP-3050			Tinted Non-Diffused	2.5 mcd @ 20 mA	24°		

T-1 3/4 Mounting Hardware

Device		Description	Page No.
Package Outline Drawing	Part No.		
	HLMP-0103	Mounting Clip and Ring for T-1 3/4 Lamps	3-128

T-1 High Intensity Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-1320	High Efficiency Red (626 nm)	T-1	Untinted Nondiffused	12.0 mcd @ 10 mA	45°	2.2 V @ 10 mA	3-73
	HLMP-1321			Tinted Nondiffused				
	HLMP-1420	Yellow (585 nm)		Untinted Nondiffused	12.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-1421			Tinted Nondiffused				
	HLMP-1520	Green (569 nm)		Untinted Nondiffused	12.0 mcd @ 10 mA		2.3 V @ 10 mA	
	HLMP-1521			Tinted Nondiffused				

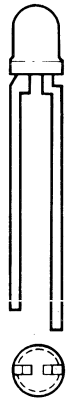
T-1 Diffused (Wide Angle) Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-1300	High Efficiency Red (626 nm)	T-1	Tinted Diffused	5.0 mcd @ 10 mA	60°	2.2 V @ 10 mA	3-77
	HLMP-1301				5.5 mcd @ 10 mA			
	HLMP-1302				7.0 mcd @ 10 mA			
	HLMP-1385				10.0 mcd @ 10 mA			
	HLMP-K400	Orange (602 nm)			4.0 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-K401				5.0 mcd @ 10 mA			
	HLMP-K402				6.5 mcd @ 10 mA			

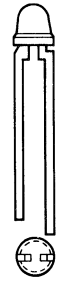
T-1 Diffused (Wide Angle) Lamps (Continued)

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-1400	Yellow (585 nm)	T-1	Tinted Diffused	5.0 mcd @ 10 mA	60°	2.2 V @ 10 mA	3-77
	HLMP-1401				6.0 mcd @ 10 mA			
	HLMP-1402				7.0 mcd @ 10 mA			
	HLMP-1485				10.0 mcd @ 10 mA			
	HLMP-1503	Green (569 nm)			5.0 mcd @ 10 mA		2.3 V @ 10 mA	
	HLMP-1523				7.0 mcd @ 10 mA			
	HLMP-1585				8.5 mcd @ 10 mA			

T-1 Standard Red Lamps

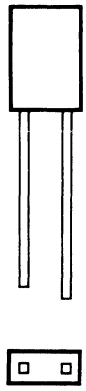
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-1000	Red (648 nm)	T-1	Tinted Diffused	1.0 mcd @ 20 mA	60°	1.6 V @ 20 mA	3-81
	HLMP-1002				2.5 mcd @ 20 mA			
	HLMP-1080			Untinted Diffused	1.5 mcd @ 20 mA			
	HLMP-1071			Untinted Non-Diffused	2.0 mcd @ 20 mA	45°	1.6 V @ 20 mA	
	HLMP-1200		T-1 Low Profile	Untinted Non-Diffused	1.0 mcd @ 20 mA	55°	1.6 V @ 20mA	
	HLMP-1201				2.5 mcd @ 20 mA			

T-1 Low Profile Diffused Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-1350	High Efficiency Red (626 nm)	T-1 Low Profile	Tinted Diffused	2.0 mcd @ 10 mA	55°	2.2 V @ 10 mA	*
	HLMP-1450	Yellow (585 nm)					2.2 V @ 10 mA	
	HLMP-1550	Green (569 nm)					2.3 V @ 10 mA	

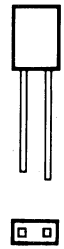
*Contact your local Sales Representative for information regarding this product. (See Section 9.)

Rectangular Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	**HLMP-R100**	DH AlGaAs Red (637 nm)	Rectangular	Tinted Diffused	7.5 mcd @ 20 mA	100°	1.8 V @ 20 mA	3-83
	HLMP-0300	High Efficiency Red (626 nm)			2.5 mcd @ 20 mA		2.2 V @ 20 mA	
	HLMP-0301				5.0 mcd @ 20 mA			
	HLMP-0400	Yellow (585 nm)			2.5 mcd @ 20 mA		2.2 V @ 20 mA	
	HLMP-0401				5.0 mcd @ 20 mA			
	HLMP-0503	Green (569 nm)			2.5 mcd @ 20 mA		2.3 V @ 20 mA	
	HLMP-0504				5.0 mcd @ 20 mA			

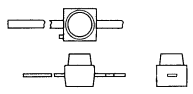
Bold Type – New Product

2 mm x 5 mm Rectangular Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	**HLMP-S100**	DH AlGaAs Red (637 nm)	2 mm x 5 mm Rectangular	Tinted Diffused	7.5 mcd @ 20 mA	110°	1.8 V @ 20 mA	3-87
	HLMP-S200	High Efficiency Red (626 nm)			3.5 mcd @ 20 mA		2.2 V @ 20 mA	
	HLMP-S201				4.8 mcd @ 20 mA			
	HLMP-S400	Orange (602 nm)			3.5 mcd @ 20 mA		2.2 V @ 20 mA	
	HLMP-S401				4.8 mcd @ 20 mA			
	HLMP-S300	Yellow (585 nm)			2.1 mcd @ 20 mA		2.2 V @ 20 mA	
	HLMP-S301				3.5 mcd @ 20 mA			
	HLMP-S500	Green (569 nm)			4.0 mcd @ 20 mA		2.3 V @ 20 mA	
	HLMP-S501				5.8 mcd @ 20 mA			

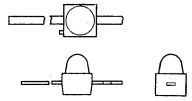
Bold Type – New Product

Subminiature Flat Top Lamps

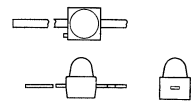
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	**HLMP-P005**	Standard Red (640 nm)	Flat Top Subminiature	Untinted Non-diffused	2.5 mcd @ 10 mA	125°	1.6 V @ 10 mA	3-91
	HLMP-P105	DH AlGaAs Red (637 nm)			45.0 mcd @ 20 mA		1.8 V @ 20 mA	
	HLMP-P205	High Efficiency Red (626 nm)			5.0 mcd @ 10 mA		1.8 V @ 10 mA	
	HLMP-P405	Orange (602 nm)			4.0 mcd @ 10 mA		1.9 V @ 10 mA	
	HLMP-P305	Yellow (585 nm)			4.0 mcd @ 10 mA		2.0 V @ 10 mA	
	HLMP-P505	Green (569 nm)			5.0 mcd @ 10 mA		2.0 V @ 10 mA	

Bold Type – New Product

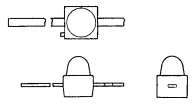
Subminiature Diffused Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-6000	Standard Red (640 nm)	Subminiature	Tinted Diffused	1.2 mcd @ 10 mA	90°	1.6 V @ 10 mA	3-91
	HLMP-6001				3.2 mcd @ 10 mA		1.6 V @ 10 mA	
	HLMP-Q101	DH AlGaAs Red (637 nm)			45.0 mcd @ 20 mA		1.8 V @ 20 mA	
	HLMP-6300	High Efficiency Red (626 nm)			3.0 mcd @ 10 mA		1.8 V @ 10 mA	
	HLMP-Q400	Orange (602 nm)			3.0 mcd @ 10 mA		1.9 V @ 10 mA	
	HLMP-6400	Yellow (585 nm)			3.0 mcd @ 10 mA		2.0 V @ 10 mA	
	HLMP-6500	Green (569 nm)			3.0 mcd @ 10 mA		2.0 V @ 10 mA	

Subminiature Nondiffused Lamps

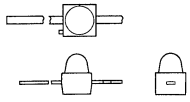
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-Q105	DH AlGaAs Red (637 nm)	Subminiature	Untinted Non-diffused	55.0 mcd @ 20 mA	28°	1.8 V @ 20 mA	3-91
	HLMP-6305	High Efficiency Red (626 nm)			12.0 mcd @ 10 mA		1.8 V @ 10 mA	
	HLMP-6405	Yellow (585 nm)			12.0 mcd @ 10 mA		2.0 V @ 10 mA	
	HLMP-6505	Green (569 nm)			12.0 mcd @ 10 mA		2.0 V @ 10 mA	

Subminiature Low Current Lamps

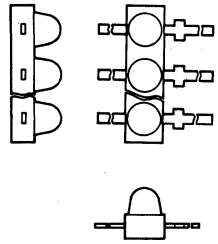
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-Q150	DH AlGaAs Red (637 nm)	Subminiature	Tinted Diffused	1.8 mcd @ 1.0 mA	90°	1.6 V @ 1.0 mA	3-91
	HLMP-Q155			Untinted Nondiffused	4.0 mcd @ 1.0 mA	28°		
	HLMP-7000	High Efficiency Red (626 nm)		Tinted Diffused	0.8 mcd @ 2.0 mA	90°	1.8 V @ 10.0 mA	
	HLMP-7019	Yellow (585 nm)			0.6 mcd @ 2.0 mA		2.0 V @ 10.0 mA	
	HLMP-7040	Green			0.6 mcd		2.0 V @	

Bold Type – New Product

Subminiature Resistor Lamps

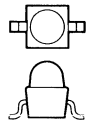
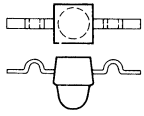
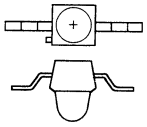
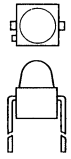
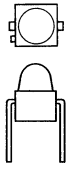
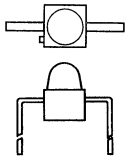
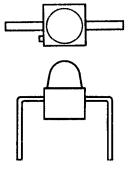
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Current	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-6600	High Efficiency Red (626 nm)	Subminiature Resistor	Tinted Diffused	5.0 mcd @ 5.0 V	90°	9.6 mA @ 5.0 V	3-91
	HLMP-6620				2.0 mcd @ 5.0 V		3.5 mA @ 5.0 V	
	HLMP-6700	Yellow (585 nm)			5.0 mcd @ 5.0 V		9.6 mA @ 5.0 V	
	HLMP-6720				2.0 mcd @ 5.0 V		3.5 mA @ 5.0 V	
	HLMP-6800	Green (569 nm)			5.0 mcd @ 5.0 V		9.6 mA @ 5.0 V	
	HLMP-6820				2.0 mcd @ 5.0 V		3.5 mA @ 5.0 V	

Subminiature Lamp Arrays

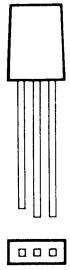
Device		Description				Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package		Lens				
	HLMP-6203 HLMP-6204 HLMP-6205 HLMP-6206 HLMP-6208	Red (640 nm)	Array †	3 4 5 6 8	Tinted Diffused	1.2 mcd @ 10 mA	90°	1.6 V @ 10 mA	3-91
	HLMP-6653 HLMP-6654 HLMP-6655 HLMP-6656 HLMP-6658	High Efficiency Red (626 nm)		3 4 5 6 8		3.0 mcd @ 10 mA		1.8 V @ 10 mA	
	HLMP-6753 HLMP-6754 HLMP-6755 HLMP-6756 HLMP-6758	Yellow (585 nm)		3 4 5 6 8				2.0 V @ 10 mA	
	HLMP-6853 HLMP-6854 HLMP-6855 HLMP-6856 HLMP-6858	Green (569 nm)		3 4 5 6 8				2.0 V @ 10 mA	

†Array length

Lead Bend Options, Subminiature Lamps

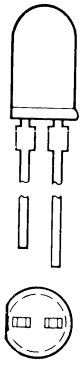
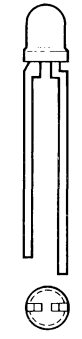
Device		Description	Page No.
Package Outline Drawing	Option No.		
	011	Gull Wing, Tape and Reel, 1500 Lamps per Reel	3-91
	012	Gull Wing, Bulk Packaging	
	013	Gull Wing Array, Shipping Tube	
	021	Yoke Lead, Tape and Reel, 1500 Lamps per Reel	
	022	Yoke Lead, Bulk Packaging	
	031	Z-Bend, Tape and Reel, 1500 Lamps per Reel	
	032	Z-Bend, Bulk Packaging	
	1L1	2.54 mm (0.100 in) Rt. Angle Bend, Long Leads	
	1S1	2.54 mm (0.100 in) Rt. Angle Bend, Short Leads	
	2L1	5.08 mm (0.200 in) Rt. Angle Bend, Long Leads	
	2S1	5.08 mm (0.200 in) Rt. Angle Bend, Short Leads	

Bicolor Solid State Lamps

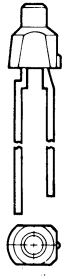
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	**HLMP-0800**	High Efficiency Red (626 nm)	2 mm x 5 mm Rectangular	Untinted Diffused	3.5 mcd @ 20 mA	100°	2.1 V @ 10 mA	3-111
		Green (569 nm)			4.0 mcd @ 20 mA		2.3 V @ 10 mA	
	HLMP-4000	High Efficiency Red (626 nm)	T-1 3/4	Untinted Diffused	5.0 mcd @ 10 mA	65°	2.1 V @ 10 mA	
		Green (569 nm)			8.0 mcd @ 10 mA		2.3 V @ 10 mA	

Bold Type – New Product

T-1 3/4 and T-1 Integrated Resistor Lamps

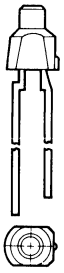
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Current	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-3105	Red (648 nm)	T-1 3/4	Tinted Diffused	3.0 mcd @ 5 V	60°	13 mA @ 5 V	3-115
	HLMP-3112				3.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-3600	High Efficiency Red (626 nm)			8.0 mcd @ 5 V		10 mA @ 5 V	
	HLMP-3601				8.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-3650	Yellow (585 nm)			8.0 mcd @ 5 V		10 mA @ 5 V	
	HLMP-3651				8.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-3680	Green (569 nm)			8.0 mcd @ 5 V		12 mA @ 5 V	
	HLMP-3681				8.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-1100	Red (648 nm)	T-1	Tinted Diffused	2.5 mcd @ 5 V	60°	13 mA @ 5 V	
	HLMP-1120			Untinted Diffused				
	HLMP-1600	High Efficiency Red (626 nm)		Tinted Diffused	8.0 mcd @ 5 V		10 mA @ 5 V	
	HLMP-1601				8.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-1620	Yellow (585 nm)			8.0 mcd @ 5 V		10 mA @ 5 V	
	HLMP-1621				8.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-1640	Green (569 nm)			8.0 mcd @ 5 V		12 mA @ 5 V	
	HLMP-1641				8.0 mcd @ 12 V		13 mA @ 12 V	

2 mm Round Flat Top Lamps

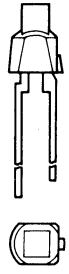
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-1800	High Efficiency Red (626 nm)	2 mm Flat Top, Round Emitting Surface	Tinted Diffused	1.8 mcd @ 10 mA	140°	2.2 V @ 10 mA	*
	HLMP-1801				2.9 mcd @ 10 mA			
	HLMP-1819	Yellow (585 nm)			1.5 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-1820				2.5 mcd @ 10 mA			
	HLMP-1840	Green (569 nm)			2.0 mcd @ 10 mA		2.3 V @ 10 mA	
	HLMP-1841				3.0 mcd @ 10 mA			
	HLMP-1740 (Low Current)	High Efficiency Red (626 nm)			0.5 mcd @ 2 mA		1.8 V @ 2 mA	
	HLMP-1760 (Low Current)	Yellow (585 nm)			0.4 mcd @ 2 mA		1.9 V @ 2 mA	

*Contact your local Sales Representative for information regarding this product. (See Section 9.)

2 mm Round Integrated Resistor Lamps

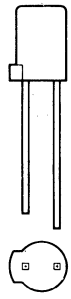
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-1660	High Efficiency Red (626 nm)	2 mm Flat Top, Round Emitting Surface	Tinted Diffused	1.0 mcd @ 5 V	140°	10 mA @ 5 V	*
	HLMP-1661				1.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-1674	Yellow (585 nm)			1.0 mcd @ 5 V		10 mA @ 5 V	
	HLMP-1675				1.0 mcd @ 12 V		13 mA @ 12 V	
	HLMP-1687	Green (569 nm)			1.0 mcd @ 5 V		10 mA @ 5 V	
	HLMP-1688				1.0 mcd @ 12 V		13 mA @ 12 V	

2 mm Square Flat Top Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-L250	High Efficiency Red (626 nm)	2 mm Flat Top, Square Emitting Surface	Tinted Diffused	1.8 mcd @ 10 mA	140°	2.2 V @ 10 mA	*
	HLMP-L251				2.9 mcd @ 10 mA			
	HLMP-L350	Yellow (585 nm)			1.5 mcd @ 10 mA		2.2 V @ 10 mA	
	HLMP-L351				2.5 mcd @ 10 mA			
	HLMP-L550	Green (569 nm)			2.0 mcd @ 10 mA		2.3 V @ 10 mA	
	HLMP-L551				3.0 mcd @ 10 mA			

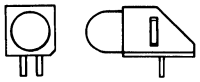
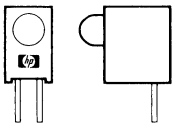
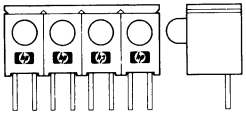
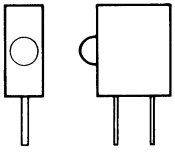
*Contact your local Sales Representative for information regarding this product. (See Section 9.)

4 mm Round Flat Top Lamps

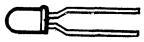
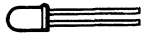
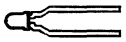
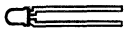
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-M200	High Efficiency Red (626 nm)	4 mm Flat Top	Tinted Diffused	5.0 mcd @ 20 mA	135°	2.2 V @ 10 mA	*
	HLMP-M201				7.0 mcd @ 20 mA			
	HLMP-M250			Tinted Non-Diffused	5.0 mcd @ 10 mA	80°		
	HLMP-M251				7.0 mcd @ 10 mA			
	HLMP-M300	Yellow (585 nm)		Tinted Diffused	5.0 mcd @ 20 mA	135°	2.2 V @ 10 mA	
	HLMP-M301				7.0 mcd @ 20 mA			
	HLMP-M350			Tinted Non-Diffused	5.0 mcd @ 10 mA	80°		
	HLMP-M351				7.0 mcd @ 10 mA			
	HLMP-M500	Green (569 nm)		Tinted Diffused	7.0 mcd @ 20 mA	135°	2.3 V @ 10 mA	
	HLMP-M501				10.0 mcd @ 20 mA			
	HLMP-M550			Tinted Non-Diffused	10.0 mcd @ 10 mA	80°		
	HLMP-M551				16.0 mcd @ 10 mA			

*Contact your local Sales Representative for information regarding this product. (See Section 9.)

Right Angle Lamp Options

Device		Description	Page No.
Package Outline Drawing	Option No.		
	010	T-1 3/4 Rt. Angle, Leads Sheared Even	3-123
	100	T-1 3/4 Rt. Angle, Leads Sheared Uneven	
	101	T-1 Rt. Angle, Leads Sheared Even	3-125
	010	T-1 Rt. Angle, Leads Sheared Uneven	
	102	T-1 Rt. Angle, 2 Element Array	3-126
	103	T-1 Rt. Angle, 3 Element Array	
	104	T-1 Rt. Angle, 4 Element Array	
	105	T-1 Rt. Angle, 5 Element Array	
	106	T-1 Rt. Angle, 6 Element Array	
	107	T-1 Rt. Angle, 7 Element Array	
	108	T-1 Rt. Angle, 8 Element Array	
	010	Subminiature Rt. Angle, Leads Sheared Even	3-127

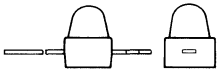
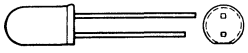
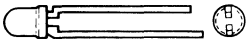
Tape and Reel Lamp Options

Device		Description	Page No.
Package Outline Drawing	Option No.		
	001	T-1 3/4, 5 mm (0.197 in) Formed Leads, 1300 Lamps per Reel	3-119
	002	T-1 3/4, 2.54 mm (0.100 in) Formed Leads, 1300 Lamps per Reel	
	001	T-1, 5 mm (0.197 in) Formed Leads, 1800 Lamps per Reel	
	002	T-1, 2.54 mm (0.100 in) Formed Leads, 1800 Lamps per Reel	

Intensity Selected Lamps

Device		Description	Page No.
Package Outline Drawing	Option No.		
	S02	This option provides the selection of lamps from two adjacent luminous intensity categories	*

Emitter Components

Device		Description	Features	Page No.
Package Outline Drawing	Part No.			
	HEMT-6000	700 nm High Intensity Subminiature Emitter	• Visible (Near IR) emission facilitates alignment. • Compatible with most silicon phototransistors and photodiodes.	*
	HEMT-3301	940 nm T-1 3/4 High Radiant Emitter	• Efficiency at Low Currents • Radiated spectrum matches response of silicon photodetectors • Non-saturated, high radiant flux output	
	HEMT-1001	940 nm T-1 High Radiant Emitter		

T-1 3/4 Mounting Hardware

Device		Description	Page No.
Package Outline Drawing	Part No.		
	HLMP-5029	Right Angle Housing for T-1 3/4 Lamps	*

*Contact your local Sales Representative for information regarding this product. (See Section 9.)

Hermetic Lamps Selection Gude (see page 3-131).

HEWLETT PACKARD

High Power T - 4 (13.3 mm) TS AlGaAs Red Lamp

Technical Data

HLMP-8150 15 Candela

Features

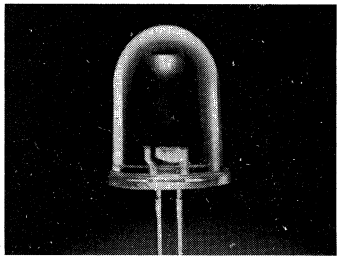
- **15 Candelas at 20 mA**
- **Outstanding LED Material Efficiency**
- **High Light Output Over a Wide Range of Drive Currents**
- **4° Viewing Angle**
- **Low Forward Voltage**
- **Low Power Dissipation**
- **CMOS/MOS Compatible**
- **Red Color**

Applications

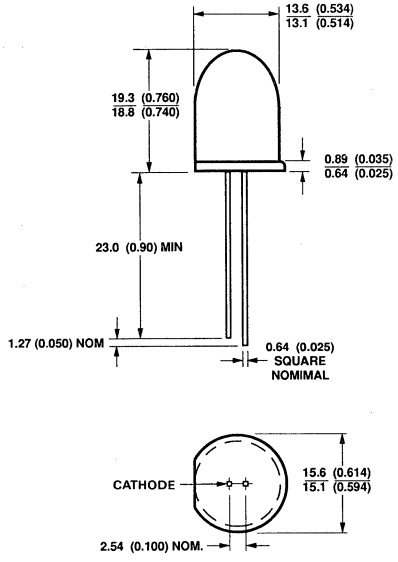
- **Emitter for Emitter/ Detector Applications**
- **Power Signaling**
- **Bright Ambient Lighting Conditions**
- **Bar Code Readers**
- **Replacement for a Low Power Laser**

Description

This untinted, nondiffused solid state lamp utilizes a highly optimized LED material, transparent substrate aluminum gallium arsenide, TS AlGaAs. This material has outstanding light output efficiency over a wide range of currents, and has superior high current capability to most other LED materials. The lamp design utilizes advanced optical methods to enable extremely high peak intensity and a very narrow viewing angle. The LED color is red at a dominant wavelength of 637 nm.



Package Dimensions



Notes:
1. All dimensions are in millimetres (inches).
2. The leads are mild steel. solder dipped.
3. An epoxy meniscus may extend about 1 mm (0.040 ") down the leads.

Axial Luminous Intensity and Viewing Angle at T_A = 25°C

Minimum Intensity (cd) @ 20 mA	Typical Intensity (cd) @ 20 mA	Maximum Intensity (cd) @ 20 mA	Typical Radiant Intensity (mW/sr) @ 20 mA	$2\theta_{1/2}$ [1] (degrees)
8.0	15.0	36.0	176	4.0

Note. 1. $\theta_{1/2}$ is the off axis angle from optical centerline where the luminous intensity is 1/2 the on-axis value.

Absolute Maximum Ratings at T_A = 25 °C

Peak Forward Current[1, 2] ..... 300 mA
Average Forward Current (@ I_{PEAK}=300 mA)[2] ..... 15 mA
DC Forward Current[3] ..... 50 mA
Power Dissipation ..... 130 mW
Reverse Voltage (I_R=100 μA) ..... 8 V
Transient Forward Current (10 μs Pulse)[4] ..... 500 mA
Operating Temperature Range ..... -55 to +100°C
Storage Temperature Range ..... -55 to +100°C
Lead Soldering Temperature
[1.6 mm (0.063 in.) from body] ..... 260°C for 5 seconds

Notes:
1. Maximum I_{PEAK} at f = 1 kHz, DF = 5%.
2. Refer to Figure 6 to establish pulsed operating conditions.
3. Derate linearly as shown in Figure 5.
4. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bonds. It is not recommended that the device be operated at peak currents above the Absolute Maximum Peak Forward Current.

Electrical/Optical Characteristics at T_A = 25 °C

Description	Symbol	Min	Typ	Max	Units	Test Condition
Forward Voltage	V_F		1.85	2.4	V	I_F = 20 mA
Reverse Voltage	V_R	8.0	20.0		V	I_R = 100 μA
Peak Wavelength	λ_{PEAK}		650		nm	
Dominant Wavelength [1]	λ_d		637		nm	
Spectral Line Halfwidth	$\Delta\lambda 1/2$		22		nm	
Speed of Response	τ_S		45		ns	Exponential Time Constant, e^{-t/τ_S}
Capacitance	C		20		pF	V_F = 0, f = 1 MHz
Thermal Resistance	$R\theta_{J\text{-}PIN}$		220		°C/W	Junction-to-Anode Lead
Luminous Efficacy [2]	η_v		85		lm/W	

Notes:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the color of the device.
2. The radiant intensity, I_e, in watts per steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is luminous efficacy in lumens/watt.
3. The approximate total luminous flux output within a cone angle of 2θ about the optical axis may be obtained from the following formula:
   $\phi_v 2(\theta) = [\phi_v(\theta)/I_v(0)]I_v$;
   Where: $\phi_v(\theta)/I_v(0)$ is obtained from Figure 7.

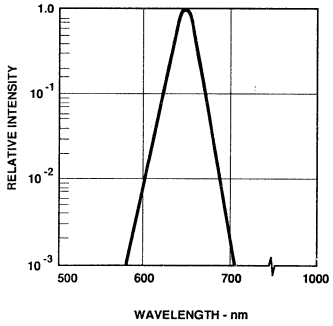


Figure 1. Relative Intensity vs. Wavelength.

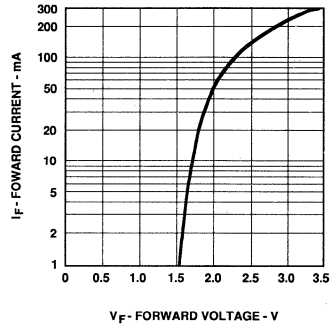


Figure 2. Forward Current vs. Forward Voltage.

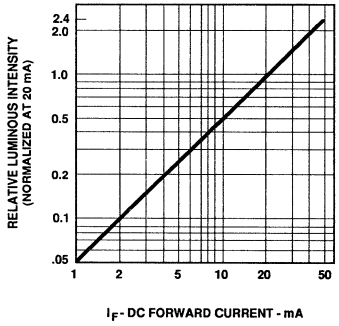


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

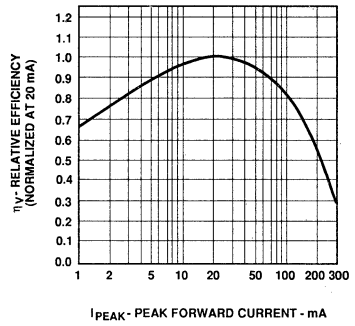


Figure 4. Relative Efficiency vs. Peak Forward Current.

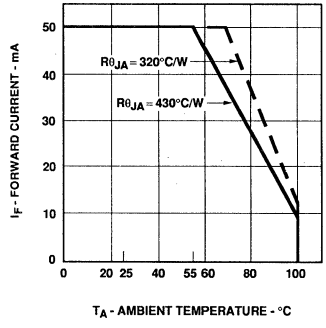


Figure 5. Maximum Forward DC Current vs. Ambient Temperature.
Derating Based on T_JMAX = 110°C.

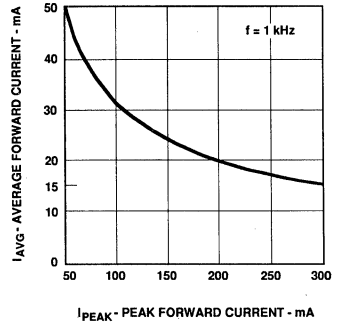


Figure 6. Maximum Average Current vs. Peak Forward Current. Refresh Rate = 1 kHz.

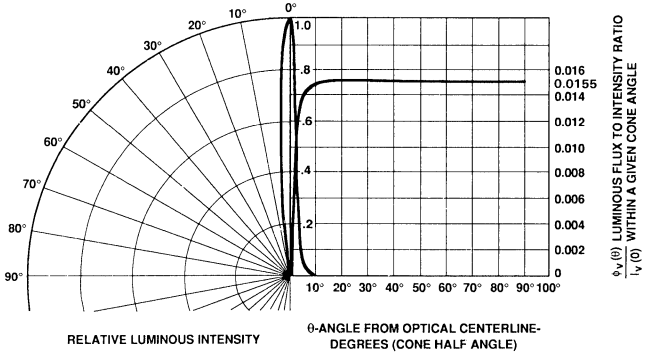


Figure 7. Relative Luminous Intensity vs. Angular Displacement, HLMP-8150.

HEWLETT PACKARD

High Power T-1 3/4 (5 mm) TS AlGaAs Red Lamps

Technical Data

HLMP-8104 4 Candela
HLMP-8103 3 Candela
HLMP-8102 2 Candela
HLMP-8100 Wide Angle

Features

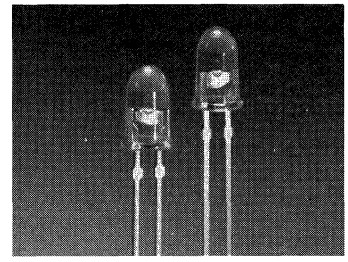
- **Exceptional Brightness**
- **Outstanding LED Material Efficiency**
- **High Light Output Over a Wide Range of Drive Currents**
- **Viewing Angle: Narrow or Wide**
- **Low Forward Voltage**
- **Low Power Dissipation**
- **CMOS/MOS Compatible**
- **Red Color**

Applications

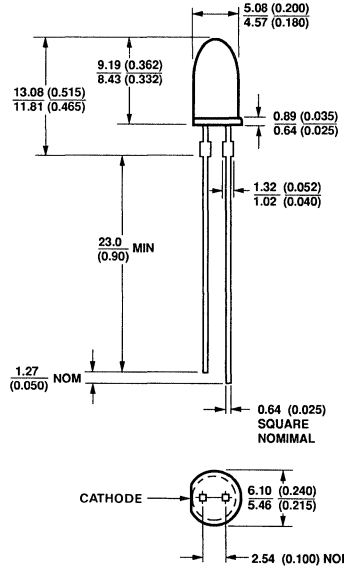
- **Signaling Applications**
- **Emitter for Emitter/ Detector Applications**
- **Moving Message Signs**
- **Bright Ambient Lighting Conditions**
- **Automotive Lighting**
- **Medical Instruments**
- **Bar Code Readers**
- **Low Power Laser Replacement**
- **Alternative to Incandescent Lighting**

Description

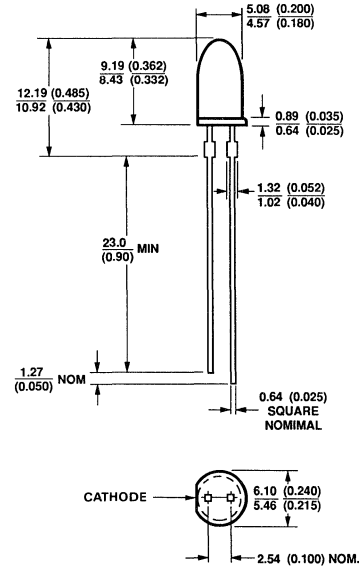
These untinted, nondiffused solid state lamps utilize a highly optimized LED material, transparent substrate aluminum gallium arsenide, TS AlGaAs. This material has outstanding light output efficiency over a wide range of currents, and has superior high current capability compared to most other LED materials. The lamp design utilizes advanced optical methods to enable extremely high peak intensity and a very narrow viewing angle. The LED color is red at a dominant wavelength of 637 nm.



Package Dimensions



HLMP-8104/8103/8102



HLMP-8100

Notes: 1. All Dimensions are in millimetres (inches).
2. The leads are mild steel. solder dipped.
3. An epoxy meniscus may extend about 1 mm (0.040 ") down the leads.

Axial Luminous Intensity and Viewing Angle at T_A= 25 °C

Part Number HLMP-	Minimum Intensity (cd) @ 20 mA	Typical Intensity (cd) @ 20 mA	Maximum Intensity (cd) @ 20 mA	Typical Radiant Intensity (mW/sr) @ 20 mA	$2\theta_{1/2}$ [1] Degrees
8104	2.9	4.0	8.4	47.1	7
8103	2.0	3.0	5.8	35.3	7
8102	1.4	2.0	4.0	23.5	7
8100	0.29	0.7	2.0	11.8	24

Note:
1. $\theta_{1/2}$ is the off axis angle from optical centerline where the luminous intensity is 1/2 the on-axis value.

Absolute Maximum Ratings at T_A = 25 °C

Peak Forward Current [1,2] ..... 300 mA
Average Forward Current (@ I_{PEAK}=300 mA) [2] ..... 15 mA
DC Forward Current [3] ..... 50 mA
Power Dissipation ..... 130 mW
Reverse Voltage (I_R=100 µA) ..... 8 V
Transient Forward Current (10 µs Pulse) [4] ..... 500 mA
Operating Temperature Range ..... -55 to +100°C
Storage Temperature Range ..... -55 to +100°C
Lead Soldering Temperature
[1.6 mm (0.063 in.) from body] ..... 260°C for 5 seconds

Notes:
1. Maximum I_{PEAK} at f = 1 kHz, DF = 5%.
2. Refer to Figure 6 to establish pulsed operating conditions.
3. Derate linearly as shown in Figure 5.
4. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bonds. It is not recommended that the device be operated at peak currents above the Absolute Maximum Peak Forward Current.

Electrical/Optical Characteristics at T_A = 25 °C

Description	Symbol	Min	Typ	Max	Units	Test Condition
Forward Voltage	V_F		1.85	2.4	V	I_F = 20 mA
Reverse Voltage	V_R	8.0	20.0		V	I_R = 100 µA
Peak Wavelength	λ_{PEAK}		650		nm	
Dominant Wavelength [1]	λ_d		637		nm	
Spectral Line Halfwidth	$\Delta\lambda 1/2$		22		nm	
Speed of Response	τ_S		45		ns	Exponential Time Constant, e^{-t/τ_S}
Capacitance	C		20		pF	V_F = 0, f = 1 MHz
Thermal Resistance	$R\theta_{J\text{-}PIN}$		220		°C/W	Junction-to-Anode Lead
Luminous Efficacy [2]	η_v		85		lm/W	

Notes:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the color of the device.
2. The radiant intensity, I_e, in watts per steradian, may be found from the equation $I_e=I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is luminous efficacy in lumens/watt.
3. The approximate total luminous flux output within a cone angle of 2θ about the optical axis may be obtained from the following formula:
$\phi_v 2(\theta) = [\phi_v(\theta)/I_v(0)]I_v$;
Where: $\phi_v(\theta)/I_v(0)$ is obtained from Figure 7.

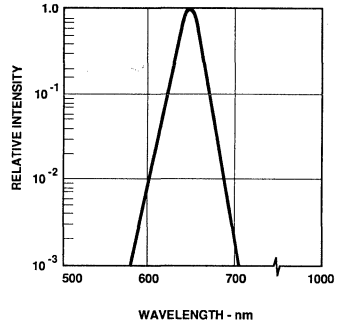


Figure 1. Relative Intensity vs. Wavelength.

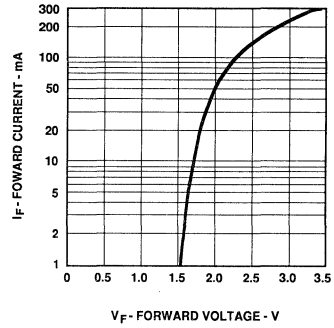


Figure 2. Forward Current vs. Forward Voltage.

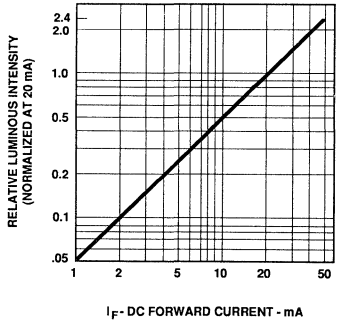


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

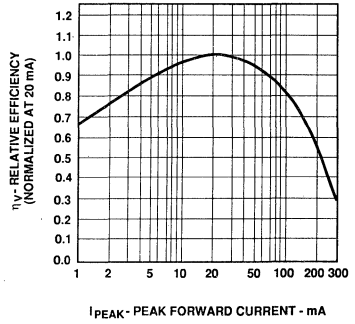


Figure 4. Relative Efficiency vs. Peak Forward Current.

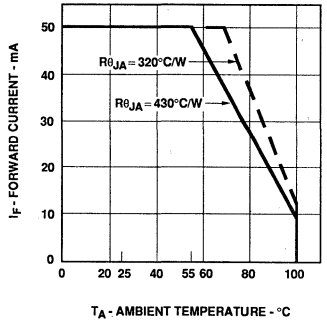


Figure 5. Maximum Forward DC Current vs. Ambient Temperature. Derating Based on T_JMAX = 110°C.

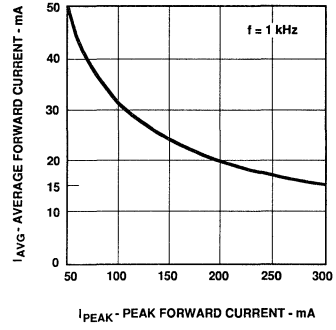


Figure 6. Maximum Average Current vs. Peak Forward Current. Refresh Rate = 1 kHz.

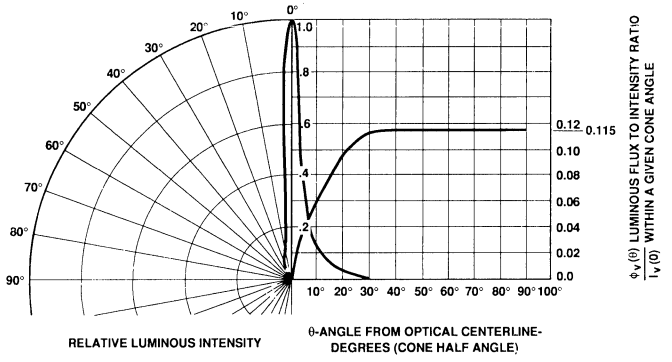


Figure 7. Relative Luminous Intensity vs. Angular Displacement. HLMP- 8104, HLMP-8103 and HLMP-8102.

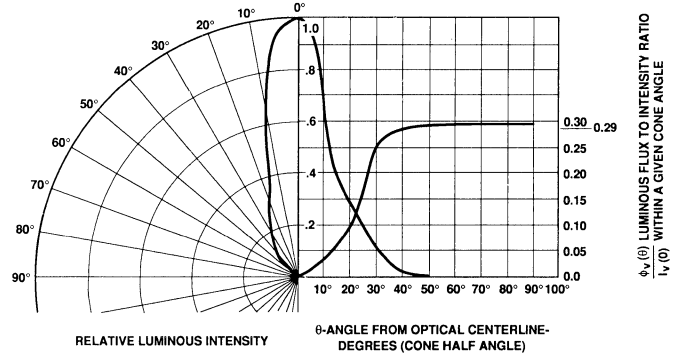


Figure 8. Relative Luminous Intensity vs. Angular Displacement. HLMP-8100.

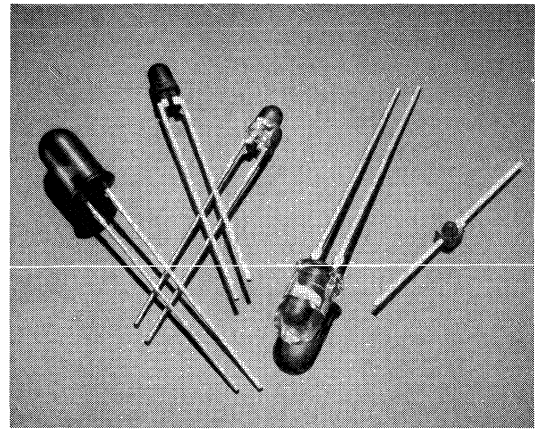
HEWLETT PACKARD

DOUBLE HETEROJUNCTION AlGaAs HIGH INTENSITY RED LED LAMPS

T-1 3/4 (5mm) HLMP-D101/D105
T-1 (3mm) HLMP-K101/K105
SUBMINIATURE HLMP-Q101

Features

- EXCEPTIONAL BRIGHTNESS
- WIDE VIEWING ANGLE
- OUTSTANDING MATERIAL EFFICIENCY
- LOW FORWARD VOLTAGE
- CMOS/MOS COMPATIBLE
- TTL COMPATIBLE
- DEEP RED COLOR



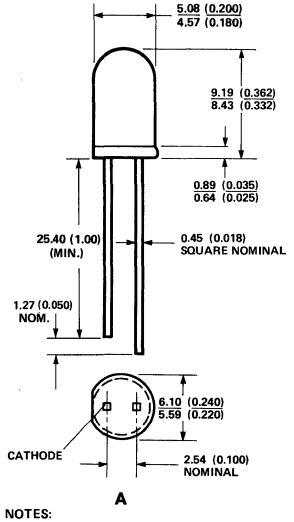
Applications

- BRIGHT AMBIENT LIGHTING CONDITIONS
- MOVING MESSAGE PANELS
- PORTABLE EQUIPMENT
- GENERAL USE

Description

These solid state LED lamps utilize newly developed double heterojunction (DH) AlGaAs/GaAs material technology. This LED material has outstanding light output efficiency over a wide range of drive currents. The color is deep red at the dominant wavelength of 637 nanometres. These lamps may be DC or pulse driven to achieve desired light output.

Package Dimensions



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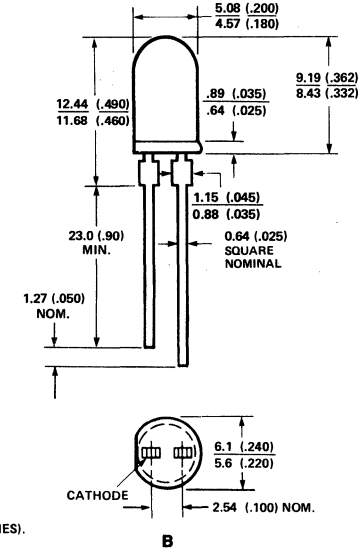

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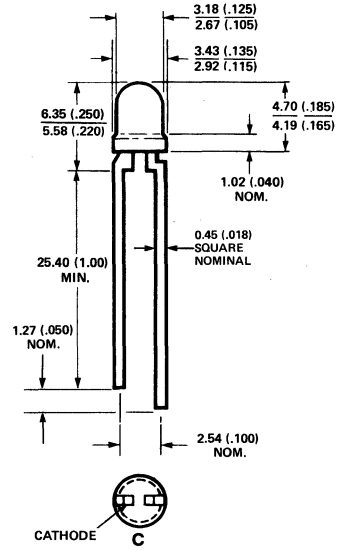
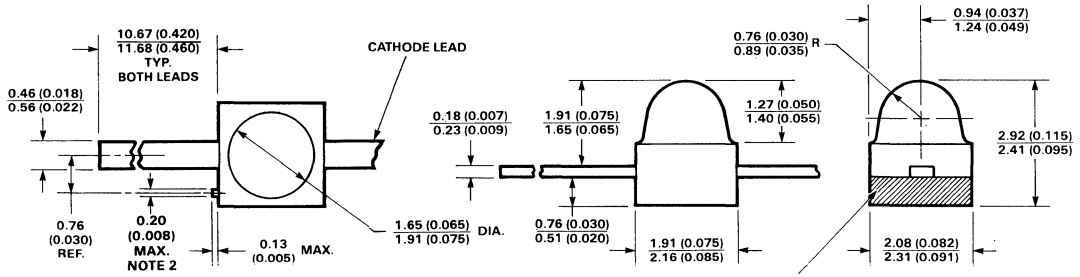


C

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MINISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.

(Continued on next page.)

Package Dimensions



NOTES: 1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)
2. PROTRUDING SUPPORT TAB IS CONNECTED TO CATHODE LEAD.

Axial Luminous Intensity and Viewing Angle @ 25°C

Part Number HLMP-	Package Description	I_V (mcd) @ 20 mA Min.	Typ.	2θ ½ Note 1. Degrees	Package Outline
D101	T-1 ¾ Red Tinted Diffused	35	70	65	A
D105	T-1 ¾ Red Untinted, Non-diffused	100	240	24	B
K101	T-1 Red Tinted Diffused	22	45	60	C
K105	T-1 Red Untinted Non-diffused	35	65	45	C
Q101	Subminiature Red Tinted Diffused	20	45	70	D

Note:
1. θ½ is the off axis angle from lamp centerline where the luminous intensity is ½ the on-axis value.

Absolute Maximum Ratings at T_A = 25°C

Peak Forward Current[1, 2] ..... 300 mA
Average Forward Current[2] ..... 20 mA
DC Current[3] ..... 30 mA
Power Dissipation ..... 87 mW
Reverse Voltage (I_R = 100μA) ..... 5 V
Transient Forward Current (10 μs Pulse)[4] ..... 500 mA
Operating Temperature Range ..... -20 to +100°C
Storage Temperature Range ..... -55 to +100°C
Lead Soldering Temperature
[1.6 mm (0.063 in.) from body] ... 260°C for 5 seconds

Notes:
1. Maximum I_{PEAK} at f = 1 kHz, DF = 6.7%.
2. Refer to Figure 6 to establish pulsed operating conditions.
3. Derate linearly as shown in Figure 5.
4. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bonds. It is not recommended that the device be operated at peak currents beyond the Absolute Maximum Peak Forward Current.

Electrical/Optical Characteristics at T_A = 25°C

Symbol	Description	Min.	Typ.	Max.	Unit	Test Condition
V_F	Forward Voltage		1.8	2.2	V	I_F = 20 mA
V_R	Reverse Breakdown Voltage	5.0	15.0		V	I_R = 100 μA
λ_p	Peak Wavelength		645		nm	Measurement at peak
λ_d	Dominant Wavelength		637		nm	Note 1
$\Delta\lambda$½	Spectral Line Halfwidth		20		nm	
τ_S	Speed of Response		30		ns	Exponential Time Constant, e^{-t}/T_S
C	Capacitance		30		pF	V_F = 0, f = 1 MHz
θ_{JC}	Thermal Resistance		220		°C/W	Junction to Cathode Lead
η_V	Luminous Efficacy		80		lm/W	Note 2

Notes:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the color of the device.
2. The radiant intensity, I_e, in watts per steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity is in candelas and η_V is luminous efficacy in lumens/watt.

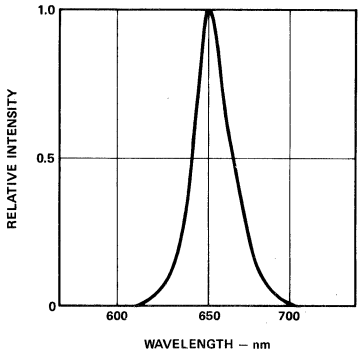


Figure 1. Relative Intensity vs. Wavelength.

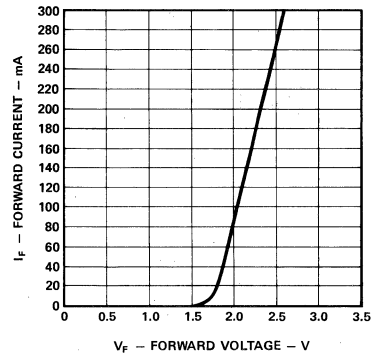


Figure 2. Forward Current vs. Forward Voltage.

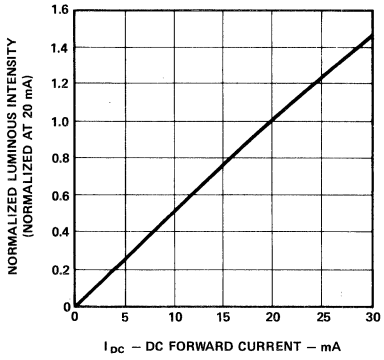


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

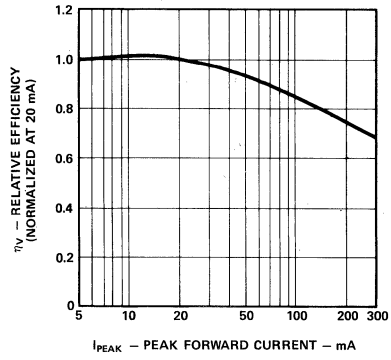


Figure 4. Relative Efficiency vs. Peak Forward Current.

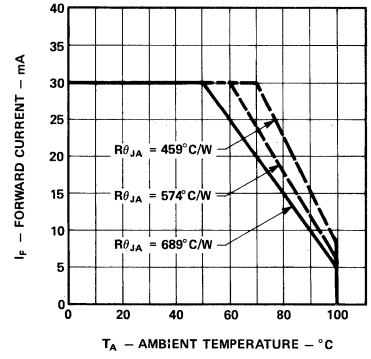


Figure 5. Maximum Forward DC Current vs. Ambient Temperature. Derating Based on T_J MAX = 110° C.

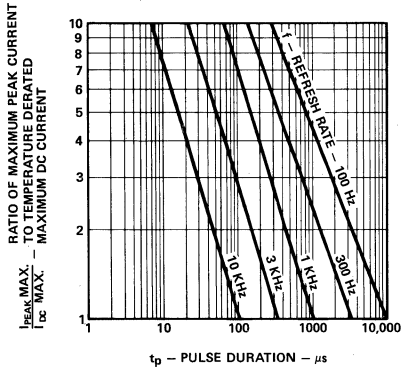


Figure 6. Maximum Tolerable Peak Current vs. Peak Duration (I_{PEAK} MAX Determined from Temperature Derated I_{DC} MAX).

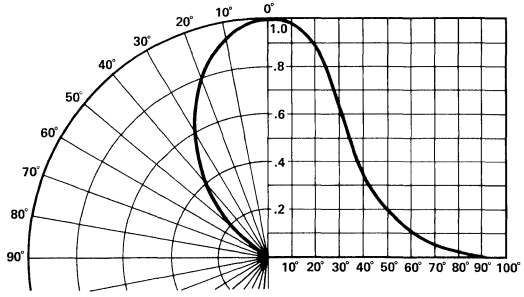


Figure 7. Relative Luminous Intensity vs. Angular Displacement. HLMP-D101.

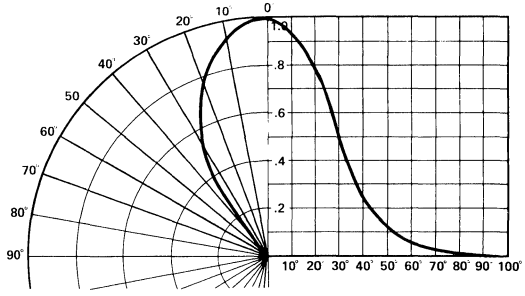


Figure 8. Relative Luminous Intensity vs. Angular Displacement. HLMP-K101.

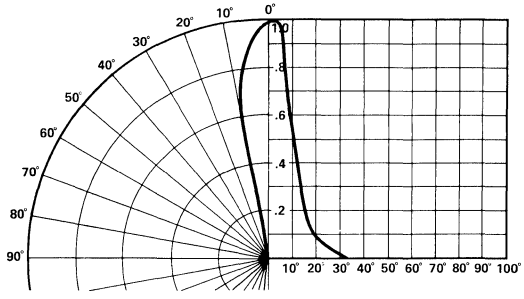


Figure 9. Relative Luminous Intensity vs. Angular Displacement. HLMP-D105.

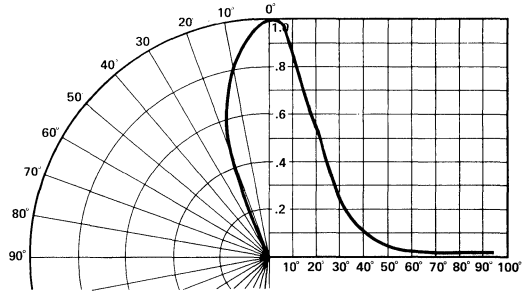


Figure 10. Relative Luminous Intensity vs. Angular Displacement. HLMP-K105.

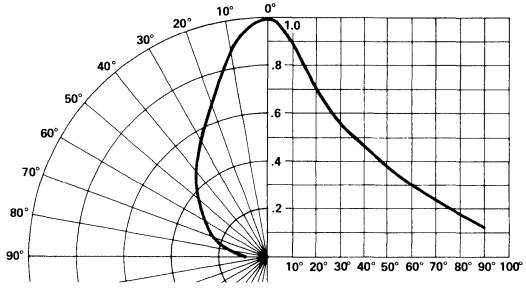


Figure 11. Relative Luminous Intensity vs. Angular Displacement for Subminiature Lamp

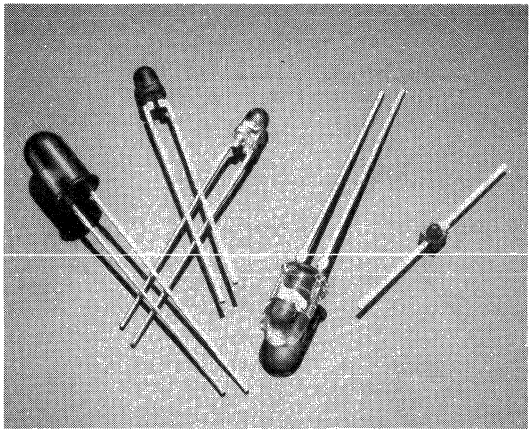
HEWLETT PACKARD

DOUBLE HETEROJUNCTION AlGaAs LOW CURRENT RED LED LAMPS

T-1 3/4 (5mm) HLMP-D150/D155
T-1 (3mm) HLMP-K150/K155
SUBMINIATURE HLMP-Q150

Features

- MINIMUM LUMINOUS INTENSITY SPECIFIED AT 1 mA
- HIGH LIGHT OUTPUT AT LOW CURRENTS
- WIDE VIEWING ANGLE
- OUTSTANDING MATERIAL EFFICIENCY
- LOW POWER/LOW FORWARD VOLTAGE
- CMOS/MOS COMPATIBLE
- TTL COMPATIBLE
- DEEP RED COLOR



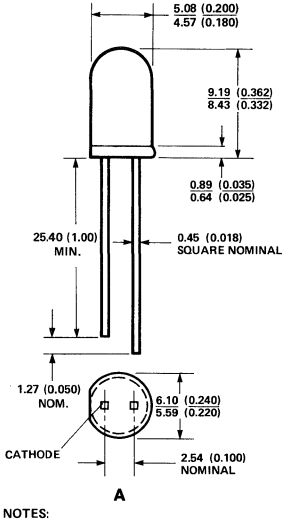
Applications

- LOW POWER CIRCUITS
- BATTERY POWERED EQUIPMENT
- TELECOMMUNICATION INDICATORS

Description

These solid state LED lamps utilize newly developed double heterojunction (DH) AlGaAs/GaAs material technology. This LED material has outstanding light output efficiency at very low drive currents. The color is deep red at the dominant wavelength of 637 nanometres. These lamps are ideally suited for use in applications where high light output is required with minimum power input.

Package Dimensions



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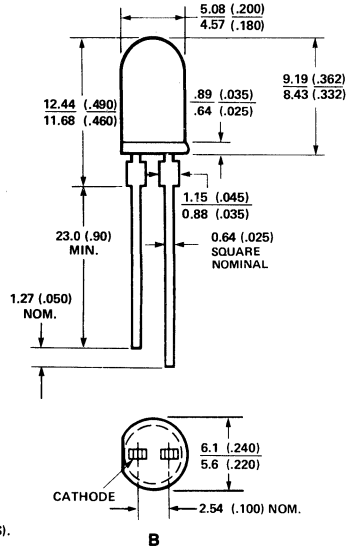

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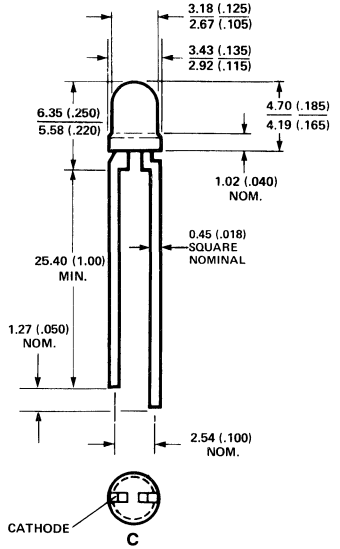
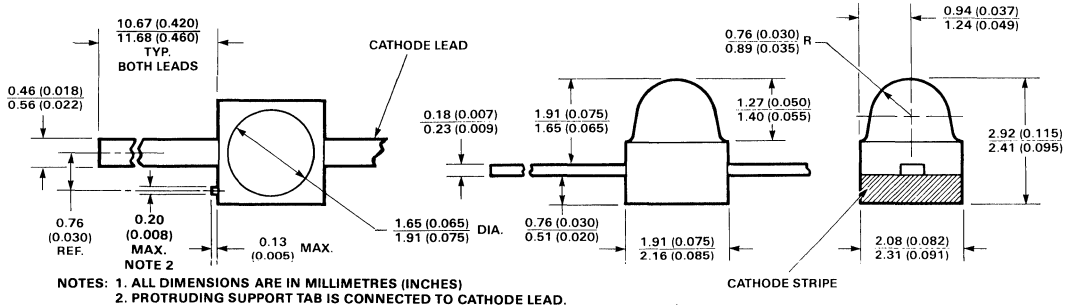


C

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MINISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.

(Continued on next page.)

Package Dimensions



NOTES: 1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)
2. PROTRUDING SUPPORT TAB IS CONNECTED TO CATHODE LEAD.

Axial Luminous Intensity and Viewing Angle @ 25°C

Part Number HLMP-	Package Description	I_V (mcd) @ 1 mA DC Min.	Typ.	2θ ½ Note 1. Degrees	Package Outline
D150	T-1 ¾ Red Tinted Diffused	1.2	3	65	A
D155	T-1 ¾ Red Untinted, Non-diffused	5	10	24	B
K150	T-1 Red Tinted Diffused	1.2	2	60	C
K155	T-1 Red Untinted Non-diffused	2	3	45	C
Q150	Subminiature Red Tinted Diffused	1	1.8	70	D

Note:
1. θ½ is the off axis angle from lamp centerline where the luminous intensity is ½ the on-axis value.

Absolute Maximum Ratings at T_A = 25°C

Peak Forward Current[1] ..... 300 mA
Average Forward Current ..... 20 mA
DC Current[2] ..... 30 mA
Power Dissipation ..... 87 mW
Reverse Voltage (I_R = 100 μA) ..... 5 V
Transient Forward Current (10 μs Pulse)[3] ..... 500 mA
Operating Temperature Range ..... -20 to +100° C
Storage Temperature Range ..... -55 to +100° C
Lead Soldering Temperature
[1.6 mm (0.063 in.) from body] ... 260° C for 5 seconds

Notes:
1. Maximum I_{PEAK} at f = 1 kHz, DF = 6.7%.
2. Derate linearly as shown in Figure 4.
3. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bonds. It is not recommended that the device be operated at peak currents beyond the Absolute Maximum Peak Forward Current.

Electrical/Optical Characteristics at T_A = 25°C

Symbol	Description	Min.	Typ.	Max.	Unit	Test Condition
V_F	Forward Voltage		1.6	1.8	V	I_F = 1 mA
V_R	Reverse Breakdown Voltage	5.0	15.0		V	I_R = 100 μA
λ_p	Peak Wavelength		645		nm	Measurement at peak
λ_d	Dominant Wavelength		637		nm	Note 1
$\Delta\lambda$½	Spectral Line Halfwidth		20		nm	
τ_S	Speed of Response		30		ns	Exponential Time Constant, e^{-t}/T_S
C	Capacitance		30		pF	V_F = 0, f = 1 MHz
θ_{JC}	Thermal Resistance		220		°C/W	Junction to Cathode Lead
η_V	Luminous Efficacy		80		lm/W	Note 2

Notes:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the color of the device.
2. The radiant intensity, I_e, in watts per steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity is in candelas and η_V is luminous efficacy in lumens/watt.

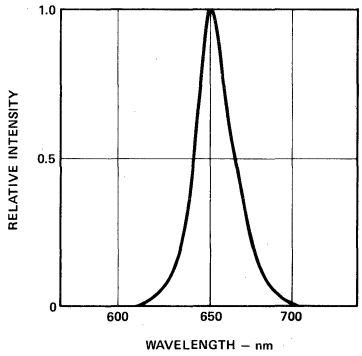


Figure 1. Relative Intensity vs. Wavelength.

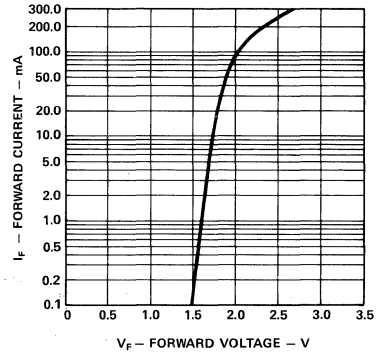


Figure 2. Forward Current vs. Forward Voltage.

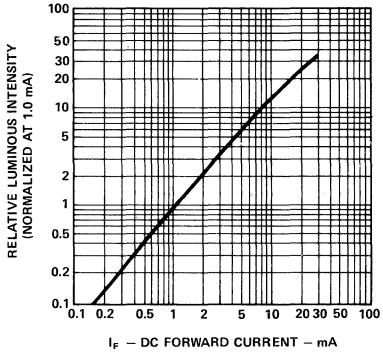


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

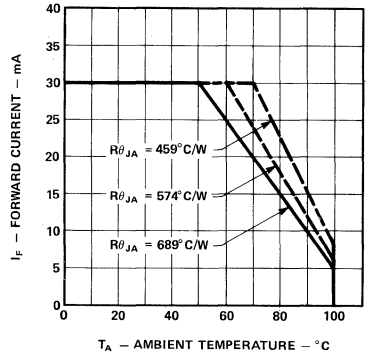


Figure 4. Maximum Forward DC Current vs. Ambient Temperature. Derating Based on T_J Max. = 110° C.

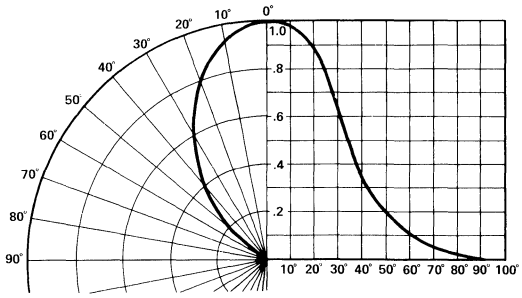


Figure 5. Relative Luminous Intensity vs. Angular Displacement. HLMP-D150.

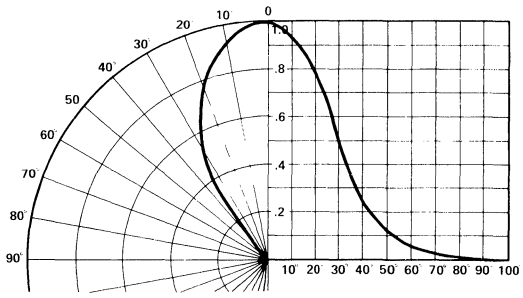


Figure 6. Relative Luminous Intensity vs. Angular Displacement. HLMP-K150.

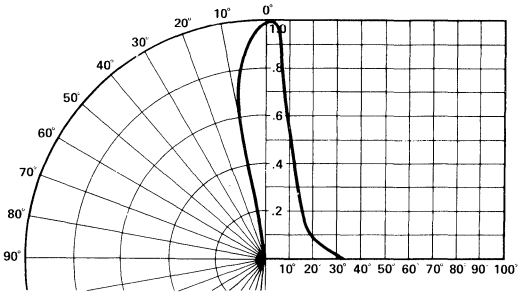


Figure 7. Relative Luminous Intensity vs. Angular Displacement. HLMP-D155.

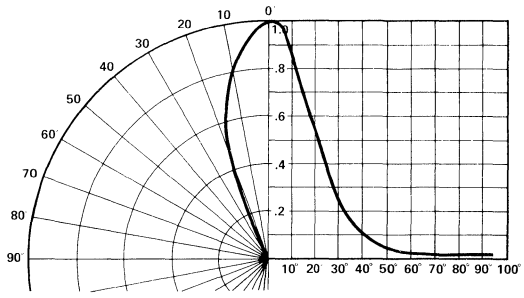


Figure 8. Relative Luminous Intensity vs. Angular Displacement. HLMP-K155.

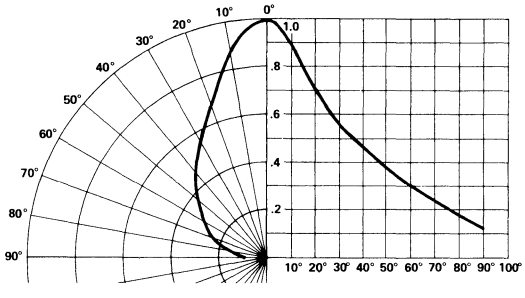


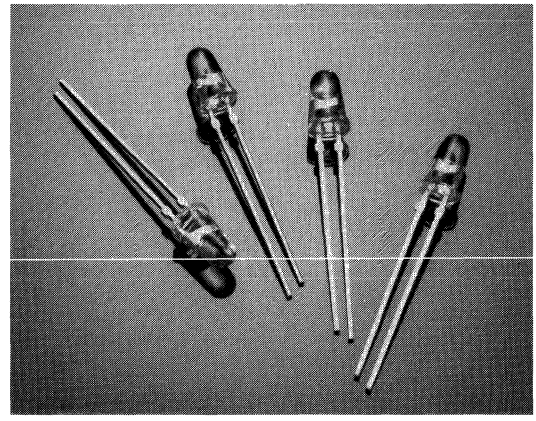
Figure 9. Relative Luminous Intensity vs. Angular Displacement for Subminiature Lamp

HEWLETT PACKARD

DOUBLE HETEROJUNCTION AlGaAs VERY HIGH INTENSITY RED LED LAMPS T-1 3/4 (5 mm) HLMP-4100,-4101

Features

- **1000 mcd AT 20 mA**
- **VERY HIGH INTENSITY AT LOW DRIVE CURRENTS**
- **NARROW VIEWING ANGLE**
- **OUTSTANDING MATERIAL EFFICIENCY**
- **LOW FORWARD VOLTAGE**
- **CMOS/MOS COMPATIBLE**
- **TTL COMPATIBLE**
- **DEEP RED COLOR**



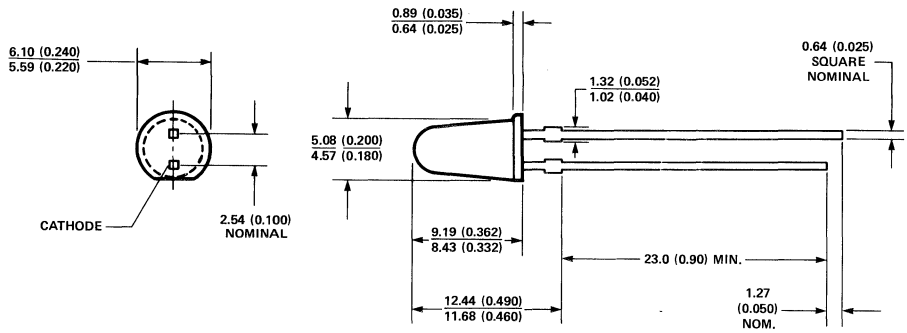
Applications

- **BRIGHT AMBIENT LIGHTING CONDITIONS**
- **EMITTER/DETECTOR AND SIGNALING APPLICATIONS**
- **GENERAL USE**

Description

These solid state LED lamps utilize newly developed double heterojunction (DH) AlGaAs/GaAs material technology. This LED material has outstanding light output efficiency over a wide range of drive currents. The lamp package has a tapered lens, designed to concentrate the luminous flux into a narrow radiation pattern to achieve a very high intensity. The LED color is deep red at the dominant wavelength of 637 nanometres. These lamps may be DC or pulse driven to achieve desired light output.

Package Dimensions



Luminous Intensity @ 25°C

P/N HLMP-	Package Description	I_V (mcd) @ 20 mA DC Min.	I_V (mcd) @ 20 mA DC Typ.	2θ1/2 Note 1. Degrees
4100	T-1 3/4 Red Untinted, Non-diffused	500	750	8
4101		700	1000	

Note:
1. θ1/2 is the angle from optical centerline where the luminous intensity is 1/2 the optical centerline value.

Absolute Maximum Ratings at T_A = 25°C

Parameter	Maximum Rating	Units
Peak Forward Current[1, 2]	300	mA
Average Forward Current[2]	20	mA
DC Current[3]	30	mA
Power Dissipation	87	mW
Reverse Voltage (I_R = 100 μA)	5	V
Transient Forward Current (10 μs Pulse)[4]	500	mA
Operating Temperature Range	-20 to +100	°C
Storage Temperature Range	-55 to +100	°C
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 5 seconds	

Notes:
1. Maximum I_{PEAK} at f = 1 kHz, DF = 6.7%.
2. Refer to Figure 6 to establish pulsed operating conditions.
3. Derate linerally as shown in Figure 5.
4. The transient peak current is the maximum non-recurring peak current the device can withstand without damaging the LED die and wire bonds. It is not recommended that the device be operated at peak currents beyond the Absolute Maximum Peak Forward Current.

Electrical/Optical Characteristics at T_A = 25°C

Symbol	Description	Min.	Typ.	Max.	Unit	Test Condition
V_F	Forward Voltage		1.8	2.2	V	20 mA
V_R	Reverse Breakdown Voltage	5.0	15.0		V	I_R = 100 μA
λ_{PEAK}	Peak Wavelength		645		nm	Measurement at peak
λ_d	Dominant Wavelength		637		nm	Note 1
$\Delta\lambda$ 1/2	Spectral Line Halfwidth		20		nm	
τ_S	Speed of Response		30		ns	Exponential Time Constant, $e^{-t/s}$
C	Capacitance		30		pF	V_F = 0, f = 1 MHz
θ_{jc}	Thermal Resistance		220		°C/W	Junction to Cathode Lead
η_V	Luminous Efficacy		80		lm/W	Note 2

Notes:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the color of the device.
2. The radiant intensity, I_e, in watts per steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is luminous efficacy in lumens/watt.
3. The approximate total luminous flux output within a cone angle of 2θ about the optical axis, $\phi_V(2\theta)$, may be obtained from the following formula:
   $\phi_V(2\theta) = [\phi_V(\theta)/I_V(0)]I_V$;
   Where: $\phi_V(\theta)/I_V(0)$ is obtained from Figure 7.

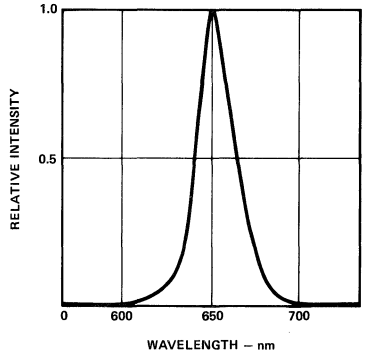


Figure 1. Relative Intensity vs. Wavelength

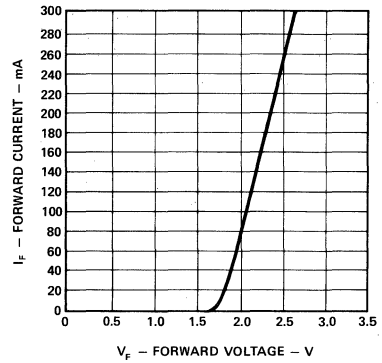


Figure 2. Forward Current vs. Forward Voltage

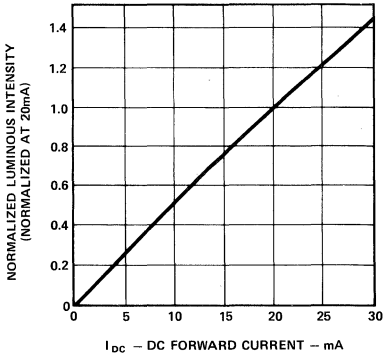


Figure 3. Relative Luminous Intensity vs. DC Forward Current

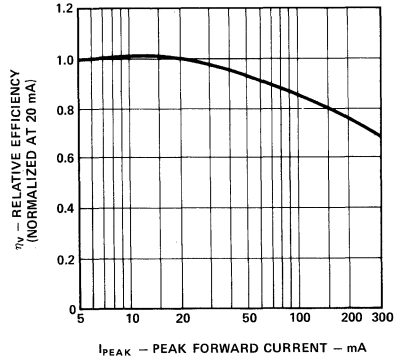


Figure 4. Relative Efficiency vs. Peak Forward Current

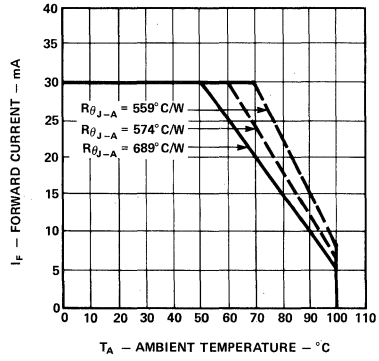


Figure 5. Maximum Forward DC Current vs. Ambient Temperature Derating Based on T_J MAX. =110° C

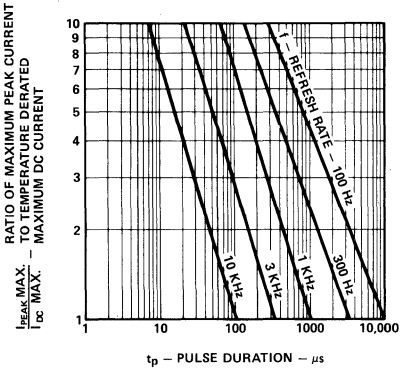


Figure 6. Maximum Tolerable Peak Current vs. Peak Duration (I_{PEAK} MAX Determined from Temperature Derated I_{DC} MAX).

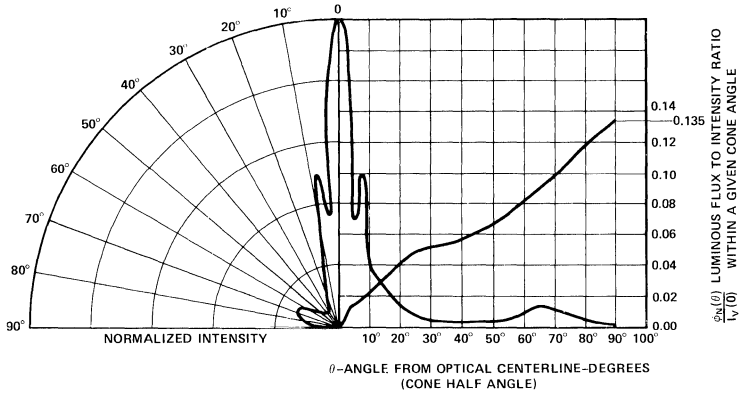


Figure 7. Relative Luminous Intensity vs. Angular Displacement

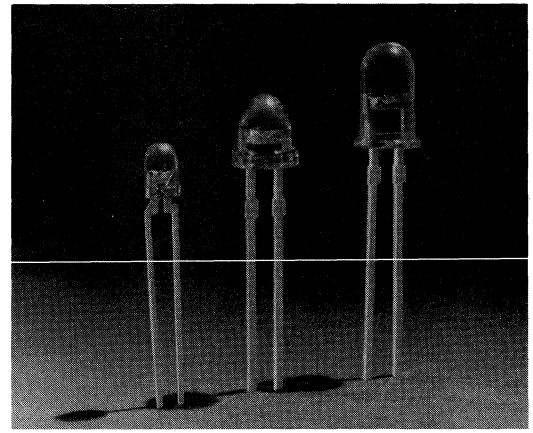
HEWLETT PACKARD

ULTRA-BRIGHT LED LAMPS

T-1 3/4 HLMP-3750,-3850,-3950
T-1 3/4 LOW PROFILE HLMP-3390,-3490,-3590
T-1 HLMP-1340,-1440,-1540

Features

- **IMPROVED BRIGHTNESS**
- **IMPROVED COLOR PERFORMANCE**
- **AVAILABLE IN POPULAR T-1 and T-1 3/4 PACKAGES**
- **NEW STURDY LEADS**
- **IC COMPATIBLE/LOW CURRENT CAPABILITY**
- **RELIABLE AND RUGGED**
- **CHOICE OF 3 BRIGHT COLORS**
  High Efficiency Red
  High Brightness Yellow
  High Performance Green



Description

These clear, non-diffused lamps out perform conventional LED lamps. By utilizing new higher intensity material, we achieve superior product performance.

The HLMP-3750/-3390/-1340 Series Lamps are Gallium Arsenide Phosphide on Gallium Phosphide red light emitting diodes. The HLMP-3850/-3490/-1440 Series are Gallium Arsenide Phosphide on Gallium Phosphide yellow light emitting diodes. The HLMP-3950/-3590/-1540 Series lamps are Gallium Phosphide green light emitting diodes.

Applications

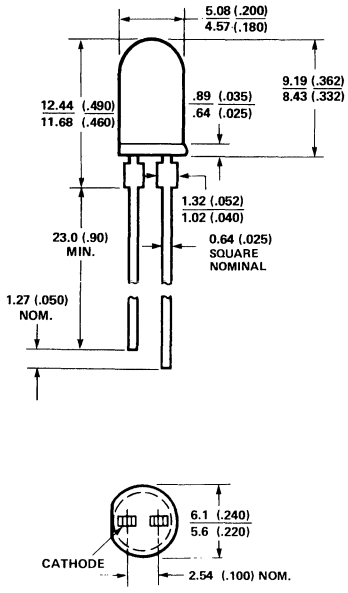
- **LIGHTED SWITCHES**
- **BACKLIGHTING FRONT PANELS**
- **LIGHT PIPE SOURCES**
- **KEYBOARD INDICATORS**

Axial Luminous Intensity and Viewing Angle @ 25°C

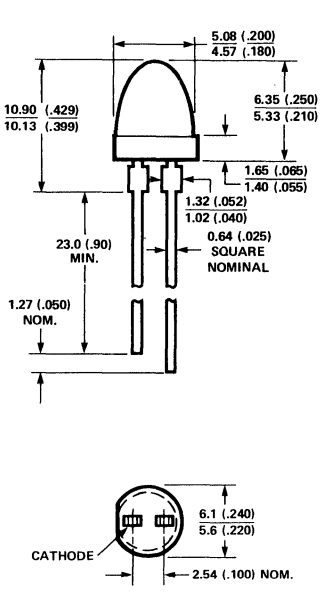
Part Number HLMP-	Package Description	Color	I_V (mcd) @ 20 mA DC		2Θ 1/2 Note 1.	Package Outline
			Min.	Typ.		
3750	T-1 3/4	HER	80	125	24°	A
3850		Yellow	80	140	24°	A
3950		Green	80	120	24°	A
3390	T-1 3/4 Low Profile	HER	35	55	32°	B
3490		Yellow	35	55	32°	B
3590		Green	35	55	32°	B
1340	T-1	HER	24	45	45°	C
1440		Yellow	24	45	45°	C
1540		Green	24	45	45°	C

NOTE:
1. Θ1/2 is the typical off-axis angle at which the luminous intensity is half the axial luminous intensity.

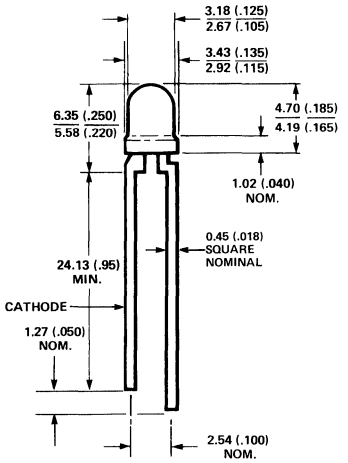
Package Dimensions



PACKAGE OUTLINE "A"
HLMP-3750, 3850, 3950



PACKAGE OUTLINE "B"
HLMP-3390, 3490, 3590



PACKAGE OUTLINE "C"
HLMP-1340, 1440, 1540

NOTES:
1. All dimensions are in millimeters (inches).
2. An epoxy meniscus may extend about 1mm (0.40") down the leads.

Absolute Maximum Ratings at T_A = 25°C

Parameter	Red	Yellow	Green	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Transient Forward Current[4] (10 μsec pulse)	500	500	500	mA
Reverse Voltage (I_R = 100 μA)	5	5	5	V
Operating Temperature Range	−55 to +100	−55 to +100	−20 to +100	°C
Storage Temperature Range			−55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

NOTES:
1. See Figure 2 to establish pulsed operating conditions.
2. For Red and Green series derate linearly from 50° C at 0.5 mA/° C. For Yellow series derate linearly from 50° C at 0.2 mA/° C.
3. For Red and Green series derate power linearly from 25° C at 1.8 mW/° C. For Yellow series derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

Electrical/Optical Characteristics at T_A = 25°C

Symbol	Description	T-1 3/4	T-1 3/4 Low Dome	T-1	Min.	Typ.	Max.	Units	Test Conditions
λ_{PEAK}	Peak Wavelength	3750 3850 3950	3390 3490 3590	1340 1440 1540		635 583 565		nm	Measurement at peak
λ_d	Dominant Wavelength	3750 3850 3950	3390 3490 3590	1340 1440 1540		626 585 569		nm	Note 1
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	3750 3850 3950	3390 3490 3590	1340 1440 1540		40 36 28		nm	
τ_S	Speed of Response	3750 3850 3950	3390 3490 3590	1340 1440 1540		90 90 500		ns	
C	Capacitance	3750 3850 3950	3390 3490 3590	1340 1440 1540		11 15 18		pF	V_F = 0; f = 1 MHz
Θ_{JC}	Thermal Resistance	3750 3850 3950	3390 3490 3590	 1340 1440 1540		95 95 95 120 120 120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	3750 3850 3950	3390 3490 3590	1340 1440 1540	1.5 1.5 1.5	2.2 2.2 2.3	3.0 3.0 3.0	V	I_F = 20 mA (Figure 3)
V_R	Reverse Breakdown Voltage	3750 3850 3950	3390 3490 3590	1340 1440 1540	5.0			V	I_F = 100 μA
η_V	Luminous Efficacy	3750 3850 3950	3390 3490 3590	1340 1440 1540		145 500 595		$\frac{\text{lumens}}{\text{watt}}$	Note 2

NOTES:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Red, Yellow and Green

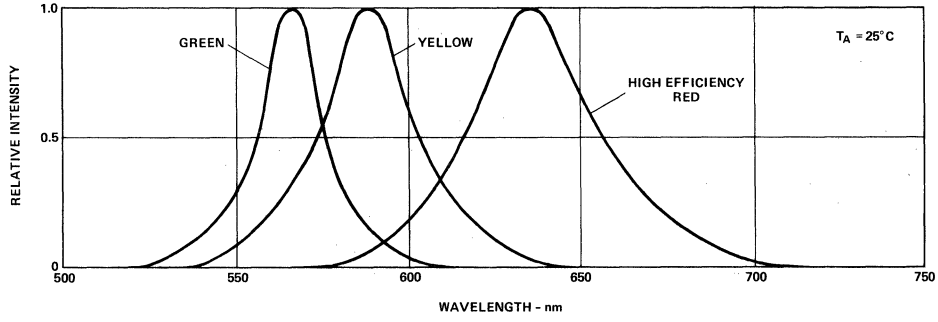


Figure 1. Relative Intensity vs. Wavelength.

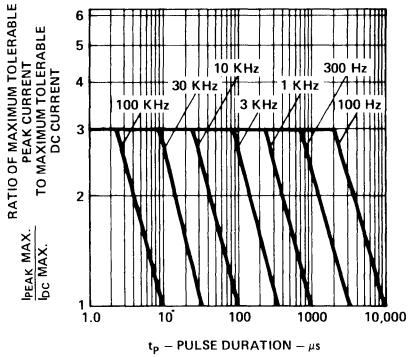


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

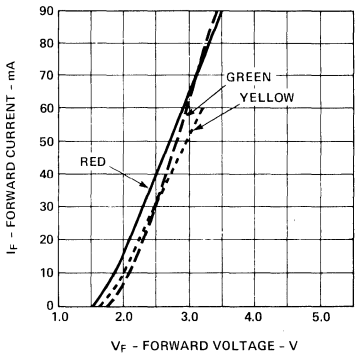


Figure 3. Forward Current vs. Forward Voltage.

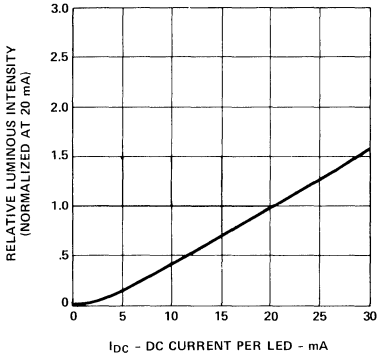


Figure 4. Relative Luminous Intensity vs. Forward Current.

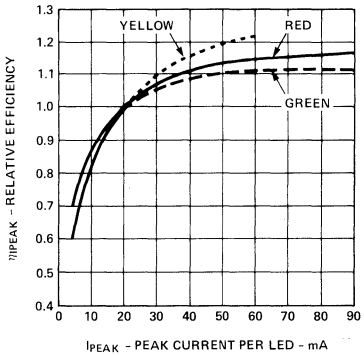


Figure 5. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

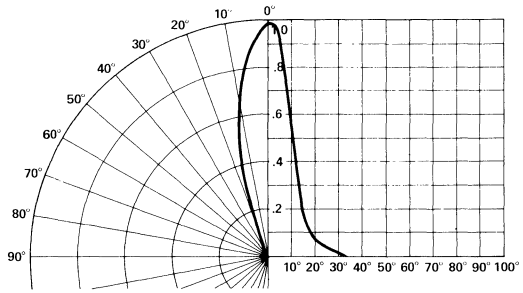


Figure 6. Relative Luminous Intensity vs. Angular Displacement. T-1 3/4 Lamp.

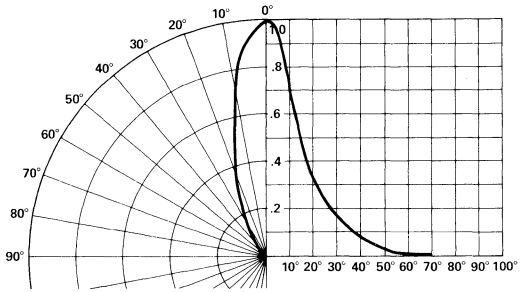


Figure 7. Relative Luminous Intensity vs. Angular Displacement. T-1 3/4 Low Profile Lamp.

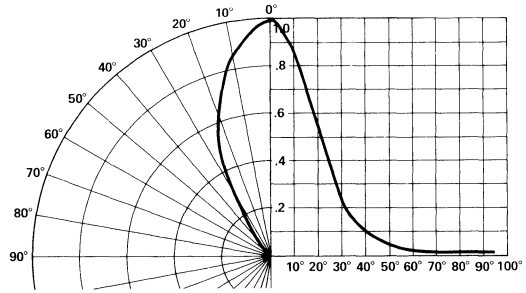


Figure 8. Relative Luminous Intensity vs. Angular Displacement. T-1 Lamp.

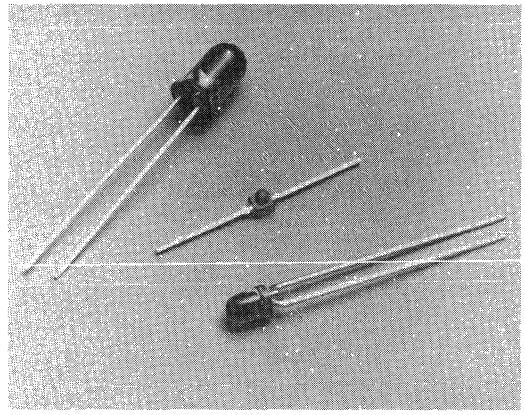
HEWLETT PACKARD

LOW CURRENT LED LAMPS

T-1 3/4 (5mm) HLMP-4700, -4719, -4740
T-1 (3mm) HLMP-1700, -1719, -1790
SUBMINIATURE HLMP-7000, -7019, -7040

Features

- LOW POWER
- HIGH EFFICIENCY
- CMOS/MOS COMPATIBLE
- TTL COMPATIBLE
- WIDE VIEWING ANGLE
- CHOICE OF PACKAGE STYLES
- CHOICE OF COLORS



Applications

- LOW POWER DC CIRCUITS
- TELECOMMUNICATIONS INDICATORS
- PORTABLE EQUIPMENT
- KEYBOARD INDICATORS

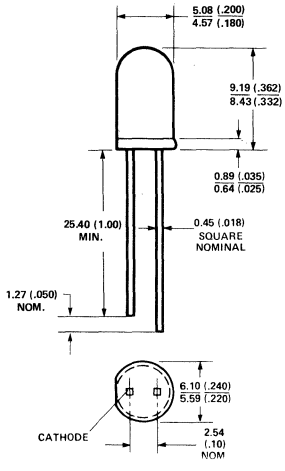
Description

These tinted diffused LED lamps were designed and optimized specifically for low DC current operation. Luminous intensity and forward voltage are tested at 2 mA to assure consistent brightness at TTL output current levels.

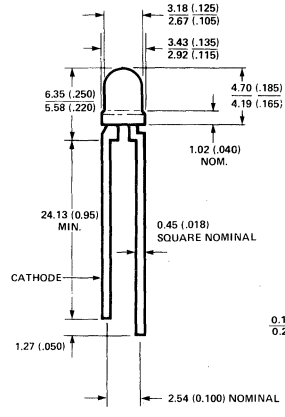
LOW CURRENT LAMP SELECTION GUIDE

Size	Color		
	Red HLMP-	Yellow HLMP-	Green HLMP-
T-1 3/4	4700	4719	4740
T-1	1700	1719	1790
Subminiature	7000	7019	7040

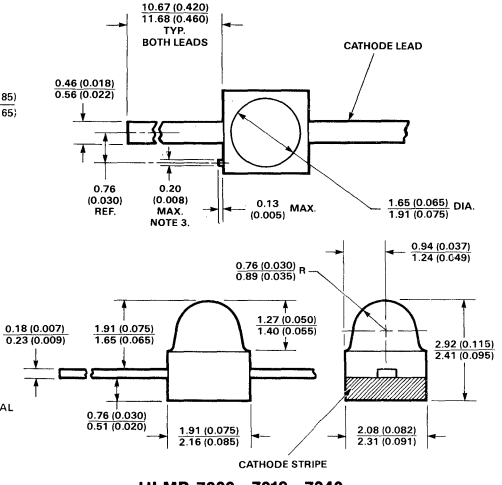
Package Dimensions



HLMP-4700, -4719, -4740



HLMP-1700, -1719, -1790



HLMP-7000, -7019, -7040

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MINISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.
3. PROTRUDING SUPPORT TAB IS CONNECTED TO CATHODE LEAD.

AXIAL LUMINOUS INTENSITY AND VIEWING ANGLE @ 25°C

Part Number HLMP-	Package Description	Color	I_V (mcd) @ 2 mA DC Min.	I_V (mcd) @ 2 mA DC Typ.	2Θ 1/2[1]	Package Outline
-4700 -4719 -4740	T-1 3/4 Tinted Diffused	Red Yellow Green	1.2 1.2 1.2	2.0 1.8 1.8	50°	A
-1700 -1719 -1790	T-1 Tinted Diffused	Red Yellow Green	1.0 1.0 1.0	1.8 1.6 1.6	50°	B
-7000 -7019 -7040	Subminiature Tinted Diffused	Red Yellow Green	0.4 0.4 0.4	0.8 0.6 0.6	90°	C

Note:
1. $\Theta 1/2$ is the typical off-axis angle at which the luminous intensity is half the axial luminous intensity.

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	T-1 3/4	T-1	Subminiature	Min.	Typ.	Max.	Units	Test Condition
V_F	Forward Voltage	4700 4719 4740	1700 1719 1790	7000 7019 7040		1.8 1.9 1.8	2.2 2.7 2.2	V	2 mA
V_R	Reverse Breakdown Voltage	4700 4719 4740	1700 1719 1790	7000 7019 7040	5.0 5.0 5.0			V	$I_R = 50\ \mu A$
λ_D	Dominant Wavelength	4700 4719 4740	1700 1719 1790	7000 7019 7040		626 585 569		nm	Note 1
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	4700 4719 4740	1700 1719 1790	7000 7019 7040		40 36 28		nm	
τ_S	Speed of Response	4700 4719 4740	1700 1719 1790	7000 7019 7040		90 90 500		ns	
C	Capacitance	4700 4719 4740	1700 1719 1790	7000 7019 7040		11 15 18		pF	$V_F = 0$ f = 1 MHz
Θ_{JC}	Thermal Resistance	4700 4719 4740	1700 1719 1790	7000 7019 7040		120 120 120		°C/W	Junction to Cathode lead
λ_{PEAK}	Peak Wavelength	4700 4719 4740	1700 1719 1790	7000 7019 7040		635 583 565		nm	Measurement at peak
η_V	Luminous Efficacy	4700 4719 4740	1700 1719 1790	7000 7019 7040		145 500 595		$\frac{\text{Lumens}}{\text{Watt}}$	Note 2

Notes:
1. The dominant wavelength, λ_D, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings

Parameter	Maximum Rating		Units
Power Dissipation (Derate linearly from 92° C at 1.0 mA/° C)	Red Yellow Green	24 36 24	mW
DC and Peak Forward Current	7		mA
Transient Forward Current (10 μsec pulse)[1]	500		mA
Reverse Voltage (I_R = 50 μA)	5.0		V
Operating Temperature Range	Red/Yellow Green	-55°C to 100°C -20°C to 100°C	
Storage Temperature Range	-55°C to 100°C		
Lead Soldering Temperature (1.6 mm [0.063 in] from body)	260° C for 5 Seconds (T-1, T-1 3/4) 260° C for 3 Seconds (Subminiature)		

Note:

1. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

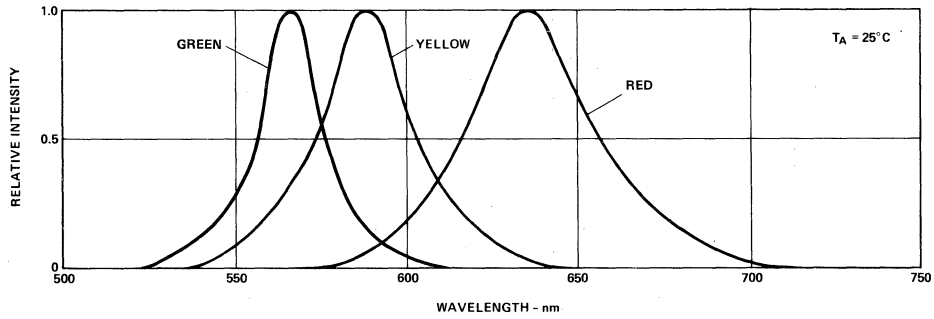


Figure 1. Relative Intensity vs. Wavelength

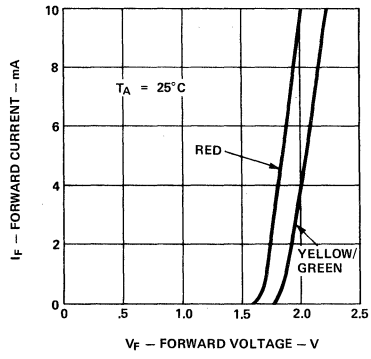


Figure 2. Forward Current vs. Forward Voltage

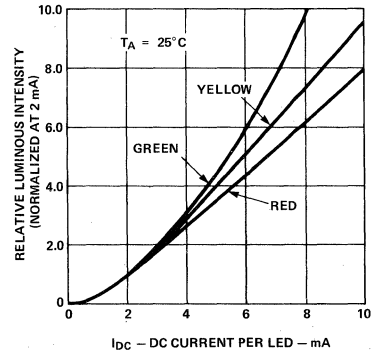


Figure 3. Relative Luminous Intensity vs. Forward Current

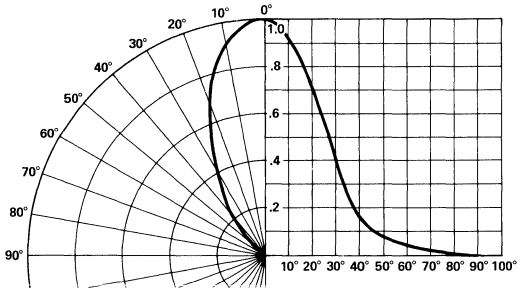


Figure 4. Relative Luminous Intensity vs. Angular Displacement for T-1 3/4 Lamp

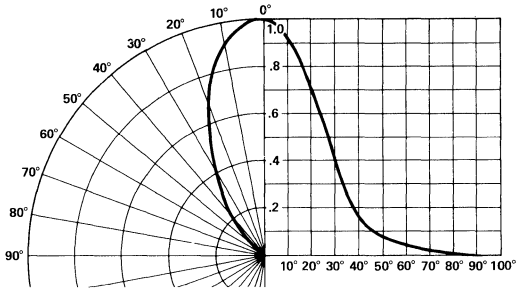


Figure 5. Relative Luminous Intensity vs. Angular Displacement for T-1 Lamp

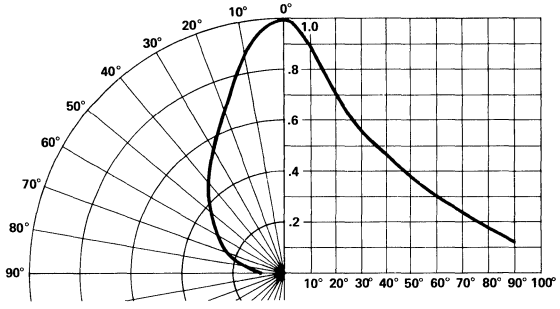


Figure 6. Relative Luminous Intensity vs. Angular Displacement for Subminiature Lamp

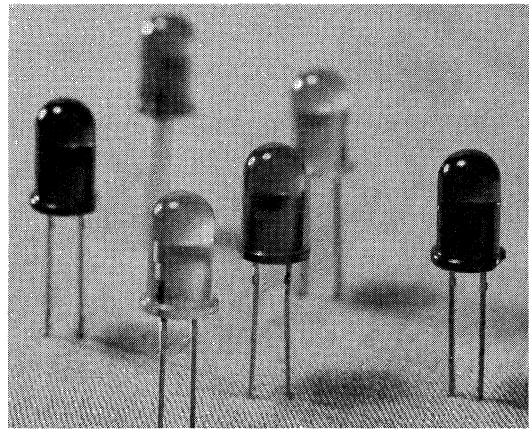
HEWLETT PACKARD

T-1 3/4 (5 mm) HIGH INTENSITY SOLID STATE LAMPS

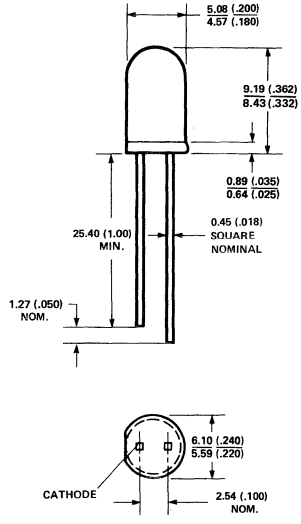
HIGH EFFICIENCY RED • HLMP-331X SERIES
YELLOW • HLMP-341X SERIES
HIGH PERFORMANCE GREEN • HLMP-351X SERIES

Features

- HIGH INTENSITY
- CHOICE OF 3 BRIGHT COLORS
  - High Efficiency Red
  - Yellow
  - High Performance Green
- POPULAR T-1 3/4 DIAMETER PACKAGE
- SELECTED MINIMUM INTENSITIES
- NARROW VIEWING ANGLE
- GENERAL PURPOSE LEADS
- RELIABLE AND RUGGED
- AVAILABLE ON TAPE AND REEL



Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Description

This family of T-1 3/4 lamps is specially designed for applications requiring higher on-axis intensity than is achievable with a standard lamp. The light generated is focused to a narrow beam to achieve this effect.

Part Number HLMP-	Description	Minimum Intensity (mcd) at 10 mA	Color (Material)
3315	Illuminator/Point Source	12	High Efficiency Red (GaAsP on GaP)
3316	Illuminator/High Brightness	20	
3415	Illuminator/Point Source	10	Yellow (GaAsP on GaP)
3416	Illuminator/High Brightness	20	
3517	Illuminator/Point Source	6.7	Green (GaP)
3519	Illuminator/High Brightness	10.6	

Electrical Characteristics at $T_A = 25°C$

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	3315 3316	12.0 20.0	40.0 60.0		mcd	I_F = 10 mA (Figure 3)
		3415 3416	10.0 20.0	40.0 50.0		mcd	I_F = 10 mA (Figure 8)
		3517 3519	6.7 10.6	50.0 70.0		mcd	I_F = 10 mA (Figure 3)
2Θ 1/2	Including Angle Between Half Luminous Intensity Points	3315 3316		35 35		Deg.	I_F = 10 mA See Note 1 (Figure 6)
		3415 3416		35 35		Deg.	I_F = 10 mA See Note 1 (Figure 11)
		3517 3519		24 24		Deg.	I_F = 10 mA See Note 1 (Figure 16)
λ_{PEAK}	Peak Wavelength	331X 341X 351X		635 583 565		nm	Measurement at Peak (Figure 1)
$\Delta\lambda$ 1/2	Spectral Line Halfwidth	331X 341X 351X		40 36 28		nm	
λ_d	Dominant Wavelength	331X 341X 351X		626 585 569		nm	See Note 2 (Figure 1)
τ_S	Speed of Response	331X 341X 351X		90 90 500		ns	
C	Capacitance	331X 341X 351X		11 15 18		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance	331X 341X 351X		120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	331X 341X 351X	1.5 1.5 1.5	2.2 2.2 2.3	3.0 3.0 3.0	V	I_F = 10 mA (Figure 2) I_F = 10 mA (Figure 7) I_F = 10 mA (Figure 12)
V_R	Reverse Breakdown Volt.	All	5.0			V	I_R = 100 μA
η_V	Luminous Efficacy	331X 341X 351X		145 500 595		lumens Watt	See Note 3

NOTES:
1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	331X Series	341X Series	351X Series	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage (I_R = 100 μA)	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	500	500	mA
Operating Temperature Range	−55 to +100	−55 to +100	−20 to +100	°C
Storage Temperature Range			−55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

NOTES:

1. See Figure 5 (Red), 10 (Yellow), or 15 (Green) to establish pulsed operating conditions.
2. For Red and Green series derate linearly from 50° C at 0.5 mA/° C. For Yellow series derate linearly from 50° C at 0.2 mA/° C.
3. For Red and Green series derate power linearly from 25° C at 1.8 mW/° C. For Yellow series derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

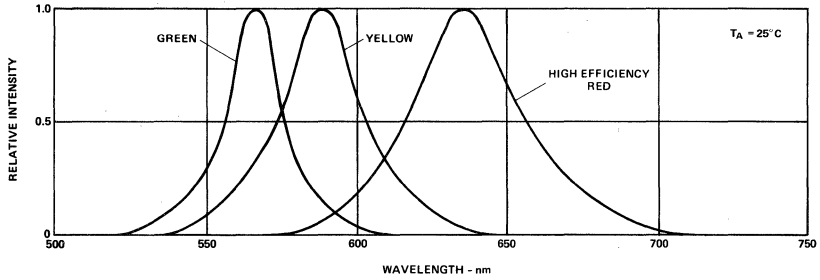


Figure 1. Relative Intensity vs. Wavelength

High Efficiency Red HLMP-331X Series

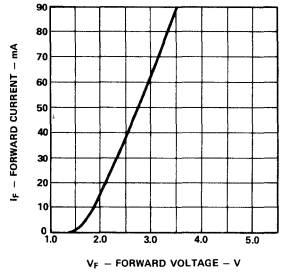


Figure 2. Forward Current vs. Forward Voltage Characteristics

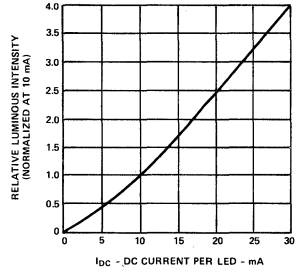


Figure 3. Relative Luminous Intensity vs. DC Forward Current

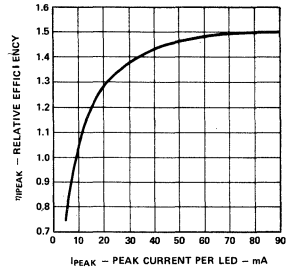


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current

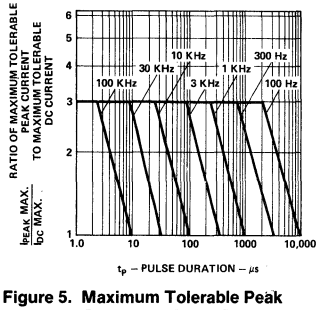


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration (I_{DC} MAX as per MAX Ratings)

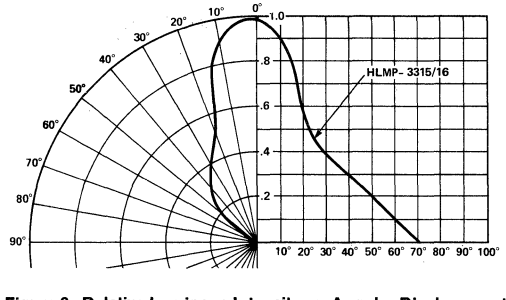


Figure 6. Relative Luminous Intensity vs. Angular Displacement

Yellow HLMP-341X Series

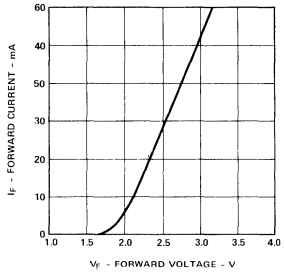


Figure 7. Forward Current vs. Forward Voltage Characteristics

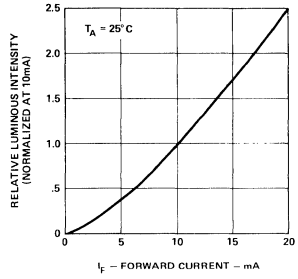


Figure 8. Relative Luminous Intensity vs. Forward Current

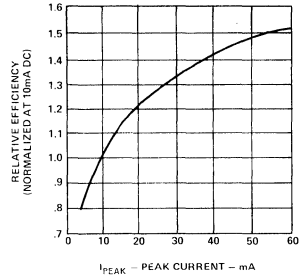


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current

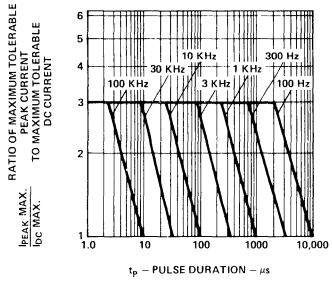


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration (I_{DC} MAX as per MAX Ratings)

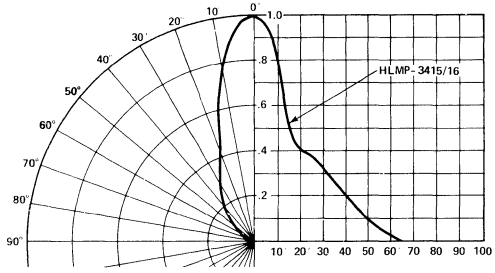


Figure 11. Relative Luminous Intensity vs. Angular Displacement

Green HLMP-351X Series

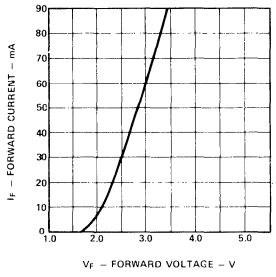


Figure 12. Forward Current vs. Forward Voltage Characteristics

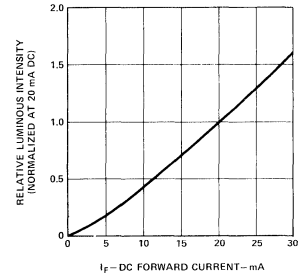


Figure 13. Relative Luminous Intensity vs. DC Forward Current

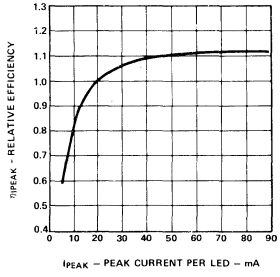


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current

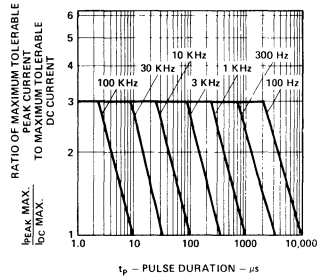


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration (I_{DC} MAX as per MAX Ratings)

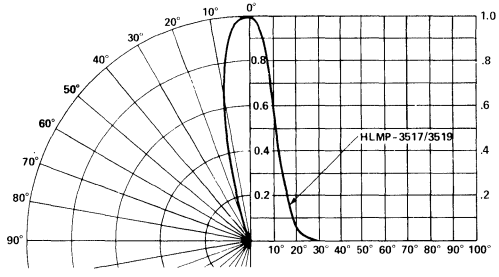


Figure 16. Relative Luminous Intensity vs. Angular Displacement. T-1 3/4 Lamp

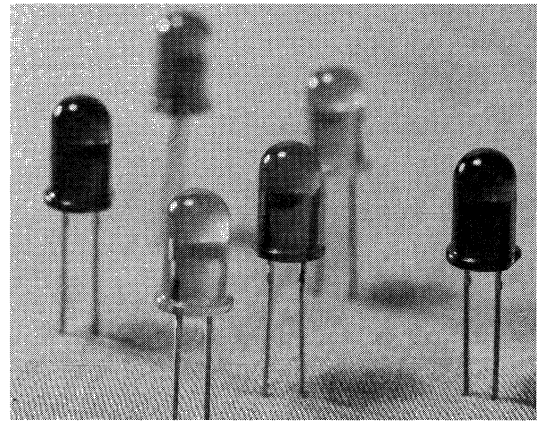
HEWLETT PACKARD

T-1 3/4 (5mm) DIFFUSED SOLID STATE LAMPS

HIGH EFFICIENCY RED ● HLMP-3300 SERIES
ORANGE ● HLMP-D400 SERIES
YELLOW ● HLMP-3400 SERIES
HIGH PERFORMANCE GREEN ● HLMP-3500 SERIES

Features

- **HIGH INTENSITY**
- **CHOICE OF 4 BRIGHT COLORS**
  - **High Efficiency Red**
  - **Orange**
  - **Yellow**
  - **High Performance Green**
- **POPULAR T-1¾ DIAMETER PACKAGE**
- **SELECTED MINIMUM INTENSITIES**
- **WIDE VIEWING ANGLE**
- **GENERAL PURPOSE LEADS**
- **RELIABLE AND RUGGED**
- **AVAILABLE ON TAPE AND REEL**

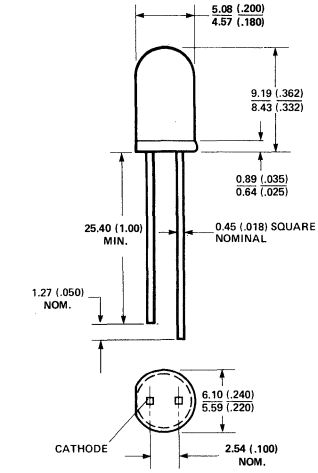


Description

This family of T-1¾ lamps is widely used in general purpose indicator applications. Diffusants, tints, and optical design are balanced to yield superior light output and wide viewing angles. Several intensity choices are available in each color for increased design flexibility.

Part Number HLMP-	Application	Minimum Intensity (mcd) at 10mA	Color (Material)
3300	General Purpose	2.1	High Efficiency Red (GaAsP on GaP)
3301	High Ambient	4.0	
3762	Premium Lamp	8.0	
D400	General Purpose	2.1	Orange (GaAsP on GaP)
D401	High Ambient	4.0	
3400	General Purpose	2.2	Yellow (GaAsP on GaP)
3401	High Ambient	4.0	
3862	Premium Lamp	8.0	
3502	General Purpose	1.6	Green (GaP) 565 nm
3507	High Ambient	4.2	
3962	Premium Lamp	8.0	

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Electrical Characteristics at $T_A = 25°C$

Symbol	Parameter	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	High Efficiency Red 3300 3301 3762	 2.1 4.0 8.0	 3.5 7.0 12.0		mcd	I_F = 10 mA
		Orange D400 D401	 2.1 4.0	 3.5 7.0			
		Yellow 3400 3401 3862	 2.2 4.0 8.0	 4.0 8.0 12.0			
		Green 3502 3507 3962	 1.6 4.2 8.0	 2.4 5.2 11.0			
$2\Theta_{1/2}$	Including Angle Between Half Luminous Intensity Points	High Efficiency Red Orange Yellow Green		60 60 60 60		Deg.	I_F = 10 mA See Note 1
λ_{PEAK}	Peak Wavelength	High Efficiency Red Orange Yellow Green		635 600 583 565		nm	Measurement at Peak
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	HER/Orange Yellow Green		40 36 28		nm	
λ_d	Dominant Wavelength	High Efficiency Red Orange Yellow Green		626 602 585 569		nm	See Note 2
τ_S	Speed of Response	High Efficiency Red Orange Yellow Green		90 280 90 500		ns	
C	Capacitance	High Efficiency Red Orange Yellow Green		11 4 15 18		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance	All		140		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	HER/Orange Yellow Green	1.5 1.5 1.5	2.2 2.2 2.3	3.0 3.0 3.0	V	I_F = 10 mA
V_R	Reverse Breakdown Voltage	All	5.0			V	I_R = 100 μA
η_V	Luminous Efficacy	High Efficiency Red Orange Yellow Green		145 380 500 595		$\frac{\text{lumens}}{\text{Watt}}$	See Note 3

NOTES:
1. $\Theta 1/2$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	HER/Orange	Yellow	Green	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage ($I_R = 100\ \mu A$)	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	500	500	mA
Operating Temperature Range	−55 to +100	−55 to +100	−20 to +100	°C
Storage Temperature Range			−55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

NOTES:

1. See Figure 5 (Red/Orange), 10 (Yellow) or 15 (Green) to establish pulsed operating conditions.
2. For Red, Orange, and Green series derate linearly from 50° C at 0.5 mA/° C. For Yellow series derate linearly from 50° C at 0.2 mA/° C. For Red, Orange, and Green series derate power linearly from 25° C at
3. 1.8 mW/°C. For Yellow series derate power linearly from 50°C at 1.6 mW/°C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

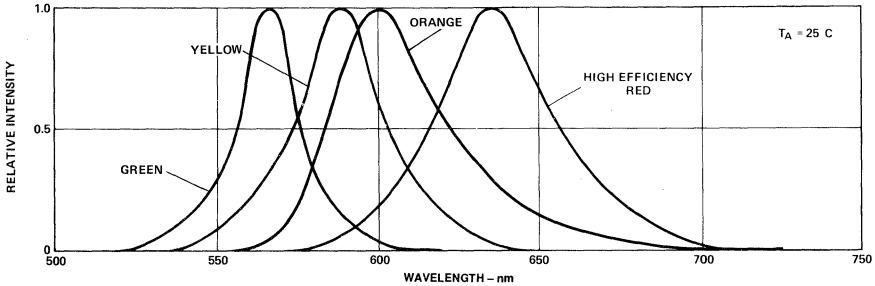


Figure 1. Relative Intensity vs. Wavelength

T-1¾ High Efficiency Red, Orange Diffused Lamps

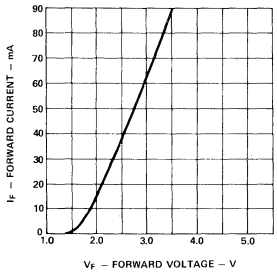


Figure 2. Forward Current vs. Forward Voltage Characteristics.

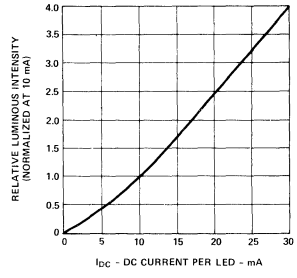


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

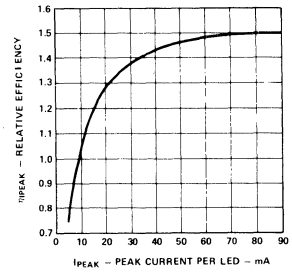


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. LED Peak Current.

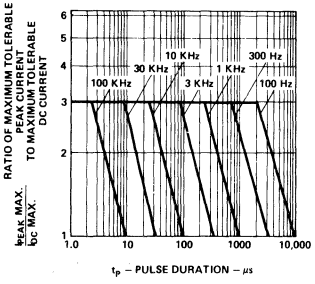


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings

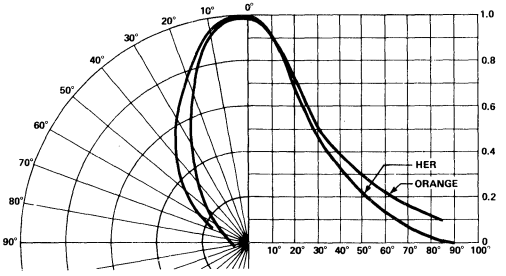


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

T-1¾ Yellow Diffused Lamps

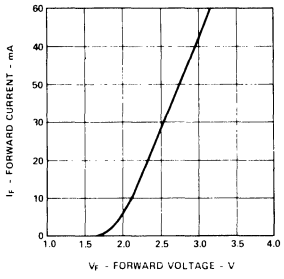


Figure 7. Forward Current vs. Forward Voltage Characteristics.

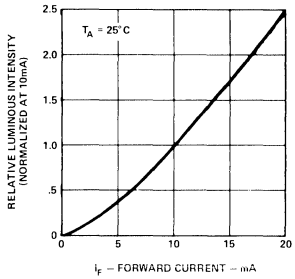


Figure 8. Relative Luminous Intensity vs. Forward Current.

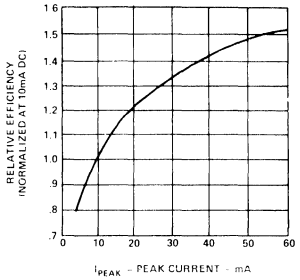


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

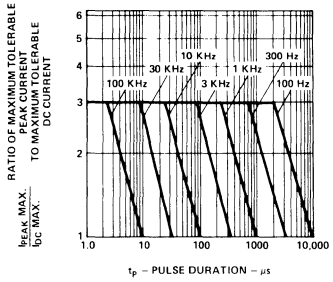


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

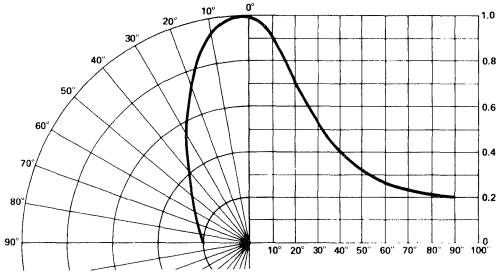


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

T-1¾ Green Diffused Lamps

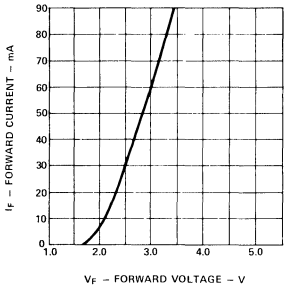


Figure 12. Forward Current vs. Forward Voltage Characteristics.

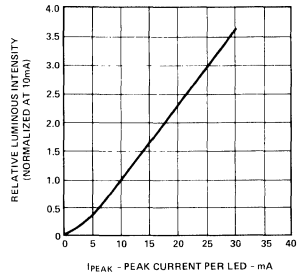


Figure 13. Relative Luminous Intensity vs. DC Forward Current.

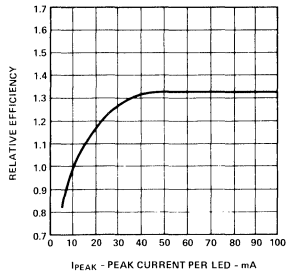


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

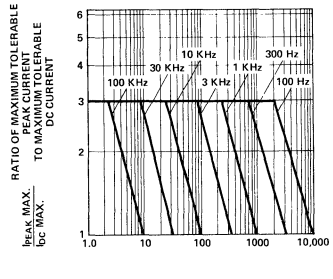


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

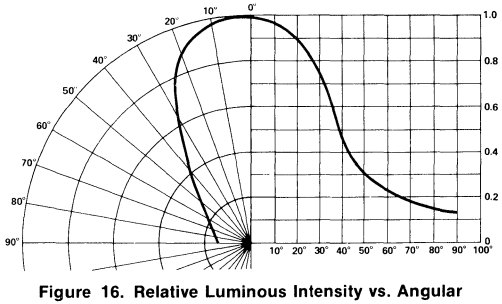


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

T-1 3/4 (5mm) LOW PROFILE SOLID STATE LAMPS

RED ● HLMP-3200 SERIES
HIGH EFFICIENCY RED ● HLMP-3350 SERIES
YELLOW ● HLMP-3450 SERIES
HIGH PERFORMANCE GREEN ● HLMP-3550 SERIES

Features

- **HIGH INTENSITY**
- **LOW PROFILE: 5.8mm (0.23 in) NOMINAL**
- **T-1¾ DIAMETER PACKAGE**
- **DIFFUSED AND NON-DIFFUSED TYPES**
- **GENERAL PURPOSE LEADS**
- **IC COMPATIBLE/LOW CURRENT REQUIREMENTS**
- **RELIABLE AND RUGGED**

Description

The HLMP-3200 Series are Gallium Arsenide Phosphide Red Light Emitting Diodes with a red diffused lens.

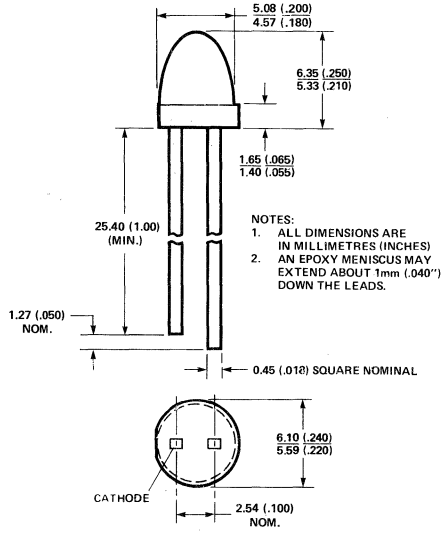
The HLMP-3350 Series are Gallium Arsenide Phosphide on Gallium Phosphide High Efficiency Red Light Emitting Diodes.

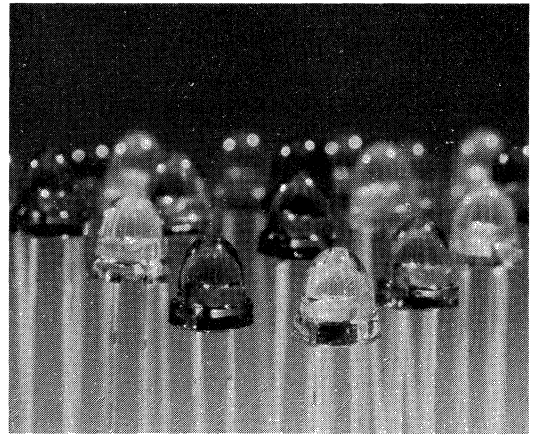
The HLMP-3450 Series are Gallium Arsenide Phosphide on Gallium Phosphide Yellow Light Emitting Diodes.

The HLMP-3550 Series are Gallium Phosphide Green Light Emitting Diodes.

The Low Profile T-1¾ package provides space savings and is excellent for backlighting applications.

Package Dimensions





Number HLMP-	Application	Minimum Intensity @ 10 mA (mcd)	Lens
3200	Indicator — General Purpose	1.0	Tinted Diffused Wide Angle Red
3201	Indicator — High Brightness	2.0	
3350	Indicator — General Purpose	2.0	Tinted Diffused Wide Angle HER
3351	Indicator — High Brightness	5.0	
3365	General Purpose Point Source	7.0	Tinted Non-diffused Narrow Angle HER
3366	Indicator — High Brightness	12.0	
3450	Indicator — General Purpose	2.5	Tinted Diffused Wide Angle Yellow
3451	Indicator — High Brightness	6.0	
3465	General Purpose Point Source	6.0	Tinted Non-diffused Narrow Angle Yellow
3466	Indicator — High Brightness	12.0	
3553	Indicator — General Purpose	1.6	Tinted Diffused Wide Angle Green
3554	Indicator — High Brightness	6.7	
3567	General Purpose Point Source	4.2	Tinted Non-diffused Narrow Angle Green
3568	Indicator — High Brightness	10.6	

RED HLMP-3200 SERIES

Electrical Specifications at T_A=25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3200	1.0	2.0		mcd	I_F = 20 mA (Figure 3)
		3201	2.0	4.0			
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points			60		deg.	Note 1 (Figure 6)
λ_{PEAK}	Peak Wavelength			655		nm	Measurement at Peak (Fig. 1)
λ_d	Dominant Wavelength			648		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth			24		nm	
τ_s	Speed of Response			10		ns	
C	Capacitance			100		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.4	1.6	2.0	V	I_F = 20 mA (Fig. 2)
V_R	Reverse Breakdown Voltage		5.0			V	I_R = 100 μA
η_V	Luminous Efficacy			65		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

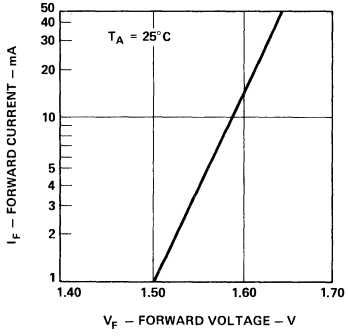


Figure 2. Forward Current versus Forward Voltage.

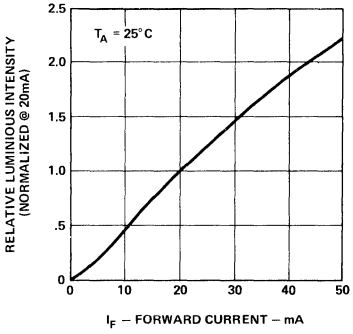


Figure 3. Relative Luminous Intensity versus Forward Current.

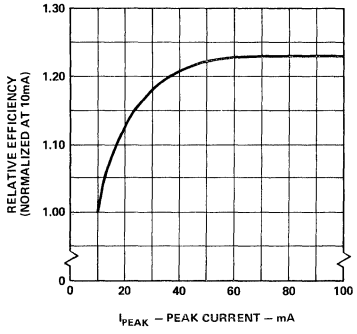


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

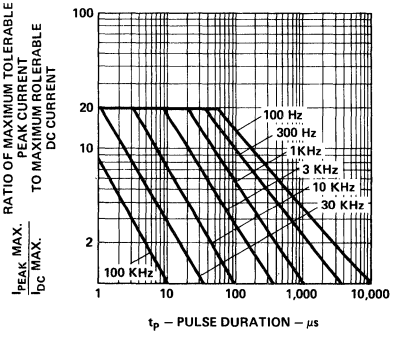


Figure 5. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

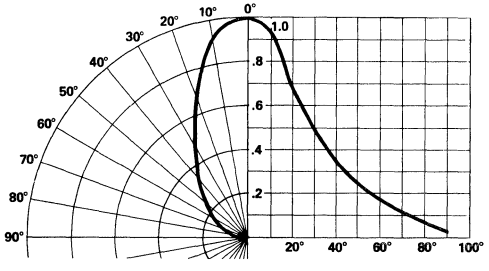


Figure 6. Relative Luminous Intensity versus Angular Displacement.

GREEN HLMP-3550 SERIES
Electrical Specifications at T_A=25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3553 3554 3567 3568	1.6 6.7 4.2 10.6	3.2 10.0 7.0 15.0		mcd	I_F = 10 mA (Fig. 18)
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	3553 3554 3567 3568		50 50 40 40		Deg.	Note 1 (Figure 21)
λ_{PEAK}	Peak Wavelength			565		nm	Measurement at Peak (Fig. 1)
λ_d	Dominant Wavelength			569		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth			28		nm	
τ_s	Speed of Response			500		ns	
C	Capacitance			18		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.5	2.3	3.0	V	I_F = 10 mA (Fig. 17)
V_R	Reverse Breakdown Voltage		5.0			V	I_R = 100 μA
η_V	Luminous Efficacy			595		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

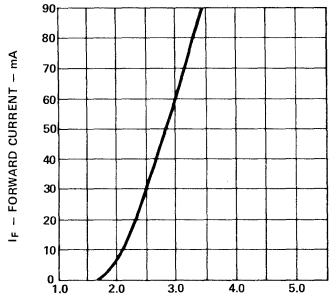


Figure 17. Forward Current versus Forward Voltage.

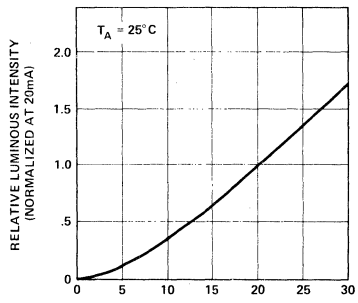


Figure 18. Relative Luminous Intensity versus Forward Current.

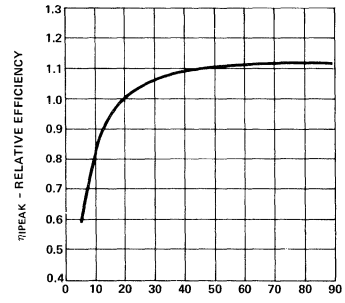


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

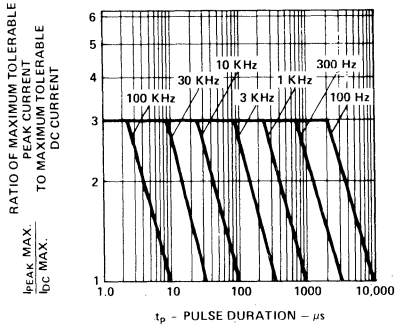


Figure 20. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX ratings).

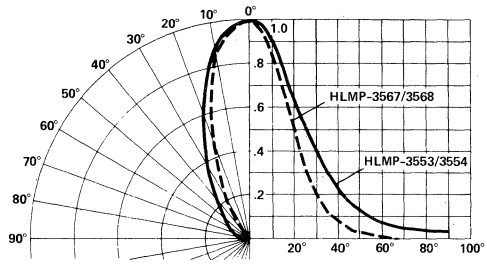


Figure 21. Relative Luminous Intensity versus Angular Displacement.

HIGH EFFICIENCY RED HLMP-3350 SERIES

Electrical Specifications at T_A=25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3350	2.0	3.5		mcd	I_F = 10 mA (Fig. 8)
		3351	5.0	7.0			
		3365	7.0	10.0			
		3366	12.0	18.0			
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	3350		50		Deg.	Note 1 (Fig. 11)
		3351		50			
		3365		45			
		3366		45			
λ_{PEAK}	Peak Wavelength			635		nm	Measurement at Peak (Fig. 1)
λ_d	Dominant Wavelength			626		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth			40		nm	
τ_s	Speed of Response			90		ns	
C	Capacitance			11		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.5	2.2	3.0	V	I_F = 10 mA (Fig. 7)
V_R	Reverse Breakdown Voltage		5.0			V	I_R = 100 μA
η_V	Luminous Efficacy			145		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

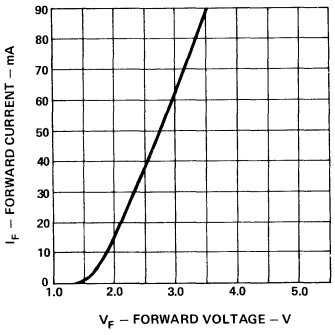


Figure 7. Forward Current versus Forward Voltage.

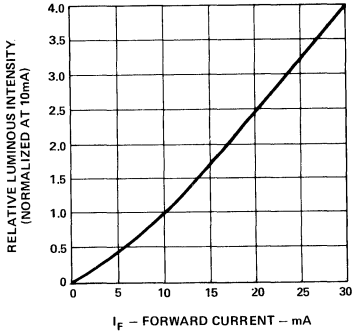


Figure 8. Relative Luminous Intensity versus Forward Current.

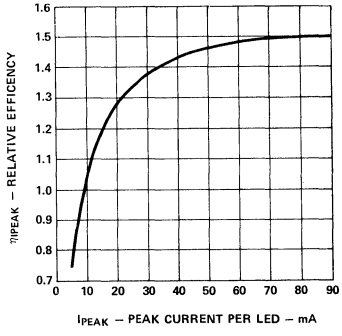


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

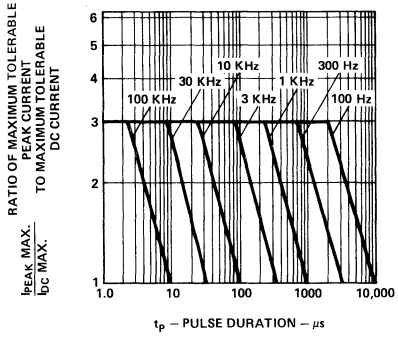


Figure 10. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

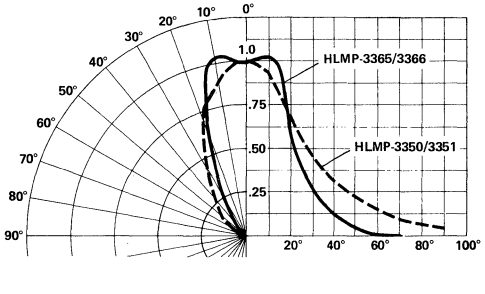


Figure 11. Relative Luminous Intensity versus Angular Displacement.

YELLOW HLMP-3450 SERIES

Electrical Specifications at T_A=25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3450	2.5	4.0		mcd	I_F = 10 mA (Fig. 13)
		3451	6.0	10.0			
		3465	6.0	12.0			
		3466	12.0	18.0			
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	3450		50		Deg.	Note 1 (Fig. 16)
		3451		50			
		3465		45			
		3466		45			
λ_{PEAK}	Peak Wavelength			583		nm	Measurement at Peak (Fig. 1)
λ_d	Dominant Wavelength			585		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth			36		nm	
τ_s	Speed of Response			90		ns	
C	Capacitance			15		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.5	2.2	3.0	V	I_F = 10 mA (Fig. 12)
V_R	Reverse Breakdown Voltage		5.0			V	I_R = 100 μA
η_V	Luminous Efficacy			500		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

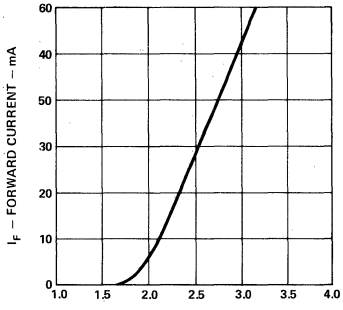


Figure 12. Forward Current versus Forward Voltage.

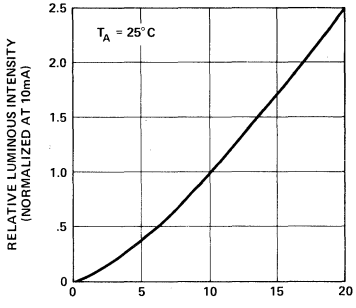


Figure 13. Relative Luminous Intensity versus Forward Current.

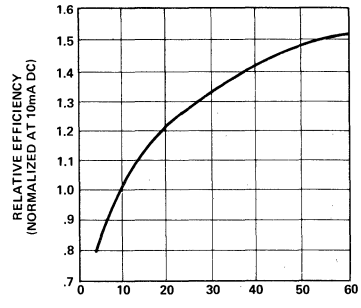


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

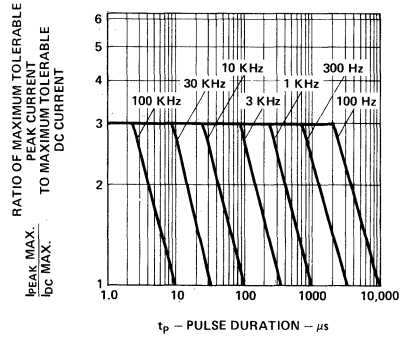


Figure 15. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings).

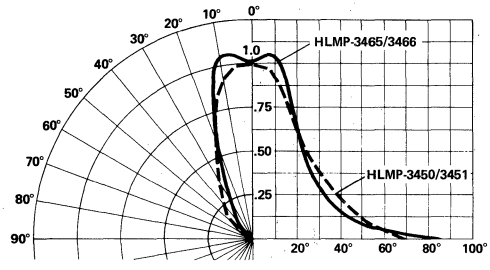


Figure 16. Relative Luminous Intensity versus Angular Displacement

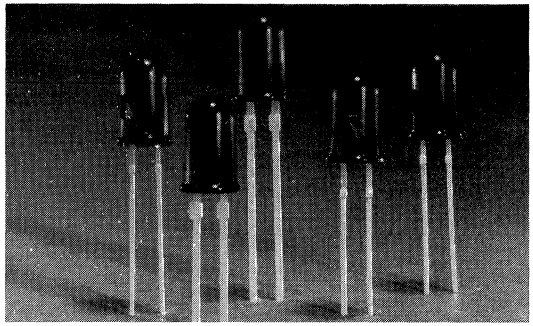
HEWLETT PACKARD

T-1 3/4 (5mm) RED SOLID STATE LAMPS

HLMP-3000
HLMP-3001
HLMP-3002
HLMP-3003
HLMP-3050

Features

- **LOW COST, BROAD APPLICATIONS**
- **LONG LIFE, SOLID STATE RELIABILITY**
- **LOW POWER REQUIREMENTS: 20 mA @ 1.6V**
- **HIGH LIGHT OUTPUT:**
  2.0 mcd Typical for HLMP-3000
  4.0 mcd Typical for HLMP-3001
- **WIDE AND NARROW VIEWING ANGLE TYPES**
- **RED DIFFUSED AND NON-DIFFUSED VERSIONS**



Description

The HLMP-3000 series lamps are Gallium Arsenide Phosphide light emitting diodes intended for High Volume/ Low Cost applications such as indicators for appliances, smoke detectors, automobile instrument panels and many other commercial uses.

The HLMP-3000/-3001/-3002/-3003 have red diffused lenses where as the HLMP-3050 has a red non-diffused lens. These lamps can be panel mounted using mounting clip HLMP-0103. The HLMP-3000/-3001 lamps have .025" leads and the HLMP-3002/-3003/-3050 have .018" leads.

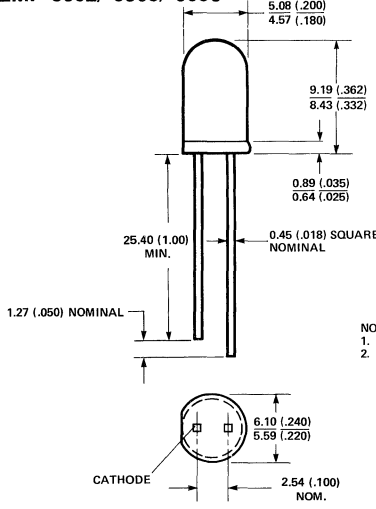
NOTES:
1. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	3000 Series	Units
Power Dissipation	100	mW
DC Forward Current (Derate linearly from 50° C at 0.2 mA/° C)	50	mA
Average Forward Current	50	mA
Peak Operating Forward Current	1000	mA
Reverse Voltage (I_R = 100 μA)	5	V
Transient Forward Current[1] (10 μsec Pulse)	2000	mA
Operating and Storage Temperature Range	-55° C to +100° C	
Lead Solder Temperature (1.6 mm [0.063 inch] below package base)	260° C for 5 seconds	

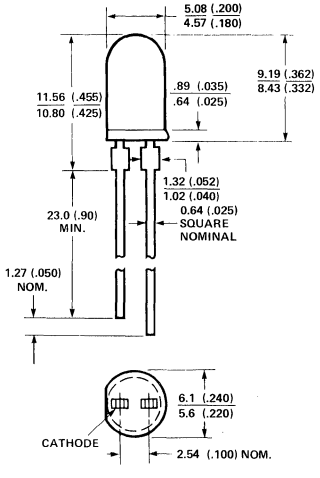
Package Dimensions

HLMP-3002/-3003/-3050



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

HLMP-3000/-3001



Electrical Characteristics at T_A=25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	3000/3002	1.0	2.0		mcd	I_F = 20 mA
		3001/3003	2.0	4.0		mcd	I_F = 20 mA
		3050	1.0	2.5		mcd	I_F = 20 mA
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	3000/3002		60		Deg.	I_F = 20 mA
		3001/3003		60			
		3050		24			
λ_P	Peak Wavelength	3000/3002		655		nm	Measurement at Peak
		3001/3003		655			
		3050		655			
λ_d	Dominant Wavelength	3000/3002		648		nm	
		3001/3003					
		3050					
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	3000/3002		24		nm	
		3001/3003					
		3050					
τ_S	Speed of Response	3000/3002		10		ns	
		3001/3003					
		3050					
C	Capacitance	3000/3002		100		pF	V_F = 0, f = 1 MHz
		3001/3003					
		3050					
Θ_{JC}	Thermal Resistance	3000/3001		95		°C/W	Junction to Cathode Lead
		3002/3003		120			
		3050		120			
V_F	Forward Voltage	3000/3002	1.4	1.6	2.0	V	I_F = 20 mA (Fig. 2)
		3001/3003					
		3050					
V_R	Reverse Breakdown Voltage	3000/3002	5.0			V	I_R = 100 μA
		3001/3003					
		3050					

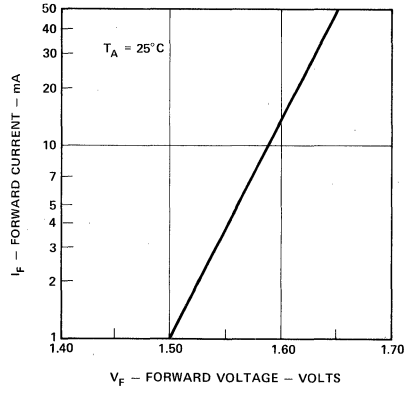


Figure 1. Forward Current Versus Forward Voltage

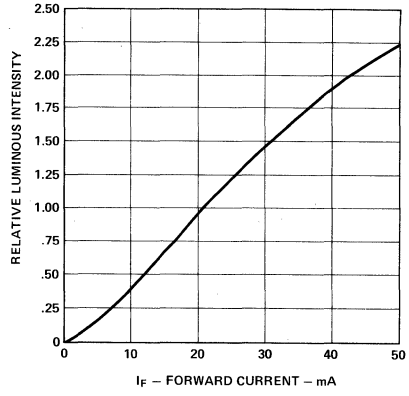


Figure 2. Relative Luminous Intensity Versus Forward Current

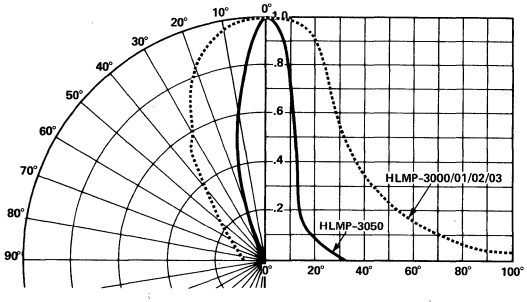


Figure 3. Relative Luminous Intensity Versus Angular Displacement.

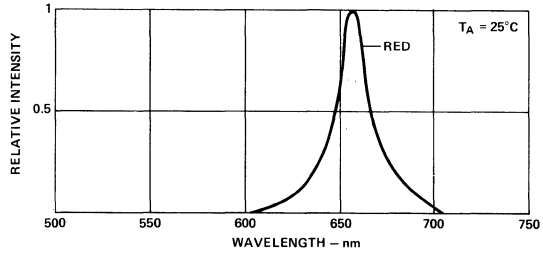


Figure 4. Relative Luminous Intensity Versus Wavelength.

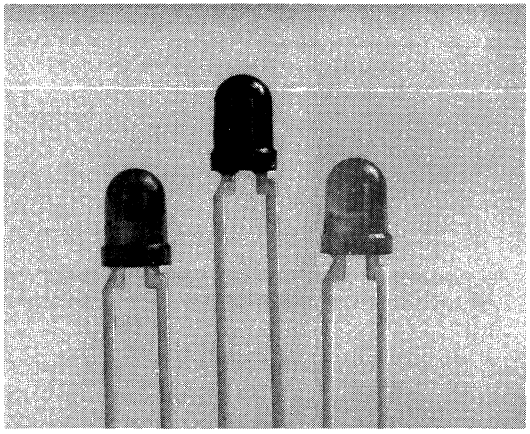
HEWLETT PACKARD

T-1 (3 mm)
HIGH INTENSITY SOLID STATE LAMPS

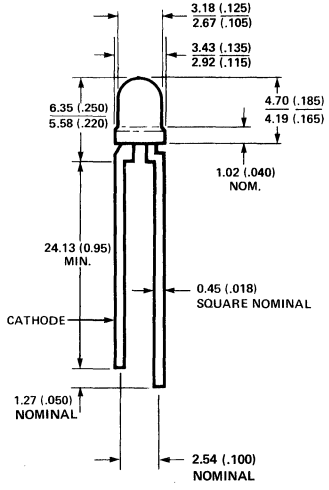
HIGH EFFICIENCY RED • HLMP-132X SERIES
YELLOW • HLMP-142X SERIES
HIGH PERFORMANCE GREEN • HLMP-152X SERIES

Features

- HIGH INTENSITY
- CHOICE OF 3 BRIGHT COLORS
  - High Efficiency Red
  - Yellow
  - High Performance Green
- POPULAR T-1 DIAMETER PACKAGE
- SELECTED MINIMUM INTENSITIES
- NARROW VIEWING ANGLE
- GENERAL PURPOSE LEADS
- RELIABLE AND RUGGED
- AVAILABLE ON TAPE AND REEL



Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Description

This family of T-1 lamps is specially designed for applications requiring higher on-axis intensity than is achievable with a standard lamp. The light generated is focused to a narrow beam to achieve this effect.

Part Number HLMP-	Description	Minimum Intensity (mcd) at 10 mA	Color (Material)
1320	Untinted Non-Diffused	8.6	High Efficiency Red (GaAsP on GaP)
1321	Tinted Non-Diffused	8.6	
1420	Untinted Non-Diffused	9.2	Yellow (GaAsP on GaP)
1421	Tinted Non-Diffused	6.0	
1520	Untinted Non-Diffused	4.2	Green (GaP)
1521	Tinted Non-Diffused	4.2	

Electrical Characteristics at $T_A = 25°C$

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	1320 1321	8.6 8.6	12.0 12.0		mcd	I_F = 10 mA (Figure 3)
		1420 1421	9.2 6.0	12.0 12.0		mcd	I_F = 10 mA (Figure 8)
		1520 1521	4.2 4.2	12.0 12.0		mcd	I_F = 10 mA (Figure 3)
$2\Theta_{1/2}$	Including Angle Between Half Luminous Intensity Points	All		45		Deg.	I_F = 10 mA See Note 1 (Figures 6, 11, 16, 21)
λ_{PEAK}	Peak Wavelength	132X 142X 152X		635 583 565		nm	Measurement at Peak (Figure 1)
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	132X 142X 152X		40 36 28		nm	
λ_d	Dominant Wavelength	132X 142X 152X		626 585 569		nm	See Note 2 (Figure 1)
τ_s	Speed of Response	132X 142X 152X		90 90 500		ns	
C	Capacitance	132X 142X 152X		11 15 18		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance	All		120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	132X 142X 152X	1.5 1.5 1.5	2.2 2.2 2.3	3.0 3.0 3.0	V	I_F = 10 mA
V_R	Reverse Breakdown Voltage	All	5.0			V	I_R = 100 μA
η_V	Luminous Efficacy	132X 142X 152X		145 500 595		$\frac{\text{lumens}}{\text{Watt}}$	See Note 3

Notes:
1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	Red	Yellow	Green	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage (I_R = 100 μA)	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	500	500	mA
Operating Temperature Range	−55 to +100	−55 to +100	−20 to +100	°C
Storage Temperature Range			−55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

NOTES:
1. See Figure 5 (Red), 10 (Yellow), or 15 (Green) to establish pulsed operating conditions.
2. For Red and Green series derate linearly from 50° C at 0.5 mA/° C. For Yellow series derate linearly from 50° C at 0.2 mA/° C.
3. For Red and Green series derate power linearly from 25° C at 1.8 mW/° C. For Yellow series derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

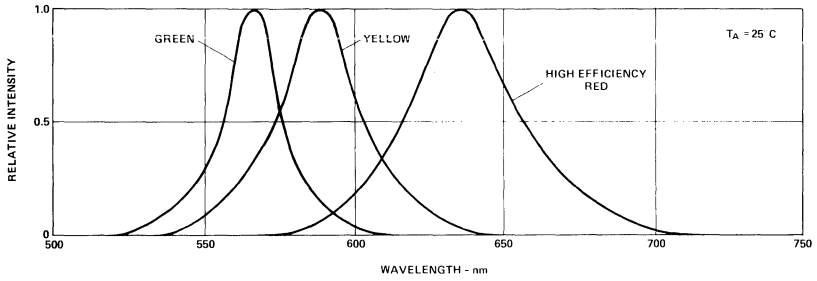


Figure 1. Relative Intensity vs. Wavelength

T-1 High Efficiency Red Non-Diffused

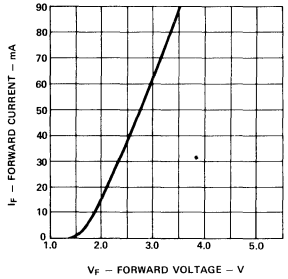


Figure 2. Forward Current vs. Forward Voltage Characteristics

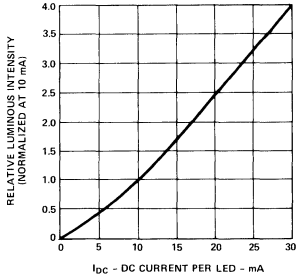


Figure 3. Relative Luminous Intensity vs. DC Forward Current

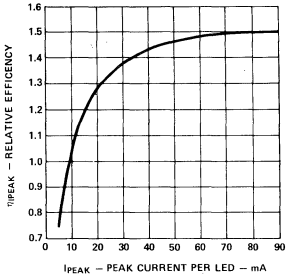


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current

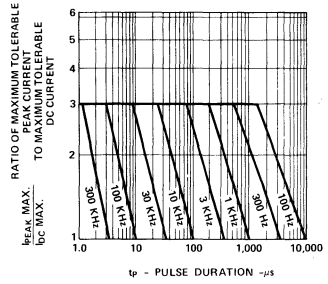


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC}MAX as per MAX Ratings)

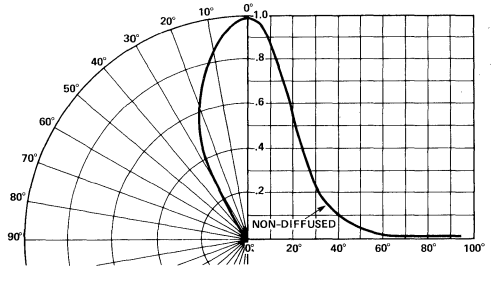


Figure 6. Relative Luminous Intensity vs. Angular Displacement

T-1 Yellow Non-Diffused

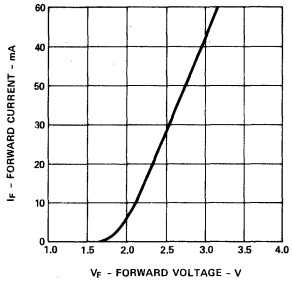


Figure 7. Forward Current vs. Forward Voltage Characteristics

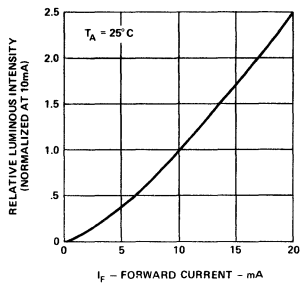


Figure 8. Relative Luminous Intensity vs. Forward Current

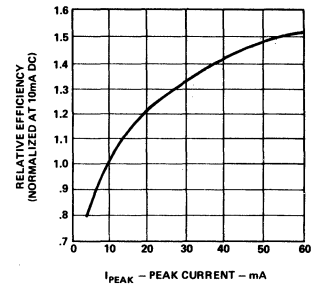


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current

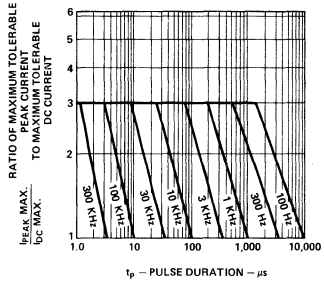


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC}MAX as per MAX Ratings)

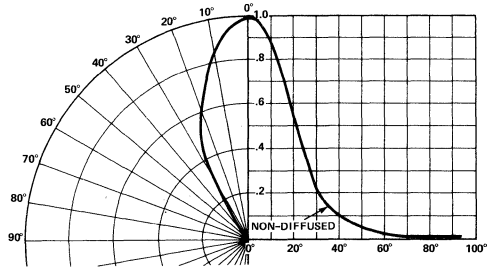


Figure 11. Relative Luminous Intensity vs. Angular Displacement

T-1 Green Non-Diffused

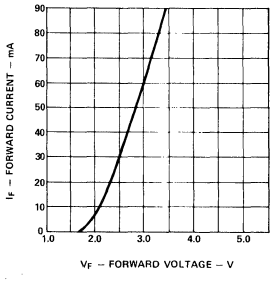


Figure 12. Forward Current vs. Forward Voltage Characteristics

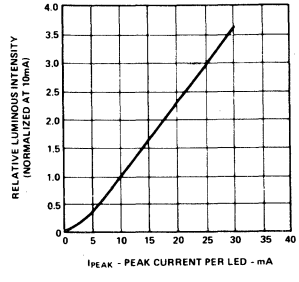


Figure 13. Relative Luminous Intensity vs. Forward Current

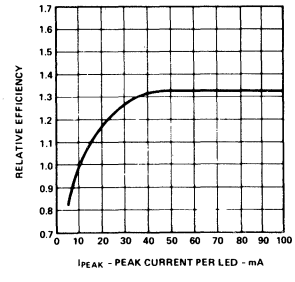


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current

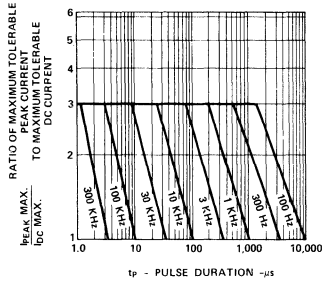


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC}MAX as per MAX Ratings)

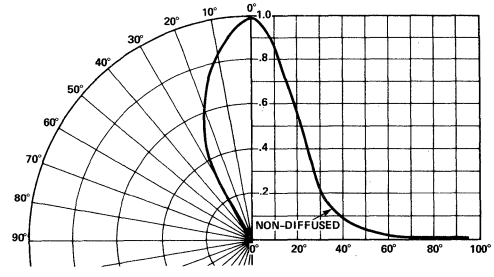


Figure 16. Relative Luminous Intensity vs. Angular Displacement

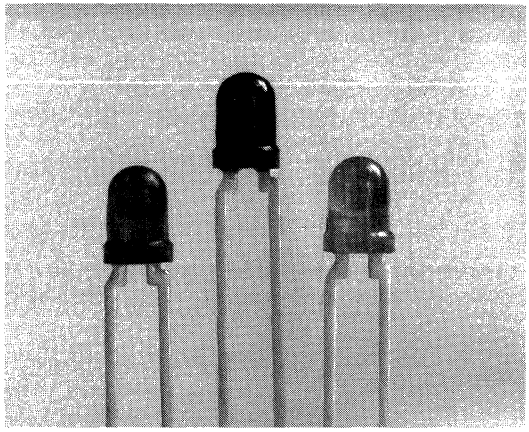
HEWLETT PACKARD

T-1 (3mm) DIFFUSED SOLID STATE LAMPS

HIGH EFFICIENCY RED ● HLMP-1300 SERIES
ORANGE ● HLMP-K400 SERIES
YELLOW ● HLMP-1400 SERIES
HIGH PERFORMANCE GREEN ● HLMP-1500 SERIES

Features

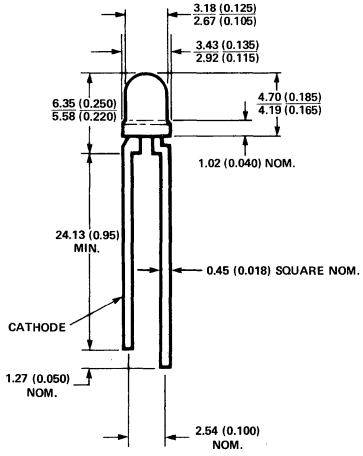
- **HIGH INTENSITY**
- **CHOICE OF 4 BRIGHT COLORS**
  - **High Efficiency Red**
  - **Orange**
  - **Yellow**
  - **High Performance Green**
- **POPULAR T-1 DIAMETER PACKAGE**
- **SELECTED MINIMUM INTENSITIES**
- **WIDE VIEWING ANGLE**
- **GENERAL PURPOSE LEADS**
- **RELIABLE AND RUGGED**
- **AVAILABLE ON TAPE AND REEL**



Description

This family of T-1 lamps is widely used in general purpose indicator applications. Diffusants, tints, and optical design are balanced to yield superior light output and wide viewing angles. Several intensity choices are available in each color for increased design flexibility.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (0.040") DOWN THE LEADS.

Part Number HLMP-	Application	Minimum Intensity (mcd) at 10mA	Color (Material)
1300	General Purpose	1.0	High Efficiency Red (GaAsP on GaP)
1301	General Purpose	2.0	
1302	High Ambient	3.0	
1385	Premium Lamp	6.0	
K400	General Purpose	1.0	Orange (GaAsP on GaP)
K401	High Ambient	2.0	
K402	Premium Lamp	3.0	
1400	General Purpose	1.0	Yellow (GaAsP on GaP)
1401	General Purpose	2.0	
1402	High Ambient	3.0	
1485	Premium Lamp	6.0	
1503	General Purpose	1.0	Green (GaP)
1523	High Ambient	2.6	
1585	Premium Lamp	4.0	

Electrical Characteristics at $T_A = 25°C$

Symbol	Description	Device	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	High Efficiency Red				mcd	$I_F = 10$ mA
		1300	1.0	5.0			
		1301	2.0	5.5			
		1302	3.0	7.0			
		1385	6.0	10.0			
		Orange					
		K400	1.0	4.0			
		K401	2.0	5.0			
		K402	3.0	6.5			
		Yellow					
		1400	1.0	5.0			
		1401	2.0	6.0			
		1402	3.0	7.0			
		1485	6.0	10.0			
		Green					
		1503	1.0	5.0			
		1523	2.6	7.0			
		1585	4.0	8.5			
$2\Theta 1/2$	Including Angle Between Half Luminous Intensity Points	All		60		Deg.	$I_F = 10$ mA See Note 1
λ_{PEAK}	Peak Wavelength	High Efficiency Red		635		nm	Measurement at Peak
		Orange		600			
		Yellow		583			
		Green		565			
λd	Dominant Wavelength	High Efficiency Red		626		nm	See Note 2
		Orange		602			
		Yellow		585			
		Green		569			
$\Delta\lambda 1/2$	Spectral Line Halfwidth	High Efficiency Red		40		nm	
		Yellow		36			
		Green		28			
τs	Speed of Response	High Efficiency Red		90		ns	
		Orange		280			
		Yellow		90			
		Green		500			
C	Capacitance	High Efficiency Red		11		pF	$V_F = 0$; f = 1 MHz
		Orange		4			
		Yellow		15			
		Green		18			
$R\theta_{JC}$	Thermal Resistance	All		120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	HER/Orange	1.5	2.2	3.0	V	$I_F = 10$ mA
		Yellow	1.5	2.2	3.0		
		Green	1.5	2.3	3.0		
V_R	Reverse Breakdown Volt.	All	5.0			V	$I_R = 100\ \mu A$
ηv	Luminous Efficacy	High Efficiency Red		145		$\frac{\text{lumens}}{\text{Watt}}$	See Note 3
		Orange		380			
		Yellow		500			
		Green		595			

NOTES:

1. $\Theta 1/2$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	HER/Orange	Yellow	Green	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Reverse Voltage ($I_R = 100\ \mu A$)	5	5	5	V
Transient Forward Current[4] (10 μsec Pulse)	500	500	500	mA
Operating Temperature Range	−55 to +100	−55 to +100	−20 to +100	°C
Storage Temperature Range			−55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

NOTES:

1. See Figure 5 (Red/Orange), 10 (Yellow) or 15 (Green) to establish pulsed operating conditions.
2. For Red, Orange, and Green series derate linearly from 50° C at 0.5 mA/° C. For Yellow series derate linearly from 50° C at 0.2 mA/° C.
3. For Red, Orange, and Green series derate power linearly from 25° C at 1.8 mW/° C. For Yellow series derate power linearly from 50° C at 1.6 mW/° C.
4. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

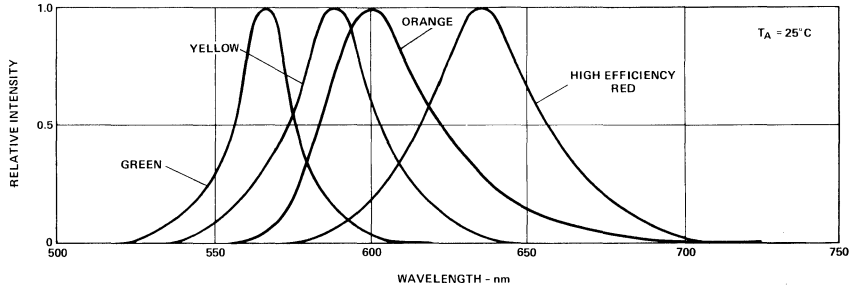


Figure 1. Relative Intensity vs. Wavelength

T-1 High Efficiency Red, Orange Diffused Lamps

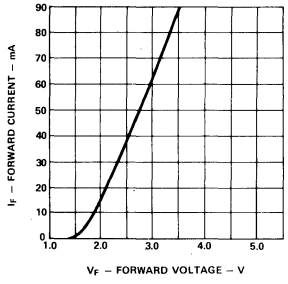


Figure 2. Forward Current vs. Forward Voltage Characteristics.

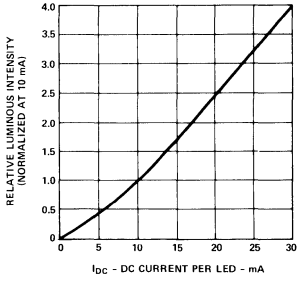


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

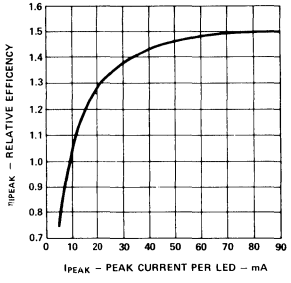


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

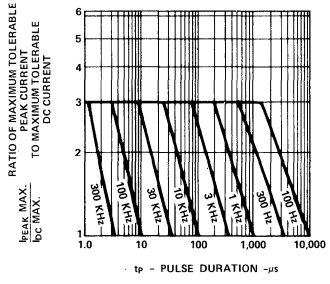


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

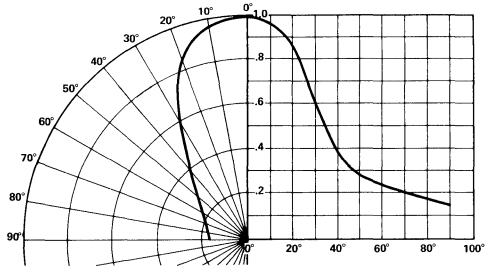


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

T-1 Yellow Diffused Lamps

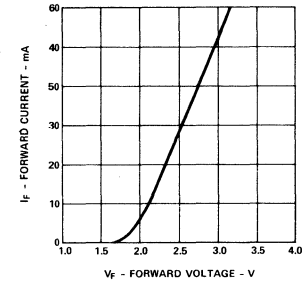


Figure 7. Forward Current vs. Forward Voltage Characteristics.

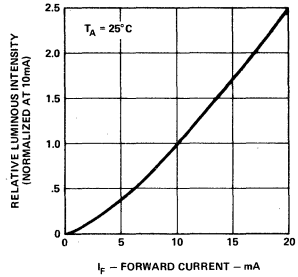


Figure 8. Relative Luminous Intensity vs. Forward Current.

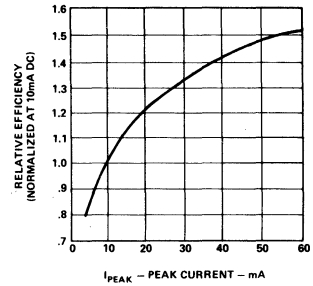


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

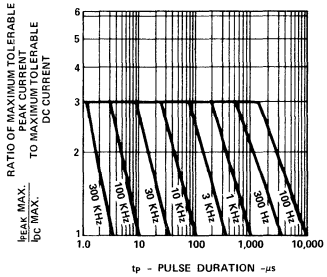


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

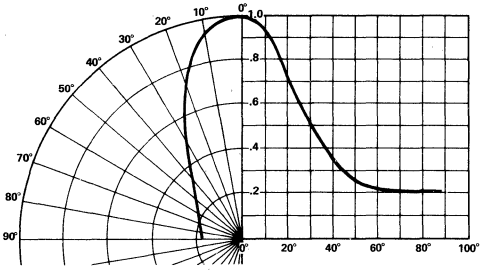


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

T-1 Green Diffused Lamps

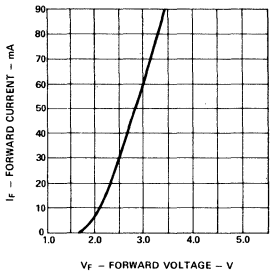


Figure 12. Forward Current vs. Forward Voltage Characteristics.

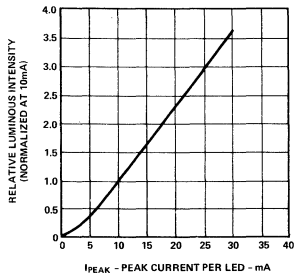


Figure 13. Relative Luminous Intensity vs. Forward Current.

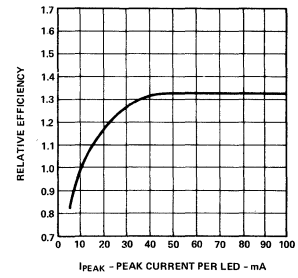


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

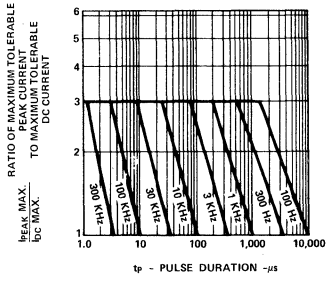


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

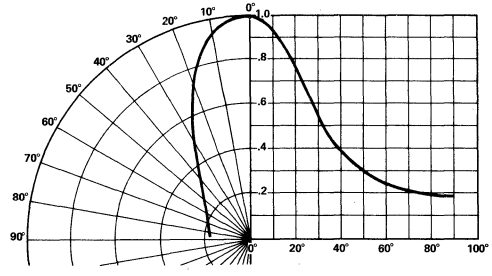


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

T-1 (3mm) RED SOLID STATE LAMPS

HLMP-1000 Series
HLMP-1200 Series

Features

- **WIDE VIEWING ANGLE**
- **SMALL SIZE T-1 DIAMETER 3.18mm (0.125")**
- **IC COMPATIBLE**
- **RELIABLE AND RUGGED**

Description

The HLMP-1000 is a series of Gallium Arsenide Phosphide Light Emitting Diodes designed for applications where space is at a premium, such as in high density arrays.

The HLMP-1000 series is available in three lens configurations.

HLMP-1000 — Red Diffused lens provides excellent on-off contrast ratio, high axial luminous intensity, and wide viewing angle.

HLMP-1080 — Same as HLMP-1000, but untinted diffused to mask red color in the "off" condition.

HLMP-1071/-1201 — Untinted non-diffused plastic lens provides a point source. Useful when illuminating external lens, annunciators, or photo-detectors.

Part Number HLMP-	Package & Lens Type	Iv (mcd) @ 20 mA		Typ. Viewing Angle 2Θ 1/2
		Min.	Typ.	
-1000	A-Tinted Diffused	.5	1.0	60°
-1002	A-Tinted Diffused	1.5	2.5	60°
-1080	A-Untinted Diffused	.5	1.5	60°
-1071	A-Untinted Non-Diffused	1.0	2.0	45°
-1200	B-Untinted Non-Diffused	.5	1.0	55°
-1201	B-Untinted Non-Diffused	1.5	2.5	55°

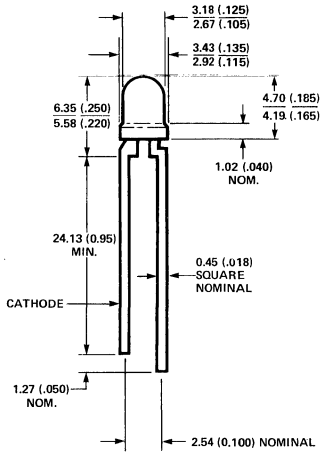


Figure A.

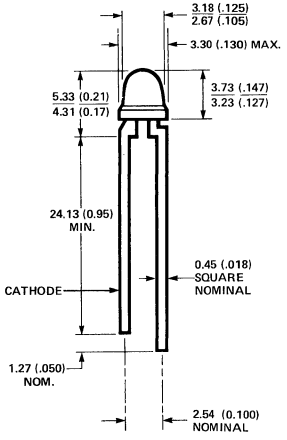


Figure B.

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	1000 Series	Units
Power Dissipation	100	mW
DC Forward Current [1]	50	mA
Average Forward Current	50	mA
Peak Operating Forward Current	1000	mA
Reverse Voltage (I_R = 100 μA)	5	V
Transient Forward Current[1] (10 μsec Pulse)	2000	mA
Operating and Storage Temperature Range	−55° C to +100° C	
Lead Solder Temperature (1.6 mm [0.063 inch] below package base)	260° C for 5 seconds	

Note:
1. Derate linerarly from 50°C at 0.2 mA/°C.

Electrical Characteristics at T_A=25°C

Symbol	Parameters	Min.	Typ.	Max.	Units	Test Conditions
λ_{PEAK}	Peak Wavelength		655		nm	Measurement at Peak
λ_d	Dominant Wavelength		648		nm	
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth		24		nm	
τ_s	Speed of Response		10		ns	
C	Capacitance		100		pF	V_F = 0, f = 1 MHz
θ_{JC}	Thermal Resistance		120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	1.4	1.6	2.0	V	I_F = 20 mA
V_R	Reverse Breakdown Voltage	5			V	I_R = 100 μA

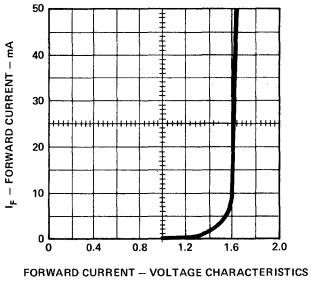


Figure 1. Forward Current vs. Voltage Characteristic.

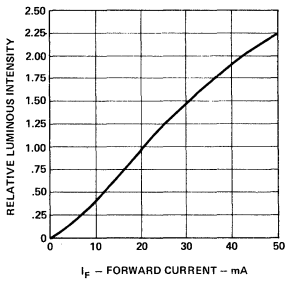


Figure 2. Luminous Intensity vs. Forward Current (IF).

HLMP-1200/-1201

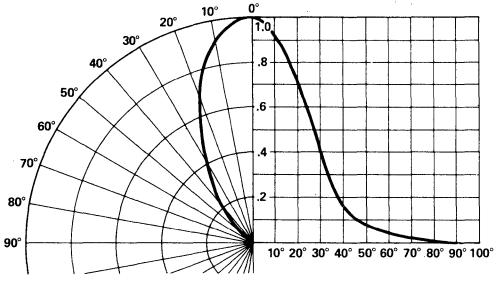


Figure 3. Typical Relative Luminous Intensity vs. Angular Displacement.

HLMP-1000/-1002/-1080

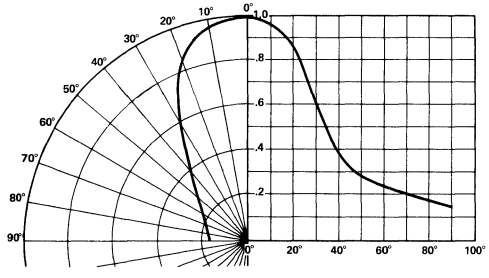


Figure 4. Relative Luminous Intensity vs. Angular Displacement.

HLMP-1071

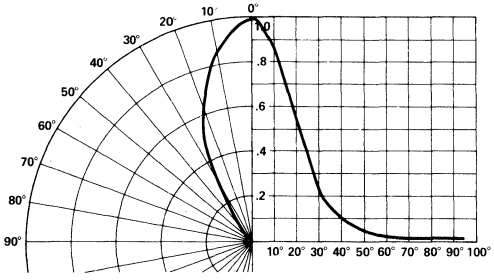


Figure 5. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

Rectangular Solid State Lamps

Technical Data

HLMP-R100
HLMP-0300/0301
HLMP-0400/0401
HLMP-0503/0504

SOLID STATE LAMPS

Features

- **Rectangular Light Emitting Surface**
- **Flat High Sterance Emitting Surface**
- **Stackable on 2.54 mm (0.100 inch) Centers**
- **Ideal as Flush Mounted Panel Indicators**
- **Ideal for Backlighting Legends**
- **Long Life: Solid State Reliability**
- **Choice of 4 Bright Colors**
  - DH AS AlGaAs Red
  - High Efficiency Red
  - Yellow
  - High Performance Green
- **IC Compatible/Low Current Requirements**

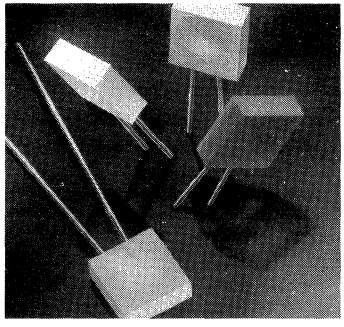
Description

The HLMP–R100, -030X, -040X, -050X are solid state lamps encapsulated in a radial lead rectangular epoxy package. They utilize a tinted, diffused epoxy to provide high on-off contrast and a flat high intensity emitting surface. Borderless package design allows creation of uninterrupted light emitting areas.

The HLMP-R100 uses a double heterojunction (DH) absorbing substrate (AS) aluminum gallium arsenide (AlGaAs) red LED chip in a light red epoxy package. This combination produces outstanding light output over a wide range of drive currents.

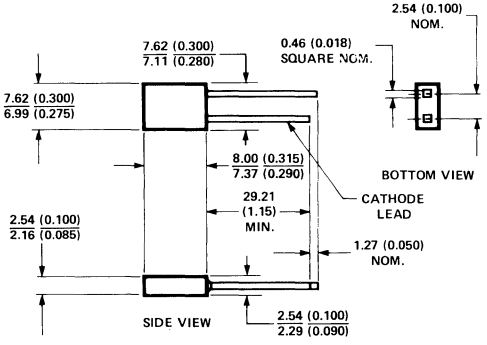
The HLMP-0300 and -0301 have a high efficiency red GaAsP on GaP LED chip in a light red epoxy package.

The HLMP-0400 and -0401 provide a yellow GaAsP on GaP LED chip in a yellow epoxy package.



The HLMP-0503 and -0504 provide a green GaP LED chip in a green epoxy package.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.
3. THERE IS A MAXIMUM 1° TAPER FROM BASE TO TOP OF LAMP.

Axial Luminous Intensity

Color	Part Number	I_v (mcd) @ 20 mA DC	
		Min.	Typ.
AlGaAs Red	HLMP-R100	3.4	7.5
High Efficiency Red	HLMP-0300	1.0	2.5
	HLMP-0301	2.5	5.0
Yellow	HLMP-0400	1.5	2.5
	HLMP-0401	3.0	5.0
High Performance Green	HLMP-0503	1.5	2.5
	HLMP-0504	3.0	5.0

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	HLMP-R100	HLMP-0300/-0301	HLMP-0400/0401	HLMP-0503/-0504	Units
Peak Forward Current	300	90	60	90	mA
Average Forward Current[1]	20	25	20	25	mA
DC Current[2]	30	30	20	30	mA
Power Dissipation	87	135	85	135	mW
Reverse Voltage (I_R = 100 μA)	5	5	5	5	V
Transient Forward Current[3] (10 μs Pulse)	500	500	500	500	mA
Operating Temperature Range	-20 to +100	-55 to +100	-55 to +100	-20 to +100	°C
Storage Temperature Range	-55 to +100			-55 to +100	
Lead Soldering Temperature (1.6 mm [0.063 in.] from body)	260°C for 5 seconds				

Notes:
1. See Figure 5 to establish pulsed operating conditions.
2. For AlGaAs Red, Red, and Green Series derate linearly from 50°C at 0.5 mA/°C. For Yellow Series derate linearly from 50°C at 0.2 mA/°C.
3. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak current beyond the peak forward current listed in the Absolute Maximum Ratings.

Electrical/Optical Characteristics at T_A = 25°C

Sym.	Description	HLMP-R100			HLMP -0300/-0301			HLMP -0400/-0401			HLMP -0503/-0504			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		100			100			100			100		Deg.	Note 1. Fig. 6
λ_p	Peak Wavelength		645			635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		637			626			585			569		nm	Note 2
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth		20			40			36			28		nm	
τ_s	Speed of Response		30			90			90			500		ns	
C	Capacitance		30			16			18			18		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance		220			120			120			120		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	1.6	1.8	2.2	1.6	2.2	3.0	1.6	2.2	3.0	1.6	2.3	3.0	V	I_F = 20 mA Figure 2.
V_R	Reverse Breakdown Voltage	5.0			5.0			5.0			5.0			V	I_R = 100 μA
η_v	Luminous Efficacy		80			145			500			595		lm/W	Note 3

Notes:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

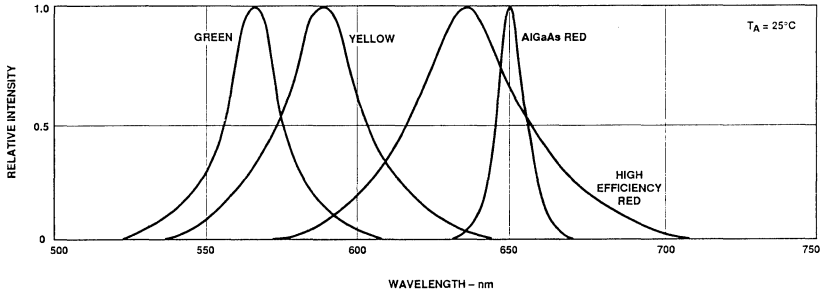


Figure 1. Relative Intensity vs. Wavelength.

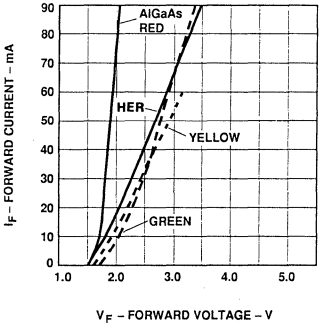


Figure 2. Forward Current vs. Forward Voltage. V_F (300 mA) for AlGaAs Red = 2.6 Volts Typical.

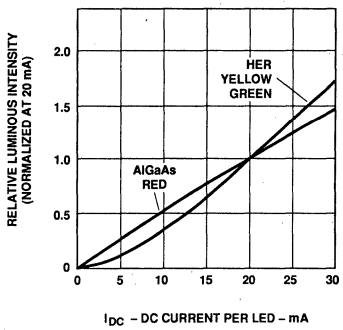


Figure 3. Relative Luminous Intensity vs. Forward Current.

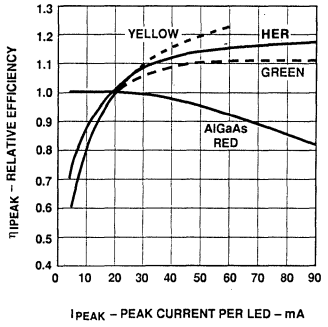
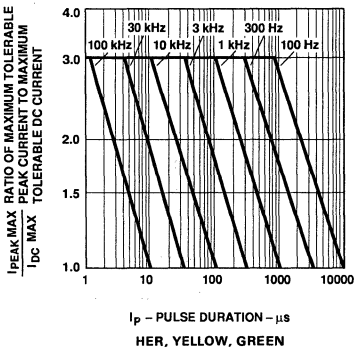


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current. η_v (300 mA) for AlGaAs Red = 0.7.



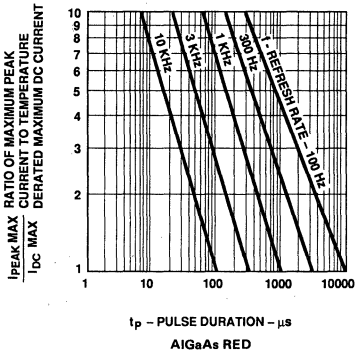


Figure 5. Maximum Tolerable Peak Current vs. Peak Duration (I_{PEAK} MAX Determined from Temperature Derated I_{DC} MAX).

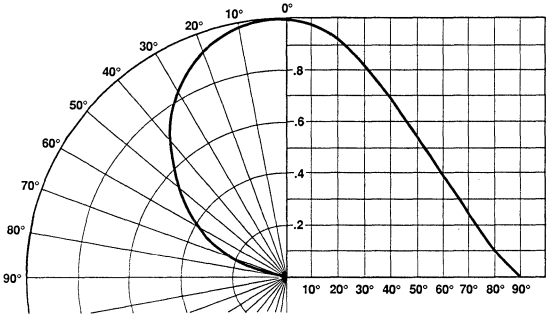


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

2 mm x 5 mm Rectangular Lamps

Technical Data

HLMP-S100 Series
HLMP-S200 Series
HLMP-S300 Series
HLMP-S400 Series
HLMP-S500 Series

Features

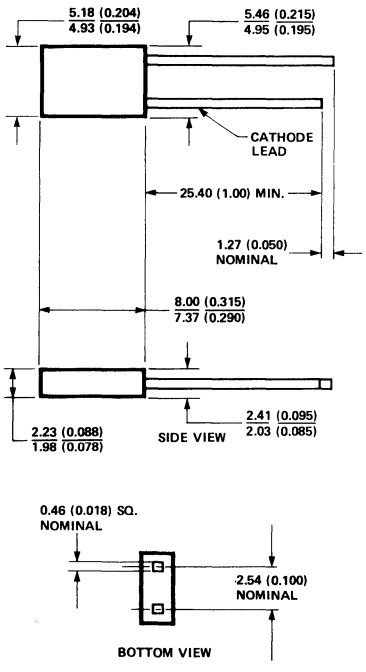
- **Rectangular Light Emitting Surface**
- **Excellent for Flush Mounting on Panels**
- **Choice of Five Bright Colors**
- **Long Life: Solid State Reliability**
- **Excellent Uniformity of Light Output**

Description

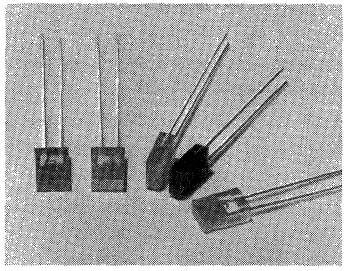
The HLMP-S100, -S200, -S300, -S400, -S500 are epoxy encapsulated lamps in rectangular packages which are easily stacked in arrays or used for discrete front panel indicators. Contrast and light uniformity are enhanced by a special epoxy diffusion and tinting process.

The HLMP-S100 uses double heterojunction (DH) absorbing substrate (AS) aluminum gallium arsenide (AlGaAs) LEDs to produce outstanding light output over a wide range of drive currents.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.
3. THERE IS A MAXIMUM 1° TAPER FROM BASE TO THE TOP OF LAMP.



Electrical/Optical Characteristics at $T_A = 25°C$

Sym.	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_v	Luminous Intensity	AlGaAs Red S100 High Efficiency Red S200 S201 Orange S400 S401 Yellow S300 S301 Green S500 S501	 3.6 2.1 3.4 2.1 3.4 1.4 2.2 2.6 4.1	 7.5 3.5 4.8 3.5 4.8 2.1 3.5 4.0 5.8		mcd	$I_F = 20$ mA
2θ1/2	Included Angle Between Half Luminous Intensity Points	All		110		Deg.	$I_F = 20$ mA See Note 1
λ_{PEAK}	Peak Wavelength	AlGaAs Red High Efficiency Red Orange Yellow Green		645 635 600 583 565		nm	Measurement at Peak
λ_d	Dominant Wavelength	AlGaAs Red High Efficiency Red Orange Yellow Green		637 626 602 585 569		nm	See Note 2
τ_s	Speed of Response	AlGaAs Red High Efficiency Red Orange Yellow Green		30 350 350 390 870		ns	
C	Capacitance	AlGaAs Red High Efficiency Red Orange Yellow Green		30 11 4 15 18		pF	$V_F = 0$; f = 1 MHz
$R\theta_{JC}$	Thermal Resistance	AlGaAs Red All Others		220 120		°C/W	Junction to Cathode Lead at Seating Plane
V_F	Forward Voltage	AlGaAs Red HER/Orange Yellow Green	1.6 1.5 1.5 1.5	1.8 2.2 2.2 2.3	2.2 3.0 3.0 3.0	V	$I_F = 20$ mA
V_R	Reverse Break-down Voltage	All	5.0			V	$I_R = 100\ \mu A$
η_V	Luminous Efficacy	AlGaAs Red High Efficiency Red Orange Yellow Green		80 145 380 500 595		lumens/ watt	See Note 3

Notes:

1. θ1/2 is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at T_A = 25°C

Parameter	AlGaAs Red	High Efficiency Red/Orange	Yellow	Green	Units
Peak Forward Current	300	90	60	90	mA
Average Forward Current[1]	20	25	20	25	mA
DC Current[2]	30	30	20	30	mA
Power Dissipation	87	135	85	135	mW
Transient Forward Current[3] (10 µsec Pulse)	500				mA
Operating Temperature Range	-20 to +100	-55 to +100	-55 to +100	-20 to +100	°C
Storage Temperature Range	-55 to +100			-55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) below seating plane]	260°C for 5 seconds				

Notes:
1. See Figure 5 to establish pulsed operating conditions.
2. For AlGaAs Red, Red, Orange, and Green series derate linearly from 50°C at 0.5 mA/°C. For Yellow series derate linearly from 50°C at 0.34 mA/°C.
3. The transient peak current is the maximum non-recurring peak current that can be applied to the device without damaging the LED die and wire bond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

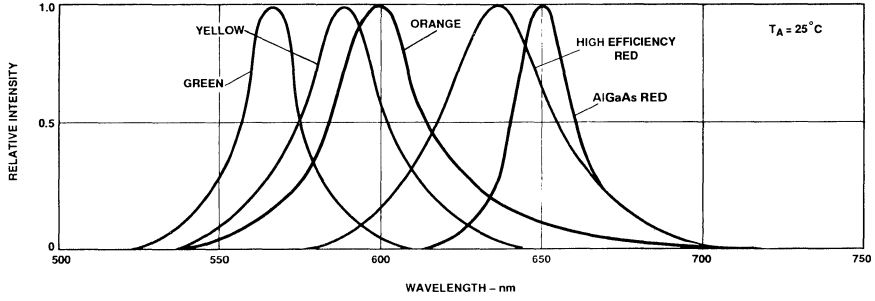


Figure 1. Relative Intensity vs. Wavelength

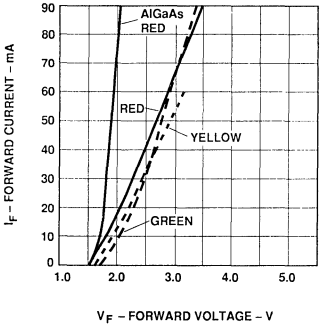


Figure 2. Forward Current vs. Forward Voltage Characteristics. V_F (300 mA) for AlGaAs Red = 2.6 Volts Typical

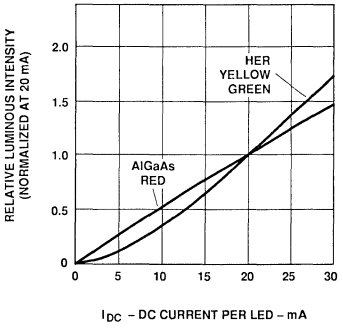


Figure 3. Relative Luminous Intensity vs. DC Forward Current

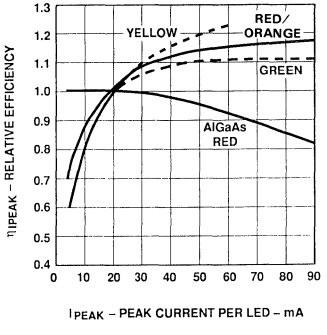


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. LED Peak Current. ηv (300 mA) for AlGaAs Red = 0.7

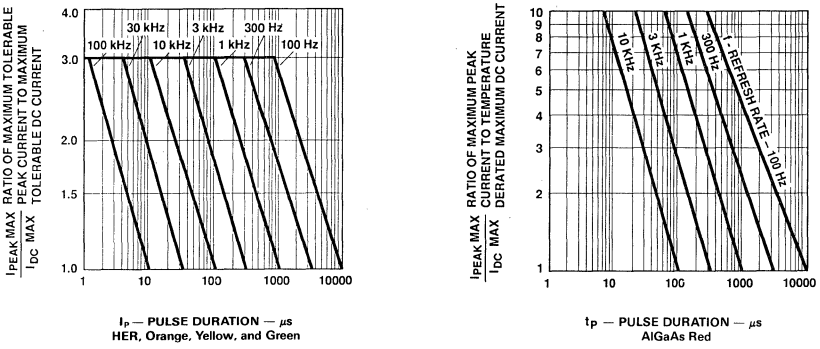


Figure 5. Maximum Tolerable Peak Current vs. Peak Duration (I_{PEAK} MAX Determined from Temperature Derated I_{DC} MAX)

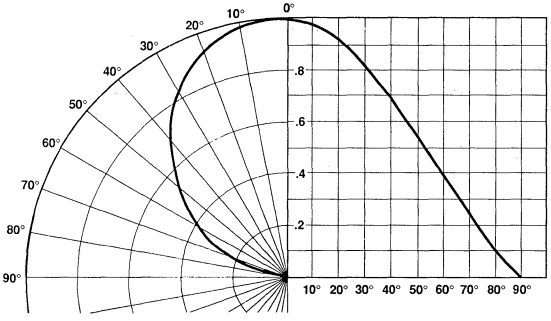


Figure 6. Relative Luminous Intensity vs. Angular Displacement

HEWLETT PACKARD

Subminiature Solid State Lamps

Technical Data

HLMP-PXXX Series
HLMP-Q1XX Series
HLMP-6XXX Series
HLMP-70XX Series

Features

- **Subminiature Flat Top Package**
  Ideal for Backlighting and Light Piping Applications
- **Subminiature Dome Package**
  Diffused Dome for Wide Viewing Angle
  Nondiffused Dome for High Brightness
- **Arrays**
- **TTL and LSTTL Compatible 5 Volt Resistor Lamps**
- **Available in Six Colors**
- **Ideal for Space Limited Applications**
- **Axial Leads**
- **Available with Lead Configurations for Surface Mount and Through Hole PC Board Mounting**

Description

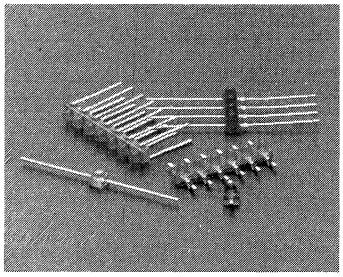
Flat Top Package
The HLMP-PXXX Series flat top lamps use an untinted, non-diffused, truncated lens to provide a wide radiation pattern that is necessary for use in backlighting applications. The flat top lamps are also ideal for use as emitters in light pipe applications.

Dome Packages
The HLMP-6XXX Series dome lamps for use as indicators use a tinted, diffused lens to provide a wide viewing angle with a high on-off contrast ratio. High brightness lamps use an untinted, nondiffused lens to provide a high luminous intensity within a narrow radiation pattern.

Arrays
The HLMP-66XX Series subminiature lamp arrays are available in lengths of 3 to 8 elements per array. The luminous intensity is matched within an array to assure a 2.1 to 1.0 ratio.

Resistor Lamps
The HLMP-6XXX Series 5 volt subminiature lamps with built in current limiting resistors are for use in applications where space is at a premium.

Lead Configurations
All of these devices are made by encapsulating LED chips on axial lead frames to form molded epoxy subminiature lamp packages. A variety of package configuration options is available. These include special surface mount lead configurations, gull wing, yoke lead or Z-bend. Right angle lead bends at 2.54 mm (0.100 inch) and 5.08 mm (0.200 inch) center spacing are available for through hole mounting.



Device Selection Guide
Part Number: HLMP-XXXX

Standard Red	DH AS AlGaAs Red	High Efficiency Red	Orange	Yellow	High Performance Green	Device Description[1]		Device Outline Drawing
P005	P105	P205	P405	P305	P505	Nondiffused, Flat Top		A
6000/6001	Q101	6300	Q400	6400	6500	Diffused		B
	Q105	6305		6405	6505	Nondiffused, High Brightness		
	Q150	7000		7019	7040	Diffused, Low Current		
	Q155					Nondiffused, Low Current		
		6600		6700	6800	Diffused, Resistor, 5 V, 10 mA		
		6620		6720	6820	Diffused, Resistor, 5 V, 4 mA		
6203		6653		6753	6853	3 Element	Matched Array, Diffused	C
6204		6654		6754	6854	4 Element		
6205		6655		6755	6855	5 Element		
6206		6656		6766	6856	6 Element		
6208		6658		6768	6858	8 Element		

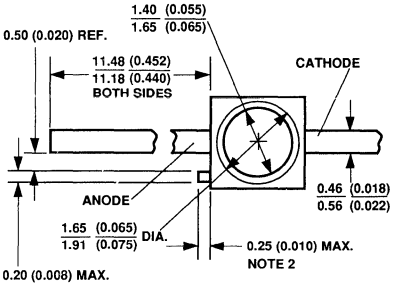
Package Configuration Options

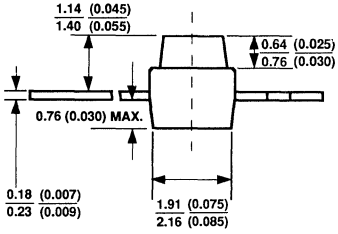
Option Code	Package Configuration Description			Package Outline Drawing
011	Gull Wing Lead, Tape and Reel[2]		Surface Mount Lead Configurations	D, L, P
012	Gull Wing Lead, Bulk Packaging[3]			
013	Gull Wing Lead, Arrays, Shipping Tube			E, M
021	Yoke Lead, Tape and Reel[2]			F, N, P
022	Yoke Lead, Bulk Packaging[3]			
031	Z-Bend, Tape and Reel[2]			G, O, P
032	Z-Bend, Bulk Packaging[3]			
1L1	2.54 mm (0.100 inch) Center Lead Spacing	Long Leads; 10.4 mm (0.410 in.)	Right Angle Lead Bends for Through Hole Mounting	H
1S1		Short Leads; 3.7 mm (0.145 in.)		I
2L1	5.08 mm (0.200 inch) Center Lead Spacing	Long Leads; 9.2 mm (0.364 in.)		J
2S1		Short Leads; 3.7 mm (0.145 in.)		K

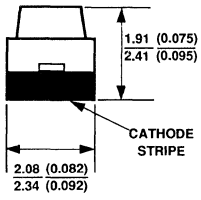
Notes:
1. Diffused lamps have tinted lenses. Nondiffused lamps have untinted lenses.
2. Lamps are supplied in 12 mm embossed tape on 178 mm (7 inch) diameter reels, with 1500 lamps per reel. Minimum order quantity and order increment are in quantity of reels only.
3. Vapor barrier bags are used for bulk packaging.

Package Dimensions

(A) Flat Top Lamps

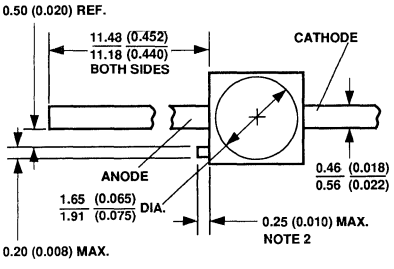


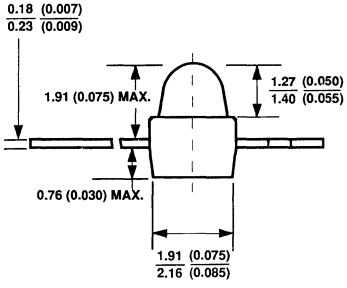


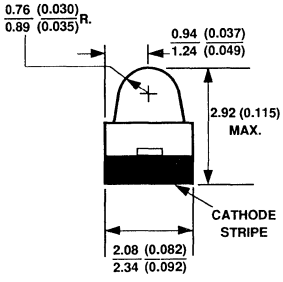


NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. PROTRUDING SUPPORT TAB IS CONNECTED TO CATHODE LEAD.

(B) Diffused and Nondiffused

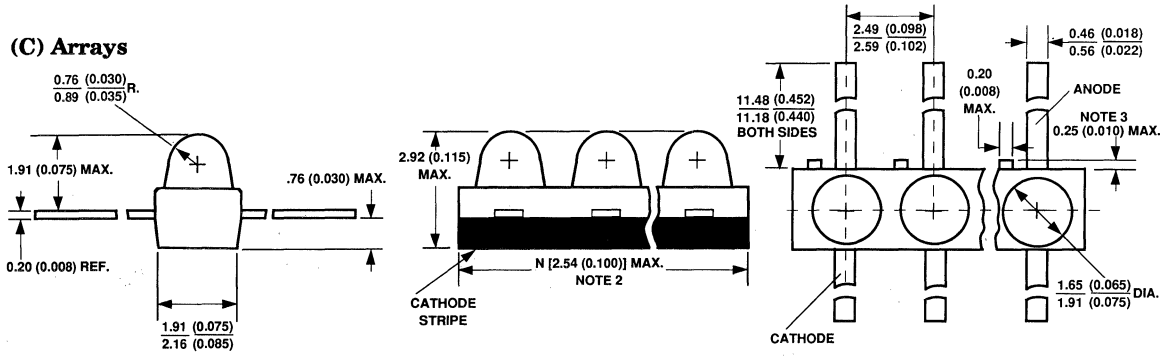






NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. PROTRUDING SUPPORT TAB IS CONNECTED TO CATHODE LEAD.

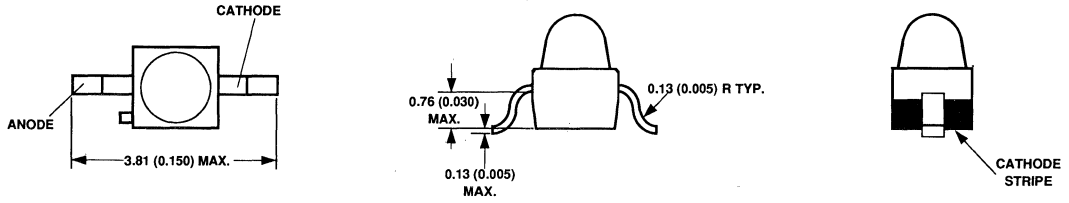
(C) Arrays



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. OVERALL LENGTH IS THE NUMBER OF ELEMENTS TIMES 2.54 mm (0.100 IN.).
3. PROTRUDING SUPPORT TAB IS CONNECTED TO CATHODE LEAD.

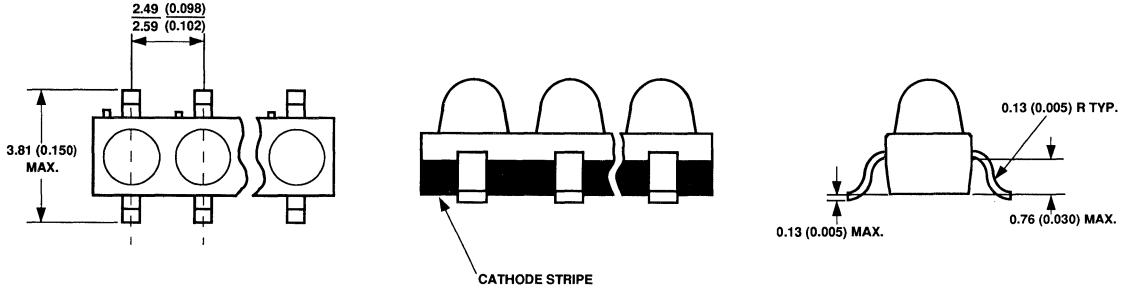
Package Dimensions, Lead Bend Options

(D) Individual Lamp, Gull Wing Lead, Option 011 and 012



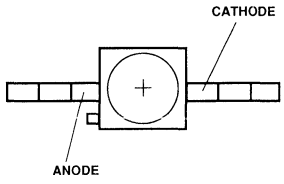
ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)

(E) Subminiature Array, Gull Wing Lead, Option 013

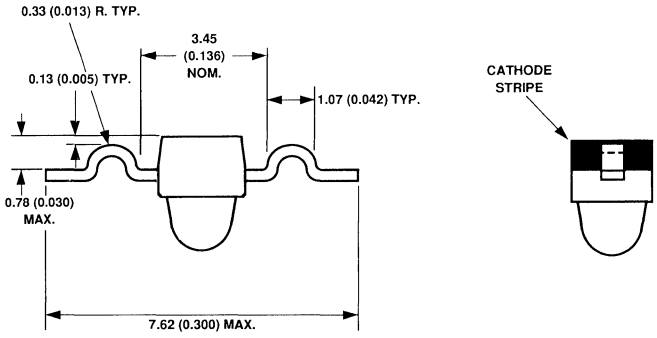


ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)

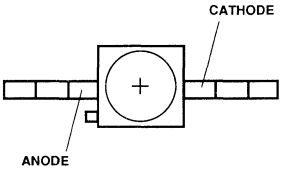
(F) Individual Lamp, "Yoke" Lead, Options 021 and 022



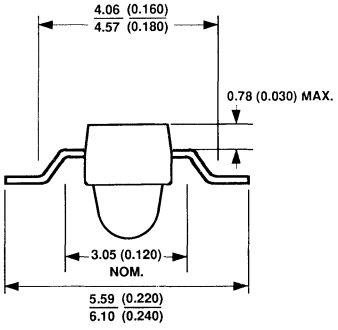
ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)

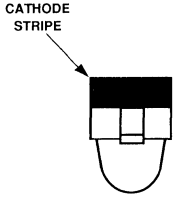


(G) Individual Lamp, Z-Bend Lead, Options 031 and 032

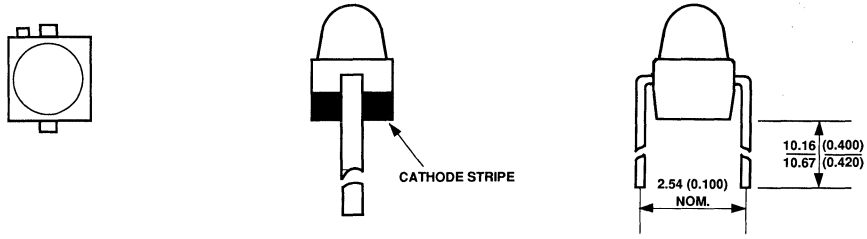


ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)



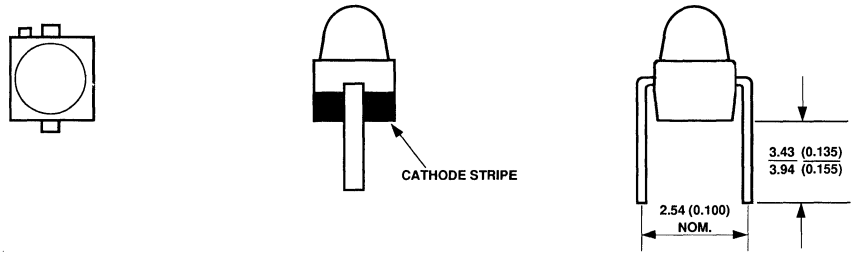


(H) Individual Lamp or Array, Rt. Angle Bend Option 1L1



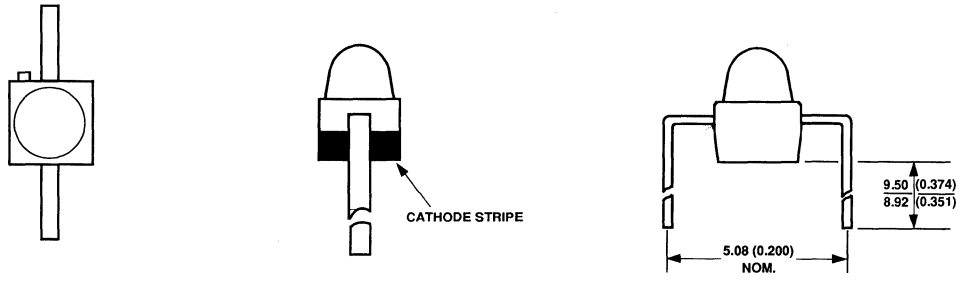
ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)

(I) Individual Lamp or Array, Rt. Angle Bend Option 1S1



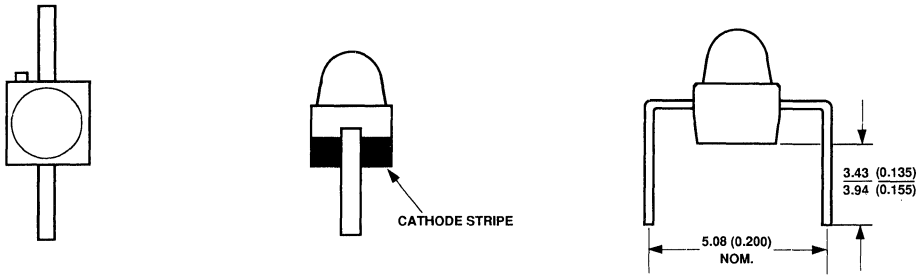
ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)

(J) Individual Lamp or Array, Rt. Angle Bend Option 2L1



ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)

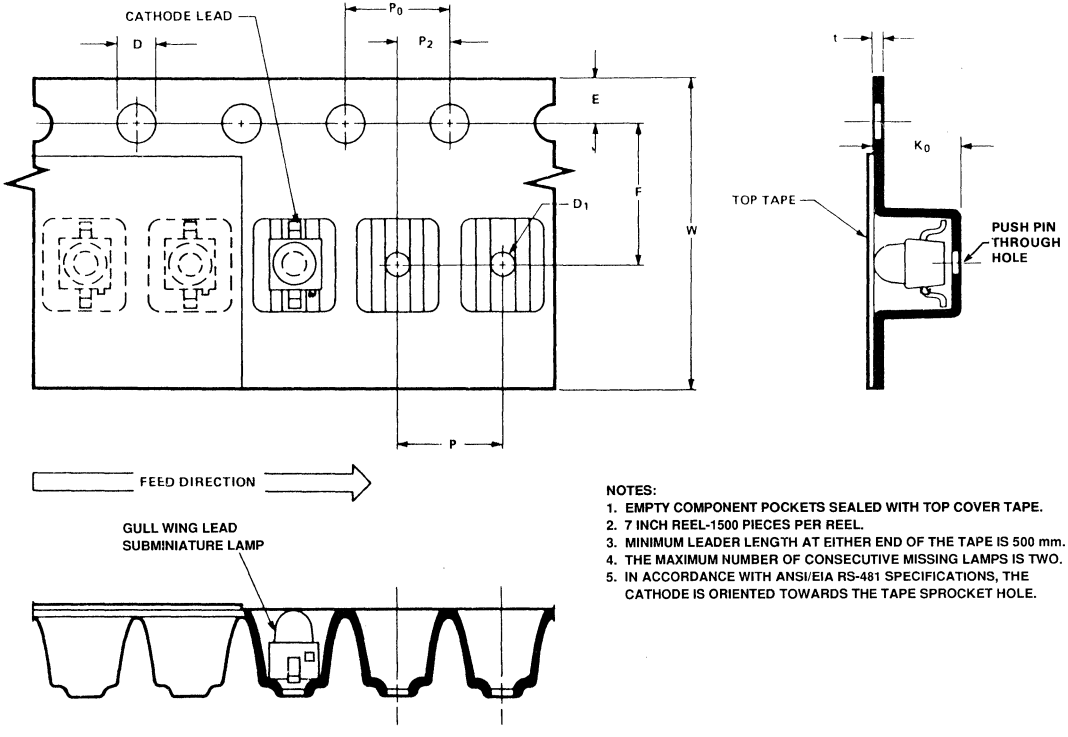
(K) Individual Lamp or Array, Rt. Angle Bend Option 2S1



ALL DIMENSIONS ARE IN MILLIMETRES (INCHES)

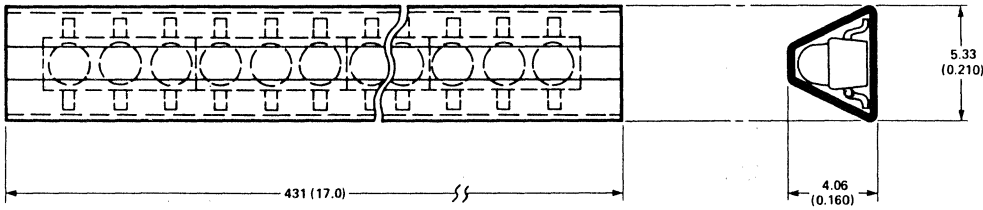
Package Dimensions: Surface Mount Tape and Reel Options

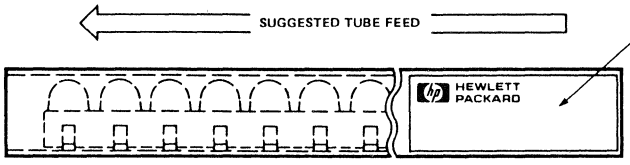
(L) 12 mm Tape and Reel, Gull Wing Lead, Option 011



NOTES:
1. EMPTY COMPONENT POCKETS SEALED WITH TOP COVER TAPE.
2. 7 INCH REEL-1500 PIECES PER REEL.
3. MINIMUM LEADER LENGTH AT EITHER END OF THE TAPE IS 500 mm.
4. THE MAXIMUM NUMBER OF CONSECUTIVE MISSING LAMPS IS TWO.
5. IN ACCORDANCE WITH ANSI/EIA RS-481 SPECIFICATIONS, THE CATHODE IS ORIENTED TOWARDS THE TAPE SPROCKET HOLE.

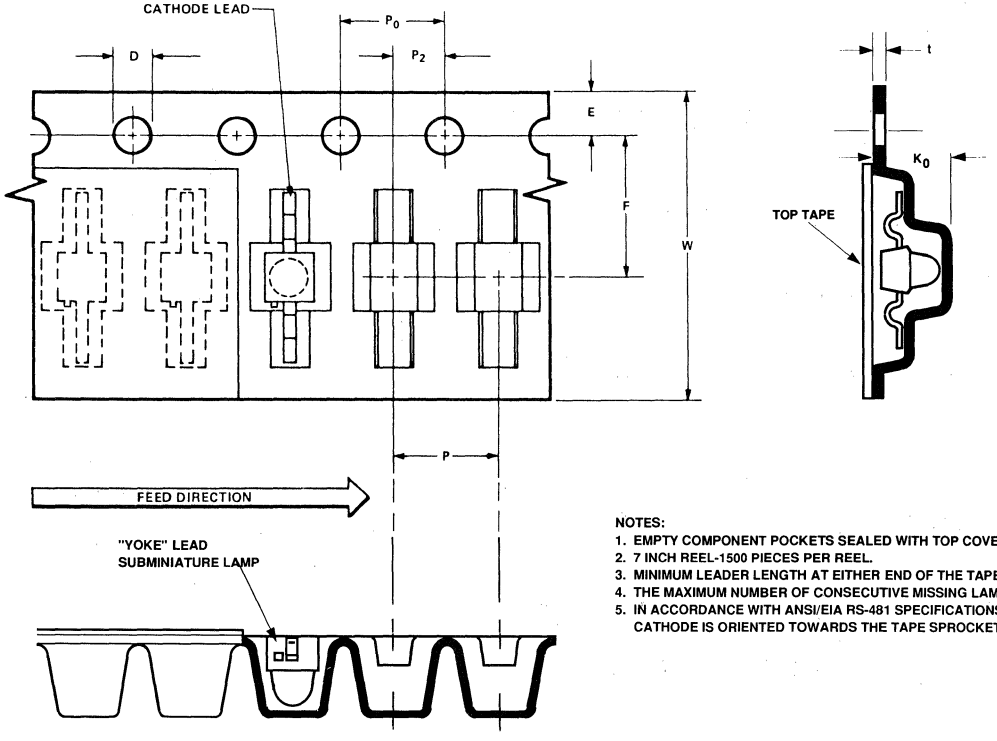
(M) Array Shipping Tube, Gull Wing Lead, Option 013





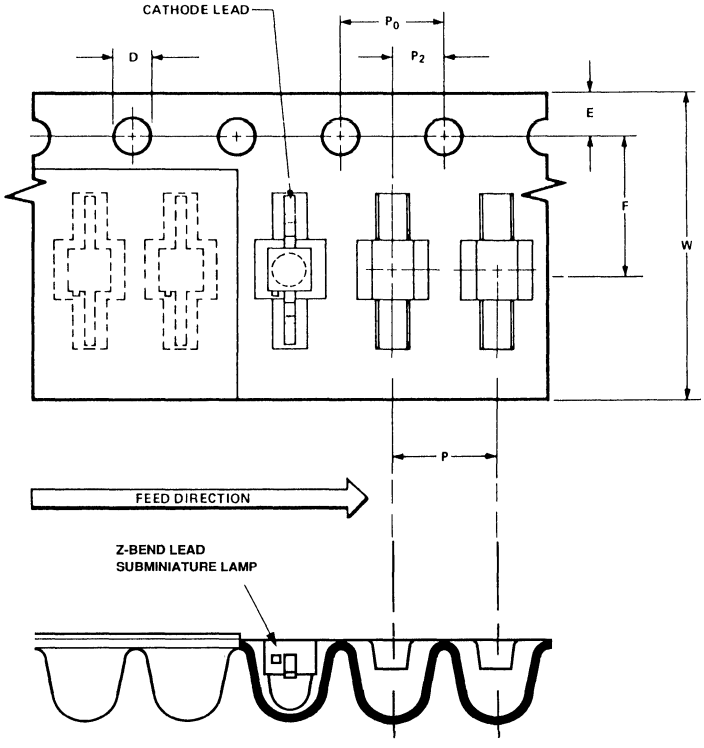
HLMP-	NO. OF LAMP ELEMENTS PER ARRAY	QUANTITY OF ARRAYS PER TUBE
6XX3	3	53
6XX4	4	40
6XX5	5	32
6XX6	6	26
6XX8	8	20

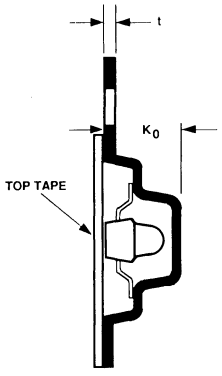
(N) 12 mm Tape and Reel, "Yoke" Lead, Option 021



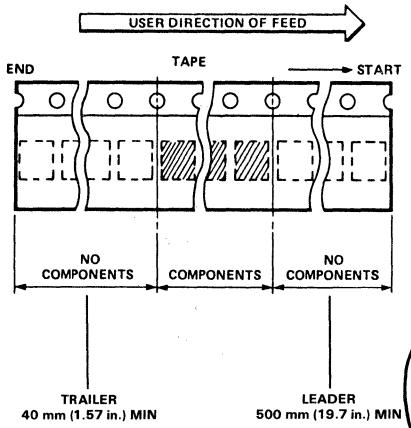
NOTES:
1. EMPTY COMPONENT POCKETS SEALED WITH TOP COVER TAPE.
2. 7 INCH REEL-1500 PIECES PER REEL.
3. MINIMUM LEADER LENGTH AT EITHER END OF THE TAPE IS 500 mm.
4. THE MAXIMUM NUMBER OF CONSECUTIVE MISSING LAMPS IS TWO.
5. IN ACCORDANCE WITH ANSI/EIA RS-481 SPECIFICATIONS, THE CATHODE IS ORIENTED TOWARDS THE TAPE SPROCKET HOLE.

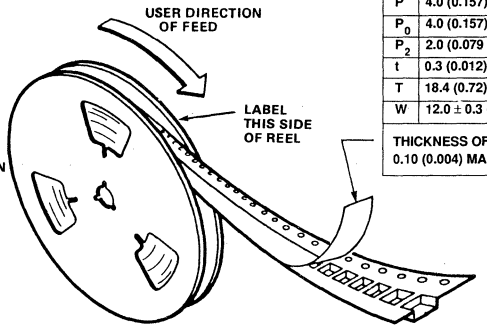
(O) 12 mm Tape and Reel, Z-Bend Lead, Option





(P) 12 mm Tape and Reel



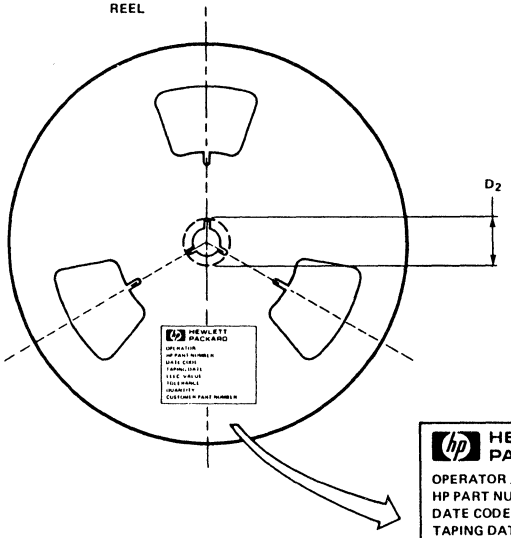


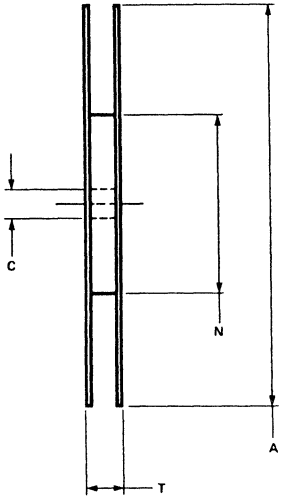
DIMENSIONS PER ANSI/EIA STANDARD RS-481.
ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).

A	178.0 ± 2.0 (7.0 ±0.08) DIA.
C	13.0 (0.512) DIA. TYP.
D	1.55 (0.061 ± 0.002) DIA.
D_1	1.0 (0.039) DIA. MIN.
D_2	20.2 (0.795) DIA. MIN.
E	1.75 ± 0.1 (0.069)
F	5.50 (0.127 ± 0.002)
K_0	3.05 ± 0.1 (0.120) TYP.
N	50.0 (1.970) MIN.
P	4.0 (0.157) TYP.
P_0	4.0 (0.157) TYP.
P_2	2.0 (0.079 ± 0.002) TYP.
t	0.3 (0.012) TYP.
T	18.4 (0.72) MAX.
W	12.0 ± 0.3 (0.472 ± 0.012)

THICKNESS OF TOP COVER TAPE
0.10 (0.004) MAX.

TOLERANCES (UNLESS OTHERWISE SPECIFIED):
.X ± .1; .XX ± .05 (.XXX ± .004)





HEWLETT PACKARD
OPERATOR _____
HP PART NUMBER _____
DATE CODE _____
TAPING DATE _____
ELEC. VALUE _____
TOLERANCE _____
QUANTITY _____
CUSTOMER PART NUMBER _____

Absolute Maximum Ratings at T_A = 25°C

Parameter	Standard Red	DH AS AlGaAs Red	High Eff. Red	Orange	Yellow	High Perf. Green	Units
Power Dissipation	100	87	135	135	85	135	mW
DC Forward Current[1]	50	30	30	30	20	30	mA
Peak Forward Current[2]	1000	300	90	90	60	90	mA
DC Forward Voltage (Resistor Lamps Only)			6		6	6	V
Reverse Voltage (I_R = 100 µA)	5	5	5	5	5	5	V
Transient Forward Current[3] (10 µs Pulse)	2000	500	500	500	500	500	mA
Operating Temperature Range: Non-Resistor Lamps	-55 to +100	-20 to +100	-55 to +100			-20 to +100	°C
Resistor Lamps			-40 to +85			-20 to +85	°C
Storage Temperature Range	-55 to +100						°C
Wave Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 3 Seconds						
Surface Mount Reflow Soldering: Convective IR	235°C for 90 Seconds						
Vapor Phase	215°C for 3 Minutes						

Notes:
1. See Figure 5 for current derating vs. ambient temperature. Derating is not applicable to resistor lamps.
2. Refer to Figure 6 showing Max. Tolerable Peak Current vs. Pulse Duration to establish pulsed operating conditions.
3. The transient peak current is the maximum non-recurring peak current the device can withstand without failure. Do not operate these lamps at this high current.

Electrical/Optical Characteristics, T_A = 25°C

Standard Red

Device HLMP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
P005	Luminous Intensity[1]	I_v	1.0	2.5		mcd	I_F = 10 mA
6000			0.5	1.2			
6001			1.3	3.2			
6203 to 6208			0.5	1.2			
All	Forward Voltage	V_F	1.4	1.6	2.0	V	I_F = 10 mA
	Reverse Breakdown Voltage	V_R	5.0	12.0		V	I_R = 100 µA
P005	Included Angle Between Half Intensity Points[2]	$2\theta_{1/2}$		125		Deg.	
All Others				90			
All	Peak Wavelength	λ_{PEAK}		655		nm	
	Dominant Wavelength[3]	λ_d		640		nm	
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		24		nm	
	Speed of Response	τ_s		15		ns	
	Capacitance	C		100		pF	V_F = 0; f = 1 MHz
	Thermal Resistance	$R\theta_{J\text{-}PIN}$		120		°C/W	Junction-to-Cathode Lead
	Luminous Efficacy[4]	η_v		65		lm/W	

DH AS AlGaAs Red

Device HLMP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
P105	Luminous Intensity	I_v	22.0	45.0		mcd	I_F = 20 mA
Q101			22.0	45.0			
Q105			22.0	55.0			
Q150			1.0	1.8			I_F = 1 mA
Q155			2.0	4.0			
Q101	Forward Voltage	V_F		1.8	2.2	V	I_F = 20 mA
P105/Q105				1.8	2.2		
Q150/Q155				1.6	1.8		I_F = 1 mA
All	Reverse Breakdown Voltage	V_R	5.0	15.0		V	I_R = 100 μA
P105	Included Angle Between Half Intensity Points[2]	$2\theta_{1/2}$		125		Deg.	
Q101/Q150				90			
Q105/Q155				28			
All	Peak Wavelength	λ_{PEAK}		645		nm	Measured at Peak
	Dominant Wavelength[3]	λ_d		637		nm	
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		20		nm	
	Speed of Response	τ_s		30		ns	Exponential Time Constant; $e^{-t/\tau}$
	Capacitance	C		30		pF	V_F = 0; f = 1 MHz
	Thermal Resistance	$R\theta_{J\text{-}PIN}$		220		°C/W	Junction-to Cathode Lead
	Luminous Efficacy[4]	η_v		80		lm/W	

High Efficiency Red

Device HLMP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
P205	Luminous Intensity[1]	I_v	1.0	5.0		mcd	I_F = 10 mA
6300			1.0	3.0			
6305			3.4	12.0			
7000			0.4	0.8			I_F = 2 mA
6600			1.3	5.0			V_F = 5.0 Volts
6620			0.8	2.0			
6653 to 6658			1.0	3.0			I_F = 10 mA
All	Forward Voltage (Nonresistor Lamps)	V_F	1.5	1.8	3.0	V	I_F = 10 mA
6600	Forward Current (Resistor Lamps)	I_F		9.6	13.0	mA	V_F = 5.0 V
6620				3.5	5.0		
All	Reverse Breakdown Voltage	V_R	5.0	30.0		V	I_R = 100 μA
P205	Included Angle Between Half Intensity Points[2]	$2\theta_{1/2}$		125		Deg.	
6305				28			
All Diffused				90			
All	Peak Wavelength	λ_{PEAK}		635		nm	Measured at Peak
	Dominant Wavelength[3]	λ_d		626		nm	
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		40		nm	
	Speed of Response	τ_s		90		ns	
	Capacitance	C		11		pF	V_F = 0; f = 1 MHz
	Thermal Resistance	$R\theta_{J\text{-}PIN}$		120		°C/W	Junction-to-Cathode Lead
	Luminous Efficacy[4]	η_v		145		lm/W	

Orange

Device HLMP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
P405	Luminous Intensity	I_v	1.0	4.0		mcd	I_F = 10 mA
Q400			1.0	3.0			
P405	Forward Voltage	V_F	1.5	1.9	3.0	V	I_F = 10 mA
	Reverse Breakdown Voltage	V_R	5.0	30.0		V	I_R = 100 µA
P405	Included Angle Between Half Intensity Points[2]	$2\theta_{1/2}$		125		Deg.	
Q400				90			
P405/ Q400	Peak Wavelength	λ_{PEAK}		600		nm	
	Dominant Wavelength[3]	λ_d		602		nm	Measured at Peak
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		40		nm	
	Speed of Response	τ_s		260		ns	
	Capacitance	C		4		pF	V_F = 0; f = 1 MHz
	Thermal Resistance	$R\theta_{J\text{-}PIN}$		120		°C/W	Junction-to-Cathode Lead
	Luminous Efficacy[4]	η_v		380		lm/W	

Yellow

Device HLMP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
P305	Luminous Intensity[1]	I_v	1.0	4.0		mcd	I_F = 10 mA
6400			1.0	3.0			
6405			3.6	12			
7019			0.4	0.6			I_F = 2 mA
6700			1.4	5.0			V_F = 5.0 Volts
6720			0.9	2.0			
6753 to 6758			1.0	3.0			I_F = 10 mA
All	Forward Voltage (Nonresistor Lamps)	V_F	1.5	2.0	3.0	V	I_F = 10 mA
6700	Forward Current (Resistor Lamps)	I_F		9.6	13.0	mA	V_F = 5.0 V
6720				3.5	5.0		
All	Reverse Breakdown Voltage	V_R	5.0	50.0		V	
P305	Included Angle Between Half Intensity Points[2]	$2\theta_{1/2}$		125		Deg.	
6405				28			
All Diffused				90			
All	Peak Wavelength	λ_{PEAK}		583		nm	Measured at Peak
	Dominant Wavelength[3]	λ_d		585		nm	
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		36		nm	
	Speed of Response	τ_s		90		ns	
	Capacitance	C		15		pF	V_F = 0; f = 1 MHz
	Thermal Resistance	$R\theta_{J\text{-}PIN}$		120		°C/W	Junction-to-Cathode Lead
	Luminous Efficacy[4]	η_v		500		lm/W	

High Performance Green

Device HLMP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
P505	Luminous Intensity[1]	I_v	1.0	5.0		mcd	I_F = 10 mA
6500			1.0	3.0			
6505			4.2	12.0			
7040			0.4	0.6			I_F = 2 mA
6800			1.6	5.0			V_F = 5.0 Volts
6820			0.8	2.0			
6853 to 6858			1.0	3.0			I_F = 10 mA
All	Forward Voltage (Nonresistor Lamps)	V_F	1.5	2.0	3.0	V	I_F = 10 mA
6800	Forward Current (Resistor Lamps)	I_F		9.6	13.0	mA	V_F = 5.0 V
6820				3.5	5.0		
All	Reverse Breakdown Voltage	V_R	5.0	50.0		V	I_R = 100 μA
P505	Included Angle Between Half Intensity Points[2]	$2\theta_{1/2}$		125		Deg.	
6505				28			
All Diffused				90			
All	Peak Wavelength	λ_{PEAK}		565		nm	
	Dominant Wavelength[3]	λ_d		569		nm	
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		28		nm	
	Speed of Response	τ_s		500		ns	
	Capacitance	C		18		pF	V_F = 0; f = 1 MHz
	Thermal Resistance	$R\theta_{J\text{-}PIN}$		120		°C/W	Junction-to-Cathode Lead
	Luminous Efficacy[4]	η_v		595		lm/W	

Notes:
1. The luminous intensity for arrays is tested to assure a 2.1 to 1.0 matching between elements. The average luminous intensity for an array determines its light output category bin. Arrays are binned for luminous intensity to allow I_v matching between arrays.
2. $\theta_{1/2}$ is the off-axis angle where the luminous intensity is half the on-axis value.
3. Dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and represents the single wavelength that defines the color of the device.
4. Radiant intensity, I_e, in watts/steradian, may be calculated from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

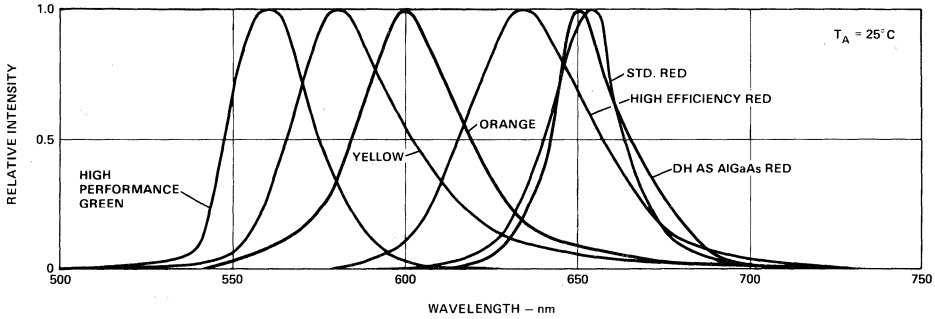


Figure 1. Relative Intensity vs. Wavelength.

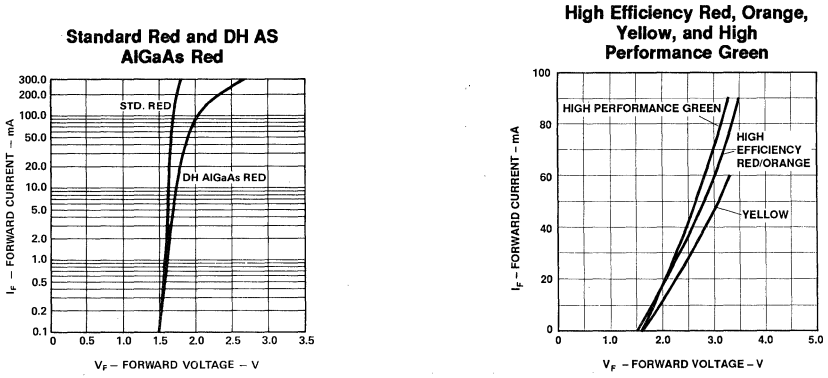


Figure 2. Forward Current vs. Forward Voltage (Non-Resistor Lamp).

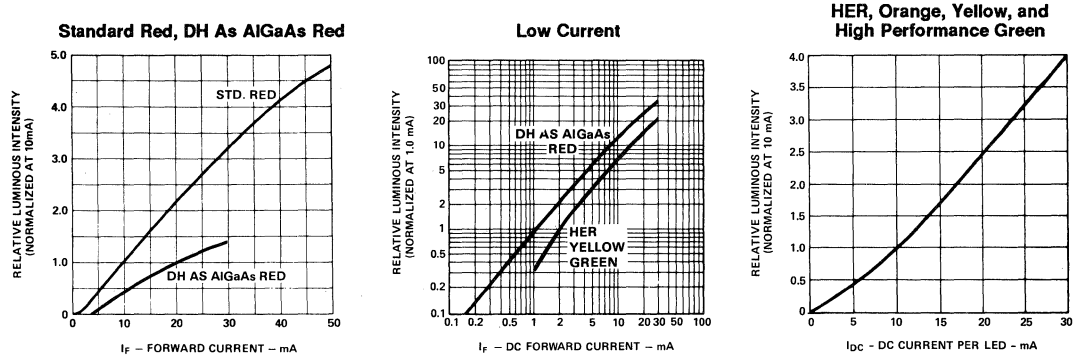


Figure 3. Relative Luminous Intensity vs. Forward Current (Non-Resistor Lamp).

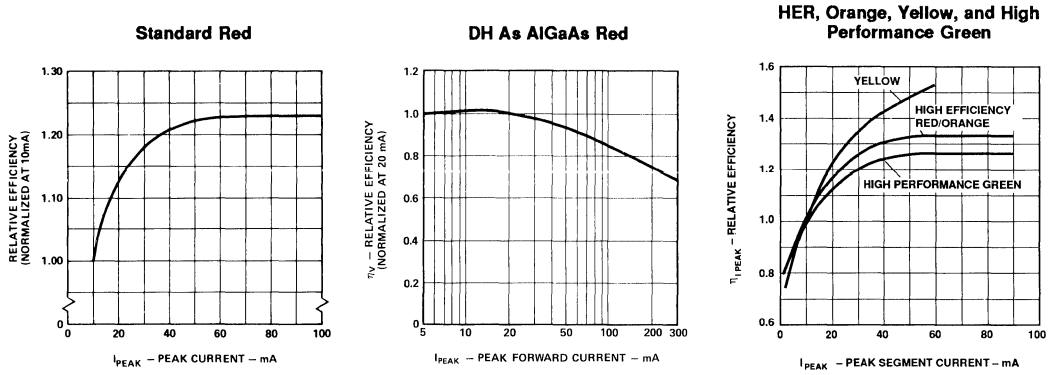
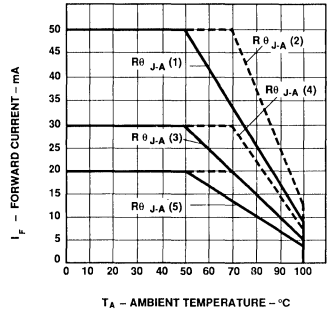


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current (Non-Resistor Lamps).



$R\theta_{J-A}$ (X)	STD RED	AlGaAs RED	HI-EFF RED	ORANGE	YELLOW	GREEN	UNITS
1	600						°C/W LED JUNCTION TO AMBIENT
2	400						
3		689	444	444	470	444	
4		559	296	296		296	
5					705		

Figure 5. Maximum Forward dc Current vs. Ambient Temperature. Derating Based on T_J MAX = 110°C (Non-Resistor Lamps).

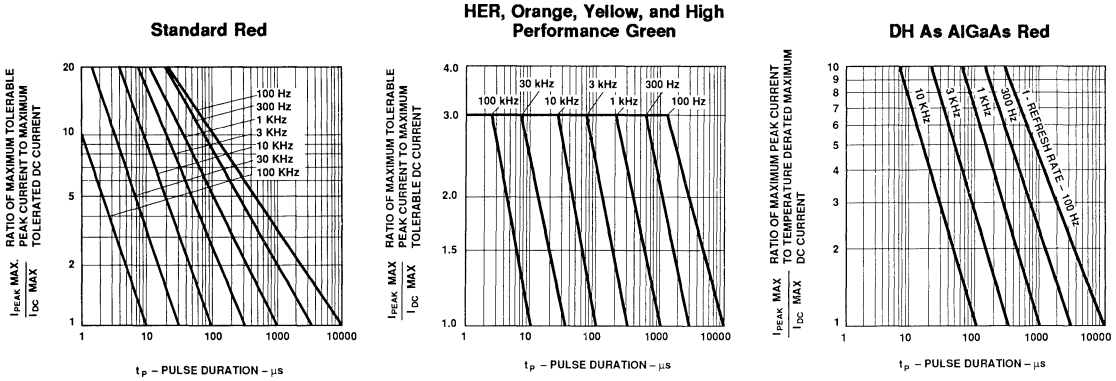


Figure 6. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings) (Non-Resistor Lamps).

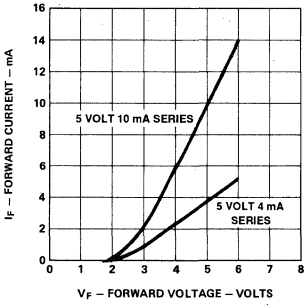


Figure 7. Resistor Lamp Forward Current vs. Forward Voltage.

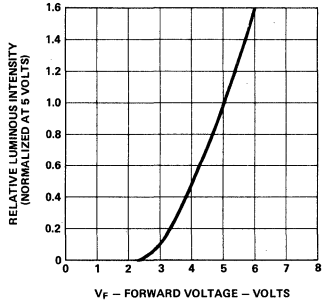


Figure 8. Resistor Lamp Luminous Intensity vs. Forward Voltage.

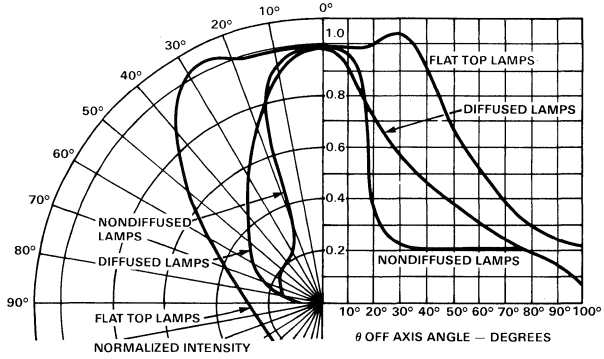


Figure 9. Relative Intensity vs. Angular Displacement.

HEWLETT PACKARD

High Efficiency Red/ High Performance Green Bicolor Solid State Lamps

Technical Data

HLMP-4000 T-1 3/4 (5 mm)
HLMP-0800 2 mm x 5 mm Rectangular

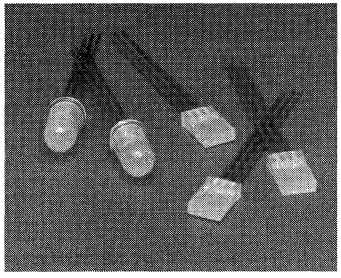
Features:

- **Two Color (Red, Green) Operation**
- **(Other Two LED Color Combinations Available)**
- **Three Leads with One Common Cathode**
- **Diffused, Wide Visibility Lens**

Description

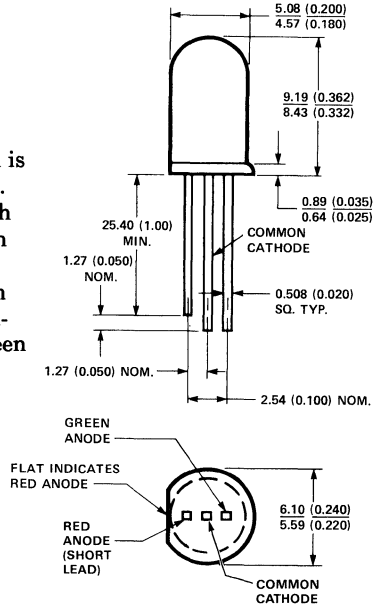
The T-1 3/4 HLMP-4000 and 2 mm by 5 mm rectangular HLMP-0800 are three leaded bicolor light sources designed for a variety of applications where dual state illumination is required in the same package. There are two LED chips, high efficiency red (HER), and high performance green (Green), mounted on a central common cathode lead for maximum on-axis viewability. Colors between HER and Green can be generated by independently pulse width modulating the LED chips.

Note: Other possible LED combinations available are AlGaAs, orange, yellow.

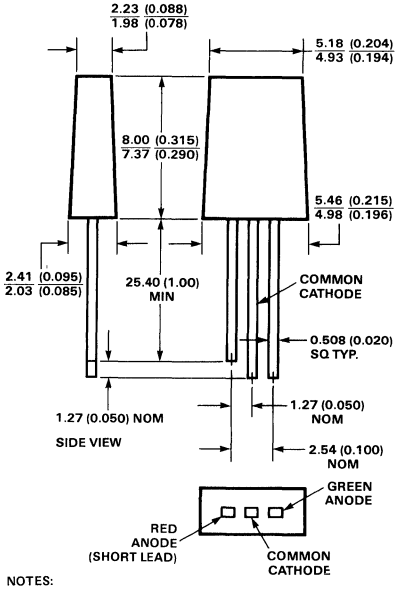


Package Dimensions

HLMP-4000



HLMP-0800



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.

Absolute Maximum Ratings at T_A = 25°C

Parameter	High Efficiency Red/Green	Units
Peak Forward Current	90	mA
Average Forward Current[1,2] (Total)	25	mA
DC Current[2,4] (Total)	30	mA
Power Dissipation[3,5] (Total)	135	mW
Operating Temperature Range	-20 to +85	°C
Storage Temperature Range	-55 to +100	
Reverse Voltage (I_R = 100 μA)	5	V
Transient Forward Current[6] (10 μsec Pulse)	500	mA
Lead Soldering Temperature [1.6 mm (0.063 in.) below seating plane]	260°C for 5 seconds	

Notes:
1. See Figure 5 to establish pulsed operating conditions.
2. The combined simultaneous current must not exceed the maximum.
3. The combined simultaneous power must not exceed the maximum.
4. For HER and Green derate linearly from 50°C at 0.5 mA/°C.
5. For HER and Green derate linearly from 25°C at 1.8 mW/°C.
6. The transient peak current is the maximum non-recurring current that can be applied to the device without damaging the LED die and wirebond. It is not recommended that the device be operated at peak currents beyond the peak forward current listed in the Absolute Maximum Ratings.

Electrical/Optical Characteristics at $T_A = 25°C$

Sym.	Parameter	Red			Green			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Luminous Intensity								
	HLMP-4000	2.1	5		4.2	8		mcd	$I_F = 10$ mA
	HLMP-0800	2.1	3.5		2.6	4.0			$I_F = 20$ mA
λ_{PEAK}	Peak Wavelength		635			565		nm	
λ_d	Dominant Wavelength[1]		626			569			
τ_s	Speed of Response		90			500		ns	
C	Capacitance		11			18		pF	$V_F = 0$, f = 1 MHz
V_F	Forward Voltage		2.1	2.5		2.3	2.7	V	$I_F = 10$ mA
V_R	Reverse Breakdown Voltage	5			5			V	$I_R = 100\ \mu A$
θ_{JC}	Thermal Resistance		120		120			°C/W	Junction to Cathode Lead
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points[2]								
	HLMP-4000		65			65		Deg.	$I_F = 10$ mA
	HLMP-0800		100			100			$I_F = 20$ mA
η_V	Luminous Efficacy[3]		145			595		Lumen/ Watt	

Notes:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
3. Radiant intensity, I_e, in watts steradian, may be found from the equation $I_e = I_v/\eta_v$ where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

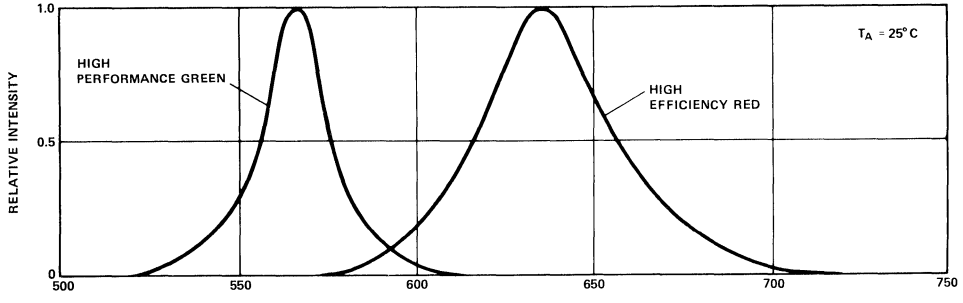


Figure 1. Relative Intensity vs. Wavelength.

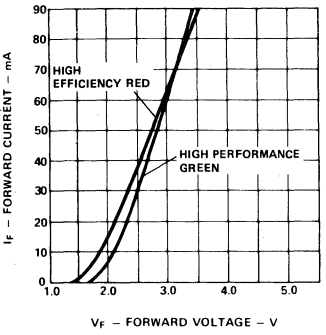


Figure 2. Forward Current vs. Forward Voltage Characteristics.

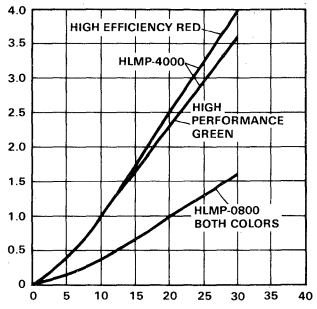


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

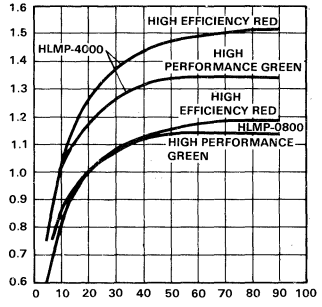


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. LED Peak Current.

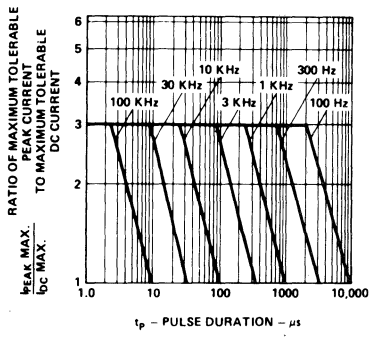


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration (I_{DC} MAX as per MAX Ratings.

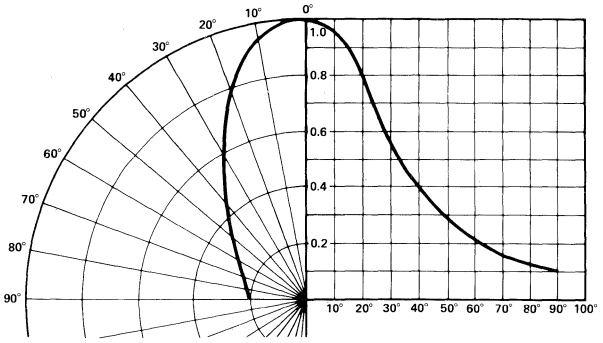


Figure 6. Relative Luminous Intensity vs. Angular Displacement for the HLMP-4000.

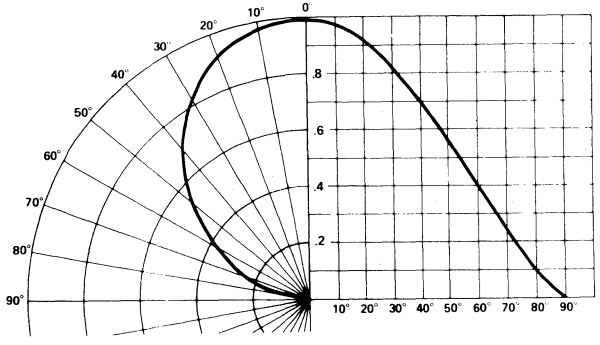


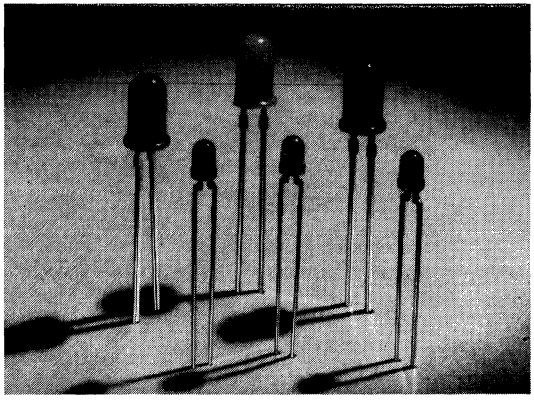
Figure 7. Relative Luminous Intensity vs. Angular Displacement for the HLMP-0800.

HEWLETT PACKARD

INTEGRATED RESISTOR LAMPS
5 Volt and 12 Volt in T-1 and T-1 3/4 Packages

Features

- **INTEGRAL CURRENT LIMITING RESISTOR**
- **TTL COMPATIBLE**
  Requires no External Current Limiter with 5 Volt/12 Volt Supply
- **COST EFFECTIVE**
  Saves Space and Resistor Cost
- **WIDE VIEWING ANGLE**
- **AVAILABLE IN ALL COLORS**
  Red, High Efficiency Red, Yellow and High Performance Green in T-1 and T-1 3/4 Packages



Description

The 5 volt and 12 volt series lamps contain an integral current limiting resistor in series with the LED. This allows the lamp to be driven from a 5 volt/12 volt source without an external current limiter. The red LEDs are made from GaAsP on a GaAs substrate. The High Efficiency Red and Yellow devices use GaAsP on a GaP substrate.

The green devices use GaP on a GaP substrate. The diffused lamps provide a wide off-axis viewing angle.

The T-1 3/4 lamps are provided with sturdy leads suitable for wire wrap applications. The T-1 3/4 lamps may be front panel mounted by using the HLMP-0103 clip and ring.

Color	P/N HLMP-	Package	Operating Voltage	I_V mcd Min.	I_V mcd Typ.	2Θ 1/2[1]	Package Outline
Red	1100	T-1 Tinted Diffused	5	0.8	2.5	60°	A
	1120	T-1 Untinted Diffused	5	0.8	2.5	60°	A
	3105	T-1 3/4 Tinted Diffused	5	1.0	3.0	60°	B
	3112		12	1.0	3.0	60°	B
High Efficiency Red	1600	T-1 Tinted Diffused	5	2.0	8.0	60°	A
	1601		12				
	3600	T-1 3/4 Tinted Diffused	5			60°	B
	3601		12				
Yellow	1620	T-1 Tinted Diffused	5	2.0	8.0	60°	A
	1621		12				
	3650	T-1 3/4 Tinted Diffused	5			60°	B
	3651		12				
High Performance Green	1640	T-1 Tinted Diffused	5	2.0	8.0	60°	A
	1641		12				
	3680	T-1 3/4 Tinted Diffused	5			60°	B
	3681		12				

Notes:
1. Θ1/2 is the off-axis angle at which the luminous intensity is half the axial luminous intensity.

Absolute Maximum Ratings at $T_A = 25°C$

	Red/HER/Yellow 5 Volt Lamps	Red/HER/Yellow 12 Volt Lamps	Green 5 Volt Lamps	Green 12 Volt Lamps
DC Forward Voltage ($T_A = 25°C$)	7.5 Volts[2]	15 Volts[3]	7.5 Volts[2]	15 Volts[3]
Reverse Voltage ($I_R = 100\ \mu A$)	5 Volts	5 Volts	5 Volts	5 Volts
Operating Temperature Range	–40° C to 85° C	–40° C to 85° C	–20° C to 85° C	–20° C to 85° C
Storage Temperature Range	–55° C to 100° C	–55° C to 100° C	–55° C to 100° C	–55° C to 100° C
Lead Soldering Temperature	260° C for 5 seconds			

Notes:
2. Derate from $T_A = 50°C$ at 0.071V/° C, see Figure 3.
3. Derate from $T_A = 50°C$ at 0.086V/° C, see Figure 4.

Electrical/Optical Characteristics at $T_A = 25°C$

		Red			High Efficiency Red			Yellow			Green				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units	Test Conditions
λ_{PEAK}	Peak Wavelength		655			635			583			565		nm	
λ_d	Dominant Wavelength		648			626			585			569		nm	Note 4
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth		24			40			36			28		nm	
θ_{JC}	Thermal Resistance		120			120			120			120		°C/W	Junction to Cathode Lead (Note 6)
θ_{JC}	Thermal Resistance		95			95			95			95		°C/W	Junction to Cathode Lead (Note 7)
I_F	Forward Current 12 V Devices		13	20		13	20		13	20		13	20	mA	$V_F = 12$ V
I_F	Forward Current 5 V Devices		13	20		10	15		10	15		12	15	mA	$V_F = 5$ V
η_V	Luminous Efficacy		65			145			500			595		lumen /watt	Note 5
V_R	Reverse Breakdown Voltage	5.0			5.0			5.0			5.0			V	$I_R = 100\ \mu A$

Notes:
4. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
5. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$. Where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.
6. For Figure A package type.
7. For Figure B package type.

Package Dimensions

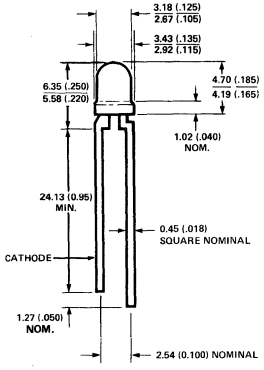


Figure A. T-1 Package

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

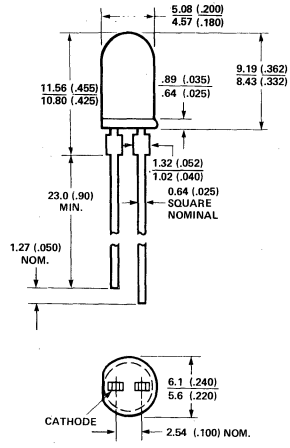


Figure B. T-1 3/4 Package

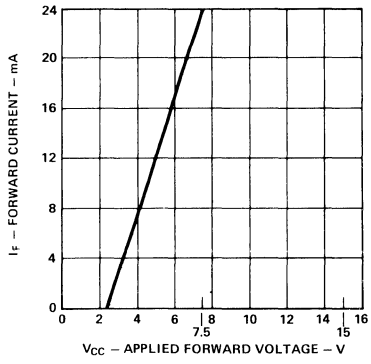


Figure 1. Forward Current vs. Applied Forward Voltage. 5 Volt Devices

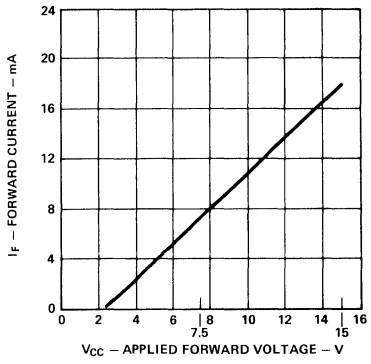


Figure 2. Forward Current vs. Applied Forward Voltage. 12 Volt Devices

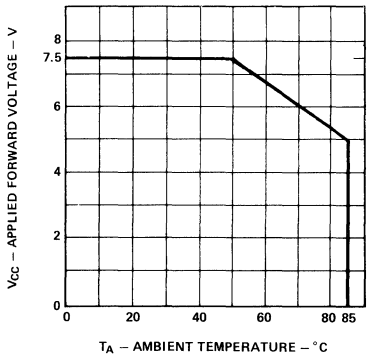


Figure 3. Maximum Allowed Applied Forward Voltage vs. Ambient Temperature $R\theta_{JA}$ = 175° C/W. 5 Volt Devices

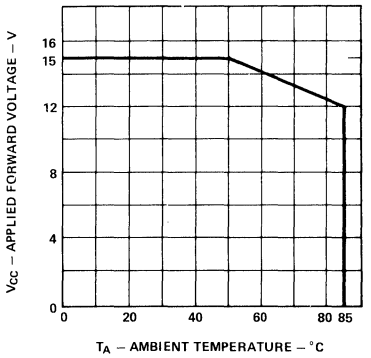


Figure 4. Maximum Allowed Applied Forward Voltage vs. Ambient Temperature $R\theta_{JA}$ = 175° C/W. 12 Volt Devices

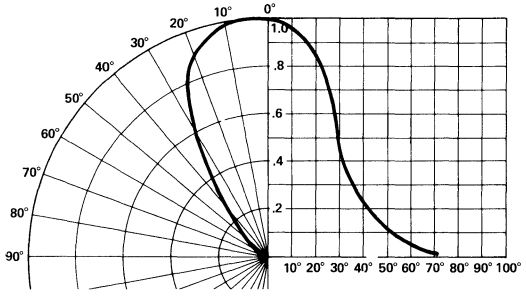


Figure 5. Relative Luminous Intensity vs. Angular Displacement for T-1 Package

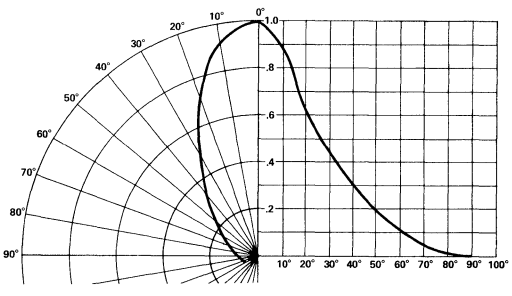


Figure 6. Relative Luminous Intensity vs. Angular Displacement for T-1 3/4 Package

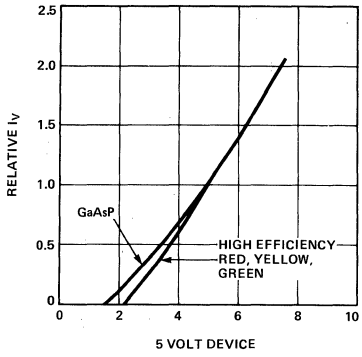


Figure 7. Relative Luminous Intensity vs. Applied Forward Voltage. 5 Volt Devices

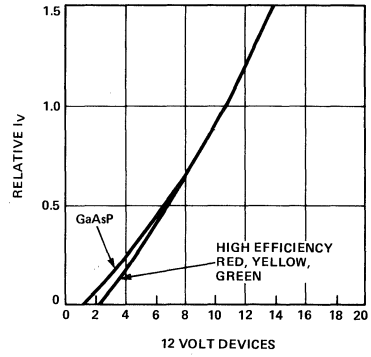


Figure 8. Relative Luminous Intensity vs. Applied Forward Voltage. 12 Volt Devices

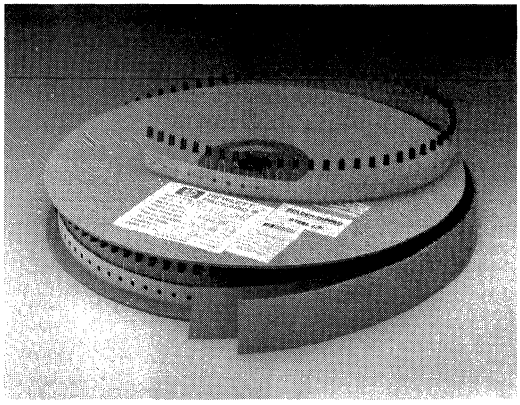
HEWLETT PACKARD

TAPE AND REEL SOLID STATE LAMPS

Leads: 5mm (0.197 inch) Formed Leads — OPTION 001
2.54mm (0.100 inch) Straight Leads — OPTION 002

Features

- **COMPATIBLE WITH RADIAL LEAD AUTOMATIC INSERTION EQUIPMENT**
- **MEETS DIMENSIONAL SPECIFICATIONS OF IEC PUBLICATION 286 AND ANSI/EIA STANDARD RS-468 FOR TAPE AND REEL**
- **REEL PACKAGING SIMPLIFIES HANDLING AND TESTING**
- **T-1 AND T-1 3/4 LED LAMPS AVAILABLE PACKAGED ON TAPE AND REEL**
- **5 mm (0.197 INCH) FORMED LEAD AND 2.54 mm (0.100 INCH) STRAIGHT LEAD SPACING AVAILABLE**



Description

T-1 and T-1 3/4 LED lamps are available on tape and reel as specified by the IEC Publication 286 and ANSI/EIA Standard RS-468. The Option 001 lamp devices have formed leads with 5 mm (0.197 inch) spacing for automatic insertion into PC boards by radial lead insertion equipment. The Option 002 lamp devices have straight leads with 2.54 mm (0.100 inch) spacing, packaged on tape and reel for ease of handling. T-1 lamps are packaged 1800/reel. T-1 3/4 lamps are packaged 1300/reel.

Device Selection Guide

Option	Description
001	Tape and reel, 5 mm (0.197 inch) formed leads.
002	Tape and reel, 2.54 mm (0.100 inch) straight leads.

Package	Quantity/Reel	Order Increments
T-1	1800	1800
T-1 3/4	1300	1300

Ordering Information

To order LED lamps packaged on tape and reel, include the appropriate option code along with the device catalog part number. Example: to order the HLMP-3300 on tape and reel with formed leads (5 mm lead spacing) order as follows: HLMP-3300 Option 001. Minimum order quantities vary by part number. Orders must be placed in reel increments. Please contact your local Hewlett-Packard sales office or franchised Hewlett-Packard distributor for a complete list of lamps available on tape and reel.

LED lamps with 0.46 mm (0.018 inch) square leads with 5 mm (0.197 inch) lead spacing are recommended for use with automatic insertion equipment. It is suggested that insertion machine compatibility be confirmed.

Absolute Maximum Ratings and Electrical/Optical Characteristics

The absolute maximum ratings, mechanical dimension tolerances and electrical/optical characteristics for lamps packaged on tape and reel are identical to the basic catalog device. Refer to the basic data sheet for the specified values.

Notes:
1. Minimum leader length at either end of tape is 3 blank part spaces.
2. Silver saver paper is used as the interlayer for silver plated lead devices.
3. The maximum number of consecutive missing lamps is 3.
4. In accordance with EIA and IEC specs, the anode lead leaves the reel first.
5. Drawings apply to devices with 0.46 mm (0.018 inch) square leads only. Contact Hewlett-Packard Sales Office for dimensions of 0.635 mm (0.025 inch) square lead devices.

Tape and Reel LED Configurations

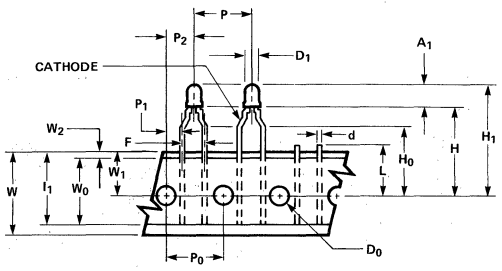


Figure 1. T-1 High Profile Lamps, Option 001

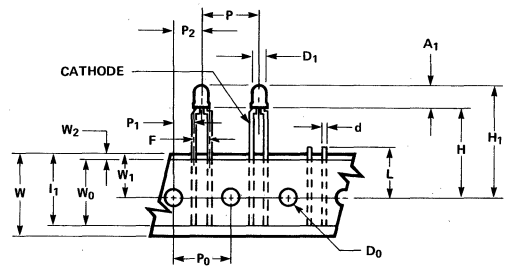


Figure 2. T-1 High Profile Lamps, Option 002

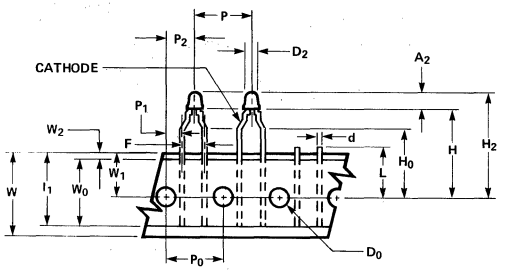


Figure 3. T-1 Low Profile Lamps, Option 001

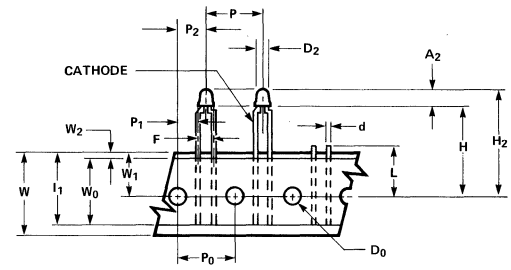


Figure 4. T-1 Low Profile Lamps, Option 002

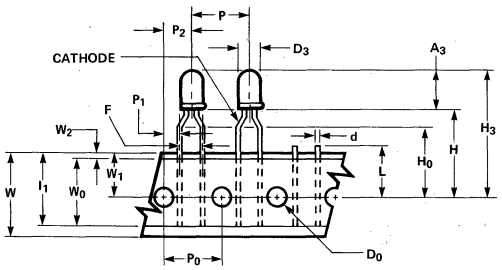


Figure 5. T-1 3/4 High Profile Lamps, Option 001

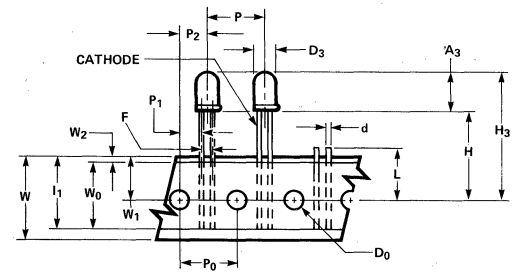


Figure 6. T-1 3/4 High Profile Lamps, Option 002

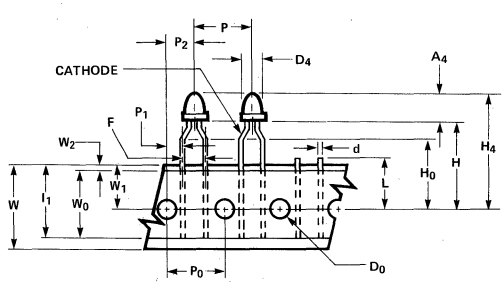


Figure 7. T-1 3/4 Low Profile Lamps, Option 001

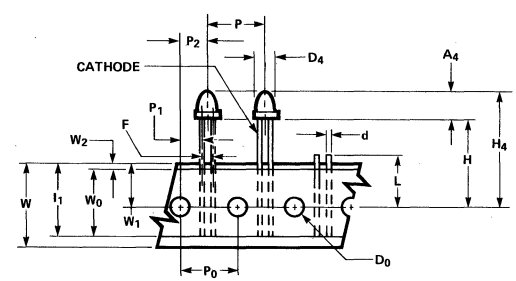
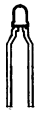
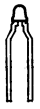
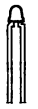
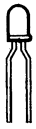
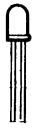
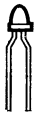
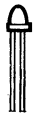


Figure 8. T-1 3/4 Low Profile Lamps, Option 002

Dimensional Specifications for Tape and Reel

Item	Option 001	002	Symbol	Specification	Notes
T1 High Profile Body Height			A1	4.70 (0.185) / 4.19 (0.165)	
Body Diameter			D1	3.18 (0.125) / 2.67 (0.105)	
Component Height			H1	25.7 (1.012) Max.	
T1 Low Profile Body Height			A2	3.73 (0.147) / 3.23 (0.127)	
Body Diameter			D2	3.05 (0.120) / 2.79 (0.110)	
Component Height			H2	24.7 (0.974) Max.	
T1-3/4 High Profile Body Height			A3	9.19 (0.362) / 8.43 (0.332)	
Body Diameter			D3	5.08 (0.200) / 4.32 (0.170)	
Component Height			H3	30.2 (1.189) Max.	
T1-3/4 Low Profile Body Height			A4	6.35 (0.250) / 5.33 (0.210)	
Body Diameter			D4	5.08 (0.200) / 4.32 (0.170)	
Component Height			H4	27.4 (1.079) Max.	
Lead wire thickness			d	0.45 (0.018)	Square Leads
Pitch of component			P	13.7 (0.539) / 11.7 (0.461)	
Feed hole pitch			P_O	12.9 (0.508) / 12.5 (0.492)	Cumulative error: 1.0 mm/20 pitches.
Feed hole center to lead center			P1	4.55 (0.179) / 3.15 (0.124)	Measure at crimp bottom. 5.78/3.68 (0.227/0.1448) for straight leads
Hole center to component center			P2	7.35 (0.289) / 5.35 (0.211)	
Lead to lead distance			F	5.40 (0.213) / 4.90 (0.193)	2.54 (0.100) nominal for straight leads.
Component alignment, front-rear			Δh	0 ± 1.0 (0.039)	Figure 9
Tape width			W	18.5 (0.728) / 17.5 (0.689)	
Hold down tape width			W_O	15.3 (0.602) / 14.7 (0.579)	
Hole position			W1	9.75 (0.384) / 8.50 (0.335)	
Hold down tape position			W2	2.54 (0.100) Max.	
Height of component from hole center			H	21.0 (0.827) / 20.0 (0.787)	
Lead clinch height			H_O	16.5 (0.650) / 15.5 (0.610)	
Feed hole diameter			D_O	4.20 (0.165) / 3.80 (0.150)	
Total tape thickness			t	0.90 (0.035) / 0.50 (0.020)	Paper thickness: 0.55 (0.022) / 0.45 (0.018) Figure 9
Length of snipped lead			L	11.0 (0.433) Max.	
Lead length under hold down tape			l1	14.5 (0.571) Min.	

Note:

1. Dimensions in millimetres (inches), maximum/minimum.

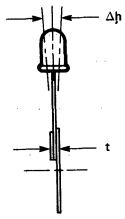


Figure 9. Front to Rear Alignment and Tape Thickness, Typical All Device Types

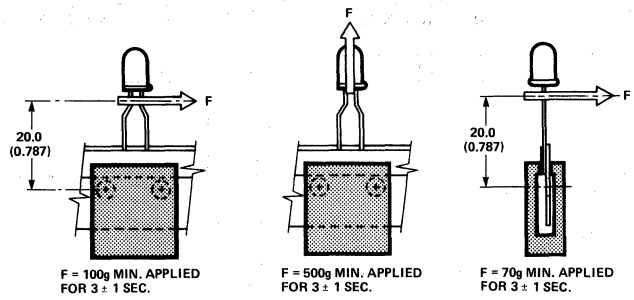
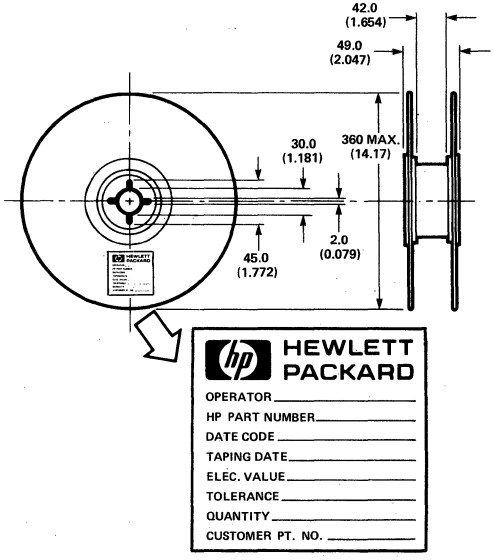


Figure 10. Device Retention Tests and Specifications



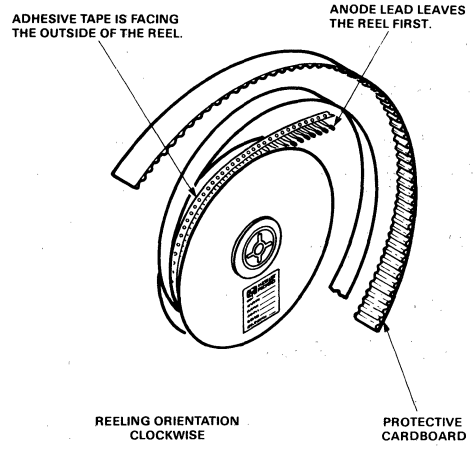


Figure 11. Reel Configuration and Labeling

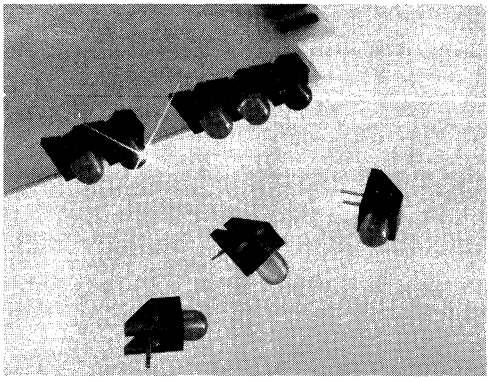
HEWLETT PACKARD

T-1 3/4 (5mm) LED RIGHT ANGLE INDICATORS

OPTION - 010
OPTION - 100

Features

- **IDEAL FOR CARD EDGE STATUS INDICATION**
- **PACKAGE DESIGN ALLOWS FLUSH SEATING ON A PC BOARD**
- **MAY BE SIDE STACKED ON 6.35 mm (0.25") CENTERS**
- **LEDs AVAILABLE IN FOUR COLORS, WITH OR WITHOUT INTEGRATED CURRENT LIMITING RESISTOR IN T-1 3/4 TINTED DIFFUSED PACKAGES**
- **ADDITIONAL CATALOG LAMPS AVAILABLE AS OPTIONS**

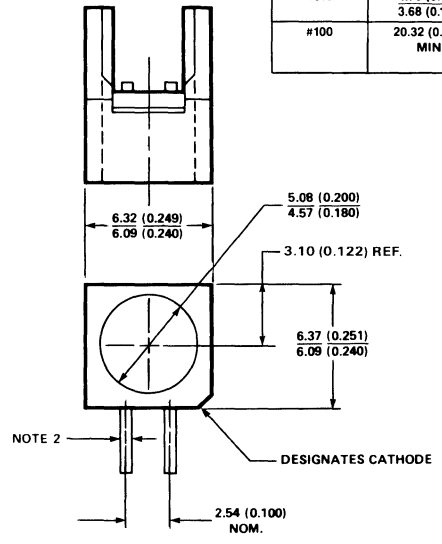


Description

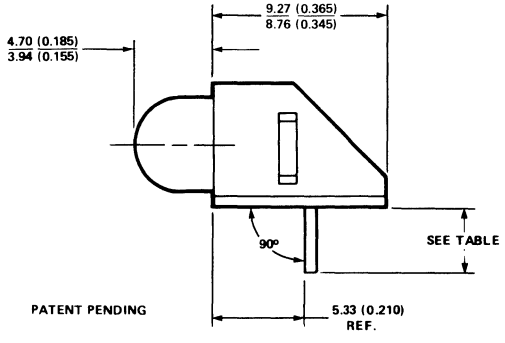
The T-1 3/4 Option 010 and 100 series of Right Angle Indicators are industry standard status indicators that incorporate a tinted diffused T-1 3/4 LED lamp in a black plastic housing. The indicators are available in standard Red, High Efficiency Red, Yellow, or High Performance Green with or without an integrated current limiting resistor. These products are designed to be used as back panel diagnostic indicators and card edge logic status indicators.

Package Dimensions

OPTION NO.	CATHODE LEAD LENGTH	ANODE LEAD LENGTH	
#010	4.70 (0.185) 3.68 (0.145)	4.70 (0.185) 3.68 (0.145)	SHEARED EVEN LEADS
#100	20.32 (0.800) MIN.	1.27 (0.050) NOM. LONGER THAN CATHODE	UNSHEARED UNEVEN LEADS



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. LEAD WIDTH MAY BE 0.45 (0.018) OR 0.64 (0.025) SQUARE NOMINAL DEPENDING UPON PRODUCT TYPE.
3. OPTION 100 IS AVAILABLE FOR LONGER LEADS.



Ordering Information

To order T-1 3/4 high dome lamps in addition to the parts indicated above, select the base part number and add the option code 010 or 100. For example: HLMP-3750-010.

All Hewlett-Packard T-1 3/4 high-dome lamps are available in right angle housing. Contact your local Hewlett-Packard Sales Office or authorized components distributor for additional ordering information.

The Plastic right angle housing may be purchased separately as part number HLMP-5029.

Absolute Maximum Ratings and Electrical/Optical Characteristics

The absolute maximum ratings and device characteristics are identical to those of the T-1 3/4 LED lamps. For information about these characteristics, see the data sheets of the equivalent T-1 3/4 LED lamp.

HEWLETT PACKARD

T-1 (3mm) RIGHT ANGLE LED INDICATORS

OPTION - 010
OPTION - 101

Features

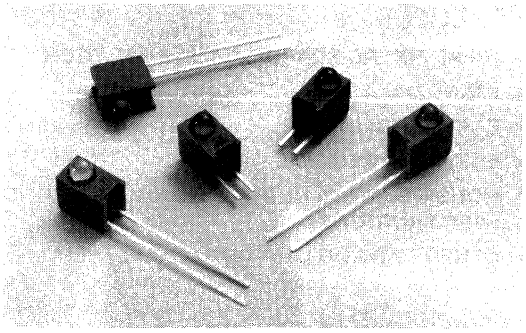
- **IDEAL FOR CARD EDGE STATUS INDICATION**
- **PACKAGE DESIGN ALLOWS FLUSH SEATING ON A PC BOARD**
- **MAY BE SIDE STACKED ON 4.57 mm (0.18 in) CENTERS**
- **UP TO 8 UNITS MAY BE COUPLED FOR A HORIZONTAL ARRAY CONFIGURATION WITH A COMMON COUPLING BAR (SEE T-1 RIGHT ANGLE ARRAY DATA SHEET)**
- **LEDs AVAILABLE IN ALL LED COLORS, WITH OR WITHOUT INTEGRATED CURRENT LIMITING RESISTOR IN T-1 PACKAGES**
- **EASY FLUX REMOVAL DESIGN**
- **HOUSING MATERIAL MEETS UL 94V-0 RATING**
- **ADDITIONAL CATALOG LAMPS AVAILABLE AS OPTIONS**

Description

Hewlett-Packard T-1 Right Angle Indicators are industry standard status indicators that incorporate a tinted diffused T-1 LED lamp in a black plastic housing. The indicators are available in Standard Red, High Efficiency Red, Orange, Yellow, and High Performance Green, with or without an integrated current limiting resistor. These products are designed to be used as back panel diagnostic indicators and card edge logic status indicators.

Ordering Information

To order other T-1 High Dome Lamps in Right Angle Housings in addition to the parts indicated above, select the base part number and add the option code 010 or 101, depending on the lead length desired (see drawing below).



For example, by ordering HLMP-1302-010, you would receive the long lead option. By ordering HLMP-1302-101, you would receive the short lead option.

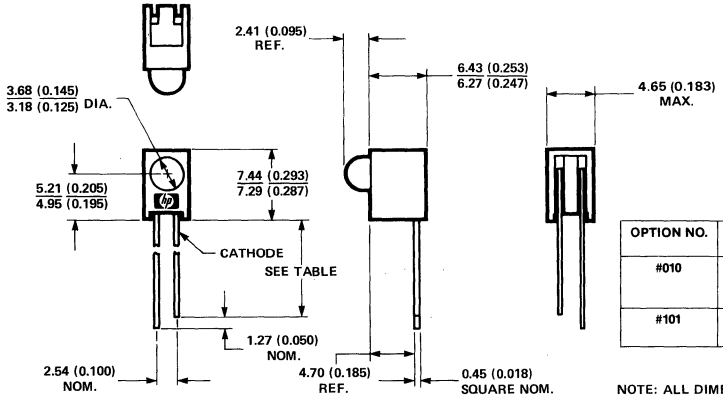
Arrays made by connecting two to eight single Right Angle Indicators with a Common Coupling Bar are available. Ordering information for arrays may be found on the T-1 Right Angle Array data sheet.

The above data sheet information is for the most commonly ordered part numbers. Refer to other T-1 base part number specifications in this catalog for other lamp types that may be ordered with the right angle option.

Absolute Maximum Ratings and Other Electrical/Optical Characteristics

The absolute maximum ratings and typical device characteristics are identical to those of the T-1 LED lamps. For information about these characteristics, see the data sheets of the equivalent T-1 LED lamp.

Package Dimensions



OPTION NO.	CATHODE LEAD LENGTH	ANODE LEAD LENGTH	
#010	18.03 (0.710) MIN.	1.27 (0.050) NOM. LONGER THAN CATHODE	UNSHEARED UNEVEN LEADS
#101	3.43 (0.135) MIN.	3.43 (0.135) MIN.	SHEARED EVEN LEADS

NOTE: ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).

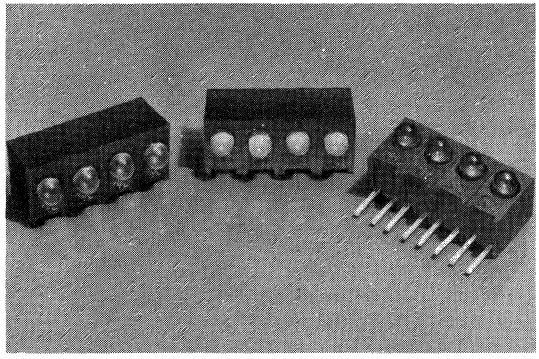
HEWLETT PACKARD

T-1 (3 mm) RIGHT ANGLE ARRAYS

OPTION:
102 103 104 105 106 107 108

Features

- **IDEAL FOR PC BOARD STATUS INDICATION**
- **STANDARD 4 ELEMENT CONFIGURATION**
- **EASY HANDLING**
- **EASY FLUX REMOVAL**
- **HOUSING MEETS UL 94V-O FLAMMABILITY SPECIFICATIONS**
- **OTHER CATALOG LAMPS AVAILABLE**



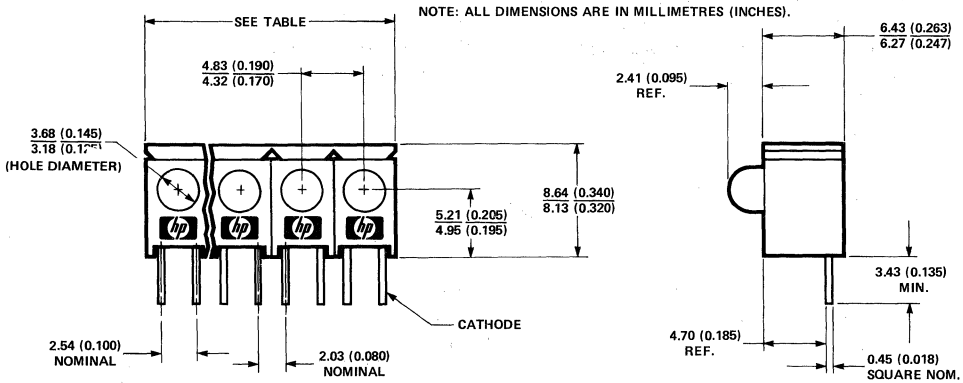
Description

These T-1 right angle arrays incorporate standard T-1 lamps for a good balance of viewing angle and intensity. Single units are held together by a plastic tie bar. The leads of each member of the array are spaced on 2.54 mm (0.100 in) centers. Lead spacing between adjacent lamps in the array is on 2.03 mm (0.080 in) centers. These products are designed to be used as back panel diagnostic indicators and logic status indicators on PC boards.

Ordering Information

Use the option code 102 through 108 in addition to the base part number to order these arrays. Arrays from 2 to 8 elements in length and special lamp color combinations within an array are available. Please contact your nearest Hewlett-Packard Components representative for ordering information on these special items.

Package Dimensions



OPTION NO.	ARRAY LENGTH	OPTION NO.	ARRAY LENGTH	OPTION NO.	ARRAY LENGTH
#102	9.65 (0.380) 8.79 (0.346)	#105	23.14 (0.911) 22.73 (0.895)	#108	36.70 (1.445) 36.45 (1.435)
#103	14.22 (0.560) 13.36 (0.526)	#106	27.71 (1.091) 27.31 (1.075)		
#104	18.57 (0.731) 18.16 (0.715)	#107	32.28 (1.271) 31.88 (1.255)		

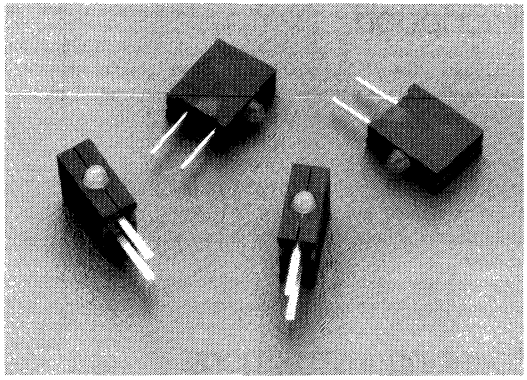
HEWLETT PACKARD

SUBMINIATURE LED RIGHT ANGLE INDICATORS

RED HLMP-6000-010
HIGH EFFICIENCY RED HLMP-6300-010
YELLOW HLMP-6400-010
GREEN HLMP-6500-010

Features

- **IDEAL FOR PC BOARD STATUS INDICATION**
- **SIDE STACKABLE ON 2.54 mm (0.100 in) CENTERS**
- **AVAILABLE IN FOUR COLORS**
- **HOUSING MEETS UL 94V-O FLAMMABILITY SPECIFICATIONS**
- **ADDITIONAL CATALOG LAMPS AVAILABLE AS OPTIONS**



Description

The Hewlett-Packard series of Subminiature Right Angle Indicators are industry standard status indicators that incorporate tinted diffused LED lamps in black plastic housings. The 2.54 mm (0.100 in) wide packages may be side stacked for maximum board space savings. The silver plated leads are in line on 2.54 mm (0.100 in) centers, a standard spacing that makes the PC board layout straightforward. These products are designed to be used as back panel diagnostic indicators and logic status indicators on PC boards.

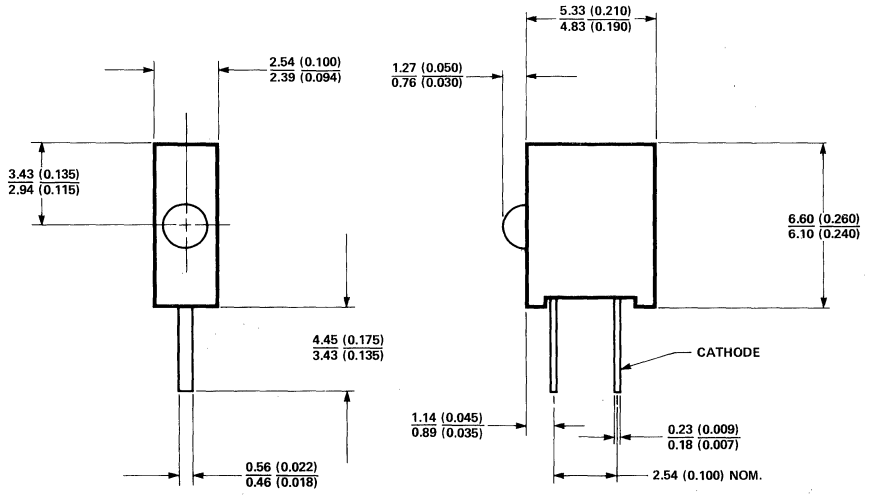
Ordering Information

To order Subminiature Right Angle indicators, order the base part number and add the option code 010. For price and delivery on Resistor Subminiature Right Angle Indicators and other subminiature LEDs not indicated above, please contact your nearest H.P. Components representative.

Absolute Maximum Ratings and Other Electrical/Optical Characteristics

The absolute maximum ratings and typical device characteristics are identical to those of the Subminiature lamps. For information about these characteristics, see the data sheets of the equivalent Subminiature lamp.

Package Dimensions



NOTE: ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).

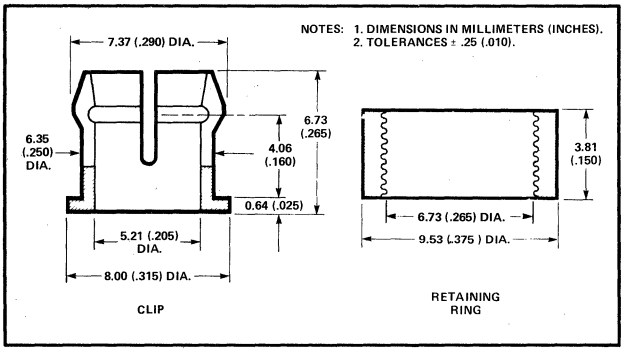
HEWLETT PACKARD

CLIP AND RETAINING RING FOR PANEL MOUNTED T1 3/4 LEDs

OPTION 009 (HLMP-0103)

Description

The Option 009 (HLMP-0103) is a black plastic mounting clip and retaining ring. It is designed to panel mount Hewlett-Packard Solid State high profile T-1 3/4 size lamps. This clip and ring combination is intended for installation in instrument panels from 1.52mm (.060") to 3.18mm (.125") thick. For panels greater than 3.18mm (.125") counterboring is required to the 3.18mm (.125") thickness.



Mounting Instructions

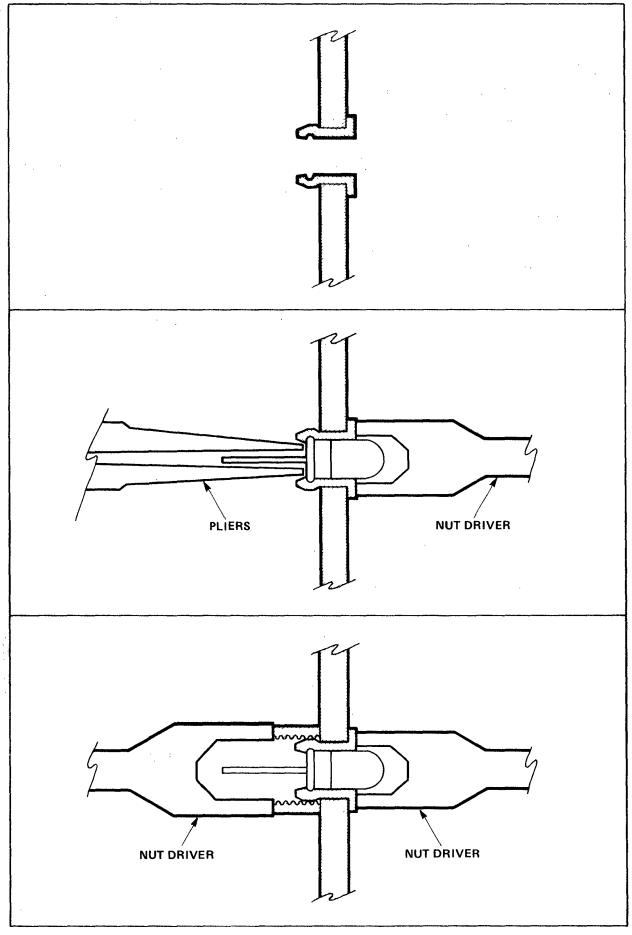
1. Drill an ASA C size 6.15mm (.242") dia. hole in the panel. Deburr but do not chamfer the edges of the hole.

2. Press the panel clip into the hole from the front of the panel.

3. Press the LED into the clip from the back. Use blunt long nose pliers to push on the LED. Do not use force on the LED leads. A tool such as a nut driver may be used to press on the clip.

Note: Clip and retaining ring are also available for T-1 package, from a non-HP source. Please contact Interconsal Association, 2584 Wyandotte Way, Mountain View, CA for additional information.

4. Slip a plastic retaining ring onto the back of the clip and press tight using tools such as two nut drivers.



Ordering Information

T-1 3/4 High Dome LED Lamps can be purchased to include clip and ring by adding Option Code 009 to the device catalog part number.

Example:

To order the HLMP-3300 including clip and ring, order as follows: HLMP-3300 Option 009.

Hermetic Lamps

Hermetic Lamps

In addition to Hewlett-Packard commercial solid state lamps, Hewlett-Packard offers a complete line of hermetically sealed solid state lamps which are listed on MIL-S-19500 Qualified Parts List. For applications where suppression of infrared (IR) emission is essential, IR-secure indicators, which conform to the Defense Electronics Supply Center (DESC) Selected Item Drawing 87019 are also available.

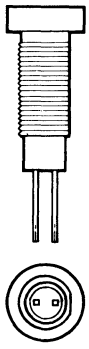
Hewlett-Packard offers the following families of military grade hermetic and panel mount hermetic LED lamps, hi-rel screened to military specifications:

- IR Secure panel mount lamps, designed and screened to meet the requirements of DESC Drawing 87019.
- JAN and JANTX hermetic and panel mount hermetic lamps, screened to the requirements of MIL-S-19500 slash sheet specifications and listed on the MIL-S-19500 Qualified Parts List (QPL).
- Ultrabright hermetic and ultrabright panel mount hermetic lamps screened to the JAN and JANTX requirements of MIL-S-19500.

These military grade hermetic and panel mount hermetic lamps are produced and hi-rel screened at Hewlett-Packard's DESC qualified facilities, approved to the requirements of MIL-S-19500 and MIL-STD-750.

The applicable MIL-S-19500 or DESC 87019 screening tables are detailed on each hermetic lamp data sheet.

IR Secure, Hermetically Sealed LED Lamps, DESC Approved

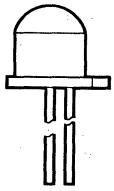
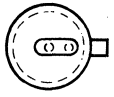
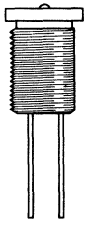
Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	**87019G01**[1]	Green (567 nm)	Panel Mount Version	Glass 0.3% IR (620 nm to 930 nm)[2]	2.0 mcd @ 10 mA	24	2.2 V @ 10 mA	3-134
	87019Y01[1]	Yellow (585 nm)	Panel Mount Version	Glass 0.2% IR (675 nm to 930 nm)[2]	2.0 mcd @ 10 mA		2.0 V @ 10 mA	

Notes:

1. Military approved to DESC Drawing 87019.
2. Percent radiometric power emission between specified wavelengths as compared to the radiometric power between 350 nm and 930 nm.

Bold Type – New Product

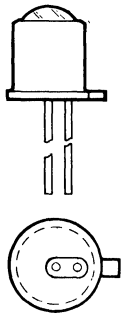
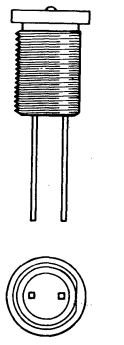
Hermetically Sealed JAN Qualified LED Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	1N5765 JAN1N5765[1] JANTX1N5765[1]	Red (640 nm)	Hermetic/T0-46	Red Diffused	1.0 mcd @ 20 mA	70°	1.6 V @ 20 mA	3-142
	1N6092 JAN1N6092[1] JANTX1N6092[1]	High Efficiency Red (626 nm)			8.0 mcd @ 20 mA		2.0 V @ 20 mA	
	1N6093 JAN1N6093[1] JANTX1N6093[1]	Yellow (585 nm)		Yellow Diffused	8.0 mcd @ 20 mA		2.0 V @ 20 mA	
	1N6094 JAN1N6094[1] JANTX1N6094[1]	Green (570 nm)		Green Diffused	8.0 mcd @ 25 mA		2.1 V @ 25 mA	
	HLMP-0904 HLMP-0930 HLMP-0931	Red (640 nm)	Panel Mount Version	Red Diffused	1.0 mcd @ 20 mA	70°	1.6 V @ 20 mA	
	HLMP-0354 JANM19500/ 51901[1] JTXM19500/ 51902[1]	High Efficiency Red (626 nm)			8.0 mcd @ 20 mA		2.0 V @ 20 mA	
	HLMP-0454 JANM19500/ 52001[1] JTXM19500/ 52002[1]	Yellow (585 nm)		Yellow Diffused	8.0 mcd @ 20 mA		2.0 V @ 20 mA	
	HLMP-0554 JANM19500/ 52101[1] JTXM19500/ 52102[1]	Green (570 nm)		Green Diffused	8.0 mcd @ 25 mA		2.1 V @ 25 mA	

Note:

1. Military qualified and listed on the MIL-S-19500 Qualified Parts List (QPL).

Hermetically Sealed JAN Qualified Ultra-Bright LED Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	**1N6609** **JAN1N6609**[1] **JANTX1N6609**[1]	High Efficiency Red (626 nm)	Hermetic TO-18[3]	Clear Glass	50.0 mcd @ 20 mA	18	2.0 V @ 20 mA	3-153
	1N6610 **JAN1N6610**[1] **JANTX6610**[1]	Yellow (585 nm)			50.0 mcd @ 20 mA		2.0 V @ 20 mA	
	1N6611 **JAN1N6611**[1] **JANTX6611**[1]	Green (570 nm)			50.0 mcd @ 25 mA		2.1 V @ 25 mA	
	**HLMP-0364** **JANM19500/ 51903**[1] **JANTXM19500/ 51904**[1]	High Efficiency Red (626 nm)	Panel Mount Version	Clear Glass	50.0 mcd @ 20 mA	18	2.0 V @ 20 mA	
	HLMP-0464 **JANM19500/ 52003**[1] **JANTXM19500/ 52004**[1]	Yellow (585 nm)			50.0 mcd @ 20 mA		2.0 V @ 20 mA	
	HLMP-0545 **JANM19500/ 52103**[1] **JANTXM19500/ 52104**[1]	Green (570 nm)			50.0 mcd @ 25 mA		2.1 V @ 25 mA	

Notes:

1. Military qualified and listed on theMIL-S-19500 Qualified Parts List (QPL).

Bold Type – New Product

HEWLETT PACKARD

IR Secure, Hermetic, Panel Mount Solid State Lamps DESC Approved

Technical Data

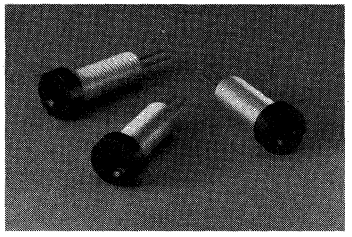
87019G01 Green
87019Y01 Yellow

Features

- **Designed for IR Secure Lighting Applications**
- **Conforms to Requirements of DESC Drawing 87019**
  100% Screening
- **Integral Glass NVG Filter with Antireflection Coating**
  Suppresses IR Emissions at all Viewing Angles
  Green: 0.3% IR (620 nm to 930 nm)[1]
  Yellow: 0.2% IR (675 nm to 930 nm)[1]
- **True Hermetic LED Lamp**
  Identical in Design to MIL-S-19500/520/521
  Produced and Tested in a DESC Qualified Facility
- **Choice of Colors**
  567 nm Green
  585 nm Yellow
- **Panel Mount Package**
  Exceeds the Sealing Requirements of MIL-L-3661
  Solder Dipped Leads, Electrically Isolated from Package
- **Low Power Operation**
- **IC Compatible**

Description

The 87019G01 high performance green and 87019Y01 yellow front panel mountable LED indicators conform to the requirements of the DESC Selected Item Drawing 87019 and are designed for use in infrared (IR) secure lighting applications. These devices are constructed by



assembling true hermetic solid state lamps into panel mountable aluminum sleeves. They are produced on Hewlett-Packard's hermetic lamp line which has been approved and qualified by the Defense Electronics Supply Center (DESC) to the requirements of MIL-S-19500 and MIL-STD-750. An integral night vision goggle (NVG) filter mounted within the collar of each sleeve provides suppression of IR emissions.

Lamp Selection Guide

DESC Part Number	Color	(λd)	I_v (10 mA) Typ (mcd)	Typical Suppressed IR Emission
87019G01	Green	567 nm	2.0	0.3% IR (620 nm to 930 nm)[1]
87019Y01	Yellow	585 nm	2.0	0.2% IR (675 nm to 930 nm)[1]

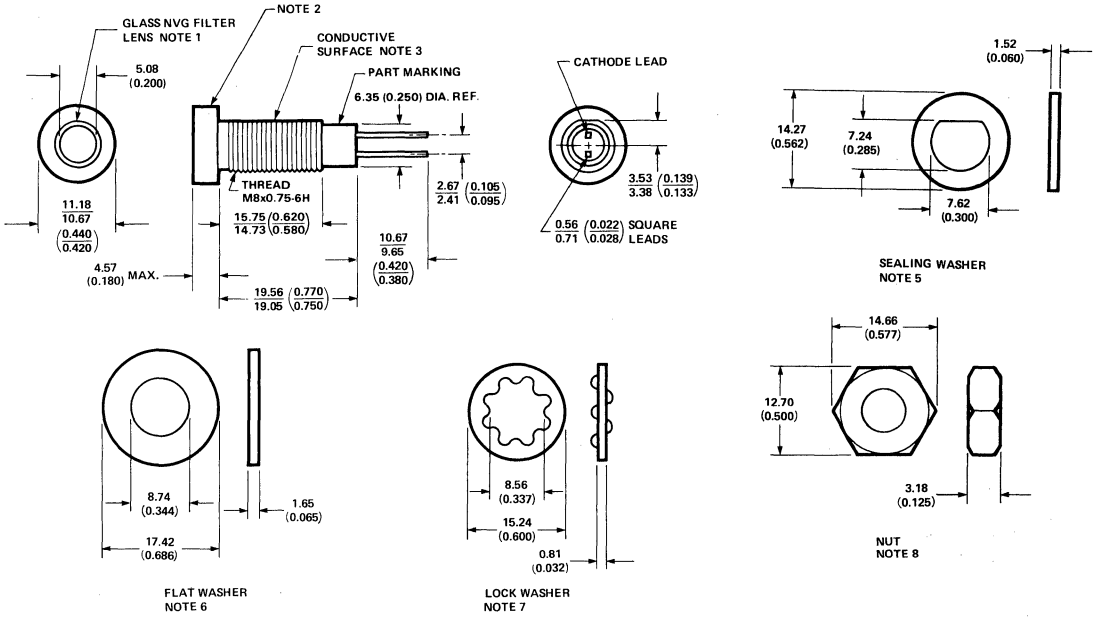
Note:
1. Percent radiometric power emission between specified wavelengths as compared to the radiometric power between 350 nm and 930 nm.

Absolute Maximum Ratings at T_A = 25°C

Parameter	Green 87019G01	Yellow 87019Y01	Units
Power Dissipation	105	100	mW
DC Forward Current[1]	35	35	mA
Peak Forward Current	90	60	mA
Average Forward Current	30	30	mA
Operating and Storage Temperature Range	-55°C to +100°C		
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 7 seconds		

Note:
1. Derate from 50°C at 0.5 mA/°C

Package Dimensions 87019G01/87019Y01



Notes:
1. Glass NVG filter with a front surface antireflection coating per MIL-C-14806.
2. Collar of sleeve is black anodized per MIL-A-8625.
3. Panel mount sleeve material is aluminum alloy with conductive chromate conversion coating per MIL-C-5541.
4. Recommended panel hole diameter for mounting is 8.03/8.00 mm (0.319/0.315 inch).
5. Sealing washer, synthetic rubber, black, 60 durometer per MIL-R-6855.
6. Stainless steel flat washer per MS-15795.
7. Steel lock washer, cadmium plated, per MS-35333.
8. Aluminum alloy nut, M8x0.75-6H metric threads, with conductive chromate conversion coating per MIL-C-5541.
9. All dimensions in millimetres (inches).
10. Weight of panel mount lamp assembly, exclusive of mounting hardware, is 2.8 grams.

Electrical/Optical Characteristics at T_A = 25°C

Symbol	Description	Green			Yellow			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
I_v	Axial Luminous Intensity	0.5	2.0 7.0	5.0	0.5	2.0 5.0	4.0	mcd	I_F = 10 mA I_F = 20 mA I_F = 25 mA
I_D	LED Diffusion	50		150	50		150	% of I_V	I_F = 10 mA[1]
P_E	Total Power Emission 350 nm to 930 nm			1			1	µW	I_F = 10 mA[2]
P_{IRG} P_{IRY}	Infrared Power Emission 620 nm to 930 nm 675 nm to 930 nm		0.3	0.5		 0.2	 0.5	% of P_E	I_F = 10 mA[3]
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		24			24		deg	I_F = 10 mA[4]
$2\theta_c$	Included Angle Between 0.5% Luminous Intensity Points		50	60		50	60	deg	I_F = 10 mA[5]
λ_{PEAK}	Peak Wavelength		568			583		nm	
λ_d	Dominant Wavelength	555	567	572	580	585	590	nm	Note 6
τ_s	Speed of Response		200			200		ns	
C	Capacitance		35	100		35	100	pF	V_F = 0; f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance LED Junction to Cathode Pin		425			425		°C/W	Note 7
V_F	Forward Voltage	1.6	2.2	2.5	1.6	2.0	2.5	V	I_F = 10 mA
I_R	Reverse Current			100			100	µA	V_R = 5 V
η_v	Luminous Efficacy		600			455		lm/W	Note 8
R_{ISO}	Insulation Resistance	1000			1000			MΩ	Note 9

Notes:

1. LED diffusion, I_D, is the variation of luminous intensity across the face of the NVG filter. Light output measurements are in accordance with DESC Drawing 87019.
2. Total power, P_E, is the amount of radiometric power in watts from 350 nm to 930 nm emitted by the lamp through the NVG filter.
3. Infrared power, P_{IRG} (green) and P_{IRY} (yellow), is the ratio of the infrared power emitted thorugh the NVG filter between the wavelengths indicated to the total radiometric power emitted between 350 nm and 930 nm, P_E.
4. $\theta_{1/2}$ is the off-axis angle where the luminous intensity is half the on-axis value. $\theta_{1/2}$ TYP = 12°C.
5. θ_c is the off-axis angle where the luminous intensity is 0.5% of the on-axis value. θ_c TYP = 25°C, θ_c MAX = 30°.
6. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and represents the single wavelength which defines the color of the device.
7. Junction to cathode lead with 3.18 mm (0.125 inch) of lead exposed between base of lamp and heat sink.
8. Radiant intensity, I_e, in watts/steradian, may be determined from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.
9. Insulation resistance is between both leads and the metal sleeve.

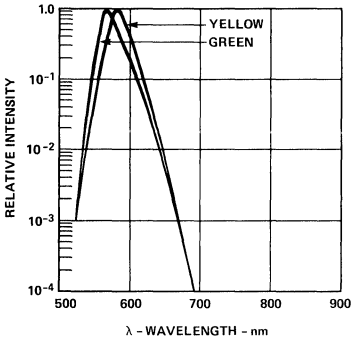


Figure 1. Relative Intensity vs. Wavelength

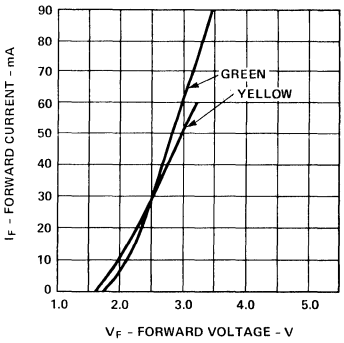


Figure 2. Forward Current vs. Forward Voltage

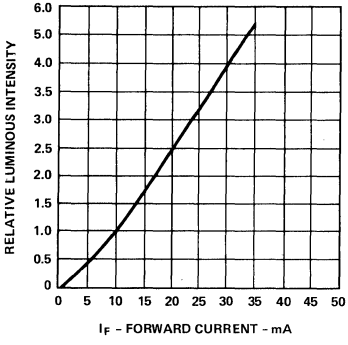


Figure 3. Relative Luminous Intensity vs. Forward Current

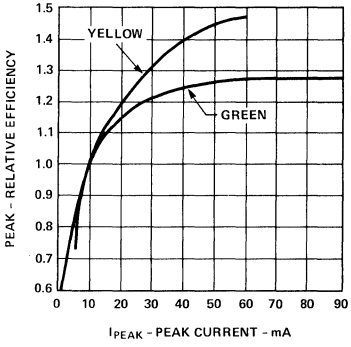


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current

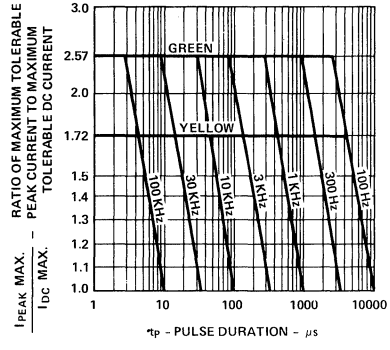


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

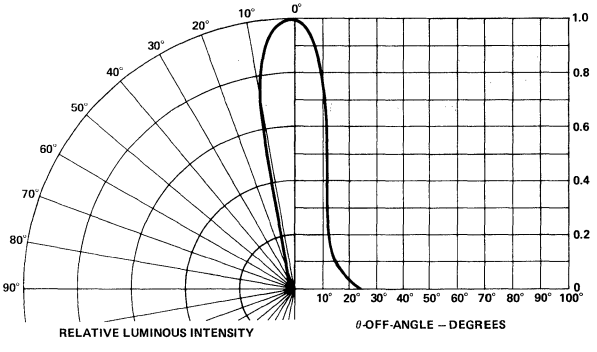


Figure 6. Relative Luminous Intensity vs. Angular Displacement

High-Reliability Screening as Defined by DESC Drawing 87019

All lamps are subjected to 100 percent screening as listed in Table I. Random samples are pulled from each lot and are subjected to Group A electrical/optical and mechanical tests as listed in Table II. Random sample Group B quality conformance tests in accordance with MIL-S-19500 subgroups, as listed in Table III, are performed every six months.

Table I. Screening Tests

Test	MIL-STD-750 Method	Measurements and Conditions
High Temperature Storage (Nonoperating)	1032	T_A = 100°C, time = 72 hours
Thermal Shock (Temperature Cycling)	1051	Test condition A, except $T_{(high)}$ = +100°C, 10 cycles; time at temperature extremes = 15 minutes minimum.
Constant Acceleration	2006	Nonoperating 20,000 g; Y_1 only.
Seal	1011	Test condition A
Pre Burn-in Measurements	4011 4016	I_V[1] V_F[1] I_R[1]
Burn-in (Forward Bias)		I_F = 20 mA dc for yellow, I_F = 30 mA dc for green, 168 hours minimum
Post Burn-in Measurements	4011 4016	I_V (within 72 hours of burn-in)[1] V_F[1] I_R[1] P_E[1] ΔI_v = -20% maximum from inital value ΔV_F = ±50 mV from initial value

Note:
1. Limits and conditions are those listed in the electrical/optical characteristics.

Table II. Group A Inspection

Inspection	MIL-STD-750 Method	MIL-STD-750 Conditions	LTPD	Symbol	Limits Min.	Limits Max.	Unit
Subgroup 1 Visual and mechanical inspection	2071		5				
Subgroup 2 Luminous intensity		I_F = 10 mA dc	7	I_V		Verify light output	
Forward voltage	4011	I_F = 10 mA dc		V_F		2.5	V dc
Reverse current	4016	V_R = 5 V dc		I_R		100	µA dc
Subgroup 3 High temperature		T_A = +100°C					
Luminous intensity		I_F = 10 mA dc	10	I_V		Verify light output	
Reverse current	4016	V_R = 5 V dc		I_R		100	µA dc
Low temperature		T_A = -55°C					
Luminous intensity		I_F = 10 mA dc		I_V		Verify light output	
Forward voltage	4011	I_F = 10 mA dc		V_F		2.5	Vdc
Subgroup 4 Insulation resistance	1016		10	R_{ISO}	1000		MΩ
Subgroup 5		Not applicable					
Subgroup 6		Not applicable					
Subgroup 7 Power emission		Note 1	10	P_{IRY} P_{IRG}		0.5 0.5	% %

Note:
1. Test conditions and wavelength limits are those listed in the electrical/optical characteristics.

Table III. Group B Inspection

Inspection	MIL-STD-750		Sampling Plan
	Method	Conditions	
Subgroup 1			5/0
Solderability	2026		
Resistance to solvents	1022		
Subgroup 2			5/0
Thermal shock	1051	Test condition A, $T_{(high)}$ = 100°C	
Immersion (seal)	1011	Test condition A	
Watertightness (panel sealing)		See MIL-L-3661, sealing test watertight, except maximum pressure is 30 psi.	
Electrical/Optical endpoints		I_v, V_F, I_R, λ_d, P_E, P_{IR}, I_D, R_{ISO}[1]	
Subgroup 3			5/0
Life test	1027		
Electrical/Optical endpoints		I_v, V_F, I_R, λ_d, P_E, P_{IR}, I_D, R_{ISO}[1]	
Subgroup 4 and 5		Not applicable	
Subgroup 6			5/0
High temperature life (nonoperating)	1032		
Electrical/Optical endpoints		I_v, V_F, I_R, λ_d, P_E, P_{IR}, I_D, R_{ISO}[1]	
Subgroup 7			5/0
Terminal strength	2036	Test condition A, 2 pounds for 20 seconds	
Vibration	2056		
Mechanical shock	2016		
Electrical/Optical endpoints		I_v, V_F, I_R, λ_d, P_E, P_{IR}, I_D, R_{ISO}[1]	

Note:
1. Limits and conditions are those listed in the electrical/optical characteristics.

Application Information

IR Secure Lighting

The objective of IR secure lighting is to suppress IR emission from a light source in order to reduce the susceptibility of detection by a threat optical infrared image intensifier. IR Secure Lighting is derived from the Priority 1 Wavelength Restriction objective of the U.S. Army CECOM Statement of Work for NVG Secure Lighting. The Priority 1 objective limits the amount of IR energy as follows:

> "Between 350 nm and 930 nm, no more than 0.5% of the total energy emitted shall be above 700 nm. The wavelength cut-off to 0.5% shall begin between 600 nm and 700 nm, and shall be as close to 600 nm as possible."

Mechanical/Optical

Each 87019G01 and 87019Y01 secure lamp is constructed by assembling a military grade true hermetic LED lamp into an aluminum alloy panel mountable sleeve. The internal design of the sleeve provides a light trap that shapes the radiation pattern into a narrow viewing angle necessary for IR Secure Lighting applications, limits the luminous intensity to less than 0.5% of the on-axis value at off-axis angles greater than 30°, and provides increased contrast enhancement for daylight viewing. A glass NVG filter with a front surface antireflection coating per MIL-C-14806 is integrally mounted in the collar of the sleeve. The NVG filter provides suppression of IR energy to meet the Priority 1 objective. The IR suppression is constant with respect to off-axis viewing angles. The luminance of these lamps may be reduced by either decreasing the DC forward current or by using pulse width modulation of the peak current.

The collar of the panel mountable sleeve surrounding the NVG filter is black anodized to enhance viewability. The chromate conversion coating on the body of the sleeve is electrically conductive, thus permitting an effective EMI attenuation seal to be formed with the front panel by way of a positive mechanical and electrical contact through the mounting hardware. The solder dipped leads are electrically insulated from the sleeve. The front and rear sealing techniques and materials maximize the sealed surface areas to achieve superior resistance to moisture and adverse environments, exceeding the sealing and immersion requirements of MIL-L-3661. The maximum torque that may be applied to the nut is 3.62 N-m (32 in-lbs).

HEWLETT PACKARD

JAN Qualified Hermetic Solid State Lamps*

Technical Data

1N5765
JAN1N5765
JANTX1N5765
1N6092
JAN1N6092
JANTX1N6092
1N6093
JAN1N6093
JANTX1N6093
1N6094
JAN1N6094
JANTX1N6094

Features

- **Military Qualified**
- **Listed on MIL-S-19500 QPL**
- **Choice of Four Colors**
  Red
  High Efficiency Red
  Yellow
  Green
- **Designed for High-Reliability Applications**
- **Hermetically Sealed**
- **Wide Viewing Angle**
- **Low Power Operation**
- **IC Compatible**
- **Long Life**
- **Panel Mount Configuration**

Description

The 1N5765, 1N6092, 1N6093 and 1N6094 solid state LEDs are hermetically sealed in a TO-46 package with a tinted, diffused plastic lens over a glass window. These devices are designed for high reliability applications and provide excellent on-off contrast, high axial luminous intensity, and a wide viewing angle. The panel mount versions consist of an LED unit permanently mounted in an anodized aluminum sleeve.

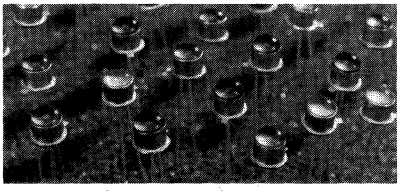
The 1N5765 utilizes a GaAsP LED chip with a red diffused lens over a glass window.

The 1N6092 has a high efficiency red GaAsP on GaP LED chip with a red diffused lens over a glass window. This device is comparable to the 1N5765 but its efficiency extends to higher currents and it provides greater luminous intensity.

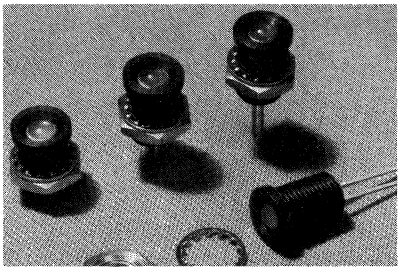
The 1N6093 provides a yellow GaAsP on GaP LED chip with a yellow, diffused lens over a glass window.

The 1N6094 utilizes a green GaP LED chip with a green, diffused lens over a glass window.

The plastic lens over glass window system is extremely durable and has exceptional temperature cycling capabilities.



HERMETIC TO-46 LAMP



PANEL MOUNT LAMP ASSEMBLY

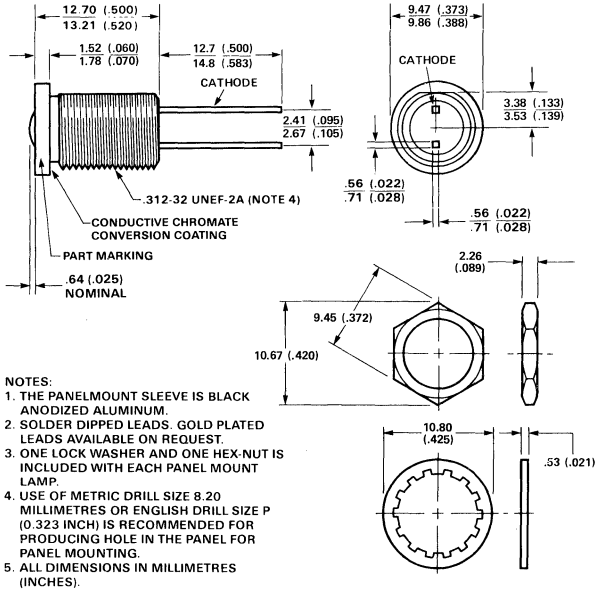
*Panel mount versions of all of the above are available per the selection matrix on the next page.

COLOR – PART NUMBER – LAMP AND PANEL MOUNT MATRIX				
Description	**Standard Product**	**With JAN Qualification[1]**	**JAN Plus TX Testing[2]**	**Controlling MIL-S-19500 Document[4]**
TABLE A. Hermetic TO-46 Part Number System				
Standard Red	1N5765	JAN1N5765	JANTX1N5765	/467
High Efficiency Red	1N6092	JAN1N6092	JANTX1N6092	/519
Yellow	1N6093	JAN1N6093	JANTX1N6093	/520
Green	1N6094	JAN1N6094	JANTX1N6094	/521
TABLE B. Panel Mountable Part Number System[3]				
Standard Red	HLMP-0904	HLMP-0930	HLMP-0931	None
High Efficiency Red	HLMP-0354	HLMP-0380 (JANM19500/51901)	HLMP-0381 (JTXM19500/51902)	/519
Yellow	HLMP-0454	HLMP-0480 (JANM19500/52001)	HLMP-0481 (JTXM19500/52002)	/520
Green	HLMP-0554	HLMP-0580 (JANM19500/52101)	HLMP-0581 (JTXM19500/52102)	/521

Notes:
1. Parts are marked with the JAN part number.
2. Parts are marked with the JANTX part number.
3. Panel mountable packaging incorporates the Table A TO-46 part into a panel mount enclosure.
4. JAN and JANTX parts only.

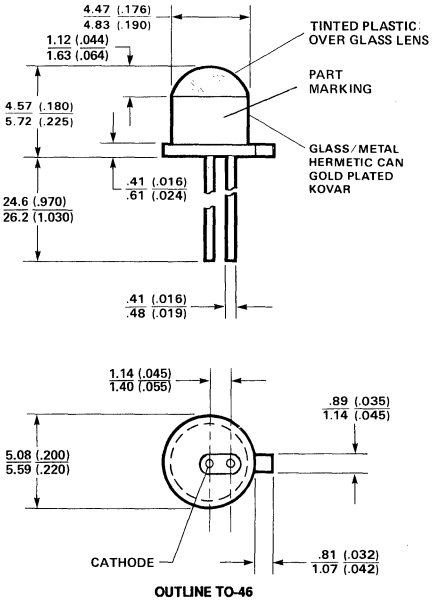
Package Dimensions

HLMP-0904, 0354, 0454, 0554



NOTES:
1. THE PANELMOUNT SLEEVE IS BLACK ANODIZED ALUMINUM.
2. SOLDER DIPPED LEADS. GOLD PLATED LEADS AVAILABLE ON REQUEST.
3. ONE LOCK WASHER AND ONE HEX-NUT IS INCLUDED WITH EACH PANEL MOUNT LAMP.
4. USE OF METRIC DRILL SIZE 8.20 MILLIMETRES OR ENGLISH DRILL SIZE P (0.323 INCH) IS RECOMMENDED FOR PRODUCING HOLE IN THE PANEL FOR PANEL MOUNTING.
5. ALL DIMENSIONS IN MILLIMETRES (INCHES).
6. PACKAGE WEIGHT INCLUDING LAMP AND PANEL MOUNT IS 1.2 - 1.8 GRAMS. NUT AND WASHER IS AN EXTRA 0.6 - 1.0 GRAM.

1N5765, 1N6092, 1N6093, 1N6094



OUTLINE TO-46

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. GOLD-PLATED KOVAR LEADS.
3. PACKAGE WEIGHT OF LAMP ALONE IS .25 - .40 GRAMS.

Absolute Maximum Ratings at T_A = 25°C

Parameter	Red HLMP-0904	High Eff. Red HLMP-0354	Yellow HLMP-0454	Green HLMP-0554	Units
Power Dissipation (derate linearly from 50°C at 1.6 mW/°C)	100	120	120	120	mW
DC Forward Current	50[1]	35[2]	35[2]	35[2]	mA
Peak Forward Current	1000 See Fig. 5	60 See Fig. 10	60 See Fig. 15	60 See Fig. 20	mA
Operating and Storage Temperature Range	-65°C to +100°C				
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 7 seconds.				

Notes:
1. Derate from 50°C at 0.2 mA/°C.
2. Derate from 50°C at 0.5 mA/°C.

Electrical/Optical Characteristics at T_A = 25°C

Sym.	Description	1N5765/ HLMP-0904			1N6092/ HLMP-0354			1N6093/ HLMP-0454			1N6094/ HLMP-0554			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{V1}	Axial Luminous Intensity	0.5	1.0		3.0	8.0		3.0	8.0		3.0	8.0		mcd	I_F = 20 mA Figs. 3, 8, 13, 18 θ = 0°
											At I_F = 25 mA				
I_{V2}	Luminous Intensity at θ = 30°	1.5			1.5			1.5			1.5			mcd	I_F = 20 mA θ = 30°
											At I_F = 25 mA				
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points[1]		60			70			70			70		deg	Figures 6, 11, 16, 21
λ_{PEAK}	Peak Wavelength	630	655	700	590	635	695	550	583	660	525	565	600	nm	Measurement at Peak
λ_d	Dominant Wavelength[2]		640			626			585			570		nm	
τ_s	Speed of Response		10			200			200			200		ns	
C	Capacitance		200	300		35	100		35	100		35	100	pF	V_F = 0; f = 1 MHz
$R\theta_{J-PIN}$	Thermal Resistance*[3]		425			425			425			425		°C/W	
$R\theta_{J-PIN}$	Thermal Resistance**[3]		550			550			550			550		°C/W	
V_F	Forward Voltage		1.6	2.0		2.0	3.0		2.0	3.0		2.1	3.0	V	I_F = 20 mA Figures 2, 7, 12, 17
												At I_F = 25 mA			
I_R	Reverse Current			1.0			1.0			1.0			1.0	μA	V_R = 3 V
BV_R	Reverse Breakdown Voltage	4.0	5.0		5.0			5.0			5.0			V	I_R = 100 μA
η_v	Luminous Efficacy[4]		56			140			455			600		lm/W	

Notes:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Junction to Cathode Lead with 3.18 mm (0.125 inch) of leads exposed between base of flange and heat sink.
4. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e=I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

*Panel mount.
**T0-46.

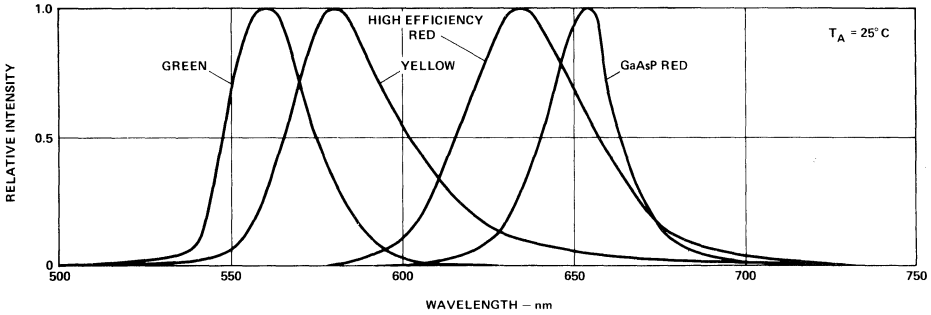


Figure 1. Relative Intensity vs. Wavelength.

Family of Red 1N5765/HLMP-0904

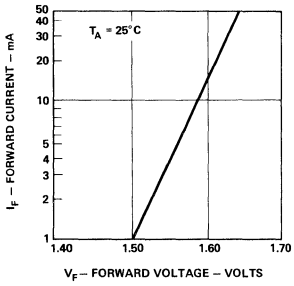


Figure 2. Forward Current vs. Forward Voltage.

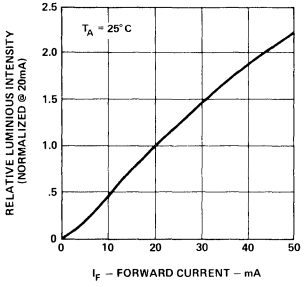


Figure 3. Relative Luminous Intensity vs. Forward Current.

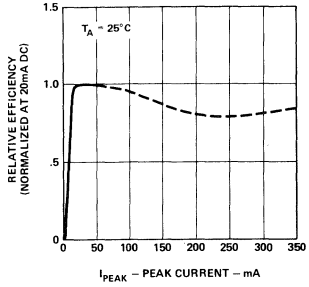


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

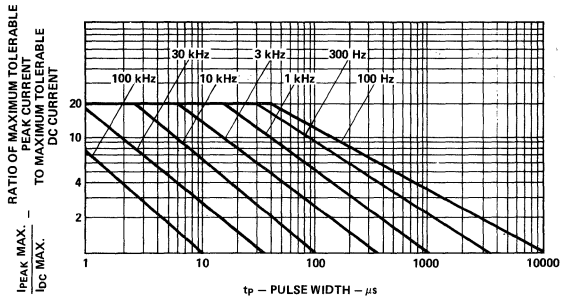


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

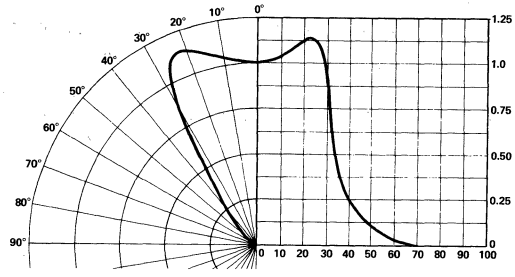


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

Family of High Efficiency Red 1N6092/HLMP-0354

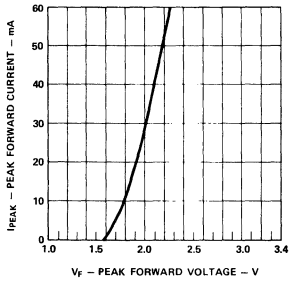


Figure 7. Forward Current vs. Forward Voltage.

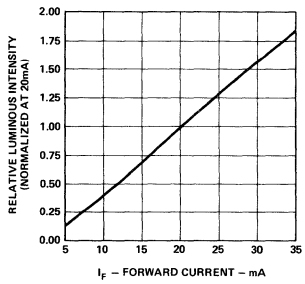


Figure 8. Relative Luminous Intensity vs. Forward Current.

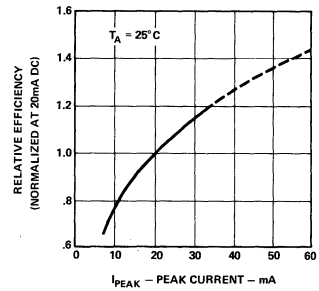


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

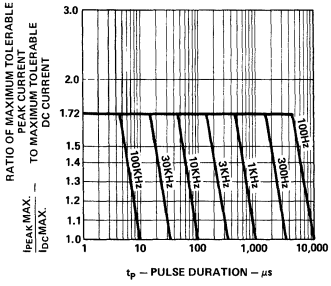


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

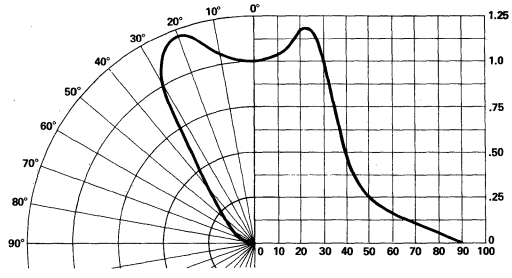


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Family of Yellow 1N6093/HLMP-0454

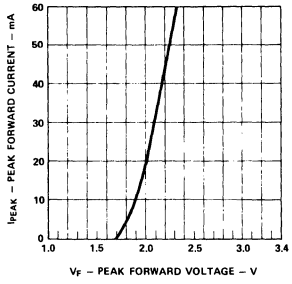


Figure 12. Forward Current vs. Forward Voltage.

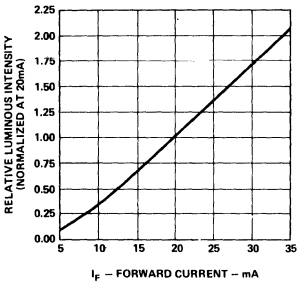


Figure 13. Relative Luminous Intensity vs. Forward Current.

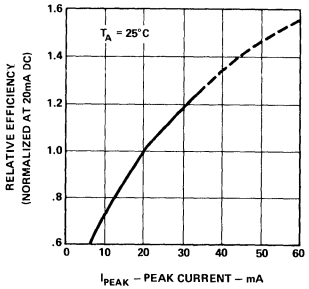


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

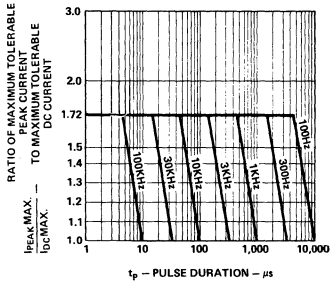


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

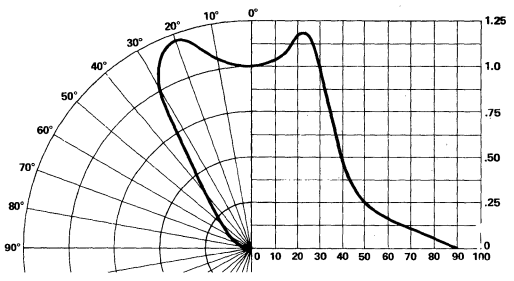


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

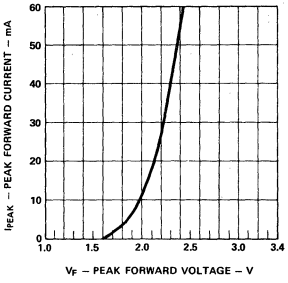


Figure 17. Forward Current vs. Forward Voltage.

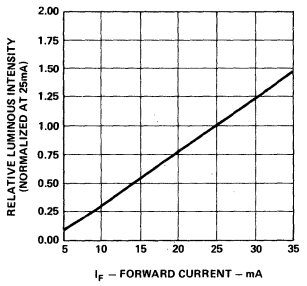


Figure 18. Relative Luminous Intensity vs. Forward Current.

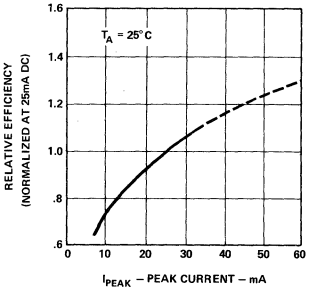


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

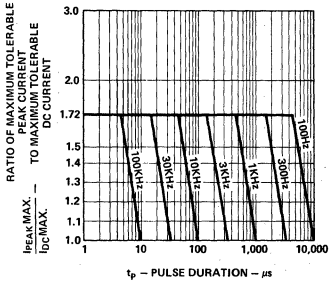


Figure 20. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

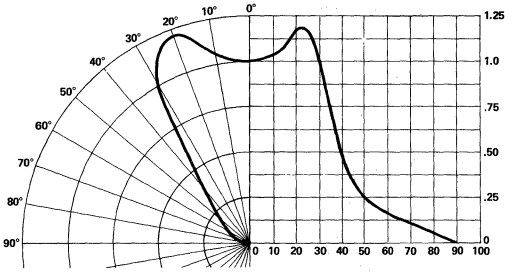


Figure 21. Relative Luminous Intensity vs. Angular Displacement.

JAN PART: Samples of each lot are subjected to Group A and B tests listed below. Every six months, samples from a single lot of each part type are subjected to Group C testing. All tests are to the conditions and limits specified by the appropriate MIL-S-19500 slash sheet.

JANTX PART: These devices undergo 100% screening tests as listed below to the conditions and limits specified by the MIL-S-19500 slash sheet. The JANTX lot has also been subjected to Group A, B, and C sample tests as for the JAN PART above.

Table I. Group A Inspection for TO-46 Lamps

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Limits Min.	Limits Max.	Unit
Subgroup 1			5				
Visual and mechanical inspection	2071						
Subgroup 2			5				
Luminous intensity		I_F = 20 mA dc;[1] θ = 0°		I_{V1}	0.5[2] 3.0[3]		mcd mcd
Luminous intensity		I_F = 20 mA dc;[1] θ = 30°		I_{V2}	0.3[2] 1.5[3]		mcd mcd
Reverse current	4016	DC method; V_R = 3 V dc		I_R		1.0	µA dc
Forward current	4011	DC method; I_F = 20 mA[1]		V_F		3.0	V dc
Subgroup 3			10				
High temperature:		T_A = 100°C					
Reverse current	4016	DC method; V_R = 3 V dc		I_R		1.0	µA dc
Forward voltage	4011	DC method; I_F = 20 mA[1]		V_F		3.0	V dc
Low Temperature:		T_A = -55°C					
Reverse current	4016	DC method; V_R = 3 V dc		I_R		1.0	µA dc
Forward voltage	4011	DC method; I_F = 20 mA[1]		V_F		3.0	V dc
Subgroup 4			5				
Capacitance	4001	V_R = 0; f = 1 MHz		C		100	pF

Notes:
1. I_F = 25 mA for 1N6094.
2. For 1N5765.
3. For 1N6092, 1N6093, and 1N6094.

Table II. Group B Inspection

Examination or Test	MIL-STD-750		LTPD	Symbol	Limits		Unit
	Method	Details			Min.	Max.	
Subgroup 1			15				
Solderability	2026						
Resistance to solvents	1022						
Subgroup 2			10				
Thermal shock (temperature cycle)	1051	Test condition A T (high) = 100°C; 25 cycles					
Hermetic seal	1071	Test condition H					
Fine leak							
Gross Leak		Test condition C or K, indicator fluid/device maintained at 100°C ±5°C					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°		I_{V1}	0.5[1] 3.0[2]		mcd mcd
Subgroup 3			5				
Steady-state-operation life	1027	I_F = 35 mA dc, 340 hours T_A = 25°C					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°		I_{V1}	0.45[1] 2.7[2]		mcd mcd
Subgroup 4							
Decap internal design verification	2075	Test 1 device/0 failure					
Subgroup 5							
(Not applicable)							
Subgroup 6			7				
High temperature life (nonoperating)	1032	T_A = 100°C, 340 hours					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°		I_{V1}	0.45[1] 2.7[2]		mcd mcd

Notes:
1. For 1N5765.
2. For 1N6092, 1N6093, and 1N6094.
3. 25 mA for 1N6094.

Table III. Group C Inspection

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Limits Min.	Limits Max.	Unit
Subgroup 1			15				
Physical dimensions	2066						
Subgroup 2			10				
Thermal shock (glass strain)	1056	Test condition A					
Terminal strength	2036	Test condition E					
Hermetic seal	1071						
Fine leak		Test condition H					
Gross leak		Test condition C or K, indicator fluid/device maintained at 100°C ± 5°C					
Moisture resistance	1021	Omit initial conditioning					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°	I_{V1}		0.5[1] 3.0[2]		mcd mcd
Subgroup 3			10				
Shock	2016	Nonoperating, 1500 g's, 0.5 ms, 5 blows in X1, Y1, Z1 orientation					
Vibration, variable frequency	2056	Nonoperating					
Constant acceleration	2006	20,000 g's X1, Y1, Z1 orientation					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°	I_{V1}		0.5[1] 3.0[2]		mcd mcd
Subgroup 4			15				
Salt atmosphere (corrosion)	1041						
Subgroup 5 (Not applicable)							
Subgroup 6							
Steady-state-operation life	1027	I_F = 35 mA dc, 1000 hours, T_A = 25°C					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°	I_{V1}		0.45[1] 2.7[2]		mcd mcd

Table III. Group C Inspection (continued)

Examination or Test	MIL-STD-750		LTPD	Symbol	Limits		Unit
	Method	Details			Min.	Max.	
Subgroup 7			10				
Peak forward pulse current (transient)		t_p = 1 µs, pps = 300, total test time = 5 s, I_{ptr} = 1.0 A(pk)					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°		I_{V1}	0.45[1] 2.7[2]		mcd mcd
Subgroup 8			10				
Peak forward pulse current (operating)		t_p = 0.5 ms, $P_{FM} \leq$ 120 mW, T_A = 25°C, I_P = 60 mA, 500 hours					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°		I_{V1}	0.45[1] 2.7[2]		mcd mcd

Notes:
1. For 1N5765.
2. For 1N6092, 1N6093, and 1N6094.
3. I_F = 25 mA for 1N6094.

Table IV. Group A Inspection for panel mount lamps

Examination or Test	MIL-STD-750		LTPD	Symbol	Limits		Unit
	Method	Details			Min.	Max.	
Subgroup 1			5				
External visual examination	2071						
Subgroup 2			5				
Luminous intensity		I_F = 20 mA dc,[3] θ = 0°		I_{V1}	0.5[1] 3.0[2]		mcd mcd
Forward voltage		DC method: I_F = 20 mA[3]		V_F		3.0	V dc
Reverse current		DC method: V_R = 3 V dc		I_R		1.0	µA dc
Subgroup 3			5				
Resistance to solvents	1022	Omit solution 2.1d					
Subgroup 4			5				
Physical dimensions	2066						

Notes:
1. For 1N5765.
2. For 1N6092, 1N6093, and 1N6094.
3. I_F = 25 mA for 1N6094.

HEWLETT PACKARD

JAN Qualified Ultra-Bright Hermetic Solid State Lamps*

Technical Data

1N6609
JAN1N6609
JANTX1N6609
1N6610
JAN1N6610
JANTX1N6610
1N6611
JAN1N6611
JANTX1N6611

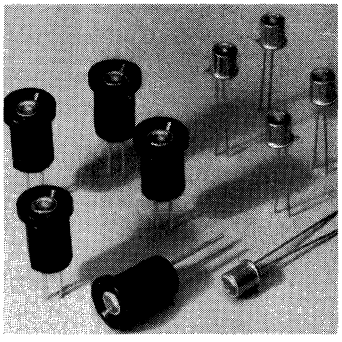
Features

- **Military Qualified**
- **Listed on MIL-S-19500 QPL**
- **Sunlight Viewable with Proper Contrast Enhancement Filter**
- **Hermetically Sealed**
- **Choice of Three Colors**
  High Efficiency Red
  Yellow
  High Performance Green
- **Low Power Operation**
- **IC Compatible**
- **Long Life/Reliable/Rugged**
- **Panel Mount Configuration**

Description

The 1N6609, 1N6610, and 1N6611 are hermetically sealed solid state lamps in a TO-18 package with a clear glass lens. These hermetic lamps provide improved brightness over conventional hermetic LED lamps, excellent on-off contrast, and high axial luminous intensity. These LED indicators are designed for use in applications requiring readability in bright sunlight. With a proper contrast enhancement filter, these LED indicators are readable in sunlight ambients, see Application Note 1015 *Contrast Enhancement Techniques for LED Displays.* The panel mount versions consist of an LED unit permanently mounted in an anodized aluminum sleeve.

The 1N6609 utilizes a high efficiency red GaAsP on GaP LED chip. The 1N6610 uses a yellow GaAsP on GaP LED chip. The 1N6611 uses a green GaP LED chip.



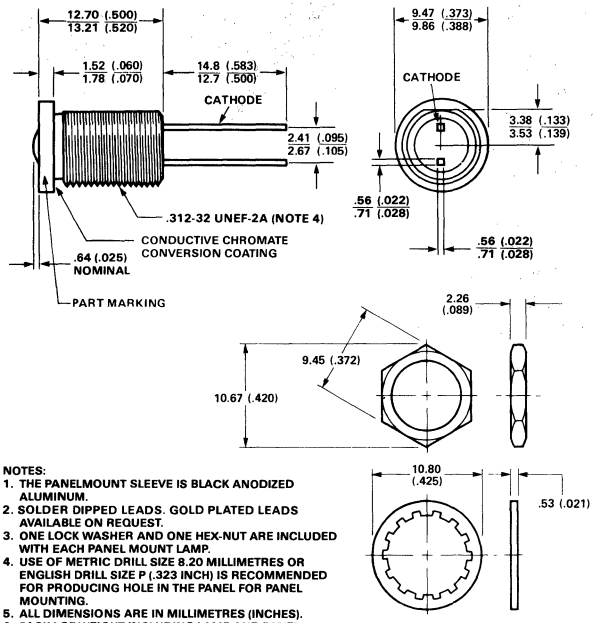
*Panel Mount versions of all of the above are available per the selection matrix on the next page.

COLOR – PART NUMBER – LAMP AND PANEL MOUNT MATRIX				
Description	**Standard Product**	**With JAN Qualification[1]**	**JAN Plus TX Testing[2]**	**Controlling MIL-S-19500 Document[4]**
TABLE A. Hermetic TO-18 Part Number System				
High Efficiency Red	1N6609	JAN1N6609	JANTX1N6609	/519
Yellow	1N6610	JAN1N6610	JANTX1N6610	/520
Green	1N6611	JAN1N6611	JANTX1N6611	/521
TABLE B. Panel Mountable Part Number System[3]				
High Efficiency Red	HLMP-0364	HLMP-0365 (JANM19500/51903)	HLMP-0366 (JANTXM19500/51904)	/519
Yellow	HLMP-0464	HLMP-0465 (JANM19500/52003)	HLMP-0466 (JANTXM19500/52004)	/520
Green	HLMP-0564	HLMP-0565 (JANM19500/52103)	HLMP-0566 (JANTXM19500/52104)	/521

Notes:
1. Parts are marked with JAN part number.
2. Parts are marked with JANTX/JTX part number.
3. Panel mountable packaging incorporates the Table A TO-18 part into a panel mount enclosure.
4. JAN and JANTX parts only.

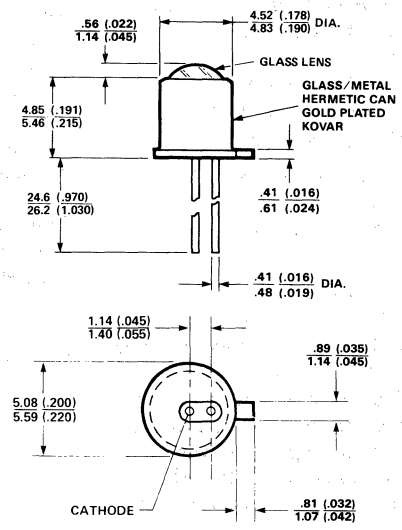
Package Dimensions

HLMP-0364, 0464, 0564



NOTES:
1. THE PANELMOUNT SLEEVE IS BLACK ANODIZED ALUMINUM.
2. SOLDER DIPPED LEADS. GOLD PLATED LEADS AVAILABLE ON REQUEST.
3. ONE LOCK WASHER AND ONE HEX-NUT ARE INCLUDED WITH EACH PANEL MOUNT LAMP.
4. USE OF METRIC DRILL SIZE 8.20 MILLIMETRES OR ENGLISH DRILL SIZE P (.323 INCH) IS RECOMMENDED FOR PRODUCING HOLE IN THE PANEL FOR PANEL MOUNTING.
5. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
6. PACKAGE WEIGHT INCLUDING LAMP AND PANEL MOUNT IS 1.2 - 1.8 GRAMS. NUT AND WASHER IS AN EXTRA .6 - 1.0 GRAM.

1N6609, 1N6610, 1N6611



OUTLINE TO-18

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. GOLD-PLATED KOVAR LEADS.
3. PACKAGE WEIGHT OF LAMP ALONE IS .25 - .40 GRAMS.

Absolute Maximum Ratings at T_A = 25°C

Parameter	High Efficiency Red 1N6609	Yellow 1N6610	Green 1N6611	Units
Power Dissipation (derate linearly from 50°C at 1.6 mW/°C)	120	120	120	mW
DC Forward Current	35[1]	35[1]	35[1]	mA
Peak Forward Current	60 See Fig. 5	60 See Fig. 10	60 See Fig. 15	mA
Operating and Storage Temperature Range	-65°C to +100°C			
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260°C for 7 seconds.			

Note:
1. Derate from 50°C at 0.5 mA/°C.

Electrical/Optical Characteristics at T_A = 25°C

Symbol	Description	1N6609			1N6610			1N6611			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{V1}	Axial Luminous Intensity	20	50		20	50		20	50		mcd	I_F = 20 mA Figs. 3, 8, 13 θ = 0°
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points[1]		18			18			18		deg.	Figures 6, 11, 16
λ_{PEAK}	Peak Wavelength	590	635	695	550	583	660	525	565	600	nm	Measurement at Peak
λ_d	Dominant Wavelength[2]		626			585			570		nm	
τ_S	Speed of Response		200			200			200		ns	
C	Capacitance		35	100		35	100		35	100	pF	V_F = 0; f = 1 MHz
$R\theta_{J\text{-}PIN}$	Thermal Resistance*[3]		425			425			425		°C/W	
$R\theta_{J\text{-}PIN}$	Thermal Resistance**[3]		550			550			550		°C/W	
V_F	Forward Voltage		2.0	3.0		2.0	3.0		2.1	3.0	V	I_F = 20 mA Figures 2, 7, 12,
I_R	Reverse Current			1.0			1.0			1.0	µA	V_R = 3 V
BV_R	Reverse Breakdown Voltage	5.0			5.0			5.0			V	I_R = 100 µA
η_v	Luminous Efficacy[4]		140			455			600		lm/W	

Notes:

1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Junction to Cathode Lead with 3.18 mm (0.125 inch) of leads exposed between base of flange and heat sink.
4. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

*Panel mount.
**T0-18.

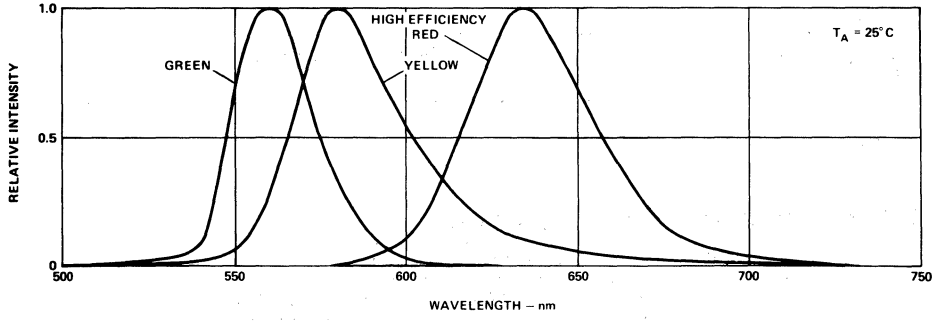


Figure 1. Relative Intensity vs. Wavelength.

Family of High Efficiency Red 1N6609/HLMP-0364

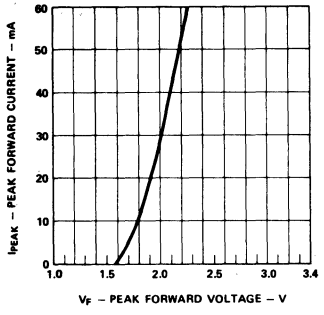


Figure 2. Forward Current vs. Forward Current.

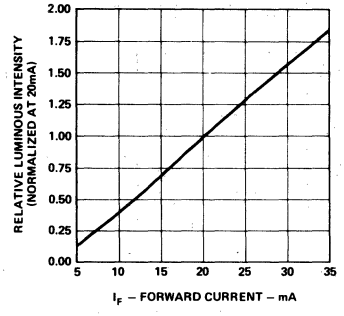


Figure 3. Relative Luminous Intensity vs. Forward Current.

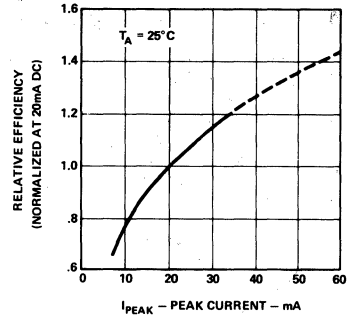


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

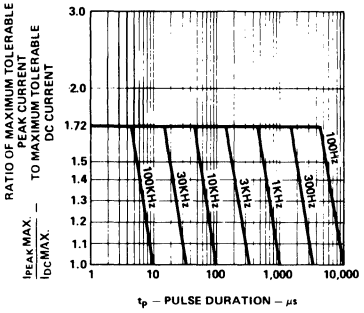


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

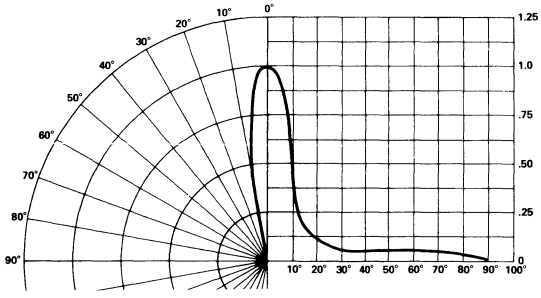


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

Family of Yellow 1N6610/HLMP-0464

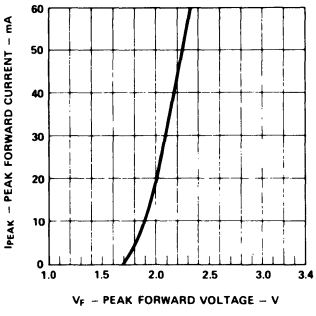


Figure 7. Forward Current vs. Forward Voltage.

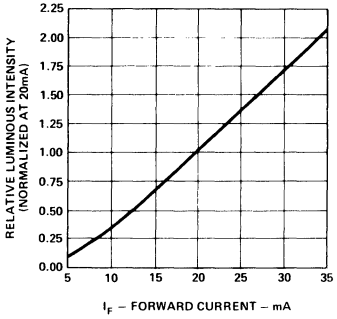


Figure 8. Relative Luminous Intensity vs. Forward Current.

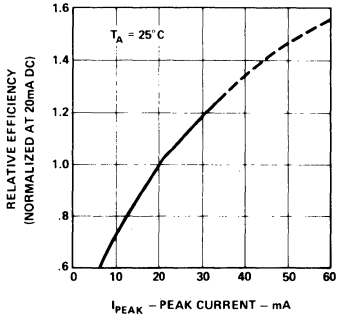


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

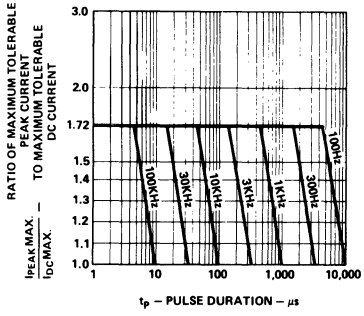


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

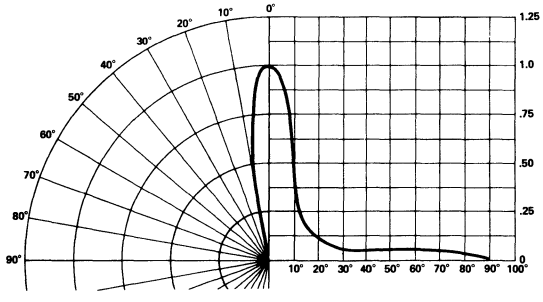


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Family of Green 1N6611/HLMP-0564

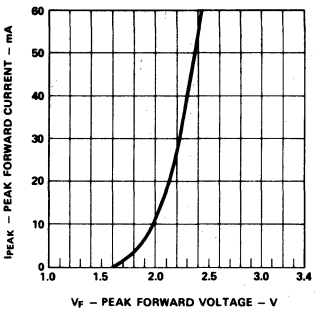


Figure 12. Forward Current vs. Forward Voltage.

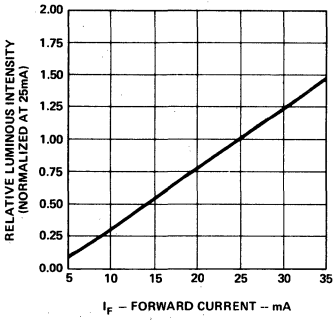


Figure 13. Relative Luminous Intensity vs. Forward Current.

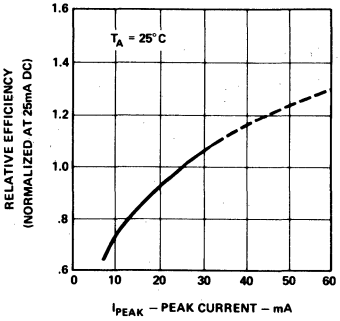


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

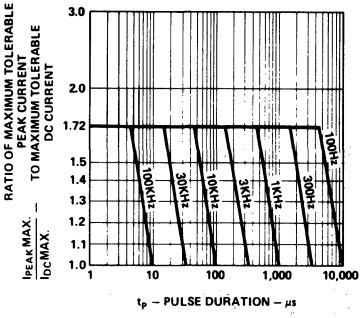


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

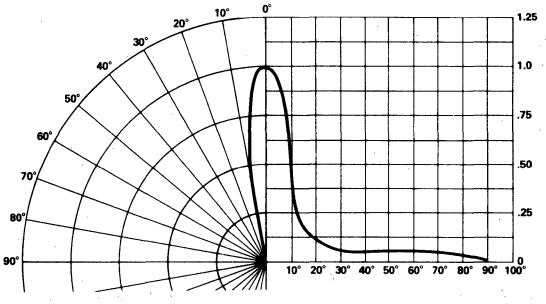


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

JAN PART: Samples of each lot are subjected to Group A and B tests listed below. Every six months, samples from a single lot of each part type are subjected to Group C testing. All tests are to the conditions and limits specified by the appropriate MIL-S-19500 slash sheet for the device under test.

JANTX PART: These devices undergo 100% screening tests as listed below to the conditions and limits specified by the MIL-S-19500 slash sheet. The JANTX lot has also been subjected to Group A, B, and C sample tests as for the JAN PART above.

Table I. Group A Inspection for TO-18 Lamps

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Sym.	Limits Min.	Limits Max.	Unit
Subgroup 1			5				
Visual and mechanical inspection	2071						
Subgroup 2			5				
Luminous intensity		I_F = 20 mA dc;[1] $\theta = 0°$		I_{V1}	20.0		mcd
Reverse current	4016	DC method; V_R = 3 V dc		I_R		1.0	µA dc
Forward current	4011	DC method; I_F = 20 mA		V_F		3.0	V dc
Subgroup 3			10				
High temperature:		T_A = 100°C					
Reverse current	4016	DC method; V_R = 3 V dc		I_R		1.0	µA dc
Forward voltage	4011	DC method; I_F = 20 mA[1]		V_F		3.0	V dc
Low Temperature:		T_A = -55°C					
Reverse current	4016	DC method; V_R = 3 V dc		I_R		1.0	µA dc
Forward voltage	4011	DC method; I_F = 20 mA[1]		V_F		3.0	V dc
Subgroup 4			5				
Capacitance	4001	V_R = 0; f = 1 MHz		C		100	pF
Subgroups 5, 6, and 7 Not applicable							

Note:
1. I_F = 25 mA for 1N6611.

Table II. Group B Inspection

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Limits Min.	Limits Max.	Unit
Subgroup 1			15				
Solderability	2026						
Resistance to solvents	1022						
Subgroup 2			10				
Thermal shock (temperature cycle)	1051	Test condition A, T (high) = 100°C; 25 cycles					
Hermetic seal	1071	Test condition H					
Fine leak							
Gross Leak		Test condition C or K, leak indicator fluid/ device maintained at 100°C ±5°C					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	20.0		mcd
Subgroup 3			5				
Steady-state-operation life	1027	I_F = 35 mA dc, 340 hours, T_A = 25°C					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	18.0		mcd
Subgroup 4							
Decap internal design verification	2075	Test 1 device/0 failure					
Subgroup 5							
(Not applicable)							
Subgroup 6			7				
High temperature life (nonoperating)	1032	T_A = 100°C, 340 hours					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	18.0		mcd

Note:
1. I_F = 25 mA for 1N6611.

Table III. Group C Inspection

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Limits Min.	Limits Max.	Unit
Subgroup 1			15				
Physical dimensions	2066						
Subgroup 2			10				
Thermal shock (glass strain)	1056	Test condition A					
Terminal strength	2036	Test condition E					
Hermetic seal	1071						
Fine leak		Test condition H					
Gross leak		Test condition C or K, indicator fluid/device maintained at 100°C ±5°C					
Moisture resistance	1021	Omit initial conditioning					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	20.0		mcd
Subgroup 3			10				
Shock	2016	Nonoperating, 1500 g's, 0.5 ms, 5 blows in X1, Y1, Z1 orientation.					
Vibration, variable frequency	2056	Nonoperating					
Constant acceleration	2006	20,000 g's; X1, Y1, Z1 orientation					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	20.0		mcd
Subgroup 4			15				
Salt atmosphere (corrosion)	1041						
Subgroup 5 (Not applicable)							
Subgroup 6							
Steady-state-operation life	1027	I_F = 35 mA dc, 1000 hours, T_A = 25°C					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	18.0		mcd

Table III. Group C Inspection (continued)

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Limits Min.	Limits Max.	Unit
Subgroup 7			10				
Peak forward pulse current (transient)		t_p = 1 µs, pps = 300, total test time = 5 s, I_{ptr} = 1.0 A(pk)					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	18.0		mcd
Subgroup 8			10				
Peak forward pulse current (operating)		t_p = 0.5 ms, $P_{FM} \leq$ 120 mW, T_A = 25°C, I_P = 60 mA, 500 hours					
Electrical test:							
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	18.0		mcd

Note:
1. I_F = 25 mA for 1N6611.

Table IV. Group A Inspection for Panel Mount Assemblies

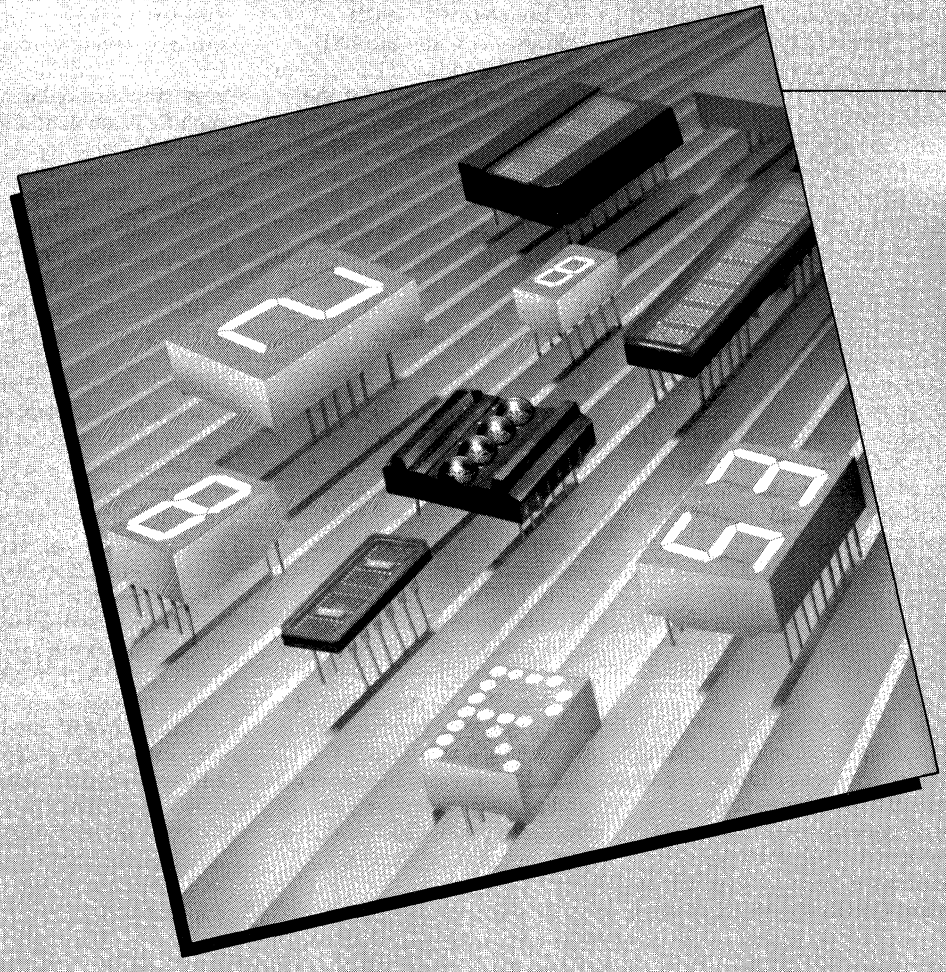
Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Limits Min.	Limits Max.	Unit
Subgroup 1			5				
External visual examination	2071						
Subgroup 2			5				
Luminous intensity		I_F = 20 mA dc,[1] θ = 0°		I_{V1}	20.0		mcd
Forward voltage		DC method: I_F = 20 mA[1]		V_F		3.0	V dc
Reverse current		DC method: V_R = 3 V dc		I_R		1.0	µA dc
Subgroup 3			5				
Resistance to solvents	1022	Omit solution 2.1d					
Subgroup 4			5				
Physical dimensions	2066						

Note:
1. I_F = 25 mA for HLMP-0564.

HEWLETT PACKARD

Solid State Displays

- Smart Alphanumeric Displays
- Alphanumeric Displays and Systems
- Seven Segment Displays
- Hexidecimal and Dot Matrix Displays
- Monolithic Numeric Displays
- Hermetic Displays (pg 4-158)



Solid State Displays

Hewlett-Packard's line of Solid State Displays answers all the needs of the designer. From smart alphanumeric displays to low cost numeric displays in sizes from 3 mm (0.15 in.) to 20 mm (0.8 in.) and colors of red, AlGaAs red, high efficiency red, yellow, and high performance green, the selection is complete.

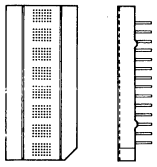
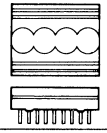
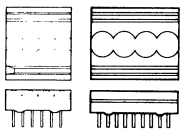
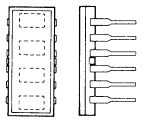
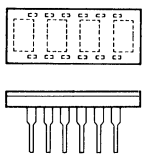
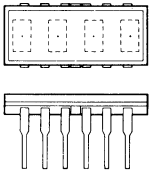
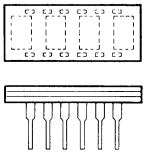
Hewlett-Packard's 5 x 7 dot matrix alphanumeric display line comes in three character sizes: 3.8 mm (0.15 in.), 5 mm (0.2 in.), and 6.9 mm (0.27 in.). In addition, there are now four colors available for each size: standard red, yellow, high efficiency red, and green. This wide selection of package sizes and colors makes these products ideal for a variety of applications in avionics, industrial control, and instrumentation.

The newest addition to HP's alphanumeric display line, the intelligent eight character, 5.0 mm (0.2 in.) alphanumeric display in the very flexible 5 x 7 dot matrix font. Product features include a low power on-board CMOS IC, ASCII decoder, the complete 128 ASCII character set, and the LED drivers. In addition, an on-board RAM offers the designer the ability to store up to 16 user-definable characters, such as foreign characters, special symbols and logos. These features make it ideal for avionics, medical, telecommunications, analytical equipment, computer products, office and industrial equipment applications.

Also part of HP's alphanumeric display line is the large (0.68 in. and 1.04 in.) 5 x 7 dot matrix alphanumeric display family. This family is offered in standard red, high efficiency red, AlGaAs red, and high performance green. These displays have excellent viewability; the 1.04 inch character font can be read at up to 18 meters (12 meters for the 0.68 inch display). Applications for these large 5 x 7 displays include industrial machinery and process controllers, weighing scales, computer tape drive systems, and transportation.

Hewlett-Packard's line of numeric seven segment displays is one of the broadest. From low cost, standard red displays to high light ambient displays producing 7.5 mcd/segment, HP's 0.3 in., 0.43 in., 0.56 in., and 0.8 in. characters can provide a solution to every display need. HP's product offering includes 0.56 in. dual digit displays and a line of small package, bright 0.3 in. displays – the 0.3 in. Microbright. HP's broad line of numeric seven segment displays is ideal for electronic instrumentation, industrial, weighing scales, point-of-sale terminals, and appliance applications. Included in HP's line of numeric seven segment displays is the Double Heterojunction AlGaAs red low current sunlight viewable display family. This family is offered in the 0.3 in. Mini, 0.43 in., 0.56 in., and 0.8 in. package sizes. These AlGaAs numeric displays are very bright at low drive currents – typical intensity of 650 mcd/segment at 1 mA/segment drive. These displays are ideal for battery operated and other low power applications.

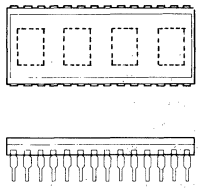
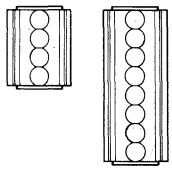
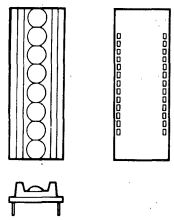
Alphanumeric LED Displays

Device	P/N	Description	Color	Application	Page No.
	**HDSP-2110** HDSP-2111 HDSP-2112 **HDSP-2113** **HDSP-2121** **HDSP-2122** **HDSP-2123**	5.0 mm (0.2 in.) 5 x 7 Eight Character Intelligent Display Operating Temperature Range: -40°C to +85°C HDSP-211X-ASCII HDSP-212X-Katakana	Orange Yellow High Efficiency Red Green Yellow High Efficiency Red Green	• Avionics • Medical • Telecommunications • Analytical Equipment • Computer Products • Office Equipment • Industrial Equipment	4-14
	**HDLR-2416** **HDLO-2416** **HDLA-2416** **HDLY-2416** **HDLG-2416**	5.0 mm (0.2 in.) 5 x 7 Four Character Intelligent Display Operating Temperature Range: -40°C to +85°C	Red High Efficiency Red Orange Yellow Green	• Portable Data Entry Devices • Industrial Instrumentation • Computer Peripherals • Telecommunications	4-30
	HPDL-1414 HPDL-2416	2.85 mm (0.112 in.) 4.1 mm (0.16 in.) 16 Segment Four Character Monolithic Intelligent Display Operating Temperature Range: -40°C to +85°C	Red Red	• Portable Data Entry Devices • Medical Equipment • Industrial Instrumentation • Computer Peripherals • Telecommunications	4-42
	**HCMS-2000** **HCMS-2001** **HCMS-2002** **HCMS-2003** **HCMS-2004**	3.8 mm (0.15 in.) 5 x 7 Four Character Display 12 pin Ceramic DIP 7.6 mm (0.30 in.) Operating Temperature Range: -40°C to +85°C	Red Yellow High Efficiency Red Green Orange	• Computer Terminals • Business Machines • Portable, Hand-held or mobile data entry, read-out, or communications	4-54
	**HCMS-2300** **HCMS-2301** **HCMS-2302** **HCMS-2303** **HCMS-2304**	5.0 mm (0.20 in.) 5 x 7 Four Character Display 12 pin Ceramic DIP 6.35 mm (0.250 in.) Operating Temperature Range: -40°C to +85°C	Red Yellow High Efficiency Red Green Orange	• Avionics • Ground Support, Cockpit, Shipboard Systems • Medical Equipment • Industrial and Process control • Computer Peripherals and Terminals	
	HDSP-2000 HDSP-2001 HDSP-2002 HDSP-2003	3.8 mm (0.15 in.) 5 x 7 Four Character Alphanumeric 12 Pin Ceramic 7.62 mm (0.3 in.) DIP with untinted glass lens Operating Temperature Range: -20°C to +85°C	Red Yellow High Efficiency Red High Performance Green	• Computer Terminals • Business Machines • Portable, Hand-held or mobile data entry, read-out or communications For further information see Application Note 1016.	*
	HDSP-2300 HDSP-2301 HDSP-2302 HDSP-2303	5.0 mm (0.20 in.) 5 x 7 Character Alphanumeric 12 Pin Ceramic 6.35 mm (0.25 in.) DIP with untinted glass lens Operating Temperature Range: -20°C to +85°C	Red Yellow High Efficiency Red High Performance Green	• Avionics • Ground Support, Cockpit, Shipboard Systems • Medical Equipment • Industrial and Process control • Computer Peripherals and Terminals For further information see Application Note 1016.	

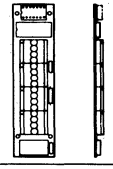
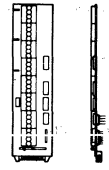
Bold Type – New Product

*Contact your local Sales Representative for information regarding this product. (See Section 9.)

Alphanumeric LED Displays (Continued)

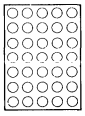
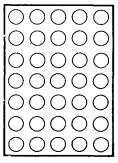
Device	P/N	Description	Color	Application	Page No.
	HDSP-2490 HDSP-2491 HDSP-2492 HDSP-2493	6.9 mm (0.27 in.) 5 x 7 Four Character Alphanumeric 28 Pin Ceramic 15.24 mm (0.6 in.) DIP with untinted glass lens Operating Temperature Range: -20°C to +85°C	Red Yellow High Efficiency Red High Performance Green	• High Brightness Ambient Systems • Industrial and Process Control • Computer Peripherals • Ground Support Systems For further information see Application Note 1016.	*
	HDSP-6504	3.8 mm (0.15 in.) Sixteen Segment Four Character Alphanumeric 22 Pin 15.2 mm (0.6 in.) DIP	Red	• Computer Terminals • Hand Held Instruments • In-Plant Control Equipment • Diagnostic Equipment	*
	HDSP-6508	3.8 mm (0.15 in.) Sixteen Segment Eight Character Alphanumeric 26 Pin 15.2 mm (0.6 in.) DIP			
	HDSP-6300	3.56 mm (0.14 in.) Sixteen Segment Eight Character Alphanumeric 26 Pin 15.2 mm (0.6 in.) DIP		• Computer Peripherals and Terminals • Computer Base Emergency Mobile Units • Automotive Instrument Panels • Desk Top Calculators • Hand-Held Instruments For further information ask for Application Note 931.	

Alphanumeric Display Systems

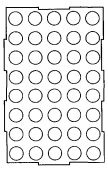
Device	P/N	Description	Color	Application	Page No.
	HDSP-6621	Single Line 16 Character Display Board Utilizing the HPDL-1414	114.30 mm (4.50 in.) L x 30.48 mm (1.20 in.) H x 8.12 mm (0.32 in.) D	• Computer Peripherals • Telecommunications • Industrial Equipment • Instruments	*
	HDSP-6624	Single Line 32 Character Display Board Utilizing the HPDL-2416	223.52 mm (8.80 in.) L x 58.42 mm (2.30 in.) H x 15.92 mm (0.62 in.) D		

*Contact your local Sales Representative for information regarding this product. (See Section 9.)

Large Alphanumeric 5 X 7 Displays

Device	P/N	Description	Color	Package	Typical I_v	Page No.
	HDSP-4701 HDSP-4703 **HDSP-L101** **HDSP-L103** **HDSP-L201** **HDSP-L203** **HDSP-5401** **HDSP-5403**	Common Row Anode Common Row Cathode Common Row Anode Common Row Cathode Common Row Anode Common Row Cathode Common Row Anode Common Row Cathode	Red Red AlGaAs Red AlGaAs Red High Efficiency Red High Efficiency Red Green Green	17.3 mm (0.68 in.) Dual-in-Line 0.70 in. H x 0.50 in. W x 0.26 in. D	770 µcd/dot 100 mA peak 1/5 Duty Factor 1650 µcd/dot 10 mA peak 1/5 Duty Factor 2800 µcd/dot 50 mA peak 1/5 Duty Factor 2700 µcd/dot 50 mA peak 1/5 Duty Factor	4-62
	HDSP-4401 HDSP-4403 **HDSP-M101** **HDSP-M103** HDSP-4501 HDSP-4503 **HDSP-5101** **HDSP-5103**	Common Row Anode Common Row Cathode Common Row Anode Common Row Cathode Common Row Anode Common Row Cathode Common Row Anode Common Row Cathode	Red Red AlGaAs Red AlGaAs Red High Efficiency Red High Efficiency Red Green Green	26.5 mm (1.04 in.) Dual-in-Line 1.10 in. H x 0.79 in. W x 0.25 in. D	800 µcd/dot 100 mA peak 1/5 Duty Factor 1850 µcd/dot 10 mA peak 1/5 Duty Factor 3500 µcd/dot 50 mA peak 1/5 Duty Factor 3100 µcd/dot 50 mA peak 1/5 Duty Factor	

Large Alphanumeric 5 X 8 Displays

Device	P/N	Description	Color	Package	Typical I_v	Page No.
	**HDSP-P101** **HDSP-P103** **HDSP-P151** **HDSP-P153**	Common Row Anode Common Row Cathode Common Row Anode Common Row Cathode	AlGaAs Red	58.4 mm (2.3 in.) 2.4 in. H x 1.5 in. W x 0.35 in. D	12000 µcd/dot 50 mA Peak 1/5 Duty Factor 15000 µcd/dot 50 mA Peak 1/5 Duty Factor	4-134

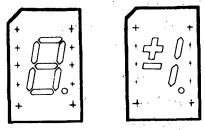
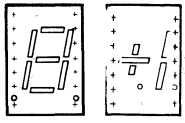
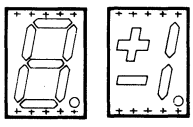
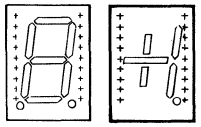
Alphanumeric Driver ICs

Device	P/N	Description	Page No.
	Smart Sets	1 Driver IC and 4 or 8 HDSP-L203 or HDSP-4501 Displays	*

Bold Type – New Product

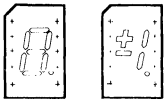
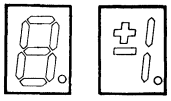
*Contact your local Sales Representative for information regarding this product. (See Section 9.)

Low Current Seven Segment Displays

Device	P/N	Description	Color	Typical I_v	Page No.
 7.62 mm (0.30 in.) Mini Dual-in-Line 0.5" H x 0.3" W x 0.24" D	HDSP-A101 HDSP-A103 HDSP-A107 HDSP-A108	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	AlGaAs Red	600 µcd @ 1 mA	4-72
	HDSP-7511 HDSP-7513 HDSP-7517 HDSP-7518	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	High Efficiency Red	270 µcd @ 2 mA	
	HDSP-A801 **HDSP-A803** **HDSP-A807** **HDSP-A808**	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	Yellow	420 µcd @ 4 mA	
	HDSP-A901 **HDSP-A903** **HDSP-A907** **HDSP-A908**	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	Green	475 µcd @ 4 mA	
10.16 mm (0.40 in.) Dual-in-Line 0.51" H x 0.39" W x 0.25" D	**HDSP-F101** **HDSP-F103** **HDSP-F107** **HDSP-F108**	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	AlGaAs Red	650 µcd @ 1 mA	
 10.92 mm (0.43 in.) Dual-in-Line 0.75" H x 0.5" W x 0.25" D	HDSP-E100 HDSP-E101 HDSP-E103 HDSP-E108	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow	AlGaAs Red	650 µcd @ 1 mA	
	HDSP-3350 HDSP-3351 HDSP-3353 HDSP-3356	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	High Efficiency Red	300 µcd @ 2 mA	
 14.2 mm (0.56 in.) Dual-in-Line (Single Digit) 0.67" H x 0.49" W x 0.31" D	HDSP-H101 HDSP-H103 HDSP-H107 HDSP-H108 **HDSP-K121** **HDSP-K123**	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow Two Digit Common Anode Right Hand Decimal Two Digit Common Cathode Right Hand Decimal	AlGaAs Red	700 µcd @ 1 mA	
	HDSP-5551 HDSP-5553 HDSP-5557 HDSP-5558	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	High Efficiency Red	370 µcd @ 2 mA	
 20 mm (0.8 in.) Dual-in-Line 1.09" H x 0.78" W x 0.33" D	HDSP-N100 HDSP-N101 HDSP-N103 HDSP-N105 HDSP-N106	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Cathode Left Hand Decimal Universal ±1. Overflow	AlGaAs Red	590 µcd @ 1 mA	

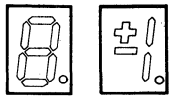
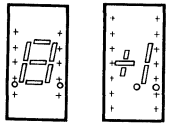
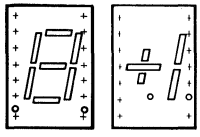
Bold Type – New Product

Seven Segment Displays

Device	P/N	Description	Color	Typical I_v	Page No.
	HDSP-7301 HDSP-7302 HDSP-7303 HDSP-7304 HDSP-7307 HDSP-7308	Common Anode Right Hand Decimal Common Anode Right Hand Decimal, Colon Common Cathode Right Hand Decimal Common Cathode Right Hand Decimal, Colon Common Anode ±1. Overflow Common Cathode ±1. Overflow	Red	1100 µcd @ 20 mA	4-88
	HDSP-7311 HDSP-7313 HDSP-7317 HDSP-7318	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	Red	1355 µcd @ 20 mA	
	HDSP-A151 **HDSP-A153** **HDSP-A157** **HDSP-A158**	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	AlGaAs Red	14 mcd @ 20 mA	
	HDSP-7501 HDSP-7502 HDSP-7503 HDSP-7504 HDSP-7507 HDSP-7508	Common Anode Right Hand Decimal Common Anode Left Hand Decimal, Colon Common Cathode Right Hand Decimal Common Cathode Left Hand Decimal, Colon Common Anode ±1. Overflow Common Cathode ±1. Overflow	High Efficiency Red	980 µcd @ 5 mA	
	HDSP-7401 HDSP-7402 HDSP-7403 HDSP-7404 HDSP-7407 HDSP-7408	Common Anode Right Hand Decimal Common Anode Left Hand Decimal, Colon Common Cathode Right Hand Decimal Common Cathode Left Hand Decimal, Colon Common Anode ±1. Overflow Common Cathode ±1. Overflow	Yellow	480 µcd @ 5 mA	
7.62 mm (0.3 in.) Microbright Dual-in-Line 0.5" H x 0.3" W x 0.24" D	HDSP-7801 HDSP-7802 HDSP-7803 HDSP-7804 HDSP-7807 HDSP-7808	Common Anode Right Hand Decimal Common Anode Left Hand Decimal, Colon Common Cathode Right Hand Decimal Common Cathode Left Hand Decimal, Colon Common Anode ±1. Overflow Common Cathode ±1. Overflow	Green	1480 µcd @ 10 mA	
	**HDSP-F001** **HDSP-F003** **HDSP-F007** **HDSP-F008**	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	Red	1200 µcd @ 20 mA	4-97
	HDSP-F151 **HDSP-F153** **HDSP-F157** **HDSP-F158**	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	AlGaAs Red	15.0 mcd @ 20 mA	
	HDSP-F201 **HDSP-F203** **HDSP-F207** **HDSP-F208**	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	High Efficiency Red	1200 µcd @ 5 mA	
10.16 mm (0.4 in.) Dual-In-Line (Single Digit) 0.51" H x 0.39" W x 0.25" D	**HDSP-F401** **HDSP-F403** **HDSP-F407** **HDSP-F408**	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	Orange	1200 µcd @ 5 mA	

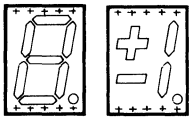
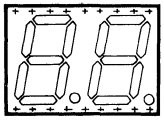
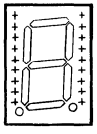
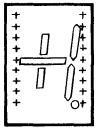
Bold Type – New Product

Seven Segment Displays (Continued)

Device	P/N	Description	Color	Typical I_V	Page No.
	**HDSP-F301** **HDSP-F303** **HDSP-F307** **HDSP-F308**	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	Yellow	800 µcd @ 5 mA	4-97
	HDSP-F501 **HDSP-F503** **HDSP-F507** **HDSP-F508**	Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Anode ±1. Overflow Common Cathode ±1. Overflow	Green	2100 µcd @ 10 mA	
 7.62 mm (0.3 in.) Dual-in-Line 0.75" H x 0.4" W x 0.18" D	5082-7730 5082-7731 5082-7740 5082-7736	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	Red	770 µcd @ 20 mA	4-105
	5082-7610 5082-7611 5082-7613 5082-7616	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	High Efficiency Red	800 µcd @ 5 mA	
	5082-7620 5082-7621 5082-7623 5082-7626	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	Yellow	620 µcd @ 5 mA	
	HDSP-3600 HDSP-3601 HDSP-3603 HDSP-3606	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	Green	1800 µcd @ 10 mA	
 10.92 mm (0.43 in.) Dual-in-Line 0.75" H x 0.5" W x 0.25" D	5082-7750 5082-7751 5082-7760 5082-7756	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	Red	1100 µcd @ 20 mA	
	HDSP-E150 **HDSP-E151** **HDSP-E153** **HDSP-E156**	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	AlGaAs Red	15.0 mcd @ 20 mA	
	5082-7650 5082-7651 5082-7653 5082-7656	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	High Efficiency Red	1115 µcd @ 5 mA	
	5082-7660 5082-7661 5082-7663 5082-7666	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	Yellow	835 µcd @ 5 mA	
	HDSP-4600 HDSP-4601 HDSP-4603 HDSP-4606	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Universal ±1. Overflow Right Hand Decimal	Green	1750 µcd @ 10 mA	

Bold Type – New Product

Seven Segment Displays (Continued)

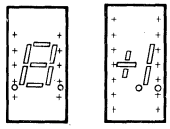
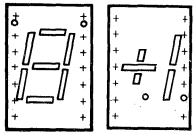
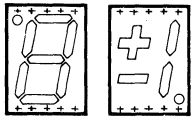
Device	P/N	Description	Color	Typical I_v	Page No.
 14.2 mm (0.56 in.) Dual-in-Line (Single Digit) 0.67" H x 0.49" W x 0.31" D	HDSP-5301	Common Anode Right Hand Decimal	Red	1300 µcd @ 20 mA	4-115
	HDSP-5303	Common Cathode Right Hand Decimal			
	HDSP-5307	Common Anode ±1. Overflow			
	HDSP-5308	Common Cathode ±1. Overflow			
	HDSP-5321	Two Digit Common Anode Right Hand Decimal			
	HDSP-5323	Two Digit Common Cathode Right Hand Decimal			
	HDSP-H151	Common Anode Right Hand Decimal	AlGaAs Red	16.0 mcd @ 20 mA	
	HDSP-H153	Common Cathode Right Hand Decimal			
	HDSP-H157	Common Anode ±1. Overflow			
	HDSP-H158	Common Cathode ±1. Overflow			
	HDSP-5501	Common Anode Right Hand Decimal	High Efficiency Red	2800 µcd @ 10 mA	
	HDSP-5503	Common Cathode Right Hand Decimal			
	HDSP-5507	Common Anode ±1. Overflow			
	HDSP-5508	Common Cathode ±1. Overflow			
	HDSP-5521	Two Digit Common Anode Right Hand Decimal			
	HDSP-5523	Two Digit Common Cathode Right Hand Decimal			
	HDSP-5701	Common Anode Right Hand Decimal	Yellow	1800 µcd @ 10 mA	
	HDSP-5703	Common Cathode Right Hand Decimal			
	HDSP-5707	Common Anode ±1. Overflow			
	HDSP-5708	Common Cathode ±1. Overflow			
	HDSP-5721	Two Digit Common Anode Right Hand Decimal			
	HDSP-5723	Two Digit Common Cathode Right Hand Decimal			
14.2 mm (0.56 in.) Dual-in-Line (Dual Digit) 0.67" H x 1.0" W x 0.31" D	HDSP-5601	Common Anode Right Hand Decimal	Green	2500 µcd @ 10 mA	
	HDSP-5603	Common Cathode Right Hand Decimal			
	HDSP-5607	Common Anode ±1. Overflow			
	HDSP-5608	Common Cathode ±1. Overflow			
	HDSP-5621	Two Digit Common Anode Right Hand Decimal			
	HDSP-5623	Two Digit Common Cathode Right Hand Decimal			
	HDSP-3400	Common Anode Left Hand Decimal	Red	1200 µcd @ 20 mA	4-125
	HDSP-3401	Common Anode Right Hand Decimal			
	HDSP-3403	Common Cathode Right Hand Decimal			
	HDSP-3405	Common Cathode Left Hand Decimal			
	HDSP-3406	Universal ±1. Overflow Right Hand Decimal			
	**HDSP-N150**	Common Anode Left Hand Decimal	AlGaAs Red	14.0 mcd @ 20 mA	
	HDSP-N151	Common Anode Right Hand Decimal			
	HDSP-N153	Common Cathode Right Hand Decimal			
	HDSP-N155	Common Cathode Left Hand Decimal			
	HDSP-N156	Universal ±1. Overflow Right Hand Decimal			
20 mm (0.8 in.) Dual-in-Line 1.09" H x 0.78" W x 0.33" D	HDSP-3900	Common Anode Left Hand Decimal	High Efficiency Red	7000 µcd @ 100 mA peak 1/5 Duty Factor	
	HDSP-3901	Common Anode Right Hand Decimal			
	HDSP-3903	Common Cathode Right Hand Decimal			
	HDSP-3905	Common Cathode Left Hand Decimal			
	HDSP-3906	Universal ±1. Overflow Right Hand Decimal			

Bold Type – New Product

Seven Segment Displays (Continued)

Device	P/N	Description	Color	Typical I_v	Page No.
(See previous page)	HDSP-4200 HDSP-4201 HDSP-4203 HDSP-4205 HDSP-4206	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Cathode Left Hand Decimal Universal ±1. Overflow Right Hand Decimal	Yellow	7000 µcd @ 100 mA peak 1/5 Duty Factor	4-125
	HDSP-8600 HDSP-8601 HDSP-8603 HDSP-8605 HDSP-8606	Common Anode Left Hand Decimal Common Anode Right Hand Decimal Common Cathode Right Hand Decimal Common Cathode Left Hand Decimal Universal ±1. Overflow Right Hand Decimal	Green	1500 µcd @ 10 mA	

High Ambient Light, Seven Segment Displays

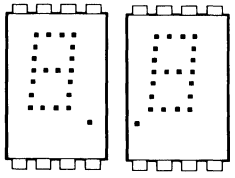
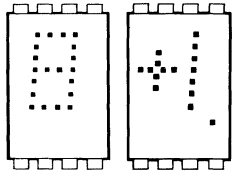
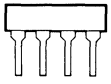
Device	P/N	Description	Typical I_v @ 100 mA Peak 1/5 Duty Factor	Publ. No.
 7.62 mm (0.3 in.) Dual-in-Line 0.75" H x 0.4" W x 0.18" D	HDSP-3530 HDSP-3531 HDSP-3533 HDSP-3536	High Efficiency Red, Common Anode, LHDP High Efficiency Red, Common Anode, RHDP High Efficiency Red, Common Cathode, RHDP High Efficiency Red, Universal Polarity Overflow Indicator, RHDP	7100 µcd/seg	*
	HDSP-4030 HDSP-4031 HDSP-4033 HDSP-4036	Yellow, Common Anode, LHDP Yellow, Common Anode, RHDP Yellow, Common Cathode, RHDP Yellow, Universal Polarity Overflow Indicator, RHDP	4500 µcd/seg	
 10.92 mm (0.43 in.) Dual-in-Line 0.75" H x 0.5" W x 0.25" D	HDSP-3730 HDSP-3731 HDSP-3733 HDSP-3736	High Efficiency Red, Common Anode, LHDP High Efficiency Red, Common Anode, RHDP High Efficiency Red, Common Cathode, RHDP High Efficiency Red, Universal Polarity Overflow Indicator, RHDP	10900 µcd/seg	
	HDSP-4130 HDSP-4131 HDSP-4133 HDSP-4136	Yellow, Common Anode, LHDP Yellow, Common Anode, RHDP Yellow, Common Cathode, RHDP Yellow, Universal Polarity Overflow Indicator, RHDP	5000 µcd/seg	
 14.2 mm (0.56 in.) Dual-in-Line 0.67" H x 0.49" W x 0.31" D	HDSP-5531 HDSP-5533 HDSP-5537 HDSP-5538	High Efficiency Red, Common Anode, RHDP High Efficiency Red, Common Cathode, RHDP High Efficiency Red ±1. Common Anode High Efficiency Red ±1. Common Cathode	6000 µcd/seg	
	HDSP-5731 HDSP-5733 HDSP-5737 HDSP-5738	Yellow, Common Anode, RHDP Yellow, Common Cathode, RHDP Yellow, ±1. Common Anode Yellow, ±1. Common Cathode	5500 µcd/seg	

*Contact your local Sales Representative for information regarding this product. (See Section 9.)

Solid State Display Intensity and Color Selections

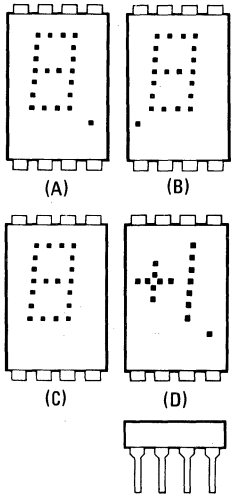
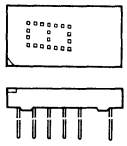
Option	Description	Publication Number
Option S01 Option S02 Option S20	Intensity and Color Selected Displays	*

Hexadecimal and Dot Matrix Displays

Device	P/N	Description	Package	Application	Page No.
 (A) (B)  (C) (D)  7.4 mm (0.29 in.) 4 x 7 Single Digit	5082-7300 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	8 Pin Epoxy 15.2 mm (0.6 in.) DIP	General Purpose Market • Test Equipment • Business Machines • Computer Peripherals • Avionics	4-139
	5082-7302 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	5082-7340 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	5082-7304 (D)	Over Range ±1			
	5082-7356 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	8 Pin Glass Ceramic 15.2 mm (0.6 in.) DIP	• Medical Equipment • Industrial and Process Control Equipment • Computers • Where Ceramic Package ICs are required • High Reliability Applications	4-143
	5082-7357 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	5082-7359 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	5082-7358 (D)	Over Range ±1			

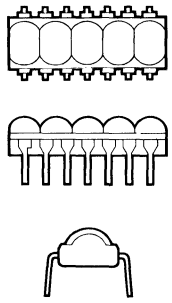
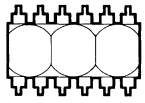
*Contact your local Sales Representative for information regarding this product. (See Section 9.)

Hexadecimal and Dot Matrix Displays (Continued)

Device	P/N	Description	Package	Application	Page No.
 7.4 mm (0.29 in.) 4 x 7 Single Digit Package: 8 Pin Glass Ceramic 15.2 mm (0.6 in.) DIP	HDSP-0760 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	High Efficiency Red Low Power	• Military Equipment • Ground Support Equipment • Avionics • High Reliability Applications	4-148
	HDSP-0761 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	HDSP-0762 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	HDSP-0763 (D)	Over Range ±1			
	HDSP-0770 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	High Efficiency Red High Brightness	• High Brightness Ambient Systems • Cockpit, Shipboard Equipment • High Reliability Applications	
	HDSP-0771 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	HDSP-0772 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	HDSP-0773 (D)	Over Range ±1			
	HDSP-0860 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	Yellow	• Business Machines • Fire Control Systems • Military Equipment • High Reliability Applications	
	HDSP-0861 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	HDSP-0862 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	HDSP-0863 (D)	Over Range ±1			
	HDSP-0960 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	High Performance Green	• Business Machines • Fire Control Systems • Military Equipment • High Reliability Applications	
	HDSP-0961 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	HDSP-0962 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	HDSP-0963 (D)	Over Range ±1			
	**HTIL-311A**	Hexadecimal Left Hand or Right Hand Decimal Built-in Decoder/Driver/ Memory/Blanking	Red	• Instrumentation • Computers and Peripherals • Status Indicators • Telecommunications	4-154

Bold Type – New Product

Monolithic Numeric Displays

Device	P/N	Description	Package	Application	Publ. No.
	5082-7404	2.79 mm (0.11 in.) Red, 4 Digits, Centered D.P.	12 Pin Epoxy, 7.62 mm (0.3 in.) DIP	Small Display Market • Portable/Battery Power Instruments • Portable Calculators • Digital Counters • Digital Thermometers • Digital Micrometers • Stopwatches • Cameras • Copiers • Digital Telephone Peripherals • Data Entry Terminals • Taxi Meters For further information ask for Application Note 937.	*
	5082-7405	2.79 mm (0.11 in.) Red, 5 Digits, Centered D.P.	14 Pin Epoxy, 7.62 mm (0.3 in.) DIP		
	5082-7414	2.79 mm (0.11 in.) Red, 4 Digits, RHDP	12 Pin Epoxy, 7.62 mm (0.3 in.) DIP		
	5082-7415	2.79 mm (0.11 in.) Red, 5 Digits, RHDP	14 Pin Epoxy, 7.62 mm (0.3 in.) DIP		
	5082-7432	2.79 mm (0.11 in.) Red, 2 Digits, Right, RHDP	12 Pin Epoxy, 7.62 mm (0.3 in.) DIP		
	5082-7433	2.79 mm (0.11 in.) Red, 3 Digits, RHDP			

Hermetic Displays (see page 4-160)

*Contact your local Sales Representative for information regarding this product. (See Section 9.)

HEWLETT PACKARD

Eight Character 5.0 mm (0.2 inch) Smart 5 X 7 Alphanumeric Displays

Technical Data

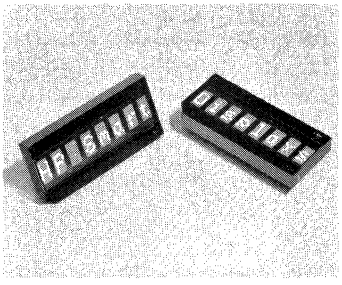
HDSP-2110
HDSP-2111
HDSP-2112
HDSP 2113
HDSP-2121
HDSP-2122
HDSP-2123

Features

- **Smart Alphanumeric Display**
  On-Board CMOS IC
  Built-In RAM
  ASCII or Katakana Decoder
  LED Drive Circuitry
- **128 ASCII Character Set or 128 Katakana Character Set**
- **16 User Definable Characters**
- **Programmable Features**
  Individual Flashing Character
  Full Display Blinking
  Multi-Level Dimming and Blanking
  Self Test
  Clear Function
- **Read/Write Capability**
- **Full TTL Compatibility**
- **Single 5 Volt Supply**
- **Excellent ESD Protection**
- **Wave Solderable**
- **End Stackable**

Description

These are eight-digit, 5 x 7 dot matrix, alphanumeric displays. The 5.0 mm (0.2 inch) high characters are packaged in a standard 15.24 mm (0.6 inch) 28 pin DIP. The on-board CMOS IC has the ability to decode 128 ASCII (Katakana) characters, which are permanently stored in ROM. In addition, 16 programmable symbols may be stored in on-board RAM. Seven brightness levels provide versatility in adjusting the display intensity and power consumption. The HDSP-211X/-212X is designed for standard microprocessor interface techniques. The display and special features are accessed through a bidirectional eight-bit data bus. These features make the HDSP-211X/-212X ideally suited for applications where a low cost, low power alphanumeric display is required.



Applications

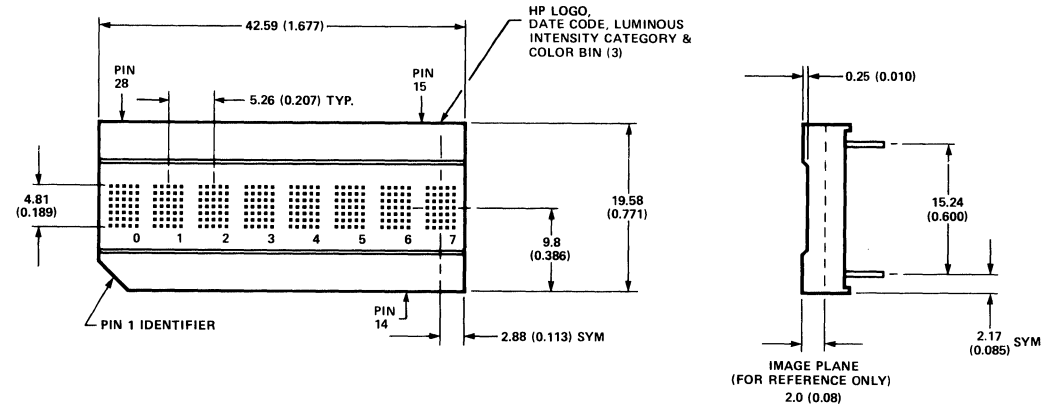
- **Avionics**
- **Computer Peripherals**
- **Industrial Instrumentation**
- **Medical Equipment**
- **Portable Data Entry Devices**
- **Telecommunications**
- **Test Equipment**

Devices

High Efficiency Red	Orange	Yellow	Green	Description
HDSP-2112	HDSP-2110	HDSP-2111	HDSP-2113	ASCII
HDSP-2122	–	HDSP-2121	HDSP-2123	Katakana*

*Katakana is a simplified version of the Japanese alphabet.

Package Dimensions



NOTES:
1. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS 0.254 mm (0.010 IN).
2. DIMENSIONS IN mm (INCHES).
3. FOR YELLOW AND GREEN ONLY.

Pin Function Assignment Table

Pin No.	Function	Pin No.	Function
1	$\overline{RST}$	15	GND (SUPPLY)
2	$\overline{FL}$	16	GND (LOGIC)
3	A_0	17	$\overline{CE}$
4	A_1	18	$\overline{RD}$
5	A_2	19	D_0
6	A_3	20	D_1
7	SUBSTR. BIAS	21	NO PIN
8	SUBSTR. BIAS	22	NO PIN
9	SUBSTR. BIAS	23	D_2
10	A_4	24	D_3
11	CLS	25	D_4
12	CLK	26	D_5
13	$\overline{WR}$	27	D_6
14	V_{DD}	28	D_7

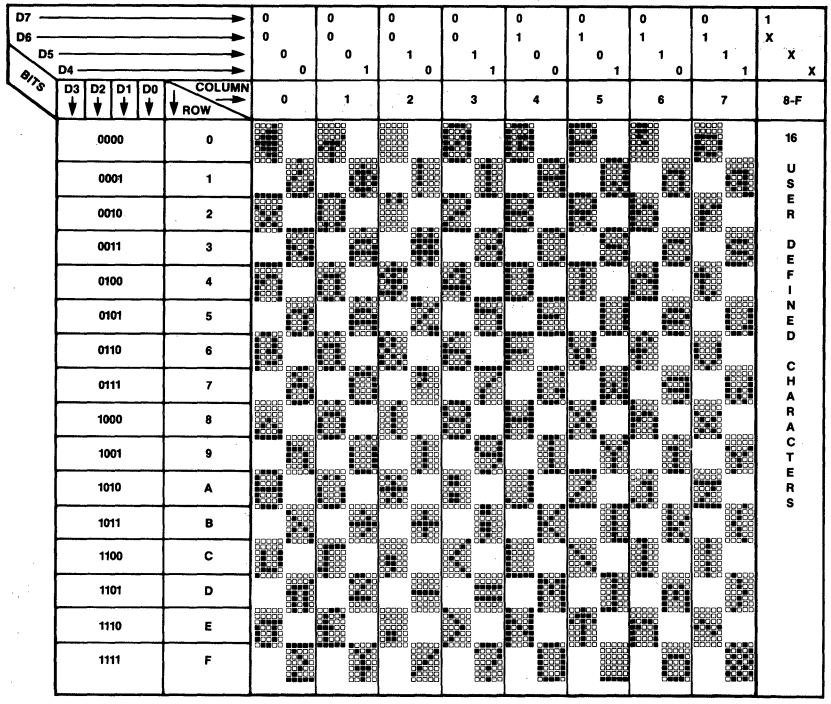
Absolute Maximum Ratings

Supply Voltage, V_{DD} to Ground[1] ..... -0.3 to 7.0 V
Operating Voltage, V_{DD} to Ground[2] ..... 5.5 V
Input Voltage, Any Pin to Ground ..... -0.3 to V_{DD} +0.3 V
Free Air Operating Temperature Range, T_A[3] ..... -45°C to +85°C
Relative Humidity (non-condensing) 85%
Storage Temperature Range, T_S ..... -55°C to +100°C
Maximum Solder Temperature
1.59 mm (0.063 in.) Below Seating Plane, t < 5 sec ..... 260°C
ESD Protection @ 1.5 kΩ, 100 pF ..... V_Z = 4 kV (each pin)

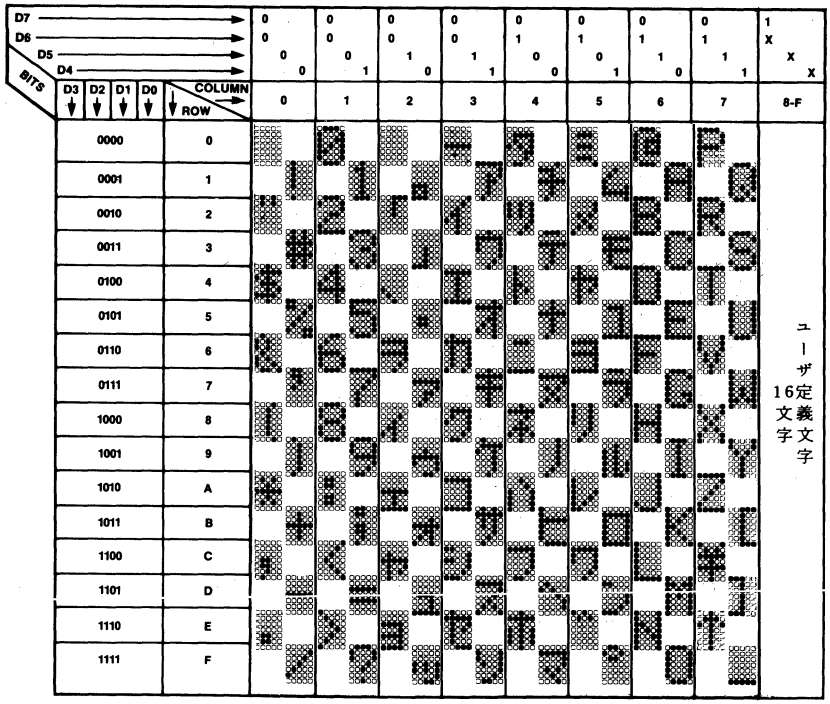
Notes:
1. Maximum Voltage is with no LEDs illuminated.
2. 20 dots ON in all locations at full brightness.
3. Maximum supply voltage is 5.25 V for operation above 70°C.

ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED WITH THE HDSP-211X AND HDSP-212X.

ASCII Character Set HDSP-2110, HDSP-2111, HDSP-2112, HDSP-2113



Katakana Character Set HDSP-2121, HDSP-2122, HDSP-2123



Recommended Operating Conditions

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

Electrical Characteristics Over Operating Temperature Range

$4.5 < V_{DD} < 5.5$ V (unless otherwise specified)

Parameter	Symbol	Min.	25°C Typ.[1]	25°C Max.[1]	Max.	Units	Test Conditions
Input Leakage (Input without pullup)	I_I	-1.0			1.0	µA	V_{IN} = 0 to V_{DD}, pins CLK, D_0-D_7, A_0-A_4
Input Current (Input with pullup)	I_{IP}	-30	-11	-18	0	µA	V_{IN} = 0 to V_{DD}, pins CLS, $\overline{RST}$, $\overline{WR}$, $\overline{RD}$, $\overline{CE}$, $\overline{FL}$
I_{DD} Blank	I_{DD} (BLK)		0.5	3.0	4.0	mA	$V_{IN} = V_{DD}$
I_{DD} 8 digits 12 dots/character[2,3]	I_{DD}(V)		200	255	330	mA	"V" on in all 8 locations
I_{DD} 8 digits 20 dots/character[2,3,4,5]	I_{DD}(#)		300	370	430	mA	"#" on in all locations
Input Voltage High	V_{IH}	2.0			V_{DD} +0.3	V	
Input Voltage Low	V_{IL}	GND -0.3 V			0.8	V	
Output Voltage High	V_{OH}	2.4				V	V_{DD} = 4.5 V, I_{OH} = -40 µA
Output Voltage Low D_0-D_7	V_{OL}				0.4	V	V_{DD} = 4.5 V, I_{OL} = 1.6 mA
Output Voltage Low CLK	V_{OL}				0.4	V	V_{DD} = 4.5 V, I_{OL} = 40 µA
Thermal Resistance IC Junction-to-Case	$R\theta_{J-C}$		15			°C/W	

Notes:
1. V_{DD} = 5.0 V.
2. Average I_{DD} measured at full brightness. See Table 2 in Control Word Section for I_{DD} at lower brightness levels. Peak I_{DD} = 28/15 x I_{DD} (#).
3. Maximum I_{DD} occurs at -55°C.
4. Maximum I_{DD}(#) = 355 mA at V_{DD} = 5.25 V and IC T_J = 150°C.
5. Maximum I_{DD}(#) = 375 mA at V_{DD} = 5.5 V and IC T_J = 150°C.

Optical Characteristics at 25°C[6]

V_{DD} = 5.0 V at Full Brightness

High Efficiency Red HDSP-2112/HDSP-2122

Description	Symbol	Min.	Typ.	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		635	nm
Dominant Wavelength	λ_d		626	nm

Orange HDSP-2110

Description	Symbol	Min.	Typ.	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		600	nm
Dominant Wavelength	λ_d		602	nm

Yellow HDSP-2111/HDSP-2121

Description	Symbol	Min.	Typ.	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		583	nm
Dominant Wavelength	λ_d		585	nm

High Performance Green HDSP-2113/HDSP-2123

Description	Symbol	Min.	Typ.	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		568	nm
Dominant Wavelength	λ_d		574	nm

Note:
6. Refers to the initial case temperature of the device immediately prior to the light measurement.

AC Timing Characteristics Over Temperature Range

V_{DD} = 4.5 to 5.5 V unless otherwise specified.

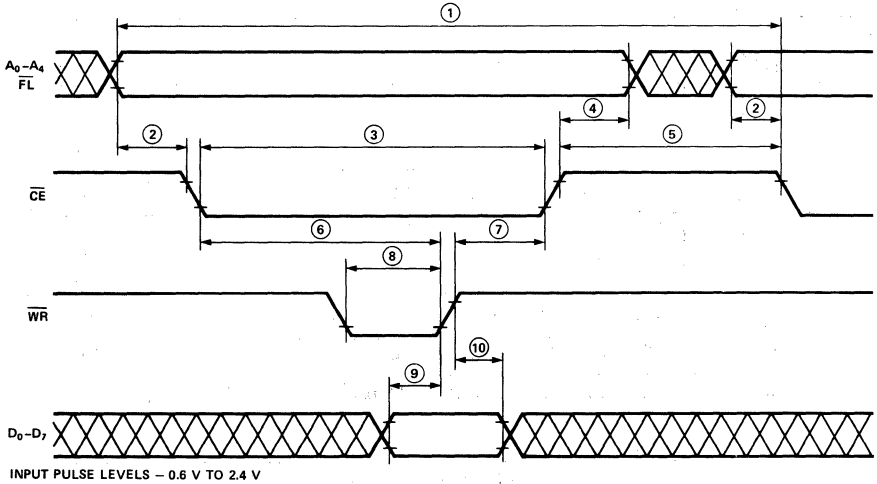
Reference Number	Symbol	Description	Min.[1]	Units
1	t_{ACC}	Display Access Time		
		Write	210	
		Read	230	ns
2	t_{ACS}	Address Setup Time to Chip Enable	10	ns
3	t_{CE}	Chip Enable Active Time[2, 3]		
		Write	140	
		Read	160	ns
4	t_{ACH}	Address Hold Time to Chip Enable	20	ns
5	t_{CER}	Chip Enable Recovery Time	60	ns
6	t_{CES}	Chip Enable Active Prior to Rising Edge of[2, 3]		
		Write	140	
		Read	160	ns
7	t_{CEH}	Chip Enable Hold Time to Rising Edge of Read/Write Signal[2, 3]	0	ns
8	t_W	Write Active Time	100	ns
9	t_{WD}	Data Valid Prior to Rising Edge of Write Signal	50	ns
10	t_{DH}	Data Write Hold Time	20	ns
11	t_R	Chip Enable Active Prior to Valid Data	160	ns
12	t_{RD}	Read Active Prior to Valid Data	75	ns
13	t_{DF}	Read Data Float Delay	10	ns
	t_{RC}	Reset Active Time[4]	300	ns

Notes:
1. Worst case values occur at an IC junction temperature of 150°C.
2. For designers who do not need to read from the display, the Read line can be tied to V_{DD} and the Write and Chip Enable lines can be tied together.
3. Changing the logic levels of the Address lines when $\overline{CE}$ = "0" may cause erroneous data to be entered into the Character RAM, regardless of the logic levels of the $\overline{WR}$ and $\overline{RD}$ lines.
4. The display must not be accessed until after 3 clock pulses (110 µs min. using the internal refresh clock) after the rising edge of the reset line.

Symbol	Description	25°C Typical	Minimum[1]	Units
F_{OSC}	Oscillator Frequency	57	28	kHz
F_{RF} [5]	Display Refresh Rate	256	128	Hz
F_{FL} [6]	Character Flash Rate	2	1	Hz
t_{ST} [7]	Self Test Cycle Time	4.6	9.2	sec

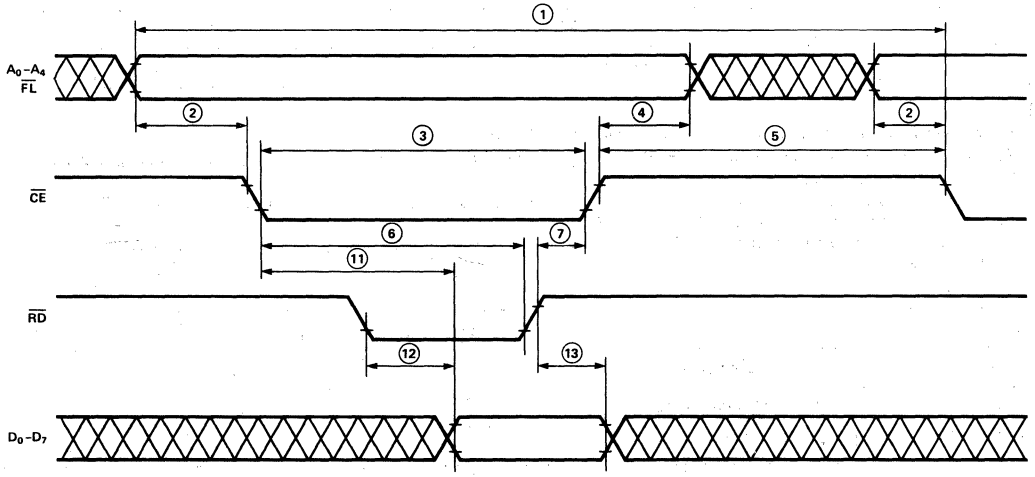
Notes:
5. $F_{RF} = F_{OSC}/224$
6. $F_{FL} = F_{OSC}/28{,}672$
7. $t_{ST} = 262{,}144/F_{osc}$

Write Cycle Timing Diagram



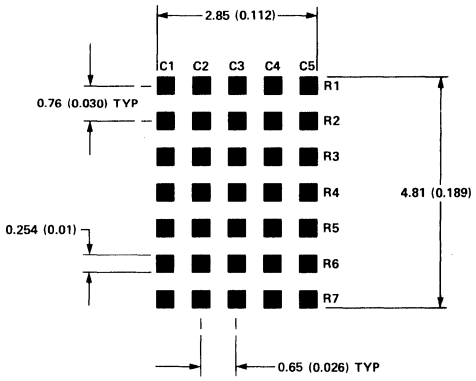
INPUT PULSE LEVELS – 0.6 V TO 2.4 V

Read Cycle Timing Diagram



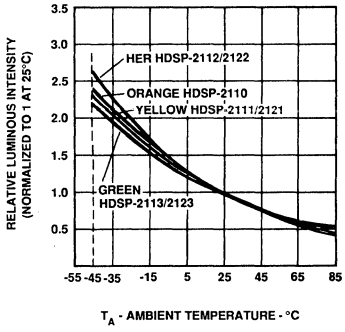
INPUT PULSE LEVELS: 0.6 V TO 2.4 V
OUTPUT REFERENCE LEVELS: 0.6 V TO 2.2 V
OUTPUT LOADING = 1 TTL LOAD AND 100pF

Character Font



(Not to Scale)

Relative Luminous Intensity vs. Temperature



Electrical Description

Pin Function	Description
RESET ($\overline{RST}$, pin 1)	Reset initializes the display.
FLASH ($\overline{FL}$, pin 2)	$\overline{FL}$ low indicates an access to the Flash RAM and is unaffected by the state of address lines A_3-A_4.
ADDRESS INPUTS (A_0-A_4, pins 3-6, 10)	Each location in memory has a distinct address. Address inputs (A_0-A_2) select a specific location in the Character RAM, the Flash RAM or a particular row in the UDC (User-Defined Character) RAM. A_3-A_4 are used to select which section of memory is accessed. Table 1 shows the logic levels needed to access each section of memory.

Table 1. Logic Levels to Access Memory

FL	A_4	A_3	Section of Memory	A_2 A_1 A_0
0	X	X	Flash RAM	Character Address
1	0	0	UDC Address Register	Don't Care
1	0	1	UDC RAM	Row Address
1	1	0	Control Word Register	Don't Care
1	1	1	Character RAM	Character Address

CLOCK SELECT (CLS, pin 11)	This input is used to select either an internal or external clock source.
CLOCK INPUT/OUTPUT (CLK, pin 12)	Outputs the master clock (CLS = 1) or inputs a clock (CLS = 0) for slave displays.
WRITE ($\overline{WR}$, pin 13)	Data is written into the display when the $\overline{WR}$ input is low and the $\overline{CE}$ input is low.
CHIP ENABLE ($\overline{CE}$, pin 17)	This input must be at a logic low to read or write data to the display and must go high between each read and write cycle.
READ ($\overline{RD}$, pin 18)	Data is read from the display when the $\overline{RD}$ input is low and the $\overline{CE}$ input is low.
DATA Bus (D_0-D_7, pins 19, 20, 23-28)	The Data bus is used to read from or write to the display.
GND (SUPPLY) (pin 15)	This is the analog ground for the LED drivers.
GND (LOGIC) (pin 16)	This is the digital ground for internal logic.
V_{DD} (POWER) (pin 14)	This is the positive power supply input.
V_{DD} (SUBSTRATE) (pins 7-9)	These pins are used to bias the IC substrate and must be connected to V_{DD}. These pins cannot be used to supply power to the display.

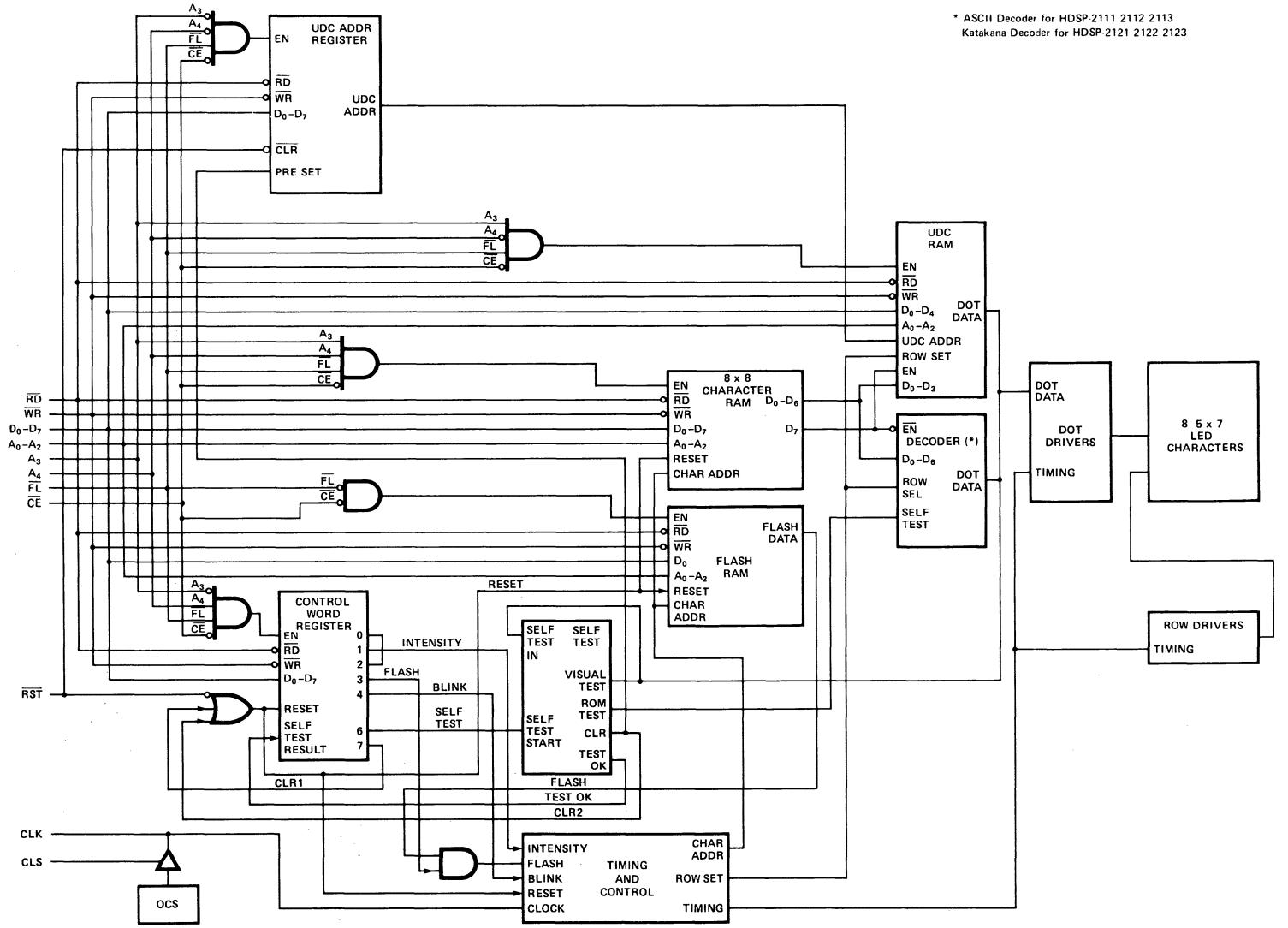


Figure 1. HDSP-213X Internal Block Diagram.

Display Internal Block Diagram

Figure 1 shows the internal block diagram of the HDSP-211X/-212X display. The CMOS IC consists of an 8 byte Character RAM, an 8 bit Flash RAM, a 128 character ASCII (Katakana) decoder, a 16 character UDC RAM, a UDC Address Register, a Control Word Register and the refresh circuitry necessary to synchronize the decoding and driving of eight 5 x 7 dot matrix characters. The major user accessible portions of the display are listed below:

Character RAM	This RAM stores either ASCII (Katakana) character data or a UDC RAM address.
Flash RAM	This is a 1 x 8 RAM which stores Flash data.
User-Defined Character RAM (UDC RAM)	This RAM stores the dot pattern for custom characters.
User-defined Character Address Register (UDC Address Register)	This register is used to provide the address to the UDC RAM when the user is writing or reading a custom character.
Control Word Register	This register allows the user to adjust the display brightness, flash individual characters, blink, self test or clear the display.

Character Ram

Figure 2 shows the logic levels needed to access the HDSP-211X/-212X Character RAM. During a normal access the $\overline{CE}$ = "0" and either $\overline{RD}$ = "0" or $\overline{WR}$ = "0". However, erroneous data may be written into the Character RAM if the Address lines are unstable when $\overline{CE}$ = "0" regardless of the logic levels of the $\overline{RD}$ or $\overline{WR}$ lines. Address lines A_0-A_2 are used to select the location in the Character RAM. Two types of data can be stored in each Character RAM location: an ASCII (Katakana) code or a UDC RAM address. Data bit D_7 is used to differentiate between the ASCII (Katakana) character and a UDC RAM address. D_7 = 0 enables the ASCII (Katakana) decoder and D_7 = 1 enables the UDC RAM. D_0-D_6 are used to input ASCII (Katakana) data and D_0-D_3 are used to input a UDC address.

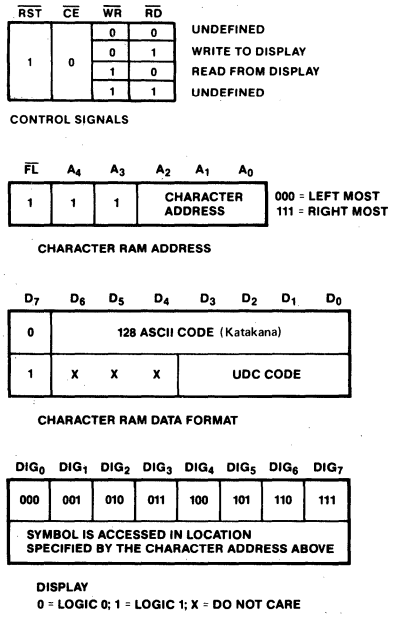


Figure 2. Logic Levels to Access the Character RAM.

UDC RAM and UDC Address Register

Figure 3 shows the logic levels needed to access the UDC RAM and the UDC Address Register. The UDC Address Register is eight bits wide. The lower four bits (D_0-D_3) are used to select one of the 16 UDC locations. The upper four bits (D_4-D_7) are not used. Once the UDC address has been stored in the UDC Address Register, the UDC RAM can be accessed.

To completely specify a 5 x 7 character requires eight write cycles. One cycle is used to store the UDC RAM address in the UDC Address Register. Seven cycles are used to store dot data in the UDC RAM. Data is entered by rows. One cycle is needed to access each row. Figure 4 shows the organization of a UDC character assuming the symbol to be stored is an "F". A_0-A_2 are used to select the row to be accessed and D_0-D_4 are used to transmit the row dot data. The upper three bits (D_5-D_7) are ignored. D_0 (least significant bit) corresponds to the right most column of the 5 x 7 matrix and D_4 (most significant bit) corresponds to the left most column of the 5 x 7 matrix.

Flash RAM

Figure 5 shows the logic levels needed to access the Flash RAM. The Flash RAM has one bit associated with each location of the Character RAM. The Flash input is used to select the Flash RAM. Address lines A_3-A_4 are ignored. Address lines A_0-A_2 are used to select the location in the Flash RAM to store the attribute. D_0 is used to store or remove the flash attribute. D_0 = "1" stores the attribute and D_0 = "0" removes the attribute.

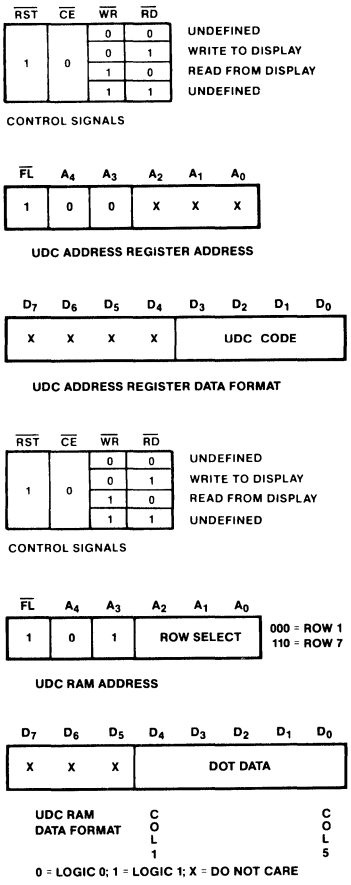


Figure 3. Logic Levels to Access a UDC Character.

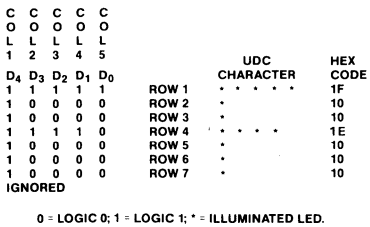


Figure 4. Data to Load "F" into the UDC RAM.

When the attribute is enabled through bit 3 of the Control Word and a "1" is stored in the Flash RAM, the corresponding character will flash at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock the flash rate can be calculated by dividing the clock frequency by 28,672.

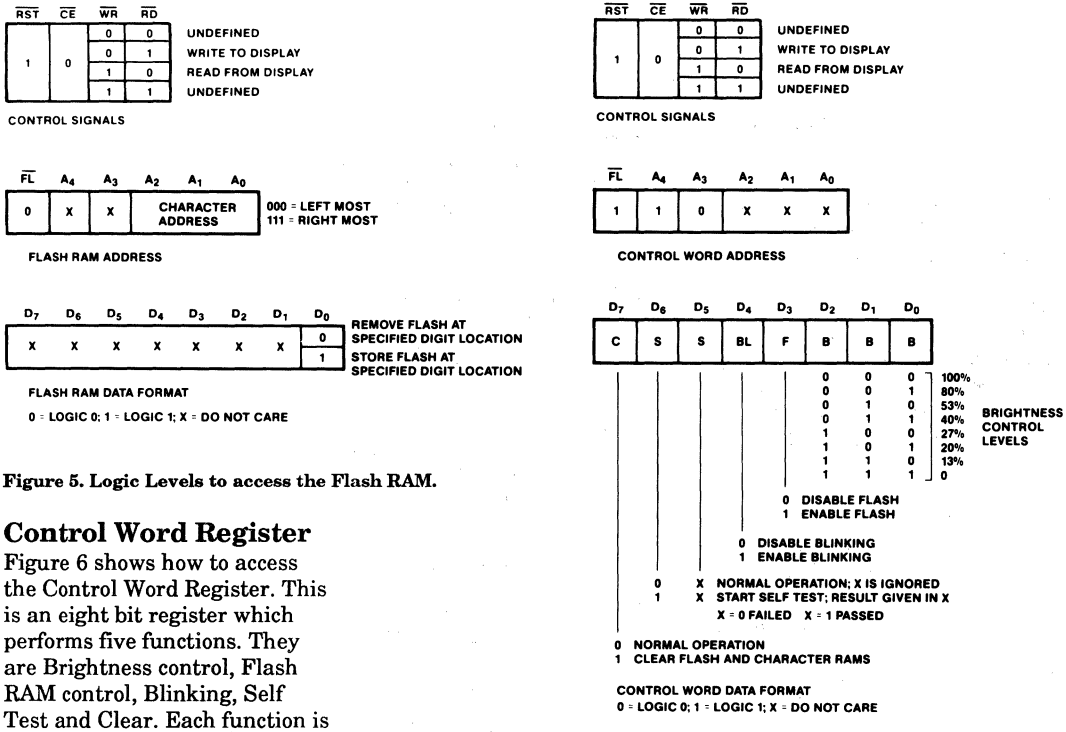


Figure 5. Logic Levels to access the Flash RAM.

Figure 6. Logic Levels to Access the Control Word Register

Control Word Register

Figure 6 shows how to access the Control Word Register. This is an eight bit register which performs five functions. They are Brightness control, Flash RAM control, Blinking, Self Test and Clear. Each function is independent of the others. However, all bits are updated during each Control Word write cycle.

Brightness (Bits 0-2)

Bits 0-2 of the Control Word adjust the brightness of the display. Bits 0-2 are interpreted as a three bit binary code with code (000) corresponding to maximum brightness and code (111) corresponding to a blanked display. In addition to varying the display brightness, bits 0-2 also vary the average value of I_{DD}. I_{DD} can be calculated at any brightness level by multiplying the percent brightness level by the value of I_{DD} at the 100% brightness level. These values of I_{DD} are shown in Table 2.

Table 2. Current Requirements at Different Brightness Levels

Symbol	D_2	D_1	D_0	% Brightness	V_{DD} = 5.0 V 25°C Typ.	Units
I_{DD} (V)	0	0	0	100	200	mA
	0	0	1	80	160	mA
	0	1	0	53	106	mA
	0	1	1	40	80	mA
	1	0	0	27	54	mA
	1	0	1	20	40	mA
	1	1	0	13	26	mA

Flash Function (Bit 3)

Bit 3 determines whether the flashing character attribute is on or off. When bit 3 is a "1", the output of the Flash RAM is checked. If the content of a location in the Flash RAM is a "1", the associated digit will flash at approximately 2 Hz. For an external clock, the blink rate can be calculated by dividing the clock frequency by 28,672. If the flash enable bit of the Control Word is a "0", the content of the Flash RAM is ignored. To use this function with multiple display systems see the Reset section.

Blink Function (Bit 4)

Bit 4 of the Control Word is used to synchronize blinking of all eight digits of the display. When this bit is a "1" all eight digits of the display will blink at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock, the blink rate can be calculated by dividing the clock frequency by 28,672. This function will override the Flash function when it is active. To use this function with multiple display systems see the Reset section.

Self Test Function (Bits 5, 6)
Bit 6 of the Control Word Register is used to initiate the self test function. Results of the internal self test are stored in bit 5 of the Control Word. Bit 5 is a read only bit where bit 5 = "1" indicates a passed self test and bit 5 = "0" indicates a failed self test.

Setting bit 6 to a logic 1 will start the self test function. The built-in self test function of the IC consists of two internal routines which exercises major portions of the IC and illuminates all of the LEDs. The first routine cycles the ASCII (Katakana) decoder ROM through all states and performs a checksum on the output. If the checksum agrees with the correct value, bit 5 is set to "1". The second routine provides a visual test of the LEDs using the drive circuitry. This is accomplished by writing checkered and inverse checkered patterns to the display. Each pattern is displayed for approximately 2 seconds.

During the self test function the display must not be accessed. The time needed to execute the self test function is calculated by multiplying the clock period by 262,144. For example, assume a clock frequency of 58 KHz, then the time to execute the self test function frequency is equal to (262,144/58,000) = 4.5 second duration.

At the end of the self test function, the Character RAM is loaded with blanks, the Control Word Register is set to zeros except for bit 5, and the Flash RAM is cleared and the UDC Address Register is set to all ones.

Clear Function (Bit 7)
Bit 7 of the Control Word will clear the Character RAM and the Flash RAM. Setting bit 7 to a "1" will start the clear function. Three clock cycles (110 µs min. using the internal refresh clock) are required to complete the clear function. The display must not be accessed while the display is being cleared. When the clear function has been completed, bit 7 will be reset to a "0". The ASCII (Katakana) character code for a space (20H) will be loaded into the Character RAM to blank the display and the Flash RAM will be loaded with "0"s. The UDC RAM, UDC Address Register and the remainder of the Control Word are unaffected.

Display Reset

Figure 7 shows the logic levels needed to Reset the display. The display should be Reset on Power-up. The external Reset clears the Character RAM, Flash RAM, Control Word and resets the internal counters. After the rising edge of the Reset signal, three clock cycles (110 µs min. using the internal refresh clock) are required to complete the reset sequence. The display must not be accessed while the display is being reset. The ASCII (Katakana) Character code for a space (20H) will be loaded into the Character RAM to blank the display. The Flash RAM and Control Word Register are loaded with all "0"s. The UDC RAM and UDC Address Register are unaffected. All displays which operate with the same clock source must be simultaneously reset to synchronize the Flashing and Blinking functions.

$\overline{RST}$	$\overline{CE}$	$\overline{WR}$	$\overline{RD}$	$\overline{FL}$	A_4-A_0	D_7-D_0
0	1	X	X	X	X	X

0 = LOGIC 0; 1 = LOGIC 1; X = DO NOT CARE
NOTE:
IF RST, CE AND WR ARE LOW, UNKNOWN DATA MAY BE WRITTEN INTO THE DISPLAY.

Figure 7. Logic Levels to Reset the Display.

Mechanical and Electrical Considerations

The HDSP-211X/-212X is a 28 pin dual-in-line package with 26 external pins, which can be stacked horizontally and vertically to create arrays of any size. The HDSP-211X/212X is designed to operate continuously from -45°C to +85°C with a maximum of 20 dots on per character at 5.25 V. Illuminating all thirty-five dots at full brightness is not recommended.

The HDSP-211X/-212X is assembled by die attaching and wire bonding 280 LED chips and a CMOS IC to a thermally conductive printed circuit board. A polycarbonate lens is placed over the PC board creating an air gap over the LED wire bonds. A protective cap creates an air gap over the CMOS IC. Backfill epoxy environmentally seals the display package. This package construction makes the display highly tolerant to temperature cycling and allows wave soldering.

The inputs to the IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HDSP-211X/-212X should be stored in antistatic tubes or in conductive material. During assembly, a grounded conductive work area should be used, and assembly personnel should wear

conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static buildup. Input current latchup is caused when the CMOS inputs are subjected to either a voltage below ground (V_{IN} < ground) or to a voltage higher than V_{DD} ($V_{IN} > V_{DD}$) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{DD}. Voltages should not be applied to the inputs until V_{DD} has been applied to the display.

Thermal Considerations

The HDSP-211X/-212X has been designed to provide a low thermal resistance path for the CMOS IC to the 26 package pins. This heat is then typically conducted through the traces of the printed circuit board to free air. For most applications no additional heatsinking is required.

Measurements were made on a 32 character display string to determine the thermal resistance of the display assembly. Several display boards were constructed using 62 mil printed circuit material, and one ounce copper 20-mil traces. Some of the device pins were connected to a heatsink formed by etching a copper area on the printed circuit board surrounding the display. A maximum metalized printed circuit board was also evaluated. The junction temperature was measured for displays soldered directly to these PC boards, displays installed in sockets, and finally displays installed in sockets with a filter over the display to restrict airflow. The results of these thermal resistance measurements, $R\theta_{J-A}$ are shown in Table 3 and include the effects of $R\theta_{J-C}$.

Ground Connections

Two ground pins are provided to keep the internal IC logic ground clean. The designer can, when necessary, route the analog ground for the LED drivers separately from the logic ground until an appropriate ground plane is available. On long interconnections between the display and the host system, the designer can keep voltage drops on the analog ground from affecting the display logic levels by isolating the two grounds.

The logic ground should be connected to the same ground potential as the logic interface circuitry. The analog ground and the logic ground should be connected at a common ground which can withstand the current introduced by the switching LED drivers. When separate ground connections are used, the analog ground can vary from -0.3 V to +0.3 V with respect to the logic ground. Voltage below -0.3 V can cause all dots to be on. Voltage above +0.3 V can cause dimming and dot mismatch.

Soldering and Post Solder Cleaning Instructions for the HDSP-211X/-212X

The HDSP-211X/-212X may be hand soldered or wave soldered with SN63 solder. When hand soldering it is recommended that an electronically temperature controlled and securely grounded soldering iron be used. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux can be used. The solder wave temperature should be set at 245°C ± 5°C (473°F ± 9°F), and the dwell in the wave should be set between 1-1/2 to 3 seconds for optimum soldering. The preheat temperature should not exceed 105°C (221°F) as measured on the solder side of the PC board.

Post solder cleaning may be performed with a solvent or aqueous process. For solvent cleaning, Allied Chemical's Genesolv DES, Baron Blakeslee's Blaco-Tron TES or DuPont's Freon TE may be used. These solvents are azeotropes of trichlorotrifluoroethane FC-113 with low concentrations of ethanol (5%). The

Table 3. Thermal Resistance, θ_{JA}, Using Various Amounts of Heatsinking Material

Heatsinking Metal per Device sq. in.	W/Sockets W/O Filter (Avg.)	W/O Sockets W/O Filter (Avg.)	W/Sockets W/Filter (Avg.)	Units
0	31	30	35	°C/W
1	31	28	33	°C/W
3	30	26	33	°C/W
Max. Metal	29	25	32	°C/W
4 Board Avg.	30	27	33	°C/W

maximum exposure time in the solvent vapors at boiling temperature should not exceed 2 minutes. Solvents containing high concentrations of alcohols such as methanol, ketones such as acetone, or chlorinated solvents should not be used as they will chemically attack the polycarbonate lens. Solvents containing trichloroethylene (TCE), FC-111, FC-112 or trichloroethylane (TCA) are also not recommended.

An aqueous cleaning process may be used. A saponifier, such as Kesterbio-kleen Formula 5799 or its equivalent, may be added to the wash cycle of an aqueous process to remove rosin flux residues. Organic acid flux residues must be thoroughly removed by an aqueous cleaning process to prevent corrosion of the leads and solder connections. The optimum water temperatuer is 60°C (140°F). The maximum cumulative exposure of the HDSP-211X/-212X to wash and rinse cycles should not exceed 15 minutes. For additionsal information on soldering and post solder cleaning, see Application Note 1027.

Contrast Enhancement

The objective of contrast enhancement is to provide good readability in the end user's ambient lighting conditions. The concept is to employ both luminance and chrominance contrast techniques. These enhance readability by having the OFF-dots blend into the display background and the ON-dots vividly stand out against the same background. Contrast enhancement may be achieved by using one of the following suggested filters.

HDSP-2112/-2122
Panelgraphic SCARLET RED 65 or GRAY 10
SGL Homalite H100-1670 RED or -1250 GRAY
3M Louvered Filter R6310 RED or ND0220 GRAY

HDSP-2110
Panelgraphic AMBER 23, AMBER 26, or GRAY 10
SGL Homqalite H100-1709 AMBER or -1250 GRAY
3M Louvered Filter ND0220 GRAY

HDSP-2111/-2121
Panelgraphic YELLOW 27 or GRAY 10
SGL Homalite H100-1720 AMBER or -1250 GRAY
3M Louvered Filter ND0220 GRAY

HDSP-2113/-2123
Panelgraphic GREEN 48 or GRAY 10
SGL Homalite H100-1440 GREEN or -1250 GRAY
3M Louvered Filter ND0220 GRAY

For additional information on contrast enhancement see Application Note 1015.

HEWLETT PACKARD

Four Character 5.0mm (0.2 in.) Smart 5 x 7 Alphanumeric Displays

Technical Data

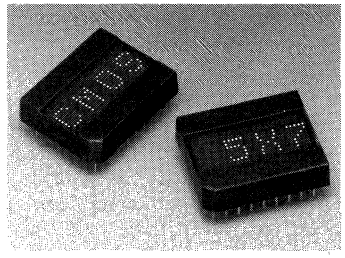
HDLR-2416
HDLO-2416
HDLA-2416
HDLY-2416
HDLG-2416

Features

- **Enhanced Drop-in Replacement to HPDL-2416**
- **Smart Alphanumeric Display**
  Built-in RAM, ASCII Decoder, and LED Drive Circuitry
- **CMOS IC for Low Power Consumption**
- **Software Controlled Dimming Levels and Blank**
- **128 ASCII Character Set**
- **End-Stackable**
- **Categorized for Luminous Intensity; YELLOW and GREEN Categorized for Color**
- **Wide Operating Temperature Range**
  -40°C to +85°C
- **Excellent ESD Protection**
- **Wave Solderable**
- **Wide Viewing Angle (50° typ)**

Description

These are 5.0 mm (0.2 inch) four character 5 x 7 dot matrix displays driven by an on-board CMOS IC. These displays are pin for pin compatible with the HPDL-2416. The IC stores and decodes 7 bit ASCII data and displays it using a 5 x 7 font. Multiplexing circuitry, and drivers are also part of the IC. The IC has fast setup and hold times which makes it easy to interface to a microprocessor.



Absolute Maximum Ratings

Supply Voltage, V_{DD} to Ground[1] ..... -0.5 V to 7.0 V
Input Voltage, Any Pin to Ground ..... -0.5 V to V_{DD} + 0.5 V
Free Air Operating Temperature Range, T_A ..... -40°C to +85°C
Relative Humidity (non-condensing) at 65°C 85%
Storage Temperature, T_S ..... -40°C to 100°C
Maximum Solder Temperature, 1.59 mm
(0.063 in.) below Seating Plane, t < 5 sec. ..... 260°C
ESD Protection, R = 1.5 kΩ, C = 100 pF ..... V_Z = 2 kV (each pin)

Note:
1. Maximum Voltage is with no LEDs illuminated.

Devices:

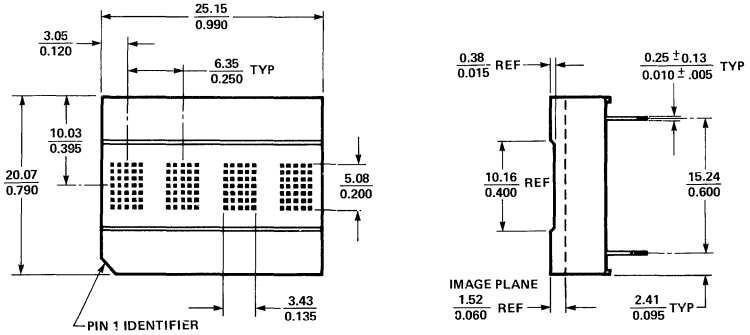
Standard Red	High Efficiency Red	Orange	Yellow	Green
HDLR-2416	HDLO-2416	HDLA-2416	HDLY-2416	HDLG-2416

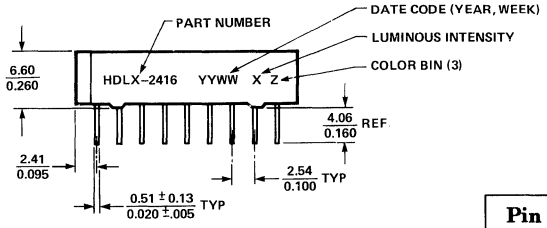
ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED WITH THE HDLX-2416

The address and data inputs can be directly connected to the microprocessor address and data buses.

The HDLX-2416 has several enhancements over the HPDL-2416. These features include an expanded character set, internal 8 level dimming control, external dimming capability, and individual digit blanking. Finally, the extended functions can be disabled which allows the HDLX-2416 to operate exactly like an HPDL-2416 by disabling all of the enhancements except the expanded character set.

Package Dimensions





Notes:
1. Unless otherwise specified the tolerance on all dimensions is ±0.254 mm (±0.010")
2. All dimensions are in mm/inches.
3. For yellow and green displays only.

Pin No.	Function	Pin No.	Function
1	$\overline{CE}_1$ Chip Enable	10	GND
2	$\overline{CE}_2$ Chip Enable	11	D_0 Data Input
3	$\overline{CLR}$ Clear	12	D_1 Data Input
4	CUE Cursor Enable	13	D_2 Data Input
5	$\overline{CU}$ Cursor Select	14	D_3 Data Input
6	$\overline{WR}$ Write	15	D_6 Data Input
7	A_1 Address Input	16	D_5 Data Input
8	A_0 Address Input	17	D_4 Data Input
9	V_{DD}	18	$\overline{BL}$ Display Blank

Character Set

ASCII CODE																		
			D0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
			D1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			D2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			D3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
D6	D5	D4	Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	0																
0	0	1	1																
0	1	0	2																
0	1	1	3																
1	0	0	4																
1	0	1	5																
1	1	0	6																
1	1	1	7																

Notes: 1. High = 1 level.
2. Low = 0 level.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

Electrical Characteristics Over Operating Temperature Range

$4.5 < V_{DD} < 5.5$ V (unless otherwise specified)

All Devices

Parameter	Symbol	Min.	25°C[1]		Max.	Units	Test Conditions
			Typ.	Max.			
I_{DD} Blank	I_{DD} (blnk)		1.0		4.0	mA	All Digits Blanked
Input Current	I_I	-40			10	µA	V_{IN} = 0 V to V_{DD} V_{DD} = 5.0 V
Input Voltage High	V_{IH}	2.0			V_{DD}	V	
Input Voltage Low	V_{IL}	GND			0.8	V	

HDLO/HDLA/HDLY/HDLG-2416

Parameter	Symbol	Min.	25°C[1]		Max.	Units	Test Conditions
			Typ.	Max.			
I_{DD} 4 digits 20 dots/character[2, 3]	I_{DD}(#)		110	130	160	mA	"#" ON in all four locations
I_{DD} Cursor all dots ON @ 50%	I_{DD} (CU)		92	110	135	mA	Cursor ON in all four locations

HDLR-2416

Parameter	Symbol	Min.	25°C[1]		Max	Units	Test Conditions
			Typ.	Max.			
I_{DD} 4 digits 20 dots/character[2,3]	I_{DD} (#)		125	146	180	mA	"#" ON in all four locations
I_{DD} Cursor all dots ON @ 50%	I_{DD}(CU)		105	124	154	mA	Cursor ON in all four locations

Notes:

1. V_{DD} = 5.0 V
2. Average I_{DD} measured at full brightness. Peak I_{DD} = 28/15 x Average I_{DD}(#).
3. I_{DD}(#) max. = 130 mA for HDLO/HDLA/HDLY/HDLG-2416 and 146 mA for HDLR-2416 at 125°C IC junction temperature and V_{DD} = 5.5 V.

Optical Characteristics at 25°C[1]

V_{DD} = 5.0 V at Full Brightness

HDLR-2416

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	0.5	1.1	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		655	nm	
Dominant Wavelength[2]	λ_d		640	nm	

HDLO-2416

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	1.2	3.5	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		635	nm	
Dominant Wavelength[2]	λ_d		626	nm	

HDLA-2416

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	1.2	3.5	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		600	nm	
Dominant Wavelength[2]	λ_d		602	nm	

HDLY-2416

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	1.2	3.7	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		583	nm	
Dominant Wavelength[2]	λ_d		585	nm	

HDLG-2416

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	1.2	5.6	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		568	nm	
Dominant Wavelength[2]	λ_d		574	nm	

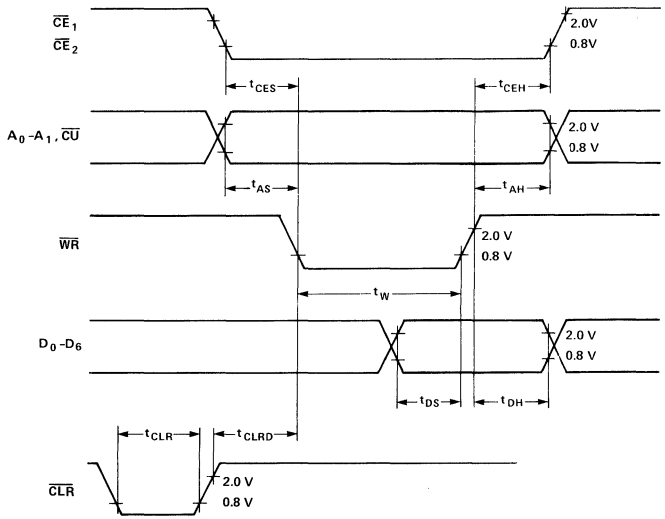
Notes:

1. Refers to the initial case temperature of the device immediately prior to the light measurement.
2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.

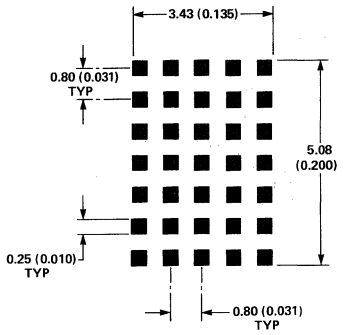
AC Timing Characteristics Over Operating Temperature Range at V_{DD} = 4.5 V

Parameter	Symbol	Min	Units
Address Setup	t_{AS}	10	ns
Address Hold	t_{AH}	40	ns
Data Setup	t_{DS}	50	ns
Data Hold	t_{DH}	40	ns
Chip Enable Setup	t_{CES}	0	ns
Chip Enable Hold	t_{CEH}	0	ns
Write Time	t_{W}	75	ns
Clear	t_{CLR}	10	µs
Clear Disable	t_{CLRD}	1	µs

Timing Diagram



Enlarged Character Font



NOTES:

1. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ± 0.254 mm (0.010 IN.)
2. DIMENSIONS ARE IN MILLIMETRES (INCHES).

Electrical Description

Pin Function	Description
Chip Enable ($\overline{CE}_1$ and $\overline{CE}_2$, pins 1 and 2)	$\overline{CE}_1$ and $\overline{CE}_2$ must be a logic 0 to write to the display.
Clear ($\overline{CLR}$, pin 3)	When $\overline{CLR}$ is a logic 0 the ASCII RAM is reset to 20hex (space) and the Control Register/ Attribute RAM is reset to 00hex.
Cursor Enable (CUE pin 4)	CUE determines whether the IC displays the ASCII or the Cursor memory. (1 = Cursor, 0 = ASCII).
Cursor Select ($\overline{CU}$, pin 5)	$\overline{CU}$ determines whether data is stored in the ASCII RAM or the Attribute RAM/Control Register. (1 = ASCII, 0 = Attribute RAM/Control Register).
Write ($\overline{WR}$, pin 6)	$\overline{WR}$ must be a logic 0 to store data in the display.
Address Inputs (A_1 and A_0, pins 8 and 7)	A_0-A_1 selects a specific location in the display memory. Address 00 accesses the far right display location. Address 11 accesses the far left location.
Data Inputs (D_0-D_6, pins 11-17)	D_0-D_6 are used to specify the input data for the display.
V_{DD} (pin 9)	V_{DD} is the positive power supply input.
GND (pin 10)	GND is the display ground.
Blanking Input ($\overline{BL}$, pin 18)	$\overline{BL}$ is used to flash the display, blank the display or to dim the display.

Display Internal Block Diagram

Figure 1 shows the HDLX-2416 display internal block diagram. The CMOS IC consists of a 4 x 7 Character RAM, a 2 x 4 Attribute RAM, a 5 bit Control Register, a 128 character ASCII decoder and the refresh circuitry necessary to synchronize the decoding and driving of four 5 x 7 dot matrix displays.

Four 7 bit ASCII words are stored in the Character RAM. The IC reads the ASCII data and decodes it via the 128 character ASCII decoder. The ASCII decoder includes the 64 character set of the HPDL-2416, 32 lower case ASCII symbols, and 32 foreign language symbols.

A 5 bit word is stored in the Control Register. Three fields within the Control Register provide an 8 level brightness control, master blank, and extended functions disable.

For each display digit location, two bits are stored in the Attribute RAM. One bit is used to enable a cursor character at each digit location. A second bit is used to individually disable the blanking features at each digit location.

The display is blanked and dimmed through an internal blanking input on the row drivers. Logic within the IC allows the user to dim the display either through the $\overline{BL}$ input or through the brightness control in the control register. Similarly the display can be blanked through the $\overline{BL}$ input, the Master Blank in the Control Register, or the Digit Blank Disable in the Attribute RAM.

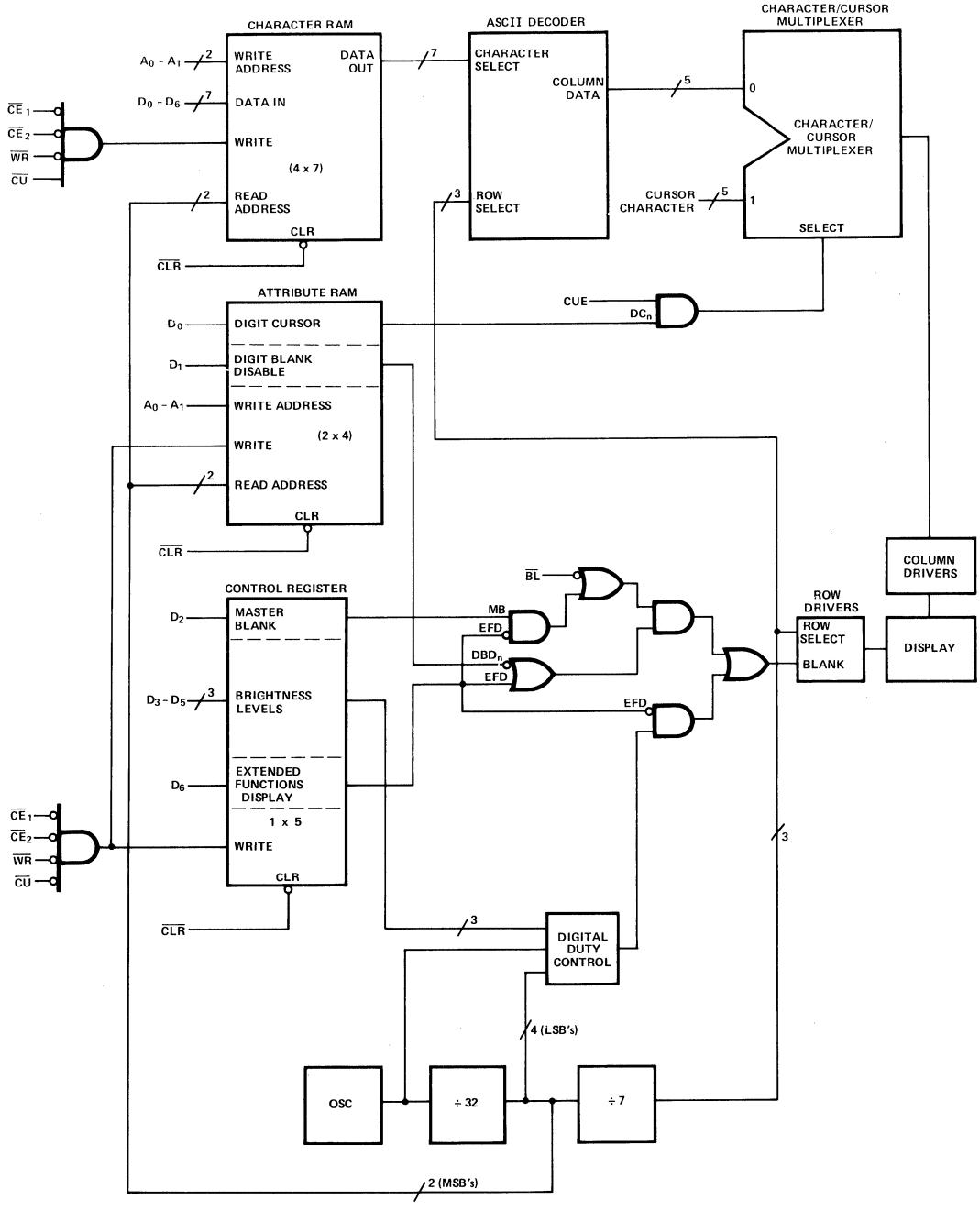


Figure 1. Internal Block Diagram

Display Clear

Data stored in the Character RAM, Control Register, and Attribute RAM will be cleared if the clear ($\overline{CLR}$) is held low for a minimum of 10 µs. Note that the display will be cleared regardless of the state of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$). After the display is cleared, the ASCII code for a space (20hex) is loaded into all character RAM locations and 00hex is loaded into all Attribute RAM/Control Register memory locations.

Data Entry

Figure 2 shows a truth table for the HDLX-2416 display. Setting the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) to logic 0 and the cursor select ($\overline{CU}$) to logic 1 will enable ASCII data loading. When cursor select ($\overline{CU}$) is set to logic 0, data will be loaded into the Control Register and Attribute RAM. Address inputs A_0-A_1 are used to select the digit location in the display. Data inputs D_0-D_6 are used to load information into the display. Data will be latched into the display on the rising edge of the $\overline{WR}$ signal. D_0-D_6, A_0-A_1, $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CU}$ must be held stable during the write cycle to ensure that correct data is stored into the display. Data can be loaded into the display in any order. Note that when A_0 and A_1 are logic 0, data is stored in the right most display location.

Cursor

When cursor enable (CUE) is a logic 1, a cursor will be displayed in all digit locations where a logic 1 has been stored in the Digit Cursor memory in the Attribute RAM. The cursor consists of all 35 dots ON at half brightness. A flashing cursor can be displayed by pulsing CUE. When CUE is a logic 0, the ASCII data stored in the Character RAM will be displayed regardless of the Digit Cursor bits.

Blanking

Blanking of the display is controlled through the $\overline{BL}$ input, the Control Register and Attribute RAM. The user can achieve a variety of functions by using these controls in different combinations, such as full hardware display blank, software blank, blanking of individual charac-

CUE	$\overline{BL}$	$\overline{CLR}$	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WR}$	$\overline{CU}$	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Function
0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Display ASCII
1	1	1															Display Stored Cursor
X	X	0															Reset RAMs
X	0	1															Blank Display but do not reset RAMS and Control Register
X	X	1	0	0	0	0	0	0	Extended Functions Disable	Intensity Control				Master Blank	Digit Blank Disable 0	Digit Cursor 0	Write to Attribute RAM and Control Register
						0	0	1	0 = Enable D_1-D_6	000 = 100% 001 = 60% 010 = 40% 011 = 27% 100 = 17% 101 = 10% 110 = 7% 111 = 3%				0 = Display ON	Digit Blank Disable 1	Digit Cursor 1	DBD_n = 0, Allows Digit n to be blanked
						0	1	0	1 = Disable D_1-D_6					1 = Display Blanked	Digit Blank Disable 2	Digit Cursor 2	DBD_n = 1 Prevents Digit n from being blanked. DC_n = 0 Removes cursor from Digit n
						0	1	1	D_0 Always Enabled						Digiit Blank Disable 3	Digit Cursor 3	DC_n = 1 Stores cursor at Digit n
X	X	1	0	0	0	1	0	0	Digit 0 ASCII Data (Right Most Character)								Write to Character RAM
						1	0	1	Digit 1 ASCII Data								
						1	1	0	Digit 2 ASCII Data								
						1	1	1	Digit 3 ASCII Data (Left Most Character)								
X	X	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	No Change
			X	1	X												
			X	X	1												

0 = Logic 0; 1 = Logic 1; X = Do Not Care

Figure 2. Display Truth Table

ters, and synchronized flashing of individual characters or entire display (by strobing the blank input). All of these blanking modes affect only the output drivers, maintaining the contents and write capability of the internal RAMs and Control Register, so that normal loading of RAMs and Control Register can take place even with the display blanked.

Figure 3 shows how the Extended Function Disable (bit D_6 of the Control Register), Master Blank (bit D_2 of the Control Register), Digit Blank Disable (bit D_1 of the Attribute RAM), and $\overline{BL}$ input can be used to blank the display.

When the Extended Function Disable is a logic 1, the display can be blanked only with the $\overline{BL}$ input. When the Extended Function Disable is a logic 0, the display can be blanked through the $\overline{BL}$ input, the Master Blank, and the Digit Blank Disable. The entire display will be blanked if either the $\overline{BL}$ input is logic 0 or the Master Blank is logic 1, providing all Digit Blank Disable bits are logic 0. Those digits with Digit Blank Disable bits a logic 1 will ignore both blank signals and remain ON. The Digit Blank Disable bits allow individual characters to be blanked or flashed in synchronization with the $\overline{BL}$ input.

EFD	MB	DBD_n	$\overline{BL}$	
0	0	0	0	Display Blanked by $\overline{BL}$
0	0	X	1	Display ON
0	X	1	0	Display Blanked by $\overline{BL}$. Individual characters "ON" based on "1" being stored in DBD_n
0	1	0	X	Display Blanked by MB
0	1	1	1	Display Blanked by MB. Individual characters "ON" based on "1" being stored in DBD_n
1	X	X	0	Display Blanked by $\overline{BL}$
1	X	X	1	Display ON

Figure 3. Display Blanking Truth Table

Dimming

Dimming of the display is controlled through either the $\overline{BL}$ input or the Control Register. A pulse width modulated signal can be applied to the $\overline{BL}$ input to dim the display. A three bit word in the Control Register generates an internal pulse width modulated signal to dim the display. The internal dimming feature is enabled only if the Extended Function Disable is a logic 0.

Bits 3-5 in the Control Register provide internal brightness control. These bits are interpreted as a three bit binary code, with code (000) corresponding to the maximum brightness and code (111) to the minimum brightness. In addition to varying the display brightness, bits 3-5 also vary the average value of I_{DD}. I_{DD} can be specified at any brightness level as shown in Table 1:

Table 1. Current Requirements at Different Brightness Levels

Symbol	D_5	D_4	D_3	Brightness	25°C Typ.	25°C Max.	Max. over Temp.	Units
I_{DD}(#)	0	0	0	100%	110	130	160	mA
	0	0	1	60%	66	79	98	mA
	0	1	0	40%	45	53	66	mA
	0	1	1	27%	30	37	46	mA
	1	0	0	17%	20	24	31	mA
	1	0	1	10%	12	15	20	mA
	1	1	0	7%	9	11	15	mA
	1	1	1	3%	4	6	9	mA

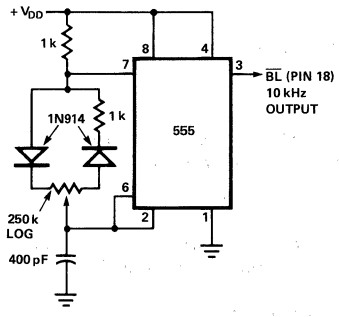


Figure 4. Intensity Modulation Control Using an Astable Multivibrator (reprinted with permission from *Electronics* magazine, Sept. 19, 1974, VNU Business pub. Inc.)

Figure 4 shows a circuit designed to dim the display from 98% to 2% by pulse width modulating the $\overline{BL}$ input. A logarithmic or a linear potentiometer may be used to adjust the display intensity. However, a logarithmic potentiometer matches the response of the human eye and therefore provides better resolution at low intensities. The circuit frequency should be designed to operate at 10 kHz or higher. Lower frequencies may cause the display to flicker.

Extended Function Disable

Extended Function Disable (bit D_6 of the Control Register) disables the extended blanking and dimming functions in the HDLX-2416. If the Extended Function Disable is a logic 1, the internal brightness control, Master Blank, and Digit Blank Disable bits are ignored. However the $\overline{BL}$ input and Cursor control are still active. This allows downward compatibility to the HPDL-2416.

Mechanical and Electrical Considerations

The HDLX-2416 is an 18 pin DIP package that can be stacked horizontally and vertically to create arrays of any size. The HDLX-2416 is designed to operate continuously from -40°C to + 85°C for all possible input conditions.

The HDLX-2416 is assembled by die attaching and wire bonding 140 LEDs and a CMOS IC to a high temperature printed circuit board. A polycarbonate lens is placed over the PC board creating an air gap environment for the LED wire bonds. Backfill epoxy environmentally seals the display package. This package construction makes the display highly tolerant to temperature cycling and allows wave soldering.

The inputs to the CMOS IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HDLX-2416 should be stored in antistatic tubes or conductive material. During assembly a grounded conductive work area should be used, and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static charge build-up.

Input current latchup is caused when the CMOS inputs are subjected either to a voltage below ground (V_{in} < ground) or to a voltage higher than V_{DD} (V_{in} > V_{DD}) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{DD}. Voltages should not be applied to the inputs until V_{DD} has been applied to the display. Transient input voltages should be eliminated.

Soldering and Post Solder Cleaning Instructions for the HDLX-2416

The HDLX-2416 may be hand soldered or wave soldered with SN63 solder. When hand soldering it is recommended that an electronically temperature controlled and securely grounded soldering iron be used. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux can be used. The solder wave temperature should be set at 245°C ±5°C (473°F ±9°F), and dwell in the wave should be set between 1 1/2 to 3 seconds for optimum soldering. The preheat temperature should not exceed 110°C (230°F) as measured on the solder side of the PC board.

Post solder cleaning may be performed with a solvent or aqueous process. For solvent cleaning, Allied Chemical's Genesolv DES, or DuPont's Freon TE may be used. These solvents are azeotropes of trichlorotrifluroethane FC-113 with low concentrations of ethanol (5%). The maximum exposure time in the solvent vapors at boiling temperature should not exceed 2 minutes. Parts should not be handled until dry and cool. Solvents containing high concentrations of alcohols such as methanol, ketones such as acetone or chlorinated solvent should not

be used as they will chemically attack the polycarbonate lens. Solvents containing trichloroethane FC-111 or FC-112 and trichloroethylene (TCE) are also not recommended.

An aqueous cleaning process may be used. A saponifier, such as Kester bio-kleen Formula 5799 or its equivalent, may be added to the wash cycle of an aqueous process to remove rosin flux residues. Organic acid flux residues must be thoroughly removed by an aqueous cleaning process to prevent corrosion of the leads and solder connections. The optimum water temperature is 60°C (140°F). The maximum cumulative exposure of the HDLX-2416 to wash and rinse cycles should not exceed 15 minutes. For additional information on soldering and post solder cleaning, see Application Note 1027.

Contrast Enhancement

The objective of contrast enhancement is to provide good readability in the end user's ambient lighting conditions. The concept is to employ both luminance and chrominance contrast techniques. These enhance readability by having the OFF-dots blend into the display background and the ON-dots vividly stand out against the same background. Contrast enhancement may be achieved by using one of the following filters listed below. For additional information on contrast enhancement, see Application Note 1015.

HDLR-2416: Panelgraphic RUBY RED 60
SGL Homalite H100-1605 RED
3M Louvered Filter R6610 RED or N0210 GRAY

HDLO-2416: Panelgraphic SCARLET RED 65 or GRAY 10
SGL Homalite H100-1670 RED or -1266 GRAY
3M Louvered Filter R6310 RED or N0210 GRAY

HDLA-2416: Panelgraphic AMBER 23, AMBER 26 or GRAY 10
SGL Homalite H100-1709 AMBER or -1266 GRAY
3M Louvered Filter A6010 or N0210 GRAY

HDLY-2416: Panelgraphic YELLOW 27 or GRAY 10
SGL Homalite H100-1720 AMBER or -1266 GRAY
3M Louvered Filter A5910 AMBER or N0210 GRAY

HDLG-2416: Panelgraphic GREEN 48
SGL Homalite H100-1440 GREEN
3M Louvered Filter G5610 GREEN or N0210 GRAY

HEWLETT PACKARD

Four Character Smart Alphanumeric Display

Technical Data

HPDL-1414
HPDL-2416

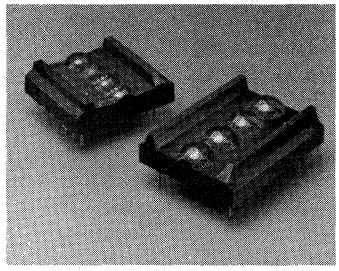
Features

- **Smart Alphanumeric Display**
  Built-in RAM, ASCII Decoder and LED Drive Circuitry
- **Wide Operating Temperature Range**
  -40°C to +85°C
- **Fast Access Time**
  160 ns
- **Excellent ESD Protection**
  Built-in Input Protection Diodes
- **CMOS IC for Low Power Consumption**
- **Full TTL Compatibility Over Operating Temperature Range**
  V_{IL} = 0.8 V
  V_{IH} = 2.0 V
- **Wave Solderable**
- **Rugged Package Construction**
- **End-Stackable**
- **Wide Viewing Angle**

Description

The HPDL-1414 and 2416 are smart, four character, sixteen-segment, red GaAsP displays. The HPDL-1414 has a character height of 2.85 mm (0.112"). The HPDL-2416 has a character height of 4.10 mm (0.160"). The on-board CMOS IC contains memory, ASCII decoder, multiplexing circuitry and drivers. The monolithic LED characters are magnified by an immersion lens which increases both character size and luminous intensity. The encapsulated dual-in-line package provides a rugged, environmentally sealed unit.

The HPDL-1414 and 2416 incorporate many improvements over competitive products. They have a wide operating temperature range, very fast IC access time, and improved ESD protection. The displays are also fully TTL compatible, wave solderable, and highly reliable. These displays are ideally suited for industrial and commercial applications where a good-looking, easy-to-use alphanumeric display is required.



Typical Applications

- **Portable Data Entry Devices**
- **Medical Equipment**
- **Process Control Equipment**
- **Test Equipment**
- **Industrial Instrumentation**
- **Computer Peripherals**
- **Telecommunication Instrumentation**

ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED WITH THE HPDL-1414 AND HPDL-2416.

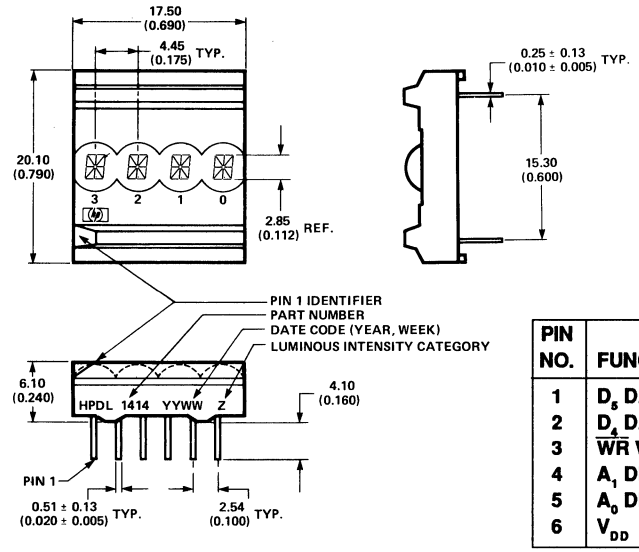
Absolute Maximum Ratings

Supply Voltage, V_{DD} to Ground ..... -0.5 V to 7.0 V
Input Voltage, Any Pin to Ground ..... -0.5 V to V_{DD} + 0.5 V
Free Air Operating Temperature Range, T_A [1] ..... -40°C to +85°C
Relative Humidity (non-condensing) at 65°C 90%
Storage Temperature, T_S ..... -40°C to +85°C
Maximum Solder Temperature, 1.59 mm (0.063 in.)
below Seating Plane, t < 5 sec. ..... 260°C
ESD Protection @ 1.5 kΩ, 100 pF ..... V_Z = 2 kV (each Pin)

Note:
1. Free air operating temperature range (HPDL-2416 only):
   T_A > 75°C No Cursors On
   T_A ≤ 75°C 1 Cursor On
   T_A ≤ 68°C 2 Cursors On
   T_A ≤ 60°C 3 Cursors On
   T_A ≤ 55°C 4 Cursors On

Package Dimensions

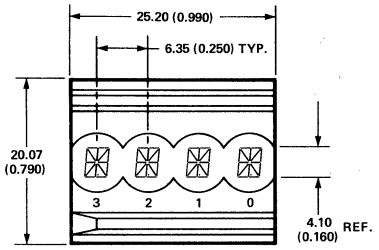
HPDL-1414

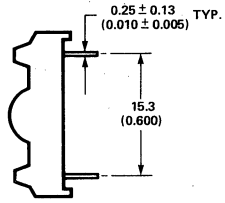


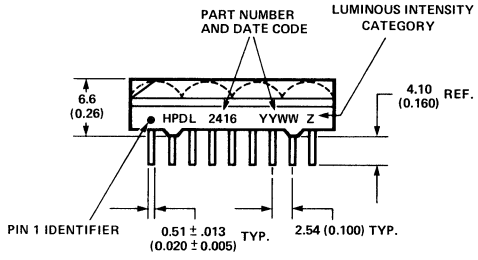
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	D_5 DATA INPUT	7	GND
2	D_4 DATA INPUT	8	D_0 DATA INPUT
3	$\overline{WR}$ WRITE	9	D_1 DATA INPUT
4	A_1 DIGIT SELECT	10	D_2 DATA INPUT
5	A_0 DIGIT SELECT	11	D_3 DATA INPUT
6	V_{DD}	12	D_6 DATA INPUT

NOTES:
1. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS 0.254 mm (0.010 in.).
2. DIMENSIONS IN mm (inches).

HPDL-2416







PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	$\overline{CE}_1$ CHIP ENABLE	10	GND
2	$\overline{CE}_2$ CHIP ENABLE	11	D_0 DATA INPUT
3	$\overline{CLR}$ CLEAR	12	D_1 DATA INPUT
4	CUE CURSOR ENABLE	13	D_2 DATA INPUT
5	$\overline{CU}$ CURSOR SELECT	14	D_3 DATA INPUT
6	$\overline{WR}$ WRITE	15	D_6 DATA INPUT
7	ADDRESS INPUT A_1	16	D_5 DATA INPUT
8	ADDRESS INPUT A_0	17	D_4 DATA INPUT
9	V_{DD}	18	$\overline{BL}$ DISPLAY BLANK

NOTES:
1. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS 0.254 mm (0.010 in.).
2. DIMENSIONS IN mm (inches).

Recommended Operating Conditions

Parameter	Sym.	Min.	Nom.	Max.	Units
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

DC Electrical Characteristics Over Operating Temperature Range

Parameter	Sym.	Min.	25°C Typ.	25°C Max.	Max.[1]	Units	Test Conditions
Input Current	I_{IL}						
HPDL-1414			17	30	50	µA	V_{DD} = 5.0 V, $\overline{BL}$ = 0.8 V
HPDL-2416			17	30	40	µA	
I_{DD} Blank	I_{DD} ($\overline{BL}$)						
HPDL-1414			1.2	2.3	4.0	mA	V_{DD} = 5.0 V, $\overline{BL}$ = 0.8 V
HPDL-2416			1.5	3.5	8.0	mA	
I_{DD} 4 Digits ON (10 Segments/digit)[2,3]	I_{DD}						
HPDL-1414			70	90	130	mA	V_{DD} = 5.0 V
HPDL-2416			85	115	170	mA	
I_{DD} 4 Digits ON Cursor[4] HPDL-2416	I_{DD}(CU)		125	165	232	mA	V_{DD} = 5.0 V
Input Voltage High	V_{IH}	2.0			V_{DD}	V	
Input Voltage Low	V_{IL}	GND			0.8	V	
Power Dissipation[5]	P_D						
HPDL-1414			350	450	715	mW	V_{DD} = 5.0 V
HPDL-2416			425	575	910	mW	

Notes:
1. V_{DD} = 5.5 V.
2. "%" illuminated in all four characters.
3. Measured at five seconds.
4. Cursor character is sixteen segments and DP ON.
5. Power Dissipation = $(V_{DD})(I_{DD})$ for 10 segments ON.

Optical Characteristics at 25°C[6]

Parameter	Sym.	Min.	Typ.	Units	Test Conditions
Peak Luminous Intensity per Digit, 8 segments ON (character average)	I_V Peak				V_{DD} = 5.0 V, "*" illuminated in all 4 digits
HPDL-1414		0.4	1.0	mcd	
HPDL-2416		0.5	1.25	mcd	
Peak Wavelength	λ_{Peak}		655	nm	
Dominant Wavelength	λ_d		640	nm	
Off Axis Viewing Angle					
HPDL-1414			±40	degrees	
HPDL-2416			±50	degrees	

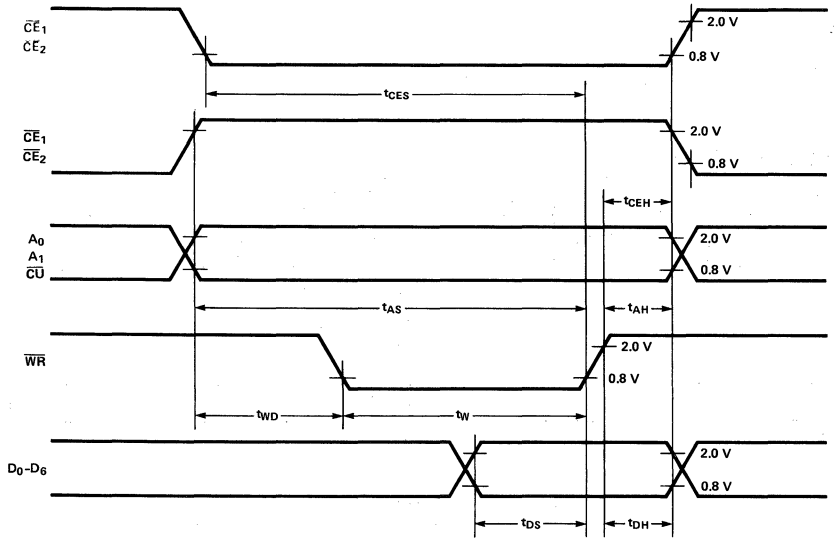
Note:
6. Refers to the initial case temperature of the device immediately prior to the light measurement.

AC Timing Characteristics Over Operating Temperature Range at V_{CC} = 4.5 V

Parameter	Symbol	20°C t_{MIN}	25°C t_{MIN}	70°C t_{MIN}	Units
Address Setup Time	t_{AS}	90	115	150	ns
Write Delay Time	t_{WD}	10	15	20	ns
Write Time	t_{W}	80	100	130	ns
Data Setup Time	t_{DS}	40	60	80	ns
Data Hold Time	t_{DH}	40	45	50	ns
Address Hold Time	t_{AH}	40	45	50	ns
Chip Enable Hold Time[1]	t_{CEH}	40	45	50	ns
Chip Enable Setup Time[1]	t_{CES}	90	115	150	ns
Clear Time[1]	t_{CLR}	2.4	3.5	4.0	ms
Access Time		130	160	200	ns
Refresh Rate		420-790	310-630	270-550	Hz

Note:
1. HPDL-2416 only.

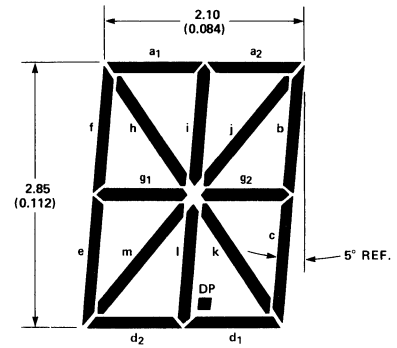
Timing Diagram



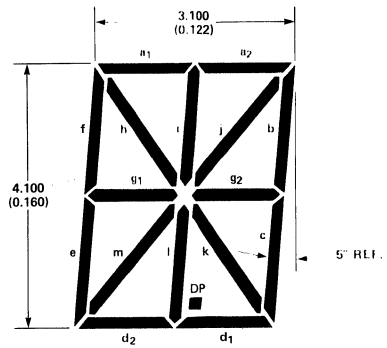
Character Set

BITS	D_3 D_2 D_1 D_0	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
D_6 D_5 D_4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 1 0	2	(space)	!	"	#	$	%	&	'	(	)	*	+	,	–	.	/
0 1 1	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
1 0 0	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1 0 1	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_

Magnified Character Font Description

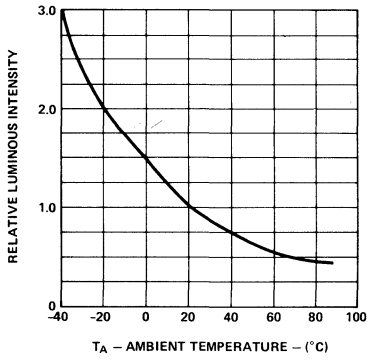


HPDL-1414



HPDL-2416

Relative Luminous Intensity vs. Temperature



Electrical Description

Display Internal Block Diagram HPDL-1414

Figure 1 shows the internal block diagram of the HPDL-1414. It consists of two parts: the display LEDs and the CMOS IC. The CMOS IC consists of a four-word ASCII memory, a 64-word character generator, 17 segment drivers, four digit drivers, and the scanning circuitry necessary to multiplex the four monolithic LED characters. In normal operation, the divide-by-four counter sequentially accesses each of the four RAM locations and simultaneously enables the appropriate display digit driver. The output of the RAM is decoded by the character generator which, in turn, enables the appropriate display segment drivers. Seven-bit ASCII data is stored in RAM. Since the display uses a 64-character decoder, half of the possible 128 input combinations are invalid. For each display location where $D_5 = D_6$ in the ASCII RAM, the display character is blanked.

Data Entry HPDL-1414

Figure 2 shows a truth table for the HPDL-1414. Data is loaded into the display through the DATA inputs (D_6-D_0), ADDRESS inputs (A_1-A_0), and WRITE ($\overline{WR}$). After a character has been written to memory, the IC decodes the ASCII data, drives the display and refreshes it without any external hardware or software.

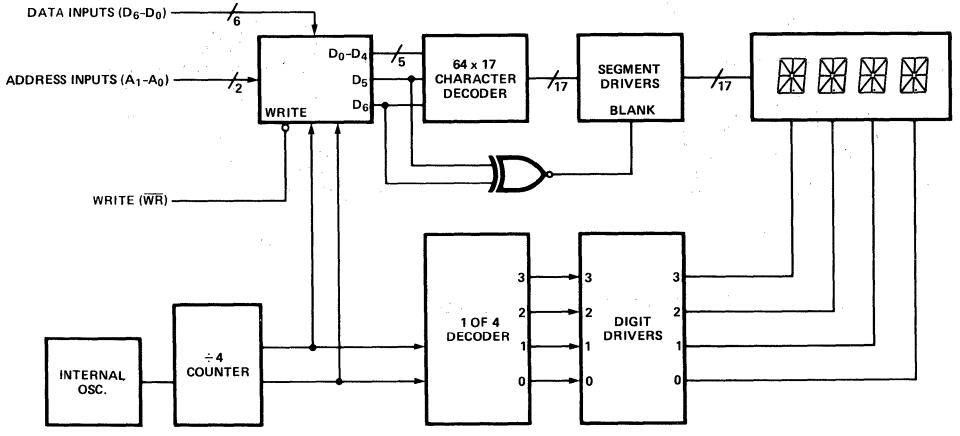


Figure 1. HPDL-1414 Internal Block Diagram.

$\overline{WR}$	A_1	A_0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	DIG_3	DIG_2	DIG_1	DIG_0
L	L	L	a	a	a	a	a	a	a	NC	NC	NC	A
L	L	H	b	b	b	b	b	b	b	NC	NC	B	NC
L	H	L	c	c	c	c	c	c	c	NC	C	NC	NC
L	H	H	d	d	d	d	d	d	d	D	NC	NC	NC
H	X	X	X	X	X	X	X	X	X	Previously Written Data			

L = LOGIC LOW INPUT
H = LOGIC HIGH INPUT
X = DON'T CARE
"a" = ASCII CODE CORRESPONDING TO SYMBOL "A"
NC = NO CHANGE

Figure 2. HPDL-1414 Write Truth Table.

Display Internal Block Diagram HPDL-2416

Figure 3 shows the internal block diagram for the HPDL-2416 display. The CMOS IC consists of a four-word ASCII memory, a four-word cursor memory, a 64-word character generator, 17 segment drivers, four digit drivers, and the scanning circuitry necessary to multiplex the four monolithic LED characters. In normal operation, the divide-by-four counter sequentially accesses each of the four RAM locations and simultaneously enables the appropriate display digit driver. The output of the RAM is decoded by the character generator which, in turn, enables the appropriate display segment drivers. For each display location, the cursor enable (CUE) selects whether the data from the ASCII RAM (CUE = 0) or the stored cursor (CUE = 1) is to be displayed. The cursor character is denoted by all sixteen segments and the DP ON. Seven-bit ASCII data is stored in RAM. Since the display utilizes a 64-character decoder, half of the possible 128 input combinations are invalid. For each display location where $D_5 = D_6$ in the ASCII RAM, the display character is blanked. The entire display is blanked when $\overline{BL} = 0$.

Data is loaded into the display through the data inputs (D_6-D_0), address inputs (A_1, A_0), chip enables ($\overline{CE_1}$, $\overline{CE_2}$), cursor select ($\overline{CU}$), and write ($\overline{WR}$). The cursor select ($\overline{CU}$) determines whether data is stored in the ASCII RAM ($\overline{CU} = 1$) or cursor memory ($CU = 0$). When $\overline{CE_1} = \overline{CE_2} = \overline{WR} = 0$ and $\overline{CU} = 1$, the information on the data inputs is stored in the ASCII RAM at the location specified by the address inputs (A_1, A_0). When $\overline{CE_1} = \overline{CE_2} = \overline{WR} = 0$ and $\overline{CU} = 0$, information on the data input, D_0, is stored in the cursor at the location specified by the address inputs (A_1, A_0). If $D_0 = 1$, a cursor character is stored in the cursor memory. If $D_0 = 0$, a previously stored cursor character will be removed from the cursor memory.

If the clear input ($\overline{CLR}$) equals zero for one internal display cycle (4 ms minimum), the data in the ASCII RAM will be rewritten with zeroes and the display will be blanked. Note that the blanking input ($\overline{BL}$) must be equal to logical one during this time.

Data Entry HPDL-2416

Figure 4 shows a truth table for the HPDL-2416 display. Setting the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) to their low state and the cursor select ($\overline{CU}$) to its high state will enable data loading. The desired data inputs (D_6-D_0) and address inputs (A_1, A_0) as well as the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) and cursor select ($\overline{CU}$) must be held stable during the write cycle to ensure that the correct data is stored into the display. Valid ASCII data codes are shown in Figure 1. The display accepts standard seven-bit ASCII data. Note that $D_6 \neq D_5$ for the codes shown in Figure 4. If $D_6 = D_5$ during the write cycle, then a blank will be stored in the display. Data can be loaded into the display in any order. Note that when $A_1 = A_0 = 0$, data is stored in the furthest right-hand display location.

Cursor Entry HPDL-2416

As shown in Figure 4, setting the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) to their low state and the cursor select ($\overline{CU}$) to its low state will enable cursor loading. The cursor character is indicated by the display symbol having all 16 segments and the DP ON. The least significant data input (D_0), the address inputs (A_1, A_0), the chip enables ($\overline{CE_1}$, $\overline{CE_2}$), and the cursor select ($\overline{CU}$) must be held stable during the write cycle to ensure that the correct data is stored in the display. If D_0 is in a low state during the write cycle, then a cursor character will be removed at the indicated location. If D_0 is in a high state during the write

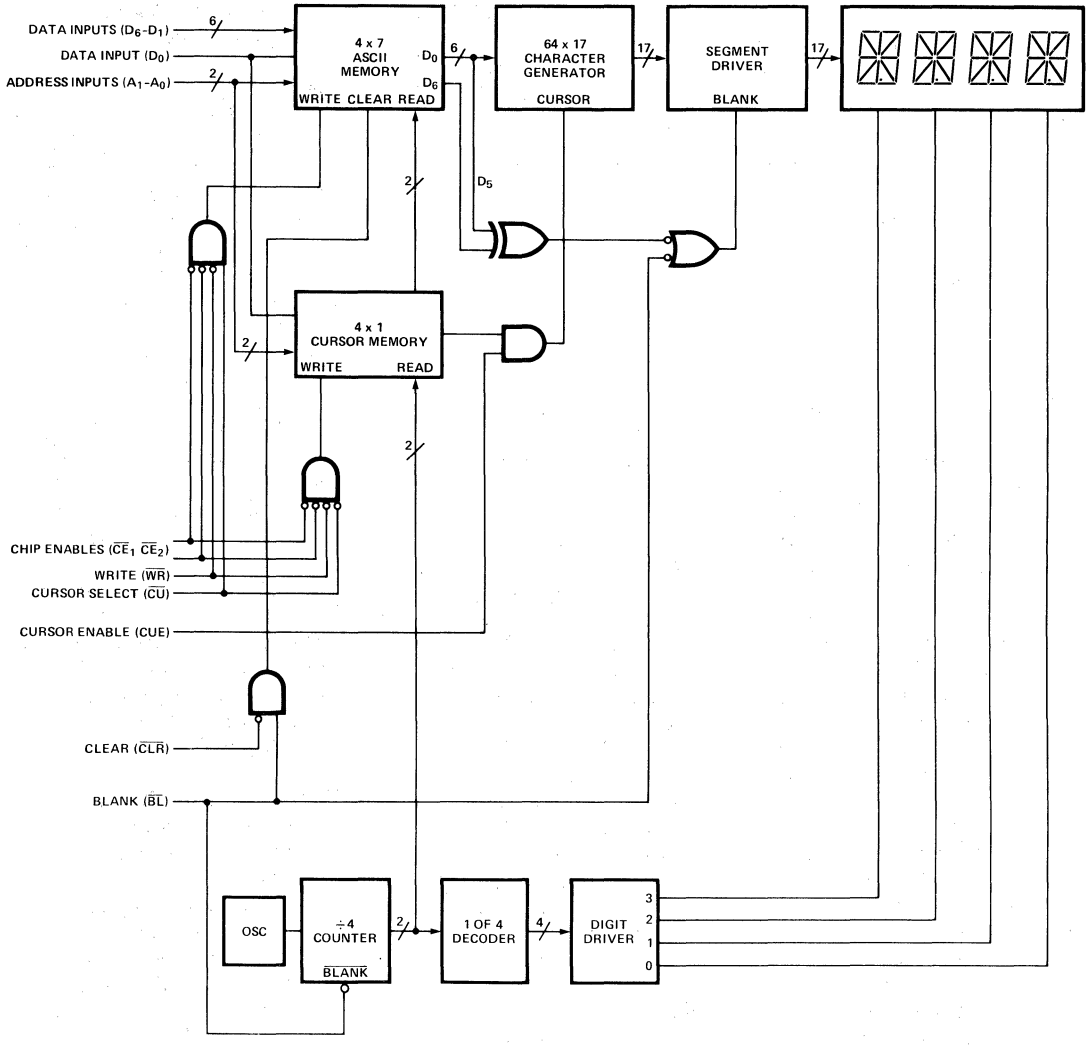


Figure 3. HPDL-2416 Internal Block Diagram.

cycle, then a cursor character will be stored at the indicated location. The presence or absence of a cursor character does not affect the ASCII data stored at that location. Again, when $A_1 = A_0 = 0$, the cursor character is stored in the furthest right-hand display location.

All stored cursor characters are displayed if the cursor enable (CUE) is high. Similarly, the stored ASCII data words are displayed, regardless of the cursor characters, if the cursor enable (CUE) is low. The cursor enable (CUE) has no effect on the storage or removal of the cursor characters within the display. A flashing cursor is displayed by pulsing the cursor enable (CUE). For applications not requiring a cursor, the cursor enable (CUE) can be connected to ground and the cursor select ($\overline{CU}$) can be connected to V_{CC}. This inhibits the cursor function and allows only ASCII data to be loaded into the display.

Function	$\overline{BL}$	$\overline{CLR}$	CUE	$\overline{CU}$	$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WR}$	A_1	A_0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	DIG_3	DIG_2	DIG_1	DIG_0
Write Data Memory	L	X	X	H	L	L	L	L	L	a	a	a	a	a	a	a	NC	NC	NC	A
				-OR-				L	H	b	b	b	b	b	b	b	NC	NC	B	NC
	X	H	X	H	L	L	L	H	L	c	c	c	c	c	c	c	NC	C	NC	NC
								H	H	d	d	d	d	d	d	d	D	NC	NC	NC
Disable Data Memory Write	X	X	X	H	X	X	H	X	X	X	X	X	X	X	X	X	Previously Written Data			
	X	X	X	H	X	H	X													
	X	X	X	H	H	X	X													
Write Cursor	X	X	X	L	L	L	L	L	L	X	X	X	X	X	X	H	NC	NC	NC	▩
								L	H	X	X	X	X	X	X	H	NC	NC	▩	NC
								H	L	X	X	X	X	X	X	H	NC	▩	NC	NC
								H	H	X	X	X	X	X	X	H	▩	NC	NC	NC
Clear Cursor	X	X	X	L	L	L	L	L	L	X	X	X	X	X	X	L	NC	NC	NC	⬚
								L	H	X	X	X	X	X	X	L	NC	NC	⬚	NC
								H	L	X	X	X	X	X	X	L	NC	⬚	NC	NC
								H	H	X	X	X	X	X	X	L	⬚	NC	NC	NC
Disable Cursor Memory	X	X	X	L	X	X	H	X	X	X	X	X	X	X	X	X	Previously Written Cursor			
	X	X	X	L	X	H	X													
	X	X	X	L	H	X	X													

L = LOGIC LOW INPUT
H = LOGIC HIGH INPUT
X = DON'T CARE

"a" = ASCII CODE CORRESPONDING TO SYMBOL "A"
NC = NO CHANGE
▩ = CURSOR CHARACTER (ALL SEGMENTS ON)

Figure 4a. Cursor/Data Memory Write Truth Table.

Function	$\overline{BL}$	$\overline{CLR}$	CUE	$\overline{CU}$	$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WR}$	DIG_3	DIG_2	DIG_1	DIG_0	
CUE	H	H	L	X	X	X	X	A	B	C	D	Display previously written data
	H	H	H	X	X	X	X	▩	▩	▩	▩	Display previously written cursor
Clear	H	L	X	X	X	X	X*	⬚	⬚	⬚	⬚	Clear data memory, cursor memory unchanged
	*NOTE: CLR should be held low for 4 ms following the last WRITE cycle to ensure all data is cleared.											
Blanking	L	X	X	X	X	X	X	⬚	⬚	⬚	⬚	Blank display, data and cursor memories unchanged.

Figure 4b. Displayed Data Truth Table.

Display Clear HPDL-2416
As shown in Figure 4, the ASCII data stored in the display will be cleared if the clear ($\overline{CLR}$) is held low and the blanking input ($\overline{BL}$) is held high for 4 ms minimum. The cursor memory is not affected by the clear ($\overline{CLR}$) input. Cursor characters can be stored or removed even while the clear ($\overline{CLR}$) is low. Note that the display will be cleared regardless of the state of the chip enables ($\overline{CE_1}$, $\overline{CE_2}$). However, to ensure that all four display characters are cleared, CLR should be held low for 4 ms following the last write cycle.

Display Blank HPDL-2416
As shown in Figure 4, the display will be blanked if the blanking input ($\overline{BL}$) is held low. Note that the display will be blanked regardless of the state of the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) or write ($\overline{WR}$) inputs. The ASCII data stored in the display and the cursor memory are not affected by the blanking input. ASCII data and cursor data can be stored even while the blanking input ($\overline{BL}$) is low. Note that while the blanking input ($\overline{BL}$) is low, the clear ($\overline{CLR}$) function is inhibited. A flashing display can be obtained by applying a low frequency square wave to the blanking input ($\overline{BL}$). Because the blanking input ($\overline{BL}$) also resets the internal display multiplex counter, the frequency applied to the blanking input ($\overline{BL}$) should be much slower than the display multiplex rate. Finally, dimming of the display through the blanking input ($\overline{BL}$) is not recommended.

For further application information please consult Application Note 1026.

Optical Considerations/ Contrast Enhancement

The HPDL-1414 and HPDL-2416 displays use a precision aspheric immersion lens to provide excellent readability and low off-axis distortion. For the HPDL-1414, the aspheric lens produces a magnified character height of 2.85 mm (0.112 in.) and a viewing angle of ±40°. For the HPDL-2416, the aspheric lens produces a magnified character height of 4.1 mm (0.160 in.) and a viewing angle of ±50°. These features provide excellent readability at distances up to 1.5 metres (4 feet) for the HPDL-1414 and 2 metres (6 feet) for the HPDL-2416.

Each HPDL-1414/2416 display is tested for luminous intensity and marked with an intensity category on the side of the display package. To ensure intensity matching for multiple package applications, mixing intensity categories for a given panel is not recommended.

The HPDL-1414/2416 display is designed to provide maximum contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60, Panelgraphic Dark Red 63, SGL Homalite H100-1650, Rohm and Haas 2423, Chequers Engraving 118, and 3M R6510. For further information on contrast enhancement, see Hewlett-Packard Application Note 1015.

Mechanical and Electrical Considerations

The HPDL-1414/2416 are dual in-line packages that can be stacked horizontally and vertically to create arrays of any size. These displays are designed to operate continuously between -40°C to +85°C with a maximum of 10 segments on per digit.

During continuous operation of all four Cursors the operating temperature should be limited to -40°C to +55°C. At temperatures above +55°C, the maximum number of Cursors illuminated continuously should be reduced as follows: No Cursors illuminated at operating temperatures above 75°C. One Cursor can be illuminated continuously at operating temperatures below 75°C. Two Cursors can be illuminated continuously at operating temperatures below 68°C. Three Cursors can be illuminated continuously at operating temperatures below 60°C.

The HPDL-1414/2416 are assembled by die attaching and wire bonding the four GaAsP/GaAs monolithic LED chips and the CMOS IC to a high temperature printed circuit board. An immersion lens is formed by placing the PC board assembly into a nylon lens filled with epoxy. A plastic cap creates an air gap to protect the CMOS IC. Backfill epoxy environmentally seals the display package. This package construction provides the display with a high tolerance to temperature cycling.

The inputs to the CMOS IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HPDL-1414/2416 should be stored in

anti-static tubes or conductive material. During assembly a grounded conductive work area should be used, and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static charge build-up. Input current latchup is caused when the CMOS inputs are subjected either to a voltage below ground (V_{IN} < ground) or to a voltage higher than V_{DD} ($V_{IN} > V_{DD}$) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{DD}. Voltages should not be applied to the inputs until V_{DD} has been applied to the display. Transient input voltages should be eliminated.

Soldering and Post Solder Cleaning Instructions

The HPDL-1414/2416 may be hand soldered or wave soldered with SN63 solder. Hand soldering may be safely performed only with an electronically temperature-controlled and securely grounded soldering iron. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux can be used. The solder wave temperature should be 245°C ± 5°C (473°F ± 9°F), and the dwell in the wave should be set at 1-1/2 to 3 seconds for optimum soldering. Preheat temperature should not exceed 93°C (200°F) as measured on the solder side of the PC board.

Post solder cleaning may be performed with a solvent or aqueous process. For solvent cleaning, Allied Chemical Genesolv DES, Baron Blakeslee Blaco-Tron TES or DuPont Freon TE can only be used. These solvents are azeotropes of trichlorotrifluoroethane FC-113 with low concentrations of ethanol (5%). The maximum exposure time in the solvent vapors at boiling temperature should not exceed 2 minutes. Solvents containing high concentrations of alcohols, pure alcohols, isopropanol or acetone should not be used as they will chemically attack the nylon lens. Solvents containing trichloroethane FC-111 or FC-112 and trichloroethylene (TCE) are not recommended.

An aqueous cleaning process is highly recommended. A saponifier, such as Kester-Biokleen Formula 5799 or equivalent, may be added to the wash cycle of an aqueous process to remove rosin flux residues. Organic acid flux residues must be thoroughly removed by an aqueous cleaning process to prevent corrosion of the leads and solder connections. The optimum water temperature is 60°C (140°F). The maximum cumulative exposure of the HPDL-2416 to wash and rinse cycles should not exceed 15 minutes.

HEWLETT PACKARD

CMOS 5x7 Alphanumeric Displays

Technical Data

HCMS-200X Series
HCMS-230X Series

Features

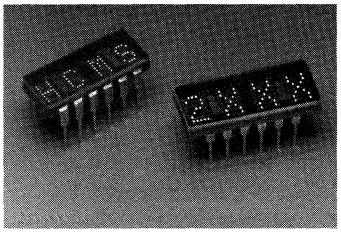
- **On-Board Low Power CMOS IC:** Integrated Shift Register with Constant Current LED Drivers
- **Wide Operating Temperature Range:** -40°C to +85°C
- **Compact Glass Ceramic 4 Character Package:** HCMS-200X Series End Stackable HCMS-230X Series X-Y Stackable
- **Five Colors:** Standard Red High Efficiency Red Orange Yellow High Performance Green
- **5 X 7 LED Matrix Displays Full ASCII Set**
- **Two Character Heights:** 3.8mm (0.15 inch) 5.0mm (0.20 inch)
- **Wide Viewing Angle:** X Axis = ± 50° Y Axis = ± 65°
- **Long Viewing Distance:** HCMS-200X Series to 2.6 Meters (8.6 Feet) HCMS-230X Series to 3.5 Meters (11.5 Feet)
- **Categorized for Luminous Intensity**
- **HCMS-2001/-2003, HCMS-2301/-2303:** Categorized for Color

Typical Applications

- **Commercial Avionics**
- **Instrumentation**
- **Medical Instruments**
- **Business Machines**

Description

The HCMS-200X and HCMS-230X series are 5x7 LED four character displays contained in 12 pin dual-in-line packages designed for displaying alphanumeric information. The character height for the HCMS-200X series displays is 3.8mm (0.15 inch), and for the HCMS-230X series displays the character height is 5.0mm (0.20 inch). These displays are available in all five LED colors: standard red, high efficiency red, orange, yellow and high performance green. The HCMS-200X series displays are end stackable and the HCMS-230X series displays are end/row stackable.



Display Selection Table

Part Number	Character Size	LED Color
HCMS-2000	3.8 mm (0.15 inch)	Standard Red
HCMS-2001	3.8 mm (0.15 inch)	Yellow
HCMS-2002	3.8 mm (0.15 inch)	High-Efficiency Red
HCMS-2003	3.8 mm (0.15 inch)	High-Performance Green
HCMS-2004	3.8 mm (0.15 inch)	Orange
HCMS-2300	5.0 mm (0.20 inch)	Standard Red
HCMS-2301	5.0 mm (0.20 inch)	Yellow
HCMS-2302	5.0 mm (0.20 inch)	High-Efficiency Red
HCMS-2303	5.0 mm (0.20 inch)	High-Performance Green
HCMS-2304	5.0 mm (0.20 inch)	Orange

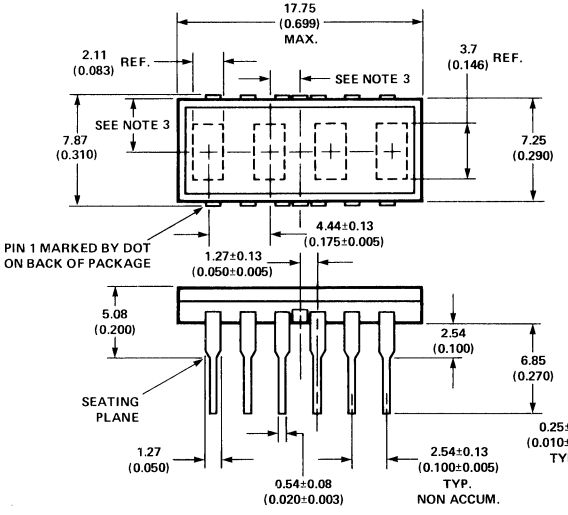
ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED.

These displays are designed with on-board CMOS integrated circuits for use in applications where conservation of power is important. The two CMOS ICs form an on-board serial-in-parallel-out 28-bit shift register with constant current output LED row drivers. Decoded column data is clocked into the on-board shift register for each refresh cycle. Full character display is achieved with external column strobing.

Compatibility with HDSP-200X/230X TTL IC Series Displays

The HCMS-200X, HCMS-230X CMOS IC displays are "drop-in" replacements for the equivalent HDSP-200X, HDSP-230X TTL IC displays. The 12 pin glass/ceramic package configuration, four digit character matrix and pin functions are identical.

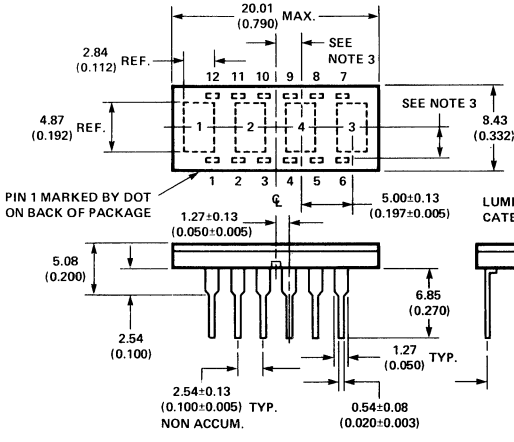
Package Dimensions

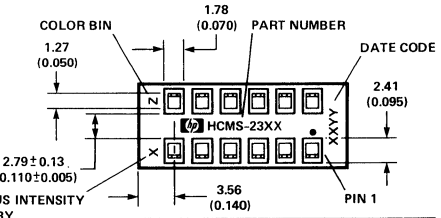


PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{DD}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

* DO NOT CONNECT OR USE

HCMS-200X Series





PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{DD}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

* DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN MILLIMETRES (INCHES)
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±0.38mm (±0.015).
3. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±0.13mm (±0.005").
4. LEAD MATERIAL IS COPPER ALLOY, SOLDER DIPPED.

HCMS-230X Series

Absolute Maximum Ratings

Supply Voltage V_{DD} to Ground ..... -0.3 V to 7.0 V
Data Input, Data Output, V_B ..... -0.3 V to V_{DD}
Column Input Voltage, V_{COL} ..... -0.3 V to V_{DD}
Free Air Operating Temperature Range, T_A ..... -40°C to +85°C
Storage Temperature Range, T_S ..... -55°C to +100°C
Maximum Allowable Package Power Dissipation, P_D [1,2]
HCMS-2000/-2001/-2002/-2003/-2004 at T_A = 78°C ..... 0.79 Watts
HCMS-2300 at T_A = 85°C ..... 0.79 Watts
HCMS-2301/-2302/-2303/-2304 at T_A = 85°C ..... 0.92 Watts
Maximum Solder Temperature
1.59 mm (0.063") Below Seating Plane, t < 5 sec ..... 260°C
ESD Protection @ 1.5 kΩ, 100 pF ..... V_Z = 4 kV (each pin)

Notes:
1. Maximum allowable power dissipation is derived from V_{DD} = 5.25 V, V_B = 2.4 V, V_{COL} = 3.5 V, 20 LEDs on per character, 20% DF.
2. The power dissipation for these displays should be derated as follows:
   HCMS-200X series derate above 78°C at 18 mW/°C, $R\theta_{J-A}$ = 60°C/W.
   HCMS-230X series may be operated without derating up to T_A = 85°C, $R\theta_{J-A}$ = 45°C/W.

Deratings based on $R\theta_{PC-A}$ = 35°C/W per display for printed circuit board assembly.
See Figure 1 for power derating.

Recommended Operating Conditions Over Operating Temperature Range (-40°C to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}	4.75	5.00	5.25	V
Data Out Current, Low State	I_{OL}			1.6	mA
Data Out Current, High State	I_{OH}			-0.5	mA
Column Input Voltage	V_{COL}	2.75	3.0	3.5	V
Setup Time	t_{SETUP}	10			ns
Hold Time	t_{HOLD}	25			ns
Clock Pulse Width High	$t_{WH(CLOCK)}$	50			ns
Clock Pulse Width Low	$t_{WL(CLOCK)}$	50			ns
Clock High to Low Transition	t_{THL}			200	ns
Clock Frequency	f_{CLOCK}			5	MHz

Electrical Characteristics Over Operating Temperature Range (-40°C to +85°C)

Parameter	Symbol	Test Conditions	Min.	Typ.*	Max.	Units
Supply Current, Dynamic[1]	I_{DDD}	f_{CLOCK} = 5 MHz		6.2	7.8	mA
Supply Current, Static[2]	I_{DDSoff} I_{DDSon}	V_B = 0.4 V V_B = 2.4 V		1.8 2.2	2.6 3.3	mA
Column Input Current	I_{COL}	V_B = 0.4 V			10	µA
HCMS-2000/-2001/-2002/-2003/-2004 HCMS-2300 HCMS-2301/-2302/-2303/-2304		V_B = 2.4 V V_B = 2.4 V V_B = 2.4 V		310 310 360	384 384 451	mA mA
Input Logic High Data, V_B, Clock	V_{IH}	V_{DD} = 4.75 V	2.0			V
Input Logic Low Data, V_B, Clock	V_{IL}	V_{DD} = 5.25 V			0.8	V
Input Current Data, Clock V_B	I_I	V_{DD} = 5.25 V 0 < V_I < 5.25 V 0 < V_B < 5.25 V	 -10 -40		 +1 0	µA
Data Out Voltage	V_{OH}	V_{DD} = 4.75 V I_{OH} = -0.5 mA I_{COL} = 0 mA	2.4	4.2		V
	V_{OL}	V_{DD} = 5.25 V I_{OL} = 1.6 mA I_{COL} = 0 mA		0.2	0.4	V
Power Dissipation Per Package[3] HCMS-2000/-2001/-2002/-2003/-2004 HCMS-2300 HCMS-2301/-2302/-2303/-2304	P_D	V_{DD} = 5.0 V V_{COL} = 3.5 V 17.5% DF V_B = 2.4 V 15 LEDs ON per Character		 414 414 481		 mW
Thermal Resistance IC Junction-to-Pin[4] HCMS-2000/-2001/-2002/-2003/-2004 HCMS-2300/-2301/-2302/-2303/-2304	$R\theta_{J\text{-}PIN}$			 25 10		 °C/W

*All typical values specified at V_{DD} = 5.0 V and T_A = 25°C.

Notes:

1. I_{DD} Dynamic is the IC current while clocking column data through the on-board shift register at a clock frequency of 5MHz, the display is not illuminated.
2. I_{DD} Static is the IC current after column data is loaded and not being clocked through the on-board shift register.
3. Four characters are illuminated with a typical ASCII character composed of 15 dots per character.
4. IC junction temperature $T_J(IC) = (P_D)(R\theta_{J\text{-}PIN} + R\theta_{PC\text{-}A}) + T_A$

Optical Characteristics at $T_A = 25°C$

Standard Red HCMS-2000/-2300

Description	Symbol	Test Condition	Min.	Typ.*	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2000 HCMS-2300	I_{vPEAK}	V_{DD} = 5.0 V, V_{COL} = 3.5 V, V_B = 2.4 V, T_j = 25°C[7]	105 130	200 300		µcd
Dominant Wavelength[8]	λ_d			639		nm
Peak Wavelength	λ_{PEAK}			655		nm

Yellow HCMS-2001/-2301

Description	Symbol	Test Condition	Min.	Typ.*	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2001 HCMS-2301	I_{vPEAK}	V_{DD} = 5.0 V, V_{COL} = 3.5 V, V_B = 2.4 V, T_j = 25°C[7]	400 650	750 1140		µcd
Dominant Wavelength[6,8]	λ_d			585		nm
Peak Wavelength	λ_{PEAK}			583		nm

High Efficiency Red HCMS-2002/-2302

Description	Symbol	Test Condition	Min.	Typ.*	Max.	Unit
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2002 HCMS-2302	I_{vPEAK}	V_{DD} = 5.0 V, V_{COL} = 3.5 V, V_B = 2.4 V, T_j = 25°C[7]	400 650	1430 1430		µcd
Dominant Wavelength[8]	λ_d			625		nm
Peak Wavelength	λ_{PEAK}			635		nm

High Performance Green HCMS-2003/-2303

Description	Symbol	Test Condition	Min.	Typ.*	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2003 HCMS-2303	I_{vPEAK}	V_{DD} = 5.0 V, V_{COL} = 3.5 V, V_B = 2.4 V, T_j = 25°C[7]	850 1280	1550 2410		µcd
Dominant Wavelength[6,8]	λ_d			574		nm
Peak Wavelength	λ_{PEAK}			568		nm

Orange HCMS-2004/-2304

Description	Symbol	Test Condition	Min.	Typ.*	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2004 HCMS-2304	I_{vPEAK}	V_{DD} = 5.0 V, V_{COL} = 3.5 V, V_B = 2.4 V, T_j = 25°C[7]	400 650	1430 1430		µcd
Dominant Wavelength[8]	λ_d			602		nm
Peak Wavelength	λ_{PEAK}			600		nm

*All typical values specified at V_{DD} = 5.0 V and T_A = 25°C unless otherwise noted.

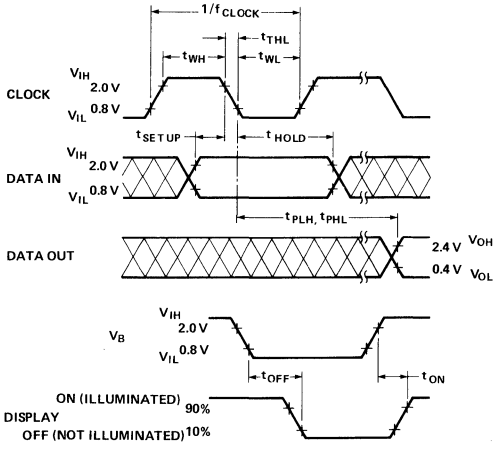
Notes:

5. These LED displays are categorized for luminous intensity, with the intensity category designated by a letter code on the back of the package.
6. The HCMS-2001/-2301 and HCMS-2003/-2303 are categorized for color with the color category designated by a number on the back of the package.
7. T_j refers to the initial case temperature of the display immediately prior to the light measurement.
8. Dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram, and represents the single wavelength which defines the color of the device.
9. The luminous sterance of the individual LED pixels may be calculated using the following equations:

$$L_v(cd/m^2) = I_v(Candela)*DF/A(Metre)^2$$
$$L_v(Footlamberts) = \pi I_v(Candela)*DF/A(Foot)^2$$

Where: A = LED pixel area = $5.3 \times 10^{-8} M^2$ or $5.8 \times 10^{-7} ft^2$
DF = LED on-time duty factor

Switching Characteristics, T_A = -40°C to +85°C



Parameter	Condition	Typ.	Max.	Units
f_{CLOCK} CLOCK Rate			5	MHz
t_{PLH}, t_{PHL} Propagation Delay CLOCK to DATA OUT	C_L = 15 pF, R_L = 2.4 kΩ		105	ns
t_{OFF} V_B (0.4 V) to Display OFF		4	5	µs
t_{ON} V_B (2.4 V) to Display ON		1	2	

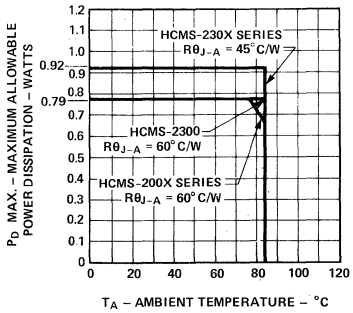


Figure 1. Maximum Allowable Power Dissipation vs Ambient Temperature as a Function of Thermal Resistance Junction-to-Ambient, $R\theta_{J\text{-}A}$. Derated Operation Assumes $R\theta_{PC\text{-}A}$ = 35°C/W Per Display for the Printed Circuit Board. T_J (IC) MAX = 125°C.

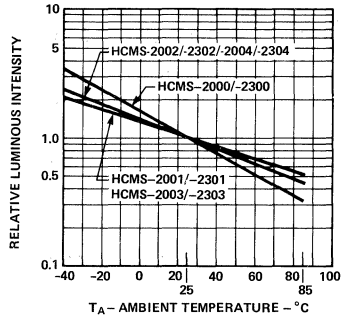


Figure 2. Relative Luminous Intensity vs Display Pin Temperature

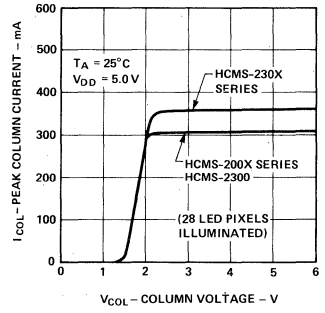


Figure 3. Peak Column Current vs Column Voltage

Electrical Description

Each display device contains four 5x7 LED dot matrix characters and two CMOS integrated circuits, as shown in Figure 4. The two CMOS integrated circuits form an on-board 28 bit serial-in-parallel-out shift register that will accept standard TTL logic levels. The Data Input, pin 12, is connected to bit position 1 and the Data Output, pin 7, is connected to bit position 28. The shift register outputs control constant current sinking LED row drivers. The nominal current sink per LED driver is 11mA for the HCMS-200X displays, 13 mA for the HCMS-230X. A logic 1 stored in the shift register enables the corresponding LED row driver and a logic 0 stored in the shift register disables the corresponding LED row driver.

The electrical configuration of these CMOS IC alphanumeric displays allows for an effective interface to a display controller circuit that supplies decoded character information. The row data for a given column (one 7 bit byte per character) is loaded (bit serial) into the on-board 28 bit shift register with high to low transitions of the Clock input. To load decoded character information into the display, column data for character 4 is loaded first and the column data for character 1 is loaded last in the following manner. The 7 data bits for column 1, character 4, are loaded into the on-board shift register. Next, the 7 data bits for column 1, character 3, are loaded into the shift register, shifting the character 4 data over one character position. This process is repeated for the other two characters until all 28 bits of column data (four 7 bit bytes of character column data) are loaded into the on-board shift register. Then the column 1 input, V_{COL} pin 1, is energized to illuminate column 1 in all four characters. This process is repeated for columns 2, 3, 4 and 5. All V_{COL} inputs should be at logic low to insure the display is off when loading data. The display will be blanked when the blanking input V_B, pin 8, is at logic low regardless of the outputs of the shift register or whether one of the V_{COL} inputs is energized.

Refer to Application Note 1016 for drive circuit information.

ESD Susceptibility

The HCMS-200X/-230X series displays have an ESD susceptibility ratings of CLASS 3 per DOD-STD-1686 and CLASS B per MIL-STD-883C. It is recommended that normal CMOS handling precautions be observed with these devices.

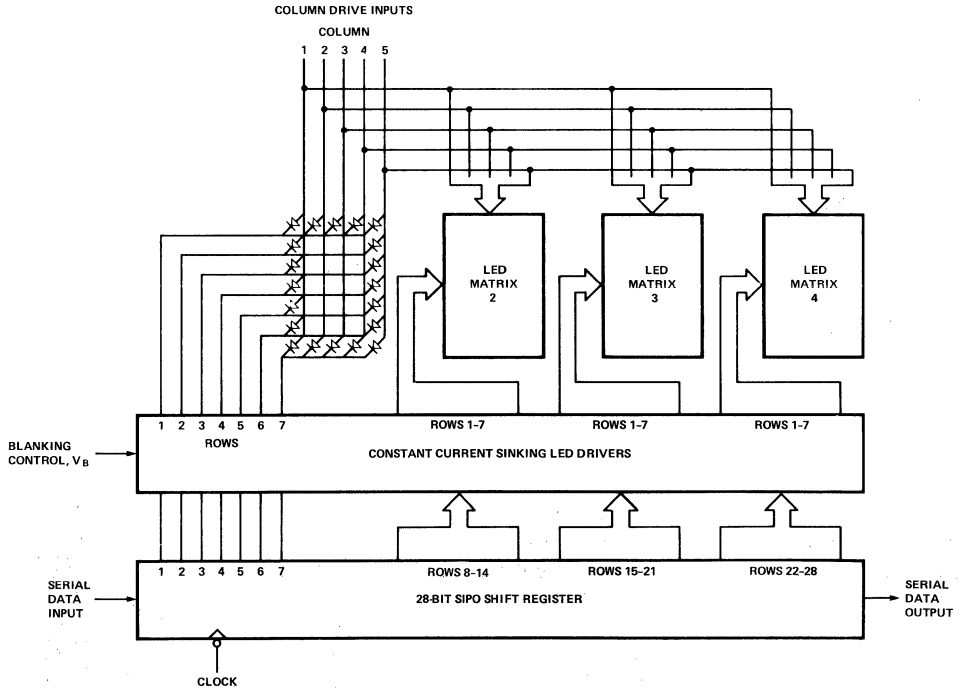


Figure 4. Block Diagram of an HCMS-2XXX Series LED Alphanumeric Display.

Soldering and Post Solder Cleaning

These displays may be soldered with a standard wave solder process using either an RMA flux and solvent cleaning or an OA flux and aqueous cleaning. For optimum soldering, the solder wave temperature should be 245°C and the dwell time for any display lead passing through the wave should be 1 1/2 to 2 seconds. The recommended solvent for post solder cleaning is Genesolv DES, manufactured by Allied Chemical. For aqueous cleaning, a water temperature of 60°C (140°F) with an immersion time not exceeding 15 minutes is recommended. For more detailed information, refer to Application Note 1027 *Soldering LED Components.*

Contrast Enhancement

When used with the proper contrast enhancement filters, the HCMS-200X/-230X series displays are readable in bright ambients. Refer to Application Note 1029 *Luminous Contrast and Sunlight Readability of the HDSP-238X Series Alphanumeric Displays for Military Applications* for contrast enhancement in bright ambients. Refer to Application Note 1015 *Contrast Enhancement Techniques for LED Displays* for information on contrast enhancement in moderate ambients.

Controller Circuits, Power Calculations and Display Dimming

Refer to Application Note 1016 *Using the HDSP-2000 Alphanumeric Display Family* for information on controller circuits to drive these displays, how to do power calculations and a technique for display dimming.

HEWLETT PACKARD

Large 5 X 7 Dot Matrix Alphanumeric Displays 17.3/26.5 mm Character Heights

Technical Data

HDSP-4701
HDSP-4703
HDSP-4401
HDSP-4403
HDSP-L101
HDSP-L103
HDSP-M101
HDSP-M103
HDSP-L201
HDSP-L203
HDSP-4501
HDSP-4503
HDSP-5401
HDSP-5403
HDSP-5101
HDSP-5103

Features

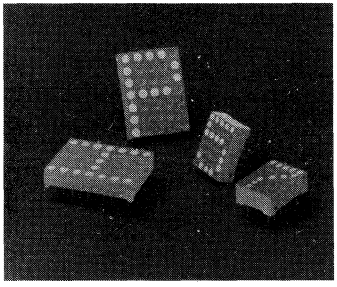
- **Multiple Colors Available**
- **Large Character Height**
- **5 X 7 Dot Matrix Font**
- **Viewable Up to 18 Meters (26.5 mm Display)**
- **X-Y Stackable**
- **Ideal for Graphics Panels**
- **Available in Common Row Anode and Common Row Cathode Configurations**
- **AlGaAs Displays Suitable for Low Power or Bright Ambients**
  Typical Intensity 1650 μcd at 2 mA Average Drive Current
- **Categorized for Intensity**
- **Mechanically Rugged**
- **Green Categorized for Color**

Description

The large 5 X 7 dot matrix alphanumeric display family consists of 26.5 mm (1.04 inch) and 17.3 mm (0.68 inch) character height packages. These devices have excellent viewability; the 26.5 mm character can be read at up to 18 meters (12 meters for the 0.68 inch part).

The 26.5 mm font has a 10.2 mm (0.4 inch) dual-in-line (DIP) configuration, while the 17.3 mm font has an industry standard 7.6 mm (0.3 inch) DIP configuration.

The HDSP-L203/4503 can be ordered with a smart driver IC. Information about the IC is available in the HDSP-211X data sheet. For ordering information see the HP Smart Display Sets data sheet.



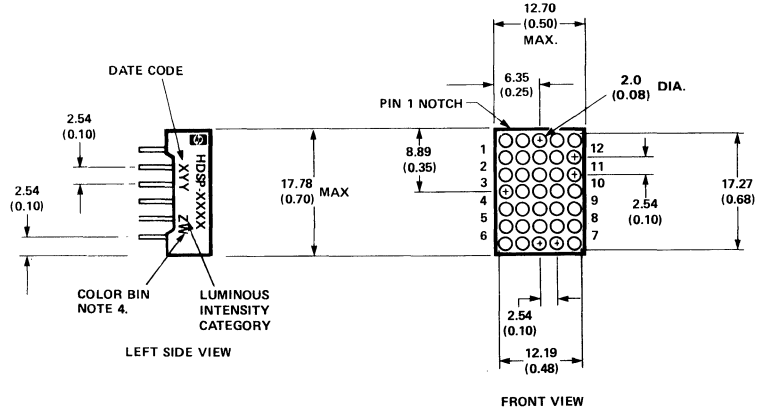
Applications include electronic instrumentation, computer peripherals, point of sale terminals, weighing scales, and industrial electronics.

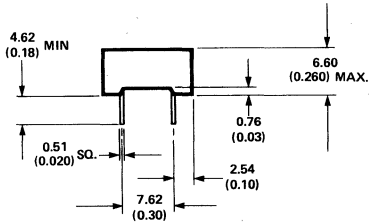
Devices

Standard Red	AlGaAs Red	High Efficiency Red	High Performance Green	Description
HDSP-4701	HDSP-L101	HDSP-L201	HDSP-5401	17.3 mm Common Row Anode
HDSP-4703	HDSP-L103	HDSP-L203	HDSP-5403	17.3 mm Common Row Cathode
HDSP-4401	HDSP-M101	HDSP-4501	HDSP-5101	26.5 mm Common Row Anode
HDSP-4403	HDSP-M103	HDSP-4503	HDSP-5103	26.5 mm Common Row Cathode

Package Dimensions

HDSP-470X/L10X/L20X/540X Series

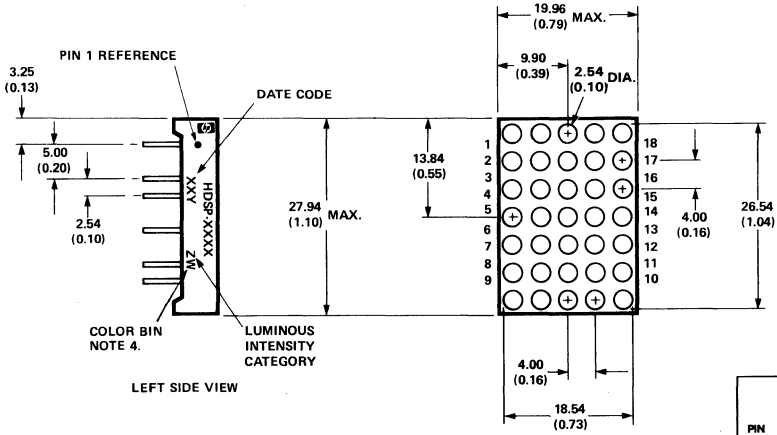


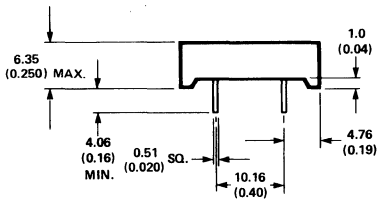


PIN	FUNCTION	
	HDSP-4701/-5401/ L101/L201	HDSP-4703/-5403/ L103/L203
1	COLUMN 1 CATHODE	ROW 1 CATHODE
2	ROW 3 ANODE	ROW 2 CATHODE
3	COLUMN 2 CATHODE	COLUMN 2 ANODE
4	ROW 5 ANODE	COLUMN 1 ANODE
5	ROW 6 ANODE	ROW 6 CATHODE
6	ROW 7 ANODE	ROW 7 CATHODE
7	COLUMN 4 CATHODE	COLUMN 3 ANODE
8	COLUMN 5 CATHODE	ROW 5 CATHODE
9	ROW 4 ANODE	COLUMN 4 ANODE
10	COLUMN 3 CATHODE	ROW 4 CATHODE
11	ROW 2 ANODE	ROW 3 CATHODE
12	ROW 1 ANODE	COLUMN 5 ANODE

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. A NOTCH ON SCRAMBLER SIDE DENOTES PIN 1.
4. FOR GREEN ONLY.

HDSP-440X/M10X/450X/510X Series



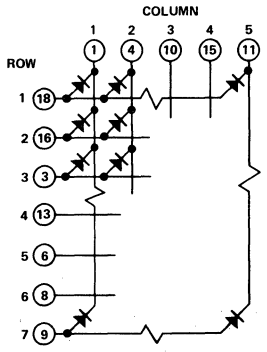


PIN	FUNCTION	
	HDSP-4401/-M101/ -4501/-5101	HDSP-4403/-M103/ -4503/-5103
1	COLUMN 1 CATHODE	ROW 1 CATHODE
2	NO PIN	NO PIN
3	ROW 3 ANODE	COLUMN 3 ANODE
4	COLUMN 2 CATHODE	ROW 3 CATHODE
5	NO PIN	NO PIN
6	ROW 5 ANODE	COLUMN 1 ANODE
7	NO PIN	NO PIN
8	ROW 6 ANODE	COLUMN 2 ANODE
9	ROW 7 ANODE	ROW 7 CATHODE
10	COLUMN 3 CATHODE	ROW 6 CATHODE
11	COLUMN 5 CATHODE	COLUMN 4 ANODE
12	NO PIN	NO PIN
13	ROW 4 ANODE	ROW 5 CATHODE
14	NO PIN	NO PIN
15	COLUMN 4 CATHODE	ROW 4 CATHODE
16	ROW 2 ANODE	ROW 2 CATHODE
17	NO PIN	NO PIN
18	ROW 1 ANODE	COLUMN 5 ANODE

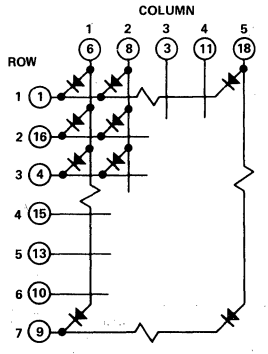
NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. A BLACK DOT ON SCRAMBLER SIDE INDICATES PIN #1.
4. FOR GREEN ONLY.

Internal Circuit Diagrams

HDSP-4401/M101/4501/5101
COMMON ANODE ROW

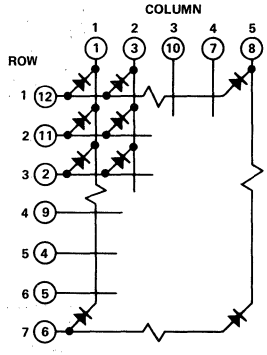


HDSP-4403/M103/4503/5103
COMMON CATHODE ROW

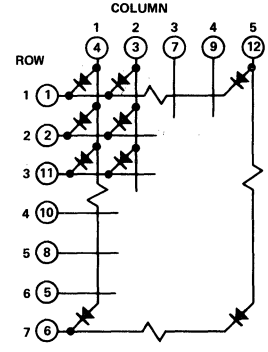


X = ROW OR COLUMN NUMBER, (X) = PIN NUMBER

HDSP-4701/L101/L201/5401
COMMON ANODE ROW



HDSP-4703/L103/L203/5403
COMMON CATHODE ROW



X = ROW OR COLUMN NUMBER, (X) = PIN NUMBER

Absolute Maximum Ratings at 25°C

Description	HDSP-470X/ 440X Series	HDSP-L10X/ M10X Series	HDSP-L20X/ 450X Series	HDSP-540X/ 510X Series
Average Power per Dot (T_A = 25°C)[1]	75 mW			
Peak Forward Current per Dot (T_A = 25°C)[1,2]	125 mA	125 mA	90 mA	90 mA
Average Forward Current per Dot (T_A = 25°C)[1,3]	32 mA	23 mA	15 mA	15 mA
Operating Temperature Range	-40°C to +85°C	-20°C to +85°C	-40°C to +85°C	-20°C to +85°C
Storage Temperature Range	-40°C to +85°C			
Lead Solder Temperature (1.59 mm [0.062 in.] below seating plane)	260°C for 3 s			

Notes:
1. Average power is based on 20 dots per character. Total package power dissipation should not exceed 1.5 W.
2. Do not exceed maximum average current per dot.
3. For the HDSP-440X/470X series displays, derate maximum average current above 35°C at 0.43 mA/°C. For the HDSP-L10X/M10X series displays, derate maximum average current above 35°C at 0.31 mA/°C. For the HDSP-L20X/450X series and HDSP-540X/510X series displays, derate maximum average current above 35°C at 0.2 mA/°C. This derating is based on a device mounted in a socket having a thermal resistance junction to ambient of 50°C/W per package.

Electrical/Optical Characteristics at $T_A = 25°C$

Standard Red HDSP-440X/470X Series

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Dot[4] (Digit Average)	I_V	100 mA pk: 1 of 5 Duty Factor (20 mA Avg.)				
HDSP-470X (17.3 mm)			360	770		µcd
HDSP-440X (26.5 mm)			400	800		
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[5]	λ_d			640		nm
Forward Voltage	V_F	$I_F = 100$ mA		1.8	2.2	V
Reverse Voltage[6]	V_R	$I_R = 100$ µA	3.0	12		V
Temperature Coefficient of V_F	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin per package						
HDSP-470X	$R\theta_{J\text{-}PIN}$			15		°C/W/
HDSP-440X				13		PACK

AlGaAs Red HDSP-L10X/M10X Series

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Dot[4] (Digit Average)	I_V	10 mA pk: 1 of 5 Duty Factor (2 mA Avg.)				
HDSP-L10X (17.3 mm)			730	1650		µcd
HDSP-M10X (26.5 mm)			760	1850		
Luminous Intensity/Dot[4] (Digit Average)	I_V	30 mA pk: 1 of 14 Duty Factor (2.1 mA Avg.)				
HDSP-L10X				1750		µcd
HDSP-M10X				1980		
Peak Wavelength	λ_{PEAK}			645		nm
Dominant Wavelength[5]	λ_d			637		nm
Forward Voltage	V_F	$I_F = 10$ mA		1.7	2.1	V
Reverse Voltage[6]	V_R	$I_R = 100$ µA	3.0	15.0		V
Temperature Coefficient of V_F	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin per package						
HDSP-L10X	$R\theta_{J\text{-}PIN}$			20		°C/W/
HDSP-M10X				18		PACK

High Efficiency Red HDSP-450X/L20X Series

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Dot[4] (Digit Average)	I_V	50 mA pk: 1 of 5 Duty Factor (10 mA Avg.)				
HDSP-L20X (17.3 mm)			1150	2800		µcd
HDSP-450X (26.5 mm)			1400	3500		
Luminous Intensity/Dot[4] (Digit Average)	I_V	30 mA pk: 1 of 14 Duty Factor (2.1 mA Avg.)				
HDSP-L20X				740		µcd
HDSP-450X				930		
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[5]	λ_d			626		nm
Forward Voltage	V_F	I_F = 50 mA		2.6	3.5	V
Reverse Voltage[6]	V_R	I_R = 100 µA	3.0	25.0		V
Temperature Coefficient of V_F	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin per package						
HDSP-L20X	$R\theta_{J\text{-}PIN}$			15		°C/W/
HDSP-450X				13		PACK

High Performance Green HDSP-540X/510X Series

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Dot[4] (Digit Average)	I_V	50 mA pk: 1 of 5 Duty Factor (10 mA Avg.)				
HDSP-540X (17.3 mm)			860	2700		µcd
HDSP-510X (26.5 mm)			1000	3100		
Luminous Intensity/Dot[4] (Digit Average)	I_V	30 mA pk: 1 of 14 Duty Factor (2.1 mA Avg.)				
HDSP-540X				570		µcd
HDSP-510X				630		
Peak Wavelength	λ_{PEAK}			566		nm
Dominant Wavelength[5,7]	λ_d			571		nm
Forward Voltage	V_F	I_F = 50 mA		2.6	3.5	V
Reverse Voltage[6]	V_R	I_R = 100 µA	3.0	25.0		V
Temperature Coefficient of V_F	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin per package						
HDSP-540X	$R\theta_{J\text{-}PIN}$			15		°C/W/
HDSP-510X				13		PACK

Notes:

4. The displays are categorized for luminous intensity with the intensity category designated by a letter on the left hand side of the package. The luminous intensity minimum and categories are determined by computing the numerical average of the individual dot intensities.
5. The dominant wavelength is derived from the C.I.E. Chromaticity diagram and is that single wavelength which defines the color of the device.
6. Typical specification for reference only. Do not exceed absolute maximum ratings.
7. The displays are categorized for dominant wavelength with the category designated by a number adjacent to the intensity category letter.

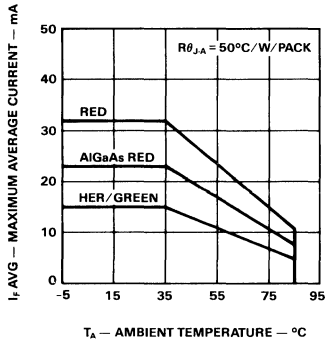


Figure 1. Maximum Allowable Average Current Per Dot as a Function of Ambient Temperature.

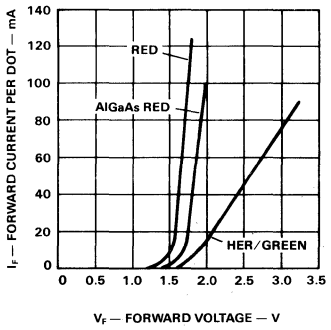


Figure 2. Forward Current vs. Forward Voltage.

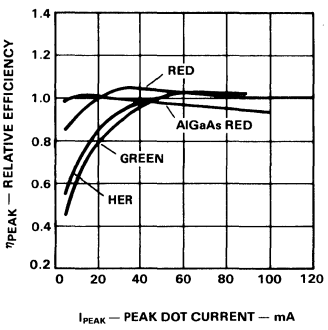


Figure 3. Relative Efficiency (Luminous Intensity per Unit Dot) vs. Peak Current per Dot.

Operational Considerations

Electrical Description

These display devices are composed of light emitting diodes, with the light from each LED optically stretched to form individual dots.

These display devices are well suited for strobed operation. The typical forward voltage values can be scaled from Figure 2. These values should be used to calculate the current limiting resistor value and the typical power dissipation. Expected maximum V_F values, for driver circuit design and maximum power dissipation, may be calculated using the following V_FMAX models:

Red (HDSP-440X/470X):
V_FMAX = 1.55 V + I_{Peak}(6.5Ω)
For $I_{Peak} \geq 5$ mA

AlGaAs Red (HDSP-L10X/M10X):
V_FMAX = 1.8 V + I_{Peak}(20Ω)
For $I_{Peak} \leq 20$ mA
V_FMAX = 2.0 V + I_{Peak}(10Ω)
For $I_{Peak} \geq 20$ mA

HER (HDSP-450X/L20X):
V_FMAX = 1.75 V + I_{Peak}(35Ω)
For $I_{Peak} \geq 5$ mA

Green (HDSP-540X/510X):
V_FMAX = 1.75 V + I_{Peak}(38Ω)
For $I_{Peak} \geq 5$ mA

Figure 3 allows the designer to calculate the luminous intensity at different peak and average currents. The following equation calculates intensity at different peak and average currents:

I_VAVG = (I_FAVG/I_FAVG DATA SHEET)(η_{peak})(I_V DATA SHEET)

Where:
I_FAVG is the desired time averaged LED current.
I_FAVG DATA SHEET is the time averaged data sheet test current for I_VDATA SHEET.
η_{peak} is the relative efficiency at the peak current, scaled from Figure 3.
I_V DATA SHEET is the time averaged data sheet luminous intensity, resulting from I_FAVG DATA SHEET.
I_VAVG is the calculated time averaged luminous intensity resulting from I_FAVG.

For example, what is the luminous intensity of an AlGaAs Red (HDSP-L10X) driven at 50 mA peak 1/5 duty factor?

I_FAVG = 50 mA * 0.2 = 10 mA
I_FAVG DATA SHEET = 2 mA
η_{peak} = 0.98
I_V DATA SHEET = 1650 µcd

Therefore

I_VAVG = (10 mA/2 mA)(0.98) (1650 µcd) = 8085 µcd

Circuit Design

Smart IC Circuit

HDSP-L203/4503 displays can be ordered with a smart IC driver. Information about the IC is available in the HDSP-211X data sheet. For ordering information see the HP Smart Displays Sets data sheet. Contact your HP field sales engineer or an authorized HP distributor for information about ordering this IC with the other parts.

Figure 4 shows how to connect one IC to drive eight 5 x 7 displays.

Coded Data Controller

Figure 5 shows a circuit designed to display eight characters of ASCII text. ASCII coded data is stored in a local 128 x 8 RAM. After the microprocessor has loaded the RAM, this circuit provides all the necessary signals to decode and display eight characters. With minor modifications the circuit can drive up to 128 display characters. The RAM used in this circuit is an MCM6810P with the address and data inputs isolated with tristate buffers. This allows the RAM to be accessed either by the microprocessor or by the local scanning electronics. The protocol is arranged such that the microprocessor always takes precedence over the local scanning electronics.

The Motorola 6810 RAM stores 8 bytes of ASCII data which is continuously read, decoded, and displayed. The ASCII data from the RAM is decoded by the Motorola 6674 128 ASCII character decoder. The 6674 decoder has five column outputs which are gated to the Sprague UCN5832A 32-bit shift register data input via a 74LS151 multiplexer. Strobing of the display is accomplished via the 74LS90, 74LS393, and 74LS197 counter string.

The 74LS197 is used as a divide by 7 counter. Output Q_D resets the counter, sets output Q_A to logic 1, and sets outputs Q_B, Q_C, and Q_D to logic 0. 74LS197 outputs Q_A, Q_B, and Q_C synchronize the row drivers and the row data entry into the shift register. Row drivers are sequentially turned on and off so only one row driver is on at a given time.

The 74LS393 counter is used as a divide by 64 counter. This counter has two functions. The first is to provide the character address to be decoded. Outputs $1Q_A$, $1Q_B$, and $1Q_C$ supply the address to the RAM. The second is to generate a control signal. This signal simultaneously clocks the 74LS197 and disables the row drivers and shift register outputs. It also provides one of the logic signals needed to enable the system clock to clock data into the shift register. Outputs $1Q_D$, $2Q_A$, and $2Q_B$ are gated to create this signal. The clock is enabled for 1 count and disabled for 7 counts. Thus, the overall display duty factor is (7/8)(1/7) = 12.5%.

The 74LS90 is connected as a divide by 5 cascaded into a divide by 2 for an effective divide by 10 counter. Outputs Q_B, Q_C, and Q_D are used to convert the parallel output from the character generator to serial input for entry into the UCN5832 shift register. Output Q_A in combination with the system clock and the gated 74LS393 counter outputs clock data into the shift register. When character data is loaded into the shift register, output Q_A alternates between allowing data to be loaded and providing enough time for data to propagate from the 74LS393 counter through the tristate buffers, RAM, character generator, and multiplexer.

This circuit can be used with the HDSP-4701 by changing the display pin assignments. HDSP-4X03 and HDSP-5X03 devices require a change of both the shift register and drive transistors. The shift register can be changed to a Sprague

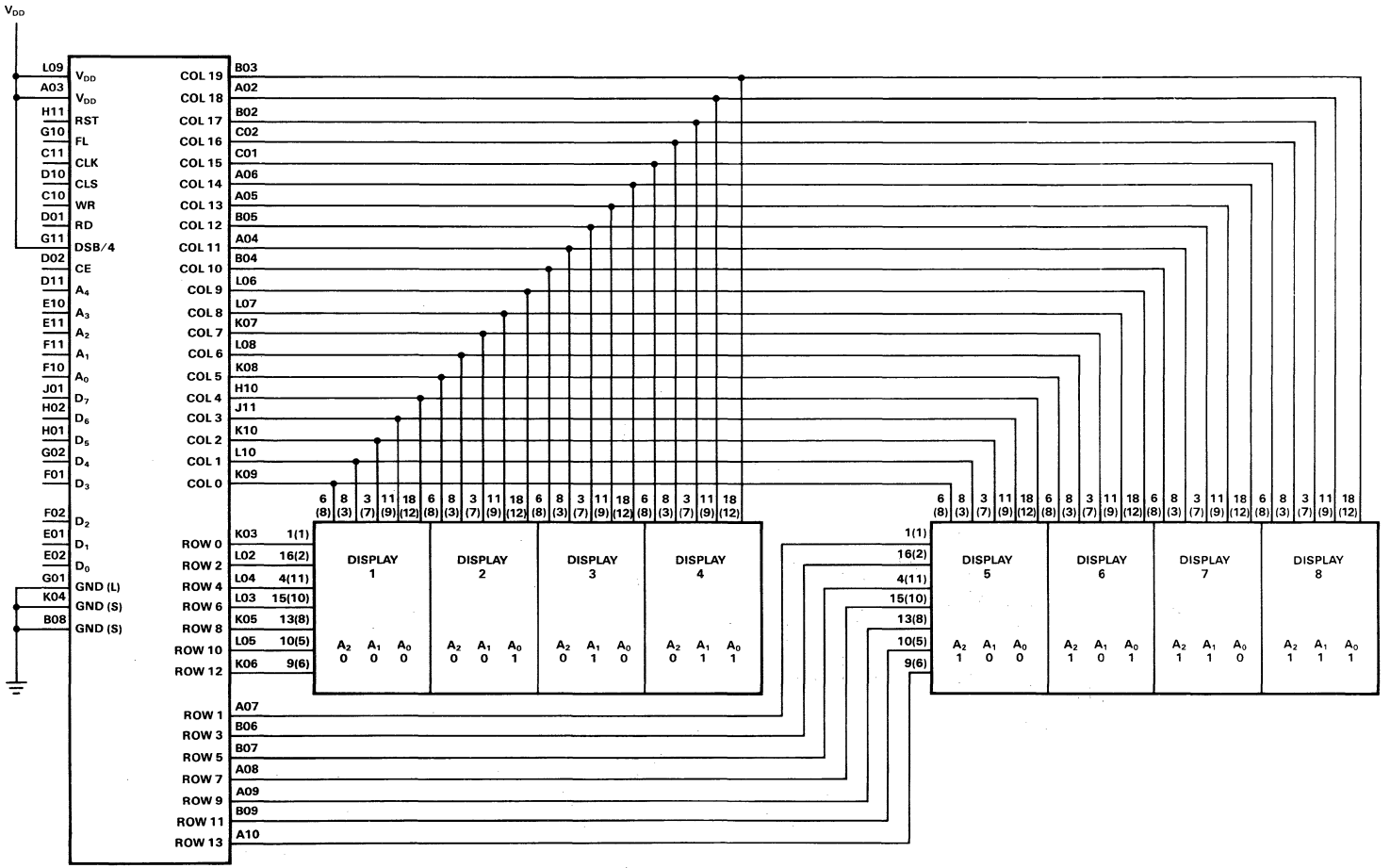


Figure 4. Low Current Circuit to Refresh Eight 5 x 7 Displays. HDSP-4503 (HDSP-L203) Display Pin Numbers Are Denoted as XX(XX).

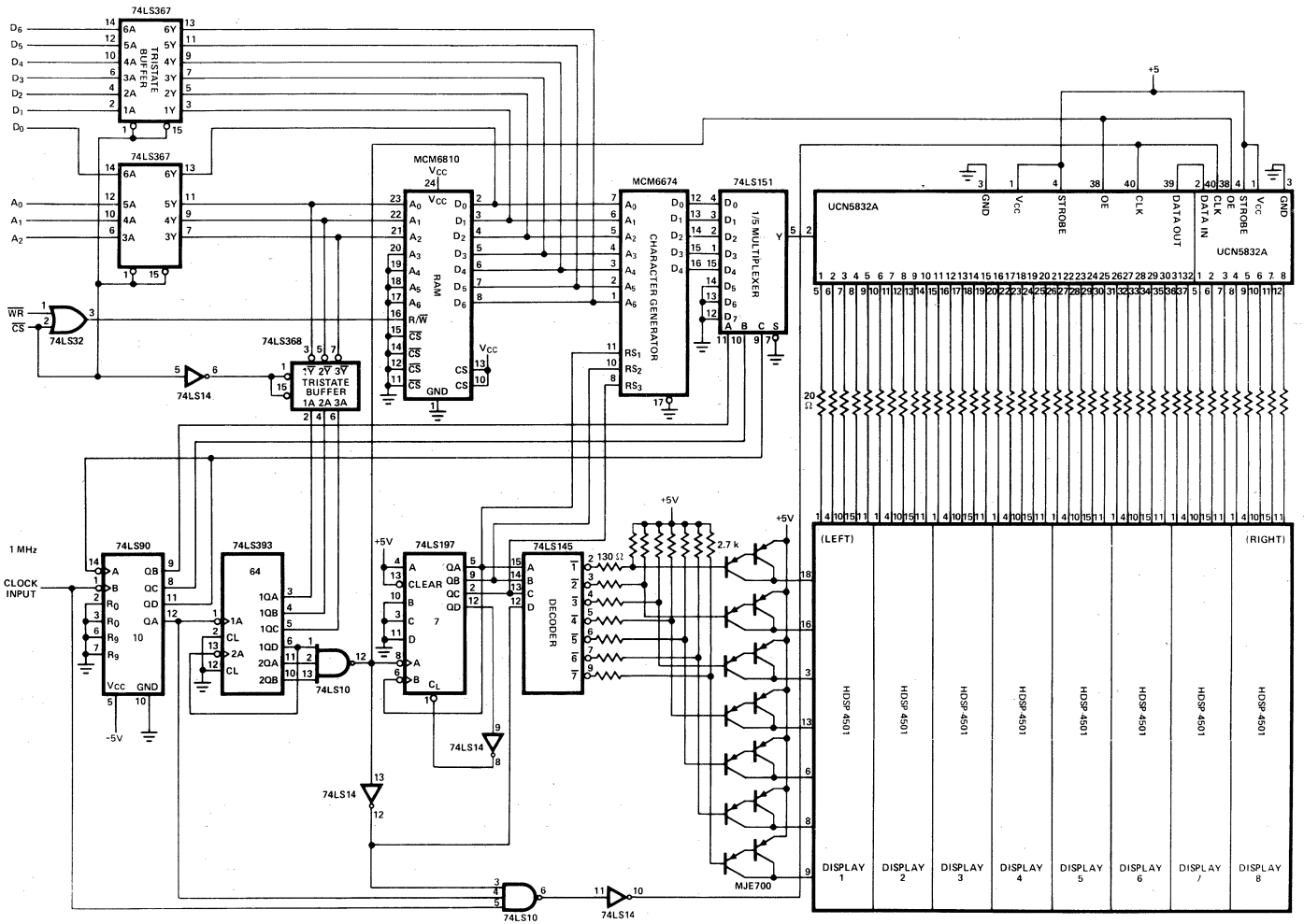


Figure 5. Coded Data Controller Circuit.

UCN-5818. This part has different pin assignments than the UCN-5832. For further details consult the Sprague data sheet. The MJE700 Darlington transistors need to be replaced with suitable npn Darlington transistors.

Thermal Considerations

The device thermal resistance may be used to calculate the junction temperature of the central LED. The equation below calculates the junction temperature of the central (hottest) LED.

$$T_J = T_A + (P_D)(R\theta_{J\text{-}A})(N)$$
$$P_D = (V_F MAX)(I_F AVG)$$
$$R\theta_{J\text{-}A} = R\theta_{J\text{-}PIN} + R\theta_{PIN\text{-}A}$$

T_J is the junction temperature of the central LED.
T_A is the ambient temperature.
P_D is the power dissipated by one LED.
N is the number of LEDs ON per character.
$V_F MAX$ is calculated using the appropriate V_F model.
$R\theta_{J\text{-}A}$ is the package thermal resistance from the central LED to the ambient.
$R\theta_{J\text{-}PIN}$ is the package thermal resistance from the central LED to pin.
$R\theta_{PIN\text{-}A}$ is the package thermal resistance from the pin to the ambient.

For example, what is the maximum ambient temperature an HDSP-L10X can operate with the following conditions:

I_{PEAK} = 125 mA
$I_F AVG$ = 10 mA
$R\theta_{J\text{-}A}$ = 50°C/W
N = 35
$T_J MAX$ = 110°C
$V_F MAX$ = 2.0 V + (0.125 A)(10)
= 3.25 V
P_D = (3.25 V)(0.01 A)
= 0.0325 W
T_A = 110°C –
(50°C/W)(0.0325 W)(35)
= 53°C

The maximum number of dots ON for the ASCII character set is 20. What is the maximum ambient temperature an HDSP-L10X can operate with the following conditions:

I_{PEAK} = 125 mA
$I_F AVG$ = 10 mA
$R\theta_{J\text{-}A}$ = 50°C/W
N = 20
$T_J MAX$ = 110°C

$V_F MAX$ = 3.25 V
P_D = 0.0325 W
T_A = 110°C –
(50°C/W)(0.0325 W)(20)
= 77°C

Therefore, the maximum ambient temperature can be increased by reducing the average number of dots ON from 35 to 20 dots ON per display.

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance the readability. This is accomplished by having the OFF dots blend into the display background and the ON dots stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the dots.

Contrast enhancement may be achieved by using one of the following suggested filters:

HDSP-440X/470X/L10X/M10X
Panelgraphic RUBY RED 60
SGL-HOMALITE H100-1605 RED
3M Louvered Filter R6610 RED OR N0210 GRAY

HDSP-450X/L20X
Panelgraphic SCARLET RED 65
SGL-Homalite H100-1670 RED or H100-1250 GRAY
3M Louvered Filter R6310 RED or N0210 GRAY

HDSP-540X/510X
Panelgraphic GREEN 48
SGL-Homalite H100-1440 GREEN or H100-1250 GRAY
3M Louvered Filter YG5610 GREEN or N0210 GRAY

For further information on contrast enhancement please see Application Note 1015.

For further information on soldering LEDs please refer to Application Note 1027.

HEWLETT PACKARD

Low Current Seven Segment Displays

Technical Data

HDSP-3350, 3351, 3353, 3356
HDSP-5551, 5553, 5557, 5558
HDSP-7511, 7513, 7517, 7518
HDSP-A101, A103, A107, A108
HDSP-A801, A803, A807, A808
HDSP-A901, A903, A907, A908
HDSP-E100, E101, E103, E106
HDSP-F101, F103, F107, F108
HDSP-H101, H103, H107, H108
HDSP-K121, K123
HDSP-N100, N101, N103, N105, N106

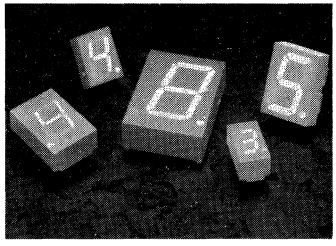
Features

- **Low Power Consumption**
- **Industry Standard Size**
- **Industry Standard Pinout**
- **Choice of Character Size**
  7.6 mm (0.30 in), 10 mm (0.40 in), 10.9 mm (0.43 in), 14.2 mm (0.56 in), 20 mm (0.8 in)
- **Choice of Colors**
  AlGaAs Red, High Efficiency Red (HER), Yellow, Green
- **Excellent Appearance**
  Evenly Lighted Segments
  ±50° Viewing Angle
- **Design Flexibility**
  Common Anode or Common Cathode
  Single and Dual Digits
  Left and Right Hand Decimal Points
  ±1. Overflow Character
- **Categorized for Luminous Intensity**
  Yellow and Green Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **Excellent for Long Digit String Multiplexing**

Description

These low current seven segment displays are designed for applications requiring low power consumption. They are tested and selected for their excellent low current characteristics to ensure that the segments are matched at low currents. Drive currents as low as 1 mA per segment are available.

Pin for pin equivalent displays are also available in a standard current or high light ambient design. The standard current displays are available in all colors and are ideal for most applications. The high light ambient displays are ideal for sunlight ambients or long string lengths. For additional information see the 7.6 mm Micro Bright Seven Segment Displays, 10 mm Seven Segment Displays, 7.6 mm/10.9 mm Seven Segment Displays, 14.2 mm Seven Segment Displays, 20 mm Seven Segment Displays, or High Light Ambient Seven Segment Displays data sheets.

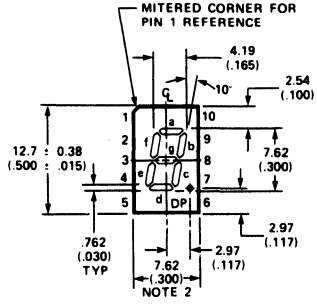


Devices

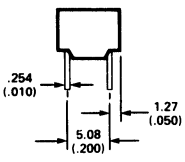
AlGaAs HDSP-	HER HDSP-	Yellow HDSP-	Green HDSP-	Description	Package Drawing
A101	7511	A801	A901	7.6 mm Common Anode Right Hand Decimal	A
A103	7513	A803	A903	7.6 mm Common Cathode Right Hand Decimal	B
A107	7517	A807	A907	7.6 mm Common Anode ±1. Overflow	C
A108	7518	A808	A908	7.6 mm Common Cathode ±1. Overflow	D
F101				10 mm Common Anode Right Hand Decimal	E
F103				10 mm Common Cathode Right Hand Decimal	F
F107				10 mm Common Anode ±1. Overflow	G
F108				10 mm Common Cathode ±1. Overflow	H
E100	3350			10.9 mm Common Anode Left Hand Decimal	I
E101	3351			10.9 mm Common Anode Right Hand Decimal	J
E103	3353			10.9 mm Common Cathode Right Hand Decimal	K
E106	3356			10.9 mm Universal ±1. Overflow[1]	L
H101	5551			14.2 mm Common Anode Right Hand Decimal	M
H103	5553			14.2 mm Common Cathode Right Hand Decimal	N
H107	5557			14.2 mm Common Anode ±1. Overflow	O
H108	5558			14.2 mm Common Cathode ±1. Overflow	P
K121				14.2 mm Two Digit Common Anode Right Hand Decimal	R
K123				14.2 mm Two Digit Common Cathode Right Hand Decimal	S
N100				20 mm Common Anode Left Hand Decimal	Q
N101				20 mm Common Anode Right Hand Decimal	T
N103				20 mm Common Cathode Right Hand Decimal	U
N105				20 mm Common Cathode Left Hand Decimal	V
N106				20 mm Universal ±1. Overflow[1]	W

Note:
1. Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagrams L or W.

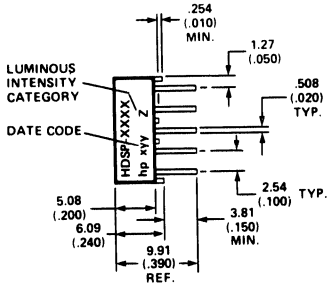
Package Dimensions

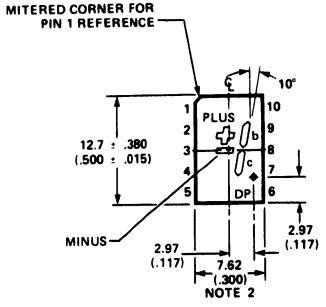


A, B



A, B, C, D



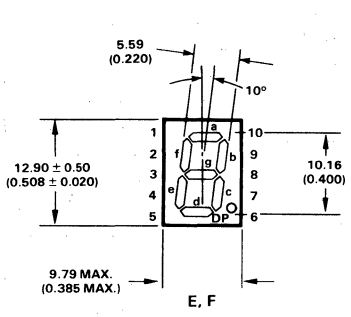


C, D

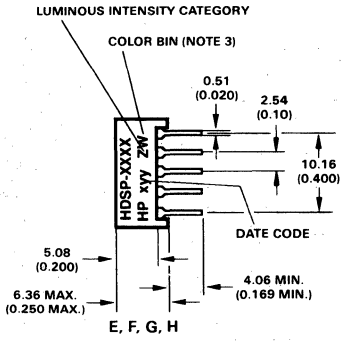
PIN	FUNCTION A	B	C	D
1	ANODE[4]	CATHODE[5]	ANODE[4]	CATHODE[5]
2	CATHODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	ANODE e	NC	NC
5	CATHODE d	ANODE d	NC	NC
6	ANODE[4]	CATHODE[5]	ANODE[4]	CATHODE[5]
7	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	ANODE a	NC	NC

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. MAXIMUM.
3. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
4. REDUNDANT ANODES.
5. REDUNDANT CATHODES.

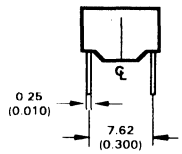
Package Dimensions (continued)



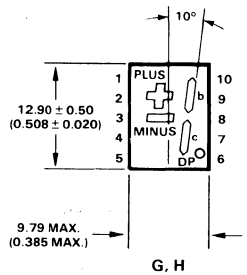
E, F



E, F, G, H



E, F, G, H



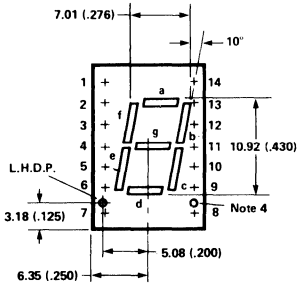
G, H

PIN	FUNCTION			
	E	F	G	H
1	ANODE[4]	CATHODE[5]	ANODE[4]	CATHODE[5]
2	CATHODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	ANODE e	NC	NC
5	CATHODE d	ANODE d	NC	NC
6	ANODE[4]	CATHODE[5]	ANODE[4]	CATHODE[5]
7	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	ANODE a	NC	NC

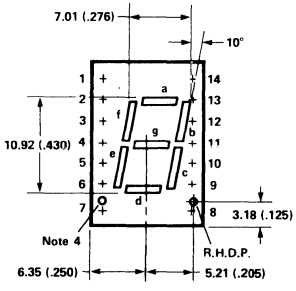
NOTES:

1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. FOR YELLOW AND GREEN SERIES PRODUCT ONLY.
4. REDUNDANT ANODES.
5. REDUNDANT CATHODES.

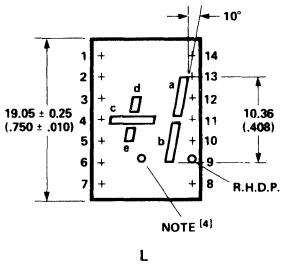
Package Dimensions (continued)



I

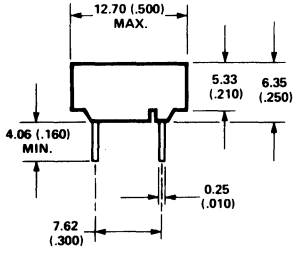


J, K

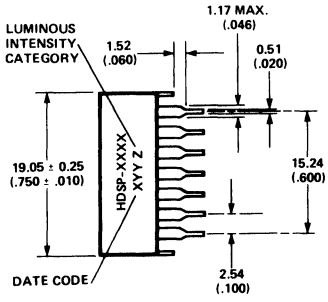


L

FRONT VIEW



END VIEW



SIDE VIEW

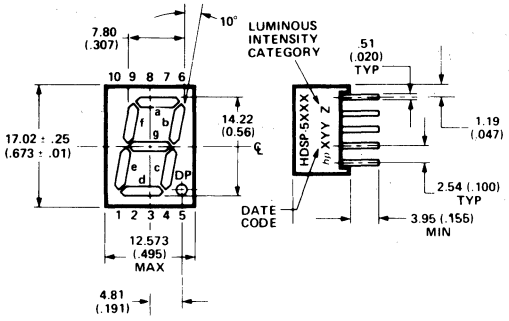
PIN	FUNCTION			
	I	J	K	L
1	CATHODE-a	CATHODE-a	ANODE-a	CATHODE-d
2	CATHODE-f	CATHODE-f	ANODE-f	ANODE-d
3	ANODE[3]	ANODE[3]	CATHODE[6]	NO PIN
4	NO PIN	NO PIN	NO PIN	CATHODE-c
5	NO PIN	NO PIN	NO PIN	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	NO CONN.[5]	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-e	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-d	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	ANODE-dp	CATHODE-dp
10	CATHODE-c	CATHODE-c	ANODE-c	CATHODE-b
11	CATHODE-g	CATHODE-g	ANODE-g	CATHODE-a
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE-b	CATHODE-b	ANODE-b	ANODE-a
14	ANODE[3]	ANODE[3]	CATHODE[6]	ANODE-b

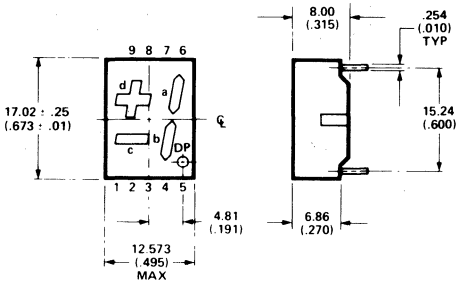
NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. REDUNDANT ANODES.
4. UNUSED dp POSITION.
5. SEE INTERNAL CIRCUIT DIAGRAM.
6. REDUNDANT CATHODES.
7. SEE PART NUMBER TABLE FOR L.H.D.P. AND R.H.D.P. DESIGNATION.

Package Dimensions (continued)

FRONT VIEW M, N

TOP END VIEW M, N, O, P





FRONT VIEW O, P

SIDE VIEW M, N, O, P

PIN	FUNCTION			
	M	N	O	P
1	CATHODE e	ANODE e	CATHODE c	ANODE c
2	CATHODE d	ANODE d	ANODE c, d	CATHODE c, d
3	ANODE [4]	CATHODE [5]	CATHODE b	ANODE b
4	CATHODE c	ANODE c	ANODE a, b, DP	CATHODE a, b, DP
5	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
6	CATHODE b	ANODE b	CATHODE a	ANODE a
7	CATHODE a	ANODE a	ANODE a, b, DP	CATHODE a, b, DP
8	ANODE [4]	CATHODE [5]	ANODE c, d	CATHODE c, d
9	CATHODE f	ANODE f	CATHODE d	ANODE d
10	CATHODE g	ANODE g	NO PIN	NO PIN

NOTES:

1. ALL DIMENSIONS IN MILLIMETRES (INCHES).

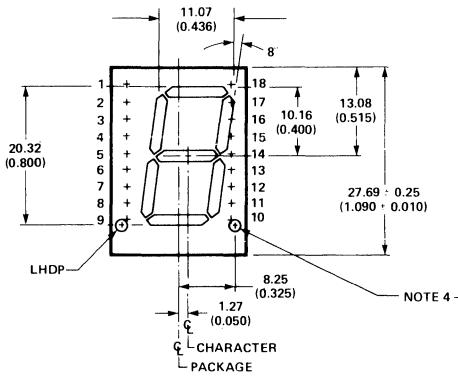
2. MAXIMUM.

3. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.

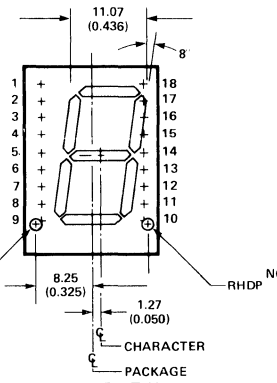
4. REDUNDANT ANODES.

5. REDUNDANT CATHODES.

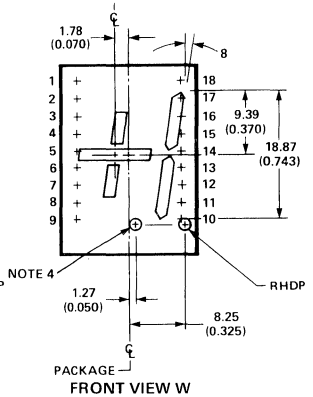
Package Dimensions (continued)



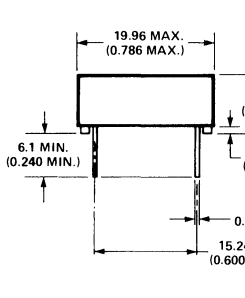
FRONT VIEW Q, V



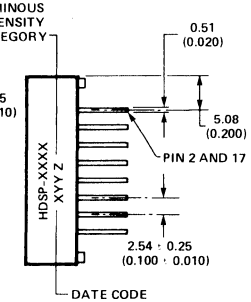
FRONT VIEW T, U



FRONT VIEW W



END VIEW Q, T, U, V, W



SIDE VIEW Q, T, U, V, W

Pin	Function				
	Q	T	U	V	W
1	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
2	CATHODE a	CATHODE a	ANODE a	ANODE a	CATHODE a
3	CATHODE f	CATHODE f	ANODE f	ANODE f	ANODE d
4	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE d
5	CATHODE e	CATHODE e	ANODE e	ANODE e	CATHODE c
6	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE e
7	CATHODE dp	NO. CONNEC.	NO. CONNEC.	ANODE dp	ANODE e
8	NO PIN	NO PIN	NO PIN	NO PIN	CATHODE dp
9	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
10	NO PIN	CATHODE dp	ANODE dp	NO PIN	ANODE dp
11	CATHODE d	CATHODE d	ANODE d	ANODE d	CATHODE dp
12	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE b
13	CATHODE c	CATHODE c	ANODE c	ANODE c	ANODE b
14	CATHODE g	CATHODE g	ANODE g	ANODE g	ANODE c
15	CATHODE b	CATHODE b	ANODE b	ANODE b	ANODE a
16	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
17	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE a
18	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN

NOTES:

1. ALL DIMENSIONS IN MILLIMETRES (INCHES).

2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.

3. REDUNDANT ANODES.

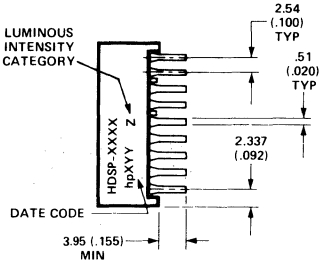
4. UNUSED dp POSITION.

5. SEE INTERNAL CIRCUIT DIAGRAM.

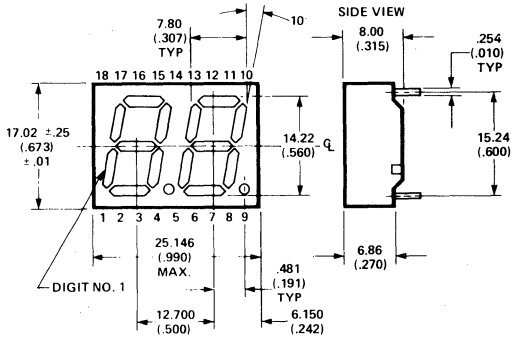
6. REDUNDANT CATHODES.

7. SEE PART NUMBER TABLE FOR L.H.D.P. AND R.H.D.P. DESIGNATION.

Package Dimensions (continued)



TOP END VIEW R, S

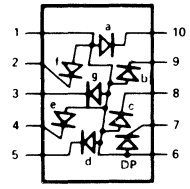


FRONT VIEW R, S

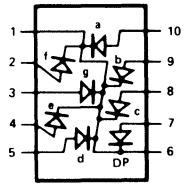
Pin	Function	
	R	S
1	E CATHODE NO. 1	E ANODE NO. 1
2	D CATHODE NO. 1	D ANODE NO. 1
3	C CATHODE NO. 1	C ANODE NO. 1
4	DP CATHODE NO. 1	DP ANODE NO. 1
5	E CATHODE NO. 2	E ANODE NO. 2
6	D CATHODE NO. 2	D ANODE NO. 2
7	G CATHODE NO. 2	G ANODE NO. 2
8	C CATHODE NO. 2	C ANODE NO. 2
9	DP CATHODE NO. 2	DP ANODE NO. 2
10	B CATHODE NO. 2	B ANODE NO. 2
11	A CATHODE NO. 2	A ANODE NO .2
12	F CATHODE NO. 2	F ANODE NO. 2
13	DIGIT NO. 2 ANODE	DIGIT NO. 2 CATHODE
14	DIGIT NO. 1 ANODE	DIGIT NO. 1 CATHODE
15	B CATHODE NO. 1	B ANODE NO. 1
16	A CATHODE NO. 1	A ANODE NO. 1
17	G CATHODE NO. 1	G ANODE NO. 1
18	F CATHODE NO. 1	F ANODE NO. 1

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.

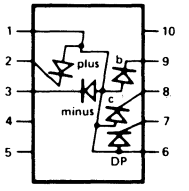
Internal Circuit Diagram



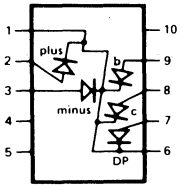
A, E



B, F

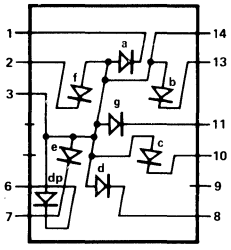


C, G



D, H

Internal Circuit Diagram (continued)



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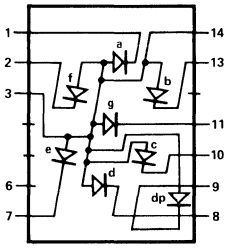

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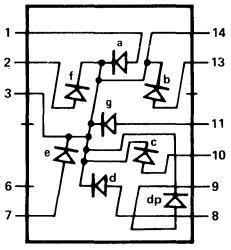

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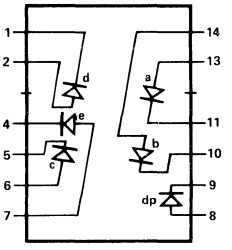

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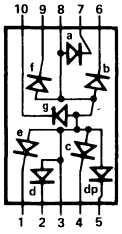

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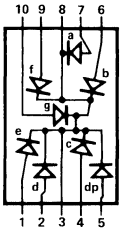

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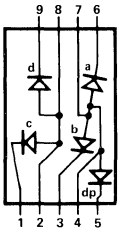

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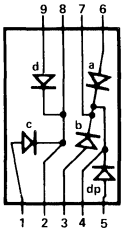

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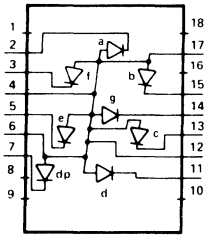

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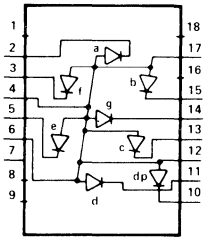

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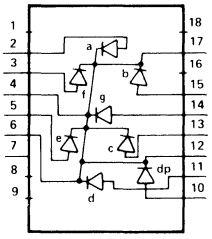

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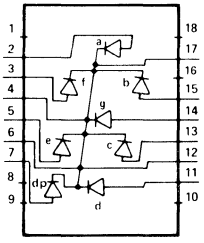

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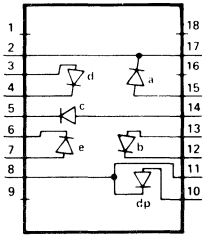
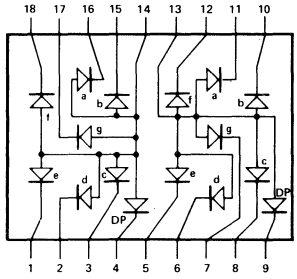
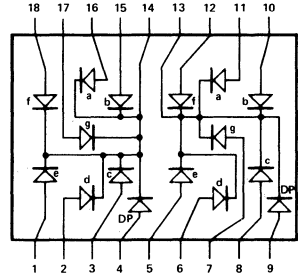


W

Internal Circuit Diagram (continued)





Absolute Maximum Ratings

Description	AlGaAs Red HDSP-A101/E100/ H101/K120/N100 Series	HER HDSP-751X/ 335X/555X Series	Yellow HDSP-A801 Series	Green HDSP-A901 Series	Units
Average Power per Segment or DP	37	52		64	mW
Peak Forward Current per Segment or DP	45				mA
DC Forward Current per Segment or DP	15[1]	15[2]			mA
Operating Temperature Range	-20 to +100	-40 to +100			°C
Storage Temperature Range	-55 to +100				°C
Reverse Voltage per Segment or DP	3.0				V
Lead Solder Temperature for 3 Seconds (1.59 mm [0.63 in.] below seating plane)	260				°C

Notes:
1. Derate above 91°C at 0.53 mA/°C.
2. Derate HER/Yellow above 80°C at 0.38 mA/°C and Green above 71°C at 0.31 mA/°C.

Electrical/Optical Characteristics at T_A = 25°C

AlGaAs Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A101	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	315	600		µcd	I_F = 1 mA
				3600			I_F = 5 mA
F101			330	650			I_F = 1 mA
				3900			I_F = 5 mA
E100			390	650			I_F = 1 mA
				3900			I_F = 5 mA
H101, K121			400	700			I_F = 1 mA
				4200			I_F = 5 mA
N100			270	590			I_F = 1 mA
				3500			I_F = 5 mA
All Devices	Forward Voltage/Segment or DP	V_F		1.6		V	I_F = 1 mA
				1.7			I_F = 5 mA
				1.8	2.2		I_F = 20 mA Pk
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2 mV		mV/°C	
A101	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		255		°C/W/Seg	
F101				320			
E100				340			
H101, K121				400			
N100				430			

High Efficiency Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
7511	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	160	270		µcd	I_F = 2 mA
				1050			I_F = 5 mA
3350, 5551			200	300			I_F = 2 mA
				1200			I_F = 5 mA
			270	370			I_F = 2 mA
				1480			I_F = 5 mA
All Devices	Forward Voltage/Segment or DP	V_F		1.6		V	I_F = 2 mA
				1.7			I_F = 5 mA
				2.1	2.5		I_F = 20 mA Pk
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
7511	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W	
3350				280			
5551				345			

Yellow

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A801	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	250	420		µcd	I_F = 4 mA
				1300			I_F = 10 mA
	Forward Voltage/Segment or DP	V_F		1.7		V	I_F = 4 mA
				1.8			I_F = 5 mA
				2.1	2.5		I_F = 20 mA Pk
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,5]	λ_d	581.5	585	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W	

Green

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A901	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	250	475		µcd	I_F = 4 mA
				1500			I_F = 10 mA
	Forward Voltage/Segment or DP	V_F		1.9		V	I_F = 4 mA
				2.0			I_F = 10 mA
				2.1	2.5		I_F = 20 mA Pk
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,5]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W	

Notes:
1. Device case temperature is 25°C prior to the intensity measurement.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is the single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. The yellow (HDSP-A800) and Green (HDSP-A900) displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

AlGaAs Red

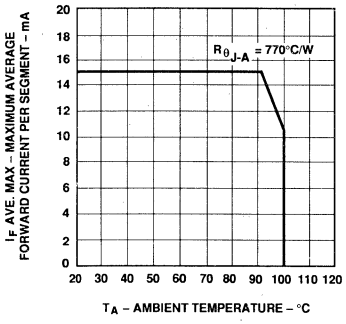


Figure 1. Maximum Allowable Average or DC Current vs. Ambient Temperature.

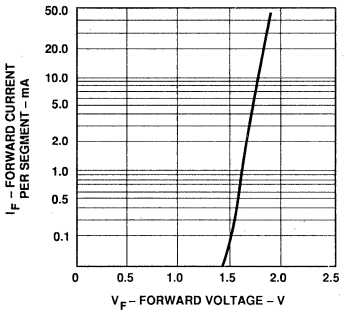


Figure 2. Forward Current vs. Forward Voltage.

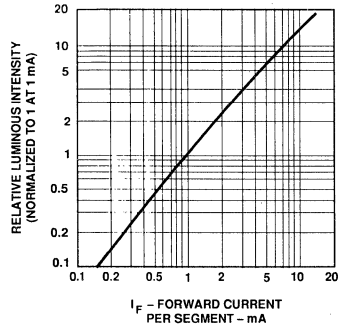


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

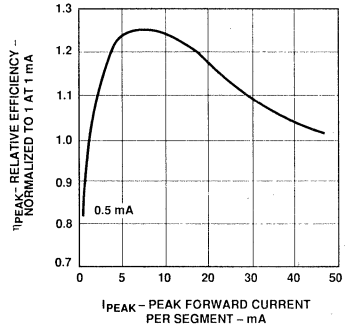


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Yellow, Green

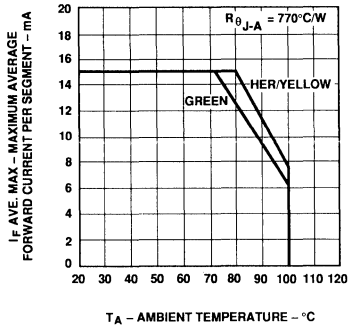


Figure 5. Maximum Allowable Average or DC Current vs. Ambient Temperature.

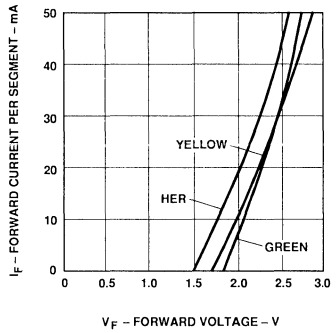


Figure 6. Forward Current vs. Forward Voltage.

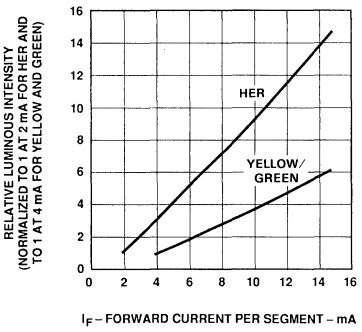


Figure 7. Relative Luminous Intensity vs. DC Forward Current.

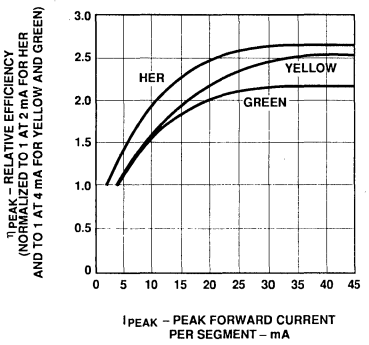


Figure 8. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Electrical/Optical

These displays use light emitting diodes, with the light from each LED optically stretched to form individual segments and decimal points. The AlGaAs Red HDSP-X100 series LEDs use double heterojunction AlGaAs on a GaAs substrate. HER HDSP-7510/3350/5550 and Yellow HDSP-A800 series LEDs have their p-n junctions diffused into a GaAsP epitaxial layer on a GaP substrate. The Green HDSP-A900 series LEDs use a liquid phase GaP epitaxial layer on GaP.

The typical forward voltage values can be scaled from Figures 2 and 6. These values should be used to calculate the current limiting resistor value and typical power consumption. Expected maximum V_F values for driver circuit design and maximum power dissipation, may be calculated using the following V_FMAX models:

AlGaAs Red HDSP-X100 series
V_FMAX = 1.8 V + I_{Peak} (20 Ω)
For: I_{Peak} ≤20 mA
V_FMAX = 2.0 V + I_{Peak} (10 Ω)
For: I_{Peak} ≥20 mA

HER (HDSP-7510/3350/5550) and Yellow (HDSP-A801) series
V_FMAX = 1.6 + I_{Peak} (45 Ω)
For: I_{Peak} ≤20 mA
V_FMAX = 1.75 + I_{Peak} (38 Ω)
For: I_{Peak} ≥20 mA

Green (HDSP-A901) series
V_FMAX = 2.0 V + I_{Peak} (50 Ω)
For: I_{Peak} ≥4 mA

Figures 4 and 8 allow the designer to calculate the luminous intensity at different peak and average currents. The following equation calculates intensity at different peak and average currents:

I_VAVG = (I_FAVG/I_FAVG DATA SHEET)(η_{peak})(I_VDATA SHEET)

Where:
I_VAVG is the desired time averaged luminous intensity resulting from I_FAVG.
I_FAVG is the desired time averaged LED current.
I_FAVG DATA SHEET is the data sheet test current for I_VDATA SHEET.
η_{peak} is the relative efficiency at the peak current, scaled from Figure 4 or 8.
I_V DATA SHEET is the data sheet luminous intensity, resulting from I_FAVG DATA SHEET.

For example, what is the luminous intensity of an HDSP-7511 driven at 20 mA peak 1/5 duty factor?

I_FAVG = (50 mA)(0.2) = 4 mA
I_FAVG DATA SHEET = 2 mA
η_{Peak} = 2.6
I_V DATA SHEET = 270 µcd

Therefore

I_VAVG = (4 mA/2 mA)(2.6)(270 µcd) = 1400 µcd

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance the readability. This is accomplished by having the OFF dots blend into the display background and the ON dots stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the dots.

Contrast enhancement may be achieved by using one of the following suggested filters:

AlGaAs Red (HDSP-X100)
Panelgraphic RUBY RED 60
SGL-Homalite H100-1605 RED or H100-1250 GRAY
3M Louvered Filter R6310 RED or ND0220 GRAY

HER (HDSP-7510/3550/5550)
Panelgraphic SCARLET RED 65
SGL-Homalite H100-1670 RED or H100-1250 GRAY
3M Louvered Filter R6310 RED or ND0220 GRAY

Yellow (HDSP-A801)
Panelgraphic YELLOW 27 or GRAY 10
SGL-Homalite H100-1720 AMBER or H100-1250 GRAY
3M Louvered Filter ND0220 GRAY

Green (HDSP-A901)
Panelgraphic GREEN 48
SGL-Homalite H100-1440 GREEN or H100-1250 GRAY
3M Louvered Filter ND0220 GRAY

For further information on contrast enhancement please see Application Note 1015.

Mechanical

Specifically developed plastics are used to optimize the displays optical performance. These plastics restrict the solvents that may be used for cleaning. Only mixtures of Freon (F113) and alcohol should be used for vapor cleaning processes. Total immersion time

in the vapors is two minutes. Some suggested mixtures are Freon TE, Arklone A or K, or Genesolv DI-15 or DE-15. A 60°C (140°F) water cleaning process may also be used. This process includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a water rinse, and a thorough air dry. Room temperature cleaning may be done with Freon T-E35 or T-P35, Ethanol, Isopropanol, or water with a mild detergent.

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

HEWLETT PACKARD

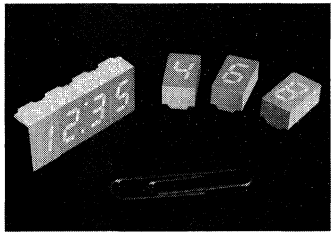
7.6 mm (0.3 inch) Micro Bright Seven Segment Displays

Technical Data

HDSP-7301, 7311, 7302, 7303, 7313, 7304, 7307, 7317, 7308, 7318
HDSP-A151, A153, A157, A158
HDSP-7501, 7502, 7503, 7504, 7507, 7508
HDSP-7401, 7402, 7403, 7404, 7407, 7408
HDSP-7801, 7802, 7803, 7804, 7807, 7808

Features

- **Available with Colon for Clock Display**
- **Compact Package**
  0.300 x 0.500 inches
  Leads on 2.54 mm (0.1 inch) Centers
- **Choice of Colors**
  Red, AlGaAs Red, High Efficiency Red, Yellow, Green
- **Excellent Appearance**
  Evenly Lighted Segments
  Mitered Corners on Segments
  Gray Package Gives Optimum Contrast
  ±50° Viewing Angle
- **Design Flexibility**
  Common Anode or Common Cathode
  Right Hand Decimal Point
  ±1. Overflow Character
- **Categorized for Luminous Intensity**
  Yellow and Green
  Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **High Light Output**
- **High Peak Current**
- **Excellent for Long Digit String Multiplexing**
- **Intensity and Color Selection Available**
  See Intensity and Color Selected Displays Data Sheet
- **Sunlight Viewable AlGaAs**



Description

The 7.6 mm (0.3 inch) LED seven segment displays are designed for viewing distances up to 3 metres (10 feet). These devices use an industry standard size package and

Devices

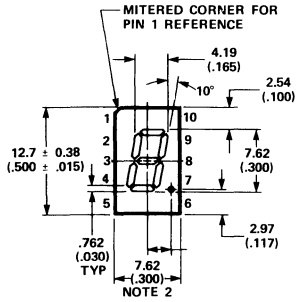
Red HDSP-	AlGaAs[1] HDSP-	HER[1] HDSP-	Yellow[1] HDSP-	Green[1] HDSP-	Description	Package Drawing
7301 7311	A151	7501	7401	7801	Common Anode Right Hand Decimal	A
7302		7502	7402	7802	Common Anode Right Hand Decimal, Colon	B
7303 7313	A153	7503	7403	7803	Common Cathode Right Hand Decimal	C
7304		7504	7404	7804	Common Cathode Right Hand Decimal, Colon	D
7307 7317	A157	7507	7407	7807	Common Anode ±1. Overflow	E
7308 7318	A158	7508	7408	7808	Common Cathode ±1. Overflow	F

Note:
1. These displays are recommended for high ambient light operation. Please refer to the HDSP-A10X AlGaAs, HDSP-335X HER, HDSP-A80X Yellow, and HDSP-A90X Green data sheet for low current operation.

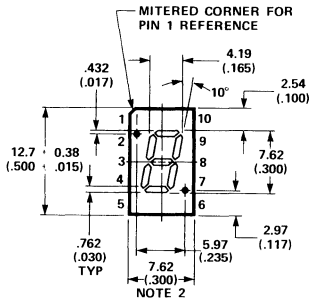
pinout. Both the numeric and ±1. overflow devices feature a right hand decimal point. All devices are available as either common anode or common cathode.

These displays are ideal for most applications. Pin for pin equivalent displays are also available in a low current design. The low current displays are ideal for portable applications. For additional information see the Low Current Seven Segment Displays.

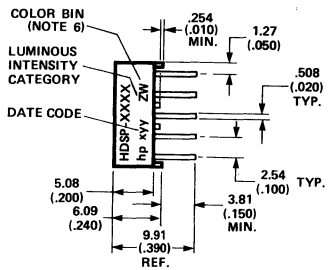
Package Dimensions

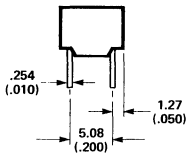


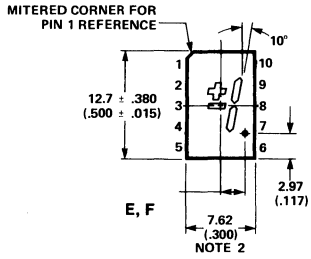
A, C



B, D





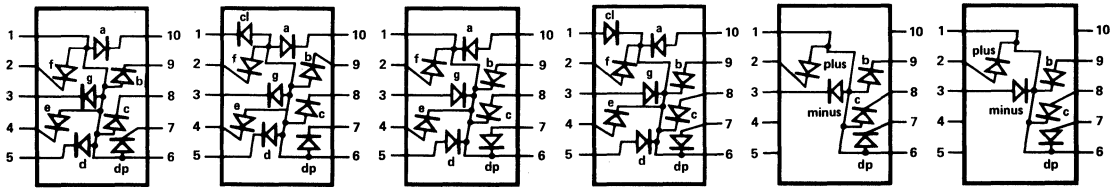


E, F

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. MAXIMUM.
3. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
4. REDUNDANT ANODES.
5. REDUNDANT CATHODES.
6. FOR HDSP-7400/-7800 SERIES PRODUCT ONLY.

	FUNCTION					
PIN	A	B	C	D	E	F
1	ANODE[4]	CATHODE COLON	CATHODE[5]	ANODE COLON	ANODE[4]	CATHODE[5]
2	CATHODE f	CATHODE f	ANODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	CATHODE g	ANODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	CATHODE e	ANODE e	ANODE e	NC	NC
5	CATHODE d	CATHODE d	ANODE d	ANODE d	NC	NC
6	ANODE[4]	ANODE	CATHODE[5]	CATHODE	ANODE[4]	CATHODE[5]
7	CATHODE DP	CATHODE DP	ANODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	CATHODE c	ANODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	CATHODE b	ANODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	CATHODE a	ANODE a	ANODE a	NC	NC

Internal Circuit Diagram



Absolute Maximum Ratings

Description	Red HDSP-7300 Series	AlGaAs Red HDSP-A150 Series	HER HDSP-7500 Series	Yellow HDSP-7400 Series	Green HDSP-7800 Series	Units
Average Power per Segment or DP	82	96	105	80	105	mW
Peak Forward Current per Segment or DP	150[1]	160[3]	90[5]	60[7]	90[9]	mA
DC Forward Current per Segment or DP	25[2]	40[4]	30[6]	20[8]	30[10]	mA
Operating Temperature Range	-40 to +100	-20 to +100[11]	-40 to +100			°C
Storage Temperature Range	-55 to +100					°C
Reverse Voltage per Segment or DP	3.0					V
Lead Solder Temperature for 3 Seconds (1.59 mm [0.063 in.] below seating plane)	260					°C

Notes:

1. See Figure 1 to establish pulsed conditions.
2. Derate above 80°C at 0.63 mA/°C.
3. See Figure 2 to establish pulsed conditions.
4. Derate above 46°C at 0.54 mA/°C.
5. See Figure 7 to establish pulsed conditions.
6. Derate above 53°C at 0.45 mA/°C.
7. See Figure 8 to establish pulsed conditions.
8. Derate above 81°C at 0.52 mA/°C.
9. See Figure 9 to establish pulsed conditions.
10. Derate above 39°C at 0.37 mA/°C.
11. For operation below -20°C, contact your local HP components sales office or an authorized distributor.

Electrical/Optical Characteristics at T_A = 25°C

Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
7300	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	600	1100		µcd	I_F = 20 mA
				500			I_F = 10 mA
7310			770	1355			I_F = 20 mA
				610			I_F = 10 mA
All	Forward Voltage/Segment or DP	V_F		1.6	2.0	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		655		nm	
	Dominant Wavelength[3]	λ_d		640		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	12		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W/Seg	

AlGaAs Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A151	Luminous Intensity/Segment[1,2,5] (Digit Average)	I_V	6.9	14.0		mcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.8		V	I_F = 20 mA
				2.0	3.0	V	I_F = 100 mA
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15.0		V	I_R = 100 μA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		255		°C/W/Seg	

High Efficiency Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
7501	Luminous Intensity/Segment[1,2,6] (Digit Average)	I_V	360	980		μcd	I_F = 5 mA
				5390			I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.0	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 μA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W/Seg	

Yellow

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
7401	Luminous Intensity/Segment[1,2,7] (Digit Average)	I_V	225	480		µcd	I_F = 5 mA
				2740			I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.2	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,9]	λ_d	581.5	586	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50.0		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W/Seg	

High Performance Green

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
7801	Luminous Intensity/Segment[1,2,8] (Digit Average)	I_V	570	1480		µcd	I_F = 10 mA
				3400			I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 10 mA
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,9]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50.0		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W/Seg	

Notes:
1. Case temperature of device immediately prior to the intensity measurement is 25°C.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. For low current operation the AlGaAs HDSP-A101 series displays are recommended.
6. For low current operation the HER HDSP-7511 series displays are recommended.
7. For low current operation the Yellow HDSP-A801 series displays are recommended.
8. For low current operation the Green HDSP-A901 series displays are recommended.
9. The yellow (HDSP-7400) and Green (HDSP-7800) displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

Red, AlGaAs Red

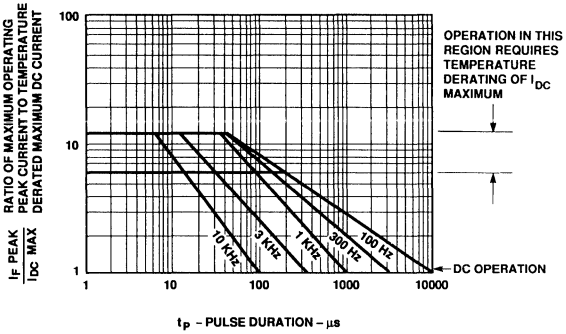


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration – Red.

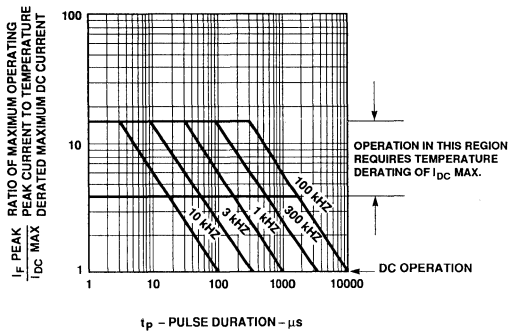


Figure 2. Maximum Allowed Peak Current vs. Pulse Duration – AlGaAs Red.

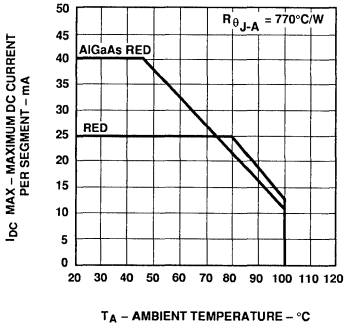


Figure 3. Maximum Allowable DC Current per Segment as a Function of Ambient Temperature.

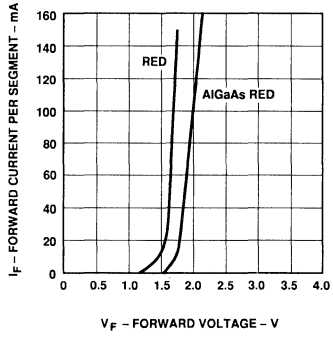


Figure 4. Forward Current vs. Forward Voltage.

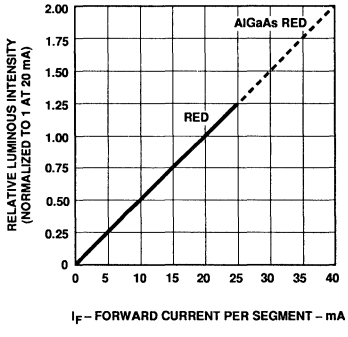


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

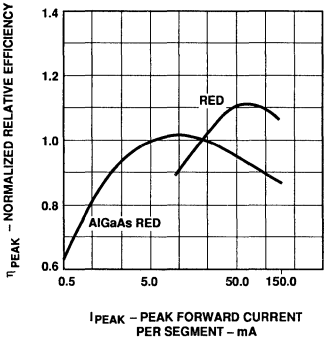


Figure 6. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Yellow, Green

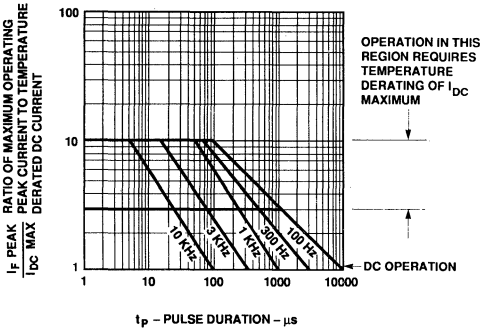


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration – HER.

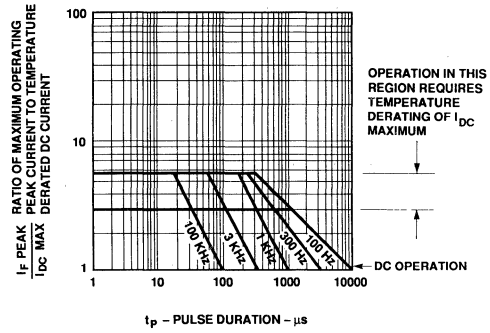


Figure 8. Maximum Tolerable Peak Current vs. Pulse Duration – Yellow.

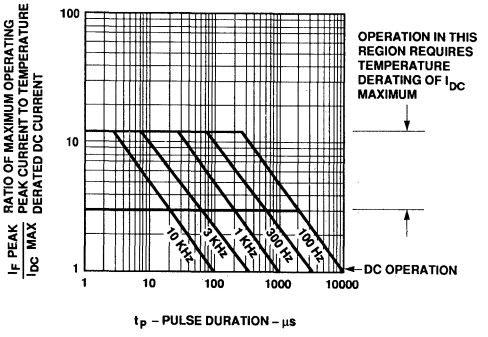


Figure 9. Allowable Peak Current vs. Pulse Duration – Green.

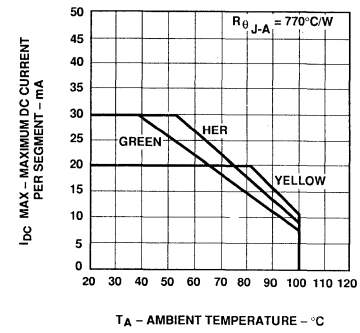


Figure 10. Maximum Allowable DC Current per Segment as a Function of Ambient Temperature.

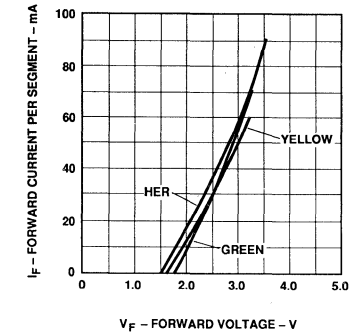


Figure 11. Forward Current vs. Forward Voltage Characteristics.

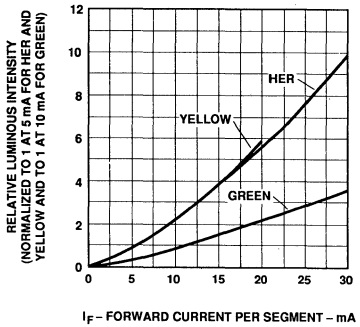


Figure 12. Relative Luminous Intensity vs. DC Forward Current.

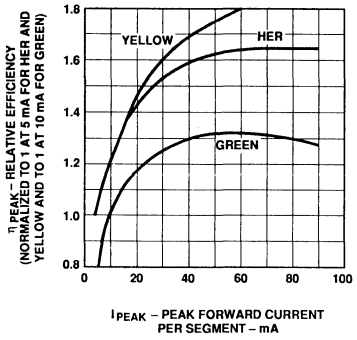


Figure 13. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Electrical/Optical

These displays use light emitting diodes, with the light from each LED optically stretched to form individual segments and decimal points. The Red HDSP-7300 series LEDs use a p-n junction diffused into a GaAsP epitaxial layer on a GaAs substrate. The AlGaAs Red HDSP-A150 series LEDs use double heterojunction AlGaAs on a GaAs substrate. HER HDSP-7500 and Yellow HDSP-7400 series LEDs have their p-n junctions diffused into a GaAsP epitaxial layer on a GaP substrate. The Green HDSP-7800 series LEDs use a liquid phase GaP epitaxial layer on GaP.

These displays are designed for strobed operation. The typical forward voltage values can be scaled from Figures 4 and 11. These values should be used to calculate the current limiting resistor value and typical power consumption. Expected maximum V_F values for driver circuit design and maximum power dissipation, may be calculated using the following V_FMAX models:

Red HDSP-7300 series
$V_F MAX = 1.8\ V + I_{Peak}\ (10\ \Omega)$
For: $I_{Peak} > 5$ mA

AlGaAs Red HDSP-A150 series
$V_F MAX = 1.8\ V + I_{Peak}\ (20\ \Omega)$
For: $I_{Peak} \leq 20$ mA
$V_F MAX = 2.0\ V + I_{Peak}\ (10\ \Omega)$
For: 20 mA $\leq I_{Peak} \leq$ 100 mA
$V_F MAX = 2.27\ V + I_{Peak}\ (7.2\ \Omega)$
For $I_{Peak} \geq 100$ mA

HER (HDSP-7500) and Yellow (7400) series
$V_F MAX = 1.6 + I_{Peak}\ (45\ \Omega)$
For: 5 mA $\leq I_{Peak} \leq$ 20 mA
$V_F MAX = 1.75 + I_{Peak}\ (38\ \Omega)$
For: $I_{Peak} \geq 20$ mA

Green (HDSP-7800) series
$V_F MAX = 2.0 + I_{Peak}\ (50\ \Omega)$
For: $I_{Peak} \geq 5$ mA

Figures 6 and 13 allow the designer to calculate the luminous intensity at different peak and average currents. The following equation calculates intensity at different peak and average currents:

$I_V AVG = (I_F AVG / I_F AVG\ DATA\ SHEET)(\eta_{peak})(I_V DATA\ SHEET)$

Where:
$I_V AVG$ is the calculated time averaged luminous intensity resulting from $I_F AVG$.
$I_F AVG$ is the desired time averaged LED current.
$I_F AVG$ DATA SHEET is the data sheet test current for I_VDATA SHEET.
η_{peak} is the relative efficiency at the peak current, scaled from Figure 6 or 13.
I_V DATA SHEET is the data sheet luminous intensity, resulting from $I_F AVG$ DATA SHEET.

For example, what is the luminous intensity of an HDSP-7500 driven at 50 mA peak 1/5 duty factor?

$I_F AVG = (50\ mA)(0.2) = 10$ mA
$I_F AVG$ DATA SHEET = 5 mA
$\eta_{Peak} = 1.62$
I_V DATA SHEET = 980 µcd

Therefore

$I_V AVG = (10\ mA/5\ mA)(1.62)(980\ \mu cd) = 1587\ \mu cd$

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance the readability. This is accomplished by having the OFF dots blend into the display background and the ON dots stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the dots.

Contrast enhancement may be achieved by using one of the following suggested filters:

Red and AlGaAs Red (HDSP-7300/A150)
Panelgraphic RUBY RED 60
SGL-Homalite H100-1605 RED
3M Louvered Filter R6310 RED or ND0220 GRAY

HER (HDSP-7500)
Panelgraphic SCARLET RED 65
SGL-Homalite H100-1670 RED or H100-1250 GRAY
3M Louvered Filter R6310 RED or ND0220 GRAY

Yellow (HDSP-7400)
Panelgraphic YELLOW 27 or GRAY 10
SGL-Homalite H100-1720 AMBER or H100-1250 GRAY
3M Louvered Filter ND0220 GRAY

Green (HDSP-7800)
Panelgraphic GREEN 48
SGL-Homalite H100-1440 GREEN or H100-1250 GRAY
3M Louvered Filter ND0220 GRAY

For further information on contrast enhancement please see Application Note 1015.

Mechanical

Specially developed plastics are used to optimize the displays optical performance. These plastics restrict the solvents that may be used for cleaning.

Only mixtures of Freon (F113) and alcohol should be used for vapor cleaning processes. Total immersion time in the vapors is two minutes. Some suggested mixtures are Freon TE, Arklone A or K, or Genesolv DES. A 60°C (140°F) water cleaning process may also be used. This process includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a water rinse, and a thorough air dry. Room temperature cleaning may be done with Freon T-E35 or T-P35, Ethanol, Isopropanol, or water with a mild detergent.

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

For further information on soldering LEDs please refer to Application Note 1027.

HEWLETT PACKARD

10 mm (0.40 inch) Seven Segment Displays

Technical Data

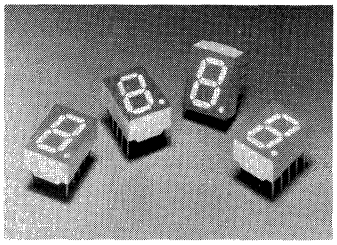
HDSP-F001, F003, F007, F008
HDSP-F151, F153, F157, F158
HDSP-F201, F203, F207, F208
HDSP-F301, F303, F307, F308
HDSP-F401, F403, F407, F408
HDSP-F501, F503, F507, F508

Features

- **Industry Standard Size**
- **Industry Standard Pinout**
  7.6 mm (0.3 inch) DIP
  Leads on 2.54 mm
  (0.1 inch) Centers
- **Choice of Colors**
  Red, AlGaAs Red, High Efficiency Red, Orange, Yellow, Green
- **Excellent Appearance**
  Evenly Lighted Segments
  Mitered Corners on Segments
  Gray Package Gives Optimum Contrast
  ±50° Viewing Angle
- **Design Flexibility**
  Common Anode or
  Common Cathode
  Right Hand Decimal Point
  ±1. Overflow Character
- **Categorized for Luminous Intensity**
  Yellow and Green Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **High Light Output**
- **High Peak Current**
- **Excellent for Long Digit String Multiplexing**
- **Intensity and Color Selection Option**
- **Sunlight Viewable AlGaAs**

Description

The 10 mm (0.40 inch) LED seven segment displays are HP's most space-efficient character size. They are designed for viewing distances up to 4.5 metres (15 feet). These devices use an industry standard size package and pinout. Both the numeric and ±1. overflow devices feature a right hand decimal point. All devices are available as either common anode or common cathode.



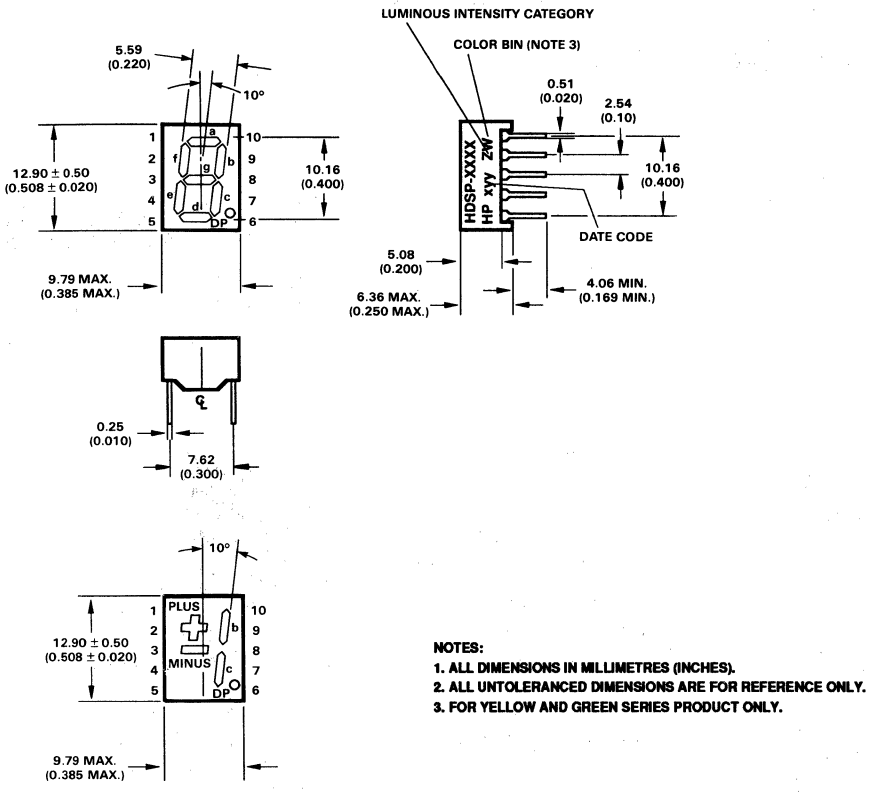
Typical applications include instruments, point of sale terminals, and appliances.

Devices

Red HDSP-	AlGaAs Red[1] HDSP-	HER HDSP-	Orange HDSP-	Yellow HDSP-	Green HDSP-	Description	Package Drawing
F001	F151	F201	F401	F301	F501	Common Anode Right Hand Decimal	A
F003	F153	F203	F403	F303	F503	Common Cathode Right Hand Decimal	B
F007	F157	F207	F407	F307	F507	Common Anode ±1. Overflow	C
F008	F158	F208	F408	F308	F508	Common Cathode ±1. Overflow	D

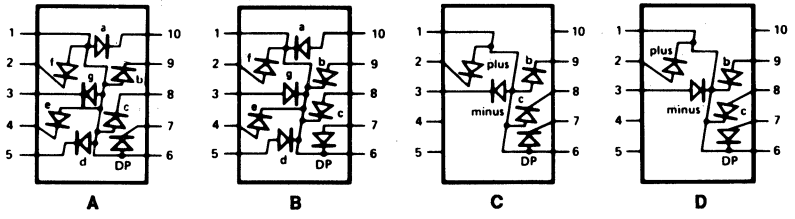
Note:
1. These displays are recommended for high ambient light operation. Please refer to the HDSP-F10X Data sheet for low current operation.

Package Dimensions



NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. FOR YELLOW AND GREEN SERIES PRODUCT ONLY.

Internal Circuit Diagram



PIN	FUNCTION			
	A	B	C	D
1	ANODE[1]	CATHODE[2]	ANODE[1]	CATHODE[2]
2	CATHODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	ANODE e	NC	NC
5	CATHODE d	ANODE d	NC	NC
6	ANODE[1]	CATHODE[2]	ANODE[1]	CATHODE[2]
7	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	ANODE a	NC	NC

NOTES: 1. REDUNDANT ANODES 2. REDUNDANT CATHODES

Absolute Maximum Ratings

Description	Red HDSP-F00X Series	AlGaAs Red HDSP-F15X Series	HER/Orange HDSP-F20X/ F40X Series	Yellow HDSP-F30X Series	Green HDSP-F50X Series	Units
Average Power per Segment or DP	82	96	105	80	105	mW
Peak Forward Current per Segment or DP	150[1]	160[3]	90[5]	60[7]	90[9]	mA
DC Forward Current per Segment or DP	25[2]	40[4]	30[6]	20[8]	30[10]	mA
Operating Temperature Range	-40 to +100	-20 to +100[11]	-40 to +100			°C
Storage Temperature Range	-55 to +100					°C
Reverse Voltage per Segment or DP	3.0					V
Lead Solder Temperature for 3 Seconds (1.59 mm [0.63 in.] below seating plane)	260					°C

Notes:
1. See Figure 1 to establish pulsed conditions.
2. Derate above 80°C at 0.63 mA/°C.
3. See Figure 2 to establish pulsed conditions.
4. Derate above 46°C at 0.54 mA/°C.
5. See Figure 7 to establish pulsed conditions.
6. Derate above 53°C at 0.45 mA/°C.
7. See Figure 8 to establish pulsed conditions.
8. Derate above 81°C at 0.52 mA/°C.
9. See Figure 9 to establish pulsed conditions.
10. Derate above 39°C at 0.37 mA/°C.
11. For operation below -20°C, contact your local HP components sales office or an authorized distributor.

Electrical/Optical Characteristics at $T_A = 25°C$

Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-F00X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	650	1200		µcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.6	2.0	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		655		nm	
	Dominant Wavelength[3]	λ_d		640		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	12		V	I_F = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		320		°C/W/Seg	

AlGaAs Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-F15X	Luminous Intensity/Segment[1,2,5] (Digit Average)	I_V	7.5	15.0		mcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.8	2.2	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		320		°C/W/Seg	

High Efficiency Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-F20X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	420	1200		µcd	I_F = 5 mA
	Forward Voltage/Segment or DP	V_F		2.0	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		320		°C/W/Seg	

Orange

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-F40X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	420	1200		µcd	I_F = 5 mA
	Forward Voltage/Segment or DP	V_F		2.0	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		600		nm	
	Dominant Wavelength[3]	λ_d		603		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		320		°C/W/Seg	

Yellow

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-F30X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	290	800		µcd	I_F = 5 mA
	Forward Voltage/Segment or DP	V_F		2.2	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,6]	λ_d	581.5	586	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	40		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		320		°C/W/Seg	

High Performance Green

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-F50X	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	820	2100		µcd	I_F = 10 mA
	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 10 mA
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,6]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		320		°C/W/Seg	

Notes:
1. Case temperature of device immediately prior to the intensity measurement is 25°C.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. For low current operation, the AlGaAs HDSP-F10X series displays are recommended. They are tested at 1 mA dc/segment and are pin for pin compatible with the HDSP-F15X series.
6. The Yellow (HDSP-F30X) series and Green (HDSP-F50X) series displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

RED, AlGaAs Red

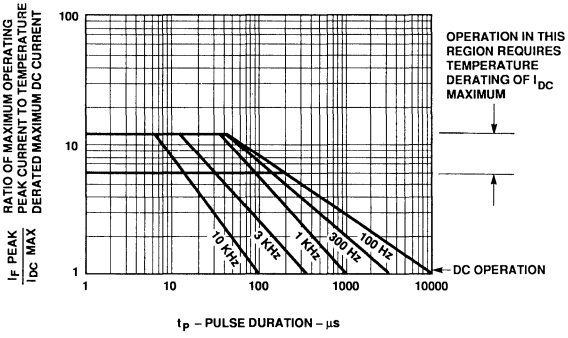


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration – Red.

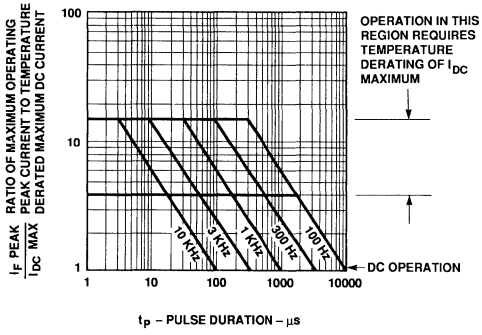


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration – AlGaAs Red.

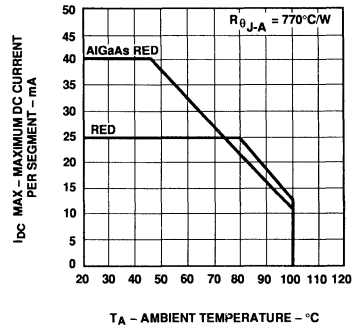


Figure 3. Maximum Allowable DC Current vs. Ambient Temperature.

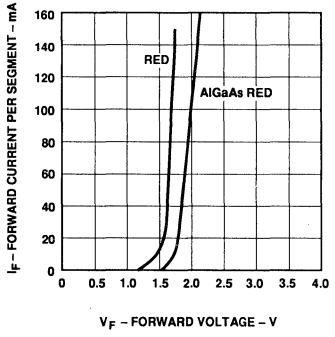


Figure 4. Forward Current vs. Forward Voltage.

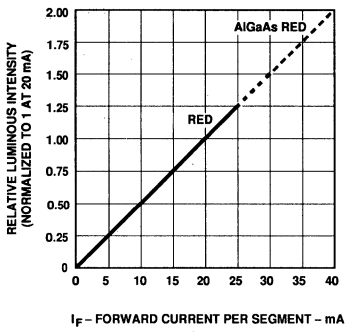


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

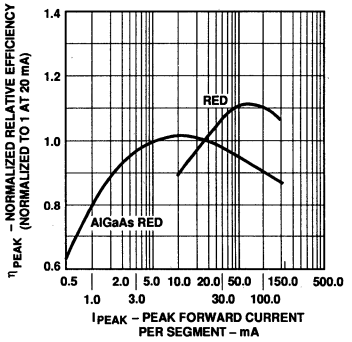


Figure 6. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Orange, Yellow, Green

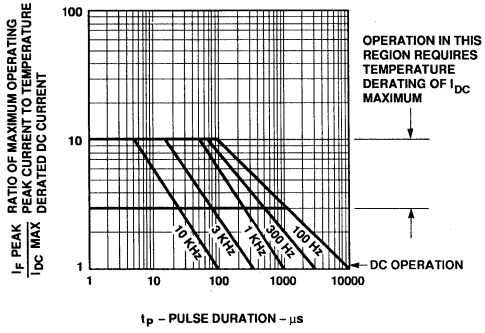


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration – HER, Orange.

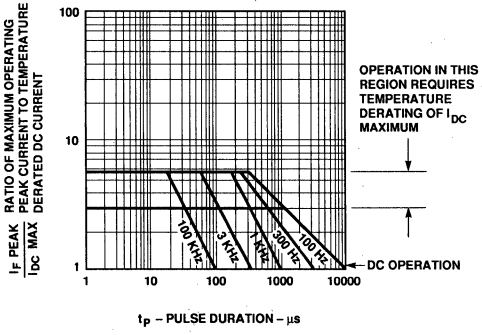


Figure 8. Maximum Tolerable Peak Current vs. Pulse Duration – Yellow.

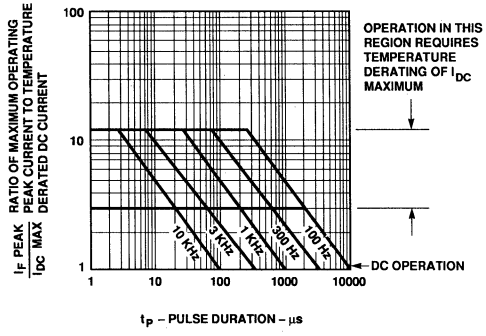


Figure 9. Maximum Tolerable Peak Current vs. Pulse Duration – Green.

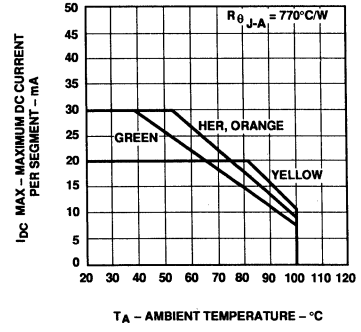


Figure 10. Maximum Allowable DC Current vs. Ambient Temperature.

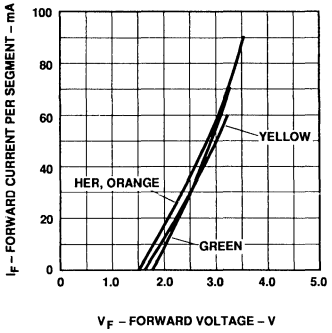


Figure 11. Forward Current vs. Forward Voltage.

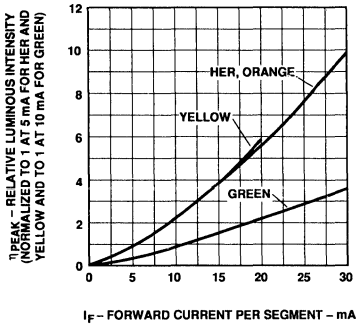


Figure 12. Relative Luminous Intensity vs. DC Forward Current.

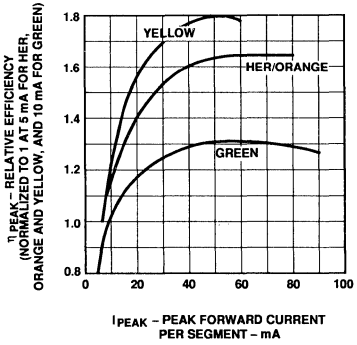


Figure 13. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Electrical/Optical

These displays use light emitting diodes, with the light from each LED optically stretched to form individual segments and decimal points. The Red HDSP-F00X series LEDs use a p-n junction diffused into a GaAsP epitaxial layer on a GaAs substrate. The AlGaAs Red HDSP-F15X series LEDS use double heterojunction AlGaAs on a GaAs substrate. HER HDSP-F20X, Orange HDSP-F40X, and Yellow HDSP-F30X series LEDs have their p-n junctions diffused into a GaAsP epitaxial layer on a GaP substrate. The Green HDSP-F50X series LEDs use a liquid phase Gap epitaxial layer on GaP.

These displays are designed for strobed operation. The typical forward voltage values can be scaled from Figures 4 and 11. These values should be used to calculate the current limiting resistor value and typical power consumption. Expected maximum V_F values for driver circuit design and maximum power dissipation, may be calculated using the following V_FMAX models:

Red HDSP-F00X series

V_FMAX = 1.8 V + I_{Peak} (10 Ω)
For: I_{Peak} > 5 mA

AlGaAs Red HDSP-F15X series

V_FMAX = 1.8 V + I_{Peak} (20 Ω)
For: $I_{Peak} \leq 20$ mA
V_FMAX = 2.0 V + I_{Peak} (10 Ω)
For: 20 mA ≤ $I_{Peak} \leq 100$ mA
V_FMAX = 2.27 V + I_{Peak} (7.2 Ω)
For $I_{Peak} \geq 100$ mA

HER HDSP-F20X, Orange HDSP-F40X, and Yellow HDSP-F30X series

V_FMAX = 1.6 + I_{Peak} (45 Ω)
For: 5 mA ≤ $I_{Peak} \leq 20$ mA
V_FMAX = 1.75 + I_{Peak} (38 Ω)
For: $I_{Peak} \geq 20$ mA

Green HDSP-F50X series

V_FMAX = 2.0 + I_{Peak} (50 Ω)
For: I_{Peak} > 5 mA

Figures 6 and 13 allow the designer to calculate the luminous intensity at different peak and average currents. The following equation calculates intensity at different peak and average currents:

$I_V AVG = (I_F AVG / I_F AVG \text{ DATA SHEET})(\eta_{peak})(I_V \text{ DATA SHEET})$

Where:

$I_V AVG$ is the calculated time averaged luminous intensity resulting from $I_F AVG$.

$I_F AVG$ is the desired time averaged LED current.

$I_F AVG$ DATA SHEET is the data sheet test current for I_V DATA SHEET.

η_{peak} is the relative efficiency at the peak current, scaled from Figure 6 or 13.

I_V DATA SHEET is the data sheet luminous intensity, resulting from $I_F AVG$ DATA SHEET.

For example, what is the luminous intensity of an HDSP-F201 driven at 50 mA peak 1/5 duty factor?

$I_F AVG = (50 \text{ mA})(0.2) = 10 \text{ mA}$
$I_F AVG \text{ DATA SHEET} = 5 \text{ mA}$
$\eta_{Peak} = 1.63$
$I_V \text{ DATA SHEET} = 1200 \ \mu cd$

Therefore

$I_V AVG = (10 \text{ mA}/5 \text{ mA})(1.63)(1200 \ \mu cd) = 3912 \ \mu cd$

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance the readability. This is accomplished by having the OFF dots blend into the display background and the ON dots stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the dots.

Contrast enhancement may be achieved by using one of the following suggested filters:

Red (HDSP-F00X) and AlGaAs Red (HDSP-F15X)
Panelgraphic RUBY RED 60, or GRAY 10
SGL-Homalite H100-1605 RED or H100-1250 GRAY
3M Louvered Filter R6310 RED or ND0220 GRAY

HER (HDSP-F20X)
Panelgraphic SCARLET RED 65, or GRAY 10
SGL-Homalite H100-1670 RED or H100-1250 GRAY
3M Louvered Filter R6310 RED or ND0220 GRAY

Yellow (HDSP-F30X)
Panelgraphic YELLOW 27 or GRAY 10
SGL-Homalite H100-1720 AMBER or H100-1250 GRAY
3M Louvered Filter ND0220 GRAY

Orange (HDSP-F40X)
Panelgraphic AMBER 23, AMBER 26, or GRAY 10
SGL-Homalite H100-1709 AMBER or H100-1250 GRAY
3M Louvered Filter ND0220 GRAY

Green (HDSP-F50X)
Panelgraphic GREEN 48, or GRAY 10
SGL-Homalite H100-1440 GREEN or H100-1250 GRAY
3M Louvered Filter ND0220 GRAY

For further information on contrast enhancement please see Application Note 1015.

Mechanical

Specially developed plastics are used to optimize the displays optical performance. These plastics restrict the solvents that may be used for cleaning. Only mixtures of Freon (F113) and alcohol should be used for vapor cleaning processes. Total immersion time in the vapors is two minutes. Some suggested mixtures are Freon TE, Arklone A or K, or Genesolv DI-15 or DE-15. A 60°C (140°F) water cleaning process may also be used. This process includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a water rinse, and a thorough air dry. Room temperature cleaning may be done with Freon T-E35 or T-P35, Ethanol, Isopropanol, or water with a mild detergent.

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloro-ethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

HEWLETT PACKARD

7.6 mm (0.3 inch)/10.9 mm (0.43 inch) Seven Segment Displays

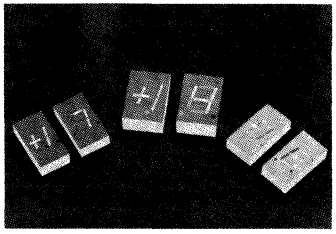
Technical Data

5082-7610, 7611, 7613, 7616, 7620, 7621, 7623, 7626, 7650, 7651, 7653, 7656, 7660, 7661, 7663, 7666, 7730, 7731, 7736, 7740, 7750, 7751, 7756, 7760

HDSP-3600, 3601, 3603, 3606, 4600, 4601, 4603, 4606, E150, E151, E153, E156

Features

- **Industry Standard Size**
- **Industry Standard Pinout**
  7.62 mm (0.300 inch) DIP Leads on 2.54 mm (0.100 inch) Centers
- **Choice of Colors**
  Red, AlGaAs Red, High Efficiency Red, Yellow, Green
- **Excellent Appearance**
  Evenly Lighted Segments
  Gray Package Gives Optimum Contrast
  ±50° Viewing Angle
- **Design Flexibility**
  Common Anode or Common Cathode
  Single Digits
  Left or Right Hand Decimal Point
  ±1. Overflow Character
- **Categorized for Luminous Intensity**
  Yellow and Green Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **High Light Output**
- **High Peak Current**
- **Excellent for Long Digit String Multiplexing**
- **Intensity and Color Selection Available**
  See Intensity and Color Selected Displays Data Sheet
- **Sunlight Viewable AlGaAs**



Description

The 7.6 mm (0.3 inch) and 10.9 mm (0.43 inch) LED seven segment displays are designed for viewing distances up to 3 metres (10 feet) and 5 metres (16 feet). These devices use an industry standard size package and pinouts. All devices are available as either common anode or common cathode.

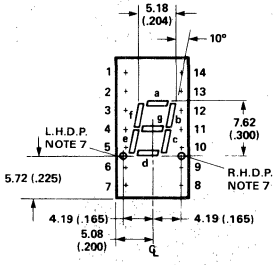
Devices

Red 5082-	AlGaAs[1] Red HDSP-	HER[1] 5082-	Yellow 5082-	Green HDSP-	Description	Package Drawing
7730		7610	7620	3600	7.6 mm Common Anode Left Hand Decimal	A
7731		7611	7621	3601	7.6 mm Common Anode Right Hand Decimal	B
7740		7613	7623	3603	7.6 mm Common Cathode Right Hand Decimal	C
7736		7616	7626	3606	7.6 mm Universal ±1. Overflow Right Hand Decimal[2]	D
7750	E150	7650	7660	4600	10.9 mm Common Anode Left Hand Decimal	E
7751	E151	7651	7661	4601	10.9 mm Common Anode Right Hand Decimal	F
7760	E153	7653	7663	4603	10.9 mm Common Cathode Right Hand Decimal	G
7756	E156	7656	7666	4606	10.9 mm Universal ±1. Overflow Right Hand Decimal[2]	H

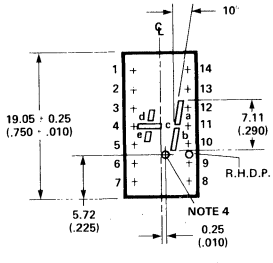
Notes:
1. These displays are recommended for high ambient light operation. Please refer to the HDSP-E10X AlGaAs and HDSP-335X HER data sheet for low current operation.
2. Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram H.

These displays are ideal for most applications. Pin for pin equivalent displays are also available in a low current or high light ambient design. The low current displays are ideal for portable applications. The high light ambient displays are ideal for high light ambients or long string lengths. For additional information see the Low Current Seven Segment Displays, or High Light Ambient Seven Segment Displays data sheets.

Package Dimensions

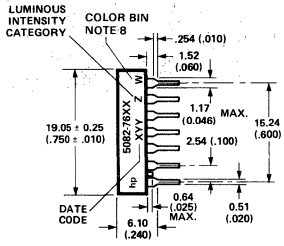


A,B,C

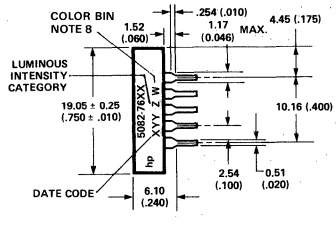


D

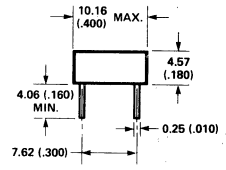
FUNCTION				
PIN	A	B	C	D
1	CATHODE-a	CATHODE-a	NO PIN	ANODE-d
2	CATHODE-f	CATHODE-f	CATHODE[6]	NO PIN
3	ANODE[3]	ANODE[3]	ANODE-f	CATHODE-d
4	NO PIN	NO PIN	ANODE-g	CATHODE-c
5	NO PIN	NO PIN	ANODE-e	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	ANODE-d	ANODE-e
7	CATHODE-d	CATHODE-e	NO PIN	ANODE-c
8	CATHODE-d	CATHODE-d	NO PIN	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	CATHODE[6]	NO PIN
10	CATHODE-c	CATHODE-c	ANODE-dp	CATHODE-dp
11	CATHODE-g	CATHODE-g	ANODE-c	CATHODE-b
12	NO PIN	NO PIN	ANODE-b	CATHODE-a
13	CATHODE-b	CATHODE-b	ANODE-a	ANODE-a
14	ANODE[3]	ANODE[3]	NO PIN	ANODE-b



A,B,D SIDE



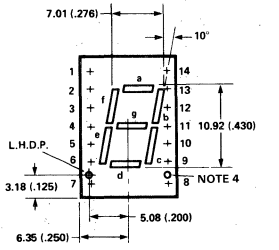
C SIDE



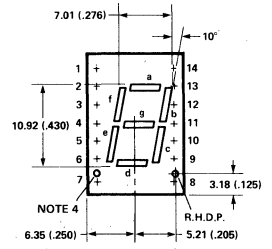
A,B,C,D END

NOTES;

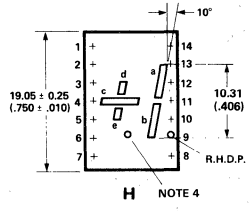
1. **DIMENSIONS IN MILLIMETRES AND (INCHES).**
2. **ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.**
3. **REDUNDANT ANODES.**
4. **UNUSED DP POSITION.**
5. **SEE INTERNAL CIRCUIT DIAGRAM.**
6. **REDUNDANT CATHODE.**
7. **SEE PART NUMBER TABLE FOR L.H.D.P. AND R.H.D.P. DESIGNATION.**
8. **FOR YELLOW AND GREEN DEVICES ONLY.**



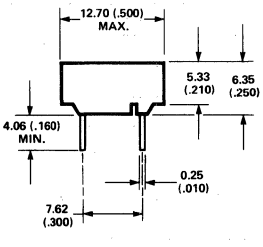
E



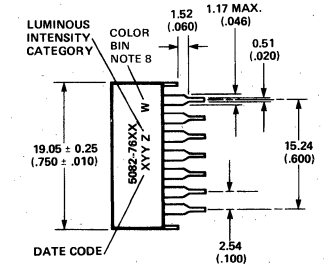
F,G FRONT VIEW



H NOTE 4



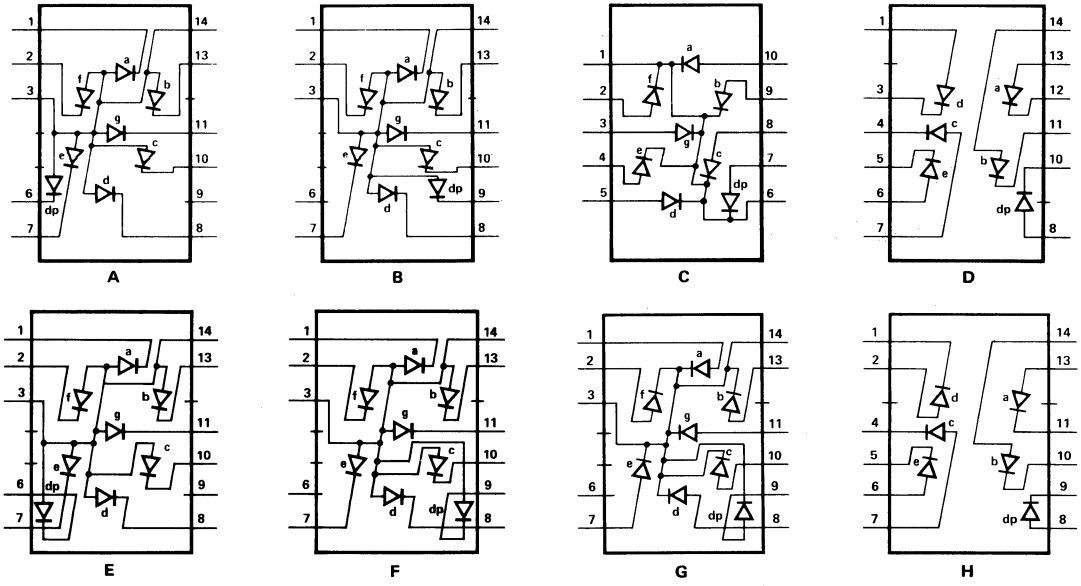
END VIEW



SIDE VIEW

FUNCTION				
PIN	E	F	G	H
1	CATHODE-a	CATHODE-a	ANODE-a	CATHODE-d
2	CATHODE-f	CATHODE-f	ANODE-f	ANODE-d
3	ANODE[3]	ANODE[3]	CATHODE[6]	NO PIN
4	NO PIN	NO PIN	NO PIN	CATHODE-c
5	NO PIN	NO PIN	NO PIN	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	NO CONN.[5]	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-e	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-d	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	ANODE-dp	CATHODE-dp
10	CATHODE-c	CATHODE-c	ANODE-c	CATHODE-b
11	CATHODE-g	CATHODE-g	ANODE-g	CATHODE-a
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE-b	CATHODE-b	ANODE-b	ANODE-a
14	ANODE[3]	ANODE[3]	CATHODE[6]	ANODE-b

Internal Circuit Diagram



Absolute Maximum Ratings

Description	Red 5082-7700 Series	AlGaAs Red HDSP-E150 Series	HER 5082-7610/ 7650 Series	Yellow 5082-7620/ 7660 Series	Green HDSP-3600/ 4600 Series	Units
Average Power per Segment or DP	82	96	105	80	105	mW
Peak Forward Current per Segment or DP	150[1]	160[3]	90[5]	60[7]	90[9]	mA
DC Forward Current per Segment or DP	25[2]	40[4]	30[6]	20[8]	30[10]	mA
Operating Temperature Range	-40 to +100	-20 to +100[11]	-40 to +100			°C
Storage Temperature Range	-55 to +100					°C
Reverse Voltage per Segment or DP	3.0					V
Lead Solder Temperature for 3 Seconds (1.59 mm [0.063 in.] below seating plane	260					°C

Notes:

1. See Figure 1 to establish pulsed conditions.
2. Derate above 80°C at 0.63 mA/°C.
3. See Figure 2 to establish pulsed conditions.
4. Derate above 46°C at 0.54 mA/°C.
5. See Figure 7 to establish pulsed conditions.
6. Derate above 53°C at 0.45 mA/°C.
7. See Figure 8 to establish pulsed conditions.
8. Derate above 81°C at 0.52 mA/°C.
9. See Figure 9 to establish pulsed conditions.
10. Derate above 39°C at 0.37 mA/°C.
11. For operation below -20°C, contact your local HP components sales office or an authorized distributor.

Electrical/Optical Characteristics at T_A = 25°C

Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
5082-7730	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	360	770		µcd	I_F = 20 mA
5082-7750			360	1100		µcd	I_F = 20 mA
All	Forward Voltage/Segment or DP	V_F		1.6	2.0	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		655		nm	
	Dominant Wavelength[3]	λ_d		640		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	12		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		280		°C/W/Seg	

AlGaAs Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-E150	Luminous Intensity/Segment[1,2,5] (Digit Average)	I_V	8.5	15.0		mcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.8		V	I_F = 20 mA
				2.0	3.0	V	I_F = 100 mA
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		340		°C/W/Seg	

High Efficiency Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
5082-7610	Luminous Intensity/Segment[1,2,6] (Digit Average)	I_V	340	800		µcd	I_F = 5 mA
5082-7650			340	1115		µcd	I_F = 5 mA
All	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		280		°C/W	

Yellow

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
5082-7620	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	205	620		µcd	I_F = 5 mA
5082-7660			290	835		µcd	I_F = 5 mA
All	Forward Voltage/Segment or DP	V_F		2.2	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,7]	λ_d	581.5	586	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	40		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		280		°C/W/Seg	

High Performance Green

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-3600	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	570	1800		µcd	I_F = 10 mA
HDSP-4600			460	1750		µcd	I_F = 10 mA
All	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 10 mA
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,7]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		280		°C/W/Seg	

Notes:
1. Device case temperature is 25°C prior to the intensity measurement.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. For low current operation, the AlGaAs HDSP-E10X series displays are recommended. They are tested at 1 mA dc/segment and are pin for pin compatible with the HDSP-E15X series.
6. For low current operation, the HER HDSP-335X series displays are recommended. They are tested at 2 mA dc/segment and are pin for pin compatible with the 5082-7650 series.
7. The Yellow (5082-7620/7660) and Green (HDSP-3600/4600) displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

Red, AlGaAs Red

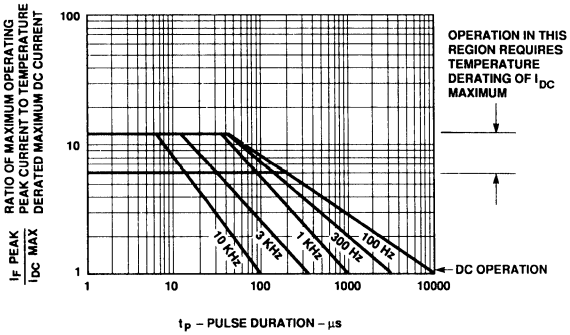


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration – Red.

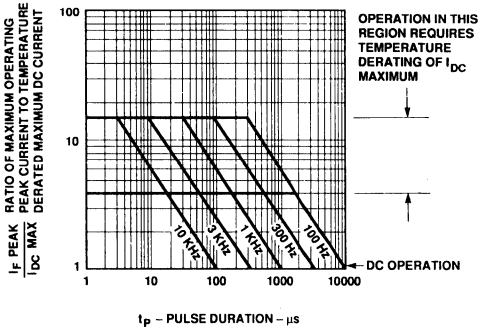


Figure 2. Maximum Allowed Peak Current vs. Pulse Duration – AlGaAs Red.

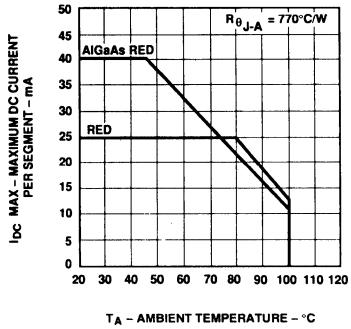


Figure 3. Maximum Allowable DC Current vs. Ambient Temperature.

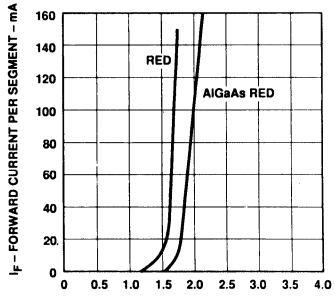


Figure 4. Forward Current vs. Forward Voltage.

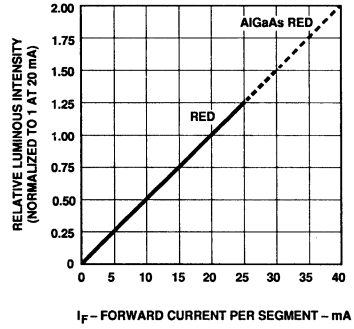


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

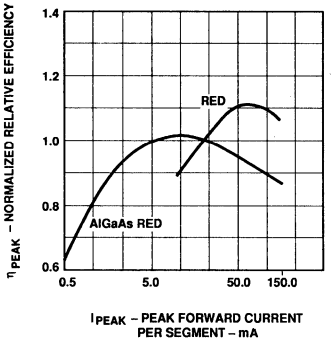


Figure 6. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Yellow, Green

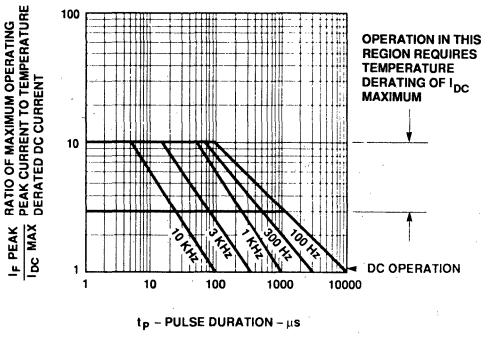


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration – HER Series.

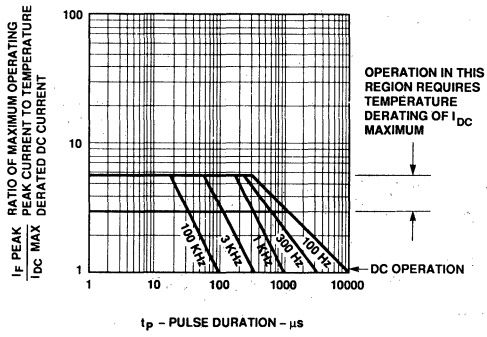


Figure 8. Maximum Tolerable Peak Current vs. Pulse Duration – Yellow Series.

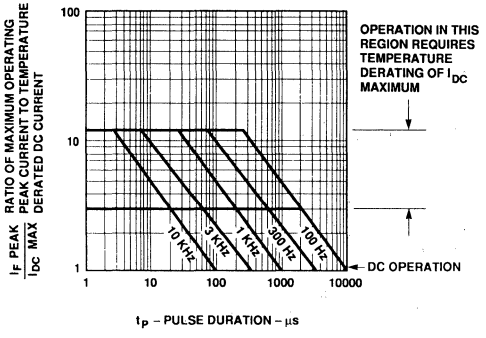


Figure 9. Allowable Peak Current vs. Pulse Duration – Green Series.

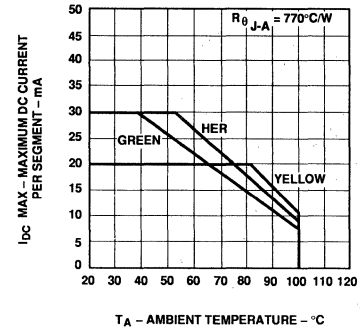


Figure 10. Maximum Allowable DC Current vs. Ambient Temperature.

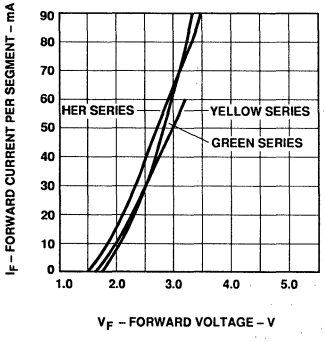


Figure 11. Forward Current vs. Forward Voltage.

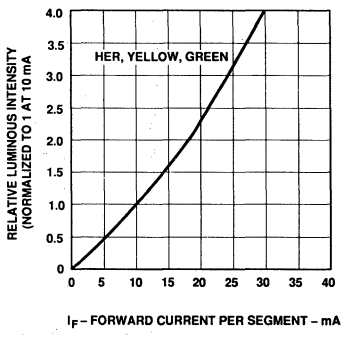


Figure 12. Relative Luminous Intensity vs. DC Forward Current.

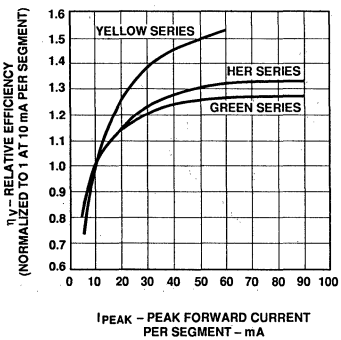


Figure 13. Relative Luminous Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Electrical/Optical

These displays use light emitting diodes, with the light from each LED optically stretched to form individual segments and decimal points. The Red 5082-7730/7750 series LEDs use a p-n junction diffused into a GaAsP epitaxial layer on a GaAs substrate. The AlGaAs Red HDSP-E150 series LEDs use double heterojunction AlGaAs on a GaAs substrate. HER 5082-7610/7650 and Yellow 5082-7620/7660 series LEDs have their p-n junctions diffused into a GaAsP epitaxial layer on a GaP substrate. The Green HDSP-3600/4600 series LEDs use a liquid phase GaP epitaxial layer on GaP.

These displays are designed for strobed operation. The typical forward voltage values can be scaled from Figures 4 and 11. These values should be used to calculate the current limiting resistor value and typical power consumption. Expected maximum V_F values for driver circuit design and maximum power dissipation may be calculated using the following V_FMAX models:

Red 5082-7730/7750 series
$V_F MAX = 1.8\ V + I_{Peak}\ (10\ \Omega)$
For: $I_{Peak} > 5$ mA

AlGaAs Red HDSP-E150 series
$V_F MAX = 1.8\ V + I_{Peak}\ (20\ \Omega)$
For: $I_{Peak} \leq 20$ mA
$V_F MAX = 2.0\ V + I_{Peak}\ (10\ \Omega)$
For: 20 mA $\leq I_{Peak} \leq$ 100 mA
$V_F MAX = 2.27\ V + I_{Peak}\ (7.2\ \Omega)$
For $I_{Peak} \geq 100$ mA

HER (5082-7610/7650) and Yellow (5082-7620/7660) series
$V_F MAX = 1.6 + I_{Peak}\ (45\ \Omega)$
For: 5 mA $\leq I_{Peak} \leq$ 20 mA
$V_F MAX = 1.75 + I_{Peak}\ (38\ \Omega)$
For: $I_{Peak} \geq 20$ mA

Green (HDSP-3600/4600) series
$V_F MAX = 2.0 + I_{Peak}\ (50\ \Omega)$
For: $I_{Peak} > 5$ mA

Figures 6 and 13 allow the designer to calculate the luminous intensity at different peak and average currents. The following equation calculates intensity at different peak and average currents:

$I_V AVG = (I_F AVG / I_F AVG\ DATA\ SHEET)(\eta_{peak})(I_V DATA\ SHEET)$

Where:
$I_V AVG$ is the calculated time averaged luminous intensity resulting from $I_F AVG$.
$I_F AVG$ is the desired time averaged LED current.
$I_F AVG$ DATA SHEET is the data sheet test current for I_VDATA SHEET.
η_{peak} is the relative efficiency at the peak current, scaled from Figure 6 or 13.
I_V DATA SHEET is the data sheet luminous intensity, resulting from $I_F AVG$ DATA SHEET.

For example, what is the luminous intensity of a 5082-7610 driven at 50 mA peak 1/5 duty factor?

$I_F AVG = (50\ mA)(0.2) = 10$ mA
$I_F AVG$ DATA SHEET = 5 mA
$\eta_{Peak} = 1.62$
I_V DATA SHEET = 800 µcd

Therefore

$I_V AVG = (10\ mA/5\ mA)(1.62)(800\ \mu cd)$
$= 2592\ \mu cd$

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance the readability. This is accomplished by having the OFF dots blend into the display background and the ON dots stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the dots.

Contrast enhancement may be achieved by using one of the following suggested filters:

Red and AlGaAs Red (5082-7730/7750/HDSP-E150)
Panelgraphic RUBY RED 60
SGL-Homalite H100-1605 RED
3M Louvered Filter R6310 RED or ND0220 GRAY

HER (5082-7610/7650)
Panelgraphic SCARLET RED 65
SGL-Homalite H100-1670 RED or H100-1250 GRAY
3M Louvered Filter R6310 RED or ND0220 GRAY

Yellow (5082-7620/7660)
Panelgraphic YELLOW 27 or GRAY 10
SGL-Homalite H100-1720 AMBER or H100-1250 GRAY
3M Louvered Filter ND0220 GRAY

Green (HDSP-3600/4600)
Panelgraphic GREEN 48
SGL-Homalite H100-1440 GREEN or H100-1250 GRAY
3M Louvered Filter ND0220 GRAY

For further information on contrast enhancement please see Application Note 1015.

Mechanical

Specially developed plastics are used to optimize the displays optical performance. These plastics restrict the solvents that may be used for cleaning. Only mixtures of Freon (F113) and alcohol should be used for vapor cleaning processes. Total immersion time in the vapors is two minutes. Some suggested mixtures are Freon TE, Arklone A or K, or Genesolv DES. A 60°C (140°F) water cleaning process may also be used. This process includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a water rinse, and a thorough air dry. Room temperature cleaning may be done with Freon T-E35 or T-P35, Ethanol, Isopropanol, or water with a mild detergent.

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

For further information on soldering LEDs please refer to Application Note 1027.

HEWLETT PACKARD

14.2 mm (0.56 inch) Seven Segment Displays

Technical Data

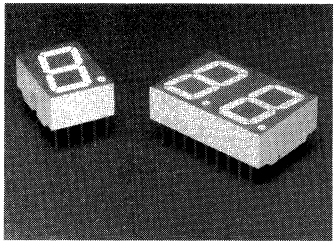
HDSP-5301, 5303, 5307, 5308, 5321, 5323
HDSP-H151, H153, H157, H158
HDSP-5501, 5503, 5507, 5508, 5521, 5527
HDSP-5701, 5703, 5707, 5708, 5721, 5723
HDSP-5601, 5603, 5607, 5608, 5621, 5623

Features

- **Industry Standard Size**
- **Industry Standard Pinout**
  15.24 mm (0.6 in.) DIP Leads on 2.54 mm (0.1 in.) Centers
- **Choice of Colors**
  Red, AlGaAs Red, High Efficiency Red, Yellow, Green
- **Excellent Appearance**
  Evenly Lighted Segments
  Mitered Corners on Segments
  Gray Package Gives Optimum Contrast
  ±50° Viewing Angle
- **Design Flexibility**
  Common Anode or Common Cathode
  Single and Dual Digits
  Right Hand Decimal Point
  ±1. Overflow Character
- **Categorized for Luminous Intensity**
  Yellow and Green Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **High Light Output**
- **High Peak Current**
- **Excellent for Long Digit String Multiplexing**
- **Intensity and Color Selection Option**
  See Intensity and Color Selected Displays Data Sheet
- **Sunlight Viewable AlGaAs**

Description

The 14.2 mm (0.56 inch) LED seven segment displays are designed for viewing distances



up to 7 metres (23 feet). These devices use and industry standard size package and pinout. Both the numeric and ±1 overflow devices feature a right hand decimal point. All devices are available as either common anode or common cathode.

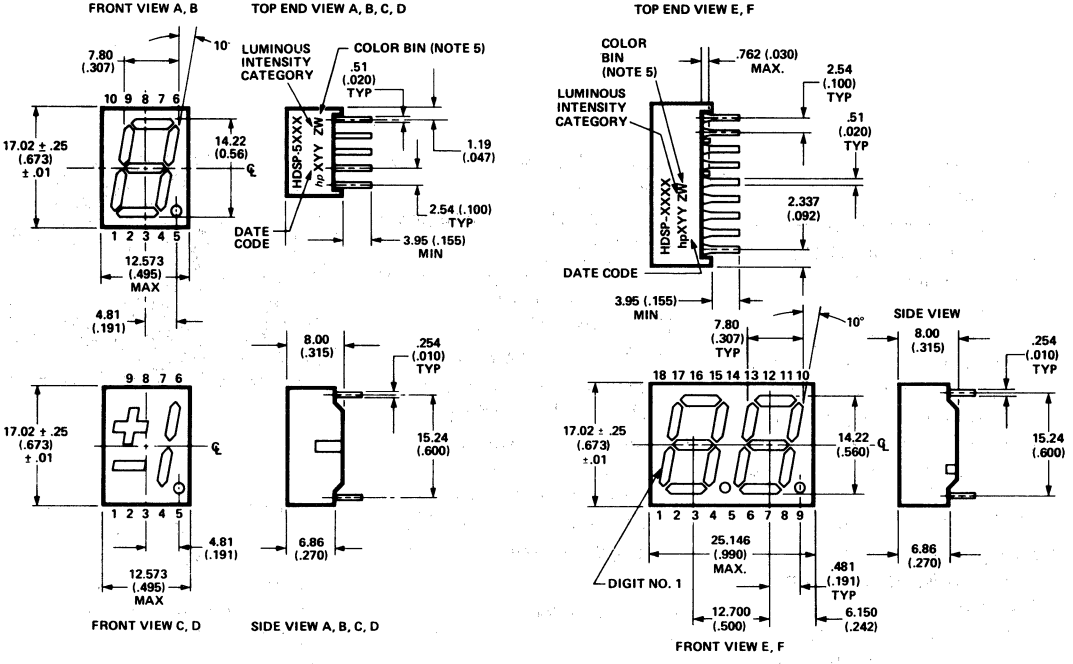
Devices

Red HDSP-	AlGaAs Red HDSP-[1]	HER HDSP-[1]	Yellow HDSP-	Green HDSP-	Description	Package Drawing
5301	H151	5501	5701	5601	Common Anode Right Hand Decimal	A
5303	H153	5503	5703	5603	Common Cathode Right Hand Decimal	B
5307	H157	5507	5707	5607	Common Anode ±1. Overflow	C
5308	H158	5508	5708	5608	Common Cathode ±1. Overflow	D
5321		5521	5721	5621	Two Digit Common Anode Right Hand Decimal	E
5323		5523	5723	5623	Two Digit Common Cathode Right Hand Decimal	F

Note:
1. These displays are recommended for high ambient light operation. Please refer to the HDSP-H10X/K12X AlGaAs and HDSP-555X HER data sheet for low current operation.

These displays are ideal for most applications. Pin for pin equivalent displays are also available in a low current design. The low current displays are ideal for portable applications. For additional information see the Low Current Seven Segment Displays data sheet.

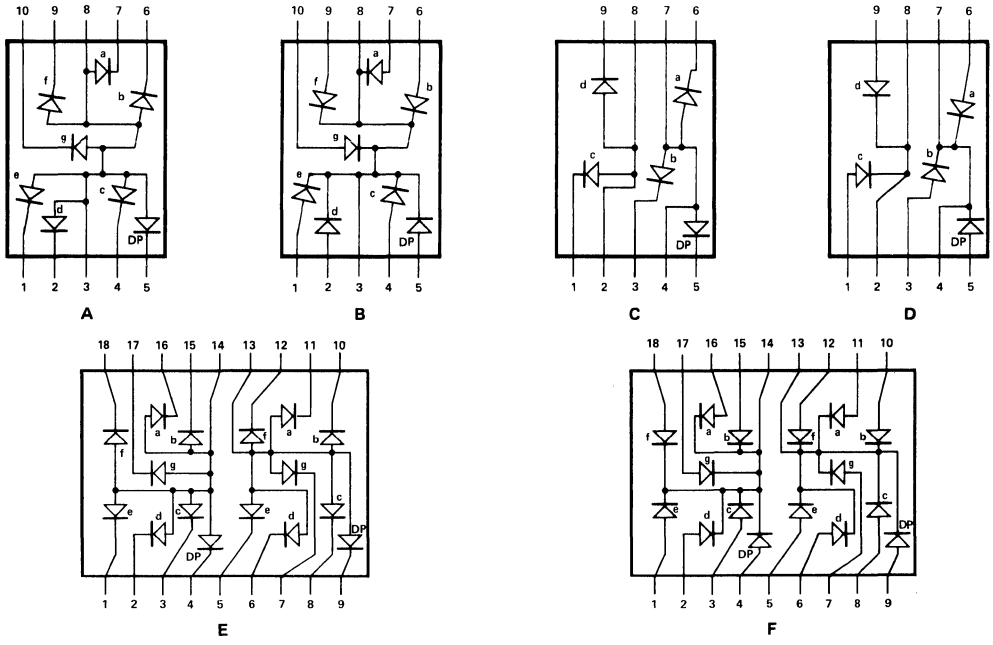
Package Dimensions



PIN	FUNCTION					
	A	B	C	D	E	F
1	CATHODE e	ANODE e	CATHODE c	ANODE c	E CATHODE NO. 1	E ANODE NO. 1
2	CATHODE d	ANODE d	ANODE c, d	CATHODE c, d	D CATHODE NO. 1	D ANODE NO. 1
3	ANODE[3]	CATHODE[4]	CATHODE b	ANODE b	C CATHODE NO. 1	C ANODE NO. 1
4	CATHODE c	ANODE c	ANODE a, b, DP	CATHODE a, b, DP	DP CATHODE NO. 1	DP ANODE NO. 1
5	CATHODE DP	ANODE DP	CATHOPDE DP	ANODE DE	E CATHODE NO. 1	E ANODE NO. 2
6	CATHODE b	ANODE b	CATHODE a	ANODE a	D CATHODE NO. 2	D ANODE NO. 2
7	CATHODE a	ANODE a	ANODE a, b, DP	CATHODE a, b, DP	G CATHODE NO. 2	G ANODE NO. 2
8	ANODE[3]	CATHODE[4]	ANODE c, d	CATHODE c, d	C CATHODE NO. 2	C ANODE NO. 2
9	CATHODE f	ANODE f	CATHODE d	ANODE d	DP CATHODE NO. 2	DP ANODE NO. 2
10	CATHODE g	ANODE g	NO PIN	NO PIN	B CATHODE NO. 2	B ANODE NO. 2
11					A CATHODE NO. 2	A ANODE NO. 2
12					F CATHODE NO. 2	F ANODE NO. 2
13					DIGIT NO. 2 ANODE	DIGIT NO. 2 CATHODE
14					DIGIT NO. 1 ANODE	DIGIT NO. 2 CATHODE
15					B CATHODE NO. 2	B ANODE NO. 1
16					A CATHODE NO. 1	A ANODE NO. 1
17					G CATHODE NO. 1	G ANODE NO. 1
18					F CATHODE NO. 1	F ANODE NO. 1

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. REDUNDANT ANODES.
4. REDUNDANT CATHODES.
5. FOR HDSP-5600/-5700 SERIES PRODUCT ONLY.

Internal Circuit Diagram



Absolute Maximum Ratings

Description	Red HDSP-5300 Series	AlGaAs Red HDSP-H150 Series	HER HDSP-5500 Series	Yellow HDSP-5700 Series	Green HDSP-5600 Series	Units
Average Power per Segment or DP	82	96	105	80	105	mW
Peak Forward Current per Segment or DP	150[1]	160[3]	90[5]	60[7]	90[9]	mA
DC Forward Current per Segment or DP	25[2]	40[4]	30[6]	20[8]	30[10]	mA
Operating Temperature Range	-40 to +100	-20 to +100[11]	-40 to +100			°C
Storage Temperature Range	-55 to +100					°C
Reverse Voltage per Segment or DP	3.0					V
Lead Solder Temperature for 3 Seconds (1.59 mm [0.63 in.] below seating plane)	260					°C

Notes:

1. See Figure 1 to establish pulsed conditions.
2. Derate above 80°C at 0.63 mA/°C.
3. See Figure 2 to establish pulsed conditions.
4. Derate above 46°C at 0.54 mA/°C.
5. See Figure 7 to establish pulsed conditions.
6. Derate above 53°C at 0.45 mA/°C.
7. See Figure 8 to establish pulsed conditions.
8. Derate above 81°C at 0.52 mA/°C.
9. See Figure 9 to establish pulsed conditions.
10. Derate above 39°C at 0.37 mA/°C.
11. For operation below -20°C, contact your local HP components sales office or an authorized distributor.

Electrical/Optical Characteristics at $T_A = 25°C$

Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
5300	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	600	1300		µcd	I_F = 20 mA
				1400			I_F = 100 mA Peak: 1 of 5 df
	Forward Voltage/Segment or DP	V_F		1.6	2.0	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		655		nm	
	Dominant Wavelength[3]	λ_d		640		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	12		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		345		°C/W/ Seg	

AlGaAs Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
H150	Luminous Intensity/Segment[1,2,5] (Digit Average)	I_V	9.1	16.0		mcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.8		V	I_F = 20 mA
				2.0	3.0		I_F = 100 mA
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		400		°C/W/ Seg	

High Efficiency Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
5500	Luminous Intensity/Segment[1,2,6] (Digit Average)	I_V	900	2800		µcd	I_F = 10 mA
				3700			I_F = 60 mA Peak: 1 of 6 df
	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		345		°C/W/	

Yellow

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
5700	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	600	1800		µcd	I_F = 10 mA
				2750			I_F = 60 mA Peak: 1 of 6 df
	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,7]	λ_d	581.5	586	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	40		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		345		°C/W/ Seg	

High Performance Green

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
5600	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	900	2500		µcd	I_F = 10 mA
				3100			I_F = 60 mA Peak: 1 of 6 df
	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 10 mA
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,7]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}Pin}$		345		°C/W/ Seg	

Notes:
1. Device case temperature is 25°C prior to the intensity measurement.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. For low current operation, the AlGaAs HDSP-H10X series displays are recommended. They are tested at 1 mA dc/segment and are pin for pin compatible with the HDSP-H15X series.
6. For low current operation, the HER HDSP-555X series displays are recommended. They are tested at 2 mA dc/segment and are pin for pin compatible with the HDSP-550X series.
7. The Yellow (HDSP-5700) and Green (HDSP-5600) displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

Red, AlGaAs Red

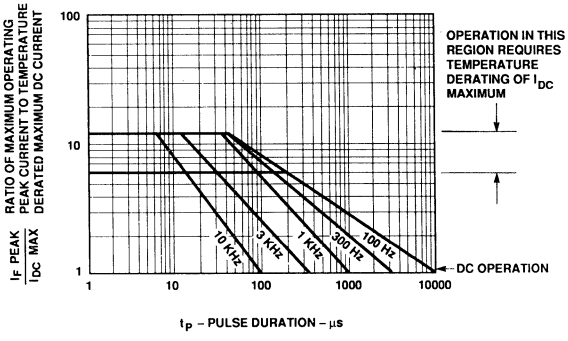


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration – Red.

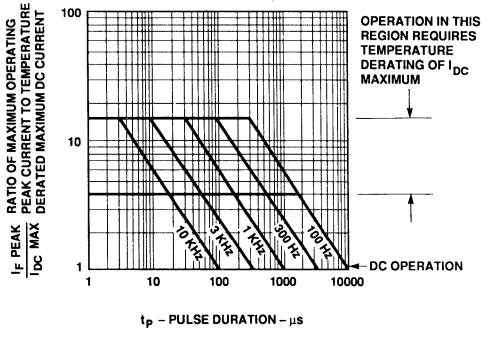


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration – AlGaAs Red.

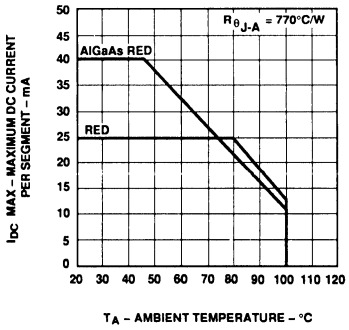


Figure 3. Maximum Allowable DC Current vs. Ambient Temperature.

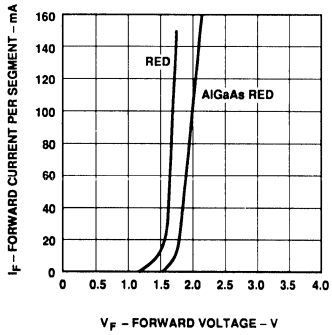


Figure 4. Forward Current vs. Forward Voltage.

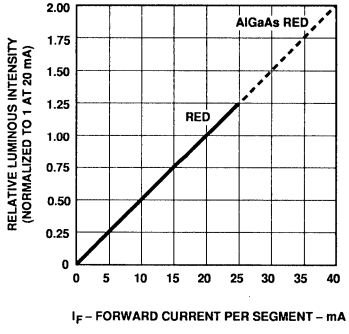


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

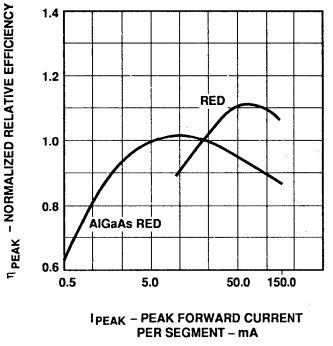


Figure 6. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Yellow, Green

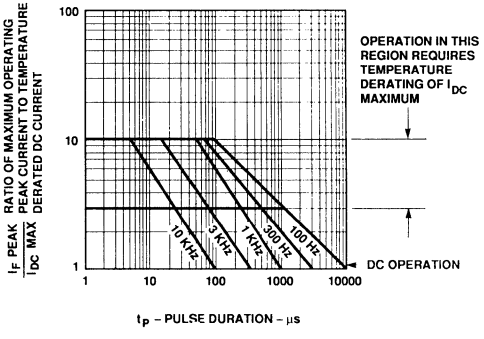


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration – HER.

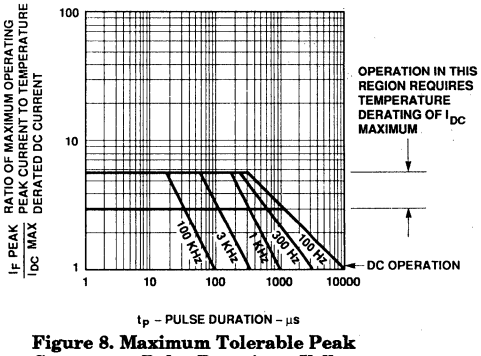


Figure 8. Maximum Tolerable Peak Current vs. Pulse Duration – Yellow.

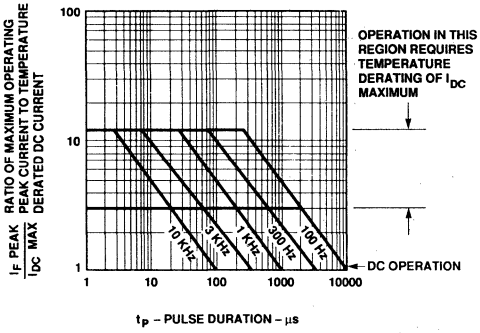


Figure 9. Maximum Tolerable Peak Current vs. Pulse Duration – Green.

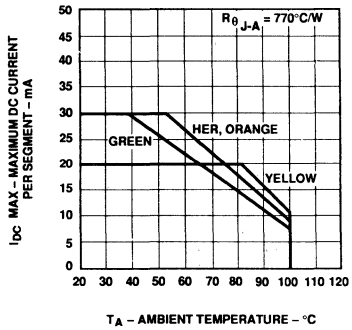


Figure 10. Maximum Allowable DC Current vs. Ambient Temperature.

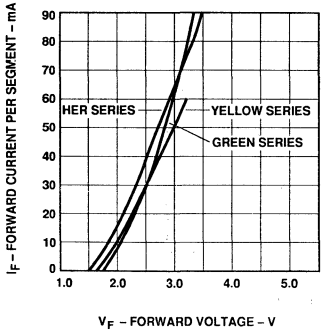


Figure 11. Forward Current vs. Forward Voltage.

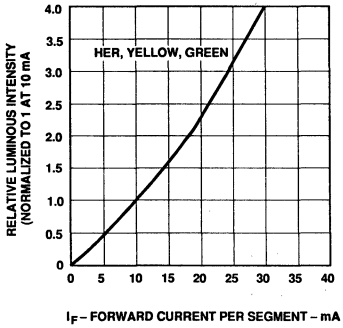


Figure 12. Relative Luminous Intensity vs. DC Forward Current.

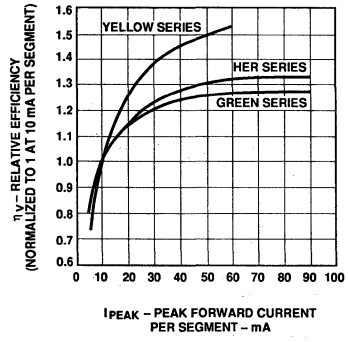


Figure 13. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Electrical/Optical

These displays use light emitting diodes, with the light from each LED optically stretched to form individual segments and decimal points. The Red HDSP-5300 series LEDs use a p-n junction diffused into a GaAsP epitaxial layer on a GaAs substrate. The AlGaAs Red HDSP-H150 series LEDs use double heterojunction AlGaAs on a GaAs substrate. HER HDSP-5500 and Yellow HDSP-5700 series LEDs have their p-n junctions diffused into a GaAsP epitaxial layer on a GaP substrate. The Green HDSP-5600 series LEDs use a liquid phase GaP epitaxial layer on GaP.

These displays are designed for strobed operation. The typical forward voltage values can be scaled from Figures 4 and 11. These values should be used to calculate the current limiting resistor value and typical power consumption. Expected maximum V_F values for driver circuit design and maximum power dissipation, may be calculated using the following V_FMAX models:

Red HDSP-5300 series
$V_F MAX = 1.8\ V + I_{Peak}\ (10\ \Omega)$
For: $I_{Peak} > 5$ mA

AlGaAs Red HDSP-H150 series
$V_F MAX = 1.8\ V + I_{Peak}\ (20\ \Omega)$
For: $I_{Peak} \leq 20$ mA
$V_F MAX = 2.0\ V + I_{Peak}\ (10\ \Omega)$
For: 20 mA $\leq I_{Peak} \leq$ 100 mA
$V_F MAX = 2.27\ V + I_{Peak}\ (7.2\ \Omega)$
For $I_{Peak} \geq 100$ mA

HER (HDSP-5500) and Yellow (5700) series
$V_F MAX = 1.6 + I_{Peak}\ (45\ \Omega)$
For: 5 mA $\leq I_{Peak} \leq 20$ mA
$V_F MAX = 1.75 + I_{Peak}\ (38\ \Omega)$
For: $I_{Peak} \geq 20$ mA

Green (HDSP-5600) series
$V_F MAX = 2.0 + I_{Peak}\ (50\ \Omega)$
For: $I_{Peak} > 5$ mA

Figures 6 and 13 allow the designer to calculate the luminous intensity at different peak and average currents. The following equation calculates intensity at different peak and average currents:

$$I_V AVG = (I_F AVG/I_F AVG\ DATA\ SHEET)(\eta_{peak})(I_V DATA\ SHEET)$$

Where:
I_VAVG is the calculated time averaged luminous intensity resulting from I_FAVG.
I_FAVG is the desired time averaged LED current.
I_FAVG DATA SHEET is the data sheet test current for I_V DATA SHEET.
η_{peak} is the relative efficiency at the peak current, scaled from Figure 6 or 13.
I_V DATA SHEET is the data sheet luminous intensity, resulting from I_FAVG DATA SHEET.

For example, what is the luminous intensity of an HDSP-5500 driven at 50 mA peak 1/5 duty factor?

$I_F AVG = (50\ mA) \bullet (0.2) = 10$ mA
I_FAVG DATA SHEET = 10 mA
$\eta_{Peak} = 1.3$
I_V DATA SHEET = 2800 µcd

Therefore

$$I_V AVG = (10\ mA/10\ mA)(1.3)(2800\ \mu cd) = 3640\ \mu cd$$

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance the readability. This is accomplished by having the OFF dots blend into the display background and the ON dots stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the dots.

Contrast enhancement may be achieved by using one of the following suggested filters:

Red and AlGaAs Red (HDSP-5300/H150)
Panelgraphic RUBY RED 60
SGL-Homalite H100-1605 RED
3M Louvered Filter R6310 RED or ND0220 GRAY

HER (HDSP-5500)
Panelgraphic SCARLET RED 65
SGL-Homalite H100-1670 RED or H100-1250 GRAY
3M Louvered Filter R6310 RED or ND0220 GRAY

Yellow (HDSP-5700)
Panelgraphic YELLOW 27 or GRAY 10
SGL-Homalite H100-1720 AMBER or H100-1250 GRAY
3M Louvered Filter ND0220 GRAY

Green (HDSP-5600)
Panelgraphic GREEN 48
SGL-Homalite H100-1440 GREEN or H100-1250 GRAY
3M Louvered Filter ND0220 GRAY

For further information on contrast enhancement please see Application Note 1015.

Mechanical

Specially developed plastics are used to optimize the displays optical performance. These plastics restrict the solvents that may be used for cleaning. Only mixtures of Freon (F113) and alcohol should be used for vapor cleaning processes. Total immersion time in the vapors is two minutes. Some suggested mixtures are Freon TE, Arklone A or K, or Genesolv DES. A 60°C (140°F) water cleaning process may also be used. This process includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a water rinse, and a thorough air dry. Room temperature cleaning may be done with Freon T-E35 or T-P35, Ethanol, Isopropanol, or water with a mild detergent.

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloro-ethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

For further information on soldering LEDs please refer to Application Note 1027.

HEWLETT PACKARD

20 mm (0.8 inch) Seven Segment Displays

Technical Data

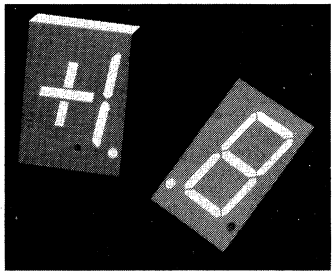
HDSP-3400, 3401, 3403, 3405, 3406
HDSP-N150, N151, N153, N155, N156
HDSP-3900, 3901, 3903, 3905, 3906
HDSP-4200, 4201, 4203, 4205, 4206
HDSP-8600, 8601, 8603, 8605, 8606

Features

- **Industry Standard Size**
- **Industry Standard Pinout**
  15.24 mm (0.6 in.) DIP Leads on 2.54 mm (0.1 in.) Centers
- **Choice of Colors**
  Red, AlGaAs Red, High Efficiency Red, Yellow, Green
- **Excellent Appearance**
  Evenly Lighted Segments
  Mitered Corners on Segments
  Gray Package Gives Optimum Contrast
  ±50° Viewing Angle
- **Design Flexibility**
  Common Anode or Common Cathode
  Left and Right Hand Decimal Points
  ±1. Overflow Character
- **Categorized for Luminous Intensity**
  Yellow and Green
  Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **High Light Output**
- **High Peak Current**
- **Excellent for Long Digit String Multiplexing Intensity and Color Selection Option**
  See Intensity and Color Selected Displays Data Sheet
- **Sunlight Viewable AlGaAs**

Description

The 20 mm (0.8 inch) LED seven segment displays are designed for viewing distances up to 10 metres (33 feet). These devices use an industry standard size package and pinout. All devices are available as either common anode or common cathode.



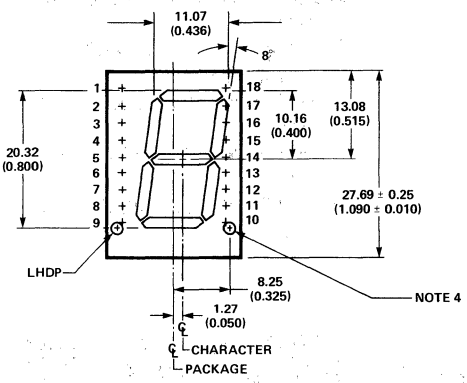
These displays are ideal for most applications. Pin for pin equivalent displays are also available in a low current design. The low current displays are ideal for portable applications. For additional information see the Low Current Seven Segment Displays data sheet.

Devices

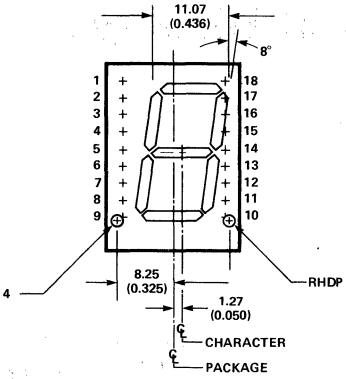
Red HDSP-	AlGaAs[1] HDSP-	HER HDSP-	Yellow HDSP-	Green HDSP-	Description	Package Drawing
3400	N150	3900	4200	8600	Common Anode Left Hand Decimal	A
3401	N151	3901	4201	8601	Common Anode Right Hand Decimal	B
3403	N153	3903	4203	8603	Common Cathode Right Hand Decimal	C
3405	N155	3905	4205	8605	Common Cathode Left Hand Decimal	D
3406	N156	3906	4206	8606	Universal ±1. Overflow[2]	E

Notes:
1. These displays are recommended for high ambient light operation. Please refer to the HDSP-N10X AlGaAs data sheet for low current operation.
2. Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram E.

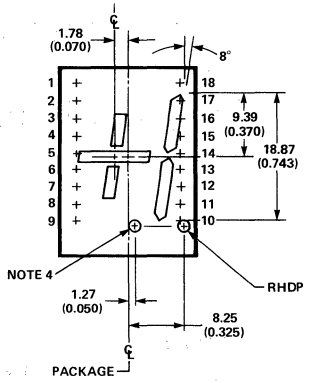
Package Dimensions



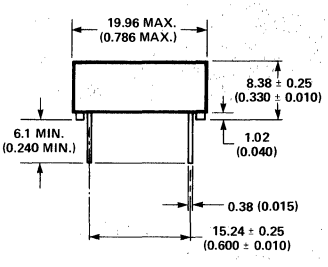
FRONT VIEW A, D



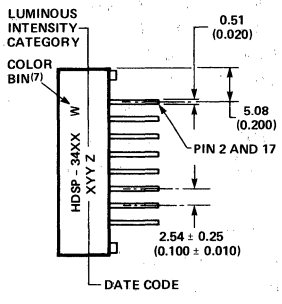
FRONT VIEW B, C



FRONT VIEW E



END VIEW

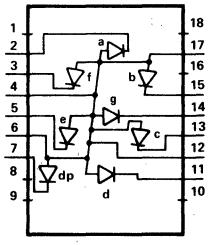


SIDE VIEW

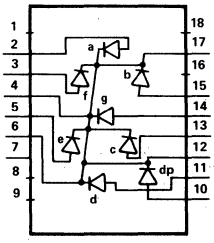
Pin	Function A	B	C	D	E
1	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
2	CATHODE a	CATHODE a	ANODE a	ANODE a	CATHODE a
3	CATHODE f	CATHODE f	ANODE f	ANODE f	ANODE d
4	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE d
5	CATHODE e	CATHODE e	ANODE e	ANODE e	CATHODE c
6	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE e
7	CATHODE dp	NO. CONNEC.	NO. CONNEC.	ANODE dp	ANODE e
8	NO PIN	NO PIN	NO PIN	NO PIN	CATHODE dp
9	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
10	NO PIN	CATHODE dp	ANODE dp	NO PIN	ANODE dp
11	CATHODE d	CATHODE d	ANODE d	ANODE d	CATHODE dp
12	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE b
13	CATHODE c	CATHODE c	ANODE c	ANODE c	ANODE b
14	CATHODE g	CATHODE g	ANODE g	ANODE g	ANODE c
15	CATHODE b	CATHODE b	ANODE b	ANODE b	ANODE a
16	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
17	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE a
18	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN

NOTES:
1. DIMENSIONS IN MILLIMETERS AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. REDUNDANT ANODES.
4. UNUSED dp POSITION.
5. SEE INTERNAL CIRCUIT DIAGRAM.
6. REDUNDANT CATHODES.
7. FOR HDSP-4200/-8600 SERIES PRODUCT ONLY.

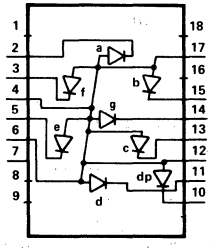
Internal Circuit Diagram



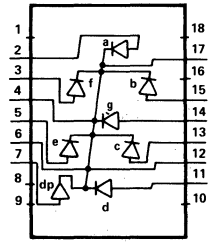
A



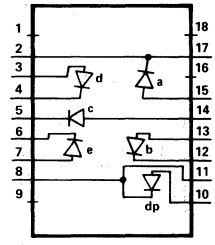
B



C



D



E

Absolute Maximum Ratings

Description	Red HDSP-3400 Series	AlGaAs Red HDSP-N150 Series	HER HDSP-3900 Series	Yellow HDSP-4200 Series	Green HDSP-8600 Series	Units
Average Power per Segment or DP	115	96	105	105	105	mW
Peak Forward Current per Segment or DP	200[1]	160[3]	135[5]	135[5]	90[7]	mA
DC Forward Current per Segment or DP	50[2]	40[4]	40[6]	40[6]	30[8]	mA
Operating Temperature Range	-40 to +85	-40 to +100	-40 to +85		-20 to +85	°C
Storage Temperature Range	-55 to +100					°C
Reverse Voltage per Segment or DP	3.0					V
Lead Solder Temperature for 3 Seconds (1.59 mm [0.63 in.] below seating plane)	260					°C

Notes:
1. See Figure 1 to establish pulsed conditions.
2. Derate above 45°C at 0.83 mA/°C.
3. See Figure 2 to establish pulsed conditions.
4. Derate above 55°C at 0.8 mA/°C.
5. See Figure 7 to establish pulsed conditions.
6. Derate above 50°C at 0.73 mA/°C.
7. See Figure 8 to establish pulsed conditions.
8. Derate above 50°C at 0.54 mA/°C.

Electrical/Optical Characteristics at T_A = 25°C

Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-3400	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	500	1200		µcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.6	2.0	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		655		nm	
	Dominant Wavelength[3]	λ_d		640		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	20		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		375		°C/W	

AlGaAs Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-N150	Luminous Intensity/Segment[1,2,5] (Digit Average)	I_V	6.0	14.0		mcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.8		V	I_F = 20 mA
				2.0	3.0	V	I_F = 100 mA
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		430		°C/W/ Seg	

High Efficiency Red

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-3900	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	3350	7000		µcd	I_F = 100 mA Peak: 1 of 5 df
				4800		µcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.6	3.5	V	I_F = 100 mA
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	25		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		375		°C/W/ Seg	

Yellow

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-4200	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	2200	7000		µcd	I_F = 100 mA Peak: 1 of 5 df
				3400		µcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.6	3.5	V	I_F = 100 mA
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,6]	λ_d	581.5	586	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	25.0		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		375		°C/W/ Seg	

Green

Device Series	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
HDSP-8600	Luminous Intensity/Segment[1,2] (Digit Average)	I_V	680	1500		µcd	I_F = 10 mA
				1960		µcd	I_F = 50 mA Peak: 1 of 5 df
	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 10 mA
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,6]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50.0		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		375		°C/W/ Seg	

Notes:
1. Case temperature of the device immediately prior to the intensity measurement is 25°C.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. For low current operation, the AlGaAs Red HDSP-N100 series displays are recommended. They are tested at 1 mA dc/ segment and are pin for pin compatible with the HDSP-N150 series.
6. The Yellow (HDSP-4200) and Green (HDSP-8600) displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

Red, AlGaAs Red

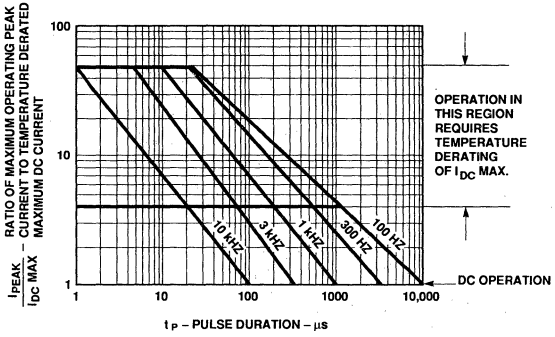


Figure 1. Maximum Allowable Peak Current vs. Pulse Duration – Red.

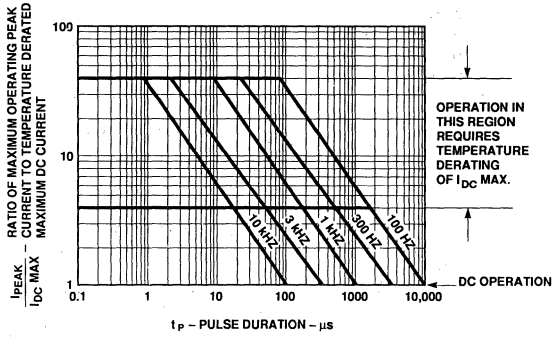


Figure 2. Maximum Allowed Peak Current vs. Pulse Duration – AlGaAs Red.

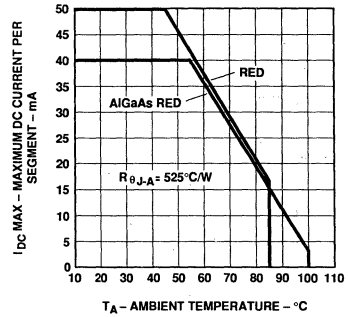


Figure 3. Maximum Allowable DC Current vs. Ambient Temperature.

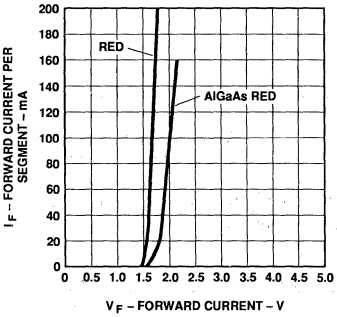


Figure 4. Forward Current vs. Forward Voltage.

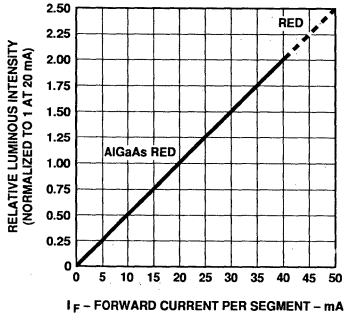


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

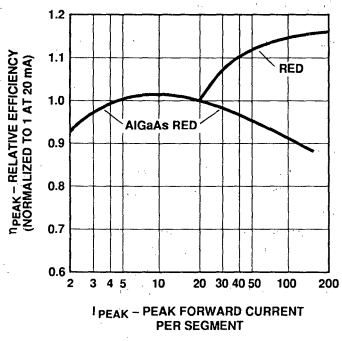


Figure 6. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Yellow, Green

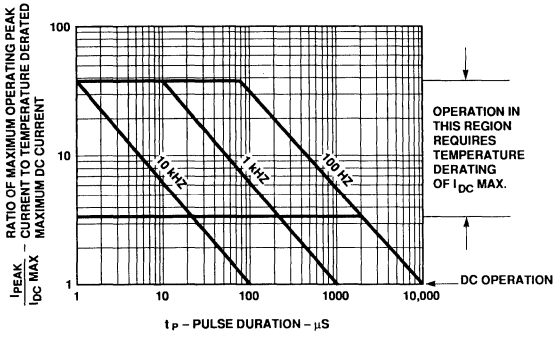


Figure 7. Maximum Allowed Peak Current vs. Pulse Duration – HER, Yellow.

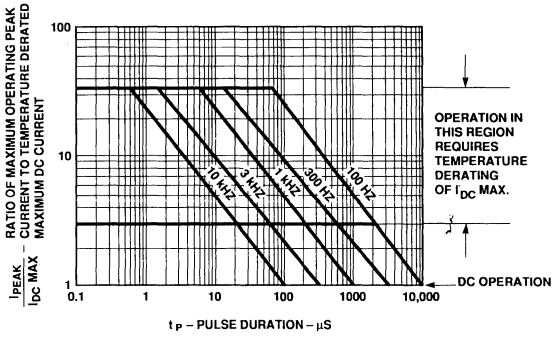


Figure 8. Maximum Allowed Peak Current vs. Pulse Duration – Green.

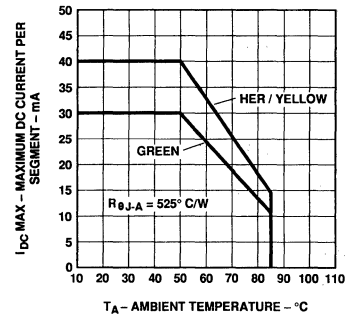


Figure 9. Maximum Allowable DC Current vs. Ambient Temperature.

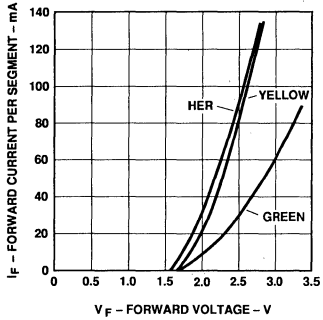


Figure 10. Forward Current vs. Forward Voltage.

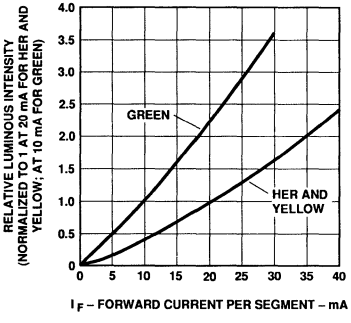


Figure 11. Relative Luminous Intensity vs. DC Forward Current.

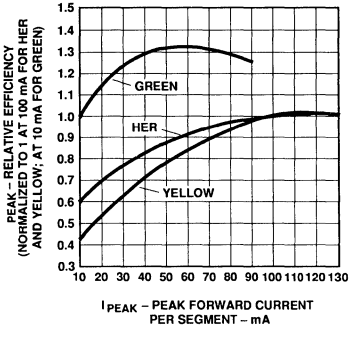


Figure 12. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Electrical/Optical

These displays use light emitting diodes, with the light from each LED optically stretched to form individual segments and decimal points. The Red HDSP-3400 series LEDs use a p-n junction diffused into a GaAsP epitaxial layer on a GaAs substrate. The AlGaAs Red HDSP-N150 series LEDs use double heterojunction AlGaAs on a GaAs substrate. HER HDSP-3900 and Yellow HDSP-4200 series LEDs have their p-n junctions diffused into a GaAsP epitaxial layer on a GaP substrate. The Green HDSP-8600 series LEDs use a liquid phase GaP epitaxial layer on GaP.

These displays are designed for strobed operation. The typical forward voltage values can be scaled from Figures 4 and 10. These values should be used to calculate the current limiting resistor value and typical power consumption. Expected maximum V_F values for driver circuit design and maximum power dissipation, may be calculated using the following V_FMAX models:

Red HDSP-3400 series

$V_F MAX = 1.8\ V + I_{Peak}\ (10\ \Omega)$
For: $I_{Peak} > 5$ mA

AlGaAs Red HDSP-N150 series

$V_F MAX = 1.8\ V + I_{Peak}\ (20\ \Omega)$
For: $I_{Peak} \leq 20$ mA
$V_F MAX = 2.0\ V + I_{Peak}\ (10\ \Omega)$
For: 20 mA $\leq I_{Peak} \leq$ 100 mA
$V_F MAX = 2.27\ V + I_{Peak}\ (7.2\ \Omega)$
For $I_{Peak} \geq 100$ mA

HER (HDSP-3900) and Yellow (HDSP-4200) series

$V_F MAX = 1.9 + I_{Peak}\ (21.8\ \Omega)$
For: 10 mA $\leq I_{Peak} \leq$ 30 mA
$V_F MAX = 2.15 + I_{Peak}\ (13.5\ \Omega)$
For: $I_{Peak} \geq 30$ mA

Green (HDSP-8600) series

$V_F MAX = 2.0\ V + I_{Peak}\ (50\ \Omega)$
For: $I_{Peak} > 5$ mA

Figures 6 and 12 allow the designer to calculate the luminous intensity at different peak and average currents. The following equation calculates intensity at different peak and average currents:

$I_V AVG = (I_F AVG / I_F AVG\ DATA\ SHEET)(\eta_{peak})(I_V DATA\ SHEET)$

Where:

$I_V AVG$ is the calculated time averaged luminous intensity resulting from $I_F AVG$

$I_F AVG$ is the desired time averaged LED current

$I_F AVG$ DATA SHEET is the data sheet test current for I_VDATA SHEET

η_{peak} is the relative efficiency at the peak current, scaled from Figure 6 or 12

I_V DATA SHEET is the data sheet luminous intensity, resulting from $I_F AVG$ DATA SHEET

For example, what is the luminous intensity of an HER HDSP-3900 driven at 135 mA peak 1/6 duty factor?

$I_F AVG = (135\ mA)(1/6) = 22.5\ mA$
$I_F AVG$ DATA SHEET = 20 mA
$\eta_{Peak} = 1.03$
I_V DATA SHEET = 7000 µcd

Therefore

$I_V AVG = (22.5\ mA/20\ mA)(1.03)(7000\ \mu cd) = 8111\ \mu cd$

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance the readability. This is accomplished by having the OFF dots blend into the display background and the ON dots stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the dots.

Contrast enhancement may be achieved by using one of the following suggested filters:

Red and AlGaAs Red (HDSP-3400/N150)
Panelgraphic RUBY RED 60
SGL-Homalite H100-1605 RED
3M Louvered Filter R6310 RED or ND0220 GRAY

HER (HDSP-3900)
Panelgraphic SCARLET RED 65
SGL-Homalite H100-1670 RED or H100-1250 GRAY
3M Louvered Filter R6310 RED or ND0220 GRAY

Yellow (HDSP-4200)
Panelgraphic YELLOW 27 or GRAY 10
SGL-Homalite H100-1720 AMBER or H100-1250 GRAY
3M Louvered Filter ND0220 GRAY

Green (HDSP-8600)
Panelgraphic GREEN 48
SGL-Homalite H100-1440 GREEN or H100-1250 GRAY
3M Louvered Filter ND0220 GRAY

For further information on contrast enhancement please see Application Note 1015.

Mechanical

Specifically developed plastics are used to optimize the displays optical performance. These plastics restrict the solvents that may be used for cleaning. Only mixtures of Freon (F113) and alcohol should be used for vapor cleaning processes. Total immersion time in the vapors is two minutes. Some suggested mixtures are Freon TE, Arklone A or K, or Genesolv DES. A 60°C (140°F) water cleaning process may also be used. This process includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a water rinse, and a thorough air dry. Room temperature cleaning may be done with Freon T-E35 or T-P35, Ethanol, Isopropanol, or water with a mild detergent.

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

For further information on soldering LEDs please refer to Application Note 1027.

HEWLETT PACKARD

2.3 Inch AlGaAs Red 5 x 8 Dot Matrix Alphanumeric Displays

Technical Data

HDSP-P101/HDSP-P151
HDSP-P103/HDSP-P153

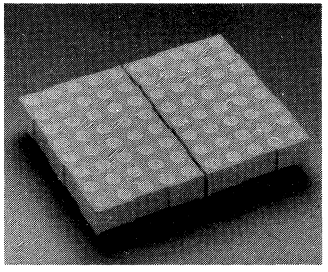
Features

- **Very Large Character Height**
- **Easily Expandable to Larger Displays**
- **X-Y Stackable**
- **Wide Viewing Angle**
- **Ideal for Graphics Panels**
- **Exceptional Brightness**
  HDSP-P15X Series Designed for High Ambient Light Conditions
- **Categorized for Intensity**
- **Mechanically Rugged**

Description

The large 5 x 8 dot matrix alphanumeric display uses newly developed Double Heterojunction (DH) AlGaAs/GaAs material technology. This LED material has outstanding light output efficiency over a wide range of drive currents. The color is deep red at the dominant wavelength of 637 nanometres. The 2.3 inch (58.4 mm) display is ideal for applications such as graphics displays and moving message panels.

The HDSP-P10X and HDSP-P15X have different optical characteristics that are optimized for different applications. The HDSP-P10X and HDSP-P15X displays differ in the amount of diffusant. The HDSP-P10X uses a large amount of diffusant. This causes the dots to have a uniform appearance across the light emitting area. The HDSP-P15X uses a smaller amount of diffusant. This causes the dots to appear brightest in the center. The HDSP-P15X is designed for high ambient light conditions or long viewing distances, where brightness is more important than uniformity.



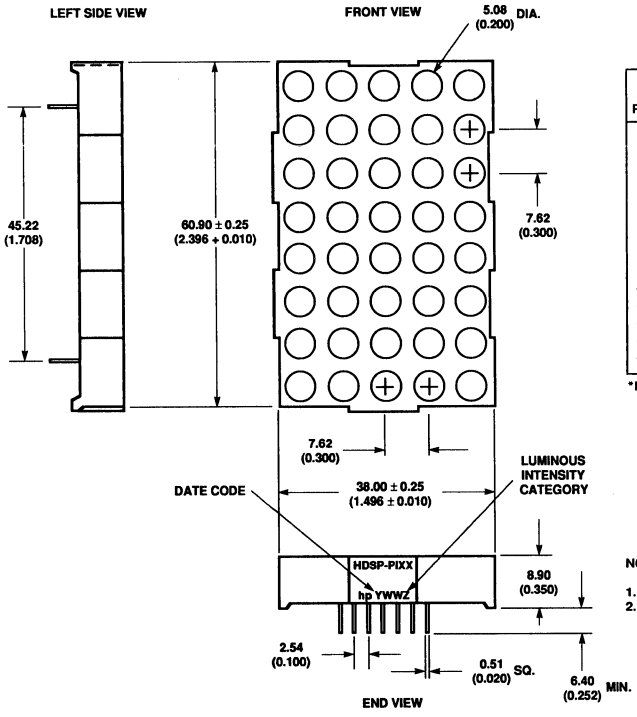
Absolute Maximum Ratings at 25°C

Average Power per Dot	36 mW
Peak Forward Current per Dot[1]	125 mA
Average Forward Current per Dot	11 mA
Operating Temperature Range	-20°C to +85°C
Storage Temperature Range	-20°C to +85°C
Reverse Voltage per Dot	3 V
Lead Solder Temperature (1.59 mm [1/16 inch] below seating plane)	260°C for 3 sec.

Note:

1. Do not exceed maximum average current per dot.

Package Dimensions



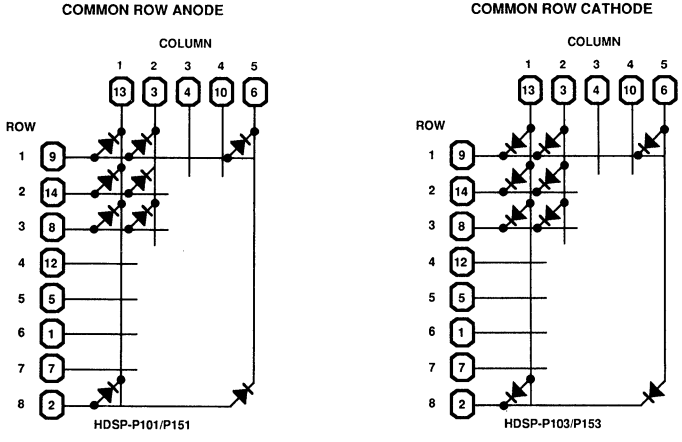
PIN	FUNCTION	
	HDSP-P101/P151	HDSP-P103/P153
1	ROW 6 ANODE	ROW 6 CATHODE
2	ROW 8 ANODE	ROW 8 CATHODE
3	COLUMN 2 CATHODE	COLUMN 2 ANODE
4*	COLUMN 3 CATHODE	COLUMN 3 ANODE
5	ROW 5 ANODE	ROW 5 CATHODE
6	COLUMN 5 CATHODE	COLUMN 5 ANODE
7	ROW 7 ANODE	ROW 7 CATHODE
8	ROW 3 ANODE	ROW 3 CATHODE
9	ROW 1 ANODE	ROW 1 CATHODE
10	COLUMN 4 CATHODE	COLUMN 4 ANODE
11*	COLUMN 3 CATHODE	COLUMN 3 ANODE
12	ROW 4 ANODE	ROW 4 CATHODE
13	COLUMN 1 CATHODE	COLUMN 1 ANODE
14	ROW 2 ANODE	ROW 2 CATHODE

*NOTE: PIN 4 AND 11 ARE INTERNALLY CONNECTED.

NOTES:

1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.

Internal Circuit Diagram



Electrical/Optical Characteristics at $T_A = 25°C$

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity/Dot (Digit Average)[1]	I_V				µcd	I_F = 50 mA: 1/5 duty factor (10 mA Avg.)
HDSP-P101		5000	12000			
HDSP-P151[2]		6000	15000			
Peak Wavelength	λ_{PEAK}		645		nm	
Dominant Wavelength[3]	λ_d		637		nm	
Forward Voltage/Dot	V_F		1.9	2.5	V	I_F = 50 mA
Reverse Voltage/Dot[4]	V_R	3.0	15.0		V	I_R = 100 µA
Temperature Coefficient of V_F/Dot	$\Delta V_F/°C$		-2.0		mV/°C	
Thermal Resistance LED Junction-to-Pin per Package	$R\theta_{J\text{-}PIN}$		18		°C/W/Pack	

Notes:
1. The displays are categorized for luminous intensity with the intensity category designated by a letter on the bottom end of the package. The luminous intensity minimum and categories are determined by computing the numerical average of the individual dot intensities.
2. The HDSP-P151 is designed for high ambient light operation. Mixing the HDSP-P101 and the HDSP-P151 displays may cause digit to digit mismatch.
3. The dominant wavelength, λ_d, is derived from the C.I.E. Chromaticity diagram and is that single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.

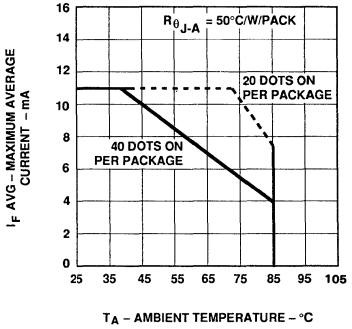


Figure 1. Maximum Allowable Average Current per Dot vs. Ambient Temperature. T_J MAX = 110°C.

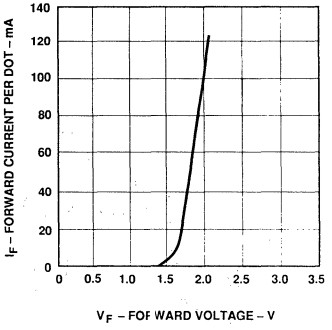


Figure 2. Forward Current vs. Forward Voltage.

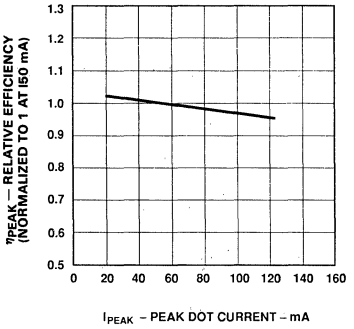


Figure 3. Relative Luminous Efficiency (per Dot) vs. Peak Current per Dot.

Operational Considerations

Electrical Description

These display devices are composed of light emitting diodes, with the light from each LED optically stretched to form individual dots.

These display devices are well suited for strobed operation. The typical forward voltage can be scaled from Figure 2. These values should be used to calculate the current limiting resistor value and the typical power dissipation. Expected maximum V_F values, for driver circuit design and maximum power dissipation, may be calculated using the following V_FMAX model:

V_FMAX = 1.8 V + I_{Peak} (20 Ω)
For: $I_{Peak} \leq 20$ mA

V_FMAX = 2.0 V + I_{Peak} (10 Ω)
For: $I_{Peak} \geq 20$ mA

Figure 3 allows the designer to calculate the luminous intensity at different peak and average currents. The following equation calculates intensity at different peak and average currents:

I_VAVG = (I_FAVG/I_FAVG DATA SHEET)(η_{peak})(I_VDATA SHEET)

Where:
I_FAVG is the desired time averaged LED current.
I_FAVG DATA SHEET is the time averaged data sheet test current for I_VDATA SHEET.
η_{peak} is the relative efficiency at the peak current, scaled from Figure 3.
I_VAVG is the calculated time averaged luminous intensity resulting from I_FAVG.

For example, what is the luminous intensity of an AlGaAs Red (HDSP-P15X) driven at 100 mA peak 1/100 duty factor?

I_FAVG = (100 mA)(0.01) = 1 mA
I_FAVG DATA SHEET = 10 mA
η_{Peak} = 0.97
I_V DATA SHEET = 15000 µcd

Therefore

I_VAVG = (1 mA/10 mA)(0.97)
(15000 µcd)
= 1455 µcd

Thermal Considerations

The device thermal resistance may be used to calculate the junction temperature of the central LED. The following equation calculates the junction temperature of the central (hottest) LED.

$T_J = T_A + (P_D)(R\theta_{J\text{-}A})(N)$
$P_D = (V_F\text{MAX})(I_F\text{AVG})$
$R\theta_{J\text{-}A} = R\theta_{J\text{-}PIN} + R\theta_{PIN\text{-}A}$

T_J is the junction temperature of the central LED.
T_A is the ambient temperature.
P_D is the power dissipated by one LED.
N is the number of LEDs on per character.
V_FMAX is calculated using the appropriate V_F model.
$R\theta_{J\text{-}A}$ is the package thermal resistance from the central LED to the ambient.
$R\theta_{J\text{-}PIN}$ is the package thermal resistance from the central LED to the pin.
$R\theta_{PIN\text{-}A}$ is the thermal resistance from the pin to the ambient.

For example, what is the maximum ambient temperature an HDSP-P1XX can operate with the following conditions:

I_{Peak} = 125 mA
I_FAVG = 11 mA
$R\theta_{J\text{-}A}$ = 50°C/W
N = 40
T_JMAX = 110°C

V_FMAX = 2.0 V + (0.125 A)
(10 Ω) = 3.25 V
P_D = (3.25 V)(0.011 A)
= 0.03575 W
T_A = 110°C - (50°C/W)
(0.03575)(40) = 38.5°C

The maximum number of dots on for the ASCII character set is 20. What is the maximum ambient temperature an HDSP-P1XX can operate with the following conditions:

I_{Peak} = 125 mA
I_FAVG = 11 mA
$R\theta_{J\text{-}A}$ = 50°C/W
N = 20
T_JMAX = 110°C

V_FMAX = 2.0 V + (0.125 A)
(10 Ω) = 3.25 V
P_D = (3.25 V)(0.011 A)
= 0.03575 W
T_A = 110°C - (50°C/W)
(0.03575)(20) = 74.3°C

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance the readability. This is accomplished by having the OFF dots blend into the display background and the ON dots stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the dots.

Contrast enhancement may be achieved by using one of the following suggested filters:

Panelgraphic RUBY RED 60 or GRAY 10
SGL-Homalite H100-1605 RED or H100-1650 GRAY
3M Louvered Filter R6310 RED or ND0220 GRAY

For further information on contrast enhancement please see Application Note 1015.

Mechanical

Specially developed plastics are used to optimize the displays optical performance. These plastics restrict the solvents that may be used for cleaning. Only mixtures of Freon (F113) and alcohol should be used for vapor cleaning processes. Total immersion time in the vapors is two minutes. Some suggested mixtures are Freon TE, Arklone A or K, or Genesolv DI-15 or DE-15. A 60°C (140°F) water cleaning process may also be used. This process includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a water rinse, and a thorough air dry.

Room temperature cleaning may be done with Freon T-E35 or T-P35, Ethanol, Isopropanol, or water with a mild detergent.

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

HEWLETT PACKARD

HEXADECIMAL AND NUMERIC DISPLAYS

5082-7300
5082-7302
5082-7304
5082-7340

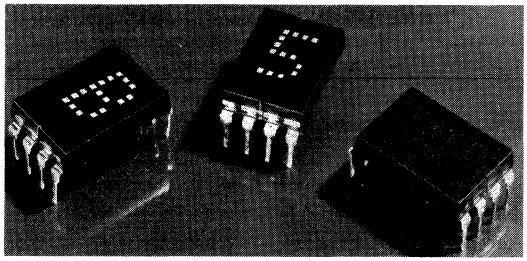
Features

- **NUMERIC**
  5082-7300/-7302
  0-9, Test State, Minus Sign, Blank States, Decimal Point
  7300 Right Hand D. P.
  7302 Left Hand D.P.
- **HEXADECIMAL**
  5082-7340
  0-9, A-F, Base 16 Operation, Blanking Control, Conserves Power, No Decimal Point
- **TTL COMPATIBLE**
- **INCLUDES DECODER/DRIVER WITH MEMORY**
  8421 Positive Logic Input
- **4 x 7 DOT MATRIX ARRAY**
  Shaped Character, Excellent Readability
- **STANDARD DUAL-IN-LINE PACKAGE INCLUDING CONTRAST FILTER**
  15.2 mm x 10.2 mm (0.6 inch x 0.4 inch)
- **CATEGORIZED FOR LUMINOUS INTENSITY**

Description

The HP 5082-7300 series solid state numeric and hexadecimal displays with on-board decoder/driver and memory provide 7.4 mm (0.29 inch) displays for reliable, low-cost methods of displaying digital information.

The 5082-7300 numeric display decodes positive 8421 BCD logic inputs into characters 0-9, a "—" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point.



The 5082-7302 is the same as the 5082-7300, except that the decimal point is located on the left-hand side of the digit.

The 5082-7340 hexadecimal display decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LEDs off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

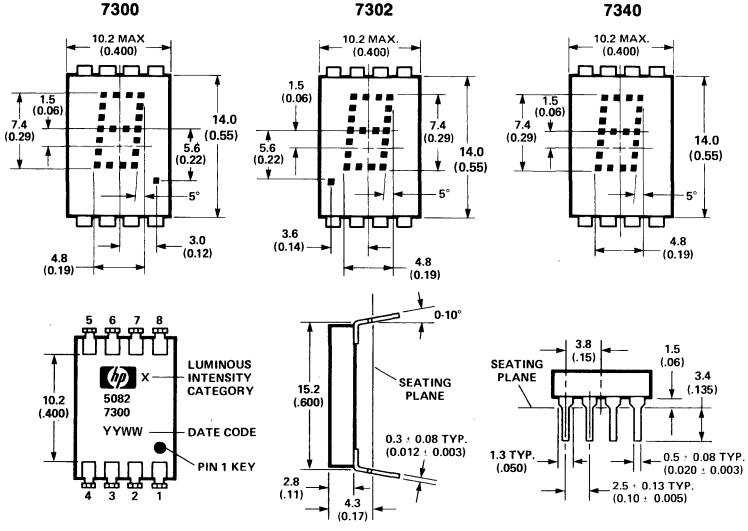
The 5082-7304 is a (±1) overrange display including a right-hand decimal point.

The ESD susceptibility of these IC devices is Class A of MIL-STD-883 or Class 2 of DOD-STD-1686 and DOD-HDBK-263.

Applications

Typical applications include point-of-sale terminals, instrumentation, and computer system.

Package Dimensions



Pin	Function	
	5082-7300 and 7302 Numeric	5082-7340 Hexadecimal
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal Point	Blanking Control
5	Latch Enable	Latch Enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

Notes:
1. Dimensions in millimeters and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±0.38 mm (± 0.015 inch).
3. Digit center line is ±0.25 mm (±0.01 inch) from package center line.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	-40	+100	°C
Operating temperature, case[1,2]	T_C	-20	+85	°C
Supply voltage[3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	+7.0	V
Voltage applied to blanking input[7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ≤ 5 seconds			230	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, case	T_C	-20		+85	°C
Enable Pulse Width	t_W	120			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics (T_C = -20° C to +85° C, Unless Otherwise Specified)

Description	Symbol	Test Conditions	Min.	Typ.[4]	Max.	Unit
Supply Current	I_{CC}	V_{CC} = 5.5 V (characters		112	170	mA
Power dissipation	P_T	"5." or "B" displayed)		560	935	mW
Luminous intensity per LED (Digit average)[5,6]	I_v	V_{CC}=5.0V, T_C = 25° C	32	70		μcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked[7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked[7]	V_{BH}		3.5			V
Blanking low-level input current[7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			20	μA
Blanking high-level input current[7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			2.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+250	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+250	μA
Peak wavelength	λ_{PEAK}	T_C = 25° C		655		nm
Dominant Wavelength[8]	λ_d	T_C = 25° C		640		nm
Weight				0.8		gm

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA} = 50° C/W; Θ_{JC} = 15° C/W; 2. Θ_{CA} of a mounted display should not exceed 35° C/W for operation up to T_C =+85° C. 3.Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC} = 5.0 Volts, T_A = 25° C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific case temperature, $I_V(T_C)$ may be calculated from this relationship: $I_V(T_C) = I_V$ (25° C) e $[-0.0188/°C(T_{C-25°C})]$ 7. Applies only to 7340. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

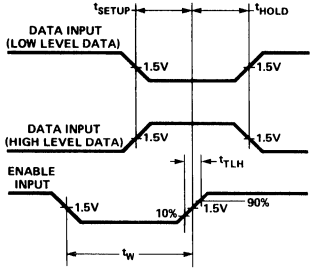


Figure 1. Timing Diagram of 5082-7300 Series Logic.

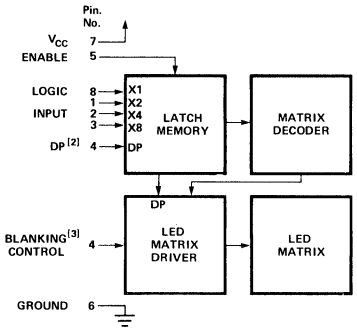


Figure 2. Block Diagram of 5082-7300 Series Logic.

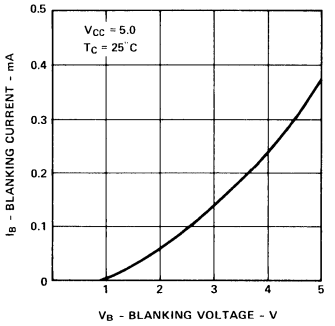


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7340.

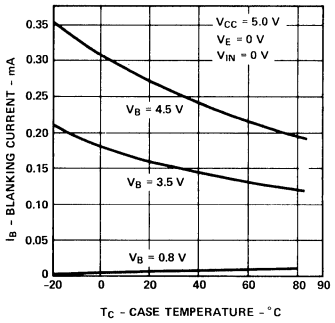


Figure 4. Typical Blanking Control Input Current vs. Temperature, 5082-7340.

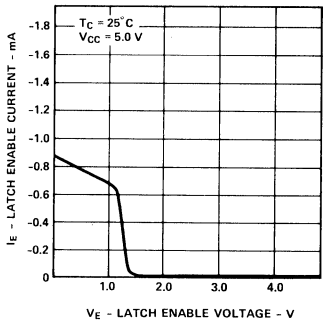


Figure 5. Typical Latch Enable Input Current vs. Voltage for the 5082-7300 Series Devices.

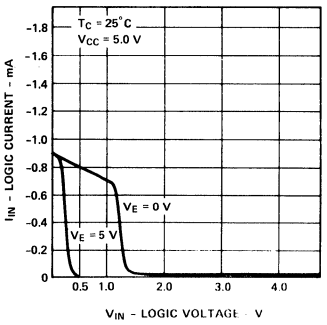


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage for the 5082-7300 Series Devices. Decimal Point Applies to 5082-7300 and -7302 Only.

TRUTH TABLE

BCD DATA[1]				5082-7300/7302	5082-7340
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	-	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	-	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F

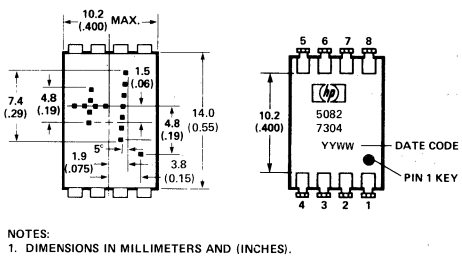
DECIMAL PT.[2]	ON	V_{DP} = L
	OFF	V_{DP} = H
ENABLE[1]	LOAD DATA	V_E = L
	LATCH DATA	V_E = H
BLANKING[3]	DISPLAY-ON	V_B = L
	DISPLAY-OFF	V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7300 and 5082-7302 displays.
3. The blanking control input, B, pertains only to the 5082-7340 hexadecimal display. Blanking input has no effect upon display memory.

Solid State Over Range Display

For display applications requiring a ±, 1, or decimal point designation, the 5082-7304 over range display is available. This display module comes in the same package as the 5082-7300 series numeric display and is completely compatible with it.

Package Dimensions



PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{CC}
8	Minus/Plus

NOTES:
1. DIMENSIONS IN MILLIMETERS AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±0.38 MM (±0.015 INCHES).

5082-7304

TRUTH TABLE FOR 5082-7304

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 7 cutoff.
H: Line switching transistor in Figure 7 saturated.
X: 'Don't care'

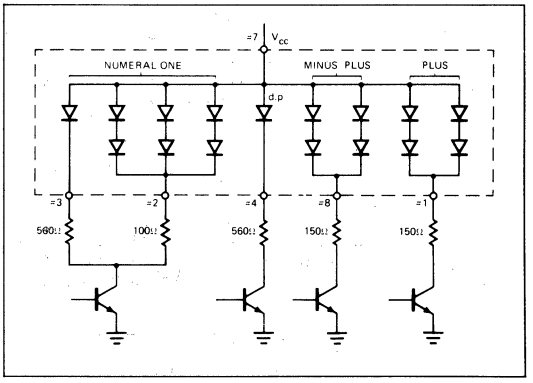


Figure 7. Typical Driving Circuit for 5082-7304

Recommended Operating Conditions

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 7 for recommended resistor values.

Absolute Maximum Ratings

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	-40	+100	°C
Operating temperature, case	T_C	-20	+85	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

Electrical/Optical Characteristics

5082-7358 (T_C = -20° C to +85° C, Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		250	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	32	70		μcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λ_d	T_C = 25°C		640		nm
Weight				0.8		gm

HEWLETT PACKARD

HEXADECIMAL AND NUMERIC DISPLAYS FOR INDUSTRIAL APPLICATIONS

5082-7356
5082-7357
5082-7358
5082-7359

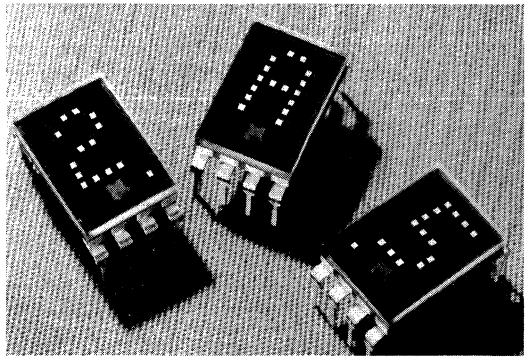
Features

- **CERAMIC/GLASS PACKAGE**
- **ADDED RELIABILITY**
- **NUMERIC 5082-7356/-7357**
  0-9, Test State, Minus Sign, Blank States, Decimal Point
  7356 Right Hand D.P., 7357 Left Hand D.P.
- **HEXADECIMAL 5082-7359**
  0-9, A-F, Base 16 Operation, Blanking Control, Conserves Power, No Decimal Point
- **TTL COMPATIBLE**
- **INCLUDES DECODER/DRIVER WITH MEMORY**
  8421 Positive Logic Input
- **4 x 7 DOT MATRIX ARRAY**
  Shaped Character, Excellent Readability
- **STANDARD DUAL-IN-LINE PACKAGE**
  15.2 mm x 10.2 mm (0.6 inch x 0.4 inch)
- **CATEGORIZED FOR LUMINOUS INTENSITY**

Description

The HP 5082-735X series solid state numeric and hexadecimal displays with on-board decoder/driver and memory provide 7.4 mm (0.29 inch) displays for use in adverse industrial environments.

The 5082-7356 numeric display decodes positive 8421 BCD logic inputs into characters 0-9 "—" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point.



The 5082-7357 is the same as the 5082-7356, except that the decimal point is located on the left-hand side of the digit.

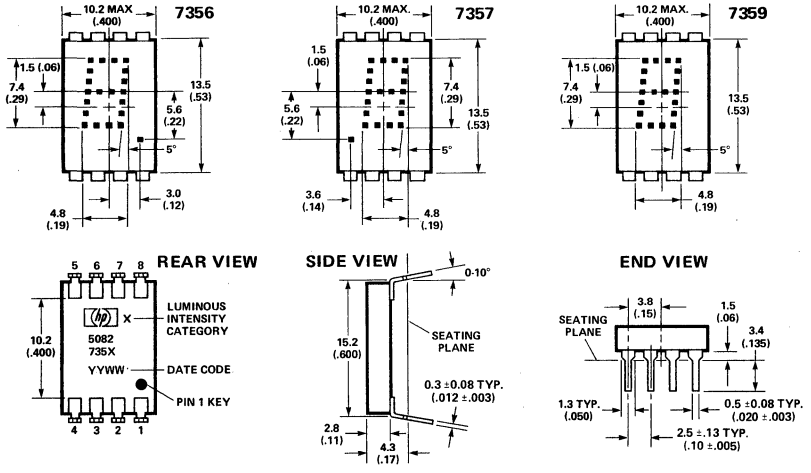
The 5082-7359 hexadecimal display decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

The 5082-7358 is a (±1) overrange display including a right-hand decimal point.

Applications

Typical applications include control systems, instrumentation, communication systems, and transportation equipment.

Package Dimensions



PIN	FUNCTION	
	5082-7356 AND 7357 NUMERIC	5082-7359 HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimeters and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ± 0.38mm (±0.015 in.)
3. Digit center line is ± 0.25mm (±0.01 in.) from package center line.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1,2]	T_A	−55	+100	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	+7.0	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ⩽ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient	T_A	-55		+85	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics (T_A = -55° C to +85° C, Unless Otherwise Specified)

Description	Symbol	Test Conditions	Min.	Typ.[4]	Max.	Unit
Supply Current	I_{CC}	V_{CC} = 5.5 V (characters "5." or "B" displayed)		112	170	mA
Power dissipation	P_T			560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_A=25°C	40	85		μcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			50	μA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			1.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+100	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+130	μA
Peak wavelength	λ_{PEAK}	T_A=25°C		655		nm
Dominant Wavelength [8]	λ_d	T_A=25°C		640		nm
Weight				1.0		gm

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50° C/W; Θ_{JC}=15° C/W; 2. Θ_{CA} of a mounted display should not exceed 35° C/W for operation up to T_A=+100° C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_A=25° C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship: $I_V(T_A)=I_{V(25°C)}(.985)^{[T_A-25°C]}$ 7. Applies only to 7359. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

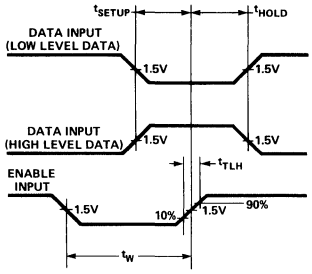


Figure 1. Timing Diagram of 5082-735X Series Logic.

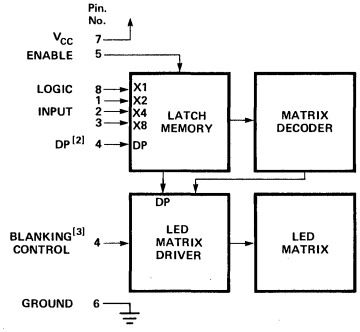


Figure 2. Block Diagram of 5082-735X Series Logic.

TRUTH TABLE					
BCD DATA[1]				5082-7356/7357	5082-7359
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	8	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	....	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE[1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING[3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7356 and 5082-7357 displays.
3. The blanking control input, B, pertains only to the 5082-7359 hexadecimal display. Blanking input has no effect upon display memory.

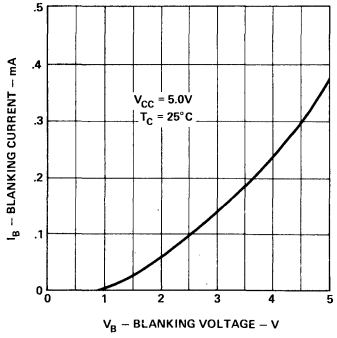


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7359.

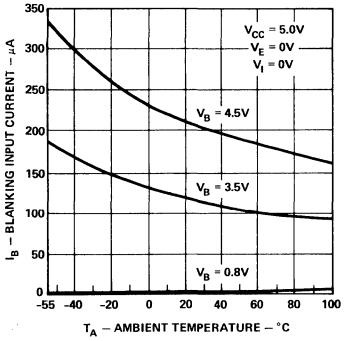


Figure 4. Typical Blanking Control Input Current vs. Ambient Temperature for 5082-7359.

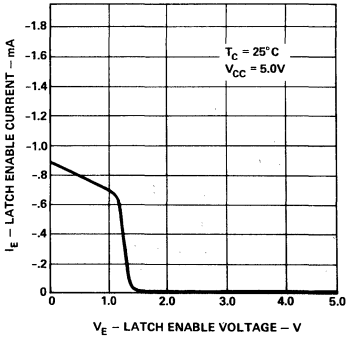


Figure 5. Typical Latch Enable Input Current vs. Voltage.

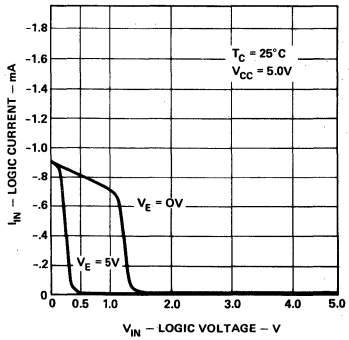


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage.

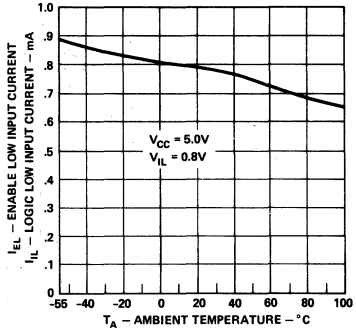


Figure 7. Typical Logic and Enable Low Input Current vs. Ambient Temperature.

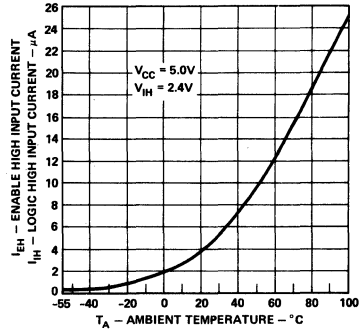


Figure 8. Typical Logic and Enable High Input Current vs. Ambient Temperature.

Operational Considerations

ELECTRICAL

The 5082-735X series devices use a modified 4 x 7 dot matrix of light emitting diodes (LED's) to display decimal/hexadecimal numeric information. The LED's are driven by constant current drivers. BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. To avoid the latching of erroneous information, the enable pulse rise time should not exceed 200 nanoseconds. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7MHz rate.

The blanking control input on the 5082-7395 display blanks (turns off) the displayed hexadecimal information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 3.5 volts. This may be easily achieved by using an open collector TTL gate and a pull-up resistor. For example, (1/6) 7416 hexinverter buffer/driver and a 120 ohm pull-up resistor will provide sufficient drive to blank eight displays. The size of the blanking pull-up resistor may be calculated from the following formula, where N is the number of digits:

$$R_{blank} = (V_{CC} - 3.5V)/[N\ (1.0mA)]$$

The decimal point input is active low true and this data is latched into the display memory in the same fashion as is the BCD data. The decimal point LED is driven by the on-board IC.

The ESD susceptibility of these IC devices is Class A of MIL-STD-883 or Class 2 of DOD-STD-1686 and DOD-HDBK-263.

MECHANICAL

These displays are designed for use in adverse industrial environments.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54mm (0.100 inch) and the lead row spacing is 15.24mm (0.600 inch). These displays may be end stacked with 2.54mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100° C, it is important to maintain a case-to-ambient thermal resistance of less than 35° C/watt as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

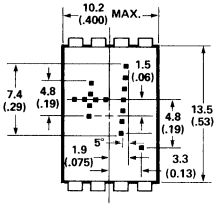
CONTRAST ENHANCEMENT

The 5082-735X displays have been designed to provide the maximum posible ON/OFF contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60 and Dark Red 63, SGL Homalite H100-1605, 3M Light Control Film and Polaroid HRCP Red Circular Polarizing Filter. For further information see Hewlett-Packard Application Note 964.

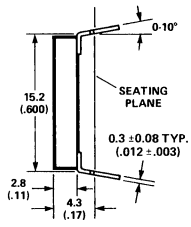
Solid State Over Range Display

For display applications requiring a ±, 1, or decimal point designation, the 5082-7358 over range display is available. This display module comes in the same package as the 5082-735X series numeric display and is completely compatible with it.

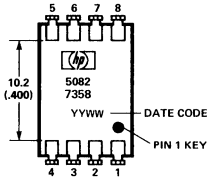
Package Dimensions



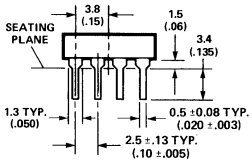
FRONT



SIDE



REAR



END

NOTES:
1. DIMENSIONS IN MILLIMETERS AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±0.38 MM (±0.015 INCHES).

PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{CC}
8	Minus/Plus

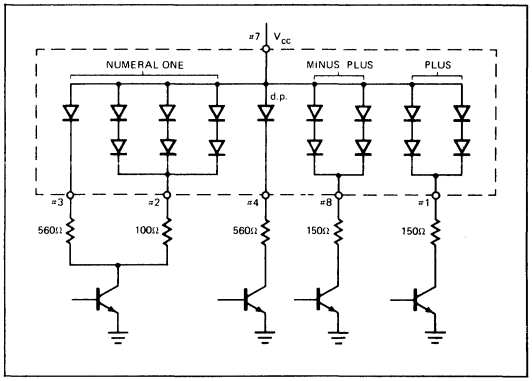


Figure 9. Typical Driving Circuit.

TRUTH TABLE

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 9 cutoff.
H: Line switching transistor in Figure 9 saturated.
X: 'Don't care'

Electrical/Optical Characteristics

5082-7358 (T_A = -55°C to +85°C, Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		280	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	40	85		μcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λd	T_C = 25°C		640		nm
Weight				1.0		gm

Recommended Operating Conditions

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 9 for recommended resistor values.

Absolute Maximum Ratings

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	-65	+125	°C
Operating temperature, ambient	T_A	-55	+100	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

HEWLETT PACKARD

HEXADECIMAL AND NUMERIC DISPLAYS FOR INDUSTRIAL APPLICATIONS

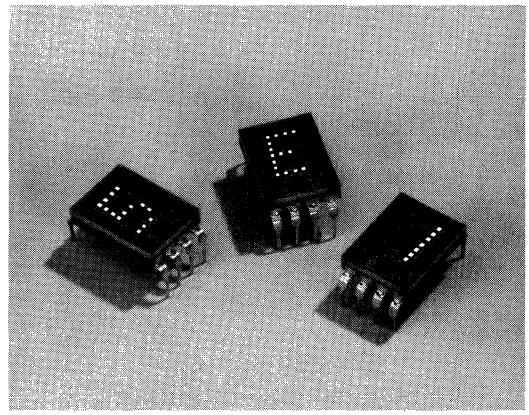
HIGH EFFICIENCY RED	
Low Power	HDSP-0760/0761/0762/0763
High Brightness	HDSP-0770/0771/0772/0763
YELLOW	HDSP-0860/0861/0862/0863
GREEN	HDSP-0960/0961/0962/0963

Features

- **THREE COLORS**
  High-Efficiency Red
  Yellow
  High Performance Green
- **THREE CHARACTER OPTIONS**
  Numeric
  Hexadecimal
  Over Range
- **TWO HIGH-EFFICIENCY RED OPTIONS**
  Low Power
  High Brightness
- **PERFORMANCE GUARANTEED OVER TEMPERATURE**
- **MEMORY LATCH/DECODER/DRIVER**
  TTL Compatible
- **4x7 DOT MATRIX CHARACTER**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
- **YELLOW AND GREEN CATEGORIZED FOR COLOR**

Typical Applications

- **INDUSTRIAL EQUIPMENT**
- **COMPUTER PERIPHERALS**
- **INSTRUMENTATION**
- **TELECOMMUNICATION EQUIPMENT**



Description

These solid state display devices are designed and tested for use in adverse industrial environments. The character height is 7.4mm (0.29 inch). The numeric and hexadecimal devices incorporate an on-board IC that contains the data memory, decoder and display driver functions.

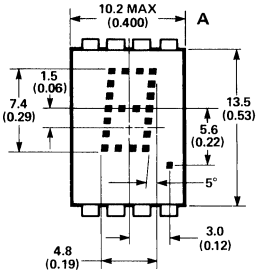
The numeric devices decode positive BCD logic into characters "0-9", a "—" sign, decimal point, and a test pattern. The hexadecimal devices decode positive BCD logic into 16 characters, "0-9, A-F". An input is provided on the hexadecimal devices to blank the display (all LED's off) without losing the contents of the memory.

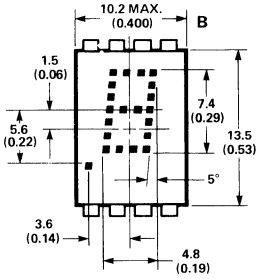
The over range device displays "±1" and right hand decimal point and is typically driven via external switching transistors.

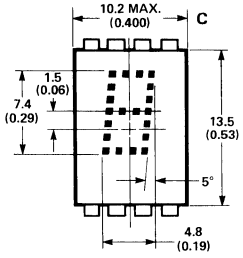
Devices

Part Number HDSP-	Color	Description	Front View
0760	High-Efficiency Red Low Power	Numeric, Right Hand DP	A
0761		Numeric, Left Hand DP	B
0762		Hexadecimal	C
0763		Over Range ±1	D
0770	High-Efficiency Red High Brightness	Numeric, Right Hand DP	A
0771		Numeric, Left Hand DP	B
0772		Hexadecimal	C
0763		Over Range ±1	D
0860	Yellow	Numeric, Right Hand DP	A
0861		Numeric, Left Hand DP	B
0862		Hexadecimal	C
0863		Over Range ±1	D
0960	Green	Numeric, Right Hand DP	A
0961		Numeric, Left Hand DP	B
0962		Hexadecimal	C
0963		Over Range ±1	D

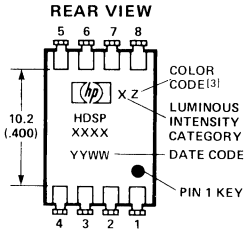
Package Dimensions

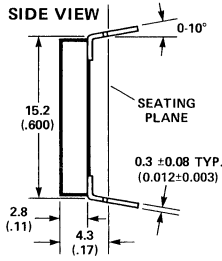


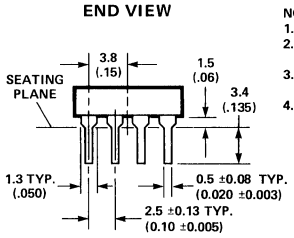




PIN	FUNCTION	
	NUMERIC	HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1







NOTES:
1. Dimensions in millimetres and (inches).
2. Digit center line is ±0.38 mm (±0.015 inch) from package center line.
3. Unless otherwise specified, the tolerance on all dimensions is ±0.38 mm (±0.015 inch).
4. HDSP-0860 and HDSP-0960 series.

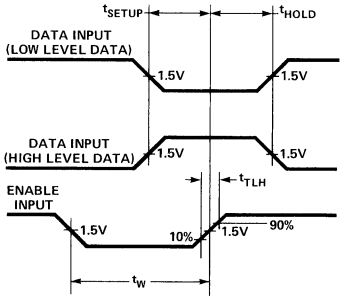


Figure 1. Timing Diagram

TRUTH TABLE					
BCD DATA[1]				NUMERIC	HEXA-DECIMAL
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	8	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	----	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE[1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING[3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels have no effect upon display memory, displayed character, or DP.
2. The decimal point input, DP, pertains only to the numeric displays.
3. The blanking control input, B, pertains only to the hexadecimal displays. Blanking input has no effect upon display memory.

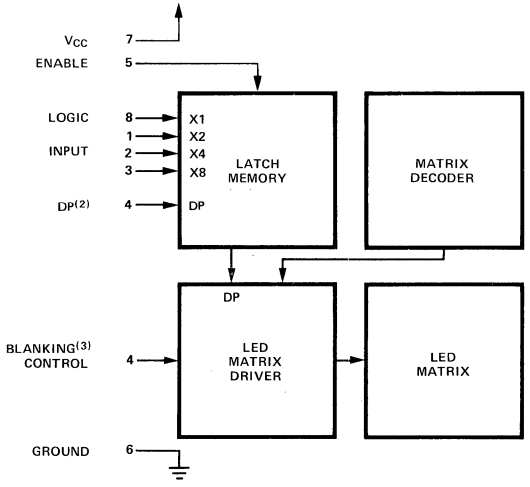


Figure 2. Logic Block Diagram

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+100	°C
Operating temperature, ambient [1]	T_A	−55	+85	°C
Supply voltage [2]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	V_{CC}	V
Voltage applied to blanking input [2]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ⩽ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage [2]	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1]	T_A	-55		+85	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			1.0	msec

Optical Characteristics at T_A = 25°C, V_{CC} = 5.0V

Device	Description	Symbol	Min.	Typ.	Max.	Unit
HDSP-0760 Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	65	140		μcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength [5]	λ_d		626		nm
HDSP-0770 Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	260	620		μcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength [5]	λ_d		626		nm
HDSP-0860 Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	215	490		μcd
	Peak Wavelength	λ_{PEAK}		583		nm
	Dominant Wavelength [5,6]	λ_d		585		nm
HDSP-0960 Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	298	1100		μcd
	Peak Wavelength	λ_{PEAK}		568		nm
	Dominant Wavelength [5,6]	λ_d		574		nm

Notes:
1. The nominal thermal resistance of a display mounted in a socket that is soldered onto a printed circuit board is $R\theta_{JA}$ = 50° C/W/device. The device package thermal resistance is $R\theta_{J-PIN}$ = 15° C/W/device. The thermal resistance device pin-to-ambient through the PC board should not exceed 35° C/W/device for operation at T_A = +85° C.
2. Voltage values are with respect to device ground, pin 6.
3. These displays are categorized for luminous intensity with the intensity category designated by a letter code located on the back of the display package. Case temperature of the device immediately prior to the light measurement is equal to 25° C.

Electrical Characteristics; T_A = -55°C to +85°C

Description		Symbol	Test Conditions	Min.	Typ.[7]	Max.	Unit
Supply Current	HDSP-0760 Series	I_{CC}	V_{CC} = 5.5V (characters "5." or "B" displayed)		78	105	mA
	HDSP-0770 Series HDSP-0860 Series HDSP-0960 Series				120	175	
Power Dissipation	HDSP-0760 Series	P_T			390	573	mW
	HDSP-0770 Series HDSP-0860 Series HDSP-0960 Series				690	963	
Logic, Enable and Blanking Low-Level Input Voltage		V_{IL}	V_{CC} = 4.5V			0.8	V
Logic, Enable and Blanking High-Level Input Voltage		V_{IH}		2.0			V
Logic and Enable Low-Level Input Current		I_{IL}	V_{CC} = 5.5V			-1.6	mA
Blanking Low-Level Input Current		I_{BL}	V_{IL} = 0.4V			-10	μA
Logic, Enable and Blanking High-Level Input Current		I_{IH}	V_{CC} = 5.5V V_{IH} = 2.4V			+40	μA
Weight					1.0		gm
Leak Rate						$5x10^{-8}$	cc/sec

Notes:

4. The luminous intensity at a specific operating ambient temperature, $I_V(T_A)$ may be approximated from the following expotential equation: $I_V(T_A = I_V(25°C)\, e^{|k(T_A - 25°C)|}$.

Device	K
HDSP-0760 Series HDSP-0770 Series	-0.0131/°C
HDSP-0860 Series	-0.0112/°C
HDSP-0960 Series	-0.0104/°C

5. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
6. The HDSP-0860 and HDSP-0960 series devices are categorized as to dominant wavelength with the category designated by a number on the back side of the display package.
7. All typical values at V_{CC} = 5.0V and T_A = 25°C.

Operational Considerations

ELECTRICAL

These devices use a modified 4 x 7 dot matrix of light emitting diode to display decimal/hexadecimal numeric information. The high efficiency red and yellow LED's are GaAsP epitaxial layer on a GaP transparent substrate. The green LED's are GaP epitaxial layer on a GaP transparent substrate. The LED's are driven by constant current drivers, BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7 MHz rate.

The decimal point input is active low true and this data is latched into the display memory in the same fashion as the BCD data. The decimal point LED is driven by the on-board IC.

The blanking control input on the hexadecimal displays blanks (turns off) the displayed information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 2.0 volts. When blanked, the display standby power is nominally 250 mW at T_A = 25°C.

MECHANICAL

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +85°C, it is important to maintain a cast-to-ambient thermal resistance of less than 35°C watt/device as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixutres formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

CONTRAST ENHANCEMENT

These display devices are designed to provide an optimum ON/OFF contrast when placed behind an appropriate contrast enhancement filter. The following filters are suggested:

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-0860 Series Yellow	Panelgraphic Yellow 27 Chequers Amber 107	Polaroid HNCP 37 3M Light Control Film Panelgraphic Gray 10 Chequers Grey 105	Polaroid Gray HNCP10 HOYA Yellowish-Orange HLF-608-3Y Marks Gray MCP-0301-8-10
HDSP-0760 Series HDSP-0770 Series High Efficiency Red	Panelgraphic Ruby Red 60 Chequers Red 112		Polaroid Gray HNCP10 HOYA Reddish-Orange HLF-608-5R Marks Gray MCP-0301-8-10 Marks Reddish-Orange MCP-0201-2-22
HDSP-0960 Series HP Green	Panelgraphic Green 48 Chequers Green 107		Polaroid Gray HNCP10 HOYA Yellow-Green HLF-608-1G Marks Yellow-Green MCP-0101-5-12

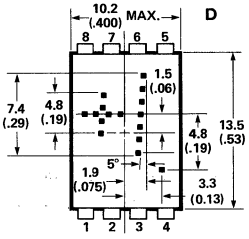
Over Range Display

The over range devices display "±1" and decimal point. The character height and package configuration are the same as the numeric and hexadecimal devices. Character selection is obtained via external switching transistors and current limiting resistors.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	-65	+100	°C
Operating Temperature Ambient	T_A	-55	+85	°C
Forward Current, Each LED	I_F		10	mA
Reverse Voltage, Each LED	V_R		5	V

Package Dimensions



FRONT VIEW

Pin	Function
1	Plus
2	Numeral One
3	Numeral One
4	DP.
5	Open
6	Open
7	V_{CC}
8	Minus/Plus

Note:
1. Dimensions in millimetres and (inches).

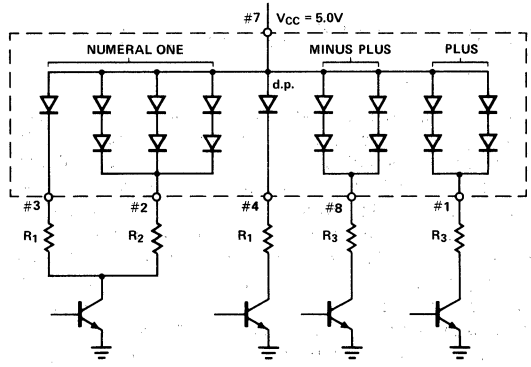


Figure 3. Typical Driving Circuit

Character	Pin			
	1	2,3	4	8
+	1	X	X	1
—	0	X	X	1
1	X	1	X	X
Decimal Point	X	X	1	X
Blank	0	0	0	0

Notes:
0: Line switching transistor in Figure 7 cutoff.
1: Line switching transistor in Figure 7 saturated.
X: 'don't care'

Recommended Operating Conditions V_{CC} = 5.0V

Device		Forward Current Per LED, mA	Resistor Value		
			R_1	R_2	R_3
HDSP-0763	Low Power	2.8	1300	200	300
	High Brightness	8	360	47	68
HDSP-0863		8	360	36	56
HDSP-0963		8	360	30	43

Luminous Intensity Per LED

(Digit Average)[3,4] at T_A = 25°C

Device	Test Conditions	Min.	Typ.	Units
HDSP-0763	I_F = 2.8 mA	65	140	μcd
	I_F = 8 mA		620	μcd
HDSP-0863	I_F = 8 mA	215	490	μcd
HDSP-0963	I_F = 8 mA	298	1100	μcd

Electrical Characteristics; T_A = -55°C to +85°C

Device	Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
HDSP-0763	Power Dissipation (all LED's Illuminated)	P_T	I_F = 2.8 mA		72		mW
			I_F = 8 mA		224	282	
	Forward Voltage per LED	V_F	I_F = 2.8 mA		1.6		V
			I_F = 8 mA		1.75	2.2	
HDSP-0863	Power Dissipation (all LED's Illuminated)	P_T	I_F = 8 mA		237	282	mW
	Forward Voltage per LED	V_F			1.90	2.2	V
HDSP-0963	Power Dissipation (all LED's Illuminated)	P_T	I_F = 8 mA		243	282	mW
	Forward Voltage per LED	V_F			1.85	2.2	V

HEWLETT PACKARD

RED HEXADECIMAL 6.86mm (0.27in)

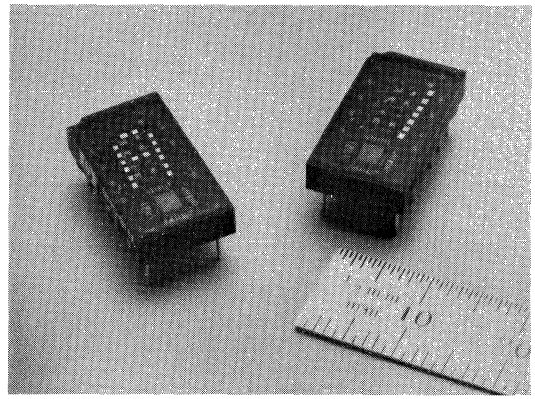
HTIL-311A

Features

- **ON-BOARD LOW POWER, EASY TO INTERFACE CMOS IC INCLUDES DECODER, DRIVER AND 4-BIT MEMORY**
- **DISPLAYS 4 X 7 DOT MATRIX HEXADECIMAL CHARACTERS DIRECTLY FROM 4 BIT DATA**
- **OPERATES FROM 5 VOLT SUPPLY**
- **CONSTANT CURRENT DRIVERS**
- **STANDARD 14 PIN DUAL-IN-LINE PACKAGE INCLUDING CONTRAST ENHANCEMENT FILTER**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
- **WIDE VIEWING ANGLE**
- **STURDY ROUND LEADS**
- **SUITABLE FOR AUTOMATIC INSERTION**

Description

The HTIL-311A is a single character red 4X7 dot matrix display with an on-board CMOS IC to accept, store and display 4-bit binary data. This display decodes positive 4-bit binary data into 16 states, 0-9 and A-F. The character height is 6.86mm (0.27 inch). The LEDs and IC are attached to a substrate which is enclosed by a plastic cap and backfill, creating an air gap environment for the LEDs and

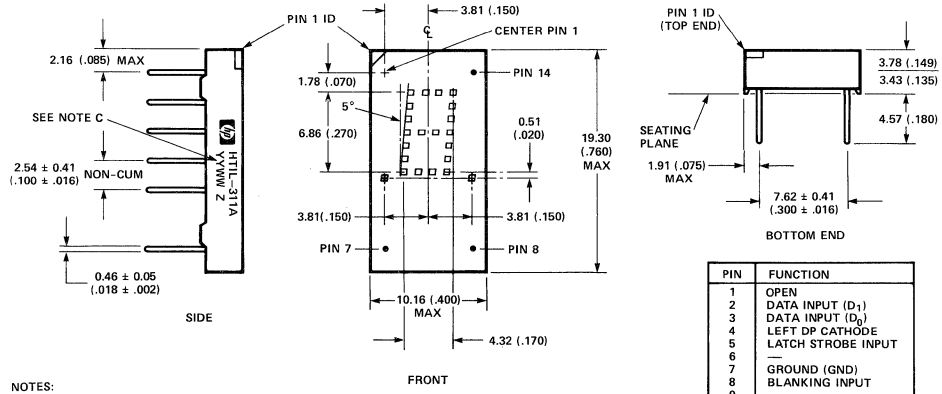


IC. The encapsulated dual-in-line package construction provides a rugged, environmentally sealed unit. The display may be stacked in either the X or Y direction to create either single or multiline systems. The bullet ended round pins are easy to insert in either PC boards or sockets.

Applications

- **INSTRUMENTATION**
- **COMPUTERS AND PERIPHERALS**
- **STATUS INDICATORS**
- **TELECOMMUNICATIONS**

Package Dimensions



NOTES:
A. DIMENSIONS IN MILLIMETERS (INCHES).
B. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
C. YY-YEAR, WW-WORK WEEK, Z INTENSITY CATEGORY NUMBER.

PIN	FUNCTION
1	OPEN
2	DATA INPUT (D_1)
3	DATA INPUT (D_8)
4	LEFT DP CATHODE
5	LATCH STROBE INPUT
6	—
7	GROUND (GND)
8	BLANKING INPUT
9	—
10	RIGHT DP CATHODE
11	—
12	DATA INPUT (D_3)
13	DATA INPUT (D_2)
14	DISPLAY SUPPLY (V_{DD})

ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED WITH THE HTIL-311A.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Units
Storage Temperature, Ambient	T_S	-25	+85	°C
Operating Case Temperature[1]	T_C	0	+85	°C
IC Supply Voltage to Ground	V_{DD}		7.0	V
Input Voltage, any Pin to Ground	V_{IN}	-0.5	V_{DD}+0.5	V
Maximum Solder Temperature at 1.59 mm (0.063 in) below seating plane; t ≤ 5 sec.			260	°C
ESD Protection @ 1.5 KΩ, 160 pF (each pin)	V_Z		2	kV

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Units
IC Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Decimal Point Current	I_{DP}		5.0	20.0	mA
Latch Pulse Width	t_L	40			ns
Data Setup Time to Rising Edge of Latch Pulse	t_S	50			ns
Data Hold Time After Rising Edge of Latch Pulse	t_H	40			ns
Latch Pulse Rise Time	t_R			200	ns

Electrical/Optical Characteristics Over Operating Temperature Range

(Unless Otherwise Specified)

Description	Symbol	Min.	Typ.[2] 25°C	Max.	Units	Test Condition
I_{DD} Current (Blank)	$I_{DD(BLK)}$		3.0	5.0	mA	V_{DD} = BLK = 5.5 V; $I_{F(DP)}$ = 0 mA All other inputs = 0 V
I_{DD} 14 Dots	$I_{DD(0)}$		74	90[9]	mA	V_{DD} = 5.5 V; $I_{F(DP)}$ = 5 mA All other inputs = 0 V
Decimal Point Forward Voltage[3]	$V_{F(DP)}$		1.5		V	$I_{F(DP)}$ = 5 mA
Input Voltage High	V_{IH}	2.0			V	V_{DD} = 4.5 - 5.5 V
Input Voltage Low	V_{IL}			0.8	V	V_{DD} = 4.5 - 5.5 V
Input Current	I_{IN}	-10		10	μA	V_{IN} = 0 V - V_{DD}
Luminous Intensity Average per Character LED[4,5,6,7]	I_V	35	100		μcd	V_{DD} = 5.0 V
Luminous Intensity Each Decimal Point[4]	I_V	35	100		μcd	$I_{F(DP)}$ = 5.0 mA
Peak Wavelength[4]	λ_P		655		nm	
Dominant Wavelength[4,7,8]	λ_D		640		nm	
Spectral Bandwidth	λ_W		24		nm	
Thermal Resistance	θ_{JC}		48		°C/W	

Notes:

1. Case temperature is the surface temperature of the plastic measured directly over the integrated circuit. Forced air cooling may be required to maintain this temperature. Maximum IC junction temperature should not exceed 125°C.
2. Typicals measured at V_{DD} = 5.0 V.
3. $V_{F(DP)}$ is not tested. See Figure 3 for forward voltage versus forward current.
4. Measured at 25°C case temperature.
5. This parameter is measured with "A" displayed, then again with "E" displayed.
6. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the side of the display.
7. See Figure 4 for relative luminous intensity versus ambient temperature. See Figure 5 for relative luminous intensity versus logic supply voltage.
8. The dominant wavelength, λ_D, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
9. Measured at 5 seconds.

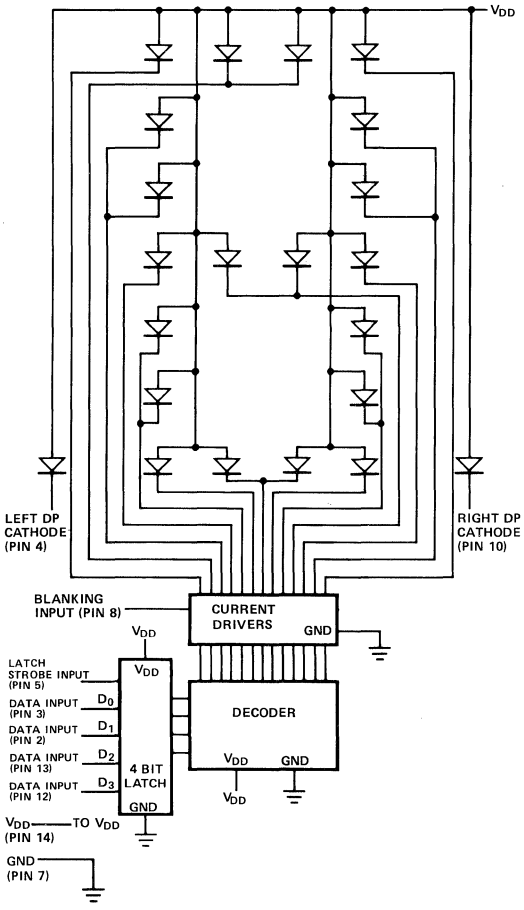


Figure 1. HTIL-311A Internal Block Diagram

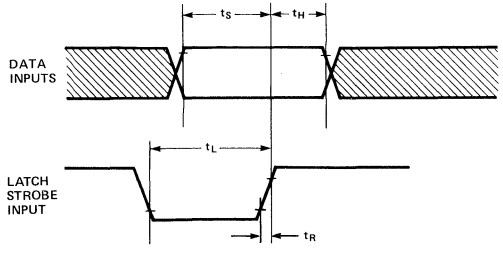


Figure 2. Timing Diagram

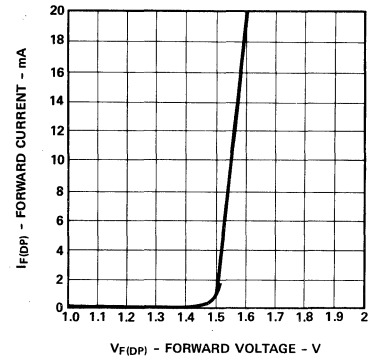


Figure 3. Forward Current vs. Forward Voltage

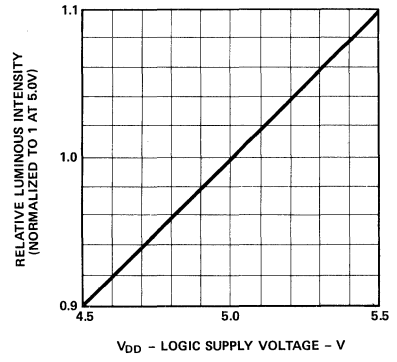


Figure 4. Relative Luminous Intensity vs. Logic Supply Voltage

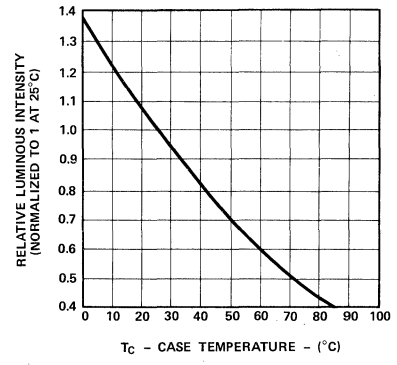


Figure 5. Relative Luminous Intensity vs. Case Temperature

Pin Function

LATCH STROBE INPUT (pin 5)

L: Data inputs are transferred to the decoder and displayed.
H: Data at D_0-D_3 is stored. Stored character is displayed regardless of the input data changes. Data stored in the latch is not affected by the blanking input.

BLANKING INPUT (BLK, pin 8)

L: Character is displayed.
H: Display is blanked, except for the decimal points. The display will be blanked regardless of the state of the other inputs. The blanking input may be used to dim the display by pulse width modulation of this input.

DATA INPUTS (D_0-D_3, pins 3, 2, 13, 12)

Four bit hexadecimal data is entered into the latch via the data inputs.

DECIMAL POINT CATHODES (pins 4, 10)

The anodes of the left and right decimal points are connected to V_{DD}. To illuminate the decimal point, the decimal point cathode must be connected to ground with a resistor or other current limiting device.

OPEN PIN (pin 1)

DISPLAY SUPPLY (V_{DD}, pin 14)

This input supplies power to the LEDs and the IC.

GROUND (GND, pin 7)

This is the display ground.

INSERTION INTO A SOCKET

During insertion into a socket, care must be taken to apply pressure only along the edges of the display window. Pressure applied at the center of the window may cause it to deform sufficiently to damage LED and IC wire bonds.

TRUTH TABLE

Blanking	Latch	Data Input D3	D2	D1	D0	Character Displayed
L	L	L	L	L	L	0
L	L	L	L	L	H	1
L	L	L	L	H	L	2
L	L	L	L	H	H	3
L	L	L	H	L	L	4
L	L	L	H	L	H	5
L	L	L	H	H	L	6
L	L	L	H	H	H	7
L	L	H	L	L	L	8
L	L	H	L	L	H	9
L	L	H	L	H	L	A
L	L	H	L	H	H	B
L	L	H	H	L	L	C
L	L	H	H	L	H	D
L	L	H	H	H	L	E
L	L	H	H	H	H	F
L	H	X	X	X	X	NOTE 1
H	L	X	X	X	X	NOTE 2
H	H	X	X	X	X	NOTE 3

$L = V_{IL}$; $H = V_{IH}$; $0 V < X < V_{DD}$

Notes:
1. The character stored in the Latch will be displayed. The contents of the Latch will remain unchanged.
2. The display will be blanked, except for the decimal points. The Latch will be updated based on the current logic levels present at the data inputs.
3. The display, except for the decimal points, will be blanked. The contents of the Latch will remain unchanged.

Hermetic Displays

Hermetic Displays

Military Grade Displays

Hewlett-Packard families of military grade numeric and alphanumeric LED displays are screened to the requirements of MIL-D-87157. MIL-D-87157 is the general specification for LED display devices and defines four screening levels for hermetic and nonhermetic devices, termed "Quality Levels".

Quality Level A: Hermetic displays with 100% screening and Group A, B, and C testing.
Quality Level B: Hermetic displays with Group A, B, and C testing, but without 100% screening.
Quality Level C: Nonhermetic displays with 100% screening and Group A, B, and C testing.
Quality Level D: Nonhermetic displays with Group A, B, and C testing, but without 100% screening.

The 4N5X series single digit dot matrix numeric and hexadecimal displays are listed on the MIL-D-87157 Qualified Parts List (QPL) under the number series M871570010XAAX.

Displays with TXV part numbers are 100% screened with Group A testing. Displays with TXVB part numbers are 100% screened to Quality Level A.

The applicable MIL-D-87157 screening tables are detailed on each display data sheet.

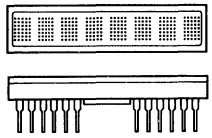
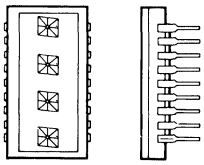
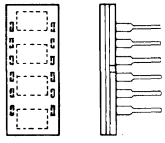
High Reliability Displays

In addition to Hewlett-Packard commercial solid state displays, Hewlett-Packard offers a complete line of hermetic packages for high reliability military and aerospace applications. These packages consist of numeric and hexadecimal displays, 5 x 7 dot matrix alphanumeric displays with extended temperature ranges, and fully intelligent monolithic 16 segment displays with extended temperature ranges and on board CMOS ICs. Similar to the commercial display product selection, the high reliability display products are offered in a variety of character sizes and colors: standard red, high efficiency red, yellow, and high performance green. Orange displays are sometimes available upon request.

Hewlett-Packard offers three different testing programs for the high reliability conscious display customer. These programs include DESC Qualification on the MIL-D-87157 for the hermetically sealed 4N51-4N54 hexadecimal and numeric displays; and two levels of in-house high reliability testing programs that conform or a modification to MIL-D-87157 Quality Level A Test Tables for all other high reliability display products. Please refer to the individual data sheets for a complete description of each display's testing program.

Integrated numeric and hexadecimal displays (with on-board ICs) solve the designer's decoding/driving problems. They are available in plastic packages for general purpose usage, ceramic/glass packages for industrial applications, and hermetic packages for high reliability applications. This family of displays has been designed for ease of use in a wide range of environments.

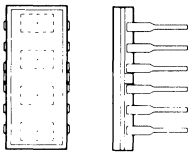
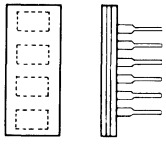
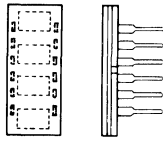
Hermetic Alphanumeric Displays

Device	P/N	Description	Color	Application	Page No.
	**HDSP-2131** **HDSP-2131 TXV** **HDSP-2131 TXVB**	5.0 mm (0.20 in.) 5 x 7 Eight Character Smart Alphanumeric Display Operating Temperature Range: -55°C to +85°C TXV – Hi Rel Screened TXVB – Hi Rel Screened to Level A MIL-D-87157	Yellow	• Military Equipment • Military Avionics • Military Ground Support Systems • Military Telecommunications	4-166
	HDSP-2132 **HDSP-2132 TXV** **HDSP-2132 TXVB**		High Efficiency Red		
	HDSP-2133 **HDSP-2133 TXV** **HDSP-2133 TXVB**		High Performance Green		
	HDSP-2179 **HDSP-2179 TXV** **HDSP-2179 TXVB**		Orange		
	HMDL-2416 HMDL-2416 TXV HMDL-2416 TXVB	4.1 mm (0.16 in.) Four Character Monolithic Smart Alphanumeric Display Operating Temperature Range: -55°C to +100°C TXV – Hi Rel Screened TXVB – Hi Rel Screened to Level A MIL-D-87157	Red	• Military Equipment • High Reliability Applications • Military Telecommunications	4-185
	**HCMS-2351** **HCMS-2351 TXV** **HCMS-2351 TXVB**	5.0 mm (0.20 in.) 5 x 7 Four Character Alphanumeric Sunlight Viewable Display CMOS IC Operating Temperature Range: -55°C to +100°C TXV – Hi Rel Screened TXVB – Hi Rel Screened to Level A Mil-D-87157	Yellow	• Military Avionics • Military Cockpit • Military Ground Support Systems	4-195
	HCMS-2352 **HCMS-2352 TXV** **HCMS-2352 TXVB**		High Efficiency Red		
	HCMS-2353 **HCMS-2353 TXV** **HCMS-2353 TXVB**		High Performance Green		
	HCMS-2354 **HCMS-2354 TXV** **HCMS-2354 TXVB**		Orange		

Bold Type – New Product

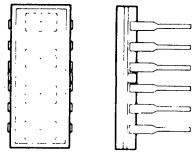
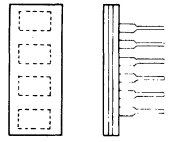
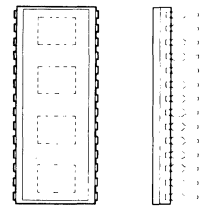
*Contact your local Sales Representative for information regarding this product. (See section 9.)

Hermetic Alphanumeric Displays (Continued)

Device	P/N	Description	Color	Application	Page No.
	**HCMS-2010** **HCMS-2010 TXV** **HCMS-2010 TXVB**	3.7 mm (0.15 in.) 5 x 7 Four Character Alphanumeric CMOS IC	Red, Red Glass Contrast Filter	• Extended temperature applications requiring high reliability. • I/O Terminals • Avionics	4-195
	HCMS-2011 **HCMS-2011 TXV** **HCMS-2011 TXVB**	Operating Temperature Range: -55°C to +100°C TXV – Hi Rel Screened	Yellow		
	HCMS-2012 **HCMS-2012 TXV** **HCMS-2012 TXVB**	TXVB – Hi Rel Screened to Level A MIL-D-87157	High Efficiency Red		
	HCMS-2013 **HCMS-2013 TXV** **HCMS-2013 TXVB**		High Performance Green		
	**HCMS-2310** **HCMS-2310 TXV** **HCMS-2310 TXVB**	5.0 mm (0.20 in.) 5 x 7 Four Character Alphanumeric CMOS IC	Standard Red	• Military Equipment • Avionics • High Rel Industrial Equipment	
	HCMS-2311 **HCMS-2311 TXV** **HCMS-2311 TXVB**	12 Pin Ceramic 6.35 mm (0.25 in.) DIP with untinted glass lens	Yellow		
	HCMS-2312 **HCMS-2312 TXV** **HCMS-2312 TXVB**	Operating Temperature Range: -55°C to +100°C TXV – Hi Rel Screened	High Efficiency Red		
	HCMS-2313 **HCMS-2313 TXV** **HCMS-2313 TXVB**	TXVB – Hi Rel Screened to Level A MIL-D-87157	High Performance Green		
	HCMS-2314 **HCMS-2314 TXV** **HCMS-2314 TXVB**		Orange		
	HDSP-2351 HDSP-2351 TXV HDSP-2351 TXVB	4.87 mm (0.19 in.) 5 x 7 Four Character Alphanumeric Sunlight Viewable Display Operating Temperature Range: -55°C to +100°C	Yellow	• Military Avionics • Military Cockpit • Military Ground Support Systems	*
	HDSP-2352 HDSP-2352 TXV HDSP-2352 TXVB		High Efficiency Red		
	HDSP-2353 HDSP-2353 TXV HDSP-2353 TXVB		High Performance Green		

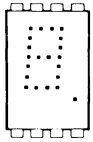
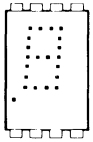
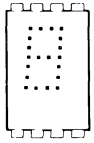
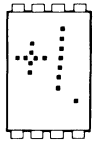
*Contact your local Sales Representative for information regarding this product. (See section 9.)

Hermetic Alphanumeric Displays (Continued)

Device	P/N	Description	Color	Application	Page No.
	HDSP-2010 HDSP-2010 TXV HDSP-2010 TXVB	3.7 mm (0.15 in.) 5 x 7 Four Character Alphanumeric Operating Temperature Range: -40°C to +85°C TXV – Hi Rel Screened TXVB – Hi Rel Screened to Level A MIL-D-87157	Red, Red Glass Contrast Filter	• Extended temperature applications requiring high reliability • I/O Terminals • Avionics For further information see Application Note 1016.	*
	HDSP-2310 HDSP-2310 TXV HDSP-2310 TXVB	5.0 mm (0.20 in.) 5 x 7 Four Character Alphanumeric 12 Pin Ceramic 6.35 mm (0.25 in.) DIP with untinted glass lens Operating Temperature Range: -55°C to +85°C True Hermetic Seal TXV – Hi Rel Screened TXVB – Hi Rel Screened to Level A MIL-D-87157	Standard Red	• Military Equipment • Avionics • High Rel Industrial Equipment	*
	HDSP-2311 HDSP-2311 TXV HDSP-2311 TXVB		Yellow		
	HDSP-2312 HDSP-2312 TXV HDSP-2312 TXVB		High Efficiency Red		
	HDSP-2313 HDSP-2313 TXV HDSP-2313 TXVB		High Performance Green		
	HDSP-2450 HDSP-2450 TXV HDSP-2450 TXVB	6.9 mm (0.27 in.) 5 x 7 Four Character Alphanumeric 28 Pin Ceramic 15.24 mm (0.6 in.) DIP Operating Temperature Range: -55°C to +85°C True Hermetic Seal TXV – Hi Rel Screened TXVB – Hi Rel Screened to Level A MIL-D-87157	Red	• Military Equipment • High Reliability Applications • Avionics • Ground Support, Cockpit, Shipboard Systems	*
	HDSP-2451 HDSP-2451 TXV HDSP-2451 TXVB		Yellow		
	HDSP-2452 HDSP-2452 TXV HDSP-2452 TXVB		High Efficiency Red		
	HDSP-2453 HDSP-2453 TXV HDSP-2453 TXVB		High Performance Green		

*Contact your local Sales Representative for information regarding this product. (See section 9.)

Hermetic Hexadecimal and Numeric Dot Matrix Displays

Device	P/N	Description	Package	Application	Page No.
 (A)	4N51 4N51TXV M87157/00101AAX[1] (4N51TXVB) (A)	Numeric RHDP Decoder/Driver/Memory TXV – Hi Rel Screened	8 Pin Hermetic Built-in 15.2 mm (0.6 in.) DIP with gold plated leads	• Military High Reliability Applications • Avionics/Space Flight Systems • Fire Control Systems • Ground Support, Shipboard Equipment	4-207
 (B)	4N52 4N52TXV M87157/00102AAX[1] (4N52TXVB) (B)	Numeric LHDP Built-in Decoder/Driver/Memory TXV – Hi Rel Screened			
 (C)	4N54 4N54TXV M87157/00104AAX[1] (4N54TXVB) (C)	Hexadecimal Built-in Decoder/Driver/Memory TXV – Hi Rel Screened			
	4N53 4N53TXV M87157/103AAX[1] (4N53TXVB) (D)	Character Plus/Minus Sign TXV – Hi Rel Screened			
 (D)	HDSP-0781 (A) HDSP-0781 TXV HDSP-0781 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157	High Efficiency Red Low Power	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	4-215
	HDSP-0782 (B) HDSP-0782 TXV HDSP-0782 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
7.4 mm (0.29 in.) 4 x 7 Single Digit Package 8 Pin Glass Ceramic 15.2 mm (0.6 in.) DIP Truly Hermetic	HDSP-0783 (D) HDSP-0783 TXV HDSP-0783 TXVB	Overrange ±1 TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0784 (C) HDSP-0784 TXV HDSP-0784 TXVB	Hexadecimal, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			

[1]Military Approved and Qualified for High Reliability Applications.

Hermetic Hexadecimal and Numeric Dot Matrix Displays (Continued)

Device	P/N	Description	Package	Application	Page No.
(See previous page)	HDSP-0791 (A) HDSP-0791 TXV HDSP-0791 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157	High Efficiency Red High Brightness	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	4-215
	HDSP-0792 (B) HDSP-0792 TXV HDSP-0792 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0783 (D) HDSP-0783 TXV HDSP-0783 TXVB	Overrange ±1 TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0794 (C) HDSP-0794 TXV HDSP-0794 TXVB	Hexadecimal, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0881 (A) HDSP-0881 TXV HDSP-0881 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157	Yellow		
	HDSP-0882 (B) HDSP-0882 TXV HDSP-0882 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0883 (D) HDSP-0883 TXV HDSP-0883 TXVB	Overrange ±1 TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0884 (C) HDSP-0884 TXV HDSP-0884 TXVB	Hexadecimal, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			

Hermetic Hexadecimal and Numeric Dot Matrix Displays (Continued)

Device	P/N	Description	Package	Application	Page No.
(See previous page)	HDSP-0981 (A) HDSP-0981 TXV HDSP-0981 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157	High Performance Green	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	4-215
	HDSP-0982 (B) HDSP-0982 TXV HDSP-0982 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0983 (C) HDSP-0983 TXV HDSP-0983 TXVB	Overrange ±1 TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			
	HDSP-0984 (D) HDSP-0984 TXV HDSP-0984 TXVB	Hexadecimal, Built-in Decoder/Driver Memory TXV Hi Rel Screened TXVB Hi Rel Screened to Level A Mil-D-87157			

HEWLETT PACKARD

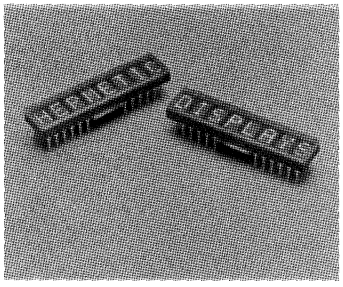
Eight Character 5.0 mm (0.2 inch) Hermetic Smart 5 X 7 Alphanumeric Displays For Military Applications

Technical Data

HDSP-2131/2131TXV/ 2131TXVB
HDSP-2132/2132TXV/ 2132TXVB
HDSP-2133/2133TXV/ 2133TXVB
HDSP-2179/2179TXV/ 2179TXVB

Features

- **Wide Operating Temperature Range -55°C to +85°C**
- **True Hermetic Package for Yellow, Orange and High Efficiency Red Displays[1]**
- **TXVB Version Conforms to MIL-D-87157 Quality Level A Test Tables**
- **Smart Alphanumeric Display**
  On-Board CMOS IC
  Built-In RAM
  ASCII Decoder
  LED Drive Circuitry
- **128 ASCII Character Set**
- **16 User Definable Characters**
- **Programmable Features**
  Individual Flashing Character
  Full Display Blinking
  Multi-Level Dimming and Blanking
  Self Test
  Clear Function
- **Read/Write Capability**
- **Full TTL Compatibility**
- **HDSP-2131/-2133/-2179 Useable in Night Vision Lighting Applications**
- **Categorized for Luminous Intensity**
- **HDSP-2131/2133 Categorized for Color**
- **Excellent ESD Protection**
- **Wave Solderable**
- **X-Y Stackable**



Description

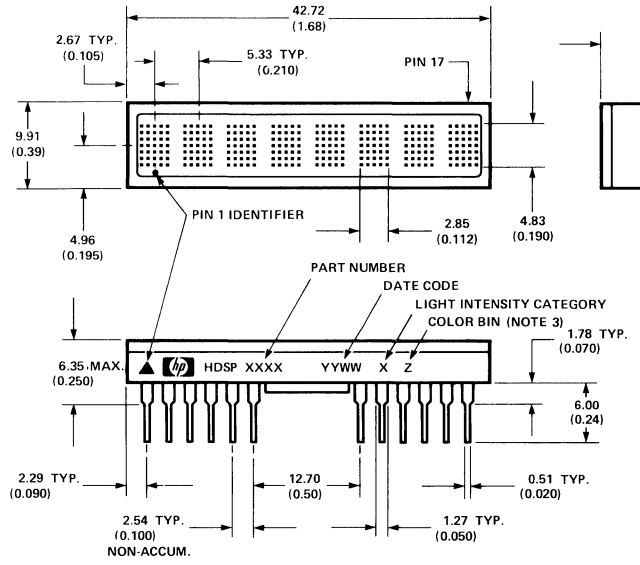
The HDSP-2131 (yellow), HDSP-2179 (orange), HDSP-2132 (high efficiency red) and the HDSP-2133 (green) are eight-digit, 5 x 7 dot matrix, alphanumeric displays. The 5.0 mm (0.2 inch) high characters are packaged in a standard 7.64 mm (0.30 inch) 32 pin DIP. The on-board CMOS IC has the ability to decode 128 ASCII characters, which are permanently stored in ROM. In addition, 16 programmable symbols may be stored in an on-board RAM. Seven brightness levels provide versatility in adjusting the display intensity and power consumption. The HDSP-213X is designed for standard microprocessor interface techniques. The display and special features are accessed through a bidirectional eight-bit data bus. These features make the HDSP-213X ideally suited for applications where an hermetic, low power alphanumeric display is required.

Devices

Yellow	High Efficiency Red	High Performance Green	Orange
HDSP-2131	HDSP-2132	HDSP-2133	HDSP-2179
HDSP-2131TXV	HDSP-2132TXV	HDSP-2133TXV	HDSP-2179TXV
HDSP-2131TXVB	HDSP-2132TXVB	HDSP-2133TXVB	HDSP-2179TXVB

Note: 1. The HDSP-2133 high peformance green displays conform to MIL-D-87157 hermeticity requirements.

Package Dimensions



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	CLS	17	GND (SUPPLY)
2	CLK	18	GND (LOGIC)
3	$\overline{WR}$	19	D4
4	$\overline{CE}$	20	D5
5	$\overline{RST}$	21	D6
6	$\overline{RD}$	22	D7
7	NO PIN	23	NO PIN
8	NO PIN	24	NO PIN
9	NO PIN	25	NO PIN
10	NO PIN	26	NO PIN
11	D0	27	$\overline{FL}$
12	D1	28	A0
13	D2	29	A1
14	D3	30	A2
15	NC	31	A3
16	V_{DD}	32	A4

Note:
1. All dimensions are in mm (inches).
2. Unless otherwise specified tolerance is ±0.30 mm (±0.015).
3. For green and yellow devices only.
4. Leads are copper alloy, solder dipped.

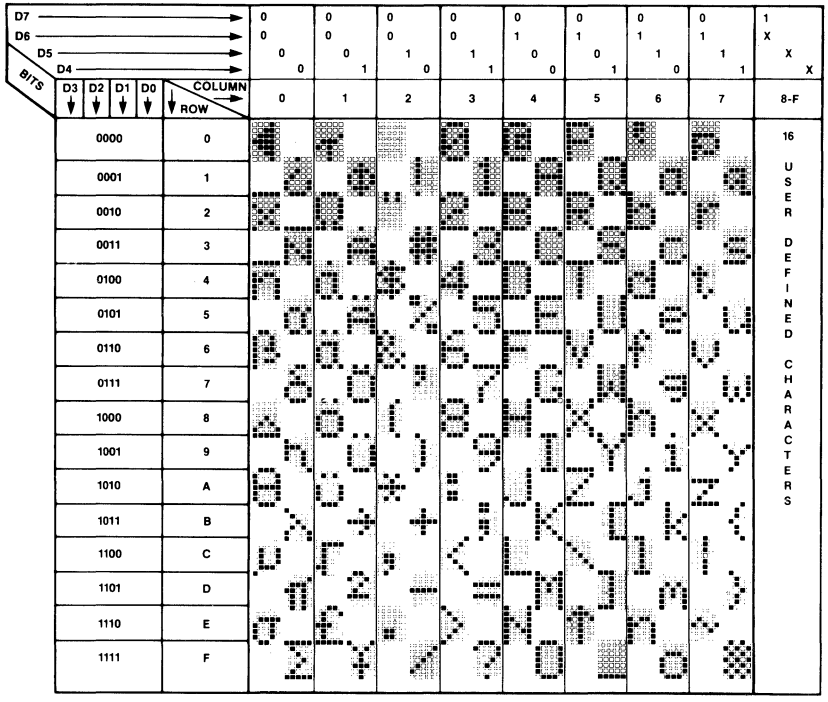
Absolute Maximum Ratings

Supply Voltage, V_{DD} to Ground[1] ..... -0.3 to 7.0 V
Operating Voltage, V_{DD} to Ground[2] ..... 5.5 V
Input Voltage, Any Pin to Ground ..... -0.3 to V_{DD} +0.3 V
Free Air Operating Temperature Range, T_A ..... -55°C to +85°C
Storage Temperature, T_S
HDSP-2131/-2132/-2179 ..... -65°C to +125°C
HDSP-2133 ..... -55°C to +100°C
Maximum Solder Temperature 1.59 mm
(0.063 in.) Below Seating Plane, t < 5 sec ..... 260°C
ESD Protection @ 1.5 kΩ, 100 pF ..... V_Z = 4 kV (each pin)

Notes:
1. Maximum Voltage is with no LEDs illuminated.
2. 20 dots ON in all locations at full brightness.

ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED WITH THE HDSP-2131, HDSP-2132, HDSP-2133, AND HDSP-2179.

Character Set



Recommended Operating Conditions

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

Electrical Characteristics Over Operating Temperature Range

$4.5 < V_{DD} < 5.5$ V (unless otherwise specified)

Parameter	Symbol	Min.	25°C Typ.[1]	25°C Max.[1]	Max.[2]	Units	Test Conditions
Input Leakage (Input without pullup)	I_I	-10.0			+10.0	µA	V_{IN} = 0 to V_{DD}, pins CLK, D_0-D_7, A_0-A_4
Input Current (Input with pullup)	I_{IP}	-30.0	11	18	30	µA	V_{IN} = 0 to V_{DD}, pins RST, CLS, WR, RD, CE, FL
I_{DD} Blank	I_{DD} (BLK)		0.5	3.0	4.0	mA	$V_{IN} = V_{DD}$
I_{DD} 8 digits 12 dots/character[3]	I_{DD}(V)		200	255	330	mA	"V" on in all 8 locations
I_{DD} 8 digits 20 dots/character[3]	I_{DD}(#)		300	370	430	mA	"#" on in all 8 locations
Input Voltage High	V_{IH}	2.0			V_{DD} +0.3	V	V_{DD} = 5.5 V
Input Voltage Low	V_{IL}	GND -0.3 V			0.8	V	V_{DD} = 4.5 V
Output Voltage High	V_{OH}	2.4				V	V_{DD} = 4.5 V, I_{OH} = -40 µA
Output Voltage Low D_0-D_7	V_{OL}				0.4	V	V_{DD} = 4.5 V, I_{OL} = 1.6 mA
Output Voltage Low CLK					0.4	V	V_{DD} = 4.5 V, I_{OL} = 40 µA
Thermal Resistance IC Junction-to-PIN	$R\theta_{J\text{-}PIN}$		11			°C/W	

Notes:
1. V_{DD} = 5.0 V.
2. Maximum I_{DD} occurs at -55°C.
3. Average I_{DD} measured at full brightness. See Table 2 in Control Word Section for I_{DD} at lower brightness levels. Peak I_{DD} = 28/15 x Average I_{DD} (#).

Optical Characteristics at 25°C[4]

V_{DD} = 5.0 V at Full Brightness

High Efficiency Red HDSP-2132

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		635	nm
Dominant Wavelength	λ_d		626	nm

Orange HDSP-2179

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		600	nm
Dominant Wavelength	λ_d		602	nm

Yellow HDSP-2131

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		583	nm
Dominant Wavelength	λ_d		585	nm

High Performance Green HDSP-2133

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}		568	nm
Dominant Wavelength	λ_d		574	nm

Note:
4. Refers to the initial case temperature of the device immediately prior to the light measurement.

AC Timing Characteristics Over Temperature Range

V_{DD} = 4.5 to 5.5 V unless otherwise specified.

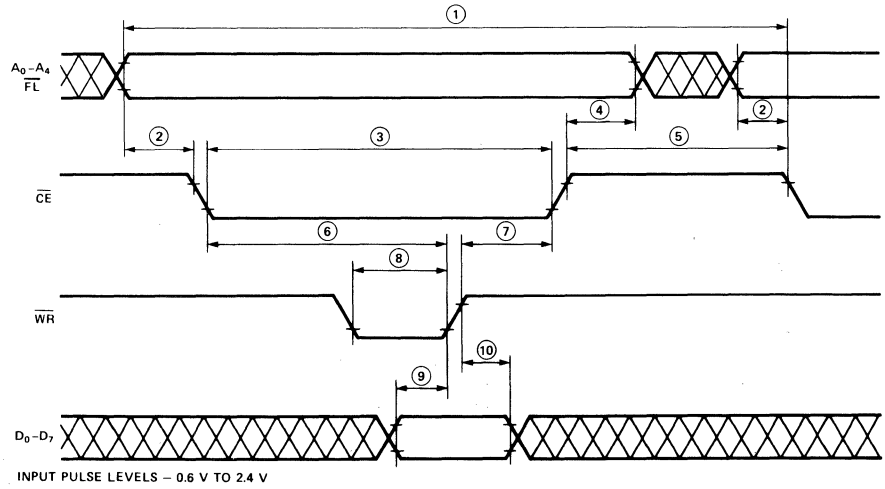
Reference Number	Symbol	Description	Min.[1]	Units
1	t_{ACC}	Display Access Time Write Read	 210 230	 ns
2	t_{ACS}	Address Setup Time to Chip Enable	10	ns
3	t_{CE}	Chip Enable Active Time[2, 3] Write Read	 140 160	 ns
4	t_{ACH}	Address Hold Time to Chip Enable	20	ns
5	t_{CER}	Chip Enable Recovery Time	60	ns
6	t_{CES}	Chip Enable Active Prior to Rising Edge of[1,2] Write Read	 140 160	 ns
7	t_{CEH}	Chip Enable Hold Time to Rising Edge of Read/Write Signal[2, 3]	0	ns
8	t_W	Write Active Time[2,3]	100	ns
9	t_{WD}	Data Valid Prior to Rising Edge of Write Signal	50	ns
10	t_{DH}	Data Write Hold Time	20	ns
11	t_R	Chip Enable Active Prior to Valid Data	160	ns
12	t_{RD}	Read Active Prior to Valid Data	75	ns
13	t_{DF}	Read Data Float Delay	10	ns
	t_{RC}	Reset Active Time[4]	300	ns

Notes:
1. Worst case values occur at an IC junction temperature of 125°C.
2. For designers who do not need to read from the display, the Read line can be tied to V_{DD} and the Write and Chip Enable lines can be tied together.
3. Changing the logic levels of the Address lines when $\overline{CE}$ = "0" may cause erroneous data to be entered into the Character RAM, regardless of the logic levels of the $\overline{WR}$ and $\overline{RD}$ lines.
4. The display must not be accessed until after 3 clock pulses (110 µs min. using the internal refresh clock) after the rising edge of the reset line.

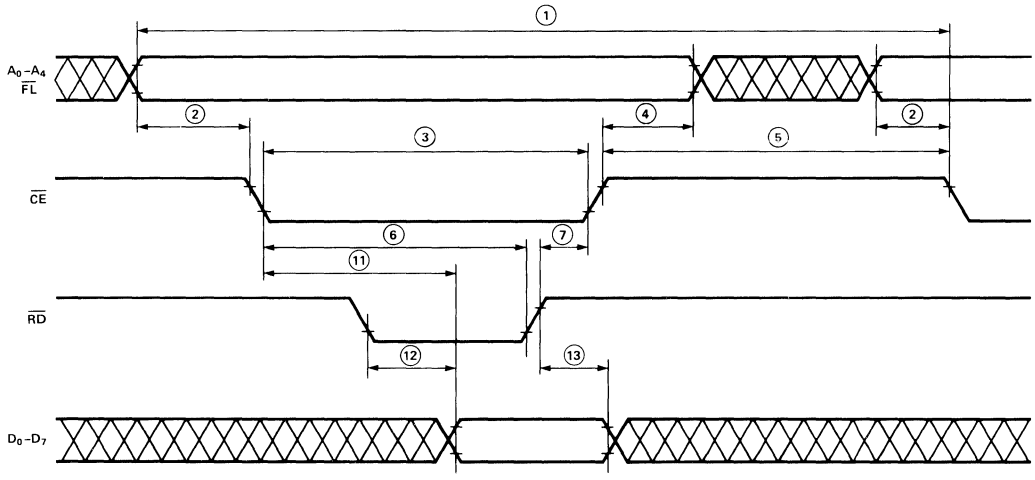
Symbol	Description	25°C Typical	Minimum[1]	Units
F_{OSC}	Oscillator Frequency	57	28	kHz
F_{RF} [5]	Display Refresh Rate	256	128	Hz
F_{FL} [6]	Character Flash Rate	2	1	Hz
t_{ST} [7]	Self Test Cycle Time	4.6	9.2	Sec

Notes:
5. $F_{RF} = F_{OSC}/224$
6. $F_{FL} = F_{OSC}/28{,}672$
7. $t_{ST} = 262{,}144/F_{OSC}$

Write Cycle Timing Diagram



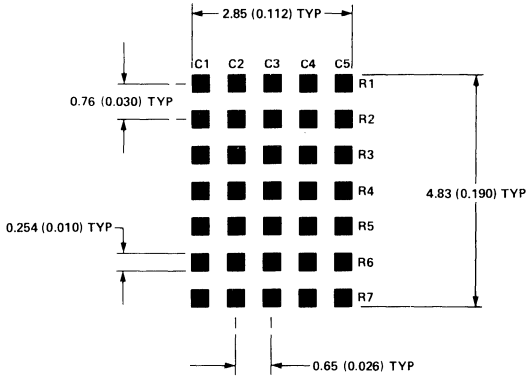
Read Cycle Timing Diagram



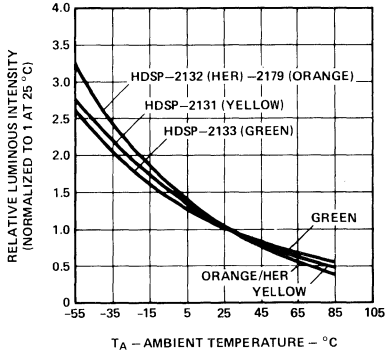
INPUT PULSE LEVELS: 0.6 V TO 2.4 V
OUTPUT REFERENCE LEVELS: 0.6 V TO 2.2 V
OUTPUT LOADING = 1 TTL LOAD AND 100pF

Character Font

(Not to Scale)



Relative Luminous Intensity vs. Temperature



Electrical Description

Pin Function

RESET ($\overline{RST}$, pin 5) — Reset initializes the display.

FLASH ($\overline{FL}$, pin 27) — $\overline{FL}$ low indicates an access to the Flash RAM and is unaffected by the state of address lines A_3-A_4.

ADDRESS INPUTS (A_0-A_4, pins 28-32) — Each location in memory has a distinct address. Address inputs (A_0-A_2) select a specific location in the Character RAM, the Flash RAM or a particular row in the UDC (User-Defined Character) RAM. A_3-A_4 are used to select which section of memory is accessed. Table 1 shows the logic levels needed to access each section of memory.

Table 1. Logic Levels to Access Memory

$\overline{FL}$	A_4	A_3	Section of Memory	A_2 A_1 A_0
0	X	X	Flash RAM	Character Address
1	0	0	UDC Address Register	Don't Care
1	0	1	UDC RAM	Row Address
1	1	0	Control Word Register	Don't Care
1	1	1	Character RAM	Character Address

CLOCK SELECT (CLS, pin 1) — This input is used to select either an internal or external clock source.

CLOCK INPUT/OUTPUT (CLK, pin 2) — Outputs the master clock (CLS = 1) or inputs a clock (CLS = 0) for slave displays.

WRITE ($\overline{WR}$, pin 3) — Data is written into the display when the $\overline{WR}$ input is low and the $\overline{CE}$ input is low.

CHIP ENABLE ($\overline{CE}$, pin 4) — This input must be at a logic low to read or write data to the display and must go high between each read and write cycle.

READ ($\overline{RD}$, pin 6) — Data is read from the display when the $\overline{RD}$ input is low and the $\overline{CE}$ input is low.

DATA Bus (D_0-D_7, pins 11-14, 19-22) — The Data bus is used to read from or write to the display.

$GND_{(SUPPLY)}$ (pin 17) — This is the analog ground for the LED drivers.

$GND_{(LOGIC)}$ (pin 18) — This is the digital ground for internal logic.

$V_{DD(POWER)}$ (pin 16) — This is the positive power supply input.

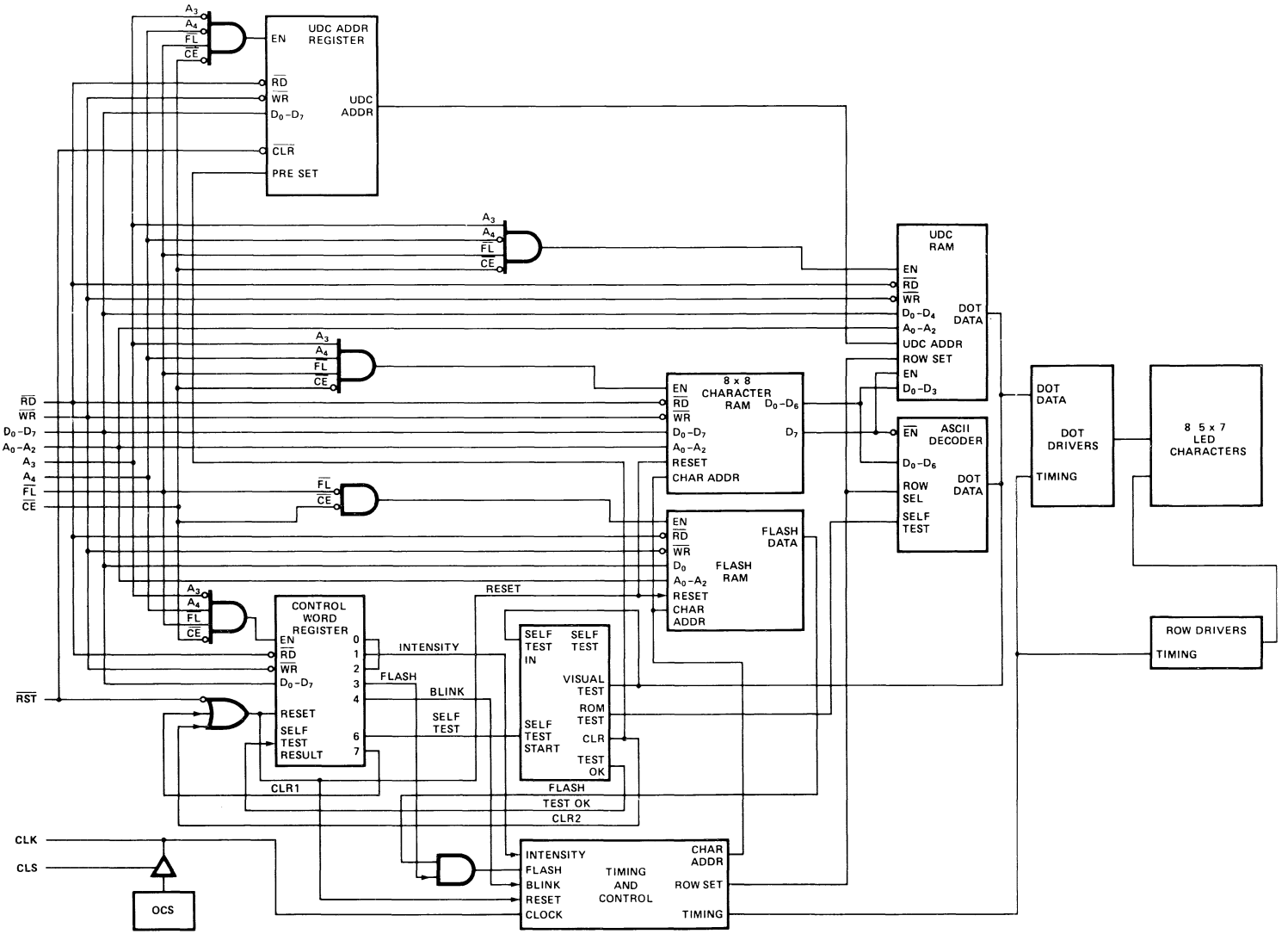


Figure 1. HDSP-213X Internal Block Diagram.

Display Internal Block Diagram

Figure 1 shows the internal block diagram of the HDSP-213X display. The CMOS IC consists of an 8 byte Character RAM, an 8 bit Flash RAM, a 128 character ASCII decoder, a 16 character UDC RAM, a UDC Address Register, a Control Word Register, and the refresh circuitry necessary to synchronize the decoding and driving of eight 5 x 7 dot matrix characters. The major user accessible portions of the display are listed below:

Character RAM	This RAM stores either ASCII character data or a UDC RAM address.
Flash RAM	This is a 1 x 8 RAM which stores Flash data.
User-Defined Character RAM (UDC RAM)	This RAM stores the dot pattern for custom characters.
User-defined Character Address Register (UDC Address Register)	This register is used to provide the address to the UDC RAM when the user is writing or reading a custom character.
Control Word Register	This register allows the user to adjust the display brightness, flash individual characters, blink, self test or clear the display.

Character Ram

Figure 2 shows the logic levels needed to access the HDSP-213X Character RAM. During a normal access the $\overline{CE}$ = "0" and either $\overline{RD}$ = "0" or $\overline{WR}$ = "0". However, erroneous data may be written into the Character RAM if the Address lines are unstable when $\overline{CE}$ = "0" regardless of the logic levels of the $\overline{RD}$ or $\overline{WR}$ lines. Address lines A_0-A_2 are used to select the location in the Character RAM. Two types of data can be stored in each Character RAM location: an ASCII code or a UDC RAM address. Data bit D_7 is used to differentiate between an ASCII character and a UDC RAM address. D_7 = 0 enables the ASCII decoder and D_7 = 1 enables the UDC RAM. D_0-D_6 are used to input ASCII data and D_0-D_3 are used to input a UDC address.

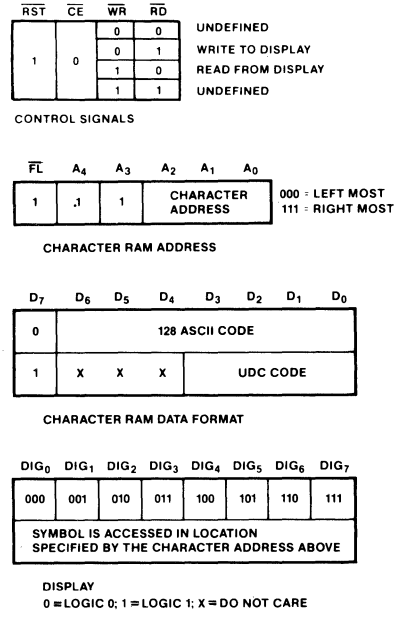


Figure 2. Logic Levels to Access the Character RAM.

UDC RAM and UDC Address Register

Figure 3 shows the logic levels needed to access the UDC RAM and the UDC Address Register. The UDC Address Register is eight bits wide. The lower four bits (D_0-D_3) are used to select one of the 16 UDC locations. The upper four bits (D_4-D_7) are not used. Once the UDC address has been stored in the UDC Address Register, the UDC RAM can be accessed.

To completely specify a 5 x 7 character requires eight write cycles. One cycle is used to store the UDC RAM address in the UDC Address Register. Seven cycles are used to store dot data in the UDC RAM. Data is entered by rows. One cycle is needed to access each row. Figure 4 shows the organization of a UDC character assuming the symbol to be stored is an "F". A_0-A_2 are used to select the row to be accessed and D_0-D_4 are used to transmit the row dot data. The upper three bits (D_5-D_7) are ignored. D_0 (least significant bit) corresponds to the right most column of the 5 x 7 matrix and D_4 (most significant bit) corresponds to the left most column of the 5 x 7 matrix.

Flash RAM

Figure 5 shows the logic levels needed to access the Flash RAM. The Flash RAM has one bit associated with each location of the Character RAM. The Flash input is used to select the Flash RAM. Address lines A_3-A_4 are ignored. Address lines A_0-A_2 are used to select the location in the Flash RAM to store the attribute. D_0 is used to store or remove the flash attribute. D_0 = "1" stores the attribute and D_0 = "0" removes the attribute.

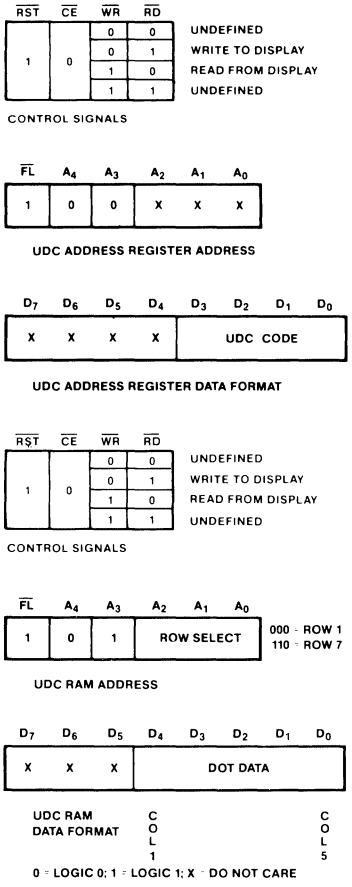


Figure 3. Logic Levels to Access a UDC Character.

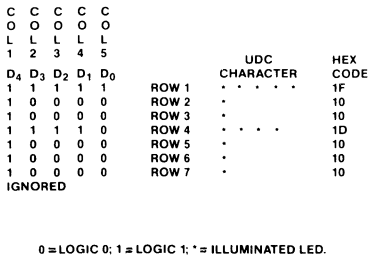


Figure 4. Data to Load "F" into the UDC RAM.

When the attribute is enabled through bit 3 of the Control Word and a "1" is stored in the Flash RAM, the corresponding character will flash at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock the flash rate can be calculated by dividing the clock frequency by 28,672.

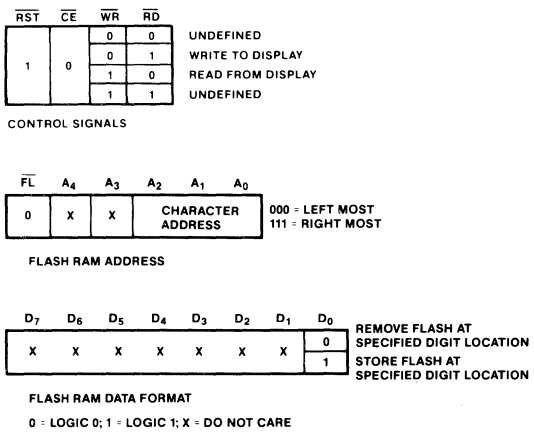


Figure 5. Logic Levels to Access the Flash RAM.

Control Word Register

Figure 6 shows how to access the Control Word Register. This is an eight bit register which performs five functions. They are Brightness control, Flash RAM control, Blinking, Self Test and Clear. Each function is independent of the others. However, all bits are updated during each Control Word write cycle.

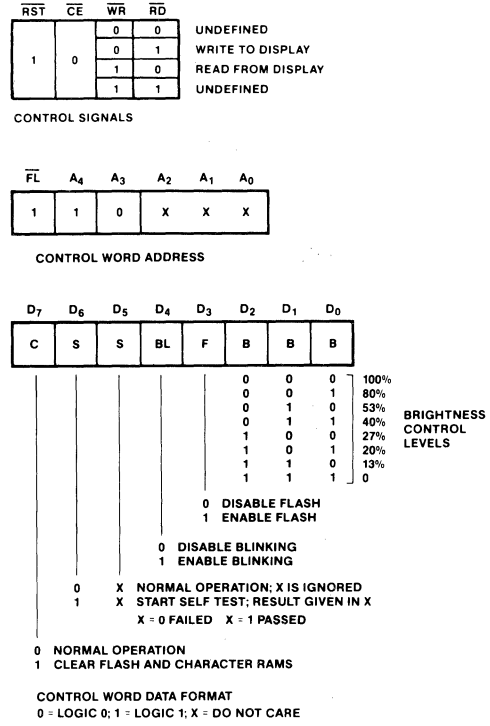


Figure 6. Logic Levels to Access the Control Word Register

Brightness (Bits 0-2)

Bits 0-2 of the Control Word adjust the brightness of the display. Bits 0-2 are interpreted as a three bit binary code with code (000) corresponding to maximum brightness and code (111) corresponding to a blanked display. In addition to varying the display brightness, bits 0-2 also vary the average value of I_{DD}. I_{DD} can be calculated at any brightness level by multiplying the percent brightness level by the value of I_{DD} at the 100% brightness level. These values of I_{DD} are shown in Table 2.

Table 2. Current Requirements at Different Brightness Levels

Symbol	D_2	D_1	D_0	% Brightness	25°C Typical	Units
I_{DD} (V)	0	0	0	100	200	mA
	0	0	1	80	160	mA
	0	1	0	53	106	mA
	0	1	1	40	80	mA
	1	0	0	27	54	mA
	1	0	1	20	40	mA
	1	1	0	13	26	mA

Flash Function (Bit 3)

Bit 3 determines whether the flashing character attribute is on or off. When bit 3 is a "1", the output of the Flash RAM is checked. If the content of a location in the Flash RAM is a "1", the associated digit will flash at approximately 2 Hz. For an external clock, the blink rate can be calculated by driving the clock frequency by 28,672. If the flash enable bit of the Control Word is a "0", the content of the Flash RAM is ignored. To use this function with multiple display systems see the Reset section.

Blink Function (Bit 4)

Bit 4 of the Control Word is used to synchronize blinking of all eight digits of the display. When this bit is a "1" all eight digits of the display will blink at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock, the blink rate can be calculated by dividing the clock frequency by 28,672. This function will override the Flash function when it is active. To use this function with multiple display systems see the Reset section.

Self Test Function (Bits 5, 6)
Bit 6 of the Control Word Register is used to initiate the self test function. Results of the internal self test are stored in bit 5 of the Control Word. Bit 5 is a read only bit where bit 5 = "1" indicates a passed self test and bit 5 = "0" indicates a failed self test.

Setting bit 6 to a logic 1 will start the self test function. The built-in self test function of the IC consists of two internal routines which exercises major portions of the IC and illuminates all of the LEDs. The first routine cycles the ASCII decoder ROM through all states and performs a checksum on the output. If the checksum agrees with the correct value, bit 5 is set to "1". The second routine provides a visual test of the LEDs using the drive circuitry. This is accomplished by writing checkered and inverse checkered patterns to the display. Each pattern is displayed for approximately 2 seconds.

During the self test function the display must not be accessed. The time needed to execute the self test function is calculated by multiplying the clock period by 262,144. For example, assume a clock frequency of 58 KHz, then the time to execute the self test function frequency is equal to (262,144/58,000) = 4.5 second duration.

At the end of the self test function, the Character RAM is loaded with blanks, the Control Word Register is set to zeros except for bit 5, and the Flash RAM is cleared and the UDC Address Register is set to all ones.

Clear Function (Bit 7)
Bit 7 of the Control Word will clear the Character RAM and the Flash RAM. Setting bit 7 to a "1" will start the clear function. Three clock cycles (110 µs min. using the internal refresh clock) are required to complete the clear function. The display must not be accessed while the display is being cleared. When the clear function has been completed, bit 7 will be reset to a "0". The ASCII character code for a space (20H) will be loaded into the Character RAM to blank the display and the Flash RAM will be loaded with "0"s. The UDC RAM, UDC Address Register, and the remainder of the Control Word are unaffected.

Display Reset

Figure 7 shows the logic levels needed to Reset the display. The display should be Reset on Power-up. The external Reset clears the Character RAM, Flash RAM, Control Word and resets the internal counters. After the rising edge of the Reset signal, three clock cycles (110 µs min. using the internal refresh clock) are required to complete the reset sequence. The display must not be accessed while the display is being reset. The ASCII Character code for a space (20H) will be loaded into the Character RAM to blank the display. The Flash RAM and Control Word Register are loaded with all "0"s. The UDC RAM and UDC Address Register are unaffected. All displays which operate with the same clock source must be simultaneously reset to synchronize the Flashing and Blinking functions.

$\overline{RST}$	$\overline{CE}$	$\overline{WR}$	$\overline{RD}$	$\overline{FL}$	A_4-A_0	D_7-D_0
0	1	X	X	X	X	X

0 = LOGIC 0; 1 = LOGIC 1; X = DO NOT CARE

NOTE:
IF $\overline{RST}$, $\overline{CE}$ AND $\overline{WR}$ ARE LOW, UNKNOWN DATA MAY BE WRITTEN INTO THE DISPLAY.

Figure 7. Logic Levels to Reset the Display.

Mechanical and Electrical Considerations

The HDSP-213X is a 32 pin dual-in-line package with 24 external pins, which can be stacked horizontally and vertically to create arrays of any size. The HDSP-213X is designed to operate continuously from -55°C to +85°C with a maximum of 20 dots ON per character. Illuminating all thirty-five dots at full brightness is not recommended.

The HDSP-213X is assembled by die attaching and wire bonding 280 LED chips and a CMOS IC to a ceramic substrate. A glass window is placed over the ceramic substrate creating an air gap over the LED wire bonds. A second glass window creates an air gap over the CMOS IC. This package construction makes the display highly tolerant to temperature cycling and allows wave soldering and visual inspection of the IC.

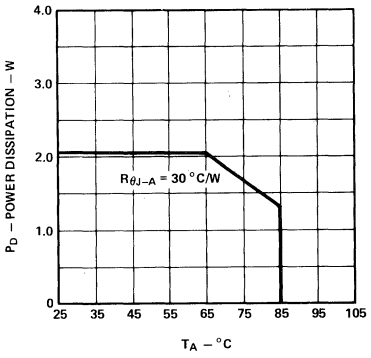


Figure 8. Maximum Power Dissipation vs. Ambient Temperature Derating Based on T_JMAX = 125°C.

The inputs to the CMOS IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HDSP-213X should be stored in antistatic packages or conductive material. During assembly, a grounded conductive work area should be used, and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static charge buildup. Input current latchup is caused when the CMOS inputs are subjected to either a voltage below ground (V_{IN} < ground) or to a voltage higher than V_{DD} ($V_{IN} > V_{DD}$) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{DD}. Voltages should not be applied to the inputs until V_{DD} has been applied to the display. Transient input voltages should be eliminated.

Thermal Considerations

The HDSP-213X has been designed to provide a low thermal resistance path from the CMOS IC to the 24 package pins. This heat is then typically conducted through the traces of the user's printed circuit board to free air. For most applications no additional heatsinking is required.

The maximum operating IC junction temperature is 125°C. The maximum IC junction temperature can be calculated using the following equation:

$$T_J(IC)\ MAX = T_A + (P_D MAX)\ (R\theta_{J\text{-}PIN} + R\theta_{PIN\text{-}A})$$

Where

$$P_D MAX = (V_{DD} MAX)\ (I_{DD} MAX)$$

I_{DD}MAX = 370 mA with 20 dots ON in eight character locations at 25°C ambient. This value is from the Electrical Characteristics table.

$$P_D MAX = (5.5\ V)(0.370\ A) = 2.04\ W$$

Ground Connections

Two ground pins are provided to keep the internal IC logic ground clean. The designer can, when necessary, route the analog ground for the LED drivers separately from the logic ground until an appropriate ground plane is available. On long interconnects between the display and the host system, the designer can keep voltage drops on the analog ground from affecting the display logic levels by isolating the two grounds.

The logic ground should be connected to the same ground potential as the logic interface circuitry. The analog ground and the logic ground should be connected at a common ground which can withstand the current introduced by the switching LED drivers. When separate ground connections are used, the analog ground can vary from -0.3 V to +0.3 V with respect to the logic ground. Voltage below -0.3 V can cause all dots to be on. Voltage above +0.3 V can cause dimming and dot mismatch.

ESD Susceptibility

These displays have ESD susceptibility ratings of CLASS 3 per DOD-STD-1686 and CLASS B per MIL-STD-883C.

Soldering and Post Solder Cleaning Instructions for the HDSP-213X

The HDSP-213X may be hand soldered or wave soldered with SN63 solder. When hand soldering it is recommended that an electronically temperature controlled and securely grounded soldering iron be used. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux can be used. The solder wave temperature should be set at 245°C ± 5°C (473°F ± 9°F), and dwell in the wave should be set between 1-1/2 to 3 seconds for optimum soldering. The preheat temperature should not exceed 105°C (221°F) as measured on the solder side of the PC board.

Post solder cleaning may be performed using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling temperature is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, Genesolv DES, and water.

An aqueous cleaning process may be used. A saponifier, such as Kester Bio-Kleen Formula 5799 or its equivalent, may be added to the wash cycle of an aqueous process to remove rosin flux residues. Organic acid flux residues must be thoroughly removed by an aqueous cleaning process to prevent corrosion of the leads and solder connections. The optimum water temper-

ature is 60°C (140°F). The maximum cumulative exposure of the HDSP-213X to wash and rinse cycles should not exceed 15 minutes. For additional information on soldering and post solder cleaning, see Application Note 1027.

High Reliability Testing

Two standard high reliability testing programs are available. The TXVB program is in conformance with MIL-D-87157 level A Test Tables. The TXVB product is tested to Tables I, II, IIIa and IVa. The TXV program is an HP modification to the full conformance program and offers the 100% screening of Quality Level A, Table I, and Group A, Table II.

Contrast Enhancement

When used with the proper contrast enhancement filters, the HCMS-213X series displays are readable daylight ambients. Refer to Application Note 1029 *Luminous Contrast and Sunlight Readability of the HDSP-238X Series Alphanumeric Displays for Military Applications* for information on contrast enhancement for daylight ambients. Refer to Application Note 1015 *Contrast Enhancement Techniques for LED Displays* for information on contrast enhancement in moderate ambients.

Night Vision Lighting

When used with the proper NVG/DV filters, the HDSP-2131, HDSP-2179 and HDSP-2133 may be used in night vision lighting applications. The HDSP-2131 (yellow), HDSP-2179 (orange) displays are used as master caution and warning indicators. The HDSP-2133 (high performance green) displays are used for general instrumentation. For a list of NVG/DV filters and a discussion on night vision lighting technology, refer to Application Note 1030 *LED Displays and Indicators and Night Vision Imaging System Lighting.* An external dimming circuit must be used to dim these displays to night vision lighting levels to meet NVIS radiance requirements. Refer to AN 1039 *Dimming HDSP-213X Displays to Meet Night Vision Lighting Levels.*

100% Screening
Table I. Quality Level A of MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	2072	Interpreted by HP Procedure 5956-7512-52
2. High Temperature Storage	1032	T_A = 125°C[3], Time = 24 hours
3. Temperature Cycling	1051	Condition B[4], 10 cycles, 15 minute dwell
4. Constant Acceleration	2006	10,000 Gs at Y_1 & Y_2 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K[5]
7. Interim Electrical/ Optical Tests[2]	—	I_{DD}(BLK), I_{DD}(V), I_{DD}(#), I_{IH}, I_{IL}, I_{OH}, I_{OL}, I_V and Visual Function T_A = 25°C
8. Burn-In[1]	1015	Condition B at V_{DD} = 5.5 V, cycle through character set 1 per second, T_A = +85°C, Time = 160 hours
9. Final Electrical Test[2]	—	Same as step 7
10. Delta Determinations	—	I_{DD}(V) & I_{DD}(#) = ±10%, I_V = -20%
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics.
3. T_A = +100°C for HDSP-2133.
4. T_A = -55°C to +100°C for HDSP-2133.
5. Fluid temperature = +100°C for HDSP-2133.

Table II. Group A Electrical Tests – MIL-D-87157

Subgroup Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_{DD}(BLK), I_{DD}(V), I_{DD}(#), I_{IH}, I_{IL}, I_{OH}, I_{OL}, I_V, and function test	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1 except delete I_V and visual function. T_A = +85°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1 except delete I_V and visual function. T_A = -55°C	7
Subgroup 4, 5, and 6 not applicable		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

Notes:
1. Limits and conditions are per the electrical/optical characteristics.

Table IIIa. Group B Electrical Tests – MIL-D-87157

Subgroup Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices 0 Failures
Internal Visual and Design Verification[1]	2075[6]		1 Device 0 Failures
Subgroup 2[2,3] Solderability[7]	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock Temperature Cycle	1051	Condition B1, 15 minute dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K[8]	
Electrical/Optical Endpoints[5]	—	I_{DD}(BLK), I_{DD}(V), I_{DD}(#), I_{IH}, I_{IL}, I_{OH}, I_{OL}, I_V & function, T_A = 25°C	
Subgroup 4 Operating Life Test 340 hrs	1027	T_A = +85°C @ V_{DD} = 5.5 V	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	
Subgroup 5 Non-Operating Storage Life Test 340 hrs	1032	T_A = +125°C[9]	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	

Notes:
1. Visual inspection is performed through the display window.
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend for one cycle.
5. Limits and conditions as per the electrical/optical characteristics.
6. Equivalent to MIL-STD-883, Method 2014.
7. The steam aging is not performed on gold plated leads.
8. Fluid temperature = +100°C for HDSP-2133.
9. T_A = +100°C for HDSP-2133.

Table IVa. Group C, Class A and B of MIL-D-87157

Subgroup Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1[1] Physical Dimensions	2066		2 Devices 0 Failures
Subgroup 2[2] Lead Integrity[7,9]	2004	Condition B2	LTPD = 15
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K[10]	
Subgroup 3 Shock	2016	1500 G. Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1, Y_2 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_{DD}(BLK), I_{DD}(V), I_{DD}(#), I_{IH}, I_{IL}, I_{OH}, I_{OL}, I_V and Visual Function, T_A = 25°C	
Subgroup 4[1,3] Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5 Bond Strength[5]	2037	Condition A	LTPD = 20 C = 0
Subgroup 6 Operating Life Test[6]	1026	T_A = +85°C at V_{DD} = 5.5 V	λ = 10
Electrical/Optical Endpoints[6]	—	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.
9. Initial conditioning is a 15° inward bend for three cycles.
10. Fluid temperature = +100°C for HDSP-2133.

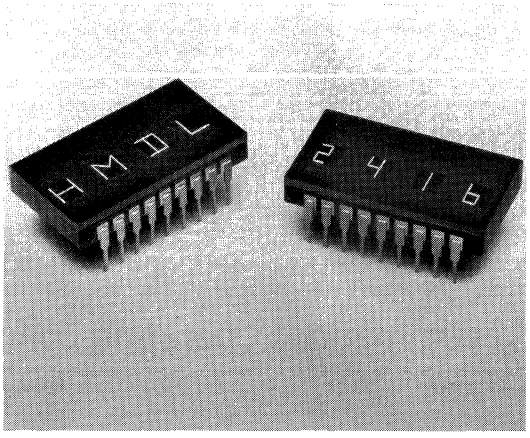
HEWLETT PACKARD

FOUR CHARACTER 3.8mm (0.15 inch) HERMETIC, SMART ALPHANUMERIC DISPLAY

HMDL-2416
HMDL-2416TXV
HMDL-2416TXVB

Features

- **WIDE OPERATING TEMPERATURE RANGE -55° C to +100° C**
- **TRUE HERMETIC PACKAGE**
- **TXVB VERSION CONFORMS TO MIL-D-87157 QUALITY LEVEL A TEST TABLES**
- **CMOS IC FOR LOW POWER CONSUMPTION**
- **SMART ALPHANUMERIC DISPLAY Built-in RAM, ASCII Decoder, and LED Drive Circuitry**
- **VERY FAST ACCESS TIME, 160 ns**
- **EXCELLENT ESD PROTECTION Built-in Protective Diodes**
- **FULL TTL COMPATIBILITY OVER OPERATING TEMPERATURE RANGE**
- **END-STACKABLE**
- **WIDE VIEWING ANGLE**
- **WAVE SOLDERABLE**



Description

The HMDL-2416 is a smart 3.8 mm (0.15") four character, sixteen segment red GaAsP display. It is contained in a hermetic 18 pin dual-in-line, glass sealed ceramic package. The on-board CMOS IC contains memory, ASCII decoder, multiplexing circuitry, and drivers. It has a wide operating temperature range, and is fully TTL compatible, wave solderable, and highly reliable. This display is ideally suited for military and high reliability industrial applications where a rugged, reliable, easy-to-use alphanumeric display is required.

Typical Applications

- **MILITARY EQUIPMENT**
- **AVIONICS**
- **HIGH RELIABILITY INDUSTRIAL EQUIPMENT**

Absolute Maximum Ratings

Supply Voltage, V_{CC} to Ground ..... -0.5 V to 7.0 V

Input Voltage,
Any Pin to Ground ..... -0.5 V to V_{CC} + .5 V

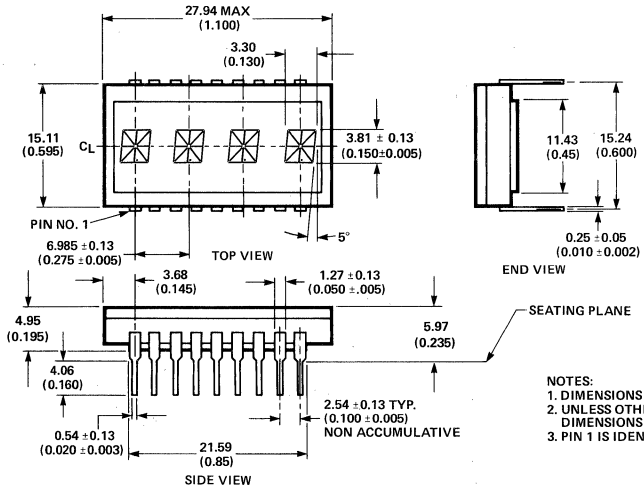
Free Air Operating
Temperature Range, T_A ..... -55° to +100° C

Storage Temperature, T_S ..... -65° to +125° C

Maximum Solder Temperature, 1.59 mm (0.063 in.)
below Seating Plane, t < 5 sec. ..... 260° C

ESD WARNING: The HMDL-2416 is implemented in a standard CMOS process with diode protection of all inputs. The ESD susceptibility of this IC device is Class A of MIL-STD-883 or Class 2 of DOD-STD-1686 and DOD-HDBK-263. Standard precautions for handling CMOS devices should be observed.

Package Dimensions



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	$\overline{CE}_1$ CHIP ENABLE	10	GND
2	$\overline{CE}_2$ CHIP ENABLE	11	D_0 DATA INPUT
3	$\overline{CLR}$ CLEAR	12	D_1 DATA INPUT
4	CUE CURSOR ENABLE	13	D_2 DATA INPUT
5	$\overline{CU}$ CURSOR SELECT	14	D_3 DATA INPUT
6	$\overline{WR}$ WRITE	15	D_6 DATA INPUT
7	A_1 DIGIT SELECT	16	D_5 DATA INPUT
8	A_0 DIGIT SELECT	17	D_4 DATA INPUT
9	V_{CC}	18	$\overline{BL}$ DISPLAY BLANK

NOTES:
1. DIMENSIONS IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±0.38 mm (0.015").
3. PIN 1 IS IDENTIFIED BY INK DOT ON BOTTOM OF PACKAGE.

Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage High	V_{IH}	2.0			V
Input Voltage Low	V_{IL}			0.8	V

DC Electrical Characteristics Over Operating Temperature Range

TYPICAL VALUES

Parameter	Symbol	Units	-55° C	25° C	+100° C	Test Condition
I_{CC} 4 digits on (10 seg/digit)[1,2]	I_{CC}	mA	120	85	70	V_{CC} = 5.0 V
I_{CC} Cursor[2,3,4]	$I_{CC}(\overline{CU})$	mA	170	125	105	V_{CC} = 5.0 V
I_{CC} Blank	$I_{CC}(\overline{BL})$	mA	1.8	1.5	1.3	V_{CC} = 5.0 V $\overline{BL}$ = 0.8 V
Input Current, Max.	I_{IL}	μA	22	17	12	V_{CC} = 5.0 V V_{IN} = 0.8 V
Thermal Resistance Junction to Case	$R\Theta_{J-C}$	°C/W/ Device		20		

GUARANTEED VALUES

Parameter	Symbol	Units	25° C V_{CC} = 5.0 V	Maximum Over Operating Temperature Range V_{CC} = 5.5 V
I_{CC} 4 digits on (10 seg/digit)[1,2]	I_{CC}	mA	115	167
I_{CC} Cursor[2,3,4]	$I_{CC}(\overline{CU})$	mA	165	225
I_{CC} Blank	$I_{CC}(\overline{BL})$	mA	3.5	8.0
Input Current, Max.	I_{IL}	μA	30	40
Power Dissipation[5]	P_D	mW	575	918
Leak Rate	LR	cc/sec		5×10^{-8}

Notes:
1. "%" illuminated in all four characters.
2. Measured at five seconds.
3. Cursor character is sixteen segments and DP on.
4. Cursor operates continuously over operating temperature range.
5. Power dissipation = $V_{CC} \cdot I_{CC}$ (10 seg.).

AC Timing Characteristics Over Temperature at V_{CC} = 4.5 V [1]

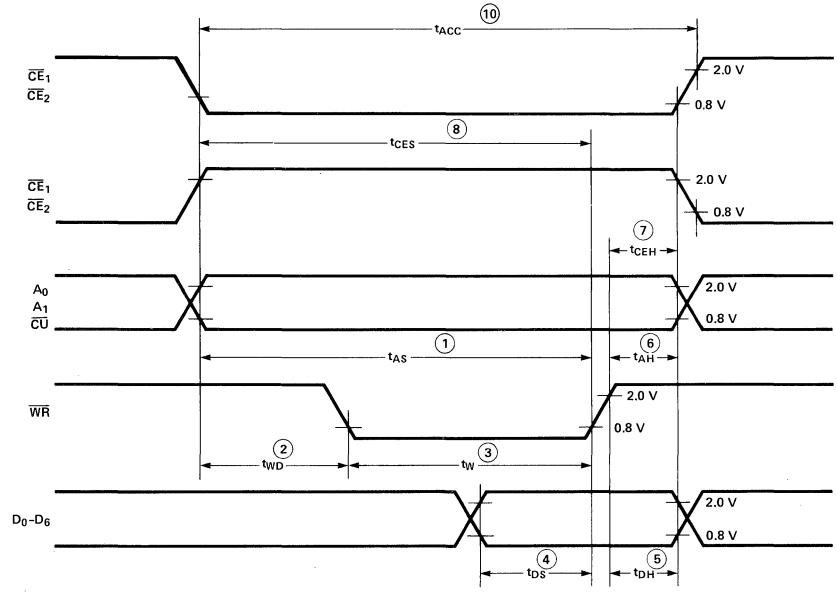
Symbol	Description	-20° C t_{MIN}	25° C t_{MIN}	70° C t_{MIN}	Units
1 t_{AS}	Address Setup Time	90	115	150	ns
2 t_{WD}	Write Delay Time	10	15	20	ns
3 t_W	Write Time	80	100	130	ns
4 t_{DS}	Data Setup Time	40	60	80	ns
5 t_{DH}	Data Hold Time	40	45	50	ns
6 t_{AH}	Address Hold Time	40	45	50	ns
7 t_{CEH}	Chip Enable Hold Time	40	45	50	ns
8 t_{CES}	Chip Enable Setup Time	90	115	150	ns
9 t_{CLR}	Clear Time	2.4	3.5	4.0	ms
10 t_{ACC}	Access Time	130	160	200	ns
	Refresh Rate	420-790	310-630	270-550	Hz

Note: 1. These parameters are guaranteed by design but are not tested.

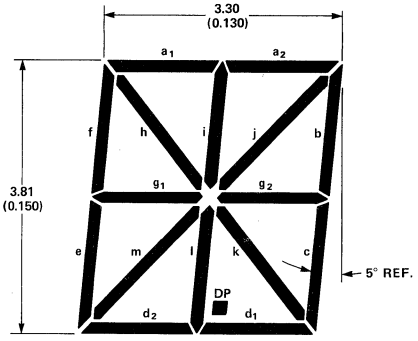
Optical Characteristics

Parameter	Symbol	Test Condition	Min.	Typ.	Units
Peak Luminous Intensity per digit, 8 segments on (character average)	I_V Peak	V_{CC} = 5.0 V "✳" illuminated in all 4 digits (25°C)	0.2	0.6	mcd
Peak Wavelength	λpeak			655	nm
Dominant Wavelength	λ_d			640	nm
Off Axis Viewing Angle				±65	degrees
Digit Size				3.81	mm

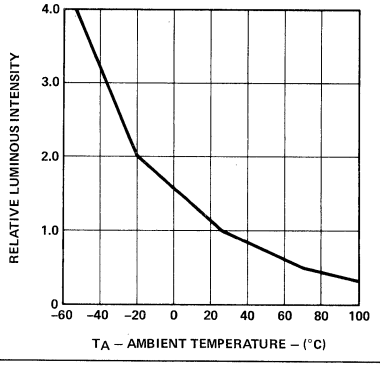
Timing Diagram



Character Font Description



Relative Luminous Intensity vs. Temperature



Electrical Description

Display Internal Block Diagram

Figure 1 shows the internal block diagram for the HMDL-2416 display. The CMOS IC consists of a four-word ASCII memory, a four-word cursor memory, a 64-word character generator, 17 segment drivers, four digit drivers, and the scanning circuitry necessary to multiplex the four monolithic LED characters. In normal operation, the divide-by-four counter sequentially accesses each of the four RAM locations and simultaneously enables the appropriate display digit driver. The output of the RAM is decoded by the character generator which, in turn, enables the appropriate display segment drivers. For each display location, the cursor enable (CUE) selects whether the data from the ASCII RAM (CUE = 0) or the stored cursor (CUE = 1) is to be displayed. The cursor character is denoted by all sixteen segments and the DP ON. Seven-bit ASCII data is stored in RAM. Since the display utilizes a 64-character decoder, half of the possible 128 input combinations are invalid. For each display location where $D_5 = D_6$ in the ASCII RAM, the display character is blanked. The entire display is blanked when $\overline{BL} = 0$.

Data is loaded into the display through the data inputs (D_6- D_0), digit selects (A_1, A_0), chip enables ($\overline{CE}_1$, $\overline{CE}_2$, cursor select ($\overline{CU}$), and write ($\overline{WR}$). The cursor select ($\overline{CU}$) determines whether data is stored in the ASCII RAM ($\overline{CU}$ = 1) or cursor memory ($\overline{CU}$ = 0). When $\overline{CE}_1 = \overline{CE}_2 = \overline{WR} = 0$ and $\overline{CU} = 1$, the information on the data inputs is stored in the ASCII RAM at the location specified by the digit selects (A_1, A_0). When $\overline{CE}_1 = \overline{CE}_2 = \overline{WR} = 0$ and $\overline{CU} = 0$, the information on the data input, D_0, is stored in the cursor at the location specified by the digit selects (A_1, A_0). If $D_0 = 1$, a cursor character is stored in the cursor memory. If $D_0 = 0$, a previously stored cursor character will be removed from the cursor memory.

If the clear input ($\overline{CLR}$) equals zero for one internal display cycle (4 ms minimum), the data in the ASCII RAM will be rewritten with zeroes and the display will be blanked. Note that the blanking input ($\overline{BL}$) must be equal to logical one during this time.

Data Entry

Figure 2 shows a truth table for the HMDL-2416 display. Setting the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) to their low state and the cursor select ($\overline{CU}$) to its high state will enable data loading. The desired data inputs (D_6-D_0) and address inputs (A_1, A_0) as well as the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and cursor select ($\overline{CU}$) must be held stable during the write cycle to ensure that the correct data is stored into the display. Valid ASCII data codes are shown in Figure 3. The display accepts standard seven-bit ASCII data. Note that $D_6 = \overline{D_5}$ for the codes shown in Figure 2. If $D_6 = D_5$ during the write cycle, then a blank will be stored in the display. Data can be loaded into the display in any order. Note that when $A_1 = A_0 = 0$, data is stored in the furthest right-hand display location.

Cursor Entry

As shown in Figure 2, setting the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) to their low state and the cursor select ($\overline{CU}$) to its low state will enable cursor loading. The cursor character is indicated by the display symbol having all 16 segments and the DP ON. The least significant data input (D_0), the digit selects (A_1, A_0), the chip enables ($\overline{CE}_1$, $\overline{CE}_2$), and the cursor select ($\overline{CU}$) must be held stable during the write cycle to ensure that the correct data is stored in the display. If D_0 is in a low state during the write cycle, then a cursor character will be removed at the indicated location. If D_0 is in a high state during the write cycle, then a cursor character will be stored at the indicated location. The presence or absence of a cursor character does not affect the ASCII data stored at that location. Again, when $A_1 = A_0 = 0$, the cursor character is stored in the furthest right-hand display location.

All stored cursor characters are displayed if the cursor enable (CUE) is high. Similarly, the stored ASCII data words are displayed, regardless of the cursor characters, if the cursor enable (CUE) is low. The cursor enable (CUE) has no effect on the storage or removal of the cursor characters within the display. A flashing cursor is displayed by pulsing the cursor enable (CUE). For applications not requiring a cursor, the cursor enable (CUE) can be connected to ground and the cursor select ($\overline{CU}$) can be connected to V_{CC}. This inhibits the cursor function and allows only ASCII data to be loaded into the display.

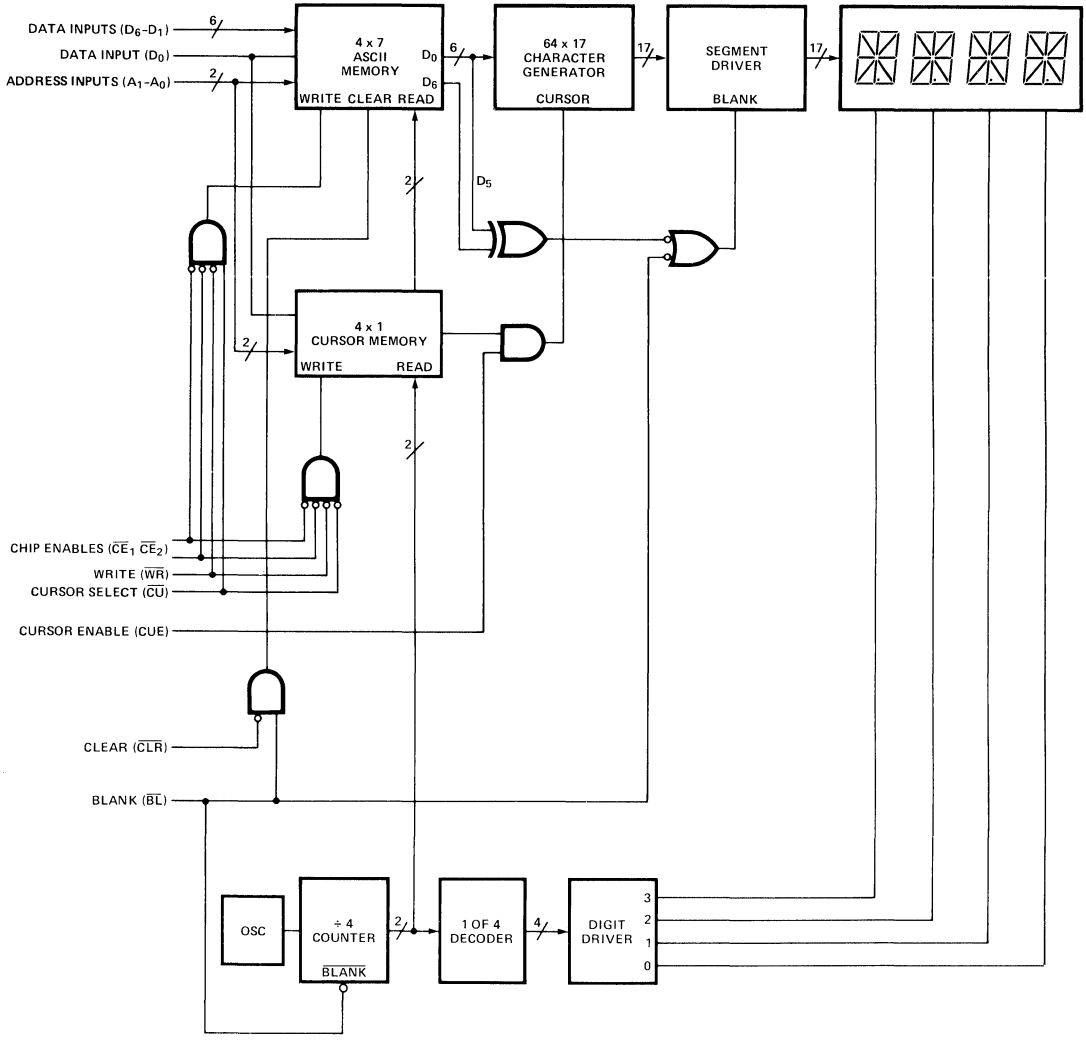


Figure 1. HMDL-2416 Internal Block Diagram

Display Clear

As shown in Figure 2, the ASCII data stored in the display will be cleared if the clear ($\overline{CLR}$) is held low and the blanking input ($\overline{BL}$) is held high for 4 ms minimum. The cursor memory is not affected by the clear ($\overline{CLR}$) input. Cursor characters can be stored or removed even while the clear ($\overline{CLR}$) is low. Note that the display will be cleared regardless of the state of the chip enables ($\overline{CE_1}$, $\overline{CE_2}$). However, to ensure that all four display characters are cleared, $\overline{CLR}$ should be held low for 4 ms following the last write cycle.

Display Blank

As shown in Figure 2, the display will be blanked if the blanking input ($\overline{BL}$) is held low. Note that the display will be blanked regardless of the state of the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) or write ($\overline{WR}$) inputs. The ASCII data stored in the display and the cursor memory are not affected by the blanking input. ASCII data and cursor data can be stored even while the blanking input ($\overline{BL}$) is low. Note that while the blanking input ($\overline{BL}$) is low, the clear ($\overline{CLR}$) function is inhibited. A flashing display can be obtained by applying a low frequency square wave to the blanking input ($\overline{BL}$). Because the blanking input ($\overline{BL}$) also resets the internal display multiplex counter, the frequency applied to the blanking input ($\overline{BL}$) should be much slower than the display multiplex rate. Finally, dimming of the display through the blanking input ($\overline{BL}$) is not recommended.

For further application information please consult Application Note 1026.

Function	$\overline{BL}$	$\overline{CLR}$	CUE	$\overline{CU}$	$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WR}$	A_1	A_0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	DIG_3	DIG_2	DIG_1	DIG_0
Write Data Memory	L	X	X	H	L	L	L	L	L	a	a	a	a	a	a	a	NC	NC	NC	A
				—OR—				L	H	b	b	b	b	b	b	b	NC	NC	B	NC
	X	H	X	H	L	L	L	H	L	c	c	c	c	c	c	c	NC	C	NC	NC
								H	H	d	d	d	d	d	d	d	D	NC	NC	NC
Disable Data Memory Write	X	X	X	H	X	X	H	X	X	X	X	X	X	X	X	X	Previously Written Data			
	X	X	X	H	X	H	X													
	X	X	X	H	H	X	X													
Write Cursor	X	X	X	L	L	L	L	L	L	X	X	X	X	X	X	H	NC	NC	NC	▩
								L	H	X	X	X	X	X	X	H	NC	NC	▩	NC
								H	L	X	X	X	X	X	X	H	NC	▩	NC	NC
								H	H	X	X	X	X	X	X	H	▩	NC	NC	NC
Clear Cursor	X	X	X	L	L	L	L	L	L	X	X	X	X	X	X	L	NC	NC	NC	⬚
								L	H	X	X	X	X	X	X	L	NC	NC	⬚	NC
								H	L	X	X	X	X	X	X	L	NC	⬚	NC	NC
								H	H	X	X	X	X	X	X	L	⬚	NC	NC	NC
Disable Cursor Memory	X	X	X	L	X	X	H	X	X	X	X	X	X	X	X	X	Previously Written Cursor			
	X	X	X	L	X	H	X													
	X	X	X	L	H	X	X													

L = LOGIC LOW INPUT
H = LOGIC HIGH INPUT
X = DON'T CARE

"a" = ASCII CODE CORRESPONDING TO SYMBOL "A"
NC = NO CHANGE
▩ = CURSOR CHARACTER (ALL SEGMENTS ON)

Figure 2a. Cursor/Data Memory Write Truth Table

Function	$\overline{BL}$	$\overline{CLR}$	CUE	$\overline{CU}$	$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WR}$	DIG_3	DIG_2	DIG_1	DIG_0	
CUE	H	H	L	X	X	X	X	A	B	C	D	Display previously written data
	H	H	H	X	X	X	X	▩	▩	▩	▩	Display previously written cursor
Clear	H	L	X	X	X	X	X*	⬚	⬚	⬚	⬚	Clear data memory, cursor memory unchanged
	*NOTE: CLR should be held low for 4 ms following the last WRITE cycle to ensure all data is cleared.											
Blanking	L	X	X	X	X	X	X	⬚	⬚	⬚	⬚	Blank display, data and cursor memories unchanged.

Figure 2b. Displayed Data Truth Table

BITS	D_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	D_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	D_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	D_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
D_6 D_5 D_4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 1 0	2	(space)	!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
0 1 1	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
1 0 0	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1 0 1	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_

Figure 3. HPDL-2416 ASCII Character Set

Mechanical and Electrical Considerations

The HMDL-2416 is an 18 pin dual-in-line package, that can be stacked horizontally and vertically to create arrays of any size. The HMDL-2416 is designed to operate continuously from -55° to +100°C for all possible input conditions including the illuminated cursor in all four character locations. The HMDL-2416 is assembled by die attaching and wire bonding the four GaAsP/GaAs monolithic LED chips and the CMOS IC to a 18 lead ceramic-glass dual-in-line package. It is designed either to plug into DIP sockets or to solder into PC boards.

The inputs of the CMOS IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HMDL-2416 should be stored in anti-static tubes or conductive material. During assembly, a grounded conductive work area should be used. The assembly personnel should use conductive wrist straps. Lab coats made of synthetic materials should be avoided since they are prone to static charge build-up. Input current latchup is caused when the CMOS inputs are subjected to a voltage either below ground (V_{IN} < ground) or to a higher voltage than V_{CC} (V_{IN} > V_{CC}) and a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{CC}, voltages should not be applied to the inputs until V_{CC} has been applied to the display, and transient input voltages should be eliminated.

Soldering and Post Solder Cleaning Instructions for the HMDL-2416

The HMDL-2416 may be hand soldered or wave soldered with SN63 solder. Hand soldering may be safely performed only with an electronically temperature-controlled and securely grounded soldering iron. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux or a water soluble organic acid (OA) flux can be used. The solder wave temperature should be 245°C ±5°C (473°F ±9°F), and the dwell in the wave should be set at 1 1/2 to 3 seconds for optimum soldering.

Post solder cleaning may be accomplished using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, Genesolv DES, and water.

For further information on soldering, refer to Application Note 1027, "Soldering LED Components".

Optical Considerations/ Contrast Enhancement

Each HMDL-2416 display is tested for luminous intensity and marked with an intensity category on the back of the display package. To ensure intensity matching for multiple package applications, all displays for a given panel should have the same category.

The HMDL-2416 display is designed to provide maximum contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Dark Red 63, SGL Homalite H100-1650, Rohm and Haas 2423, Chequers Engraving 118, and 3M R6510. For further information on contrast enhancement, see Hewlett-Packard Application Note 1015.

High Reliability Testing

Two standard high reliability testing programs are available. The TXVB program is in conformance with MIL-D-87157 level A Test Tables. The TXVB product is tested to Tables I, II, IIIa, and IVa. The TXV program is an HP modification to the full conformance program and offers the 100% screening of Quality Level A, Table I, and Group A, Table II.

Part Marking System

Standard Product	With Table I and II	With Tables I, II, IIIa, IVa
HMDL-2416	HMDL-2416TXV	HMDL-2416TXVB

100% Screening

Table I. Quality Level A of MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	2072	Interpreted by HP Procedure 5956-7235-52
2. High Temperature Storage	1032	$T_A = 125°C$, Time = 24 hours
3. Temperature Cycling	1051	Condition B, 10 cycles, 15 min. dwell
4. Constant Acceleration	2006	5,000 G's at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K
7. Interim Electrical/Optical Tests[2]	—	I_{CC}, I_V @ $V_{CC} = 5.0$ V $T_A = 25°C$
8. Burn-In[1]	1015	Condition B at $V_{CC} = 5.5$ V $T_A = 100°C$ t = 160 hours
9. Final Electrical Test[2]	—	I_{CC}%, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$) I_{IL}, I_V @ $V_{CC} = 5.0$ V $T_A = 25°C$
10. Delta Determinations	—	$\Delta I_{CC} = \pm 10\%$ $\Delta I_V = -20\%$ $T_A = 25°C$
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method Applies
2. Limits and conditions are per the electrical optical characteristics.

Table II. Group A Electrical Tests — MIL-D-87157

Subgroup/Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_{CC}%, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V and visual function @ V_{CC} = 5.0 V	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = +100°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = -55°C	7
Subgroup 4, 5, and 6 not applicable		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

Note:
1. Limits and conditions are per the electrical/optical characteristics.

Table IIIa. Group B, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Design Verification[1]	2075[6]		1 Device/ 0 Failures
Subgroup 2[2,3] Solderability	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	Condition B1, 15 minute dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Electrical/Optical Endpoints[5]	—	I_{CC}%, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V @ V_{CC} = 5.0 V and visual function. T_A = 25°C	
Subgroup 4 Operating Life Test (340 hrs.)	1027	T_A = 100°C @ V_{CC} = 5.5 V	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	
Subgroup 5 Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +125°C	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	

Notes:
1. Visual inspection is performed through the display window.
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend for one cycle.
5. Limits and conditions are per the electrical/optical characteristics.
6. Equivalent to MIL-STD-883, Method 2014.

Table IVa. Group C, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2]			
Lead Integrity[7, 9]	2004	Condition B2	LTPD = 15
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	5,000 G's at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_{CC}%, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V @ V_{CC} = 5.0 V and visual function. T_A = 25°C	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			
Operating Life Test[6]	1026	T_A = 100°C @ V_{CC} = 5.5 V	λ = 10
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.
9. Initial conditioning is a 15° inward bend for three cycles.

HEWLETT PACKARD

CMOS Hermetic Extended Temperature Range 5x7 Alphanumeric Displays

Technical Data

HCMS-201X/201XTXV/ 201XTXVB Series HCMS-231X/231XTXV/ 231XTXVB

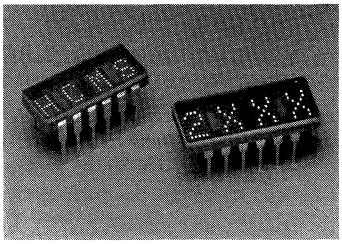
Sunlight Viewable Series HCMS-235X/ 235XTXV/235XTXVB Series

Features

- **On-Board Low Power CMOS IC**
  Integrated Shift Register with Constant Current LED Drivers
- **Wide Operating Temperature Range**
  -55°C to +100°C
- **HI-REL Screening per MIL-D-87157**
  Quality Level A
  TXV or TVXB
- **Hermetic Package**
- **Compact Glass Ceramic 4 Character Package**
  HCMS-201X Series End Stackable
  HCMS-231X/-235X Series X-Y Stackable
- **HCMS-235X Series are Sunlight Viewable**
- **Five Colors**
  Standard Red
  High Efficiency Red
  Orange
  Yellow
  High Performance Green
- **5x7 LED Matrix Displays Full ASCII Set**
- **Two Character Heights**
  3.8mm (0.15 inch)
  5.0mm (0.20 inch)
- **Wide Viewing Angle**
  X Axis = ±50°
  Y Axis = ±65°
- **Long Viewing Distance**
  HCMS-201X Series to 2.6 Meters (8.6 Feet)
  HCMS-231X/-235X Series to 3.5 Meters(11.5 Feet)
- **Categorized for Luminous Intensity**
- **HCMS-2011/2013 HCMS-2311/-2313/-2314 HCMS-2351/-2353/-2354**
  Useable in Night Vision Lighting Applications
- **HCMS-2011/-2013, HCMS-2311/-2313 and HCMS-2351/-2353:**
  Categorized for Color

Typical Applications

- **Military Avionics**
- **Communications Systems**
- **Radar Systems**
- **Fire Control Systems**



Description

The HCMS-201X, HCMS-231X and the sunlight viewable HCMS-235X series are 5x7 LED four character displays contained in 12 pin dual-in-line packages designed for displaying alphanumeric information. The character height for the HCMS-201X series displays is 3.8mm (0.15 inch), and for the HCMS-231X and HCMS-235X series displays the character height is 5.0mm (0.20 inch). The HCMS-201X series displays are available in four LED colors: standard red, high efficiency red, yellow and high performance green. The HCMS-231X series are available in all five

ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED.

LED colors. The HCMS-235X series displays are available in four LED colors: high efficiency red, orange, yellow and high performance green. The HCMS-201X series displays are end stackable. The HCMS-231X and HCMS-235X series displays are end/row stackable.

These displays are designed with on-board CMOS integrated circuits for use in applications where conservation of power is important. The two CMOS ICs form an on-board 28-bit serial-in-parallel-out shift register with constant current output LED row drivers. Decoded column data is clocked into the on-board shift register for each refresh cycle. Full character display is achieved with external column strobing.

Compatibility with HDSP-201X/-231X/-235X TTL IC Series Displays

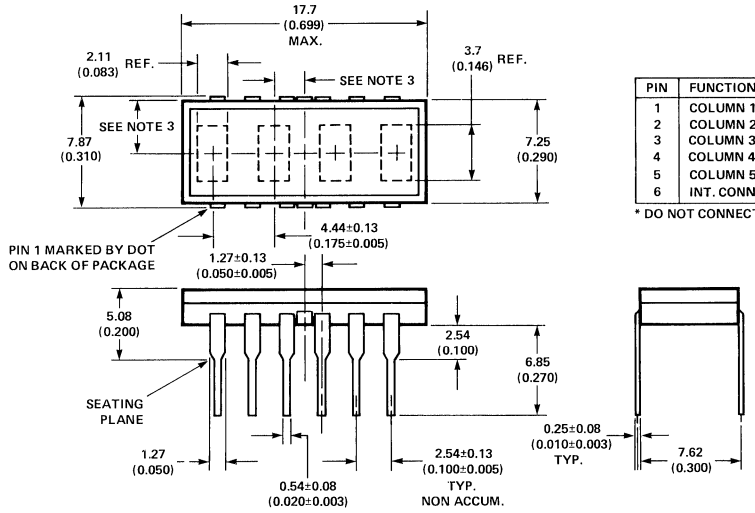
The HCMS-201X, HCMS-231X and HCMS-235X CMOS IC displays are "drop-in" replacements for the equivalent HDSP-201X, HDSP-231X and HDSP-235X TTL IC displays. The 12 pin glass/ceramic package configuration, four digit character matrix and pin functions are identical.

Display Selection Table

Part Number	Character Size	LED Color
HCMS-2010/2010TXV/2010TXVB	3.8 mm (0.15 inch)	Standard Red
HCMS-2011/2011TXV/2011TXVB	3.8 mm (0.15 inch)	Yellow
HCMS-2012/2012TXV/2012TXVB	3.8 mm (0.15 inch)	High-Efficiency Red
HCMS-2013/2013TXV/2013TXVB	3.8 mm (0.15 inch)	High-Performance Green
HCMS-2310/2310TXV/2310TXVB	5.0 mm (0.20 inch)	Standard Red
HCMS-2311/2311TXV/2311TXVB	5.0 mm (0.20 inch)	Yellow
HCMS-2312/2312TXV/2312TXVB	5.0 mm (0.20 inch)	High-Efficiency Red
HCMS-2313/2313TXV/2313TXVB	5.0 mm (0.20 inch)	High-Performance Green
HCMS-2314/2314TXV/2314TXVB	5.0 mm (0.20 inch)	Orange
Sunlight Viewable Displays		
HCMS-2351/2351TXV/2351TXVB	5.0 mm (0.20 inch)	Yellow
HCMS-2352/2352TXV/2352TXVB	5.0 mm (0.20 inch)	High-Efficiency Red
HCMS-2353/2353TXV/2353TXVB	5.0 mm (0.20 inch)	High-Performance Green
HCMS-2354/2354TXV/2354TXVB	5.0 mm (0.20 inch)	Orange

Note:
Basic part numbers (ie. HCMS-2351) are without hi-rel screening. Part numbers with TXV or TXVB suffix (ie. HCMS-2351TXV) are with hi-rel screening per MIL-D-87157, Quality Level A.

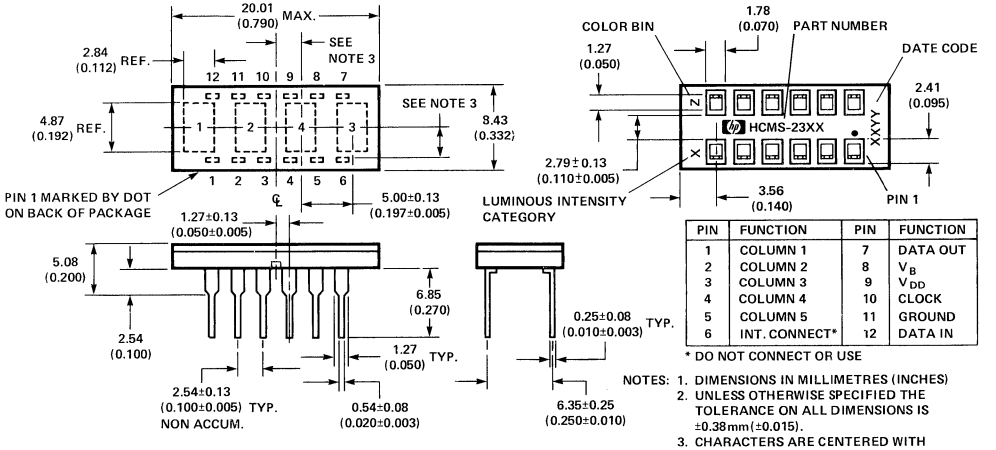
Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{DD}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

* DO NOT CONNECT OR USE

HCMS-201X Series



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{DD}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

* DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN MILLIMETRES (INCHES)
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±0.38mm(±0.015).
3. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±0.13mm (±0.005").
4. LEAD MATERIAL IS COPPER ALLOY, SOLDER DIPPED.

HCMS-231X/-235X Series

Absolute Maximum Ratings

Supply Voltage V_{DD} to Ground .....–0.3 V to 7.0 V
Data Input, Data Output, V_B .....–0.3 V to V_{DD}
Column Input Voltage,V_{COL} .....–0.3 V to V_{DD}
Free Air Operating Temperature Range, T_A .....–55°C to +100°C
Storage Temperature Range, T_S .....–65°C to +125°C
HCMS-2310/-2311/-2312/-2314
HCMS-2351/-2352/-2354
Storage Temperature Range, T_S .....–55°C to +100°C
HCMS-2010/-2011/-2012/-2013
HCMS-2313
HCMS-2353
Maximum Allowable Package Power Dissipation, P_D[1,2]
HCMS-2010/-2011/-2012/-2013 at T_A = 83°C .....0.79 Watts
HCMS-2310/-2311/-2312/-2313/-2314 at T_A = 88°C .....0.92 Watts
HCMS-2351/-2352/-2353/-2354 at T_A = 71°C .....1.31 Watts
Maximum Solder Temperature
1.59 mm (0.063") Below Seating Plane, t ≤ 5 sec .....260°C
ESD Protection @ 1.5kΩ, 100pf .....V_Z = 4 kV (each pin)

Notes:
1. Maximum allowable power dissipation is derived from V_{DD} = 5.25 V, V_B = 2.4 V, V_{COL} = 3.5 V, 20 LEDs ON per character, 20% DF.
2. The power dissipation for these displays should be derated as follows:
   HCMS-201X series derate above 83°C at 17 mW/°C, $R\theta_{J-A}$ = 60°C/W
   HCMS-231X series derate above 88°C at 22 mW/°C, $R\theta_{J-A}$ = 45°C/W
   HCMS-325X series derate above 71°C at 23 mW/°C, $R\theta_{J-A}$ = 45°C/W.

Deratings based on $R\theta_{PC-A}$ = 35°C/W per display for printed circuit board assembly.
See Figure 1 for power derating based on lower $R\theta_{J-A}$ values.

Recommended Operating Conditions Over Operating Temperature Range (-55°C to +100°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}	4.75	5.00	5.25	V
Data Out Current, Low State	I_{OL}			1.6	mA
Data Out Current, High State	I_{OH}			-0.5	mA
Column Input Voltage	V_{COL}	2.75	3.0	3.5	V
Setup Time	t_{SETUP}	10			ns
Hold Time	t_{HOLD}	25			ns
Clock Pulse Width High	$t_{WH(CLOCK)}$	50			ns
Clock Pulse Width Low	$t_{WL(CLOCK)}$	50			ns
Clock High to Low Transition	t_{THL}			200	ns
Clock Frequency	f_{CLOCK}			5	MHz

Electrical Characteristics
Over Operating Temperature Range (-55°C to +100°C)

Parameter	Symbol	Test Conditions	Min.	Typ.*	Max.	Units
Supply Current, Dynamic[1]	I_{DDD}	f_{CLOCK} = 5 MHz		6.2	7.8	mA
Supply Current, Static[2]	I_{DDSoff} I_{DDSon}	V_B = 0.4 V V_B = 2.4 V		1.8 2.2	2.6 3.3	mA
Column Input Current	I_{COL}	V_B = 0.4 V			10	µA
HCMS-2010/-2011/-2012/-2013 HCMS-2310/-2311/-2312/-2313/-2314 HCMS-2351/-2352/-2353/-2354		V_B = 2.4 V V_B = 2.4 V V_B = 2.4 V		310 360 500	384 451 650	mA mA mA
Input Logic High Data, V_B, Clock	V_{IH}	V_{DD} = 4.75 V	2.0			V
Input Logic Low Data, V_B, Clock	V_{IL}	V_{DD} = 5.25 V			0.8	V
Input Current Data, Clock V_B	I_I	V_{DD} = 5.25 V $0 \le V_I \le 5.25$ V $0 \le V_B \le 5.25$ V	 -10 -40		 +10 0	µA
Data Out Voltage	V_{OH}	V_{DD} = 4.75 V I_{OH} = -0.5 mA I_{COL} = 0 mA	2.4	4.2		V
	V_{OL}	V_{DD} = 5.25 V I_{OL} = 1.6 mA I_{COL} = 0 mA		0.2	0.4	V
Power Dissipation Per Package[3] HCMS-2010/-2011/-2012/-2013 HCMS-2310/-2311/-2312/-2313/-2314 HCMS-2351/-2352/-2353/-2354	P_D	V_{DD} = 5.0 V V_{COL} = 3.5 V 17.5% DF V_B = 2.4 V 15 LEDs ON per Character		 414 481 668		mW
Thermal Resistance IC Junction-to-Pin[4] HCMS-2010/-2011/-2012/-2013 HCMS-2310/-2311/-2312/-2313/-2314 HCMS-2351/-2352/-2353/-2354	$R\theta_{J\text{-}PIN}$			 25 10 10		°C/W
Leak Rate					$5x10^{-8}$	cc/sec

*All typical values specified at V_{DD} = 5.0V and T_A = 25°C.

Notes:
1. I_{DD} Dynamic is the IC current while clocking column data through the on-board shift register at a clock frequency of 5MHz, the display is not illuminated.
2. I_{DD} Static is the IC current after column data is loaded and not being clocked through the on-board shift register.
3. Four characters are illuminated with a typical ASCII character composed of 15 dots per character.
4. IC junction temperature $T_J(IC) = (P_D)(R\theta_{J\text{-}PIN} + R\theta_{PC\text{-}A}) + T_A$

Optical Characteristics at $T_A = 25°C$

Standard Red HCMS-2010/-2310

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2010	I_{vPEAK}	$V_{DD} = 5.0$ V, $V_{COL} = 3.5$ V, $V_B = 2.4$ V, $T_j = 25°C$[7]	105	200		µcd
HCMS-2310			220	370		
Dominant Wavelength[8]	λ_d			639		nm
Peak Wavelength	λ_{PEAK}			655		nm

Yellow HCMS-2011/-2311/-2351

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2011	I_{vPEAK}	$V_{DD} = 5.0$ V, $V_{COL} = 3.5$ V, $V_B = 2.4$ V, $T_j = 25°C$[7]	400	750		µcd
HCMS-2311			650	1140		
HCMS-2351			2400	3400		
Dominant Wavelength[6,8]	λ_d			585		nm
Peak Wavelength	λ_{PEAK}			583		nm

High Efficiency Red HCMS-2012/-2312/-2352

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2012	I_{vPEAK}	$V_{DD} = 5.0$ V, $V_{COL} = 3.5$ V, $V_B = 2.4$ V, $T_j = 25°C$[7]	400	1430		µcd
HCMS-2312			650	1430		
HCMS-2352			1920	2850		
Dominant Wavelength[8]	λ_d			625		nm
Peak Wavelength	λ_{PEAK}			635		nm

High Performance Green HCMS-2013/-2313/-2353

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2013	I_{vPEAK}	$V_{DD} = 5.0$ V, $V_{COL} = 3.5$ V, $V_B = 2.4$ V, $T_j = 25°C$[7]	850	1550		µcd
HCMS-2313			1280	2410		
HCMS-2353			2400	3000		
Dominant Wavelength[6,8]	λ_d			574		nm
Peak Wavelength	λ_{PEAK}			568		nm

Orange HCMS-2314/-2354

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Peak Luminous Intensity per LED[5,9] (Character Average) HCMS-2314	I_{vPEAK}	V_{DD} = 5.0 V V_{COL} = 3.5 V V_B = 2.4 V T_i = 25°C[7]	650	1430		µcd
HCMS-2354			1920	2850		
Dominant Wavelength[8]	λ_d			602		nm
Peak Wavelength	λ_{PEAK}			600		nm

All typical values specified at V_{DD} = 5.0 V and T_A = 25°C unless otherwise noted.

Notes:

5. These LED displays are categorized for luminous intensity, with the intensity category designated by a letter code on the back of the package.
6. The HCMS-2011/-2311/-2351 and HCMS-2013/-2313/-2353 are categorized for color with the color category designated by a number on the back of the package.
7. Ti refers to the initial case temperature of the display immediately prior to the light measurement.
8. Dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram, and represents the single wavelength which defines the color of the device.
9. The luminous sterance of the individual LED pixels may be calculated using the following equations:

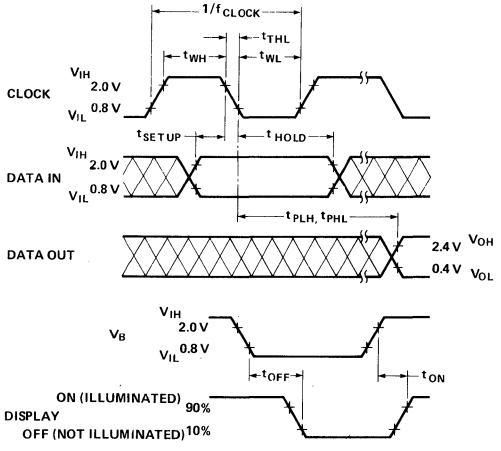
$L_v(cd/m^2) = I_v(Candela)*DF/A(Metre)^2$

$L_v(Footlamberts) = \pi I_v(Candela)*DF/A(Foot)^2$

Where: A = LED pixel area = $5.3 \times 10^{-8} M^2$ or $5.8 \times 10^{-7} ft^2$

DF = LED on-time duty factor

Switching Characteristics, T_A = –55°C to +100°C



Parameter	Condition	Typ.	Max.	Units
f_{clock} CLOCK Rate			5	MHz
t_{PLH}, t_{PHL} Propagation Delay CLOCK to DATA OUT	C_L = 15 pF R_L = 2.4 kΩ		105	ns
t_{OFF} V_B (0.4 V) to Display OFF		4	5	µs
t_{ON} V_B (2.4 V) to Display ON		1	2	

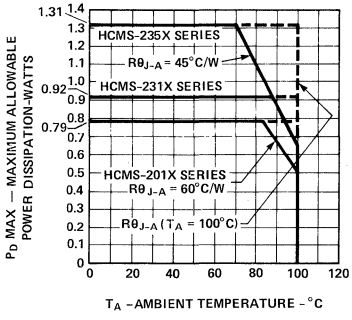


Figure 1. Maximum Allowable Power Dissipation vs Ambient Temperature as a Function of Thermal Resistance Junction-to-Ambient, $R\theta_{J-A}$. Derated Operation Assumes $R\theta_{PC-A}$ = 35°C/W per Display for Printed Circuit Board. T_J (IC) MAX = 130°C. $R\theta_{J-A}$ (T_A = 100°C) = 22°C/W for HCMS-235X Series = 32°C/W for HCMS-231X Series = 38°C/W for HCMS-201X Series

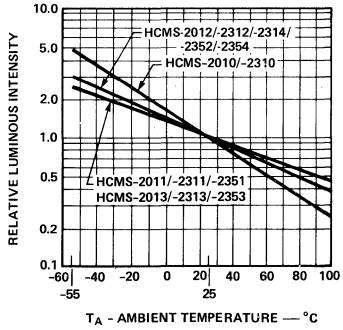


Figure 2. Relative Luminous Intensity vs Display Pin Temperature

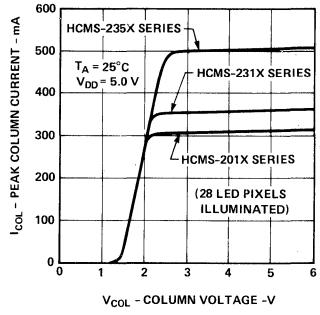


Figure 3. Peak Column Current vs Column Voltage

Electrical Description

Each display device contains four 5x7 LED dot matrix characters and two CMOS integrated circuits, as shown in Figure 4. The two CMOS integrated circuits form an on-board 28 bit serial-in-parallel-out shift register that will accept standard TTL logic levels. The Data Input, pin 12, is connected to bit position 1 and the Data Output, pin 7, is connected to bit position 28. The shift register outputs control constant current sinking LED row drivers. The nominal current sink per LED driver is 11mA for the HCMS-201X displays, 13mA for the HCMS-231X displays and 18mA for the HCMS-235X displays. A logic 1 stored in the shift register enables the corresponding LED row driver and a logic 0 stored in the shift register disables the corresponding LED row driver.

The electrical configuration of these CMOS IC alphanumeric displays allows for an effective interface to a display controller circuit that supplies decoded character information. The row data for a given column (one 7 bit byte per character) is loaded (bit serial) into the on-board 28 bit shift register with high to low transitions of the Clock input. To load decoded character information into the display, column data for character 4 is loaded first and the column data for character 1 is loaded last in the following manner. The 7 data bits for column 1, character 4, are loaded into the on-board shift register. Next, the 7 data bits for column 1, character 3, are loaded into the shift register, shifting the character 4 data over one character position. This process is repeated for the other two characters until all 28 bits of column data (four 7 bit bytes of character column data) are loaded into the on-board shift register. Then the column 1 input, V_{COL} pin 1, is energized to illuminate column 1 in all four characters. This process is repeated for columns 2, 3, 4 and 5. All V_{COL} inputs should be at logic low to insure the display is off when loading data. The display will be blanked when the blanking input V_B, pin 8, is at logic low regardless of the outputs of the shift register or whether one of the V_{COL} inputs is energized.

Refer to Application Note 1016 for drive circuit information.

ESD Susceptibility

The HCMS-201X/-231X/-235X series displays have an ESD susceptibility ratings of CLASS 3 per DOD-STD-1686 and CLASS B per MIL-STD-883C. It is recommended that normal CMOS handling precautions be observed with these devices.

Soldering and Post Solder Cleaning

These displays may be soldered with a standard wave solder process using either an RMA flux and solvent cleaning or an OA flux and aqueous cleaning.

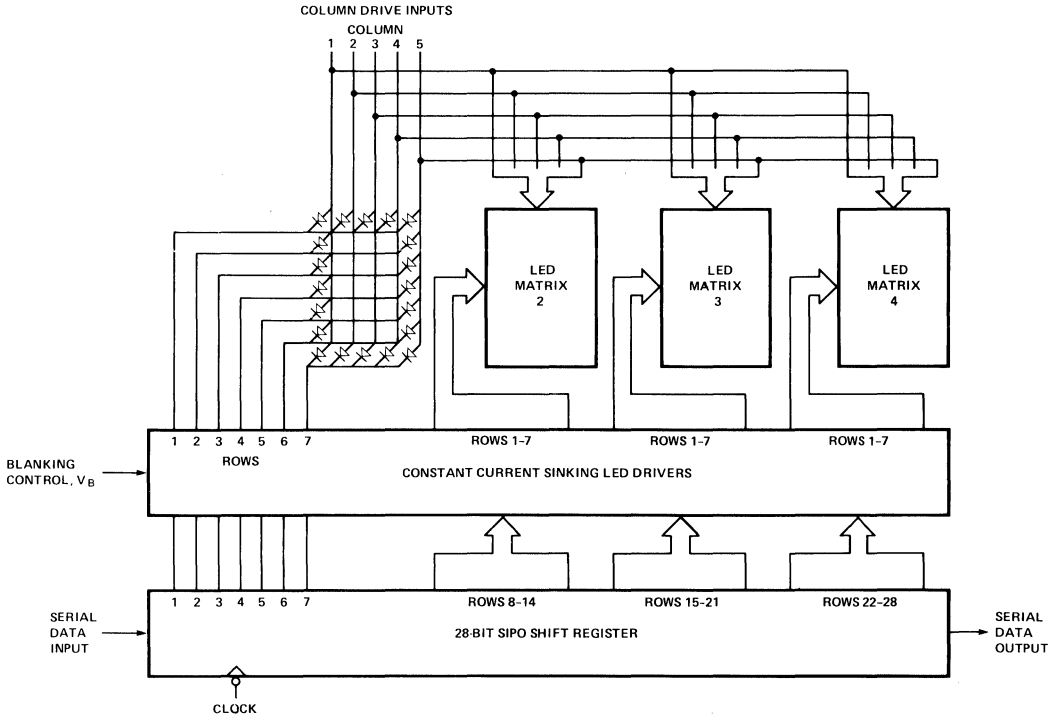


Figure 4. Block Diagram of an HCMS-2XXX Series LED Alphanumeric Display.

For optimum soldering, the solder wave temperature should be 245°C and the dwell time for any display lead passing through the wave should be 1 1/2 to 2 seconds. The recommended solvent for post solder cleaning is Genesolv DES, manufactured by Allied Chemical. For aqueous cleaning, a water temperature of 60°C (140°F) with an immersion time not exceeding 15 minutes is recommended. For more detailed information, refer to Application *Note 1027 Soldering LED Components.*

Contrast Enhancement

When used with the proper contrast enhancement filters, the HCMS-235X series displays are readable in sunlight and the HCMS-201X/231X series displays are readable in daylight ambients. Refer to Application Note 1029 *Luminous Contrast and Sunlight Readability of the HDSP-238X Series Alphanumeric Displays* for Military Applications for information on contrast enhancement for sunlight and daylight ambients. Refer to Application Note 1015 *Contrast Enhancement Techniques for LED Displays* for information on contrast enhancement in moderate ambients.

Night Vision Lighting

When used with the proper NVG/DV filters, the HCMS-2311/-2351 and HCMS-2133/-2353 displays may be used in night vision lighting applications. The HCMS-2311/-2351 (yellow) displays are used as master caution and warning indicators. The HCMS-2313/-2353 (high performance green) displays are used for general instrumentation. For a list of NVG/DV filters and a discussion on night vision lighting technology, refer to Application Note 1030 *LED Displays and Indicators and Night Vision Imaging System Lighting.*

Controller Circuits, Power Calculations and Display Dimming

Refer to Application Note 1016 *Using the HDSP-2000 Alphanumeric Display Family* for information on controller circuits to drive these displays, how to do power calculations and a technique for display dimming.

Table I. Quality Level A of MIL-D-87157 – 100% Screening

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	2072	Interpreted by HP Procedure 5956-7512-52
2. High Temperature Storage	1032	T_A = 125°C, Time = 24 hours[3]
3. Temperature Cycling	1051	Condition B, 10 cycles, 15 minute dwell
4. Constant Acceleration	2006	10,000 G's at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K[4]
7. Interim Electrical/ Optical Tests[1]	—	I_{DD} (at V_B = 0.4 V and 2.4 V), I_{COL} (at V_B = 0.4 V and 2.4 V) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} and I_{VPEAK}. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C
8. Burn-In[1]	1015	Condition B at V_{DD} = V_B = 5.25 V, V_{COL} = 3.5 V, T_A = +100°C LED ON-Time Duty Factor = 5%, 35 Dots On; t = 160 hours
9. Final Electrical Test[2]	—	Same as step 7
10. Delta Determinations	—	ΔI_{DD} = ±6 mA, ΔI_{IH} (clock) = ±10 µA, ΔI_{IH} (Data In) = ±10 µA ΔI_{OH} = ±10% of initial value, and ΔI_V = -20%, T_A = 25°C
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.
3. T_A = +100°C for HCMS-2013/-2313/-2353.
4. Fluid temperature = +100°C for HCMS-2013/-2313/-2353.

Table II. Group A Electrical Tests – MIL-D-87157

Subgroup Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_{DD} (at V_B = 0.4 V and 2.4 V), I_{COL} (at V_B = 0.4 V and 2.4 V) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and I_{VPEAK}. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test.	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1 except delete I_V and visual function, T_A = +100°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1 except delete I_V and visual function, T_A = -55°C	7
Subgroup 4, 5, and 6 not tested		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

Notes:
1. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

Table IIIa. Group B, Class A and B of MIL-D-87157

Subgroup Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Design Verification[1]	2075[7]		1 Device/ 0 Failures
Subgroup 2[2,3] Solderability	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	Condition B1, 15 minute dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K[8]	
Electrical/Optical Endpoints[5]	—	I_{DD} (at V_B = 0.4 V and 2.4 V), I_{COL} (at V_B = 0.4 V and 2.4 V), I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and I_{VPEAK}. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C	
Subgroup 4 Operating Life Test (340 hrs.)	1027	T_A = +100°C at V_{DD} = V_B = 5.25 V, V_{COL} = 3.5 V, LED ON-Time Duty Factor = 5%, 35 Dots On	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	
Subgroup 5 Non-Operating Storage Life Test (340 hrs.)	1032	T_A = +125°C[6]	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	

Notes:
1. Visual inspection is performed through the display window.
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend for one cycle.
5. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.
6. T_A = 100°C for HCMS-2013/-2313/-2353.
7. Equivalent to MIL-STD-883, Method 2014.
8. Fluid temperature = +100°C for HCMS-2013/-2313/-2353.

Table IVa. Group C, Class A and B of MIL-D-87157

Subgroup Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2] Lead Integrity[7,9]	2004	Condition B2	LTPD = 15
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K[10]	
Subgroup 3 Shock	2016	1500G. Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_{DD} (at V_B = 0.4 V and 2.4 V), I_{COL} (at V_B = 0.4 V and 2.4 V), I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL}, Visual Function and I_{VPEAK}. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C	
Subgroup 4[1,3] Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5 Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6 Operating Life Test[6]	1026	T_A = +100°C at V_{DD} = V_B = 5.25 V, V_{COL} = 3.5 V LED ON-Time Duty Factor = 5%, 35 Dots On	λ = 10
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

Notes:

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical specifications.
9. Initial conditioning is a 15° inward bend for three cycles.
10. Fluid temperature = +100°C for HCMS-2013/-2313/-2353.

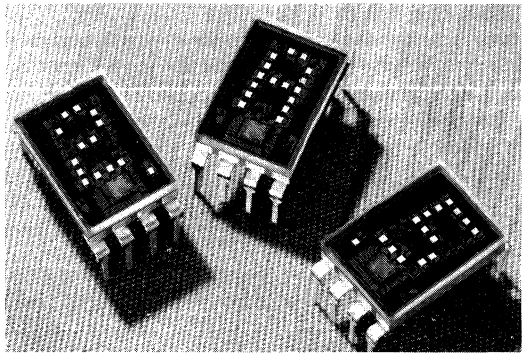
HEWLETT PACKARD

JAN QUALIFIED, HERMETIC, NUMERIC AND HEXADECIMAL DISPLAYS FOR MILITARY APPLICATIONS

4N51 / 4N51TXV / M87157/00101AAX
4N52 / 4N52TXV / M87157/00102AAX
4N53 / 4N53TXV / M87157/00103AAX
4N54 / 4N54TXV / M87157/00104AAX

Features

- **MILITARY QUALIFIED LISTED ON MIL-D-87157 QPL**
- **TRUE HERMETIC PACKAGE**
- **TXV VERSION AVAILABLE**
- **THREE CHARACTER OPTIONS Numeric, Hexadecimal, Over Range**
- **4 x 7 DOT MATRIX CHARACTER**
- **PERFORMANCE GUARANTEED OVER TEMPERATURE**
- **HIGH TEMPERATURE STABILIZED**
- **SOLDER DIPPED LEADS**
- **MEMORY LATCH/DECODER/DRIVER TTL Compatible**
- **CATEGORIZED FOR LUMINOUS INTENSITY**



Description

These standard red solid state displays have a 7.4 mm (0.29 inch) dot matrix character and an on-board IC with data memory latch/decoder and LED drivers in a glass/ceramic package. These devices utilize a solder glass frit seal and conform to the hermeticity requirements of MIL-D-87157, the general specification for LED displays. These 4N5X series displays are designed for use in military and aerospace applications.

These military qualified displays are designated as M87157/00101 AAX through -/00104AAX in the MIL-D-87157 Qualified Parts List (QPL). The letter designations at the end of the part numbers are defined as follows: "A" signifies MIL-D-87157 Quality Level A. "A" signifies solder dipped leads, "X" signifies the luminous intensity category.

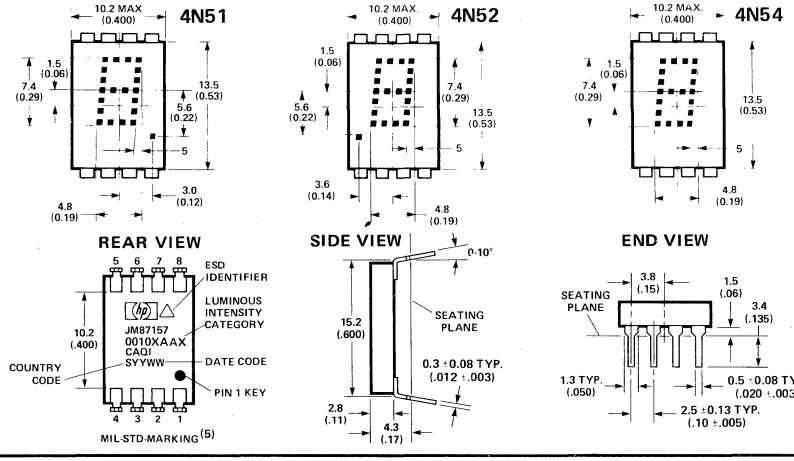
The 4N51 numeric display decodes positive 8421 BCD logic inputs into characters 0-9, a "—" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point.

The 4N52 is the same as the 4N51 except that the decimal point is located on the left-hand side of the digit.

The 4N54 hexadecimal display decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory.

The 4N53 is a "±1." overrange display, including a right-hand decimal point.

Package Dimensions*



PIN	FUNCTION	
	4N51 4N52 NUMERIC	4N54 HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38mm (±.015")
3. Digit center line is ±.25mm (±.01") from package center line.
4. Solder dipped leads.
5. See over range package drawing for HP standard marking.

*JEDEC Registered Data.

Absolute Maximum Ratings*

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1,2]	T_A	−55	+100	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	V_{CC}	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ⩽ 5 seconds			260	°C

Recommended Operating Conditions*

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1,2]	T_A	−55		+100	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics* (T_A = −55°C to +100°C, unless otherwise specified)

Description	Symbol	Test Conditions	Min.	Typ. [4]	Max.	Unit
Supply Current	I_{CC}	V_{CC} = 5.5 V (Characters "5." or "B")		112	170	mA
Power dissipation	P_T			560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_A=25°C	40	85		μcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			50	μA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			1.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+100	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+130	μA
Peak wavelength	λ_{PEAK}	T_A=25°C		655		nm
Dominant Wavelength [8]	λ_d	T_A=25°C		640		nm
Weight**				1.0		gm
Leak Rate					$5x10^{-8}$	cc/sec

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50°C/W; Θ_{JC}=15°C/W. 2. Θ_{CA} of a mounted display should not exceed 35°C/W for operation up to T_A=+100°C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_A=25°C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship: $I_V(T_A)=I_{V(25°C)}(.985)^{[T_A-25°C]}$ 7. Applies only to 4N54. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

*JEDEC Registered Data. **Non Registered Data.

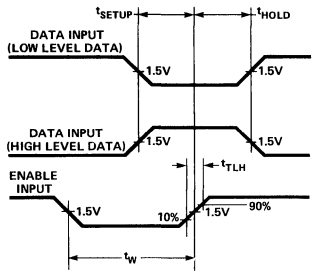


Figure 1. Timing Diagram of 4N51-4N54 Series Logic.

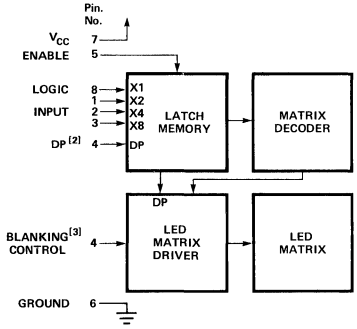


Figure 2. Block Diagram of 4N51-4N54 Series Logic.

TRUTH TABLE					
BCD DATA[1]				4N51 AND 4N52	4N54
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	⊟	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	⋯	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE[1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING[3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

Notes:

1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 4N51 and 4N52 displays.
3. The blanking control input, B, pertains only to the 4N54 hexadecimal display. Blanking input has no effect upon display memory.

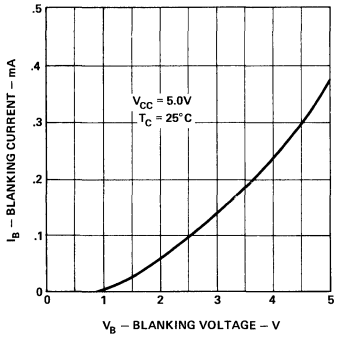


Figure 3. Typical Blanking Control Current vs. Voltage for 4N54.

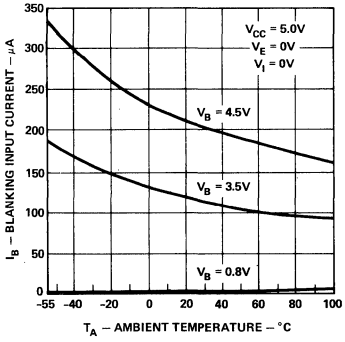


Figure 4. Typical Blanking Control Input Current vs. Ambient Temperature for 4N54.

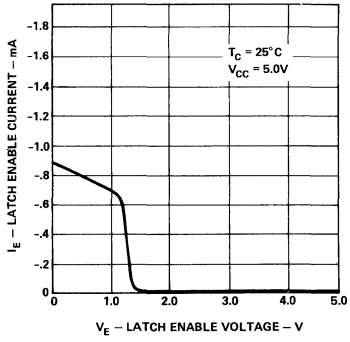


Figure 5. Typical Latch Enable Input Current vs. Voltage.

*JEDEC Registered Data.

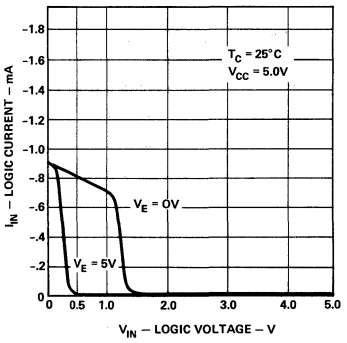


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage.

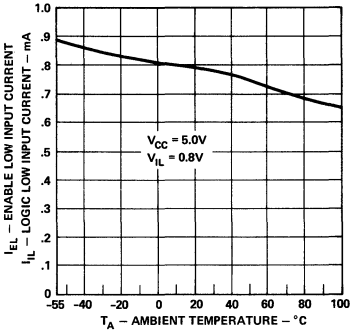


Figure 7. Typical Logic and Enable Low Input Current vs. Ambient Temperature.

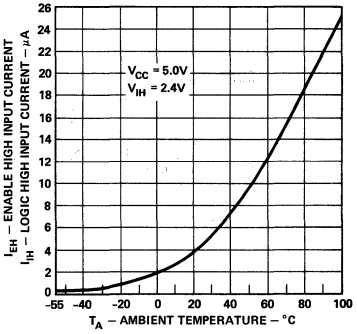


Figure 8. Typical Logic and Enable High Input Current vs. Ambient Temperature.

Operational Considerations

ELECTRICAL

The 4N51-4N54 series devices use a modified 4 x 7 dot matrix of light emitting diodes (LED's) to display decimal/hexadecimal numeric information. The LED's are driven by constant current drivers. BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. To avoid the latching of erroneous information, the enable pulse rise time should not exceed 200 nanoseconds. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7MHz rate.

The blanking control input on the 4N54 display blanks (turns off) the displayed hexadecimal information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 3.5 volts. This may be easily achieved by using an open collector TTL gate and a pull-up resistor. For example, (1/6) 7416 hexinverter buffer/driver and a 120 ohm pull-up resistor will provide sufficient drive to blank eight displays. The size of the blanking pull-up resistor may be calculated from the following formula, where N is the number of digits:

$$R_{blank} = (V_{CC} - 3.5V)/[N\ (1.0mA)]$$

The decimal point input is active low true and this data is latched into the display memory in the same fashion as the BCD data. The decimal point LED is driven by the on-board IC.

The ESD susceptibility of the IC devices is Class A of MIL-STD-883 or Class 2 of DOD-STD-1686 and DOD-HDBK-263.

MECHANICAL

4N51-4N54 series displays are hermetically tested for use in environments which require a high reliability device. These displays are designed and tested to meet a helium leak rate of 5 x 10^{-8} CC/SEC and a fluorocarbon gross leak bubble test.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54mm (0.100 inch) and the lead row spacing is 15.24mm (0.600 inch). These displays may be end stacked with 2.54mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100°C, it is important to maintain a case-to-ambient thermal resistance of less than 35°C/watt as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

PRECONDITIONING

4N51-4N54 series displays are 100% preconditioned by 24 hour storage at 125° C.

CONTRAST ENHANCEMENT

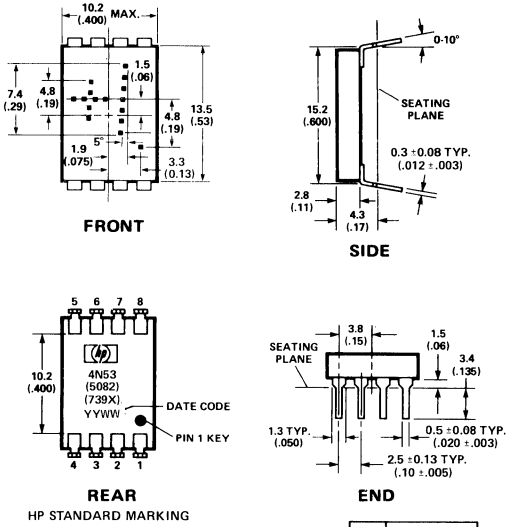
The 4N51-4N54 displays have been designed to provide the maximum posible ON/OFF contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60 and Dark Red 63, SGL Homalite H100-1605, 3M Light Control Film and Polaroid HRCP Red Circular Polarizing Filter. For further information see Hewlett-Packard Application Note 1015.

*JEDEC Registered Data.

Solid State Over Range Display

For display applications requiring a ±, 1, or decimal point designation, the 4N53 over range display is available. This display module comes in the same package as the 4N51-4N54 series numeric display and is completely compatible with it.

Package Dimensions*



NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±.38 MM (± .015 INCHES).

PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{cc}
8	Minus/Plus

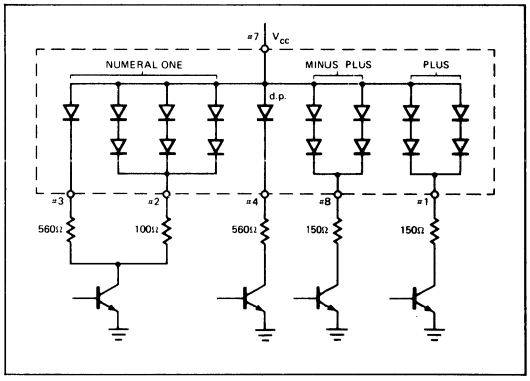


Figure 9. Typical Driving Circuit.

TRUTH TABLE

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 9 cutoff.
H: Line switching transistor in Figure 9 saturated.
X: 'Don't care'

Electrical/Optical Characteristics*

4N53 (T_A = -55°C to +100°C, Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		280	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	40	85		µcd
Peak wavelength	λpeak	T_C = 25°C		655		nm
Dominant Wavelength	λd	T_C = 25°C		640		nm
Weight * *				1.0		gm

Recommended Operating Conditions*

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 9 for recommended resistor values.

*JEDEC Registered Data. **Non Registered Data.

Absolute Maximum Ratings*

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	-65	+125	°C
Operating temperature, ambient	T_A	-55	+100	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

High Reliability Testing

Two standard reliability testing programs are available. The military program provides QPL parts that comply to MIL-D-87157 Quality Level A, per Tables I, II, IIIa, and IVa. A second program is an HP modification to the full conformance program and offers the 100% screening portion of Level A, Table I, and Group A, Table II. In addition, a MIL-D-87157 Level B equivalent testing program is available upon request.

PART MARKING SYSTEM

Standard Product	With Table I and II	With Tables I, II, IIIa and IVa
PREFERRED PART NUMBER SYSTEM		
4N51	4N51TXV	M87157/00101AAX
4N52	4N52TXV	M87157/00102AAX
4N54	4N54TXV	M87157/00104AAX
4N53	4N53TXV	M87157/00103AAX

100% Screening

TABLE I.
QUALITY LEVEL A OF MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	2072	Interpreted by HP Procedure 5956-7572-52
2. High Temperature Storage	1032	T_A = 125°C, Time = 24 hours
3. Temperature Cycling	1051	Condition B, 10 Cycles, 15 Min. Dwell
4. Constant Acceleration	2006	10,000 G's at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K
7. Interim Electrical/Optical Tests[2]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} T_A = 25°C
8. Burn-In[1, 3]	1015	Condition B at V_{CC} = 5V and cycle through logic at 1 character per second. T_A = 100°C, t = 160 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	ΔI_V = -20%, ΔI_{CC} = ± 10 mA, ΔI_{IH} = ±10μA and ΔI_{EH} = ±13 μA
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics.
3. Burn-in for the over range display shall use Condition B at a nominal I_F = 8 mA per LED, with all LEDs illuminated for t = 160 hours minimum.

TABLE II
GROUP A ELECTRICAL TESTS — MIL-D-87157

Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} and visual function, T_A = 25°C	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. T_A = +100°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. T_A = -55°C	7
Subgroup 4, 5, and 6 not applicable		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

1. Limits and conditions are per the electrical/optical characteristics.

TABLE IIIa
GROUP B, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Design Verification[1]	2075[7]		1 Device/ 0 Failures
Subgroup 2[2,3]			
Solderability	2026	T_A = 245° C for 5 seconds	LTPD = 15
Subgroup 3			
Thermal Shock (Temp. Cycle)	1051	Condition B1, 15 Min. Dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Electrical/Optical Endpoints[5]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual function. T_A = 25° C	
Subgroup 4			
Operating Life Test (340 hrs.)[6]	1027	T_A = +100° C at V_{CC} = 5.0V and cycling through logic at 1 character per second.	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3.	
Subgroup 5			
Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +125° C	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	

Notes:
1. Visual inspection performed through the display window.
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend, one cycle.
5. Limits and conditions are per the electrical/optical characteristics.
6. Burn-in for the over range display shall use Condition B at a nominal I_F = 8 mA per LED, with all LEDs illuminated for t = 160 hours minimum.
7. Equivalent to MIL-STD-883, Method 2014.

TABLE IVa
GROUP C, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7,9]			LTPD = 15
Lead Integrity	2004	Condition B2	
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual Function, $T_A = 25°C$	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			$\lambda = 10$
Operating Life Test[6]	1026	$T_A = +100°C$	
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C Life Test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.
9. Initial conditioning is a 15° inward bend, three cycles.

HEWLETT PACKARD

HERMETIC, NUMERIC AND HEXADECIMAL DISPLAYS FOR MILITARY APPLICATIONS

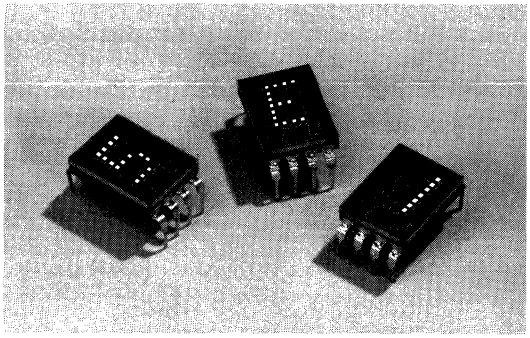
HIGH EFFICIENCY RED	
Low Power	HDSP-078X/078XTXV/078XTXVB
High Brightness	HDSP-079X/079XTXV/079XTXVB
YELLOW	HDSP-088X/088XTXV/088XTXVB
High Performance GREEN	HDSP-098X/098XTXV/098XTXVB

Features

- **CONFORM TO MIL-D-87157, QUALITY LEVEL A TEST TABLES**
- **TRUE HERMETIC PACKAGE FOR HIGH EFFICIENCY RED AND YELLOW[1]**
- **TXV AND TXVB VERSIONS AVAILABLE**
- **THREE CHARACTER OPTIONS**
  Numeric, Hexadecimal, Over Range
- **THREE COLORS**
  High Efficiency Red, Yellow, High Performance Green
- **4 x 7 DOT MATRIX CHARACTER**
- **HIGH EFFICIENCY RED, YELLOW, AND HIGH PERFORMANCE GREEN**
- **TWO HIGH EFFICIENCY RED OPTIONS**
  Low Power, High Brightness
- **PERFORMANCE GUARANTEED OVER TEMPERATURE**
- **HIGH TEMPERATURE STABILIZED**
- **GOLD PLATED LEADS**
- **MEMORY LATCH/DECODER/DRIVER**
  TTL Compatible
- **CATEGORIZED FOR LUMINOUS INTENSITY**

Description

These solid state displays have a 7.4 mm (0.29 inch) dot matrix character and an onboard IC with data memory latch/decoder and LED drivers in a glass/ceramic package.



The hermetic HDSP-078X,-079X/-088X displays utilize a solder glass frit seal. The HDSP-098X displays utilize an epoxy glass-to-ceramic seal. All packages conform to the hermeticity requirements of MIL-D-87157, the general specification for LED displays. These displays are designed for use in military and aerospace applications.

The numeric devices decode positive BCD logic into characters "0-9", a "—" sign, decimal point, and a test pattern. The hexadecimal devices decode positive BCD logic into 16 characters, "0-9, A-F". An input is provided on the hexadecimal devices to blank the display (all LEDs off) without losing the contents of the memory.

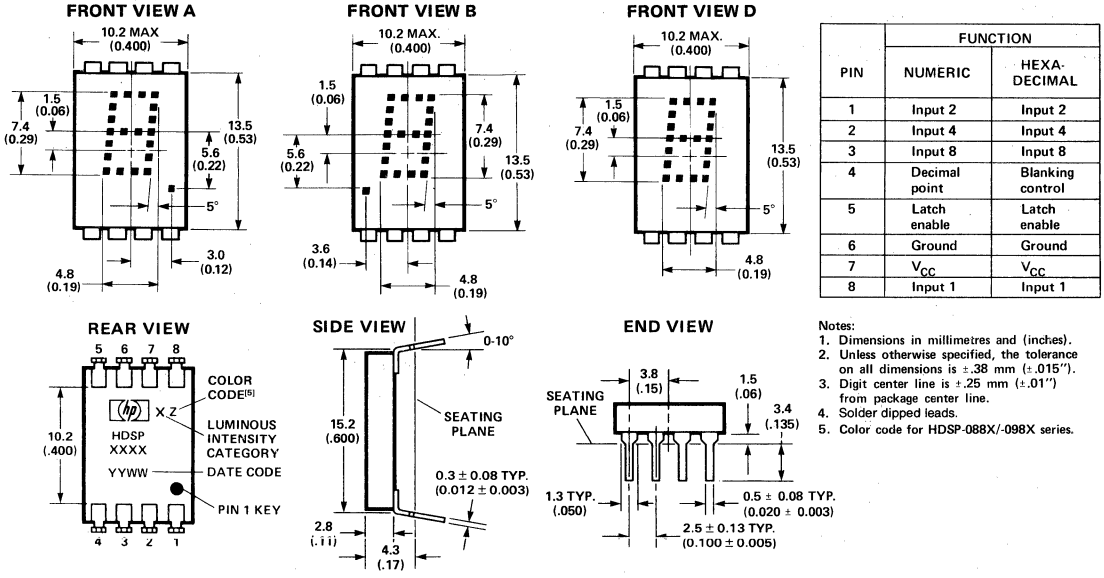
The over range device displays "±1" and right hand decimal point and is typically driven via external switching transistors.

Note:
1. The HDSP-098X high performance green displays are epoxy sealed and conform to MIL-D-87157 hermeticity requirements.

Devices

Part Number HDSP-	Color	Description	Front View
0781/0781TXV/0781TXVB	High-Efficiency Red Low Power	Numeric, Right Hand DP	A
0782/0782TXV/0782TXVB		Numeric, Left Hand DP	B
0783/0783TXV/0783TXVB		Over Range ±1	C
0784/0784TXV/0784TXVB		Hexadecimal	D
0791/0791TXV/0791TXVB	High-Efficiency Red High Brightness	Numeric, Right Hand DP	A
0792/0792TXV/0792TXVB		Numeric, Left Hand DP	B
0783/0783TXV/0783TXVB		Over Range ±1	C
0794/0794TXV/0794TXVB		Hexadecimal	D
0881/0881TXV/0881TXVB	Yellow	Numeric, Right Hand DP	A
0882/0882TXV/0882TXVB		Numeric, Left Hand DP	B
0883/0883TXV/0883TXVB		Over Range ±1	C
0884/0884TXV/0884TXVB		Hexadecimal	D
0981/0981TXV/0981TXVB	High Performance Green	Numeric, Right Hand DP	A
0982/0982TXV/0982TXVB		Numeric, Left Hand DP	B
0983/0983TXV/0983TXVB		Over Range ±1	C
0984/0984TXV/0984TXVB		Hexadecimal	D

Package Dimensions



PIN	FUNCTION	
	NUMERIC	HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

Notes:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38 mm (±.015").
3. Digit center line is ±.25 mm (±.01") from package center line.
4. Solder dipped leads.
5. Color code for HDSP-088X/-098X series.

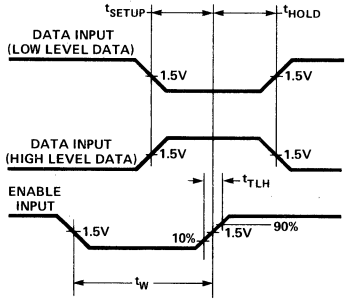


Figure 1. Timing Diagram

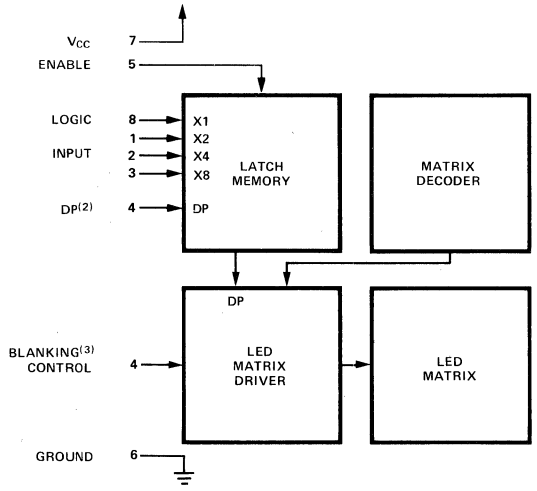


Figure 2. Logic Block Diagram

TRUTH TABLE					
BCD DATA[1]				NUMERIC	HEXA-DECIMAL
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	[	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	----	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]			ON		V_{DP} = L
			OFF		V_{DP} = H
ENABLE[1]			LOAD DATA		V_E = L
			LATCH DATA		V_E = H
BLANKING[3]			DISPLAY ON		V_B = L
			DISPLAY OFF		V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels have no effect upon display memory, displayed character, or DP.
2. The decimal point input, DP, pertains only to the numeric displays.
3. The blanking control input, B, pertains only to the hexadecimal displays. Blanking input has no effect upon display memory.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient HDSP-078X/-079X/-088X	T_S	-65	+125	°C
HDSP-098X		-55	+100	
Operating temperature, ambient[1]	T_A	-55	+100	°C
Supply voltage[2]	V_{CC}	-0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	-0.5	V_{CC}	V
Voltage applied to blanking input[2]	V_R	-0.5	V_{CC}	V
Maximum solder temperature at 1.59 mm (0.062 inch) below seating plane: t ≤ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage [2]	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1]	T_A	-55		+100	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			1.0	msec

Optical Characteristics at T_A = 25°C, V_{CC} = 5.0V

Device	Description	Symbol	Min.	Typ.	Max.	Unit
HDSP-078X Series	Luminous Intensity per LED (Digit Average)[3,4]	I_V	65	140		μcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength[5]	λ_d		626		nm
HDSP-079X Series	Luminous Intensity per LED (Digit Average)[3,4]	I_V	260	620		μcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength[5]	λ_d		626		nm
HDSP-088X Series	Luminous Intensity per LED (Digit Average)[3,4]	I_V	215	490		μcd
	Peak Wavelength	λ_{PEAK}		583		nm
	Dominant Wavelength[5,6]	λ_d		585		nm
HDSP-098X Series	Luminous Intensity per LED (Digit Average)[3,4]	I_V	298	1100		μcd
	Peak Wavelength	λ_{PEAK}		568		nm
	Dominant Wavelength	λ_d		574		nm

Notes:
1. The nominal thermal resistance of a display mounted in a socket that is soldered onto a printed circuit board is $R\theta_{JA}$ = 50° C/W/device. The device package thermal resistance is $R\theta_{J-PIN}$ = 15° C/W/device. The thermal resistance device pin-to-ambient through the PC board should not exceed 35° C/W/device for operation at T_A = +100° C.
2. Voltage values are with respect to device ground, pin 6.
3. These displays are categorized for luminous intensity with the intensity category designated by a letter code located on the back of the display package. Case temperature of the device immediately prior to the light measurement is equal to 25° C.

Electrical Characteristics; (T_A = -55° C to +100° C)

Description		Symbol	Test Conditions	Min.	Typ.[7]	Max.	Unit
Supply Current	HDSP-078X Series	I_{CC}	V_{CC} = 5.5 V Characters "5." or "B" displayed		78	105	mA
	HDSP-079X/-088X/ -098X Series				120	175	
Power Dissipation	HDSP-078X Series	P_T	V_{CC} = 5.5 V Characters "5." or "B" displayed		390	573	mW
	HDSP-079X/-088X/ -098X Series				690	963	
Logic, Enable and Blanking Low-Level Input Voltage		V_{IL}	V_{CC} = 4.5 V			0.8	V
Logic, Enable High-Level Input Voltage		V_{IH}		2.0			V
Blanking High Voltage; Display Blanked		V_{BH}		2.3			V
Logic and Enable Low-Level Input Current		I_{IL}	V_{CC} = 5.5 V			-1.6	mA
Blanking Low-Level Input Current		I_{BL}	V_{IL} = 0.4 V			-10	μA
Logic, Enable and Blanking High-Level Input Current		I_{IH}	V_{CC} = 5.5 V V_{IH} = 2.4 V			+40	μA
Weight					1.0		gm
Leak Rate						5×10^{-8}	cc/sec.

Notes:

4. The luminous intensity at a specific operating ambient temperature, $I_V(T_A)$ may be approximated from the following expotential equation: $I_V(T_A = I_V(25° C)\, e^{[k(T_A - 25° C)]}$.

Device	K
HDSP-078X Series HDSP-079X Series	-0.0131/° C
HDSP-088X Series	-0.0112/° C
HDSP-098X Series	-0.0104/° C

5. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
6. The HDSP-088X and HDSP-098X series devices are categorized as to dominant wavelength with the category disignated by a number on the back side of the display package.
7. All typical values at V_{CC} = 5.0 V and T_A = 25° C.

Operational Considerations

ELECTRICAL

These devices use a modified 4 x 7 dot matrix of light emitting diodes to display decimal/hexadecimal numeric information. The high efficiency red and yellow displays use GaAsP/GaP LEDs and the high performance green displays use GaP/GaP LEDs. The LEDs are driven by constant current drivers, BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at 6.7 MHz rate.

The decimal point input is active low true and this data is latched into the display memory in the same fashion as the BCD data. The decimal point LED is driven by the on-board IC.

The blanking control input on the hexadecimal displays blanks (turns off) the displayed information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 2.0 volts. When blanked, the display standby power is nominally 250 mW at T_A = 25° C.

The ESD susceptibility of the IC devices is Class A of MIL-STD-883 or Class 2 of DOD-STD-1686 and DOD-HDBK-263.

MECHANICAL

These displays are hermetically sealed for use in environments that require a high reliability device. These displays are designed and tested to meet a helium leak rate of 5 x 10^{-8} cc/sec.

These displays may be mounted by soldering directly to a printed circuit board or insertion into a socket. The lead-to-lead pin spacing is 2.54 mm (0.100 inch) and the lead row spacing is 15.24 mm (0.600 inch). These displays may be end stacked with 2.54 mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100° C, it is important to maintain a base-to-ambient thermal resistance of less than 35° C watt/device as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

PRECONDITIONING

These displays are 100% preconditioned by 24 hour storage at 125°C, at 100°C for the HDSP-098X Series.

CONTRAST ENHANCEMENT

These display devices are designed to provide an optimum ON/OFF contrast when placed behind an appropriate contrast enhancement filter. The following filters are suggested:

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-088X Yellow	Panelgraphic Yellow 27 Chequers Amber 107	Polaroid HNCP 37 3M Light Control Film Panelgraphic Gray 10	Polaroid Gray HNCP10 HOYA Yellowish-Orange HLF-608-3Y Marks Gray MCP-0301-8-10
HDSP-078X/-079X HER	Panelgraphic Ruby Red 60 Chequers Red 112	Chequers Grey 105	Polaroid Gray HNCP10 HOYA Reddish-Orange HLF-608-5R Marks Gray MCP-0301-8-10 Marks Reddish-Orange MCP-0201-2-22
HDSP-098X HP Green	Panelgraphic Green 48 Chequers Green 107		Polaroid Gray HNCP10 HOYA Yellow-Green HLF-608-1G Marks Yellow-Green MCP-0101-5-12

Over Range Display

The over range devices display "±1" and decimal point. The character height and package configuration are the same as the numeric and hexadecimal devices. Character selection is obtained via external switching transistors and current limiting resistors.

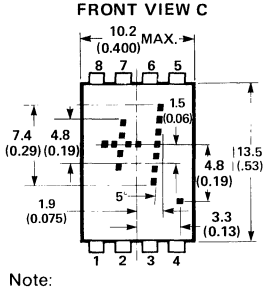
Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	-65	+125	°C
Operating Temperature Ambient	T_A	-55	+100	°C
Forward Current, Each LED	I_F		10	mA
Reverse Voltage, Each LED	V_R		5	V

Character	Pin			
	1	2,3	4	8
+	1	X	X	1
—	0	X	X	1
1	X	1	X	X
Decimal Point	X	X	1	X
Blank	0	0	0	0

Notes:
0: Line switching transistor in Figure 7 cutoff.
1: Line switching transistor in Figure 7 saturated.
X: 'don't care'

Package Dimensions



Pin	Function
1	Plus
2	Numeral One
3	Numeral One
4	DP.
5	Open
6	Open
7	V_{CC}
8	Minus/Plus

Note:
1. Dimensions in millimetres and (inches).

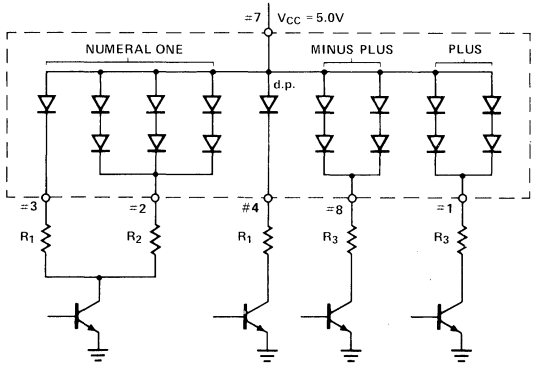


Figure 3. Typical Driving Circuit

Luminous Intensity Per LED

(Digit Average) at $T_A = 25°C$

Device	Test Conditions	Min.	Typ.	Units
HDSP-0783	I_F = 2.8 mA	65	140	μcd
	I_F = 8 mA		620	μcd
HDSP-0883	I_F = 8 mA	215	490	μcd
HDSP-0983	I_F = 8 mA	298	1100	μcd

Recommended Operating Conditions $V_{CC} = 5.0V$

Device	Forward Current Per LED, mA	Resistor Value		
		R_1	R_2	R_3
HDSP-0783 Low Power	2.8	1300	200	300
HDSP-0783 High Brightness	8	360	47	68
HDSP-0883	8	360	36	56
HDSP-0983	8	360	30	43

Electrical Characteristics ($T_A = -55°C$ to $+100°C$)

Device	Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
HDSP-0783	Power Dissipation (all LEDs Illuminated)	P_T	I_F = 2.8 mA		72		mW
			I_F = 8 mA		224	282	
	Forward Voltage per LED	V_F	I_F = 2.8 mA		1.6		V
			I_F = 8 mA		1.75	2.2	
HDSP-0883	Power Dissipation (all LEDs Illuminated)	P_T	I_F = 8 mA		237	282	mW
	Forward Voltage per LED	V_F			1.90	2.2	V
HDSP-0983	Power Dissipation (all LEDs illuminated)	P_T	I_F = 8 mA		243	282	mW
	Forward Voltage per LED	V_F			1.85	2.2	V

High Reliability Testing

Two standard reliability testing programs are available. The TXVB program is in conformance with Quality Level A Test Tables of MIL-D-87157 for hermetically sealed displays with 100% screening tests. A TXVB product is tested to Tables I, II, IIIa, and IVa, A second program is an HP modification to the full conformance program and offers the 100% screening portion of Level A, Table I, and Group A, Table II.

PART MARKING SYSTEM

Standard Product	With Table I and II	With Tables I, II, IIIa and IVa
HDSP-078X	HDSP-078XTXV	HDSP-078XTXVB
HDSP-079X	HDSP-079XTXV	HDSP-079XTXVB
HDSP-088X	HDSP-088XTXV	HDSP-088XTXVB
HDSP-098X	HDSP-098XTXV	HDSP-098XTXVB

100% Screening **TABLE I. QUALITY LEVEL A OF MIL-D-87157**

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	2072	Interpreted by HP Procedure 5956-7572-52
2. High Temperature Storage	1032	T_A = 125°C, Time = 24 hours[4]
3. Temperature Cycling	1051	Condition B, 10 Cycles, 15 Min. Dwell
4. Constant Acceleration	2006	10,000 G at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K[5]
7. Interim Electrical/Optical Tests[2]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} T_A = 25°C
8. Burn-In[1, 3]	1015	Condition B at V_{CC} = 5V and cycle through logic at 1 character per second. T_A = 100°C, t = 160 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	ΔI_V = -20%, ΔI_{CC} = ± 10 mA, ΔI_{IH} = ±10μA and ΔI_{EH} = ±13 μA
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics.
3. Burn-in for the over range display shall use Condition B at a nominal I_F = 8 mA per LED, with all LEDs illuminated for T = 160 hours minimum.
4. T_A = +100°C for HDSP-098X Series.
5. Fluid temperature = +100°C for HDSP-098X Series.

TABLE II
GROUP A ELECTRICAL TESTS — MIL-D-87157

Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} and visual function, T_A = 25°C	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. T_A = +100°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. T_A = -55°C	7
Subgroup 4, 5, and 6 not applicable		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

Notes:
1. Limits and conditions are per the electrical/optical characteristics.

TABLE IIIa
GROUP B, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Design Verification[1]	2075[7]		1 Device/ 0 Failures
Subgroup 2[2,3] Solderability	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	Condition B1, 15 min. Dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K[9]	
Electrical/Optical Endpoints[5]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual function. T_A = 25°C	
Subgroup 4 Operating Life Test (340 hrs.)[6]	1027	T_A = +100°C at V_{CC} = 5.0V and cycling through logic at 1 character per second.	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3.	
Subgroup 5 Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +125°C[7,8]	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	

Notes:
1. Visual inspection performed through the display window.
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend, one cycle.
5. Limits and conditions are per the electrical/optical characteristics.
6. Burn-in for the over range display shall use Condition B at a nominal $I_F \pm 8$ mA with '+' illuminated for t = 160 hours.
7. Equivalent to MIL-STD-883, Method 2014.
8. T_A = +100°C for HDSP-098X Series.
9. Fluid temperature = +100°C for HDSP-098X Series.

TABLE IVa
GROUP C, CLASS A AND B OF MIL-D-87157

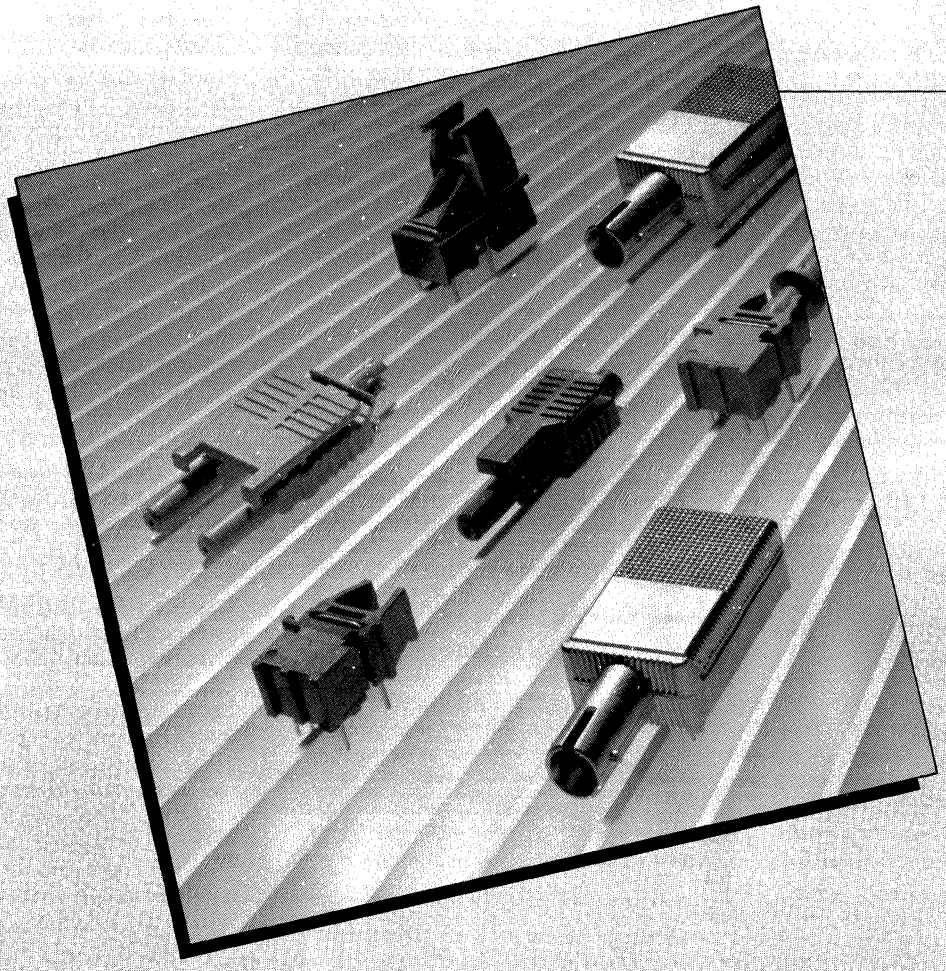
Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7,9]			LTPD = 15
Lead Integrity	2004	Condition B2	
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K[10]	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual Function, $T_A = 25°C$	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			$\lambda = 10$
Operating Life Test[6]	1026	$T_A = +100°C$	
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C Life Test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.
9. Initial conditioning is a 15° inward bend, 3 cycles.
10. Fluid temperature = +100°C for HDSP-098X Series.

HEWLETT PACKARD

Fiber Optics

- Fiber Optic Transmitter/Receiver Components
- Cables, Connectors, and Accessories



Fiber Optics

HP's Commitment

Hewlett-Packard has been committed to Fiber Optics since the introduction of our first link in 1978. Years of technological experience with LED emitters, detectors, integrated circuits, precision optical packaging, and optical fiber qualify HP to provide practical solutions for your application needs.

HP's unique combination of technologies and high volume manufacturing processes provide you with high quality transmitter and receiver components to meet a wide variety of computer, local area network, telecommunication, and industrial communication needs.

Three major families of fiber optic components offer a wide range of application solutions. Each family is designed to match HP's technology to your application requirements resulting in minimum cost and maximum reliability. The design and specification of each of these families allow easy design-in and provide guaranteed performance.

Hewlett-Packard's method of specification assures guaranteed link performance and easy design-in. The transmitter optical power and receiver sensitivity are specified at the end of a length of test cable. These specifications take into account variations over temperature and connector tolerances. All families of components incorporate the fiber optic connector receptacle in the transmitter and receiver packages. Factory alignment of the emitter/detector inside the package minimizes the variation of coupled optical power, resulting in smaller dynamic range requirements for the receiver. The guaranteed distance and data rates for various transmitter/receiver pairs are shown in the following selection guide.

Hewlett-Packard offers a choice of fiber optic cable, either glass fiber or plastic, simplex or duplex, factory connectored or bulk. Connector attachment has been designed for your production line economy.

Versatile Link Components

Low cost and ease of use make this family of link components well suited for applications connecting computers to terminals, printers, plotters, test equipment, medical equipment, and industrial control equipment. These links utilize 665 nm technology and 1 mm diameter plastic fiber cable. Assembling the plastic snap-in connectors onto the cable is extremely easy. The HFBR-0501 evaluation kit contains a complete working link including transmitter, receiver, five metres of connectored cable, extra connectors, polishing kit, and technical literature.

Low Cost Miniature Link Components

This family offers a wide range of price/performance choice for computers, central office switch, PBX, local area network, and industrial-control applications. These components utilize 820 nm technology and glass or plastic clad silica fiber cable. The unique design of the lensed optical coupling system makes this family of components extremely reliable. The dual-in-line package

requires no mounting hardware. The package is designed for auto insertion and wave soldering. The components are available for use with industry standard ST* or SMA connectors. Specifications are provided for four fiber sizes: 62.5/125 µm, 50/125 µm, 100/140 µm, and 200 µm Plastic Clad Silica (PCS) cable. Evaluation kits are available for both ST and SMA connectors. A transmitter, receiver, connectored cable, and technical literature are contained in the evaluation kits.

1300 nm Module Components

Hewlett-Packard began the development of 1300 nm materials and device technology in the early 1980s based on the need for greater performance and reliability in the local area fiber optic component market. After many years of development, Hewlett-Packard is proud to introduce its new family of 1300 nm transmitters and receivers. These components are available for use with the industry standard ST* connector. The precision stainless steel bore assures that the ST* connector ferrule tip will be optimally aligned with the optics of the module.

Hewlett-Packard's long tradition of quality and reliability is insured by the vertical integration of this new product family. The 1300 nm LED, PIN, and three custom bipolar integrated circuits (IC) used in these products have been developed and are manufactured by HP. Hewlett-Packard's manufacturing and test facilities provide consistent performance and high volume capability. A driver IC allows the 1300 nm LED to translate ECL signals into an optical signal. On the other end of the link, the PIN receiver converts the optical pulses into electrical signals. These signals are processed in Hewlett-Packard's module through preamplifier and quantizer ICs before being transferred as an ECL signal to the external circuitry.

New General Purpose High Speed Transmitter and Receiver Pair

HP now offers two varieties of high speed, general purpose 1300 nm components. They are specified for applications between 10-160 MBd (HFBR-1160/2100) or 10-200 MBd (HFBR-1160/2100). Alternate sources of supply are available to those designers who require multiple sources.

New FDDI Transmitter and Receiver Pair

Hewlett-Packard's first Fiber Distributed Data Interface (FDDI) compatible transmitter and receiver pair, the HFBR-1125/2125 parts are fully characterized and guaranteed to meet or exceed the optoelectronic requirements of the FDDI Local Area Network Standard. Drawing on Hewlett-Packard's experience in the test and measurement field, the outgoing production tests for the module guarantee interoperability with other FDDI compatible components.

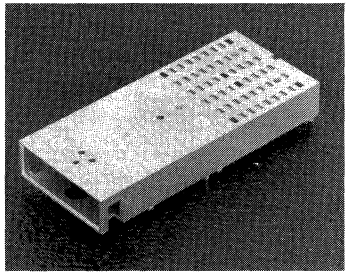
The modules use a shifted ECL interface and are directly compatible with the FDDI PHY integrated circuits available today. Designed for FDDI stations with minimum board space, the component pair has a sufficient power budget to allow for optical bypass switches.

1300 nm Products under Development

FDDI Transceiver

The second generation of FDDI optical components from Hewlett-Packard is packaged in a transceiver module with a PMD-compatible MIC receptacle. The module is directly compatible with FDDI PHY integrated circuits. It uses the same LED, PIN, and integrated circuits as the individual transmitter and receiver modules.

The Hewlett-Packard transceiver is packaged in a dual-in-line package with two rows of 11 pins. Several suppliers have commited to supply FDDI transceivers in this package assuring multiple sources of supply. The HP transceiver has been Beta Site tested during mid-1990. Product release is targeted for the fourth quarter 1990. Contact your local field sales engineer for more information.



*ST (R) is a registered trademark of AT&T for Lightguide Cable Connectors.

HP Fiber Optic Performance Characteristics

The charts on this page illustrate the performance ranges of Hewlett-Packard's fiber optic components. Both charts are coded by family. To determine which family is appropriate for your design, use the distance/data rate chart (Figure 1). The performance of each family incorporates the entire area below each boundary. Specific component choices and their associated optical-power budget are indicated in Figure 2.

The optical-power budget is determined by subtracting the receiver sensitivity (dBm) from the transmitter optical output power (dBm). The distance specification can be calculated simply by dividing the optical-power budget (dBm) by the cable attenuation (dB/km).

The newer transmitter/receiver product families provide the designer with significantly improved price/performance benefits over older products. These newer product families have been specifically designed for easy use in high volume manufacturing operations.

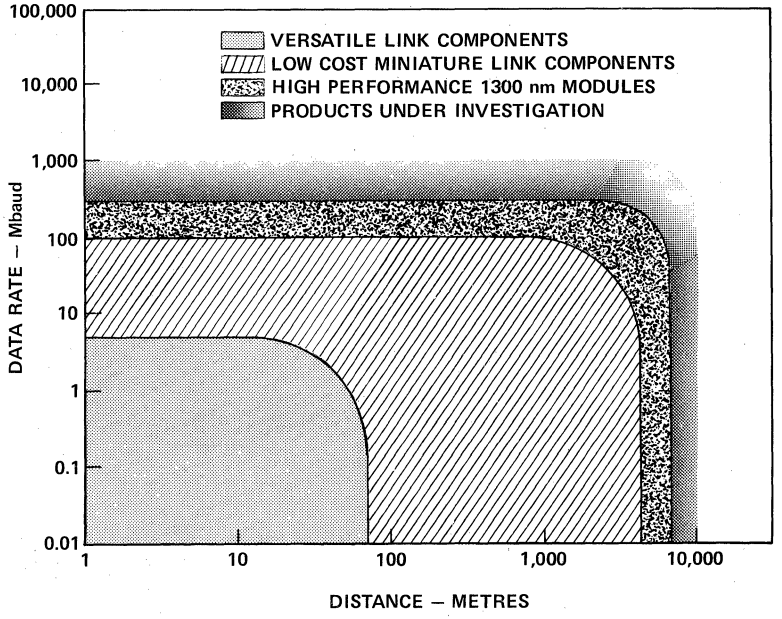


Figure 1

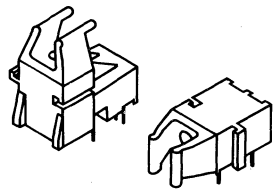
Figure 2

NOTES:
1. Optical power budget calculations are at 25°C.
2. For Link performance with other fiber sizes contact your local HP sales office.
3. All transmitters are LEDs except for 1300 nm modules which include a driver IC.

					VERSATILE LINK				LOW COST MINIATURE				FUTURE 1300 nm MODULES	
					TRANSMITTERS[3]									
					λ = 665 nm HFBR-1521/1531	λ = 665 nm HFBR-1522/1532	λ = 665 nm HFBR-1524/1534	λ = 665 nm HFBR-1523/1533	λ = 820 nm HFBR-1402/1412	λ = 820 nm HFBR-1402/1412	λ = 820 nm HFBR-1404/1414	λ = 820 nm HFBR-1404/1414	λ = 1300 nm HFB-1125	λ = 1300 nm HFBR-1100
					COUPLED OPTICAL POWER (dBm)									
					-11.1 @ 60 mA	-8.2 @ 60 mA	-10.3 @ 60 mA	-8.2 @ 60 mA	-6.5 @ 60 mA	-12.0 @ 60 mA	-12.0 @ 60 mA	-16.5 @ 60 mA	-16.0	-16.0
					FIBER SIZE (μm) (ATTENUATION)									
					1000 (0.25 dB/m)	1000 (0.25 dB/m)	1000 (0.25 dB/m)	1000 (0.25 dB/m)	200 PCS (5.3 dB/km)	100/140 (3.3 dB/km)	62.5/125 (2.8 dB/km)	50/125 (2.8 dB/km)	62.5/125 (2.8 dB/km)	62.5/125 (2.8 dB/km)
VERSATILE LINK	RECEIVERS	HFBR-2521/2531	FUNCTION	Logic IC	SENSITIVITY (dBm) -21.6	5 MBd 40 m								
		HFBR-2522/2532		Logic IC	-24		1 MBd 65 m							
		HFBR-2524/2534		Logic IC	-20			1 MBd 35 m						
		HFBR-2523/2533		Logic IC	-39				40 KBd 125 m					
LOW COST MINIATURE		HFBR-2402/2412		Logic IC	-25.4					5 MBd 3.5 Km	5 MBd 4.1 Km	5 MBd 4.7 Km	5 MBd 3.2 Km	
		HFBR-2404/2414		PIN/ Preamp	-36					5 MBd 5.6 Km	5 MBd 7.3 Km	5 MBd 8.6 Km	5 MBd 7.0 Km	
		HFBR-2404/2414		PIN/ Preamp	-33					30 MBd 600 m*	30 MBd 3.0 Km*	30 MBd 4.0 Km*	30 MBd 4.0 Km*	
		HFBR-2406/2416		PIN/ Preamp	-35.6					30 MBd 650 m*	30 MBd 3.3 Km*	30 MBd 4.5 Km*	30 MBd 4.5 Km*	
		HFBR-2406/2416		PIN/ Preamp	-32					100 MBd 130 m*	100 MBd 750 m*	100 MBd 1.0 Km*	100 MBd 1.0 Km*	
FUTURE 1300 nm MODULES		HFBR-Module 2125		Logic IC									125 MBd 2.0 Km	
		HFBR-Module 2100		Logic IC										200 MBd 2.0 Km

Future 1300 nm modules are discussed on page 8-3.
*Distance is limited by a combination of fiber bandwidth and transmitter optical rise/fall time and LED spectral width.

Versatile Link Family



Features: Dual-in-line package, horizontal and vertical PCB mounting, plastic snap-in connectors, specified for 1 mm dia. plastic fiber. TTL/CMOS compatible output, auto insertable, wave solderable.

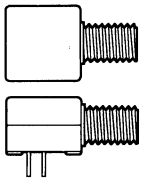
Product/Part Numbers			Description		Page No.
Evaluation Kit HFBR-0501			HFBR1524 Transmitter. HFBR-2524 Receiver. 5 metre connectored cable, connectors, bulkhead feedthrough adapter, polishing kit, literature.		5-11
Transmitter/Receiver Pairs					
	Horizontal	**Vertical**	**Distance***	**Data Rate**	
5 MBd High Performance Link	HFBR-1521/2521	HFBR-1531/2531	40 m	5 MBd	
1 MBd High Performance Link	HFBR-1522/2522	HFBR-1532/2532	65 m	1 MBd	
1 MBd Standard Performance Link	HFBR-1524/2524	HFBR-1534/2534	35 m	1 MBd	
40 KBd Extended Distance Link	HFBR-1523/2523	HFBR-1533/2533	125 m	40 KBd	
Low Current Link	HFBR-1523/2523	HFBR-1533/2523	40 m	40 KBd	
Photo Interrupter Link	HFBR-1523/2523	HFBR-1533/2523	N.A.	20 KHz	
	HFBR-1522/2522	HFBR-1532/2532	N.A.	500 KHz	
Plastic Fiber Cable Available in 1 meter increments (yyy m)					
Attenuation	**Simplex**	**Duplex**			
Standard	HFBR-PUSyyy	HFBR-PUDyyy	Unconnectored cable		
Standard	HFBR-PNSyyy	HFBR-PNDyyy	Simplex connectored cable		
Standard	HFBR-PLSyyy	HFBR-PLDyyy	Latching simplex connectored cable		
Standard	N.A.	HFBR-PMDyyy	Duplex connectored cable		
Standard	N.A.	HFBR-PLDyyy	Latching duplex connectored cable		
Improved	HFBR-QUSyyy	N.A.	Unconnectored cable		
Improved	HFBR-QNSyyy	N.A.	Simplex connectored cable		
Improved	HFBR-QLS-yyy	N.A.	Latching simplex connectored cable		
Connectors					
	Simplex Standard	HFBR-4501	Gray connector/crimp ring		
		HFBR-4511	Blue connector/crimp ring		
	Simplex Latching	HFBR-4503	Gray connector/crimp ring		
		HFBR-4513	Blue connector/crimp ring		
	Duplex Standard	HFBR-4506	Parchment connector/crimp ring		
	Duplex Latching	HFBR-4516	Parchment connector/crimp ring		

*Link performance at 25°C, improved attenuation cable.

Versatile Link Family (continued)

Polishing Kit HFBR-4593	Plastic polishing fixture (used for all connectores), abrasive paper, lapping film.	5-11
Bulkhead Feedthrough/In-line splice HFBR-4505 HFBR-4515	Gray bulkhead feedthrough adapter Blue bulkhead feedthrough adapter	

Low Cost Miniature Link Family



Features: Dual-in-line package, interfaces directly with ST or SMA connectors, specified for use with 50/125 µm, 62.5 µm, 100/140 µm and 200 µm Plastic Coated Silica (PCS) fiber. Auto insertable, wave solderable, no mounting hardware required.

Product/Part Numbers	Description	Page No.
Evaluation Kits		
HFBR-0410 (ST)	HFBR-1412 transmitter, HFBR-2412 receiver, 3 meter connectored 62.5/125 µm cable, literature.	5-35
HFBR-0400 (SMA)	HFBR-1402 transmitter, HFBR-2404 receiver, 2 meter connectored 1,000 µm (plastic) cable, literature.	
Transmitters/Receivers		
HFBR-14X2 Standard Transmitter	Optimized for large size fiber such as 100/140 µm and 200 µm PCS	5-46
HFBR-14X4 High Power Transmitter	Optimized for small size fiber such as 50/125 µm or 62.5/125 µm	
HFBR-24X2 5 MBd Receiver	TTL/CMOS compatible receiver with -25.4 dBm sensitivity	5-51
HFBR-24X4 25 MHz Receiver	PIN-preamp receiver for signal rates up to 35 MBd	5-54
HFBR-24X6 125 MHz Receiver	PIN-preamp receiver for signal rates up to 150 MBd	5-58

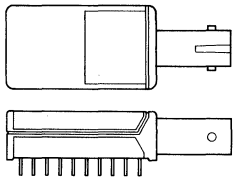
Transmitter/Receiver Pairs	Optical Power Budget*	Data Rate	
HFBR-14X2/24X2	20.5 dB (200 µm fiber)	5 MBd	5-46/51
	15 dB (100/140 µm fiber)	5 MBd	
HFBR-14X4/24X2	15 dB (62.5/125 µm fiber)	5 MBd	
	10.5 dB (50/125 µm fiber)	5 MBd	
HFBR-14X2/24X4	18 dB (100/140 µm fiber)	5 MBd	5-46/55
	13.5 dB (100/140 µm fiber)	30 MBd-	
HFBR-14X4/24X4	18 dB (62.5/125 µm fiber)	5 MBd	
	13.5 dB (62.5/125 µm fiber)	30 MBd	
HFBR-14X2/24X6	21 dB (100/140 µm fiber)	30 MBd	5-46/58
	19 dB (100/140 µm fiber)	150 MBd	
HFBR-14X4/24X6	21 dB (62.5/125 µm fiber)	30 MBd	
	19 dB (62.5/125 µm fiber)	150 MBd	

*Link performance at 25 C.

Low Cost Miniature Link Family (continued)

Mechanical Styles	Description	Page
HFBR-XX0X	SMA housed product	5-35/63/65
HFBR-XX3X	SMA port product, bent leads	
HFBR-XX5X	SMA port product, straight leads	
HFBR-XX0XC	HFBR-XX0X with Conductive Port Option (RX only)	
HFBR-XX3XC	HFBR-XX3X with Conductive Port Option (RX only)	
HFBR-XX5XC	HFBR-XX5X with Conductive Port Option (RX only)	
HFBR-XX1X	ST housed product (not recommended for new designs)	
HFBR-XX4X	ST port product, bent leads (not recommended for new designs)	
HFBR-XX6X	ST port product, straight leads (not recommended for new designs)	
HFBR-XX1XT	HFBR-XX1X with Threaded ST Option (recommended for new designs)	
HFBR-XX4XT	HFBR-XX4X with Threaded ST Option (recommended for new designs)	
HFBR-X6XT	HFBR-XX6X with Threaded ST Option (recommended for new designs)	
HFBR-XX1XTC	HFBR-XX1XT with Conductive Port Option (RX only)	
HFBR-XX4XTC	HFBR-XX4XT with Conductive Port Option (RX only)	
HFBR-XX6XTC	HFBR-XX6XT with Conductive Port Option (RX only)	

1300 nm Transmitter/Receiver Module Link Family

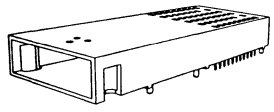


Features: Dual-in-line package, interfaces directly with ST* connectors, specified for use with 62.5/125 μm and 50/125 μm fiber. Single +5 V power supply and shifted ECL logic interface.

Product/Part Numbers		Description		Page No.
Transmitter/Receiver Pairs		**Distance**	**Data Rate**	
200 MBd link	**HFBR-1100/2100**	2 km	200 MBd	5-116
160 MBd link	**HFBR-1160/2100**	2 km	160 MBd	
FDDI link	**HFBR-1125/2125**	2 km	125 MBd	5-125

*ST(R) is a registered trademark of AT&T for Lightware Cable Connectors.

1300 nm Transceiver Module Link Family



Features: Dual-in-line package, interfaces directly with FDDI MIC connector, specified for use with 62.5/125 μm and 50/125 μm fiber. Single +5 V power supply and shifted ECL logic interface.

Product/Part Numbers		Description		Page No.
Transmitter/Receiver Pairs		**Distance**	**Data Rate**	
FDDI link	HFBR-5125	2 km	125 MBd	Contact Field Sales Office

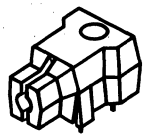
*ST(R) is a registered trademark of AT&T for Lightware Cable Connectors.

ST and SMA Connectored Cable

Part Number	Description								Page No.
	Fiber Size			Connector Style			Cable Type		
	100/140/.30	62.5/125/.275	50/125/.18	SMA	ST	Uncon-nectored	Single Channel	Dual Channel	
HFBR-AWSyyy	X			X			X		5-67
HFBR-AWDyyy	X			X				X	
HFBR-AXSyyy	X				X		X		
HFBR-AXDyyy	X				X			X	
HFBR-AUSyyy	X					X	X		
HFBR-AUDyyy	X					X		X	
HFBR-BWSyyy		X		X			X		
HFBR-BWDyyy		X		X				X	
HFBR-BXSyyy		X			X		X		
HFBR-BXDyyy		X			X			X	
HFBR-BUSyyy		X				X	X		
HFBR-BUDyyy		X				X		X	
HFBR-CXSyyy*			X		X		X		

*Note: All cable assemblies except for HFBR-CXSyyy are available in 1 metre increments from 1 metre to 999 metres and 100 metre increments from 1 km to 2 km. HFBR-CXSyyy is available in 1 and 10 metre lengths only. Eg. yyy = 050 designates 50 metres and yyy = 1K5 designates 1.5 km.

Snap-In Link Family



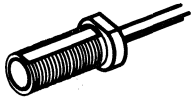
Features: Operate with 1 mm dia. plastic fiber, plastic snap-in connector compatible (standard simplex only). TTL compatible output.

FOR NEW DESIGNS: Refer to the Versatile Link Family on page 5-6 to achieve the best price/performance value.

Product/Part Numbers		Description		Page No.
Transmitter/Receiver Pairs		**Distance***	**Data Rate***	5-72
5 MBd link	HFBR-1510/2501	40 metre	5 MBd	
1 MBd Link	HFBR-1502/-2502	65 metre	1 MBd	
Extended Distance Link	HFBR-1512/-2503	125 metre	40 kBd	
Low Current Link	HFBR-1512/-2503	40 metre	40 kBd	
Photo Interrupter Link	HFBR-1512/-2503	N/A	20 kHz	
	HFBR-1502/-2502	N/A	500 kHz	

*Link performance at 25°C, improved attenuation cable.

Miniature Link Family



Features: Interfaces directly with SMA style connectors, specified for use with 100/140 µm fiber. Precision metal connector interface.

FOR NEW DESIGNS: Refer to the Low Cost Miniature Link Family on page 5-7 to achieve the best price/performance value.

Product/Part Numbers	Description		Page No.
Transmitter/Receiver Pairs	**Distance***	**Data Rate***	5-90/98/ 102/110
HFBR-1202/-2202	800 metre	5 MBd	
HFBR-1202/-2204	1200 metre	40 MBd	
HFBR-1204/-2202	1800 metre	5 MBd	
HFBR-1204/-2204	2100 metre	40 MBd	
HFBR-1204/-2208	500 metre (typical)	125 MBd (typical)	
Mounting Hardware			5-90
HFBR-4202	PCB mounting bracket, EMI shield, misc. hardware for HFBR-1202/-1204/-2202/-2204/-2208.		

*Link performance at 25°C.

HEWLETT PACKARD

VERSATILE LINK
The Versatile Fiber Optic Connection

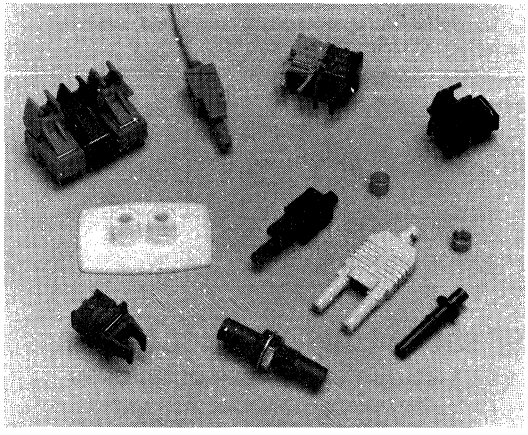
HFBR-0501 SERIES

Features

- **LOW COST FIBER OPTIC COMPONENTS**
- **GUARANTEED LINK PERFORMANCE OVER TEMPERATURE**
  High Speed Links: dc to 5 MBd
  Extended Distance Links: up to 82 m
  Low Current Link: 6 mA Peak Supply Current
  Low Cost Standard Link: dc to 1 MBd
  Photo Interrupter Link
- **COMPACT, LOW PROFILE PACKAGES**
  Horizontal and Vertical Mounting
  "N-plex" Stackable
  Flame Retardant
- **EASY TO USE RECEIVERS**
  TTL, CMOS Compatible Output Level
  High Noise Immunity
- **EASY CONNECTORING**
  Simplex, Duplex and Latching Connectors
  Flame Retardant Material
- **LOW LOSS PLASTIC CABLE**
  Selected Super Low Loss Simplex
  Simplex and Zip Cord Style Duplex
  Flame Retardant
- **NO OPTICAL DESIGN REQUIRED**
- **AUTO-INSERTABLE AND WAVE SOLDERABLE**
- **DEMONSTRATED RELIABILITY @ 40°C EXCEEDS 2 MILLION HOURS MTBF**

Description

The Versatile Link series is a complete family of fiber optic link components for applications requiring a low cost solution. The HFBR-0501 series includes transmitters, receivers, connectors and cable specified for easy design. This series of components is ideal for solving problems with voltage isolation/insulation, EMI/RFI immunity or data security. The Link design is simplified by the logic compatible receivers and complete specifications for each component. No optical design is necessary. The key optical and electrical parameters of links configured with the HFBR-0501 family are fully guaranteed from 0° to 70° C. A wide variety of package configurations and connectors provide the designer with numerous mechanical solutions to meet application requirements. The transmitter and receiver components have been designed for use in high volume/low cost assembly processes such as auto-insertion and wave sclderlng.



Versatile Link Applications

- **Reduction of lightning/voltage transient susceptability**
- **Motor controller triggering**
- **Data communications and Local Area Networks**
- **Electromagnetic Compatibility (EMC) for regulated systems: FCC, VDE, CSA, etc.**
- **Tempest—secure data processing equipment**
- **Isolation in test and measurement instruments**
- **Error free signalling for industrial and manufacturing equipment**
- **Automotive communications and control networks**
- **Power supply control**
- **Communication and isolation in medical instruments**
- **Noise immune communication in audio and video equipment**
- **Remote photo interrupter for office and industrial equipment**
- **Robotics communication**
- **PC to peripheral links**

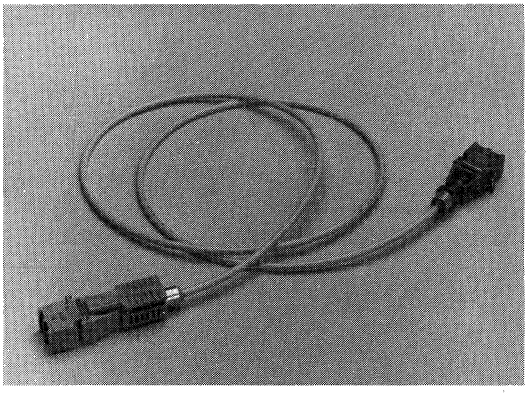
Link Selection Guide

Specific Product Numbers and Component Selection Guide on page 23.

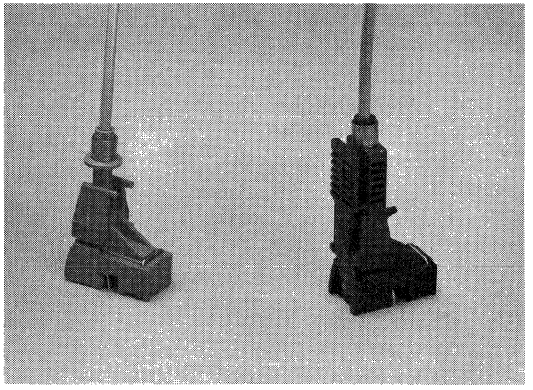
Versatile Link		Guaranteed Minimum Link Length Metres				Typical Link Length Metres		Page
		0°C - 70°C		25°C		25°C		
		Standard Cable	Improved Cable	Standard Cable	Improved Cable	Standard Cable	Improved Cable	
High Performance	5 MBd	12	17	17	24	35	40	5-14
High Performance	1 MBd	24	34	30	41	50	65	5-14
Low Current Link	40 kBd	8	11	—	—	30	35	5-14
Extended Distance Link	40 kBd	60	82	65	90	100	125	5-14
Standard	1 MBd	5	7	11	15	30	40	5-14
Photo Interrupter	500 kHz	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	5-20
Evaluation Kit	1 MBd (Standard)	Contents: Horizontal transmitter, horizontal receiver packages; 5 metres of simplex cable with simplex and simplex latching connectors installed; individual connectors: simplex, duplex, simplex latching, bulkhead adapter; polishing tool, abrasive paper, literature.						5-34

Versatile Link Product Family

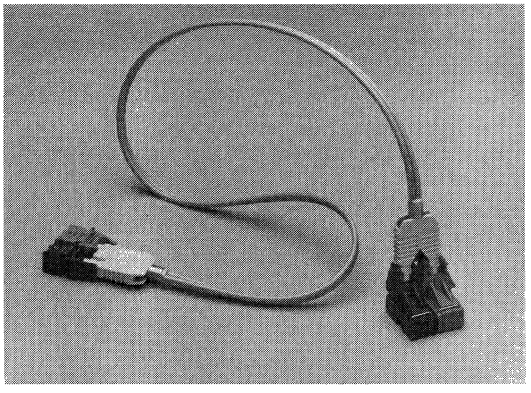
5 MBd, 1 MBd and 40 kBd FIBER OPTIC LINKS



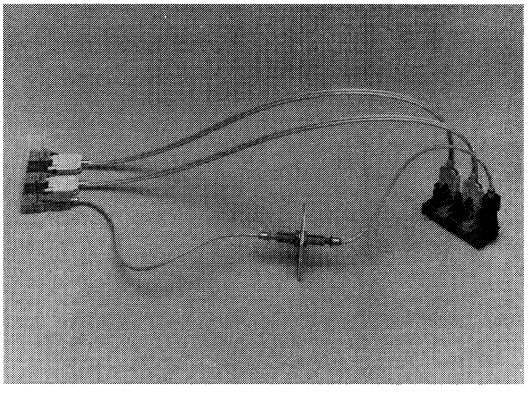
Simplex Link — Horizontal Packages



Simplex Link — Vertical Packages



Duplex Link — Combination of Horizontal & Vertical Packages



N-Plex Link — Combinations

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- Low Current Extended Distance 40 kBd Link 5-14
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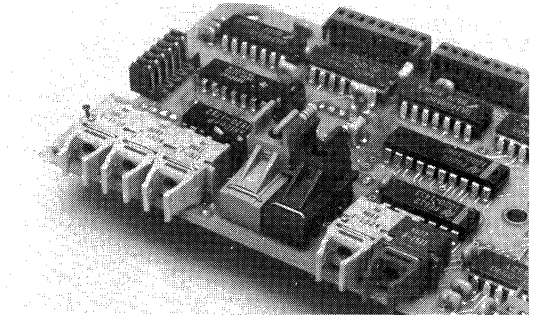
Versatile Link Product Description

Mechanical: The compact Versatile Link package is made of a flame retardant material (UL V-0) in a standard, eight pin dual-in-line package (DIP) with 7.6 millimetre (0.3 inch) pin spacing. Vertical and horizontal mountable parts are available. These low profile Versatile Link packages are stackable and are enclosed to provide a dust resistant seal. Snap action simplex, simplex latching, duplex, and duplex latching connectors are offered with simplex or duplex cables.

Electrical: Transmitters incorporate a 660 nanometre light emitting diode (LED). Receivers include a monolithic dc coupled, digital IC receiver with open collector Schottky output transistor. An internal pullup resistor is available for use in the HFBR-25X1/2/4 receivers. Transmitter and receiver are compatible with standard TTL circuitry. A shield has been integrated into the receiver IC to provide additional, localized noise immunity.

Optical: Internal optics have been optimized for use with 1 mm diameter plastic optical fiber. Versatile Link specifications incorporate all component interface losses. Therefore, the need of optical calculations for common link applications is eliminated.

Optical power budget is graphically displayed to facilitate electrical design for customized links.



Designing with Versatile Link

When designing with Versatile Link, the following topics should be considered:

Distance and Data Rate

Distances and data rates guaranteed with Versatile Link depend upon the Versatile Link transmitter/receiver pair chosen. See the Versatile Link guide (page 5-14).

Typically, a data rate requirement is first specified. This determines the choice of the 5 MBd, 1 MBd or 40 kBd Versatile Link components. Distances guaranteed with Versatile Link then depend upon choice of cable, specific drive condition and circuit configuration. Extended distance operation is possible with pulsed operation of the LED (see Figure 2a, 2b, 2c, 2d, 2e and 2f dotted lines.)

Drive circuits are described on page 5-17. Cable is discussed on page 5-29. Pulsed operation of the LED at larger current will result in increased pulse width distortion of the receiver output signal.

Versatile Link can also be used as a photo interrupter at frequencies up to 500 KHz. This is described on page 10.

Package Orientation

As shown in the photograph, Versatile Link is available in vertical and horizontal packages. Performance and pinouts for the two packages are identical. To provide additional attachment support for the Vertical Versatile Link housing, the designer has the option of using a self-tapping screw through a printed circuit board into a mounting hole at the bottom of the package. For most applications this is not necessary.

Package Housing Color

Versatile Link components and simplex connectors are color coded to eliminate confusion when making connections. The HFBR-15X1/2/4 transmitters are gray, and the HFBR-25X1/2/3/4 receivers are blue. The HFBR-15X3 transmitter is black.

All of the above transmitters and receivers are also available in black versions for special applications. These black components, combined with black fiber optic cable, form a "black link" which has superior immunity to external light. The black link is appropriate where improved housing opacity is required due to very bright ambient light or bright flashes of light. Black link components are otherwise identical to blue and gray components.

Connector Style

As shown, Versatile Link can be used with snap-in connectors: simplex, simplex latching, duplex, and duplex latching.

The simplex connector is intended for applications requiring simple, stable connection capability with a moderate retention force. The simplex latching connector provides similar convenience with a larger retention force. Connector/cable retention force can be improved by using a RTV adhesive within the connector. A suggested adhesive is 3M Company product: RTV-739.

The duplex connector connects a cable containing two fibers to two similar Versatile Link components. A lockout feature ensures the connection can be made in only one orientation. The duplex connector is intended for Versatile Link components "n-plexed" together, as discussed in the next section.

N-plexing
Versatile Link components can be stacked or interlocked (n-plexed) together to minimize use of printed circuit board space and to provide efficient, dual connections via the duplex connector. Up to eight identical package styles can be n-plexed and inserted by hand into a printed circuit board without difficulty. However, auto-insertability of stacked units becomes limited when more than two packages are n-plexed together.

Cable
Two cable versions are available: Simplex (single channel) and color coded duplex (dual channel). Each version of the cable is flame retardant (UL VW-1) and of low optical loss.

Two grades of the simplex cable are available: standard cable and improved cable. Improved cable is recommended for applications requiring longer distance needs, as reflected in the Link Selection Guide on page 5-12. Flexible cable construction allows simple cable installation techniques. Cables are discussed in detail on page 5-29.

Accessories
A variety of accessories are available. The bulkhead feed-through adapter discussed on page 5-30 can be used to mate two simplex snap-in connectors. It can be used either as a splice or a panel feedthrough for a panel thickness < 4.1 mm (0.16 inch).

Several accessories are offered to help with proper fiber/connector polishing. These are shown on page 5-31.

Manufacturing with Versatile Link

Non-stacked Versatile Link parts require no special handling during assembly of units onto printed circuit boards. Versatile Link components are auto-insertable. When wave soldering is performed with Versatile Link components, an optical port plug is recommended to be used to prevent contamination of the port. Water soluble fluxes, not rosin based fluxes, are recommended for use with Versatile Link components.

Refer to the Connectoring Section on page 5-33 for details of connectors and cable connectoring.

Versatile Link Performance

5 MEGABITS PER SECOND (NRZ)
1 MEGABIT PER SECOND (NRZ)
40 KILOBITS PER SECOND (NRZ)

The 5 Megabaud (MBd) Versatile Link is guaranteed to perform from dc to 5 Mb/s (megabits per second, NRZ). Distances up to 17 metres are guaranteed when the transmitter is driven with a current of 60 milliamperes. This represents worst case performance throughout the temperature range of 0 to 70 degrees centigrade. With the required drive circuit of Figure 1b and at 60 milliamp drive current, the 1 Megabaud Versatile Link has guaranteed performance over 0 to 70 degrees centigrade from dc to 1 Mb/s (NRZ) up to 34 metres.

The low current link requires only 6 mA peak supply current for the transmitter and receiver combined to achieve an 11 metre link. Extended distances up to 82 metres can be achieved at a maximum transmitter drive current of 60 mA peak. The 40 kBd Versatile Link is guaranteed to perform from dc to 40 kb/s (NRZ) over 0° to 70°C up to the distances just described.

Receivers are compatible with LSTTL, TTL, CMOS logic levels and offer a choice of an internal pull-up resistor or an open collector output. Horizontal or vertical packages provide identical performance and are compatible with simplex, simplex latching, duplex, and duplex latching connectors. Refer to the connector section (page 5-30) and the cable section (page 5-29) for further information about these products. A list of specific part numbers is found below and in the Selection Guide on page 5-11.

VERSATILE LINK GUIDE

Versatile Link		Unit	Horizontal Package	Vertical Package	Cable Link Length	
					Standard Cable	Improved Cable
High Performance	5 MBd	T_X	HFBR-1521	HFBR-1531	12 metres	17 metres
		R_X	HFBR-2521	HFBR-2531		
High Performance	1 MBd	T_X	HFBR-1522	HFBR-1532	24 metres	34 metres
		R_X	HFBR-2522	HFBR-2532		
Low Current/ Extended Distance	40 kBd	T_X	HFBR-1523	HFBR-1533	8 metres/ 60 metres	11 metres/ 82 metres
		R_X	HFBR-2523	HFBR-2533		
Standard	1 MBd	T_X	HFBR-1524	HFBR-1534	5 metres	7 metres
		R_X	HFBR-2524	HFBR-2534		

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min.	Max.	Units	Ref.
Ambient Temperature		T_A	0	70	°C	
Transmitter Peak Forward Current		$I_{F\,PK}$	10	750	mA	Note 1,8
Avg. Forward Current		$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	HFBR-25X3	V_{CC}	4.50	5.50	V	Note 2
	HFBR-25X1/25X2/25X4		4.75	5.25		
Output Voltage	HFBR-25X3	V_O		V_{CC}	V	
	HFBR-25X1/25X2/25X4			18		
Fanout (TTL)	HFBR-25X3	N		1		
	HFBR-25X1/25X2/25X4			5		

SYSTEM PERFORMANCE Under recommended operating conditions unless otherwise specified.

	Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
High Performance 5 MBd	Data Rate		dc		5	MBd	BER ≤ 10^{-9}, PRBS: 2^7-1	
	Link Distance with Standard Cable	ℓ	12			m	I_{Fdc} = 60 mA	Fig. 2a Note 7
			17	35		m	I_{Fdc} = 60 mA, 25°C	
	Link Distance with Improved Cable	ℓ	17			m	I_{Fdc} = 60 mA	Fig. 2b Note 7
			24	40		m	I_{Fdc} = 60 mA, 25°C	
	Propagation Delay	t_{PLH}		80	140	ns	R_L = 560 Ω, C_L = 30 pF ℓ = 0.5 metre -21.6 ≤ P_R ≤ -9.5 dBm	Fig. 3, 5 Notes 3, 6
		t_{PHL}		50	140	ns		
	Pulse Width Distortion	t_D		30		ns	P_R = -15 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 3, 4 Note 4
High Performance 1 MBd	Data Rate		dc		1	MBd	BER ≤ 10^{-9}, PRBS: 2^7-1	
	Link Distance with Standard Cable	ℓ	24			m	I_{Fdc} = 60 mA	Fig. 2a Notes 1, 7, 8
			30	50		m	I_{Fdc} = 60 mA, 25°C	
			30			m	I_{FPK} = 120 mA, 50% Duty Factor	
			36	60		m	I_{FPK} = 120 mA, 25°C, 50% Duty Factor	
	Link Distance with Improved Cable	ℓ	34			m	I_{Fdc} = 60 mA	Fig. 2b Notes 1, 7, 8
			41	65		m	I_{Fdc} = 60 mA, 25°C	
			44			m	I_{FPK} = 120 mA, 50% Duty Factor	
			51	75		m	I_{FPK} = 120 mA, 25°C, 50% Duty Factor	
	Propagation Delay	t_{PLH}		180	250	ns	R_L = 560 Ω, C_L = 30 pF ℓ = 0.5 metre P_R = -24 dBm	Fig. 3, 5 Notes 3, 8
		t_{PHL}		100	140	ns		
	Pulse Width Distortion	t_D		80		ns	P_R = -24 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 3, 4 Notes 4, 8

FIBER OPTICS

SYSTEM PERFORMANCE Under recommended operating conditions unless otherwise specified.

Link	Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Low Current/ Extended Distance 40 kBd	Data Rate		dc		40	kBd	BER ≤ 10^{-9}, PRBS: 2^7-1	
	Link Distance with Standard Cable	ℓ	8	30		m	I_{Fdc} = 2 mA	Fig. 2c Note 7
			60	100		m	I_{Fdc} = 60 mA	
	Link Distance with Improved Cable	ℓ	11	35		m	I_{Fdc} = 2 mA	Fig. 2d Note 7
			82	125		m	I_{Fdc} = 60 mA	
	Propagation Delay	t_{PLH}		4		μs	R_L = 3.3 kΩ, C_L = 30 pF = 1 metre P_R = -25 dBm	Fig. 3, 7 Note 3
		t_{PHL}		2.5		μs		
	Pulse Width Distortion	t_D			7.0	μs	-39 ≤ P_R ≤ -14 dBm R_L = 3.3 kΩ, C_L = 30 pF	Fig. 3, 6 Note 4
Standard 1 MBd	Data Rate		dc		1	MBd	BER ≤ 10^{-9}, PRBS: 2^7-1	
	Link Distance with Standard Cable	ℓ	5			m	I_{Fdc} = 60 mA	Fig. 2e Notes 1, 7, 8
			11	30		m	I_{Fdc} = 60 mA, 25°C	
			12			m	I_{FPK} = 120 mA, 50% Duty Factor	
			18	40		m	I_{FPK} = 120 mA, 25°C, 50% Duty Factor	
	Link Distance with Improved Cable	ℓ	7			m	I_{Fdc} = 60 mA	Fig. 2f Notes 1, 7, 8
			15	40		m	I_{Fdc} = 60 mA, 25°C	
			17			m	I_{FPK} = 120 mA, 50% Duty Factor	
			25	50		m	I_{FPK} = 120 mA, 25°C, 50% Duty Factor	
	Propagation Delay	t_{PLH}		180	250	ns	R_L = 560 Ω, C_L = 30 pF ℓ = 0.5 metre P_R = -20 dBm	Fig. 3, 5 Notes 3, 8
		t_{PHL}		100	140	ns		
	Pulse Width Distortion	t_D		80		ns	P_R = -20 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 3, 4 Notes 4, 8

Notes:

1. For I_{FPK} > 80 mA, the duty factor must be such as to keep I_{FDC} ≤ 80 mA. In addition, for I_{FPK} > 80 mA, the following rules for pulse width apply:
   I_{FPK} ≤ 160 mA: Pulse width ≤ 1 ms
   I_{FPK} ≥ 160 mA: Pulse width ≤ 1 μs, period ≥ 20 μS.
2. It is essential that a bypass capacitor, 0.1 μF ceramic, be connected from pin 2 to pin 3 of the HFBR-25X1/25X2/25X4 receivers and from pin 2 to pin 4 of the HFBR-25X3 receiver. Total lead length between both ends of the capacitor and the supply pins should not exceed 20 mm.
3. The propagation delay for one metre of cable is typically 5 ns.
4. $t_D = t_{PLH} - t_{PHL}$.
5. Typical data is at 25° C, V_{CC} = 5 V.
6. Typical propagation delay is measured at P_R = -15 dBm.
7. Estimated typical link life expectancy at 40° C exceeds 10 years at 60 mA.
8. Pulsed LED operation at I_{FPK} > 80 mA will cause increased link t_{PLH} propagation delay time. This extended t_{PLH} time contributes to increased pulse width distortion of the receiver output signal.
9. Pins 5 and 8 of both the transmitter and receiver are for mounting and retaining purposes only. Do not electrically connect pin 5 and/or pin 8.

Versatile Link Design Considerations

Simple interface circuits for 5 MBd, 1 MBd and 40 kBd applications are shown in Figure 1. The value of the transmitter drive current depends upon the desired link distance. This is shown in Figures 2a through 2f. After selecting a value of transmitter drive current, I_F, the value of R1 can be determined with the aid of Figures 1a, 1b and 1d. Note that the 5 MBd and 40 kBd Versatile Links can have an overdrive and underdrive limit for the chosen value of I_F while the 1 MBd Versatile Link has only an underdrive limit. Dotted lines in Figures 2a through 2f represent pulsed operation for extended link distance requirements. For the 1 MBd interface circuit, the R1C1 time constant must be > 75 ns. Conditions described in Note 1 must be met for pulsed operation. Refer to Note 8 for performance comments when pulsed operation is used.

All specifications are guardbanded for worst case conditions between 0 to 70 degrees centigrade. All tolerances and variations (including end-of-life transmitter power, receiver sensitivity, coupling variances, connector and cable variations) are taken into account.

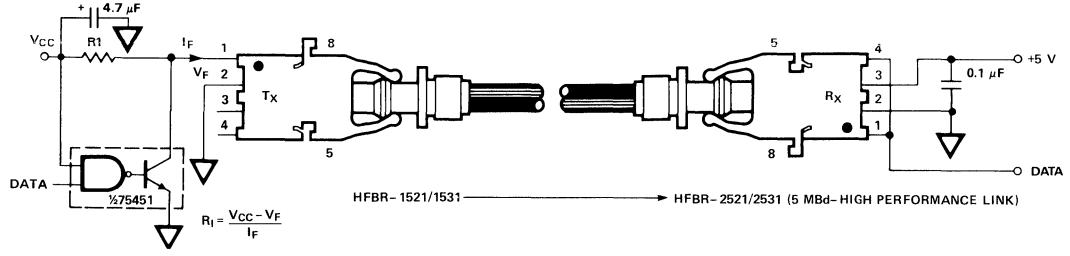
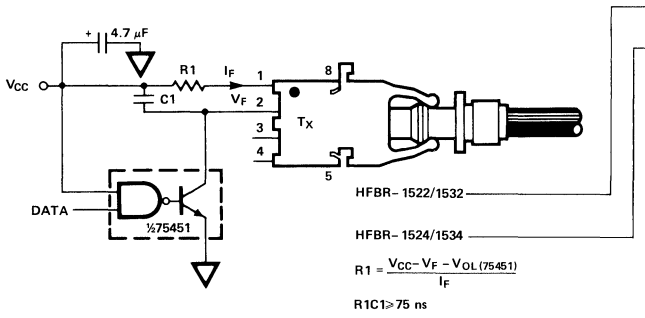


Figure 1a. Typical 5 MBd Interface Circuit;

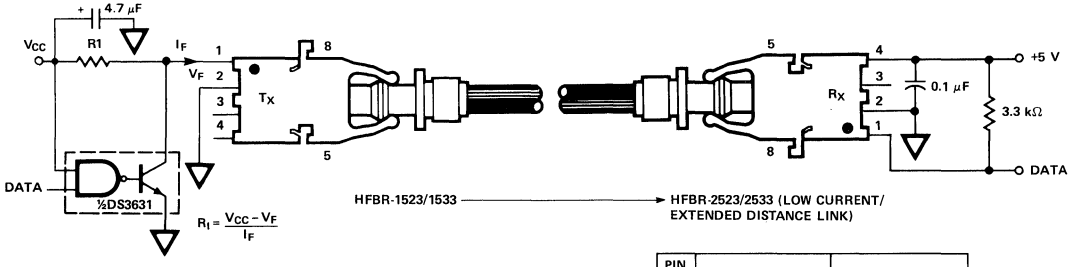


1b. Required 1 MBd Interface Circuit;

PIN NO.	TX	RX
1	ANODE	V_O
2	CATHODE	GND
3	OPEN	V_{CC}
4	OPEN	R_L
5	DO NOT CONNECT*	DO NOT CONNECT*
6	–	–
7	–	–
8	DO NOT CONNECT*	DO NOT CONNECT*

*SEE NOTE 9 PG.6

1c. Electrical Pin Assignments for 5 MBd and 1 MBd Transmitters and Receivers



1d. Typical 40 kBd Interface Circuit;

PIN NO.	TX	RX
1	ANODE	V_O
2	CATHODE	GND
3	OPEN	OPEN
4	OPEN	V_{CC}
5	DO NOT CONNECT*	DO NOT CONNECT*
6	–	–
7	–	–
8	DO NOT CONNECT*	DO NOT CONNECT*

*SEE NOTE 9 PG.6

1e. Electrical Pin Assignments for 40 kBd Transmitters and Receivers

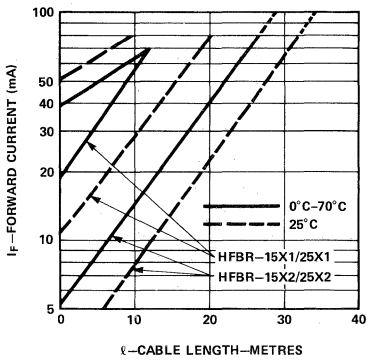


Figure 2a. Guaranteed System Performance for the HFBR-15X1/25X1 and HFBR-15X2/25X2 Links with Standard Cable

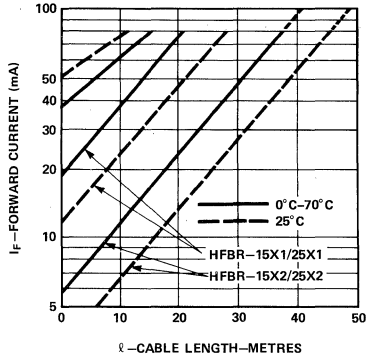


Figure 2b. Guaranteed System Performance for the HFBR-15X1/25X1 and HFBR-15X2/25X2 Links with Improved Cable

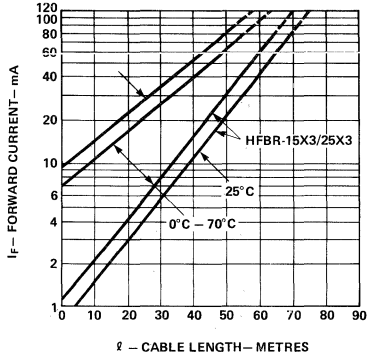


Figure 2c. Guaranteed System Performance for the HFBR-15X3/25X3 Link with Standard Cable

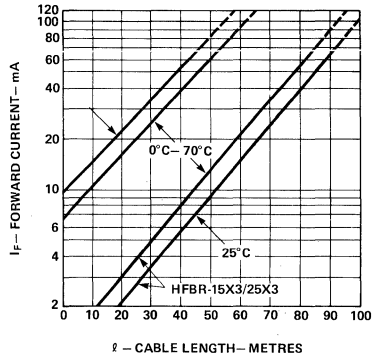


Figure 2d. Guaranteed System Performance for the HFBR-15X3/25X3 Link with Improved Cable

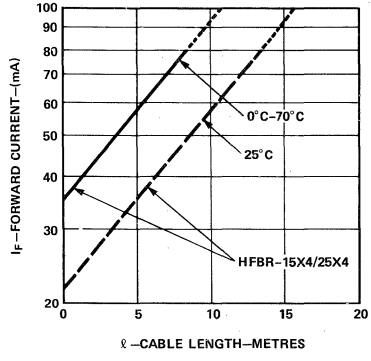


Figure 2e. Guaranteed System Performance for the HFBR-15X4/25X4 Link with Standard Cable

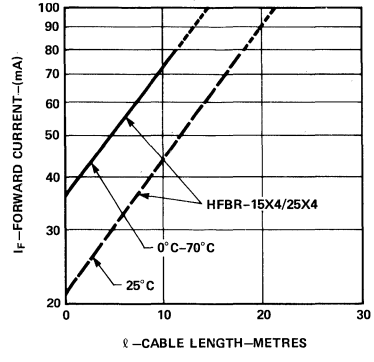


Figure 2f. Guaranteed System Performance for the HFBR-15X4/25X4 Link with Improved Cable

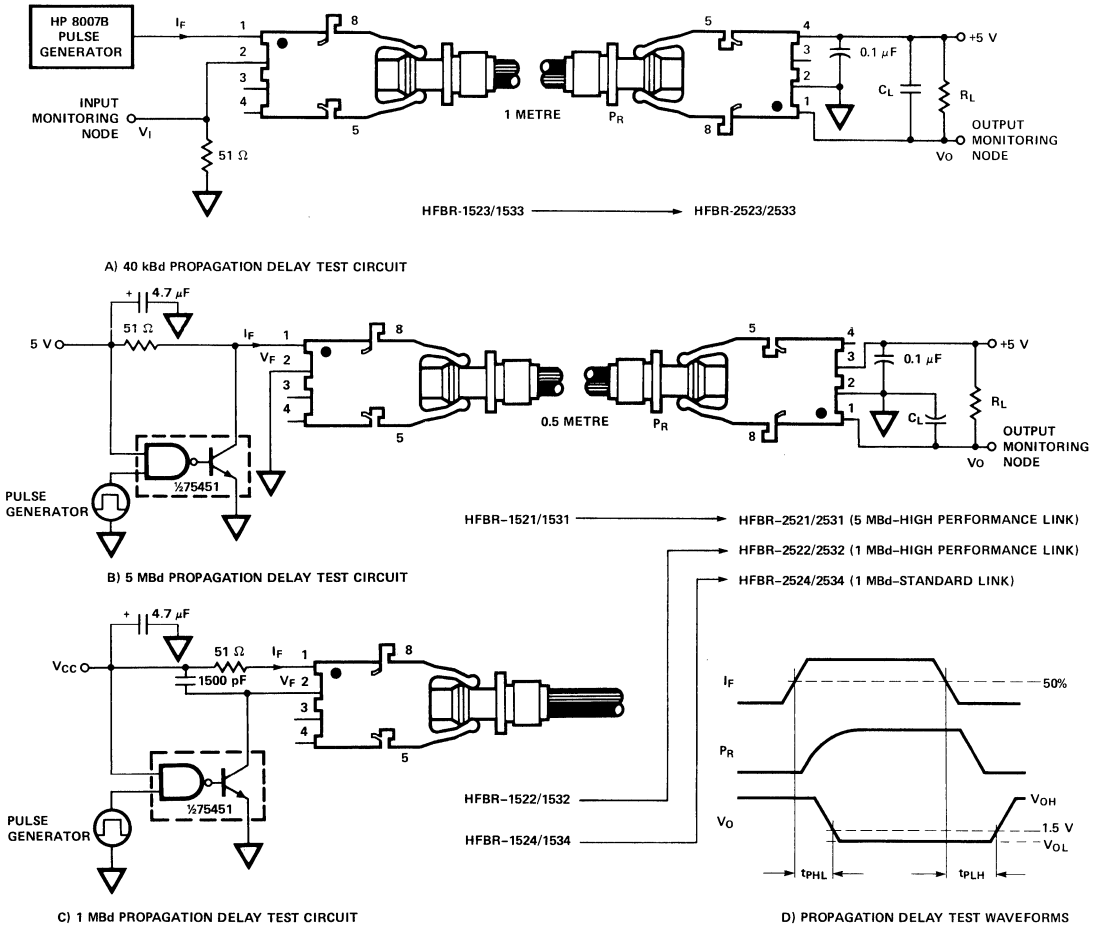


Figure 3. Propagation Delay Test Circuits and Waveforms: a) 40 kBd, b) 5 MBd, c) 1 MBd, d) Test Waveforms

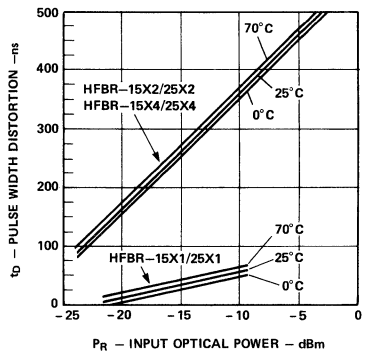


Figure 4. Typical HFBR-15X1/25X1, HFBR-15X2/25X2 and HFBR-15X4/25X4 Link Pulse Width Distortion vs. Optical Power

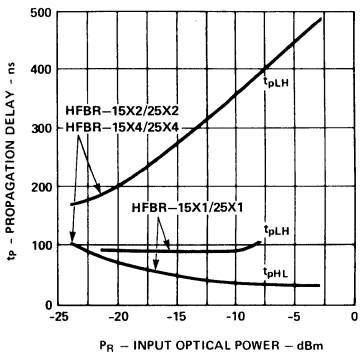


Figure 5. Typical HFBR-15X1/25X1, HFBR-15X2/25X2 and HFBR-15X4/25X4 Link Propagation Delay vs. Optical Power

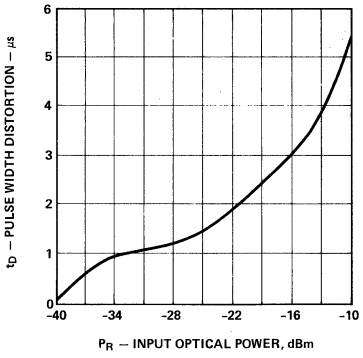


Figure 6. Typical HFBR-15X3/25X3 Link Pulse Width Distortion vs. Optical Power

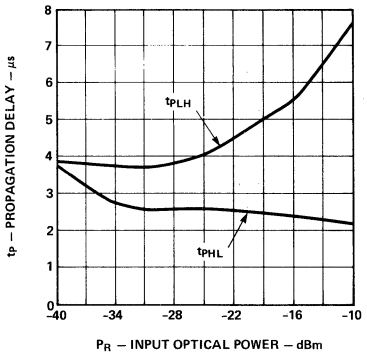


Figure 7. Typical HFBR-15X3/25X3 Link Propagation Delay vs. Optical Power

Versatile Link Photo Interrupter

20 KHz (40 kBd) LINK, 500 kHz (1 MBd) LINK

Versatile Link may be used as a photo-interrupter in optical switches, shaft position sensors, velocity sensors, position sensors, and other similar applications. This link is particularly useful where high voltage, electrical noise, or explosive environments prohibit the use of electromechanical or optoelectronic sensors. The 20 kHz (40 kBd) transmitter/receiver pair has an optical power budget of 25 dB. The 500 kHz (1 MBd) transmitter/receiver pair has an optical power budget of 10 dB. Total system losses (cable attenuation, air gap loss, etc.) must not exceed the link optical power budget.

RECOMMENDED OPERATING CONDITIONS

Recommended operating conditions are identical to those of the Low Current/Extended Distance and High Performance 1 MBd links. Refer to page 5-15.

SYSTEM PERFORMANCE

These specification apply when using Standard and Improved cable and, unless otherwise specified, under recommended operating conditions. Refer to the appropriate link data on pages 5-17 and 5-18 for additional design information.

Parameter	Min.	Typ.[1]	Max.	Units	Conditions	Ref.
HFBR-15X3/25X3						
Max. Count Frequency	dc		20	kHz		
Optical Power Budget	25.4			dB	I_{Fdc} = 60 mA, 0-70°C	Note 2
	27.8	34		dB	I_{Fdc} = 60 mA, 25°C	
HFBR-15X2/25X2						
Max. Count Frequency	dc		500	kHz		
Optical Power Budget	10.4			dB	I_{Fdc} = 60 mA, 0-70°C	Note 2
	12.8	15.6		dB	I_{Fdc} = 60 mA, 25°C	

1. Typical data is at T_A = 25°C, V_{CC} = 5 V.
2. Optical Power Budget = P_T min. = P_R (L) min. Refer to page XX for additional design information.

Photo Interrupter Link Design Considerations

The fiber optic Transmitter/Receiver pair is intended for applications where the photo interrupter must be physically separated from the optoelectronic emitter and detector. This separation would be useful where high voltage, electrical noise or explosive environments prohibit the use of electronic devices. To ensure reliable long term operation, link design for this application should operate with an ample optical power margin $\alpha_M \geq 3$ dB, since the exposed fiber ends are subject to environmental contamination that will increase the optical attenuation of the slot with time. A graph of air gap separation versus attenuation for clean fiber ends with minimum radial error $\leq$ 0.127 mm (0.005 inches) and angular error ($\leq$3.0°) is provided in Figure 8.

The following equations can be used to determine the transmitter output power, P_T, for both the overdrive and underdrive cases. Overdrive is defined as a condition where excessive optical power is delivered to the receiver. The first equation calculates, for a predetermined link length and slot attenuation, the maximum P_T in order not to overdrive the receiver. The second equation defines the minimum P_T allowed for link operation to prevent underdrive condition from occurring, where α_o is the fiber attenuation.

$$P_T\,(MAX) - P_R\,(MAX) \leq \alpha_{O\,MIN}\,\ell + \alpha_{SLOT} \qquad \text{Eq. 1}$$

$$P_T\,(MIN) - P_{RL}\,(MIN) \geq \alpha_{O\,MAX}\,\ell + \alpha_{SLOT} + \alpha_M \qquad \text{Eq. 2}$$

Once P_T (MIN) has been determined in the second equation for a specific link length (ℓ), slot attenuation (α_{SLOT}) and margin (α_M). Figure 9 can then be used to find I_F.

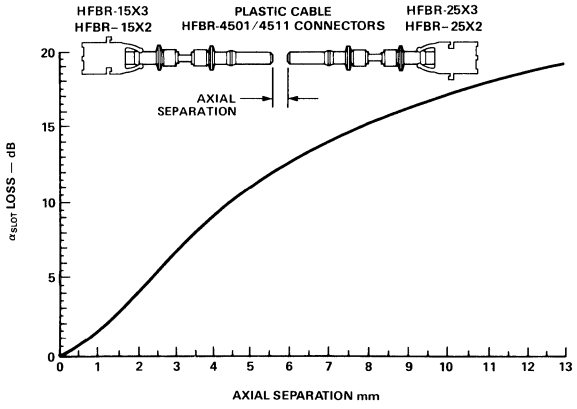


Figure 8. Typical Loss vs. Axial Separation.

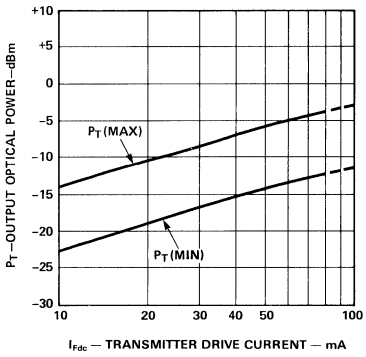


Figure 9. Typical HFBR-15X3/15X2 Optical Power vs. Transmitter I_F (0-70°C)

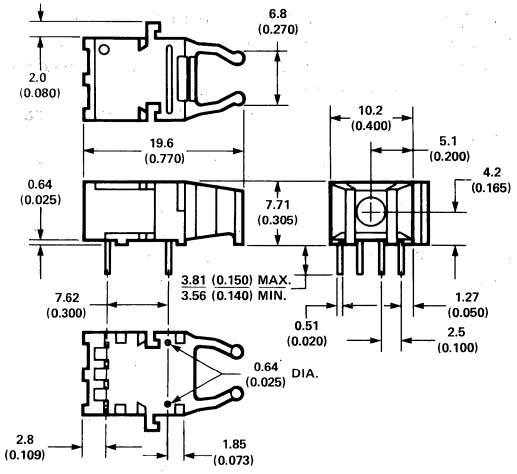
FIBER OPTICS

Versatile Link Mechanical Dimensions

All dimensions in mm (inches).
All dimensions ±0.25 mm unless otherwise specified.

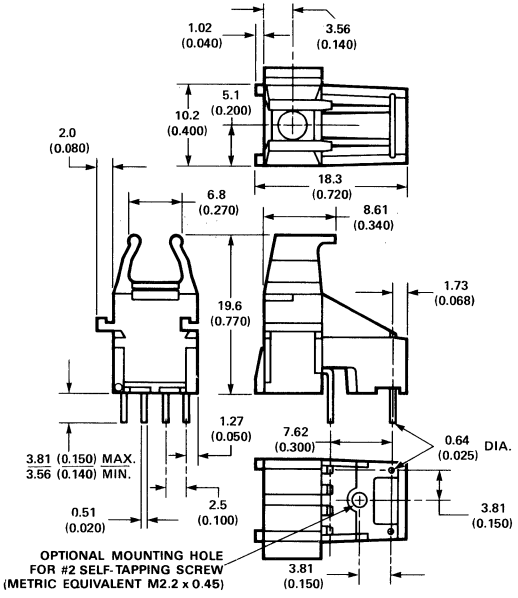
HORIZONTAL MODULES

HFBR-1521/1522/1524 (GRAY), HFBR-1523 (BLACK)
HFBR-2521/2522/2523/2524 (BLUE)

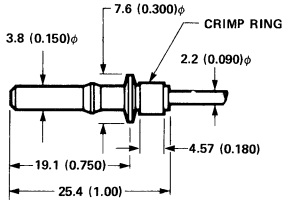


VERTICAL MODULES

HFBR-1531/1532/1534 (GRAY, HFBR-1533 (BLACK)
HFBR-2531/2532/2533/2534 (BLUE)

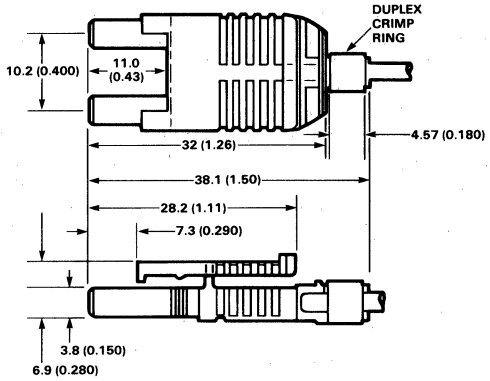


HFBR-4501 (GRAY)/4511 (BLUE) SIMPLEX CONNECTOR

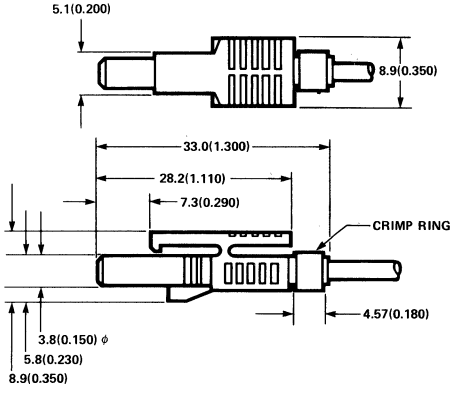


CONNECTORS DIFFER ONLY IN COLOR

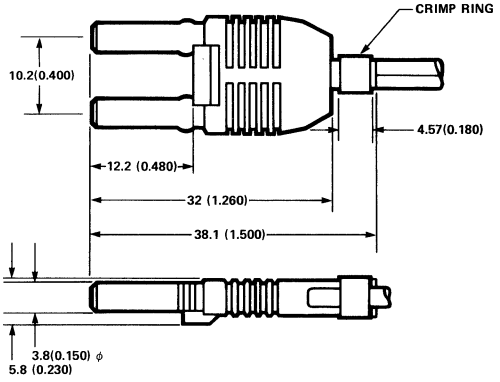
HFBR-4516 (PARCHMENT) DUPLEX LATCHING CONNECTOR



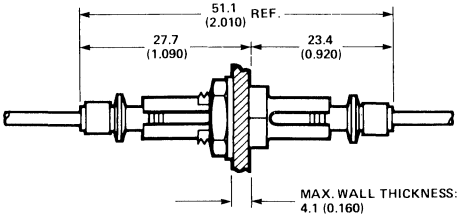
HFBR-4503 (GRAY)/4513 (BLUE) SIMPLEX LATCHING CONNECTOR



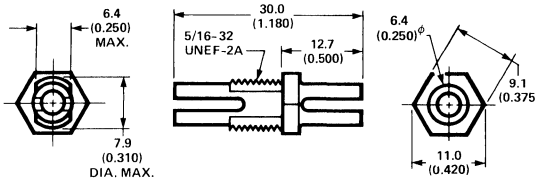
HFBR-4506 (PARCHMENT) DUPLEX CONNECTOR



BULKHEAD FEEDTHROUGH WITH TWO HFBR-4501/4511 CONNECTORS



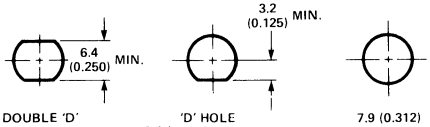
HFBR-4505 (GRAY)/4515 (BLUE) ADAPTERS



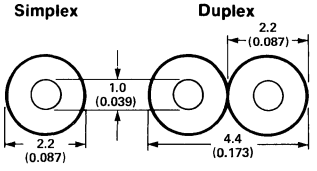
PANEL MOUNTING — BULKHEAD FEEDTHROUGH

THREE TYPES OF PANEL/BULKHEAD HOLES CAN BE USED.

DIMENSIONS IN mm (INCHES)
ALL DIMENSIONS ±0.2 mm



FIBER OPTIC CABLE DIMENSIONS

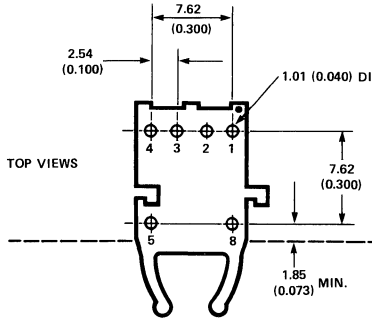


DIMENSIONS IN MILLIMETRES AND (INCHES)

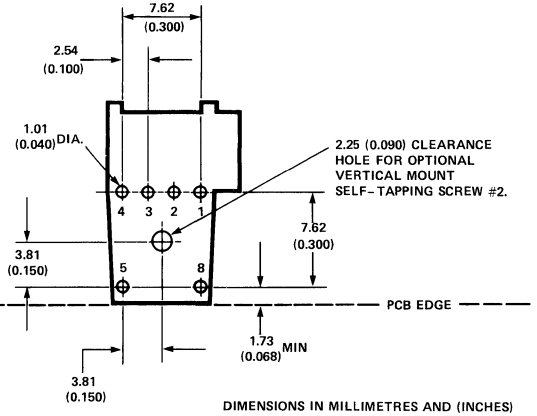
Versatile Link Printed Circuit Board Layout Dimensions

TOP VIEWS

HORIZONTAL MODULE



VERTICAL MODULE



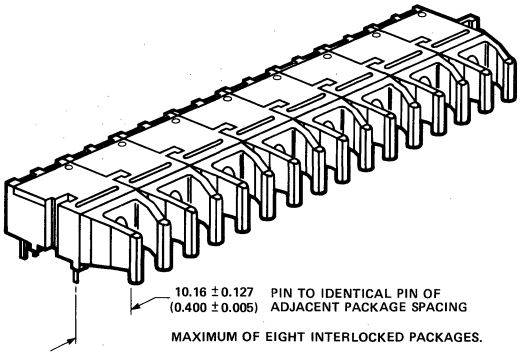
DIMENSIONS IN MILLIMETRES AND (INCHES)

ELECTRICAL PIN FUNCTIONS

PIN NO.	TRANSMITTERS HFBR-15XX	RECEIVERS EXCLUDING HFBR-25X3	RECEIVER HFBR-25X3
1	ANODE	V_O	V_O
2	CATHODE	GROUND	GROUND
3	OPEN	V_{CC}	OPEN
4	OPEN	R_L	V_{CC}
5	DO NOT CONNECT	DO NOT CONNECT	DO NOT CONNECT
8	DO NOT CONNECT	DO NOT CONNECT	DO NOT CONNECT

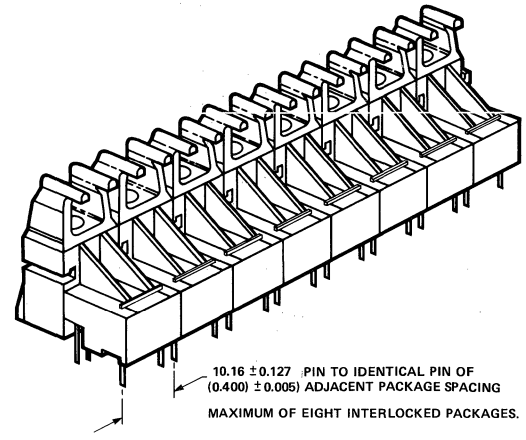
Interlocked (Stacked) Assemblies

STACKING HORIZONTAL MODULES



Recommended stacking assembly of horizontal packages is easily accomplished by placing units upside down with pins facing upward. Initially engage the interlocking mechanism by sliding the L bracket body from above into the L slot body of the lower package. Lay the partially interlocked units on a flat surface and push down with a thin, rigid, rectangular edged object to bring all stacked units into uniform alignment. This technique prevents potential harm that could occur to fingers and hands of assemblers from the package pins. Refer to Figure 1 below that illustrates this assembly. Stacked horizontal packages can be disengaged should there be a need to do so. Repeated stacking and unstacking causes no damage to individual units.

STACKING VERTICAL MODULES



Recommended stacking of vertical packages is to hold two vertical units, one in each hand, with the pins facing away from the assembler and the optical ports located in the bottom front of each unit. Engage completely, the L bracket unit from above into the lower L slot unit. Package to package alignment is easily insured by laying the full, flat, bottom side of the assembled units onto a flat surface pushing with a finger the two packages into complete, parallel alignment. The thin rectangular edged tool, used for horizontal package alignment, is not needed with the vertical packages. Stacked vertical packages can be disengaged should there be a need to do so. Repeated stacking and unstacking causes no damage to individual units.

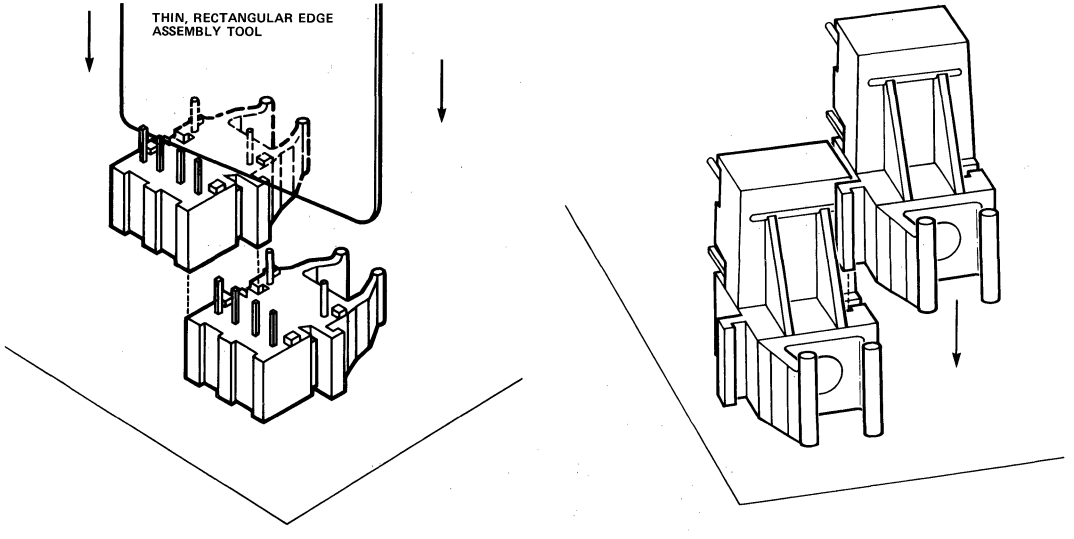


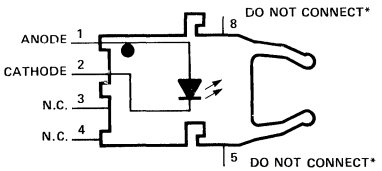
Figure 11. Interlocked (Stacked) Horizontal or Vertical Packages.

Versatile Link Transmitters

HFBR-1521/1531 (5 MBd - High Performance)
HFBR-1522/1532 (1 MBd - High Performance)
HFBR-1523/1533 (40 kBd - Low Current/Extended Distance)
HFBR-1524/1534 (1 MBd - Standard)

Versatile Link transmitters incorporate a 660 nanometre LED in a horizontal or vertical housing. The HFBR-15X3 transmitter housing is black. HFBR-15X1/2/4 standard housings are gray, but black versions are available. The transmitters can be easily interfaced to standard TTL or CMOS logic. The optical output power of the HFBR-152X/153X series is specified at the end of 0.5 m of cable. The mechanical and electrical pin spacing and connections are identical for both the horizontal and vertical packages.

HFBR-152X/153X SERIES TRANSMITTERS



*SEE NOTE 7

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec.	
Peak Forward Input Current		I_{FPK}		1000	mA	Note 2
DC Forward Input Current		I_{FDC}		80	mA	
Reverse Input Voltage		V_R		5	V	

Electrical/Optical Characteristics 0°C to +70°C Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Transmitter Output Optical Power	HFBR-15X1	P_T	-16.5		-7.6	dBm	I_{Fdc} = 60 mA, 0-70°C	Fig. 2
			-14.3		-8.0	dBm	I_{Fdc} = 60 mA, 25°C	Notes 3, 4
	HFBR-15X2 and HFBR-15X3	P_T	-13.6		-4.5	dBm	I_{Fdc} = 60 mA, 0-70°C	
			-11.2		-5.1	dBm	I_{Fdc} = 60 mA, 25°C	
	HFBR-15X3	P_T	-35.5			dBm	I_{Fdc} = 2 mA, 0-70°C	
	HFBR-15X4	P_T	-17.8		-4.5	dBm	I_{Fdc} = 60 mA, 0-70°C	
			-15.5		-5.1	dBm	I_{Fdc} = 60 mA, 25°C	
Output Optical Power Temperature Coefficient		$\frac{\Delta P_T}{\Delta T}$		-0.85		%/°C		
Peak Emission Wavelength		λ_{PK}		660		nm		
Forward Voltage		V_F	1.45	1.67	2.02	V	I_{Fdc} = 60 mA	
Forward Voltage Temperature Coefficient		$\frac{\Delta V_F}{\Delta T}$		-1.37		mV/°C		Fig. 1
Effective Diameter		D_T		1		mm		
Numerical Aperture		N.A.		0.5				
Reverse Input Breakdown Voltage		V_{BR}	5.0	11.0		V	I_{Fdc} = 10 μA, T_A = 25°C	
Diode Capacitance		C_O		86		pF	V_F = 0, f = 1 MHz	
Rise Time		t_r		80		ns	10% to 90%, I_F = 60 mA	Note 6
Fall Time		t_f		40		ns		

Notes:

1. 1.6 mm below seating plane.
2. 1 μs pulse, 20 μs period.
3. Measured at the end of 0.5 m Standard Fiber Optic Cable with large area detector.
4. Optical power, P (dBm) = 10 Log [P (μW)/1000 μW].
5. Typical data is at 25°C.
6. Rise and fall times are measured with a voltage pulse driving the transmitter and a series connected 50 ohm load. A wide bandwidth optical to electrical waveform analyzer (transducer), terminated to a 50 ohm input of a wide bandwidth oscilloscope, is used for this response time measurement.
7. Pins 5 and 8 of the transmitter are for mounting and retaining purposes only. Do not electrically connect pin 5 and/or pin 8.

WARNING: When viewed under some conditions, the optical port of the Transmitter may expose the eye beyond the Maximum Permissible Exposure recommended in ANSI Z-136-1, 1981. Under most viewing conditions there is no eye hazard.

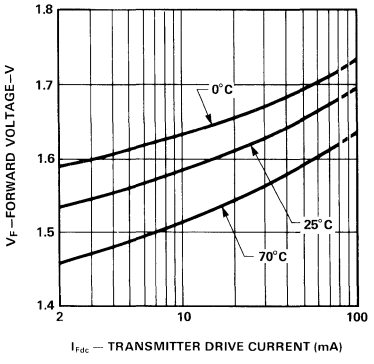


Figure 12. Typical Forward Voltage vs. Drive current for HFBR-152X/153X Series Transmitters.

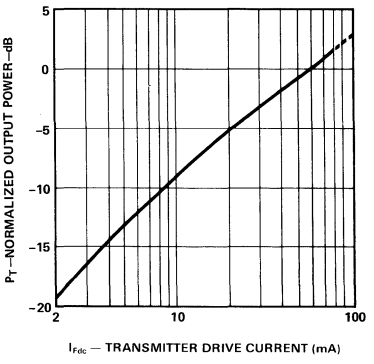


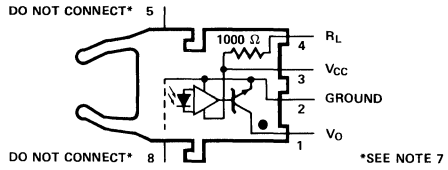
Figure 13. Normalized HFBR-152X/153X Series Transmitter Typical Output Optical Power vs. Drive Current.

Versatile Link Receivers

HFBR-2521/2531 (5 MBd - High Performance)
HFBR-2522/2532 (1 MBd - High Performance)
HFBR-2524/2534 (1 MBd - Standard)

The Versatile Link receivers feature a shielded, integrated photodetector and a wide bandwidth dc amplifier with high EMI immunity. A Schottky clamped open-collector output transistor allows interfacing to common logic families and enables "wired-OR" circuit designs. The open collector output is specified up to 18 V. An integrated 1000 ohm resistor internally connected to V_{CC} may be externally connected to provide a pull-up for ease of use with +5 V logic. Under pulsed LED current operation (I_F > 80 mA), the combination of a high optical power level and the optical falling edge of the LED transmitter will result in increased pulse width distortion of the receiver output signal. The standard receiver housings are blue; black versions are available.

HFBR-25X1/25X2/25X4 RECEIVER



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec.	
Supply Voltage		V_{CC}	-0.5	7	V	Note 6
Output Collector Current		I_O		25	mA	
Output Collector Power Dissipation		P_{OD}		40	mW	
Output Voltage		V_O	-0.5	18	V	
Pullup Voltage		V_{RL}	-0.5	V_{CC}	V	

Electrical/Optical Characteristics

0°C to +70°C, 4.75 V ≤ V_{CC} ≤ 5.25 V Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Receiver Input Optical Power Level for Logic "0"	HFBR-2521 and HFBR-2531	$P_{R(L)}$	-21.6		-9.5	dBm	V_{OL} = 0.5 V, I_{OL} = 8 mA	Notes 2, 3, 8
			-21.6		-8.7	dBm	25°C, V_{OL} = 0.5 V, I_{OL} = 8 mA	
	HFBR-2522 and HFBR-2532	$P_{R(L)}$	-24			dBm	V_{OL} = 0.5 V, I_{OL} = 8 mA	Notes 2, 3, 8, 9
			-24			dBm	25°C, V_{OL} = 0.5 V, I_{OL} = 8 mA	
	HFBR-2524 and HFBR-2534	$P_{R(L)}$	-20			dBm	V_{OL} = 0.5 V, I_{OL} = 8 mA	Notes 2, 3, 8, 9
			-20			dBm	25°C, V_{OL} = 0.5 V, I_{OL} = 8 mA	
Input Optical Power Level for Logic "1"		$P_{R(H)}$			-43	dBm	V_{OH} = 5.25 V, I_{OH} ≤ 250 μA	Note 2
High Level Output Current		I_{OH}		5	250	μA	V_O = 18 V, P_R = 0	Note 4
Low Level Output Voltage		V_{OL}		0.4	0.5	V	I_{OL} = 8 mA, P_R = $P_{R(L)\,MIN}$	Note 4
High Level Supply Current		I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V, P_R = 0 μW	Note 4
Low Level Supply Current		I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V, P_R = -12.5 dBm	Note 4
Effective Diameter		D_R		1		mm		
Numerical Aperture		**N.A.**		0.5				
Internal Pull-Up Resistor		R_L	680	1000	1700	Ohms		

FIBER OPTICS

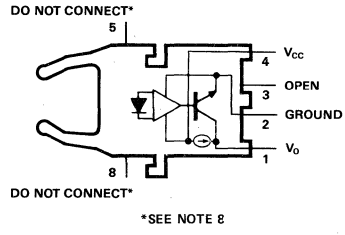
Notes:
1. 1.6 mm below seating plan.
2. Optical flux, P (dBm) = 10 Log [P (μW)/1000 μW].
3. Measured at the end of Fiber Optic Cable with large area detector. detector.
4. R_L is open.
5. Typical data is at 25°C, V_{CC} = 5 V.
6. It is essential that a bypass capacitor 0.01 μF be connected from pin 2 to pin 3 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.
7. Pins 5 and 8 of both the transmitter and receiver are for mounting and retaining purposes only. Do not electrically connect pin 5 and/or pin 8.
8. Pulsed LED operation at I_F > 80 mA will cause increased link t_{PLH} propagation delay time. This extended t_{PLH} time contributes to increased pulse width distortion of the receiver output signal.
9. The LED driver circuit of Figure 1b (Link Design Considerations) is required for 1 MBd operation of the HFBR-2522/2532/2524/2534.

High Sensitivity Receiver

HFBR-25X3

The blue plastic HFBR-25X3 Receiver module has a sensitivity of -39 dBm. It features an integrated photodetector and dc amplifier with high EMI immunity. The output is an open collector with a 150 μA internal current source pull-up and is compatible with TTL/LSTTL and most CMOS logic families. For minimum rise time add an external pull-up resistor of at least 3.3K ohms. V_{CC} must be greater than or equal to the supply voltage for the pull-up resistor.

HFBR-25X3 RECEIVER



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp			260	°C	Note 1
	Time			10	sec	
Supply Voltage		V_{CC}	-0.5	7	V	Note 7
Output Collector Current (Average)		I_O	-1	5	mA	
Output Collector Power Dissipation		P_{OD}		25	mW	
Output Voltage		V_O	-0.5	V_{CC}	V	

Electrical/Optical Characteristics 0° C to +70° C, 4.5 ≤ V_{CC} ≤ 5.5 Unless Otherwise Specified

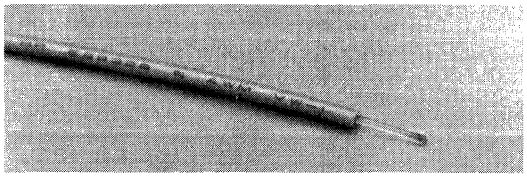
Parameter		Symbol	Min.	Typ. (5)	Max.	Units	Conditions	Ref.
Receiver Input Optical Power Level for Logic "0"	HFBR-2523 and HFBR-2533	$P_{R(L)}$	-39		-13.7	dBm	$V_O = V_{OL}$, I_{OL} = 3.2 mA	Note 2, 3, 4
			-39		-13.3	dBm	25° C, $V_O = V_{OL}$, I_{OL} = 3.2 mA	
Input Optical Power Level for Logic "1"		$P_{R(H)}$			-53	dBm	V_{OH} = 5.5V, $I_{OH} \leq 40$ μA	Note 2
High Level Output Voltage		V_{OH}	2.4			V	I_{OH} = -40 μA, P_R = 0 μW	
Low Level Output Voltage		V_{OL}			0.4	V	I_{OL} = 3.2 mA, $P_R = P_{RL\ MIN}$	Note 6
High Level Supply Current		I_{CCH}		1.2	1.9	mA	V_{CC} = 5.5V, P_R = 0 μW	
Low Level Supply Current		I_{CCL}		2.9	3.7	mA	V_{CC} = 5.5V, $P_R \geq P_{RL}$ (MIN)	Note 6
Effective Diameter		D_R		1		mm		
Numerical Aperture		N.A.		0.5				

Notes:
1. 1.6 mm below seating plan.
2. Optical flux, P (dBm) = 10 Log P (μW)/1000 μW.
3. Measured at the end of Fiber Optic Cable with large area detector.
4. Because of the very high sensitivity of the HFBR-25X3, the digital output may switch in response to ambient light levels when a cable is not occupying the receiver optical port. The designer should take care to filter out signals from this source if they pose a hazard to the system.
5. Typical data is at 25° C, V_{CC} = 5 V.
6. Including current in 3.3 K pull-up resistor.
7. It is recommended that a bypass capacitor 0.01 μF to 0.1 μF ceramic be connected from pin 2 to pin 4 of the receiver.
8. Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect pin 5 and/or pin 8.

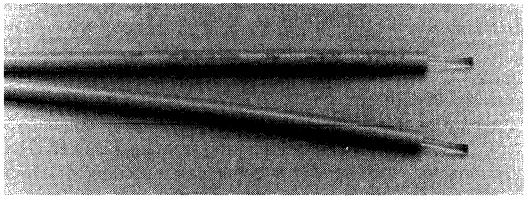
Plastic Fiber Optic Cable

Simplex Fiber Optic Cable is constructed of a single step index plastic fiber sheathed in a plastic jacket. Duplex Fiber Optic Cable has two plastic fibers, each in a cable of construction similar to the Simplex Cable, joined with a web. The individual channels are identified by a marking on one channel of the cable. The Improved Fiber Optic Cable is identical to the Standard Cable except that the attenuation is lower.

These cables are UL recognized components and pass UL VW-1 flame retardancy specification. Safe cable properties in flammable environments, along with non-conductive electrical characteristics of the cable may make the use of conduit unnecessary. Plastic cable is available unconnectored or connectored. Refer to page 5-34 for part numbers. numbers.



SIMPLEX CABLE



DUPLEX CABLE

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	-40	+75	°C	
Installation Temperature		T_I	-20	+70	°C	
Short Term Tensile Force	Single Channel	F_T		50	N	Note 1
	Dual Channel	F_T		100	N	
Short Term Bend Radius		r	10		mm	Note 2
Long Term Bend Radius		r	35		mm	
Long Term Tensile Load		F_T		1	N	
Flexing				1000	Cycles	Note 3
Impact		m		0.5	kg	Note 4
		h		150	mm	

Electrical/Optical Characteristics 0°C to +70°C Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Cable Attenuation	Standard Cable	α_o	0.19	0.31	0.43	dB/m	Source is HFBR-152X/153X (660 nm), ℓ = 20 m	Note 7
	Improved Cable		0.19	0.25	0.31			
Numerical Aperture		N.A.		0.5			$\ell > 2$ m	
Diameter, Core		D_C		1.0		mm		
Diameter, Jacket		D_J		2.2		mm	Simplex Cable	
Travel Time Constant		ℓ/v		5.0		nsec/m		Note 6
Mass per Unit Length/Channel		m/ℓ		4.6		g/m	Without Connectors	
Cable Leakage Current		I_L		12		nA	50 kV, ℓ = 0.3 m	

Notes:

1. Less than 30 minutes.
2. Less than 1 hour, non-operating.
3. 90° bend on 10 mm radius mandrel. Bend radius is the radius of the mandrel around which the cable is bent.
4. Tested at 1 impact according to MIL-STD-1678, Method 2030, Procedure 1.
5. Typical data is at 25°C.
6. Travel time constant is the reciprocal of the group velocity for propagation of optical power. Group velocity is v = c/n, where c is the velocity of light in space (3×10^8 m/s) and n equals effective core index of refraction. Unit length of cable is ℓ.
7. In addition to standard Hewlett-Packard 100% product testing, HP provides additional margin to ensure link performance. Under certain conditions, cable installation and improper connectoring may reduce performance. Contact Hewlett-Packard for recommendations.
8. Improved cable is available in 500 metre spools and in factory-connectored lengths less than 100 metres.

Versatile Link Fiber Optic Connectors

CONNECTORS FEEDTHROUGH/SPLICE POLISHING TOOLS

Versatile Link transmitters and receivers are compatible with three connector styles; simplex, simplex latching, and duplex. All connectors provide a snap-action when mated to Versatile Link components. Simplex connectors are color coded to match with transmitter and receiver color coding. Duplex connectors are keyed so that proper orientation is ensured. When removing a connector from a module, pull at the connector body. Do not pull on the cable alone. The same, quick and simple connectoring technique is used with all connectors and cable. This technique is described on page 18. Note that simplex and duplex crimp rings are different.

Simplex Connector Styles

HFBR-4501/4511 — Simplex

The simplex connector provides a quick and stable connection for applications that require a component to provide retention force of 8 newtons (1.8 lb). These connectors are available in colors of gray (HFBR-4501) or blue (HFBR-4511).

HFBR-4503/4513 — Simplex Latching

The simplex latching connector is designed for rugged applications requiring greater retention force, 80 N (18 lbs), than that provided by a simplex connector. When inserting the simplex latching connector into a module, the connector latch mechanism should be aligned with the top surface of the horizontal module, or with the tall vertical side of the vertical module. Misorientation of an inserted latching connector into either module housing will not result in a positive latch. The connector is released by depressing the rear section of the connector lever, and then pulling the connector assembly away from the module housing.

If the cable/connector will be used at elevated operating temperatures or experience frequent and wide temperature cycling effects, the cable/connector attachment can be strengthened by applying a RTV adhesive within the connector. A recommended adhesive is GE Company RTV-128. In most applications, use of RTV is unnecessary. The simplex latching connector is available in gray (HFBR-4503) or blue (HFBR-4513).

Duplex Connector HFBR-4506 — Duplex

Duplex connectors provide convenient duplex cable termination and are keyed to prevent incorrect connection. The duplex connector is compatible with dual combinations of identical Versatile Link components (e.g., two horizontal transmitters, two vertical receivers, a horizontal transmitter and a horizontal receiver, etc.). A duplex connector cannot connect to two different packages simultaneously. The duplex connector is an off-white color.

Feedthrough/Splice HFBR-4505/4515 — Adapter

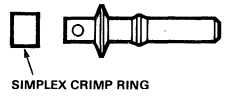
The HFBR-4505/4515 adapter mates two simplex connectors for panel/bulkhead feedthrough of plastic fiber cable. Maximum panel thickness is 4.1 mm (0.16 inch). This adapter can serve as a cable in-line splice using two simplex connectors. The colors of the adapters are gray (HFBR-4505) and blue (HFBR-4515). The adapter is not compatible with the duplex or simplex latching connectors.

Absolute Maximum Ratings

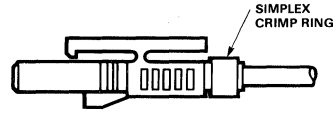
Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	+75	°C	
Operating Temperature	T_A	0	+70	°C	
Nut Torque HFBR-4505/4515	T_N		0.7	N-m	1
			100	OzF-in	

Notes:
1. Recommended nut torque is 0.57 N-m (80 OzF-in).

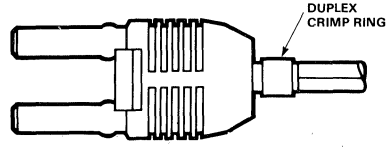
HFBR-4501 (GRAY)/4511 (BLUE) SIMPLEX CONNECTOR



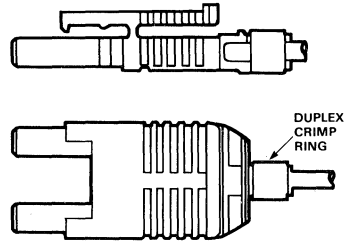
HFBR-4503 (GRAY)/4513 (BLUE) SIMPLEX LATCHING CONNECTOR



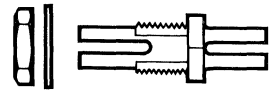
HFBR-4506 (PARCHMENT) DUPLEX CONNECTOR



HFBR-4516 (PARCHMENT) DUPLEX LATCHING CONNECTOR



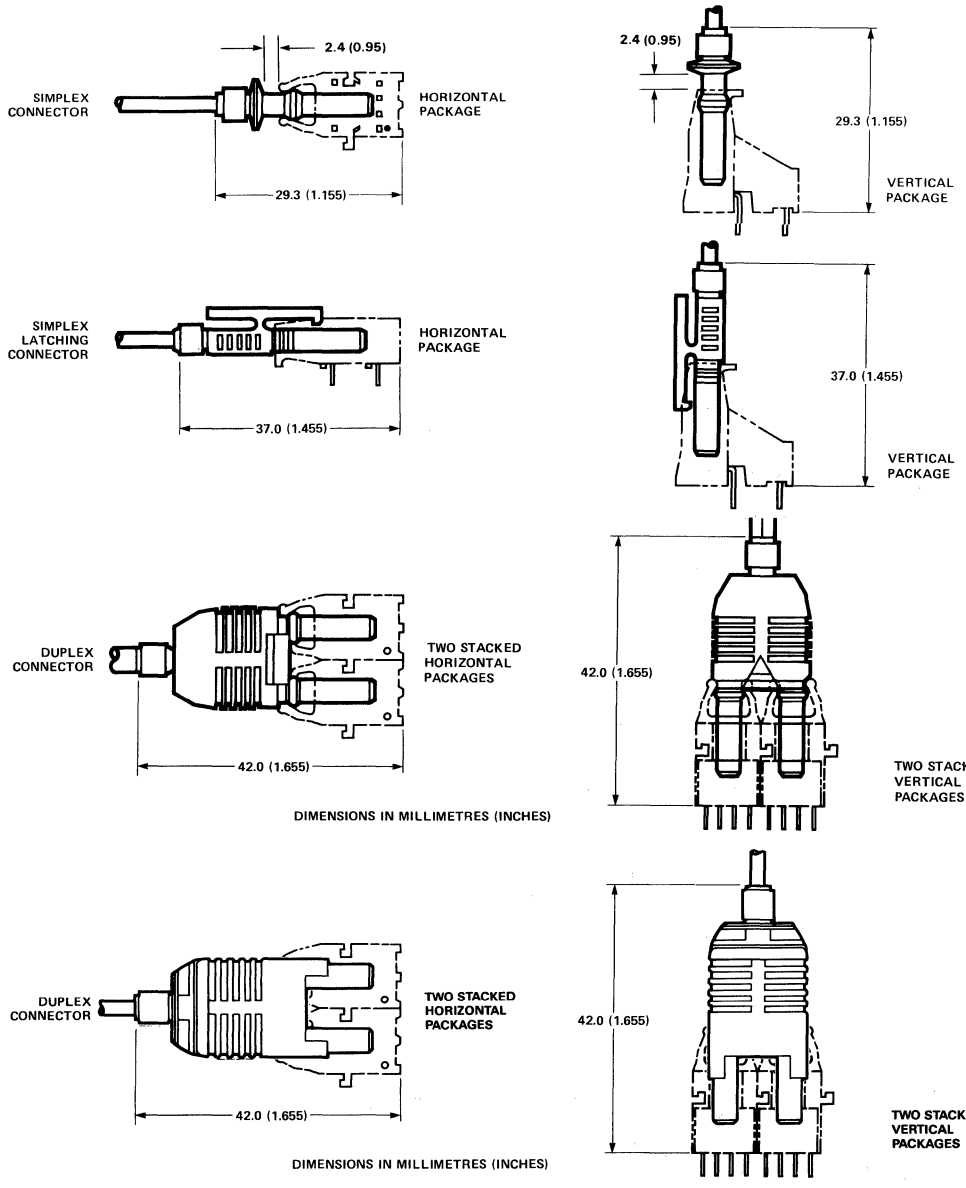
HFBR-4505 (GRAY)/4515 (BLUE) ADAPTER



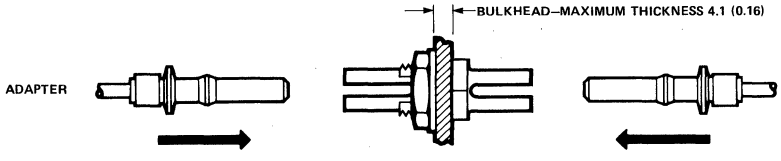
(USE WITH SIMPLEX CONNECTORS ONLY)

Connector Applications

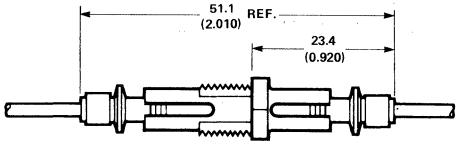
ATTACHMENT TO HEWLETT-PACKARD HFBR-152X/153X/252X/253X VERSATILE LINK FIBER OPTIC COMPONENTS



BULKHEAD FEEDTHROUGH OR PANEL MOUNTING FOR HFBR-4501/4511 SIMPLEX CONNECTORS



IN-LINE SPLICE FOR HFBR-35XX/36XX FIBER OPTIC CABLE WITH HFBR-4501/4511 SIMPLEX CONNECTORS



DIMENSIONS IN MILLIMETRES (INCHES)

Connector Mechanical/Optical Characteristics 25°C Unless Otherwise Specified.

Parameter	Part Number		Sym.	Min.	Typ.	Max.	Units	Ref.
Retention Force Connector to HFBR-152X 153X/ 252X/253X Modules	Simplex	HFBR-4501/4511	F_{R-C}	7	8		N	Note 4
	Simplex Latching	HFBR-4503/4513		47	80			
	Duplex	HFBR-4506		7	12			
	Duplex Latching	HFBR-4516		50	80			
Tensile Force Connector to Cable	Simplex	HFBR-4501/4511	F_T	8.5	22		N	Notes 3, 4
	Simplex Latching	HFBR-4503/4513		8.5	22			
	Duplex	HFBR-4506		14	35			
	Duplex Latching	HFBR-4516		14	35			
Adapter Connector to Connector Loss	HFBR-4505/4515 with HFBR-4501/4511		α_{CC}	0.7	1.5	2.8	dB	Notes 1, 5
Retention Force Connector to Adapter	HFBR-4505/4515 with HFBR-4501/4511		F_{R-B}	7	8		N	Note 4
Insertion Force Connector to HFBR-152X/153X/ 252X/253X Modules	Simplex	HFBR-4501/4511	F_I		8	12	N	Notes 2, 4
	Simplex Latching	HFBR-4503/4513			16	35		
	Duplex	HFBR-4506			13	46		
	Duplex Latching	HFBR-4516			22	51		

Notes:

1. Factory polish or field polish per recommended procedure.
2. No perceivable reduction in insertion force was observed after 2000 insertions. Destructive insertion force was typically at 178 N (40 lbs).
3. For applications where frequent temperature cycling over temperature extremes is expected please contact Hewlett-Packard for alternate connectoring techniques.
4. All mechanical forces were measured after units were stored at 70°C for 168 hours and returned to 25°C for one hour.
5. Minimum and maximum limits of α_{CC} are for 0°C to 70°C temperature range. Typical value of α_{CC} is at 25°C.

Connectoring

The following easy procedure describes how to make cable terminations. It is ideal for both field and factory installation. If a high volume connectoring technique is required please contact your Hewlett-Packard sales engineer for the recommended procedure and equipment.

Connectoring the cable is accomplished with the Hewlett-Packard HFBR-4593 Polishing Kit consisting of a Polishing Fixture, 600 grit abrasive paper and 3-μm pink lapping film (3M Company, OC3-14). No adhesive material is needed to secure the cable in the connector, and the connector can be used immediately after polishing. Improved connector to cable attachment can be achieved with the use of a RTV (GE Company, RTV-128) adhesive for frequent, extreme temperature cycling environments or for elevated temperature operation.

Connectors may be easily installed on the cable ends with readily available tools. Materials needed for the terminating procedure are:

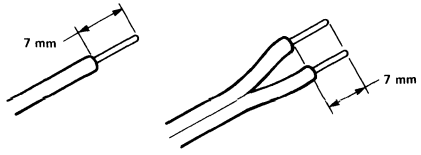
1) Hewlett-Packard Plastic Fiber Optic Cable
2) HFBR-4593 Polishing Kit
3) HFBR-4501/4503 Gray Simplex/Simplex Latching Connector and Silver Color Crimp Ring
4) HFBR-4511/4513 Blue Simplex/Simplex Latching Connector and Silver Color Crimp Ring
5) HFBR-4506 Parchment Duplex Connector and Duplex Crimp Ring
6) Industrial Razor Blade or Wire Cutters
7) 16 Gauge Latching Wire Strippers
8) Crimp Tool, HFBR-4597

Step 1

The zip cord structure of the duplex cable permits easy separation of the channels. The channels should be separated approximately 50 mm (2.0 in.) back from the ends to permit connectoring and polishing.

After cutting the cable to the desired length, strip off approximately 7 mm (0.3 in.) of the outer jacket with the 16 gauge wire strippers. Excess webbing on duplex cable may have to be trimmed to allow the simplex or simplex latching connector to slide over the cable.

When using the duplex connector and duplex cable, the separated duplex cable must be stripped to equal lengths on each cable. This allows easy and proper seating of the cable into the duplex connector.

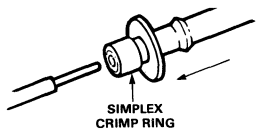


Step 2

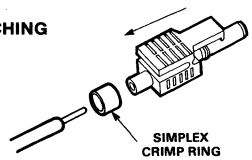
Place the crimp ring and connector over the end of the cable; the fiber should protrude about 3 mm (0.12 in.) through the end of the connector. Carefully position the ring so that it is entirely on the connector with the rim of the crimp ring flush with the connector, leaving a small space between the crimp ring and the flange. Then crimp the ring in place with the crimping tool. One crimp tool is used for all connector crimping requirements.

Note: *Place the gray connector on the cable end to be connected to the transmitter and the blue connector on the cable end to be connected to the receiver to maintain the color coding (both connectors are the same mechanically). For duplex connector and duplex cable application, align the color coded side of the cable with the appropriate ferrule of the duplex connector in order to match connections to the respective optical ports. The simplex connector crimp ring cannot be used with the duplex connector. The duplex connector crimp ring cannot be used with the simplex or simplex latching connectors. The simplex crimp has a dull lustre; the duplex ring is shiny and has a thinner wall.*

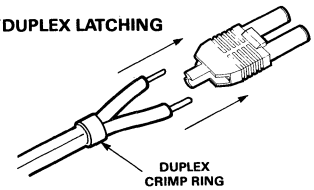
SIMPLEX



SIMPLEX LATCHING



DUPLEX/DUPLEX LATCHING



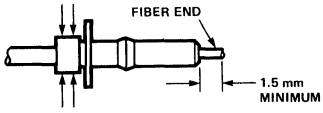
Step 3

Any excess fiber protuding from the connector end may be cut off; however, the trimmed fiber should extend at least 1.5 mm (0.06 in.) from the connector end.

Insert the connector fully into the polishing fixture with the trimmed fiber protruding from the bottom of the fixture. This plastic polishing fixture can be used to polish two simplex connectors or two simplex latching connectors simultaneously, or one duplex connector.

Note: *The four dots on the bottom of the polishing fixture are wear indicators. Replace the polishing fixture when any dot is no longer visible.*

Place the 600 grit abrasive paper on a flat smooth surface. Pressing down on the connector, polish the fiber and the connector using a figure eight pattern of strokes until the connector is flush with the bottom of the polishing fixture. Wipe the connector and fixture with a clean cloth or tissue.

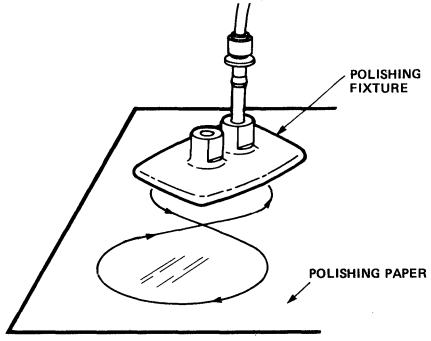


Step 4

Place the flush connector and polishing fixture on the dull side of the 3 micron pink lapping film and continue to polish the fiber and connector for approximately 25 strokes. The fiber end should be flat, smooth and clean.

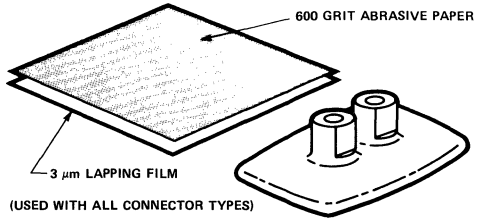
The cable is now ready for use.

Note: *Use of the pink lapping film fine polishing step results in approximately 2 dB improvement in coupling performance of either a transmitter-receiver link or a bulkhead/splice over 600 grit polish alone. This fine polish is comparable to Hewlett-Packard factory polish. The fine polishing step may be omitted where an extra 2 dB of optical power is not essential, as with short link lengths. Proper polishing of the tip of the fiber/connector face results in a tip diameter between 2.8 mm (0.110 in.) minimum and 3.2 mm (0.125 in.) maximum.*



For simultaneous multiple connector polishing techniques please contact Hewlett-Packard.

HFBR-4593 POLISHING KIT



Ordering Guide

TRANSMITTERS (T_X)/RECEIVERS (R_X) Pages 5-24/5-27

Versatile Link	Unit	Horizontal Modules	Vertical Modules
5 MBd High Performance	T_X	HFBR-2521	HFBR-2531
1 MBd High Performance	T_X	HFBR-2522	HFBR-2532
40 kBd Low Current/ Extended Distance	T_X	HFBR-2523	HFBR-2533
1 MBd Standard	T_X	HFBR-2524	HFBR-2534
5 MBd High Performance	R_X	HFBR-1521	HFBR-1531
1 MBd High Performance	R_X	HFBR-1522	HFBR-1532
40 kBd Low Current/ Extended Distance	R_X	HFBR-1523	HFBR-1533
1 MBd Standard	R_X	HFBR-1524	HFBR-1534

CONNECTORS Page 5-30

HFBR-4501	Gray Simplex Connector/Crimp Ring
HFBR-4511	Blue Simplex Connector/Crimp Ring
HFBR-4503	Gray Simplex Latching Connector with Crimp Ring
HFBR-4513	Blue Simplex Latching Connector with Crimp Ring
HFBR-4506	Parchment Duplex Connector with Crimp Ring
HFBR-4516	Parchment Duplex Latching Connector with Crimp Ring
HFBR-4505	Gray Adapter
HFBR-4515	Blue Adapter

EVALUATION KIT, HFBR-0501 **CONTENTS:**

HFBR-1524	Transmitter
HFBR-2524	Receiver
HFBR-4501	Gray Simplex Connector with Crimp Ring
HFBR-4506	Duplex Connector with Crimp Ring
—	5 metres of Connectored Simplex Cable with Blue Simplex and Gray Simplex Latching Connectors
HFBR-4513	Blue Simplex Latching Connector with Crimp Ring
HFBR-4505	Gray Adapter
—	Polishing Tool and 600 grit paper
HFBR-0501	Data Sheet and Brochure

ACCESSORIES

HFBR-4522	500 Port Plugs
HFBR-4525	1000 Simplex Crimp Rings
HFBR-4526	500 Duplex Crimp Rings
HFBR-4593	Polishing Kit (one polishing tool, two pieces 600 grit abrasive paper, and two pieces 3-μm lapping film).
HFBR-4597	Crimping Tool

A Note About Ordering Cable

Four steps are required to determine the proper part number for a desired cable.

Step 1 Select Standard or Improved Cable.

As explained on page 5-29, two levels of attenuation are available: Standard and Improved.

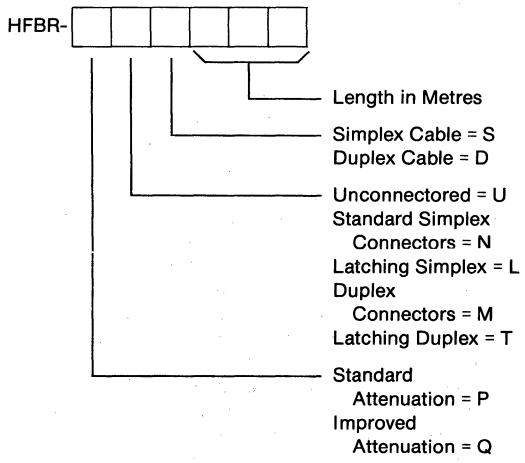
Step 2 Select the connector style.

Connector styles are described on page 5-30.

Step 3 Select Simplex or Duplex.

Step 4 Determine the cable length.

To determine the appropriate part number, select the letter corresponding to your selection and fill in the following:



For example:

HFBR-PUD500 is a Standard Attenuation, Unconnectored, Duplex, 500 metre cable.

HFBR-QLS001 is an Improved Attenuation, Latching Simplex Connectored, Simplex, 1 metre cable.

HFBR-PMD010 is a Standard Attenuation, Standard Duplex Connectored, Duplex, 10 metre cable.

HFBR-PND100 is a Standard Attenuation, Standard Simplex Connectored, Duplex, 100 metre cable.

Note: 0.1 metre Standard Attenuation Simplex lengths are available; 0.5 metre Standard Attenuation Simplex and Duplex lengths are also available. The lengths are ordered as HFBR-xxx1DM or HFBR-xxx5DM.

ATTENTION: Pre-connectored simplex cables have oppositely colored (GRAY vs. BLUE) connectors at the opposite ends of the same fiber; although oppositely colored, the connectors are mechanically identical. For duplex cables with simplex connectors, the same rule applies to each fiber; also, the side-by-side fibers at each end of the cable have oppositely colored connectors. For duplex cables with duplex connectors similar rules apply, so the connectors at opposite ends are oppositely keyed relative to the marked fiber in a duplex cable.

HEWLETT PACKARD

Low Cost, Miniature Fiber Optic Components with ST* and SMA Ports

Technical Data

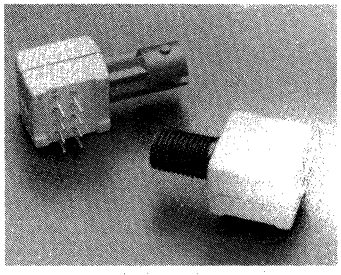
HFBR-0400 ST* and SMA Series

Features

- Low Cost Transmitters and Receivers
- Choice of ST or SMA Ports
- 820 Nanometre Wavelength Technology
- Signal Rates up to 150 Megabaud
- Link Distances up to 4 Kilometres
- Specified with 50/125 µm, 62.5/125 µm, 100/140µm, and 200 µm PCS Fiber Sizes
- Repeatable ST Connections within 0.2 dB Typical
- Unique Optical Port Design for Efficient Coupling
- Auto-Insertable and Wave Solderable
- No Board Mounting Hardware Required
- Wide Operating Temperature Range –40°C to 85°C
- AlGaAs Emitters 100% Burn-In Ensures High Reliability
- Demonstrated Reliability @ 40°C Exceeds 4 Million Hours MTBF

Applications

- Local Area Networks
- Computer to Peripheral Links
- Computer Monitor Links
- Digital Cross Connect Links
- Central Office Switch Links
- PBX Links
- Video Links
- Modems and Multiplexers
- Suitable for Tempest Systems



Description

The HFBR-0400 Series of components is designed to provide cost effective, high performance fiber optic communication links for information systems and industrial applications with link distances of up to 4 kilometres. With the latest addition to the HFBR-0400 series, the 125 MHz analog receiver, data rates of up to 150 megabaud are attainable.

Transmitters and receivers are directly compatible with popular "industry-standard" connectors: ST and SMA. They are completely specified with multiple fiber sizes; including 50/125 µm, 62.5/125 µm, 100/140 µm, and 200 µm.

Complete evaluation kits are available for ST and SMA product offerings; including transmitter, receiver, connectored cable, and technical literature. In addition, ST and SMA connectored cables are available.

*ST is a registered trademark of AT&T Lightguide Cable Connectors.

HFBR-0400 Series Selection Guide

Description	SMA Series[1]	SMA Conductive Port[1]	ST Series[2]	ST Threaded Port[2]	ST Threaded, Conductive[2]
Standard Transmitter	HFBR-1402	—	HFBR-1412	HFBR-1412T	—
High Power Transmitter	HFBR-1404	—	HFBR-1414	HFBR1414T	—
5 MBd TTL Receiver	HFBR-2402	HFBR-2402C	HFBR-2412	HFBR-2412T	HFBR-2412TC
25 MHz Analog Receiver	HFBR-2404	HFBR-2404C	HFBR-2414	HFBR-2414T	HFBR-2414TC
125 MHz Analog Receiver	HFBR-2406	HFBR-2406C	HFBR-2416	HFBR-2416T	HFBR-2416TC
Evaluation Kit (5 MBd)	HFBR-0400	—	HFBR-0410	—	—

Notes:
1. These products are also available unhoused. HFBR-xx3x references port product with bent leads and HFBR-xx5x references port product with straight leads.
2. These products are also available unhoused. HFBR-xx4x references port product with bent leads and HFBR-xx6x references port product with straight leads.

Literature Guide

Title	Description
HFBR-0400 Series Reliability Data	Transmitter & Receiver Reliability Data
Application Bulletin 73	Low-Cost Fiber Optic Transmitter & Receiver Interface Circuits
Application Bulletin 78	Low-Cost Fiber Optic Links for Digital Applications up to 150 MBd
Application Note 1038	Low-Cost Components for IEEE 802.3 Fiber Optic Inter-Repeater Links
Technical Brief 105	ST Connector/Cable Guide
Technical Brief 101	Fiber Optic SMA Connector Technology
HFBR-0400 ST and SMA Series	Transmitter & Receiver Specifications

Contact your local HP components sales office to obtain these publications.

Package Information

All HFBR-0400 Series transmitters and receivers are housed in a low-cost, dual-in-line package that is made of high strength, heat resistant, chemically resistant, and UL V-O flame retardant plastic. The transmitters are easily identified by the light grey color connector port. The receivers are easily identified by the dark grey color connector port. (Black color for conductive port.) The package is designed for auto-insertion and wave soldering so it is ideal for high volume production applications.

Handling and Design Information

When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean.

Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path.

Clean compressed air often is sufficient to remove particles of dirt; methanol on a cotton swab also works well.

CAUTION: The small junction sizes inherent to the design of these components increases the components' susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of these components to prevent damage and/or degradation which may be induced by ESD.

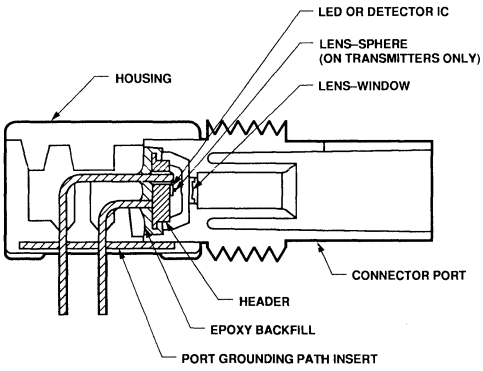


Figure 1. HFBR-0400 ST Series Cross-Sectional View

Link Design Considerations

The HFBR-14XX transmitter and the HFBR-24XX receiver can be used to design fiber optic data links that operate with 50/125 µm, 62.5/125 µm, 100/140 µm and 200 µm PCS fiber cables.

The HFBR-14X2 standard transmitter and the HFBR-24X2 receiver are suitable for systems requiring up to 5 MBd and 2 Km. For higher data rate or longer distance, the HFBR-14X4 high power transmitter and/or the HFBR-24X4 receiver should be considered.

5 MBd Logic Link Design

The HFBR-14X4/24X2 Logic Link is guaranteed to work with 62.5/125 µm fiber optic cable over the entire range of 0 to 1200 metres at a data rate of dc to 5 MBd, with arbitrary data format and typically less than 25% pulse width distortion, when the transmitter is driven with I_F = 30 mA, R_L = 115 Ohm as shown in Figure 2. If it is desired to economize on power or achieve lower pulse distortion, then a lower drive current (I_F) may be used. The following example will illustrate the technique for optimizing I_F

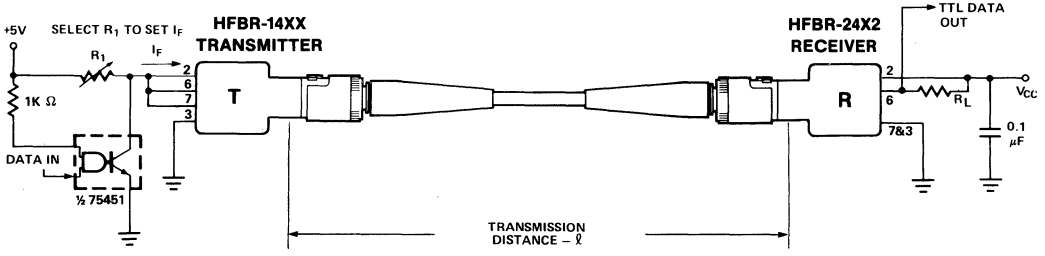
Example: Maximum distance required = 400 metres. From Figure 3 the drive current should be 15 mA. From the transmitter data V_F = 1.5 V (max.) as shown in Figure 9.

$$R_1 = \frac{V_{CC} - V_F}{I_F} = \frac{5\text{ V} - 1.5\text{ V}}{15\text{ mA}}$$

$$= 233 \text{ ohm}$$

The curves in Figures 3, 4, and 5 are constructed assuming no in-line splice or any additional system loss. Should the link consist of any in-line splices, these curves can still be used to calculate link limits provided they are shifted by the additional system loss in dB. For example, with 20 mA of transmitter drive current, 1.6 km link distance is achievable. With 2 dB of additional system loss, 1.2 km link distance is achievable.

5 MBd Link Performance



NOTE:
IT IS ESSENTIAL THAT A BYPASS CAPACITOR (0.01 µF TO 0.1 µF CERAMIC) BE CONNECTED FROM PIN 2 TO PIN 7 OF THE RECEIVER. TOTAL LEAD LENGTH BETWEEN BOTH ENDS OF THE CAPACITOR AND THE PINS SHOULD NOT EXCEED 20 mm.

Figure 2. Typical Circuit Configuration

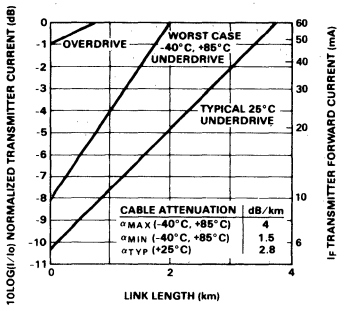


Figure 3. HFBR-1414/HFBR-2412 Link Design Limits with 62.5/125 µm Cable

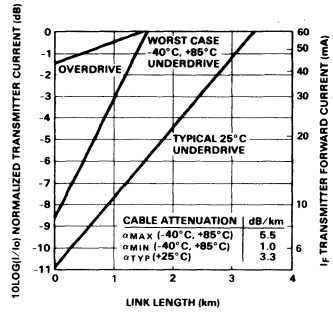


Figure 4. HFBR-14X2/HFBR-24X2 Link Design Limits with 100/140 µm Cable

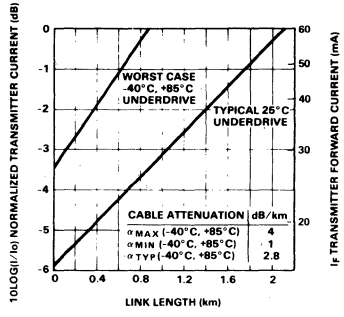


Figure 5. HFBR-14X4/HFBR-24X2 Link Design Limits with 50/125 µm Cable

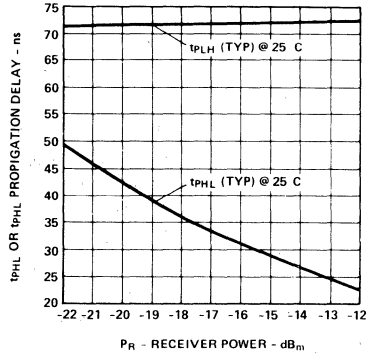


Figure 6. Propagation Delay through System with One Metre of Cable

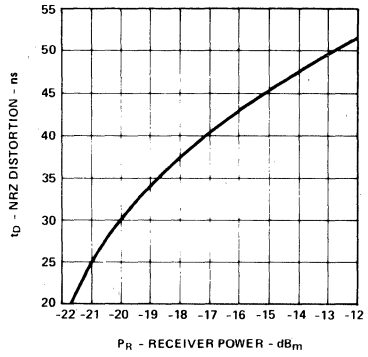


Figure 7. Typical Distortion of NRZ EYE-pattern with Pseudo Random Data at 5 Mb/s (see Note 2)

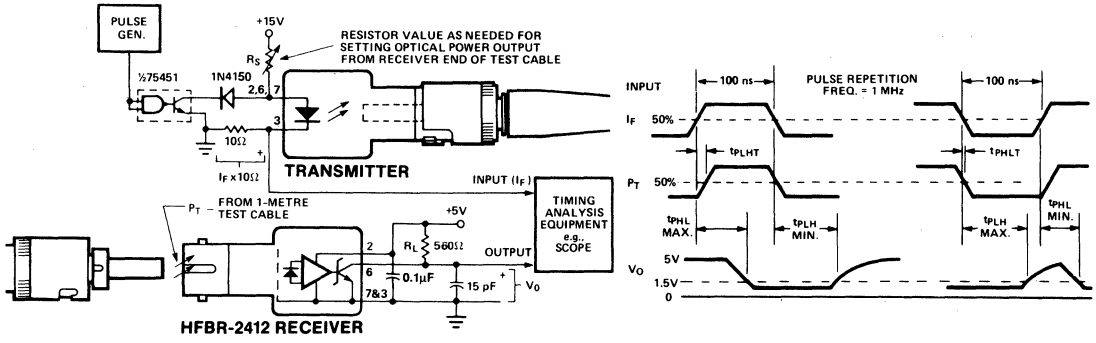


Figure 8. System Propagation Delay Test Circuit and Waveform Timing Definitions

Logic Link Design up to 35 MBd

For data rates up to 35 MBd, or longer distance, the HFBR-14X4 high power transmitter and/or the HFBR-24X4 receiver can be used. The table on the following page summarizes the typical performance of a 30 MBd link. For more details, please refer to HP Application Bulletin 73 (5954-8415). If circuit design assistance is needed, please contact your local Hewlett-Packard Components Field Sales Engineer.

Logic Link Design up to 150 MBd

For data rates of up to 150 MBd, the HFBR-14XX transmitters and the HFBR-24X6 receiver can be used. The table on the following page summarizes the typical performance of a 100 MBd link. For more details, please refer to HP Application Bulletin 78. If circuit design assistance is needed, please contact your local Hewlett-Packard Components Field Sales Engineer.

Cable Selection

The HFBR-0400 Series can be used with fiber sizes such as 50/125 μm, 62.5/125 μm, 100/140 μm, 200 μm PCS, and 1000 μm Plastic. Before selecting a fiber type, several parameters need to be carefully evaluated.

The bandwidth and attenuation (dB/km) of the selected fiber, in conjunction with the amount of optical power coupled into it will determine the achievable link length. The parameters that will significantly affect the optical power coupled into the fiber are as follows:

a. Fiber Core Diameter. As the core diameter is increased, the optical power coupled increases, leveling off at about 250 μm diameter.

b. Numerical Aperture (NA). As the NA is increased, the optical power coupled increases, leveling off at an NA of about 0.34.

In addition to the optical parameters, the environmental performance of the selected fiber/cable must be evaluated. Finally, the ease of installing connectors on the selected fiber/cable must be considered.

ST connectored fiber optic cable is available from a variety of manufacturers and distributors, including those listed in HP Technical Brief 105; ST Connector/Cable Guide. For ST Evaluation Cables from Hewlett-Packard, please refer to page 12.

ST Connectors

ST connections are locking, vibration resistant, low loss and very repeatable. The HFBR-0400 ST Series Transmitters and Receivers are compatible with AT&T's ST and ST-II Connectors and bayonet connectors from a variety of manufacturers and distributors. For more information about ST Connectors, please refer to Technical Brief 105; ST Connector/Cable Guide.

SMA Connectors

The HFBR-0400 SMA Series Transmitters and Receivers are compatible with SMA type connectors. Depending upon the type of SMA connector that is chosen, price, performance, and reliability will vary. For more information about SMA connectors, please refer to Technical Brief 101; Fiber Optic SMA Connector Technology.

5 MBd Link Performance –40°C to +85°C unless otherwise specified

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions	Reference
Optical Power Budget w/50/125 µm Fiber	OPB_{50}	4.2	9.6		dB	HFBR-14X4/24X2 w/50/125 µm, NA = 0.2	
Optical Power Budget w/62.5/125 µm Fiber	$OPB_{62.5}$	8.0	15.0		dB	HFBR-14X4/24X2 w/62.5/125 µm, NA = 0.27	
Optical Power Budget w/100/140 µm Fiber	OPB_{100}	8.5	15.0		dB	HFBR-14X2/24X2 w/100/140 µm, NA = 0.30	
Optical Power Budget w/200 µm PCS Fiber	OPB_{200}	13	20.5		dB	HFBR-14X2/24X2 w/200 µm PCS, NA = 0.40	
Data Rate Synchronous		dc		5	MBaud		Note 2
Asynchronous		dc		2.5	MBaud		Note 2, Fig. 7
Propagation Delay LOW to HIGH	t_{PLH}		72		nsec	T_A = 25°C P_R = –21 dBm Peak	Fig. 6, 7, 8
Propagation Delay HIGH to LOW	t_{PHL}		46		nsec		
System Pulse Width Distortion	t_{PLH}-t_{PHL}		26		nsec	= 1.0 metre	
Bit Error Rate	BER			10^{-9}		Data Rate ≤ 5 MBaud P_R > –24 dBm Peak	

Notes:

1. Typical data at T = 25°C, V_{CC} = 5.0 V dc, P_R = 27.0 dBm.
2. Synchronous data rate limit is based on these assumptions: a) 50% duty factor modulation, e.g., Manchester I or BiPhase Manchester II; b) continuous data; c) PLL Phase Lock Loop demodulation; d) TTL threshold.

   Asynchronous data rate limit is based on these assumptions: a) NRZ data; b) arbitrary timing—no duty factor restriction; c) TTL threshold.

   The EYE pattern describes the timing range within which there is no uncertainty of the logic state, relative to a specific threshold, due to either noise or intersymbol prop. delay effects.

30 MBd Link Performance (see Application Bulletin 73 for details)

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions
Optical Power Budget w/50/125 μm Fiber	OPB_{50}		9.7		dB	HFBR-14X4/24X4 w/50/125 μm, NA = 0.2
Optical Power Budget w/62.5/125 μm Fiber	$OPB_{62.5}$		13.5		dB	HFBR-14X4/24X4 w/62.5/125 μm, NA = 0.27
Optical Power Budget w/100/140 μm Fiber	OPB_{100}		13.5		dB	HFBR-14X2/24X4 w/100/140 μm, NA = 0.30
Optical Power Budget w/200 μm PCS Fiber	OPB_{200}		19		dB	HFBR-14X4/24X4 w/200 μm PCS, NA = 0.40
Data Format NRZ		dc	30		MBaud	Reference AB 73 for circuit details, Note 2, 3
Propagation Delay LOW to HIGH	t_{PLH}		12		nsec	T_A = 25°C P_R = –13 dBm Peak
Propagation Delay HIGH to LOW	t_{PHL}		8		nsec	
System Pulse Width Distortion	t_{PLH}-t_{PHL}		4		nsec	= 1.0 metre
Bit Error Rate	BER			10^{-9}		Data Rate ≤ 30 MBaud P_R > –25.5 dBm Peak

Notes:
1. Typical data at T = 25°C, V_{CC} = 5.0 V dc.
2. This circuit utilizes the LT1016 comparator from Linear Technology Corporation. If operated at 5 MBd, an additional 4.5 dB of optical power budget can be obtained.
3. If HFBR-24X4 is replaced with the HFBR-24X6, an additional 5.5 dB of optical power budget can be obtained at 30 MHz NRZ.

100 MBd Link Performance (see Application Bulletin 78 for details)

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions
Optical Power Budget w/50/125 μm Fiber	OPB_{50}		14.7		dB	HFBR-14X4/24X6 w/50/125 μm, NA = 0.2
Optical Power Budget w/62.5/125 μm Fiber	$OPB_{62.5}$		19		dB	HFBR-14X4/24X6 w/62.5/125 μm, NA = 0.27
Optical Power Budget w/100/140 μm Fiber	OPB_{100}		19		dB	HFBR-14X2/24X6 w/100/140 μm, NA = 0.30
Optical Power Budget w/200 μm PCS Fiber	OPB_{200}		24		dB	HFBR-14X2/24X6 w/200 μm PCS, NA = 0.40
Data Format 20% to 80% Duty Factor			100		MBaud	Reference AB 78 for circuit details, Note 2
Propagation Delay LOW to HIGH	t_{PLH}		5		nsec	T_A = 25°C P_R = –7 dBm Peak
Propagation Delay HIGH to LOW	t_{PHL}		4		nsec	
System Pulse Width Distortion	t_{PLH}-t_{PHL}		1		nsec	= 1.0 metre
Bit Error Rate	BER			10^{-9}		Data Rate ≤ 100 MBaud P_R > –31 dBm Peak

Notes:
1. Typical data at T_A = 25°C, V_{EE} = –5.2 V dc, V_{CC} = 0 (ECL).
2. The optical power budgets at 100 MBd were measured with an unrestricted receiver, without a Nyquist filter. A 10116 ECL line receiver was used in the receiver digitizing circuit. If unnecessary bandwidth is eliminated by low-pass filtering, an additional 2 dB of link budget is attainable at 30 MBd.

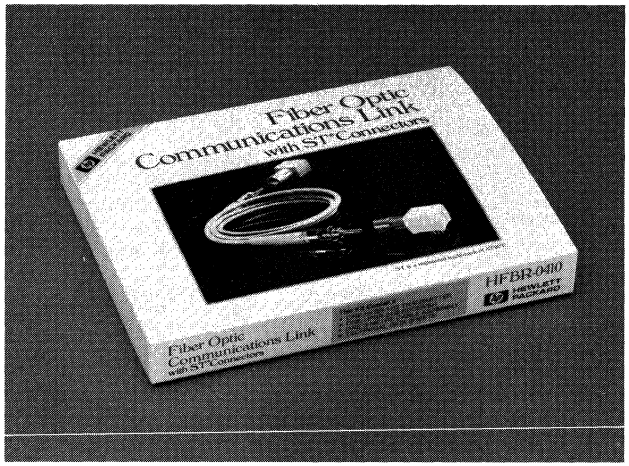
ST Evaluation Kit

The HFBR-0410 kit is a simple and inexpensive way to demonstrate the performance of Hewlett-Packard's HFBR-0400 ST Series transmitters and receivers.

The HFBR-0410 ST Evaluation Kit contains the following items:

- One HFBR-1412 transmitter
- One HFBR-2412 five megabaud TTL receiver
- Three metres of ST connectored 62.5/125 μm fiber optic cable with low cost plastic ferrules
- HFBR-0400 Series data sheets
- HP Application Bulletin 73
- ST connector and cable data sheets

To order an ST Evaluation Kit, please specify HFBR-0410, Quantity 1.



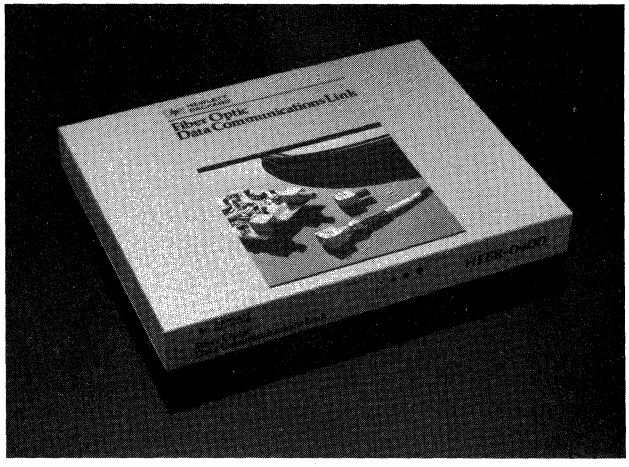
SMA Evaluation Kit

The HFBR-0400 kit is a simple and inexpensive way to demonstrate the performance of Hewlett-Packard's HFBR-0400 SMA Series transmitters and receivers.

The HFBR-0400 SMA Evaluation Kit contains the following items:

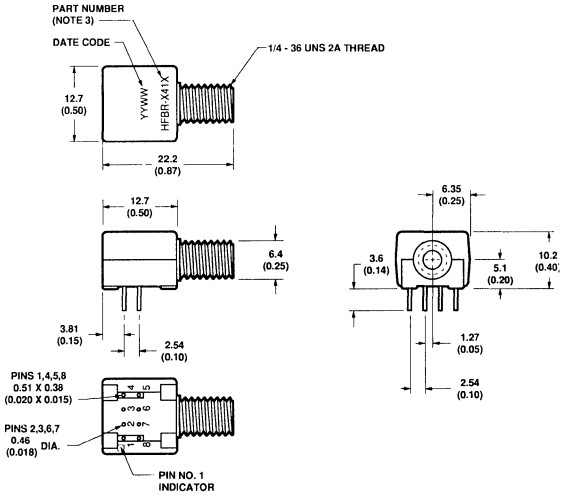
- One HFBR-1402 transmitter
- One HFBR-2402 five megabaud TTL receiver
- Two metres of SMA connectored 1000 μm plastic core fiber optic cable
- HFBR-0400 Series data sheets
- HP Application Bulletin 73

To order an SMA Evaluation Kit, please specify HFBR-0400, Quantity 1.

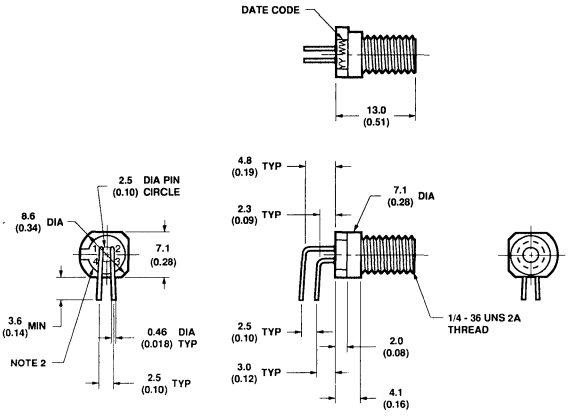


Mechanical Dimensions
HFBR-0400 SMA Series

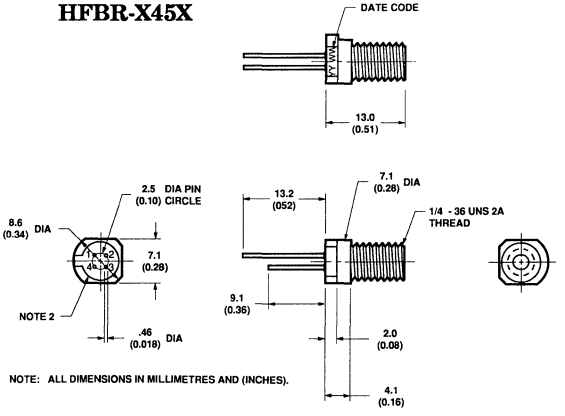
HFBR-X40X



HFBR-X43X



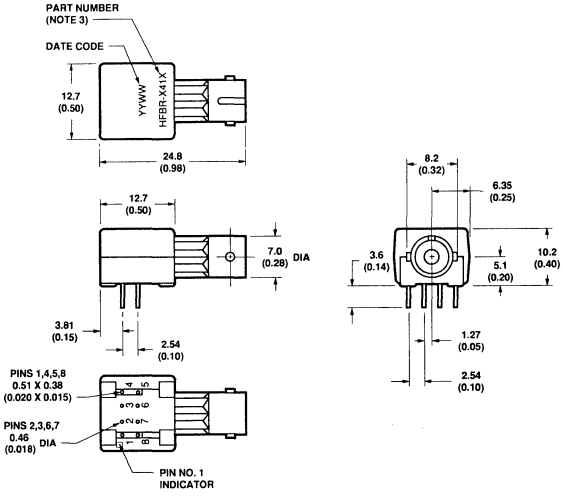
HFBR-X45X



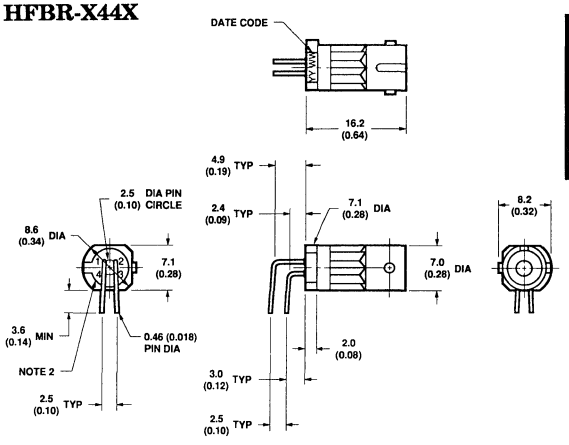
NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES).

Mechanical Dimensions
HFBR-0400 ST Series

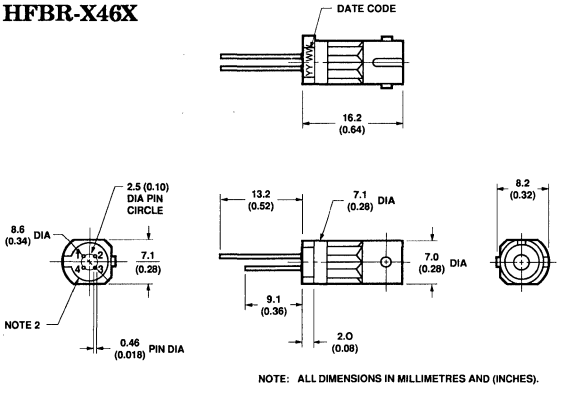
HFBR-X41X



HFBR-X44X



HFBR-X46X

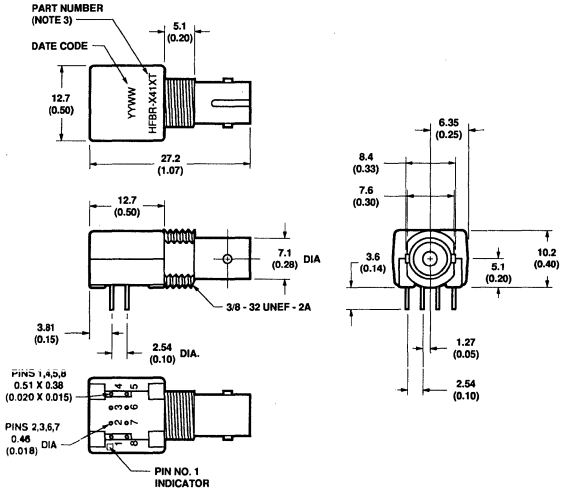


NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES).

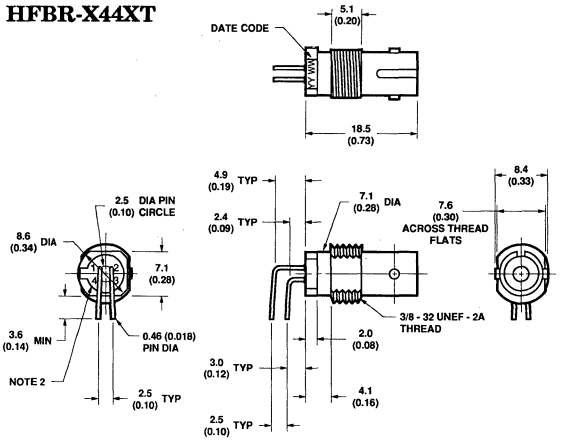
FIBER OPTICS

Mechanical Dimensions
HFBR-0400T Threaded
ST Series

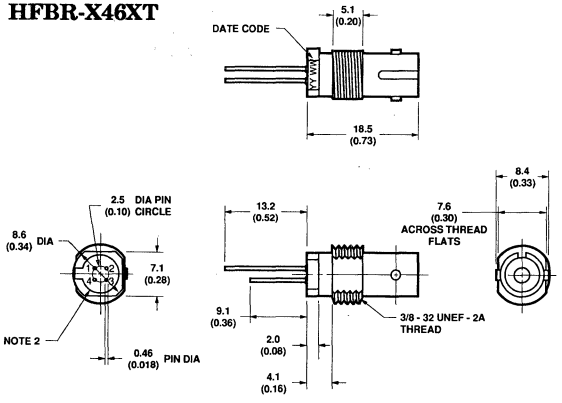
HFBR-X41XT



HFBR-X44XT

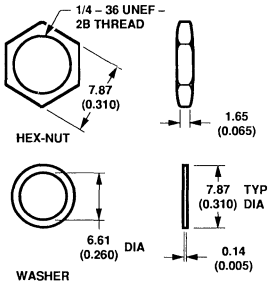


HFBR-X46XT

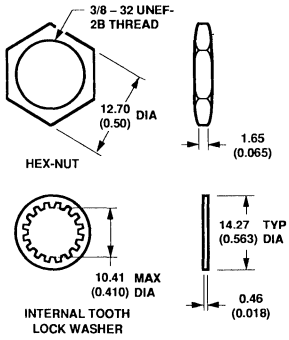


Panel Mounting Hardware

HFBR-4401



HFBR-4411



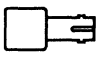
(Each HFBR-4401 and HFBR-4411 kit consists of 100 nuts and 100 washers.)

Recommended Chemicals for Cleaning/Degreasing HFBR-0400 Products

Alcohols (methyl, isopropyl, isobutyl)
Aliphatics (hexane, heptane)
Other (soap solution, naphtha)

(Do not use partially halogenated hydrocarbons (such as 1.1.1 trichloroethane), ketones (such as MEK), acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride, or N-methylpyrolldone. Also, HP does not recommend the use of cleaners that use halogenated hydrocarbons because of their potential environmental harm.)

Notes:
1. All dimensions are in millimetres and (inches).
2. Unhoused products are distinguished by the color of the backfill epoxy used in construction.
   white - HFBR-14X2
   red - HFBR-14X4
   black - HFBR-24X2
   green - HFBR-24X4
   blue - HFBR-24X6
3. Color coding; part marking is in red for HFBR-14XX transmitters and black for HFBR-24XX receivers. The ports are shaded as shown below.



Transmitters

Receivers

Conductive Port Receivers

HEWLETT PACKARD

High Speed Low Cost Fiber Optic Transmitter

Technical Data

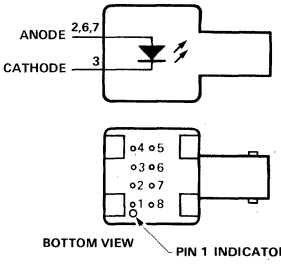
HFBR-14X2 and HFBR-14X4 Series

Description

The HFBR-14XX fiber optic transmitter contains an 820 nm GaAlAs emitter capable of efficiently launching optical power into four different optical fiber sizes: 50/125 µm, 62.5/125 µm, 100/140 µm, and 200 µm PCS. This allows the designer flexibility in choosing the fiber size. The HFBR-14XX is designed to operate with the Hewlett-Packard HFBR-24XX fiber optic receivers.

The HFBR-14XX transmitter's high coupling efficiency allows the emitter to be driven at low current levels resulting in low power consumption and increased reliability of the transmitter. The HFBR-14X4 high power transmitter is optimized for small size fiber and typically can launch –15.8 dBm optical power @ 60 mA into 50/125 µm fiber and –12 dBm into 62.5/125 µm fiber. The HFBR-14X2 standard transmitter typically can couple –11.5 dBm of optical power @ 60 mA into 100/140 µm fiber cable. It is ideal for large size fiber such as 100/140 µm. The high power level is useful for systems where star couplers, taps, or inline connectors create large fixed losses.

Housed Product



PIN	FUNCTION
1†	N.C.
2	ANODE
3*	CATHODE
4†	N.C.
5†	N.C.
6	ANODE
7*	ANODE
8†	N.C.

*PINS 2,6 AND 7 ARE ELECTRICALLY CONNECTED TO HEADER

†PINS 1, 4, 5, AND 8 ARE ELECTRICALLY CONNECTED

Unhoused Product

BOTTOM VIEW

PIN	FUNCTION
1	ANODE
2	CATHODE
3	ANODE
4	ANODE

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–55	+85	°C	
Operating Temperature		T_A	–40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	
	Time			10	sec	
Forward Input Current	Peak	I_{FPK}		200	mA	Note 1
	DC	I_{FDC}		100	mA	
Reverse Input Voltage		V_{BR}		1.8	V	

Consistent coupling efficiency is assured by the double-lens optical system (Figure 1). Power coupled into any of the three fiber types varies less than 5 dB from part to part at a given drive current and temperature. The benefit of this is reduced dynamic range requirements on the receiver.

CAUTION: The small junction sizes inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Electrical / Optical Specifications –40°C to +85°C unless otherwise specified.

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Reference
Forward Voltage	V_F	1.48	1.70	2.09	V	I_F = 60 mA	Figure 9
			1.84			I_F = 100 mA	
Forward Voltage Temperature Coefficient	V_F/T		–0.22		mV/°C	I_F = 60 mA	Figure 9
			–0.18			I_F = 100 mA	
Reverse Input Voltage	V_{BR}	1.8	3.8		V	I_R = 100 µA	
Peak Emission Wavelength	λ_P	792	820	852	nm		Figure 12
Full Width Half Maximum	FWHM		45	75	nm		Figure 12
Diode Capacitance	C_T		55		pF	V = 0, f = 1 MHz	
Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		–0.006		dB/°C	I = 60 mA	
			–0.010			I = 100 mA	
Thermal Resistance	θ_{JA}		260		°C/W		Notes 3, 8
Numerical Aperture (HFBR – 14X4)	NA_{14X4}		0.31				
Numerical Aperture (HFBR – 14X2)	NA_{14X2}		0.49				
Optical Port Diameter (HFBR – 14X4)	D_{14X4}		150		µm		Note 4
Optical Port Diameter (HFBR – 14X2)	D_{14X2}		290		µm		Note 4

Electrical / Optical Specifications –40°C to +85°C unless otherwise specified

HFBR-14X4 Peak Output Power Measured Out of 1m of Cable

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions		Reference
50/125 µm Fiber Cable NA = 0.20	$P_{T_{50}}$	–18.8	–15.8	–13.8	dBm	T_A = 25°C	I_F = 60 mA	
		–19.8		–12.8				
		–17.3	–13.8	–11.4		T_A = 25°C	I_F = 100 mA	
		–18.9		–10.8				
62.5/125 µm Fiber Cable NA = 0.275	$P_{T_{62}}$	–15.0	–12.0	–10.0	dBm	T_A = 25°C	I_F = 60 mA	
		–16.0		–9.0				
		–13.5	–10.0	–7.6		T_A = 25°C	I_F = 100 mA	
		–15.1		–7.0				
100/140 µm Fiber Cable NA = 0.30	$P_{T_{100}}$	–9.5	–6.5	–4.5	dBm	T_A = 25°C	I_F = 60 mA	Notes 5, 6, 9
		–10.5		–3.5				
		–8.0	–4.5	–2.1		T_A = 25°C	I_F = 100 mA	
		–9.6		–1.5				
200 µm PCS Fiber Cable NA = 0.40	$P_{T_{200}}$	–4.5	–3.0	+1.5	dBm	T_A = 25°C	I_F = 60 mA	
		–5.5		+2.5				
		–3.0	–1.0	+3.9		T_A = 25°C	I_F = 100 mA	
		–4.6		+4.5				

HFBR-14X2 Peak Output Power Measured Out of 1m of Cable

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions		Reference
50/125 µm Fiber Cable NA = 0.20	$P_{T_{50}}$	–21.8	–18.8	–16.8	dBm	T_A = 25°C	I_F = 60 mA	
		–22.8		–15.8				
		–20.3	–16.8	–14.4		T_A = 25°C	I_F = 100 mA	
		–21.9		–13.8				
62.5/125 µm Fiber Cable NA = 0.275	$P_{T_{62}}$	–19.0	–16.0	–14.0	dBm	T_A = 25°C	I_F = 60 mA	
		–20.0		–13.0				
		–17.5	–14.0	–11.6		T_A = 25°C	I_F = 100 mA	
		–19.1		–11.0				
100/140 µm Fiber Cable NA = 0.30	$P_{T_{100}}$	–15.0	–12.0	–10.0	dBm	T_A = 25°C	I_F = 60 mA	Notes 5, 6, 9
		–16.0		–9.0				
		–13.5	–10.0	–7.6		T_A = 25°C	I_F = 100 mA	
		–15.1		–7.0				
200 µm PCS Fiber Cable NA = 0.40	$P_{T_{200}}$	–10.0	–6.5	–4.0	dBm	T_A = 25°C	I_F = 60 mA	
		–11.0		–3.0				
		–8.5	–4.5	–1.6		T_A = 25°C	I_F = 100 mA	
		–10.1		–1.0				

WARNING: Obbserving the transmitter output power under magnification may cause injury to the eye. When viewed with the unaided eye, the infrared output is radiologically safe. However, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Reference
Rise Time, Fall Time (10% to 90%)	t_r, t_f		4.0	6.5	nsec	I_F = 60 mA No Pre-bias	Note 7, Figure 13
Rise Time, Fall Time (10% to 90%)	t_r, t_f		3.0		nsec	I_F = 10 to 100 mA	Note 7, Figure 11
Pulse Width Distortion	PWD		0.5		nsec		Figure 11

Notes:
1. For I_{FPK} > 100 mA, the time duration should not exceed 2 ns.
2. Typical data at T_A = 25°C.
3. Thermal resistance is measured with the transmitter coupled to a connector assembly and mounted on a printed circuit board.
4. D_T is measured at the plane of the fiber face and defines a diameter where the optical power density is within 10 dB of the maximum.
5. P_T is measured with a large area detector at the end of 1 metre of mode stripped cable, with an ST* precision ceramic ferrule (MIL-STD-83522/13) for HFBR-1412/1414, and with an SMA 905 precision ceramic ferrule for HFBR-1402/1404. This approximates a standard test connector.
6. When changing μW to dBm, the optical power is referenced to 1 mW (1000 μW). Optical Power P (dBm) = 10 log P (μW)/ 1000 μW.
7. Pre-bias is recommended if signal rate > 10 MBd, see recommended drive circuit in Figure 11.
8. Pins 2, 6 and 7 are welded to the anode header connection to minimize the thermal resistance from junction to ambient. To further reduce the thermal resistance, the anode trace should be made as large as is consistent with good RF circuit design.
9. Fiber NA is measured at the end of 2 metres of mode stripped fiber, using the far-field pattern. NA is defined as the sine of the half angle, determined at 5% of the peak intensity point. When using other manufacturer's fiber cable, results will vary due to differing NA values and specification methods.

Recommended Drive Circuits

The circuit used to supply current to the LED transmitter can significantly influence the optical switching characteristics of the LED. The optical rise/fall times and propagations delays can be improved by using certain circuit techniques.

The LED drive circuit shown in Figure 11 uses current-peaking to reduce the typical rise/fall times of the LED and a small pre-bias voltage to minimize propagation delay differences that cause pulse-width distortion. The circuit will typically produce rise/fall times of 3 ns, and a total jitter including pulse-width distortion of less than 2 ns. This circuit is recommended for applications requiring low edge jitter or high-speed data transmission at signal rates of up to 125 MBd. Component values for this circuit can be calculated for different LED drive currents using the equations shown below.

For additional details about LED drive circuits, the reader is encouraged to read Hewlett-Packard Application Bulletin 78 and Application Note 1038.

$$R_y\,(\Omega) = \frac{(V_{CC} - V_F) + 3.97\,(V_{CC} - V_F - 1.6\ V)}{I_{F_{ON}}\,(A)}$$

$$R_{x_1}\,(\Omega) = \frac{1}{2}\left(\frac{R_y}{3.97}\right)$$

$$R_{EQ_2}\,(\Omega) = R_{x_1} - 1$$

$$R_{x_2} = R_{x_3} = R_{x_4} = 3\,(R_{EQ_2})$$

$$C\,(pF) = \frac{2000\,(ps)}{R_{x_1}\,(\Omega)}$$

Example for $I_{F_{ON}}$ = 100 mA: V_F can be obtained from Figure 9 (= 1.84 V)

$$R_y = \frac{(5 - 1.84) + 3.97\,(5 - 1.79 - 1.6)}{0.100}$$

$$R_y = \frac{3.16 + 6.39}{0.100} = 95.5\ \Omega$$

$$R_{x_1} = \frac{1}{2}\left(\frac{R_y}{3.97}\right) = 12.0\ \Omega$$

$$R_{EQ_2} = 12.0 - 1 = 11.0\ \Omega$$

$$R_{x_2} = R_{x_3} = R_{x_4} = 3\,(11.0) = 33.0\ \Omega$$

$$C = \frac{2{,}000\ pS}{12.0\ \Omega} = 167\ pF$$

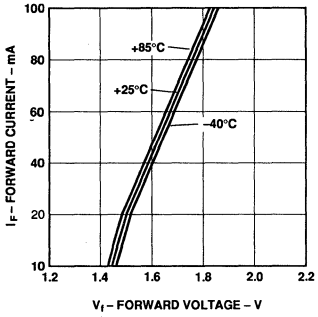


Figure 9. Forward Voltage and Current Characteristics.

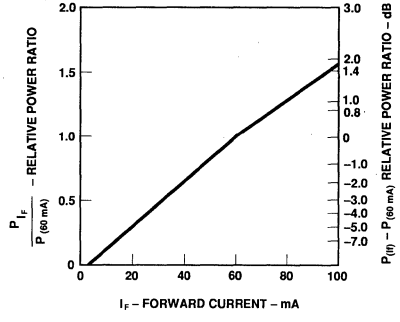


Figure 10. Normalized Transmitter Output vs. Forward Current.

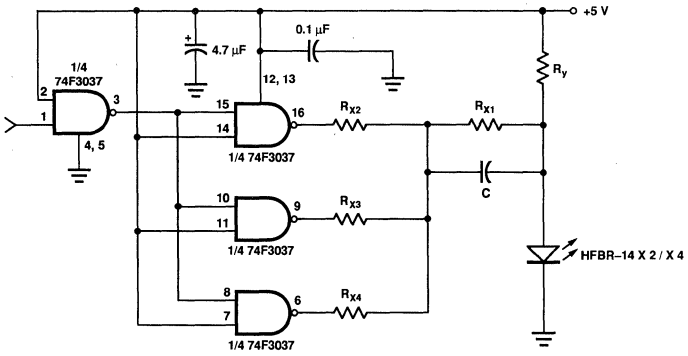


Figure 11. Recommended Drive Circuit.

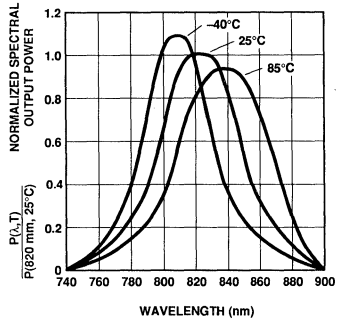


Figure 12. Transmitter Spectrum Normalized to the Peak at 25°C.

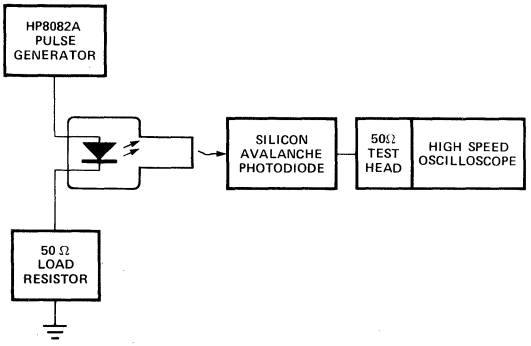


Figure 13. Test Circuit for Measuring t_r, t_f.

HEWLETT PACKARD

5 MBd Low Cost Fiber Optic Receiver

Technical Data

HFBR-24X2 Series

Description

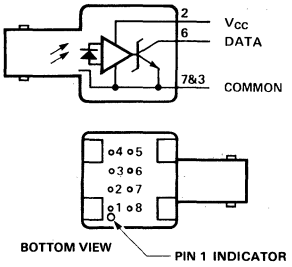
The HFBR-24X2 fiber optic receiver is designed to operate with the Hewlett-Packard HFBR-14XX fiber optic transmitter and 50/125 µm, 62.5/125 µm, and 100/140 µm fiber optic cable. Consistent coupling into the receiver is assured by the lensed optical system (Figure 1). Response does not vary with fiber size.

The HFBR-24X2 receiver incorporates an integrated photo IC containing a photodetector and dc amplifier driving an open-collector Schottky output transistor. The HFBR-24X2 is designed for direct interfacing to popular logic families. The absence of an internal pull-up resistor allows the open-collector output to be used with logic families such as CMOS requiring voltage excursions much higher than V_{CC}.

Both the open-collector "Data" output Pin 6 and V_{CC} Pin 2 are referenced to "Com" Pin 3, 7. The "Data" output allows busing, strobing and wired "OR" circuit configurations. The transmitter is designed to operate from a single +5 V supply. It is essential that a bypass capacitor (0.1 µF ceramic) be connected from Pin 2 (V_{CC}) to Pin 3 (circuit common) of the receiver.

CAUTION: The small junction sizes inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Housed Product



PIN	FUNCTION
1†	N.C.
2	V_{CC} (5 V)
3*	COMMON
4†	N.C.
5†	N.C.
6	DATA
7*	COMMON
8†	N.C.

*PINS 3 AND 7 ARE ELECTRICALLY CONNECTED TO HEADER

†PINS 1, 4, 5, AND 8 ARE ELECTRICALLY CONNECTED

Unhoused Product

BOTTOM VIEW

PIN	FUNCTION
1	V_{CC} (5 V)
2	COMMON
3	DATA
4	COMMON

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–55	+85	°C	
Operating Temperature		T_A	–40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	Note 1
	Time			10	sec	
Supply Voltage		V_{CC}	–0.5	7.0	V	
Output Current		I_O		25	mA	
Output Voltage		V_O	–0.5	18.0	V	
Output Collector Power Dissipation		$P_{O\,AV}$		40	mW	
Fan Out (TTL)		N		5		Note 2

Electrical / Optical Characteristics –40°C to + 85°C unless otherwise specified;

Fiber sizes with core diameter ≤ 100 µm and NA ≤ 0.35, 4.75 V ≤ V_{CC} ≤ 5.25 V

Parameter	Symbol	Min.	Typ.[3]	Max.	Units	Conditions	Reference
High Level Output Current	I_{OH}		5	250	µA	V_O = 18 V P_R < –40 dBm	
Low Level Output Voltage	V_{OL}		0.4	0.5	V	I_O = 8 mA P_R > –24 dBm	
High Level Supply Current	I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V P_R < –40 dBm	
Low Level Supply Current	I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V P_R > –24 dBm	
Equivalent N.A.	NA		0.50				
Optical Port Diameter	D_R		400		µm		Note 4

Dynamic Characteristics –40°C to +85°C unless otherwise specified; 4.75 V ≤ V_{CC} ≤ 5.25 V; BER ≤ 10^{-9}

Parameter	Symbol	Min.	Typ.[3]	Max.	Units	Conditions	Reference
Peak Input Power Level Logic HIGH	P_{RH}			–40 0.1	dBm μW	λ_P = 820 nm	Note 5
Peak Input Power Level Logic LOW	P_{RL}	–25.4		–9.2	dBm	T_A = +25°C,	Note 5
		2.9		120	μW	I_{OL} = 8 mA	
		–24.0		–10.0	dBm	I_{OL} = 8 mA	
		4.0		100	μW		
Propagation Delay LOW to HIGH	t_{PLHR}		65		nsec	T_A = 25°C, P_R = –21 dBm, Data Rate = 5 MBd	Note 6
Propagation Delay HIGH to LOW	t_{PHLR}		49		nsec		

Notes:
1. 2.0 mm from where leads enter case.
2. 8 mA load (5 x 1.6 mA), R_L = 560 Ω.
3. Typical data at T_A = 25° C, V_{CC} = 5.0 Vdc.
4. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
5. Measured at the end of 100/140 μm fiber optic cable with large area detector.
6. Propagation delay through the system is the result of several sequentially-occurring phenomena. Consequently it is a combination of data-rate-limiting effects and of transmission-time effects. Because of this, the data-rate limit of the system must be described in terms of time differentials between delays imposed on falling and rising edges.
   As the cable length is increased, the propagation delays increase at 5 ns per metre of length. Data rate, as limited by pulse width distortion, is not affected by increasing cable length if the optical power level at the receiver is maintained.

HEWLETT PACKARD

25 MHz Low Cost Fiber Optic Receiver

Technical Data

HFBR-24X4 Series

Description

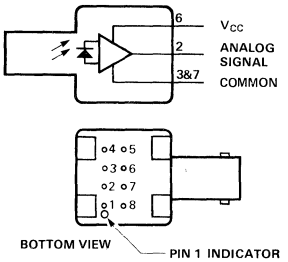
The HFBR-24X4 fiber optic receiver is designed to operate with the Hewlett-Packard HFBR-14XX fiber optic transmitters and 50/125 µm, 62.5/125 µm, and 100/140 µm fiber optic cable. Consistent coupling into the receiver is assured by the lensed optical system (Figure 1). Response does not vary with fiber size.

The receiver output is an analog signal that can be optimized for a variety of distance/data rate requirements. Low-cost external components can be used to convert the analog output to logic compatible signal levels for various data formats and data rates up to 35 MBaud. This distance/data rate tradeoff results in increased optical power budget at lower data rates which can be used for additional distance or splices.

The HFBR-24X4 receiver contains a PIN photodiode and low noise transimpedance pre-amplifier integrated circuit with an inverting output (see note 3). The HFBR-24X4 receives an optical signal and converts it to an analog voltage. The output is a buffered emitter-follower. Because the signal amplitude from the HFBR-24X4 receiver is much larger than from a simple PIN photodiode, it is less susceptible to EMI, especially at high signal rates. A receiver dynamic range of 15 dB over temperature is achievable (assuming 10^{-9} BER). For very noisy environments, the conductive port option is recommended.

The frequency response is typically dc to 25 MHz. Although the HFBR-24X4 is an analog receiver, it is easily made compatible with digital systems. Please refer to Application Bulletin 73 for simple and inexpensive circuits that operate up to 35 MBd.

Housed Product



PIN	FUNCTION
1†	N.C.
2	SIGNAL
3*	COMMON
4†	N.C.
5†	N.C.
6	V_{CC} (5 V)
7*	COMMON
8†	N.C.

*PINS 3 AND 7 ARE ELECTRICALLY CONNECTED TO HEADER

†PINS 1, 4, 5, AND 8 ARE ELECTRICALLY CONNECTED

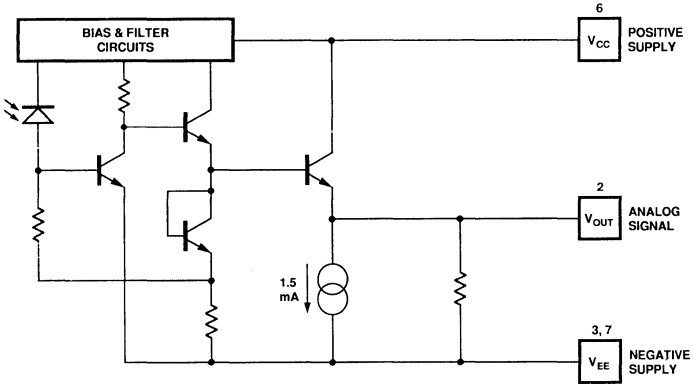
Unhoused Product

BOTTOM VIEW

PIN	FUNCTION
1	SIGNAL
2	COMMON
3	V_{CC} (5 V)
4	COMMON

CAUTION: *The small junction sizes inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Simplified Schematic Diagram



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–55	+85	°C	
Operating Temperature		T_A	–40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	Note 1
	Time			10	sec	
Signal Pin Voltage		V_{SIGNAL}	–0.5	1	V	
Supply Voltage		V_{CC}	–0.5	7.0	V	

Electrical /Optical Characteristics –40°C to +85°C; 4.75 V ≤ V_{CC} ≤ 5.25 V; R_{LOAD} = 511 Ω; Fiber sizes with core diameter ≤ 100 µm, and N.A. ≤ 0.35 unless otherwise specified.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Reference
Responsivity	R_P	5.1	7	10.9	mV/µW	T_A = 25°C @ 820 nm	Figure 14
		4.6		12.3	mV/µW		
RMS Output Noise Voltage	V_{NO}		0.30	0.36	mV	T_A = 25°C, P_R = 0 µW	Figure 15
				0.43	mV	P_R = 0 µW	
Equivalent Optical Noise Input Power (RMS)	P_N		–43.7	–40.3	dBm		
			0.042	0.094	µW		
Peak Input Power	P_R			–12.6	dBm	T_A = 25°C	Note 2
				55	µW		
				–14	dBm		
				40	µW		
Output Impedance	Z_O		20		Ω	Test Frequency = 20 MHz	
DC Output Voltage	V_{odc}		0.7		V	P_R = 0 µW	Note 3
Power Supply Current	I_{CC}		3.4	6.0	mA	R_{LOAD} = ∞	
Equivalent N.A.	NA		0.35				
Equivalent Diameter	D_R		250		µm		Note 4

Dynamic Characteristics –40°C to +85°C; 4.75 V ≤ V_{CC} ≤ 5.25 V; R_{LOAD} = 511 Ω, C_{LOAD} = 13 pF unless otherwise specified.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Reference
Rise/Fall Time, 10% to 90%	t_r, t_f		14	19.5	ns	T_A = 25°C P_R = 10 µW Peak	Note 6
				26	ns		
Pulse Width Distortion	$t_{phl} - t_{plh}$			2	ns	P_R = 40 µW Peak	
Overshoot			10		%	T_A = 25°C	Note 7
Bandwidth (Electrical)	BW_e		25		MHz	–3 dB Electrical	
Power Supply Rejection Ratio (Referred to Output)	PSRR		50		dB	at 1 MHz	Figure 16 Note 8
Bandwidth - Rise Time Product			0.35		Hz · s		

Notes:
1. 2.0 mm from where leads enter case.
2. If P_R > 40 µW, then pulse width distortion may increase. At P_{in} = 80 µW and T_A = 85°C, some units have exhibited as much as 100 ns pulse width distortion.
3. $V_{OUT} = V_{ODC} - (R_P \times P_R)$.
4. D_s is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
5. Typical specifications are for operation at T_A = 25°C and V_{CC} = 5.0 V.
6. Input optical signal is assumed to have 10% - 90% rise and fall times of less than 6 ns.
7. Percent overshoot is defined as: $\left(\frac{V_{PK} - V_{100\%}}{V_{100\%}}\right) \times 100\%$.
8. Output referred P.S.R.R. is defined as 20 log $\left(\frac{V_{POWER\ SUPPLY\ RIPPLE}}{V_{OUT\ RIPPLE}}\right)$.

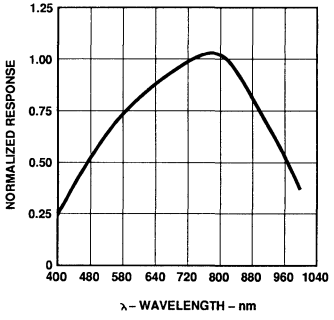


Figure 14. Receiver Spectral Response Normalized to 820 nm.

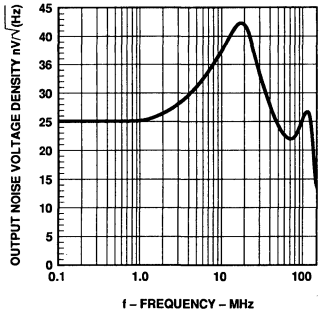


Figure 15. Receiver Noise Spectral Density.

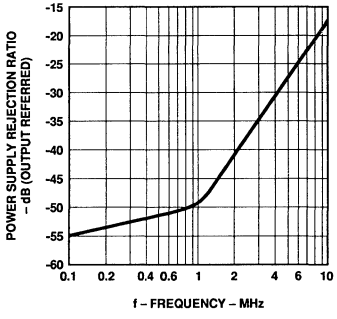


Figure 16. Receiver Power Supply Rejection vs. Frequency.

HEWLETT PACKARD

125 MHz Low Cost Fiber Optic Receiver

Technical Data

HFBR-24X6 Series

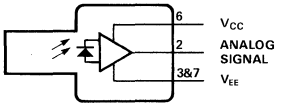
Description

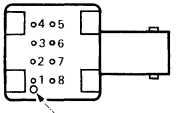
The HFBR-24X6 fiber optic receiver is designed to operate with the Hewlett-Packard HFBR-14XX fiber optic transmitters and 50/125 µm, 62.5/125 µm, and 100/140 µm fiber optic cable. Consistent coupling into the receiver is assured by the lensed optical system (Figure 1). Response does not vary with fiber size for core diameters of 100 µm or less.

The receiver output is an analog signal which allows follow-on circuitry to be optimized for a variety of distance/data rate requirements. Low-cost external components can be used to convert the analog output to logic compatible signal levels for various data formats and data rates up to 150 MBd. This distance/data rate tradeoff results in increased optical power budget at lower data rates which can be used for additional distance or splices.

The HFBR-24X6 receiver contains a PIN photodiode and low noise transimpedance pre-amplifier integrated circuit. The HFBR-24X6 receives an optical signal and converts it to an analog voltage. The output is a buffered emitter-follower. Because the signal amplitude from the HFBR-24X6 receiver is much larger than from a simple PIN photodiode, it is less susceptible to EMI, especially at high signal rates. For very noisy environments, the conductive port option is recommended. A receiver dynamic range of 23 dB over temperature is achievable (assuming 10^{-9} BER). Because the maximum receiver input power is 6 dB larger and the noise is 2 dB lower over temperature than HP's HFBR-24X4 25 MHz receiver, the HFBR-24X6 is well suited for more demanding link designs that require wide receiver dynamic range.

Housed Product





BOTTOM VIEW — PIN 1 INDICATOR

PIN	FUNCTION
1†	N.C.
2	SIGNAL
3*	V_{EE}
4†	N.C.
5†	N.C.
6	V_{CC}
7*	V_{EE}
8†	N.C.

*PINS 3 AND 7 ARE ELECTRICALLY CONNECTED TO HEADER

†PINS 1, 4, 5 AND 8 ARE ELECTRICALLY CONNECTED.

Unhoused Product

BOTTOM VIEW

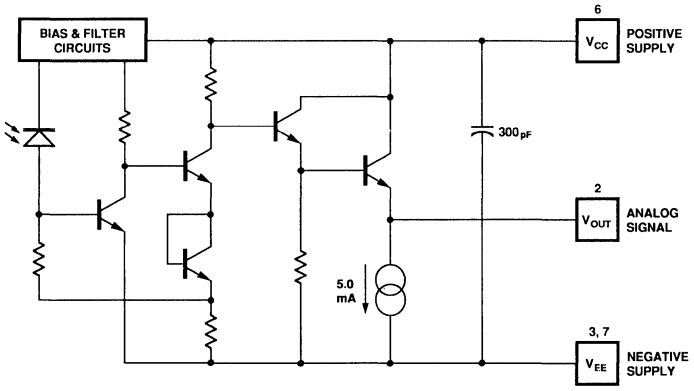
PIN	FUNCTION
1	SIGNAL
2*	V_{EE}
3	V_{CC}
4*	V_{EE}

CAUTION: *The small junction sizes inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

The frequency response is typically dc to 125 MHz. Although the HFBR-24X6 is an analog receiver, it is easily made compatible with digital systems. Please refer to Application Bulletin 78 for simple and inexpensive circuits that operate up to 150 MBd.

The recommended ac coupled receiver circuit is shown in Figure 17. It is essential that a 10 ohm resistor be connected between V_{EE} and the power supply, and a 0.1 µF ceramic bypass capacitor be connected between the power supply and ground.

Simplified Schematic Diagram



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–55	+85	°C	
Operating Temperature		T_A	–40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	Note 1
	Time			10	sec	
Signal Pin Voltage		V_{SIGNAL}	–0.5	V_{CC}	V	
Supply Voltage		V_{CC}-V_{EE}	–0.5	6.0	V	
Output Current		I_O		25	mA	

Electrical / Optical Characteristics –40°C to +85°C; –5.45 V ≤ Supply Voltage ≤ –4.75 V, R_{LOAD} = 511 Ω, Fiber sizes with core diameter ≤ 100 µm, and N.A. ≤ 0.35 unless otherwise specified.

Parameter	Symbol	Min.	Typ.[3]	Max.	Units	Conditions	Reference
Responsivity	R_P	5.3	7	9.6	mV/µW	T_A = 25° C @ 820 nm, 50 MHz	Note 3, 4
		4.5		11.5	mV/µW	@ 820 nm, 50 MHz	
RMS Output Noise Voltage	V_{NO}		0.40	0.59	mV	Bandwidth Filtered @ 75 MHz P_R = 0 µW	Note 5
				0.70	mV	Unfiltered Bandwidth P_R = 0 µW	Figure 18
Equivalent Optical Noise Input Power (RMS)	P_N		–43.0	–41.4	dBm	Bandwidth Filtered @ 75 MHz	
			0.050	0.065	µW		
Peak Input Power	P_R			–7.6	dBm	T_A = 25°C	Figure 19
				175	µW		Note 6
				–8.2	dBm		
				150	µW		
Output Impedance	Z_O		30		Ω	Test Frequency = 50 MHz	
DC Output Voltage	V_{odc}	–4.2	–3.1	–2.4	V	P_R = 0 µW	
Power Supply Current	I_{EE}		9	15	mA	R_{LOAD} = ∞	
Equivalent N.A.	NA		0.35				
Equivalent Diameter	D_R		324		µm		Note 7

Dynamic Characteristics –40°C to +85°C; –5.45 V ≤ Supply Voltage ≤ –4.75 V; R_{LOAD} = 511 Ω, C_{LOAD} = 5 pF unless otherwise specified.

Parameter	Symbol	Min.	Typ.[8]	Max.	Units	Conditions	Reference
Rise/Fall Time 10% to 90%	t_r, t_f		3.3	6.3	ns	P_R = 100 µW	Figure 20
Pulse Width Distortion	PWD		0.4	2.5	ns	P_R = 150 µW Peak	Note 8, Figure 19
Overshoot			2		%	P_R = 5 µW Peak, $t_{r_{optical}}$ = 1.5 ns	Note 9
Bandwidth (Electrical)	BW_e		125		MHz	–3 dB Electrical	
Power Supply Rejection Ratio	PSRR		20		dB	@ 10 MHz	Note 10
Bandwidth - Rise Time Product			0.41		Hz · s		Note 11

Notes:

1. 2.0 mm from where leads enter case.
2. Typical specifications are for operation at T_A = 25°C and V_{EE} = –5.2 Vdc.
3. For 200 µm PCS fibers, typical responsivity will be 6 mV/µW. Other parameters will change as well.
4. Pin #2 should be ac coupled to a 511 ohm load. Load capacitance must be less than 5 pF.
5. Measured with a 3 pole Bessel filter with a 75 MHz, –3 dB bandwidth. Recommended receiver filters for various bandwidths are provided in Application Bulletin 78.
6. Overdrive is defined at PWD = 2.5 ns.
7. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
8. Measured with a 10 ns pulse width, 50% duty cycle, at the 50% amplitude point of the waveform.
9. Percent overshoot is defined as: $\left(\frac{V_{PK} - V_{100\%}}{V_{100\%}}\right)$ x 100%.
10. Output referred P.S.R.R. is defined as 20 log $\left(\frac{V_{POWER\ SUPPLY\ RIPPLE}}{V_{OUT\ RIPPLE}}\right)$.
11. The conversion factor for the rise time to bandwidth is 0.41 since the HFBR-24X6 has a second order bandwidth limiting characteristic.

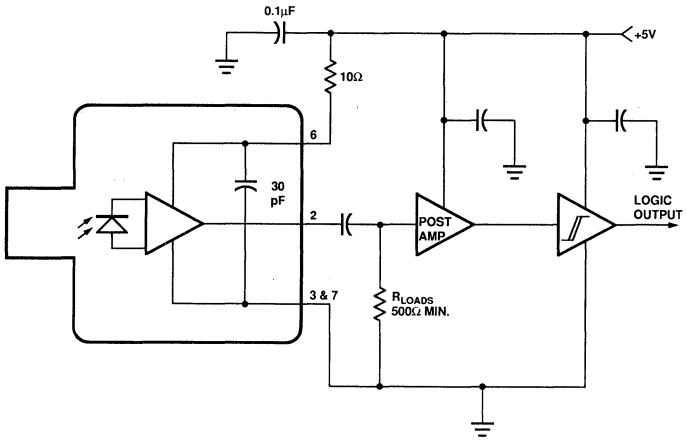


Figure 17. Recommended ac Coupled Receiver Circuit (See AB 78 and AN 1038 for More Information)

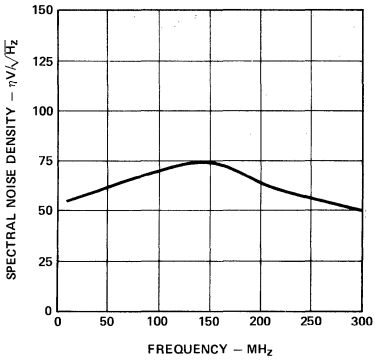


Figure 18. Typical Spectral Noise Density vs. Frequency

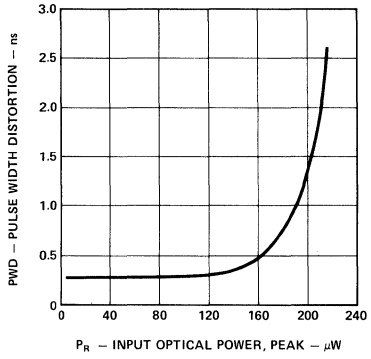


Figure 19. Typical Pulse Width Distortion vs. Peak Input Power

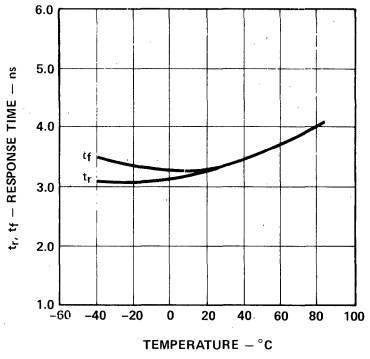


Figure 20. Typical Rise and Fall Times vs. Temperature

Conductive Port Option for Low Cost Miniature Link Components

Technical Data

OPTION C

Features

- **Withstands Electro-static Discharge (ESD) of 25kV to the Port**
- **Significantly Decreases Effect of Electro-magnetic Interference (EMI) on Receiver Sensitivity**
- **Available with Both SMA and Threaded ST Styled Port Receivers**
- **Allows the Designer to Separate the Signal and Conductive Port Grounds**

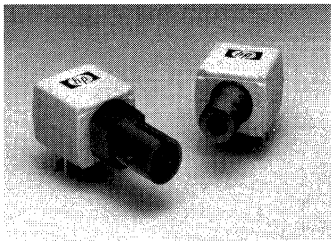
Description

The conductive port option for the Low Cost Miniature Link component family consists of a grounding path from the conductive port to four grounding pins as shown in the package outline drawing. Signal ground is separate from the four grounding pins to give the designer more flexibility. This option is available with all SMA and ST panel mount styled port receivers. Electrical/optical performance of the receivers is not affected by the conductive port. Refer to the HFBR-0400 data sheets for more information.

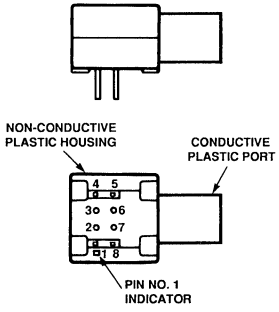
Applications

HP recommends that the designer use separate ground paths for the signal ground and the conductive port ground in order to minimize the effects of coupled noise on the receiver circuitry. If the designer notices that extreme noise is present on the system chassis, care should be taken to electrically isolate the conductive port from the chassis.

In the case of ESD, the conductive port option does not alleviate the need for system recovery procedures. This option ensures that a 25kV ESD event entering through the connector port will not cause catastrophic failure, but does not guarantee error-free performance.



Package Outline



Pin	Function
1	Port Ground Pin
2	Part Dependent
3	Part Dependent
4	Port Ground Pin
5	Port Ground Pin
6	Part Dependent
7	Part Dependent
8	Port Ground Pin

Reliability Information

Low Cost Miniature Link components with the Conductive Port Option are as reliable as standard HFBR-0400 components. The following tests were performed to verify the mechanical reliability of this option.

Ordering Information

To order the Conductive Port Option with a particular receiver component, place a "C" after the base part number. For example, to order an HFBR-2406 with this option, order an HFBR-2406C. As another example, to order an HFBR-2416T with this option, order an HFBR-2416TC.

This option is available with the following part numbers:

HFBR-2402	HFBR-2442T
HFBR-2404	HFBR-2444T
HFBR-2406	HFBR-2446T
HFBR-2412T	HFBR-2452
HFBR-2414T	HFBR-2454
HFBR-2416T	HFBR-2456
HFBR-2432	HFBR-2462T
HFBR-2434	HFBR-2464T
HFBR-2436	HFBR-2466T

Mechanical and Environmental Tests[1]

Test	MIL-STD-883/ Other Reference	Test Conditions	Units Tested	Total Failed
Temperature Cycling	1010 Condition B	-55°C to +125°C 15 min. dwell/5 min. transfer 100 cycles	70	0
Thermal Shock	1011 Condition B	-55°C to +125°C 5 min. dwell/10 sec. transfer 500 cycles	45	0
High Temp. Storage	1008 Condition B	T_A = 125°C 1000 Hours	50	0
Mechanical Shock	2002 Condition B	1500 g/0.5 ms 5 impacts each axis	40	0
Port[2] Strength	T_A = 25°C	6 Kg-cm no port damage	20	0
Seal Dye Penetrant (Zyglo)	1014 Condition D	45 psi, 10 Hours No leakage into microelectronic cavity	15	0
Solderability	2003	245°C	10	0
Resistance to Solvents	2015	3 one min. immersion brush after solvent	13	0
Chemical Resistance	—	5 minutes in Acetone, Methanol, Boiling Water	12	0
Temperature-Humidity	—	T_A = 85°C, RH = 85% Biased, 500 hours	30	0
Lead Integrity	2004 Condition B2	8 Oz. Wt. to each lead tested for three 90° arcs of the case	16	0

Notes:
1. Tests were performed on both SMA and ST products with the conductive port option.
2. The Port Strength test was designed to address the concerns with hand tightening the SMA connector to the fiber optic port. The limit is set to a level beyond most reasonable hand fastening loading.

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Threaded ST Port Option for Low Cost Miniature Link Components

Technical Data

OPTION T
(Recommended for New Designs)

Features

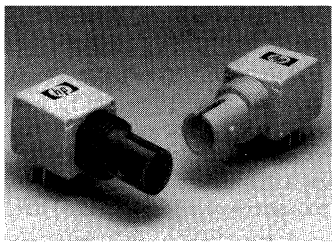
- **Threading Allows ST Styled Port Components to be Panel Mounted**
- **Compatible with all Current Makes of ST Multimode Connectors**
- **Mechanical Dimensions are Compliant with MIL-STD-83522/13**

Description

Low Cost Miniature Link components with the Threaded ST Port Option come with 0.2 inch (5.1mm) of 3/8-32 UNEF-2A threads on the port. This option is available with all HFBR-0400, ST styled port components. Components with this option retain the same superior electrical/optical and mechanical performance as that of the base HFBR-0400 components. Refer to the HFBR-0400 data sheets for more information on electrical/optical performance and the HFBR-0400 Reliability data sheet for more information on mechanical durability.

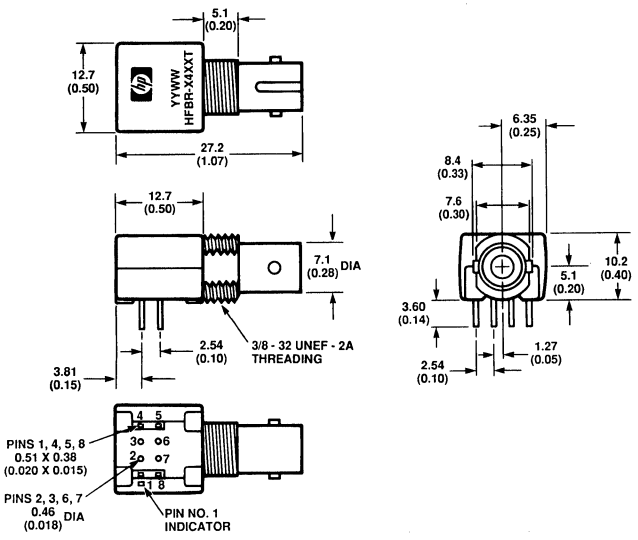
Panel Mounting

Low Cost Miniature Link components with the Threaded ST Port Option are suitable for panel mounting to chasis walls. The maximum wall thickness possible when using nuts and washers from the HFBR-4411 kit is 0.11 inch (2.8mm).



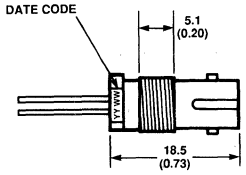
Package Outline

Housed Product

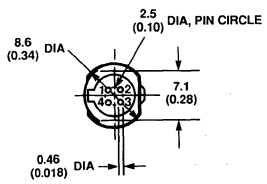


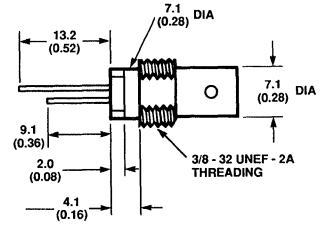
FIBER OPTICS

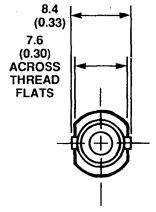
Package Outline
Port Product



NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES)

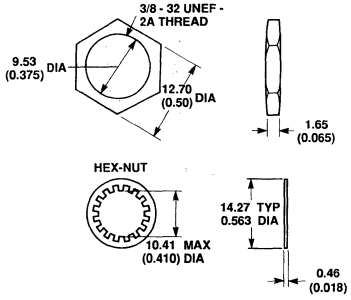






The HFBR-4411 kit consists of 100 nuts and 100 washers with dimensions as shown in Figure 1. These kits are available from HP or any authorized distribtor. Any standard size nut and washer will work, provided the total thickness of the wall, nut, and washer does not exceed 0.2 inch (5.1mm).

When preparing the chasis wall for panel mounting, use the mounting template in Figure 2. When tightening the nut, torque should not exceed 0.8 N-m (8.0 in-lb).



NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES)

INTERNAL TOOTH LOCK WASHER

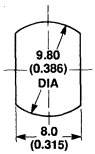
Figure 1. HFBR-4411 Mechanical Dimensions.

Ordering Information

To order the Threaded ST Port Option with a particular component, place a "T" after the base part number. For example, to order an HFBR-2416 with this option, order an HFBR-2416T.

This option is available with the following part numbers:

HFBR-1412	HFBR-2416
HFBR-1414	HFBR-2442
HFBR-1442	HFBR-2444
HFBR-1444	HFBR-2446
HFBR-1462	HFBR-2462
HFBR-1464	HFBR-2464
HFBR-2412	HFBR-2466
HFBR-2414	



NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES)

Figure 2. Recommended Cut-out for Panel Mounting.

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Glass Fiber-Optic Cable/ Connector Assemblies

Technical Data

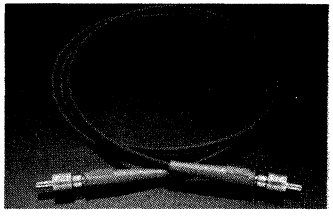
Features

- **Choice of ST or SMA Connectors**
- **Connectors Factory Installed and Tested**
- **Choice of 50/125 µm, 62.5/ 125 µm or 100/140 µm Fiber**
- **Tight Jacket Construction**
- **UL Recognized, Meets OFNR Listing (UL 1666)**
- **Parameters Optimized for Data Communication Applications**

Description

HP connectored cable assemblies are available in various industry standard sizes and styles. The designer may choose among 50/125 µm, 62.5/125 µm and 100/140 µm cable and ST and SMA connectors (50/125 µm is available with only ST connectors in one- and ten-metre lengths). These cable assemblies have been specified for use with HP's 820 nm and 1300 nm fiber-optic transmitters and receivers and are ideal for various data communication applications.

Each cable assembly has been factory assembled and 100% tested according to industry-standard procedures. Therefore, designers can be assured that they are receiving the highest possible quality cable assemblies for their prototyping, testing or production needs.



FIBER OPTICS

Ordering Information[1]

HFBR- □ □ □ □ □ □

Cable Code
- A - 100/140 µm
- B - 62.5/125 µm
- C - 50/125 µm*

Connector Code
- U - unconnectored
- W - SMA connector
- X - ST connector

Length Code
- 1-999 m, 1-m increments
  e.g. 016 = 16 m
- 1-2 km, 100-m increments
  e.g. 1K6 = 1.6 km

Channel Code
- S - single channel
- D - dual channel

*Available only in single channel one- and ten-metre lengths with ST connectors.

Order Examples

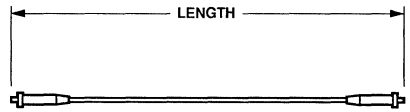
HFBR-AWS050, quantity 1: one 50 m simplex, 100/140 µm cable assembly with SMA connectors

HFBR-BXD2K0, quantity 2: two 2 km duplex, 62.5/125 µm cable assemblies with ST connectors

HFBR-BUS1K5, quantity 3: three 1.5 km simplex, 62.5/125 µm unconnectored cables

Cable Length Tolerances

Cable Length (metres)	Tolerance
1 - 10	+10/-0 %
11 - 100	+1/-0 metre
> 100	+1/-0 %



Cable Information

Temperature Ratings

Parameter	Min.	Max.	Unit
Storage Temperature	-40	+70	°C
Operating Temperature	-20	+70	°C

Mechanical Specifications (25°C)

Parameter	Single Channel	Dual Channel	Unit	Conditions	Note
Maximum Tensile Load				EIA-455-33	
Short Term	500	1000	N		2
Long Term	300	500	N		
Minimum Bend Radius					
Short Term	5.0	5.0	cm	500 N Tensile Load	
Long Term	3.0	3.0	cm	300 N Tensile Load	
Crush Resistance	750	750	N/cm	EIA-455-41	
Impact Resistance	1000	1000	cycles	EIA-455-25 @ 1.6 N-m	
Flex Resistance	7500	7500	cycles	EIA-455-104	
Maximum Vertical Rise	1000	1000	m		

Mechanical Dimensions

	50/125 μm	62.5/125 μm	100/140 μm
Core Diameter (μm)	50	62.5	100
Cladding Diameter (μm)	125	125	140
Buffer Diameter (μm)	900	900	900
Cable Outside Diameter (mm)			
Single Channel	2.9	2.9	2.9
Dual Channel	2.9x5.8	2.9x5.8	2.9x5.8

Optical Specifications (850 nm/1300 nm)

	50/125 μm	62.5/125 μm	100/140μm	Conditions
Maximum Attenuation (dB/km)	5.0/4.0	5.0/3.0	6.0/5.0	EIA-455-46
Typical Attenuation (dB/km)	4.0/2.0	4.5/2.0	5.5/3.5	
Minimum Modal Bandwidth (MHz-km)	400/400	160/200	100/100	EIA-455-30
Typical 3dB Optical Bandwidth- Length Product (MHz-km)[3]	41/250	40/180	38/95	
Numerical Aperture	0.20	0.275	0.29	EIA-455-47 method A,B,C

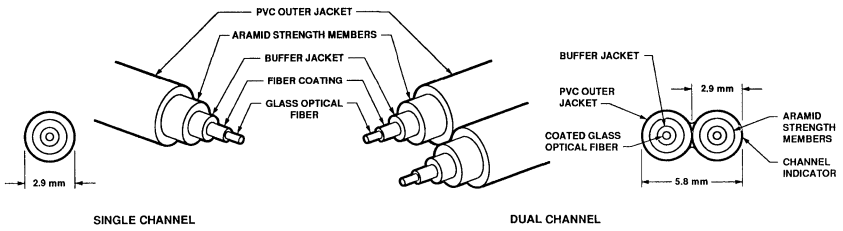


Figure 1. Cable Construction Diagram.

Connector/Mating Adapter Information

Ordering Information

Part Number	Description	Reference
HFBR-4001	100/140 µm SMA style piece part connector	Note 4, Fig. 2
HFBR-4002	62.5/125 µm SMA style piece part connector	Note 4, Fig. 2
HFBR-4003	100/140 µm ST style piece part connector	Note 4, Fig. 3
HFBR-4004	62.5/125 µm ST style piece part connector	Note 4, Fig. 3
HFBR-4409	SMA style mating adapter (nuts/washers incl.)	Fig. 4
HFBR-4419	ST style mating adapter (nut/washer incl.)	Fig. 5

Mating Adapter Mechanical/Optical Specifications

	Max.	Units	Conditions	Note
SMA Mating Adapter				
Fixed Loss (α_F)	2	dB	50/125 µm fiber	5
	2	dB	62.5/125 µm fiber	5
	2	dB	100/140 µm fiber	5
ST Mating Adapter				
Fixed Loss (α_F)	1	dB	50/125 µm fiber	5
	1	dB	62.5/125 µm fiber	5
	1	dB	100/140 µm fiber	5

Mechanical Dimensions[6]

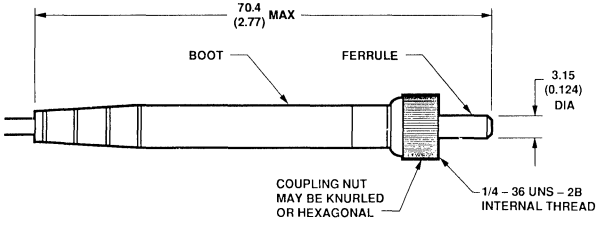


Figure 2. HFBR-4001 and HFBR-4002 SMA Style Connector.

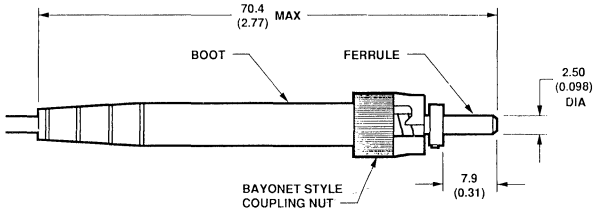


Figure 3. HFBR-4003 and HFBR-4004 ST Style Connector.

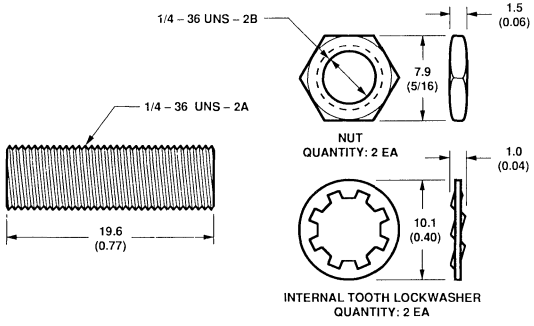


Figure 4. HFBR-4409 SMA Style Mating Adapter.

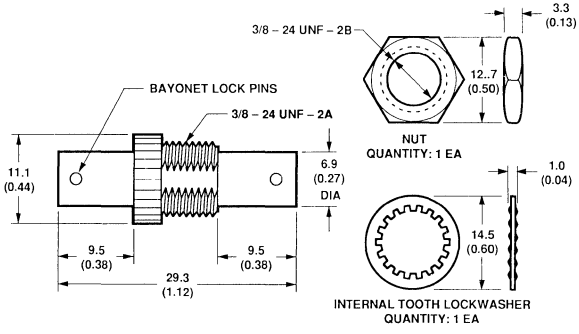


Figure 5. HFBR-4419 ST Style Mating Adapter.

Notes:

1. HP is in the process of obsoleting the following part numbers and does not recommend their use for new designs: HFBR-AHDxxx and HFBR-AHSxxx cable assemblies, the HFBR-4000 connector, the HFBR-3099 mating adapter, and HFBR-0100/0101/0102 connectoring kits. Please contact your local HP components representative for more information.
2. Short term is ≤ 6 hours.
3. Calculations are based on worst case parameters of HP 820 nm and 1300 nm optical components.
4. Recommended connectoring kit: OFTI 400 Series Field Installation Kit.
5. Fixed losses (length independent) apply only to the use of mating adapters in link design calculations. Fixed losses at transmitter/receiver interfaces are included in HP transmitter/receiver optical specifications.
6. Dimensions in millimetres (inches).

HEWLETT PACKARD

SNAP-IN FIBER OPTIC LINKS TRANSMITTERS, RECEIVERS, CABLE AND CONNECTORS

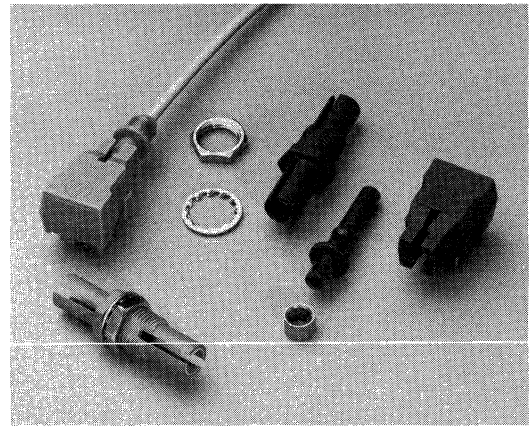
HFBR-0500 SERIES

Features

- **GUARANTEED LINK PERFORMANCE OVER TEMPERATURE**
  High Speed Links: dc to 5 MBd
  Extended Distance Links up to 82 m
  Low Current Links: 6 mA Peak Supply Current for an 8 m Link
  Photo Interrupters
- **LOW COST PLASTIC DUAL-IN-LINE PACKAGE**
- **EASY FIELD CONNECTORING**
- **EASY TO USE RECEIVERS:**
  Logic Compatible Output Level
  Single +5 V Receiver Power Supply
  High Noise Immunity
- **LOW LOSS PLASTIC CABLE:**
  Selected Super Low Loss Simplex Cable
  Simplex and Zip Cord Style Duplex Cable

Applications

- **HIGH VOLTAGE ISOLATION**
- **SECURE DATA COMMUNICATIONS**
- **REMOTE PHOTO INTERRUPTER**
- **LOW CURRENT LINKS**
- **INTER/INTRA-SYSTEM LINKS**
- **STATIC PROTECTION**
- **EMC REGULATED SYSTEMS (FCC, VDE)**



Description

The HFBR-0500 series is a complete family of fiber optic link components for configuring low-cost control, data transmission, and photo interrupter links. These components are designed to mate with plastic snap-in connectors and low-cost plastic cable.* Link design is simplified by the logic compatible receivers and the ease of connectoring the plastic fiber cable. The key parameters of links configured with the HFBR-0500 family are fully guaranteed.

* Cable is available in standard low loss and selected super low loss varieties.

Link Selection Guide

GUARANTEED LINKS

		Guaranteed Link Length 0-70° C		Typical Link Lengths 25° C				
	Data Rate	Standard Cable	Improved Cable	Standard Cable	Improved Cable	Transmitter	Receiver	Page
5 MBd Link	5 MBd	12	17	35 m	40 m	HFBR-1510	HFBR-2501	5-74
1 MBd Link	1 MBd	24	34	50 m	65 m	HFBR-1502	HFBR-2502	5-76
Low Current Link	40 kBd	8	11	30 m	35 m	HFBR-1512	HFBR-2503	5-78
Extended Distance Link	40 kBd	60	82	100 m	125 m	HFBR-1512	HFBR-2503	5-78
Photo Interrupter Link	20 kHz 500 kHz	N/A N/A	N/A N/A	N/A N/A	N/A N/A	HFBR-1512 HFBR-1502	HFBR-2503 HFBR-2502	5-80 5-80

Component Selection Guide

TRANSMITTERS

	Minimum Output Optical Power 0 to 70° C	Peak Emission Wavelength	Page
HFBR-1510	−16.5 dBm	665 nm	5-82
HFBR-1502	−13.6 dBm	665 nm	5-82
HFBR-1512	−13.6 dBm	665 nm	5-82

RECEIVERS

	Sensitivity 0 to 70° C	Data Rate	Page
HFBR-2501	−21.6 dBm	5 MBd	5-83
HFBR-2502	−24 dBm	1 MBd	5-83
HFBR-2503	−39 dBm	40 kBd	5-85

CABLES

Please refer to page 15 (of the Versatile Link Fiber Optics Data Sheet) for cable specifications.

CONNECTORS

Page 5-86

HFBR-4501 Gray Connector/Crimp Ring
HFBR-4511 Blue Connector/Crimp Ring
HFBR-4595 Polishing Kit
Polishing Fixture — Abrasive Paper
HFBR-4596 Polishing Fixture
Bulkhead Feedthrough/In-Line Splice
HFBR-4505 Gray
HFBR-4515 Blue

Mechanical Dimensions

Page 5-88

5 MBd Link

HFBR-1510 AND HFBR-2501

The dc to 5 MBd link is guaranteed over temperature to operate up to 17 m with a transmitter drive current of 60 mA. This link uses the 665 nm HFBR-1510 Transmitter, the HFBR-2501 Receiver, and Plastic Cable. The receiver compatible with LSTTL/TTL/CMOS logic levels offers a choice of internal pull-up or open collector output.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units	Ref.
Ambient Temperature	T_A	0	70	°C	
Transmitter Peak Forward Current	$I_{F\,PK}$	10	750	mA	Note 1
Avg. Forward Current	$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	V_{CC}	4.75	5.25	V	Note 2
Fan-Out (TTL)	N		5		

SYSTEM PERFORMANCE Using Standard Cable under recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Data Rate		dc		5	MBd	BER ≤ 10^{-9}	
Transmission Distance Standard Cable	ℓ	12			m	I_{FPK} = 60 mA, 0–70° C	
		17	35		m	I_{FPK} = 60 mA, 25° C	
Transmission Distance Improved Cable		17			m	I_{FPK} = 60 mA, 0–70° C	
		24	40		m	I_{FPK} = 60 mA, 25° C	
Propagation Delay	t_{PLH}		80	140	ns	R_L = 560 Ω, C_L = 30 pF	Fig. 4, 5
	t_{PHL}		50	140	ns	P_R = −21.6≤P_R≤−9.5dBm	Note 3
Pulse Width Distortion	t_D		30		ns	P_R = −15 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 4, 6 Note 4
EMI Immunity			8000		V/m	BER ≤ 10^{-9}	

Notes: 1. For I_{FPK} > 80 mA, the duty factor must be such as to keep I_{FAV} ≤ 80 mA. In addition, for I_{FPK} > 80 mA, the following rules for pulse width apply: I_{FPK} ≤ 160 mA: Pulse width ≤ 1 ms I_{FPK} > 160 mA: Pulse width ≤ 1 μs

2. It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from pin 3 to pin 4 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.
3. The propagation delay of 1 m of cable (5 ns) is included.
4. $T_D = t_{PLH} - t_{PHL}$.
5. Typical data is at 25° C, V_{CC} = 5 V.

Link Design Considerations

The HFBR-1510/2501 Transmitter/Receiver pair is guaranteed for operation at data rates up to 5 MBd over link distances from 0 to 12 metres with standard cable and from 0 to 17 metres with improved cable. The value of transmitter drive current, I_F, depends on the link distance as shown in Figures 2 and 3. Note that there is an upper as well as a lower limit on the value of I_F for any given distance. The dotted lines in Figures 2 and 3 represent pulsed operation. When operating in the pulsed mode, the conditions in Note 1 must be met. After selecting a value of the transmitter drive current I_F, the value of R_1 in Figure 1 can be calculated as follows:

$$R_1 = \frac{V_{CC} - V_F}{I_F}$$

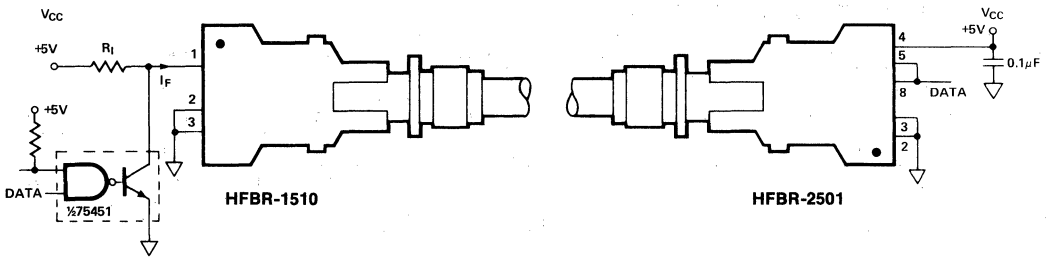


Figure 1. Typical Circuit Operation (5 MBd ≤ 12 m)

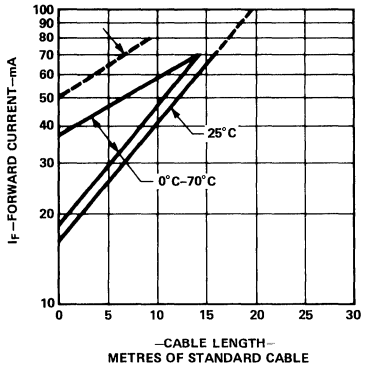


Figure 2. Guaranteed System Performance with HFBR-1510 and HFBR-2501, Standard Cable

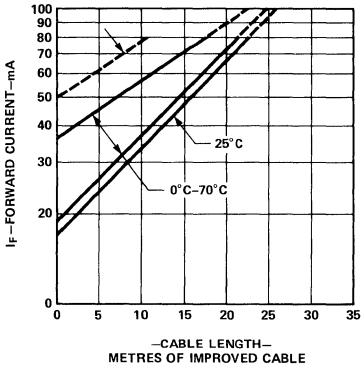


Figure 3. Guaranteed System Performance with HFBR-1510 and HFBR-2501, Improved Cable

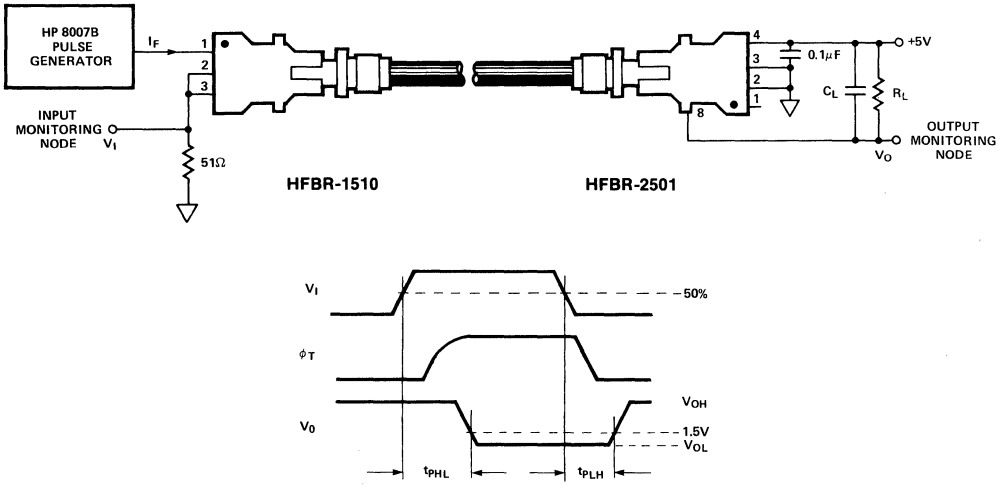


Figure 4. A.C. Test Circuit

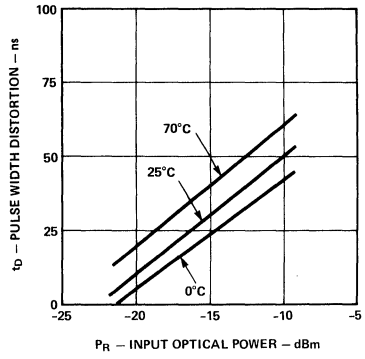


Figure 5. HFBR-1510/2501 Link Pulse Width Distortion vs. Optical Power

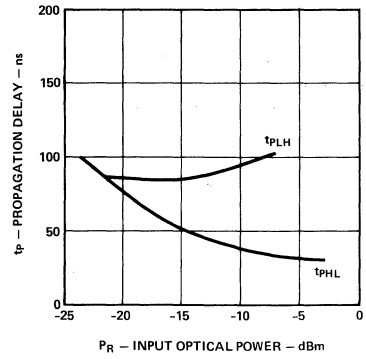


Figure 6. HFBR-1510/2501 Link Propagation Delay vs. Optical Power

FIBER OPTICS

1 MBd Link HFBR-1502 AND HFBR-2502

The dc to 1 MBd link is guaranteed over temperature to operate from 0 to 34 m with a transmitter drive current of 60 mA. This link uses the 665 nm HFBR-1502 Transmitter, the HFBR-2502 Receiver, and Improved Cable. The receiver is compatible with LSTTL/TTL/CMOS logic levels and offers a choice of an internal pull-up or open collector output.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units	Ref.
Ambient Temperature	T_A	0	70	°C	
Transmitter Peak Forward Current	$I_{F\,PK}$	10	750	mA	Note 1
Avg. Forward Current	$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	V_{CC}	4.75	5.25	V	Note 2
Fan-Out (TTL)	N		5		

SYSTEM PERFORMANCE Using Standard Cable under recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Data Rate		dc		1	MBd	BER ≤ 10^{-9}	
Transmission Distance Standard Cable	ℓ	24			m	I_{FPK} = 60 mA, 0–70° C	
		30	50		m	I_{FPK} = 60 mA, 25° C	
Transmission Distance Improved Cable	ℓ	34			m	I_{FPK} = 60 mA, 0–70° C	
		41	65		m	I_{FPK} = 60 mA, 25° C	
Transmission Distance Standard Cable	ℓ	30				I_{FPK} = 120 mA, 0–70° C	
		36	60			I_{FPK} = 120 mA, 25° C	
Transmission Distance Improved Cable	ℓ	41				I_{FPK} = 120 mA, 0–70° C	
		50	75			I_{FPK} = 120 mA, 25° C	
Propagation Delay	t_{PLH}		180	250	ns	R_L = 560 Ω, C_L = 30 pF	Fig. 4, 5
	t_{PHL}		100	140	ns	P_R = −24 dBm	Note 3
Pulse Width Distortion	t_D		80		ns	P_R = −24 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 4, 6 Note 4
EMI Immunity			8000		V/m	BER ≤ 10^{-9}	

Notes: 1. For I_{FPK} > 80 mA, the duty factor must be such as to keep I_{FAV} ≤ 80 mA. In addition, for I_{FPK} > 80 mA, the following rules for pulse width apply: I_{FPK} ≤ 160 mA: Pulse width ≤ 1 ms I_{FPK} > 160 mA: Pulse width ≤ 1 μs

2. It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from pin 3 to pin 4 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.

3. The propagation delay of 1 m of cable (5 ns) is included. 4. $T_D = t_{PLH} - t_{PHL}$. 5. Typical data is at 25°C, V_{CC} = 5 V.

Link Design Considerations

The HFBR-1502/2502 Transmitter/Receiver pair is guaranteed for operation at data rates up to 1 MBd over link distances from 0 to 24 metres with standard cable and from 0 to 34 metres with improved cable. The value of transmitter drive current, I_F, depends on the link distance as shown in Figures 2 and 3. Note that there is a lower limit on the value of I_F for any given distance. The dotted lines in Figures 2 and 3 represent pulsed operation. When operating in the pulsed mode, the conditions in Note 1 must be met. After selecting a value of the transmitter drive current I_F, the value of R_1 in Figure 1 can be calculated as follows:

$$R_1 = \frac{V_{CC} - V_F - V_{OL}\,(75451)}{I_F}$$

For the HFBR-1502/2502 pair, the value of the capacitor, C_1 (Figure 1) must be chosen such that $R_1 C_1 \geq 75$ ns.

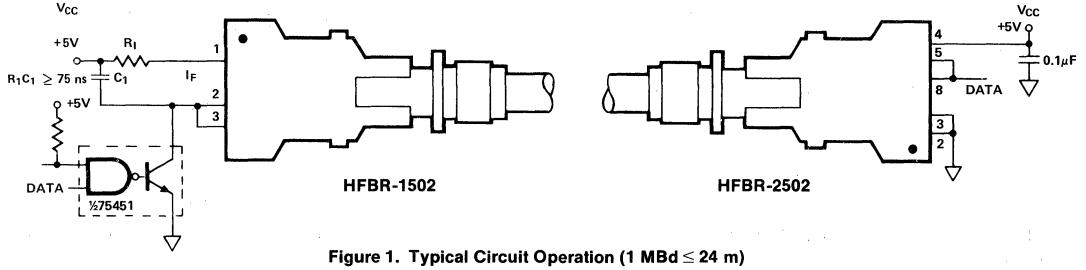


Figure 1. Typical Circuit Operation (1 MBd ≤ 24 m)

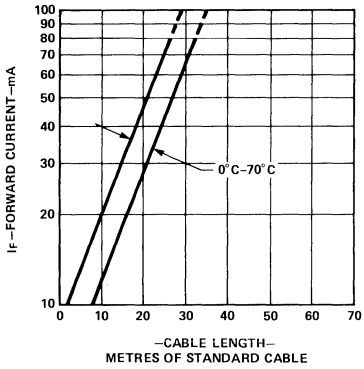


Figure 2. Guaranteed System Performance with HFBR-1502 and HFBR-2502, Standard Cable

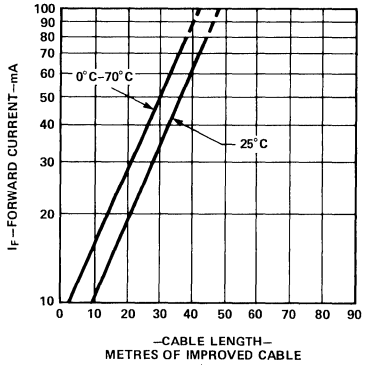


Figure 3. Guaranteed System Performance with HFBR-1502 and HFBR-2502, Improved Cable

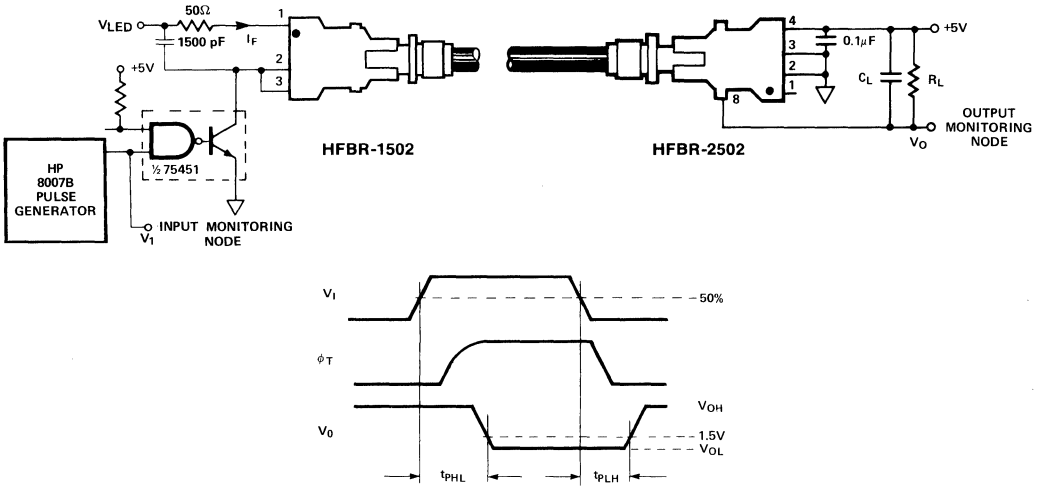


Figure 4. A.C. Test Circuit

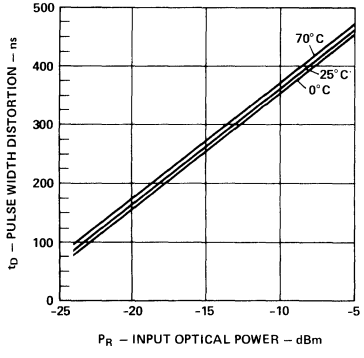


Figure 5. HFBR-1502/2502 Link Pulse Width Distortion vs. Optical Power

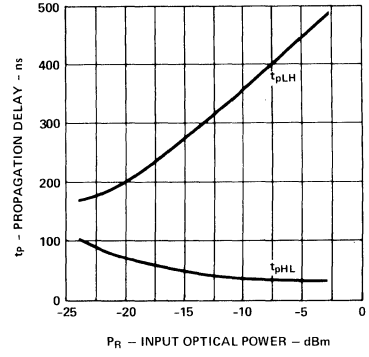


Figure 6. HFBR-1502/2502 Link Propagation Delay vs. Optical Power

Low Current/Extended Distance Link

HFBR-1512 AND HFBR-2503

The low current link requires only 6 mA peak supply current for the transmitter and receiver combined to achieve an 11 m link. Extended distances up to 82 m can be achieved at a maximum transmitter drive current of 60 mA peak. This link can be driven with TTL/LSTTL and most CMOS logic gates.

The black plastic housing of the HFBR-1512 Transmitter is designed to prevent the penetration of ambient light into the cable through the transmitter. This prevents the sensitive receiver from being triggered by ambient light pulses.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units	Ref.
Ambient Temperature	T_A	0	70	°C	
Transmitter Peak Forward Current	$I_{F\,PK}$	2	120	mA	Note 1
Avg. Forward Current	$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	V_{CC}	4.5	5.5	V	Note 2
Output Voltage	V_O		V_{CC}	V	
Fan-Out (TTL)	N		1		

SYSTEM PERFORMANCE Using Standard Cable under recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Data Rate		dc		40	kBd	$t_D \leq 7.0\ \mu s$	
Transmission Distance Standard Cable	ℓ	8	30		m	I_{FPK} = 2 mA, 0–70° C	
		60	100		m	I_{FPK} = 60 mA, 0–70° C	
Transmission Distance Improved Cable	ℓ	11	35		m	I_{FPK} = 2 mA, 0–70° C	
		82	125		m	I_{FPK} = 60 mA, 0–70° C	
Propagation Delay	t_{PLH}		4		μs	R_L = 3.3K Ω, C_L = 30 pF	Fig. 4, 5
	t_{PHL}		2.5		μs	P_R = −25 dBm	Note 3
Pulse Width Distortion	t_D			7.0	μs	$-39 \leq P_R \leq -14$ dBm R_L = 3.3 KΩ, C_L = 30 pF	Fig. 4, 6 Note 4
Bit Error Rate	BER		10^{-9}			P_R = −30 dBm	
EMI Immunity			5000		V/m	P_R = 0 mW	

Notes:
1. For I_{FPK} > 80 mA, the duty factor must be such as to keep $I_{FAV} \leq 80$ mA. In addition, if I_{FAV} > 80 mA, then the pulse width must be equal to or less than 1 ms.
2. It is recommended that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from pin 3 to pin 4 of the receiver.
3. The propagation delay of 1 m of cable (5 ns) is included.
4. $t_D = t_{PLH} - t_{PHL}$.
5. Typical data is at 25° C, V_{CC} = 5 V.

Link Design Considerations

The HFBR-1512/2503 Transmitter/Receiver pair is guaranteed for operation at data rates up to 40 kBd for transmitter drives as low as 2 mA. The value of transmitter drive current, I_F, depends on the link distance as shown in Figures 2 and 3. Note that there is an upper as well as a lower limit on the value of I_F for any given distance. After selecting a value of the transmitter drive current I_F, the value of R_1 in Figure 1 can be calculated as follows:

$$R_1 = \frac{V_{CC} - V_F}{I_F}$$

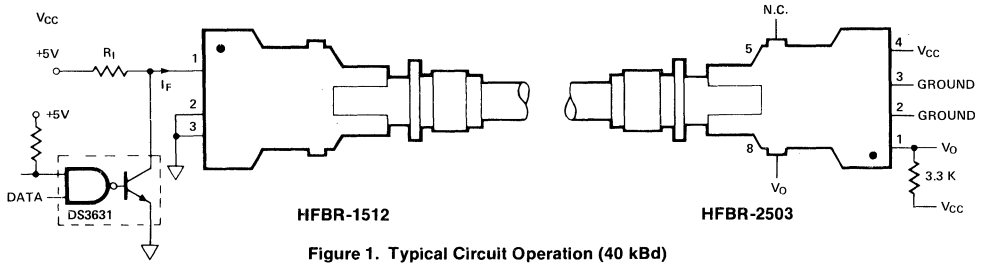


Figure 1. Typical Circuit Operation (40 kBd)

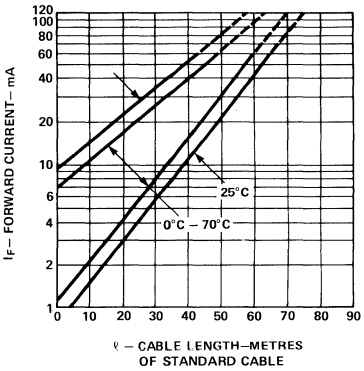


Figure 2. Guaranteed System Performance with HFBR-1512 and HFBR-2503, Standard Cable

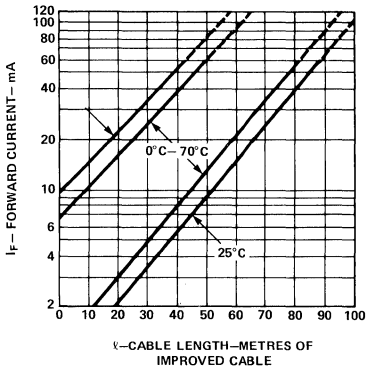


Figure 3. Guaranteed System Performance with HFBR-1512 and HFBR-2503, Improved Cable

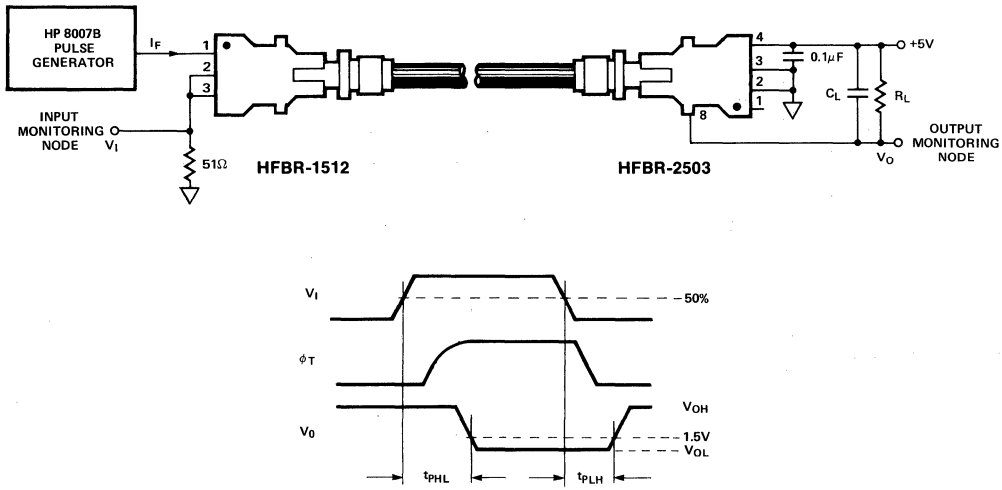


Figure 4. A.C. Test Circuit

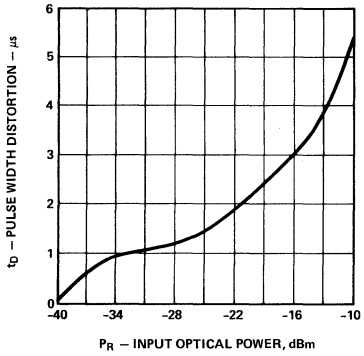


Figure 5. HFBR-1512/2503 Link Pulse Width Distortion vs. Optical Power

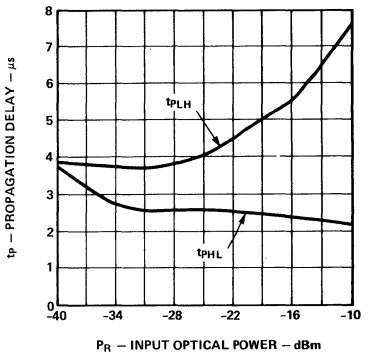


Figure 6. HFBR-1512/2503 Link Propagation Delay vs. Optical Power

Photo Interrupter Links

HFBR-1502/2502
HFBR-1512/2503

These links may be used in optical switches, shaft position sensors, and velocity sensors. They are particularly useful where high voltage, electrical noise, or explosive environments prohibit the use of electromechanical or optoelectronic sensors.

The HFBR-1512/2503 link (20 kHz) has an optical power budget of 24 dB, and the HFBR-1502/2502 link (500 kHz) budget is 10 dB. Total system losses (cable attenuation, air-gap loss, etc) must not exceed the link optical power budget.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min.	Max.	Units	Ref.
Ambient Temperature		T_A	0	70	°C	
Transmitter Peak Forward Current		$I_{F\,PK}$	10	750	mA	Note 1
Avg. Forward Current		$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	HFBR-2503	V_{CC}	4.50	5.50	V	
	HFBR-2502		4.75	5.25		Note 2
Output Voltage	HFBR-2503	V_O		V_{CC}	V	
	HFBR-2502			18		
Fanout (TTL)	HFBR-2503			1		
	HFBR-2502			5		

SYSTEM PERFORMANCE

See HFBR-1502/2502 link data sheet (page 5) and HFBR-1512/2503 link data sheet (page 7) for more design information.

These specifications apply when using Standard Cable and, unless otherwise specified, under recommended operating conditions.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
HFBR-1512/HFBR-2503							
Max. Count Frequency		dc		20	kHz		
Optical Power Budget		25.4			dB	I_{FPK} = 60 mA, 0–70° C	
		27.8	34		dB	I_{FPK} = 60 mA, 25° C	Note 3, 4
HFBR-1502, HFBR-2502							
Max. Count Frequency		dc		500	kHz		
Optical Power Budget		10.4			dB	I_{FPK} = 60 mA, 0–70° C	
		12.8	15.6		dB	I_{FPK} = 60 mA, 25° C	Note 3

Notes:

1. For I_{FPK} > 80 mA, the duty factor must be such as to keep $I_{FAV} \leq 80$ mA. In addition, for I_{FPK} > 80 mA, the following rules for pulse width apply:
   $I_{FPK} \leq 160$ mA: Pulse width ≤ 1 ms
   $I_{FPK} > 160$ mA: Pulse width ≤ 1 μs
2. A bypass capacitor (0.01 μF to 0.1 μF ceramic) connected from pin 3 to pin 4 of the receiver is recommended for the HFBR-2503 and essential for the HFBR-2502. For the HFBR-2502, the total lead length between both ends of the capacitor and the pins should not exceed 20 mm.
3. Optical Power Budget = P_T Min. – $P_{R(L)}$ Min. Refer to HFBR-1502/1512 data sheet, page 11; HFBR-2502 data sheet, page 12; and HFBR-2503 data sheet, page 14 for additional design information.
4. In addition to a minimum power budget, care should be taken to avoid overdriving the HFBR-2503 receiver with too much optical power. For this reason power levels into the receiver should be kept less than –13.7 dBm to eliminate any overdrive with the recommended operating conditions.
5. Typical data is at 25° C, V_{CC} = 5 V.

Link Design Considerations

The HFBR-1512/2503 and HFBR-1502/2502 Transmitter/Receiver pairs are intended for applications where the photo interrupter must be physically separate from the optoelectronic emitter and detector. This separation would be useful where high voltage, electrical noise or explosive environments prohibit the use of electronic devices. To ensure reliable long term operation, links designed for this application should operate with an ample optical power margin $\alpha_M \geq 3$ dB, since the exposed fiber ends are subject to environmental contamination that will increase the optical attenuation of the slot with time. A graph of air gap separation versus attenuation for clean fiber ends with minimum radial error ≤ 0.005 inches (0.127 mm) and angular error ($\leq 3.0°$) is provided in Figure 2. The following equations can now be used to determine the transmitter output power, P_T, for both the overdrive and minimum drive cases. Overdrive is defined as a condition where excessive optical power is delivered to the receiver. The first equation enables the maximum P_T that will not result in receiver overdrive to be calculated for a predetermined link length and slot attenuation. The second equation defines the minimum P_T allowed for link operation.

$$P_T\,(MAX) - P_R\,(MAX) \leq \alpha_{O\,MIN}\ell + \alpha_{SLOT} \qquad \text{Eq. 1}$$

$$P_T\,(MIN) - P_{RL}\,(MIN) \geq \alpha_{O\,MAX}\ell + \alpha_{SLOT} + \alpha_M \qquad \text{Eq. 2}$$

Once P_T (MIN) has been determined in the second equation for a specific link length (ℓ), slot attenuation (α_{SLOT}) and margin (α_M), Figure 3 can then be used to find I_F.

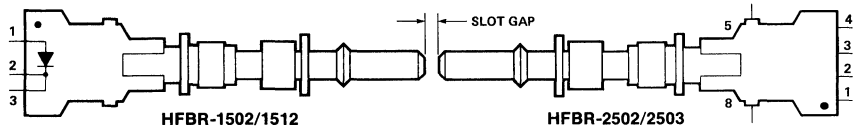


Figure 1. Typical Slot Interrupter Configuration. Refer to 1 MBd or Low Current Links for Schematic Diagrams

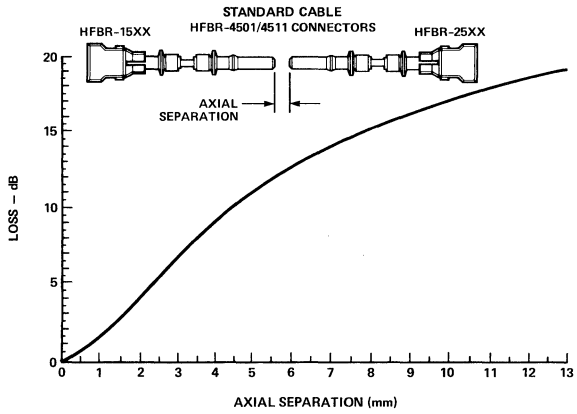


Figure 2. Typical Loss vs. Axial Separation

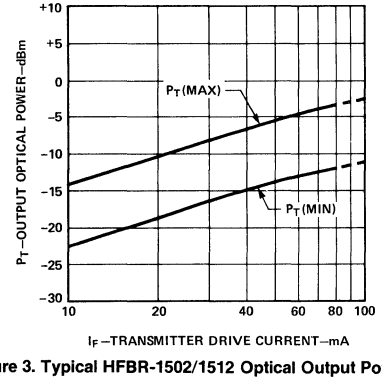


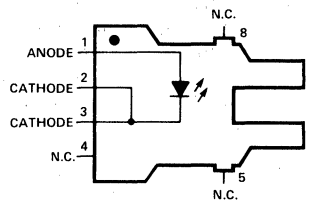
Figure 3. Typical HFBR-1502/1512 Optical Output Power vs. Transmitter I_F (0—70° C)

665 nm Transmitters

HFBR-1502/HFBR-1510 and HFBR-1512

The HFBR-1510/1502/1512 Transmitter modules incorporate a 665 nm LED emitting at a low attenuation wavelength for the HFBR-3510/3610 plastic fiber optic cable. The transmitters can be easily interfaced to standard TTL logic. The optical power output of the HFBR-1510/1512/1502 is specified at the end of 0.5 m of cable. The HFBR-1512 output optical power is tested and guaranteed at low drive currents.

HFBR-1510/1512/1502 Transmitter



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	−40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec.	
Peak Forward Input Current		$I_{F\,PK}$		1000	mA	Note 2
Average Forward Input Current		$I_{F\,AV}$		80	mA	
Reverse Input Voltage		V_R		5	V	

Electrical/Optical Characteristics 0° C to +70° C Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Transmitter Output Optical Power	HFBR-1510	P_T	−16.5		−7.6	dBm	I_F = 60 mA, 0–70° C	
			−14.3		−8.0	dBm	I_F = 60 mA, 25° C	
	HFBR-1502 and HFBR-1512	P_T	−13.6		−4.5	dBm	I_F = 60 mA, 0–70° C	Fig. 2
			−11.2		−5.1	dBm	I_F = 60 mA, 25° C	Note 4
	HFBR-1512	P_T	−35.5			dBm	I_F = 2 mA, 0–70° C	Note 3
Output Optical Power Temperature Coefficient		$\frac{\Delta P_T}{\Delta T}$		−0.026		dB/° C		
Peak Emission Wavelength		λ_{PK}		665		nm		
Forward Voltage		V_F	1.45	1.67	2.02	V	I_F = 60 mA	
Forward Voltage Temperature Coefficient		$\frac{\Delta V_F}{\Delta T}$		−1.37		mV/° C		Fig. 1
Effective Diameter		D_T		1		mm		
Numerical Aperture		N.A.		0.5				
Reverse Input Breakdown Voltage		V_{BR}	5.0	12.4		V	I_F = −10 μA, T_A = 25° C	
Diode Capacitance		C_O		86		pF	V_F = 0, f = 1 MHz	
Rise and Fall Time		t_R, t_F		50		ns	10% to 90%	

Notes:
1. 1.6 mm below seating plane.
2. 1 μs pulse, 20 μs period.
3. Measured at the end of 0.5 m standard Fiber Optic Cable with large area detector.
4. Optical power, P (dBm) = 10 Log P (μW)/1000 μW.
5. Typical data is at 25° C.

WARNING. When viewed under some conditions, the optical port of the Transmitter may expose the eye beyond the Maximum Permissible Exposure recommended in ANSI Z-136-1, 1981. Under most viewing conditions there is no eye hazard.

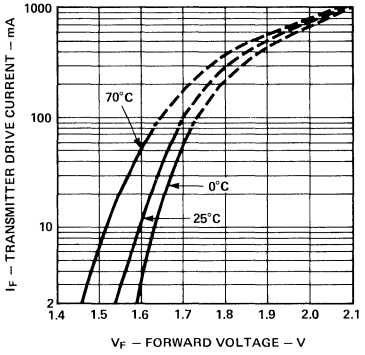


Figure 1. Typical Forward Voltage vs. Drive Current for HFBR-1510/1502/1512

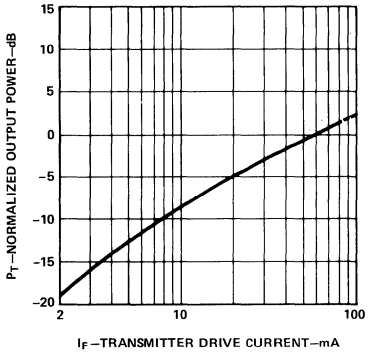


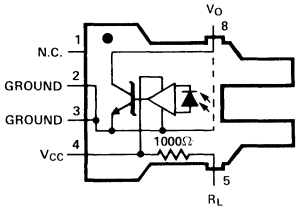
Figure 2. Normalized HFBR-1510/1502/1512 Typical Output Optical Power vs. Drive Current

Receivers

HFBR-2501 (5 MBd) and HFBR-2502 (1 MBd)

The HFBR-2501/2502 Receiver modules feature a shielded integrated photodetector and wide bandwidth DC amplifier for high EMI immunity. A Schottky clamped open-collector output transistor allows interfacing to common logic families and enables "wired-OR" circuit designs. The open collector output is specified up to 18V. An integrated 1000 ohm resistor internally connected to V_{CC} may be externally jumpered to provide a pull-up for ease-of-use with +5V logic. The combination of high optical power levels and fast transitions falling edge could result in distortion of the output signal (HFBR-2502 only), that could lead to multiple triggering of following circuitry.

HFBR-2501/2502 Receiver



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp			260	°C	Note 1
	Time			10	sec	
Supply Voltage		V_{CC}	-0.5	7	V	Note 6
Output Collector Current		I_O		25	mA	
Output Collector Power Dissipation		P_{OD}		40	mW	
Output Voltage		V_O	-0.5	18	V	
Pullup Voltage		V_{RL}	-0.5	V_{CC}	V	

Electrical/Optical Characteristics $0°C$ to $+70°C$, $4.75 \leq V_{CC} \leq 5.25$ Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Receiver Input Optical Power Level for Logic "0"	HFBR-2501	$P_{R(L)}$	-21.6		-9.5	dBm	0-70°C, V_{OL} = 0.5 V I_{OL} = 8 mA	Note 2, 3
			-21.6		-8.7	dBm	25°C, V_{OL} = 0.5 V I_{OL} = 8 mA	
	HFBR-2502	$P_{R(L)}$	-24			dBm	0-70°C, V_{OL} = 0.5 V I_{OL} = 8 mA	
			-24			dBm	25°C, V_{OL} = 0.5 V I_{OL} = 8 mA	
Input Optical Power Level for Logic "1"		$P_{R(H)}$			-43	dBm	V_{OH} = 5.25 V, $I_{OH} \leq 250\ \mu A$	Note 2
High Level Output Current		I_{OH}		5	250	μA	V_O = 18 V, P_R = 0	Note 4
Low Level Output Voltage		V_{OL}		0.4	0.5	V	I_{OL} = 8 mA, $P_R = P_{RL\ MIN}$	Note 4
High Level Supply Current		I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V, P_R = 0 μW	Note 4
Low Level Supply Current		I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V, P_R = -12.5 dBm	Note 4
Effective Diameter		D_R		1		mm		
Numerical Aperture		N.A.$_R$		0.5				
Internal Pull-Up Resistor		R_L	680	1000	1700	Ohms		

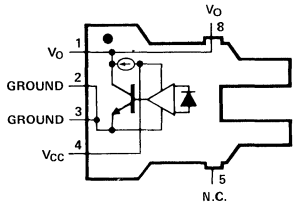
Notes:
1. 1.6 mm below seating plane.
2. Optical flux, P (dBm) = 10 Log P (μW)/1000 μW.
3. Measured at the end of standard Fiber Optic Cable with large area detector.
4. R_L is open.
5. Typical data is at 25° C, V_{CC} = 5 V.
6. It is essential that a bypass capacitor 0.01 μF to 0.1 μF be connected from pin 3 to pin 4 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.

High Sensitivity Receiver

HFBR-2503

The blue plastic HFBR-2503 Receiver module has a sensitivity of -39 dBm. It features an integrated photodetector and DC amplifier for high EMI immunity. The output is an open collector with a 150 μA internal current source pull-up and is compatible with TTL/LSTTL and most CMOS logic families. For minimum rise time add an external pull-up resistor of at least 3.3K ohms. V_{CC} must be greater than or equal to the supply voltage for the pull-up resistor.

HFBR-2503 Receiver



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp			260	°C	Note 1
	Time			10	sec	
Supply Voltage		V_{CC}	-0.5	7	V	Note 7
Output Collector Current (Average)		I_O	-1	5	mA	
Output Collector Power Dissipation		P_{OD}		25	mW	
Output Voltage		V_O	-0.5	V_{CC}	V	

Electrical/Optical Characteristics 0° C to +70° C, 4.5 ≤ V_{CC} ≤ 5.5 Unless Otherwise Specified

Parameter		Symbol	Min.	Typ. (5)	Max.	Units	Conditions	Ref.
Receiver Input Optical Power Level for Logic "0"	HFBR-2503	$P_{R(L)}$	-39		-13.7	dBm	0-70° C, $V_O = V_{OL}$ I_{OL} = 3.2 mA	Note 2, 3, 4
			-39		-13.3	dBm	25° C, $V_O = V_{OL}$ I_{OL} = 3.2 mA	
Input Optical Power Level for Logic "1"		$P_{R(H)}$			-53	dBm	V_{OH} = 5.5V, $I_{OH} \leq 40$ μA	Note 2
High Level Output Voltage		V_{OH}	2.4			V	I_{OH} = -40 μA, P_R = 0 μW	
Low Level Output Voltage		V_{OL}			0.4	V	I_{OL} = 3.2 mA, $P_R = P_{RL\ MIN}$	Note 6
High Level Supply Current		I_{CCH}		1.2	1.9	mA	V_{CC} = 5.5V, P_R = 0 μW	
Low Level Supply Current		I_{CCL}		2.9	3.7	mA	V_{CC} = 5.5V, $P_R \geq P_{RL}$ (MIN)	Note 6
Effective Diameter		D_R		1		mm		
Numerical Aperture		N.A.R		0.5				

Notes:

1. 1.6 mm below seating plane.
2. Optical flux, P (dBm) = 10 Log P (μW)/1000 μW.
3. Measured at the end of the standard Fiber Optic Cable with large area detector.
4. Because of the very high sensitivity of the HFBR-2503, the digital output may switch in response to ambient light levels when a cable is not occupying the receiver optical port. The designer should take care to filter out signals from this source if they pose a hazard to the system.
5. Typical data is at 25° C, V_{CC} = 5 V.
6. Including current in 3.3K pull-up resistor.
7. It is recommended that a bypass capacitor 0.01 μF to 0.1 μF ceramic be connected from pin 3 to pin 4 of the receiver.

Snap-in Fiber Optic Connector, Bulkhead Feedthrough/Splice and Polishing Tools

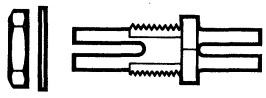
HFBR-4501/4511 CONNECTORS
HFBR-4505/4515 BULKHEAD FEEDTHROUGHS

The HFBR-4501 and HFBR-4511 snap-in connectors terminate low cost plastic fiber cable and mate with the Hewlett-Packard HFBR-0500 family of fiber optic transmitters and receivers. They are quick and easy to install. The metal crimp ring provides strong and stable cable retention and the polishing technique ensures a smooth optical finish which results in consistently high optical coupling efficiency.

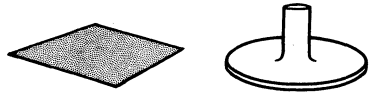
The HFBR-4505 and HFBR-4515 bulkhead feedthroughs mate two snap-in connectors and can be used either as an in-line splice or as a panel feedthrough for plastic fiber cable. The connector to connector loss is low and repeatable.

HFBR-4501 (GRAY)/4511 (BLUE) CONNECTOR

HFBR-4505 (GRAY)/4515 (BLUE) BULKHEAD FEEDTHROUGH

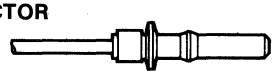


HFBR-4595 POLISHING KIT

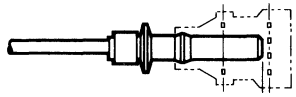


Applications

- **CONNECTOR**

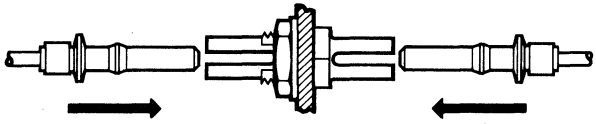


TERMINATION FOR HEWLETT-PACKARD PLASTIC FIBER OPTIC CABLE

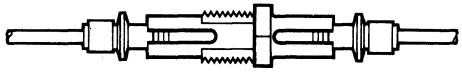


INTERFACE TO HEWLETT-PACKARD HFBR-15XX/25XX SNAP-IN FIBER OPTIC LINK COMPONENTS

- **BULKHEAD FEEDTHROUGH**



BULKHEAD FEEDTHROUGH OR PANEL MOUNTING OF HFBR-45XX CONNECTORS



IN-LINE SPLICE FOR PLASTIC FIBER OPTIC CABLE

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	+75	°C	
Operating Temperature	T_A	0	+70	°C	
Nut Torque HFBR-4505/4515	T_N		$\frac{0.7}{100}$	$\frac{\text{N-m}}{\text{OzF-IN}}$	1

Notes:
1. Recommended nut torque is $\frac{0.57}{80}\ \frac{\text{N-m}}{\text{OzF-IN}}$

Mechanical/Optical Characteristics 0° to 70°C Unless Otherwise Specified.

Typical Data at 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Retention Force Connector/Module HFBR-4501/4511 to HFBR-15XX/25XX	F_{RC}		6.8		N	
Tensile Force Connector/Cable	F_T		22		N	
HFBR-4505/4515 Conn. to Conn. Loss	α_{CC}	0.7	1.5	2.8	dB	2, 3
Retention Force Connector/ Bulkhead HFBR-4501/4511 to HFBR-4505/4515	F_{RB}		7.8		N	

Notes:
2. Factory polish or field polish per recommended procedure.
3. Module to connector insertion loss is factored into the transmitter output optical power and the receiver input optical power level specifications.

Note:
For applications where frequent temperature cycling over extremes is expected please contact Hewlett-Packard for alternate connectoring techniques.

Cable Terminations

The following easy procedure describes how to make cable terminations. It is ideal for both field and factory installaiton. If a high volume connectoring technique is required please contact your Hewlett-Packard sales engineer for the recommended procedure and equipment.

Connectoring the cable is accomplished with the Hewlett-Packard HFBR-4595 Polishing Kit consisting of a Polishing Fixture and 600 grit abrasive paper and 3 micron pink lapping film (3M Company, OC3-14). No adhesive material is needed to secure the cable in the connector, and the connector can be used immediately after polishing.

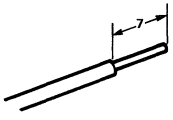
Connectors may be easily installed on the cable ends with readily available tools. Materials needed for the terminating procedure are:

1) Plastic Fiber Optic Cable
2) HFBR-4595 Polishing Kit
3) HFBR-4501 Gray Connector and Crimp Ring
4) HFBR-4511 Blue Connector and Crimp Ring
5) Industrial razor blade or wire cutters
6) 16 gauge latching wire strippers
7) Crimp Tool, AMP 90364-2

Step 1

The zip cord structure of the duplex cable permits easy separation of the channels. The channels should be separated approximately 50 mm (2.0 in.) back from the ends to permit connecting and polishing.

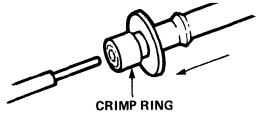
After cutting the cable to the desired length, strip off approximately 7 mm (0.3 in) of the outer jacket with the 16 gauge wire strippers. Excess webbing on duplex cable may have to be trimmed to allow the connector to slide over the cable.



Step 2

Place the crimp ring and connector over the end of the cable; the fiber should protrude about 3 mm (0.12 in.) through the end of the connector. Carefully position the ring so that it is entirely on the connector and then crimp the ring in place with the crimping tool.

Note: *Place the gray connector on the cable end to be connected to the transmitter and the blue connector on the cable end to be connected to the receiver to maintain the color coding (both connectors are the same mechanically).*



Step 3

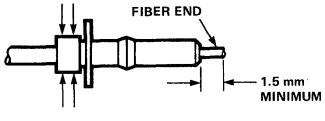
Any excess fiber protruding from the connector end may be cut off; however, the trimmed fiber should extend at least 1.5 mm (0.06 in.) from the connector end.

Insert the connector fully into the polishing fixture with the connector end protruding from the bottom of the fixture.

For high volume connectoring use the hardened steel HFBR-4596 polishing fixture.

Note: *The four dots on the bottom of the polishing fixture are wear indicators. Replace the polishing fixture when any dot is no longer visible.*

Place the 600 grit abrasive paper on a flat smooth surface. Pressing down on the connector, polish the fiber and the connector until the connector is flush with the end of the polishing fixture. Wipe the connector and fixture with a clean cloth or tissue.

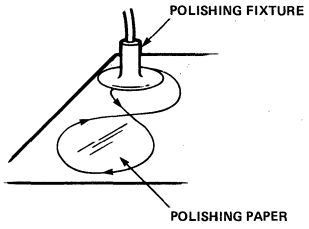


Step 4

Place the flush connector and polishing fixture on the dull side of the 3 micron pink lapping film and continue to polish the fiber and connector for approximately 25 strokes. The fiber end should be flat, smooth and clean.

The cable can now be used.

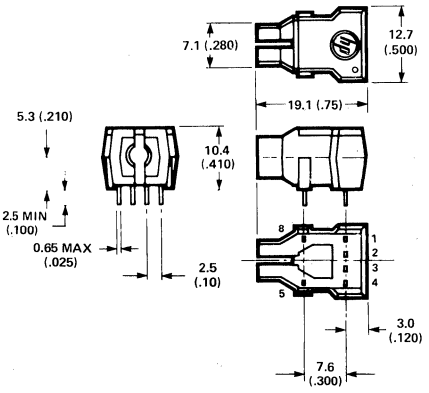
Note: *Use of the pink lapping film fine polishing step results in approximately a 2 dB improvement in coupling performance of either a transmitter-receiver link or a bulkhead/splice over 600 grit polish alone. This polish is comparable to Hewlett-Packard's factory polish. The fine polishing step may be omitted where an extra 2 dB of optical power is not essential as with short link lengths.*



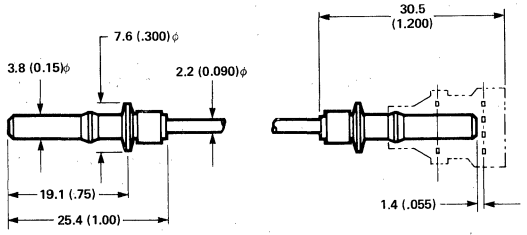
Mechanical Dimensions

All dimensions in mm (inches).
All dimensions ±0.25 mm unless otherwise specified.

HFBR-15XX (GRAY OR BLACK)/250X (BLUE) MODULE

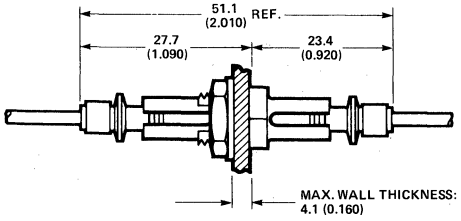


HFBR-4501 (GRAY)/4511 (BLUE) CONNECTOR

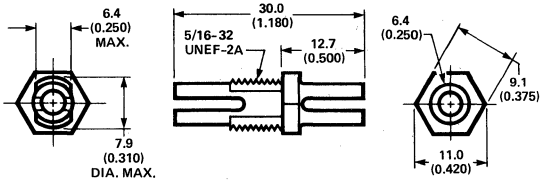


CONNECTORS DIFFER ONLY IN COLOR

BULKHEAD FEEDTHROUGH WITH TWO HFBR-4501/4511 CONNECTORS

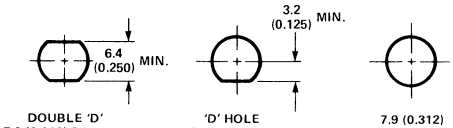


HFBR-4505 (GRAY)/4515 (BLUE) BULKHEAD FEEDTHROUGH



BULKHEAD FEEDTHROUGHS DIFFER ONLY IN COLOR

PANEL MOUNTING



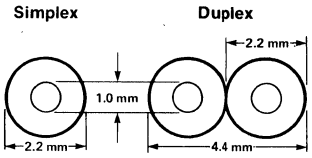
DOUBLE 'D'
7.9 (0.312) DIA. MIN.

'D' HOLE
7.9 (0.312) DIA. MIN.

7.9 (0.312)
HOLE MIN.

DIMENSIONS IN mm (INCHES)
ALL DIMENSIONS ±0.2 mm UNLESS NOTED.

FIBER OPTIC CABLE CONSTRUCTION



HEWLETT PACKARD

MINIATURE FIBER OPTIC LOGIC LINK

HFBR-1202
HFBR-2202
HFBR-4202

Features

- DC TO 5 MBAUD DATA RATE
- MAXIMUM LINK LENGTH
  625 Metres (Guaranteed)
  1600 Metres (Typical)
- TTL/CMOS COMPATIBLE OUTPUT
- MINIATURE, RUGGED METAL PACKAGE
- SINGLE +5V RECEIVER POWER SUPPLY
- INTERNALLY SHIELDED RECEIVER FOR EMI/RFI IMMUNITY
- PCB AND PANEL MOUNTABLE
- LOW POWER CONSUMPTION

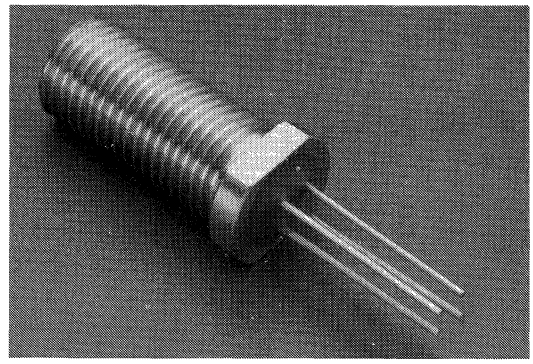
Applications

- EMC REGULATED SYSTEMS (FCC, VDE)
- EXPLOSION PROOF SYSTEMS IN OIL INDUSTRY/CHEMICAL PROCESS CONTROL INDUSTRY
- SECURE DATA COMMUNICATIONS
- WEIGHT SENSITIVE SYSTEMS (e.g. Avionics, Mobile Stations)
- HIGH VOLTAGE ISOLATION IN POWER GENERATION

Description

The HFBR-1202 Transmitter and HFBR-2202 Receiver are SMA style connector compatible fiber optic link components. Distances to 1600 metres at data rates up to 5 MBaud are achievable with these components.

The HFBR-1202 Transmitter contains a high efficiency GaAlAs emitter operating at 820 nm. Consistent coupling



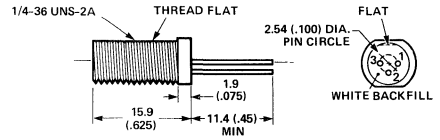
efficiency is assured by factory alignment of the LED with the optical axis of the package. Power coupled into the fiber varies less that 4 dB from part to part at a given temperature and drive current. The benefit of this is reduced dynamic range requirements on the receiver.

The HFBR-2202 Receiver incorporates a photo IC containing a photodetector and dc amplifier. An open collector Schottky transistor on the IC provides logic compatibility. The combination of an internal EMI shield, the metal package and an isolated case ground provides excellent immunity to EMI/RFI. For unusually severe EMI/ESD environments, a snap-on metal shield is available. The receiver is easily identified by the black epoxy backfill.

The HFBR-1202 Transmitter and HFBR-2202 Receiver are compatible with SMA style connectors, types A and B (see Figure 11.

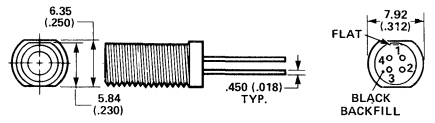
Mechanical Dimensions

HFBR-1202 TRANSMITTER



PIN	FUNCTION
1	ANODE
2	CATHODE
3	CASE

HFBR-2202 RECEIVER



PIN	FUNCTION
1	CASE
2	V_{CC}
3	DATA
4	COMMON

DIMENSIONS IN MILLIMETRES (INCHES)
UNLESS OTHERWISE SPECIFIED, THE TOLERANCES ARE:
.X ± .51 mm (.XX ± .02 IN)
.XX ± .13 mm (.XXX ± .005 IN)

System Design Considerations

The Miniature Fiber Optic Logic Link is guaranteed to work over the entire range of 0 to 625 metres at a data rate of dc -5 MBd, with arbitrary data format and typically less than 25% pulse width distortion, if the Transmitter is driven with I_F = 40 mA, R_1 = 82Ω. If it is desired to economize on power or achieve lower pulse distortion, then a lower drive current (I_F) may be used. The following example will illustrate the technique for optimizing I_F.

EXAMPLE: Maximum distance required = 250 metres. From Figure 2 the worst case drive current = 20 mA. From the Transmitter data — V_F = 1.8V (max.).

$$R_1 = \frac{V_{CC} - V_F}{I_F} = \frac{5 - 1.8V}{20\ mA} = 160\Omega$$

The optical power margin between the typical and worst case curves (Figure 2) at 250 metres is 4 dB. To calculate the worst case pulse width distortion at 250 metres, see Figure 8. The power into the Receiver is P_{RL} + 4 dB = -20 dBm. Therefore, the typical distortion is 40 ns or 20% at 5 MBd.

CABLE SELECTION

The link performance specifications on the following page are based on using cables that contain glass-clad silica fibers with a 100 μm core diameter and 140 μm cladding diameter. This fiber type is now a user accepted standard for local data communications links (RS-458, Class I, Type B). The HFBR-1202 Transmitter and HFBR-2202 Receiver are optimized for use with the 100/140 μm fiber. There is, however, no fundamental restriction against using other fiber types. Before selecting an alternate fiber type, several parameter need to be carefully evaluated.

will significantly affect the optical power coupled into the fiber are as follows:

a. **Fiber Core Diameter.** As the core diameter is increased, the optical power coupled increases, leveling off at about 250 μm diameter.
b. **Numerical Aperture (NA).** As the NA is increased, the optical power coupled increases, leveling off at an NA of about 0.34.
c. **Index Profile (α).** The Index profile parameter of fibers varies from 2 (fully graded index) to infinite (step index). Some gains in coupled optical power can be achieved at the expense of bandwidth, when α is increased.

In addition to the optical parameters, the environmental performance of the selected fiber/cable must be evaluated. Finally, the ease of installing connectors on the selected fiber/cable must be considered. Given the large number of parameters that must be evaluated when using a non-standard fiber, it is recommended that the 100/140 μm fiber be used unless unusual circumstances warrant the use of an alternate fiber/cable type.

SMA STYLE CONNECTORS

The HFBR-1202/2202 is compatible with either the Type A or Type B SMA style fiber optic connector (see Figure 11). The basic difference between the two connectors is the plastic half-sleeve on the stepped ferrule tip of the Type B connector. This step provides the capability to use a full length plastic sleeve to ensure good alignment of two connectors for an inline splice. Hewlett-Packard offers connectored cable that utilizes the Type A connector system because of the inherent environmental advantages of metal-to-metal interfaces.

Typical Circuit Configuration

NOTE:
IT IS ESSENTIAL THAT A BYPASS CAPACITOR (0.01 μF to 0.1 μF CERAMIC) BE CONNECTED FROM PIN 2 TO PIN 4 OF THE RECEIVER. TOTAL LEAD LENGTH BETWEEN BOTH ENDS OF THE CAPACITOR AND THE PINS SHOULD NOT EXCEED 20 mm.

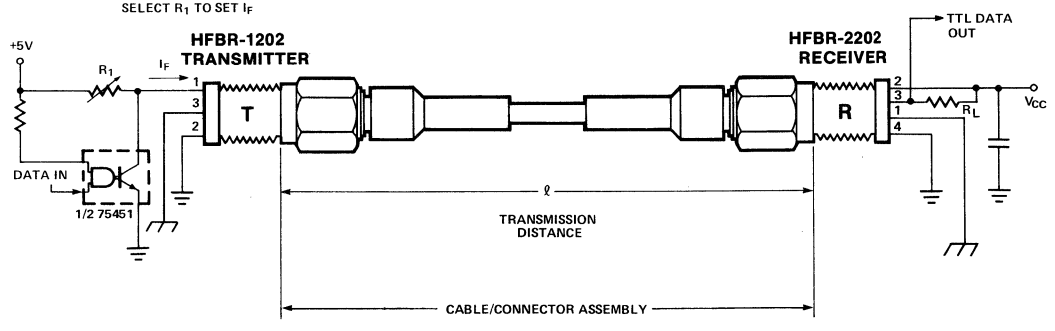


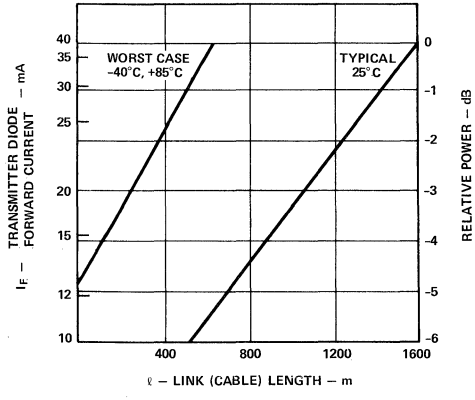
Figure 1.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Reference
TRANSMITTER					
Ambient Temperature	T_A	-40	+85	°C	
Peak Forward Input Current	$I_{F,PK}$		40	mA	Note 7
Average Forward Input Current	I_{FAV}		40	mA	Note 7
RECEIVER					
Ambient Temperature	T_A	-40	+85	°C	
Supply Voltage	V_{CC}	4.75	5.25	V	
Fan Out (TTL)	N		5		Note 3, Fig. 1
CABLE (see SMA connectored cable data sheet)					

System Performance -40°C to +85°C unless otherwise specified

Parameter	Symbol	Min.[1]	Typ.	Max.	Units	Conditions	Reference
Transmission Distance	ℓ	625	1600		Metres		Fig. 2, Note 9
Data Rate Synchronous		dc		5	MBaud		Note 10
Asynchronous		dc		2.5	MBaud		Note 10, Fig. 8
Propagation Delay LOW to HIGH	t_{PLH}		82		nsec	T_A = 25°C, P_R = -21 dBm $I_{F,PK}$ = 15 mA ℓ = 1 metre	Fig. 7, 8, 9
Propagation Delay HIGH to LOW	t_{PHL}		55		nsec		
System Pulse Width Distortion	t_D		27		nsec		
Bit Error Rate	BER			10^{-9}		Data Rate ≤5 MBaud P_R > -24 dBm (4μW)	



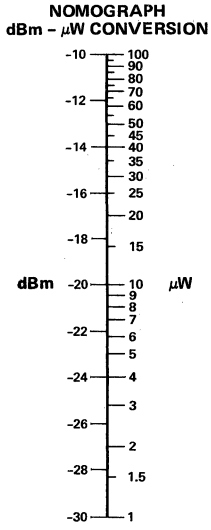
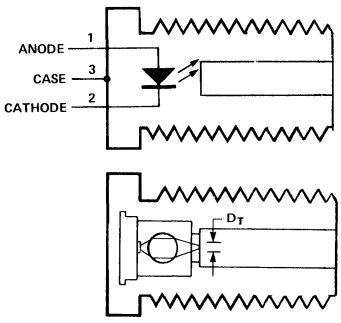


Figure 2. System Performance: HFBR-1202/HFBR-2202 with HP's 100/140 μm fiber cable

HFBR-1202 TRANSMITTER

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Reference
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	-40	+85	°C	Note 13
Lead Soldering Cycle	Temp.			+260	°C	Note 2
	Time			10	sec	
Forward Input Current	Peak	$I_{F,PK}$		40	mA	Note 7
	Average	$I_{F,AV}$		40	mA	
Reverse Input Voltage		V_R		2.5	V	



Electrical/Optical Characteristics -40° C to +85° C unless otherwise specified

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions	Reference
Forward Voltage	V_F		1.5	1.8	V	I_F = 40 mA	Figure 5
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-0.91		mV/° C	I_F = 40 mA	Figure 5
Reverse Breakdown Voltage	V_{BR}	2.5	4.0		V	I_R = 100 μA	
Numerical Aperture	NA		.34				
Optical Port Diameter	D_T		250		μm		Note 11
Peak Emission Wavelength	λ_P		820		nm		Figure 6
Peak Output Optical Power Coupled into HFBR-3000 Fiber Cable/Connector Assembly, 100/140 μm	P_T	-17	-16	-13	dBm	I_F = 40 mA	Figure 3
		20	25	50	μW	T_A = 25° C	Notes 4, 15
		-18		-12.3	dBm	I_F = 40 mA	
		15.8		59	μW	-40° C < T_A < 85° C	
Output Optical Power Coupled into 50/125 μm Fiber	P_T		-24		dBm	I_F = 40 mA	Figure 3
			4		μW	T_A = 25° C	Notes 14, 15
Output Optical Power Coupled into Siecor 100/140 μm Fiber Cable or Equivalent	P_T		-18		dBm	I_F = 40 mA T_A = 25° C	Figure 3 Notes 15, 16
Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-.017		dB/° C		Figure 4

Dynamic Characteristics -40° C to +85° C unless otherwise specified

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions	Reference
Propagation Delay LOW to HIGH	t_{PLH}		17		nsec	$I_{F\,PK}$ = 10 mA	Note 8 Figure 7
Propagation Delay HIGH to LOW	t_{PHL}		6		nsec		

Notes:

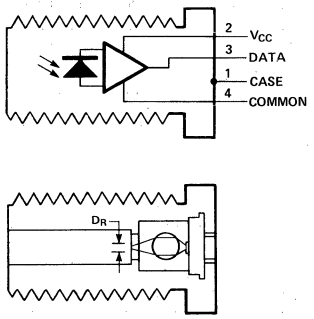
1. Typical data at T_A = 25° C, V_{CC} = 5.0V dc.
2. 2.0 mm from where leads enter case.
3. 8 mA load (5 x 1.6 mA). R_L = 560Ω.
4. Measured at the end of 1.0 metre HP's 100/140 μm Fiber Optic Cable with large area detector and cladding modes stripped, terminated with the appropriate type of connector. This assembly approximates a Standard Test Fiber. The fiber NA is 0.28, measured at the end of greater than 300 metres length of fiber, the NA being defined as the sine of the half angle determined by the 10% intensity points.
5. Measured at the end of HP's 100/140 μm Fiber Optic Cable with large area detector.
6. When changing microwatts to dBm, the optical flux is referenced to one milliwatt (1000 μW).
   Optical Flux, $P\,(dBm) = 10 \log \frac{P\,(\mu W)}{1000\,\mu W}$
7. I_{FPK} should not be less than 10 mA in the "ON" state. This is to avoid the long turn-on time that occurs at low input current. I_{FAV} may be arbitrarily low, as there is no duty factor restriction.

WARNING: OBSERVING THE TRANSMITTER OUTPUT POWER UNDER MAGNIFICATION MAY CAUSE INJURY TO THE EYE. When viewed with the unaided eye, the infrared output is radiologically safe; however, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	-40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	Note 2
	Time			10	sec	
Supply Voltage		V_{CC}	-0.5	+7.0	V	
Output Current		I_O		25	mA	
Output Voltage		V_O	-0.5	+18.0	V	
Output Collector Power Dissipation		$P_{O,AV}$		40	mW	

HFBR/2202 RECEIVER



Electrical/Optical Characteristics

-40° C to +85° C and 4.75 ≤ V_{CC} ≤ 5.25 V unless otherwise specified.

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions	Reference
High Level Output Current	I_{OH}		5	250	μA	V_O = 18V P_R < -40 dBm	
Low Level Output Voltage	V_{OL}		0.4	0.5	V	I_O = 8 mA P_R > -24 dBm	
High Level Supply Current	I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V P_R < -40 dBm	
Low Level Supply Current	I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V P_R > -24 dBm	
Optical Port Diameter	D_R		700		μm		Note 12
Numerical Aperture	NA		.32				

Dynamic Characteristics

-40° C to +85° C and 4.75 ≤ V_{CC} ≤ 5.25 V unless otherwise specified.

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions	Reference
Input Power Level Logic HIGH	P_{RH}			-40 0.1	dBm μW	λ_P = 820 nm	Note 5
Input Power Level Logic LOW	P_{RL}	-25.4		-11.2	dBm	T_A = +25° C	Fig. 4, Note 5
		2.9		76	μW		
		-24		-12.0	dBm	-40 < T_A < 85° C	
		4.0		63	μW		
Propagation Delay LOW to HIGH	t_{PLHR}		65		nsec	T_A = 25° C, P_R = -21 dBm	Note 8, Fig. 7
Propagation Delay HIGH to LOW	t_{PHLR}		49		nsec		

Notes:

8. Propagation delay through the system is the result of several sequentially-occurring phenomena. Consequently it is a combination of data-rate-limiting effects and of transmission-time effects. Because of this, the data-rate limit of the system must be described in terms of time differentials between delays imposed on falling and rising edges.

   As the cable length is increased, the propagation delays increase at 5 ns per metre of length increase. Data rate, as limited by pulse width distortion, is not affected by increasing cable length if the optical power level at the Receiver is maintained.
9. Worst case system performance is based on worst case performance of individual components: transmitter at +85° C, receiver at -40° C and cable at- 20° C.
10. Synchronous data rate limit is based on these assumptions: (a) 50% duty factor modulation, e.g. Manchester I or BiPhase (Manchester II); (b) continuous data; (c) PLL (Phase Lock Loop) demodulation; (d) TTL threshold.

    Asynchronous data rate limit is based on these assumptions: (a) NRZ data; (b) arbitrary timing — no duty factor restriction; (c) TTL threshold.

    The EYE pattern describes the timing range within which there is no uncertainty of the logic state, relative to a specific threshold, due to either noise or intersymbol (prop. delay) effects.
11. D_T is measured at the plane of the fiber face and defines a diameter where the optical power density is within 10 dB of its maximum.
12. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
13. HP's 100/140 μm Fiber Cable is specified at a narrower temperature range, -20° C to 85° C.
14. Measured at the end of 1.0 metre 50/125 μm fiber with large area detector and cladding modes stripped, approximating a Standard Test Fiber. The fiber NA is 0.21, measured at the end of a 2.0 metre length, the NA being defined as the sine of the half angle determined by the 5% of peak intensity points.
15. Output Optical Power into connectored fiber cable other than HP's Fiber Optic Cable/Connector Assemblies may be different than specified because of mechanical tolerances of the connector, quality of the fiber surface, and other variables.
16. Measured at the end of 1.0 metre Siecor 100/140 μm fiber cable or equivalent, with large area detector and cladding modes stripped, terminated with the appropriate type of connector. This assembly approximates a Standard Test Fiber. The fiber NA is 0.275, measured at the end of a 2.0 metre length, the NA being defined as the sine of the half angle determined by the 5% of peak intensity points.

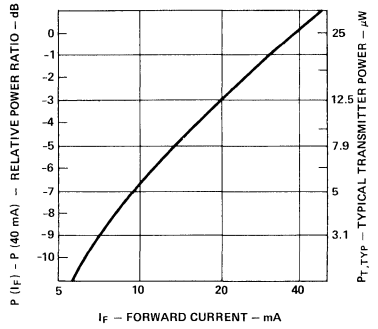


Figure 3. Normalized Transmitter Output vs. Forward Current

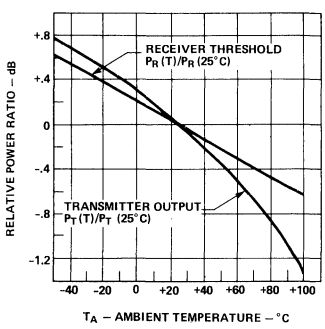


Figure 4. Normalized Thermal Effects in Transmitter Output, Receiver Threshold, and Link Performance (Relative Threshold)

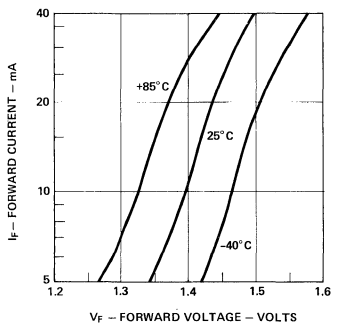


Figure 5. Forward Voltage and Current Characteristics for the Transmitter LED.

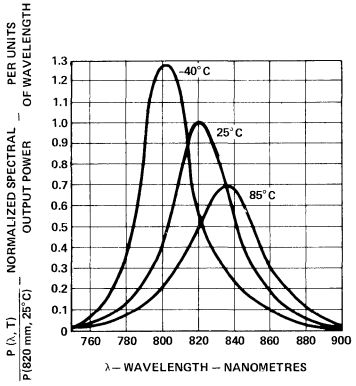


Figure 6. Transmitter Spectrum Normalized to the Peak at 25° C

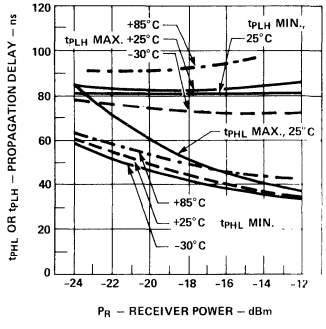


Figure 7. Propagation Delay through System with One Metre of Cable

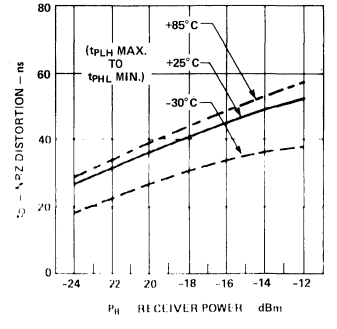
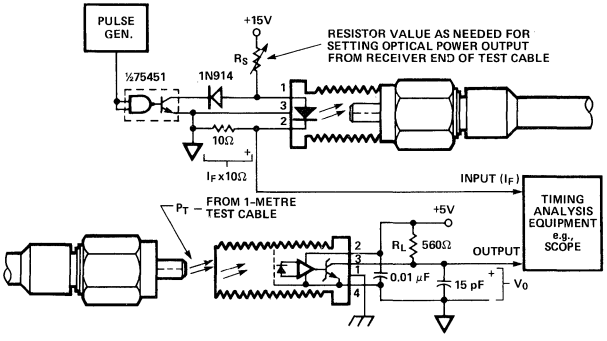


Figure 8. Worst-Case Distortion of NRZ EYE-pattern with Pseudo Random Data at 5 Mb/s. (see note 10)



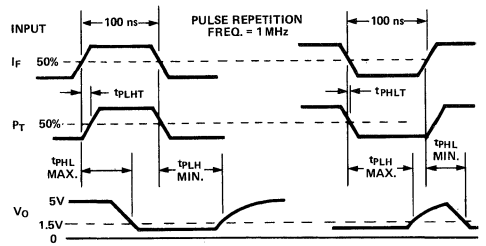
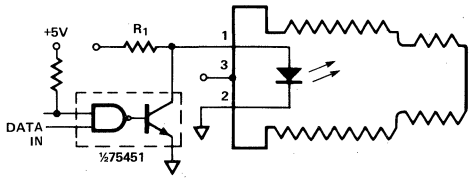
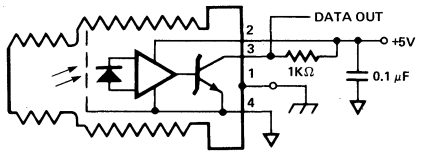


Figure 9. System Propagation Delay Test Circuit and Waveform Timing Definitions

Typical Circuit Configuration



HFBR-1201 TRANSMITTER



HFBR-2201 RECEIVER

Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol or Freon™ on a cotton swab also works well.

It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from pin 2 to pin 4 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.

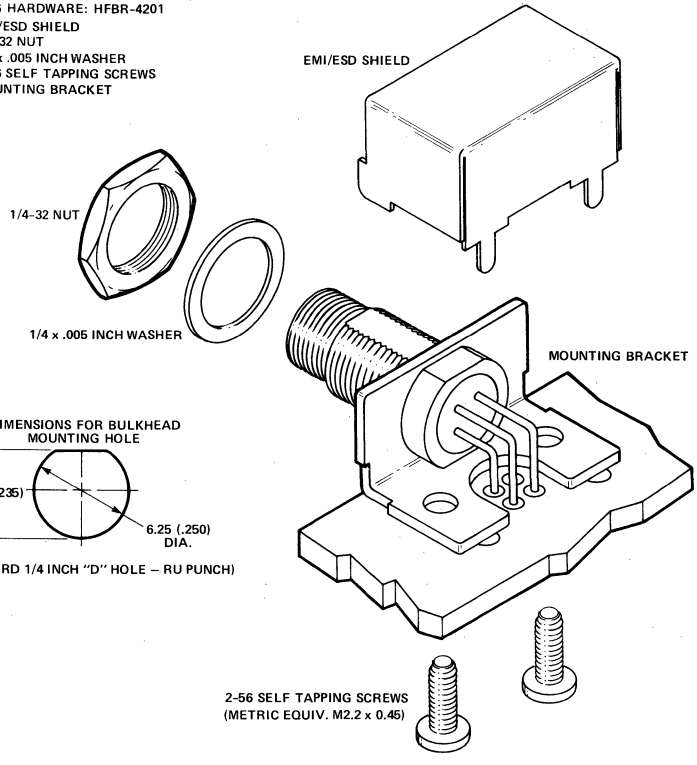
Horizontal PCB Mounting

Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

When bending the leads, avoid sharp bends right where the lead enters the backfill. Use needle nose pliers to support the leads at the base of the package and bend the leads as desired.

When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean.

MOUNTING HARDWARE: HFBR-4201
- 1 EMI/ESD SHIELD
- 1 1/4-32 NUT
- 1 1/4 x .005 INCH WASHER
- 2 2-56 SELF TAPPING SCREWS
- 1 MOUNTING BRACKET



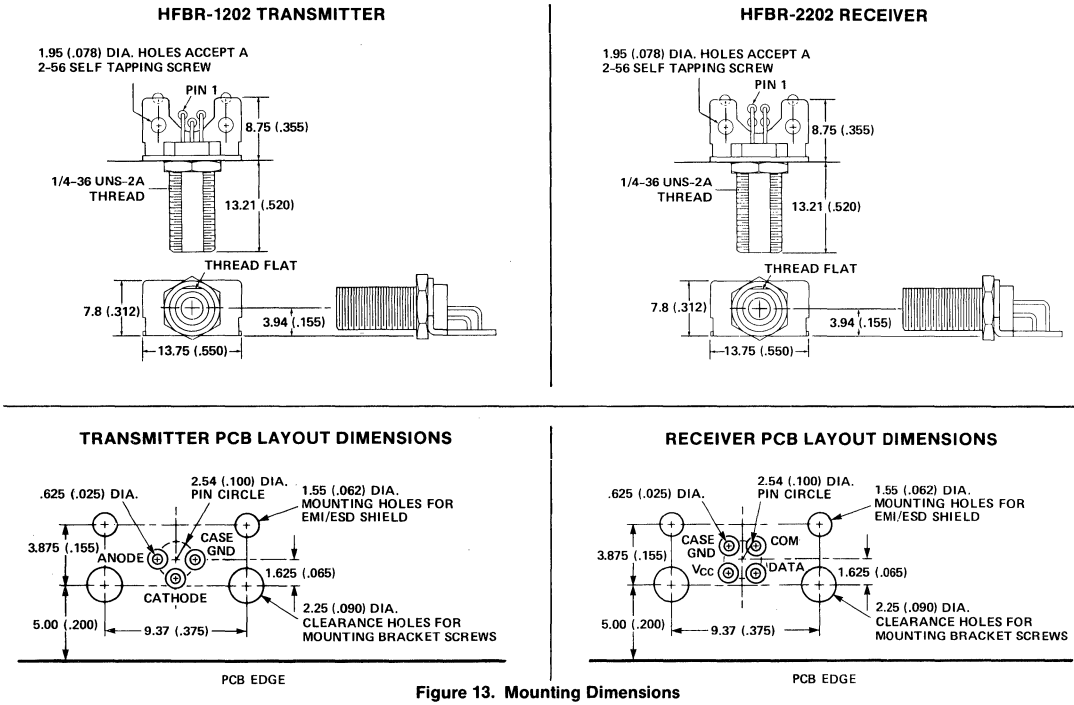


Figure 13. Mounting Dimensions

DIMENSIONS IN MILLIMETRES (INCHES).

Ordering Guide

Transmitter: HFBR-1202 (SMA Connector Compatible)

Receiver: HFBR-2202 (SMA Connector Compatible)

Mounting Hardware: HFBR-4202 (SMA Connector Compatible)

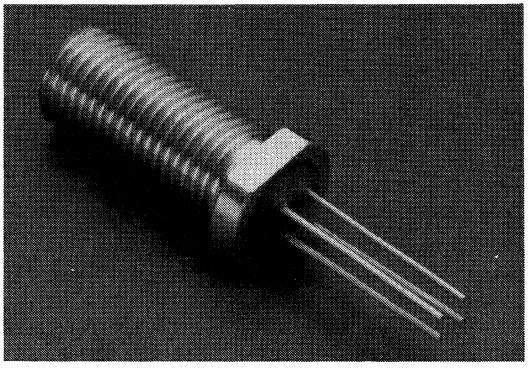
HEWLETT PACKARD

HIGH EFFICIENCY FIBER OPTIC TRANSMITTER

HFBR-1204

Features

- **OPTICAL POWER COUPLED INTO 100/140 μm FIBER CABLE**
  —9.8 dBm Guaranteed at 25° C
  —7.4 dBm Typical
- **FACTORY ALIGNED OPTICS**
- **RUGGED MINIATURE PACKAGE**
- **COMPATIBLE WITH SMA CONNECTORS**



Description

The HFBR-1204 Fiber Optic Transmitter contains an etched-well 820 nm GaAlAs emitter capable of coupling greater than −10 dBm of optical power into HP's 100/140 μm SMA connectored cable assemblies. This high power level is useful for fiber lengths greater than 1 km, or systems where star couplers, taps, or in-line connectors create large fixed losses.

Consistent coupling efficiency is assured by factory alignment of the LED with the mechanical axis of the package connector port. Power coupled into the fiber varies less than 5 dB from part to part at a given drive current and temperature. The benefit of this is reduced dynamic range requirements on the receiver.

High coupling efficiency allows the emitters to be driven at low current levels resulting in low power consumption and increased reliability of the transmitter. Another advantage of the high coupling efficiency is that a significant amount of power can still be launched into smaller fiber such as 50/125 μm (−19.1 dBm typ.).

The HFBR-1204 transmitter is housed in a rugged miniature package. The lens is suspended to avoid mechanical contact with the active devices. This assures improved reliability by eliminating mechanical stress on the die due to the lens. For increased ESD protection and design flexibility, both the anode and cathode are insulated from the case.

HFBR-1204 is compatible with SMA style connectors. The low profile package is designed for direct mounting on printed circuit boards or through panels without additional heat sinking. A complete mounting hardware package (HFBR-4202) is available for horizontal mounting on PCBs, including a snap-on metal shield for harsh EMI/ESD environments.

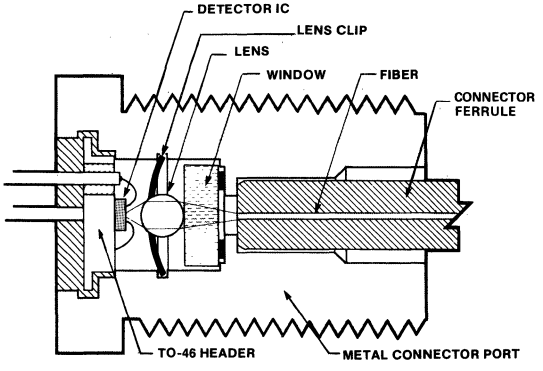
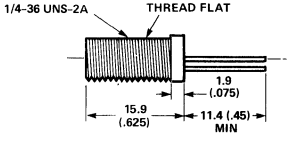
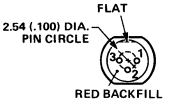


Figure 1. Cross Sectional View

Mechanical Dimensions

HFBR-1204





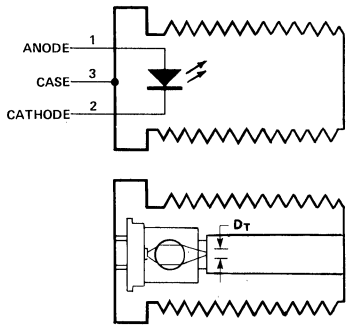
PIN	FUNCTION
1	ANODE
2	CATHODE
3	CASE

DIMENSIONS IN MILLIMETRES (INCHES)

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Reference
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	-40	+85	°C	Note 4
Lead Soldering Cycle	Temp.			+260	°C	Note 1
	Time			10	sec	
Forward Input Current	Peak	$I_{F,PK}$		100	mA	
	Average	$I_{F,AV}$		100	mA	
Reverse Input Voltage		V_R		1.0	V	
Voltage, Case-to-Junction		V_C		25	V	

HFBR-1204 TRANSMITTER



Electrical/Optical Characteristics -40° C to +85° C unless otherwise specified

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Reference
Forward Voltage	V_F	1.44	1.72	1.94	V	I_F = 100 mA	Figure 2
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-0.54		mV/° C	I_F = 100 mA	Figure 2
Reverse Breakdown Voltage	V_{BR}	1.0	3.1		V	I_R = 100 μA	
Numerical Aperture	NA		0.38				
Optical Port Diameter	D_T		250		μm		Note 3
Peak Emission Wavelength	λ_P		820		nm		Figure 5
Peak Output Optical Power Coupled into HP's 100/140 μm SMA Connectored Cable	P_T	-9.8	-7.4	-5.0	dBm	I_F = 100 mA	Figure 3, 4
		105	182	316	μW	T_A = 25° C	Notes 4, 5, 6, 8
		-11.2		-4.2	dBm	I_F = 100 mA	
		76		380	μW	-40° C < T_A < 85° C	
Output Optical Power Coupled into 50/125 μm Fiber	P_T		-19.1		dBm	I_F = 100 mA	Figure 3, 4
			12		μW	T_A = 25° C	Notes 5, 7
Output Optical Power Coupled into Siecor 100/140 μm Fiber Cable or Equivalent	P_T		-9.4		dBm	I_F = 100 mA T_A = 25° C	Figure 3, 4 Notes 5, 11
Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-.014		dB/° C	I_F = 100 mA	Figure 3
Case Isolation Resistance (Case to Pins 1 or 2)	R_{CASE}	1			MΩ	V_{CASE} = 25 V	
Thermal Resistance	Θ_{JC}		90		°C/W		Note 9
Rise Time, Fall Time (10 to 90%)	t_r, t_f		11		nsec		Figure 6 Note 10

WARNING: OBSERVING THE TRANSMITTER OUTPUT POWER UNDER MAGNIFICATION MAY CAUSE INJURY TO THE EYE. When viewed with the unaided eye, the infrared output is radiologically safe; however, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

Notes:
1. 2.0 mm from where leads enter case.
2. Typical data at T_A = 25° C.
3. D_T is measured at the plane of the fiber face and defines a diameter where the optical power density is within 10 dB of the maximum.
4. HP's 100/140 μm fiber cable specified at a narrower temperature range, -20° C to 85° C.
5. Output Optical Power into connectored fiber cable other than HP's Cable/Connector Assemblies may be different than specified because of mechanical tolerances of the connector, quality of the fiber surface and other variables.
6. Measured at the end of 1.0 metre of HP's 100/140 μm Fiber Optic Cable with large area detector and cladding modes stripped, terminated with the appropriate type of connector. This assembly approximates a Standard Test Fiber. The fiber NA is 0.28, measured at the end of greater than 300 metres length of fiber, the NA being defined as the sine of the half angle determined by the 5% intensity points.

7. Measured at the end of 1.0 metre 50/125 μm fiber with large area detector and cladding modes stripped, approximating a Standard Test Fiber. The fiber NA is 0.21, measured at the end of a 2.0 metre length, the NA being defined as the sine of the half angle determined by the 5% of peak intensity points.
8. When changing microwatts to dBm, the optical power is referenced to 1 milliwatt (1000 μW).
   Optical Power, P (dBm) = 10 log P (μW)/1000 μW
9. Thermal resistance is measured with the transmitter coupled to a connector assembly and mounted on a printed circuit board with the HFBR-4202 mounting hardware.
10. Measured with a 1 mA pre-bias current and terminated into a 50 ohm load.
11. Measured at the end of 1.0 metre Siecor 100/140 μm fiber cable or equivalent, with large area detector and cladding modes stripped, terminated with the appropriate type of connector. This assembly approximates a Standard Test Fiber. The fiber NA is 0.275, measured at the end of a 2.0 metre length, the NA being defined as the sine of the half angle determined by the 5% of peak intensity points.

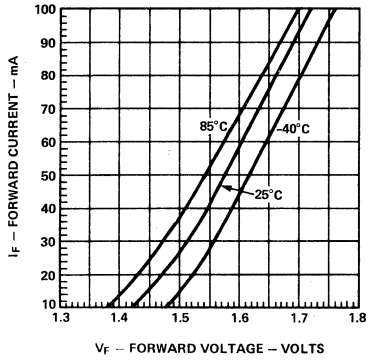


Figure 2. Forward Voltage and Current Characteristics

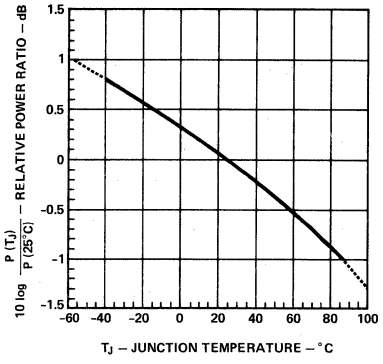


Figure 3. Normalized Thermal Effects in Transmitter Output

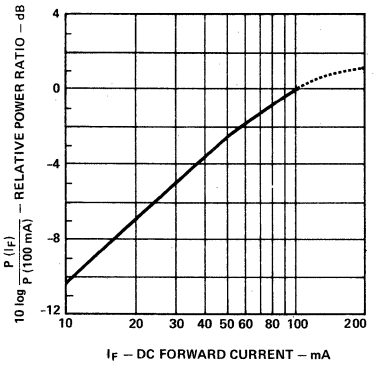


Figure 4. Normalized Transmitter Output vs. DC Forward Current

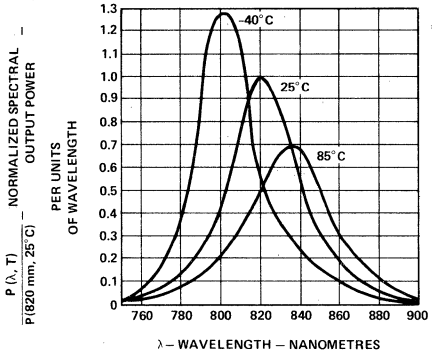


Figure 5. Transmitter Spectrum Normalized to the Peak at 25° C

Ordering Guide

Transmitter: HFBR-1204 (SMA Connector Compatible)

Receiver: HFBR-2202 (5 MBaud, SMA Connector)
HFBR-2204 (40 Mbaud, SMA Connector Compatible)

Mounting Hardware: HFBR-4202 (SMA Connector Compatible)

Fiber Optic Cable — see data sheets

High Speed Operation

Rise and fall times can be improved by using a pre-bias current and "speed-up" capacitor. A 1 mA pre-bias current will significantly reduce the junction capacitance and will couple less than -34 dBm of optical power into the fiber cable. The TTL compatible circuit in Figure 7 using a speed-up capacitor will provide typical rise and fall times of 10 ns.

$$I_{PEAK} = 100\ mA = \frac{V_{CC} - V_F}{34.9\Omega}$$

$$I_{AVG} = 78\ mA = \frac{V_{CC} - V_F}{34.9 + 10\Omega}$$

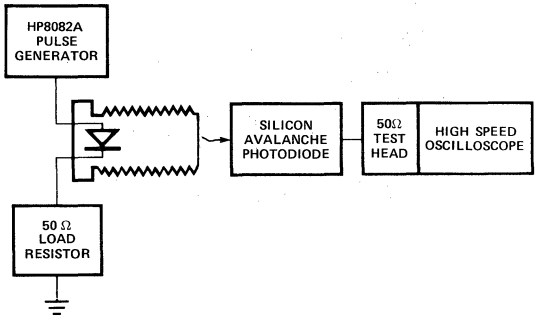


Figure 6. Test Circuit for Measuring t_r, t_f

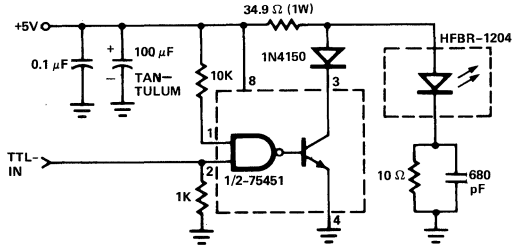


Figure 7. High Speed TTL Circuit

Link Design

With transmitter performance specified as power in dBm into a fiber of particular properties (core size, NA, and index profile), and receiver performance given in terms of the power in dBm radiated from the same kind of fiber, then the link design equation is simply:

(1) $P_T - \ell \cdot \alpha_O = P_R$

where

P_T = transmitter power into fiber (dBm)
ℓ = fiber (cable) length (km)
α_O = fiber attenuation (dB/km)
P_R = receiver power, from fiber, (dBm)

For transmitter input current in the range from 10 to 100 mA, the power varies approximately linearly:

(2) $P_T = P_O + 10 \log (I/I_O)$

where

P_O = transmitter power specification (dBm) at I_O
I_O = specified transmitter current (100 mA)
I = selected transmitter current (mA)

To allow for the dynamic range limits of proper receiver performance, it is necessary that a link with maximum transmitter power and minimum attenuation does not OVERDRIVE the receiver and that minimum transmitter power with maximum attenuation does not UNDERDRIVE it. These limits can be expressed in a combination of the two equations above:

(3) $P_{O\ MAX} + 10 \log (I_{MAX}/I_O) - \ell * \alpha_{OMIN} < P_{R\ MAX}$

(4) $P_{O\ MIN} + 10 \log (I_{MIN}/I_O) - \ell * \alpha_{OMAX} > P_{R\ MIN}$

where

$P_{O\ MAX}$, $P_{O\ MIN}$ = max., min. specified power from transmitter (dBm) at $I = I_O$
I_{MAX}, I_{MIN} = max., min. selected transmitter operating current (mA)
$P_{R\ MAX}$, $P_{R\ MIN}$ = max., min. specified power at receiver (dBm)
α_{OMAX}, α_{OMIN} = max., min. attenuation (dB/km)

A more useful form of these equations comes from solving them for the current ratio, expressed in dB:

(5) $10 \log (I_{MAX}/I_O) < P_{R\ MAX} - P_{O\ MAX} + \ell \cdot \alpha_{OMIN}$

(6) $10 \log (I_{MIN}/I_O) > P_{R\ MIN} - P_{O\ MIN} + \ell \cdot \alpha_{OMAX}$

These are plotted in Figure 8 as the OVERDRIVE LINE, and UNDERDRIVE LINE, respectively for the following components:

HFBR-1204 Transmitter $-11.2 < P_T < -4$ dBm
HFBR-2204 Receiver (25 MHz) $-28.5 < P_R < 12.6$ dBm
HFBR-2204 Receiver (2.5 MHz) $-35.5 < P_R < -12.6$ dBm
HP's 100/140 μm Fiber Cable $4 < \alpha_O < 8$ dB/km

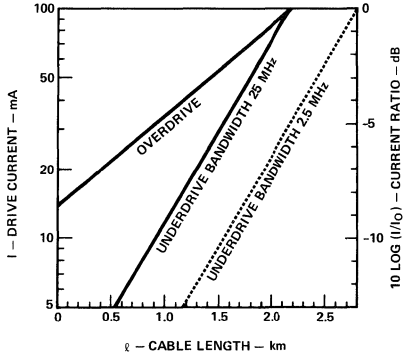


Figure 8. Link Design Limits.

These design equations take account only of the power loss due to attenuation. The specifications for the receiver and transmitter include loss effects in end connectors. If the system has other fixed losses, such as from directional couplers or additional in-line connectors, the effect is to shift both OVERDRIVE and UNDERDRIVE lines upward by the amount of the additional loss ratio.

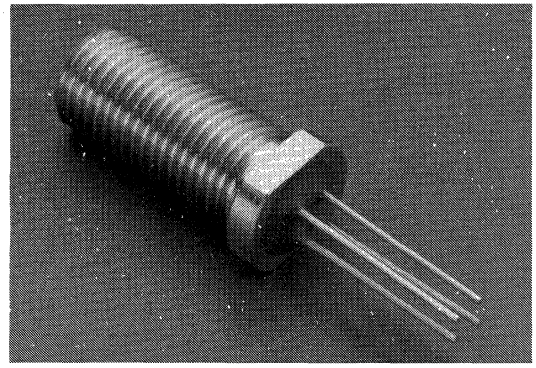
HEWLETT PACKARD

40 MBd MINIATURE FIBER OPTIC RECEIVER

HFBR-2204

Features

- DATA RATES UP TO 40 MBd
- HIGH OPTICAL COUPLING EFFICIENCY
- RUGGED, MINIATURE METAL PACKAGE
- COMPATIBLE WITH SMA STYLE CONNECTORS
- VERSATILE ANALOG RECEIVER OUTPUT
- 25 MHz ANALOG BANDWIDTH



Applications

- DATA ACQUISITION AND PROCESS CONTROL
- SECURE DATA COMMUNICATION
- EMC REGULATED SYSTEMS (FCC/VDE)
- EXPLOSION PROOF SYSTEMS
- WEIGHT SENSITIVE SYSTEMS (e.g., AVIONICS, MOBILE STATIONS)
- VIDEO TRANSMISSION

Description

The HFBR-2204 Receiver is capable of data rates up to 40 MBd at distances greater than 1 km when used with cable and HFBR-1202/4 Transmitters. The HFBR-2204 Receivers contains a discrete PIN photodiode and preamplifier IC.

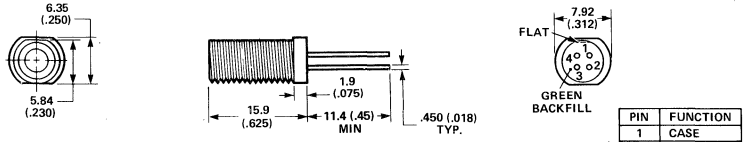
The signal from this simple analog receiver can be optimized for a variety of transmission requirements. For example, the circuits in Application Bulletin 73 add low-cost external components to achieve logic compatible signal levels optimized for various data formats and data rates.

Each of these fiber optic components uses the same rugged, lensed, miniature package. This package assures a consistent, efficient optical coupling between the active devices and the optical fiber.

The HFBR-2204 Receiver is compatible with SMA style connectors, types A and B (see Figure 11 and HP's 100/140 μm SMA connectored cable assemblies. HP's 100/140 μm fiber ootic cable can be ordered with or without connectors.

Mechanical Dimensions

HFBR-2204 RECEIVER



PIN	FUNCTION
1	CASE
2	SIGNAL
3	COMMON
4	V_{CC}

DIMENSIONS IN MILLIMETRES (INCHES)
UNLESS OTHERWISE SPECIFIED, THE TOLERANCES ARE:
.X ± .51 mm (.XX ± .02 IN)
.XX ± .13 mm (.XXX ±.005 IN)

Electrical Description

The HFBR-2204 Fiber Optic Receiver contains a PIN photodiode and low noise transimpedance pre-amplifier hybrid circuit with an inverting output (see note 10). The HFBR-2204 receives an optical signal and converts it ot an analog voltage. The output is a buffered emitter-follower. Because the signal amplitude from the HFBR-2204 Receiver is much larger than from a simple PIN photodiode, it is less susceptible to EMI, especially at high signal rates.

The frequency response is typically dc to 25 MHz. Although the HFBR-2204 is an analog receiver, it is easily made compatible with digital systems (see Application Bulletin 73). Separate case and signal ground leads are provided for maximum design flexibility.

It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from Pin 4 (V_{CC}) to Pin 3 (circuit common) of the receiver. Total lead length between both ends of the capacitor and the pins should be less than 20 mm.

Mechanical Description

The HFBR-2204 Fiber Optic Receiver is housed in a miniature package intended for use with HP's 100/140 μm SMA connectored cable assemblies. This package has important performance advantages:

1. Precision mechanical design and assembly procedures assure the user of consistent high efficiency optical coupling.
2. The lens is suspended to avoid contact with the active devices, thereby assuring improved reliability.
3. The versatile miniature package is easy to mount. This low profile package is designed for direct mounting on printed circuit boards or through panels without additional heat sinking.

   A complete mounting hardware package is available for horizontal PCB applications, including a snap-on metal shield for harsh EMI/ESD environments.

   Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; Methanol or Freon on a cotton swab also works well.

   Note:
   When installing connectored cable on the optical port, do not use excessive force to tighten the nut. Finger tightening is sufficient to ensure connectoring integrity, while use of a wrench may cause damage to the connector or the optics.

System Design Considerations

For additional information, see Application Bulletin 73.

OPTICAL POWER BUDGETING

The HFBR-2204 Fiber Optic Receivers when used with the HFBR-1202 Fiber Optic Transmitter can be operated at a signalling rate of more than 40 MBd over a distance greater than 1000 metres (assuming 8 dB/km cable attenuation). For shorter transmission distances, power consumption can be reduced by decreasing Transmitter drive current. At a lower data rate, the transmission distance may be increased by applying bandwidth-filtering at the output of the HFBR

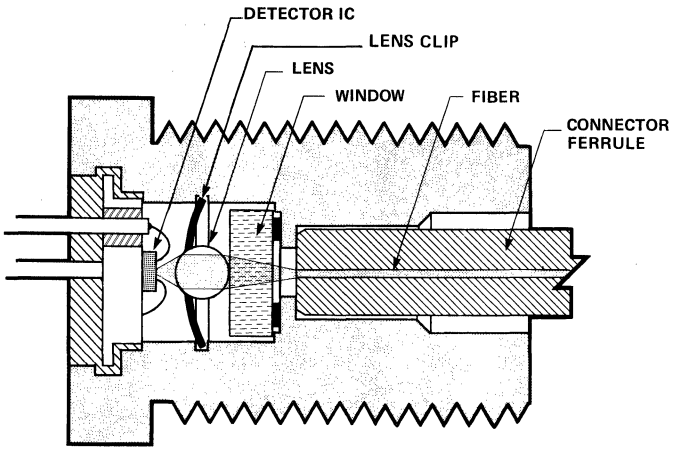


Figure 1. Cross Sectional View

2204 Receiver; since noise is reduced as the square root of the bandwidth, the sensitivity of the circuit is proportionately improved provided these two conditions are met:

a. input-referred noise of the follow on circuit is well below the filtered noise of the Receiver
b. logic comparator threshold is reduced in the same proportion as the noise reduction

As an example, consider a link with a maximum data rate of 10 MBd (e.g., 5 Mb/s Manchester); this requires a 3 dB bandwidth of only 5 MHz. For this example, the input-referred rms noise voltage of the follow-on circuit is 0.03 mV. The equivalent optical noise power of the complete receiver (P_{NO}) is given by:

$$P_{NO} = [(V_{NO})^2 (B/Bo) + (V_{NI})^2]^{0.5} / R_P$$

V_{NO} = rms output noise voltage of the HFBR-2203/04 with no bandwidth filtering
V_{NI} = input-referred rms noise voltage of the follow-on circuit
B = filtered 3 dB bandwidth
Bo = Unfiltered 3dB bandwidth of the HFBR-2203/04 (25 MHz)
R_P = optical-to-electrical responsivity (mV/μW) of the HFBR-2240

Note that noise adds in an rms fashion, and that the square of the rms noise voltage of the HFBR-2204 is reduced by the bandwidth ratio, B/Bo.

From the receiver data (Electrical/Optical Characteristics) taking worst-case values, and applying NO bandwidth filtering (B/Bo = 1):

$$P_{NO} = \frac{[(0.43)^2+(0.03)^2]^{0.5} \text{ mV}}{4.6 \text{ mV}/\mu\text{W}} = 0.094\,\mu\text{W or } -40.3 \text{ dBm}$$

To ensure a bit error rate less than 10^{-9} requires the signal power to be 12 times larger (+11 dB) than the rms noise as referred to the Receiver input. The minimum Receiver input power is then:

$$P_{RMIN} = P_{NO} + 11 \text{ dB} = -29.3 \text{ dBm}$$

With the application of a 5 MHz low-pass filter, the bandwidth ratio becomes:

$$B/Bo = 5 \text{ MHz}/25 \text{ MHz} = 0.2$$

Note that 25 MHz should be used for the total noise bandwidth of the HFBR-2204. Inserting this value of the bandwidth ratio in the expressions for P_{NO} and P_{RMIN} above yields the results:

$$P_{NO} = 0.042\,\mu\text{W or } -43.8 \text{ dBm and } P_{RMIN} = -32.8 \text{ dBm}$$

Given the HFBR-1202 Transmitter optical power P_T = −18 dBm at I_F = 40 mA, and allowing a 3 dB margin, a minimum optical power budget of 11.8 dB is obtained:

$$[-18 \text{ dBm} - 3 \text{ dB} - (-32.8 \text{ dBm})] = 11.8 \text{ dB}$$

Using 8 dB/km optical fiber, this translates into a minimum link length of 1475 metres (typical link power budget for this configuration is approximately 17.2 dB or 3130 metres with 5.5 dB/km fiber).

BANDWIDTH

The bandwidth of the HFBR—2204 is typically 25 MHz. Over the entire temperature range of -40° C to +85° C, the rise and fall times vary in an approximately linear fashion with temperature. Under worst case conditions, t_r and t_f may reach a maximum of 26 ns, which translates to a 3 dB bandwidth of:

$$f_{3dB} \simeq \frac{350}{t_r} = \frac{350}{26 \text{ ns}} = 13.5 \text{ MHz}$$

The receiver response is essentially that of a single-pole system, rolling off at 6 dB/octave. In order for the receiver to operate up to 40 MBd even though its worst case 3 dB bandwidth is 13.5 MHz, the received optical power must be increased by 3 dB to compensate for the restricted receiver transmission bandwidth.

PRINTED CIRCUIT BOARD LAYOUT

When operating at data rates above 10 MBd, standard PC board precautions should be taken. Lead lengths greater than 20 mm should be avoided whenever possible and a ground plane should be used. Although transmission line techniques are not required, wire wrap and plug boards are not recommended.

OPERATION WITH HEWLETT-PACKARD TRANSMITTERS

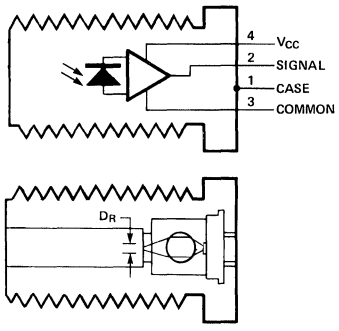
Hewlett-Packard offers two transmitters compatible with the HFBR-2204 Link performance with each transmitter is shown below for 25°C operation with HP's 100/140 μm glass fiber cable. See product data sheets for further information.

	HFBR-1202 -17 dBm Coupled Optical Power	**HFBR-1204 -9.8 dBm Coupled Optical Power**
HFBR-2204 -27 dBm Sensitivity	1200 m 40 MBd	2100 m 40 MBd
HFBR-2204 -32 dBm Sensitivity	1800 M 10 MBd	2800 M 10 MBd

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Reference
Storage Temperature		T_S	-55	85	°C	
Operating Temperature		T_A	-40	85	°C	Note 9
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec	
Case Voltage		V_{CASE}		25	V	
Signal Pin Voltage		V_{SIGNAL}	-0.5	1	V	
Supply Voltage		V_{CC}	-0.5	7.0	V	

HFBR-2204 RECEIVER



Electrical/Optical Characteristics

-40° C to +85° C; $4.75 \le V_{CC} \le 5.25$; $R_{LOAD} = 511\Omega$ unless otherwise specified

Parameter	Symbol	Min.	Typ.[4]	Max.	Unit	Conditions	Reference
Responsivitity	R_P	5.1	7	10.9	mV/μW	T_A = 25° C at 820 nm	Note 10 Figure 3
		4.6		12.3	mV/μW	-40 ≤ T_A ≤ +85° C	
RMS Output Noise Voltage	V_{NO}		.30	.36	mV	T_A = 25° C, P_{IN} = 0μW	Figures 4, 7
				.43	mV	-40 ≤ T_A ≤85° C, P_{IN}= 0 μW	
Peak Input Power	P_R			-12.6	dBm	T_A = 25° C	Note 2
				55	μW		
				-14	dBm	-40 ≤ T_A ≤ 85° C	
				40	μW		
Output Impedance	Z_O		20		Ω	Test Frequency = 20 MHz	
DC Output Voltage	V_{odc}		.7		V	P_{IN} = 0 μW	
Power Supply Current	I_{CC}		3.4	6.0	mA	R_{LOAD} = ∞	
Equivalent N.A.	NA		.35				
Equivalent Diameter	D_R		250		μm		Note 3
Equivalent Optical Noise Input Power	P_N		-43.7	-40.3	dBm		
			.042	.094	μW		

Dynamic Characteristics

-40° C to +85° C; $4.75 \le V_{CC} \le 5.25$; $R_{LOAD} = 511\Omega$, C_{LOAD} = 13 pF unless otherwise specified

Parameter	Symbol	Min.	Typ.[7]	Max.	Units	Conditions	Reference
Rise/Fall Time, 10% to 90%	t_r, t_f		14	19.5	ns	T_A = 25° C P_{IN} = 10 μW Peak	Note 5
				26	ns	-40 ≤ T_A ≤ 85° C	Figures 8, 9
Pulse Width Distortion	$t_{phl} - t_{plh}$			2	ns	P_{IN} = 40 μW Peak	Figure 9
Overshoot			4		%	T_A = 25° C	Note 6 Figures 8, 9
Bandwidth			25		MHz		
Power Supply Rejection Ratio (Referred to Output)	PSRR		50		dB	at 2 MHz	Note 7 Figures 5, 6

Notes:

1. 2.0 mm from where leads enter case.
2. If Pin < 40 μW, then pulse width distortion may increase. At Pin = 80 μW and T_A = 80° C, some units have exhibited as much as 100 ns pulse width distortion.

Notes (cont.):

3. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
4. Typical specifications are for operation at $T_A = 25°C$ and $V_{CC} = 5.0V$.
5. Input optical signal is assumed to have 10% — 90% rise and fall times of less than 6 ns.
6. Percent overshoot is defined as:

$$\frac{V_{PK} - V_{100\%}}{V_{100\%}} \times 100\%$$ See Figure 16.

7. Output referred P.S.R.R. is defined as

$$20 \log \left(\frac{V_{\text{POWER SUPPLY RIPPLE}}}{V_{\text{OUT RIPPLE}}} \right)$$

8. It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from pin 4 (V_{CC}) to pin 3 (circuit common) of the receiver. Total lead length between both ends of the capacitor and the pins should be less than 20 mm.
9. HP's 100/140 μm fiber cable is specified at a narrower temperature range, -20°C to 85°C.
10. $V_{OUT} = V_{ODC} - (R_P \times P_{IN})$.

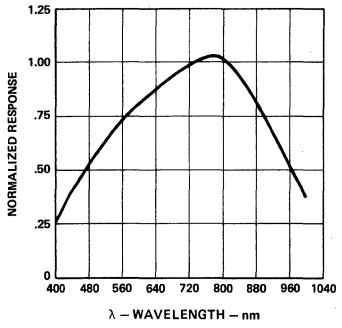


Figure 3. Receiver Spectral Response Normalized to 820 nm

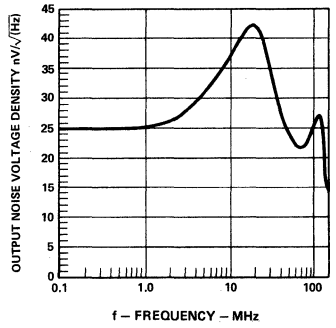


Figure 4. Receiver Noise Spectral Density

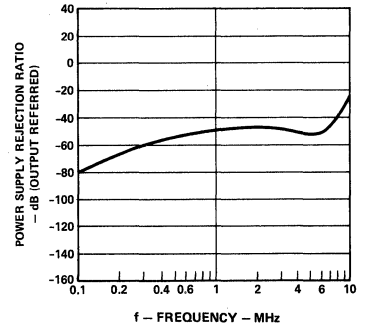


Figure 5. Receiver Power Supply Rej. vs. Freq.

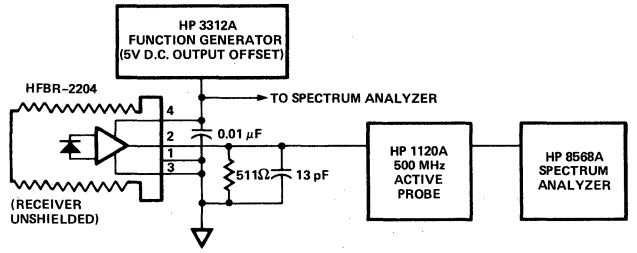


Figure 6. Power Supply Rejection Test Circuit

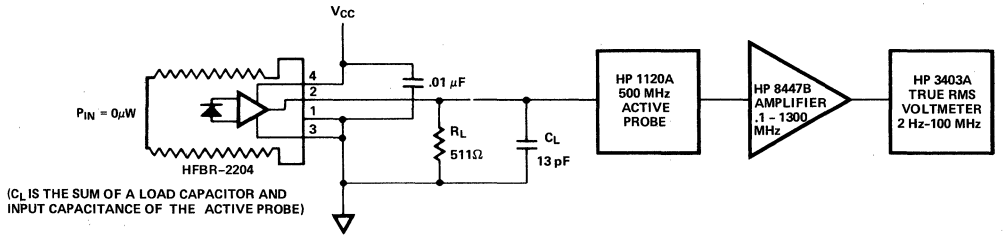


Figure 7. RMS Output Noise Voltage Test Circuit

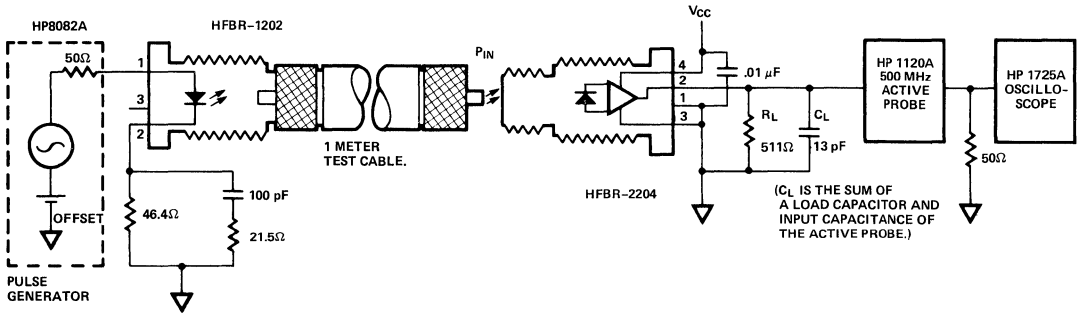


Figure 8. Rise and Fall Time Test Circuit

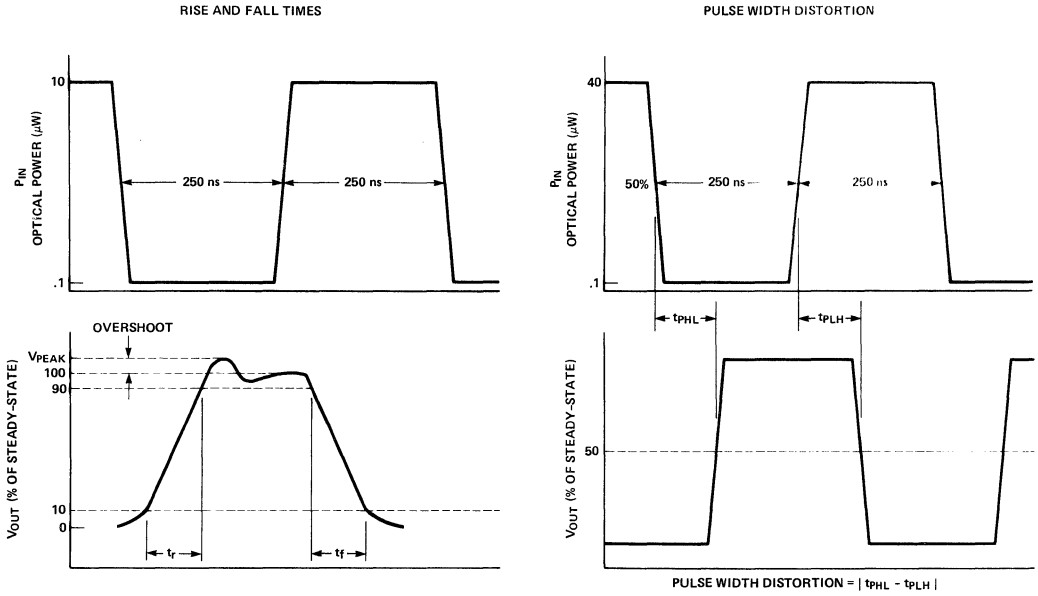
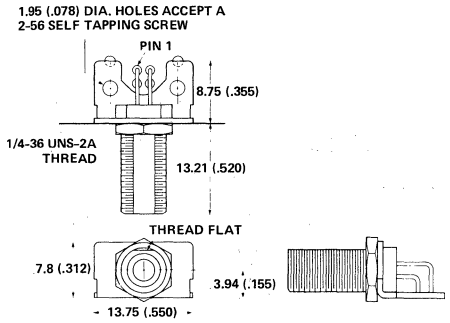


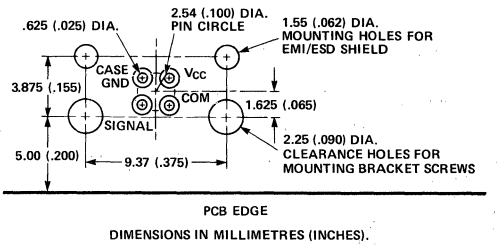
Figure 9. Waveform Timing Definitions

FIBER OPTICS

HFBR-2204 RECEIVER



RECEIVER PCB LAYOUT DIMENSIONS

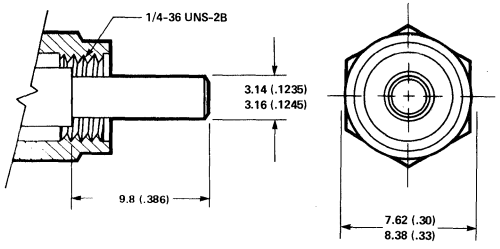


DIMENSIONS IN MILLIMETRES (INCHES).

Figure 10. Mounting Dimensions

SMA STYLE CONNECTORS

TYPE A
(Used in HP's SMA Connectored Cable Assemblies).



TYPE B
(Not Available from Hewlett-Packard)

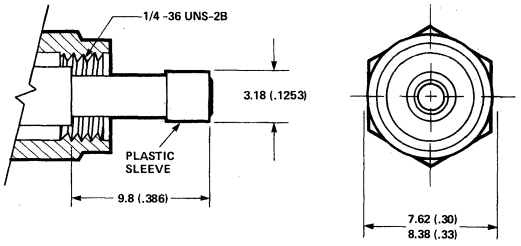


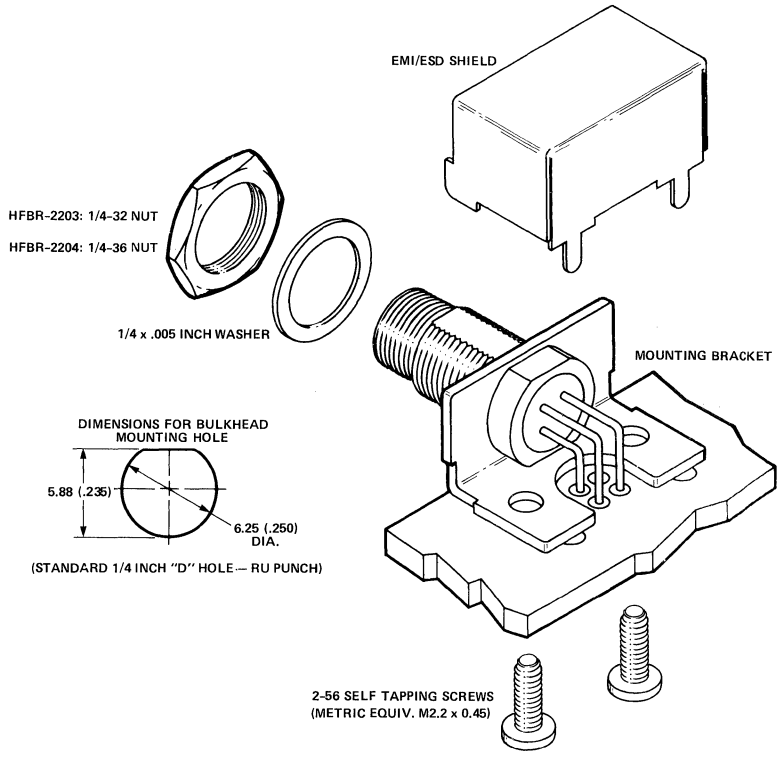
Figure 11. Fiber Optic Connector Styles

Horizontal PCB Mounting

Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

When bending the leads, avoid sharp bends right where the lead enters the backfill. Use needle nose pliers to support the leads at the base of the package and bend the leads as desired.

When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean.



MOUNTING HARDWARE: HFBR-4202 (HFBR-2204)

1 EMI/ESD SHIELD
1 1/4-36 NUT
1 1/4 x .005 INCH WASHER
2 2-56 SELF TAPPING SCREWS
1 MOUNTING BRACKET

Ordering Guide

Transmitter: HFBR-1202 (SMA Connector Compatible)
HFBR-1204 (SMA Connector Compatible)

Receiver: HFBR-2204 (SMA Connector Compatible)

Mounting Hardware: HFBR-4202 (SMA Connector Compatible)

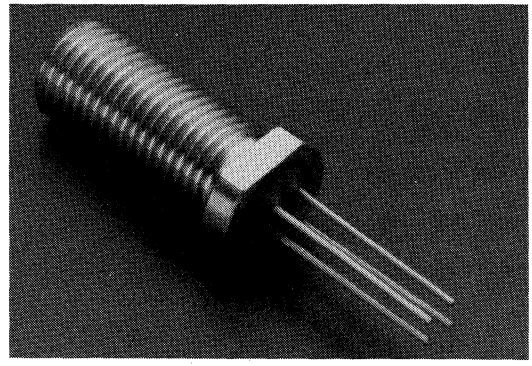
HEWLETT PACKARD

PIN PHOTODIODE FIBER OPTIC RECEIVER

HFBR-2208

Features

- **GUARANTEED PERFORMANCE:**
  60 MHz Bandwidth at 5 V Reverse Bias
  Low Capacitance: Less than 1.6 pF
  0.29 A/W Minimum Responsivity
  Low Dark Current: Less than 500 pA
- **MATES DIRECTLY WITH SMA STYLE CONNECTORS**
- **RUGGED, ISOLATED MINIATURE METAL PACKAGE WITH FACTORY ALIGNED OPTICS**



Applications

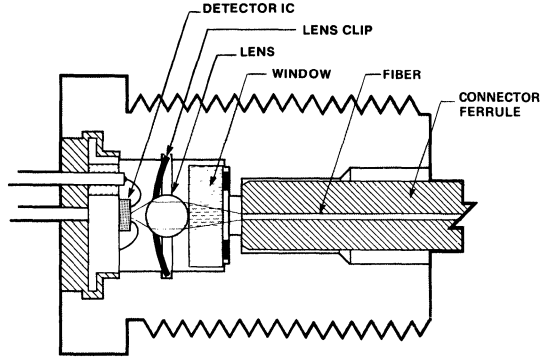
- **HIGH SPEED FIBER OPTIC LINKS**
- **WIDE BANDWIDTH ANALOG FIBER OPTIC LINKS**
- **HIGH SENSITIVITY, LOW BANDWIDTH LINKS**
- **OPTICAL POWER SENSOR**

Description

The HFBR-2208 Fiber Optic Receiver is a silicon PIN photodiode mounted in a rugged metal package. Well suited for high speed applications, the HFBR-2208 Fiber Optic Receiver has low capacitance and low noise. The high coupling efficiency of the miniature package provides a minimum of 0.29 A/W responsivity. Receiver responsivity includes the optical power lost in coupling light from the fiber onto the PIN photodiode as well as the responsivity of the PIN photodiode itself.

HFBR-2208 mates with SMA style connectors.

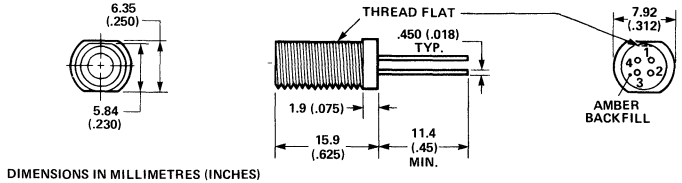
The HFBR-2208 is a member of the family of transmitters and receivers which use the miniature package. HP also offers connectored and unconnectored 100/140 μm fiber cable in simplex and duplex configurations.



Cross Sectional View

Mechanical Dimensions

HFBR-2208 SMA STYLE COMPATIBLE



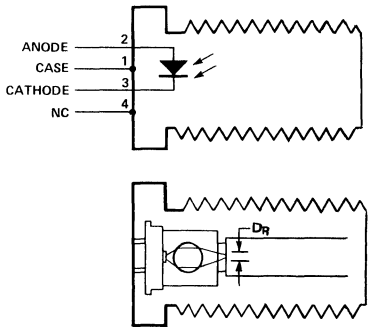
PIN	FUNCTION
1	CASE
2	ANODE
3	CATHODE
4	NC

DIMENSIONS IN MILLIMETRES (INCHES)

HFBR-2208 PIN PHOTODIODE

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	−55	85	°C	
Operating Temperature		T_A	−55	85	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec	
Reverse Bias Voltage		V_R	−0.5	50	V	
Voltage, Case-to-Junction		V_C		100	V	Note 2



Electrical/Optical Characteristics

−55° C to +85° C; V_R = 5 V; P_R = −20 dBm at 820 nm unless otherwise specified. Typical data at T_A = 25° C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Reference
Effective Optical Port DC Responsivity	R_P	0.29	0.38	0.40	A/W	HP's 100/140 μm Fiber N.A. = 0.3, g = 2	Fig. 1, 2, 3, 8
Dark Current	I_D		50	500	pA	T_A = 25° C, P_R = 0 μW, V_R = 20 V	Fig. 4, 9
Noise Equivalent Power	NEP			3.4×10^{-14}	$\frac{W}{\sqrt{Hz}}$		Note 5
Total Capacitance	C_T		1.3	1.6	pF		Fig. 5
Series Resistance	R_S		5	15	Ω		
Equivalent N.A.	NA		0.4				
Equivalent Diameter	D_R		250		μm		Note 3
Case Isolation Resistance	R_{CASE}	1			MΩ	V_C = 100 V	Note 2, Fig. 9

Dynamic Characteristics

T_A = 25° C, R_{LOAD} = 50 Ω, P_R = −20 dBm at 820 nm unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Reference
3 dB Bandwidth	BW	60	100		MHz	V_R = 5 V	Fig. 6, 7
		150	250			V_R = 20 V	Fig. 10
Rise/Fall Time (10–90%)	t_r,t_f		3.5		ns	V_R = 5 V	Note 4
Relative Incremental Response	$\Delta R_P/R_P$		0.5		%	$P_R \leq$ −20 dBm, V_R = 5 V	Fig. 8, Note 6

Notes:

1. 2.0 mm from where leads enter case.
2. V_C (100 V) is applied simultaneously to Pin 2 and Pin 3 with respect to Pin 1.
3. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
4. Rise/Fall time is calculated from the equation:

$$t_r, t_f = \frac{350}{3\text{ dB BW (MHz)}} \text{ ns}$$

5. For (λ, f, Δf) = (820 nm, 100 Hz, 6 Hz) where f is the frequency for a spot noise measurement and Δf is the noise bandwidth, NEP is the optical flux required for unity signal/-noise ratio normalized for bandwidth.

Thus:

$$NEP = \frac{I_N/\sqrt{\Delta f}}{R_P}$$

where $I_N/\sqrt{\Delta f}$ is the bandwidth — normalized noise current computed from the shot noise formula:
$I_N/\sqrt{\Delta f} = \sqrt{2qI_D} = 17.9 \times 10^{-15} \sqrt{I_D}$ (A/$\sqrt{Hz}$) where I_D is nA.

6. Relative incremental response is defined as:

$$\frac{\Delta R_P}{R_P} \times 100\% = \frac{R_{AC}(P_R) - R_{AC}(-25\text{ dBm})}{R_{AC}(-25\text{ dBm})} \times 100\%$$

where:
R_{AC} = Small signal AC (20 MHz, −30 dBm) response
P_R = DC optical power incident on port.

FIBER OPTICS

V_R = 5 V; P_R = −20 dBm at 820 nm; T_A = 25°C unless otherwise specified.

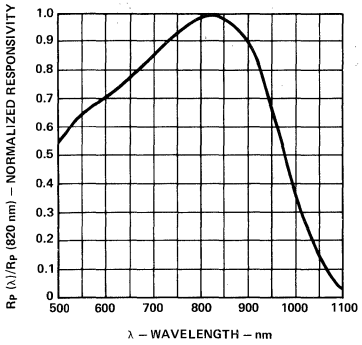


Figure 1. Normalized Responsivity vs. Wavelength

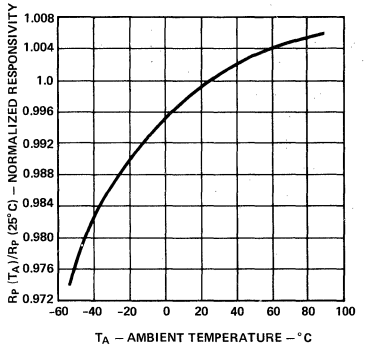


Figure 2. Normalized Responsivity vs. Ambient Temperature

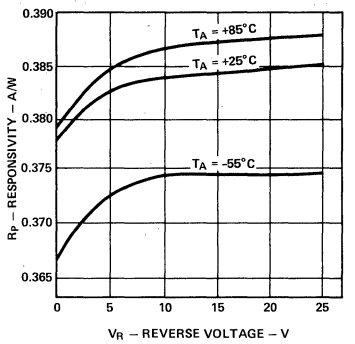


Figure 3. Responsivity vs. Reverse Voltage

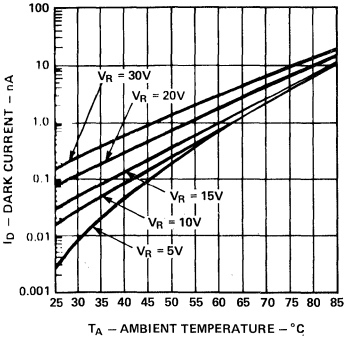


Figure 4. Dark Current vs. Ambient Temperature

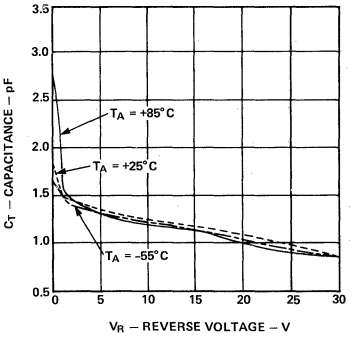


Figure 5. Capacitance vs. Reverse Voltage

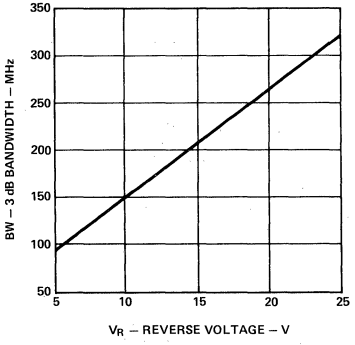


Figure 6. 3 dB Bandwidth vs. Reverse Voltage

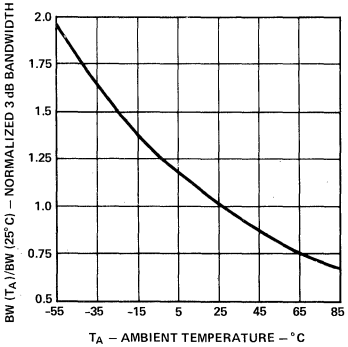


Figure 7. Normalized Bandwidth vs. Ambient Temperature

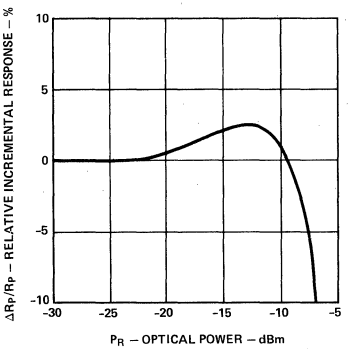


Figure 8. Linearity Characteristic vs. Optical Power

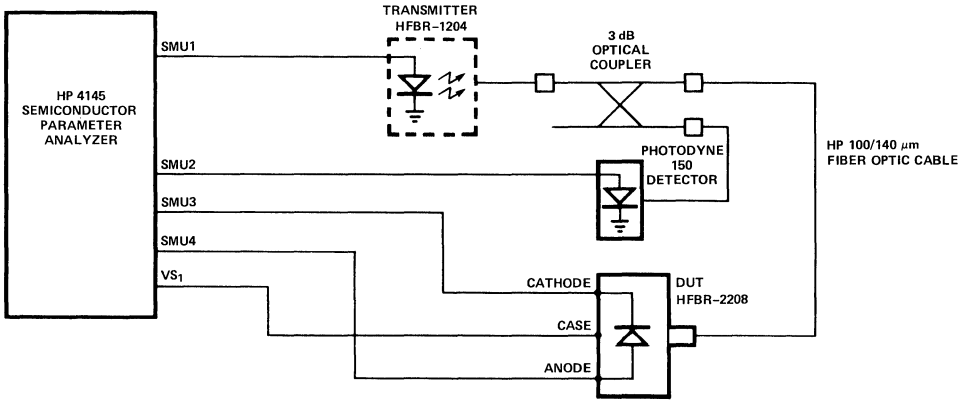


Figure 9. Test Set-up

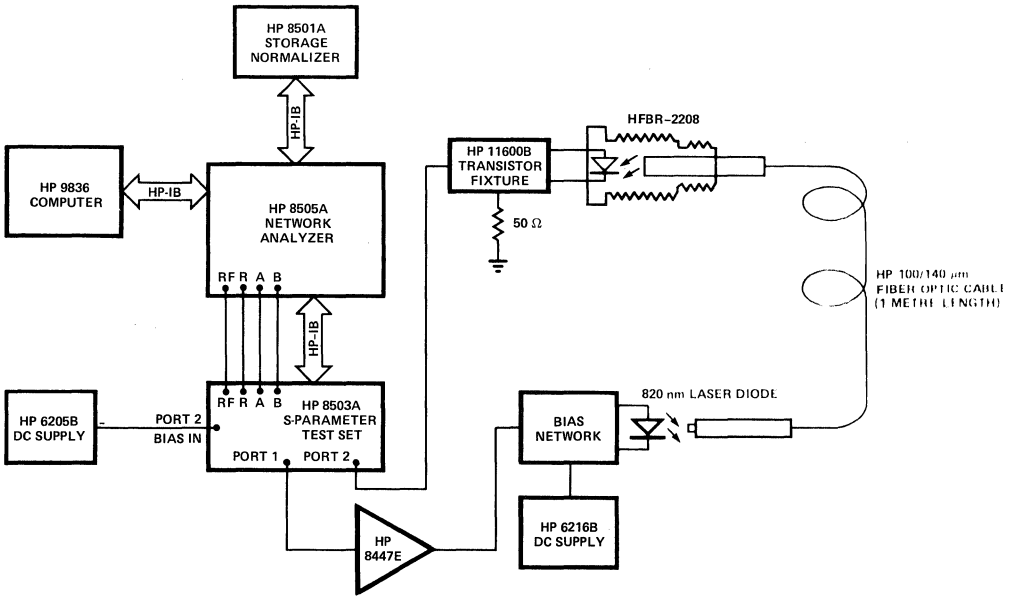
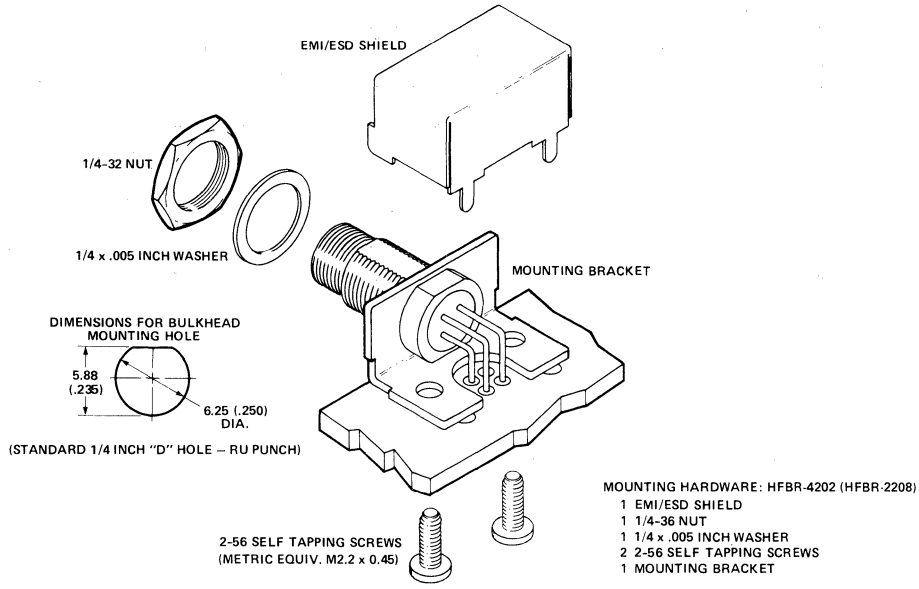


Figure 10. Bandwidth Measurement Set-up

Mechanical Description

The HFBR-2208 fiber optic receivers are housed in rugged metal packages intended for use with the SMA style connectored fiber cables. The low profile package is designed for direct mounting on printed circuit boards or through panels without additional heat sinking. A flat on the mounting threads of the device is provided to prevent rotation in all mounting configurations and to provide an orientation reference for the pin-out. Hardware is available for horizontal mounting applications on printed circuit boards. The hardware consists of a stainless steel mounting bracket fastened directly to the printed circuit board with two stainless steel self-tapping screws and a nut and washer for fastening the device in the bracket. A metal shield which snaps directly on the mounting bracket is also available for unusually severe EMI/ESD environments. When mounted in the horizontal configuration, the overall height of the component conforms with guidelines allowing printed circuit board spacing on 12.7 mm (0.500) centers. A thorough environmental characterization has been performed on these products. The test data as well as information regarding operation beyond the specified limits is available from any Hewlett-Packard sales office.

Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol or Freon™ on a cotton swab also works well.



Horizontal PCB Mounting

Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

When bending the leads, avoid sharp bends right where the lead enters the backfill. Use needle nose pliers to support the leads at the base of the package and bend the leads as desired.

When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean.

Application Information

NOISE FREE PROPERTIES

The noise current of the HFBR-2208 is negligible. This is a direct result of the exceptionally low leakage current, in accordance with the shot noise formula $I_N = (2qI_D\Delta f)^{1/2}$. Since the leakage current does not exceed 500 picoamps at a reverse bias of 20 volts, shot noise current is less than 9.8×10^{-15} amp $Hz^{-1/2}$ at this voltage.

Excess noise is also very low, appearing only at frequencies below 10 Hz, and varying approximately as 1/f. When the output of the diode is observed in a load, thermal noise of the load resistance (R_L) is $1.28 \times 10^{-10} (R_L)^{-1/2} \times (\Delta f)^{1/2}$ at 25° C, and far exceeds the diode shot noise for load resistance less than 100 megohms. Thus in high frequency operation where low values of load resistance are required for high cut-off frequency, the HFBR-2208 contributes virtually no noise to the system.

HIGH SPEED PROPERTIES

High speed operation is possible since the HFBR-2208 has low capacitance and wide bandwidth at a low reverse bias.

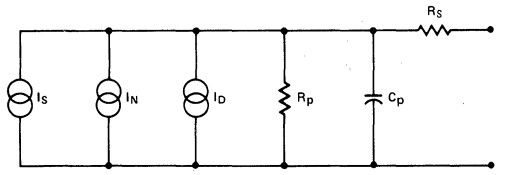


Figure 11. Photodiode Equivalent Circuit

I_S = Signal current ≈ 0.38 μA/μW x P_R
I_N = Shot noise current
< 9.8×10^{-15} amps/$Hz^{1/2}$

I_D = Dark current
< 500×10^{-12} amps at 20 V dc bias

$R_P = 10^{11}\ \Omega$
$R_S = <50\ \Omega$

LINEAR OPERATION

Operation of the photodiode is most linear when operated with a current amplifier as shown in Figure 12.

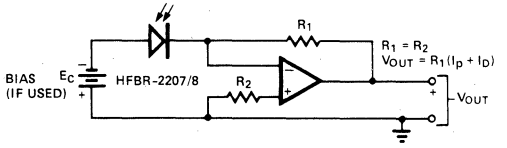
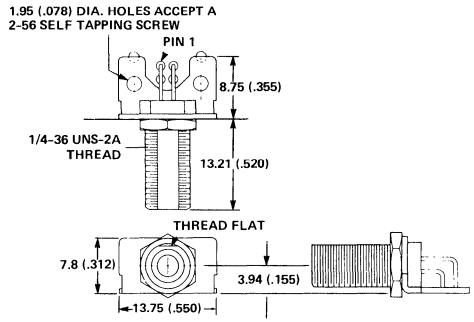


Figure 12. Linear Operation

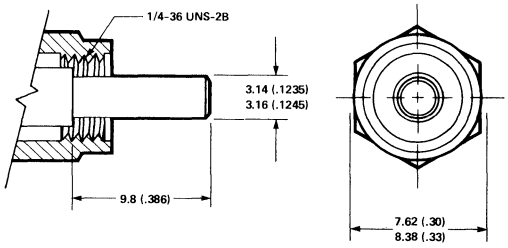
Lowest noise is obtained with $E_C = 0$, but higher speed and wider dynamic range are obtained if $5 < E_C < 20$ volts. The amplifier should have as high an input resistance as possible to permit high loop gain. If the photodiode is reversed, bias should also be reversed.

HFBR-2208 RECEIVER

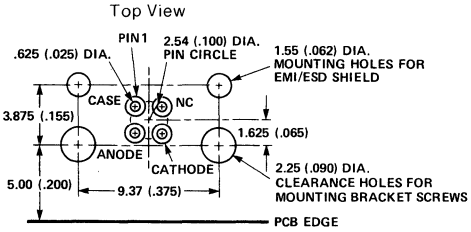


SMA STYLE CONNECTORS TYPE A

(Used on HP's 100/140 μm fiber optic cable)

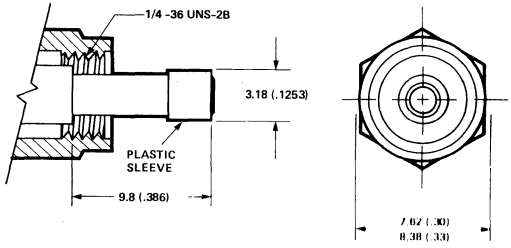


RECEIVER PCB LAYOUT DIMENSIONS



SMA STYLE CONNECTORS TYPE B

(Type B is not available from HP)



DIMENSIONS IN MILLIMETRES (INCHES).

Ordering Guide

Receivers: HFBR-2208 (SMA Connector Compatible)

Transmitters: HFBR-1202
HFBR-1204
(see data sheets)

Mounting Hardware: HFBR-4202 (SMA Connector Compatible)

Fiber Optic Cable

Hewlett-Packard offers connectored or unconnectored 100/140 μm fiber cables in simplex or duplex configurations. See data sheets for details.

HEWLETT PACKARD

1300 nm General Purpose Transmitter and Receiver

Technical Data

Transmitter HFBR-1100
Transmitter HFBR-1160
Receiver HFBR-2100

Features

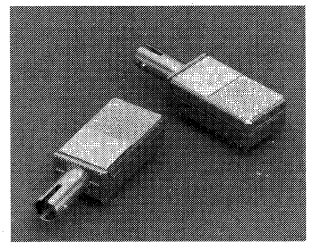
- **Data Rates from 10 MBd to 200 MBd**
- **Link Lengths of 2 km at 200 MBd**
- **Single +5 V Power Supply**
- **Shifted ECL Logic Interface**
- **High Immunity to EMI/ RFI and ESD**
- **High Reliability**
- **ST®* Style Fiber Optic Connector**
- **Multiple Sources of Supply**
- **Directly Compatible with TAXIchip™** Encode/ Decode Circuits**

Applications

- **General Purpose Serial Data Links with Encoded Data Rates of 10 MBd to 200 MBd**
- **Multimode Telecommunication Links at T3, and T3C Rates**
- **SONET Multimode Links at STS-1 and STS-3c Rates**
- **High Speed Computer to Disc or Tape Memory Interconnects**
- **Proprietary Local Area Networks**
- **High Speed Multiplexer Interconnects**
- **Digital Graphics and Digital Video Transmission Links**

Description

The general purpose transmitter and receiver products described in this data sheet are members of a growing family of 1300 nm technology fiber optic products available from Hewlett-Packard. These products supply the performance necessary for the system designer who seeks to develop data links using multimode fiber that will have distance capability beyond that obtainable with first window (820 nm wavelength) products. Link lengths of 2000 meters are possible at 200 MBd data rates with margin to spare for in-line connection losses. Longer distances are possible depending on data rate and the number of in-line connections. The performance of both the transmitter and receiver



products are guaranteed over the operating temperature and power supply voltage ranges found in most commercial equipment with sufficient margin to allow for substantial equipment mission-life and configuration flexibility.

Hewlett-Packard is a vertically integrated supplier. The 1300 nm LED and PIN devices along with the three custom bipolar integrated circuits(ICs) used in these products have been developed and manufactured by Hewlett-Packard. The assembly and testing of the transmitter and receiver products is performed in facilities wholly owned and operated by Hewlett-Packard.

*ST® is a registered trademark of AT&T for Lightguide Cable Connectors.
**TAXIchip™ is a trademark of Advanced Micro Devices, Inc.

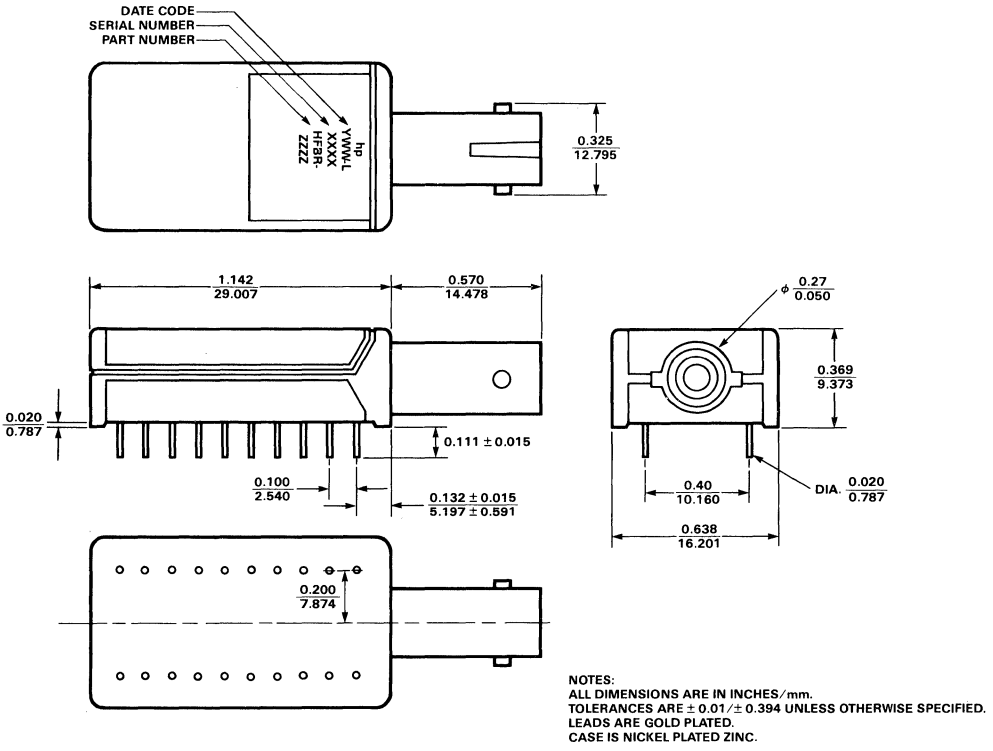


Figure 1. Outline Drawing.

Transmitters - HFBR-1100 and HFBR-1160

The transmitters use a 1300 nm InGaAsP LED and a single, custom silicon bipolar LED driver integrated circuit. The LED is an advanced planar device with an integral etched lens that provides efficient coupling to multimode fibers when combined with the Hewlett-Packard custom optical subassembly. The driver circuit provides temperature compensation for a predictable output optical power over the recommended operating temperature range. It also maintains a steady power supply current due to internal loads which conduct the LED drive current when logic "0s" are being transmitted to minimize creation of high frequency noise on power supply lines. The data input to the transmitter is differential, 100K ECL compatible, referenced (shifted) to operate from a +5 volt supply. The HFBR-1100 is specified to operate from dc to 200 MBd and the HFBR-1160 is specified from dc to 160 MBd.

Receiver - HFBR-2100

The receiver uses a 1300 nm InGaAs PIN photodiode and two custom silicon bipolar integrated circuits. The PIN is a planar top-illuminated device which provides ease of assembly into the Hewlett-Packard custom optical subassembly. The preamplifier IC is mounted in the optical subassembly with the PIN detector to maximize the receiver sensitivity. This sensitivity is guaranteed over a wide time-window in the data output eye-pattern. This assures performance with various clock recovery circuitry. The second IC, a quantizer, provides the final pulse shaping for the logic output and the Signal Detect functions. Both the data and Signal Detect logic outputs are differential, 100K ECL compatible, referenced (shifted) to a +5 volt power supply. The HFBR-2100 is specified for operation from 10 to 200 MBd and is compatible with both the HFBR-1100 and HFBR-1160 transmitters.

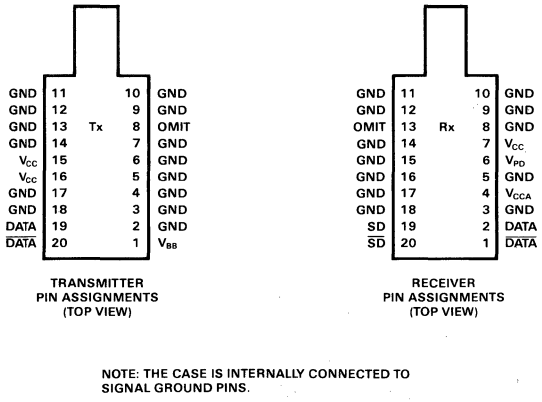


Figure 2. Pin Assignments.

Package

The overall package concept for the Hewlett-Packard general purpose transmitter and receiver products consists of three basic elements: the optical subassembly, the electrical subassembly, and the overall housing and connector port. The objective of the design is to provide consistent optoelectronic performance in commercial equipment environments over extended equipment mission-lifetimes.

The optical subassembly contains either the 1300 nm LED or the 1300 nm PIN and preamplifier devices in a hermetic enclosure which is actively aligned to a GRIN rod optical element in the precision stainless steel ferrule-bore. This active alignment provides optimal optical performance for both the transmitters and the receiver. The precision stainless steel bore assures that the ST® connector ferrule tip containing the fiber will be precisely positioned relative to the focal point of the optics.

The electrical subassembly is a multilayer, ceramic substrate containing the driver or quantizer integrated circuits along with various surface-mounted passive components. This multilayer substrate provides optimum electrical performance with good noise immunity and noise emission suppression.

The housing and connector port are die-cast zinc with nickel plating. Zinc is used for its excellent thermal conductivity which maintains the junction temperatures of the active semiconductors at the lowest levels possible for high reliability and long mission-life. The optical subassembly with its precision stainless steel connector ferrule bore fits into the ST® style bayonet connector port. The electrical and optical subassembly signal grounds are connected to the zinc housing for maximum shielding. The electrical and optical subassemblies are mounted into the zinc housing and epoxy sealed for environmental protection. The optical port is protected with an easily removable, high temperature, vinyl cap for protection from contamination during assembly onto circuit boards and shipment to the end-user site.

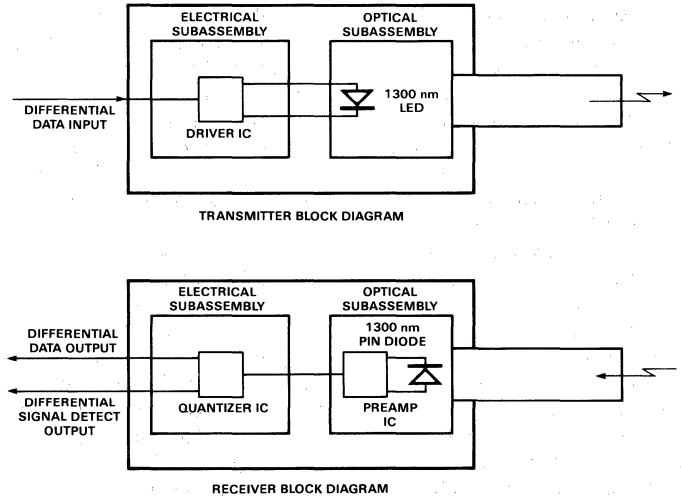


Figure 3. Block Diagrams.

Application Assistance

The Applications Engineering group in the Hewlett Packard Optical Communication Division is available to assist with the analysis of the performance of these products within a given circuit design. The effects of various data-encoding schemes and cable plants can be analyzed to predict the system performance for a particular data link.

Assistance is also available to obtain the best performance from these parts with appropriate board layout techniques for these high signaling rates. Figure 8 provides a good example of a decoupling scheme that works well with these products. Contact your local Hewlett-Packard sales representative to obtain this assistance.

Product Reliability Data

Various environmental and life tests have been performed on these products and these tests are ongoing. Contact your local Hewlett-Packard sales representative to obtain copies of the summaries of these test results as they become available.

*ST® is a registered trademark of AT&T for Lightguide Cable Connectors

General Purpose Transmitter and Receiver

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	-40		100	°C	
Operating Temperature-Ambient	T_A	-10		80	°C	Note 1
Lead Soldering Temperature	T_{SOLD}			270	°C	
Lead Soldering Time	t_{SOLD}			4	sec.	
Supply Voltage	V_{CC}	-0.5		7.0	V	Note 2
Data Input Voltage	V_I	-0.5		Vcc	V	
Differential Input Voltage	V_D			1.4	V	Note 3
Output Current	I_O			50	mA	Note 4

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Operating Temperature-Ambient	T_A	0		70	°C	Note 1
Supply Voltage	V_{CC}	4.75		5.25	V	Note 2
Supply Voltage – ECL Driver	V_{CCA}	4.75		5.25	V	Note 2
Supply Voltage – PIN	V_{PD}	4.75		5.25	V	Note 2
Data Input Voltage – Low	V_{IL} - V_{CC}	-1.810		-1.475	V	
Data Input Voltage – High	V_{IH} - V_{CC}	-1.165		-0.880	V	
Data Input Current – Low	I_{IL}	-350			µA	
Data Input Current – High	I_{IH}			350	µA	
Data and Signal Detect Output Load	R_L		50		Ω	Note 5
Signaling Rate						
HFBR-1100/2100	f_S	10		200	MBd	Note 6, Figures 4, 5
HFBR-1160/2100	f_S	10		160	MBd	Note 6, Figure 4

General Purpose Transmitter

General Purpose Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		220	270	mA	Note 7
Power Dissipation	P_{DISS}		1.1	1.4	W	
Threshold Voltage	V_{BB} - V_{CC}	-1.420		-1.240	V	Note 8

General Purpose Transmitter Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Reference
Output Optical Power						
HFBR-1100						
62.5/125 µm, NA = 0.275 Fiber	P_O	-19	-16	-14	dBm avg	Note 9
50/125 µm, NA = 0.20 Fiber	P_O		-20		dBm avg	Note 10
HFBR-1160						
62.5/125 µm, NA = 0.275 Fiber	P_O	-19	-16	-14	dBm avg	Note 11
50/125 µm, NA = 0.20 Fiber	P_O		-20		dBm avg	Note 10
Output Optical Power Temperature Coefficient	$\frac{\Delta P_O}{\Delta T}$		-0.015	-0.02	dB/°C	
Optical Extinction Ratio			0.01 -40	1 -20	% dB	Note 12
Center Wavelength	λ_C	1260	1300	1380	nm	Note 13
Spectral Width – FWHM	$\Delta\lambda$		130	170	nm	Note 14
Optical Rise Time						
HFBR-1100	t_r		1.2	2.5	ns	Note 15
HFBR-1160	t_r		1.2	3.1	ns	Note 15
Optical Fall Time						
HFBR-1100	t_f		2.3	2.5	ns	Note 15
HFBR-1160	t_f		2.3	3.1	ns	Note 15
Duty Cycle Distortion	DCD		0.10	0.35	ns pk-to-pk	Note 16
Data Dependent Jitter	DDJ		0.05	0.25	ns pk-to-pk	Note 17

General Purpose Receiver

General Purpose Receiver Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power Minimum at Window Edge	$P_{IN\ Min\ (W)}$		-34	-30.5	dBm avg	Note 18 Figures 5, 6
Minimum at Center	$P_{IN\ Min\ (C)}$		-35.5	-32.0	dBm avg	Note 19 Figures 4, 5, 6
Maximum	$P_{IN\ Max}$	-14.5	-13		dBm avg	Note 19
Operating Wavelength	λ	1260		1380	nm	
Signal Detect						
Asserted	P_A	P_D +1.5 dB	-34.5	-32	dBm avg	Note 20 Figure 7
Deasserted	P_D	-45	-37		dBm avg	Note 21 Figure 7
Hysteresis	$P_A - P_D$	1.0	2.5		dB	Figure 7

General Purpose Receiver

General Purpose Receiver Electrical Characteristics

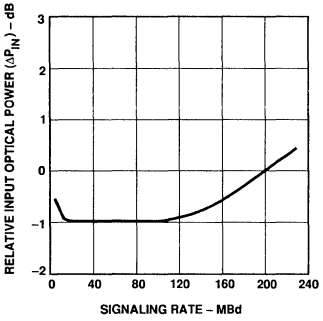
(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		70	100	mA	Note 22
Supply Current	I_{CCA}		30	40	mA	Note 22
Supply Current – PIN DIODE	I_{PD}		35	500	µA	Note 23
Power Dissipation	P_{DISS}		0.3	0.5	W	Note 24
Data Output Voltage – Low	$V_{OL} - V_{CC}$	-1.840		-1.620	V	Note 25
Data Output Voltage – High	$V_{OH} - V_{CC}$	-1.045		-0.880	V	Note 25
Data Output Rise Time	t_r	0.35	0.7	1.3	ns	Note 26
Data Output Fall Time	t_f	0.35	0.7	1.3	ns	Note 26
Duty Cycle Distortion	DCD		0.15	0.4	ns pk-to-pk	Note 27
Data Dependent Jitter	DDJ		0.40	1.0	ns pk-to-pk	Note 28
Signal Detect						
Output Voltage – Low	$V_{OL} - V_{CC}$	-1.840		-1.620	V	Note 25
Output Voltage – High	$V_{OH} - V_{CC}$	-1.045		-0.880	V	Note 25
Output Rise Time	t_r	0.35	1.0	1.6	ns	Note 29
Output Fall Time	t_f	0.35	1.0	1.6	ns	Note 29
Assert Time (off to on)	t_{SD-ON}	0	75	150	µs	Note 20 Figure 7
Deassert Time (on to off)	t_{SD-OFF}	0	190	350	µs	Note 21 Figure 7

Notes:

1. This maximum rating applies to still air environments around the transmitter and the receiver.
2. When component testing these products all supply voltages should be applied simultaneously to avoid damage to the part.
3. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
4. When component testing these products do not short the receiver data or signal detect outputs directly to ground to avoid damage to the part.
5. The outputs are terminated with 50 ohms connected to V_{CC} - 2 V.
6. The specified signaling rate guarantees operation of the transmitter and receiver link to the full conditions described in the Electrical and Optical Characteristics sections. Specifically, the link bit error ratio will be equal to or better than 10^{-12} for pseudo-random-bit-sequences (PRBS) of 2^7 - 1 data patterns with a 50% duty factor. The HFBR-1100 transmitter is capable of dc to 200 MBd operation. The HFBR-1160 is capable of operation from dc to 160 MBd. The HFBR-2100 receiver is internally ac-coupled which limits the lower signaling rate to 10 MBd. For purposes of definition, the symbol rate f_s (Baud), also called signaling rate, is the reciprocal of the shortest symbol time. Data rate (bits/sec) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit).
7. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated, whether the noise is conducted or emitted, to neighboring receiver or logic circuitry.
8. This value is measured with an output load R_L = 10 kohms.
9. These optical power values are measured with the following conditions;
   - At the Beginning Of Life (BOL).
   - Over the specified operating voltage and temperature ranges.
   - With a data input of 200 MBd (100 MHz) square wave.
   - At the end of one meter of noted optical fiber with cladding modes removed.
   - The average power value can be converted to a peak power value by adding 3 dB.
   - Higher output optical power transmitters are available on special request.
10. This transmitter is available on special request with coupled optical power guaranteed into 50/125 µm fiber cables. The value will depend on the specific NA of the 50/125 µm fiber used.
11. These optical power values are measured with the following conditions;
    - At the Beginning Of Life (BOL).
    - Over the specified operating voltage and temperature ranges.
    - With a data input of 160 MBd (80 MHz) square wave.
    - At the end of one meter of noted optical fiber with cladding modes removed.

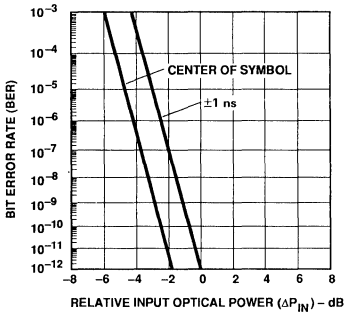
    The average power value can be converted to a peak power value by adding 3 dB. Higher output optical power transmitters are available on special request.
12. This value of Optical Extinction Ratio is the ratio of the steady state optical power in the logic-low state to the steady state optical power in the logic-high state.
13. The temperature coefficient of the center wavelength is typically +0.37 nm/°C.
14. The temperature coefficient of the spectral width is typically +0.25 nm/°C.
15. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by 12.5 MHz square wave data input.
16. Duty Cycle Distortion is measured at a 50% threshold using a 200 MBd (100 MHz) square wave input signal. The input optical power level is -20 dBm average.
17. Data Dependent Jitter is specified with a 2^7 - 1 PRBS input signal at 200 MBd. The input optical power level is -20 dBm average.
18. The Input Optical Power range from -31 dBm average to -14 dBm average is the range over which the receiver is guaranteed to provide a Data Output with a Bit Error Rate (BER) better than or equal to 1×10^{-12}. The measurement conditions are stated below.
    - At the Beginning Of Life (BOL).
    - Over the specified operating temperature and voltage ranges.
    - Input symbol pattern is 2^7 - 1 PRBS at 200 MBd.
    - Sampled over the range from the center of the symbol ±1.0 ns.
    - Input optical signal rise/fall times are approximately 1 ns/2 ns.
19. All conditions of Note 18 apply except that the measurement is made at the center of the symbol with no window time-width.
20. This value is measured during the transition from low to high levels of input optical power.
21. This value is measured during the transition from high to low levels of input optical power.
22. These values are measured with the outputs terminated into 50 ohms connected to V_{CC} - 2 V.
23. Measured at P_{IN} = -14 dBm average.
24. The power dissipation value is the power dissipated in the receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and supply currents, minus the sum of the products of the output voltages and currents.
25. These values are measured with respect to V_{CC} with the output terminated into 50 ohms connected to V_{CC} - 2 V. The minimum values are corrected for +5.25 V operation for 100K ECL values that are usually specified at -4.8 V operation.
26. The output rise and fall times are measured between 20% and 80% levels with the output connected to V_{CC} – 2 V through 50 ohms.
27. Duty Cycle Distortion is measured at a 50% threshold using a 200 MBd (100 MHz) square wave input signal. The input optical power level is -20 dBm average.
28. Data Dependent Jitter is specified with a 2^7 - 1 PRBS input signal at 200 MBd. The input optical power level is -20 dBm average.
29. The output rise and fall times are measured between 20% and 80% levels with the output connected to V_{CC} – 2 V through 50 ohms.



CONDITIONS:

1. P_{IN} NORMALIZED (ΔP_{IN} = 0 dB) TO $P_{IN\ Min}$ (C) AT 200 MBd AT CENTER OF SYMBOL.
2. $\Delta P_{IN} = P_{IN}$ @ MBd - P_{IN} @ 200 MBd
3. TEST DATA PATTERN IS PRBS 2^7 - 1.
4. BER = 10^{-12}
5. T_A = 25°C.
6. V_{CC} = 5 Vdc
7. INPUT OPTICAL RISE/FALL TIMES = 1.2 ns/2.3 ns

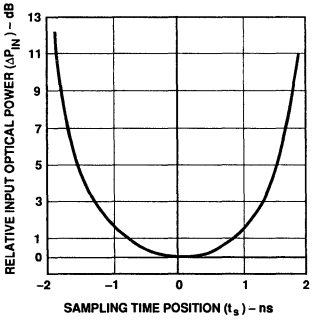
Figure 4. Relative Input Optical Power vs. Signaling Rate.



CONDITIONS:

1. P_{IN} IS NORMALIZED (ΔP_{IN} = 0 dB) TO $P_{IN\ Min}$ (w) WITH BER = 10^{-12} AND WINDOW TIME-WIDTH OF ±1.0 ns EITHER SIDE OF SYMBOL CENTER.
2. $\Delta P_{IN} = P_{IN}$ @ BER - P_{IN} @ 10^{-12} BER
3. 200 MBd TEST DATA PATTERN IS PRBS 2^{-7}- 1
4. T_A = 25°C
5. V_{CC} = 5.0 Vdc
6. INPUT OPTICAL RISE/FALL TIMES = 1.2 ns/2.3 ns

Figure 5. Typical Bit Error Rate vs. Relative Input Optical Power.



CONDITIONS:

1. P_{IN} IS NORMALIZED ($\Delta P_{IN\ Min}$ (C) AT CENTER OF SYMBOL.
2. $\Delta P_{IN} = P_{IN}$ @ t_s - P_{IN} @ t_{center}
3. TEST DATA PATTERN IS PRBS 2^7 - 1 @ 200 MBd
4. BER = 10^{-12}
5. T_A = 25°C
6. V_{CC} = 5 Vdc
7. INPUT OPTICAL RISE/FALL TIMES = 1.2 ns/2.3 ns

Figure 6. Relative Input Optical Power vs. Sampling Time Position.

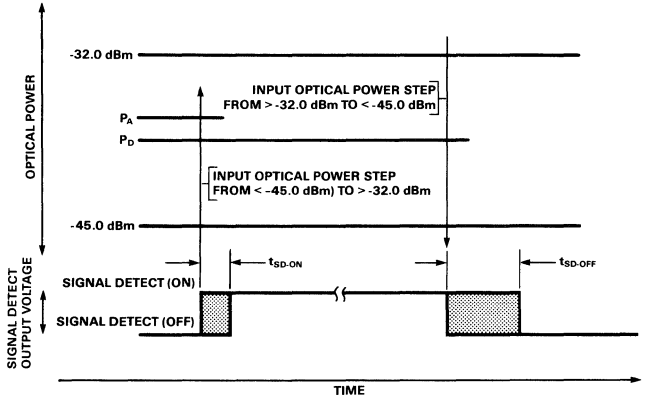
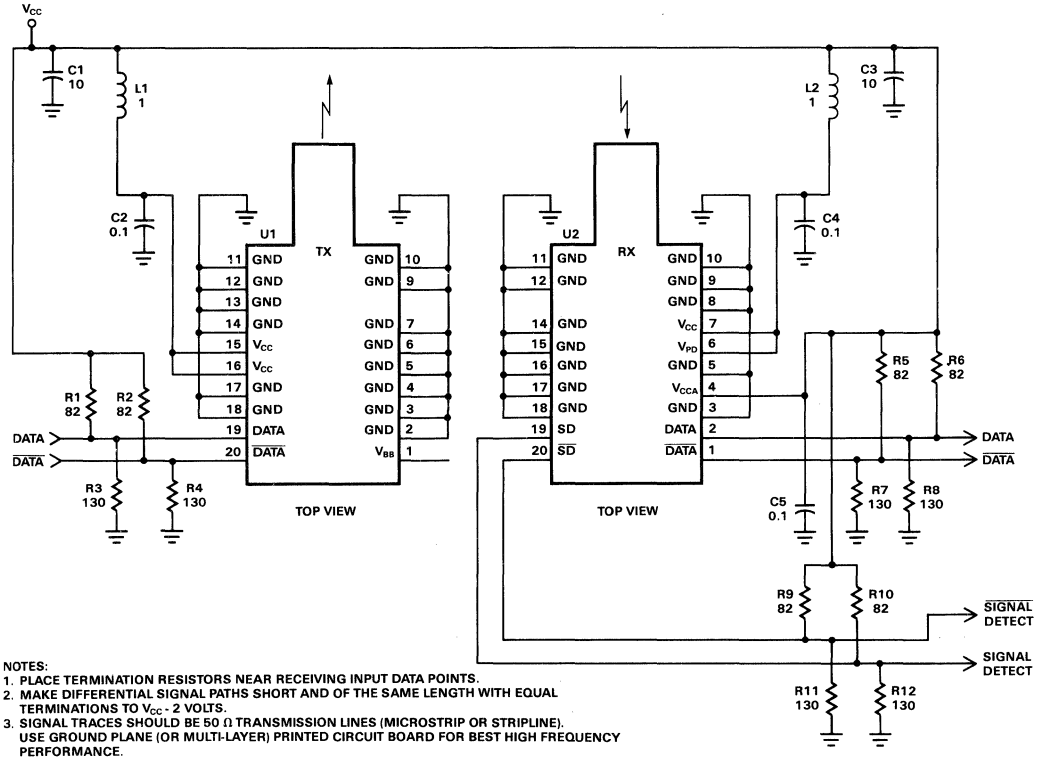


Figure 7. Signal Detect Thresholds and Timing.



NOTES:
1. PLACE TERMINATION RESISTORS NEAR RECEIVING INPUT DATA POINTS.
2. MAKE DIFFERENTIAL SIGNAL PATHS SHORT AND OF THE SAME LENGTH WITH EQUAL TERMINATIONS TO V_{CC} - 2 VOLTS.
3. SIGNAL TRACES SHOULD BE 50 Ω TRANSMISSION LINES (MICROSTRIP OR STRIPLINE). USE GROUND PLANE (OR MULTI-LAYER) PRINTED CIRCUIT BOARD FOR BEST HIGH FREQUENCY PERFORMANCE.
4. RESISTORS IN OHMS. CAPACITORS IN MICROFARADS. INDUCTORS IN MICROHENRIES.
5. USE HIGH-FREQUENCY MONOLITHIC CERAMIC BYPASS CAPACITORS AND LOW SERIES dc RESISTANCE INDUCTORS. FERRITE INDUCTORS CAN BE USED. LOCATE POWER SUPPLY FILTER, COMPONENTS CLOSE TO FIBER OPTIC DEVICES.
6. CAUTION: DO NOT DIRECTLY CONNECT FIBER OPTIC MODULE ECL OUTPUTS (DATA, $\overline{DATA}$, SIGNAL DETECT, $\overline{SIGNAL\ DETECT}$) TO GROUND WITHOUT PROPER CURRENT LIMITING IMPEDANCE.
7. ALL POWER SUPPLY VOLTAGES FOR THE FIBER OPTIC RECEIVER OR TRANSMITTER SHOULD BE APPLIED SIMULTANEOUSLY TO PREVENT POSSIBLE DAMAGE TO THE DEVICE.
8. DEVICE GROUND PINS SHOULD BE DIRECTLY AND INDIVIDUALLY CONNECTED TO GROUND.

Figure 8. Recommended Decoupling Circuit Diagram.

HEWLETT PACKARD

1300 nm FDDI Transmitter and Receiver

Technical Data

Transmitter HFBR-1125
Receiver HFBR-2125

Features

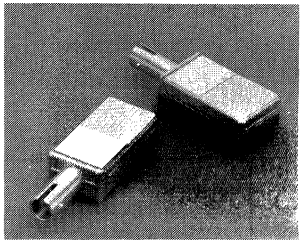
- **Full Compliance with FDDI PMD Standard Performance Requirements**
- **Single +5 V Power Supply**
- **Shifted ECL Logic Interface Directly Compatible with FDDI PHY Integrated Circuits**
- **Directly Compatible with TAXIchip™* Encode/Decode Circuits**
- **High Reliability**
- **ST®** Style Fiber Optic Connector**
- **High Immunity to EMI/RFI and ESD**

Applications

- **FDDI Single or Dual Attachment Stations**
- **FDDI Bridges, Routers and Concentrators**
- **FDDI Backbone Servers**
- **FDDI Workstations**
- **FDDI Stations With Internal Optical Bypass Switches to Minimize Board Space**
- **FDDI Stations With Packaging That Does Not Allow The Use of The FDDI Media Interface Connector (MIC)**
- **Non-FDDI Proprietary Data Links**

Description

The FDDI† transmitter and receiver described in this data sheet are members of a growing family of 1300 nm technology fiber optic products available from Hewlett-Packard. These FDDI transmitter and receiver products supply the performance necessary for the system designer who seeks to develop equipment with fully compliant FDDI interfaces per the FDDI Physical Layer Medium Dependent (PMD) standard. The performance of both the transmitter and receiver are guaranteed over the operating temperature and power supply voltage ranges found in most commercial equipment with sufficient margin over the FDDI PMD requirements to allow for substantial equipment mission-life and configuration flexibility.



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FIBER OPTICS

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**ST® is a registered trademark of AT&T for Lightguide Cable Connectors.
†FDDI represents Fiber Distributed Data Interface. The FDDI Physical Layer Medium Dependent (PMD) document has been approved as International Standard for Organization (ISO) Developmental International Standard (DIS) 9314-3.

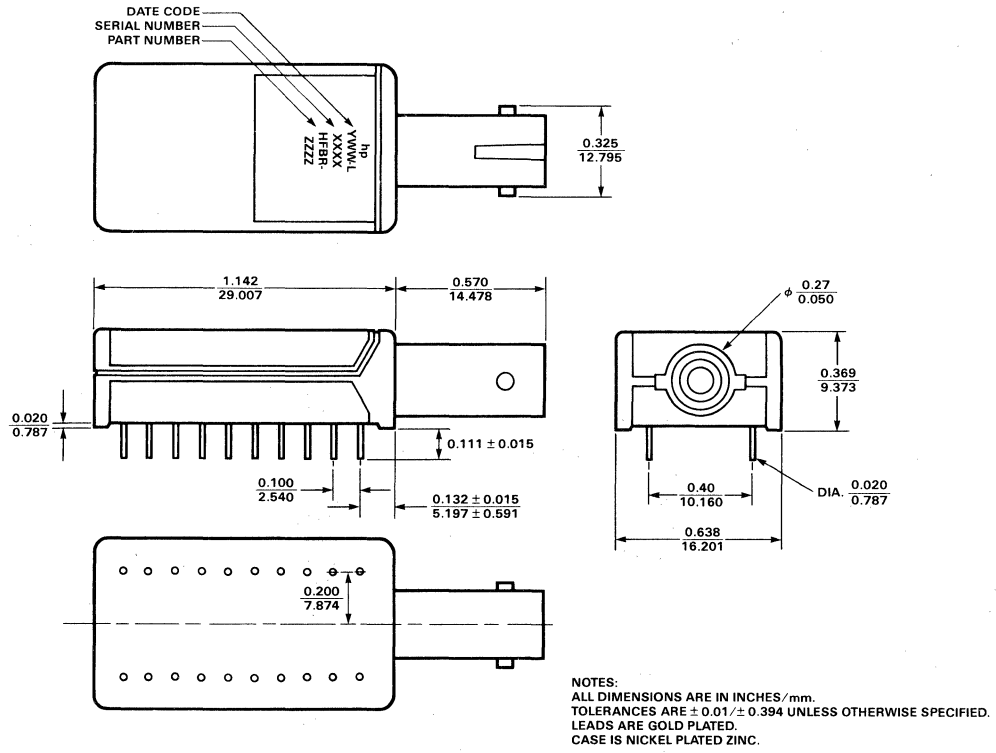


Figure 1. Outline Drawing.

Transmitter - HFBR-1125

The HFBR-1125 transmitter uses a 1300 nm InGaAsP LED and a single, custom silicon bipolar LED driver integrated circuit. The LED is an advanced planar device with an integral etched lens that provides efficient coupling to multimode fibers when combined with the Hewlett-Packard custom optical subassembly. The driver circuit provides temperature compensation for a predictable output optical power over the recommended operating temperature range. It also maintains a steady power supply current due to internal loads which conduct the LED drive current when logic "0s" are being transmitted to minimize creation of high frequency noise on power supply lines. The data input to the transmitter is differential, 100K ECL compatible, referenced (shifted) to operate from a +5 volt supply.

Receiver - HFBR-2125

The HFBR-2125 receiver uses a 1300 nm InGaAs PIN photodiode and two custom silicon bipolar integrated circuits. The PIN is a planar top-illuminated device which provides ease of assembly into the Hewlett-Packard custom optical subassembly. The preamplifier IC is mounted in the optical subassembly with the PIN detector to maximize the receiver sensitivity. This sensitivity is guaranteed over a wide time-window in the data output eye-pattern. This assures performance with the clock recovery circuit when any possible FDDI input optical signal condition exists. The second IC, a quantizer, provides the final pulse shaping for the logic output and the Signal Detect function. Both the data and Signal Detect logic outputs are differential, 100K ECL compatible, referenced (shifted) to a +5 volt power supply.

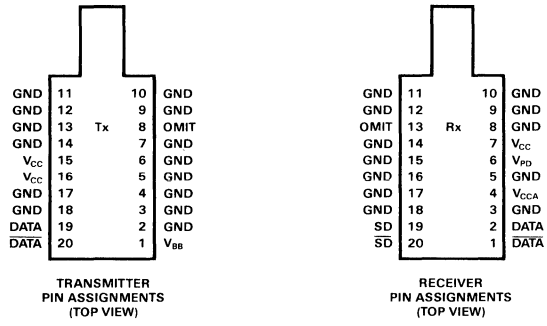


Figure 2. Pin Assignments.

Package

The overall package concept for the Hewlett-Packard FDDI transmitter and receiver consists of three basic elements: the optical subassembly, the electrical subassembly and the overall housing and connector port. The objective of the design is to provide consistent optoelectronic performance in commercial equipment environments over extended equipment mission-lifetimes.

The optical subassembly contains either the 1300 nm LED or the 1300 nm PIN and preamplifier devices in a hermetic enclosure which is actively aligned to a GRIN rod optical element in the precision stainless steel ferrule-bore. This active alignment provides optimal optical performance for both the transmitter and receiver. The precision stainless steel bore assures that the ST® connector ferrule tip containing the fiber will be precisely positioned relative to the focal point of the optics.

The electrical subassembly is a multilayer, ceramic substrate containing the driver or quantizer integrated circuits along with various surface-mounted passive components. This multilayer substrate provides optimum electrical performance with good noise immunity and noise emission suppression.

The housing and connector port are die-cast zinc with nickel plating. Zinc is used for its excellent thermal conductivity which maintains the junction temperatures of the active semiconductors at the lowest levels possible for high reliability and long mission-life. The optical subassembly with its precision stainless steel connector ferrule bore fits into the ST® style bayonet connector port. The electrical and optical subassembly signal grounds are connected to the zinc housing for maximum shielding. The electrical and optical subassemblies are mounted into the zinc housing and epoxy sealed for environmental protection. The optical port is protected with an easily removable, high temperature, vinyl cap for protection from contamination during assembly onto circuit boards and shipment to the end-user site.

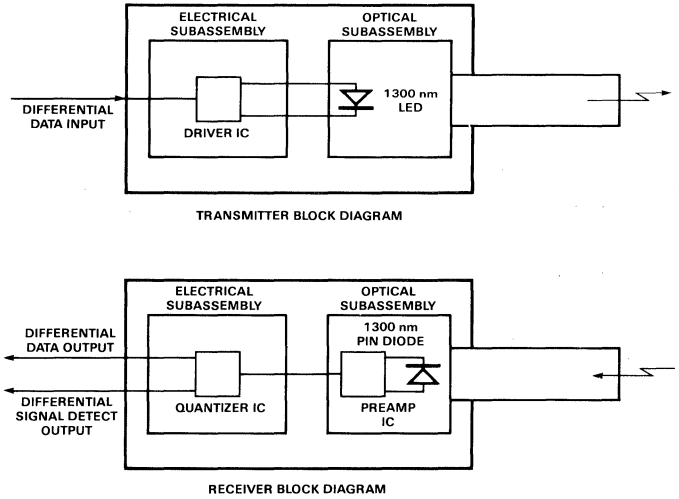


Figure 3. Block Diagrams.

Application Assistance

The Applications Engineering group in the Hewlett Packard Optical Communication Division is available to assist with the analysis of the performance of these products within a given circuit design. The effects of various data-encoding schemes and cable plants can be analyzed to predict the system performance for a particular data link.

Assistance is also available to obtain the best performance from these parts with appropriate board layout techniques for these high signaling rates. Figure 10 provides a good example of a decoupling scheme that works well with these products. Contact your local Hewlett–Packard sales representative to obtain this assistance.

Product Reliability Data

Various environmental and life tests have been performed on these products and these tests are ongoing. Contact your local Hewlett-Packard sales representative to obtain copies of the summaries of these test results as they become available.

FDDI Transmitter and Receiver

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	-40		100	°C	
Operating Temperature-Ambient	T_A	-10		80	°C	Note 1
Lead Soldering Temperature	T_{SOLD}			270	°C	
Lead Soldering Time	t_{SOLD}			4	sec.	
Supply Voltage	V_{CC}	-0.5		7.0	V	Note 2
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage	V_D			1.4	V	Note 3
Output Current	I_O			50	mA	Note 4

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Operating Temperature-Ambient	T_A	0		70	°C	Note 1
Supply Voltage	V_{CC}	4.75		5.25	V	Note 2
Supply Voltage – ECL Driver	V_{CCA}	4.75		5.25	V	Note 2
Supply Voltage – PIN	V_{PD}	4.75		5.25	V	Note 2
Data Input Voltage – Low	V_{IL} - V_{CC}	-1.810		-1.475	V	
Data Input Voltage – High	V_{IH} - V_{CC}	-1.165		-0.880	V	
Data Input Current – Low	I_{IL}	-350			µA	
Data Input Current – High	I_{IH}			350	µA	
Data and Signal Detect Output Load	R_L		50		Ω	Note 5
Signaling Rate	f_S	10		125	MBd	Note 6 Figures 4, 5

FDDI Transmitter

FDDI Transmitter Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		220	270	mA	Note 7
Power Dissipation	P_{DISS}		1.1	1.4	W	
Threshold Voltage	V_{BB} - V_{CC}	-1.420		-1.240	V	Note 8

FDDI Transmitter Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 62.5/125 µm, NA = 0.275 Fiber	P_O	-18.5	-16	-14	dBm avg	Note 9
50/125 µm, NA = 0.20 Fiber	P_O		-20		dBm avg	Note 9, 10
Output Optical Power Temperature Coefficient	$\frac{\Delta P_O}{\Delta T}$		-0.015	-0.02	dB/°C	
Optical Extinction Ratio			.01 -40	10 -10	% dB	Note 11
Center Wavelength	λ_C	1270	1300	1380	nm	Note 12 Figure 6
Spectral Width – FWHM	$\Delta\lambda$		130	170	nm	Note 13 Figure 6
Optical Rise Time	t_r	0.6	2.1	3.5	ns	Note 14 Figures 6, 7
Optical Fall Time	t_f	0.6	2.7	3.5	ns	Note 14 Figures 6, 7
Duty Cycle Distortion	DCD		0.07	0.6	ns pk-to-pk	Note 15
Data Dependent Jitter	DDJ		0.20	0.6	ns pk-to-pk	Note 16
Random Jitter	RJ		0.01	0.69	ns pk-to-pk	Note 17

FDDI Receiver

FDDI Receiver Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power						
Minimum at Window Edge	$P_{IN\ Min}$ (W)		-35.3	-32.1	dBm avg	Note 18 Figure 8
Minimum at Center	$P_{IN\ Min}$ (C)		-37.5	-34	dBm avg	Note 19 Figure 8
Maximum	$P_{IN\ Max}$	-14	-13		dBm avg	Note 19
Operating Wavelength	λ	1270		1380	nm	
Signal Detect						
Asserted	P_A	P_D +1.5 dB	-36.2	-33.5	dBm avg	Note 20, 31 Figure 9
Deasserted	P_D	-45	-38.5		dBm avg	Note 21, 32 Figure 9
Hysteresis	P_A - P_D	1.5	2.3		dB	Figure 9

FDDI Receiver Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		70	100	mA	Note 22
Supply Current	I_{CCA}		30	40	mA	Note 22
Supply Current – PIN Diode	I_{PD}		35	500	µA	Note 23
Power Dissipation	P_{DISS}		0.3	0.5	W	Note 24
Data Output Voltage – Low	V_{OL} - V_{CC}	-1.840		-1.620	V	Note 25
Data Output Voltage – High	V_{OH} - V_{CC}	-1.045		-0.880	V	Note 25
Data Output Rise Time	t_r	0.35	0.7	1.3	ns	Note 26
Data Output Fall Time	t_f	0.35	0.7	1.3	ns	Note 26
Duty Cycle Distortion	DCD		0.08	0.4	ns pk-to-pk	Note 27
Data Dependent Jitter	DDJ		0.40	1.0	ns pk-to-pk	Note 28
Random Jitter	RJ			2.14	ns pk-to-pk	Note 29
Signal Detect						
Output Voltage – Low	V_{OL} - V_{CC}	-1.840		-1.620	V	Note 25
Output Voltage – High	V_{OH} - V_{CC}	-1.045		-0.880	V	Note 25
Output Rise Time	t_r	0.35	1.0	1.6	ns	Note 30
Output Fall Time	t_f	0.35	1.0	1.6	ns	Note 30
Assert Time (off to on)	AS_Max	0	75	100	µs	Note 20, 31 Figure 9
Deassert Time (on to off)	ANS_Max	0	190	350	µs	Note 21, 32 Figure 9

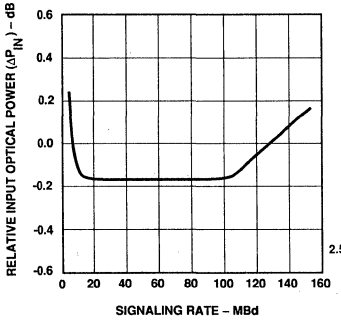
Notes:

1. This maximum rating applies to still air environments around the transmitter and receiver.
2. When component testing these products all supply voltages should be applied simultaneously to avoid damage to the part.
3. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
4. When component testing these products do not short the receiver data or signal detect outputs directly to ground to avoid damage to the part.
5. The outputs are terminated with 50 ohms connected to V_{CC} - 2 V.
6. The specified signaling rate of 10 MBd to 125 MBd guarantees operation of the transmitter and receiver link to the full conditions listed in the FDDI Physical Layer Medium Dependent standard. Specifically, the link bit error ratio will be equal to or better than 2.5 x 10^{-10} for any valid FDDI pattern. The transmitter section of the link is capable of dc to 125 MBd operation. The receiver is internally ac-coupled which limits the lower signaling rate to 10 MBd. For purposes of definition, the symbol rate (Baud), also called signaling rate, f_s, is the reciprocal of the shortest symbol time. Data rate (bits/sec) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit).
7. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated, whether the noise is conducted or emitted, to neighboring receiver or logic circuitry.
8. This value is measured with an output load R_L = 10 kohms.
9. These optical power values are measured with the following conditions;
   - At the Beginning Of Life (BOL).
   - Over the specified operating voltage and temperature ranges.
   - With HALT Line State, (12.5 MHz) square-wave, input signal.
   - At the end of one meter of noted optical fiber with cladding modes removed.

   The average power value can be converted to a peak power value by adding 3 dB.

   Higher output optical power transmitters are available on special request.
10. This transmitter is available on special request with coupled optical power guaranteed into 50/125 µm fiber cables. The value will depend on the specific NA of the 50/125 µm fiber used.
11. The Extinction Ratio is a measure of the modulation depth of the optical signal. The data "0" output optical power is compared to the data "1" peak output optical power and expressed as a percentage. With the transmitter driven by a HALT Line State (12.5 MHz square-wave) the optical signal is detected with a receiver that linearly converts optical power to voltage, the extinction ratio is the ratio of the voltage of the "0" level compared to the voltage at the "1" level expressed as a percentage.
12. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 6. The temperature coefficient of the center wavelength is typically +0.37 nm/°C.
13. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 6. The temperature coefficient of the spectral width is typically +0.25 nm/°C.
14. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 6. This parameter also complies with the optical pulse envelope shown in Figure 7. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by the FDDI HALT Line State logic input signal.
15. Duty Cycle Distortion is measured at a 50% threshold using an IDLE Line State, 125 MBd (62.5 MHz) square-wave, input signal.
16. Data Dependent Jitter is specified with the FDDI test pattern described in FDDI PMD Appendix A.5.
17. Random Jitter is specified with an IDLE Line State, 125 MBd (62.5 MHz) square-wave, input signal.
18. The Input Optical Power dynamic range, from the maximum value of "$P_{IN\ Min}$ (W)" to the minimum value of "$P_{IN\ Max}$", is the range over which the receiver is guaranteed to provide output data with a Bit Error Rate (BER) better than or equal to 2.5 x 10^{-10}. The BER will be better than or equal to 1 x 10^{-12} at input optical power levels greater than the maximum "$P_{IN\ Min}$ (W)" plus approximately 0.8 dB with this Hewlett-Packard receiver. This is 1.2 dB better than required by the FDDI PMD. The measurement conditions are stated below.
   - At the Beginning of Life (BOL)
   - Over the specified operating temperature and voltage ranges
   - Input symbol pattern is the FDDI test pattern defined in FDDI PMD Appendix A.5 with 4B/5B NRZI encoded data that contains a baseline wander effect of 50 kHz. Baseline wander is the alternation of data that contains a low frequency variation in the data pattern.
   - Input optical rise and fall times are approximately 1 ns and 2 ns respectively.
   - Sampled over the range from the center of the symbol ±2.3 ns. This is because a window time-width of 4.6 ns is the worst case allowed between the FDDI PMD Active Input Interface and the FDDI PHY PM_Data.indication input per the example in FDDI PMD Appendix E. This window time-width value is based upon a nearly ideal input optical signal presented to the receiver, i.e., no DCD, insignificant DDJ and RJ and fast optical rise and fall times. Per the Appendix E example the receiver is allowed to contribute a peak-to-peak jitter of DCD(0.4ns) + DDJ(1.0ns) + RJ(2.14ns pk-pk) = 3.54ns. The valid data window time-width then becomes 8.0ns - 3.54ns = 4.46ns, or conservatively 4.6ns.
19. All conditions of Note 18 apply except that the measurement is made at the center of the symbol with no window time-width.
20. This value is measured during the transition from low to high levels of input optical power.
21. This value is measured during the transition from high to low levels of input optical power. The minimum value will be either -45 dBm average or when the input optical power yields a BER of 10^{-2} or less which ever power is higher.

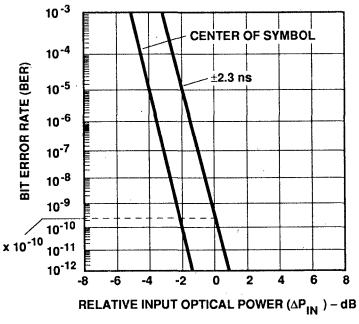
22. These values are measured with the outputs terminated into 50 ohms connected to V_{CC} - 2 V.
23. Measured at P_{IN} = -14 dBm average.
24. The power dissipation value is the power dissipated in the receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and supply currents, minus the sum of the products of the output voltages and currents.
25. These values are measured with respect to V_{CC} with the output terminated into 50 ohms connected to V_{CC} - 2 V. The minimum values are corrected for +5.25 V operation for 100K ECL values that are usually specified at -4.8 V operation.
26. The output rise and fall times are measured between 20% and 80% levels with the output connected to V_{CC} - 2 V through 50 ohms.
27. Duty Cycle Distortion is measured at a 50% threshold using an IDLE pattern, 125 MBd (62.5 MHz) square-wave, input signal. The input optical power level is -20 dBm average.
28. Data Dependent Jitter is specified with the FDDI test pattern described in PMD Appendix A.5. The input optical power level is -20 dBm average.
29. Random Jitter is specified with an IDLE Line State pattern, 125 MBd (62.5 MHz) square-wave, input signal. The input optical power level is at maximum "P_{IN_Min} (W)".
30. The output rise and fall times are measured between 20% and 80% levels with the output connected to V_{CC} - 2 V through 50 ohms.
31. The Signal Detect output shall be asserted within 100 µs after a step increase of the Input Optical Power. The step will be from a low Input Optical Power, ≤ -45 dBm, into the range between greater than P_A and -14 dBm. The BER of the receiver output will be less than 10^{-2} from 15 µs (LS_Max) after Signal Detect has been asserted. See Figure 9 for more information.
32. Signal detect output shall be deasserted within 350 µs after a step decrease in the Input Optical Power from a level which is the lower of; -31 dBm or P_D + 4 dB (P_D is the power level at which signal detect was deasserted), to a power level of -45 dBm or less. This step decrease will have occurred in less than 8 ns. The receiver output will have a BER of 10^{-2} or less for a period of 12 µs or until signal detect is deasserted. The input data stream is Quiet symbols. Also, signal detect will be deasserted within a maximum of 350 µs after the BER of the receiver output degrades below 10^{-2} for an input optical data stream that decays with a negative ramp function instead of a step function. See Figure 9 for more information.



CONDITIONS:

1. P_{IN} NORMALIZED (ΔP_{IN} = 0 dB) TO $P_{IN\ Min}$ (C) AT 125 MBd AT CENTER OF SYMBOL.
2. $\Delta P_{IN} = P_{IN}$ @ MBd - P_{IN} @ 125 MBd
3. FDDI PMD APPENDIX A.5 125 MBd TEST PATTERN WITH 50 kHz BASELINE WANDER
4. BER = 2.5 X 10^{-10}
5. T_A = 25°C
6. V_{CC} = 5 Vdc
7. INPUT OPTICAL RISE/FALL TIMES = 1.0 ns/2.1 ns

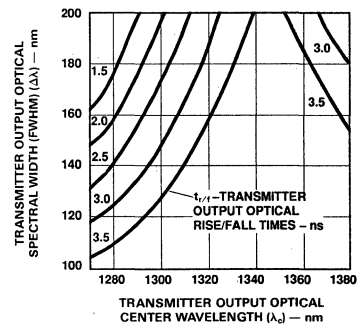
Figure 4. Relative Input Optical Power vs. Signaling Rate.



CONDITIONS:

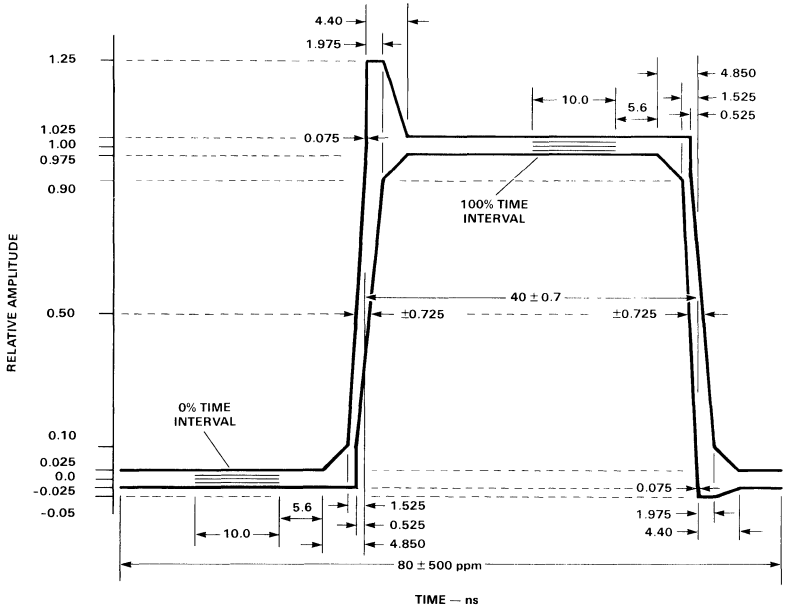
1. P_{IN} IS NORMALIZED (ΔP_{IN} = 0 dB) AT $P_{IN\ Min}$ (W) WITH BER = 2.5 x 10^{-10} AND WINDOW TIME-WIDTH OF ±2.3 ns EITHER SIDE OF SYMBOL CENTER.
2. $\Delta P_{IN} = P_{IN}$ @ BER - P_{IN} @ 2.5 x 10^{-10} BER
3. FDDI PMD APPENDIX A.5 125 MBd TEST PATTERN WITH 50 kHz BASELINE WANDER.
4. T_A = 25°C
5. V_{CC} = 5.0 Vdc
6. INPUT OPTICAL RISE/FALL TIMES = 1.0 ns/2.1 ns

Figure 5. Typical Bit Error Rate vs. Relative Input Optical Power.



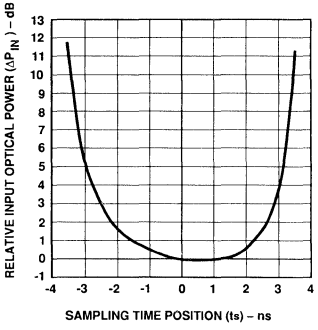
HEWLETT PACKARD FDDI TRANSMITTER TEST RESULTS OF λ_C, $\Delta\lambda$ AND $t_{r/f}$ ARE CORRELATED AND COMPLY WITH THE ALLOWED SPECTRAL WIDTH AS A FUNCTION OF CENTER WAVELENGTH FOR VARIOUS RISE AND FALL TIMES. REFERENCE FIGURE 5-1 OF FDDI PMD.

Figure 6. Transmitter Output Optical Spectral Width (FWHM) vs. Transmitter Output Optical Center Wavelength.



THE OUTPUT OPTICAL PULSE SHAPE SHALL FIT WITHIN THE BOUNDARIES OF THE PULSE ENVELOPE. FOR RISE AND FALL TIME MEASUREMENTS, THE MAXIMUM POSITIVE AND MINIMUM NEGATIVE WAVEFORM EXCURSIONS IN THE ZERO AND 100% TIME INTERVALS SHALL BE CENTERED AROUND THE 0.0 AND 1.00 LEVELS, RESPECTIVELY. A MINIMUM BANDWIDTH RANGE OF 100 kHz TO 750 MHz IS REQUIRED FOR THE MEASUREMENT EQUIPMENT USED TO EVALUATE THE PULSE ENVELOPE.

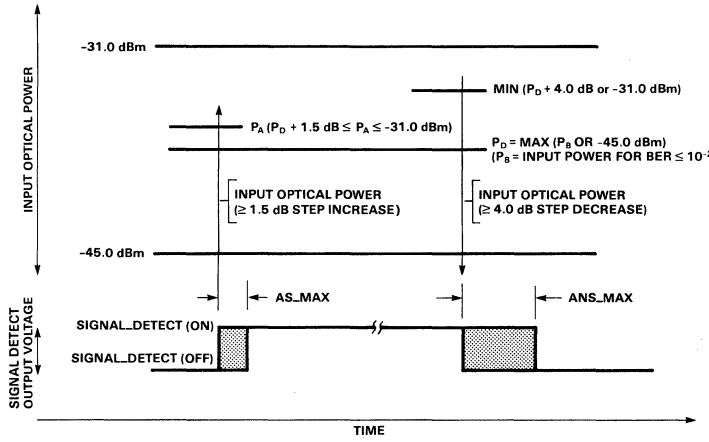
Figure 7. Output Optical Pulse Envelope.



CONDITIONS:

1. P_{IN} IS NORMALIZED TO $P_{IN\ Min}$ (C) AT CENTER OF SYMBOL.
2. $\Delta P_{IN} = P_{IN}$ @ $t_s - P_{IN}$ @ t_{center}
3. FDDI PMD APPENDIX A.5 125 MBd TEST PATTERN WITH 50 kHz BASELINE WANDER.
4. BER = 2.5×10^{-10}
5. $T_A = 25°C$
6. $V_{CC} = 5$ Vdc
7. INPUT OPTICAL RISE/FALL TIMES = 1.0 ns/2.1 ns

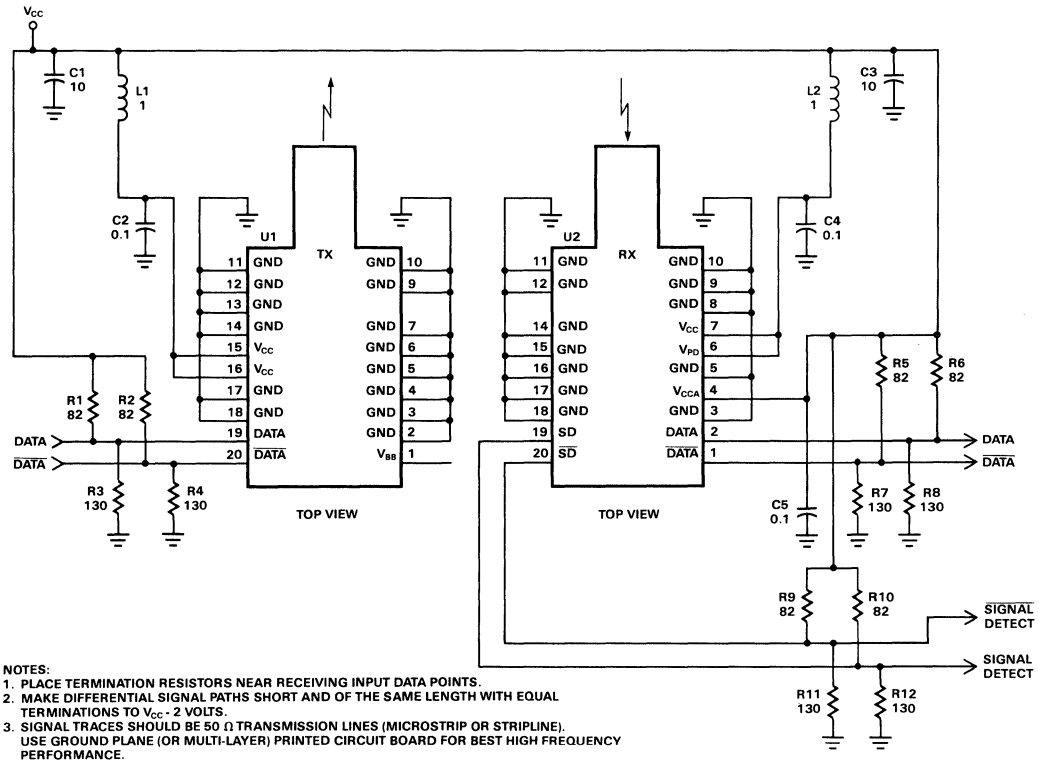
Figure 8. Relative Input Optical Power vs. Sampling Time Position.



AS_MAX—MAXIMUM ACQUISITION TIME (SIGNAL).
AS_MAX IS THE MAXIMUM SIGNAL_DETECT ASSERTION TIME FOR THE STATION.
AS_MAX SHALL NOT EXCEED 100.0 μs. THE DEFAULT VALUE OF AS_MAX IS 100.0 μs.

ANS_MAX—MAXIMUM ACQUISITION TIME (NO SIGNAL).
ANS_MAX IS THE MAXIMUM SIGNAL_DETECT DEASSERTION TIME FOR A STATION.
ANS_MAX SHALL NOT EXCEED 350 μs. THE DEFAULT VALUE OF ANS_MAX IS 350 μs.

Figure 9. Signal Detect Thresholds and Timing.



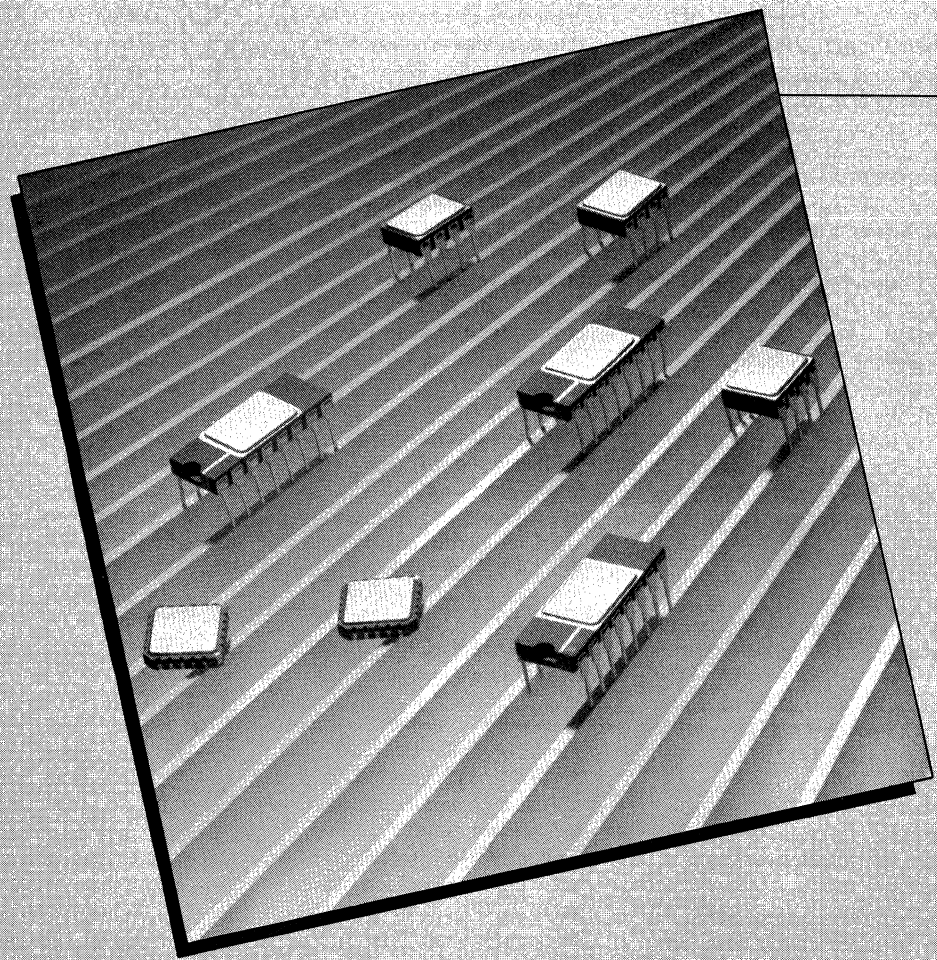
NOTES:
1. PLACE TERMINATION RESISTORS NEAR RECEIVING INPUT DATA POINTS.
2. MAKE DIFFERENTIAL SIGNAL PATHS SHORT AND OF THE SAME LENGTH WITH EQUAL TERMINATIONS TO V_{CC} - 2 VOLTS.
3. SIGNAL TRACES SHOULD BE 50 Ω TRANSMISSION LINES (MICROSTRIP OR STRIPLINE). USE GROUND PLANE (OR MULTI-LAYER) PRINTED CIRCUIT BOARD FOR BEST HIGH FREQUENCY PERFORMANCE.
4. RESISTORS IN OHMS. CAPACITORS IN MICROFARADS. INDUCTORS IN MICROHENRIES.
5. USE HIGH-FREQUENCY MONOLITHIC CERAMIC BYPASS CAPACITORS AND LOW SERIES dc RESISTANCE INDUCTORS. FERRITE INDUCTORS CAN BE USED. LOCATE POWER SUPPLY FILTER, COMPONENTS CLOSE TO FIBER OPTIC DEVICES.
6. CAUTION: DO NOT DIRECTLY CONNECT FIBER OPTIC MODULE ECL OUTPUTS (DATA, $\overline{\text{DATA}}$, SIGNAL DETECT, $\overline{\text{SIGNAL DETECT}}$) TO GROUND WITHOUT PROPER CURRENT LIMITING IMPEDANCE.
7. ALL POWER SUPPLY VOLTAGES FOR THE FIBER OPTIC RECEIVER OR TRANSMITTER SHOULD BE APPLIED SIMULTANEOUSLY TO PREVENT POSSIBLE DAMAGE TO THE DEVICE.
8. DEVICE GROUND PINS SHOULD BE DIRECTLY AND INDIVIDUALLY CONNECTED TO GROUND.

Figure 10. Recommended Decoupling Circuit Diagram.

HEWLETT PACKARD

Optocouplers

- High Speed Optocouplers
- Low Current Optocouplers
- High Gain Optocouplers
- Application Specific Optocouplers
- Hermetic Optocouplers (pg 6-203)



Optocouplers

Plastic Optocouplers

Put an end to erroneous data, false control signals, and damaged circuits with HP's line of high-performance plastic optocouplers. There are six basic families of optocouplers to choose from: high-speed logic gate, high-speed transistor output, high-gain, high-speed CMOS logic-to-logic, AC/DC-to-logic interface, and 20 mA current loop. All plastic optocouplers are UL approved and have a withstand voltage of 2500 Vrms/1 minute as a standard feature. A 5000 Vrms/1 minute option is available on selected families. VDE 0883 approval has been obtained for our entire line of plastic optocouplers. Also available are two surface mount options for our standard package.

New this year are two new packages and a new optocoupler family. A true surface mount SO-8 package is available for all 6N series optocouplers, the HCPL-2601/11, and the HCPL-4502/3.

A VDE 0884 approved version of the 6N135/6 and 6N138/9 optocouplers has been designed to meet safety requirements worldwide. The CNW135/6 and CNW138/9 optocouplers feature a "widebody" package to ensure conformance to stringent creepage and clearance requirements.

The HCPL-7100 is the first optocoupler of our new CMOS family. This optocoupler combines the latest CMOS IC technology, a new high-speed AlGaAs LED and an optimized light coupling system to achieve outstanding performance with very low power consumption.

Common mode noise rejection has been improved on several of our optocouplers. Enhanced performance up to 15 kV/μs and a Vcm of 1500 volts are available.

Hewlett-Packard offers a new miniature solid-state relay featuring withstand voltages of 200 V; and current rating of 40 mA. This 4 pin dual in-line package (DIP) product offers the reliability and long life required in instrumentation, telecommunication, and industrial control applications. The HSSR-8200 replaces electromechanical relays now used in signal and low power switching applications.

Furthermore, with Hewlett-Packard's solid-state relays you get lower power dissipation as a result of the 1 mA control current requirement. The HSSR-8200 features an output with very low leakage current, offset voltage, and capacitance which permits the design of multiplexers that require greater measurement accuracy.

A Selection Flowchart has been added immediately following this introduction to facilitate selection of the correct optocoupler or solid state relay for your application.

Product Safety Regulations and Optocouplers

Optocouplers are frequently used to optically connect a signal line to an electrical circuit in a piece of equipment. Besides providing signal isolation, the optocoupler may be used to provide high voltage insulation. It does this by preventing voltage transients on

a signal line from affecting the equipment, and by preventing high voltage powerline transients, which may be present inside the box, from reaching an equipment user.

Because optocouplers perform this safety function, they are regulated by many national safety agencies. They can be regulated in two ways: at a component level, as UL (US) and VDE (West Germany) do and at an electrical system or sub-system level. Additional national agencies that have regulations concerning optocouplers include BSI (UK), CSA (Canada), and FEI (Finland).

The key items that are regulated are insulation integrity under an array of use conditions, flammability, and in the case of telecommunications applications, ability to protect the telecom network and equipment connected to it. Different types of equipment have different levels of requirements.

Insulation Coordination

The equipment designer selecting an optocoupler to provide insulation uses the principles of insulation coordination found in the IEC 664 and 664A (1980 and 1981). The optocoupler must block both the working voltage and allowable transients. The driving factors are power line (or working) voltage, installation classification, and pollution degree. The higher the installation class, the higher the magnitude of transient voltages on the line can be. The power line voltage and the max rated impulse value together determine the CLEARANCE (distance through air between input metal and output metal).

The power line voltage, pollution degree, and CTI (comparative tracking index) of the molding compound determine the CREEPAGE, (minimum distance along the surface of the package from input metal to output metal). Pollution degree comes from the end-use application and corresponds to the conductivity of dust, dirt, water, etc. that the optocoupler may be exposed to. The higher the CTI, the more resistant the material is to electrical arc tracking, so the creepage distances can be smaller.

VDE 0883 and 0884

There are currently two VDE standards that govern optocouplers, VDE 0883 and its successor, VDE 0884. As of January 1990 VDE 0883 approval will no longer be granted for new equipment. A grandfather clause will be in effect for two years to allow time for recertification under VDE 0884. There are two basic differences between the standards: the dielectric voltage test and the manner in which the parts are evaluated for equipment applications. The production dielectric test in VDE 0883 is a one-minute withstand test of four times the working voltage plus one kilovolt AC. The production test in VDE 0884 is a more sensitive test which measures partial discharge carried out at a lower voltage to guarantee the integrity of the insulation. Parts submitted under VDE 0883 would also be evaluated for suitability for various equipment applications. Each equipment standard is listed separately on the optocoupler license. This will no longer be the case under VDE 0884. VDE 0884 is a safety standard, VDE 0883 was not. The partial discharge testing of VDE 0884 more thoroughly guarantees the insulation integrity than VDE 0883 could. VDE supplies a letter saying which equipment standards the VDE 0884 optocoupler is suitable for.

Currently, all Hewlett-Packard plastic bipolar optocouplers are certified to VDE 0883 and UL 1577. In addition, the CNW family of "widebody" optocouplers and the HCPL-7100 CMOS optocoupler are certified to VDE 0884 and have received other approvals from agencies worldwide.

Please see the data sheets of these products for a complete list.

Optocoupler for Safe Electrical Separation per VDE 0884

Optocouplers providing safe electrical separation per VDE 0884 do so only within the safety-limiting values to which they are qualified. Protective cut-out switches must be used to ensure that the safety limits are not exceeded.

The partial discharge measurement ensures that no partial discharge will occur

during operation at maximum allowable working insulation voltage ($V_{INITIAL}$). Prolonged partial discharge degrades the insulation material and can lead to high voltage breakdown.

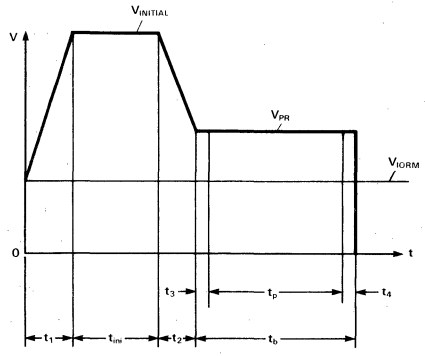
The Mains Voltage and Installation Class desired determines the required voltages for Type and Production testing. For example, if the mains voltage is 300 volts and the Installation Class desired is Class III, then $V_{INITIAL}$ must be 2828 Vrms (4000 V peak). V_{PR} is determined from the value of V_{IORM}. See Figure 1 and Table 1 below.

TIME – TEST VOLTAGE DIAGRAM IN ACC. WITH VDE 0884

PROCEDURE A)

(FOR TYPE AND SAMPLING TESTS, DESTRUCTIVE TESTS)

t_1, t_2 = 1 to 10 s
t_3, t_4 = 1 s
t_p (MEASURING TIME FOR PARTIAL DISCHARGE) = 60 s
t_b = 62 s
t_{ini} = 10 s



PROCEDURE B)

(FOR 100% PRODUCTION TESTING)

t_3, t_4 = 0.1 s
t_p (MEASURING TIME FOR PARTIAL DISCHARGE) = 1 s
t_b = 1.2 s

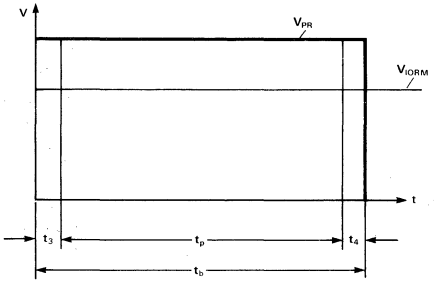


Figure 1.

Table 1.

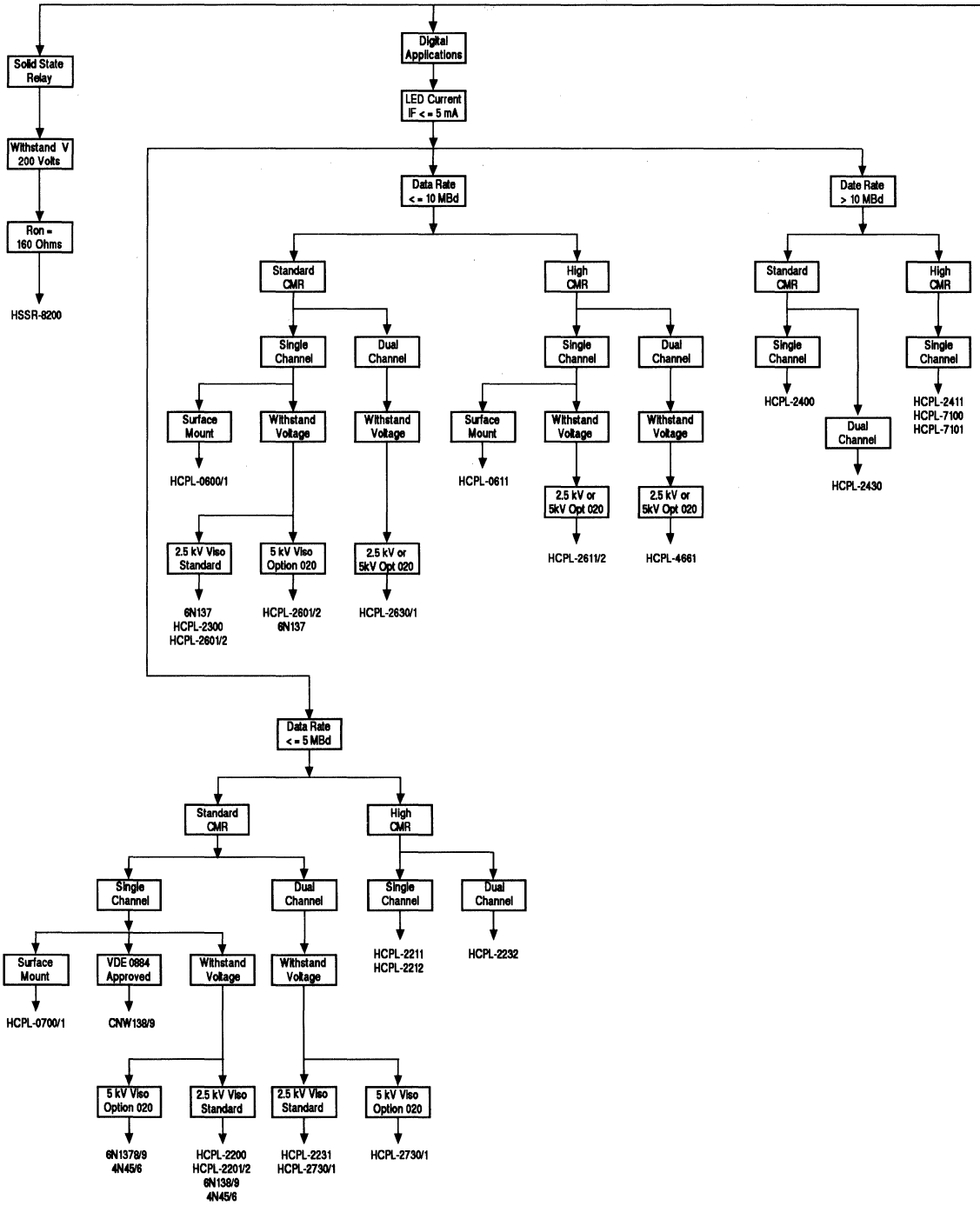
Mains Voltage (RMS) V_{IORM}	Preferred Insulation Test Voltages for Service Class ($V_{INITIAL}$) I PEAK (VAC)	I RMS (VAC)	II PEAK (VAC)	II RMS (VAC)	III PEAK (VAC)	III RMS (VAC)	IV PEAK (VAC)	IV RMS (VAC)
50	330	233	500	353	800	565	1500	1060
100	500	353	800	565	1500	1060	2500	1767
150	800	656	1500	1060	2500	1767	4000	2828
300	1500	1060	2500	1767	4000	2828	6000	4242
600	2500	1767	4000	2828	6000	4242	8000	5656
1000	4000	2828	6000	4242	8000	5656	12000	8484

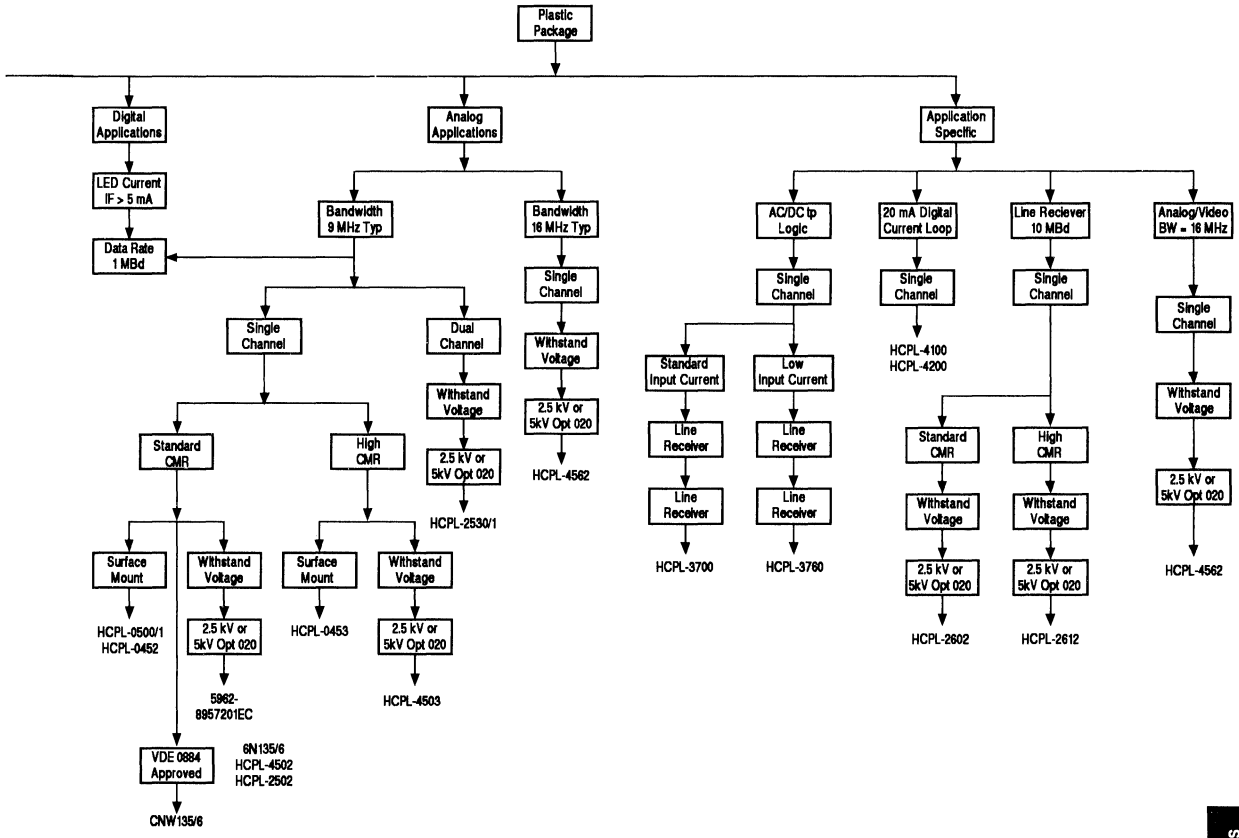
Either the peak AC or the RMS ac test voltage can be used in this test. In the case of the AOT VISO-700 tester the RMS test voltage has to be used because test voltage settings are in RMS.

Definition of Terms Used in the Qualification Test Diagram

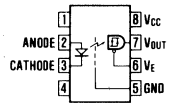
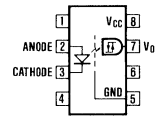
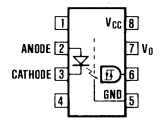
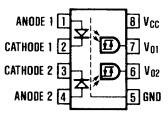
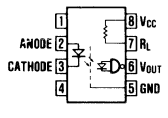
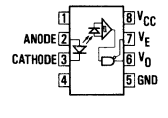
Term Name	Definition
$V_{INITIAL}$	Maximum test voltage applied to device under test. This voltage is determined from the Mains Voltage rating and the preferred insulation test voltage by service class.
V_{PR}	Test voltage applied to the device to verify isolation capacity. This voltage is usually 1.2 times the mains rating (V_{IORM}) for Procedure a and 1.6 times V_{IORM} for Procedure b.
V_{IORM}	Maximum continuous voltage which may be applied to device. Also known as the mains voltage in Table 2, above.
T_P	Test time for partial discharge testing and equals 60 seconds.
T (ini)	Time at $V_{INITIAL}$ test voltage and equals 10 seconds.
T1, T2, T3, T4	These test times are preset by the VISO-700 and are not to be adjusted.
Pass/Fail Criteria	No leakage failures and no unit to have more than 5 pC Partial Discharge during partial discharge test time T_P.

Optocoupler and Solid State Relay Selection Flowchart

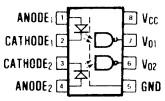
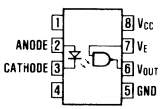
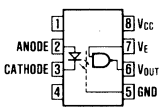
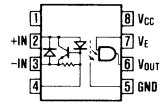
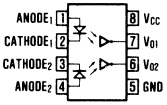



Plastic Package
Digital Applications
LED Current IF > 5 mA
Data Rate 1 MBd
Surface Mount
HCPL-0500/1 HCPL-0452
Withstand Voltage
2.5 kV or 5kV Opt 020
5962-8957201EC
VDE 0884 Approved
CNW135/6
6N135/6 HCPL-4502 HCPL-2502
Standard CMR
High CMR
Surface Mount
HCPL-0453
Withstand Voltage
2.5 kV or 5kV Opt 020
HCPL-4503
Single Channel
Dual Channel
Withstand Voltage
2.5 kV or 5kV Opt 020
HCPL-2530/1
Analog Applications
Bandwidth 9 MHz Typ
Bandwidth 16 MHz Typ
Single Channel
Withstand Voltage
2.5 kV or 5kV Opt 020
HCPL-4562
Application Specific
AC/DC tp Logic
Single Channel
Standard Input Current
Line Receiver
Line Receiver
HCPL-3700
Low Input Current
Line Receiver
Line Receiver
HCPL-3760
20 mA Digital Current Loop
Single Channel
HCPL-4100 HCPL-4200
Standard CMR
Withstand Voltage
2.5 kV or 5kV Opt 020
HCPL-2602
Line Reciever 10 MBd
Single Channel
High CMR
Withstand Voltage
2.5 kV or 5kV Opt 020
HCPL-2612
Analog/Video BW = 16 MHz
Single Channel
Withstand Voltage
2.5 kV or 5kV Opt 020
HCPL-4562

High-Speed Logic Gate Optocouplers

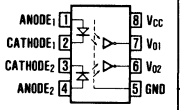
Device		Description	Application	Typical Data Rate [NRZ]	Guaranteed CMR	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	HCPL-2200	3 State Output Low Input Current Optically Coupled Logic Gate V_{CC} = 20 V Max.	High Speed Logic Ground Isolation, LSTTL, TTL, CMOS Logic Interface	5 Mb/s	1000 V/µs @ V_{CM} = 50 V	1.6 mA	2500 Vac/ 1 min. VDE 0883	6-17
	HCPL-2219				5000 V/µs @ V_{CM} = 800 V			
	HCPL-2201	Low Input Current Optically Coupled Logic Gate V_{CC} = 20 V Max.			1000 V/µs @ V_{CM} = 50 V			6-22
	HCPL-2211				5000 V/µs @ V_{CM} = 800 V			
	HCPL-2202		Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments		1000 V/µs @ V_{CM} = 50 V			
	HCPL-2212				5000 V/µs @ V_{CM} = 800 V			
	HCPL-2231	Dual Channel Low Input Current Optically Coupled Logic Gate V_{CC} = 20 V Max.	High Speed Logic Ground Isolation, LSTTL, TTL, CMOS Logic Interface	5 Mb/s	1000 V/µs @ V_{CM} = 50 V	1.8 mA	2500 Vac/ 1 min. VDE 0883	6-27
	HCPL-2232		Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments		5000 V/µs @ V_{CM} = 800 V			
	HCPL-2300	Very Low Input Current, High Speed Optocoupler	High Speed, Long Distance Line Receiver, Computer Peripheral Interfaces, CMOS Logic Interface	8 Mb/s	100 V/µs @ V_{CM} = 50 V	0.5 mA	2500 Vac/ 1 min. VDE 0883	6-32
	HCPL-2400	20 MBaud, High Common Mode Rejection, Optically Coupled Logic Gate 3 State Output	Very High Speed Logic Isolation, I/O and Parallel-to-Serial Conversion	40 Mb/s	1000 V/µs @ V_{CM} = 50 V	4.0 mA	2500 Vac/ 1 min. VDE 0883	6-39
	HCPL-2411		Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments		1000 V/µs @ V_{CM} = 300 V			

High-Speed Logic Gate Optocouplers (Continued)

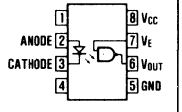
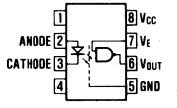
Device		Description	Application	Typical Data Rate [NRZ]	Guaranteed CMR	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	**HCPL-2430**	Dual Channel, 20 MBd High Common Mode Rejection	Very High Speed Logic Isolation, I/O and Parallel-to-Serial Conversion	40 Mb/s	1000 V/µs @ V_{CM} = 50 V	4.0 mA	2500 Vac/ 1 min. VDE 0883	6-46
	6N137	Optically Coupled Logic Gate	Line Receiver, High Speed Ground Isolation	10 Mb/s	>100 V/µs V_{CM} = 10 V (Typical)	5.0 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) VDE 0883	6-53
	HCPL-2601	High Common Mode Rejection, Optically Coupled Logic Gate	High Speed Logic Ground Isolation	10 Mb/s	1000 V/µs @ V_{CM} = 50 V	5.0 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) VDE 0883	
	HCPL-2611		Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments		5 k V/µs @ V_{CM} = 1000 V			
	HCPL-2602	Optically Coupled Line Receiver	Replace Conventional Line Receivers	10 Mb/s	1000 V/µs @ V_{CM} = 50 V	5.0 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) VDE 0883	6-60
	HCPL-2612		Electrically Noisy Environments		5 K V/µs @ V_{CM} = 1000 V			
	HCPL-2630	Dual Channel Optically Coupled Gate	Line Receiver, High Speed Logic Ground Isolation	10 Mb/s	>100 V/µs V_{CM} = 10 V (Typical)	5.0 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) VDE 0883	6-68

Bold Type – New Product

High-Speed Logic Gate Optocouplers (Continued)

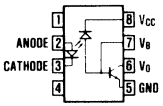
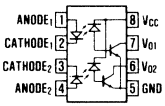
Device		Description	Application	Typical Data Rate [NRZ]	Guaranteed CMR	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	HCPL-2631	Dual Channel, High Common Mode Rejection, Optically Coupled Logic Gate	High Speed Logic Ground Isolation	10 Mb/s	1000 V/µs @ V_{CM} = 50 V	5.0 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. VDE 0883	6-68
	HCPL-4661		Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments		5 K V/µs @ V_{CM} = 1000 V			

Small Outline High-Speed Logic Gate Optocouplers

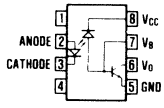
Device		Description	Application	Typical Data Rate [NRZ]	Guaranteed CMR	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	**HCPL-0600**	Small Outline Optically Coupled Logic Gate	Line Receiver, High Speed Ground Isolation	10 Mb/s	> 100 V/µs @ V_{CM} = 10 V (Typical)	5.0 mA	2500 Vac/ 1 min.	6-74
	**HCPL-0601**	Small Outline High CMR, Optically Coupled Logic Gate	High Speed Logic Ground Isolation		1000 V/µs @ V_{CM} = 50 V			
	HCPL-0611		Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments		5 K V/µs @ V_{CM} = 1000 V			

Bold Type – New Product

High-Speed Transistor Output Optocouplers

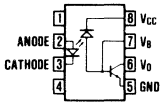
Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	6N135	Transistor Output	Line Receiver, Analog Circuits, TTL/CMOS, TTL/LSTTL Ground Isolation	1 Mb/s	7% Min.	16 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) VDE 0883	6-80
	6N136				19% Min.			
	HCPL-4502	Pin 7 Not Connected						
	HCPL-4503	Pin 7 Not Connected, Very High CMR	Electrically Noisy Environments					
	HCPL-2502				15-22%			
	HCPL-2530	Dual Channel Transistor Output	Line Receiver, Analog Circuits, TTL/CMOS, TTL/LSTTL Ground Isolation	1 Mb/s	7% Min.	16 mA	2500 Vac/ 1 min 5000 Vac/ 1 min (Option 020) VDE 0883	6-87
	HCPL-2531				19% Min.			

Small Outline High-Speed Transistor Output Optocouplers

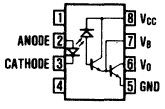
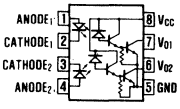
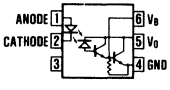
Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	**HCPL-0500**	Small Outline Transistor Output	Line Receiver, Analog Circuits, TTL/CMOS, TTL/LSTTL Ground Isolation	1 Mb/s	7% Min.	16 mA	2500 Vac/ 1 min.	6-93
	HCPL-0501				19% Min.			
	HCPL-0452	Pin 7 Not Connected						
	HCPL-0453	Small Outline Ultra High CMR Transistor Output (Pin 7 Not Connected)	Motor Controls, Switch-mode Power Supplies, Electrically Noisy Environments					

Bold Type – New Product

Widebody High-Speed Transistor Output Optocouplers

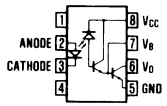
Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Voltage/ Regulatory Approval	Page No.
	CNW135	Transistor Output Widebody (4e pitch) Package	High Voltage Insulation Line Receiver Feedback Element in Switch-mode Power Supplies	1 Mb/s	7% Min.	16 mA	5000 Vac/ 1 min. UL 1577 VDE 0804, 0805, 0806, 0883, 0884, 0860, 0750 IEC 65, 380, 950, 335, 435, 601 BSI 415, 7002	6-100
	CNW136				19% Min.			

High Gain Optocouplers

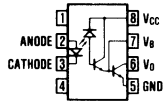
Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	6N138	Low Saturation Voltage, High Gain Output, V_{CC} = 7 V Max.	Line Receiver, Low Current Ground Isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL	100 kb/s	300% Min.	1.6 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) VDE 0883	6-107
	6N139	Low Saturation Voltage, High Gain Output, V_{CC} = 18 V Max.	Line Receiver, Ultra Low Current Ground Isolation, CMOS/ LSTTL, CMOS/TTL, CMOS/CMOS		400% Min.	0.5 mA		
	HCPL-2730	Dual Channel, High Gain, V_{CC} = 7 V Max.	Line Receiver, Polarity Sensing, Low Current Ground Isolation	100 kb/s	300% Min.	1.6 mA	2500 Vac/ 1 min. 5000 Vac/ 1 min. (Option 020) VDE 0883	6-112
	HCPL-2731	Dual Channel, High Gain, V_{CC} = 18 V Max.			400% Min.	0.5 mA		
	4N45	Darlington Output V_{CC} = 7 V Max.	AC Isolation, Relay-Logic Isolation	3 kb/s	250% Min.	1.0 mA		6-117
	4N46	Darlington Output, V_{CC} = 20 V Max.			350% Min.	0.5 mA		

Bold Type – New Product

Small Outline High Gain Optocouplers

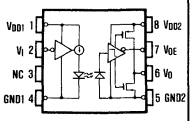
Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	**HCPL-0700**	Small Outline Low Saturation Voltage, High Gain Output, V_{CC} = 7 V Max.	Line Receiver, Low Current Ground Isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL	100 kb/s	300% Min.	1.6 mA	2500 Vac/ 1 min	6-122
	HCPL-0701	Small Outline Low Saturation Voltage, High Gain Output, V_{CC} = 18 V Max.	Line Receiver, Ultra Low Current Ground Isolation, CMOS/LSTTL, CMOS/TTL, CMOS/CMOS		400% Min.	0.5 mA		

Widebody High Gain Optocouplers

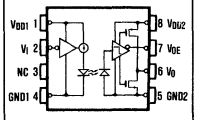
Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	**CNW138**	Low Saturation Voltage, High Gain Output, V_{CC} = 7 V Max. Widebody (4e pitch) Package	Line Receiver, Low Current Ground Isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL	100 kb/s	300% Min.	1.6 mA	5000 Vac/ 1 min UL 1577 VDE 0804, 0805, 0806, 0883, 0884, 0860, 0750 IEC 65, 380, 950, 335, 435, 601 BSI 415, 7002	6-128
	CNW139	Low Saturation Voltage, High Gain Output, V_{CC} = 18 V Max. Widebody (4e pitch) Package	Line Receiver, Ultra Low Current Ground Isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL		400% Min.	0.5 mA		

Bold Type – New Product

High-Speed CMOS Optocoupler

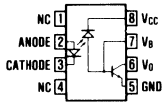
Device		Description	Application	Data Rate [NRZ]	Guaran-teed CMR	Total Power Supply Current	Withstand Voltage/ Regulatory Approval	Page No.
	**HCPL-7100**	High-Speed, Low Power 3 State Output CMOS IC Technology	Computer-Peripheral Interface Digital Isolation for A/D, D/A Converters, Motor Control, Power Inverter, +5 V Compatibility CMOS and TTL Logic	15 MBd	1000 V/μs @ 50 V V_{CM}	10 mA (Typical)	2500 Vac/ 1 min UL 1577 VDE 0700, 0804, 0884, 0160	6-135

Ultra High-Speed CMOS Optocoupler

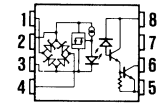
Device		Description	Application	Data Rate [NRZ]	Guaran-teed CMR	Total Power Supply Current	Withstand Voltage/ Regulatory Approval	Page No.
	**HCPL-7101**	High-Speed, Low Power 3 State Output CMOS IC Technology	Computer-Peripheral Interface Digital Isolation for A/D, D/A Converters, Motor Control, Power Inverter, +5 V Compatibility CMOS and TTL Logic	50 MBd	2000 V/μs @ 200 V V_{CM}	10 mA (Typical)	2500 Vac/ 1 min UL 1577 VDE 0804, 0884, 0160	6-147

Bold Type – New Product

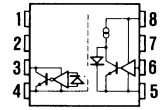
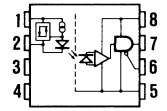
Wideband Analog/Video Optocoupler

Device		Description	Application	Typical Bandwidth	Differential Gain	Linearity	Withstand Test Voltage/ Regulatory Approval	Page No.
	HCPL-4562	Wideband Analog/ Video Optocoupler	Video Isolation, Feedback Element in Switch-mode Power Supplies	17 MHz	±1%	0.25%	2500 Vac/ 1 min 5000 Vac/ 1 min (option 020)	6-159

AC/DC to Logic Interface Optocouplers

Device		Description	Application	Operating Frequency	Input Threshold Current	Output Current	Withstand Test Voltage/ Regulatory Approval	Page No.
	HCPL-3700	AC/DC to Logic Threshold Sensing Interface Optocoupler	Limit Switch Sensing, Low Voltage Detector, Relay Contact Monitor	4 KHz	2.5 mA TH^+ 1.3 mA TH^-	4.2 mA	2500 Vac/ 1 min 5000 Vac/ 1 min (Option 020) VDE 0883	6-165
	HCPL-3760	Low Input Current			1.2 mA TH^+ 0.6 mA TH^-			

20 mA Current Loop Optocouplers

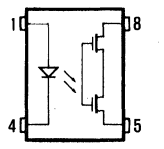
Device		Description	Application	Typical Data Rates	Input Characteristics	Output Characteristics	Withstand Test Voltage/ Regulatory Approval	Page No.
	HCPL-4100	Optically Coupled 20 mA Current Loop Transmitter	Isolated 20 mA Current Loop in: • Computer Peripherals • Industrial Control Equipment • Data Communication Equipment	20 kBd (at 400 metres)	TTL/CMOS	27 V Max. Compliance Voltage	2500 Vac/ 1 min	6-175
	HCPL-4200	Optically Coupled 20 mA Current Loop Receiver			6.5 mA Typ. Threshold Current	3 State Output	2500 Vac/ 1 min	6-183

Bold Type – New Product

Optocoupler Options

Option	Description	Page
020	Special construction and testing to ensure the capability to withstand 5000 V ac input to output for one minute. Testing is recognized by Underwriters Laboratories, Inc. (File No. E55361). This specification is required by U.L. in some applications where working voltages can exceed 220 V ac.	6-191
100	Surface mountable optocoupler in a standard sized dual-in-line package with leads trimmed (butt joint). Provides an optocoupler which is compatible with surface mounting processes.	6-193
300	Surface mountable optocoupler in a standard sized dual-in-line package with gull wing leads. Provides an optocoupler which is compatible with surface mounting processes.	

Plastic Solid State Relay

Device		Application	Output Withstand Voltage	Output On-Resistance	Maximum Load Current	Maximum Off-State Leakage	Input/ Output Insulation	Page No.
	**HSSR-8200**	Data Acquisition, Test & Measurement, Analog Multiplexers, & Reed Relay Replacement	200 V	160 Ω	40 mA	0.25 nA	3 kV dc	6-195

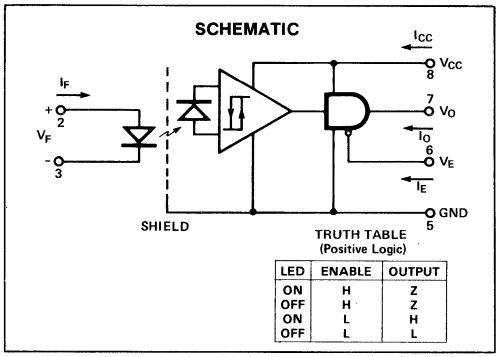
Bold Type – New Product

Hermetic Optocouplers Selection Guide (see pg. 6-214).

HEWLETT PACKARD

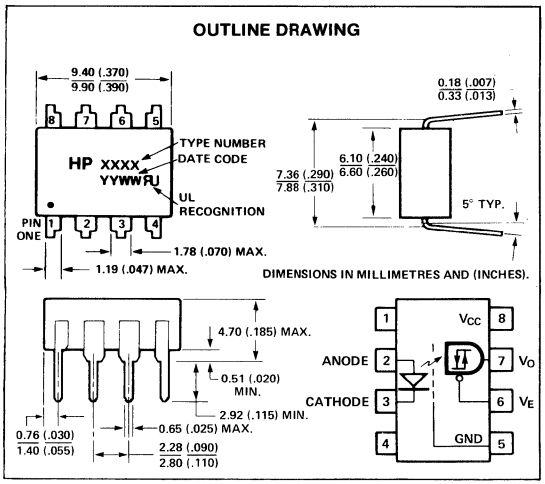
LOW INPUT CURRENT LOGIC GATE OPTOCOUPLER

HCPL-2200
HCPL-2219



TRUTH TABLE
(Positive Logic)

LED	ENABLE	OUTPUT
ON	H	Z
OFF	H	Z
ON	L	H
OFF	L	L



Features

- **VERY HIGH COMMON MODE REJECTION 2.5 KV/μs AT 400 V V_{CM} GUARANTEED (HCPL-2219)**
- **COMPATIBLE WITH LSTTL, TTL, AND CMOS LOGIC**
- **WIDE V_{CC} RANGE (4.5 TO 20 VOLTS)**
- **2.5 MBAUD GUARANTEED OVER TEMPERATURE**
- **LOW INPUT CURRENT (1.6 mA)**
- **THREE STATE OUTPUT (NO PULLUP RESISTOR REQUIRED)**
- **GUARANTEED PERFORMANCE FROM 0° C TO +85° C**
- **INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **VDE 0883 APPROVAL AVAILABLE**
- **MIL-STD-1772 VERSION AVAILABLE (HCPL-5200/1)**

Applications

- **Isolation of High Speed Logic Systems**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **Isolated Buss Driver**
- **High Speed Line Receiver**

Description

The HCPL-2200 is an optically coupled logic gate that combines a GaAsP LED and an integrated high gain photon detector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data busses. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1,000 volts/μsec. Higher CMR specifications are available upon request.

The Electrical and Switching Characteristics of the HCPL-2200 are guaranteed over the temperature range of 0° C to 85° C. The HCPL-2200 is guaranteed to operate over a V_{CC} range of 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic. Low I_F and low I_{CC} result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a typical propagation delay of 160 nsec.

The HCPL-2200 is useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Enable Voltage High	V_{EH}	2.0	20	Volts
Enable Voltage Low	V_{EL}	0	0.8	Volts
Forward Input Current	$I_{F(ON)}$	1.6*	5	mA
Forward Input Current	$I_{F(OFF)}$	—	0.1	mA
Operating Temperature	T_A	0	85[1]	°C
Fan Out	N		4	TTL Loads

*The initial switching threshold is 1.6 mA or less. It is recommended that 2.2 mA be used to permit at least a 20% CTR degradation guardband.

OPTOCOUPLERS

Recommended Circuit Design

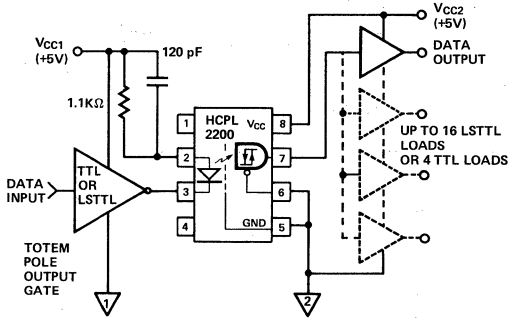


Figure 1. Recommended LSTTL to LSTTL Circuit

Absolute Maximum Ratings

(No Derating Required up to 70° C)

Storage Temperature ..... -55° C to +125° C
Operating Temperature ..... -40° C to +85° C[1]
Lead Solder Temperature ..... 260° C for 10 s
(1.6 mm below seating plane)
Average Forward Input Current — I_F ..... 10 mA
Peak Transient Input Current — I_F 1A
(≤1 μs Pulse Width, 300 pps)
Reverse Input Voltage 5V
Supply Voltage — V_{CC} ..... 0.0V min., 20V max.
Three State Enable Voltage
— V_E ..... -0.5V min., 20V max.
Output Voltage — V_O ..... -0.5V min., 20V max.
Total Package Power
Dissipation — P ..... 210 mW[1]
Average Output Current — I_O ..... 25 mA

Electrical Specifications

For 0°C ≤ T_A[1] ≤ 85°C, 4.5 V ≤ V_{CC} ≤ 20 V, 1.6 mA ≤ $I_{F(ON)}$ ≤ 5 mA, 2.0 V ≤ V_{EH} ≤ 20 V, 0.0 V ≤ V_{EL} ≤ 0.8 V, 0 mA ≤ $I_{F(OFF)}$ ≤ 0.1 mA. All Typicals at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 3 mA unless otherwise specified. See note 7.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads)		2	
Logic High Output Voltage	V_{OH}	2.4	*		Volts	I_{OH} = -2.6 mA	*V_{OH} = V_{CC} - 2.1V	3	
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	μA	V_O = 5.5V	I_F = 5 mA		
				500	μA	V_O = 20V	V_{CC} = 4.5V		
Logic High Enable Voltage	V_{EH}	2.0			Volts				
Logic Low Enable Voltage	V_{EL}			0.8	Volts				
Logic High Enable Current	I_{EH}			20	μA	V_{EN} = 2.7V			
				100	μA	V_{EN} = 5.5V			
			.004	250	μA	V_{EN} = 20V			
Logic Low Enable Current	I_{EL}			-0.32	mA	V_{EN} = 0.4V			
Logic Low Supply Current	I_{CCL}		4.5	6.0	mA	V_{CC} = 5.5V	I_F = 0 mA		
			5.25	7.5	mA	V_{CC} = 20V	V_E = Don't Care		
Logic High Supply Current	I_{CCH}		2.7	4.5	mA	V_{CC} = 5.5V	I_F = 5 mA,		
			3.1	6.0	mA	V_{CC} = 20V	V_E = Don't Care		
High Impedance State Output Current	I_{OZL}			-20	μA	V_O = 0.4V	V_{EN} = 2V, I_F = 5 mA		
	I_{OZH}			20	μA	V_O = 2.4V	V_{EN} = 2V, I_F = 0		
				100	μA	V_O = 5.5V			
				500	μA	V_O = 20V			
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	V_O = V_{CC} = 5.5V	I_F = 0 mA		2
		40			mA	V_O = V_{CC} = 20V			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5V	I_F = 5 mA, V_O = GND		2
		-25			mA	V_{CC} = 20V			
Input Current Hysteresis	I_{HYS}		0.12		mA	V_{CC} = 5V		4	
Input Forward Voltage	V_F		1.5	1.7	Volts	T_A = 25°C	I_F = 5 mA	5	
				1.75					
Input Reverse Breakdown Voltage	BV_R	5			Volts	I_R = 10 μA			
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.7		mV/° C	I_F = 5 mA			
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C		12	6
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 VDC			3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 VDC			3
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0V, Pins 2 and 3			

Switching Specifications

For $0°C \le T_A^{[1]} \le 85°C$, $4.5V \le V_{CC} \le 20V$, $1.6\ mA \le I_{F(ON)} \le 5\ mA$, $0.0\ mA \le I_{F(OFF)} \le 0.1\ mA$. All Typicals at $T_A = 25°C$, $V_{CC} = 5V$, $I_{F(ON)} = 3\ mA$ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		210		ns	Without Peaking Capacitor	6,7	4,5
			160	300		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		170		ns	Without Peaking Capacitor	6,7	4,5
			115	300		With Peaking Capacitor		
Output Enable Time to Logic High	t_{PZH}		25		ns		8,10	
Output Enable Time to Logic Low	t_{PZL}		28		ns		8,9	
Output Disable Time from Logic High	t_{PHZ}		105		ns		8,10	
Output Disable Time from Logic Low	t_{PLZ}		60		ns		8,9	
Output Rise Time (10-90%)	t_r		55		ns		6,11	
Output Fall Time (90-10%)	t_f		15		ns		6,11	

Parameter	Symbol	Device	Min.	Units	Test Conditions		Figure	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	HCPL-2200	1,000	V/μs	$\|Vcm\| = 50\ V$	$I_F = 1.6\ mA$, $V_{CC} = 5\ V$, $T_A = 25°C$	12	6
		HCPL-2219	2,500	V/μs	$\|Vcm\| = 400\ V$			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	HCPL-2200	1,000	V/μs	$\|Vcm\| = 50\ V$	$V_F = 0\ V$, $V_{CC} = 5\ V$, $T_A = 25°C$	12	6
		HCPL-2219	2,500	V/μs	$\|Vcm\| = 400\ V$			

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

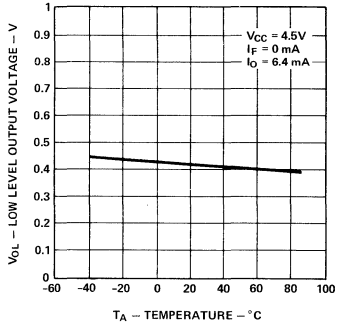


Figure 2. Typical Logic Low Output Voltage vs. Temperature

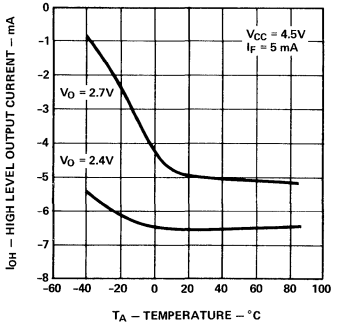


Figure 3. Typical Logic High Output Current vs. Temperature

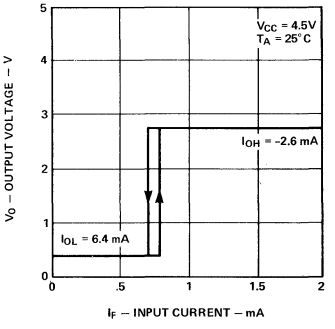


Figure 4. Output Voltage vs. Forward Input Current

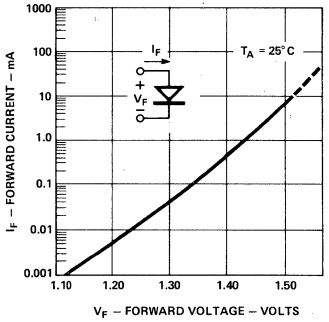


Figure 5. Typical Input Diode Forward Characteristic

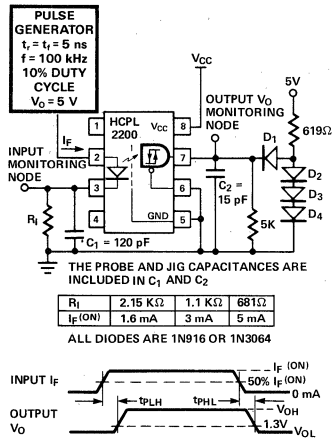


Figure 6. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

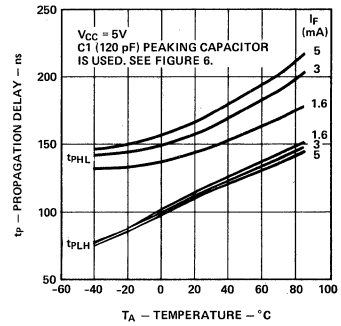


Figure 7. Typical Propagation Delays vs. Temperature

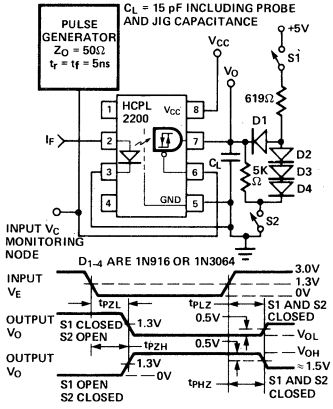


Figure 8. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}

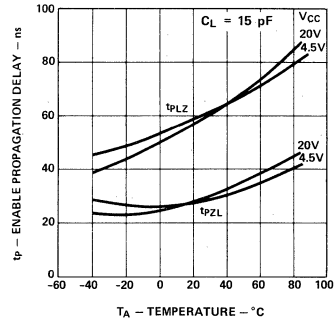


Figure 9. Typical Logic Low Enable Propagation Delay vs. Temperature

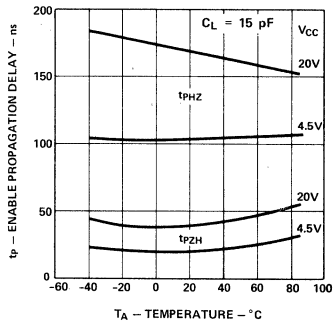


Figure 10. Typical Logic High Enable Propagation Delay vs. Temperature

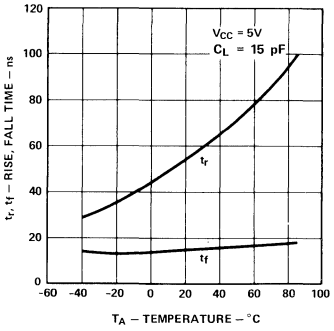


Figure 11. Typical Rise, Fall Time vs. Temperature

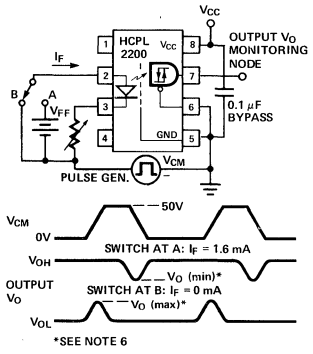


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

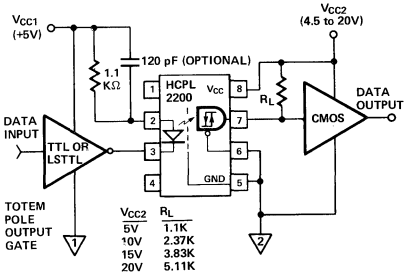


Figure 13. LSTTL to CMOS Interface Circuit

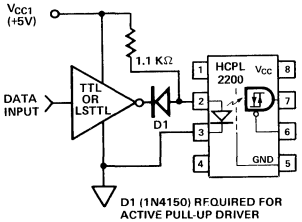


Figure 14. Recommended LED Drive Circuit

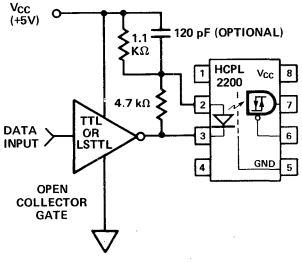


Figure 15. Series LED Drive with Open Collector Gate (4.7 kΩ Resistor Shunts I_{OH} from the LED)

The 120 pF capacitor may be omitted in applications where 500 ns propagation delay is sufficient.

Notes:

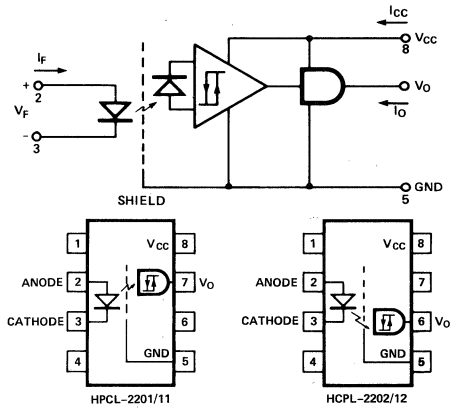
1. Derate total package power dissipation, P, linearly above 70° C free air temperature at a rate of 4.5 mW/° C.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.
5. When the peaking capacitor is omitted, propagation delay times may increase by 100 ns.
6. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0V).
7. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.

HEWLETT PACKARD

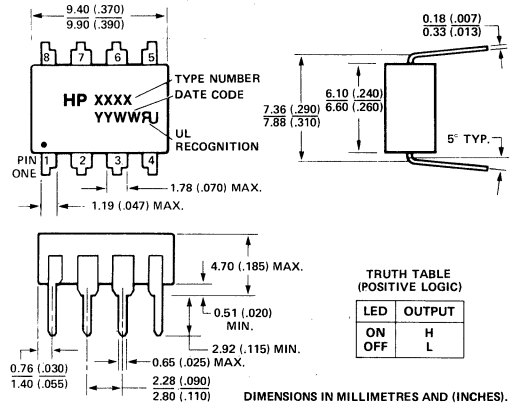
VERY HIGH CMR, WIDE V_{CC} LOGIC GATE OPTOCOUPLER

HCPL-2201
HCPL-2202
HCPL-2211
HCPL-2212

SCHEMATIC



OUTLINE DRAWING



TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	H
OFF	L

DIMENSIONS IN MILLIMETRES AND (INCHES).

Features

- **VERY HIGH COMMON MODE REJECTION, 5 kV/μs AT 300 V GUARANTEED (HCPL-2211/12)**
- **WIDE V_{CC} RANGE (4.5 TO 20 VOLTS)**
- **300 ns PROPAGATION DELAY GUARANTEED OVER THE FULL TEMPERATURE RANGE**
- **5 MBd TYPICAL SIGNAL RATE**
- **LOW INPUT CURRENT (1.6 mA)**
- **TOTEM POLE OUTPUT (NO PULLUP RESISTOR REQUIRED)**
- **GUARANTEED PERFORMANCE FROM -40°C TO +85°C**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **VDE 0883 APPROVAL PENDING**

Applications

- **ISOLATION OF HIGH SPEED LOGIC SYSTEMS**
- **COMPUTER-PERIPHERAL INTERFACES**
- **MICROPROCESSOR SYSTEM INTERFACES**
- **GROUND LOOP ELIMINATION**
- **PULSE TRANSFORMER REPLACEMENT**
- **HIGH SPEED LINE RECEIVER**

Description

The HCPL-2201/02/11/12 are single-channel, optically-coupled logic gates. The detectors have totem pole output stages and optical receiver input stages with built-in Schmitt triggers to provide logic-compatible waveforms, eliminating the need for additional waveshaping.

A superior internal shield on the HCPL-2211/12 guarantees common mode transient immunity of 5,000 V/μs at a common mode voltage of 300 volts.

The electrical and switching characteristics of the HCPL-2201/02/11/12 are guaranteed from -40°C to +85°C and a V_{CC} from 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed couplers. Logic signals are transmitted with a typical propagation delay of 150 ns.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Forward Input Current	$I_{F(ON)}$	1.6*	5	mA
Forward Input Voltage	$V_{F(OFF)}$	—	0.8	Volts
Operating Temperature	T_A	-40	85	°C
Fan Out	N		4	TTL Loads

*The initial switching threshold is 1.6 mA or less. It is recommended that 2.2 mA be used to permit at least a 20% CTR degradation guardband.

Recommended Circuit Design

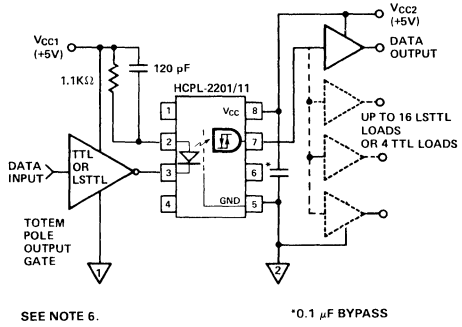


Figure 1. Recommended LSTTL to LSTTL Circuit

Absolute Maximum Ratings

(No Derating Required up to 70°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Forward Input Current — I_F ..... 10 mA
Peak Transient Input Current — I_F ..... 1 A
(≤1 μs Pulse Width, 300 pps)
Reverse Input Voltage ..... 5 V
Supply Voltage — V_{CC} ..... 0.0 V min., 20 V max.
Output Voltage — V_O ..... -0.5 V min., 20 V max.
Total Package Power Dissipation — P ..... 210 mW[1]
Average Output Current — I_O ..... 25 mA

Electrical Specifications

-40°C ≤ T_A ≤ 85°C, 4.5 V ≤ V_{CC} ≤ 20 V, 1.6 mA ≤ $I_{F(ON)}$ ≤ 5 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, unless otherwise specified.
All Typicals at T_A = 25°C. See Note 7.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads)		2, 4	
Logic High Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -2.6 mA	V_{CC} = 4.5 V	3, 4, 8	
		2.7				I_{OH} = -0.4 mA			
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	μA	V_O = 5.5 V	I_F = 5 mA, V_{CC} = 4.5 V		
				500	μA	V_O = 20 V			
Logic Low Supply Current	I_{CCL}		3.7	6.0	mA	V_{CC} = 5.5 V	V_F = 0 V		
			4.3	7.0	mA	V_{CC} = 20 V			
Logic High Supply Current	I_{CCH}		2.4	4.0	mA	V_{CC} = 5.5 V	I_F = 5 mA		
			2.7	5.0	mA	V_{CC} = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	15			mA	V_O = V_{CC} = 5.5 V	V_F = 0 V		2
		20			mA	V_O = V_{CC} = 20 V			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5 V	I_F = 5 mA, V_O = GND		2
		-20			mA	V_{CC} = 20 V			
Input Forward Voltage	V_F		1.5	1.7 / 1.85	Volts	T_A = 25°C	I_F = 5 mA	5	
Input Reverse Breakdown Voltage	BV_R	5			Volts	I_R = 10 μA			
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.7		mV/°C	I_F = 5 mA			
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%; t = 1 min., T_A = 25°C			3
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 VDC			3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 VDC			3
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V, Pins 2 and 3			

Switching Specifications

$-40°C \le T_A \le 85°C$, $4.5\ V \le V_{CC} \le 20\ V$, $1.6\ mA \le I_{F(ON)} \le 5\ mA$, $0\ V \le V_{F(OFF)} \le 0.8\ V$. All Typicals at $T_A = 25°C$, $V_{CC} = 5\ V$, $I_{F(ON)} = 3\ mA$ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		150		ns	Without Peaking Capacitor	6, 7	4
			150	300		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		110		ns	Without Peaking Capacitor	6, 7	4
			90	300		With Peaking Capacitor		
Output Rise Time (10-90%)	t_r		30		ns		6, 9	
Output Fall Time (90-10%)	t_f		7		ns		6, 9	

Parameter	Symbol	Device	Min.	Units	Test Conditions		Figure	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	HCPL-2201 HCPL-2202	1,000	V/μs	$\|Vcm\| = 50\ V$	$I_F = 1.6\ mA$, $V_{CC} = 5\ V$, $T_A = 25°C$	10	5
		HCPL-2211 HCPL-2212	5,000	V/μs	$\|Vcm\| = 300\ V$			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	HCPL-2201 HCPL-2202	1,000	V/μs	$\|Vcm\| = 50\ V$	$V_F = 0\ V$, $V_{CC} = 5\ V$, $T_A = 25°C$	10	5
		HCPL-2211 HCPL-2212	5,000	V/μs	$\|Vcm\| = 300\ V$			

Insulation Related Specifications

Parameter	Symbol	Min.	Units	Conditions
Min. External Air Gap (Clearance)	L (IO1)	≥ 7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L (IO2)	≥ 7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

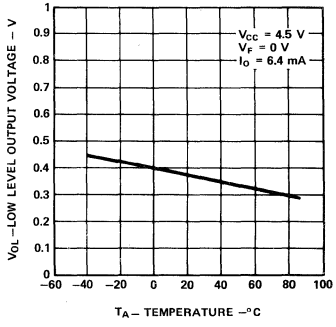


Figure 2. Typical Logic Low Output Voltage vs. Temperature

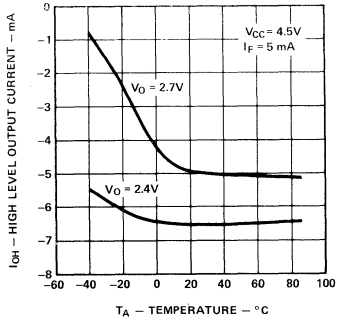


Figure 3. Typical Logic High Output Current vs. Temperature

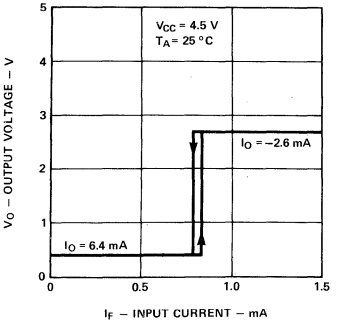


Figure 4. Output Voltage vs. Forward Input Current

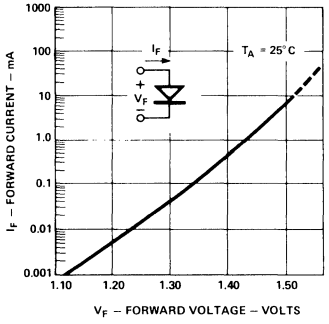
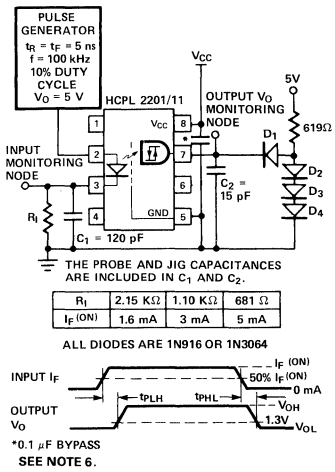


Figure 5. Typical Input Diode Forward Characteristic



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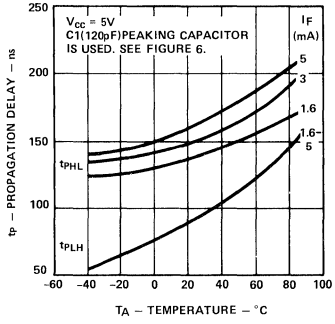

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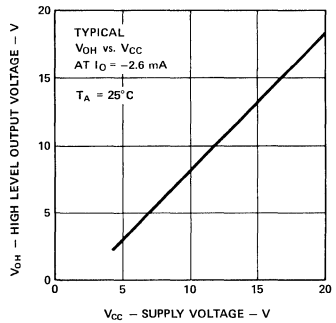
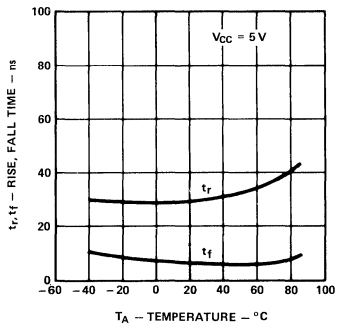


Figure 8. Typical Logic High Output Voltage vs. Supply Voltage



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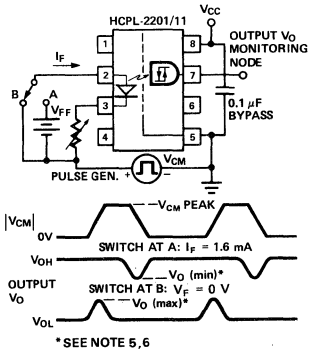

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OPTOCOUPLERS

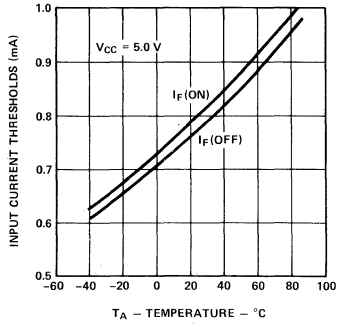
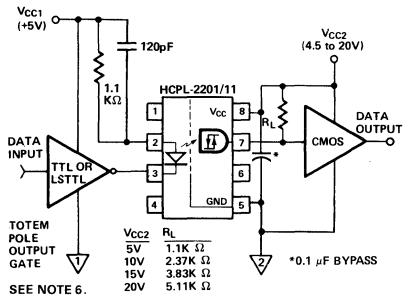


Figure 11. Typical Input Threshold Current vs. Temperature



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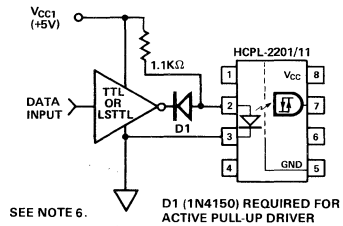


Figure 13. Alternative LED Drive Circuit

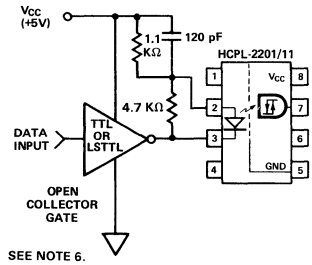


Figure 14. Series LED Drive with Open Collector Gate (4.7 kΩ Resistor Shunts I_{OH} from the LED)

Notes:

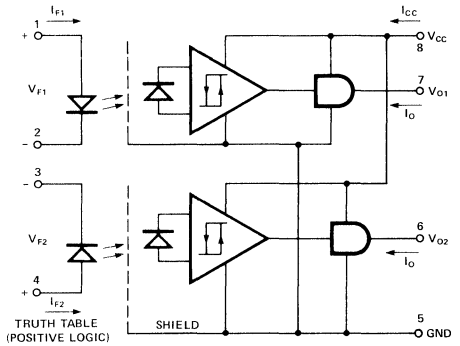
1. Derate total package power dissipation, P, linearly above 70°C free air temperature at a rate of 4.5 mW/°C.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
5. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state. V_O < 0.8 V. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state V_O > 2.0 V.
6. For HCPL-2202/12, V_O is on pin 6.
7. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.

HEWLETT PACKARD

VERY HIGH CMR, WIDE V_{CC} DUAL LOGIC GATE OPTOCOUPLER

HCPL-2231
HCPL-2232

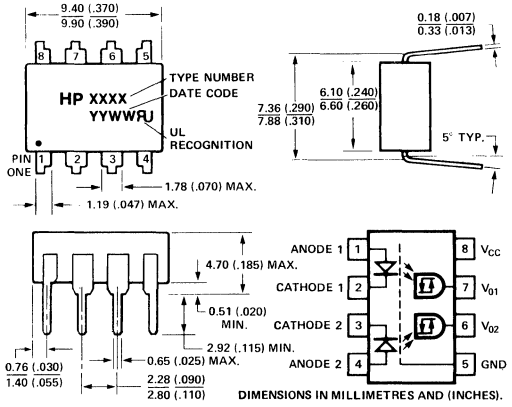
SCHEMATIC



TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	H
OFF	L

OUTLINE DRAWING



Features

- **VERY HIGH COMMON MODE REJECTION 5 kV/μs AT 300 V GUARANTEED (HCPL-2232)**
- **WIDE V_{CC} RANGE (4.5 TO 20 VOLTS)**
- **300 ns PROPAGATION DELAY GUARANTEED OVER THE FULL TEMPERATURE RANGE**
- **5 MBd TYPICAL SIGNAL RATE**
- **LOW INPUT CURRENT (1.8 mA)**
- **TOTEM POLE OUTPUT (NO PULLUP RESISTOR REQUIRED)**
- **GUARANTEED PERFORMANCE FROM -40°C TO +85°C**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **VDE 0883 APPROVAL AVAILABLE**
- **MIL-STD-1772 VERSION AVAILABLE (HCPL-5230/1)**

Applications

- **ISOLATION OF HIGH SPEED LOGIC SYSTEMS**
- **COMPUTER-PERIPHERAL INTERFACES**
- **MICROPROCESSOR SYSTEM INTERFACES**
- **GROUND LOOP ELIMINATION**
- **PULSE TRANSFORMER REPLACEMENT**
- **HIGH SPEED LINE RECEIVER**

Description

The HCPL-2231/2 are dual-channel, optically-coupled logic gates. The detectors have totem pole output stages and optical receiver input stages with built-in Schmitt triggers to provide logic compatible waveforms, eliminating the need for additional waveshaping.

A superior internal shield on the HCPL-2232 guarantees common mode transient immunity of 5,000 V/μs at a common mode voltage of 300 volts.

The electrical and switching characteristics of the HCPL-2231/2 are guaranteed from -40°C to +85°C and a V_{CC} from 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed couplers. Logic signals are transmitted with a typical propagation delay of 150 ns.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Input Current (High)	$I_{F(ON)}$	1.8*	5	mA
Input Voltage (Low)	$V_{F(OFF)}$	—	0.8	Volts
Operating Temperature	T_A	-40	85	°C
Fan Out per Channel	N		4	TTL Loads

*The initial switching threshold is 1.8 mA or less. It is recommended that 2.5 mA be used to permit at least a 20% CTR degradation guardband.

OPTOCOUPLERS

Recommended Circuit Design

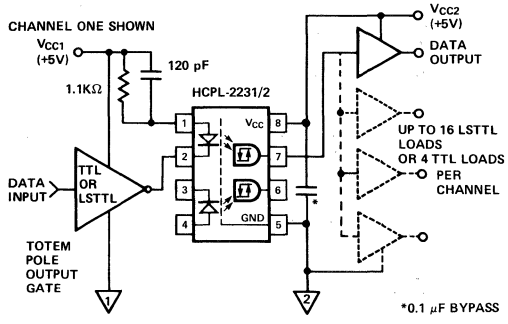


Figure 1. Recommended LSTTL to LSTTL Circuit

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Forward Input Current — I_F ..... 10 mA[1]
Peak Transient Input Current — I_F ..... 1 A[1]
(≤1 μs Pulse Width, 300 pps)
Reverse Input Voltage ..... 5 V[1]
Supply Voltage — V_{CC} ..... 0.0 V min., 20 V max.
Output Voltage — V_O ..... -0.5 V min., 20 V max.[1]
Total Package Power Dissipation ..... 294 mW
Output Power Dissipation — P_O per Channel ..... Fig. 8
Average Output Current — I_O per Channel ..... 25 mA

Electrical Specifications

-40°C ≤ T_A ≤ 85°C, 4.5 V ≤ V_{CC} ≤ 20 V, 1.8 mA ≤ $I_{F(ON)}$ ≤ 5 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, unless otherwise specified.
All Typicals at T_A = 25°C. See note 7.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads)		2, 4	1
Logic High Output Voltage	V_{OH}	2.4 2.7			Volts	I_{OH} = -2.6 mA I_{OH} = -0.4 mA	V_{CC} = 4.5 V	3, 4, 9	1
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	μA	V_O = 5.5 V	I_F = 5 mA V_{CC} = 4.5 V		1
				500	μA	V_O = 20 V			
Logic Low Supply Current	I_{CCL}		7.4	12.0	mA	V_{CC} = 5.5 V	V_F = 0 V		
			8.6	14.0	mA	V_{CC} = 20 V			
Logic High Supply Current	I_{CCH}		4.8	8.0	mA	V_{CC} = 5.5 V	I_F = 5 mA		
			5.4	10.0	mA	V_{CC} = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	15			mA	V_O = V_{CC} = 5.5 V	V_F = 0 V		1, 2
		20			mA	V_O = V_{CC} = 20 V			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5 V	I_F = 5 mA V_O = GND		1, 2
		-20			mA	V_{CC} = 20 V			
Input Forward Voltage	V_F		1.5	1.7 1.85	Volts	T_A = 25°C	I_F = 5 mA	5	1
Input Reverse Breakdown Voltage	BV_R	5			Volts	I_R = 10 μA			1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.7		mV/°C	I_F = 5 mA			
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C			3
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 VDC			3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 VDC			3
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V			1
Input-Input Insulation Leakage Current	I_{I-I}		0.005		μA	Relative Humidity = 45% t = 5 s, V_{I-I} = 500 V			6
Resistance (Input-Input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500 V			6
Capacitance (Input-Input)	C_{I-I}		0.25		pF	f = 1 MHz			6

Switching Specifications

$-40°C \le T_A \le 85°C$, $4.5\ V \le V_{CC} \le 20\ V$, $1.8\ mA \le I_{F\ (ON)} \le 5\ mA$, $0\ V \le V_{F\ (OFF)} \le 0.8\ V$. All Typicals at $T_A = 25°C$, $V_{CC} = 5\ V$, $I_{F\ (ON)} = 3\ mA$ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		150		ns	Without Peaking Capacitor	6, 7	1, 4
			150	300		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		110		ns	Without Peaking Capacitor	6, 7	1, 4
			90	300		With Peaking Capacitor		
Output Rise Time (10-90%)	t_r		30		ns		6, 10	1
Output Fall Time (90-10%)	t_f		7		ns		6, 10	1

Parameter	Symbol	Device	Min.	Units	Test Conditions		Figure	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	HCPL-2231	1,000	V/μs	$\|Vcm\| = 50\ V$	$I_F = 1.8\ mA$, $V_{CC} = 5\ V$, $T_A = 25°C$	11	1, 5
		HCPL-2232	5,000	V/μs	$\|Vcm\| = 300\ V$			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	HCPL-2231	1,000	V/μs	$\|Vcm\| = 50\ V$	$V_F = 0\ V$, $V_{CC} = 5\ V$, $T_A = 25°C$	11	1, 5
		HCPL-2232	5,000	V/μs	$\|Vcm\| = 300\ V$			

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

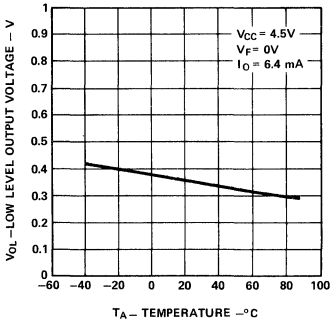


Figure 2. Typical Logic Low Output Voltage vs. Temperature

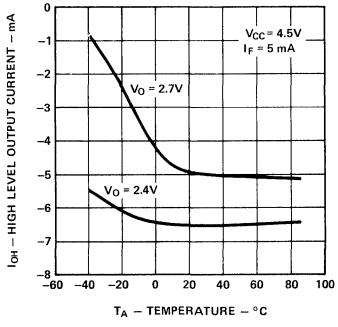


Figure 3. Typical Logic High Output Current vs. Temperature

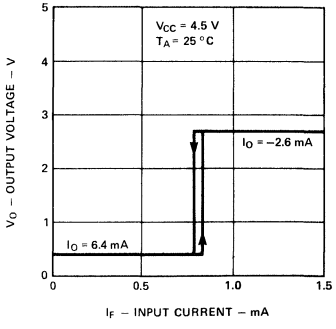


Figure 4. Output Voltage vs. Forward Input Current

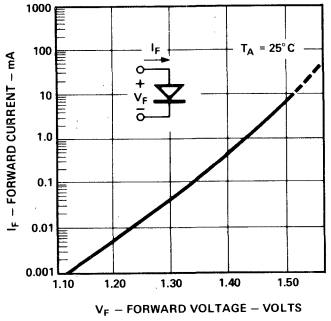
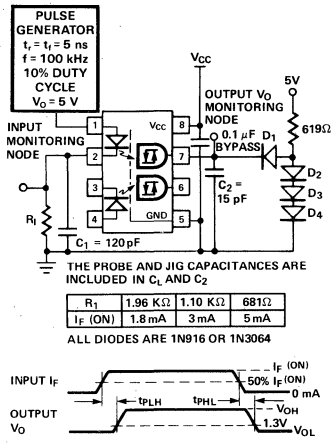


Figure 5. Typical Input Diode Forward Characteristic



Note: Channel one shown.

Figure 6. Circuit for t_{PLH}, t_{PHL}, t_r, t_f

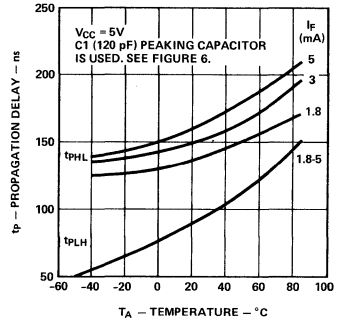


Figure 7. Typical Propagation Delays vs. Temperature

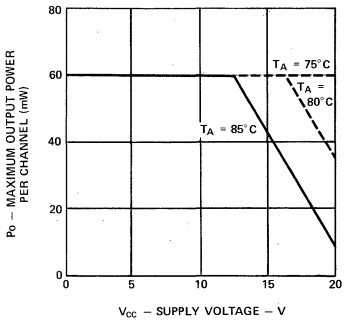


Figure 8. Maximum Output Power per Channel vs. Supply Voltage

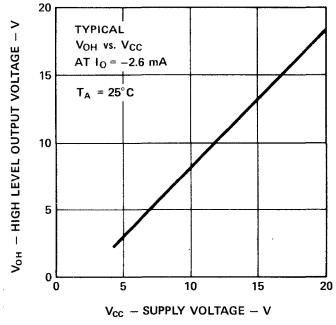


Figure 9. Typical Logic High Output Voltage vs. Supply Voltage

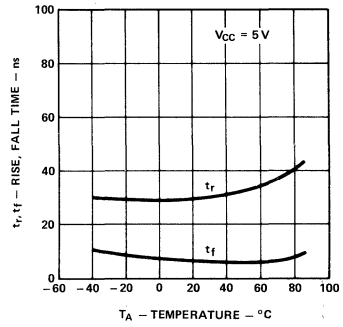


Figure 10. Typical Rise, Fall Time vs. Temperature

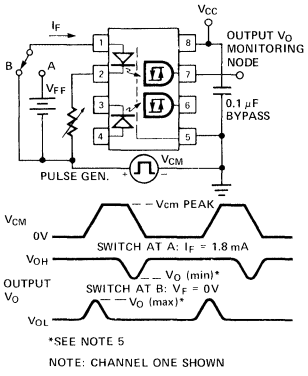


Figure 11. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

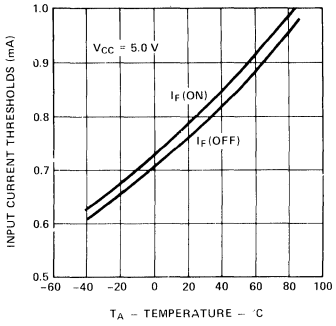


Figure 12. Typical Input Threshold Current vs. Temperature

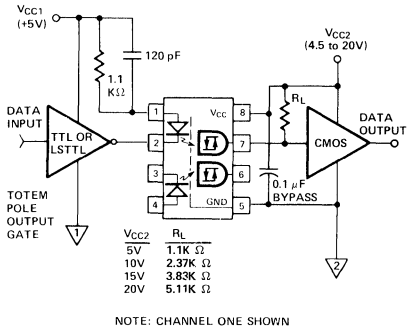


Figure 13. LSTTL to CMOS Interface Circuit

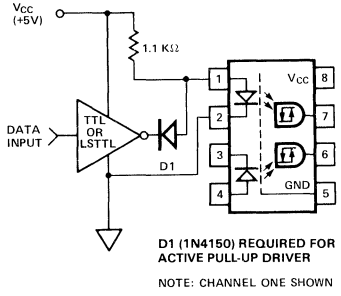


Figure 14. Alternate LED Drive Circuit

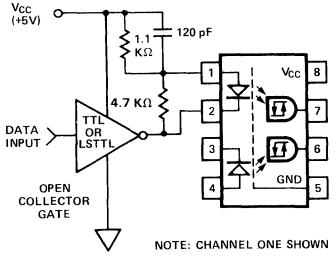


Figure 15. Series LED Drive with Open Collector Gate (4.7 kΩ Resistor Shunts I_{OH} from the LED)

Notes:

1. Each channel.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
5. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state. V_O < 0.8 V. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state V_O > 2.0 V.
6. Measured between pins 1 and 2, shorted together, and pins 3 and 4, shorted together.
7. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.

HEWLETT PACKARD

LOW INPUT CURRENT HIGH SPEED OPTOCOUPLER

HCPL-2300

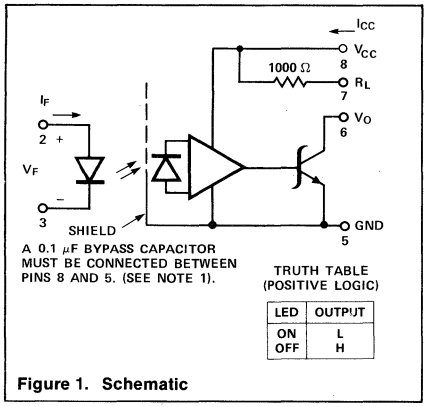
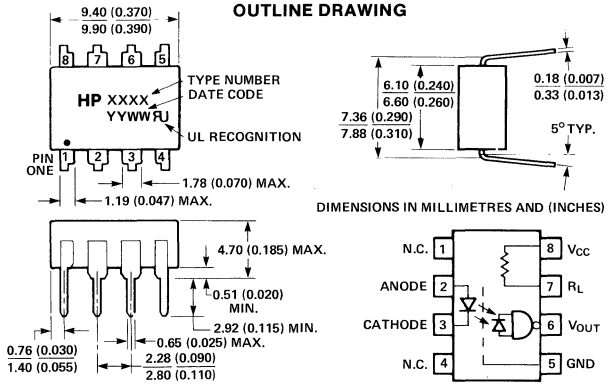


Figure 1. Schematic



Features

- **GUARANTEED LOW THRESHOLDS: I_F = 0.5 mA, $V_F \leq$ 1.5 V**
- **HIGH SPEED: GUARANTEED 5 MBd OVER TEMPERATURE**
- **VERSATILE: COMPATIBLE WITH TTL, LSTTL AND CMOS**
- **MORE EFFICIENT 820 nm AlGaAs LED**
- **INTERNAL SHIELD FOR GUARANTEED COMMON MODE REJECTION**
- **SCHOTTKY CLAMPED, OPEN COLLECTOR OUTPUT WITH OPTIONAL INTEGRATED PULL-UP RESISTOR**
- **STATIC AND DYNAMIC PERFORMANCE GUARANTEED FROM -40°C TO 85°C**
- **SPECIAL SELECTION FOR LOW FORWARD CURRENT APPLICATIONS ($I_F \geq$ 150 μA)**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **VDE 0883 APPROVAL AVAILABLE**

Applications

- **GROUND LOOP ELIMINATION**
- **COMPUTER-PERIPHERAL INTERFACES**
- **LEVEL SHIFTING**
- **MICROPROCESSOR SYSTEM INTERFACES**
- **DIGITAL ISOLATION FOR A/D, D/A CONVERSION**
- **RS-232-C INTERFACE**
- **HIGH SPEED, LONG DISTANCE ISOLATED LINE RECEIVER**

Description

The HCPL-2300 optocoupler combines an 820 nm AlGaAs photon emitting diode with an integrated high gain photon detector. This combination of Hewlett-Packard designed and manufactured semiconductor devices brings new high performance capabilities to designers of isolated logic and data communication circuits.

The new low current, high speed AlGaAs emitter manufactured with a unique diffused junction, has the virtue of fast rise and fall times at low drive currents. Figure 6 illustrates the propagation delay vs. input current characteristic. These unique characteristics enable this device to be used in an RS-232-C interface with ground loop isolation and improved common mode rejection. As a line receiver, the HCPL-2300 will operate over longer line lengths for a given data rate because of lower I_F and V_F specifications.

The output of the shielded integrated detector circuit is an open collector Schottky clamped transistor. The shield, which shunts capacitively coupled common mode noise to ground, provides a guaranteed transient immunity specification of 100 V/μs. The output circuit includes an optional integrated 1000 Ohm pull-up resistor for the open collector. This gives designers the flexibility to use the internal resistor for pull-up to five volt logic or to use an external resistor for 18 volt CMOS logic.

The Electrical and Switching Characteristics of the HCPL-2300 are guaranteed over a temperature range of -40°C to 85°C. This enables the user to confidently design a circuit which will operate under a broad range of operating conditions.

Recommended Operating Conditions

		Sym.	Min.	Max.	Units
Input Voltage, Low Level		V_{FL}	-2.5	0.8	V
Input Current High Level	0° C to 85° C	I_{FH}	0.5	1.0	mA
	-40° C to 85° C		0.5	0.75	
Supply Voltage, Output		V_{CC}	4.75	5.25	V
Fan Out (TTL Load)		N		5	
Operating Temperature		T_A	-40	85	°C

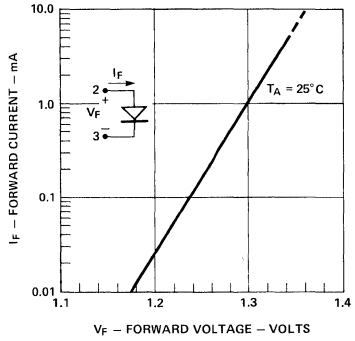


Figure 2. Typical Input Diode Forward Characteristic.

Absolute Maximum Ratings

(No derating required)

Parameter	Symbol	Min.	Max.	Units	Reference
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	85	°C	
Lead Solder Temperature	260° C for 10 s. (1.6 mm below seating plane)				
Average Forward Input Current	I_F		5	mA	See Note 2
Reverse Input Voltage	V_R		3.5	V	
Supply Voltage	V_{CC}	0.0	7.0	V	
Pull-up Resistor Voltage	V_{RL}	-0.5	V_{CC}	V	
Output Collector Current	I_O	-25	25	mA	
Input Power Dissipation	P_I		10	mW	
Output Collector Power Dissipation	P_O		40	mW	
Output Collector Voltage	V_O	-0.5	18	V	

Electrical Specifications

For -40°C ≤ T_A ≤ 85°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{FL} ≤ 0.8 V, unless otherwise specified.
All typicals at T_A = 25°C, V_{CC} = 5 V, unless otherwise specified. See note 1.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		0.05	250	μA	V_F = 0.8 V, V_O = 18 V	4	
Low Level Output Voltage	V_{OL}		0.4	0.5	V	I_F = 0.5 mA I_{OL} (Sinking) = 8 mA	3	
High Level Supply Current	I_{CCH}		4.0	6.3	mA	I_F = 0 mA, V_{CC} = 5.25 V		
Low Level Supply Current	I_{CCL}		6.2	10.0	mA	I_F = 1.0 mA, V_{CC} = 5.25 V		
Input Forward Voltage	V_F	1.0	1.3	1.5	Volts	T_A = 25°C, I_F = 1.0 mA	2	
		0.85		1.65				
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 1.0 mA		
Input Reverse Breakdown Voltage	BV_R	4.5			Volts	T_A = 25°C, I_R = 10 μA		
		3.5						
Input Capacitance	C_{IN}		18		pF	V_F = 0 V, f = 1 MHz		
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C		3
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3
Internal Pull-up Resistor	R_L	680	1000	1700	Ohms	T_A = 25°C		

Switching Specifications

For -40° C ≤ T_A ≤ 85° C, 0.5 mA ≤ I_{FH} ≤ 0.75 mA;
For 0° C ≤ T_A ≤ 85° C, 0.5 mA ≤ I_{FH} ≤ 1.0 mA; With 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{FL} ≤ 0.8 V, unless otherwise specified.
All typicals at T_A = 25° C, V_{CC} = 5 V, I_{FH} = 0.625 mA, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		95		ns	C_P = 0 pF	5, 6, 8	4, 8
			85	160		C_P = 20 pF	5, 8	
Propagation Delay Time to Logic Low Output Level	t_{PHL}		110		ns	C_P = 0 pF	5, 6, 8	5, 8
			35	200		C_P = 20 pF	5, 8	
Output Rise Time (10-90%)	t_r		40		ns	C_P = 20 pF	7, 8	8
Output Fall Time (90-10%)	t_f		20		ns			
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	100	400		V/μs	V_{CM} = 50 V (peak), V_O (min.) = 2 V, R_L = 560Ω, I_F = 0 mA	9, 10	6
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	100	400		V/μs	V_{CM} = 50 V (peak), V_O (max.) = 0.8 V, R_L = 560Ω, I_F = 0.5 mA	9, 10	7

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

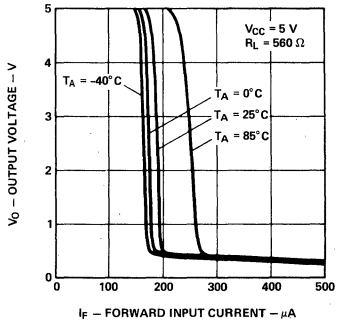


Figure 3. Typical Output Voltage vs. Forward Input Current vs. Temperature.

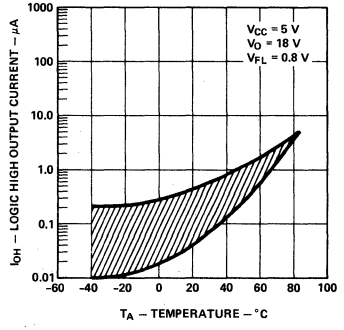


Figure 4. Typical Logic High Output Current vs. Temperature.

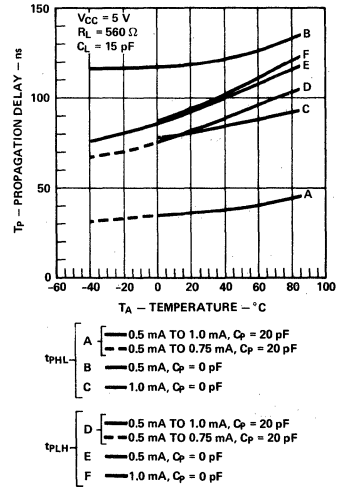


Figure 5. Typical Propagation Delay vs. Temperature and Forward Current With and Without Application of a Peaking Capacitor.

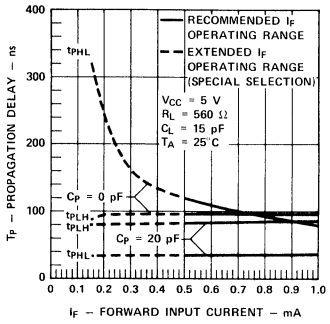


Figure 6. Typical Propagation Delay vs. Forward Current.

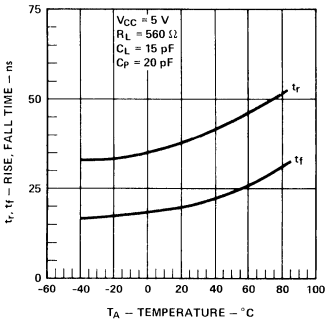


Figure 7. Typical Rise, Fall Time vs. Temperature.

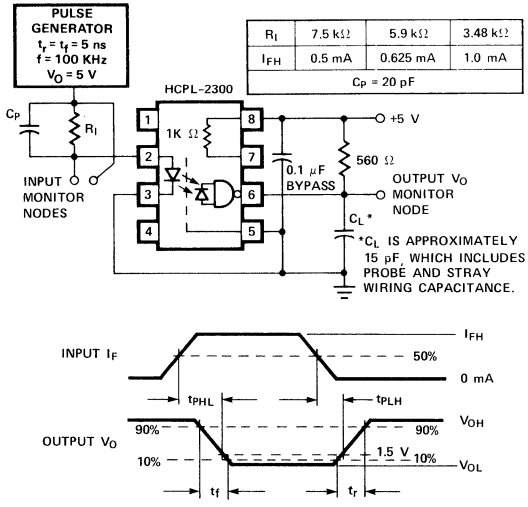


Figure 8. Test Circuit for t_{PHL}, t_{PLH}, t_r and t_f.

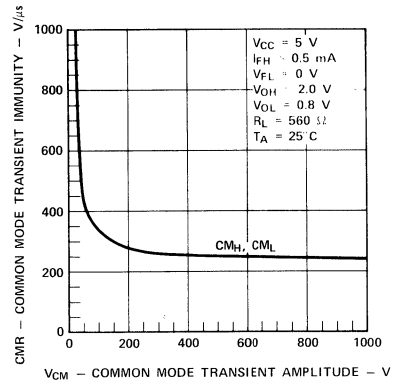
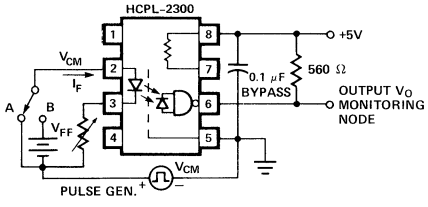
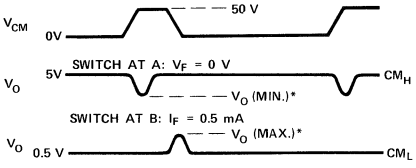


Figure 9. Typical Common Mode Transient Immunity vs. Common Mode Transient Amplitude.





*SEE NOTES 6, 7.

Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

OPTOCOUPLERS

Applications

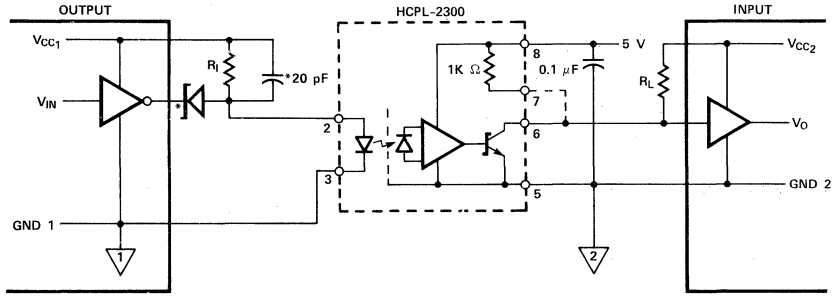
The HCPL-2300 optocoupler has the unique combination of low 0.5 mA LED operating drive current at a 5 MBd speed performance. Low power supply current requirement of 10 mA maximum and the ability to provide isolation between logic systems fulfills numerous applications ranging from logic level translations, line receiver and party line receiver applications, microprocessor I/O port isolation, etc. The open collector output allows for wired-OR arrangement. Specific interface circuits are illustrated in Figures 11 through 18 with corresponding component values, performance data and recommended layout.

For -40° C to 85° C operating temperature range, a mid range LED forward current (I_F) of 0.625 mA is recommended in order to prevent overdriving the integrated circuit detector due to increased LED efficiency at temperatures between 0° C and -40° C. For narrower temperature range of 0° C to 85° C, a suggested operating LED current of 0.75 mA is recommended for the mid range operating point and for minimal propagation delay skew. A peaking capacitance of 20 pF in parallel with the current limiting resistor for the LED shortens t_{PHL} by approximately 33% and t_{PLH} by 13%. Maintaining LED forward voltage (V_F) below 0.8 V will guarantee that the HCPL-2300 output is off.

The recommended shunt drive technique for TTL/LSTTL/CMOS of Figure 11 provides for optimal speed performance, no leakage current path through the LED, and reduced common mode influences associated with series switching of a "floating" LED. Alternate series drive techniques with either an active CMOS inverter or an open collector TTL/LSTTL inverter are illustrated in Figures 12 and 13 respectively. Open collector leakage current of 250 μA has been compensated by the 3.16K Ohms resistor (Figure 13) at the expense of twice the operating forward current.

An application of the HCPL-2300 as an unbalanced line receiver for use in long line twisted wire pair communication links is shown in Figure 14. Low LED I_F and V_F allow longer line length, higher speed and multiple stations on the line in comparison to higher I_F, V_F optocouplers. Greater speed performance along with nearly infinite common mode immunity are achieved via the balanced split phase circuit of Figure 15. Basic balanced (differential line receiver can be accomplished with one HCPL-2300 in Figure 15, but with a typical 400 V/μs common mode immunity. Data rate versus distance for both the above unbalanced and balanced line receiver applications are compared in Figure 16. The RS-232-C interface circuit of Figure 17 provides guaranteed minimum common mode immunity of 100 V/μs while maintaining the 2:1 dynamic range of I_F.

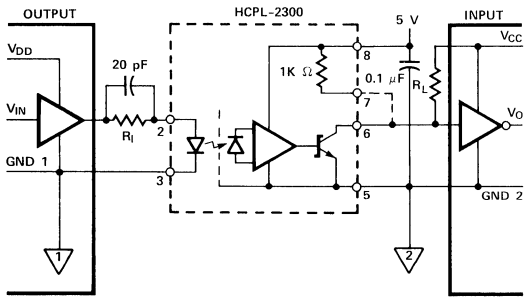
A recommended layout for use with an internal 1000 Ohms resistor or an external pull-up resistor and required V_{CC} bypass capacitor is given in Figure 18. V_{CC1} is used with an external pull-up resistor for output voltage levels (V_O) greater than or equal to 5 V. As illustrated in Figure 18, an optional V_{CC} and GND trace can be located between the input and the output leads of the HCPL-2300 to provide additional noise immunity at the compromise of insulation capability (V_{I-O}).



V_{IN} V_{DC}	V_{CC1} V_{DC}	R_I kΩ	R_L kΩ	V_{CC2} V_{DC}
5	5	6.19	1 (INTERNAL)	5
10	10	14.7	2.37	10
15	15	21.5	3.16	15

*SCHOTTKY DIODE (HP 5082-2800, OR EQUIVALENT) AND 20 pF CAPACITOR ARE NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

Figure 11. Recommended Shunt Drive Circuit for Interfacing Between TTL/LSTTL/CMOS Logic Systems.



V_{IN} V_{DC}	V_{DD} V_{DC}	R_I kΩ	R_L kΩ	V_{CC} V_{DC}
5	5	5.11	1 (INTERNAL)	5
10	10	13.3	2.37	10
15	15	19.6	3.16	15

Figure 12. Active CMOS Series Drive Circuit.

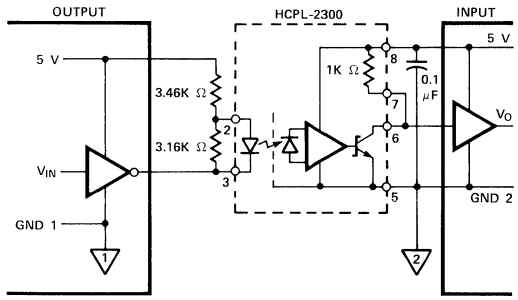
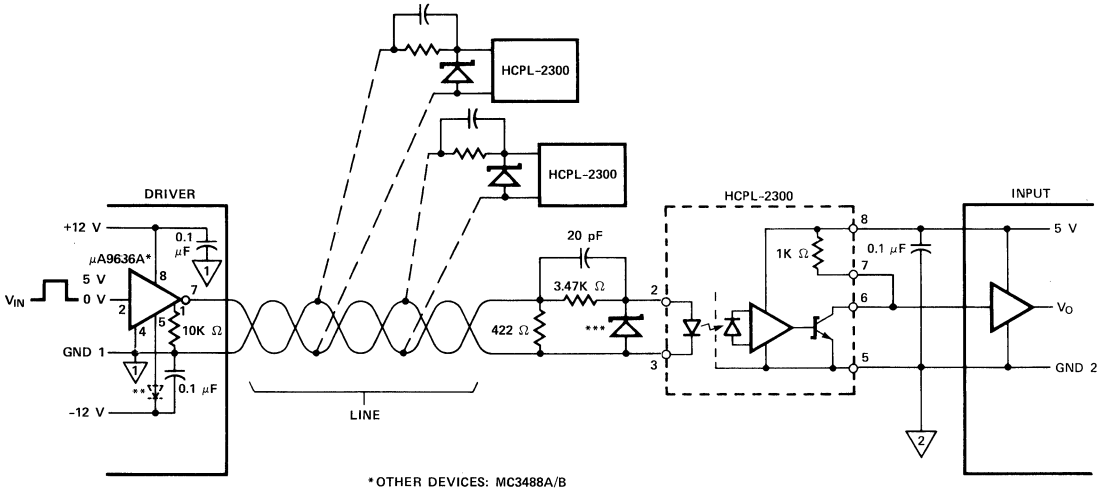


Figure 13. Series Drive from Open Collector TTL/LSTTL Units.



*OTHER DEVICES: MC3488A/B
TI-μA9636A.
**MAY BE REQUIRED ON OLDER VERSIONS OF μA9636A.
***SCHOTTKY DIODE (HP 5082-2800, OR EQUIVALENT).

REFERENCE FIGURE 16 FOR DATA RATE vs. LINE DISTANCE L.

Figure 14. Application of HCPL-2300 as Isolated, Unbalanced Line Receiver(s).

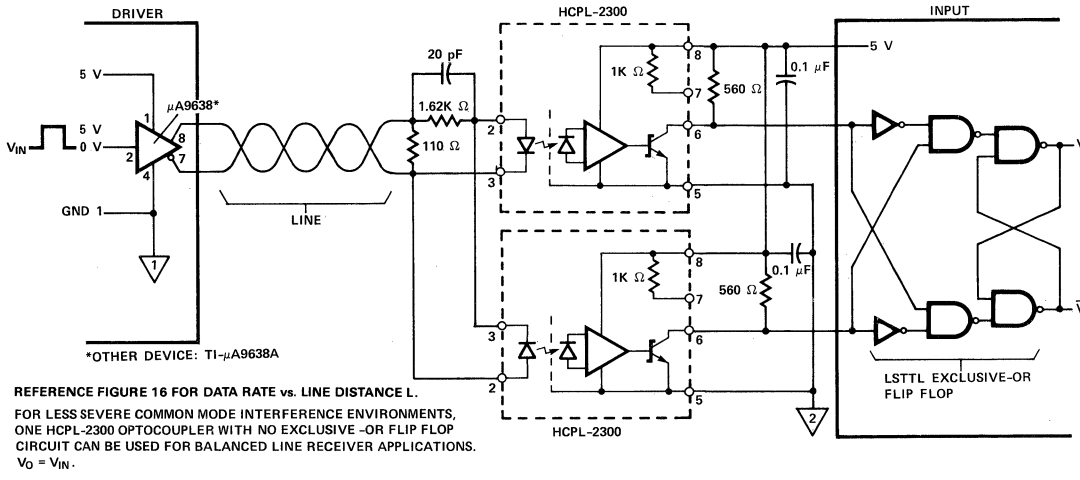


Figure 15. Application of Two HCPL-2300 Units Operating as an Isolated, High Speed, Balanced, Split Phase Line Receiver with Significantly Enhanced Common Mode Immunity.

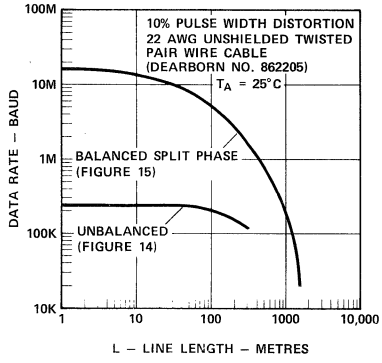


Figure 16. Typical Point to Point data Rate vs. Length of Line for Unbalanced (Figure 14) and Balanced (Figure 15) Line Receivers using HCPL-2300 Optocouplers.

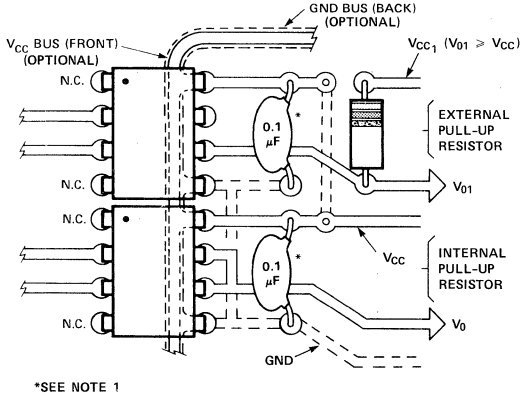


Figure 18. Recommended Printed Circuit Board Layout.

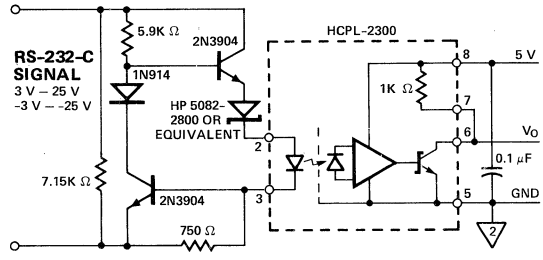


Figure 17. RS-232-C Interface Circuit with HCPL-2300. 0°C < T_A < 85°C.

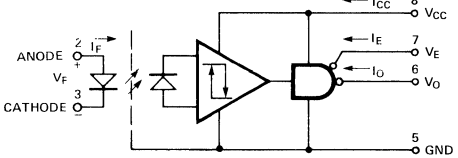
NOTES:
1. Bypassing the power supply line is required with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 18. The power supply bus for the optocoupler(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.
2. Peaking circuits may produce transient input currents up to 100 mA, 500 ns maximum pulse width, provided average current does not exceed 5 mA.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
7. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} < 0.8 V).
8. C_P is the peaking capacitance. Refer to test circuit in Figure 8.

HEWLETT PACKARD

20 M BAUD HIGH CMR LOGIC GATE OPTOCOUPLER

HCPL-2400
HCPL-2411

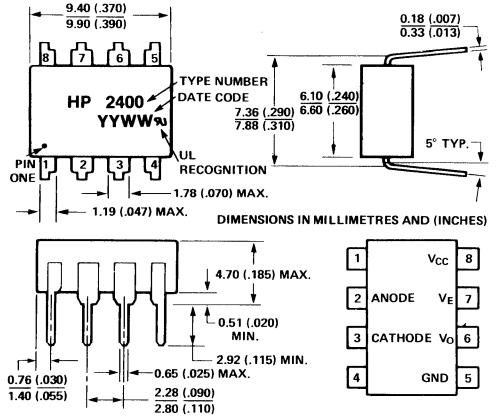
SCHEMATIC



TRUTH TABLE
(POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	L	L
OFF	L	H
ON	H	Z
OFF	H	Z

OUTLINE DRAWING



Features

- **HIGH SPEED: 40 MBd TYPICAL DATA RATE**
- **HIGH COMMON MODE REJECTION**
- **HCPL-2400 = 1kV/μs @ 50 V_{CM}**
- **HCPL-2411 = 1kV/μs @ 300 V_{CM}**
- **AC PERFORMANCE GUARANTEED OVER TEMPERATURE**
- **COMPATIBLE WITH TTL, STTL, LSTTL, AND HCMOS LOGIC FAMILIES**
- **HIGH SPEED AlGaAs EMITTER**
- **THREE STATE OUTPUT (NO PULL-UP RESISTOR REQUIRED)**
- **HIGH POWER SUPPLY NOISE IMMUNITY**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **VDE 0883 APPROVAL AVAILABLE**
- **MIL-STD-1772 VERSION AVAILABLE (HCPL-5400/1)**

Applications

- **ISOLATION OF HIGH SPEED LOGIC SYSTEMS**
- **COMPUTER-PERIPHERAL INTERFACES**
- **ISOLATED BUS DRIVER (NETWORKING APPLICATIONS)**
- **SWITCHING POWER SUPPLIES**
- **GROUND LOOP ELIMINATION**
- **HIGH SPEED DISK DRIVE I/O**
- **DIGITAL ISOLATION FOR A/D, D/A CONVERSION**
- **PULSE TRANSFORMER REPLACEMENT**

Description

The HCPL-2400/11 high speed optocouplers combine an 820 nm AlGaAs light emitting diode with a high speed photo-detector. This combination results in very high data rate capability and low input current. The three state output eliminates the need for a pull-up resistor and allows for direct drive of data buses. The hysteresis provides differential mode noise immunity and minimizes the potential for output signal chatter. Improved power supply rejection minimizes the need for special power supply bypassing precautions.

The electrical and switching characteristics of the HCPL-2400/11 are guaranteed over the temperature range of 0°C to 70°C.

The HCPL-2400/11 are compatible with TTL, STTL, LSTTL and HCMOS logic families. When Schottky type TTL devices (STTL) are used, a data rate performance of 20 MBd over temperature is guaranteed when using the application circuit of Figure 13. Typical data rates are 40 MBd.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.75	5.25	Volts
Input Current (High)	$I_{F(ON)}$	4	8	mA
Input Voltage (Low)	$V_{F(OFF)}$	—	0.8	Volts
Enable Voltage (Low)	V_{EL}	0	0.8	Volts
Enable Voltage (High)	V_{EH}	2.0	V_{CC}	Volts
Operating Temperature	T_A	0	70°	°C
Fan Out	N		5	TTL Loads

OPTOCOUPLERS

Absolute Maximum Ratings

(No derating required up to 85° C)

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	−55	125	°C	
Operating Temperature	T_A	−40	85	°C	
Lead Solder Temperature	260° C for 10 s. (1.6 mm below seating plane)				
Average Forward Input Current	I_F		10.0	mA	
Peak Forward Input Current	I_{FPK}		20.0	mA	9
Reverse Input Voltage	V_R		3.0	V	
Supply Voltage	V_{CC}	0	7.0	V	
Three State Enable Voltage	V_E	−0.5	10.0	V	
Average Output Collector Current	I_O	−25.0	25.0	mA	
Output Collector Voltage	V_O	−0.5	10.0	V	
Output Collector Power Dissipation	P_O		40.0	mW	

Electrical Specifications

For 0°C ≤ T_A ≤ 70°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, 4 mA ≤ $I_{F(ON)}$ ≤ 8 mA, 2.0 V ≤ V_{EH} ≤ 5.25, 0 V ≤ V_{EL} ≤ 0.8 V, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V except where noted. All typicals at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 6.0 mA, $V_{F(OFF)}$ = 0 V except where noted. See note 9.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 8.0 mA (5 TTL Loads)		1	
Logic High Output Voltage	V_{OH}	2.4			Volts	I_{OH} = −4.0 mA		2	
Output Leakage Current	I_{OHH}			100	μA	V_O = 5.25 V	V_F = 0.8 V		
Logic High Enable Voltage	V_{EH}	2.0			Volts				
Logic Low Enable Voltage	V_{EL}			0.8	Volts				
Logic High Enable Current	I_{EH}			20	μA	V_E = 2.4 V			
				100	μA	V_E = 5.25 V			
Logic Low Enable Current	I_{EL}		−0.28	−0.4	mA	V_E = 0.4V			
Logic Low Supply Current	I_{CCL}		19	26	mA	V_{CC} = 5.25 V			
Logic High Supply Current	I_{CCH}		17	26	mA	V_E = 0 V			
High Impedance State Supply Current	I_{CCZ}		22	28	mA	V_{CC} = 5.25 V V_E = 5.25 V			
High Impedance State Output Current	I_{OZL}			20	μA	V_O = 0.4V			
	I_{OZH}			20	μA	V_O = 2.4 V	V_E = 2 V		
	I_{OZH}			100	μA	V_O = 5.25 V			
Logic Low Short Circuit Output Current	I_{OSL}		52		mA	V_O = V_{CC} = 5.25 V	I_F = 8 mA		1
Logic High Short Circuit Output Current	I_{OSH}		−45		mA	V_{CC} = 5.25 V	I_F = 0 mA, V_O = GND		1
Input Current Hysteresis	I_{HYS}		0.25		mA	V_{CC} = 5 V		3	
Input Forward Voltage	V_F	1.1	1.3	1.5	Volts	T_A = 25°C	I_F = 8 mA	4	
		1.0		1.55					
Input Reverse Breakdown Voltage	BV_R	3.0	5.0		Volts	T_A = 25°C	I_R = 10 μA		
		2.0							
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		−1.44		mV/° C	I_F = 6 mA		4	
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min. T_A = 25°C			2
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 VDC			2
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 V dc			2
Input Capacitance	C_{IN}		20		pF	f = 1 MHz, V_F = 0V, Pins 2 and 3			

Switching Specifications

$0°C \le T_A \le 70°C$, $4.75\ V \le V_{CC} \le 5.25\ V$, $0.0\ V \le V_{EN} \le 0.8\ V$, $4\ mA \le I_F \le 8.0\ mA$. All typicals $V_{CC} = 5\ V$, $T_A = 25°C$, $I_F = 6.0\ mA$ except where noted.

Parameter	Symbol		Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}				55	ns	$I_{F(ON)} = 7.0\ mA$		5, 6, 7	4
			15	33	60	ns			5, 6, 7	3
Propagation Delay Time to Logic High Output Level	t_{PLH}				55	ns	$I_{F(ON)} = 7.0\ mA$		5, 6, 7	4
			15	30	60	ns			5, 6, 7	3
Pulse Width Distortion	$\lvert t_{PHL}-t_{PLH}\rvert$			2	15	ns	$I_{F(ON)} = 7.0\ mA$		5, 8	4
				3	25	ns			5, 8	
Propagation Delay Skew	t_{PSK}				35	ns			15, 16	5
Output Rise Time	t_r			20		ns			5	
Output Fall Time	t_f			10		ns			5	
Output Enable Time to Logic High	t_{PZH}			15		ns			9, 10	
Output Enable Time to Logic Low	t_{PZL}			30		ns			9, 10	
Output Disable Time from Logic High	t_{PHZ}			20		ns			9, 10	
Output Disable Time from Logic Low	t_{PLZ}			15		ns			9, 10	
Logic High Common Mode Transient Immunity	$\lvert CM_H\rvert$	2400	1000	10,000		V/μs	$V_{CM} = 50\ V$	$T_A = 25°C$, $I_F = 0$	11	6
		2411	1000			V/μs	$V_{CM} = 300\ V$			
Logic Low Common Mode Transient Immunity	$\lvert CM_L\rvert$	2400	1000	10,000		V/μs	$V_{CM} = 50\ V$	$T_A = 25°C$, $I_F = 4\ mA$	11	6
		2411	1000			V/μs	$V_{CM} = 300\ V$			
Power Supply Noise Immunity	PSNI			0.5		V_{p-p}	$V_{CC} = 5.0\ V$, $48\ Hz \le F_{AC} \le 50\ MHz$			7

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min.External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

Notes:

1. Duration of output short circuit time not to exceed 10 ms.
2. Device considered a two terminal device: pins 1–4 shorted together, and pins 5–8 shorted together.
3. t_{PHL} propagation delay is measured from the 50% level on the rising edge of the input current pulse to the 1.5 V level on the falling edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% level on the falling edge of the input current pulse to the 1.5 V level on the rising edge of the output pulse.
4. This specification simulates the worst case operating conditions of the HCPL-2400/11 over the recommended operating temperature and V_{CC} range with the suggested applications circuit of Figure 13.
5. Propagation delay skew is discussed later in this data sheet.
6. CM_H is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic high state ($V_{O(MIN)} > 2.0\ V$). CM_L is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic low state ($V_{O(MAX)} < 0.8\ V$).
7. Power Supply Noise Immunity is the peak to peak amplitude of the ac ripple voltage on the V_{CC} line that the device will withstand and still remain in the desired logic state. For desired logic high state, $V_{OH(MIN)} > 2.0\ V$, and for desired logic low state, $V_{OL(MAX)} < 0.8$ volts.
8. Peak Forward Input Current pulse width < 50 μs at 1 KHz maximum repetition rate.
9. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.

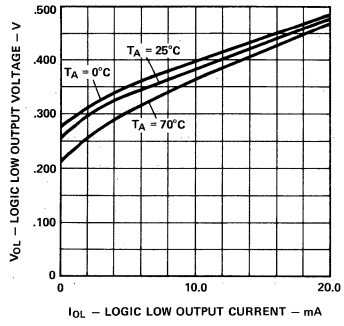


Figure 1. Typical Logic Low Output Voltage vs. Logic Low Output Current

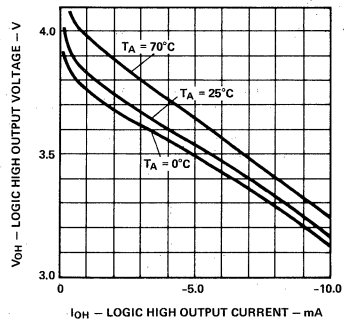


Figure 2. Typical Logic High Output Voltage vs. Logic High Output Current

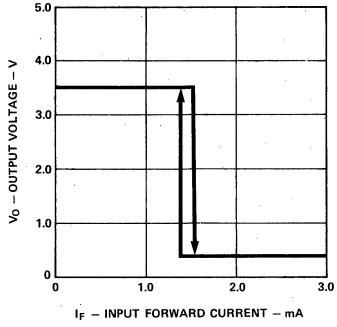


Figure 3. Typical Output Voltage vs. Input Forward Current

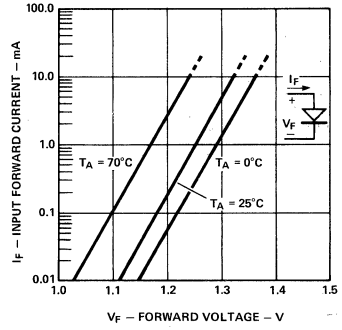


Figure 4. Typical Diode Input Forward Current Characteristic

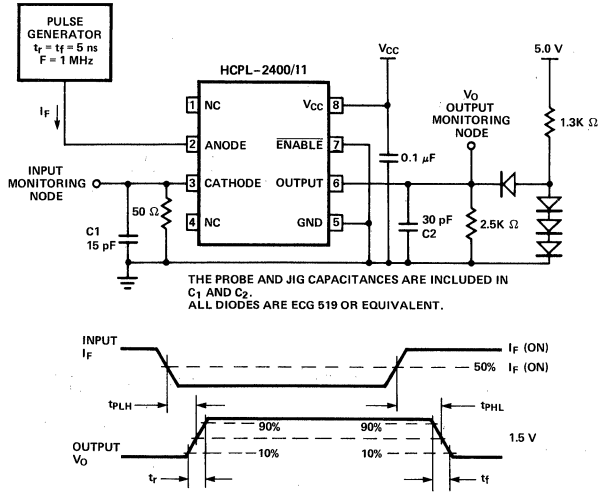


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

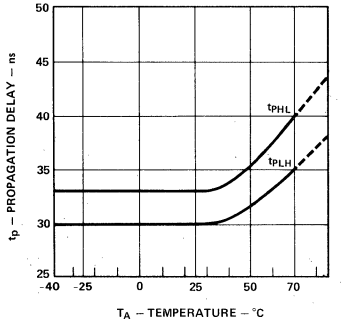


Figure 6. Typical Propagation Delay vs. Ambient Temperature

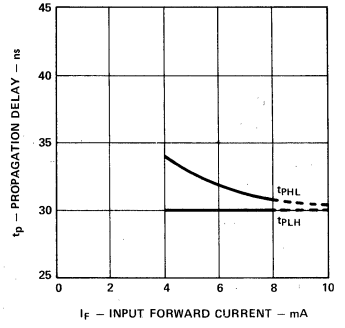


Figure 7. Typical Propagation Delay vs. Input Forward Current

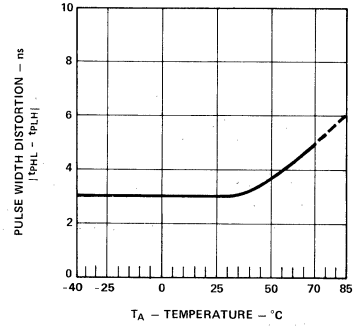


Figure 8. Typical Pulse Width Distortion vs. Ambient Temperature

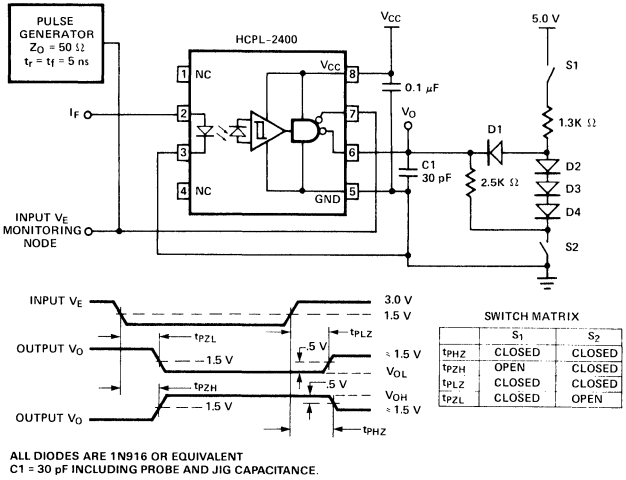


Figure 9. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ} and t_{PZL}.

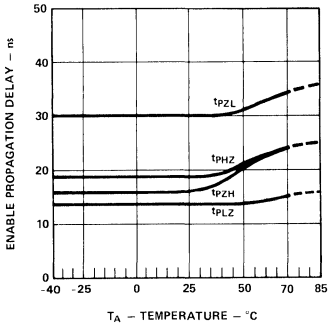
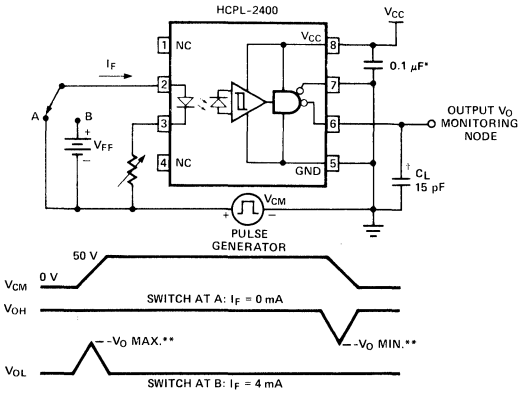


Figure 10. Typical Enable Propagation Delay vs. Ambient Temperature



*MUST BE LOCATED ≤ 1 cm FROM DEVICE UNDER TEST.
**SEE NOTE 6.
† C_L IS APPROXIMATELY 15 pF, WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

Figure 11. Test Diagram for Common Mode Transient Immunity and Typical Waveforms

Applications

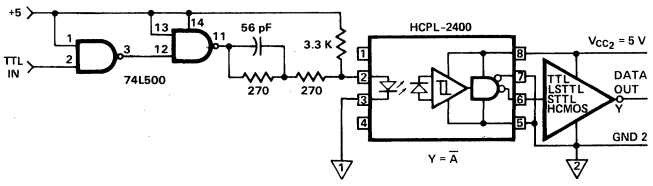


Figure 13. Recommended 20 MBd HCPL-2400/11 Interface Circuit

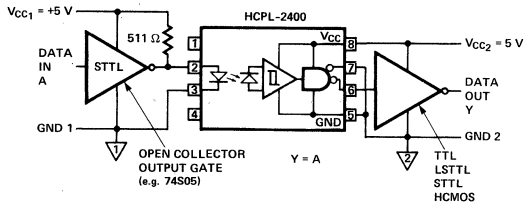


Figure 14. Alternative HCPL-2400/11 Interface Circuit

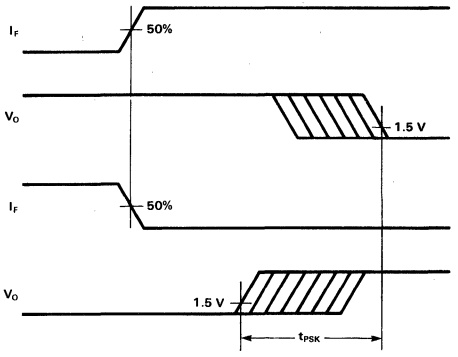


Figure 15. Illustration of Propagation Delay Skew — t_{PSK}.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 5).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 15, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 16 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 16 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The HCPL-2400/11 optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion, and propagation delay skew over the recommended temperature, input current, and power supply ranges.

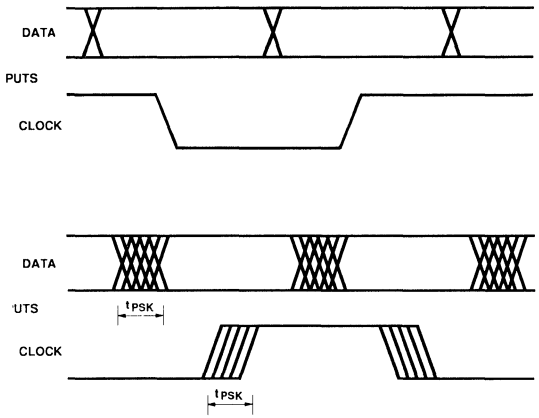


Figure 16. Parallel Data Transmission Example.

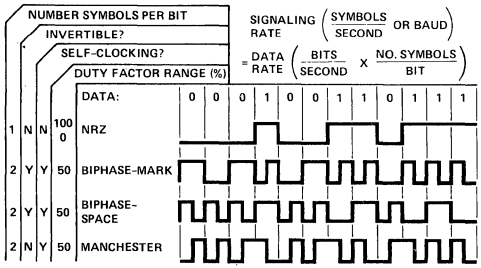


Figure 17. Modulation Code Selections

Application Circuit

A recommended LED drive circuit is shown in Figure 13. This circuit utilizes several techniques to minimize the total pulse-width distortion at the output of the optocoupler. By using two inverting TTL gates connected in series, the inherent pulse-width distortion of each gate cancels the distortion of the other gate. For best results, the two series-connected gates should be from the same package.

The circuit in Figure 13 also uses techniques known as prebias and peaking to enhance the performance of the optocoupler LED. Prebias is a small forward voltage applied to the LED when the LED is off. This small prebias voltage partially charges the junction capacitance of the LED, allowing the LED to turn on more quickly. The speed of the LED is further increased by applying momentary current peaks to the LED during the turn-on and turn-off transitions of the drive current. These peak currents help to charge and discharge the capacitances of the LED more quickly, shortening the time required for the LED to turn on and off.

Switching performance of the HCPL-2400/11 optocouplers is not sensitive to the TTL logic family used in the recommended drive circuit. The typical and worst-case switching parameters given in the data sheet can be met using common 74LS TTL inverting gates or buffers. Use of faster TTL families will slightly reduce the overall propagation delays from the input of the drive circuit to the output of the optocoupler, but will not necessarily result in lower pulse-width distortion or propagation delay skew. This reduction in overall propagation delays is due to shorter delays in the drive circuit, not to changes in the propagation delays of the optocoupler; optocoupler propagation delays are not affected by the speed of the logic used in the drive circuit.

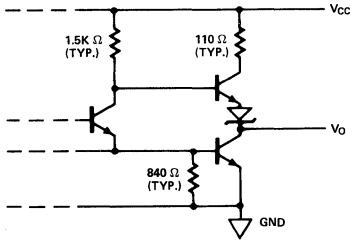
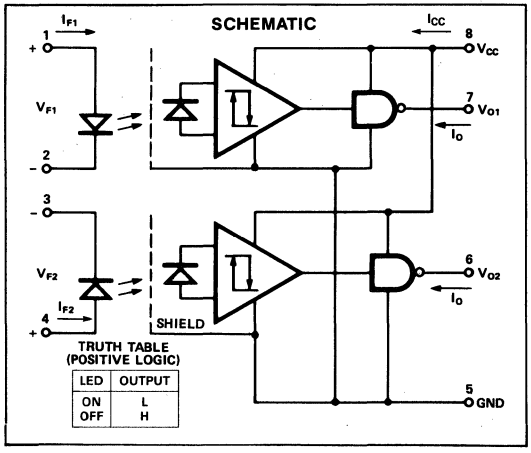


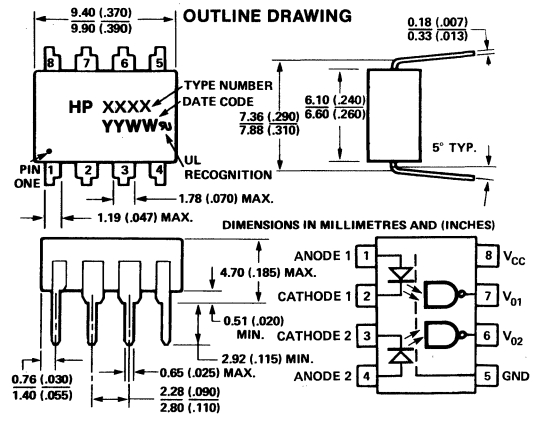
Figure 18. Typical HCPL-2400/11 Output Schematic

HEWLETT PACKARD

DUAL CHANNEL, 20 M BAUD HIGH CMR LOGIC GATE OPTOCOUPLER

HCPL-2430





Features

- VDE 0883 APPROVAL AVAILABLE
- HIGH SPEED: 40 MBd TYPICAL DATA RATE
- HIGH COMMON MODE REJECTION — 1000 V/μs GUARANTEED MINIMUM COMMON MODE TRANSIENT IMMUNITY
- AC PERFORMANCE GUARANTEED OVER TEMPERATURE
- COMPATIBLE WITH TTL, STTL, LSTTL, AND HCMOS LOGIC FAMILIES
- HIGH SPEED AlGaAs EMITTER
- TOTEM POLE OUTPUT (NO PULLUP RESISTOR REQUIRED)
- HIGH POWER SUPPLY NOISE IMMUNITY
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE
- MIL-STD-1772 VERSION AVAILABLE (HCPL-5430/1)

Applications

- ISOLATION OF HIGH SPEED LOGIC SYSTEMS
- COMPUTER-PERIPHERAL INTERFACES
- SWITCHING POWER SUPPLIES
- GROUND LOOP ELIMINATION
- HIGH SPEED DISK DRIVE I/O
- DIGITAL ISOLATION FOR A/D, D/A CONVERSION
- PULSE TRANSFORMER REPLACEMENT

Description

The HCPL-2430 high speed optocoupler combines an 820 nm AlGaAs LED with a high speed photo detector. This combination results in very high data rate capability and low input current. The totem pole output eliminates the need for a pull-up resistor.

The detectors have totem pole output stages and optical receiver input stages with built-in Schmitt triggers to provide logic compatible waveforms, eliminating the need for additional waveshaping. Improved power supply rejection minimizes the need for special power supply bypassing precautions; however, it is still recommended as good design practice.

The electrical and switching characteristics of the HCPL-2430 are guaranteed over the temperature range of 0°C to 70°C.

The HCPL-2430 is compatible with TTL, STTL, LSTTL and HCMOS logic families. A data rate performance of 20 MBd over temperature is guaranteed when using the application circuit of Figure 10. Typical data rates are 40 MBd.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.75	5.25	Volts
Input Current (High)	$I_{F(ON)}$	4	8	mA
Input Voltage (Low)	$V_{F(OFF)}$	—	0.8	Volts
Operating Temperature	T_A	0	70°	°C
Fan Out	N		5	TTL Loads

Absolute Maximum Ratings (No derating required up to 70°C)

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	85	°C	
Lead Solder Temperature	260°C for 10 s. (1.6 mm below seating plane)				
Average Forward Input Current	I_F		10.0	mA	
Peak Forward Input Current	I_{FPK}		20.0	mA	10
Reverse Input Voltage	V_R		3.0	V	
Supply Voltage	V_{CC}	0	7.0	V	
Total Package Power Dissipation	P		350	mW	11
Average Output Collector Current	I_O	-25.0	25.0	mA	
Output Collector Voltage	V_O	-0.5	10.0	V	
Output Collector Power Dissipation	P_O		40.0	mW	

Electrical Specifications

For 0°C ≤ T_A ≤ 70°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, 4 mA ≤ $I_{F(ON)}$ ≤ 8 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V except where noted.
All Typicals at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 6.0 mA, $V_{F(OFF)}$ = 0 V except where noted. See note 12.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Notes
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 8.0 mA (5 TTL Loads)		1,3	1
Logic High Output Voltage	V_{OH}	2.4 2.7			Volts	I_{OH} = -4.0 mA I_{OH} = -0.4 mA		2,3	1
Output Leakage Current	I_{OHH}			100	μA	V_O = 5.25 V	V_F = 0.8 V		1
Logic Low Supply Current	I_{CCL}		34	46	mA	V_{CC} = 5.25 V			12
Logic High Supply Current	I_{CCH}		32	42	mA				
Logic Low Short Circuit Output Current	I_{OSL}		60		mA	V_O = V_{CC} = 5.25 V	I_F = 8 mA		1,2
Logic High Short Circuit Output Current	I_{OSH}		-51		mA	V_{CC} = 5.25 V	I_F = 0 mA, V_O = GND		1,2
Input Forward Voltage	V_F	1.10 1.0	1.3	1.50 1.55	Volts	T_A = 25°C	I_F = 8 mA	4	1
Input Reverse Breakdown Voltage	BV_R	3.0 2.0	5		Volts	T_A = 25°C	I_R = 10 μA		1
Input Diode Forward Voltage Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.34		mV/°C	I_F = 6 mA		4	
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min. T_A = 25°C			3
Resistance Input-Output	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 Vdc			3
Capacitance Input-Output	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 Vdc			3
Input Capacitance	C_{IN}		20		pF	f = 1 MHz, V_F = 0 V, Pins 2 and 3			
Input-Input Insulation Leakage Current	I_{I-I}		0.005		μA	Relative Humidity = 45% t = 5 s, V_{I-I} = 500 V			11
Resistance (Input-Input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500 V			11
Capacitance (Input-Input)	C_{I-I}		0.25		pF	f = 1 MHz			11

Switching Specifications

$0°C \le T_A \le 70°C$, $4.75\ V \le V_{CC} \le 5.25\ V$, $4\ mA \le I_F \le 8.0\ mA$. All Typicals $V_{CC} = 5\ V$, $T_A = 25°C$, $I_F = 6.0\ mA$ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		33	60	ns		5, 6, 7	1, 4
Propagation Delay Time to Logic High Output Level	t_{PLH}		30	60	ns		5, 6, 7	1, 4
Pulse Width Distortion	$\lvert t_{PHL} - t_{PLH} \rvert$		5	25	ns		5, 8	
Propagation Delay Skew	t_{PSK}			35	ns		11, 12	
Output Rise Time	t_r		12		ns		5	
Output Fall Time	t_f		10		ns		5	
Logic High Common Mode Transient Immunity	$\lvert CM_H \rvert$	1000	10,000		V/μs	$T_A = 25°C$, $I_F = 0$, $V_{CM} = 50\ V$	9	7
Logic Low Common Mode Transient Immunity	$\lvert CM_L \rvert$	1000	10,000		V/μs	$T_A = 25°C$, $I_F = 4\ mA$, $V_{CM} = 50\ V$	9	7
Power Supply Noise Immunity	PSNI		0.5		V_{p-p}	$V_{CC} = 5.0\ V$, $48\ Hz \le F_{AC} \le 50\ MHz$		8

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min.External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

Notes:

1. Each channel.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
5. The typical data shown is indicative of what can be expected using the application circuit in Figure 11.
6. Propagation delay skew is discussed later in this data sheet.
7. CM_H is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic high state ($V_{O(MIN)} > 2.0\ V$). CM_L is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic low state ($V_{O(MAX)} < 0.8\ V$).
8. Power Supply Noise Immunity is the peak to peak amplitude of the ac ripple voltage on the V_{CC} line that the device will withstand and still remain in the desired logic state. For desired logic high state, $V_{OH(MIN)} > 2.0\ V$, and for desired logic low state, ($V_{OL(MAX)} < 0.8\ V$).
9. Peak Forward Input Current pulse width < 50 μs at 1 KHz maximum repetition rate.
10. Derate power dissipation above 70°C at 6.0 mW/°C.
11. Measured between pins 1 and 2, shorted together, and pins 3 and 4, shorted together.
12. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.

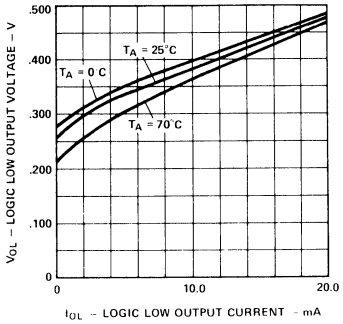


Figure 1. Typical Logic Low Output Voltage vs. Logic Low Output Current

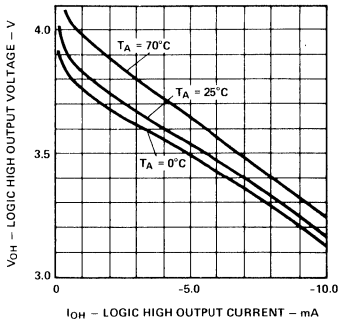


Figure 2. Typical Logic High Output Voltage vs. Logic High Output Current

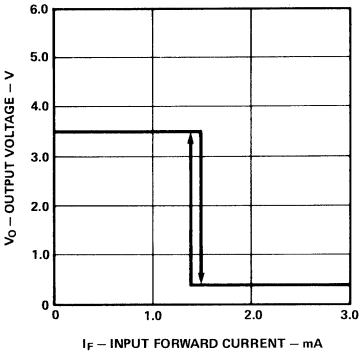


Figure 3. Typical Output Voltage vs. Input Forward Current

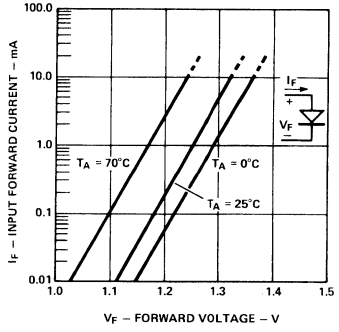


Figure 4. Typical Diode Input Forward Current Characteristic

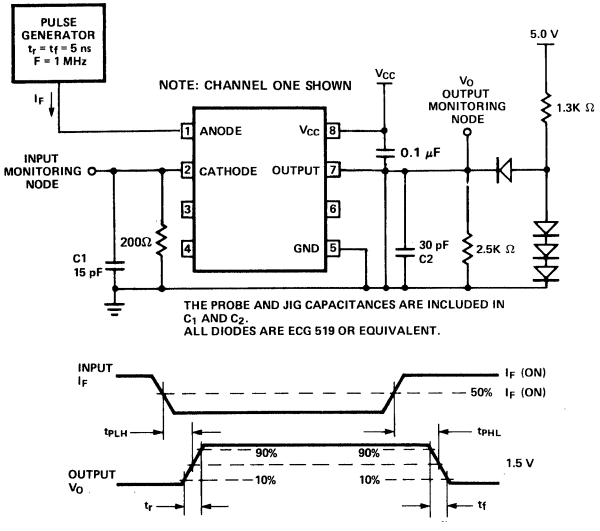


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r and t_f

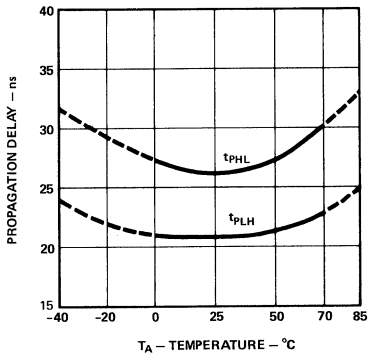


Figure 6. Typical Propagation Delay vs. Ambient Temperature

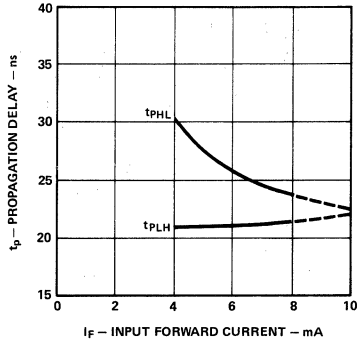


Figure 7. Typical Propagation Delay vs. Input Forward Current

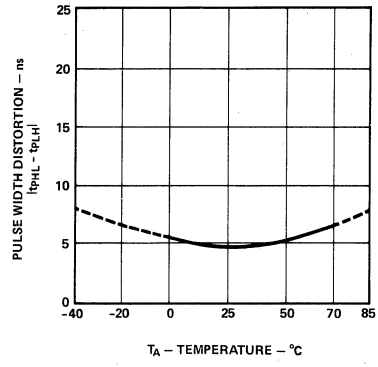
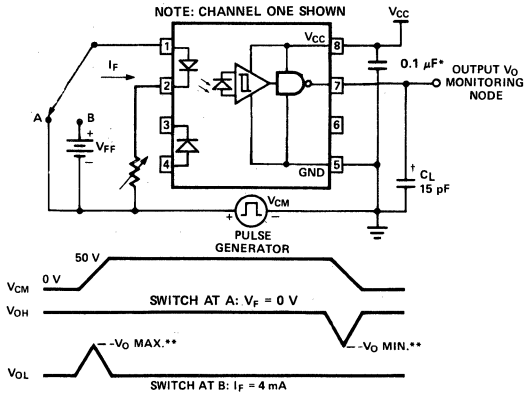


Figure 8. Typical Pulse Width Distortion vs. Ambient Temperature



*MUST BE LOCATED < 1 cm FROM DEVICE UNDER TEST.
**SEE NOTE 7.
† C_L IS APPROXIMATELY 15 pF, WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

Figure 9. Test Diagram for Common Mode Transient Immunity and Typical Waveforms

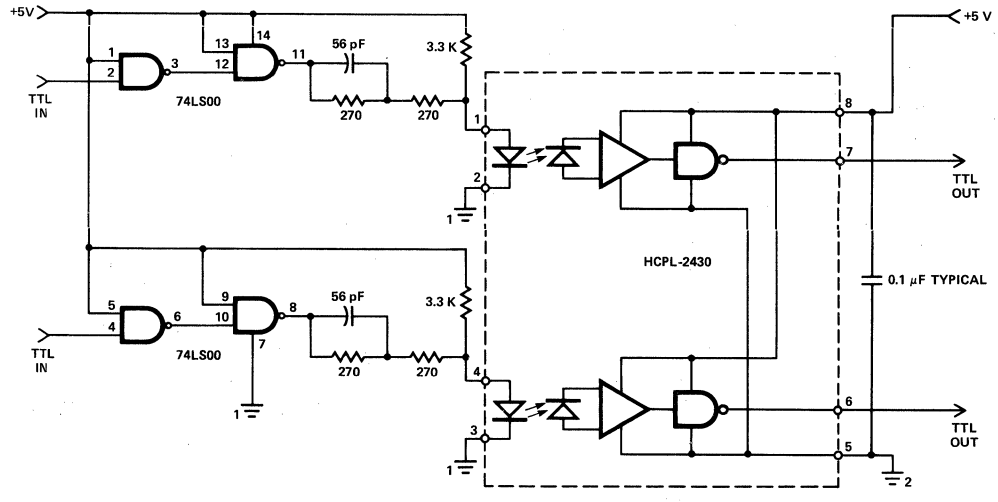


Figure 10. Recommended 20 Mbd HCPL-2430 Interface Circuit.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 5).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 11, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 12 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 12 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The HCPL-2430 optocoupler offers the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, input current, and power supply ranges.

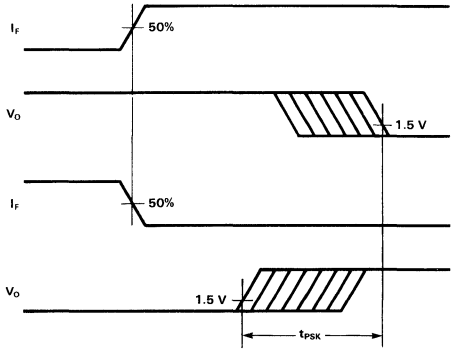


Figure 11. Illustration of Propagation Delay Skew — t_{PSK}.

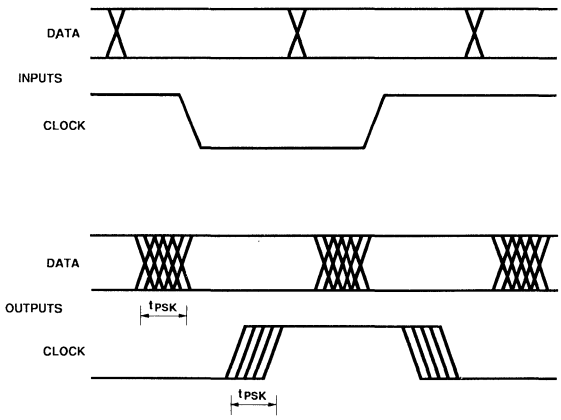


Figure 12. Parallel Data Transmission Example.

Application Circuit

A recommended LED drive circuit is shown in Figure 11. This circuit utilizes several techniques to minimize the total pulse-width distortion at the output of the optocoupler. By using two inverting TTL gates connected in series, the inherent pulse-width distortion of each gate cancels the distortion of the other gate. For best results, the two series-connected gates should be from the same package.

The circuit in Figure 11 also uses techniques known as prebias and peaking to enhance the performance of the optocoupler LED. Prebias is a small forward voltage applied to the LED when the LED is off. This small prebias voltage partially charges the junction capacitance of the LED, allowing the LED to turn on more quickly. The speed of the LED is further increased by applying momentary current peaks to the LED during the turn-on and turn-off transistions of the drive current. These peak currents help to charge and discharge the capacitances of the LED more quickly, shortening the time required for the LED to turn on and off.

Switching performance of the HCPL-2430 optocoupler is not sensitive to the TTL logic family used in the recommended drive circuit. The typical and worst-case switching parameters given in the data sheet can be met using common 74LS TTL inverting gates or buffers. Use of faster TTL families will slightly reduce the overall propagation delays from the input of the drive circuit to the output of the optocoupler, but will not necessarily result in lower pulse-width distortion or propagation delay skew. This reduction in overall propagation delays is due to shorter delays in the drive circuit, not to changes in the propagation delays of the optocoupler; optocoupler propagation delays are not affected by the speed of the logic used in the drive circuit.

HEWLETT PACKARD

High CMR, High Speed TTL Compatible Optocoupler

Technical Data

6N137
HCPL-2601
HCPL-2611

Features

- **Internal Shield for High Common Mode Rejection (CMR)**
  HCPL-2601: 1000 V/μs at V_{CM} = 50 V
  HCPL-2611: 5000 V/μs at V_{CM} = 1000 V
- **High Speed: 10 MBd Typical**
- **LSTTL/TTL Compatible**
- **Low Input Current Capability: 5 mA**
- **Guaranteed ac and dc Performance over Temperature: 0°C to 70°C**
- **Strobable Output**
- **Recognized Under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 VAC, 1 Minute and 5000 VAC, 1 Minute (Option 020)**
- **Hermetic Equivalent Device Available (HCPL-5600/1)**
- **VDE 0883 Approval Available**

*JEDEC Registered Data (The HCPL-2601 and HCPL-2611 are not registered.)

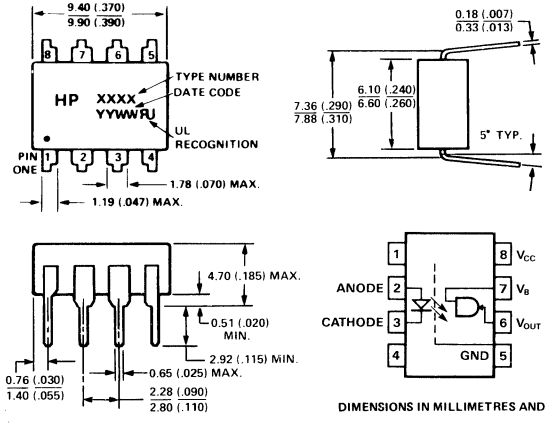
Description

The 6N137/HCPL-2601/11 optically coupled gates combine a GaAsP light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed. The output of the detector I.C. is an open collector Schottky clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 1000 V/μs for the 2601, and 5000 V/μs with the 2611.

This unique design provides maximum ac and dc circuit isolation while achieving TTL compatibility. The optocoupler ac and dc operational parameters are guaranteed from 0°C to 70°C allowing troublefree system performance.

The 6N137/HCPL-2601/11 are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Outline Drawing*



DIMENSIONS IN MILLIMETRES AND (INCHES).

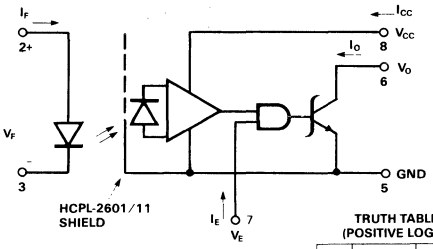
CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

OPTOCOUPLERS

Applications

- **Isolated Line Receiver**
- **Simplex/Multiplex Data Transmission**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Switching Power Supply**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**

Schematic



USE OF A 0.1 μF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}	0	250	μA
Input Current, High Level	I_{FH}*	5	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

*The initial switching threshold is 5 mA or less. It is recommended that 6.3 mA to 10 mA be used for best performance and to permit at least a 20% CTR degradation guardband.

Absolute Maximum Ratings

(No Derating Required up to 85°C)

Storage Temperature ..... -55°C to +125°C

Operating Temperature ..... -40°C to +85°C

Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)

Forward Input Current – I_F (see Note 2) ..... 20 mA

Reverse Input Voltage ..... 5 V

Supply Voltage – V_{CC} ..... 7 V (1 Minute Maximum)

Enable Input Voltage – V_E ..... 5.5 V
(Not to exceed V_{CC} by more than 500 mV)

Output Collector Current – I_O ..... 50 mA

Output Collector Power Dissipation ..... 85 mW

Output Collector Voltage – V_O ..... 7 V
(Selection for higher output voltages up to 20 V is available.)

Electrical Characteristics

Over recommended temperature (T_A = 0°C to +70°C) unless otherwise specified. (See note 1.)

Parameter	Sym.	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}*		8	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 µA, V_E = 2.0 V	1	13
Low Level Output Voltage	V_{OL}*		0.4	0.6	V	V_{CC} = 5.5 V, I_F = 5 mA, V_E = 2.0 V, I_{OL} (Sinking) = 13 mA	2, 4, 14	
High Level Supply Current	I_{CCH}*		7.5	10	mA	V_{CC} = 5.5 V, I_F = 0, V_E = 0.5 V		14
Low Level Supply Current	I_{CCL}*		10	13	mA	V_{CC} = 5.5 V, I_F = 10 mA, V_E = 0.5 V		15
High Level Enable Current	I_{EH}		-0.8		mA	V_{CC} = 5.5 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}*		-1.1	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5 V		16
High Level Enable Voltage	V_{EH}	2.0			V			11
Low Level Enable Voltage	V_{EL}			0.8	V			
Input Forward Voltage	V_F		1.5	1.75*	V	T_A = 25°C	3, 13	
				1.80		I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R = 10 µA		
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz		
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 10 mA	13	
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 MIN		12
OPT 020	V_{ISO}	5000			V_{RMS}			
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

*JEDEC registered data for the 6N137.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to +70°C), V_{CC} = 5 V, I_F = 7.5 mA unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}			45	75*	ns	T_A = 25°C	5, 6, 7	4
					100	ns			
Propagation Delay Time to Low Output Level	t_{PHL}			55	75*	ns	T_A = 25°C	5, 6, 8	5
					100	ns			
Pulse Width Distortion	$\lvert t_{PHL}-t_{PLH} \rvert$			14		ns	R_L = 350 Ω, C_L = 15 pF		4, 5
Output Rise Time (10-90%)	t_r			20		ns		11	
Output Fall Time (90-10%)	t_f			15		ns		11	
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}			30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	9, 10	6
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}			25		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	9, 10	7
Common Mode Transient Immunity at High Output Level	$\lvert CM_H \rvert$	6N137		100		V/μs	V_{CM} = 10 V	12	8, 10
		HCPL-2601	1000	10,000		V/μs	V_{CM} = 50 V		
		HCPL-2611	5000			V/μs	V_{CM} = 1000 V		
							$V_{O(MIN)}$ = 2 V, R_L = 350 Ω, I_F = 0 mA, T_A = 25°C		
Common Mode Transient Immunity at Low Output Level	$\lvert CM_L \rvert$	6N137		300		V/μs	V_{CM} = 10 V	12	9, 10
		HCPL-2601	1000	10,000		V/μs	V_{CM} = 50 V		
		HCPL-2611	5000			V/μs	V_{CM} = 1000 V		
							$V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, I_F = 7.5 mA T_A = 25°C		

*JEDEC registered data for the 6N137.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Notes:

1. Bypassing of the power supply line is required, with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 15. The power supply bus for the optocoupler(s) should be separate from the bus for any active loads.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
7. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
8. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
9. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} < 0.8 V).
10. For sinusoidal voltages,
$$\left(\frac{\lvert dv_{CM} \rvert}{dt}\right)_{max} = \pi f_{CM} V_{CM}\ (p\text{-}p)$$
11. No external pull up is required for a high logic state on the enable input.
12. See Option 020 data sheet for more information.
13. The JEDEC registration for the 6N137 specifies a maximum I_{OH} of 250 μA. HP guarantees a maximum I_{OH} of 100 μA.
14. The JEDEC registration for the 6N137 specifies a maximum I_{CCH} of 15 mA. HP guarantees a maximum I_{CCH} of 10 mA.
15. The JEDEC registration for the 6N137 specifies a maximum I_{CCL} of 18 mA. HP guarantees a maximum I_{CCL} of 13 mA.
16. The JEDEC registration for the 6N137 specifies a maximum I_{EL} of –2.0 mA. HP guarantees a maximum I_{EL} of –1.6 mA.

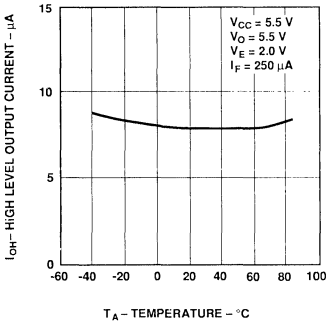


Figure 1. High Level Output Current vs. Temperature.

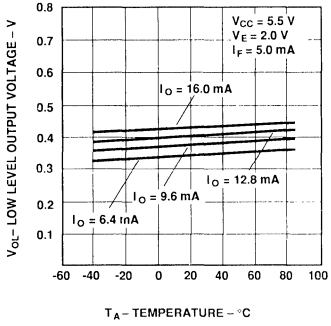


Figure 2. Low Level Output Voltage vs. Temperature.

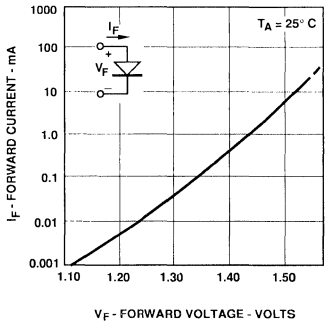


Figure 3. Input Diode Forward Characteristic.

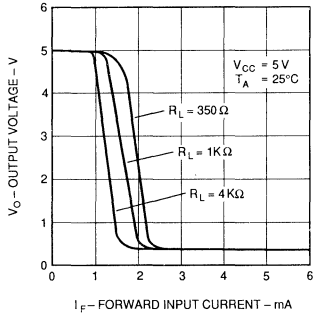


Figure 4. Output Voltage vs. Forward Input Current.

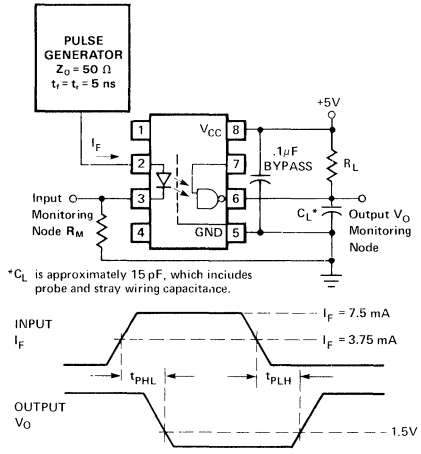


Figure 5. Test Circuit for t_{PHL} and t_{PLH}.**
**JEDEC Registered Data

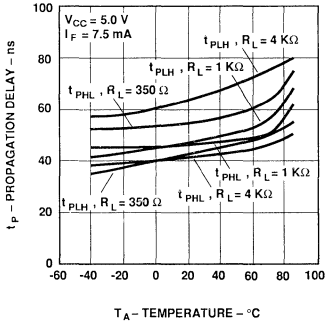


Figure 6. Propagation Delay vs. Temperature.

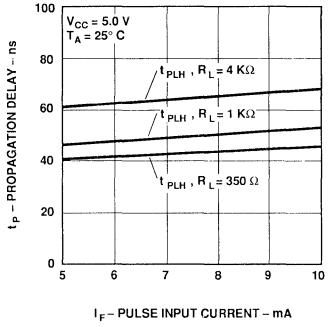


Figure 7. Propagation Delay (t_{PLH}) vs. Pulse Input Current.

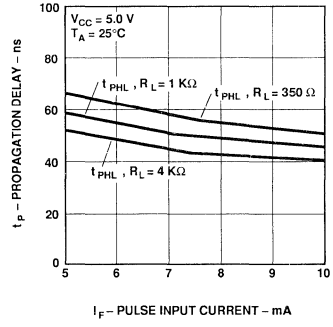


Figure 8. Propagation Delay (t_{PHL}) vs. Pulse Input Current.

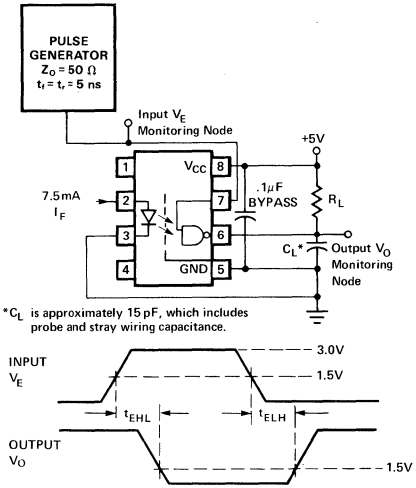


Figure 9. Test Circuit for t_{EHL} and t_{ELH}.

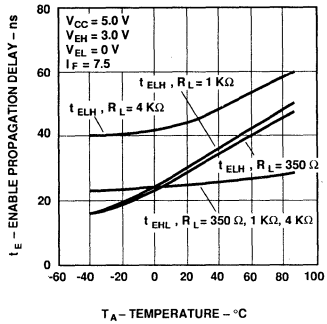


Figure 10. Enable Propagation Delay vs. Temperature.

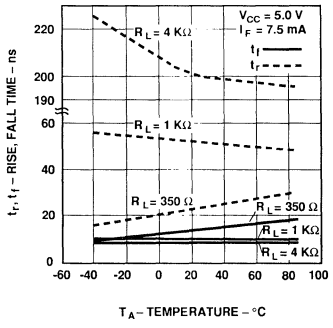


Figure 11. Rise and Fall Time vs. Temperature.

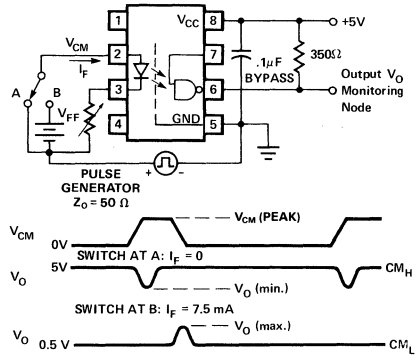


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

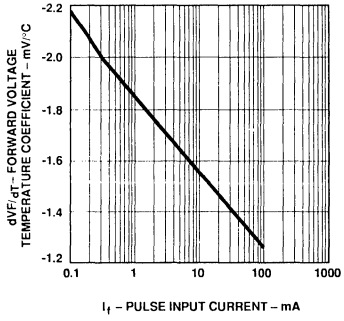


Figure 13. Temperature Coefficient of Forward Voltage vs. Input Current.

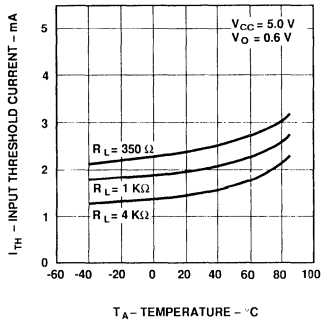


Figure 14. Input Threshold Current vs. Temperature.

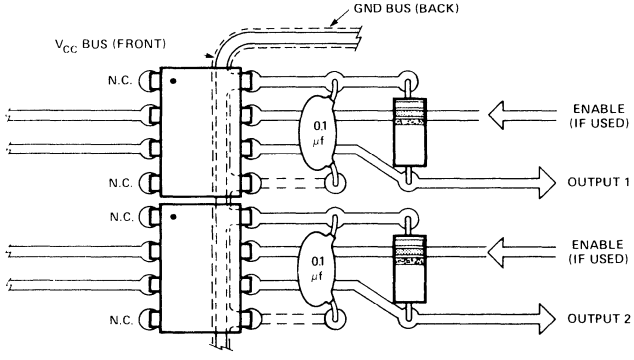


Figure 15. Recommended Printed Circuit Board Layout.

HEWLETT PACKARD

High CMR Line Receiver Optocoupler

Technical Data

HCPL-2602
HCPL-2612

Features

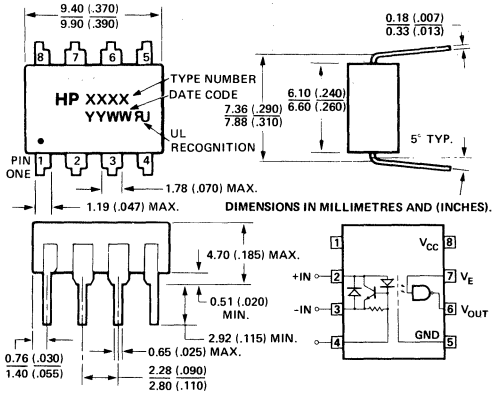
- **Internal Shield for High Common Mode Rejection (CMR)**
  HCPL-2602: 1000 V/μs at V_{CM} = 50 V
  HCPL-2612: 3500 V/μs at V_{CM} = 300 V
- **Line Termination Included – No Extra Circuitry Required**
- **Accepts a Broad Range of Drive Conditions**
- **LED Protection Minimizes LED Efficiency Degradation**
- **High Speed: 10 MBd (Limited by Transmission Line in Many Applications)**
- **Guaranteed ac and dc Performance Over Temperature: 0°C to 70°C**
- **External Base Lead Allows "LED Peaking" and LED Current Adjustment**
- **Recognized Under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 VAC.**
- **VDE 0883 Approval Pending**
- **Hermetic Equivalent Device Available (HCPL-1930/1)**

Description

The HCPL-2602/12 optically coupled line receivers combine a GaAsP light emitting diode, an input current regulator and an integrated high gain photo detector. The input regulator serves as a line termination for line receiver applications. It clamps the line voltage and regulates the LED current so line reflections do not interfere with circuit performance.

The regulator allows a typical LED current of 8.5 mA before it starts to shunt excess current. The output of the detector IC is an open collector Schottky clamped transistor. An enable input gates the detector. The internal detector shield provides a guaranteed common mode transient immunity specification of 1000 V/μs for the 2602, and 3500 V/μs for the 2612.

Outline Drawing



CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

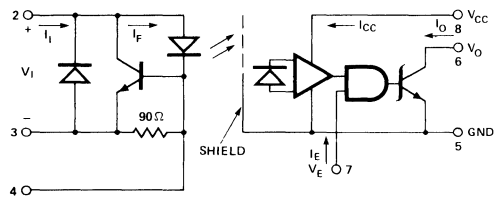
DC specifications are defined similar to TTL logic. The optocoupler ac and dc operational parameters are guaranteed from 0°C to 70°C allowing trouble-free interfacing with digital logic circuits. An input current of 5 mA will sink an eight gate fan-out (TTL) at the output.

The HCPL-2602/12 are useful as line receivers in high noise environments that conventional line receivers cannot tolerate. The higher LED threshold voltage provides improved immunity to differential noise and the internally shielded detector provides orders of magnitude improvement in common mode rejection with little or no sacrifice in speed.

Applications

- **Isolated Line Receiver**
- **Simplex/Multiplex Data Transmission**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Current Sensing**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**

Schematic



USE OF A 0.1 μF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED. (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_L	0	250	μA
Input Current, High Level	I_{IH}	5*	60	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

*The initial switching threshold is 5 mA or less. It is recommended that an input current between 6.3 mA and 10 mA be used to obtain best performance and to provide at least 20% LED degradation guardband.

Absolute Maximum Ratings

(No derating required up to 85°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to 85°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Forward Input Current – I_I ..... 60 mA
Reverse Input Current ..... 60 mA
Supply Voltage – V_{CC} (1 Minute Maximum) ..... 7 V
Enable Input Voltage – V_E ..... 5.5 V
(Not to exceed V_{CC} by more than 500 mV)
Output Collector Current – I_O ..... 25 mA
Output Collector Power Dissipation ..... 40 mW
Output Collector Voltage – V_O** ..... 7 V
Input Current, Pin 4 ..... ±10 mA

**Selection for higher output voltages up to 20 V is available.

Electrical Characteristics

Over recommended temperature (T_A = 0°C to +70°C) unless otherwise specified. See note 1.

Parameter	Sym.	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}		8	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_I = 250 µA, V_E = 2.0 V	1	
Low Level Output Voltage	V_{OL}		0.4	0.6	V	V_{CC} = 5.5 V, I_I = 5 mA, V_E = 2.0 V, I_{OL} (Sinking) = 13 mA	2, 4, 13	
High Level Supply Current	I_{CCH}		7.5	10	mA	V_{CC} = 5.5 V, I_I = 0 mA, V_E = 0.5 V		
Low Level Supply Current	I_{CCL}		10	13	mA	V_{CC} = 5.5 V, I_I = 10 mA, V_E = 0.5 V		
High Level Enable Current	I_{EH}		-0.8		mA	V_{CC} = 5.5 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}		-1.1	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5 V		
High Level Enable Voltage	V_{EH}	2.0			V			10
Low Level Enable Voltage	V_{EL}			0.8	V			
Input Voltage	V_I		2.0	2.4	V	I_I = 5 mA	3	
			2.3	2.7		I_I = 60 mA		
Input Reverse Voltage	V_R		0.75	0.95	V	I_R = 5 mA		
Input Capacitance	C_{IN}		60		pF	V_I = 0, f = 1 MHz		
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min T_A = 25°C		2
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		2
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		2

*All typicals at V_{CC} = 5 V, T_A = 25°C.

Notes:

1. Bypassing of the power supply line is required, with a 0.1 µF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 14. The power supply bus for the optocoupler(s) should be separate from the bus for any active loads.
2. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
3. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
4. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
5. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.

Switching Specifications

Over recommended temperature (T_A = 0°C to +70°C), V_{CC} = 5 V, I_I = 7.5 mA, unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}			45	75	ns	T_A = 25°C		5, 6, 7	3
					100	ns				
Propagation Delay Time to Low Output Level	t_{PHL}			55	75	ns	T_A = 25°C		5, 6, 8	4
					100	ns				
Pulse Width Distortion	$\lvert t_{PHL}-t_{PLH} \rvert$			14		ns	R_L = 350 Ω, C_L = 15 pF			
Output Rise Time (10-90%)	t_r			20		ns			11	
Output Fall Time (90-10%)	t_f			15		ns			11	
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}			30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V		9, 10	5
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}			25		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V		9. 10	6
Common Mode Transient Immunity at High Output Level	$\lvert CM_H \rvert$	HCPL-2602	1000	10,000		V/μs	V_{CM} = 50 V	$V_{O(MIN)}$ = 2 V, R_L = 350 Ω, I_I = 0 mA, T_A = 25°C	12	7, 9
		HCPL-2612	3500				V_{CM} = 300 V			
Common Mode Transient Immunity at Low Output Level	$\lvert CM_L \rvert$	HCPL-2602	1000	10,000		V/μs	V_{CM} = 50 V	$V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, I_I = 7.5 mA, T_A = 25°C	12	8, 9
		HCPL-2612	3500				V_{CM} = 300 V			

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L (IO1)	≥ 7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L (IO2)	≥ 7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

7. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
8. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} < 0.8 V).
9. For sinusoidal voltages,

$$\left(\frac{\lvert dv_{CM} \rvert}{dt}\right)_{max} = \pi f_{CM} V_{CM}\,(p\text{-}p)$$

10. No external pull up is required for a high logic state on the enable input.

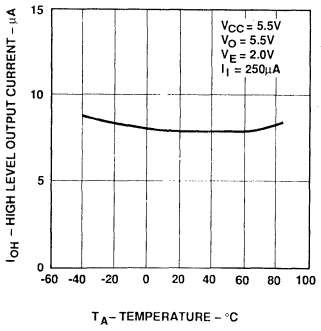


Figure 1. High Level Output Current vs. Temperature.

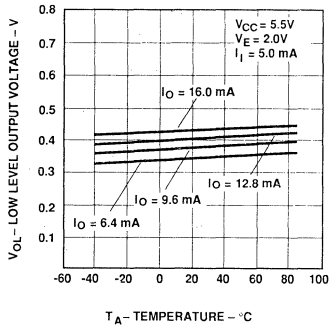


Figure 2. Low Level Output Voltage vs. Temperature.

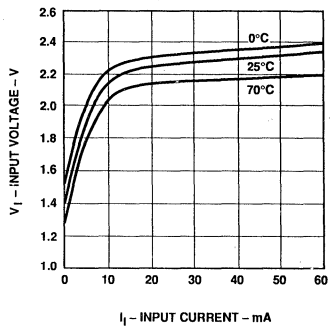


Figure 3. Input Characteristics.

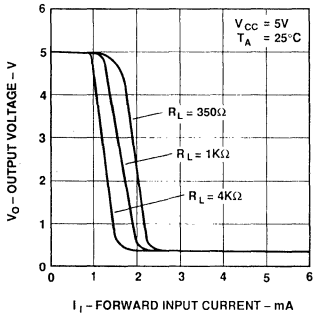


Figure 4. Output Voltage vs. Forward Input Current.

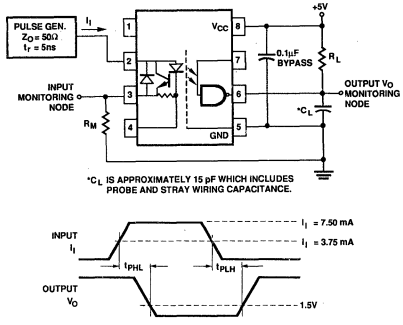


Figure 5. Test Circuit for t_{PHL} and t_{PLH}.

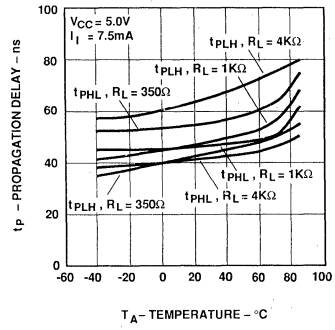


Figure 6. Propagation Delay vs. Temperature.

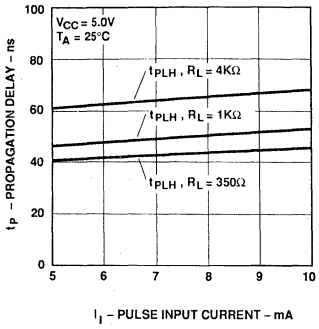


Figure 7. Propagation Delay (t_{PLH}) vs. Pulse Input Current.

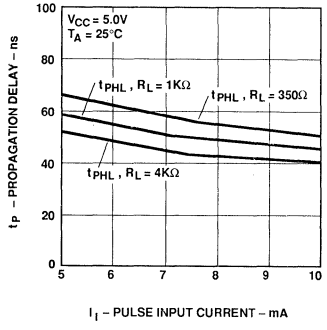
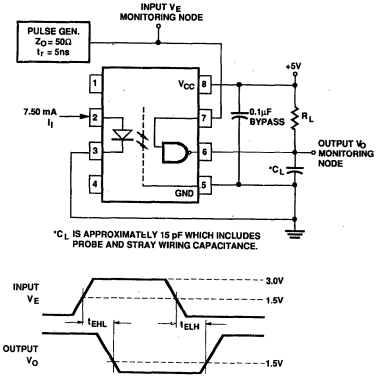


Figure 8. Propagation Delay (t_{PHL}) vs. Pulse Input Current.



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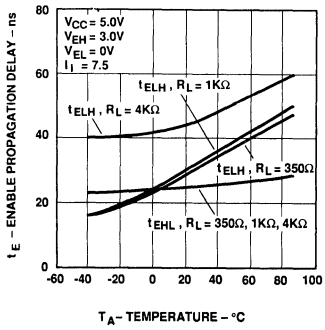


Figure 10. Enable Propagation Delay vs. Temperature.

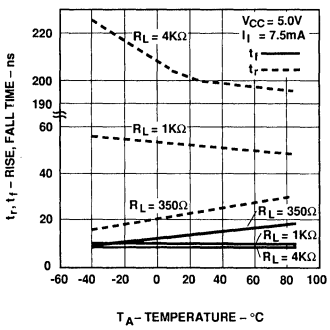
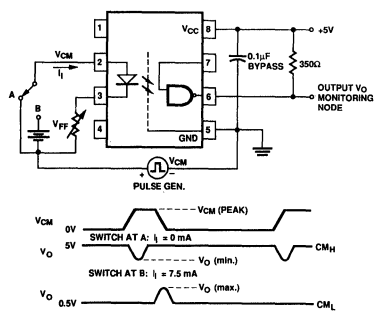


Figure 11. Rise and Fall Time vs. Temperature.



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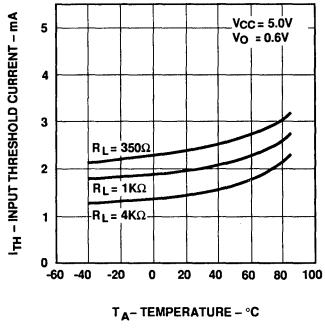


Figure 13. Input Threshold Current vs. Temperature.

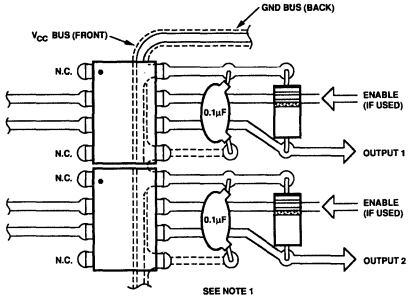


Figure 14. Recommended Printed Circuit Board Layout.

Using the HCPL-2602/12 Line Receiver Optocouplers

The primary objectives to fulfill when connecting an optocoupler to a transmission line are to provide a minimum, but not excessive, LED current and to properly terminate the line. The internal regulator in the HCPL-2602/12 simplifies this task. Excess current from variable drive conditions such as line length variations, line driver differences and power supply fluctuations are shunted by the regulator. In fact, with the LED current regulated, the line current can be increased to improve the immunity of the system to differential-mode-noise and to enhance the data rate capability. The designer must keep in mind the 60 mA input current maximum rating of the HCPL-2602/12 in such cases, and may need to use series limiting or shunting to prevent overstress.

Design of the termination circuit is also simplified; in most cases the transmission line can simply be connected directly to the input terminals of the HCPL-2602/12 without the need for additional series or shunt resistors. If reversing line drive is used it may be desirable to use two HCPL-2602/12 or an external Schottky diode to optimize data rate.

Polarity Non-Reversing Drive

High data rates can be obtained with the HCPL-2602/12 with polarity non-reversing drive. Figure (a) illustrates how a 74S140 line driver can be used with the HCPL-2602/12 and shielded, twisted pair or coax cable without any additional components. There are some reflections due to the "active termination" but they do not interfere with circuit performance because the regulator clamps the line voltage. At longer line lengths t_{PLH} increases faster than t_{PHL} since the switching threshold is not exactly halfway between asymptotic line conditions. If optimum data rate is desired, a series resistor and peaking capacitor can be used to equalize t_{PLH} and t_{PHL}. In general, the peaking capacitance should be as large as possible; however, if it is too large it may keep the regulator from achieving turn-off during the negative (or zero) excursions of the input signal. A safe rule:

make $C \leq 16t$

where:
C = peaking capacitance in picofarads
t = data bit interval in nanoseconds

Polarity Reversing Drive

A single HCPL-2602/12 can also be used with polarity reversing drive (Figure b). Current reversal is obtained by way of the substrate isolation diode (substrate to collector). Some reduction of data rate occurs, however, because the substrate diode stores charge, which must be removed when the current changes to the forward direction. The effect of this is a longer t_{PHL}. This effect can be eliminated and data rate improved considerably by use of a Schottky diode on the input of the HCPL-2602/12.

For optimum noise rejection as well as balanced delays a split-phase termination should be used along with a flip-flop at the output (Figure c). The result of current reversal in split-phase operation is seen in Figure (c) with switches A and B both OPEN. The coupler inputs are then connected in ANTI-SERIES; however, because of the higher steady-state termination voltage, in comparison to the single HCPL-2602/12 termination, the forward current in the substrate diode is lower and consequently there is less junction charge to deal with when switching.

Closing switch B with A open is done mainly to enhance common mode rejection, but also reduces propagation delay slightly because line-to-line capacitance offers a slight peaking effect. With switches A and B both CLOSED, the shield acts as a current return path which prevents either input substrate diode from becoming reversed biased. Thus the data rate is optimized as shown in Figure (c).

Improved Noise Rejection

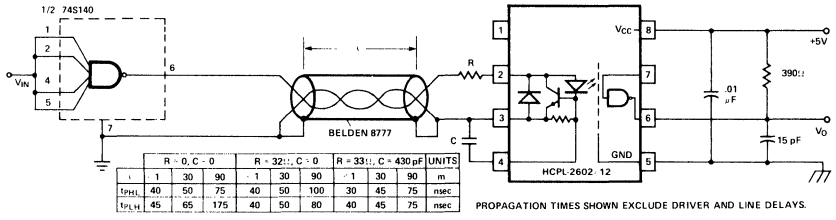
Use of additional logic at the output of two HCPL-2602/12s, operated in the split phase termination, will greatly improve system noise rejection in addition to balancing propagation delays as discussed earlier.

A NAND flip-flop offers infinite common mode rejection (CMR) for NEGATIVELY sloped common mode transients but requires $t_{PHL} > t_{PLH}$ for proper operation. A NOR flip-flop has infinite CMR for POSITIVELY sloped transients but requires $t_{PHL} < t_{PLH}$ for proper operation. An exclusive-OR flip-flop has infinite CMR for common mode transients of EITHER polarity and operates with either $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$.

With the line driver and transmission line shown in Figure (c), $t_{PHL} > t_{PLH}$, so NAND gates are preferred in the R-S flip-flop. A higher drive amplitude or different circuit configuration could make $t_{PHL} < t_{PLH}$, in which case NOR gates would be preferred. If it is not known whether $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$, or if the drive conditions may vary over the boundary for these conditions, the exclusive-OR flip-flop of Figure (d) should be used.

RS-422 and RS-423

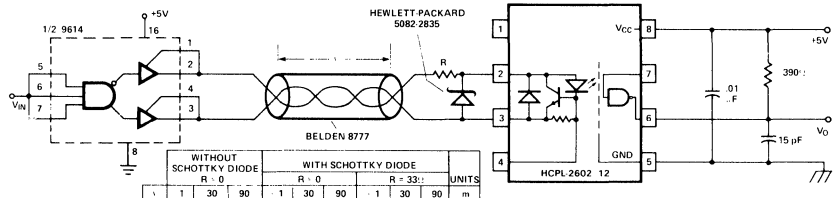
Line drivers designed for RS-422 and RS-423 generally provide adequate voltage and current for operating the HCPL-2602/12. Most drivers also have characteristics allowing the HCPL-2602/12 to be connected directly to the driver terminals. Worst case drive conditions, however, would require current shunting to prevent overstress of the HCPL-2602/12.



	R = 0, C = 0			R = 32Ω, C = 0			R = 33Ω, C = 430 pF			UNITS
ℓ	1	30	90	1	30	90	1	30	90	m
t_{PHL}	40	50	75	40	50	100	30	45	75	nsec
t_{PLH}	45	65	175	40	50	80	40	45	75	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

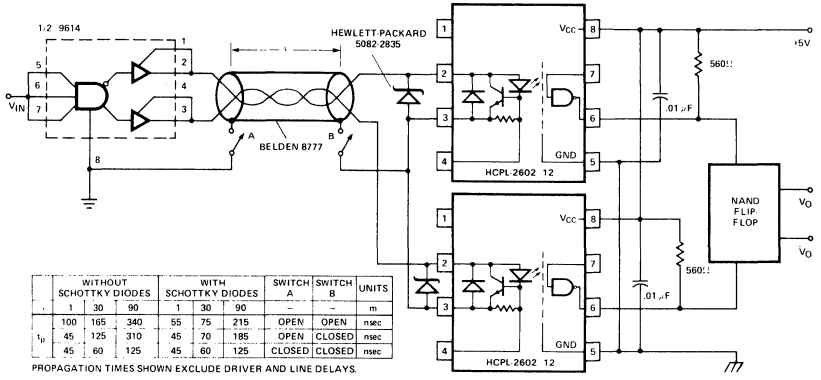
Figure a. Polarity Non-Reversing.



	WITHOUT SCHOTTKY DIODE	WITH SCHOTTKY DIODE					UNITS
	R = 0	R = 0		R = 33Ω			
ℓ	1	30	90	1	30	90	m
t_{PHL}	210	365	450	50	80	235	50	70	200	nsec
t_{PLH}	35	45	60	35	45	60	35	45	60	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

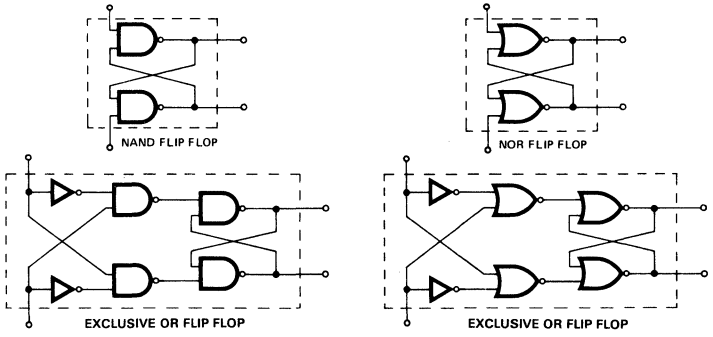
Figure b. Polarity Reversing, Single Ended.



	WITHOUT SCHOTTKY DIODES			WITH SCHOTTKY DIODES			SWITCH A	SWITCH B	UNITS
ℓ	1	30	90	1	30	90	–	–	m
t_p	100	165	340	55	75	215	OPEN	OPEN	nsec
	45	125	310	45	70	185	OPEN	CLOSED	nsec
	45	60	125	45	60	125	CLOSED	CLOSED	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

Figure c. Polarity Reversing, Split Phase.



NAND flip flop tolerates simultaneously HIGH inputs; NOR flip flop tolerates simultaneously LOW inputs; EXCLUSIVE-OR flip flop tolerates simultaneously HIGH OR LOW inputs without causing either of the outputs to change.

Figure d. Flip-Flop Configurations.

HEWLETT PACKARD

Dual Channel High CMR High Speed TTL Compatible Optocoupler

Technical Data

HCPL-2630
HCPL-2631
HCPL-4661

Features

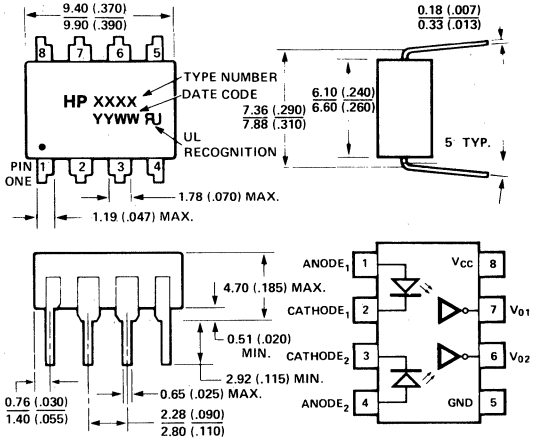
- **Internal Shield for High Common Mode Rejection (CMR)**
  HCPL-2631: 1000 V/μs @ V_{CM} = 50 V
  HCPL-4661: 5000 V/μs @ V_{CM} = 1000 V
- **High Density Packaging**
- **Low Input Current Capability: 5 mA**
- **High Speed: 10 MBd Typical**
- **LSTTL and TTL Compatible**
- **Guaranteed AC and DC Performance Over Temperature: 0°C to 70°C**
- **Recognized Under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 VAC, 1 Minute.**
- **VDE 0883 Approval Pending**
- **Hermetic Equivalent Device Available (HCPL-5630/1)**

Description

The HCPL-2630/HCPL-2631/4661 are dual channel optically coupled logic gates that combine GaAsP light emitting diodes and integrated high gain photodetectors. The photons are collected in the detector by a photodiode and the current is amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. Each circuit is temperature, current and voltage compensated. The internal shield provides a guaranteed common mode transient immunity specification of 1000 V/μs for the 2631, and 5000 V/μs with the HCPL-4661.

The unique design provides maximum AC and DC circuit isolation while achieving LSTTL and TTL compatibility. The optocoupler AC and DC operational parameters are guaranteed from 0°C to 70°C. The dual channel design minimizes space and results in increased convenience.

Outline Drawing



DIMENSIONS IN MILLIMETRES AND (INCHES).

The HCPL-2630/2631/4661 are recommended for high speed logic interfacing, input/output buffering, and for use as line receivers in environments that conventional line receivers cannot tolerate. The HCPL-2630/2631/4661 can be used for the digital programming of machine control systems, motors and floating power supplies. The internal shield makes the HCPL-2631/4661 ideal for use in extremely high ground or induced noise environments.

Applications

- **Isolation of High Speed Logic Systems**
- **Microprocessor System Interfaces**
- **Isolated Line Receiver**
- **Computer-Peripheral Interfaces**
- **Ground Loop Elimination**
- **Digital Isolation for A/D, D/A Conversion**

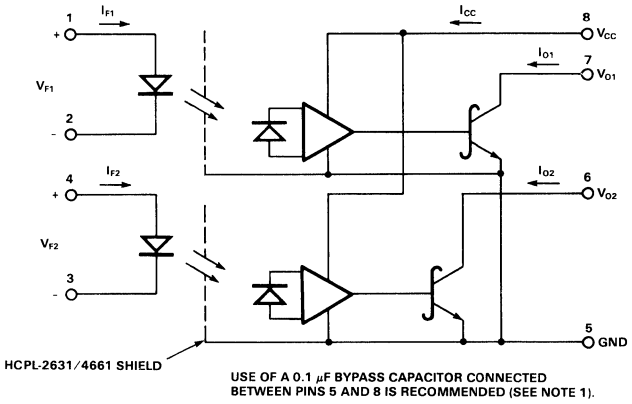


Figure 1. Schematic.

Recommended Operation Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}*	5	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		8	
Operating Temperature	T_A	0	70	°C

*The initial switching threshold is 5 mA or less. It is recommended that input current between 6.3 mA and 10 mA be used to obtain best performance and to provide at least a 20% LED degradation guardband.

Absolute Maximum Ratings

(No Derating Required up to 85°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)

Average Forward
Input Current (each channel, See note 2) ..... 15 mA
Reverse Input Voltage (each channel) ..... 5 V
Supply Voltage – V_{CC} (1 Minute Maximum) ..... 7 V
Output Collector Current – I_O (each channel) ..... 16 mA
Output Collector Voltage – V_O (each channel)** ..... 7 V
Output Collector Power Dissipation (each channel) ..... 60 mW

**Selection for higher output voltages up to 20 V is available.

Electrical Characteristics

Over recommended temperature (T_A = 0°C to +70°C) unless otherwise specified. See note 1.

Parameter	Sym.	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}		8	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 µA	2	3
Low Level Output Voltage	V_{OL}		0.4	0.6	V	V_{CC} = 5.5 V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	3, 5, 14	3
High Level Supply Current	I_{CCH}		10	15	mA	V_{CC} = 5.5 V, I_F = 0 mA (Both Channels)		
Low Level Supply Current	I_{CCL}		16	21	mA	V_{CC} = 5.5 V, I_F = 10 mA (Both Channels)		
Input Forward Voltage	V_F		1.5	1.75	V	T_A = 25°C	4	3
				1.80		I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA,		3
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz		3
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 10 mA	12	
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 Min T_A = 25°C		
Input-Input Leakage Current	I_{I-I}		0.005		µA	Relative Humidity = 45% t = 5 s, V_{I-I} = 500 V		5
Resistance (Input-Input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500 V		5
Capacitance (Input-Input)	C_{I-I}		0.25		pF	f = 1 MHz		
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		4
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to +70°C), V_{CC} = 5 V, I_F = 7.5 mA, unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}			45	75	ns	T_A = 25°C	R_L = 350 Ω C_L = 15 pF	6, 7, 8	3, 6
					100	ns				
Propagation Delay Time to Low Output Level	t_{PHL}			55	75	ns	T_A = 25°C		6, 7, 9	3, 7
					100	ns				
Pulse Width Distortion	$\|t_{PHL}-t_{PLH}\|$			14		ns				
Output Rise Time (10-90%)	t_r			20		ns			10	3
Output Fall Time (90-10%)	t_f			15		ns			10	3
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	HCPL-2630		100		V/μs	V_{CM} = 10 V	$V_{O(MIN)}$ = 2 V, R_L = 350 Ω, I_F = 0 mA, T_A = 25°C	11	3, 8, 10
		HCPL-2631	1000	10,000		V/μs	V_{CM} = 50 V			
		HCPL-4661	5000	10,000		V/μs	V_{CM} = 1000 V			
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	HCPL-2630		300		V/μs	V_{CM} = 10 V	$V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, I_F = 7.5 mA T_A = 25°C	11	3, 9, 10
		HCPL-2631	1000	10,000		V/μs	V_{CM} = 50 V			
		HCPL-4661	5000	10,000		V/μs	V_{CM} = 1000 V			

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L (IO1)	≥ 7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L (IO2)	≥ 7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

Notes:

1. Bypassing of the power supply line is required, with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm. The power supply bus for the optocoupler(s) should be separate from the bus for any active loads.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 15 mA.
3. Each channel.
4. Measured between pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
5. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
6. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
7. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
8. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
9. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} > 0.8 V).
10. For sinusoidal voltages,

$$\left(\frac{|dv_{CM}|}{dt}\right)_{max} = \pi f_{CM} V_{CM} \text{ (p-p)}$$

11. As illustrated in Figure 15 the V_{CC} and GND traces can be located between the input and the output leads of the HCPL-2630/2631/4661 to provide additional noise immunity at the compromise of insulation capability.

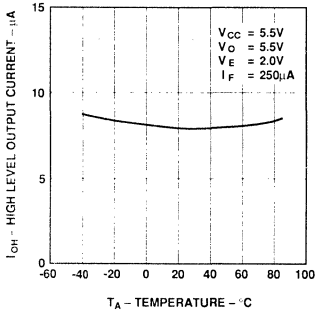


Figure 2. High Level Output Current vs. Temperature.

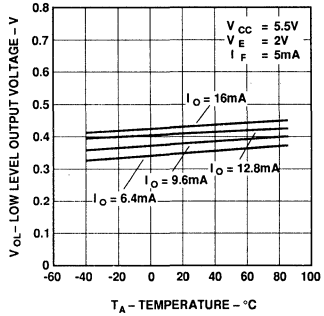


Figure 3. Low Level Output Voltage vs. Temperature.

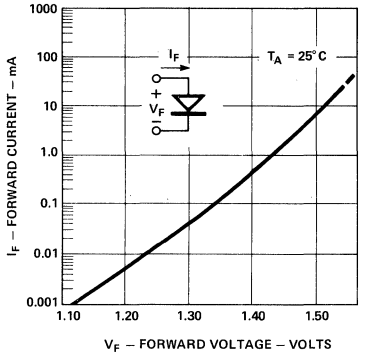


Figure 4. Input Diode Forward Characteristic.

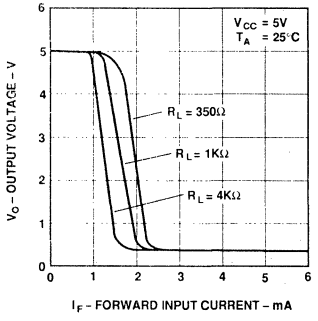


Figure 5. Output Voltage vs. Forward Input Current.

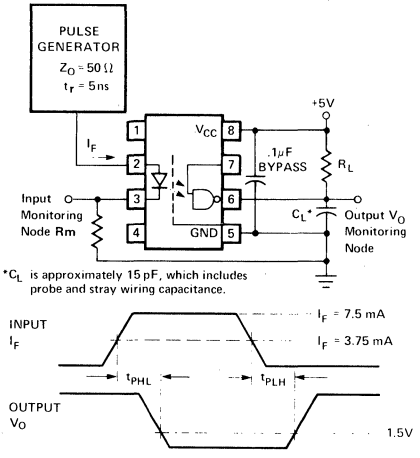


Figure 6. Test Circuit for t_{PHL} and t_{PLH} (See Note 3).

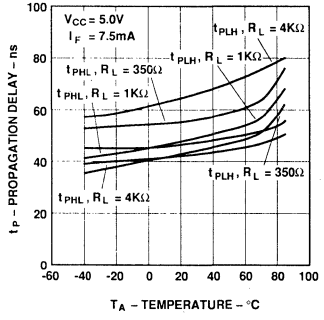


Figure 7. Propagation Delay vs. Temperature.

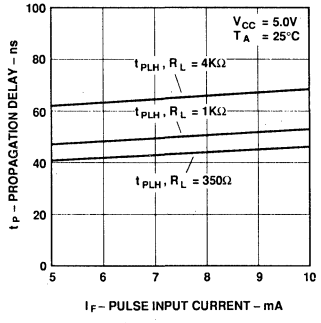


Figure 8. Propagation Delay (t_{PLH}) vs. Pulse Input Current.

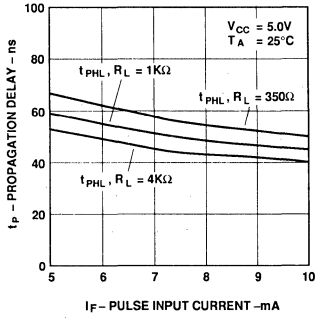


Figure 9. Propagation Delay (t_{PHL}) vs. Pulse Input Current.

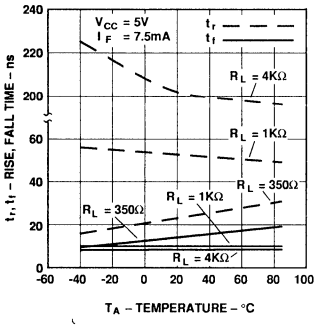


Figure 10. Rise and Fall Time vs. Temperature.

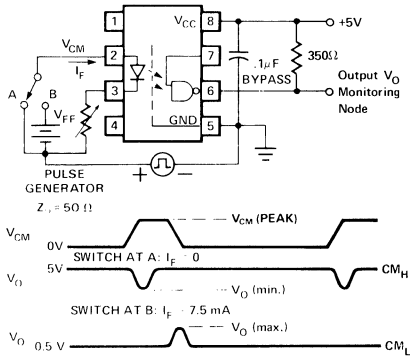


Figure 11. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

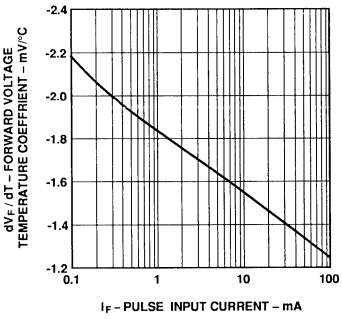
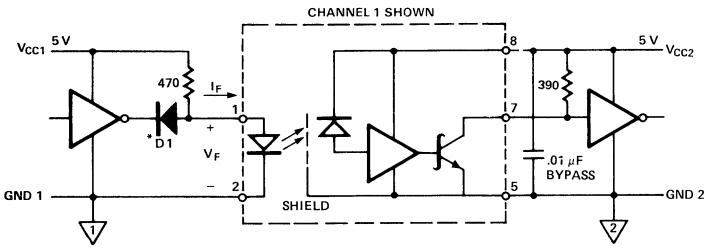


Figure 12. Temperature Coefficient of Forward Voltage vs. Input Current.



*DIODE D1 (1N916 OR EQUIVALENT) IS NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

Figure 13. Recommended TTL/ LSTTL to TTL/LSTTL Interface Circuit.

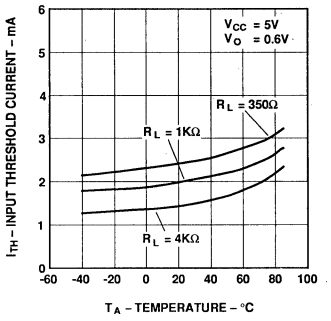


Figure 14. Input Threshold Current vs. Temperature.

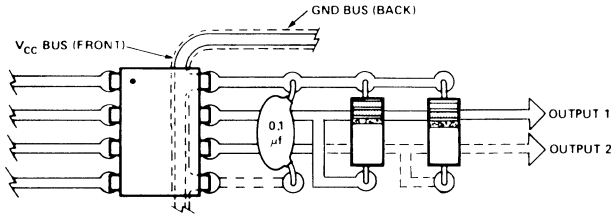


Figure 15. Recommended Printed Circuit Board Layout. See notes 1, 11.

OPTOCOUPLERS

HEWLETT PACKARD

Small Outline High CMR, High Speed, Logic Gate Optocouplers

Technical Data

HCPL-0600
HCPL-0601
HCPL-0611

Features

- **Surface Mountable**
- **Industry Standard SOIC-8 Footprint**
- **Compatible with Infrared Vapor Phase Reflow and Wave Soldering Processes**
- **Internal Shield for High Common Mode Rejection (CMR)**
  HCPL-0601: 1000 V/μs at V_{CM} = 50 V
  HCPL-0611: 5000 V/μs at V_{CM} = 1000 V
- **High Speed: 10 Mbd Typical**
- **LSTTL/TTL Compatible**
- **Low Input Current Required: 5 mA**
- **Guaranteed ac and dc Performance Over Temperature: 0°C to 70°C**
- **Strobable Output**
- **Recognized under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltage of 2500 Vac, 1 Minute**

Description

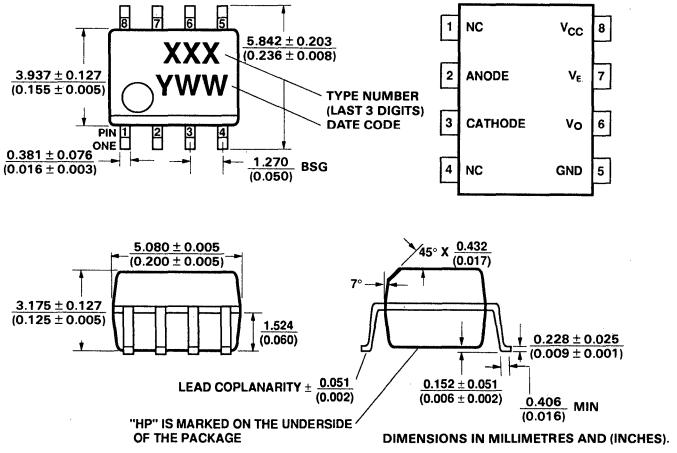
These small outline high CMR, high speed, logic gate optocouplers are single channel devices in an industry standard SOIC-8 footprint. They are electrically equivalent to the following HP optocouplers:

Small Outline	Standard DIP
HCPL-0600	6N137
HCPL-0601	HCPL-2601
HCPL-0611	HCPL-2611

The SOIC-8 package does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

The HCPL-0600/01/11 optically coupled gates combine a GaAsP light emitting diode and an

Outline Drawing*



*See notes, following page.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

integrated high gain photon detector. An enable input allows the detector to be strobed. The output of the detector I.C. is an open-collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification for the HCPL–0601/11.

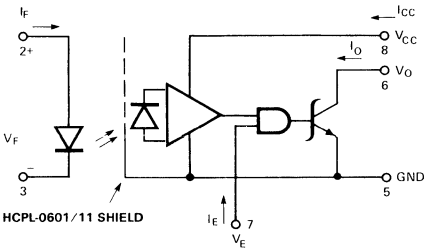
This unique design provides maximum ac and dc circuit isolation while achieving TTL compatibility. The optocoupler ac and dc operational parameters are guaranteed from 0°C to 70°C allowing trouble free system performance.

The HCPL-0600/01/11 are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Applications

- **Isolated Line Receiver**
- **Simplex/Multiplex Data Transmission**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Switching Power Supply**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**

Schematic



A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5 (See Note 1).

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}	0	250	μA
Input Current, High Level	I_{FH}*	5	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

*The initial switching threshold is 5 mA or less. It is recommended that an input current between 6.3 mA and 10 mA be used to obtain best performance and to provide at least 20% LED degradation guardband.

Absolute Maximum Ratings

(No Derating Required up to 85°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to 85°C
Infrared and Vapor Phase Reflow Temperature ..... 215°C for 90 s
Forward Input Current – I_F (see Note 2) ..... 20 mA
Reverse Input Voltage ..... 5 V
Supply Voltage – V_{CC} ..... 7 V (1 Minute Maximum)
Enable Input Voltage – V_E ..... 5.5 V
(Not to exceed V_{CC} by more than 500 mV)
Output Collector Current – I_O ..... 50 mA
Output Collector Power Dissipation ..... 85 mW
Output Collector Voltage – V_O (see Note 12) ..... 7 V

Electrical Characteristics

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. (See note 1.)

Parameter	Symbol	Min.	Typ.*	Max.	Units	Conditions	Fig.	Note
High Level Output Current	I_{OH}		8	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 µA, V_E = 2.0 V	1	
Low Level Output Voltage	V_{OL}		0.4	0.6	V	V_{CC} = 5.5 V, I_F = 5 mA, V_E = 2.0 V, I_{OL} (Sinking) = 13 mA	2, 4, 14	
High Level Supply Current	I_{CCH}		7.5	10	mA	V_{CC} = 5.5 V, I_F = 0 mA, V_E = 0.5 V		
Low Level Supply Current	I_{CCL}		10	13	mA	V_{CC} = 5.5 V, I_F = 10 mA, V_E = 0.5 V		
High Level Enable Current	I_{EH}		-0.8		mA	V_{CC} = 5.5 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}		-1.1	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5 V		
High Level Enable Voltage	V_{EH}	2.0			V			11
Low Level Enable Voltage	V_{EL}			0.8	V			
Input Forward Voltage	V_F		1.5	1.75 1.85	V	T_A = 25°C I_F = 10 mA	3, 13	
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA		
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz		
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 10 mA		
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 MIN		3
Resistance (Input-Output)	R_{I-O}		10^{14}		Ω	V_{I-O} = 500 V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

*All typicals at T_A = 25°C, V_{CC} = 5 V.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 7.5 mA unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}			45	75	ns	T_A = 25°C	5, 6, 7, 8	4
					100	ns			
Propagation Delay Time to Low Output Level	t_{PHL}			55	75	ns	T_A = 25°C	5, 6, 7, 9	5
					100	ns			
Pulse Width Distortion	$\lvert t_{PHL}-t_{PLH} \rvert$			14		ns	R_L = 350 Ω		4, 5
Output Rise Time (10-90%)	t_r			20		ns	C_L = 15 pF	11	
Output Fall Time (90-10%)	t_f			15		ns		11	
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}			30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	9, 10	6
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}			25		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	10, 11	7
Common Mode Transient Immunity at High Output Level	$\lvert CM_H \rvert$	HCPL-0600		100		V/μs	V_{CM} = 10 V; $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, I_F = 0 mA, T_A = 25°C	13	8, 10
		HCPL-0601	1000	10,000			V_{CM} = 50 V		
		HCPL-0611	5,000				V_{CM} = 1000 V		
Common Mode Transient Immunity at Low Output Level	$\lvert CM_L \rvert$	HCPL-0600		300		V/μs	V_{CM} = 10 V; $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, T_A = 25°C	13	9, 10
		HCPL-0601	1000	10,000			V_{CM} = 50 V		
		HCPL-0611	5,000				V_{CM} = 1000 V		

*All typicals are at V_{CC} = 5 V, T_A = 25°C.

Notes:

1. Bypassing of the power supply line is required with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler. The power supply bus for the optocoupler(s) should be separate from the bus for any active loads.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
7. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
8. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
9. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} < 0.8 V).
10. For sinusoidal voltages,

$$\left(\frac{\lvert dv_{CM} \rvert}{dt}\right)_{max} = \pi f_{CM} V_{CM} \text{ (p-p)}$$

11. No external pull up is required for a high logic state on the enable input.
12. Selection for higher output voltages up to 20 V is available.

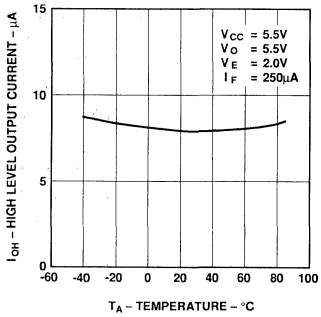


Figure 1. High Level Output Current vs. Temperature.

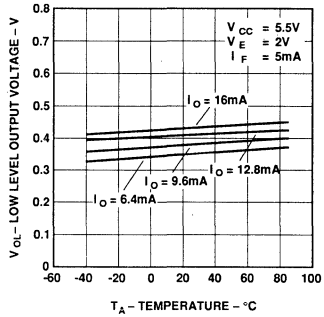


Figure 2. Low Level Output Voltage vs. Temperature.

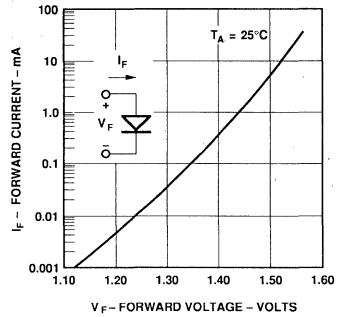


Figure 3. Input Diode Forward Characteristic.

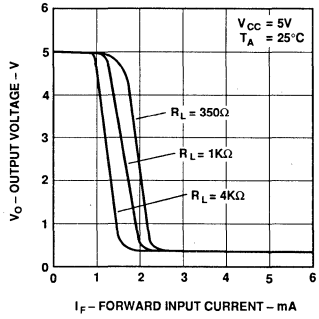


Figure 4. Output Voltage vs. Forward Input Current.

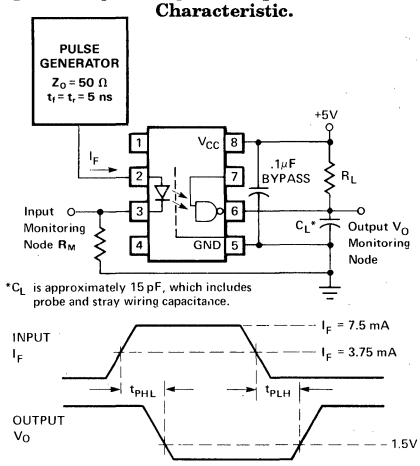


Figure 5. Test Circuit for t_{PHL} and t_{PLH}.

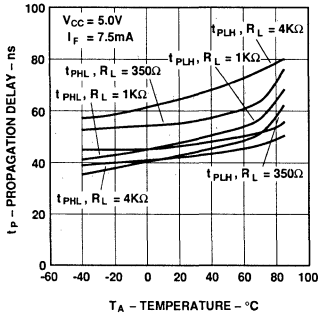


Figure 6. Propagation Delay vs. Temperature.

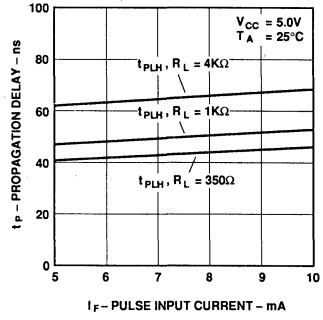


Figure 7. Propagation Delay (t_{PLH}) vs. Pulse Input Current.

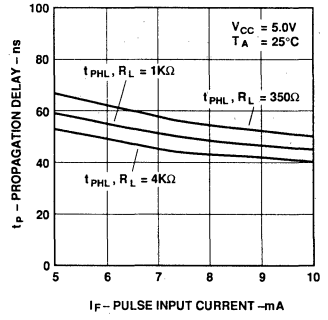


Figure 8. Propagation Delay (t_{PHL}) vs. Pulse Input Current.

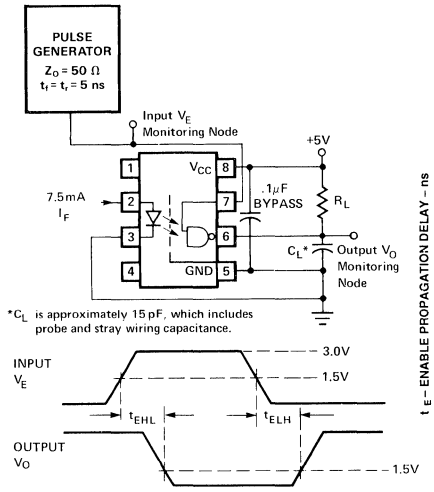


Figure 9. Test Circuit for t_{EHL} and t_{ELH}.

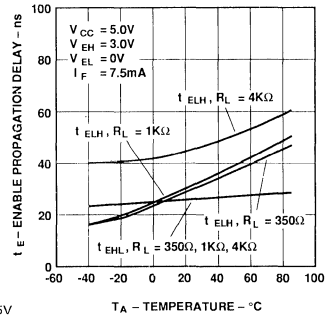


Figure 10. Enable Propagation Delay vs. Temperature.

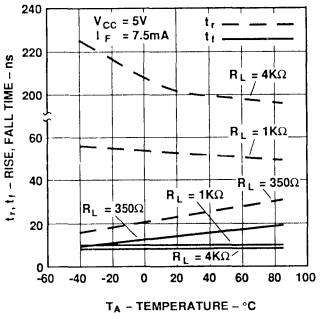


Figure 11. Rise and Fall Time vs. Temperature.

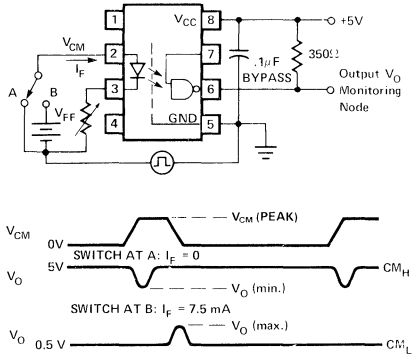


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

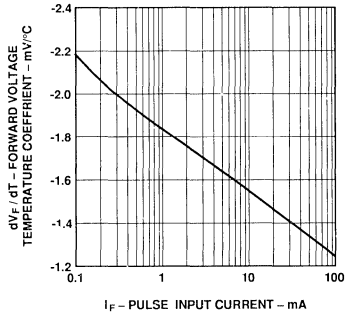


Figure 13. Temperature Coefficient of Forward Voltage vs. Input Current.

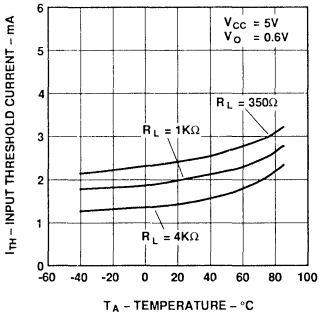


Figure 14. Input Threshold Current vs. Temperature.

HEWLETT PACKARD

High Speed Optocouplers

Technical Data

6N135
6N136
HCPL-2502
HCPL-4502
HCPL-4503

Features

- **Very High Common Mode Transient Immunity: 15000 V/μs at V_{CM} = 1500 V Guaranteed (HCPL-4503)**
- **High Speed: 1 Mb/s**
- **TTL Compatible**
- **Guaranteed ac and dc Performance Over Temperature: 0°C to 70°C**
- **Open Collector Output**
- **Recognized under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 Vac, 1 Minute and 5000 Vac, 1 Minute (Option 020).**
- **VDE 0883 Approval Pending**

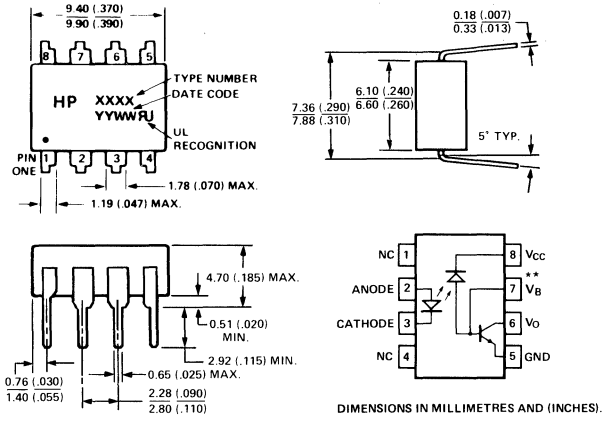
Description

These diode-transistor optocouplers use an insulating layer between the light emitting diode and an integrated photon detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

The 6N135 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the 6N135 is 7% minimum at I_F = 16 mA.

The 6N136 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the 6N136 is 19% minimum at I_F = 16 mA.

Outline Drawing



DIMENSIONS IN MILLIMETRES AND (INCHES).

*See notes, following page.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

The HCPL-2502 is suitable for use in applications where matched or known CTR is desired such as in the feedback path of switch-mode power supplies. CTR is 15 to 22% at I_F = 16mA.

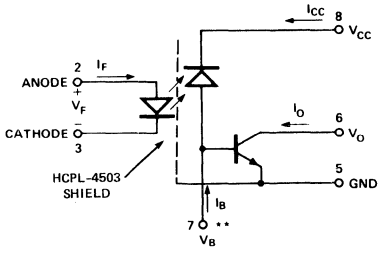
The HCPL-4502 provides the electrical and switching performance of the 6N136 with increased ESD protection.

The HCPL-4503 is an HCPL-4502 with increased common mode transient immunity of 15000 V/μs minimum at V_{CM} = 1500 guaranteed.

Applications

- **Video Signal Isolation**
- **Line Receivers** – High common mode transient immunity (>1000 V/μs) and low input-output capacitance (0.6 pF).
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Slow Phototransistor Isolators** – Pins 2-7 of the 6N135/6 series conform to pins 1-6 of 6 pin phototransistor couplers. Pin 8 can be tied to any available bias voltage of 1.5 V to 30 V for high speed operation.
- **Replace Pulse Transformers** – Save board space and weight
- **Analog Signal Ground Isolation** – Integrated photon detector provides improved linearity over phototransistor type.

Schematic



**NOTE: FOR HCPL-4502/3, PIN 7 IS NOT CONNECTED

Absolute Maximum Ratings

Storage Temperature * ..... -55°C to +125°C
Operating Temperature* ..... -55°C to 100°C
Lead Solder Temperature* ..... 260°C for 10s
(1.6 mm below seating plane)
Average Input Current – I_F* .....25 mA[1]
Peak Input Current – I_F* ..... 50 mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F* ..... 1.0 A
(≤1 μs pulse width, 300 pps)
Reverse Input Voltage – V_R* (Pin 3-2) ..... 5 V
Input Power Dissipation* ..... 45 mW[3]
Average Output Current – I_O* (Pin 6) ..... 8 mA
Peak Output Current* ..... 16 mA
Emitter-Base Reverse Voltage *.....5 V
(Pin 5-7, except HCPL-4502/3)
Output Voltage* – V_O (Pin 6-5) .....-0.5 V to 15 V
Supply Voltage* – V_{CC} (Pin 8-5) ..... -0.5 V to 15 V
Output Voltage – V_O (Pin 6-5) .....-0.5 V to 20 V
Supply Voltage – V_{CC} (Pin 8-5) ..... -0.5 V to 30 V
Base Current – I_B* (Pin 7, except HCPL-4502/3) ..... 5 mA
Output Power Dissipation*.....100 mW[4]

*JEDEC Registered Data (The HCPL-2502 and HCPL-4502/3 are not registered.)

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. See note 13.

Parameter	Symbol	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	6N135	7	18	50	%	T_A = 25°C, V_O = 0.4 V; I_F = 16 mA, V_{CC} = 4.5 V	1, 2 4	5, 11
			5	19			V_O = 0.5 V		
		6N136 HCPL-4502 HCPL-4503	19	24	50	%	T_A = 25°C, V_O = 0.4 V		
			15	25			V_O = 0.5 V		
		HCPL-2502	15	18	22	%	T_A = 25°C, V_O = 0.4 V		
Logic Low Output Voltage	V_{OL}	6N135		0.1	0.4	V	T_A = 25°C, I_O = 1.1 mA; I_F = 16 mA, V_{CC} = 4.5 V		
					0.5		I_O = 0.8 mA		
		6N136 HCPL-2502 HCPL-4502 HCPL-4503		0.1	0.4	V	T_A = 25°C, I_O = 3.0 mA		
					0.5		I_O = 2.4 mA		
Logic High Output Current	I_{OH}*			0.003	0.5	µA	T_A = 25°C, V_O = V_{CC} = 5.5 V; I_F = 0 mA	6	
				0.01	1	µA	T_A = 25°C, V_O = V_{CC} = 15.0 V; I_F = 0 mA		
					50				
Logic Low Supply Current	I_{CCL}			50	200	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V		13
Logic High Supply Current	I_{CCH}*			0.02	1	µA	T_A = 25°C, I_F = 0 mA, V_O = Open, V_{CC} = 15 V		13
					2				
Input Forward Voltage	V_F*			1.5	1.7	V	T_A = 25°C, I_F = 16 mA	3	
					1.8				
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10 µA		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16 mA		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0 V		
Input-Output Insulation Voltage	V_{ISO}		2500			V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C		6
		OPT. 020	5000			V_{RMS}			
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc		6
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		6
Transistor DC Current Gain	h_{FE}			150			V_O = 5 V, I_O = 3 mA		
				130			V_O = 0.4 V, Ib = 20 µA		

*For JEDEC registered parts. **All typicals at T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}*	6N135		0.2	1.5	µs	T_A = 25°C, R_L = 4.1 kΩ	5, 9, 11	8, 9
					2.0				
		6N136 HCPL-2502 HCPL-4502 HCPL-4503		0.2	0.8		T_A = 25°C, R_L = 1.9 kΩ		
					1.0				
Propagation Delay Time to Logic High at Output	t_{PLH}*	6N135		1.3	1.5	µs	T_A = 25°C, R_L = 4.1 kΩ	5, 9, 11	8, 9
					2.0				
		6N136 HCPL-2502 HCPL-4502 HCPL-4503		0.6	0.8		T_A = 25°C, R_L = 1.9 kΩ		
					1.0				
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	6N135		1		kV/µs	R_L = 4.1 kΩ, I_F = 0 mA, T_A = 25°C, V_{CM} = 10 V_{p-p}	10	7, 8, 9
		6N136 HCPL-2502 HCPL-4502		1			R_L = 1.9 kΩ		
		HCPL-4503	15	30			R_L = 1.9 kΩ, I_F = 0 mA, T_A = 25°C, V_{CM} = 1500 V_{p-p}		
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	6N135		1		kV/µs	R_L = 4.1 kΩ, I_F = 16 mA, T_A = 25°C, V_{CM} = 10 V_{p-p}	10	7, 8, 9
		6N136 HCPL-2502 HCPL-4502		1			R_L = 1.9 kΩ		
		HCPL-4503	15	30			R_L = 1.9 kΩ, I_F = 16 mA, T_A = 25°C, V_{CM} = 1500 V_{p-p}		
Bandwidth	BW			9		MHz	See Test Circuit	7, 8	10

*For JEDEC registered parts.
**All typicals at T_A = 25°C.

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C.
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
8. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
9. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull-up resistor.
10. The frequency at which the ac output voltage is 3 dB below its mid-frequency value.
11. The JEDEC registration for the 6N136 specifies a minimum CTR of 15%. HP guarantees a minimum CTR of 19%.
12. See Option 020 data sheet for more information.
13. Use of a 0.1 µf bypass capacitor connected between pins 5 and 8 is recommended.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(I01)	≥ 7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(I02)	≥ 7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Insulation thickness between emitter and detector
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (Per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

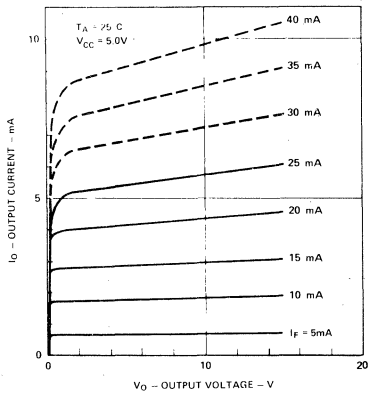


Figure 1. DC and Pulsed Transfer Characteristics.

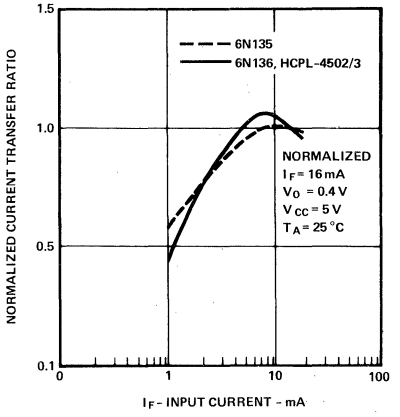


Figure 2. Current Transfer Ratio vs. Input Current.

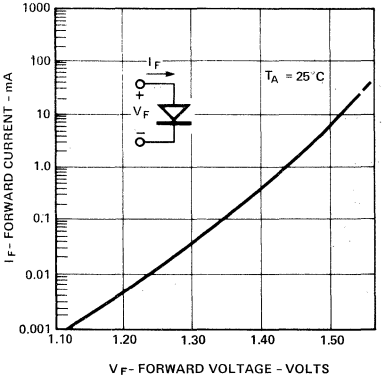


Figure 3. Input Current vs. Forward Voltage.

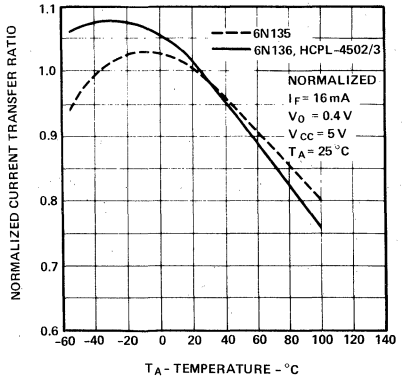


Figure 4. Current Transfer Ratio vs. Temperature.

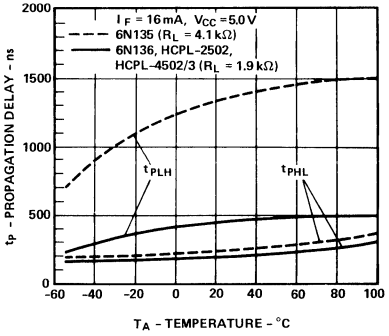


Figure 5. Propagation Delay vs. Temperature.

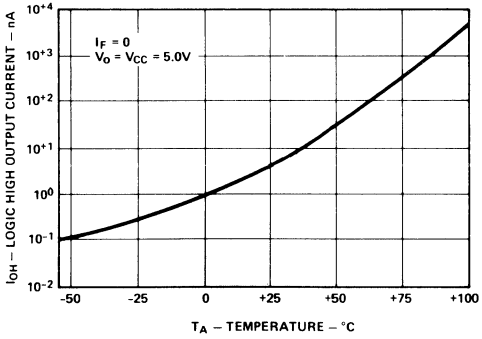


Figure 6. Logic High Output Current vs. Temperature.

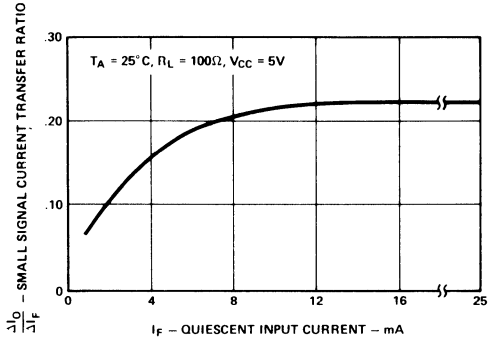
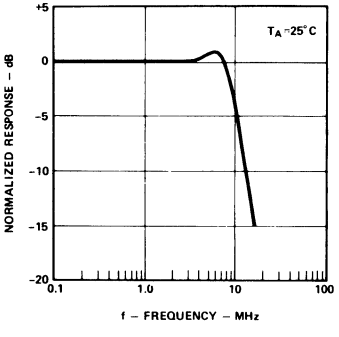


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.



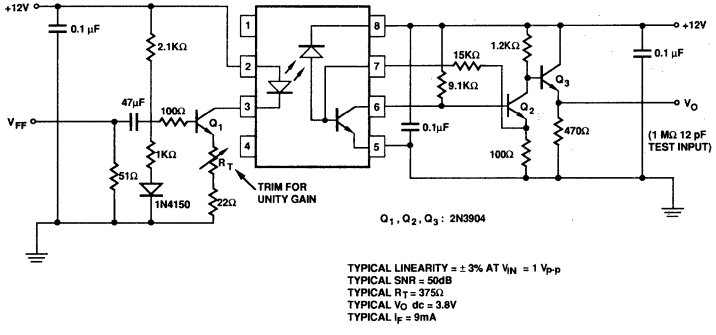


Figure 8. Frequency Response.

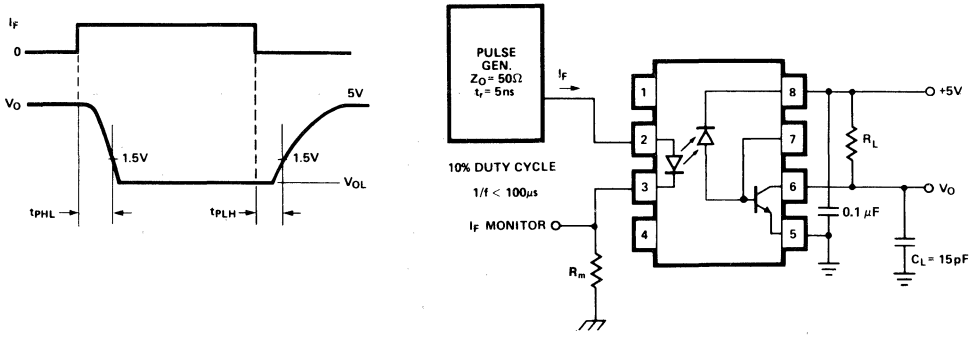


Figure 9. Switching Test Circuit.*

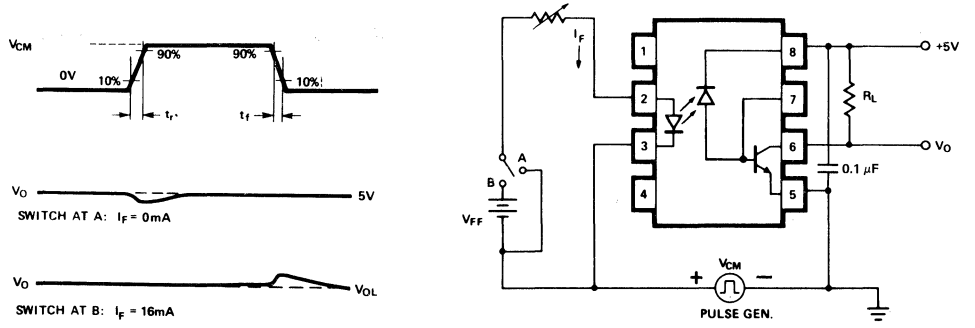


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

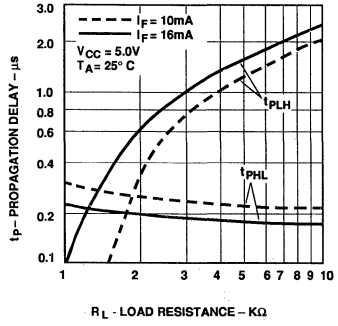


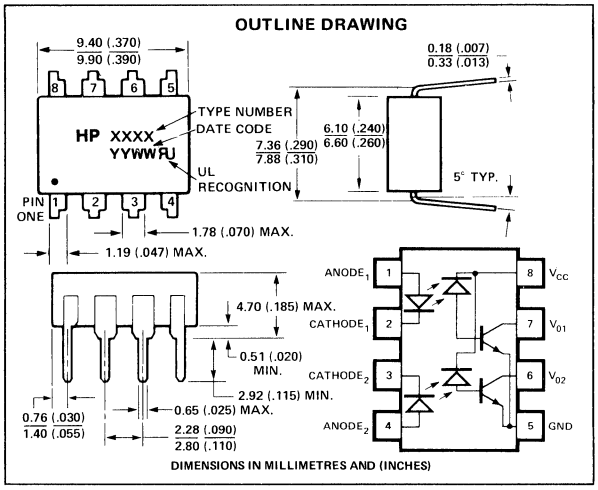
Figure 11. Propagation Delay Time vs. Load Resistance.

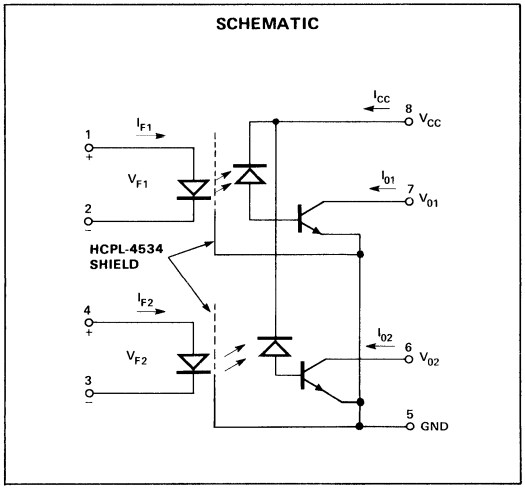
*JEDEC Registered Data

HEWLETT PACKARD

DUAL HIGH SPEED OPTOCOUPLER

HCPL-2530
HCPL-2531
HCPL-4534





Features

- **HIGH SPEED: 1 Mb/s**
- **TTL COMPATIBLE**
- **VERY HIGH COMMON MODE TRANSIENT IMMUNITY: 15000 V/μs @ V_{CM} = 1500 V GUARANTEED (HCPL-4534)**
- **HIGH DENSITY PACKAGING**
- **3 MHz BANDWIDTH**
- **OPEN COLLECTOR OUTPUTS**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **VDE 0883 APPROVAL AVAILABLE**
- **MIL-STD-1772 VERSION AVAILABLE (HCPL-5530/31)**

Description

These dual optocouplers contain a pair of light emitting diodes and integrated photo detectors with electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collectors increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

The HCPL-2530 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the -2530 is 7% minimum at I_F = 16 mA.

The HCPL-2531 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the -2531 is 19% minimum at I_F = 16 mA.

The HCPL-4534 is an HCPL-2531 with increased common mode transient immunity of 15000 V/μs minimum at V_{CM} = 1500 V guaranteed.

Applications

- **Line Receivers** — High common mode transient immuni (>1000V/μs) and low input-output capacitance (0.6pF).
- **High Speed Logic Ground Isolation** — TTL/TTL, TT LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Pulse Transformers** — Save board space and weigh
- **Analog Signal Ground Isolation** — Integrated photon d tector provides improved linearity over phototransistor type.
- **Polarity Sensing.**
- **Isolated Analog Amplifier** — Dual channel packaging enhances thermal tracking.

Absolute Maximum Ratings

Storage Temperature . . . . . -55°C to +125°C
Operating Temperature . . . . . -55°C to +100°C
Lead Solder Temperature . . . . . 260°C for 10s
(1.6mm below seating plane)
Average Input Current — I_F (each channel) . . . . . 25mA[1]
Peak Input Current — I_F (each channel) . . . . . 50mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — I_F (each channel) . . . . 1.0 A
(≤1μs pulse width, 300pps)
Reverse Input Voltage — V_R (each channel) 5V
Input Power Dissipation (each channel) . . . . . 45mW[3]
Average Output Current — I_O (each channel) 8mA
Peak Output Current — I_O (each channel) 16mA
Supply Voltage - V_{CC} (Pin 8-5) . . . . . - 0.5V to 30V
Output Voltage - V_O (Pin 7,6-5) . . . . . - 0.5V to 20V
Output Power Dissipation (each channel) . . . . . 35mW[4]

See notes, following page.

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. See note 13.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions			Fig.	Note
Current Transfer Ratio	CTR	HCPL-2530	7	18	50	%	T_A = 25°C	V_O = 0.4 V	I_F = 16 mA, V_{CC} = 4.5 V	1, 2 4	5, 6
			5					V_O = 0.5 V			
		HCPL-2531 HCPL-4534	19	24	50	%	T_A = 25°C	V_O = 0.4 V			
			15					V_O = 0.5 V			
Logic Low Output Voltage	V_{OL}	HCPL-2530		0.1	0.4	V	T_A = 25°C	I_O = 1.1 mA	I_F = 16 mA, V_{CC} = 4.5 V	1	5
					0.5			I_O = 0.8 mA			
		HCPL-2531 HCPL-4534		0.1	0.4	V	T_A = 25°C	I_O = 3.0 mA			
					0.5			I_O = 2.4 mA			
Logic High Output Current	I_{OH}			0.003	0.5	µA	T_A = 25°C	V_O = V_{CC} = 5.5 V	I_F = 0 mA	6	5
							T_A = 25°C	V_O = V_{CC} = 15.0 V			
					50						
Logic Low Supply Current	I_{CCL}			100	400	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V				
Logic High Supply Current	I_{CCH}			0.05	4	µA	I_F = 0 mA, V_O = Open, V_{CC} = 15 V				
Input Forward Voltage	V_F			1.5	1.7	V	T_A = 25°C	I_F = 16 mA		3	5
					1.8						
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA				5
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16 mA				
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0 V				5
Input-Output Insulation Voltage	V_{ISO}		2500			V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C				7
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc				7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz				7
Input-Input Insulation Leakage Current	I_{I-I}			0.005		µA	45% Relative Humidity, t = 5 s V_{I-I} = 500 Vdc				8
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω	V_{I-I} = 500 Vdc				8
Capacitance (Input-Input)	C_{I-I}			0.25		pF	f = 1 MHz				8

*All typicals at 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA, unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	HCPL-2530		0.2	1.5	μs	T_A = 25°C	R_L = 4.1 kΩ	5, 9, 11	10, 11
					2.0					
		HCPL-2531 HCPL-4534		0.2	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Propagation Delay Time to Logic High at Output	t_{PLH}	HCPL-2530		1.3	1.5	μs	T_A = 25°C	R_L = 4.1 kΩ	5, 9, 11	10, 11
					2.0					
		HCPL-2531 HCPL-4534		0.6	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	HCPL-2530		1000		V/μs	R_L = 4.1 kΩ	I_F = 0 mA, T_A = 25°C, V_{CM} = 10 V_{P-P}	10	9, 10, 11
		HCPL-2531		1000			R_L = 1.9 kΩ			
		HCPL-4534		15000			R_L = 1.9 kΩ	I_F = 0 mA, T_A = 25°C, V_{CM} = 1500 V_{P-P}		
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	HCPL-2530		1000		V/μs	R_L = 4.1 kΩ	I_F = 16 mA, T_A = 25°C, V_{CM} = 10 V_{P-P}	10	9, 10, 11
		HCPL-2531		1000			R_L = 1.9 kΩ			
		HCPL-4534		15000			R_L = 1.9 kΩ	I_F = 16 mA, T_A = 25°C, V_{CM} = 1500 V_{P-P}		

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min.External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 1.0 mW/°C.
5. Each channel.
6. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
7. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
10. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
11. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull-up resistor.
12. The frequency at which the ac output voltage is 3 dB below the low frequency asymptote.
13. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.

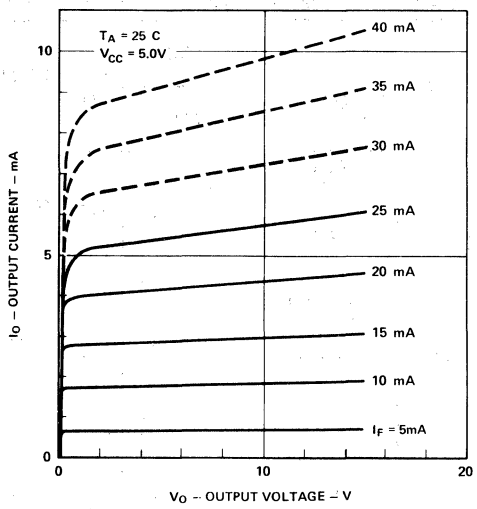


Figure 1. DC and Pulsed Transfer Characteristics.

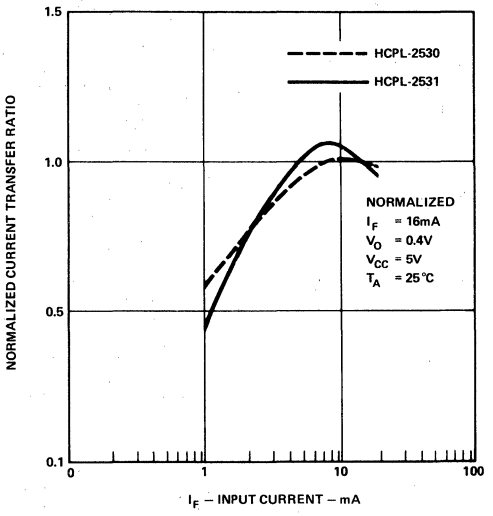


Figure 2. Current Transfer Ratio vs. Input Current.

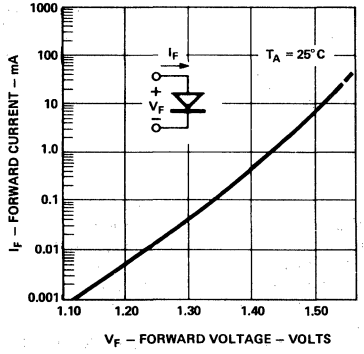


Figure 3. Input Current vs. Forward Voltage.

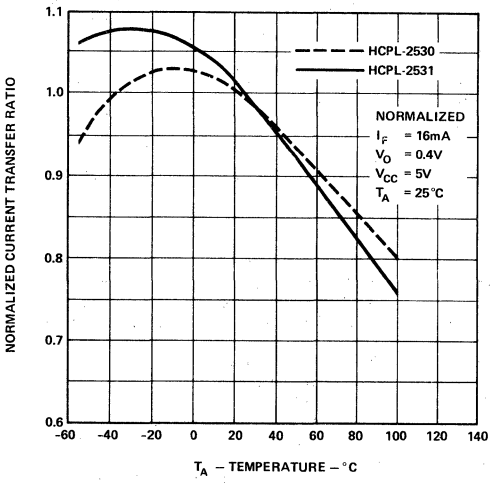


Figure 4. Current Transfer Ratio vs. Temperature.

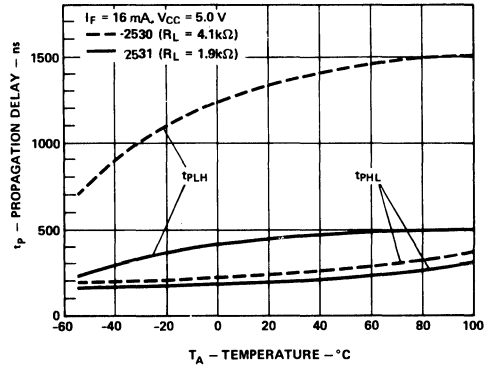


Figure 5. Propagation Delay vs. Temperature.

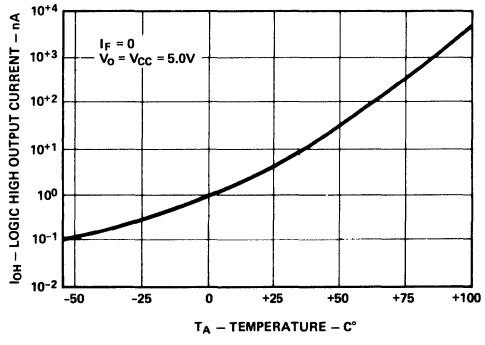


Figure 6. Logic High Output Current vs. Temperature.

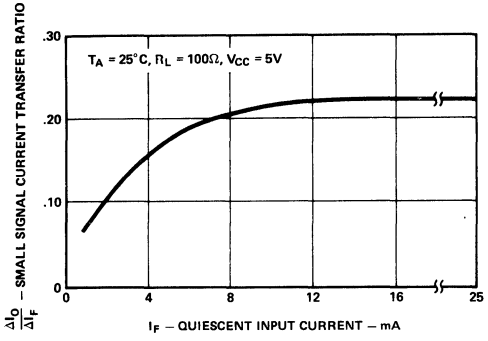
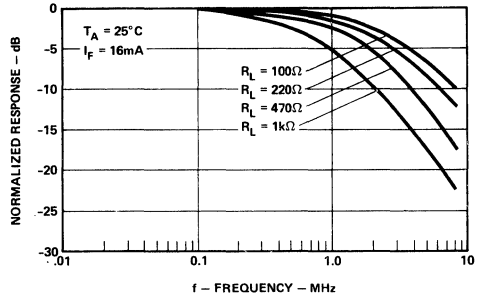


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.



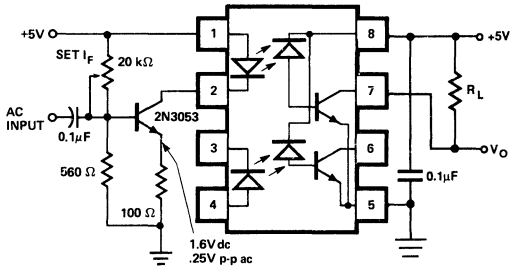


Figure 8. Frequency Response.

OPTOCOUPLERS

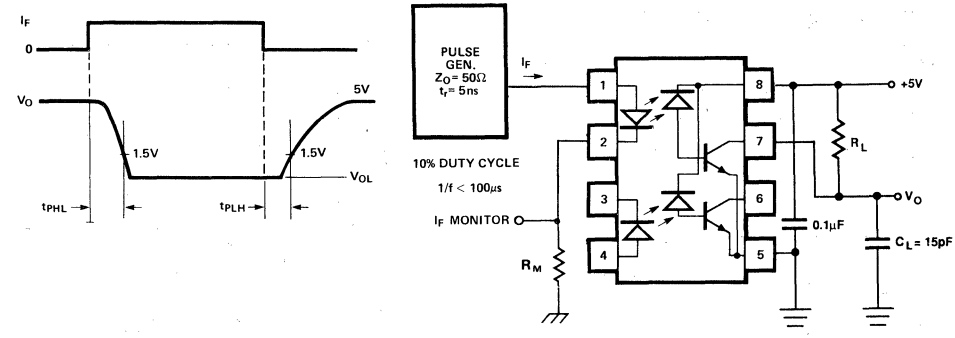


Figure 9. Switching Test Circuit.

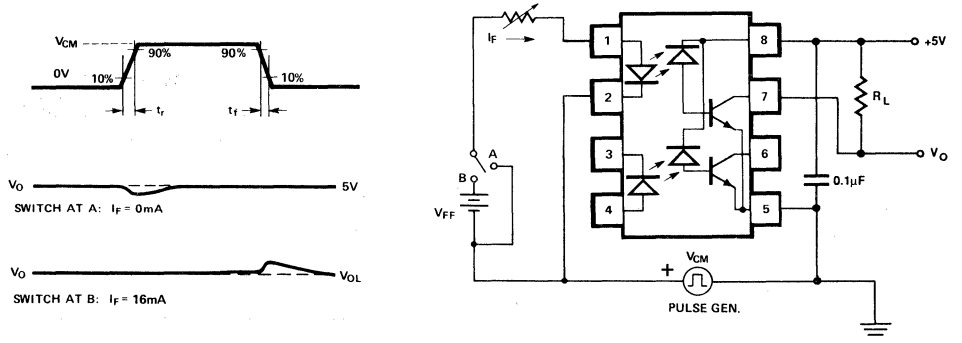


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

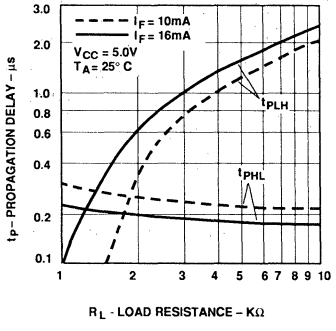


Figure 11. Propagation Delay Time vs. Load Resistance.

HEWLETT PACKARD

Small Outline High Speed Optocouplers

Technical Data

HCPL-0500
HCPL-0501
HCPL-0452
HCPL-0453

Features

- **Surface Mountable**
- **Industry Standard SOIC-8 Footprint**
- **Compatible with Infrared Vapor Phase Reflow and Wave Soldering Processes**
- **Very High Common Mode Transient Immunity: 15000 V/μs at V_{CM} = 1500 V Guaranteed (HCPL-0453)**
- **High Speed: 1 Mb/s**
- **TTL Compatible**
- **Guaranteed ac and dc Performance Over Temperature: 0°C to 70°C**
- **Open Collector Output**
- **Recognized Under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltage of 2500 VAC, 1 Minute**

Description

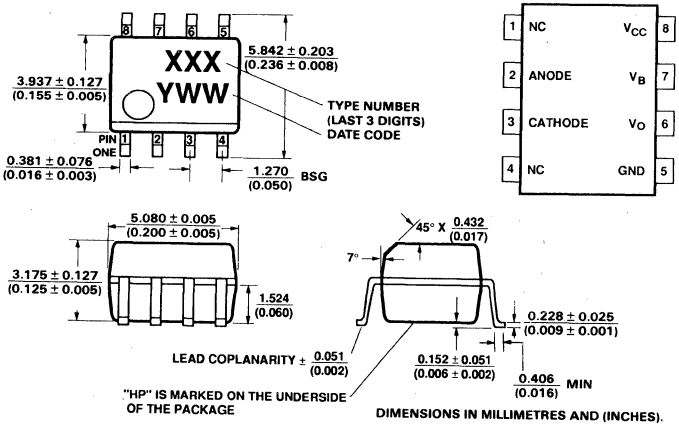
These small outline high CMR, high speed, logic gate optocouplers are single channel devices in an industry standard SOIC-8 footprint. They are electrically equivalent to the following HP optocouplers:

Small Outline	Standard DIP
HCPL-0500	6N135
HCPL-0501	6N136
HCPL-0452	HCPL-4502
HCPL-0453	HCPL-4503

The SOIC-8 package does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

These diode-transistor optocouplers use an insulating layer between the light emitting diode and an integrated photon detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

Outline Drawing*



*See notes, following page.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

The HCPL-0500 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the HCPL-0500 is 7% minimum at I_F = 16 mA.

The HCPL-0501 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the HCPL-0501 is 19% minimum at I_F = 16 mA.

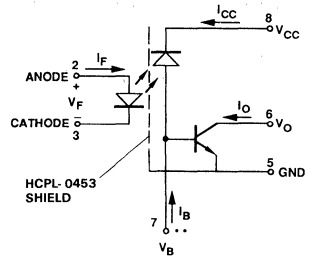
The HCPL-0452 provides the electrical and switching performance of the HCPL-0501 with increased ESD protection.

The HCPL-0453 is an HCPL–0452 with increased common mode transient immunity of 15000 V/μs minimum at V_{CM} = 1500 V guaranteed.

Applications

- **Video Signal Isolation**
- **Line Receivers** – High common mode transient immunity (>1000 V/μs) and low input-output capacitance (0.6 pF).
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Slow Phototransistor Isolators** – Pins 2-7 of the HCPL-0500/0501 series conform to pins 1-6 of 6 pin phototransistor couplers. Pin 8 can be tied to any available bias voltage of 1.5 V to 30 V for high speed operation.
- **Replace Pulse Transformers** – Save board space and weight
- **Analog Signal Ground Isolation** – Integrated photon detector provides improved linearity over phototransistor type.

Schematic



**NOTE: FOR HCPL-0452/3, PIN 7 IS NOT CONNECTED.

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -55°C to 100°C
Infrared and Vapor Phase Reflow Temperature .....215°C for 90 s
Average Input Current – I_F .....25 mA[1]
Peak Input Current – I_F ..... 50 mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F ..... 1.0 A
(≤1 μs pulse width, 300 pps)
Reverse Input Voltage – V_R (Pin 3-2) ..... 5 V
Input Power Dissipation ..... 45 mW[3]
Average Output Current – I_O (Pin 6) ..... 8 mA
Peak Output Current ..... 16 mA
Emitter-Base Reverse Voltage .....5 V
(Pin 5-7, except HCPL-0452/3)
Output Voltage – V_O (Pin 6-5) .....-0.5 V to 20 V
Supply Voltage – V_{CC} (Pin 8-5) ..... -0.5 V to 30 V
Base Current – I_B (Pin 7, except HCPL-0452/3)..... 5 mA
Output Power Dissipation .....100 mW[4]

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C), unless otherwise specified. (See note 11.)

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	HCPL-0500	7	18	50	%	T_A = 25°C, V_O = 0.4 V	1, 2, 4	5
			5	19			V_O = 0.5 V, I_F = 16 mA, V_{CC} = 4.5 V		
		HCPL-0501 HCPL-0452 HCPL-0453	19	24	50	%	T_A = 25°C, V_O = 0.4 V		
			15	25			V_O = 0.5 V		
Logic Low Output Voltage	V_{OL}	HCPL-0500		0.1	0.4	V	T_A = 25°C, I_O = 1.1 mA		
					0.5		I_O = 0.8 mA, I_F = 16 mA, V_{CC} = 4.5 V		
		HCPL-0501 HCPL-0452 HCPL-0453		0.1	0.4	V	T_A = 25°C, I_O = 3.0 mA		
					0.5		I_O = 2.4 mA		
Logic High Output Current	I_{OH}			0.003	0.5	µA	T_A = 25°C, V_O = V_{CC} = 5.5 V, I_F = 0 mA	7	
				0.01	1		T_A = 25°C, V_O = V_{CC} = 15.0 V		
					50				
Logic Low Supply Current	I_{CCL}			50	200	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V		11
Logic High Supply Current	I_{CCH}			0.02	1	µA	T_A = 25°C, I_F = 0 mA, V_O = Open, V_{CC} = 15 V		11
					2				
Input Forward Voltage	V_F			1.5	1.7	V	T_A = 25°C, I_F = 16 mA	3	
					1.8				
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16 mA		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		
Input-Output Insulation	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 MIN., T_A = 25°C		6
Resistance (Input-Output)	R_{I-O}			10^{14}		Ω	V_{I-O} = 500 Vdc		6
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		6
Transistor DC Current Gain	h_{FE}			150			V_O = 5 V, I_O = 3 mA		
				130			V_O = 0.4 V, I_O = 20 mA		

*All typicals at T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	HCPL-0500		0.2	1.5	µs	T_A = 25°C, R_L = 4.1 kΩ	5, 6, 10	8, 9
					2.0				
		HCPL-0501 HCPL-0452 HCPL-0453		0.2	0.8		T_A = 25°C, R_L = 1.9 kΩ		
					1.0				
Propagation Delay Time to Logic High at Output	t_{PLH}	HCPL-0500		1.3	1.5	µs	T_A = 25°C, R_L = 4.1 kΩ	5, 6, 10	8, 9
					2.0				
		HCPL-0501 HCPL-0452 HCPL-0453		0.6	0.8		T_A = 25°C, R_L = 1.9 kΩ		
					1.0				
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	HCPL-0500		1		kV/µs	R_L = 4.1 kΩ, I_F = 0 mA, T_A = 25°C, V_{CM} = 10 V_{p-p}	11	7, 8, 9
		HCPL-0501 HCPL-0452		1			R_L = 1.9 kΩ, I_F = 0 mA, T_A = 25°C, V_{CM} = 10 V_{p-p}		
		HCPL-0453	15	30			R_L = 1.9 kΩ, I_F = 0 mA, T_A = 25°C, V_{CM} = 1500 V_{p-p},		
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	HCPL-0500		1		kV/µs	R_L = 4.1 kΩ, I_F = 16 mA, T_A = 25°C, V_{CM} = 10 V_{p-p}	11	7, 8, 9
		HCPL-0501 HCPL-0452		1			R_L = 1.9 kΩ, I_F = 16 mA, T_A = 25°C, V_{CM} = 10 V_{p-p}		
		HCPL-0453	15	30			R_L = 1.9 kΩ, I_F = 16 mA, T_A = 25°C, V_{CM} = 1500 V_{p-p},		
Bandwidth	BW			9		MHz	See Test Circuit	8, 9	10

*All typicals at T_A = 25°C.

Notes:

1. Derate linearly above 85°C free-air temperature at a rate of 0.5 mA/°C.
2. Derate linearly above 85°C free-air temperature at a rate of 1.0 mA/°C.
3. Derate linearly above 85°C free-air temperature at a rate of 1.1 mW/°C.
4. Derate linearly above 85°C free-air temperature at a rate of 2.3 mW/°C.
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together. The 2500 Vac/1 MINUTE CAPABILITY IS VALIDATED by a factory 3200 Vac/1 second dielectric voltage withstand test.
7. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
8. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
9. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull-up resistor.
10. The frequency at which the ac output voltage is 3 dB below its mid-frequency value.
11. Use of a 0.1 µf bypass capacitor connected between pins 5 and 8 is recommended.

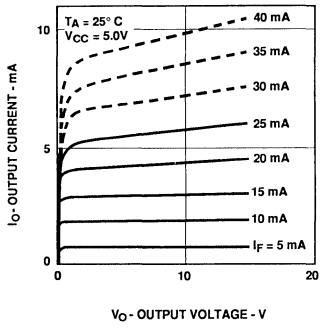


Figure 1. DC and Pulsed Transfer Characteristics.

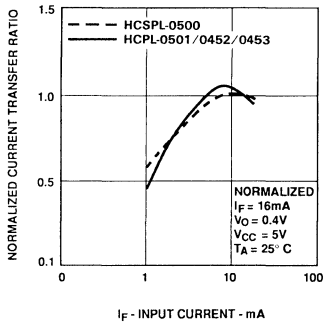


Figure 2. Current Transfer Ratio vs. Input Current.

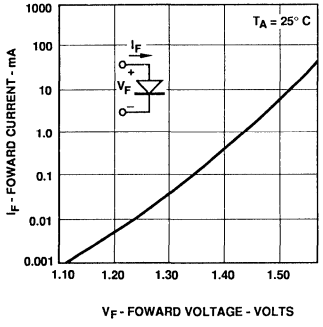


Figure 3. Input Current vs. Forward Voltage.

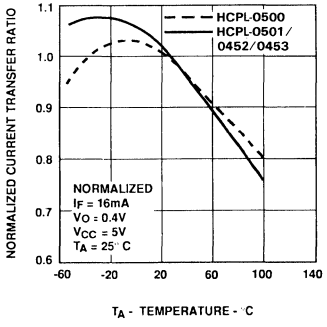


Figure 4. Current Transfer Ratio vs. Temperature.

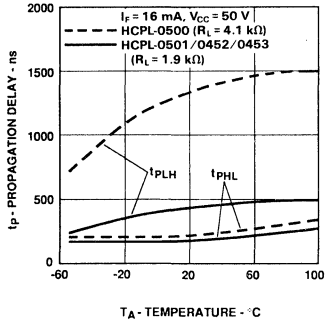


Figure 5. Propagation Delay vs. Temperature.

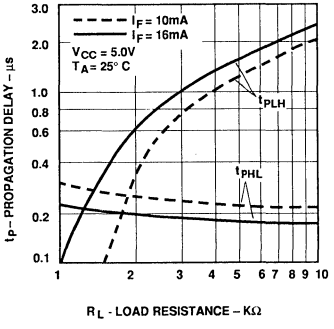


Figure 6. Propagation Delay Time vs. Load Resistance.

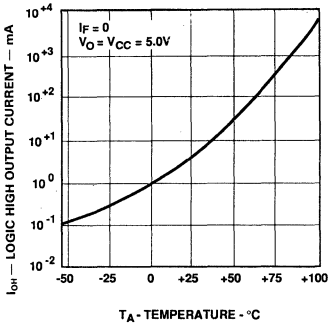


Figure 7. Logic High Output Current vs. Temperature.

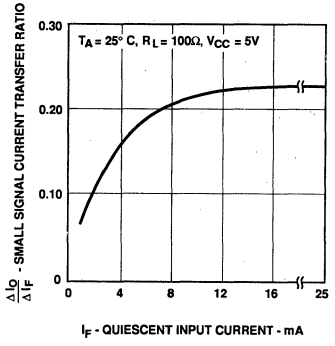
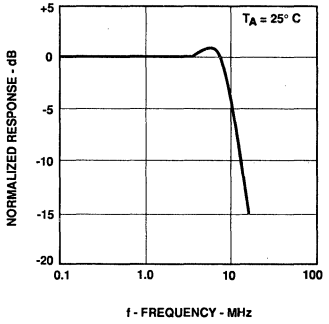


Figure 8. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.



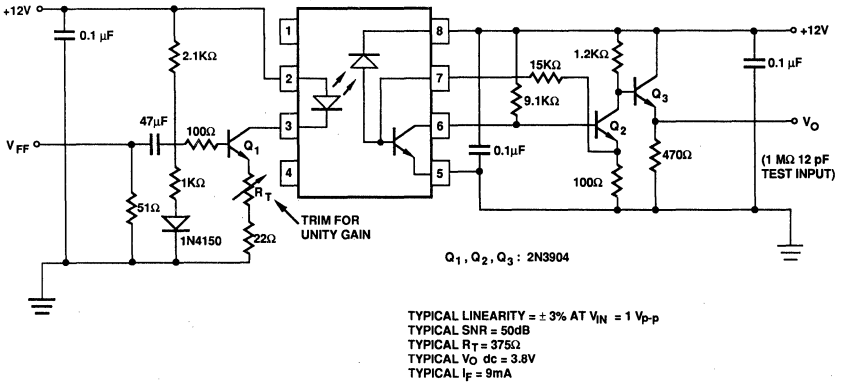


Figure 9. Frequency Response.

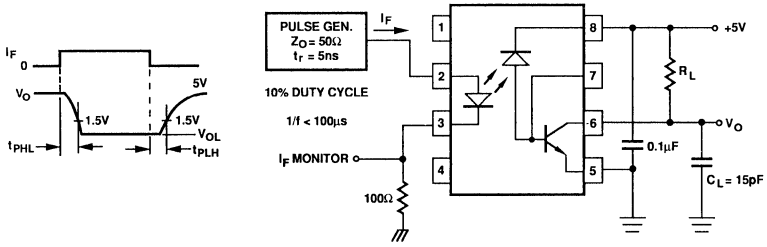


Figure 10. Switching Test Circuit.

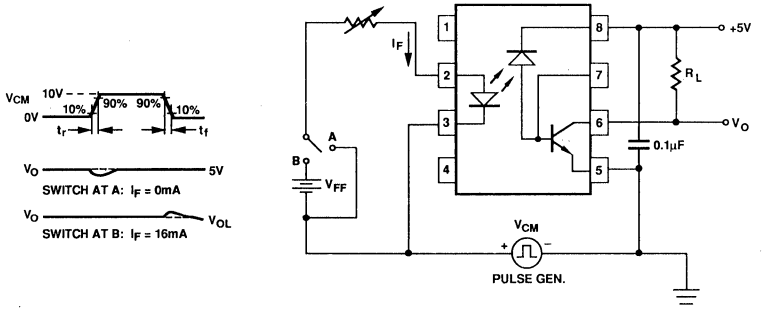


Figure 11. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

High Speed Optocouplers

Technical Data

CNW135
CNW136
CNW4502

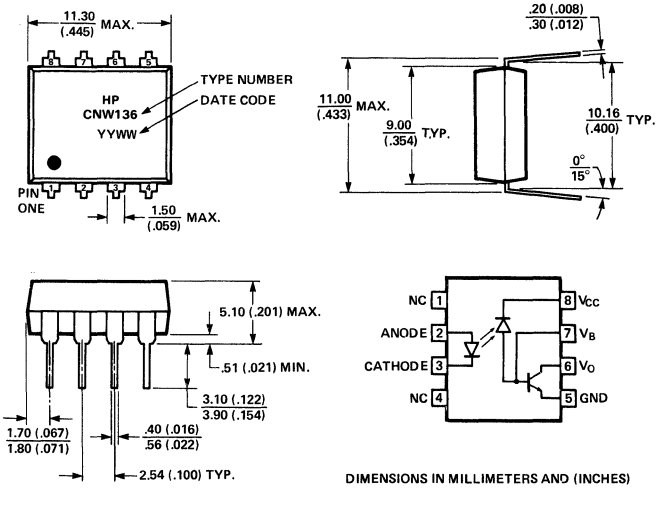
Features

- **5000 Vrms/1 Minute Insulation Withstand Capability**
- **Worldwide Safety Approval**
  UL1577 (File No. E55361)
  VDE 883/884/860/805/806/804/750
  BS 415/7002/6301
  IEC 65/380/950/335/435/601
- **High Speed: 1 Mbit/s**
- **TTL Compatible**
- **Performance Guaranteed Over Temperature 0°C to 70°C**
- **Pin Compatible with 6N135/6 and HCPL-4502**

Applications

- **High Voltage Insulation**
- **Video Signal Isolation**
- **Feedback Element in Switched Mode Power Supplies**
- **Line Receivers: >1000 V/μs common mode transient immunity and low input-output capacitance of 0.6 pF**
- **High Speed Logic Ground Isolation – TTL/TTL, TTL/CMOS, TTL/LSTTL**
- **Replaces Pulse Transformers**
- **Analog Signal Ground Isolation – Integrated photon detector provides improved linearity over phototransistor type**
- **Replaces Slow Phototransistor Isolators – Pins 2-7 of the CNW 135/6 conforms to pins 1-6 of 6 pin phototransistor couplers. Pin 8 can be tied to any available bias voltage of 1.5 V to 30 V for high speed operation**

Package Outline



DIMENSIONS IN MILLIMETERS AND (INCHES)

Description

These devices are high voltage and fast switching optocouplers consisting of an AlGaAs LED and a silicon photodetector. A wide body encapsulation is used to provide creepage and clearance dimensions suitable for safety approval by regulatory agencies worldwide.

The CNW135 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications.

Current transfer ratio (CTR) for the CNW135 is 7% minimum at I_F = 16 mA.

The CNW136 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6K pullup resistor. CTR of the CNW136 is 19% minimum at I_F = 16 mA.

The CNW4502 provides the electrical and switching performance of the CNW 136, increased ESD protection and increased transient immunity.

Regulatory Information

The CNW135/6 features a wide body 8 PIN DIP. This package was specifically designed to meet regulatory requirements worldwide. The CNW135/6 has been approved by the following organizations:

UL – Covered under UL component recognition FILE E55361

VDE – Approved according to VDE 0883/6.80
VDE 0884/08.87 certification pending
Reference voltage (VDE 0110b Tab. 4):
500 V AC/600 V DC
Complied for reinforced insulation at 250 V AC with:
DIN IEC 380/VDE 0806/8.81
DIN IEC 435/VDE 0805 "ENTWURF" Nov 84
DIN 57804/VDE 0804/1.83 (isolation group C)
DIN VDE 0860/8.86/HD 195 S4
DIN IEC 601 Teil 1/VDE 0750 Teil 1/5.82

NORDIC – Tested for applications (reinforced insulation) – Class II applications for plugable apparatus in normal tight execution.
-SETI-SEMKO-NEMKO-DEMKO-According to IEC 65-IEC380-IEC950-IEC335

BSI – Certification according to BS415:1979, BS7002:1989 and BS6301: 1987 pending

BABT – Certification pending

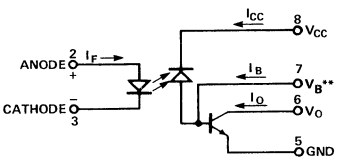
Absolute Maximum Ratings

Storage Temperature ..... -55°C to +150°C
Operating Temperature ..... -55°C to 85°C
Lead Solder Temperature ..... 260°C for 10s (up to seating plane)
Average Input Current – I_F ..... 100 mA
Peak Transient Input Current – I_F ..... 1.0 A (≤1 µs pulse width, 300 Hz)
Reverse Input Voltage – V_R (Pin 3-2) ..... 5 V
Input Power Dissipation (up to 70°C) ..... 250 mW*
Average Output Current – I_O (Pin 6) ..... 10 mA
Emitter-Base Reverse Voltage (Pin 5-7) ..... 5 V
Output Voltage – V_O (Pin 6-5) ..... -0.5 V to 20 V
Supply Voltage – V_{CC} (Pin 8-5) ..... -0.5 V to 30 V
Base Current – I_B (Pin 7, except HCPL-4502) ..... 5 mA
Output Power Dissipation ..... 100 mW

*Derate at 5.0 mW/°C for operating temperatures above 70°C.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assemby of this component to prevent damage and/or degradation which may be induced by ESD.

Schematic



**Note: For CNW4502, Pin 7 is not connected.

OPTOCOUPLERS

VDE 0884 Insulation Characteristics – Pending Approval

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0109/12.83, Table 1 for rated mains voltage ≤ 600 V_{RMS} for rated mains voltage ≤ 1000 V_{RMS}		 I-IV I-III	
Climatic Classification		55/150/21	
Pollution Degree (DIN VDE 0109/12.83)		2	
Maximum Working Insulation Voltage	V_{IORM}	1000	V_{RMS}
Input to Output Test Voltage, Method b* V_{PR} = 1.6 x V_{IORM}, 100% Production Test with tp = 1 sec, Partial Discharge < 5 pC	V_{PR}	1600	V_{RMS}
Input to Output Test Voltage, Method a* V_{PR} = 1.2 x V_{IORM}, Type and sample test, tp = 60 sec, Partial Discharge < 5 pC	V_{PR}	1200	V_{RMS}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	8000	V_{PK}
Safety-Limiting Values (Maximum values allowed in the event of a failure, also see Figure 9) Case Temperature Current (Input Current I_F, P_{SI} = 0) Output Power (obtained by setting pin 8 = 5.5 V, pins 7, 6, 5 = ground)	 T_{SI} I_{SI} $P_{SI, OUTPUT}$	 175 400 700	 °C mA mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V V_{IO} = 500 V	R_{IS}	≥ 10^9	ohm

*Refer to the front of the optocoupler section of the 1991 Designer's Catalog, under regulatory information, (VDE 0884) for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuts in the application.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (clearance)	L(IO1)	9.6	mm	Measured from input terminals to output terminals
Min. External Tracking Path (creepage)	L(IO2)	10.0	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (clearance)		1.0	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	volts	DIN IEC 112/VDE 0303 PART 1
Isolation Group (per DIN VDE 0109)		IIIa		Material group (DIN VDE 0109)

Electrical Specifications

Over Recommended Temperature (T_A = 0°C to 70°C) unless otherwise specified. (See note 8.)

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	CNW135	7	18	75	%	T_A = 25°C, V_O = 0.4 V, I_F = 16 mA, V_{CC} = 4.5 V	1, 2, 4	1
			5				V_O = 0.5 V, I_F = 16 mA, V_{CC} = 4.5 V		
		CNW136 CNW4502	19	40	75	%	T_A = 25°C, V_O = 0.4 V, I_F = 16 mA, V_{CC} = 4.5 V		
			15				V_O = 0.5 V, I_F = 16 mA, V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}	CNW135		0.1	0.4	V	T_A = 25°C, I_O = 1.1 mA, I_F = 16 mA, V_{CC} = 4.5 V		
					0.5		I_O = 0.8 mA, I_F = 16 mA, V_{CC} = 4.5 V		
		CNW136 CNW4502		0.1	0.4	V	T_A = 25°C, I_O = 3.0 mA, I_F = 16 mA, V_{CC} = 4.5 V		
					0.5		I_O = 2.4 mA, I_F = 16 mA, V_{CC} = 4.5 V		
Logic High Output Current	I_{OH}			0.002	0.5	µA	T_A = 25°C, V_O = V_{CC} = 5.5 V, I_F = 0 mA	6	
					1		T_A = 25°C, V_O = V_{CC} = 15 V, I_F = 0 mA		
					50				
Logic Low Supply Current	I_{CCL}			50	200	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V		
Logic High Supply Current	I_{CCH}				1	µA	T_A = 25°C, I_F = 0 mA, V_O = Open, V_{CC} = 15 V		
					2				
Input Forward Voltage	V_F		1.25	1.52	1.70	V	T_A = 25°C, I_F = 16 mA	3	
			1.20		1.80				
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			1.9		mV/°C	I_F = 16 mA		
Input Capacitance	C_{IN}			200		pF	f = 1 MHz, V_F = 0 V		
Input-Output Insulation Voltage	V_{ISO}		5000			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C		2, 7
Resistance (Input-Output)	R_{I-O}		10^{12}	10^{13}		Ω	T_A = 25°C, V_{I-O} = 500 VDC		2
			10^{11}				T_A = 100°C, V_{I-O} = 500 VDC		
Capacitance (Input-Output)	C_{I-O}			0.4	0.6	pF	f = 1 MHz		2
Transistor DC Current Gain	h_{FE}			180			V_O = 5 V, I_O = 3 mA		
				160			V_O = 0.4 V, I_B = 40 µA		

*All typicals at T_A = 25°C.

Switching Specifications

Over Recommended Temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA, unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	CNW135		0.3	1.5	µs	T_A = 25°C	R_L = 4.1 kΩ	5, 8, 11	4, 5
					2.0					
		CNW136 CNW4502		0.4	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Propagation Delay Time to Logic High at Output	t_{PLH}	CNW135		0.6	1.5	µs	T_A = 25°C	R_L = 4.1 kΩ	5, 8, 11	4, 5
					2.0					
		CNW136 CNW4502		0.35	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	CNW135	1,000			V/µs	R_L = 4.1 kΩ	I_F = 0 mA, T_A = 25°C, V_{CM} = 10 V	12	3, 4, 5
		CNW136 CNW4502	1,000				R_L = 1.9 kΩ			
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	CNW135	1,000			V/µs	R_L = 4.1 kΩ	I_F = 16 mA, T_A = 25°C, V_{CM} = 10 V	12	3, 4, 5
		CNW136 CNW4502	1,000				R_L = 1.9 kΩ			
Bandwidth	BW	CNW135 CNW136		11		MHz	See Test Circuit		7, 10	6

*All typicals are at T_A = 25°C.

Notes:

1. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
2. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
3. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e. V_O > 2.0 V) Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM} dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e. V_O > 0.8 V).
4. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
5. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull-up resistor.
6. The frequency at which the ac output voltage is 3 dB below the low frequency asymptote.
7. Each product is tested by applying an isolation test voltage of 6000 Vrms for 2 seconds. This test is in accordance with UL1577 and is performed in addition to the tests shown in the VDE0884 INSULATION CHARACTERISTICS TABLE.
8. Use of a 0.1 µf bypass capacitor connected between pins 5 and 8 is recommended for operation.

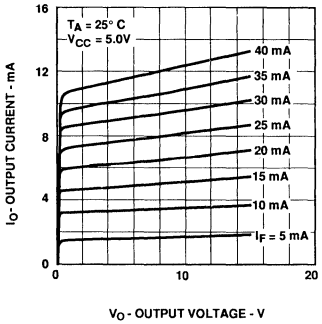


Figure 1. DC and Pulsed Transfer Characteristics.

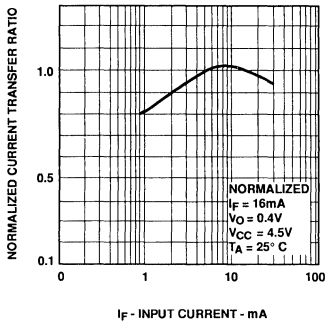


Figure 2. Current Transfer Ratio vs Input Current

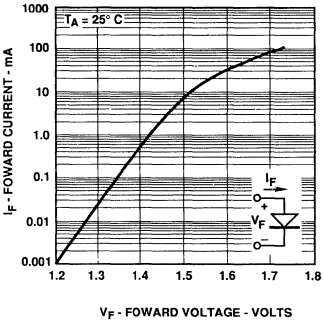


Figure 3. Input Current vs Forward Voltage.

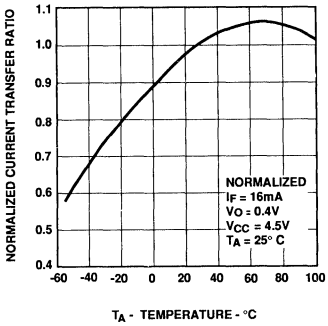


Figure 4. Current Transfer Ratio vs Temperature.

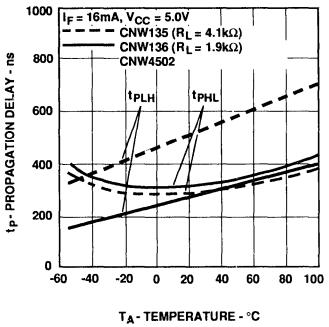


Figure 5. Propagation Delay vs Temperature.

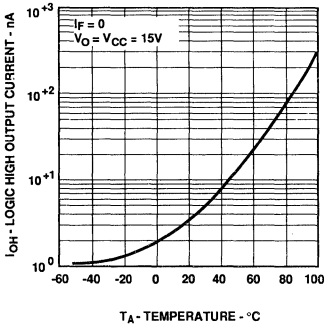


Figure 6. Logic High Output Current vs Temperature.

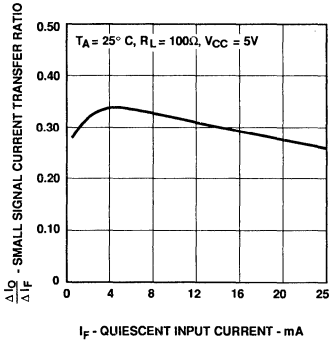


Figure 7. Small-Signal Current Transfer Ratio vs Quiescent Input Current.

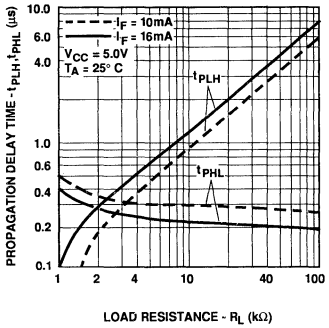


Figure 8. Propagation Delay Time vs Load Resistance.

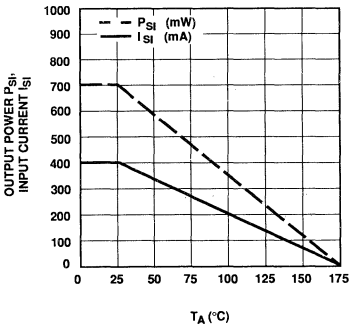


Figure 9. Dependence of Safety Maximum Ratings with Ambient Temperature.

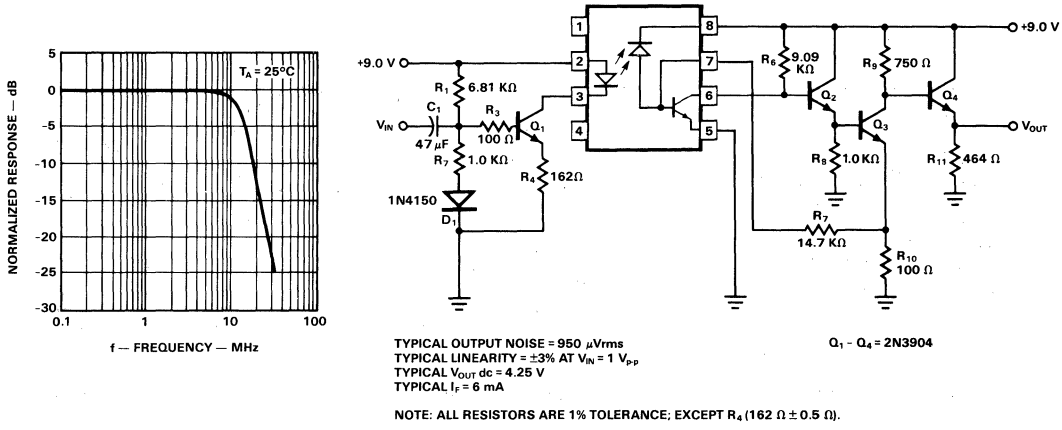


Figure 10. Frequency Response.

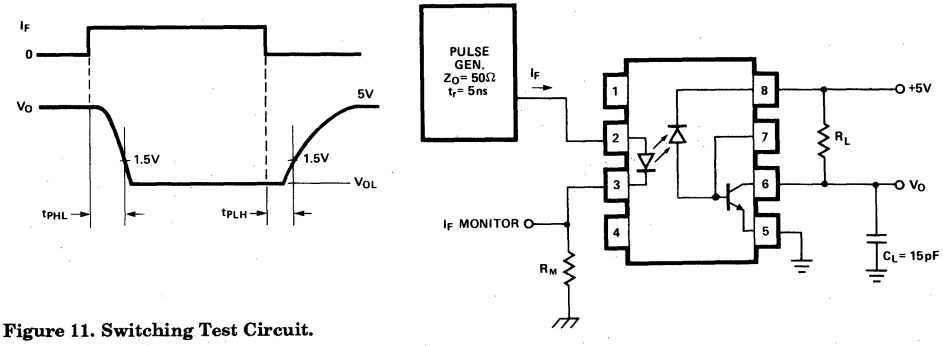


Figure 11. Switching Test Circuit.

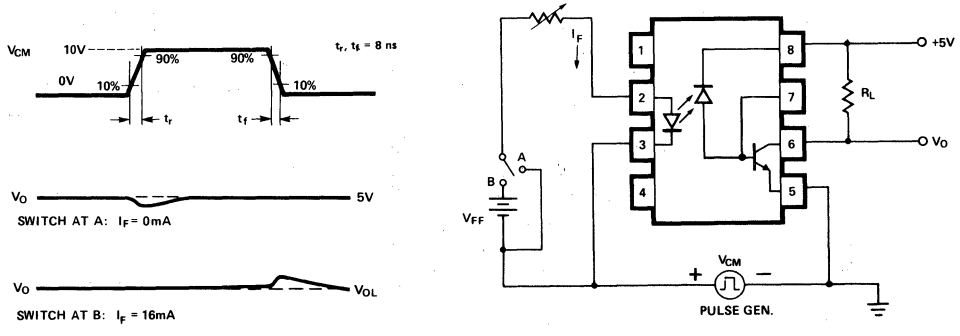
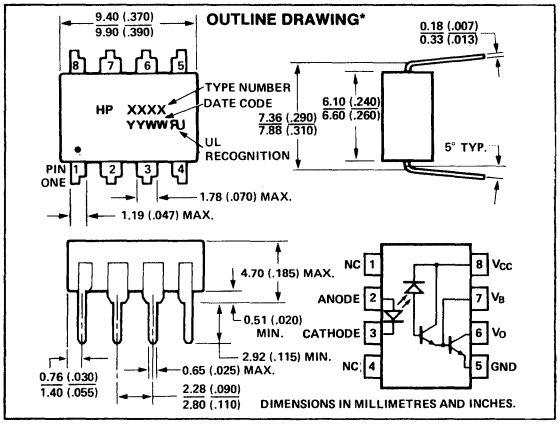


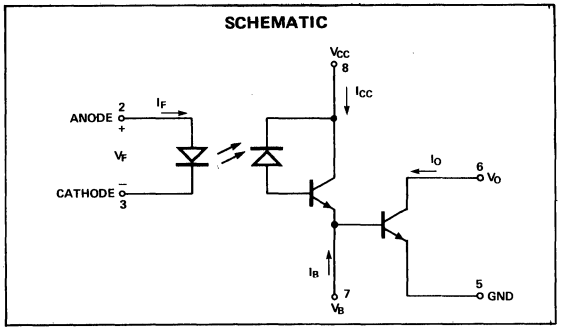
Figure 12. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

6N138
6N139





Features

- **HIGH CURRENT TRANSFER RATIO — 2000% TYPICAL**
- **LOW INPUT CURRENT REQUIREMENT — 0.5 mA**
- **TTL COMPATIBLE OUTPUT — 0.1 V V_{OL} TYPICAL**
- **PERFORMANCE GUARANTEED OVER TEMPERATURE 0°C TO 70°C**
  BASE ACCESS ALLOWS GAIN BANDWIDTH ADJUSTMENT
- **HIGH OUTPUT CURRENT — 60 mA**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE AND 5000 Vac, 1 MINUTE (OPTION 020)**
- **VDE 0883 APPROVAL AVAILABLE**
- **MIL-STD-1772 VERSION AVAILABLE (HCPL-5700/1)**

Description

These high gain series couplers use a Light Emitting Diode and an integrated high gain photo detector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

The 6N139 is for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70°C operating range for only 0.5 mA of LED current.

The 6N138 is designed for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70°C for an LED current of 1.6 mA [1 TTL Unit load (U.L.)]. A 300% minimum CTR enables operation with 1 U.L. out with a 2.2 kΩ pull-up resistor.

Selection for lower input current down to 250 μA is available upon request.

Applications

- Ground Isolate Most Logic Families – TTL/TTL, CMOS/TTL, CMOS/CMOS, LSTTL/TTL, CMOS/LSTTL
- Low Input Current Line Receiver – Long Line or Party line
- EIA RS-232C Line Receiver
- Telephone Ring Detector
- 117 V ac Line Voltage Status Indicator – Low Input Power Dissipation
- Low Power Systems – Ground Isolation

Absolute Maximum Ratings*

(No Derating Required up to 85°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature** ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10s
(1.6 mm below seating plane)
Average Input Current — I_F ..... 20 mA
Peak Input Current — I_F ..... 40 mA
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — I_F ..... 1.0 A
(≤1 μs pulse width, 300 pps)
Reverse Input Voltage — V_R ..... 5 V
Input Power Dissipation ..... 35 mW
Output Current — I_O (Pin 6) ..... 60 mA
Emitter-Base Reverse Voltage (Pin 5-7) ..... 0.5 V
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 6-5)
6N138 ..... -0.5 to 7 V
6N139 ..... -0.5 to 18 V
Output Power Dissipation ..... 100 mW

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

*JEDEC Registered Data.
**0° to 70° on JEDEC Registration.

OPTOCOUPLERS

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C), unless otherwise specified. (See note 7.)

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	6N139	400* 500*	2000 1600	3500 2600	%	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V	2, 3	1, 2
		6N138	300*	1600	2600	%	I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}	6N139		0.1 0.1 0.2	0.4 0.4 0.4	V	I_F = 1.6 mA, I_O = 8 mA, V_{CC} = 4.5 V I_F = 5 mA, I_O = 15 mA, V_{CC} = 4.5 V I_F = 12 mA, I_O = 24 mA, V_{CC} = 4.5 V	1	2
		6N138		0.1	0.4	V	I_F = 1.6 mA, I_O = 4.8 mA, V_{CC} = 4.5 V		
Logic High Output Current	I_{OH}	6N139		0.05	100	μA	I_F = 0 mA, V_O = V_{CC} = 18 V		2
		6N138		0.1	250	μA	I_F = 0 mA, V_O = V_{CC} = 7 V		
Logic Low Supply Current	I_{CCL}			0.4	1.5	mA	I_F = 1.6 mA, V_O = Open, V_{CC} = 18 V		2
Logic High Supply Current	I_{CCH}			0.01	10	μA	I_F = 0 mA, V_O = Open, V_{CC} = 18 V		2
Input Forward Voltage	V_F			1.4	1.7* 1.75	V	T_A = 25°C, I_F = 1.6 mA	4	
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10 μA		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.6 mA		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		
Input-Output Insulation	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C		3
Option 020	V_{ISO}		5000						
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 VDC		3
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		3

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	6N139		5	25*	μs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 6, 7	2, 4
					30				
				0.2	1*		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω		
					2				
		6N138		1.6	10*		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ		
					15				
Propagation Delay Time to Logic High at Output	t_{PLH}	6N139		18	60*	μs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 6, 7	2, 4
					90				
				2	7*		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω		
					10				
		6N138		10	35*		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ		
					50				
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$			500		V/μs	I_F = 0 mA, T_A = 25°C, R_L = 2.2 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}	8	5, 6
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$			500		V/μs	I_F = 1.6 mA, T_A = 25°C, R_L = 2.2 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}	8	5, 6

*JEDEC registered data.
**All typicals at T_A = 25°C and V_{CC} = 5 V, unless otherwise noted.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min.External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

1. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
2. Pin 7 Open.
3. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
4. Use of a resistor between pin 5 and 7 will decrease gain and delay time. See Application Note 951-1 for more details.
5. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8$ V).
6. In applications where dV/dt may exceed 50,000 V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is $R_{CC} = 220\ \Omega$.
7. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.

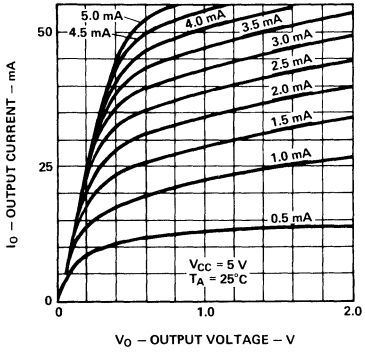


Figure 1. 6N138/6N139 DC Transfer Characteristics

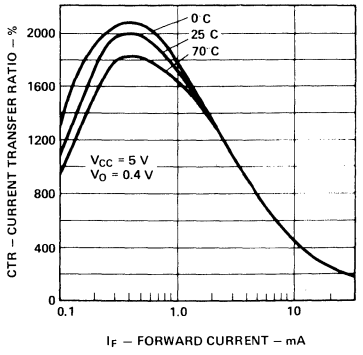


Figure 2. Current Transfer Ratio vs Forward Current 6N138/6N139

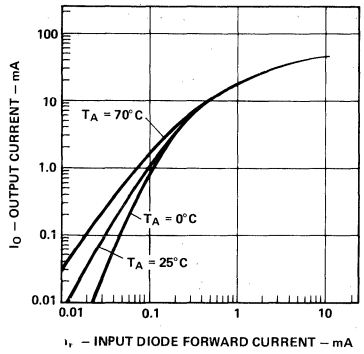


Figure 3. 6N138/6N139 Output Current vs Input Diode Forward Current

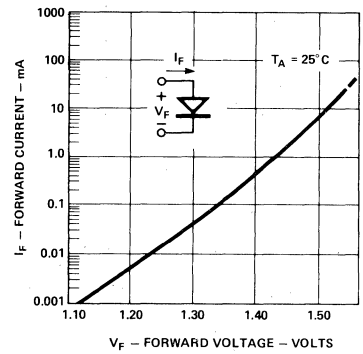


Figure 4. Input Diode Forward Current vs. Forward Voltage.

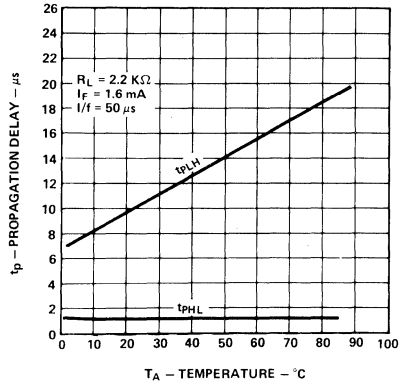


Figure 5. Propagation Delay vs. Temperature.

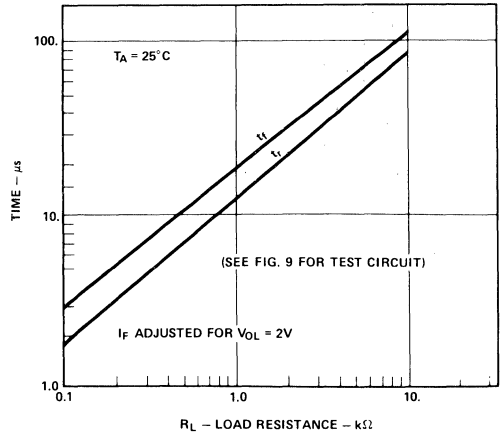


Figure 6. Non Saturated Rise and Fall Times vs. Load Resistance.

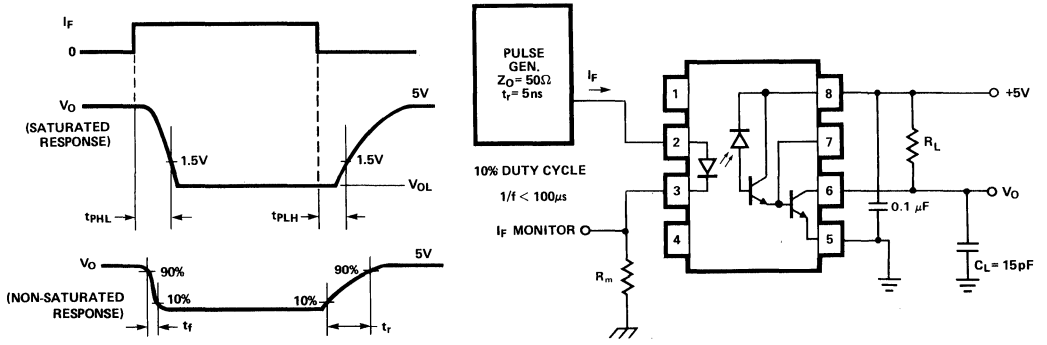


Figure 7. Switching Test Circuit.*

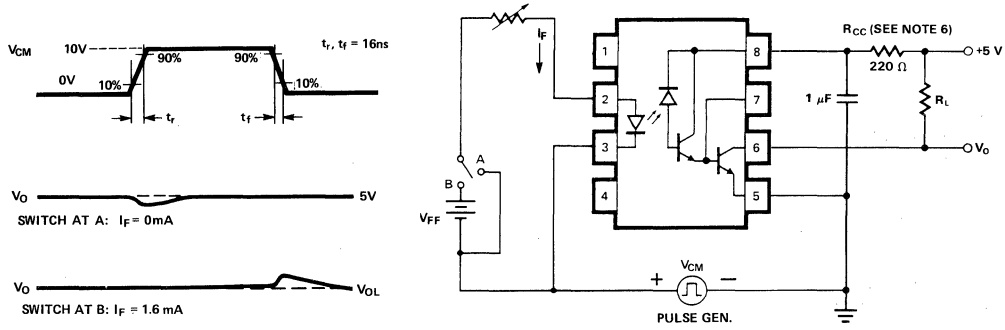


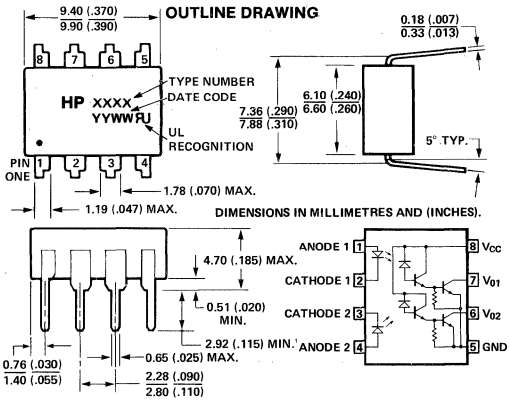
Figure 8. Test Circuit for Transient Immunity and Typical Waveforms.

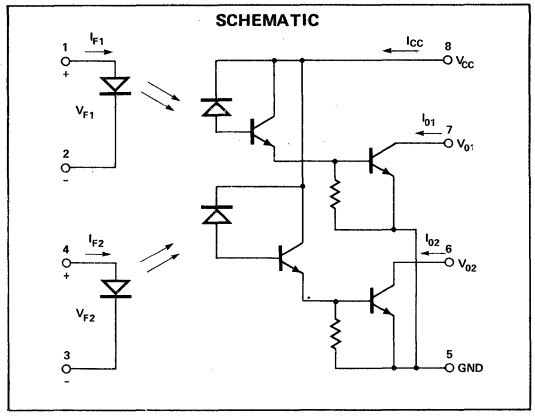
*JEDEC Registered Data.

HEWLETT PACKARD

DUAL LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

HCPL-2730
HCPL-2731





Features

- **HIGH CURRENT TRANSFER RATIO — 1800% TYPICAL**
- **LOW INPUT CURRENT REQUIREMENT — 0.5 mA**
- **LOW OUTPUT SATURATION VOLTAGE — 0.1 V TYPICAL**
- **HIGH DENSITY PACKAGING**
- **PERFORMANCE GUARANTEED OVER 0°C TO 70°C TEMPERATURE RANGE**
- **LSTTL COMPATIBLE**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **VDE 0883 APPROVAL AVAILABLE**
- **MIL-STD VERSION AVAILABLE (HCPL-5730/1)**

Applications

- **Digital Logic Ground Isolation**
- **Telephone Ring Detector**
- **EIA RS-232C Line Receiver**
- **Low Input Current Line Receiver — Long Line or Party Line**
- **Microprocessor Bus Isolation**
- **Current Loop Receiver**
- **Polarity Sensing**
- **Level Shifting**
- **Line Voltage Status Indicator — Low input Power Dissipation**

Description

The HCPL-2730/31 dual channel couplers contain a separated pair of GaAsP light emitting diodes optically coupled to a pair of integrated high gain photo detectors. They provide extremely high current transfer ratio and excellent input-output common mode transient immunity. A separate pin for the photodiodes and first gain stages (V_{CC}) permits lower output saturation voltage and higher speed operation than possible with conventional photodarlington type optocouplers. In addition V_{CC} may be as low as 1.6 V without adversely affecting the parametric performance.

Guaranted operation at low input currents and the high current transfer ratio (CTR) reduce the magnitude and effects of CTR degradation.

The outstanding high temperature performance of this split Darlington type output amplifier results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground.

The HCPL-2731 has a 400% minimum CTR at an input current of only 0.5 mA making it ideal for use in low input current application such as MOS, CMOS and low power logic interfacing or RS232C data transmission systems. In addition, the high CTR and high output current capability make this device extremely useful in applications where a high fanout is required. Compatibility with high voltage CMOS logic systems is guaranteed by the 18V V_{CC} and V_O specifications and by testing output high leakage (I_{OH}) at 18V.

The HCPL-2730 is specified at an input current of 1.6 mA and has a 7 V V_{CC} and V_O rating. The 300% minimum CTR allows TTL to TTL interfacing at this input current.

Important specifications such as CTR, leakage current and output saturation voltage are guaranteed over the 0°C to 70°C temperature range to allow trouble-free system operation. Selection for lower input current down to 250 μA is available upon request.

Electrical Specifications

(Over recommended temperature T_A = 0°C to 70°C, unless otherwise specified.) See note 12.

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	2731	400 500	1800 1600	3500 2600	%	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V	2, 3	6, 7
		2730	300	1600	2600	%	I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}	2731		0.1 0.1 0.2	0.4 0.4 0.4	V	I_F = 1.6 mA, I_O = 8 mA, V_{CC} = 4.5 V I_F = 5 mA, I_O = 15 mA, V_{CC} = 4.5 V I_F = 12 mA, I_O = 24 mA, V_{CC} = 4.5 V	1	6
		2730		0.1	0.4	V	I_F = 1.6 mA, I_O = 4.8 mA, V_{CC} = 4.5 V		
Logic High Output Current	I_{OH}	2731		0.005	100	μA	I_F = 0 mA, V_O = V_{CC} = 18 V		6
		2730		0.01	250	μA	I_F = 0 mA, V_O = V_{CC} = 7 V		
Logic Low Supply Current	I_{CCL}	2731		1.2	3	mA	V_{CC} = 18 V; I_{F1} = I_{F2} = 1.6 mA, V_{O1} = V_{O2} = Open	5	
		2730		0.9			V_{CC} = 7 V; I_{F1} = I_{F2} = 1.6 mA, V_{O1} = V_{O2} = Open		
Logic High Supply Current	I_{CCH}	2731		0.005	20	μA	V_{CC} = 18 V; I_{F1} = I_{F2} = 0 mA, V_{O1} = V_{O2} = Open	5	
		2730		0.004			V_{CC} = 7 V; I_{F1} = I_{F2} = 0 mA, V_{O1} = V_{O2} = Open		
Input Forward Voltage	V_F			1.4	1.7	V	T_A = 25°C, I_F = 1.6 mA	4	6
					1.75		T_A = 0°C to 70°C, I_F = 1.6 mA		
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 μA		6
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.6 mA		6
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		6
Input-Output Insulation	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C		8
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 VDC		8
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		8
Input-Input Insulation Leakage Current	I_{I-I}			0.005		μA	45% Relative Humidity, t = 5 s, V_{I-I} = 500 VDC		9
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω	V_{I-I} = 500 VDC		9
Capacitance (Input-Input)	C_{I-I}			0.25		pF	f = 1 MHz		9

*All typicals at T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	2731		25	100	μs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	6, 7, 8, 9	6
					120				
		2730/1		5	20		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ		
					25				
				0.5	2		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω		
					3				
Propagation Delay Time to Logic High at Output	t_{PLH}	2731		10	60	μs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	7, 8, 9	6
					90				
		2730/1		10	35		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ		
					50				
				1	10		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω		
					15				
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$			500		V/μs	I_F = 0 mA, R_L = 2.2 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}, T_A = 25°C	10	6, 10, 11
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$			500		V/μs	I_F = 1.6 mA, R_L = 2.2 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}, T_A = 25°C	10	6, 10, 11

*All typicals at 25°C

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min.External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

NOTES:

1. Derate linearly above 50 C free-air temperature at a rate of 0.5 mA/°C.
2. Derate linearly above 50 C free-air temperature at a rate of 0.9 mW/°C.
3. Derate linearly above 35 C free-air temperature at a rate of 0.6 mA/°C.
4. Pin 5 should be the most negative voltage at the detector side.
5. Derate linearly above 35 C free-air temperature at a rate of 1.7 mW/°C. Output power is collector output power plus supply power.
6. Each channel.
7. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
8. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
9. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
10. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM} dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
11. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is R_{CC} = 110 Ω.
12. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 sec
(1.6mm below seating plane)
Average Input Current — I_F
(each channel) ..... 20 mA [1]
Peak Input Current — I_F
(each channel) ..... 40 mA
(50% duty cycle, 1 ms pulse width)
Reverse Input Voltage — V_R
(each channel) 5V
Input Power Dissipation
(each channel) ..... 35 mW [2]
Output Current — I_O
(each channel) ..... 60 mA [3]
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 7,6-5) [4]
HCPL-2730 ..... -0.5 to 7V
HCPL-2731 ..... -0.5 to 18V
Output Power Dissipation
(each channel) ..... 100 mW [5]

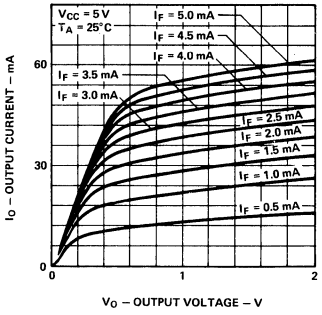


Figure 1. DC Transfer Characteristics (HCPL-2730/HCPL-2731)

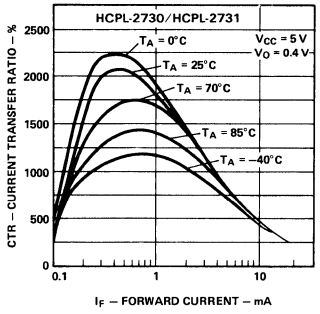


Figure 2. Current Transfer Ratio vs. Forward Current

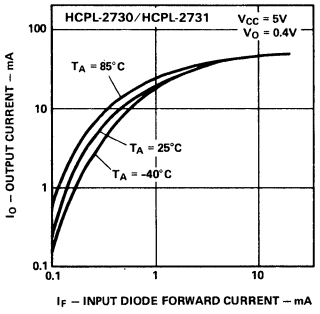


Figure 3. Output Current vs. Input Diode Forward Current

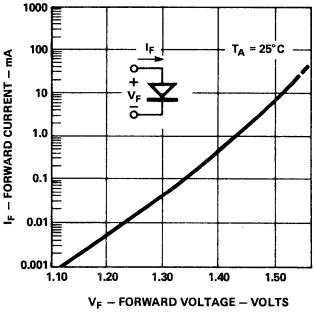


Figure 4. Input Diode Forward Current vs. Forward Voltage.

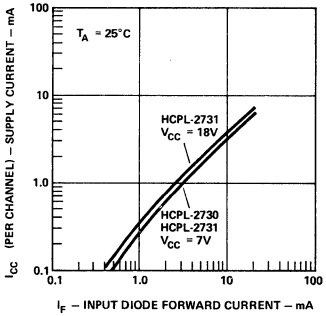


Figure 5. Supply Current Per Channel vs. Input Diode Forward Current.

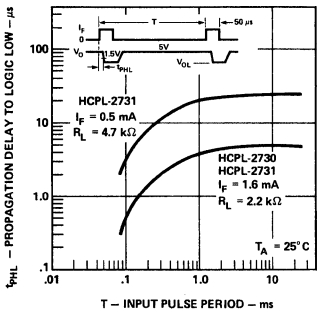


Figure 6. Propagation Delay To Logic Low vs. Pulse Period.

OPTOCOUPLERS

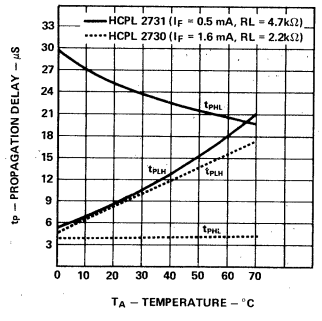


Figure 7. Propagation Delay vs. Temperature.

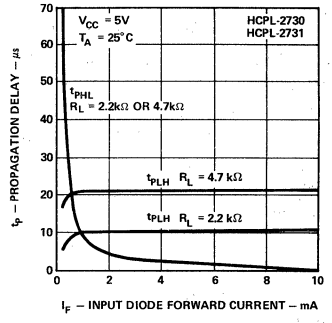


Figure 8. Propagation Delay vs. Input Diode Forward Current.

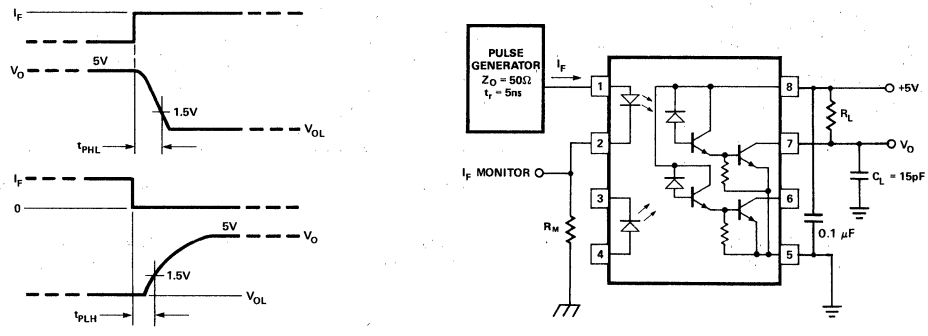


Figure 9. Switching Test Circuit.

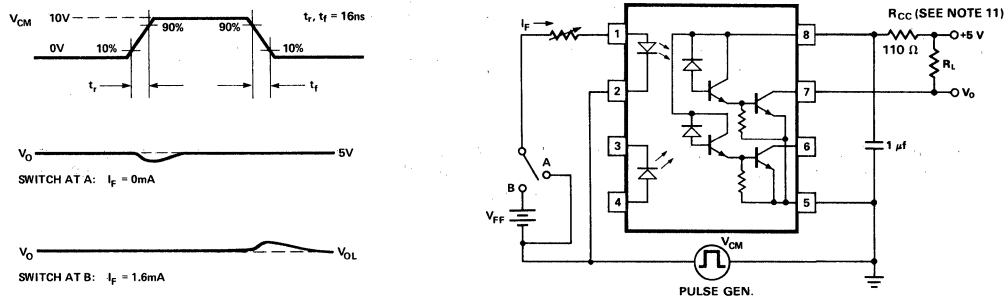
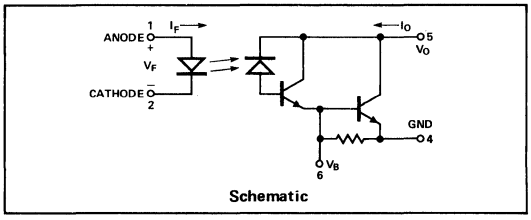


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

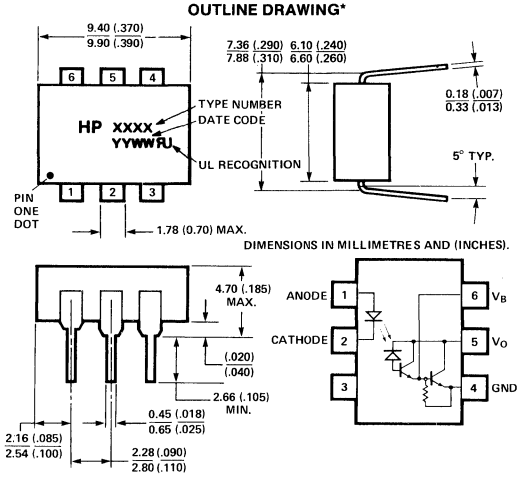
HEWLETT PACKARD

LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLER

4N45
4N46



OUTLINE DRAWING*



Features

- **HIGH CURRENT TRANSFER RATIO — 1500% TYPICAL**
- **LOW INPUT CURRENT REQUIREMENT — 0.5 mA**
- **PERFORMANCE GUARANTEED OVER 0°C to 70°C TEMPERATURE RANGE**
- **INTERNAL BASE-EMITTER RESISTOR MINIMIZES OUTPUT LEAKAGE**
- **GAIN-BANDWIDTH ADJUSTMENT PIN**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **VDE 0883 APPROVAL AVAILABLE**

Description

The 4N45/46 optocouplers contain a GaAsP light emitting diode optically coupled to a high gain photodetector IC.

The excellent performance over temperature results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground. External access to the second stage base provides better noise rejection than a conventional photodarlington detector. An external resistor or capacitor at the base can be added to make a gain-bandwidth or input current threshold adjustment. The base lead can also be used for feedback.

The high current transfer ratio at very low input currents permits circuit designs in which adequate margin can be allowed for the effects of CTR degradation over time.

The 4N46 has a 350% minimum CTR at an input current of only 0.5mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing. Compatibility with high voltage CMOS logic systems is assured by the 20V minimum breakdown voltage of the output transistor and by the guaranteed maximum output leakage (I_{OH}) at 18V.

The 4N45 has a 250% minimum CTR at 1.0mA input current and a 7V minimum breakdown voltage rating.

Selection for lower input current down to 250 μA is available upon request.

*JEDEC Registered Data. **JEDEC Registered up to 70°C

Applications

- **Telephone Ring Detector**
- **Digital Logic Ground Isolation**
- **Low Input Current Line Receiver**
- **Line Voltage Status Indicator — Low Input Power Dissipation**
- **Logic to Reed Relay Interface**
- **Level Shifting**
- **Interface Between Logic Families**

Absolute Maximum Ratings*

Storage Temperature ..... -55°C to +125°C
Operating Temperature** ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 s.
(1.6mm below seating plane)
Average Input Current — I_F ..... 20 mA[1]
Peak Input Current — I_F ..... 40 mA
(50% duty cycle, 1ms pulse width)
Peak Transient Input Current — I_F 1.0A
($\leq$1 μs pulse width, 300pps)
Reverse Input Voltage — V_R 5V
Input Power Dissipation ..... 35mW[2]
Output Current — I_O (Pin 5) ..... 60 mA[3]
Emitter-Base Reverse Voltage (Pins 4-6) 0.5V
Output Voltage — V_O (Pin 5-4)
4N45 ..... -0.5 to 7V
4N46 ..... -0.5 to 20V
Output Power Dissipation ..... 100mW[4]

See notes, following page

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C), unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	4N46	350* 500* 200*	1500 1500 600	3200 2000 1000	%	I_F = 0.5 mA, V_O = 1.0 V I_F = 1.0 mA, V_O = 1.0 V I_F = 10 mA, V_O = 1.2 V	3, 4 10, 11	5, 6
		4N45	250* 200*	1200 500	2000 1000	%	I_F = 1.0 mA, V_O = 1.0 V I_F = 10 mA, V_O = 1.2 V		
Logic Low Output Voltage	V_{OL}	4N46		0.90 0.92 0.95	1.0 1.0 1.2	V	I_F = 0.5 mA, I_{OL} = 1.75 mA I_F = 1.0 mA, I_{OL} = 5.0 mA I_F = 10 mA, I_{OL} = 20 mA	2	6
		4N45		0.90 0.95	1.0 1.2	V	I_F = 1.0 mA, I_{OL} = 2.5 mA I_F = 10 mA, I_{OL} = 20 mA		
Logic High Output Current	I_{OH}*	4N46		0.001	100	μA	I_F = 0 mA, V_O = 18 V		6
		4N45		0.001	250	μA	I_F = 0 mA, V_O = 5 V		
Input Forward Voltage	V_F			1.4	1.7* 1.75	V	T_A = 25°C, I_F = 1.0 mA	1	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.0 mA		
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10 μA		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		
Input-Output Insulation	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C		7
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 VDC		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		7

Switching Specifications

(Over recommended temperature T_A = 0°C to 70°C unless otherwise specified.) V_{CC} = 5.0 V.

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		80		μs	T_A = 25°C, I_F = 0.5 mA, R_L = 10 kΩ	5, 6 7, 8 10, 12	6
	t_{PHL}		5	50*	μs	T_A = 25°C, I_F = 10 mA, R_L = 2.2 kΩ		8
				60				
Propagation Delay Time to Logic High at Output	t_{PLH}		1500		μs	T_A = 25°C, I_F = 10 mA, R_L = 10 kΩ	5, 6 7, 8 10, 12	6
	t_{PLH}		150	500*	μs	T_A = 25°C, I_F = 10 mA, R_L = 220 kΩ		8
				600				
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$		500		V/μs	I_F = 0 mA, R_L = 10 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}	9	9
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$		500		V/μs	I_F = 1.0 mA, R_L = 10 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}	9	9

*JEDEC Registered Data.

**All typicals at T_A = 25°C, unless otherwise noted.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

NOTES:
1. Derate linearly above 50° C free-air temperature at a rate of 0.4mA/° C.
2. Derate linearly above 50° C free-air temperature at a rate of 0.7mW/° C.
3. Derate linearly above 25° C free-air temperature at a rate of 0.8mA/° C.
4. Derate linearly above 25° C free-air temperature at a rate of 1.5mW/° C.
5. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Pin 6 Open.
7. Device considered a two-terminal device: Pins 1, 2, 3 shorted together and Pins 4, 5, and 6 shorted together.
8. Use of a resistor between pin 4 and 6 will decrease gain and delay time. (See Figures 10 and 12).
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.5V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 2.5V$).

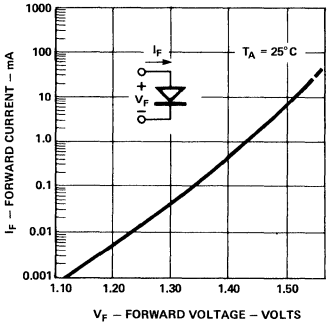


Figure 1. Input Diode Forward Current vs. Forward Voltage.

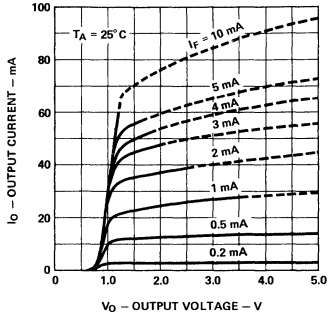


Figure 2. Typical DC Transfer Characteristics.

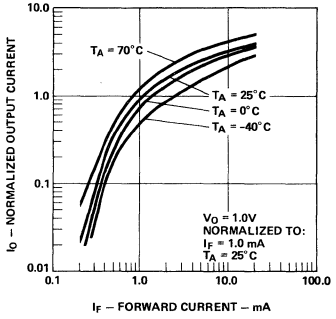


Figure 3. Output Current vs. Input Current.

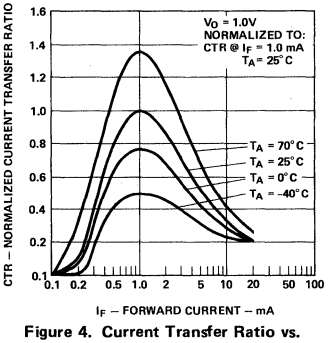


Figure 4. Current Transfer Ratio vs. Input Current.

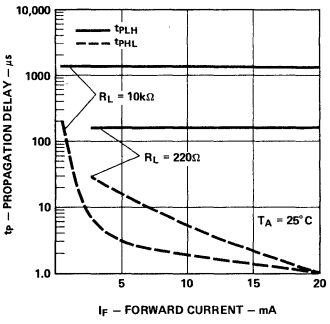


Figure 5. Propagation Delay vs. Forward Current.

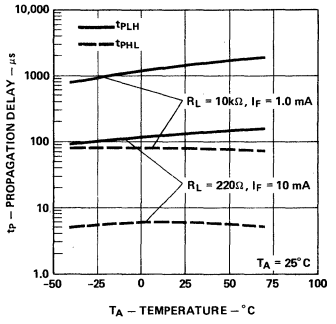


Figure 6. Propagation Delay vs. Temperature.

OPTOCOUPLERS

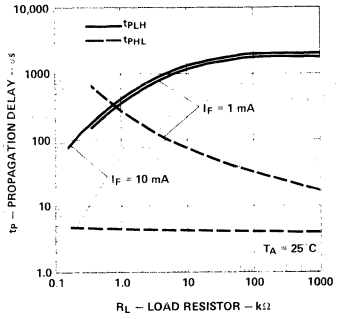
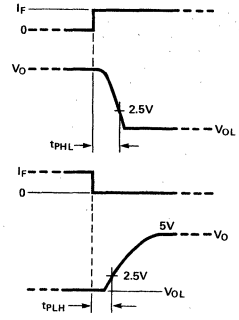


Figure 7. Propagation Delay vs Load Resistor.



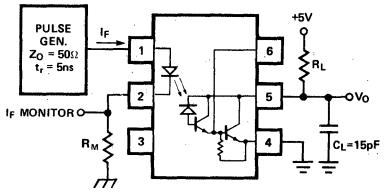
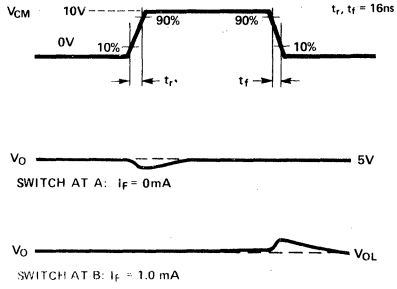


Figure 8. Switching Test Circuit



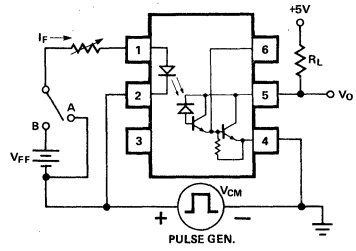


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

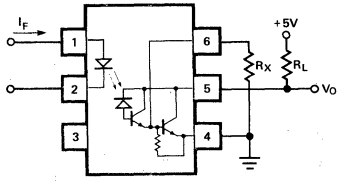


Figure 10. External Base Resistor, R_X

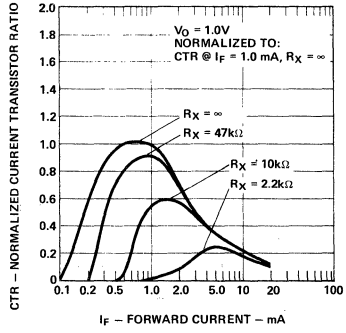


Figure 11. Effect of R_X On Current Transfer Ratio

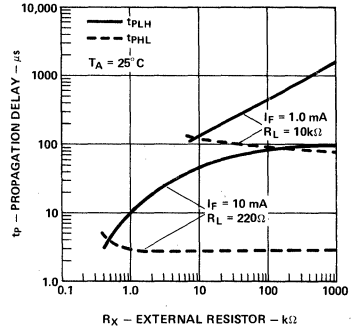
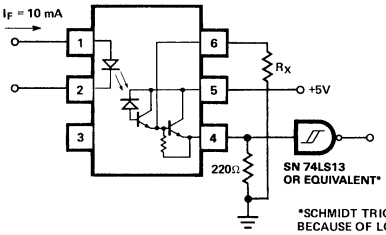


Figure 12. Effect of R_X On Propagation Delay

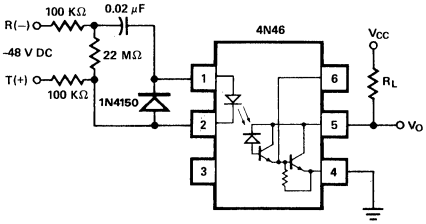
Applications



R_X (kΩ)	t_{PHL} (μs)	t_{PLH} (μs)
∞	5	320
100	5	200
47	5	140
20	6	80
10	6	45

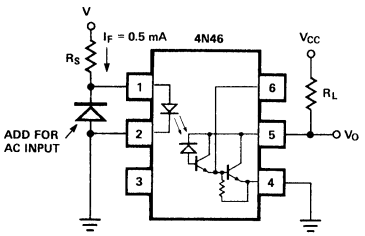
*SCHMIDT TRIGGER RECOMMENDED BECAUSE OF LONG t_r, t_f.

TTL Interface



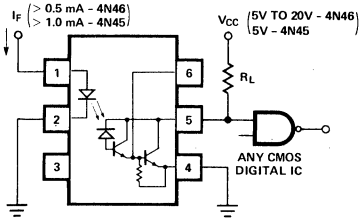
NOTE: AN INTEGRATOR MAY BE REQUIRED AT THE OUTPUT TO ELIMINATE DIALING PULSES AND LINE TRANSIENTS.

Telephone Ring Detector

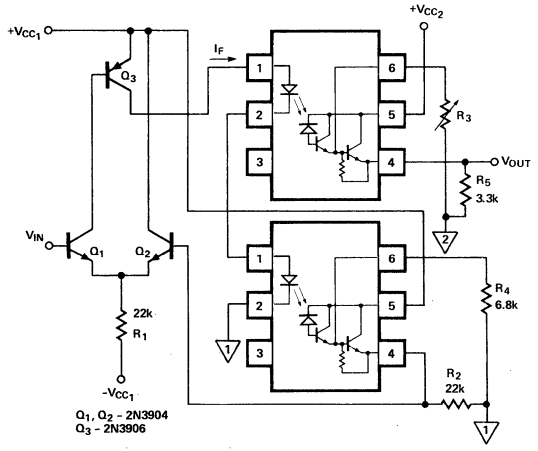


V (Vdc or Vrms)	R_S	V • I_F (mW)
24	47kΩ	11
48	100kΩ	22
115	220kΩ	62
230	470kΩ	113

Line Voltage Monitor



CMOS Interface



Analog Signal Isolation

CHARACTERISTICS

$R_{IN} \approx 30M\Omega$, $R_{OUT} \approx 50\Omega$
$V_{IN(MAX.)} = V_{CC_1} - 1V$, LINEARITY BETTER THAN 5%

DESIGN COMMENTS

R_1 - NOT CRITICAL $\left(\ll \frac{V_{IN\ (MAX.)} - (-V_{CC_1}) - V_{BE}}{I_{F\ (MAX.)}}\right) h_{FE}\ Q_3$

R_2 - NOT CRITICAL (OMIT IF 0.2 TO 0.3V OFFSET IS TOLERABLE)

$R_4 > \frac{V_{IN\ (MAX.)} + V_{BE}}{1\ mA}$

$R_5 > \frac{V_{IN\ (MAX.)}}{2.5\ mA}$

NOTE: ADJUST R_3 SO $V_{OUT} = V_{IN}$ AT $V_{IN} = \frac{V_{IN\ (MAX.)}}{2}$

HEWLETT PACKARD

Small Outline Low Input Current, High Gain Optocouplers

Technical Data

HCPL-0700
HCPL-0701

Features

- **Surface Mountable**
- **Industry Standard SOIC-8 Footprint**
- **Compatible With Infrared Vapor Phase Reflow and Wave Soldering Processes**
- **High Current Transfer Ratio – 2000% Typical**
- **Low Input Current Requirement – 0.5 mA**
- **TTL Compatible Output – 0.1 V V_{OL} Typical**
- **Guaranteed ac and dc Performance Over Temperature 0°C to 70°C**
- **Base Access Allows Gain Bandwidth Adjustment**
- **High Output Current – 60 mA**
- **Recognized Under The Component Program Of U.L. (File No. E55361) For Dielectric Withstand Proof Test Voltage Of 2500 VAC, 1 Minute**

Description

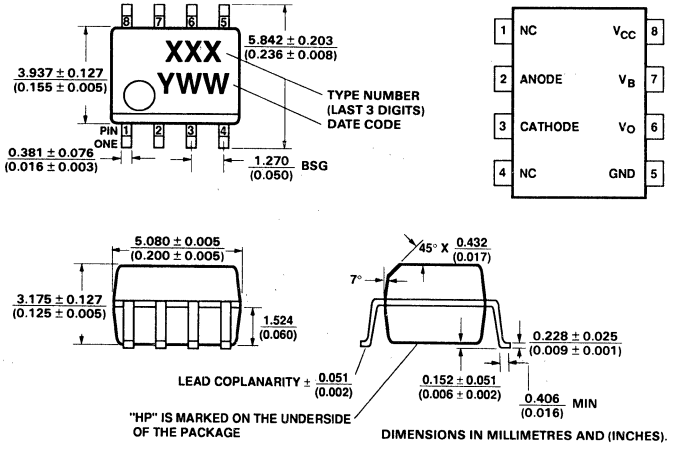
These small outline, low input current, high gain optocouplers are single channel devices in an industry standard SOIC-8 footprint. They are electrically equivalent to the following HP optocouplers:

Small Outline	Standard DIP
HCPL-0700	6N138
HCPL-0701	6N139

The SOIC-8 package does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

These high gain series couplers use a Light Emitting Diode and an integrated high gain photodetector to provide extremely high current transfer

Outline Drawing*



CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

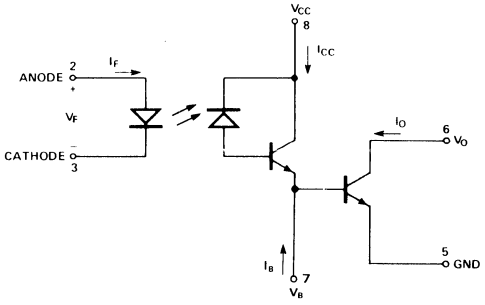
ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

The HCPL-0701 is for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70°C operating range for only 0.5 mA of LED current.

The HCPL-0700 is designed for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70°C for an LED current of 1.6 mA [1 TTL Unit Load (U.L.)]. A 300% minimum CTR enables operation with 1 U.L. out with a 2.2 kΩ pull-up resistor.

Selection for lower input currents down to 250 μA is available upon request.

Schematic



Applications

- **Ground Isolate Most Logic Families – TTL/TTL, CMOS/TTL, CMOS/CMOS, LSTTL/TTL, CMOS/LSTTL**
- **Low Input Current Line Receiver – Long Line or Party Line**
- **EIA RS-232C Line Receiver**
- **Telephone Ring Detector**
- **117 V ac Line Voltage Status Indicator – Low Input Power Dissipation**
- **Low Power Systems – Ground Isolation**

Absolute Maximum Ratings

(No Derating Required Up To 85°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Infrared and Vapor Phase Reflow Temperature ..... 215°C for 90 s
Average Input Current – I_F ..... 20 mA
Peak Input Current – I_F ..... 40 mA
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F ..... 1.0 A
(≤1 μs pulse width, 300 pps)
Reverse Input Voltage – V_R ..... 5 V
Input Power Dissipation ..... 35 mW
Output Current – I_O (Pin 6) ..... 60 mA
Emitter-Base Reverse Voltage (Pin 5-7) ..... 0.5 V
Supply and Output Voltage – V_{CC} (Pin 8-5), V_O (Pin 6-5)
HCPL-0700 ..... -0.5 V to 7 V
HCPL-0701 ..... -0.5 V to 18 V
Output Power Dissipation ..... 100 mW

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C), unless otherwise specified. (See note 7.)

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	HCPL-0701	400 500	2000 1600	3500 2600	%	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V	2, 3	1, 2, 4
		HCPL-0700	300	1600	2600	%	I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}	HCPL-0701		0.1 0.1 0.2	0.4 0.4 0.4	V	I_F = 1.6 mA, I_O = 8 mA, V_{CC} = 4.5 V I_F = 5 mA, I_O = 15 mA, V_{CC} = 4.5 V I_F = 12 mA, I_O = 24 mA, V_{CC} = 4.5 V	1	2
		HCPL-0700		0.1	0.4	V	I_F = 1.6 mA, I_O = 4.8 mA, V_{CC} = 4.5 V		
Logic High Output Current	I_{OH}	HCPL-0701		0.05	100	µA	I_F = 0 mA, V_O = V_{CC} = 18 V		2
		HCPL-0700		0.1	250	µA	I_F = 0 mA, V_O = V_{CC} = 7 V		
Logic Low Supply Current	I_{CCL}			0.4	1.5	mA	I_F = 1.6 mA, V_O = Open, V_{CC} = 18 V		2
Logic High Supply Current	I_{CCH}			0.01	10	µA	I_F = 0 mA, V_O = Open, V_{CC} = 18 V		2
Input Forward Voltage	V_F			1.4	1.7 1.75	V	T_A = 25°C, I_F = 1.6 mA	4	
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.6 mA		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		
Input-Output Insulation	V_{ISO}	2500				V_{RMS}	RH ≤ 50%, t = 1 min.		3
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 V dc		3
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		3

*All typicals are at T_A = 25°C and V_{CC} = 5 V, unless otherwise noted.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	HCPL-0701		5	25	µs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 6, 7	2, 4
					30				
				0.2	1		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω		
					2				
		HCPL-0700		1.6	10		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ		
					15				
Propagation Delay Time to Logic High at Output	t_{PLH}	HCPL-0701		18	60	µs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 6, 7	2, 4
					90				
				2	7		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω		
					10				
		HCPL-0700		10	35		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ		
					50				
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$			500		V/µs	I_F = 0 mA, R_L = 2.2 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}	8	5, 6
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$			500		V/µs	I_F = 1.6 mA, R_L = 2.2 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}	8	5, 6

*All typicals are at T_A = 25°C.

Notes:

1. DC CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
2. Pin 7 open.
3. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
4. Use of a resistor between pin 5 and 7 will decrease gain and delay time. See Application Note 951-1 for more details.
5. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
6. In applications where dV/dt may exceed 50,000 V/µs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is R_{CC} = 220 Ω.
7. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 is recommended.

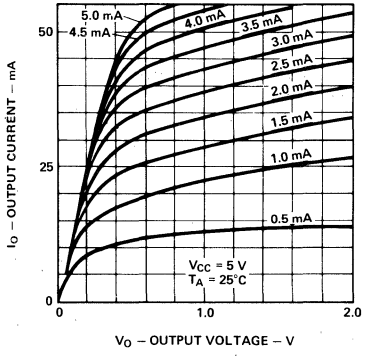


Figure 1. HCPL-0700/0701 DC Transfer Characteristics.

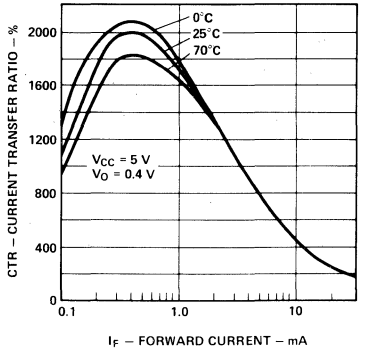


Figure 2. Current Transfer Ratio vs. Forward Current HCPL-0700/0701.

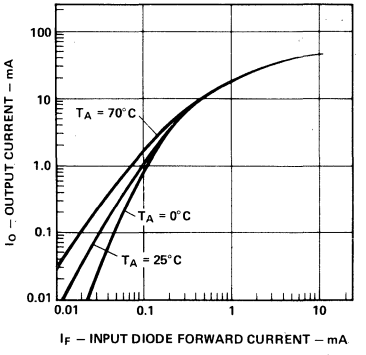


Figure 3. HCPL-0700/0701 Output Current vs. Input Diode Forward Current.

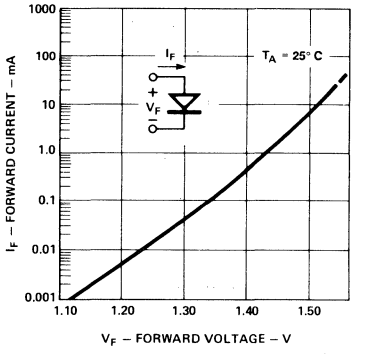


Figure 4. Input Diode Forward Current vs. Forward Voltage.

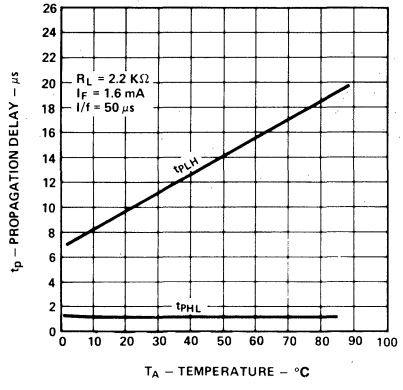


Figure 5. Propagation Delay vs. Temperature.

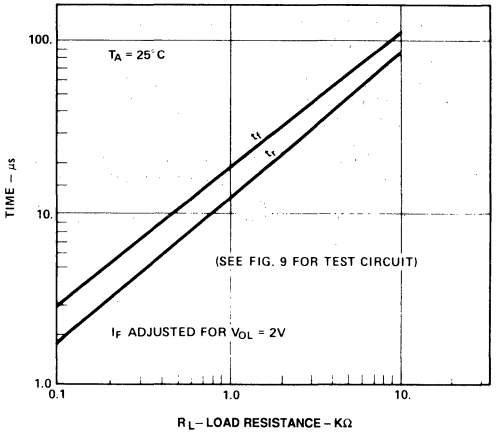


Figure 6. Non-Saturated Rise and Fall Times vs. Load Resistance.

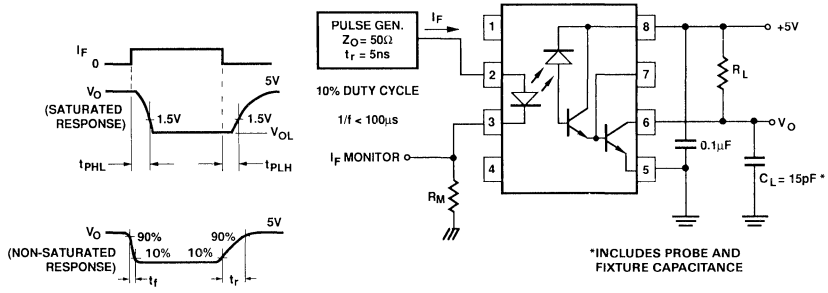


Figure 7. Switching Test Circuit.

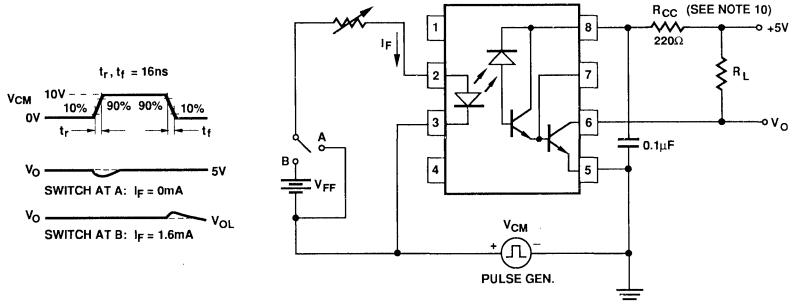


Figure 8. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

Low Input Current, High Gain Optocouplers

Technical Data

CNW138
CNW139

Features

- 5000 Vrms/1 Minute Insulation Withstand Capability
- Worldwide Safety Approval
  UL1577 (File No. E55361)
  VDE 883/884/804/805/806/860/750
  IEC 65/380/950/335/435/601
  BS 415/7002/6301
- High Current Transfer Ratio – 3000% Typical
- Low Input Current Requirement – 0.5 mA
- TTL Compatible Output – 0.1 V V_{OL} Typical
- Performance Guaranteed Over Temperature 0°C to 70°C
- Base Access Allows Gain Bandwidth Adjustment
- High Output Current – 60 mA
- Pin Compatible with 6N138/9

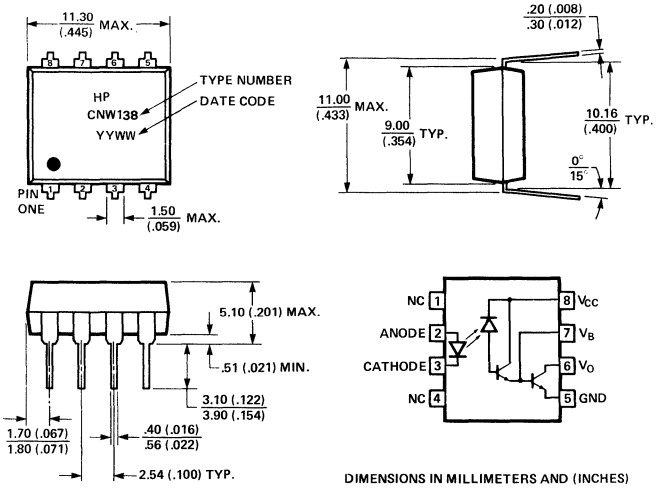
Applications

- High Voltage Insulation
- Low Input Current Line Receiver
- Ground Isolation - TTL/TTL, CMOS/TTL, CMOS/CMOS, LSTTL/TTL, CMOS/LSTTL
- EIA RS-232C Line Receiver
- Telephone Ring Detector
- AC Line Voltage Sensing
- Low Power Systems

Description

These high-voltage, high-gain optocouplers use an AlGaAs LED and an integrated high gain photodetector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

Package Outline



DIMENSIONS IN MILLIMETERS AND (INCHES)

A widebody encapsulation is used to provide creepage and clearance dimensions suitable for safety approval by regulatory agencies worldwide.

The CNW139 is for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70°C operating range for only 0.5 mA of LED current.

The CNW138 is designed for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70°C for an LED current of 1.6 mA (1 TTL load). A 300% minimum CTR enables operation with a fanout of 1 TTL Load using a 2.2 kΩ pull-up resistor.

Regulatory Information

The CNW138/9 features a wide body DIL 8 encapsulation. This package was specifically designed to meet regulatory insulation requirements worldwide. The CNW138/9 has been approved by the following organizations:

UL – Covered under UL component recognition FILE E55361

VDE – Approved according to VDE 0883/6.80
VDE 0884/08.87 certification pending
Reference voltage (VDE 0110b Tab. 4):
500 V AC/600 V DC
Complied for reinforced insulation at 250 V AC with:
DIN IEC 380/VDE 0806/8.81
DIN IEC 435/VDE 0805 "ENTWURF" Nov 84
DIN 57804/VDE 0804/1.83 (insulation group C)
DIN VDE 0860/8.86/HD 195 S4
DIN IEC 601 Teil 1/VDE 0750 Teil 1/5.82

NORDIC – Tested for applications (reinforced insulation) – Class II applications for plugable apparatus in normal tight execution.
-SETI-SEMKO-NEMKO-DEMKO-According to IEC 65-IEC380-IEC950-IEC335

BSI – Certification according to BS415:1979, BS7002:1989 and BS6301:1987 pending

BABT – Certification pending

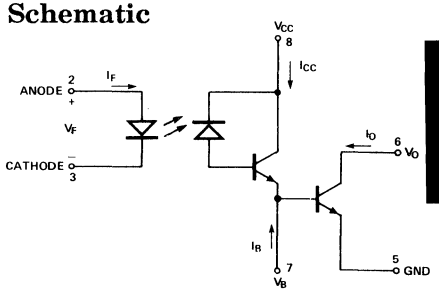
Absolute Maximum Ratings

Storage Temperature	-55°C to +150°C
Operating Temperature	-55°C to 85°C
Lead Solder Temperature	260°C for 10 s (up to seating plane)
Average Input Current – I_F	100 mA
Peak Transient Input Current – I_F	1.0 A (≤1 µs pulse width, 300 pps)
Reverse Input Voltage – V_R	5 V
Input Power Dissipation (up to 70°C)	250 mW*
Output Current – I_O (Pin 6)	60 mA
Emitter-Base Reverse Voltage (Pin 5-7)	0.5 V
Supply and Output Voltage – V_{CC} (Pin 8-5), V_O (Pin 6-5)	
CNW138	-0.5 to 7 V
CNW139	-0.5 to 18 V
Output Power Dissipation	100 mW

*Derate at 5.0 mW/°C for operating temperatures above 70°C.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Schematic



VDE 0884 Insulation Characteristics – Pending Approval

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0109/12.83, Table 1 for rated mains voltage ≤ 600 V_{RMS} for rated mains voltage ≤ 1000 V_{RMS}		 I-IV I-III	
Climatic Classification		55/150/21	
Pollution Degree (DIN VDE 0109/12.83)		2	
Maximum Working Insulation Voltage	V_{IORM}	1000	V_{RMS}
Input to Output Test Voltage, Method b* V_{PR} = 1.6 x V_{IORM}, 100% Production Test with tp = 1 sec, Partial Discharge < 5 pC	V_{PR}	1600	V_{RMS}
Input to Output Test Voltage, Method a* V_{PR} = 1.2 x V_{IORM}, Type and sample test, tp = 60 sec, Partial Discharge < 5 pC	V_{PR}	1200	V_{RMS}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	8000	V_{PK}
Safety-Limiting Values (Maximum values allowed in the event of a failure, also see Figure 10) Case Temperature Current (Input Current I_F, P_{SI} = 0) Output Power (obtained by setting pin 8 = 5.5 V, pins 7, 6, 5 = ground)	 T_{SI} I_{SI} $P_{SI, OUTPUT}$	 175 400 700	 °C mA mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V	R_{IS}	≥ 10^9	ohm

*Refer to the front of the optocoupler section of the 1991 Designer's Catalog, under regulatory information, (VDE 0884) for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (clearance)	L(IO1)	9.6	mm	Measured from input terminals to output terminals
Min. External Tracking Path	L(IO2)	10.0	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (clearance)		1.0	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	volts	DIN IEC 112/VDE 0303 PART 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group (DIN VDE 0109)

Electrical Specifications

Over Recommended Temperature (T_A = 0°C to 70°C) unless otherwise specified. (See note 7.)

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	CNW139	400	4500		%	I_F = 0.5 mA; V_{CC} = 4.5 V, V_O = 0.4 V	1, 2, 3	1, 2
			500	3000			I_F = 1.6 mA		
			300	1600			I_F = 5.0 mA		
			200	850			I_F = 12 mA		
		CNW138	300	1500		%	I_F = 1.6 mA; V_{CC} = 4.5 V, V_O = 0.4 V		
Logic Low Output Voltage	V_{OL}	CNW139		0.1	0.4	V	I_F = 0.5 mA, I_O = 2 mA; V_{CC} = 4.5 V	1	2
							I_F = 1.6 mA, I_O = 8 mA		
							I_F = 5.0 mA, I_O = 15 mA		
							I_F = 12 mA, I_O = 24 mA		
		CNW138		0.1	0.4	V	I_F = 1.6 mA, I_O = 4.8 mA		
Logic High Output Current	I_{OH}	CNW139		0.10	100	µA	V_O = V_{CC} = 18 V; I_F = 0 mA		2
		CNW138		0.05	250		V_O = V_{CC} = 7 V		
Logic Low Supply Current	I_{CCL}			0.5	2	mA	I_F = 1.6 mA, V_O = Open, V_{CC} = 18 V	9	2
Logic High Supply Current	I_{CCH}			0.010	1	µA	I_F = 0 mA, V_O = Open V_{CC} = 18 V		2
Input Forward Voltage	V_F		1.25	1.4	1.70	V	T_A = 25°C; I_F = 1.6 mA	4, 8	
			1.10		1.80				
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			1.9		mV/°C	I_F = 1.6 mA		
Input Capacitance	C_{IN}			200		pF	f = 1 MHz, V_F = 0 V		
Input-Output Insulation Voltage	V_{ISO}		5000			V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C		3, 8
Resistance (Input-Output)	R_{I-O}		10^{12}	10^{13}		Ω	T_A = 25°C; V_{I-O} = 500 V_{DC}		3
			10^{11}				T_A = 100°C		
Capacitance (Input-Output)	C_{I-O}			0.4	0.6	pF	f = 1 MHz, T_A = 25°C		3

*All typicals at T_A = 25°C.

Switching Specifications

Over Recommended Temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	CNW139		7	25	µs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 11	2, 4
					30				
				0.3	1		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω	7, 11	
					1.1				
		CNW138		2	10		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ	6, 11	
					11				
Propagation Delay Time to Logic High at Output	t_{PLH}	CNW139		40	60	µs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 11	2, 4
					115				
				3.5	7		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω	7, 11	
					11				
		CNW138		20	35		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ	6, 11	
					70				
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$		500			V/µs	I_F = 0 mA, R_L = 2.2 kΩ, R_{CC} = 0 Ω, V_{CM} = 10 V, T_A = 25°C	12	5, 6
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$		500			V/µs	I_F = 1.6 mA, R_L = 2.2 kΩ, R_{CC} = 0 Ω, V_{CM} = 10 V, T_A = 25°C	12	5, 6

*All typicals are at T_A = 25°C.

Notes:

1. DC CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
2. Pin 7 Open.
3. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
4. Use of a resistor between pin 5 and 7 will decrease gain and delay time. See Application Note 951-1 for more details.
5. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e. V_O > 2.0 V) Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM} dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e. V_O < 0.8 V).
6. In applications where dV/dt may exceed 50,000 V/µs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is
$$R_{CC} \approx \frac{1V}{0.15\ I_F\ (mA)}\ k\Omega.$$
7. Use of a 0.1 mf bypass capacitor connected betweens pin 5 and 8 is recommended for operation.
8. Each product is tested by applying an isolation test voltage of 6000 Vrms for 2 seconds. This test is in accordance with UL1577 and is performed in addition to the tests shown in the VDE 0884 INSULATION CHARACTERISTICS TABLE.

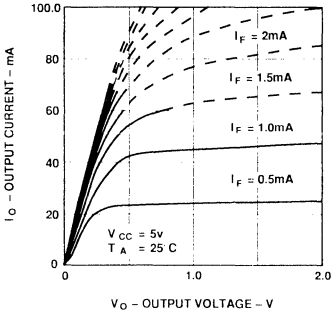


Figure 1. CNW138/9 DC Transfer Characteristics.

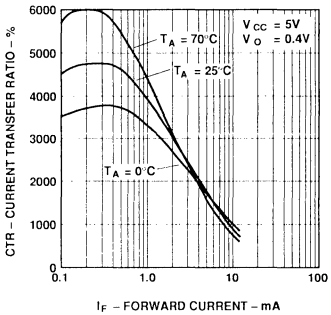


Figure 2. Current Transfer Ratio vs. Forward Current CNW138/9.

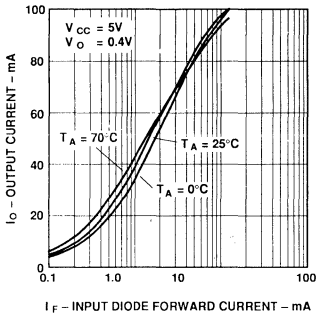


Figure 3. CNW 138/9 Output vs. Input Diode Forward Current.

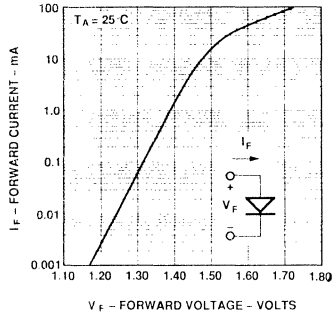


Figure 4. Input Diode Forward Current vs. Forward Voltage.

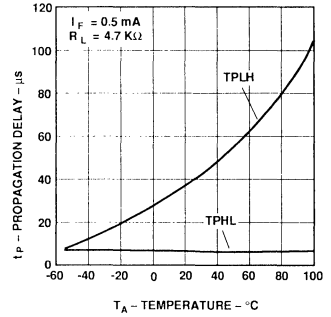


Figure 5. Propagation Delay vs. Temperature.

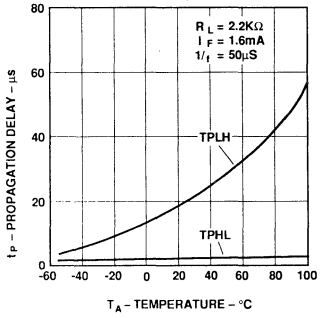


Figure 6. Propagation Delay vs. Temperature.

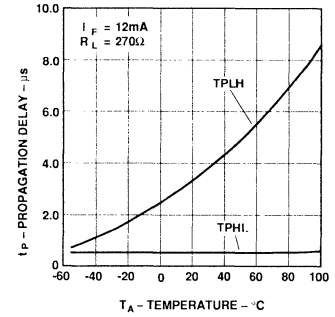


Figure 7. Propagation Delay vs. Temperature.

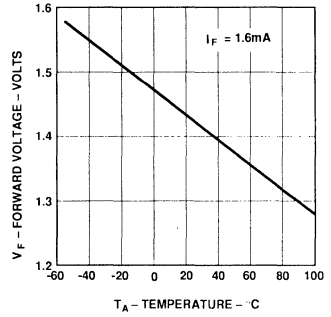


Figure 8. Forward Voltage vs. Temperature.

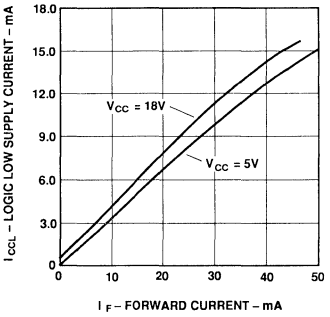


Figure 9. Logic Low Supply Current vs. Forward Current, CNW139.

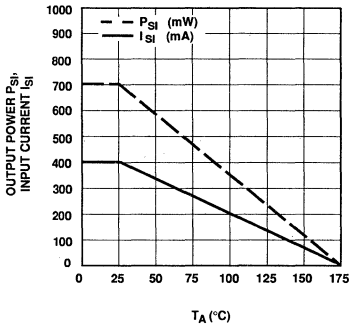


Figure 10. Dependence of Safety Maximum Ratings with Ambient Temperature.

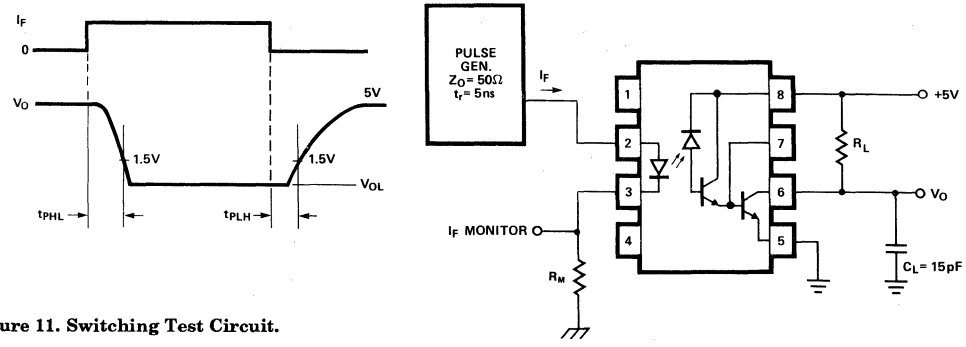


Figure 11. Switching Test Circuit.

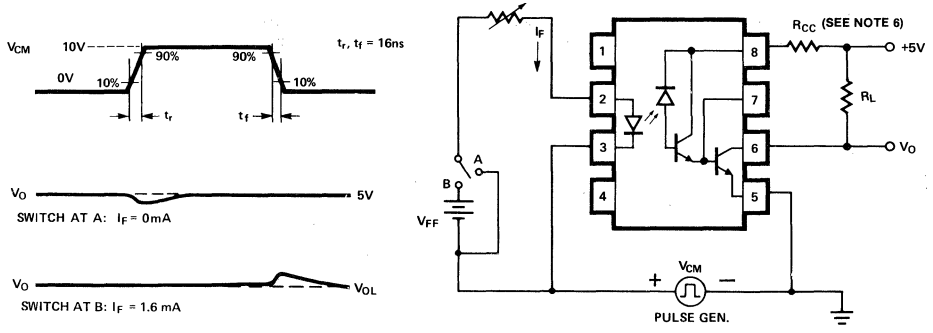


Figure 12. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

High Speed CMOS Optocoupler

Technical Data

HCPL-7100

Features

- **CMOS IC Technology**
- **Compatibility with All +5 V CMOS and TTL Logic Families**
- **No External Components Required for Logic Interface**
- **High Speed: 15 MBd Guaranteed**
- **Low Power Consumption**
- **World Wide Safety Approval**
  UL 1577
  VDE 0884/0700/0804/ 0860/0160
  EN 60 950
- **3-State Output**
- **3750 Vac/1 Minute Dielectric Withstand**

Applications

- **Multiplexed Data Transmission**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Instrument Input/Output Isolation**
- **Motor Control**
- **Power Inverter**

Description

The HCPL-7100 optocoupler combines the latest CMOS IC technology, a new high-speed high-efficiency AlGaAs LED, and an optimized light coupling system to achieve outstanding performance with very low power consumption. It requires only two bypass capacitors for complete CMOS/TTL compatibility.

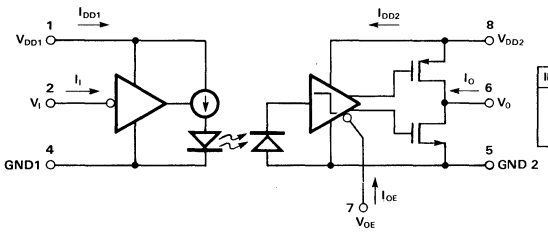
Basic building blocks of the HCPL-7100 are a CMOS LED driver IC, an AlGaAs LED, and and a CMOS detector IC. A CMOS or TTL logic input signal controls the LED driver IC which supplies current to the LED. The detector IC incorporates an integrated photodiode, a high-speed transimpedance amplifier and a voltage comparator with hysteresis. The 3-state output is CMOS and TTL compatible and is controlled by the output enable pin, V_{OE}.

The HCPL-7100 consumes very little power, due to the CMOS IC technology and the light coupling system. The entire optocoupler typically uses only 10 mA of supply current, including the LED current.

World wide safety approval and 3750 Vac/1 minute dielectric withstand is achieved with a new packaging process.

The HCPL-7100 provides the user with an easy-to-use CMOS or TTL compatible optocoupler ideally suited for a variety of applications where high speed and low power consumption are desired.

Schematic



TRUTH TABLE (POSITIVE LOGIC)

INPUT	ENABLE	OUTPUT
H	H	Z
L	H	Z
H	L	H
L	L	L

CAUTION: The small device geometries inherent to the design of this CMOS component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

OPTOCOUPLERS

Regulatory Information

The HCPL-7100 has been approved by the following organizations:

UL

Covered under UL component recognition FILE E55361

VDE

Approved according to VDE 0884/08.87

Can be used for safe electrical separation between AC mains and SELV (safety extra-low voltage) in equipment according to the following specifications:

DIN VDE 0700 part 1/09.86
DIN VDE 0804/05.89
DIN VDE 0860/05.89/HD 195 S4
DIN VDE 0160/05.88
EN 60 950/09.87 (CENELEC)

Reference voltage (VDE 0110b Tab 4): 650 Vac

VDE 0884 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0109/12.83, Table 1 for rated mains voltage ≤300 V_{RMS} for rated mains voltage ≤600 V_{RMS}		 I-IV I-III	
Climatic Classification		40/85/21	
Pollution Degree (DIN VDE 0109/12.83)**		2	
Maximum Working Insulation Voltage	V_{IORM}	600	V_{RMS}
Input to Output Test Voltage, Method b* V_{PR} = 1.6 x V_{IORM}, Production test with t_p = 1 sec, Partial discharge < 5 pC	V_{PR}	960	V_{RMS}
Input to Output Test Voltage, Method a* V_{PR} = 1.2 x V_{IORM}, Type and sample test, t_p = 60 sec, Partial discharge < 5 pC	V_{PR}	720	V_{RMS}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	6000	V_{PEAK}
Safety-limiting values (Maximum values allowed in the event of a failure, also see Figure 11) Case Temperature Input Power (obtained by setting pin 1 = 5.5 V, pin 2 = 0.5 V, pin 4 = gnd) Output Power (obtained by setting pin 8 = 5.5 V, pins 7, 6, 5 = ground)	 T_{SI} $P_{SI, Input}$ $P_{SI, Output}$	 175 50 220	 °C mW mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V	R_{IS}	≥10E11	Ohm

*Refer to the front of the optocoupler section in the 1991 Optoelectronics Designer's Catalog, under regulatory information, (VDE 0884) for a detailed description.

**This part may also be used in Pollution Degree 3 environments where the rated mains voltage is ≤ 300 V_{RMS} (per DIN VDE 0109/12.83).

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External air gap (clearance)	L (IO1)	>7	mm	Measured from input terminals to output terminals
Min. External tracking path (creepage)	L (IO2)	8.0	mm	Measured from input terminals to output terminals
Min. Internal plastic gap (clearance)		0.5	mm	Through insulation distance conductor to conductor
Tracking resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		III a		Material Group DIN VDE 0109

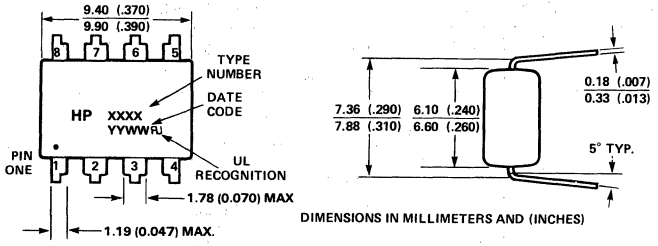
Absolute Maximum Ratings

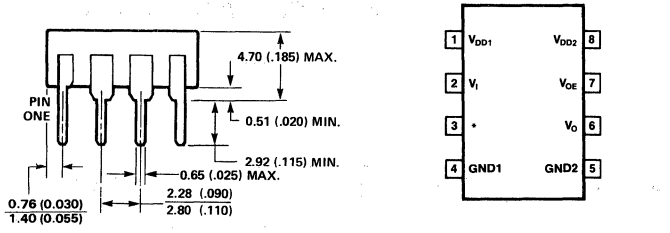
Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-55	125	°C
Supply Voltages	$V_{DD1,2}$	0.0	5.5	V
Input Voltage	V_I	-0.5	V_{DD1} + 0.5	V
Output Voltage	V_O	-0.5	V_{DD2} + 0.5	V
Output Enable Voltage	V_{OE}	-0.5	V_{DD2} + 0.5	V
Average Output Current	I_O		25	mA
Package Power Dissipation	P_{PD}		125	mW
Operating Temperature	T_A	-40	85	°C
Lead Solder Temperature	260°C for 10 s, 1.6 mm below seating plane			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Operating Temperature	T_A	-40	85	°C	Ambient Temperature
Supply Voltages	$V_{DD1,2}$	4.5	5.5	V	
Logic High Input Voltage	V_{IH}	2.0	V_{DD1}	V	
Logic Low Input Voltage	V_{IL}	0.0	0.8	V	
Logic High Output Enable Voltage	V_{OEH}	2.0	V_{DD2}	V	Output in high impedance state
Logic Low Output Enable Voltage	V_{OEL}	0.0	0.8	V	Output enabled
Input Signal Rise and Fall Times	t_r, t_f		1	ms	
TTL Fanout	N		6		Standard Loads

Outline Drawing





***Pin 3 is the anode of the internal LED and must be left unconnected for guaranteed data sheet performance.**

Electrical Specifications

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Logic Low Input Supply Current	I_{DD1L}		5.2	10.0	mA	V_{DD1} = 5.5 V $V_I = V_{IL}$		1
Logic High Input Supply Current	I_{DD1H}		0.3	0.6	mA	V_I = 4.5 V; V_{DD1} = 5.5 V		1
			0.9	1.6		V_I = 2.0 V; V_{DD1} = 5.5 V		
Logic Low Output Supply Current	I_{DD2L}		5.0	9.0	mA	V_{DD2} = 5.5 V $V_{OE} = V_{OEL}$ $V_I = V_{IL}$		
Logic High Output Supply Current	I_{DD2H}		5.2	9.0	mA	V_{DD2} = 5.5 V $V_{OE} = V_{OEL}$ I_O = 0 mA $V_I = V_{IH}$		
Tri-State Output Supply Current	I_{DD2Z}		5.1	9.0	mA	V_{OE} = 4.5 V; V_{DD2} = 5.5 V		
			5.6	10.0		V_{OE} = 2.0 V; V_{DD2} = 5.5 V		
Input Current	I_I	-1		1	µA	$V_I = V_{DD1}$ or GND V_{DD1} = 5.5 V		
Output Enable Current	I_{OE}	-1		1	µA	$V_{OE} = V_{DD2}$ or GND V_{DD2} = 5.5 V		
Logic High Output Voltage	V_{OH}	4.4	5.0		V	V_{DD2} = 4.5 V I_O = -20 µA $V_I = V_{IH}$ $V_{OE} = V_{OEL}$	6	
Logic High Output Voltage	V_{OH}	4.0	4.8		V	V_{DD2} = 4.5 V I_O = -4.0 mA $V_I = V_{IH}$ $V_{OE} = V_{OEL}$	6	

Electrical Specifications (cont.)

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Logic High Output Voltage	V_{OH}	3.7	4.7		V	V_{DD2} = 4.5 V I_O = -6.0 mA $V_I = V_{IH}$, $V_{OE} = V_{OEL}$	6	
Logic High Output Current	I_{OH}	-7.5	-25		mA	V_{DD2} = 4.5 V V_O = 3.6 V $V_I = V_{IH}$, $V_{OE} = V_{OEL}$	6	
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	V_{DD2} = 4.5 V I_O = 20 µA $V_I = V_{IL}$, $V_{OE} = V_{OEL}$	5	
Logic Low Output Voltage	V_{OL}		0.1	0.3	V	V_{DD2} = 4.5 V I_O = 4.0 mA $V_I = V_{IL}$, $V_{OE} = V_{OEL}$	5	
Logic Low Output Voltage	V_{OL}		0.15	0.4	V	V_{DD2} = 4.5 V I_O = 6.0 mA $V_I = V_{IL}$, $V_{OE} = V_{OEL}$	5	
Logic Low Output Current	I_{OL}	10.5	23		mA	V_{DD2} = 4.5 V V_O = 0.6 V $V_I = V_{IL}$, $V_{OE} = V_{OEL}$	5	
High Impedance State Output Current	I_{OZ}	-5		5	µA	V_{DD2} = 5.5 V $V_{OE} = V_{OEH}$, $V_O = V_{DD2}$ or GND		
Insulation Voltage	V_{ISO}	3750			V_{RMS}	t = 1 minute RH ≤ 50% T_A = 25°C		2, 3
Input Capacitance	C_I		4.3		pF	f = 1 MHz		4
Input-Output Resistance	R_{I-O}		10^{13}		Ohms	V_{I-O} = 500 V_{DC}		2
Input-Output Capacitance	C_{I-O}		0.7		pF	f = 1 MHz		2

Switching Specifications

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output	t_{PHL}			70	ns	C_L = 50 pF CMOS Signal Levels	7	5, 6
				70	ns	C_L = 15 pF TTL Signal Levels		
Propagation Delay Time to Logic High Output	t_{PLH}			70	ns	C_L = 50 pF CMOS Signal Levels	7	5, 6
				70	ns	C_L = 15 pF TTL Signal Levels		
Pulse Width Distortion $\lvert t_{PHL}-t_{PLH} \rvert$	PWD			20	ns	C_L = 50 pF CMOS Signal Levels	7	6, 7
				20	ns	C_L = 15 pF TTL Signal Levels		
Data Rate		15			MBd	% PWD < 30%		8
Output Rise Time (10-90%)	t_R		12		ns	C_L = 50 pF CMOS Signal Levels	7	
Output Fall Time (90-10%)	t_F		8		ns	C_L = 50 pF CMOS Signal Levels	7	
Propagation Delay Time From Output Enabled to Logic High Output	t_{PZH}		13		ns	C_L = 50 pF CMOS Signal Levels	8	6
			12		ns	C_L = 15 pF TTL Signal Levels		
Propagation Delay Time From Output Enabled to Logic Low Output	t_{PZL}		11		ns	C_L = 50 pF CMOS Signal Levels	8	6
			10		ns	C_L = 15 pF TTL Signal Levels		
Propagation Delay Time From Logic High to Output Disabled	t_{PHZ}		12		ns	C_L = 50 pF CMOS Signal Levels	8	6
			12		ns	C_L = 15 pF TTL Signal Levels		

Switching Specifications (cont.)

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time From Logic Low to Output Disabled	t_{PLZ}		9		ns	C_L = 50 pF CMOS Signal Levels	8	6
			11		ns	C_L = 15 pF TTL Signal Levels		
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$	1000			V/µs	V_{CM} = 50 V $V_I = V_{IH}$ V_O > 3.2 V	9, 10	9
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	1000			V/µs	V_{CM} = 50 V $V_I = V_{IL}$ V_O < 0.8 V	9, 10	9
Input Dynamic Power Dissipation Capacitance	C_{PD1}		68		pF			10
Output Dynamic Power Dissipation Capacitance	C_{PD2}		10		pF			10

Notes:

1. The LED is OFF when the V_I is high and ON when V_I is low.
2. Device considered a two terminal device; pins 1-4 shorted together and pins 5-8 shorted together.
3. This is a proof test.
4. C_I is the capacitance measured at pin 2 (V_I).
5. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the V_I signal to the logic switching level of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the V_I signal to the logic switching level of the V_O signal.
6. The logic switching levels are 1.5 V for TTL signals (0-3 V) and 2.5 V for CMOS signals (0-5 V).
7. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD (percent pulse width distortion) is equal to PWD in ns divided by symbol duration (bit length) in ns.
8. Minimum data rate is calculated as follows: %PWD/PWD where %PWD is typically chosen by the design engineer (30% is common).
9. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining V_O > 3.2 V. CM_L is the maximum common mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
10. Unloaded dynamic power dissipation is calculated as follows: $C_{PD} \bullet V_{DD}^2 \bullet f + I_{DD} \bullet V_{DD}$ where f is switching frequency in MHz.

HCPL-7100 Application Information

The HCPL-7100 is extremely easy to use. Because the optocoupler uses high-speed CMOS IC technology, the inputs and output are fully compatible with all +5 V TTL and CMOS logic. TTL or CMOS logic can be connected directly to the inputs and output; no external interface circuitry is required.

As shown in Figure 1, the only external components required for proper operation are two ceramic bypass capacitors. Capacitor values should be between 0.01 µF and 0.1 µF. For each capacitor, the total lead length between both ends of the capacitor and the power-supply pins should not exceed 20 mm. Figure 2 illustrates the recommended printed circuit board layout for the HCPL-7100.

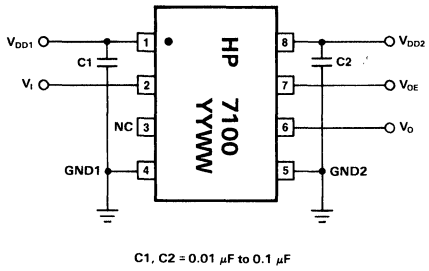


Figure 1. HCPL-7100 Recommended Application Circuit.

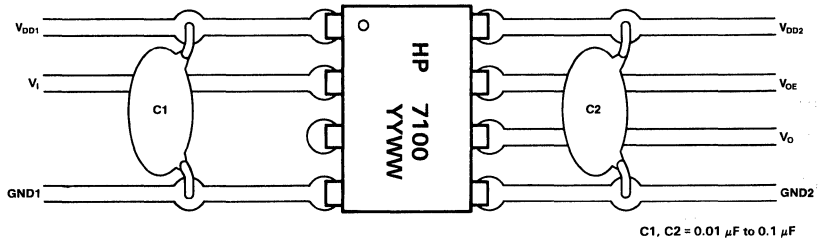


Figure 2. HCPL-7100 Recommended Printed Circuit Board Layout.

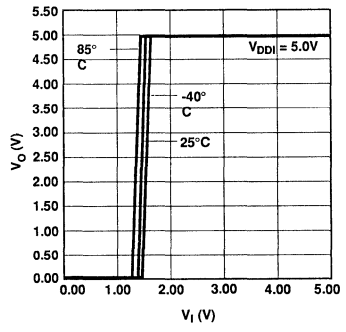


Figure 3. Typical Output Voltage vs. Input Voltage.

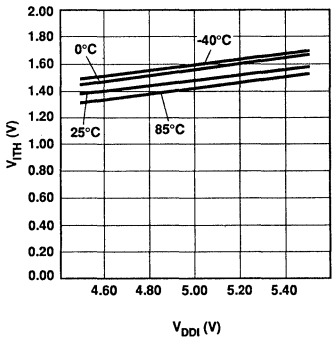


Figure 4. Typical Input Voltage Switching Threshold vs. Input Supply Voltage.

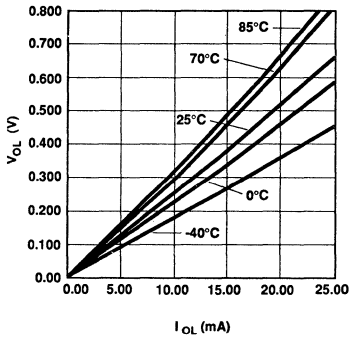


Figure 5. Typical Logic Low Output Voltage vs. Logic Low Output Current.

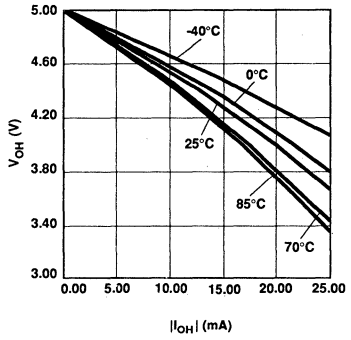


Figure 6. Typical Logic High Output Voltage vs. Logic High Output Current.

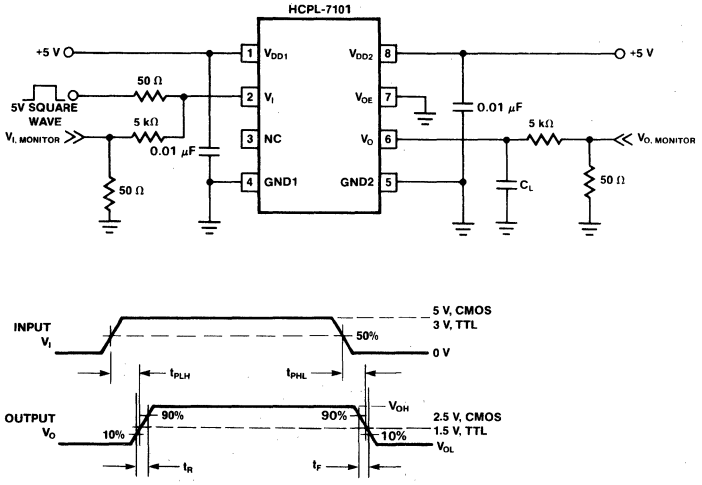


Figure 7. Test Circuit for Propagation Delay, Rise Time and Fall Time.

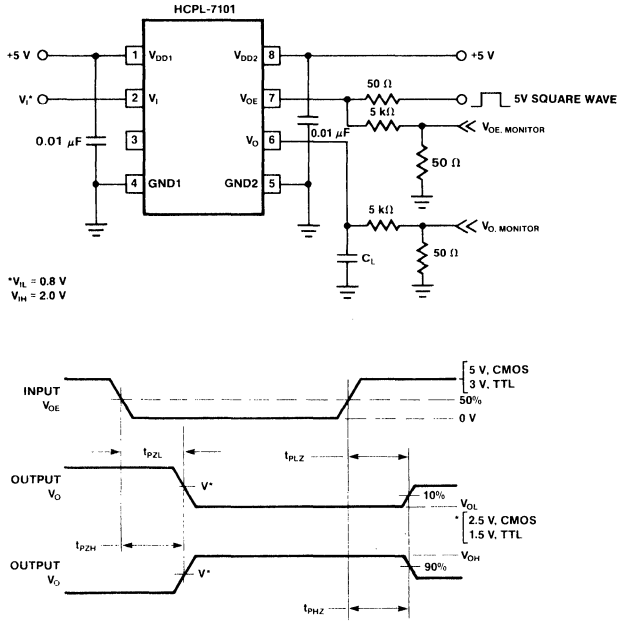


Figure 8. Test Circuit for 3-State Output Enable and Disable Propagation Delays.

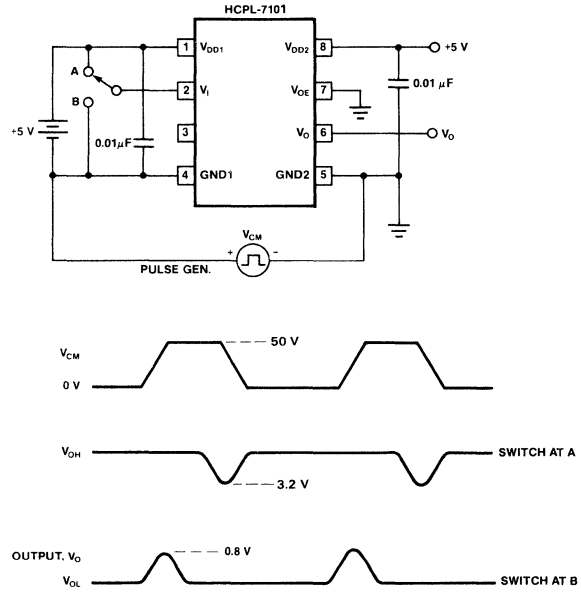


Figure 9. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

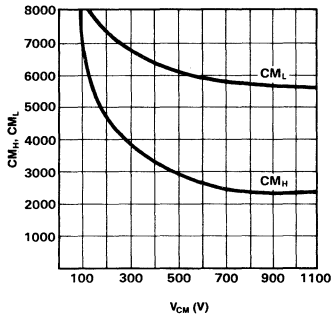


Figure 10. Typical Common Mode Transient Immunity vs. Common Mode Transient Voltage.

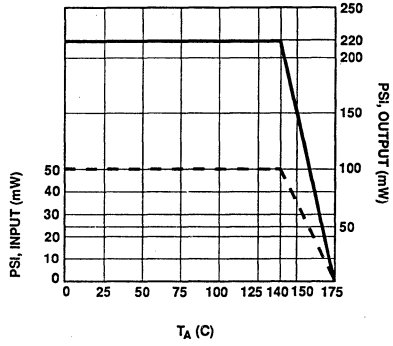


Figure 11. Dependence of Safety-Limiting Data on Ambient Temperature.

HEWLETT PACKARD

Ultra High Speed CMOS Optocoupler

Technical Data

HCPL-7101

Features

- **Ultra High Speed: 50 MBd Guaranteed**
- **Lowest Power-Delay Product Available**
- **CMOS IC Technology**
- **Compatible with All CMOS and TTL +5 V Logic Families**
- **No External Components Required for Logic Interface**
- **Low Power Consumption**
- **World Wide Safety Approval**
  UL 1577
  VDE 0884/0804/0160
- **2500 Vac/1 Minute Dielectric Withstand**
- **3-State Output**
- **High Common Mode Transient Immunity: >2000 V/μs @ 200 V Vcm**

Applications

- **Microprocessor System Interface**
- **Multiplexed Data Transmission**
- **Digital Isolation for A/D, D/A Conversion**
- **Computer-Peripheral Interface**
- **Isolated Line Receiver**

Description

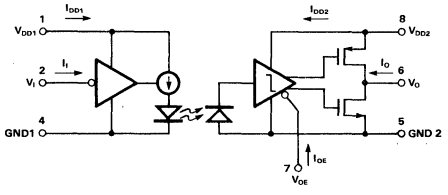
The HCPL-7101 ultra high-speed optocoupler utilizes CMOS IC technology, a new high-speed AlGaAs LED and an optimized light coupling system to achieve 50 MBd data rates with very low power consumption.

Both the LED driver IC and the detector IC have been designed using the state-of-the-art CMOS IC technology. The light coupling system and the high-speed high efficiency AlGaAs LED provide optimum light coupling from the LED to the integrated photodiode at minimal power levels. The LED driver IC can be controlled by either CMOS or TTL input logic signals. Pre-biasing and peaking circuitry in the driver IC ensure maximum speed from the LED. In addition, the internal LED drive current is compensated for LED degradation.

The detector IC incorporates an integrated photodiode, a high-speed transimpedance amplifier and a voltage comparator with hysteresis. The 3-state output is CMOS and TTL compatible and is controlled by the output enable pin, V_{OE}.

The HCPL-7101 provides the user with an easy-to-use ultra high-speed and low-power optocoupler. Compatibility with CMOS and TTL logic makes it ideally suited for a variety of applications.

Schematic



TRUTH TABLE (POSITIVE LOGIC)

INPUT	ENABLE	OUTPUT
H	H	Z
L	H	Z
H	L	H
L	L	L

OPTOCOUPLERS

CAUTION: The small device geometries inherent to the design of this CMOS component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Regulatory Information

The HCPL-7101 has been approved by the following organizations:

UL

Covered under UL component recognition FILE E55361

VDE

Approved according to VDE 0884/08.87

Can be used for safe electrical separation between AC mains and SELV (safety extra-low voltage) in equipment according to the following specifications:

DIN VDE 0804/05.89
DIN VDE 0160/05.88

Reference voltage (VDE 0110b Tab 4): 650 Vac

VDE 0884 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0109/12.83, Table 1 for rated mains voltage ≤300 V_{RMS} for rated mains voltage ≤600 V_{RMS}		 I-IV I-III	
Climatic Classification		40/85/21	
Pollution Degree (DIN VDE 0109/12.83)**		2	
Maximum Working Insulation Voltage	V_{IORM}	600	V_{RMS}
Input to Output Test Voltage, Method b* V_{PR} = 1.6 x V_{IORM}, Production test with t_p = 1 sec, Partial discharge < 5 pC	V_{PR}	960	V_{RMS}
Input to Output Test Voltage, Method a* V_{PR} = 1.2 x V_{IORM}, Type and sample test, t_p = 60 sec, Partial discharge < 5 pC	V_{PR}	720	V_{RMS}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	6000	V_{PEAK}
Safety-limiting values (Maximum values allowed in the event of a failure, also see Figure 15) Case Temperature Input Power (obtained by setting pin 1 = 5.5 V, pin 2 = 0.5 V, pin 4 = ground) Output Power (obtained by setting pin 8 = 5.5 V, pins 7, 6, 5 = ground)	 T_{SI} $P_{SI, Input}$ $P_{SI, Output}$	 175 50 220	 °C mW mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V	R_{IS}	≥10E11	Ohm

*Refer to the front of the optocoupler section in the 1991 Optoelectronics Designer's Catalog, under regulatory information, (VDE 0884) for a detailed description.

**This part may also be used in Pollution Degree 3 environments where the rated mains voltage is ≤ 300 V_{RMS} (per DIN VDE 0109/12.83).

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External air gap (clearance)	L (IO1)	>7	mm	Measured from input terminals to output terminals
Min. External tracking path (creepage)	L (IO2)	8.0	mm	Measured from input terminals to output terminals
Min. Internal plastic gap (clearance)		0.5	mm	Through insulation distance conductor to conductor
Tracking resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		III a		Material Group DIN VDE 0109

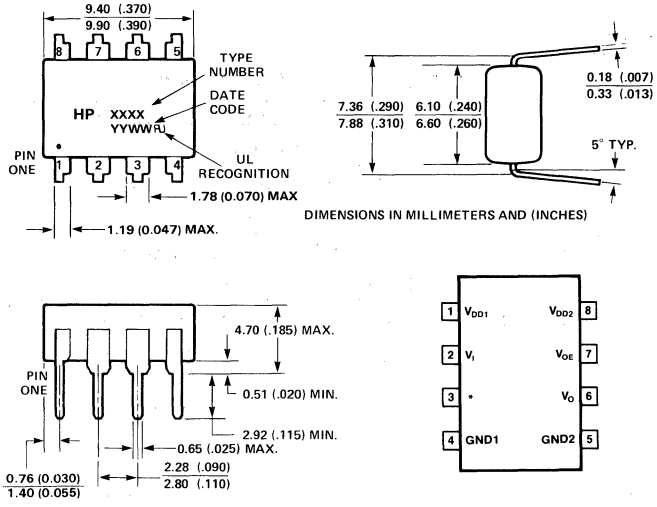
Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-55	125	°C
Supply Voltages	$V_{DD1,2}$	0.0	5.5	V
Input Voltage	V_I	-0.5	V_{DD1} + 0.5	V
Output Voltage	V_O	-0.5	V_{DD2} + 0.5	V
Output Enable Voltage	V_{OE}	-0.5	V_{DD2} + 0.5	V
Average Output Current	I_O		25	mA
Package Power Dissipation	P_{PD}		220	mW
Operating Temperature	T_A	-40	85	°C
Lead Solder Temperature	260°C for 10 s, 1.6 mm below seating plane			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Operating Temperature	T_A	-40	85	°C	Ambient Temperature
Supply Voltages	$V_{DD1,2}$	4.5	5.5	V	
Logic High Input Voltage	V_{IH}	2.0	V_{DD1}	V	
Logic Low Input Voltage	V_{IL}	0.0	0.8	V	
Logic High Output Enable Voltage	V_{OEH}	2.0	V_{DD2}	V	Output in high impedance state
Logic Low Output Enable Voltage	V_{OEL}	0.0	0.8	V	Output enabled
Input Signal Rise and Fall Times	t_r, t_f		1	ms	
TTL Fanout	N		6		Standard Loads

Outline Drawing



***Pin 3 is the anode of the internal LED and must be left unconnected for guaranteed data sheet performance.**

Electrical Specifications

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Logic Low Input Supply Current	I_{DD1L}		5.2	10.0	mA	V_{DD1} = 5.5 V $V_I = V_{IL}$		1
Logic High Input Supply Current	I_{DD1H}		0.3	0.6	mA	V_I = 4.5 V; V_{DD1} = 5.5 V		1
			0.9	1.6		V_I = 2.0 V; V_{DD1} = 5.5 V		
Logic Low Output Supply Current	I_{DD2L}		5.0	9.0	mA	V_{DD2} = 5.5 V $V_{OE} = V_{OEL}$ $V_I = V_{IL}$		
Logic High Output Supply Current	I_{DD2H}		5.2	9.0	mA	V_{DD2} = 5.5 V $V_{OE} = V_{OEL}$ I_O = 0 mA $V_I = V_{IH}$		
Tri-State Output Supply Current	I_{DD2Z}		5.1	9.0	mA	V_{OE} = 4.5 V; V_{DD2} = 5.5 V		
			5.6	10.0		V_{OE} = 2.0 V; V_{DD2} = 5.5 V		
Input Current	I_I	-1		1	µA	$V_I = V_{DD1}$ or GND V_{DD1} = 5.5 V		
Output Enable Current	I_{OE}	-1		1	µA	$V_{OE} = V_{DD2}$ or GND V_{DD2} = 5.5 V		
Logic High Output Voltage	V_{OH}	4.4	5.0		V	V_{DD2} = 4.5 V I_O = -20 µA $V_I = V_{IH}$ $V_{OE} = V_{OEL}$	6	

Electrical Specifications (cont.)

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Logic High Output Voltage	V_{OH}	4.0	4.8		V	V_{DD2} = 4.5 V I_O = -4.0 mA $V_I = V_{IH}$ $V_{OE} = V_{OEL}$	6	
Logic High Output Voltage	V_{OH}	3.7	4.7		V	V_{DD2} = 4.5 V I_O = -6.0 mA $V_I = V_{IH}$, $V_{OE} = V_{OEL}$	6	
Logic High Output Current	I_{OH}	-7.5	-25		mA	V_{DD2} = 4.5 V V_O = 3.6 V $V_I = V_{IH}$, $V_{OE} = V_{OEL}$	6	
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	V_{DD2} = 4.5 V I_O = 20 µA $V_I = V_{IL}$ $V_{OE} = V_{OEL}$	5	
Logic Low Output Voltage	V_{OL}		0.1	0.3	V	V_{DD2} = 4.5 V I_O = 4.0 mA $V_I = V_{IL}$, $V_{OE} = V_{OEL}$	5	
Logic Low Output Voltage	V_{OL}		0.15	0.4	V	V_{DD2} = 4.5 V I_O = 6.0 mA $V_I = V_{IL}$, $V_{OE} = V_{OEL}$	5	
Logic Low Output Current	I_{OL}	10.5	23		mA	V_{DD2} = 4.5 V V_O = 0.6 V $V_I = V_{IL}$, $V_{OE} = V_{OEL}$	5	
High Impedance State Output Current	I_{OZ}	-5		5	µA	V_{DD2} = 5.5 V $V_{OE} = V_{OEH}$, $V_O = V_{DD2}$ or GND		
Insulation Voltage	V_{ISO}	3750			V_{RMS}	t = 1 minute RH ≤ 50% T_A = 25°C		2, 3
Input Capacitance	C_I		4.3		pF	f = 1 MHz		4
Input-Output Resistance	R_{I-O}		10^{13}		Ohms	V_{I-O} = 500 V_{DC}		2
Input-Output Capacitance	C_{I-O}		0.7		pF	f = 1 MHz		2

Switching Specifications

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output	t_{PHL}		28	40	ns	C_L = 50 pF CMOS Signal Levels	7, 8	5, 6
				40	ns	C_L = 15 pF TTL Signal Levels		
Propagation Delay Time to Logic High Output	t_{PLH}		27	40	ns	C_L = 50 pF CMOS Signal Levels	7, 8	5, 6
				40	ns	C_L = 15 pF TTL Signal Levels		
Pulse Width Distortion $\lvert t_{PHL}-t_{PLH} \rvert$	PWD		2	6	ns	C_L = 50 pF CMOS Signal Levels	7, 9	6, 7
				6	ns	C_L = 15 pF TTL Signal Levels		
Data Rate		50	65		MBd	% PWD < 30%		8
Propagation Delay Skew	t_{PSK}			10	ns		10	9
Output Rise Time (10-90%)	t_R		10		ns	C_L = 50 pF CMOS Signal Levels	7	
Output Fall Time (90-10%)	t_F		7		ns	C_L = 50 pF CMOS Signal Levels	7	
Random Jitter	RJ		50		ps rms	V_I = 0-5 V square wave, f = 25 MHz, input rise/fall time = 5 ns. R_L = 10 kΩ, C_L = 5 pF. TTL threshold levels.		
Propagation Delay Time From Output Enabled to Logic High Output	t_{PZH}		13		ns	C_L = 50 pF CMOS Signal Levels	12	6
			12		ns	C_L = 15 pF TTL Signal Levels		
Propagation Delay Time From Output Enabled to Logic Low Output	t_{PZL}		11		ns	C_L = 50 pF CMOS Signal Levels	12	6
			10		ns	C_L = 15 pF TTL Signal Levels		
Propagation Delay Time From Logic High to Output Disabled	t_{PHZ}		12		ns	C_L = 50 pF CMOS Signal Levels	12	6
			12		ns	C_L = 15 pF TTL Signal Levels		

Switching Specifications (cont.)

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time From Logic Low to Output Disabled	t_{PLZ}		9		ns	C_L = 50 pF CMOS Signal Levels	12	6
			11		ns	C_L = 15 pF TTL Signal Levels		
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$	2000			V/µs	V_{CM} = 200 V $V_I = V_{IH}$ V_O > 3.2 V	13, 14	10
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	2000			V/µs	V_{CM} = 200 V $V_I = V_{IL}$ V_O < 0.8 V	13, 14	10
Input Dynamic Power Dissipation Capacitance	C_{PD1}		68		pF			11
Output Dynamic Power Dissipation Capacitance	C_{PD2}		10		pF			11

Notes:

1. The LED is OFF when the V_I is high and ON when V_I is low.
2. Device considered a two terminal device; pins 1-4 shorted together and pins 5-8 shorted together.
3. This is a proof test.
4. C_I is the capacitance measured at pin 2 (V_I).
5. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the V_I signal to the logic switching level of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the V_I signal to the logic switching level of the V_O signal.
6. The logic switching levels are 1.5 V for TTL signals (0-3 V) and 2.5 V for CMOS signals (0-5 V).
7. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD (percent pulse width distortion) is equal to PWD in ns divided by symbol duration (bit length) in ns.
8. Minimum data rate is calculated as follows: %PWD/PWD where %PWD is typically chosen by the design engineer (30% is common).
9. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the operating condition range.
10. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining V_O > 3.2 V. CM_L is the maximum common mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
11. Unloaded dynamic power dissipation is calculated as follows: $C_{PD} \cdot V_{DD}^2 \cdot f + I_{DD} \cdot V_{DD}$ where f is switching frequency in MHz.

HCPL-7101 Application Information

The HCPL-7101 is extremely easy to use. Because the optocoupler uses high-speed CMOS IC technology, the inputs and output are fully compatible with all +5 V TTL and CMOS logic. TTL or CMOS logic can be connected directly to the inputs and output; no external interface circuitry is required.

As shown in Figure 1, the only external components required for proper operation are two ceramic bypass capacitors. Capacitor values should be between 0.01 µF and 0.1 µF. For each capacitor, the total lead length between both ends of the capacitor and the power-supply pins should not exceed 20 mm. Figure 2 illustrates the recommended printed circuit board layout for the HCPL-7101.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 7).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference bewteen t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same supply voltage, output load, and operating temperature). As illustrated in Figure 10, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 11 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 11 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The HCPL-7101 optocoupler offers the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, and power supply ranges.

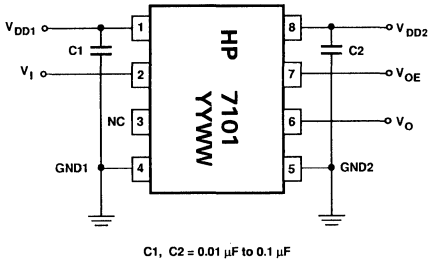


Figure 1. HCPL-7101 Recommended Application Circuit.

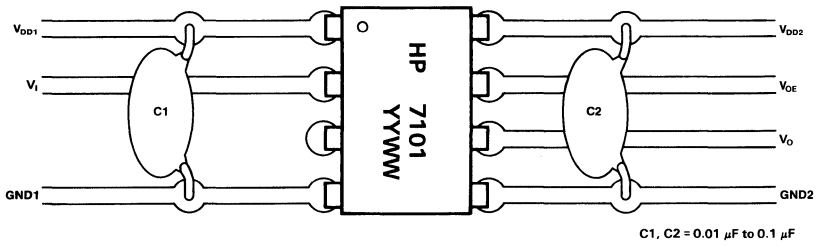


Figure 2. HCPL-7101 Recommended Printed Circuit Board Layout.

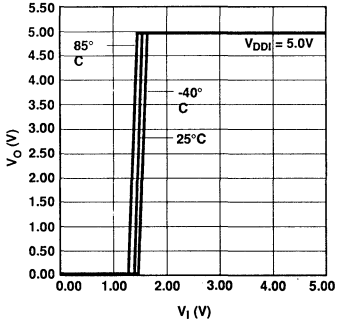


Figure 3. Typical Output Voltage vs. Input Voltage.

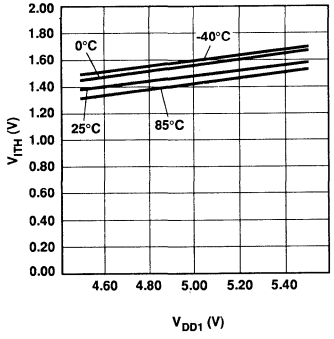


Figure 4. Typical Input Voltage Switching Threshold vs. Input Supply Voltage.

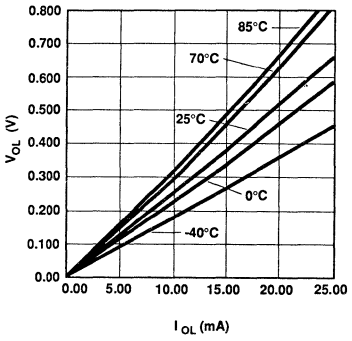


Figure 5. Typical Logic Low Output Voltage vs. Logic Low Output Current.

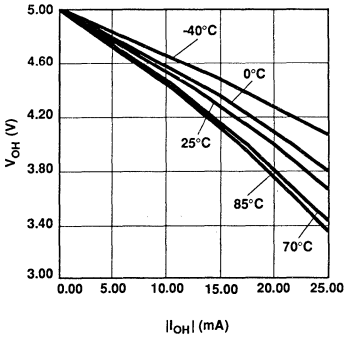


Figure 6. Typical Logic High Output Voltage vs. Logic High Output Current.

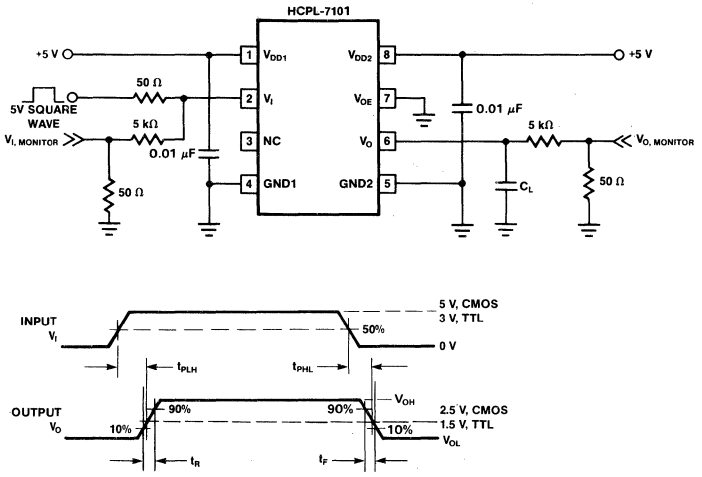


Figure 7. Test Circuit for Propagation Delay, Rise Time and Fall Time.

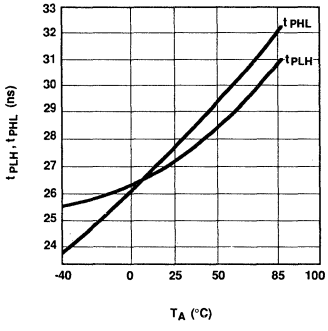


Figure 8. Typical Propagation Delay vs. Temperature.

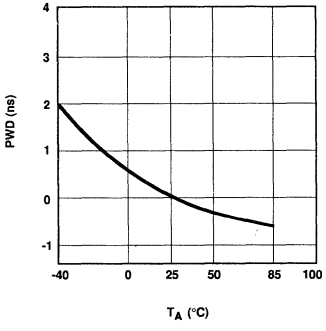


Figure 9. Typical Pulse Width Distortion vs. Temperature.

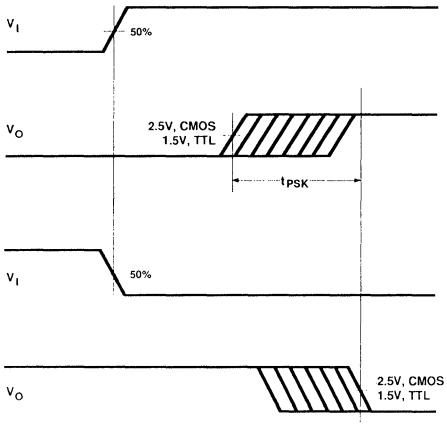


Figure 10. Propagation Delay Skew Waveform.

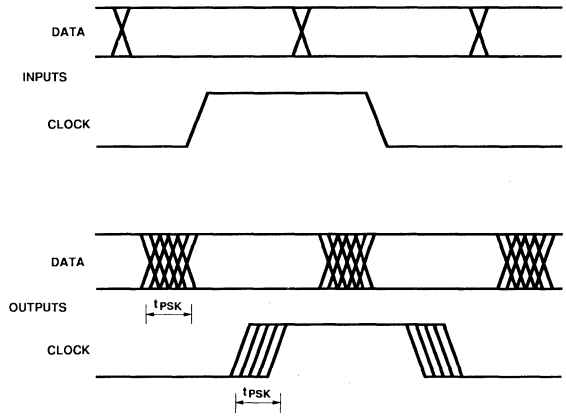


Figure 11. Parallel Data Transmission Example.

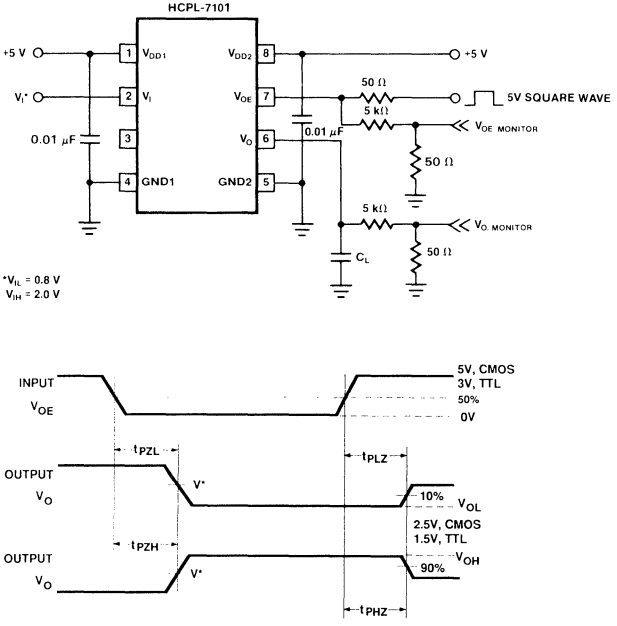


Figure 12. Test Circuit for 3-State Output Enable and Disable Propagation Delays.

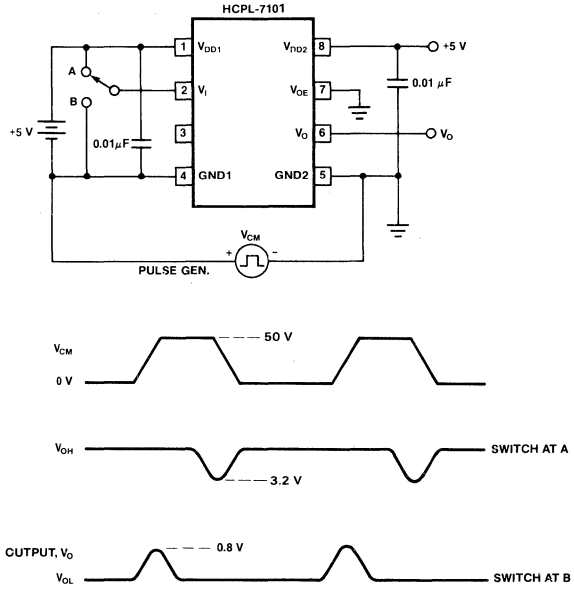


Figure 13. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

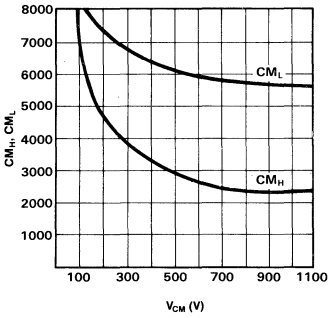


Figure 14. Typical Common Mode Transient Immunity vs. Common Mode Transient Voltage.

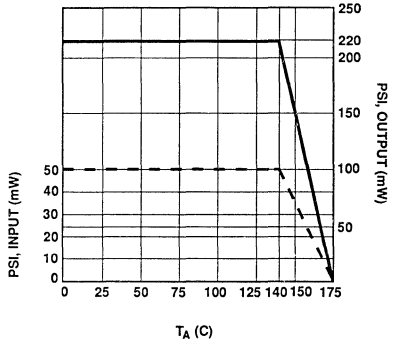
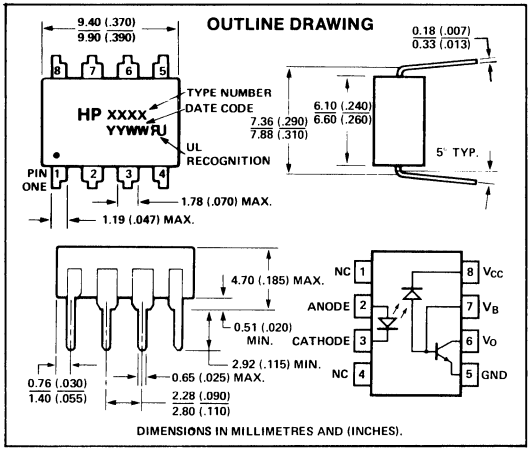


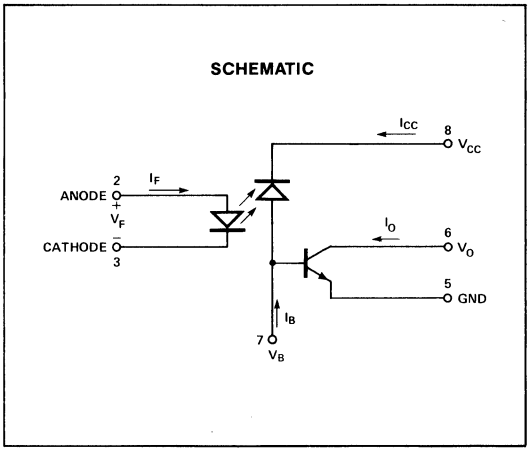
Figure 15. Dependence of Safety-Limiting Data on Ambient Temperature.

HEWLETT PACKARD

WIDEBAND ANALOG/VIDEO OPTOCOUPLER

HCPL-4562





Features

- **WIDE BANDWIDTH: 17 MHz[1]**
- **HIGH VOLTAGE GAIN: 2.0[1]**
- **LOW TEMPERATURE COEFFICIENT (G_V): -0.3% PER °C[1]**
- **HIGHLY LINEAR AT LOW DRIVE CURRENTS**
- **HIGH-SPEED AlGaAs EMITTER**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF VOLTAGES OF 2500 VAC, 1 MINUTE AND 5000 VAC, 1 MINUTE (OPTION 020).**
- **VDE 0883 APPROVAL AVAILABLE**

Description

The HCPL-4562 optocoupler provides wide-bandwidth isolation for analog signals. It is ideal for video isolation when combined with its application circuit (Figure 4). High linearity and low phase shift are achieved through an 820 nm AlGaAs emitter, combined with a high-speed detector.

Applications

- **VIDEO ISOLATION FOR THE FOLLOWING STANDARDS/FORMATS: NTSC, PAL, SECAM, S-VHS, ANALOG RGB**
- **LOW-DRIVE-CURRENT FEEDBACK ELEMENT IN SWITCHING POWER SUPPLIES, *e.g.* FOR ISDN NETWORKS**
- **A/D CONVERTER SIGNAL ISOLATION**
- **ANALOG SIGNAL GROUND ISOLATION**

Recommended Operating Conditions

Operating Temperature	-10°C to +70°C
Quiescent Input Current — I_{F_Q}	6 mA
Peak Input Current — I_F	10 mA

Absolute Maximum Ratings

Storage Temperature	-55°C to +125°C
Operating Temperature	-40°C to +85°C
Lead Solder Temperature	260°C for 10 s (1.6 mm below seating plane)
Average Input Current — I_F	12 mA DC
Peak Input Current — I_F	18.6 mA
Effective Input Current — I_F	12.9 mA rms
Supply Voltage — V_{CC} (Pin 8-5)	-0.3 V to 30 V
Output Voltage — V_O (Pin 6-5)	-0.3 V to 20 V
Reverse Input Voltage — V_R (Pin 3-2)	1.8 V
Emitter-Base Reverse Voltage (Pin 5-7)	5 V
Peak Output Current — I_O (Pin 6)	16 mA
Average Output Current — I_O (Pin 6)	8 mA
Base Current — I_B (Pin 7)	5 mA
Output Power Dissipation[2]	100 mW

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

OPTOCOUPLERS

DC Electrical Specifications (T_A = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Notes
Base Photo Current	I_{PB}	13	32 19.2	65	μA μA	I_F = 10 mA, $V_{PB} \geq$ 5 V I_F = 6 mA, $V_{PB} \geq$ 5 V	2, 6 2, 6	
I_{PB} Temperature Coefficient	$\Delta I_{PB}/\Delta T$		−0.3		%/°C	2 mA < I_F < 10 mA, $V_{PB} \geq$ 5 V	2	
I_{PB} Nonlinearity			0.25		%	2 mA < I_F < 10 mA	2, 6	3
Input Forward Voltage	V_F	1.1	1.3	1.6	V	I_F = 5 mA	5	
Input Reverse Breakdown Voltage	BV_R	1.8	5		V	I_R = 10 μA		
Transistor Current Gain	h_{FE}	60	160			I_C = 1 mA, V_{CE} = 1.25 V		
Current Transfer Ratio	CTR		45		%	I_F = 6 mA, V_{CE} = 1.25 V, $V_{PB} \geq$ 5 V	8,9	4
DC Output Voltage	V_O		4.25		V	G_V = 2, V_{CC} = 9 V	4, 15	
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		5
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz		5
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	$R_H \leq$ 50%, t = 1 min.		5
OPTION 020	V_{ISO}	5000						

Small-Signal Characteristics (T_A = 25°C unless otherwise noted)

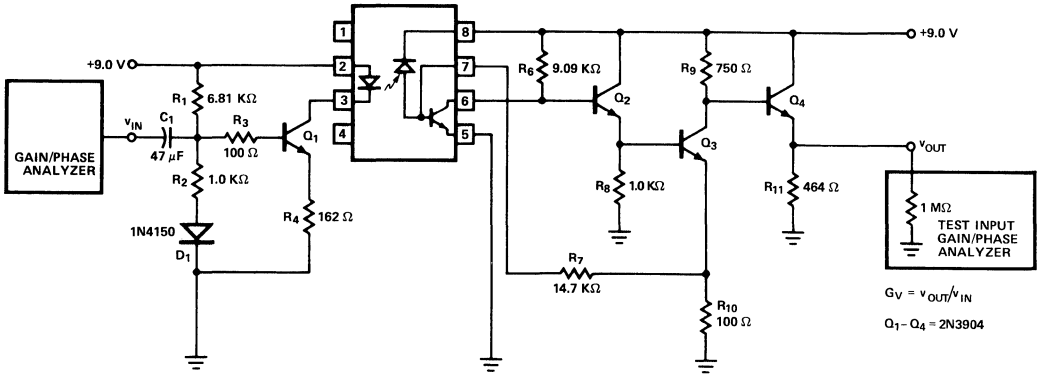
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Notes
Voltage Gain	G_V(0.1 MHz)	0.8	2.0	4.2		v_{IN} = 1 V_{p-p}	1	6
G_V Temperature Coefficient	$\Delta G_V/\Delta T$		−0.3		%/°C	v_{IN} = 1 V_{p-p}, f = 0.1 MHz	1, 11	
Base Photo Current Variation	Δi_{PB} (6 MHz)		1.1	3.0	−dB	I_{FQ} = 6 mA, v_{IN} = 1 V_{p-p}, f_{REF} = 0.1 MHz	3, 10, 12	
−3 dB Frequency (i_{PB})	i_{PB} (−3 dB)	6	15		MHz	v_{IN} = 1 V_{p-p}, f_{REF} = 0.1 MHz, I_{FQ} = 6 mA	3, 10, 12	7
−3 dB Frequency (G_V)	G_V(−3 dB)	6	17		MHz	v_{IN} = 1 V_{p-p}, f_{REF} = 0.1 MHz	1, 11	7
Gain Variation	ΔG_V(6 MHz)		0.8		−dB	T_A = −10°C, v_{IN} = 1 V_{p-p}, f_{REF} = 0.1 MHz	1, 11	
			1.1	3.0	−dB	v_{IN} = 1 V_{p-p}, f_{REF} = 0.1 MHz	1, 11	
			1.5		−dB	T_A = 70°C, v_{IN} = 1 V_{p-p}, f_{REF} = 0.1 MHz	1, 11	
	ΔG_V (10 MHz)		1.15		−dB	v_{IN} = 1 V_{p-p}, f_{REF} = 0.1 MHz	1, 11	
Differential Gain			±1		%	I_{Fac} = 0.7 mA pk-pk, I_{Fdc} = 3 to 9 mA, f = 3.58 MHz	3, 7	8
Differential Phase			±1		deg.	I_{Fac} = 0.7 mA pk-pk, I_{Fdc} = 3 to 9 mA, f = 3.58 MHz	3, 7	9
Total Harmonic Distortion	THD		2.5		%	f = 3.58 MHz, G_V = 2, V_{IN} = 1 V_{p-p}, I_{FQ} = 6 mA	4	10
Output Noise Voltage	$V_{O_{NOISE}}$		950		μV_{RMS}	10 Hz to 10 MHz	1	
Isolation Mode Rejection Ratio	IMRR		122		dB	f = 120 Hz, G_V = 2	14	11

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	≥7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

Notes:

1. When used in the circuit of Figure 1 or Figure 4; $G_V = V_{OUT}/V_{IN}$.
2. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C.
3. Maximum variation from the best fit line of I_{PB} vs. I_F expressed as a percentage of the peak-to-peak full-scale output.
4. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
5. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
6. Flat-band small-signal voltage gain.
7. The frequency at which the gain is 3 dB below the flat-band gain.
8. Differential gain is the change in the small-signal gain of the optocoupler at 3.58 MHz as the bias level is varied over a given range.
9. Differential phase is the change in the small-signal phase response of the optocoupler at 3.58 MHz as the bias level is varied over a given range.
10. TOTAL HARMONIC DISTORTION is defined as the square root of the sum of the square of each harmonic distortion component.
11. ISOLATION MODE REJECTION RATIO, a measure of the optocoupler's ability to reject signals or noise that may exist between input and output terminals, is defined by $(V_{OUT}/V_{IN})/(V_{OUT}/V_{IM})$, where V_{IM} is the isolation mode voltage signal.



NOTE: ALL RESISTORS ARE 1% TOLERANCE; EXCEPT R_4 (162 Ω ±0.5 Ω).

Figure 1. Gain and Bandwidth Test Circuit

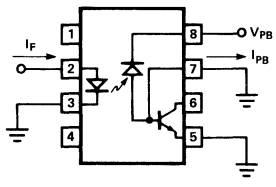


Figure 2. Base Photo Current Test Circuit

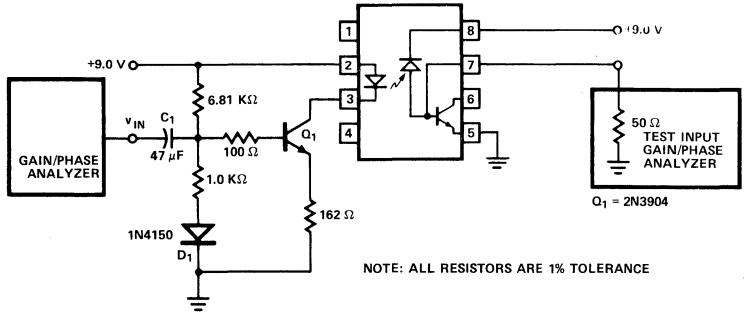


Figure 3. Base Photo Current Frequency Response Test Circuit

OPTOCOUPLERS

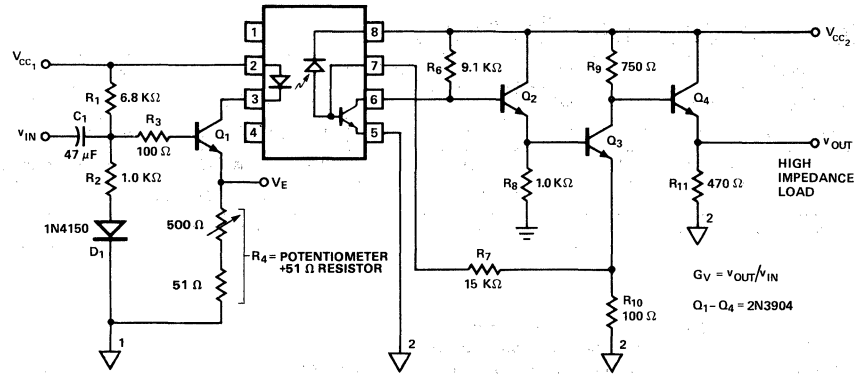


Figure 4. Recommended Isolated Video Interface Circuit

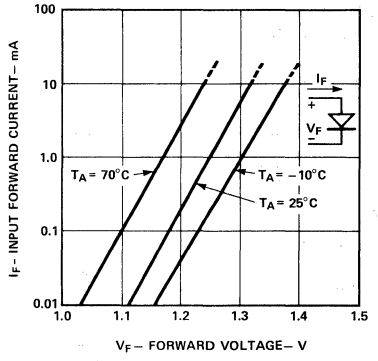


Figure 5. Input Current vs. Forward Voltage

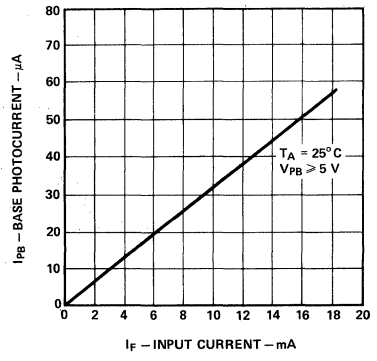


Figure 6. Base Photo Current vs. Input Current

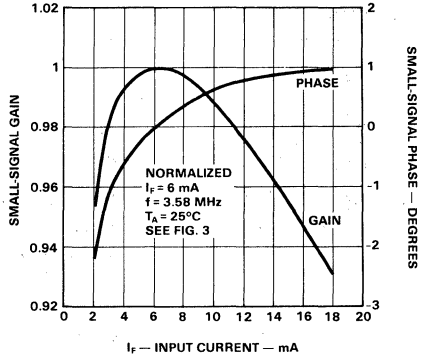


Figure 7. Small-Signal Response vs. Input Current

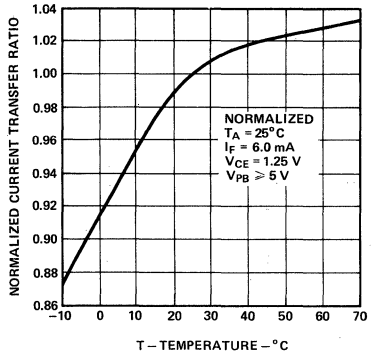


Figure 8. Current Transfer Ratio vs. Temperature

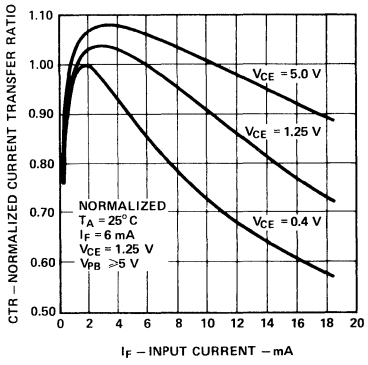


Figure 9. Current Transfer Ratio vs. Input Current

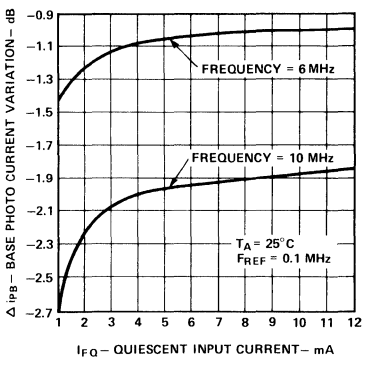


Figure 10. Base Photo Current Variation vs. Bias Conditions

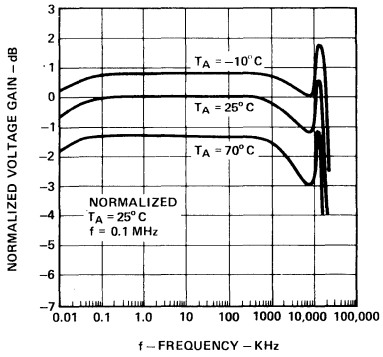


Figure 11. Normalized Voltage Gain vs. Frequency

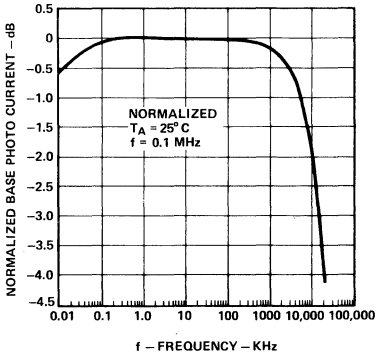


Figure 12. Normalized Base Photo Current vs. Frequency

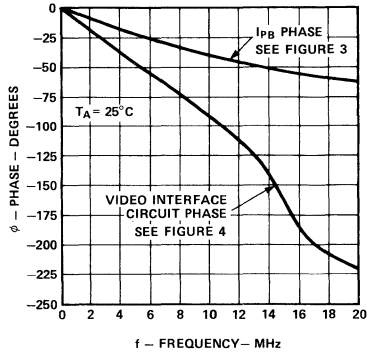


Figure 13. Phase vs. Frequency

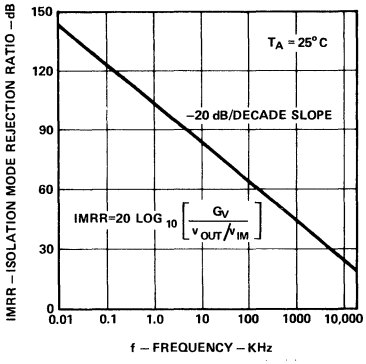


Figure 14. Isolation Mode Rejection Ratio vs. Frequency

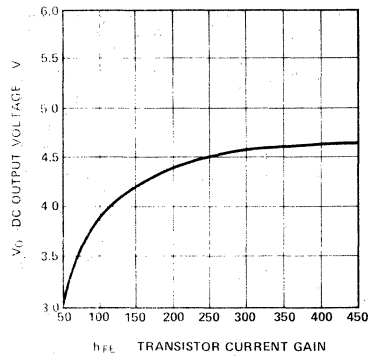


Figure 15. DC Output Voltage vs. Transistor Current Gain

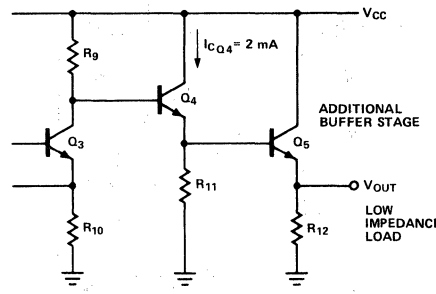


Figure 16. Output Buffer Stage for Low Impedance Loads

Design Considerations of the Application Circuit

The application circuit in Figure 4 incorporates several features that help maximize the bandwidth performance of the HCPL-4562. Most important of these features is peaked response of the detector circuit that helps extend the frequency range over which the voltage gain is relatively constant. The number of gain stages, the overall circuit topology and the choice of DC bias points are all consequences of the desire to maximize bandwidth performance.

To use the circuit, first select R_1 to set V_E for the desired LED quiescent current by:

$$I_{FQ} = \frac{V_E}{R_4} \cong \frac{G_V V_E R_{10}}{(\partial I_{PB}/\partial I_F) R_7 R_9} \quad (1)$$

For a constant value of $v_{IN_{p-p}}$, the circuit topology (adjusting the gain with R_4) preserves linearity by keeping the modulation factor (MF) dependent only on V_E.

$$i_{F_{p-p}} \cong v_{IN}/R_4 \quad (2)$$

$$\frac{i_{F_{p-p}}}{I_{FQ}} \cong \frac{i_{PB_{p-p}}}{I_{PBQ}} = \frac{v_{IN_{p-p}}}{V_E} \quad (3)$$

$$\text{Modulation Factor (MF)} \frac{i_{F(p-p)}}{2 I_{FQ}} \cong \frac{v_{IN_{p-p}}}{2 V_E} \quad (4)$$

For a given G_V, V_E, and V_{CC}, DC output voltage will vary only with h_{FEX}.

$$V_O = V_{CC} - V_{BE_4} - \frac{R_9}{R_{10}} (V_{BEX} - (I_{PBQ} - I_{BXQ}) R_7) \quad (5)$$

Where:

$$I_{PBQ} \cong \frac{G_V V_E R_{10}}{R_7 R_9} \quad (6)$$

and,

$$I_{BXQ} \cong \frac{V_{CC} - 2 V_{BE}}{R_6 h_{FEX}} \quad (7)$$

Figure 15 shows the dependency of the DC output voltage on h_{FEX}.

For 9 V < V_{CC} < 12 V, select the value of R_{11} such that

$$I_{C_{Q4}} \cong \frac{V_O}{R_{11}} \leq \frac{4.25V}{470\Omega} \leq 9.0\,mA \quad (8)$$

The voltage gain of the second stage (Q_3) is approximately equal to:

$$\frac{R_9}{R_{10}} * \frac{1}{1 + s R_9 \left[C_{CQ_3} + \frac{1}{2\pi R'_{11} f_{T_4}} \right]} \quad (9)$$

Increasing R'_{11} (R'_{11} includes the parallel combination of R_{11} and the load impedance) or reducing R_9 (keeping R_9/R_{10} ratio constant) will improve the bandwidth.

If it is necessary to drive a low impedance load, bandwidth may also be preserved by adding an additional emitter following the buffer stage (Q_5 in Figure 16), in which case R_{11} can be increased to set $I_{CQ4} \cong 2$ mA.

Finally, adjust R_4 to achieve the desired voltage gain.

$$G_V \cong \frac{v_{OUT}}{v_{IN}} \cong \frac{\partial I_{PB}}{\partial I_F} \left[\frac{R_7 R_9}{R_4 R_{10}} \right] \quad (10)$$

$$\text{where typically } \frac{\partial I_{PB}}{\partial I_F} = 0.0032$$

Definition:

- G_V = Voltage Gain
- I_{FQ} = Quiescent LED forward current
- $i_{F_{p-p}}$ = Peak-to-peak small signal LED forward current
- $v_{IN_{p-p}}$ = Peak-to-peak small signal input voltage
- $i_{PB_{p-p}}$ = Peak-to-peak small signal base photo current
- I_{PBQ} = Quiescent base photo current
- V_{BEX} = Base-Emitter voltage of HCPL-4562 transistor
- I_{BXQ} = Quiescent base current of HCPL-4562 transistor
- h_{FEX} = Current Gain (IC/IB) of HCPL-4562 transistor
- V_E = Voltage across emitter degeneration resistor R_4
- f_{T_4} = Unity gain frequency of Q_4
- C_{CQ_3} = Effective capacitance from collector of Q_3 to ground

HEWLETT PACKARD

AC/DC to Logic Interface Optocoupler

Technical Data

HCPL-3700
HCPL-3760

Features

- **Standard and Low Input Current (HCPL-3760) Versions**
- **AC or DC Input**
- **Programmable Sense Voltage**
- **Hysteresis**
- **Logic Compatible Output**
- **Thresholds Guaranteed Over Temperature**
- **Thresholds Independent of LED Degradation**
- **Recognized Under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 VAC, 1 Minute**
- **VDE 0883 Approval Available**

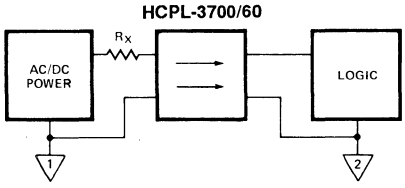
Applications

- **Limit Switch Sensing**
- **Low Voltage Detector**
- **5 V-240 V AC/DC Voltage Sensing**
- **Relay Contact Monitor**
- **Relay Coil Voltage Monitor**
- **Current Sensing**
- **Microprocessor Interfacing**

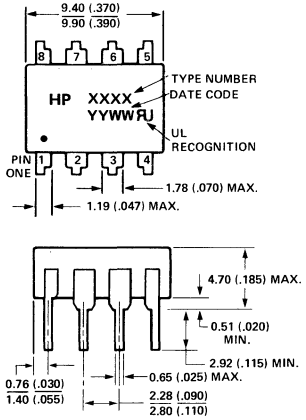
Description

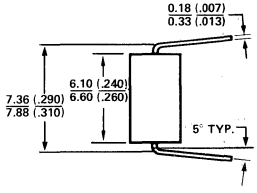
The HCPL-3700 and HCPL-3760 are voltage/current threshold detection optocouplers. The HCPL-3760 is a low-current version of the HCPL-3700. To obtain lower current operation, the HCPL-3760 uses a high-efficiency AlGaAs LED which provides higher light output at lower drive currents. Both devices utilize threshold sensing input buffer ICs which permit control of threshold levels over a wide range of input voltages with a single external resistor.

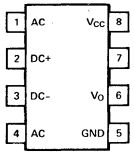
The input buffer incorporates several features: hysteresis for extra noise immunity and switching immunity, a diode bridge for easy use with ac input signals, and internal clamping diodes to protect the buffer and LED from a wide range of over-voltage and over-current transients. Because



Outline Drawing







DIMENSIONS IN MILLIMETRES AND (INCHES).

OPTOCOUPLERS

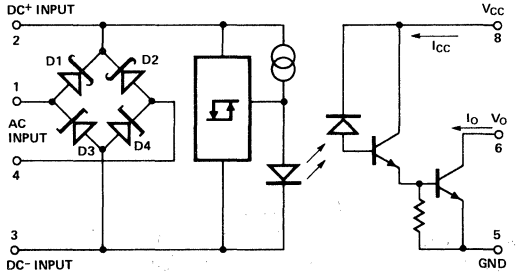
threshold sensing is done prior to driving the LED, variations in optical coupling from the LED to the detector will have no effect on the threshold levels.

The HCPL-3700's input buffer IC has a nominal turn on threshold of 2.5 mA (I_{TH} +) and 3.7 volts (V_{TH} +).

The buffer IC for the HCPL-3760 was redesigned to permit a lower input current. The nominal turn on threshold for the HCPL-3760 is 1.2 mA (I_{TH} +) and 3.7 volts (V_{TH} +).

The high gain output stage features an open collector output providing both TTL compatible saturation voltages and CMOS compatible break-down voltages.

Schematic



By combining several unique functions in a single package, the user is provided with an ideal component for industrial control computer input boards and other applications where a predetermined input threshold level is desirable.

Absolute Maximum Ratings (No derating required up to 70°C)

Parameter		Symbol	Min.	Max.	Units	Note
Storage Temperature		T_S	-55	125	°C	
Operating Temperature		T_A	-40	85	°C	
Lead Soldering Cycle	Temperature			260	°C	1
	Time			10	sec	
Input Current	Average	I_{IN}		50	mA	2
	Surge			140		2, 3
	Transient			500		
Input Voltage (Pins 2-3)		V_{IN}	-0.5		V	
Input Power Dissipation		P_{IN}		230	mW	4
Total Package Power Dissipation		P		305	mW	5
Output Power Dissipation		P_O		210	mW	6
Output Current	Average	I_O		30	mA	7
Supply Voltage (Pins 8-5)		V_{CC}	-0.5	20	V	
Output Voltage (Pins 6-5)		V_O	-0.5	20	V	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Supply Voltage	V_{CC}	2	18	V	
Operating Temperature	T_A	0	70	°C	
Operating Frequency	f	0	4	KHz	8

Electrical Specifications

Over Recommended Temperature T_A = 0°C to 70°C, Unless Otherwise Specified.

Parameter		Sym.	Device	Min.	Typ.[9]	Max.	Units	Conditions	Fig.	Note
Input Threshold Current		I_{TH+}	HCPL-3700	1.96	2.5	3.11	mA	$V_{IN} = V_{TH+}$; V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 4.2 mA	2, 3	14
			HCPL-3760	0.87	1.2	1.56				
		I_{TH-}	HCPL-3700	1.00	1.3	1.62		$V_{IN} = V_{TH-}$; V_{CC} = 4.5 V; V_O = 2.4 V; $I_{OH} \leq$ 100 µA		
			HCPL-3760	0.43	0.6	0.80				
Input Threshold Voltage	DC (Pins 2, 3)	V_{TH+}		3.35	3.7	4.05	V	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 4.2 mA		
		V_{TH-}		2.01	2.6	2.86	V	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 100 µA		
	AC (Pins 1, 4)	V_{TH+}		4.23	4.9	5.50	V	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 4.2 mA		14, 15
		V_{TH-}		2.87	3.7	4.20	V	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 100 µA		
Hysteresis		I_{HYS}	HCPL-3700		1.2		mA	$I_{HYS} = I_{TH+} - I_{TH-}$	2	
			HCPL-3760		0.6					
		V_{HYS}			1.2		V	$V_{HYS} = V_{TH+} - V_{TH-}$		
Input Clamp Voltage		V_{IHC1}		5.4	6.0	6.6	V	$V_{IHC1} = V_2 - V_3$; V_3 = GND; I_{IN} = 10 mA; Pin 1 & 4 Connected to Pin 3	1	
		V_{IHC2}		6.1	6.7	7.3	V	$V_{IHC2} = \lvert V_1 - V_4 \rvert$; $\lvert I_{IN} \rvert$ = 10 mA; Pins 2 & 3 Open		
		V_{IHC3}			12.0	13.4	V	$V_{IHC3} = V_2 - V_3$; V_3 = GND; I_{IN} = 15 mA; Pins 1 & 4 Open		
		V_{ILC}			-0.76		V	$V_{ILC} = V_2 - V_3$; V_3 = GND; I_{IN} = -10 mA		
Input Current		I_{IN}	HCPL-3700	3.0	3.7	4.4	mA	$V_{IN} = V_2 - V_3$ = 5.0 V Pins 1 & 4 Open	5	
			HCPL-3760	1.5	1.8	2.2				
Bridge Diode Forward Voltage		$V_{D1,2}$	HCPL-3700		0.59		V	I_{IN} = 3 mA		
			HCPL-3760		0.51			I_{IN} = 1.5 mA		
		$V_{D3,4}$	HCPL-3700		0.74			I_{IN} = 3 mA		
			HCPL-3760		0.71			I_{IN} = 1.5 mA		

Electrical Specifications (Continued)

Parameter	Sym.	Device	Min.	Typ.[9]	Max.	Units	Conditions	Fig.	Note
Logic Low Output Voltage	V_{OL}			0.1	0.4	V	V_{CC} = 4.5 V; I_{OL} = 4.2 mA	5	14
Logic High Output Current	I_{OH}				100	µA	V_{OH} = V_{CC} = 18 V		14
Logic Low Supply Current	I_{CCL}	HCPL-3700		1.2	4	mA	V_2 – V_3 = 5.0 V; V_O = Open; V_{CC} = 5.0 V		
		HCPL-3760		0.7	3				
Logic High Supply Current	I_{CCH}			0.002	4	µA	V_{CC} = 18 V; V_O = Open	4	14
Input-Output Insulation	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 min; T_A = 25°C		16
Input-Output Resistance	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 VDC		16
Input-Output Capacitance	C_{I-O}			0.6		pF	f = 1 MHz; V_{I-O} = 0 VDC		
Input Capacitance	C_{IN}			50		pF	f = 1 MHz; V_{IN} = 0 V, Pins 2 & 3, Pins 1 & 4 Open		

*For JEDEC registered parts.

Switching Specifications

T_A = 25°C, V_{CC} = 5.0 V Unless Otherwise Specified

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	HCPL-3700		4.0	15.0	µs	R_L = 4.7 kΩ, C_L = 30 pF	6, 9	10
		HCPL-3760		4.5					
Propagation Delay Time to Logic High at Output	t_{PLH}	HCPL-3700		10.0	40.0	µs	R_L = 4.7 kΩ, C_L = 30 pF		11
		HCPL-3760		8.0					
Output Rise Time (10-90%)	t_r	HCPL-3700		20		V/µs	R_L = 4.7 kΩ, C_L = 30 pF	7	
		HCPL-3760		14					
Output Fall Time (90-10%)	t_f	HCPL-3700		0.3		V/µs	R_L = 4.7 kΩ, C_L = 30 pF		
		HCPL-3760		0.4					
Common Mode Transient Immunity at Logic Low Output	$\|CM_H\|$			4000		V/µs	I_{IN} = 0 mA, R_L = 4.7 kΩ, $V_{O\,min}$ = 2.0 V, V_{CM} = 1400 V	8, 10	12, 13
Common Mode Transient Immunity at Logic High Output	$\|CM_L\|$	HCPL-3700		600		V/µs	I_{IN} = 3.11 mA; R_L = 4.7 kΩ, $V_{O\,max}$ = 0.8 V, V_{CM} = 140 V		
		HCPL-3760					I_{IN} = 1.56 mA; R_L = 4.7 kΩ, $V_{O\,max}$ = 0.8 V, V_{CM} = 140 V		

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L (IO1)	≥ 7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L (IO2)	≥ 7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

Notes:

1. Measured at a point 1.6 mm below seating plane.
2. Current into/out of any single lead.
3. Surge input current duration is 3 ms at 120 Hz pulse repetition rate. Transient input current duration is 10 μs at 120 Hz pulse repetition rate. Note that maximum input power, P_{IN}, must be observed.
4. Derate linearly above 70°C free-air temperature at a rate of 4.1 mW/°C. Maximum input power dissipation of 230 mW allows an input IC junction temperature of 125°C at an ambient temperature of T_A = 70°C with a typical thermal resistance from junction to ambient of θ_{JA1} = 240°C W. Excessive P_{IN} and T_J may result in IC chip degradation.
5. Derate linearly above 70°C free-air temperature at a rate of 5.4 mW/°C.
6. Derate linearly above 70°C free-air temperature at a rate of 3.9 mW/°C. Maximum output power dissipation of 210 mW allows an output IC junction temperature of 125°C at an ambient temperature of T_A = 70°C with a typical thermal resistance from junction to ambient of θ_{JA0} = 265°C/W.
7. Derate linearly above 70°C free-air temperature at a rate of 0.6 mA/°C.
8. Maximum operating frequency is defined when output waveform Pin 6 obtains only 90% of V_{CC} with R_L = 4.7 kΩ, C_L = 30 pF using a 5 V square wave input signal.
9. All typical values are at T_A = 25°C, V_{CC} = 5.0 V unless otherwise stated.
10. The t_{PHL} propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 μs rise time) to the 1.5 V level on the leading edge of the output pulse (see Figure 9).
11. The t_{PLH} propagation delay is measured from the 2.5 V level of the trailing edge of a 5.0 V input pulse (1 μs fall time) to the 1.5 V level on the trailing edge of the output pulse (see Figure 9).
12. Common mode transient immunity in Logic High level is the maximum tolerable (positive) $dV_{CM/dt}$ on the leading edge of the common mode pulse, V_{CM}, to insure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) $dV_{CM/dt}$ on the trailing edge of the common mode pulse signal, V_{CM}, to insure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V). See Figure 10.
13. In applications where $dV_{CM/dt}$ may exceed 50,000 V/μs (such as static discharge), a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value for R_{CC} is 240Ω per volt of allowable drop in V_{CC} (between Pin 8 and V_{CC}) with a minimum value of 240Ω.
14. Logic low output level at Pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH-}$ once V_{IN} has exceeded V_{TH+}. Logic high output level at Pin 6 occurs under the conditions of $V_{IN} \leq V_{TH-}$ as well as the range of $V_{IN} < V_{TH+}$ once V_{IN} has decreased below V_{TH-}.
15. AC voltage is instantaneous voltage.
16. Device considered a two terminal device: Pins 1, 2, 3, 4 connected together, and Pins 5, 6, 7, 8 connected together.

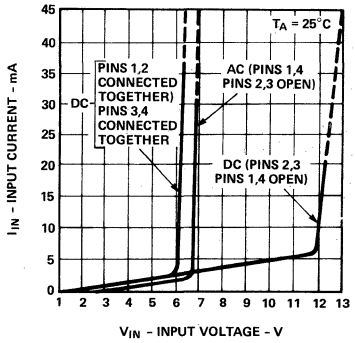
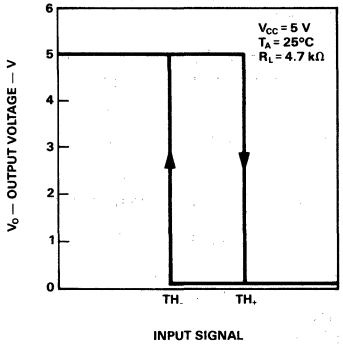
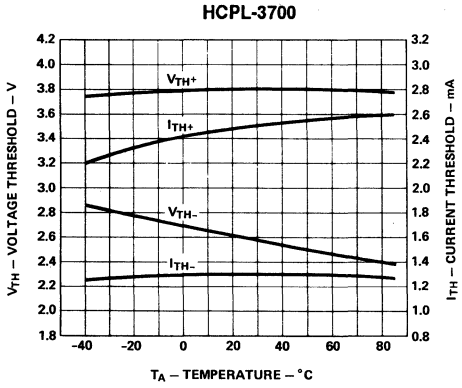


Figure 1. Typical Input Characteristics, I_{IN} vs. V_{IN} (AC Voltage is Instantaneous Value).



	DEVICE	TH_+	TH_-	INPUT CONNNECTION
I_{TH}	HCPL-3700	2.5 mA	1.3 mA	PINS 2, 3
	HCPL-3760	1.2 mA	0.6 mA	OR 1, 4
$V_{TH(dc)}$	BOTH	3.7 V	2.6 V	PINS 2, 3
$V_{TH(ac)}$	BOTH	4.9 V	3.8 V	PINS 1, 4

Figure 2. Typical Transfer Characteristics.



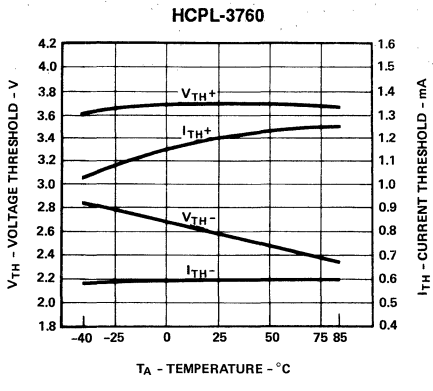


Figure 3. Typical DC Threshold Levels vs. Temperature.

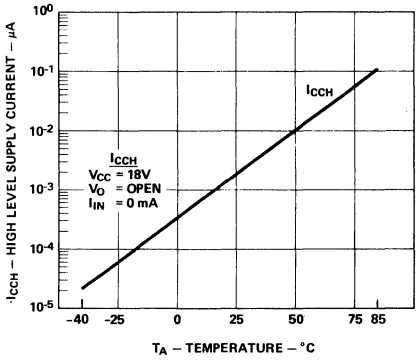


Figure 4. Typical High Level Supply Current, I_{CCH} vs. Temperature.

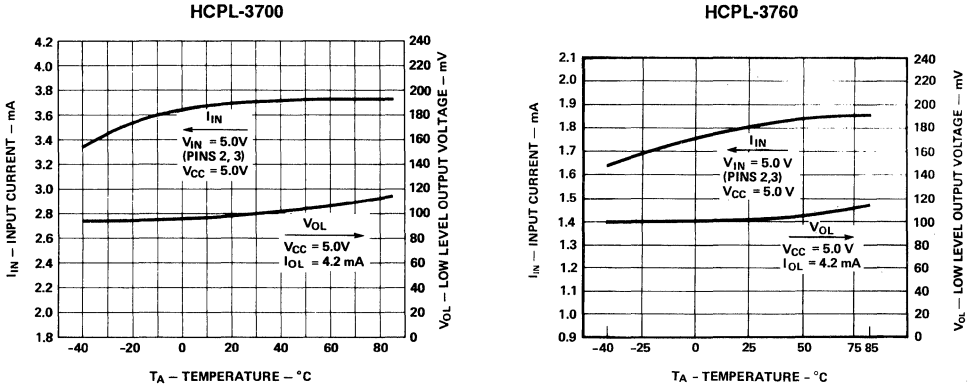


Figure 5. Typical Input Current, I_{IN}, and Low Level Output Voltage, V_{OL}, vs. Temperature.

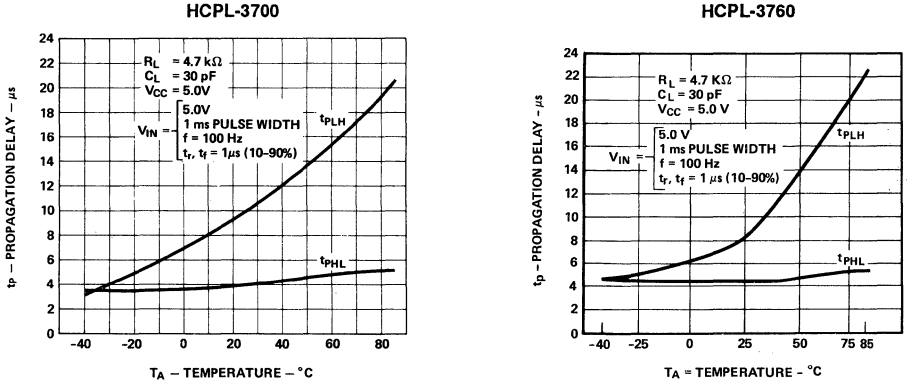


Figure 6. Typical Propagation Delay vs. Temperature.

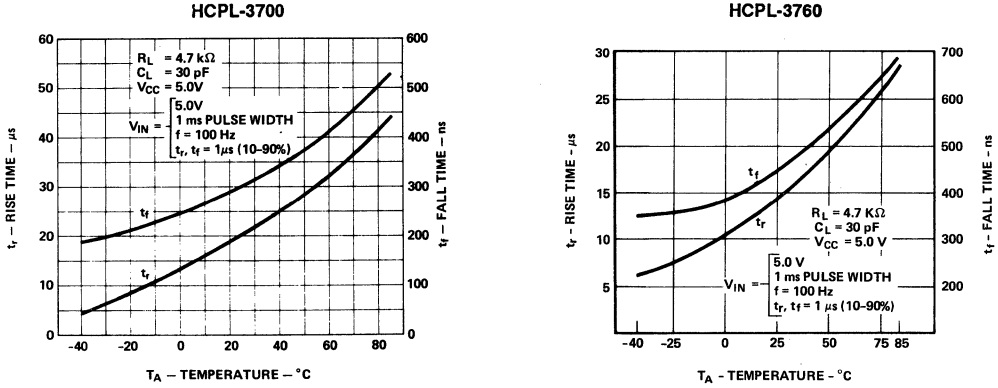


Figure 7. Typical Rise, Fall Times vs. Temperature.

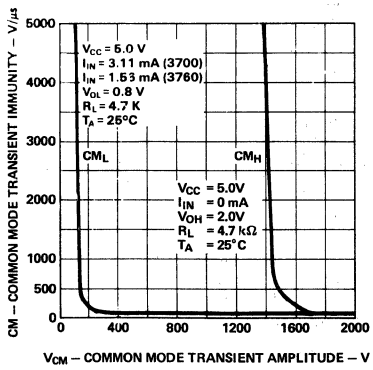
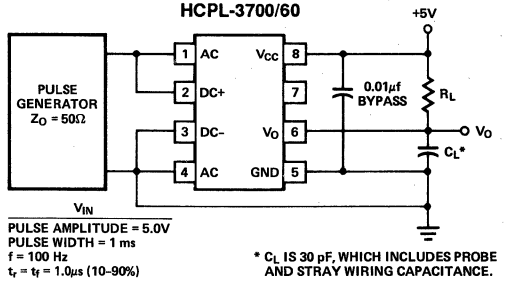


Figure 8. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.



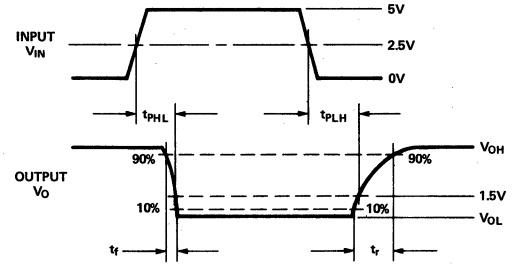


Figure 9. Switching Test Circuit.

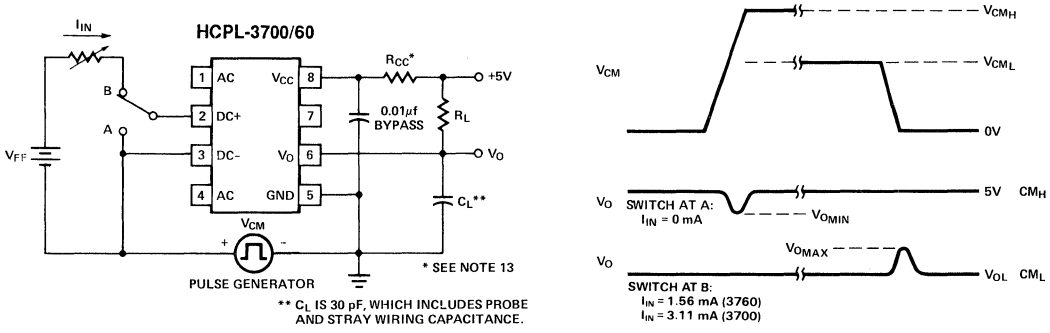


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

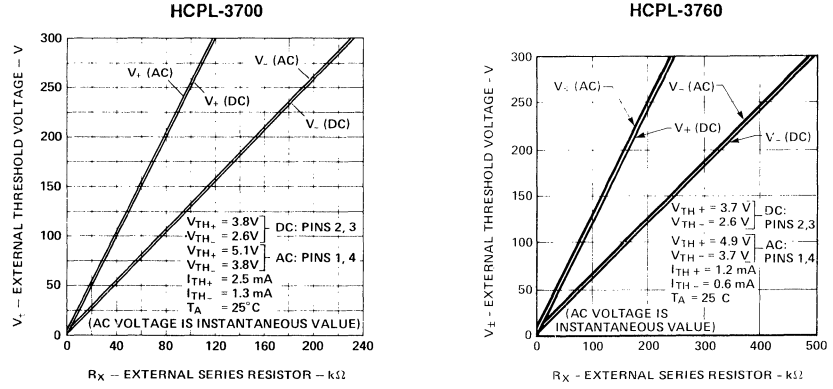


Figure 11. Typical External Threshold Characteristics, V± vs. R_X.

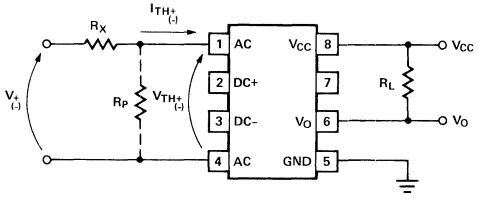


Figure 12. External Threshold Voltage Level Selection.

Electrical Considerations

The HCPL-3700/3760 optocouplers have internal temperature compensated, predictable voltage and current threshold points which allow selection of an external resistor, R_X, to determine larger external threshold voltage levels. For a desired external threshold voltage, $V_{\pm}$, a corresponding typical value of R_X can be obtained from Figure 11. Specific calculation of R_X can be obtained from Equation (1). Specification of both V_+ and V_- voltage threshold levels simultaneously can be obtained by the use of R_x and R_p as shown in Figure 12 and determined by Equations (2) and (3).

R_X can provide over-current transient protection by limiting input current during a transient condition. For monitoring contacts of a relay or switch, the HCPL-3700/3760 in combination with R_x and R_p can be used to allow a specific current to be conducted through the contacts for cleaning purposes (wetting current).

The choice of which input voltage clamp level to choose depends upon the application of this device (see Figure 1). It is recommended that the low clamp condition be used when possible. The low clamp condition in conjunction with the low input current feature will ensure extremely low input power dissipation.

In applications where $dV_{CM/dt}$ may be extremely large (such as static discharge), a series resistor, R_{CC}, should be connected in series with V_{CC} and Pin 8 to protect the detector IC from destructively high surge currents. See Note 13 for determination of R_{CC}. In addition, it is recommended that a ceramic disc bypass capacitor of 0.01 µf be placed between Pins 8 and 5 to reduce the effect of power supply noise.

For interfacing AC signals to TTL systems, output low pass filtering can be performed with a pullup resistor of 1.5 kΩ and 20 µf capacitor. This application requires a Schmitt trigger gate to avoid slow rise time chatter problems. For AC input applications, a filter capacitor can be placed across the DC input terminals for either signal or transient filtering.

Either AC (Pins 1, 4) or DC (Pins 2, 3) input can be used to determine external threshold levels.

For one specifically selected external threshold voltage level V_+ or V_-, R_x can be determined without use of R_p via

$$R_X = \frac{V_{+(-)} - V_{TH(-)}}{I_{TH+(-)}} \quad (1)$$

For two specifically selected external threshold voltage levels, V_+ and V_-, the use of R_X and R_p will permit this selection via equations (2), (3) provided the following conditions are met. If the denominator of equation (2) is positive, then

$$\frac{V_+}{V_-} \geq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}}$$

Conversely, if the denominator of equation (2) is negative, then

$$\frac{V_+}{V_-} \leq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} > \frac{I_{TH+}}{I_{TH-}}$$

$$R_X = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_{TH-}) - I_{TH-}(V_{TH+})} \quad (2)$$

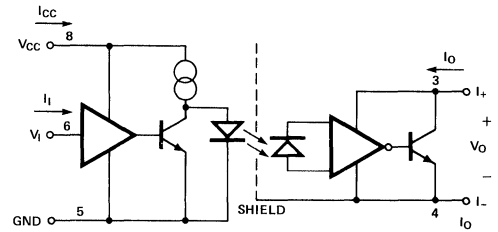
$$R_p = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_- - V_{TH-}) + I_{TH-}(V_{TH+} - V_+)} \quad (3)$$

HEWLETT PACKARD

OPTICALLY COUPLED 20 mA CURRENT LOOP TRANSMITTER

HCPL-4100

SCHEMATIC

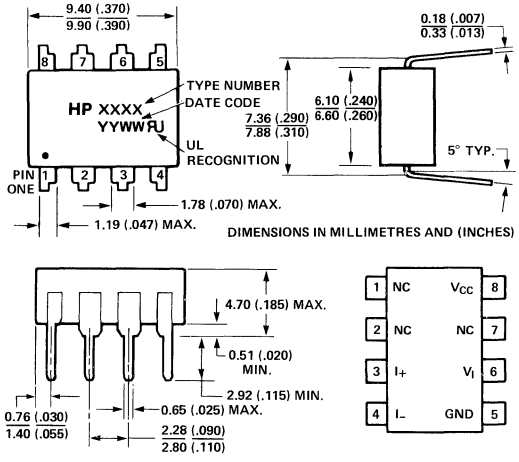


TRUTH TABLE
(POSITIVE LOGIC)*

V_I	V_{CC}	I_O
H	ON	H
L	ON	L
H	OFF	H
L	OFF	H

*CURRENT LOOP CONVENTION —
H = MARK: $I_O \geq 12$ mA,
L = SPACE: $I_O \leq 2$ mA.

OUTLINE DRAWING*



Features

- **GUARANTEED 20 mA LOOP PARAMETERS**
- **DATA INPUT COMPATIBLE WITH LSTTL, TTL AND CMOS LOGIC**
- **GUARANTEED PERFORMANCE OVER TEMPERATURE (0°C TO 70°C)**
- **INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION**
- **20 KBaud DATA RATE AT 400 METRES LINE LENGTH**
- **GUARANTEED ON AND OFF OUTPUT CURRENT LEVELS**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **VDE 0883 APPROVAL PENDING**
- **OPTICALLY COUPLED 20 mA CURRENT LOOP RECEIVER, HCPL-4200, ALSO AVAILABLE.**

Applications

- **IMPLEMENT AN ISOLATED 20 mA CURRENT LOOP TRANSMITTER IN:**
  - **Computer Peripherals**
  - **Industrial Control Equipment**
  - **Data Communications Equipment**

Description

The HCPL-4100 optocoupler is designed to operate as a transmitter in equipment using the 20 mA current loop. 20 mA current loop systems conventionally signal a logic high state by transmitting 20 mA of loop current (MARK), and signal a logic low state by allowing no more than a few milliamperes of loop current (SPACE). Optical coupling of the signal from the logic input to the 20 mA current loop breaks ground loops and provides very high immunity to common mode interference.

The HCPL-4100 data input is compatible with LSTTL, TTL, and CMOS logic gates. The input integrated circuit drives a GaAsP LED. The light emitted by the LED is sensed by a second integrated circuit that allows 20 mA to pass with a voltage drop of less than 2.7 volts when no light is emitted and allows less than 2 mA to pass when light is emitted. The transmitter output is capable of withstanding 27 volts. The input integrated circuit provides a controlled amount of LED drive current and takes into account LED light output degradation. The internal shield allows a guaranteed 1000 V/μs common mode transient immunity.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Input Voltage Low	V_{IL}	0	0.8	Volts
Input Voltage High	V_{IH}	2.0	20	Volts
Operating Temperature	T_A	0	70	°C
Output Voltage	V_O	0	27	Volts
Output Current	I_O	0	24	mA

Absolute Maximum Ratings

(No Derating Required up to 55° C)

Storage Temperature ..... -55° C to 125° C
Operating Temperature ..... -40° C to 85° C
Lead Solder Temperature ..... 260° C for 10 sec.
(1.6 mm below seating plane)
Supply Voltage — V_{CC} ..... 0 to 20 V
Average Output Current — I_O ..... -30 mA to 30 mA
Peak Output Current — I_O ..... internally limited
Output Voltage — V_O ..... -0.4 V to 27 V
Input Voltage — V_I ..... -0.5 V to 20 V
Input Power Dissipation — P_I ..... 265 mW[1]
Output Power Dissipation — P_O ..... 125 mW[2]
Total Power Dissipation — P ..... 360 mW[3]

Electrical Specifications

For 0°C ≤ T_A ≤ 70°C, 4.5 V ≤ V_{CC} ≤ 20 V, all typicals at T_A = 25°C and V_{CC} = 5 V unless otherwise noted. See note 12.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Mark State Output Voltage	V_{MO}		1.8 2.2 2.35	2.25 2.7	Volts Volts Volts	I_O = 2 mA I_O = 12 mA I_O = 20 mA	V_I = 2.0 V	1, 2	
Mark State Short Circuit Output Current	I_{SC}	30	85		mA	V_I = 2 V, V_O = 5 V to 27 V			4
Space State Output Current	I_{SO}	0.5	1.1	2.0	mA	V_I = 0.8 V, V_O = 27 V		3	
Low Level Input Current	I_{IL}		-0.12	-0.32	mA	V_{CC} = 20 V, V_I = 0.4 V			
Low Level Input Voltage	V_{IL}			0.8	Volts				
High Level Input Voltage	V_{IH}	2.0			Volts				
High Level Input Current	I_{IH}		 0.005	20 100 250	μA μA μA	V_I = 2.7 V V_I = 5.5 V V_I = 20 V			
Supply Current	I_{CC}		7.0 7.8	11.5 13	mA mA	V_{CC} = 5.5 V V_{CC} = 20 V	0 V ≤ V_I ≤ 20 V		
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	R_H ≤ 50%, t = 1 min. T_A = 25°C			5
Resistance (input-output)	R_{I-O}		10^{12}		Ohms	V_{I-O} = 500 V dc			5
Capacitance (input-output)	C_{I-O}		1		pF	f = 1 MHz, V_{I-O} = 0 V dc			5

Notes:
1. Derate linearly above 55° C free air temperature at a rate of 3.8 mW/° C. Proper application of the derating factors will prevent IC junction temperatures from exceeding 125° C for ambient temperatures up to 85° C.
2. Derate linearly above a free-air temperature of 70° C at a rate of 2.3 mW/° C. A significant amount of power may be dissipated in the HCPL-4100 output circuit during the transition from the SPACE state to the MARK state when driving a data line or capacitive load (C_{OUT}). The average power dissipation during the transition can be estimated from the following equation which assumes a linear discharge of a capacitive load: $P = I_{SC} (V_{SO} + V_{MO})/2$, where V_{SO} is the output voltage in the SPACE state. The duration of this transition can be estimated as $t = C_{OUT} (V_{SO} - V_{MO})/I_{SC}$. For typical applications driving twisted pair data lines with NRZ data as shown in Figure 11, the transition time will be less than 10% of one bit time.
3. Derate linearly above 55° C free-air temperature at a rate of 5.1 mW/° C.
4. The maximum current that will flow into the output in the mark state (I_{SC}) is internally limited to protect the device. The duration of the output short circuit shall not exceed 10 ms.
5. The device is considered a two terminal device, pins 1, 2, 3, and 4 are connected together, and pins 5, 6, 7, and 8 are connected together.

Switching Specifications

for $0 \leq T_A \leq 70°C$, $4.5\ V \leq V_{CC} \leq 20\ V$, all typicals at $T_A = 25°C$ and $V_{CC} = 5\ V$ unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units	Testing Conditions	Fig.	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		0.3	1.6	μs	$C_O = 1000\ pF$, $C_L = 15\ pF$, $I_O = 20\ mA$	4, 5, 6	6
Propagation Delay Time to Logic Low Output Level	t_{PHL}		0.2	1.0	μs	$C_O = 1000\ pF$, $C_L = 15\ pF$, $I_O = 20\ mA$	4, 5, 6	7
Propagation Delay Time Skew	t_{PLH}-t_{PHL}		0.1		μs	$I_O = 20\ mA$		
Output Rise Time (10-90%)	t_r		16		ns	$I_O = 20\ mA$, $C_O = 1000\ pF$, $C_L = 15\ pF$.	5, 7	8
Output Fall Time (90-10%)	t_f		23		ns	$I_O = 20\ mA$, $C_O = 1000\ pF$, $C_L = 15\ pF$.	5, 7	9
Common Mode Transient Immunity at Logic High Output Level	$\lvert CM_H \rvert$	1,000	10,000		$V/\mu s$	$V_I = 2\ V$, $T_A = 25°C$ $V_{CM} = 50\ V$ (peak), $V_{CC} = 5\ V$ I_O (min.) = 12 mA	8, 9	10
Common Mode Transient Immunity at Logic Low Output Level	$\lvert CM_L \rvert$	1,000	10,000		$V/\mu s$	$V_I = 0.8\ V$, $T_A = 25°C$ $V_{CM} = 50\ V$ (peak), $V_{CC} = 5\ V$ I_O (max.) = 3 mA	8, 9	11

Insulation Related Specifications

Parameter	Symbol	Min.	Units	Conditions
Min. External Air Gap (Clearance)	L (IO1)	≥ 7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L (IO2)	≥ 7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

Notes:

6. The t_{PLH} propagation delay is measured from the 1.3 volt level on the leading edge of the input pulse to the 10 mA level on the leading edge of the output pulse.
7. The t_{PHL} propagation delay is measured from the 1.3 volt level on the trailing edge of the input pulse to the 10 mA level on the trailing edge of the output pulse.
8. The rise time, t_r, is measured from the 10% to the 90% level on the rising edge of the output current pulse.
9. The fall time, t_f, is measured from the 90% to the 10% level on the falling edge of the output current pulse.
10. The common mode transient immunity in the logic high level is the maximum (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, that can be sustained with the output in a Mark ("H") state (i.e., $I_O > 12\ mA$).
11. The common mode transient immunity in the logic low level is the maximum (negative) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, that can be sustained with the output in a Space ("L") state (i.e., $I_O > 3\ mA$).
12. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.

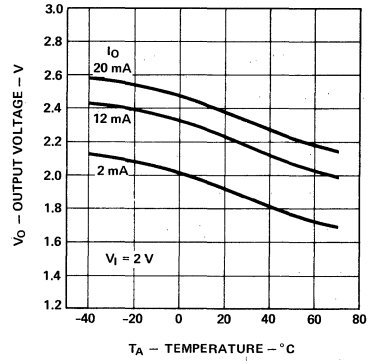


Figure 1. Typical Mark State Output Voltage vs. Temperature

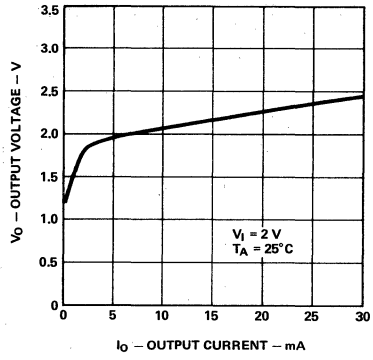


Figure 2. Typical Output Voltage vs. Output Current in Mark State

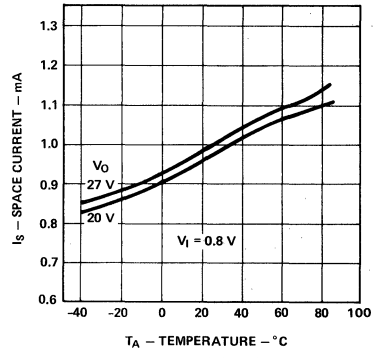


Figure 3. Typical Space State Output Current vs. Temperature

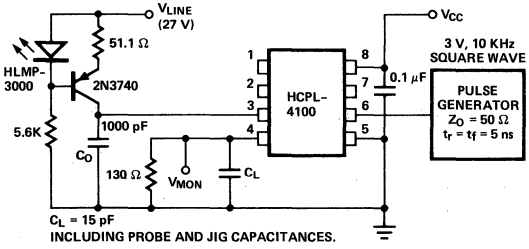


Figure 4. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

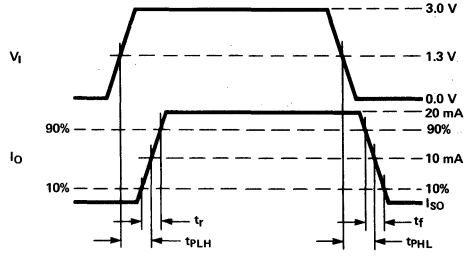


Figure 5. Waveforms for t_{PLH}, t_{PHL}, t_r, and t_f

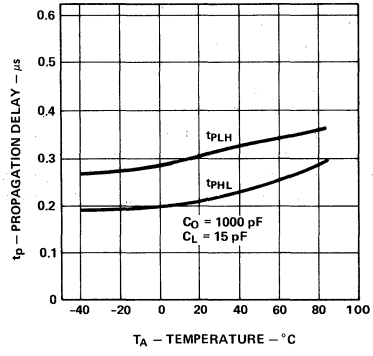


Figure 6. Typical Propagation Delay vs. Temperature

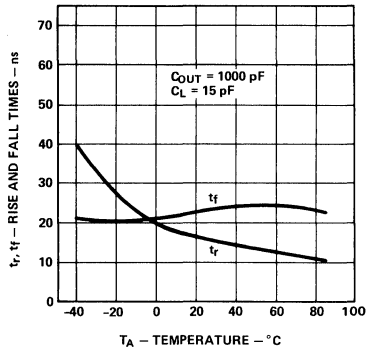


Figure 7. Typical Rise, Fall Times vs. Temperature

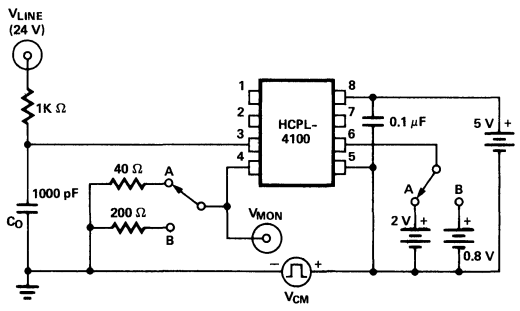


Figure 8. Test Circuit for Common Mode Transient Immunity

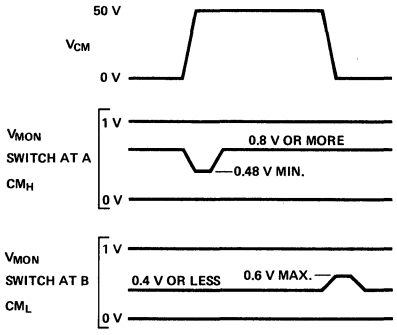


Figure 9. Typical Waveforms for Common Mode Transient Immunity

Applications

Data transfer between equipment which employs current loop circuits can be accomplished via one of three configurations: simplex, half duplex or full duplex communication. With these configurations, point to point and multidrop arrangements are possible. The appropriate configuration to use depends upon data rate, number of stations, number and length of lines, direction of data flow, protocol, current source location and voltage compliance value, etc.

SIMPLEX

The simplex configuration, whether point to point or multidrop, gives unidirectional data flow from transmitter(s) to receiver. This is the simplest configuration for use in long line length (two wire), moderate data rate, and low current source compliance level applications. A block diagram of simplex point to point arrangement is given in Figure 10 for the HCPL-4100 transmitter optocoupler.

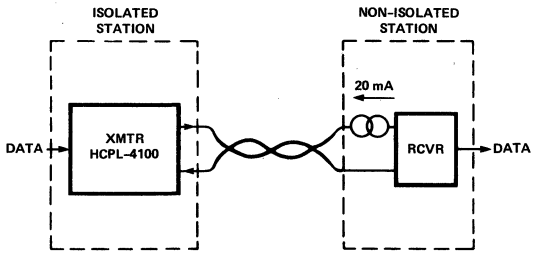


Figure 10. Simplex Point to Point Current Loop System Configuration

Major factors which limit maximum data rate performance for a simplex loop are the location and compliance voltage of the loop current source as well as the total line capacitance. Application of the HCPL-4100 transmitter in a simplex loop necessitates that a non-isolated active receiver (containing current source) be used at the opposite end of the current loop. With long line length, large line capacitance will need to be charged to the compliance voltage level of the current source before the receiver loop current decreases to zero. This effect limits upper data rate performance. Slower data rates will occur with larger compliance voltage levels. The maximum compliance level is determined by the transmitter breakdown characteristic. In addition, adequate compliance of the current source must be available for voltage drops across station(s) during the MARK state in multidrop applications for long line lengths.

In a simplex multidrop application with multiple HCPL-4100 transmitters and one non-isolated active receiver, priority of transmitters must be established.

A recommended non-isolated active receiver circuit which can be used with the HCPL-4100 in point to point or in multidrop 20 mA current loop applications is given in Figure 11. This non-isolated active receiver current threshold must be chosen properly in order to provide adequate noise immunity as well as not to detect SPACE state current (bias current) of the HCPL-4100 transmitter. The receiver input threshold current is Vth/Rth ≈ 10 mA. A simple transistor current source provides a nominal 20 mA loop current over a V_{CC} compliance range of 6 V dc to 27 V dc. A resistor can be used in place of the constant current source for simple applications where the wire loop distance and number of stations on the loop are fixed. A minimum transmitter output load capacitance of 1000 pF is required between pins 3 and 4 to ensure absolute stability.

Length of the current loop (one direction) versus minimum required DC supply voltage, V_{CC}, of the circuit in Figure 11 is graphically illustrated in Figure 12. Multidrop configurations will require larger V_{CC} than Figure 12 predicts in order to account for additional station terminal voltage drops.

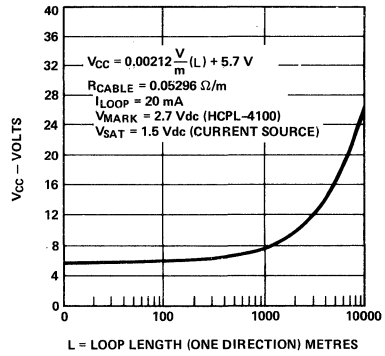


Figure 12. Miminum Required Supply Voltage, V_{CC}, vs. Loop Length for Current Loop Circuit of Figure 12

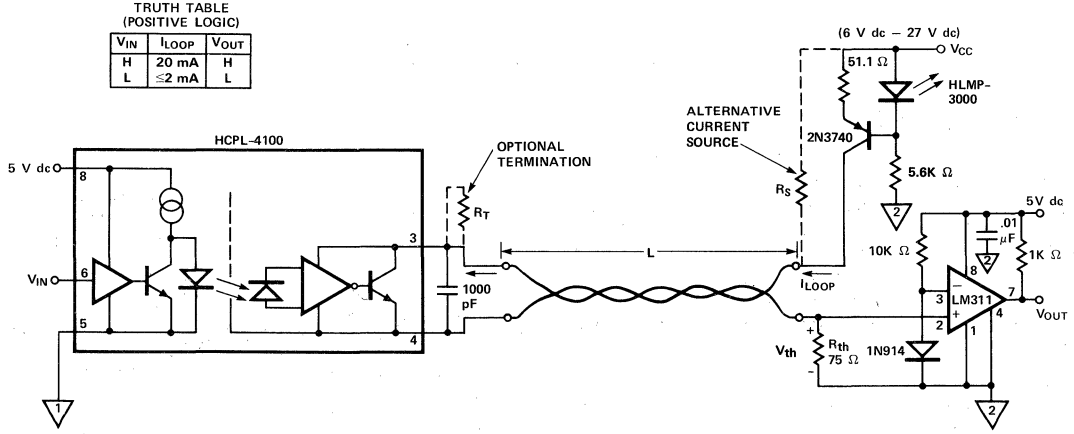


Figure 11. Recommended Non-Isolated Active Receiver with HCPL-4100 Isolated Transmitter for Simplex Point to Point 20 mA Current Loop

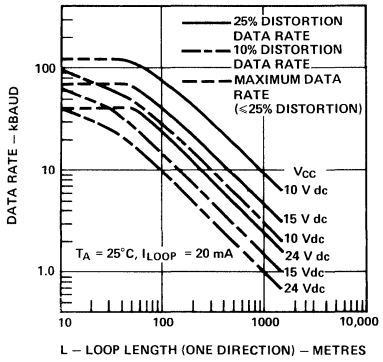


Figure 13. Typical Data Rate vs. Distance and Supply Voltage

Typical data rate performance versus distance is illustrated in Figure 13 for the combination of a non-isolated active receiver and HCPL-4100 optically coupled current loop transmitter shown in Figure 11. Curves are shown for 25% distortion data rate at different V_{CC} values. 25% distortion data rate is defined as that rate at which 25% distortion occurs to output bit interval with respect to the input bit interval. Maximum data rate (dotted line) is restricted by device characteristics. An input Non-Return-to-Zero (NRZ) test waveform of 16 bits (0000001011111101) was used for data rate distortion measurements. Enhanced speed performance of the loop system can be obtained with lower V_{CC} supply levels, as illustrated in Figure 13. In addition, when loop current is supplied through a resistor instead of by a current source, an additional series termination resistance equal to the characteristic line impedance can be used at the HCPL-4100 transmitter end to enhance speed of response by approximately 20%.

The cable used contained five pairs of unshielded, twisted, 22 AWG wire (Dearborn #862205). Loop current is 20 mA nominal. Input and output logic supply voltages are 5 V dc.

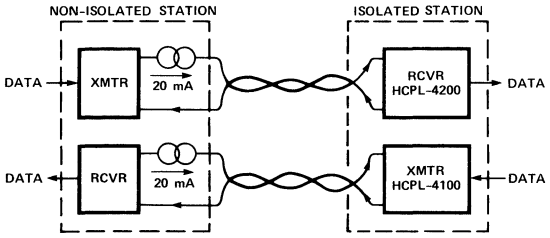


Figure 14. Full Duplex Point to Point Current Loop System Configuration

FULL DUPLEX

Full duplex point to point communication of Figure 14 uses a four wire system to provide simultaneous, bi-directional data communication between local and remote equipment. Basic application uses two simplex point to point loops which have two separate, active, non-isolated units at one common end of the loops. The other end of each loop is isolated.

As Figure 14 illustrates, the combination of Hewlett-Packard current loop optocouplers, HCPL-4100 transmitter and HCPL-4200 receiver, can be used at the isolated end of current loops. Cross talk and common mode coupling are greatly reduced when optical isolation is implemented at the same end of both loops, as shown. Full duplex data rate is limited by the non-isolated active receiver current loop. Comments mentioned under simplex configuration apply to the full duplex case. Consult the HCPL-4200 receiver optocoupler data sheet for specified device performance.

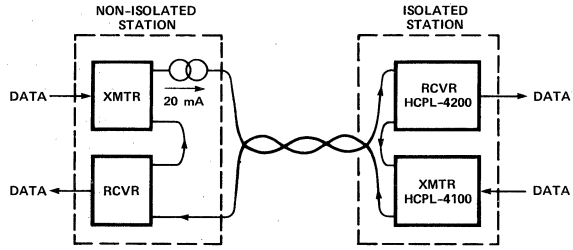
HALF DUPLEX

The half duplex configuration, whether point to point or multidrop, gives non-simultaneous bidirectional data flow from transmitters to receivers shown in Figures 15a and 15b. This configuration allows the use of two wires to carry data back and forth between local and remote units. However, protocol must be used to determine which specific transmitter can operate at any given time. Maximum data rate for a half duplex system is limited by the loop current charging time. These considerations were explained in the Simplex configuration section.

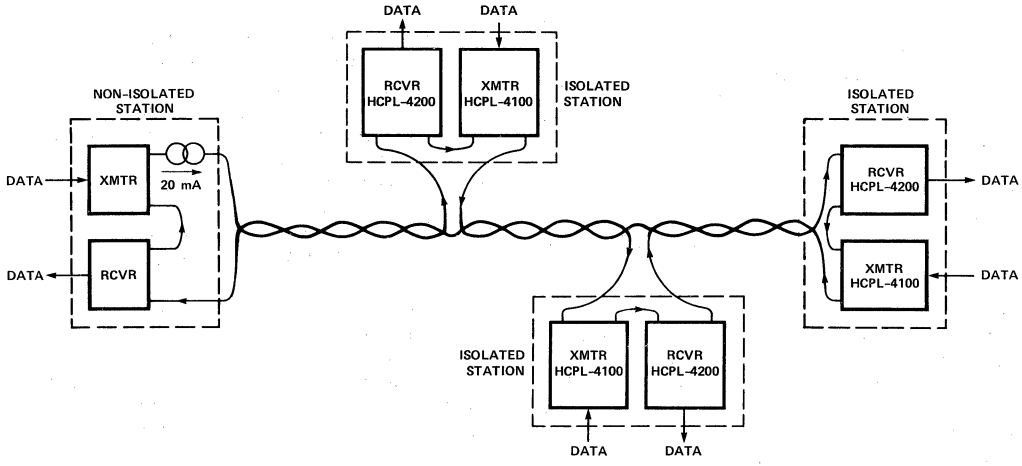
Figures 15a and 15b illustrate half duplex application for the combination of HCPL-4100/-4200 optocouplers. The unique and complementary designs of the HCPL-4100 transmitter and HCPL-4200 receiver optocouplers provide many designed-in benefits. For example, total optical isolation at one end of the current loop is easily accomplished, which results in substantial removal of common mode influences, elimination of ground potential differences and reduction of power supply requirements. With this combination of HCPL-4100/-4200 optocouplers, specific current loop noise immunity is provided, i.e., minimum SPACE state current noise immunity is 1 mA, MARK state noise immunity is 8 mA.

Voltage compliance of the current source must be of an adequate level for operating all units in the loop while not exceeding 27 V dc, the maximum breakdown voltage for the HCPL-4100. Note that the HCPL-4100 transmitter will allow output loop current to conduct when input V_{CC} power is off. Consult the HCPL-4200 receiver optocoupler data sheet for specified device performance.

For more informaton about the HCPL-4100/-4200 optocouplers, consult Application Note 1018.



(a) POINT TO POINT



(b) MULTIDROP

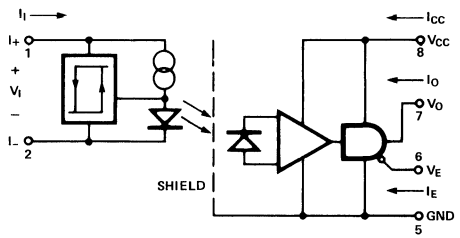
Figure 15. Half Duplex Current Loop System Configurations for (a) Point to Point, (b) Multidrop

HEWLETT PACKARD

OPTICALLY COUPLED 20 mA CURRENT LOOP RECEIVER

HCPL-4200

SCHEMATIC

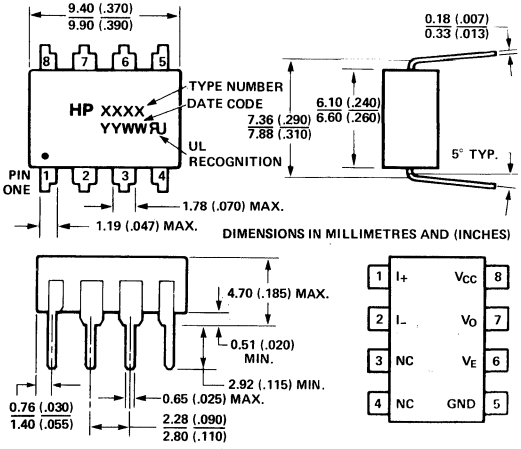


TRUTH TABLE (POSITIVE LOGIC)*

I_I	V_E	V_O
H	H	Z
L	H	Z
H	L	H
L	L	L

*CURRENT LOOP CONVENTION —
H = MARK: $I_I \geq 12$ mA,
L = SPACE: $I_I \leq 3$ mA,
Z = OFF (HIGH IMPEDANCE) STATE.

OUTLINE DRAWING*



Features

- **DATA OUTPUT COMPATIBLE WITH LSTTL, TTL AND CMOS**
- **20 K BAUD DATA RATE AT 1400 METRES LINE LENGTH**
- **GUARANTEED PERFORMANCE OVER TEMPERATURE (0°C TO 70°C)**
- **GUARANTEED ON AND OFF THRESHOLDS**
- **LED IS PROTECTED FROM EXCESS CURRENT**
- **INPUT THRESHOLD HYSTERESIS**
- **THREE-STATE OUTPUT COMPATIBLE WITH DATA BUSES**
- **INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 2500 Vac, 1 MINUTE**
- **OPTICALLY COUPLED 20 mA CURRENT LOOP TRANSMITTER, HCPL-4100, ALSO AVAILABLE.**
- **VDE 0883 APPROVAL PENDING**

Applications

- **IMPLEMENT AN ISOLATED 20 mA CURRENT LOOP RECEIVER IN:**
  - **Computer Peripherals**
  - **Industrial Control Equipment**
  - **Data Communications Equipment**

Description

The HCPL-4200 optocoupler is designed to operate as a receiver in equipment using the 20 mA Current Loop. 20 mA current loop systems conventionally signal a logic high state by transmitting 20 mA of loop current (MARK), and signal a logic low state by allowing no more than a few milliamperes of loop current (SPACE). Optical coupling of the signal from the 20 mA current loop to the logic output breaks ground loops and provides for a very high common mode rejection. The HCPL-4200 aids in the design process by providing guaranteed thresholds for logic high state and logic low state for the current loop, providing an LSTTL, TTL, or CMOS compatible logic interface, and providing guaranteed common mode rejection. The buffer circuit on the current loop side of the HCPL-4200 provides typically 0.8 mA of hysteresis which increases the immunity to common mode and differential mode noise. The buffer also provides a controlled amount of LED drive current which takes into account LED light output degradation. The internal shield allows a guaranteed 1000 V/μs common mode transient immunity.

OPTOCOUPLERS

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Forward Input Current (SPACE)	I_{SI}	0	2.0	mA
Forward Input Current (MARK)	I_{MI}	14	24	mA
Operating Temperature	T_A	0	70	°C
Fan Out	N	0	4	TTL Loads
Logic Low Enable Voltage	V_{EL}	0	0.8	Volts
Logic High Enable Voltage	V_{EH}	2.0	20	Volts

Absolute Maximum Ratings

(No Derating Required up to 70° C)

Storage Temperature ..... —55° C to 125° C
Operating Temperature ..... —40° C to 85° C
Lead Solder Temperature ..... 260° C for 10 sec.
(1.6 mm below the seating plane)
Supply Voltage — V_{CC} ..... 0 V to 20 V
Average Input Current — I_I ..... —30 mA to 30 mA
Peak Transient Input Current — I_I ..... 0.5 A[1]
Enable Input Voltage — V_E ..... —0.5 V to 20 V
Output Voltage — V_O ..... —0.5 V to 20 V
Average Output Current — I_O ..... 25 mA
Input Power Dissipation — P_I ..... 90 mW[2]
Output Power Dissipation — P_O ..... 210 mW[3]
Total Power Dissipation — P ..... 255 mW[4]

Electrical Specifications

For 0° C ≤ T_A ≤ 70° C, 4.5 V ≤ V_{CC} ≤ 20 V, V_E = 0.8 V, all typicals at T_A = 25° C and V_{CC} = 5 V unless otherwise noted. See note 13.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Mark State Input Current	I_{MI}	12			mA			1, 2, 3	
Mark State Input Voltage	V_{MI}		2.52	2.75	Volts	I_I = 20 mA	V_E = Don't Care	3, 4	
Space State Input Current	I_{SI}			3	mA			1, 2, 3	
Space State Input Voltage	V_{SI}		1.6	2.2	Volts	I_I = 0.5 to 2.0 mA	V_E = Don't Care	1, 3	
Input Hysteresis Current	I_{HYS}	0.3	0.8		mA			1	
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads)	I_I = 3 mA	5	
Logic High Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -2.6 mA,	I_I = 12 mA	6	
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	μA	V_O = 5.5 V	I_I = 20 mA		
				500	μA	V_O = 20 V	V_{CC} = 4.5 V		
Logic High Enable Voltage	V_{EH}	2.0			Volts				
Logic Low Enable Voltage	V_{EL}			0.8	Volts				
Logic High Enable Current	I_{EH}			20	μA	V_E = 2.7 V			
				100	μA	V_E = 5.5 V			
			.004	250	μA	V_E = 20 V			
Logic Low Enable Current	I_{EL}			-0.32	mA	V_E = 0.4 V			
Logic Low Supply Current	I_{CCL}		4.5	6.0	mA	V_{CC} = 5.5 V	I_I = 0 mA		
			5.25	7.5	mA	V_{CC} = 20 V	V_E = Don't Care		
Logic High Supply Current	I_{CCH}		2.7	4.5	mA	V_{CC} = 5.5 V	I_I = 20 mA		
			3.1	6.0	mA	V_{CC} = 20 V	V_E = Don't Care		
High Impedance State Output Current	I_{OZL}			-20	μA	V_O = 0.4 V	V_E = 2.0 V, I_I = 20 mA		
	I_{OZH}			20	μA	V_O = 2.4 V	V_E = 2 V, I_I = 0 mA		
				100	μA	V_O = 5.5 V			
				500	μA	V_O = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	V_O = V_{CC} = 5.5 V	I_I = 0 mA		
		40			mA	V_O = V_{CC} = 20 V			5
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5 V	I_I = 20 mA		5
		-25			mA	V_{CC} = 20 V	V_O = GND		
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	R_H ≤ 50%, t = 1 min. T_A = 25° C			6
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 V dc			6
Input-Output Capacitance	C_{I-O}		1.0		pF	f = 1 MHz, V_{I-O} = 0 V dc			6
Input Capacitance	C_{IN}		120		pF	f = 1 MHz, V_I = 0 V dc, Pins 1 and 2			

Switching Specifications

For 0° C ≤ T_A ≤ 70° C, 4.5 V ≤ V_{CC} ≤ 20 V, V_E = 0.8 V, all typicals at T_A = 25° C and V_{CC} = 5 V unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		0.23	1.6	μs	V_E = 0 V, C_L = 15 pF	7, 8, 9	7
Propagation Delay Time to Logic Low Output Level	t_{PHL}		0.17	1.0	μs	V_E = 0 V, C_L = 15 pF	7, 8, 9	8
Propagation Delay Time Skew	t_{PLH}-t_{PHL}		60		ns	I_I = 20 mA, C_L = 15 pF	7, 8, 9	
Output Enable Time to Logic Low Level	t_{PZL}		25		ns	I_I = 0 mA, C_L = 15 pF	11, 12, 14	
Output Enable Time to Logic High Level	t_{PZH}		28		ns	I_I = 20 mA, C_L = 15 pF	11, 12, 13	
Output Disable Time from Logic Low Level	t_{PLZ}		60		ns	I_I = 0 mA, C_L = 15 pF	11, 12, 14	
Output Disable Time from Logic High Level	t_{PHZ}		105		ns	I_I = 20 mA, C_L = 15 pF	11, 12, 13	
Output Rise Time (10-90%)	t_r		55		ns	V_{CC} = 5 V, C_L = 15 pF	7, 8, 10	9
Output Fall Time (90-10%)	t_f		15		ns	V_{CC} = 5 V, C_L = 15 pF	7, 8, 10	10
Common Mode Transient Immunity at Logic High Output Level	$\|CM_H\|$	1,000	10,000		V/μs	V_{CM} = 50 V (peak) I_I = 12 mA, T_A = 25° C	15, 16	11
Common Mode Transient Immunity at Logic Low Output Level	$\|CM_L\|$	1,000	10,000		V/μs	V_{CM} = 50 V (peak) I_I = 3 mA, T_A = 25° C	15, 16	12

Insulation Related Specifications

Parameter	Symbol	Min.	Units	Conditions
Min. External Air Gap (Clearance)	L (IO1)	≥ 7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L (IO2)	≥ 7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

NOTES:

1. ≤ 1 μs pulse width, 300 pps.
2. Derate linearly above 70° C free air temperature at a rate of 1.6 mW/° C. Proper application of the derating factors will prevent IC junction temperatures from exceeding 125° C for ambient temperatures up to 85° C.
3. Derate linearly above 70° C free air temperature at a rate of 3.8 mW/° C.
4. Derate linearly above 70° C free air temperature at a rate of 4.6 mW/° C.
5. Duration of output short circuit time shall not exceed 10 ms.
6. The device is considered a two terminal device, pins 1, 2, 3, and 4 are connected together and pins 5, 6, 7, and 8 are connected together.
7. The t_{PLH} propagation delay is measured from the 10 mA level on the leading edge of the input pulse to the 1.3 V level on the leading edge of the output pulse.
8. The t_{PHL} propagation delay is measured from the 10 mA level on the trailing edge of the input pulse to the 1.3 V level on the trailing edge of the output pulse.
9. The rise time, t_r, is measured from the 10% to the 90% level on the rising edge of the output logic pulse.
10. The fall time, t_f, is measured from the 90% to the 10% level on the falling edge of the output logic pulse.
11. Common mode transient immunity in the logic high level is the maximum (negative) dV_{CM}/dt on the trailing edge of the common mode pulse, V_{CM}, which can be sustained with the output voltage in the logic high state (i.e., $V_O \geq 2$ V).
12. Common mode transient immunity in the logic low level is the maximum (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, which can be sustained with the output voltage in the logic low state (i.e., $V_O \geq 0.8$ V).
13. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.

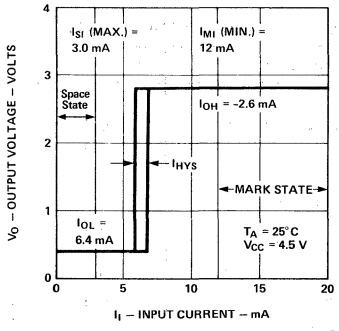


Figure 1. Typical Output Voltage vs. Loop Current

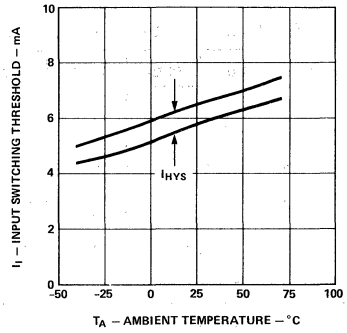


Figure 2. Typical Current Switching Threshold vs. Temperature

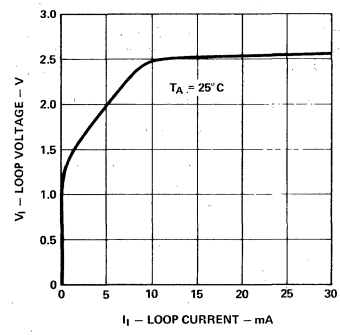


Figure 3. Typical Input Loop Voltage vs. Input Current

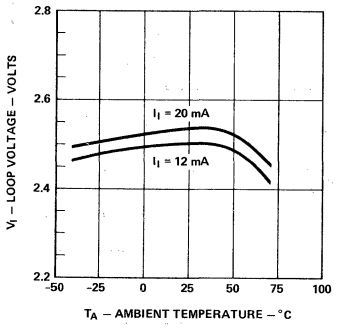


Figure 4. Typical Input Voltage vs. Temperature

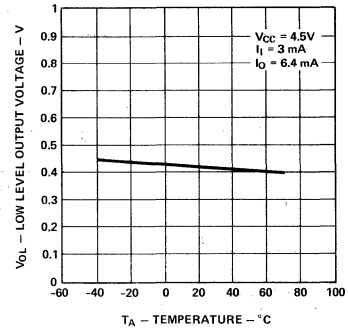


Figure 5. Typical Logic Low Output Voltage vs. Temperature

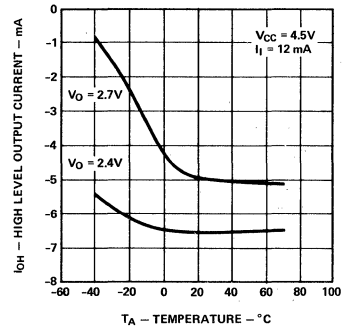
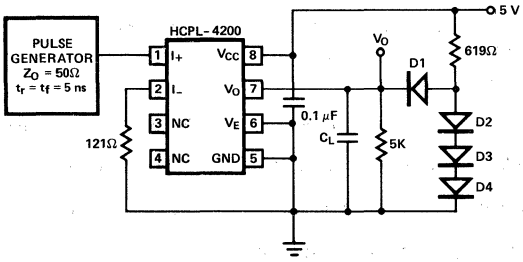


Figure 6. Typical Logic High Output Current vs. Temperature



V_{IN} = 5 VOLT, 100 KHz 10% DUTY CYCLE
D1 - D4 ARE 1N916 OR 1N3064

C_L = 15 pF INCLUDING PROBE AND JIG CAPACITANCE

Figure 7. Test Circuit for t_{PHL}, t_{PLH}, t_r, and t_f

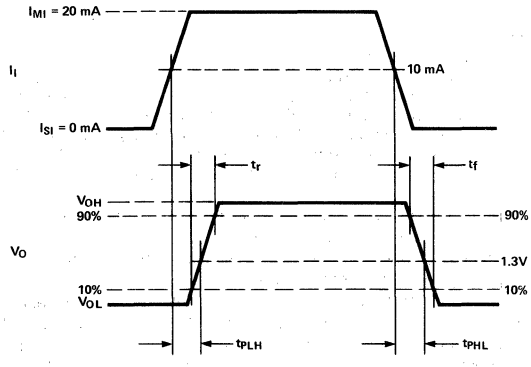


Figure 8. Waveforms for t_{PHL}, t_{PLH}, t_r, and t_f

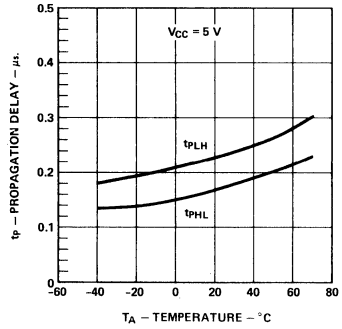


Figure 9. Typical Propagation Delay vs. Temperature

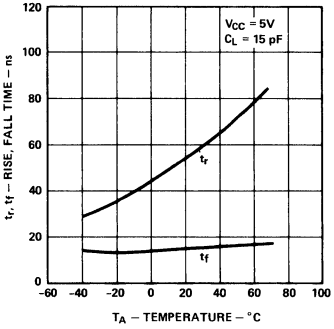


Figure 10. Typical Rise, Fall Time vs. Temperature

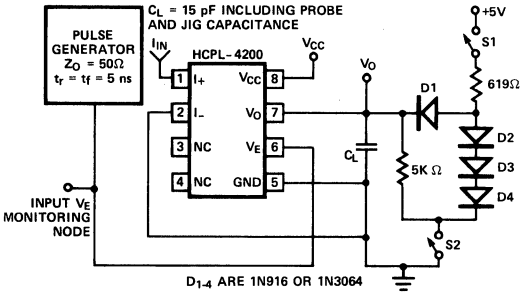


Figure 11. Test Circuit for t_{PZH}, t_{PZL}, t_{PHZ}, and t_{PLZ}

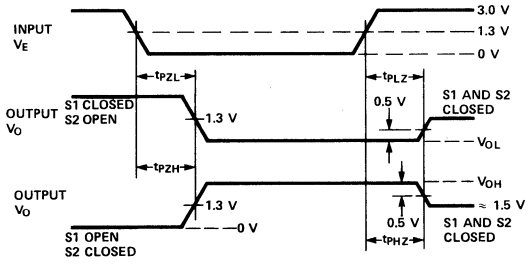


Figure 12. Waveforms for t_{PZH}, t_{PZL}, t_{PHZ}, and t_{PLZ}

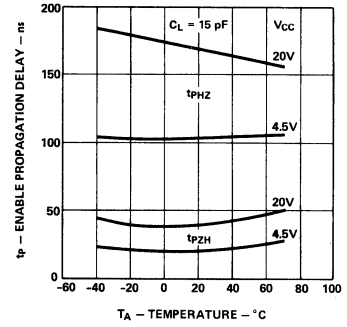


Figure 13. Typical Logic High Enable Propagation Delay vs. Temperature

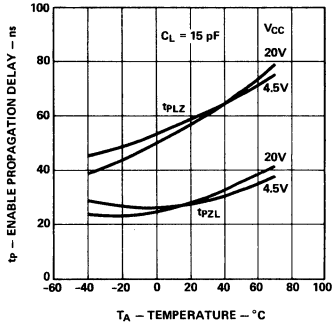


Figure 14. Typical Logic Low Enable Propagation Delay vs. Temperature

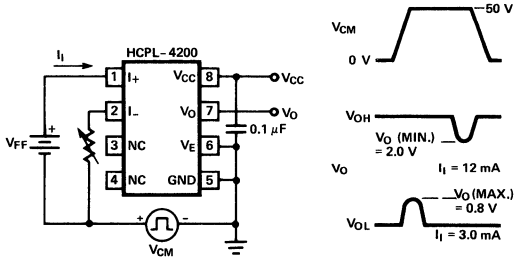


Figure 15. Test Circuit for Common Mode Transient Immunity

Applications

Data transfer between equipment which employs current loop circuits can be accomplished via one of three configurations: simplex, half duplex or full duplex communication. With these configurations, point-to-point and multidrop arrangements are possible. The appropriate configuration to use depends upon data rate, number of stations, number and length of lines, direction of data flow, protocol, current source location and voltage compliance value, etc.

SIMPLEX

The simplex configuration, whether point to point or multidrop, gives unidirectional data flow from transmitter to receiver(s). This is the simplest configuration for use in long line length (two wire), for high data rate, and low current source compliance level applications. Block diagrams of simplex point-to-point and multidrop arrangements are given in Figures 16a and 16b respectively for the HCPL-4200 receiver optocoupler.

For the highest data rate performance in a current loop, the configuration of a non-isolated active transmitter (containing current source) transmitting data to a remote isolated receiver(s) should be used. When the current source is located at the transmitter end, the loop is charged approximately to V_{MI} (2.5 V). Alternatively, when the current source is located at the receiver end, the loop is charged to the full compliance voltage level. The lower the charged voltage level the faster the data rate will be. In the configurations of Figures 16a and 16b, data rate is independent of the current source voltage compliance level. An adequate compliance level of current source must be available for voltage drops across station(s) during the MARK state in multidrop applications or for long line length. The maximum compliance level is determined by the transmitter breakdown characteristic.

A recommended non-isolated active transmitter circuit which can be used with the HCPL-4200 in point-to-point or in multidrop 20 mA current loop applications is given in Figure 18. The current source is controlled via a standard TTL 7407 buffer to provide high output impedance of current source in both the ON and OFF states. This non-isolated active transmitter provides a nominal 20 mA loop current for the listed values of V_{CC}, R2 and R3 in Figure 17.

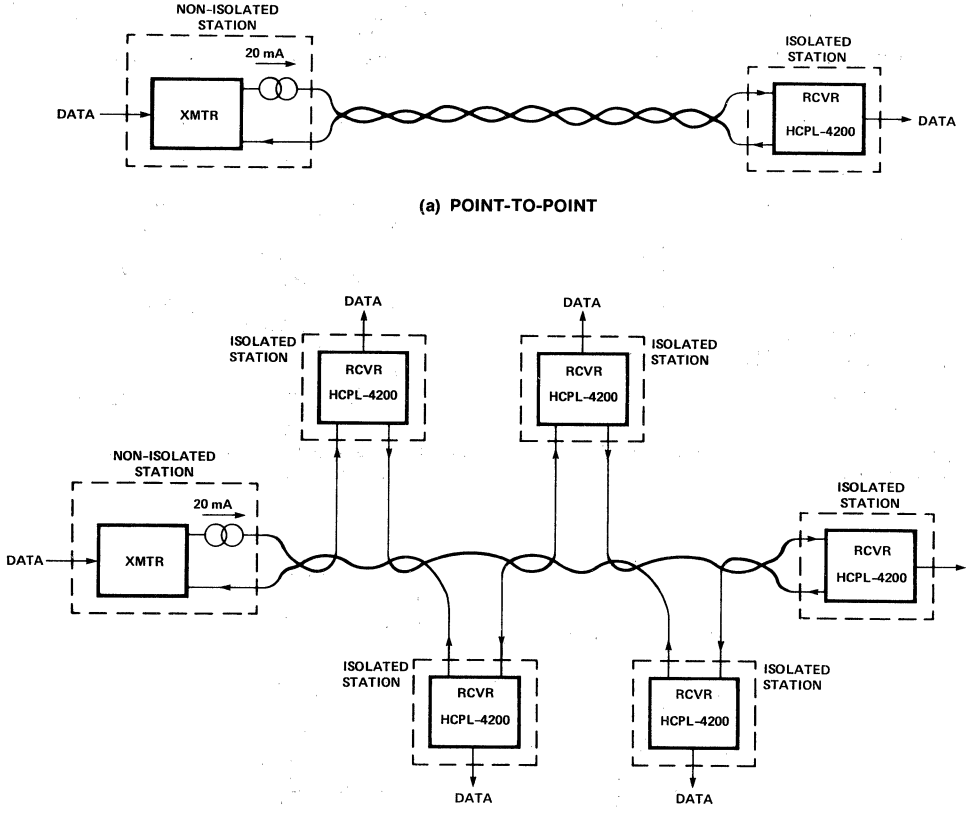


Figure 16. Simplex Current Loop System Configurations for (a) Point-to-Point, (b) Multidrop

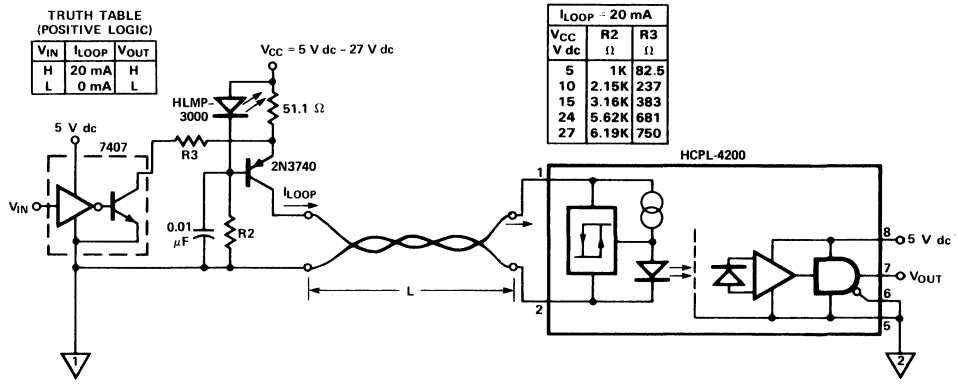


Figure 17. Recommended Non-Isolated Active Transmitter with HCPL-4200 Isolated Receiver for Simplex Point-to-Point 20 mA Current Loop

Length of current loop (one direction) versus minimum required DC supply voltage, V_{CC}, of the circuit in Figure 17 is graphically illustrated in Figure 18. Multidrop configurations will require larger V_{CC} than Figure 18 predicts in order to account for additional station terminal voltage drops.

Typical data rate performance versus distance is illustrated in Figure 19 for the combination of a non-isolated active transmitter and HCPL-4200 optically coupled current loop receiver shown in Figure 17. Curves are shown for 10% and 25% distortion data rate. 10% (25%) distortion data rate is defined as that rate at which 10% (25%) distortion occurs to output bit interval with respect to input bit interval. An input Non-Return-to-Zero (NRZ) test waveform of 16 bits (0000001011111101) was used for data rate distortion measurements. Data rate is independent of current source supply voltage, V_{CC}.

The cable used contained five pairs of unshielded, twisted, 22 AWG wire (Dearborn #862205). Loop current is 20 mA nominal. Input and output logic supply voltages are 5 V dc.

FULL DUPLEX

The full duplex point-to-point communication of Figure 20 uses a four wire system to provide simultaneous, bi-directional data communication between local and remote equipment. The basic application uses two simplex point-to-point loops which have two separate, active, non-isolated units at one common end of the loops. The other end of each loop is isolated.

As Figure 20 illustrates, the combination of Hewlett-Packard current loop optocouplers, HCPL-4100 transmitter and HCPL-4200 receiver, can be used at the isolated end of current loops. Cross talk and common mode coupling are greatly reduced when optical isolation is implemented at the same end of both loops, as shown. The full duplex data rate is limited by the non-isolated active receiver current loop. Comments mentioned under simplex configuration apply to the full duplex case. Consult the HCPL-4100 transmitter optocoupler data sheet for specified device performance.

HALF DUPLEX

The half duplex configuration, whether point-to-point or multidrop, gives non-simultaneous bidirectional data flow from transmitters to receivers shown in Figures 21a and 21b. This configuration allows the use of two wires to carry data back and forth between local and remote units. However, protocol must be used to determine which specific transmitter can operate at any given time. Maximum data rate for a half duplex system is limited by the loop current charging time. These considerations were explained in the Simplex configuration section.

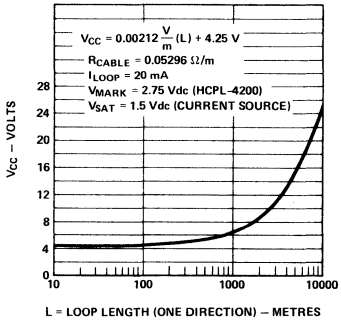


Figure 18. Minimum Required Supply Voltage, V_{CC}, vs. Loop Length for Current Loop Circuit of Figure 18

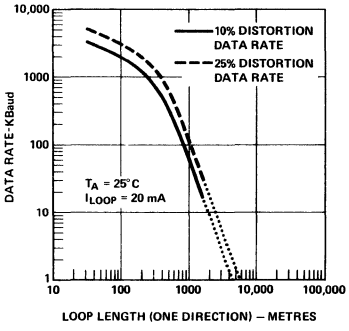


Figure 19. Typical Data Rate vs. Distance

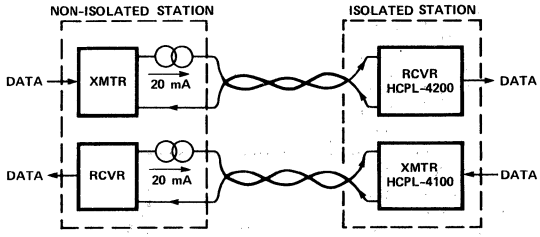
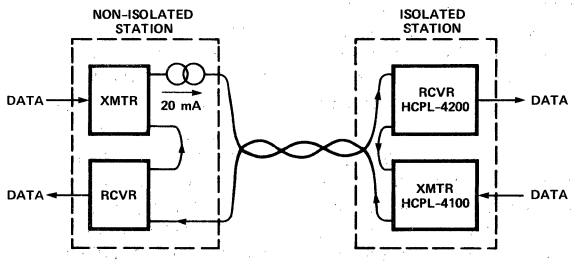


Figure 20. Full Duplex Point-to-Point Current Loop System Configuration

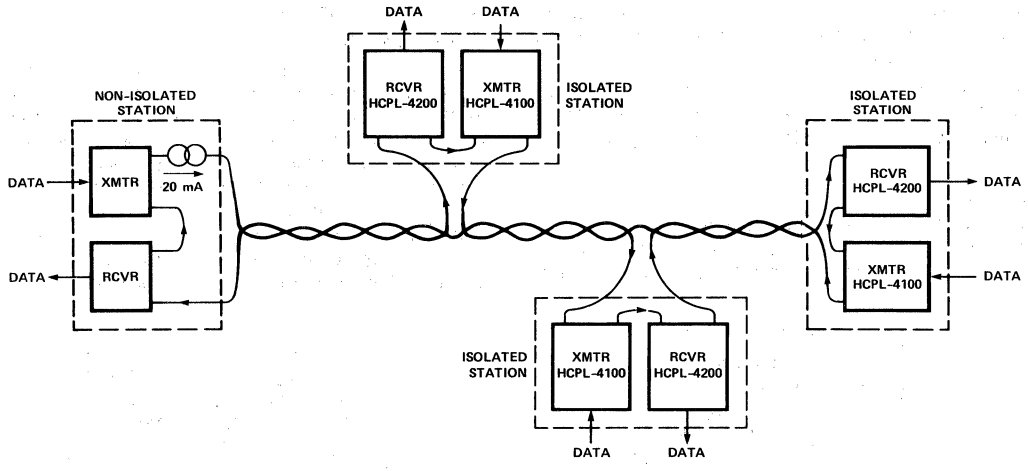
Figures 21a and 21b illustrate half duplex application for the combination of HCPL-4100/-4200 optocouplers. The unique and complementary designs of the HCPL-4100 transmitter and HCPL-4200 receiver optocouplers provide many designed-in benefits. For example, total optical isolation at one end of the current loop is easily accomplished, which results in substantial removal of common mode influences, elimination of ground potential differences and reduction of power supply requirements. With this combination of HCPL-4100/-4200 optocouplers, specific current loop noise immunity is provided, i.e., minimum SPACE state current noise immunity is 1 mA, MARK state noise immunity is 8 mA.

Voltage compliance of the current source must be of an adequate level for operating all units in the loop while not exceeding 27 V dc, the maximum breakdown voltage for the HCPL-4100. Note that the HCPL-4100 transmitter will allow loop current to conduct when input V_{CC} power is off. Consult the HCPL-4100 transmitter optocoupler data sheet for specified device performance.

For more information about the HCPL-4100/-4200 optocouplers, consult Application Note 1018.



(a) POINT-TO-POINT



(b) MULTIDROP

Figure 21. Half Duplex Current Loop System Configurations for (a) Point-to-Point, (b) Multidrop

HEWLETT PACKARD

Optocoupler Option for 5000 Vac/1 Minute Requirement

Technical Data

OPTION 020

Features

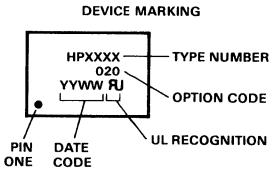
- **Special Construction and Testing**
- **UL Recognition for 5000 Vac/1 Minute Requirement (File No. E55361)**

Description

Option 020 consists of special construction on a wide range of Hewlett-Packard plastic optocouplers. After assembly, each unit is subjected to an equivalent electrical performance test to ensure its capability to withstand 5000 Vac input to output for one minute. This test is recognized by Underwriters Laboratory as proof that these components may be used in many high voltage applications.

Applications

Dielectric withstand voltage ratings are required by Underwriters Laboratory when components are used in certain types of electronic equipment. The voltage rating depends on the type of electronic equipment and the specific application within the equipment. The 5000 Vac/1 Minute dielectric withstand voltage rating provided by Option 020 offers excellent high voltage input to output protection. Some applicable UL documents are listed below.



UL Spec Number	Specification Title
1577	Standard for Optical Isolators Applications
114	Appliance and Business Equipment
347	High Voltage Industrial Control Equipment
478	Information Processing and Business Equipment
508	Industrial Control Equipment
544	Medical and Dental Equipment
698	Industrial Control Equipment for Use in Hazardous Locations
773	Plug-in, Locking Type Photocontrols
913	Intrinsically Safe Apparatus and Associated Apparatus
916	Standard for Energy Management Equipment
1012	Power Supplies
1244	Electrical and Electronic Measuring and Testing Equipment
1410	Television and Video Products

Specifications

All specifications for optocouplers remain unchanged when this option is ordered.

Ordering Information

To obtain this high voltage capability on plastic optocouplers order the standard part number and Option 020.

Examples:

6N135	HCPL-2601
Option 020	Option 020

This option is currently available on the following plastic optocouplers.

6N135/6
6N137
6N138/9
HCPL-2601/11
HCPL-4562
HCPL-4502/3

Contact your local HP Sales Representative concerning availability of this option for optocouplers not listed.

HEWLETT PACKARD

Surface Mount Options for Optocouplers

Technical Data

Option 100/300

Features

- **Surface Mountable**
  - **Leads Trimmed for a Butt Joint Connection (Option 100)**
  - **Leads Formed to a Gull Wing Profile (Option 300)**
- **Compatible with Vapor Phase Reflow and Wave Soldering Process**
- **Meets All Electrical Specifications of Corresponding Standard Part Numbers**
- **Available for All Optocouplers in Plastic Packages**

Description

Option 100 is an optocoupler in a standard sized dual-in-line package, with trimmed leads (butt joint). The distance from the printed circuit board (PCB), to the bottom of the optocoupler package, will be typically 0.035 inches. The height of the optocoupler package is typically 0.150 inches, leaving a distance of 0.185 inches from PCB to the top of the optocoupler package.

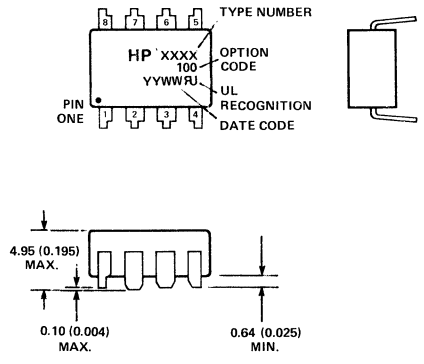
Option 300 is an optocoupler in a standard dual-in-line package with gull wing leads. The lead profile is designed to be compatible with standard surface mount processes. These optocouplers, particularly the duals, allow efficient utilization of valuable board space.

Applications

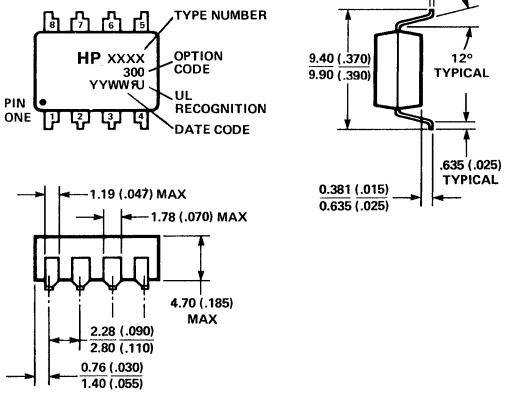
Both options enable electronic component assemblers to include Hewlett-Packard optocouplers on a PCB that utilizes surface mount assembly processes. These options do not require "through holes" in a PCB. This reduces board costs, while potentially increasing assembly rates and increasing component density per board.

OPTOCOUPLERS

Option 100 Drawing



Option 300 Drawing



DIMENSIONS IN MILLIMETRES (INCHES)

Specifications

All electrical specifications for optocouplers remain unchanged when this option is ordered. In addition, the device will withstand typical vapor phase reflow soldering conditions of 215°C for 30 seconds, and wave solder immersion for 5 seconds at 260°C.

Ordering Information

Both options are available for all optocouplers in plastic packages. To obtain these options, order the standard part number and Option 100 or 300.

Examples:

6N136	HCPL-2200
Option 100	Option 300

HEWLETT PACKARD

200-Volt/160-Ohm, 1 Form A Small-Signal Solid State Relay

Technical Data

HSSR-8200

Features

- Compact Solid-State Bi-Directional Signal Switch
- Normally-Off Single-Pole Relay Function (1 Form A)
- Very High Output Off-Impedance: 10,000 Gigaohms Typical at 25°C
- Very Low Output Offset Voltage: < 0.5 μV
- 200-Volt Output Withstand Voltage
- High-Transient Immunity: > 2000 V/μs
- Monolithic High-Voltage IC
- Operating Range: –40°C to +85C
- Very Low Input Current (1 mA); CMOS Compatibility
- High-Speed Switching: 50 μs Typical
- 160-Ohm Maximum On-Resistance at 25°C
- Surface Mount Option
- 8-kV ESD Immunity: MIL-STD-883 Method 3015
- Input-to-Output Insulation Voltage: 2500 Vac, 1 Minute
- UL Certification Pending

Applications

- Relay Scanners & Analog Input Modules of Data Acquisition Systems
- Analog Input Modules of Programmable Logic Controllers
- Relay Multiplexers of High-Performance Voltmeters
- Telecommunication Test Instruments
- Functional Tester of Board Test Equipment
- Analog Signal Multiplexer
- Flying Capacitor Multiplexer
- Reed Relay Replacement

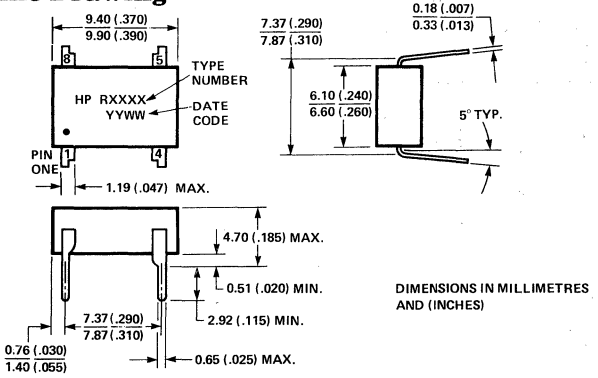
Description

The HSSR-8200 consists of a high-voltage integrated circuit optically coupled with a light emitting diode. This device is a solid-state replacement for single-pole, normally-open electromechanical relays used for general purpose switching of analog signals.

The light-emitting diode controls the ON/OFF function of the solid-state relay. The detector contains high voltage MOS transistors and a high speed photosensitive drive circuit. This relay has superior OFF impedance, very low output offset voltage and input drive current.

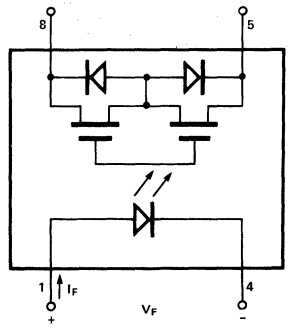
OPTOCOUPLERS

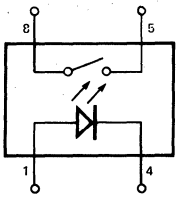
Outline Drawing



The electrical and switching characteristics of the HSSR-8200 are specified from –40°C to +85°C. The low I_F allows compatibility with TTL, LSTTL, and CMOS logic resulting in low power consumption compared to other solid state and mechanical relays.

Schematic





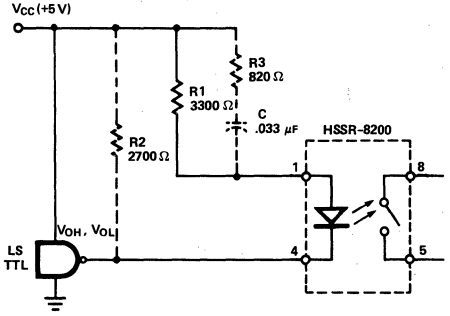
EQUIVALENT RELAY DIAGRAM

Recommended Operating Conditions

Description	Symbol	Min.	Max.	Units
Input Current (ON)	$I_{F(ON)}$	1	5	mA
Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	Volt
Operating Temperature	T_A	–40	+85	°C

Absolute Maximum Ratings

Storage Temperature ..... –55°C to 125°C
Operating Temperature ..... –40°C to +85°C
Lead Solder Temperature ..... 215°C for 30 s; Reflow Solder
260°C for 5 s; Wave Solder
Average Input Current – I_F ..... 10 mA
Repetitive Peak Input Current – I_F ..... 20 mA; 50% Duty Cycle
Transient Peak Input Current – I_F ..... 100 mA;
(≤ 1 μs pulse width; 1 kHz Pulse Repetition Rate)
Reverse Input Voltage ..... 5 V
Average Output Current – I_O ..... 40 mA[1]
Input-Output Insulation Voltage ..... 2500 VAC[6]
Output Power Dissipation ..... 320 mW[2]
Output Voltage – V_O ..... –200 V to 200 V



R1–REQUIRED CURRENT-LIMITING RESISTOR FOR $I_{F(ON)}$ = 1 mA
R2–PULL-UP RESISTOR FOR $V_{F(OFF)}$ < 800 mV; IF (V_{CC} – V_{OH}) < 800 mV, OMIT R2
R3, C– OPTIONAL PEAKING CIRCUIT FOR $I_{F(PK)}$ = 5 mA, t_{ON} < 200 μs

Figure 1. Recommended Input Circuit

Electrical Specifications

$-40°C \le T_A \le +85°C$, 1 mA $\le I_{F(ON)} \le$ 5 mA, 0 V $\le V_{F(OFF)} \le$ 0.8 V, and all Typicals at $T_A = 25°C$ unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Output Withstand Voltage	$\|V_{O(OFF)}\|$	200	245		V	$I_O = 1\ \mu A$		5
Output On-Resistance	$R_{(ON)}$	70	125	160	Ω	$T_A = 25°C$, $I_O = 1$ MA	2, 3, 4	
		40	125	250		$I_O = 1$ MA		
		30	100	200		$I_O = 40$ mA		
Output On-Current Rating	$\|I_{O(ON)}\|$			40	mA	$V_O \le 8$ V, $T_A \le 40°C$		1
Output Off-Resistance	$R_{(OFF)}$	50	10,000		GΩ	$V_O = 200$ V	5	6
Output Off-Leakage Current	$I_{O(OFF)}$		0.02	4.0	nA	$V_O = 200$ V	5	
Output Off-Capacitance	$C_{(OFF)}$			4.5	pF	$V_O = 0$ V, f = 1 MHz	6	
Output Offset Voltage	$V_{O(OS)}$	Note 3	−0.2	Note 3	μV	$I_O = 0$ A; $I_F = 1$ mA	7, 16, 17	3
			−1.3			$I_O = 0$ A; $I_F = 5$ mA		
Input Reverse Breakdown Voltage	V_R	5	45		V	$I_R = 10\ \mu A$		
Input Diode Temperature Coefficient	dV_F/dT		−1.75		mV/°C	$I_F = 1$ mA		
Input Forward Voltage	V_F	1.0	1.2	1.85	V	$I_F = 5$ mA	8	
Input Capacitance	C_{IN}		21		pF	$V_F = 0$ V; f = 1 MHz		
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH = 45%, t = 1 min; $T_A = 25°C$		4, 5
Input-Output Capacitance	C_{I-O}		0.6	1.0	pF	$V_{I-O} = 0$ V; f = 1 MHz; $T_A = 25°C$		4
Input-Output Resistance	R_{I-O}	100	100,000		GΩ	$V_{I-O} = 500$ VDC; t = 1 min; RH = 45%		4

Switching Specifications

$-40°C \le T_A \le +85°C$, $1\ mA \le I_{F(ON)} \le 5\ mA$, $0\ V \le V_{F(OFF)} \le 0.8\ V$, and all Typicals at $T_A = 25°C$ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Notes
Turn On Time	t_{ON}		50	200	µs	$I_F = 5\ mA$	$V_O = 50\ V$	9, 10, 11, 12	
			300	1500		$I_F = 1\ mA$			
Turn Off Time	t_{OFF}		45	250	µs	$I_F = 5\ mA$	$V_O = 50\ V$	9, 10, 11, 12	
			75	350		$I_F = 1\ mA$			
Output Transient Rejection	dV_O/dt		≥7000		V/µs	$\Delta V_O = 200\ V$	$T_A = 25°C$	13	
		2000				$\Delta V_O = 50\ V$			
Input-Output Transient Rejection	dV_{I-O}/dt		≥7000		V/µs	$\Delta V_{I-O} = 300\ V$	$T_A = 25°C$	14	
		2000				$\Delta V_{I-O} = 50\ V$			

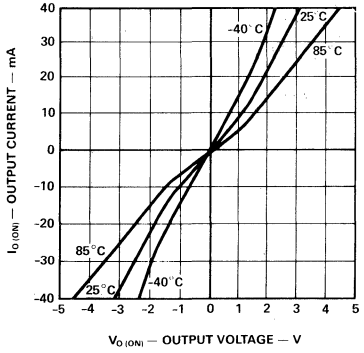


Figure 2. Typical On State I-V Characteristics.

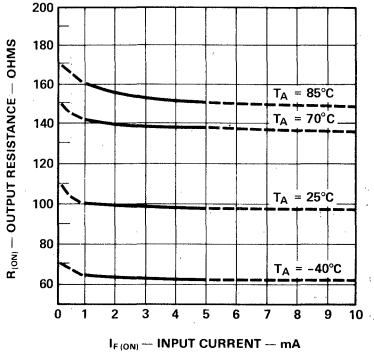


Figure 3. Typical Output Resistance vs. Input Current.

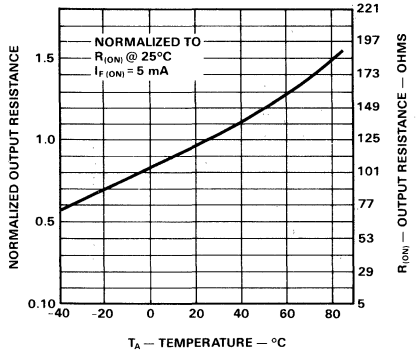


Figure 4. Typical Output Resistance vs. Temperature.

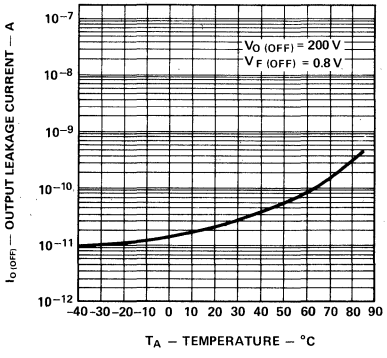


Figure 5. Typical Output Leakage vs. Temperature.

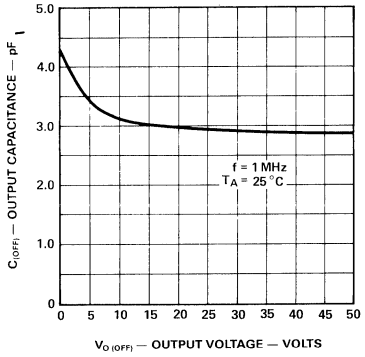


Figure 6. Typical Output Capacitance vs. Output Voltage.

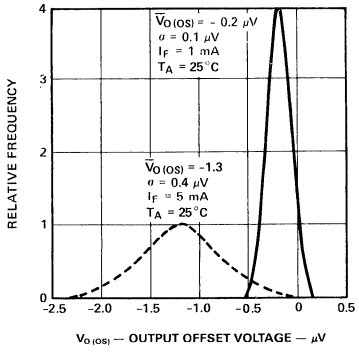


Figure 7. Output Offset Voltage Distribution.

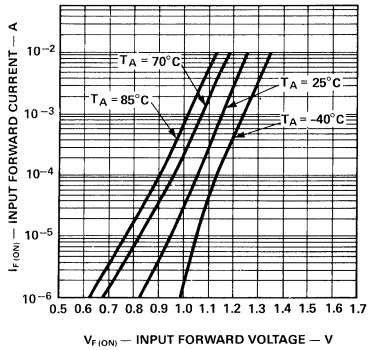


Figure 8. Typical Input Forward Current vs. Forward Voltage.

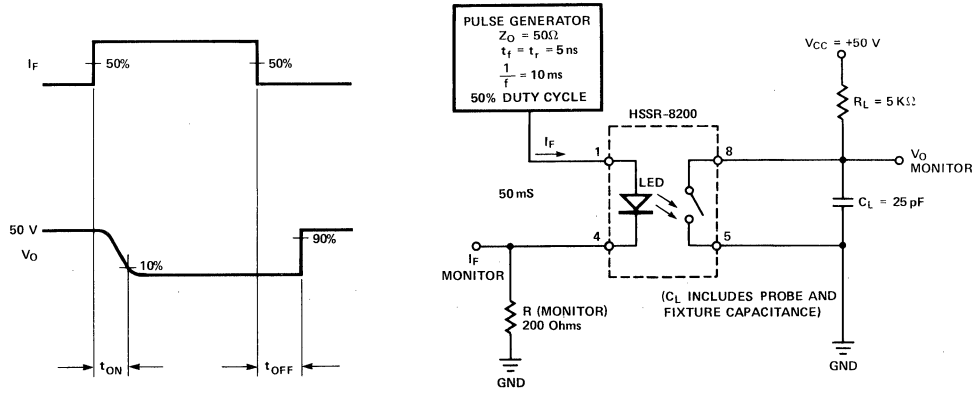


Figure 9. Switching Test Circuit for t_{ON}, t_{OFF}.

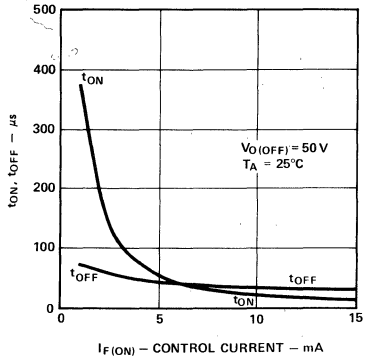


Figure 10. Typical t_{ON} and t_{OFF} vs. Input Current.

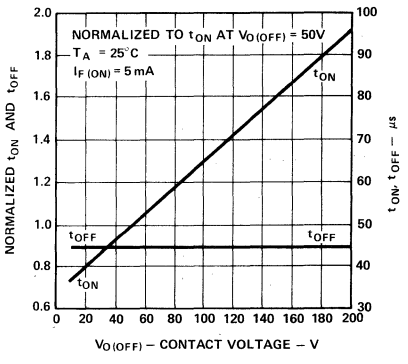


Figure 11. t_{ON} and t_{OFF} vs. Output Voltage.

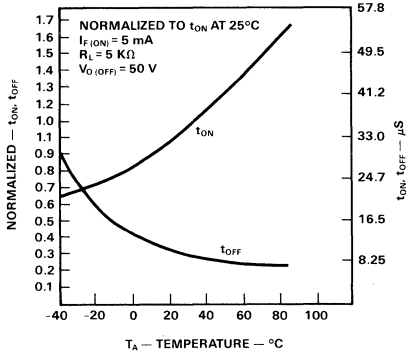


Figure 12. Normalized t_{ON} and t_{OFF} vs. Temperature.

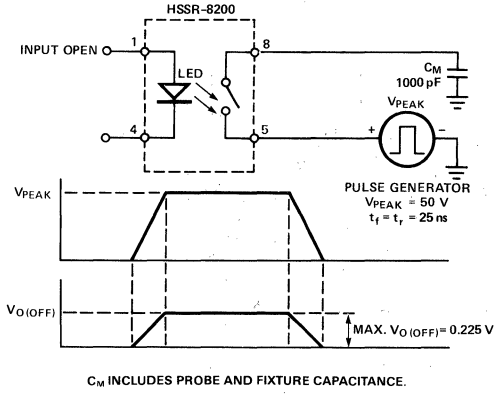
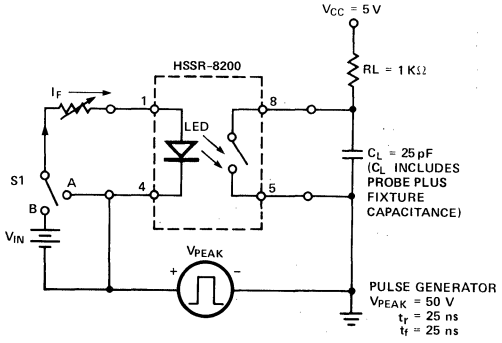


Figure 13. Output Transient Rejection Test Circuit.



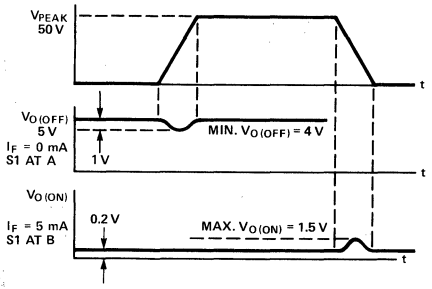


Figure 14. Input-Output Transient Rejection.

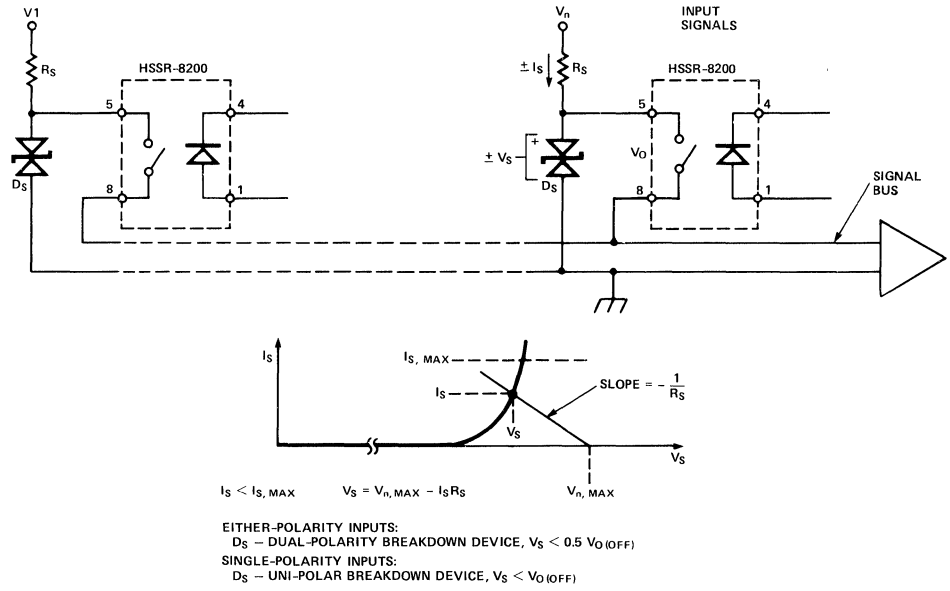


Figure 15. Over-Voltage Protection in Multiplexer Applications.

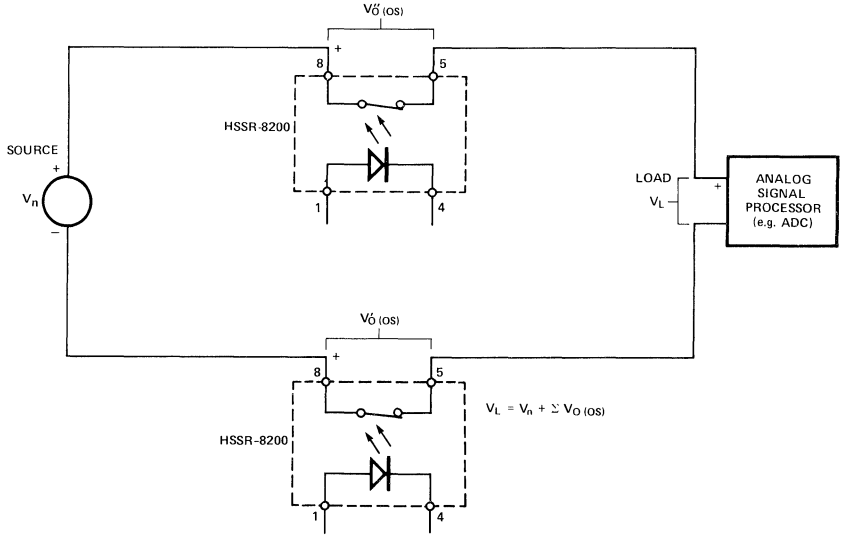


Figure 16. Differential Output Connections to Minimize Offset Voltage Effects.

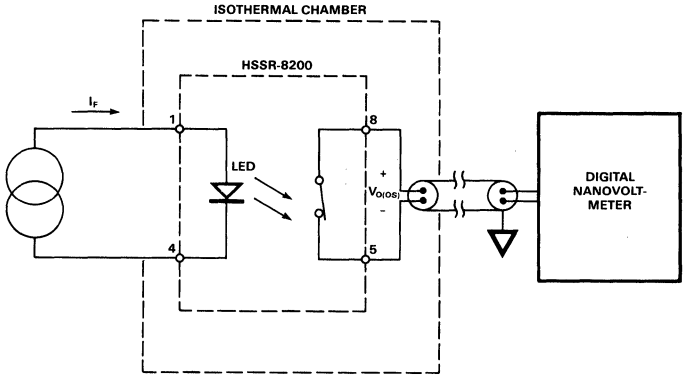


Figure 17. Voltage Offset Test Setup.

Notes:

1. Derate linearly above 40°C at a rate of 0.3 mA/°C.
2. Derate linearly above 60°C at a rate of 5 mW/°C.
3. $V_{O(OS)}$ is a function of $I_{F(ON)}$, and is defined between pins 8 and 5 with pin 5 as reference. $V_{O(OS)}$ must be measured in a stable ambient. See Figure 7 for variation of $V_{O(OS)}$ around the typical value.
4. Device considered a two terminal device: pins 1 and 4 shorted together, and pins 5 and 8 shorted together.
5. For higher withstand voltage rating and regulatory certification, please contact your HP Field Sales Engineer.
6. $R_{(OFF)}$ is defined as $V_{O(OFF)}/I_{O(OFF)}$.

Hermetic Optocouplers

Hermetic Optocouplers

Choose from Hewlett-Packard's broad line of high performance hermetic optocouplers to meet your military, aerospace, and high reliability applications. There are three ceramic package styles to choose from: 8 and 16 pin dual in-line packages, and a 20 terminal leadless chip carrier (LCC) package. Available in each package style are four basic families of optocouplers: high gain, high speed transistor, high speed logic gate, and several application specific devices. Most 8 pin units allow a choice of either single or dual channels. Three functional device types are offered in dual channel configuration in the 16 pin package. Also in the 16 pin package are two functional types in four channel configuration. The LCC catalog products are all two channel optocouplers.

HP's hermetic optocouplers are classified by the Department of Defense as hybrid microcircuits and are manufactured and tested on a MIL-STD-1772 certified and qualified line. Our facilities and assembly processes meet MIL-H-38534 class B, and we have listing on QML-38534.

All product families are represented by standard (commercial grade) units and by high reliability tested units. The hi-rel parts are tested to MIL-STD-883 class B. Most hi-rel tested parts are also offered with recognized DESC part numbers either from DESC Drawings, Standard Military Drawings (SMDs), or from DESC's new, "One Part, One Part Numbering System". All hi-rel parts are tested and guaranteed over the full military temperature range from –55°C to +125°C.

New this year is the expanded list and wide variety of optocouplers in three package styles. Our complete line of products offered in 20 terminal LCC were released in 1989. Released in 1990 are the transistor output devices and the expanded line of logic gate units in 8 pin DIP. And, to give you more opportunities to use recognized DESC parts, we now offer 13 devices under DESC drawings with more to come.

Hermetic Optocoupler Product Screening and Quality Conformance Test Program (MIL-STD-883 Class B)

The following 100% Screening and Quality Conformance Inspection programs show in detail the capabilities of our hermetic optocouplers. MIL-H-38534 Quality assurance requirements are in accordance with Option 2 for all testing programs (Methods 5008 and 2017). Hewlett-Packard further exercises a testing option as allowed by MIL-STD-883, Method 5008, Par. 3.1a which states that "hybrid and multi-chip microcircuits, which are contained in packages having an inner seal perimeter of less than 2.0 inches", may be tested in accordance with the requirements of MIL-STD-883, Methods 5004 and 5005, with a change to the internal visual from Method 2010 to Method 2017. All devices marked /883B and DESC Drawing parts have standardized test programs suitable for product used in military, aerospace, and other high reliability applications and are the preferred devices by systems contractors.

100% Screening MIL-STD-883, Method 5004 (Class B Devices)

Test	Method	Conditions
1. Precap Internal Visual	2017 & 2032	
2. Temperature Cycling	1010	Condition C, –65°C to +150°C, 10 cycles
3. Constant Acceleration	2001	Condition A, 5KG's
4. Fine Leak	1014	Condition A
5. Gross Leak	1014	Condition C
6. Interim Electrical Test	–	Optional
7. Burn-In	1015	Condition B, Time = 160 hours, min. T_A = 125°C
8. Final Electrical Test Electrical Test		Group A Subgroup 1, 5% PDA Group A, Subgroups 2, 3, 9
9. External Visual	2009	

Quality Conformance Inspection

Group A electrical tests are product dependent and are given in the individual device data sheets. Group A and B testing is performed on each inspection lot.

Group A Testing, MIL-STD-883, Method 5005 (Class B Devices) Quantity/Accept Number = 116/0

Subgroup 1 Static tests at T_A = 25°C
Subgroup 2 Static tests at T_A = + 125°C
Subgroup 3 Static tests at T_A = –55°C
Subgroup 4 Dynamic test at T_A = 25°C (where applicable)
Subgroups 5, 6, 7, and 8a & 8b These subgroups are non-applicable to this device type
Subgroup 9 Switching tests at T_A = 25°C
Subgroup 10 Switching tests at T_A = +125°C
Subgroup 11 Switching Tests at T_A = –55°C

Group B Testing, MIL-STD-883, Method 5005 (Class B Devices)

Test	Method	Conditions	Quantity/ Accept No.
Subgroup 2 Resistance to Solvents	2015		4 Devices (no failures)
Subgroup 3 Solderability	2003	Soldering temperature of 245 ± 5°C for 10 seconds	22/0 leads 3 devices minimum
Subgroup 5 Bond Strength Thermocompression (performed prior to seal)	2011	Test Condition D	15/0 wires

Group C testing is performed on a periodic basis from current manufacturing every three months.

Group C Testing, MIL-STD-883, Method 5005 (Class B Devices)

Test	Method	Conditions	Quantity/ Accept No.
Subgroup 1 Steady State Life Test	1005	Cond. B, time = 1000 hours total T_A = +125°C	45/0
Endpoint Electricals at 1000 hours		Group A, Subgroup 1,2,3	

Group D testing is performed on a periodic basis from current manufacturing every six months.

Group D Testing, MIL-STD-883, Method 5005 (Class B Devices)

Test	Method	Conditions	Quantity/ Accept No.
Subgroup 1 Physical Dimensions	2016		15/0
Subgroup 2 Lead Integrity	2004	Test Cond. B2 (Test Cond. D for LCCs)	15/0
Subgroup 3 Thermal Shock	1011	Cond. B, –55°C to +125°C 15 cycles min.	15/0
Temperature Cycling	1010	Cond. C, –65°C to +150°C 100 cycles min.	
Moisture Resistance	1004		
Fine Leak	1014	Cond. A	
Gross Leak	1014	Cond. C	
Visual Examination		Per visual criteria of methods 1004, 1010	
Endpoint Electricals		Group A, Subgroup 1,2,3	

Group D Testing, MIL-STD-883, Method 5005 (Class B Devices), Continued

Test	Method	Conditions	Quantity/ Accept No.
Subgroup 4			15/0
Mechanical Shock	2002	Cond. B, 1500G, t = 0.5 ms, 5 blows in each orientation	
Vibration Variable Frequency	2007	Cond. A	
Constant Acceleration	2001	Cond. A, 5 KGs	
Fine Leak	1014	Cond. A	
Gross Leak	1014	Cond. C	
Visual Examination	1010	Per visual criteria of Method 1010	
Endpoint Electricals		Group A, Subgroup 1,2,3	
Subgroup 5			15/0
Salt Atmosphere	1009	Cond. A min.	
Fine Leak	1014	Cond. A	
Gross Leak	1014	Cond. C	
Visual Examination	1009	Per visual criteria of Method 1009	
Subgroup 6			3/0 or 5/1
Internal Water Vapor Content	1018	5,000 ppm maximum water content at 100°C	
Subgroup 7			15/0 leads
Adhesion of Lead Finish (not required for LCCs)	2025		3 devices minimum

Controlling Government Specifications and Standards

MIL-H-38534 General Specification for Hybrid Microcircuits

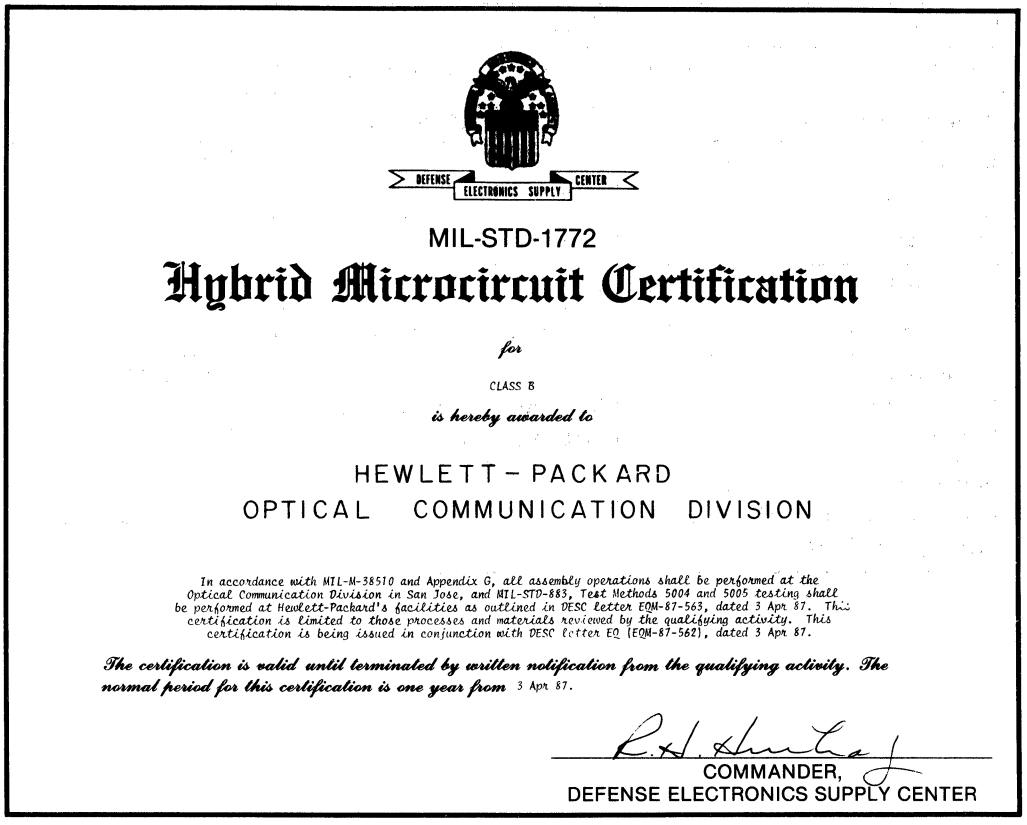
All Hewlett-Packard /883B, DESC Drawing and SMD products are in full compliance with the applicable parts of MIL-H-38534.

MIL-STD-883 Test Methods and Procedures for Microelectronics

Hewlett-Packard's testing of all hermetic hybrid products is in compliance with current revisions, requirements and test methods of MIL-STD-883 class B.

MIL-STD-1772 Certification Requirements for Hybrid Microcircuit Facilities and Lines

Our hermetic optocoupler line is certified and parts are qualified to MIL-STD-1772. Certification to MIL-STD-1772 must exist before a part can be marked with 883B or with a DESC SMD number.



DEFENSE ELECTRONICS SUPPLY CENTER

MIL-STD-1772

Hybrid Microcircuit Certification

for

CLASS B

is hereby awarded to

HEWLETT - PACKARD

OPTICAL COMMUNICATION DIVISION

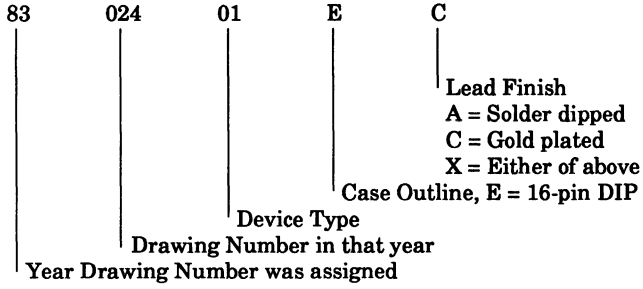
In accordance with MIL-M-38510 and Appendix G, all assembly operations shall be performed at the Optical Communication Division in San Jose, and MIL-STD-883, Test Methods 5004 and 5005 testing shall be performed at Hewlett-Packard's facilities as outlined in DESC letter EQM-87-563, dated 3 Apr 87. This certification is limited to those processes and materials reviewed by the qualifying activity. This certification is being issued in conjunction with DESC letter EQ (EQM-87-562), dated 3 Apr 87.

The certification is valid until terminated by written notification from the qualifying activity. The normal period for this certification is one year from 3 Apr 87.

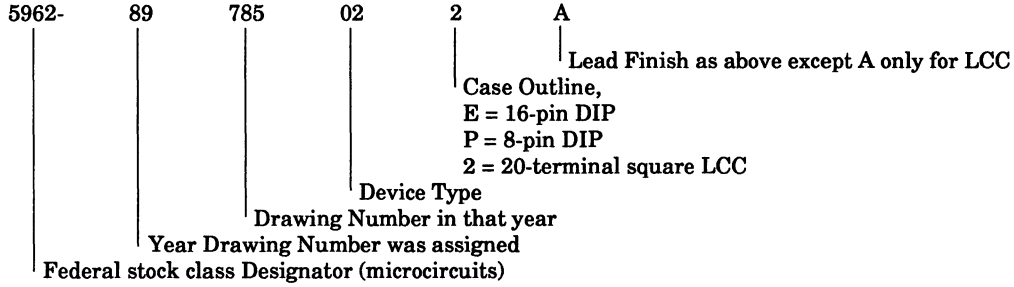
COMMANDER,
DEFENSE ELECTRONICS SUPPLY CENTER

DESC Part Number Systems[1]

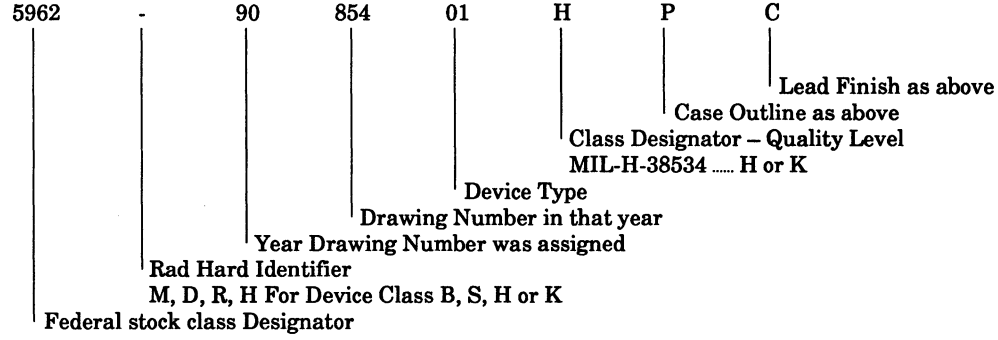
DESC Drawings[2]



Standard Military Drawings (SMD)

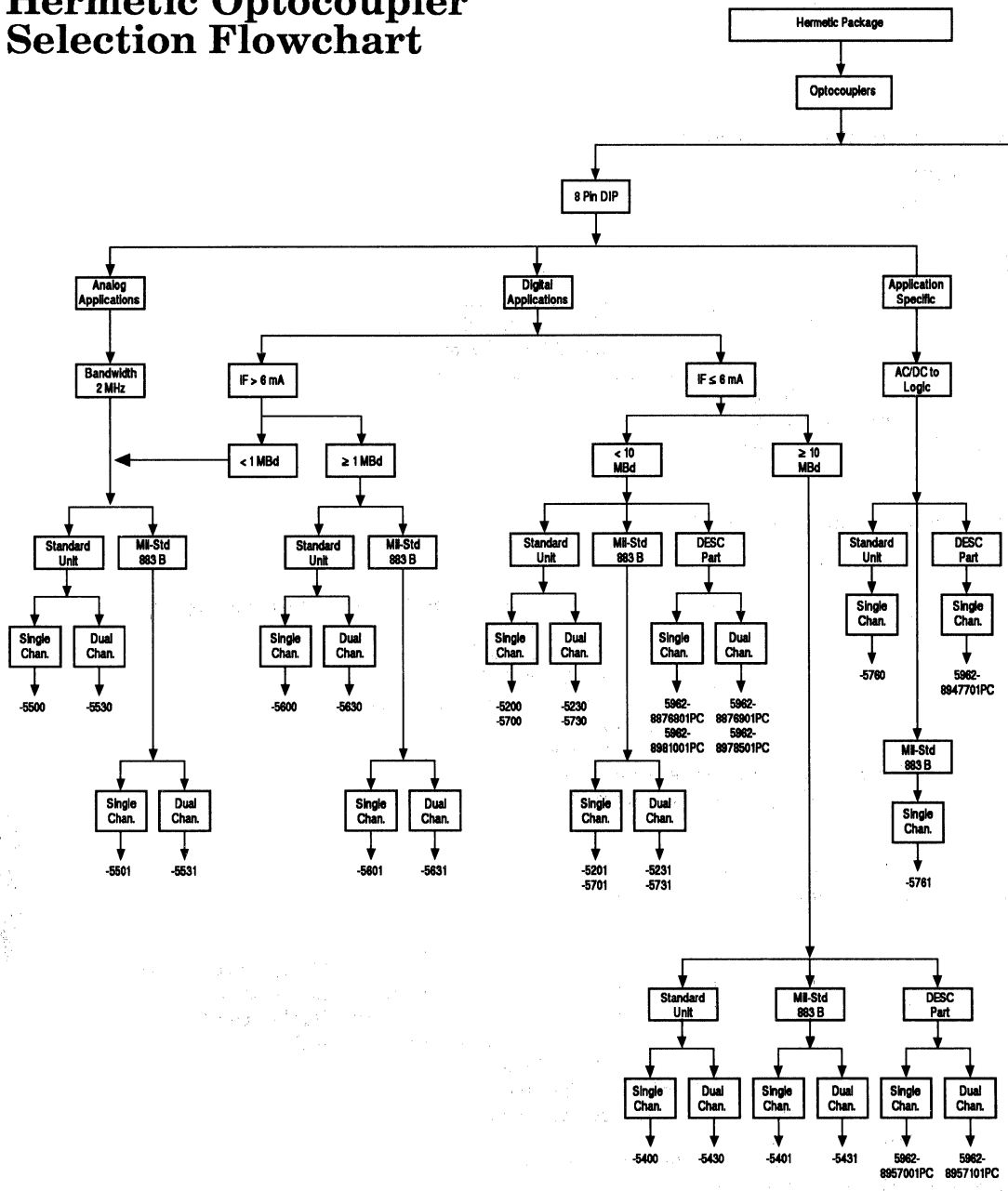


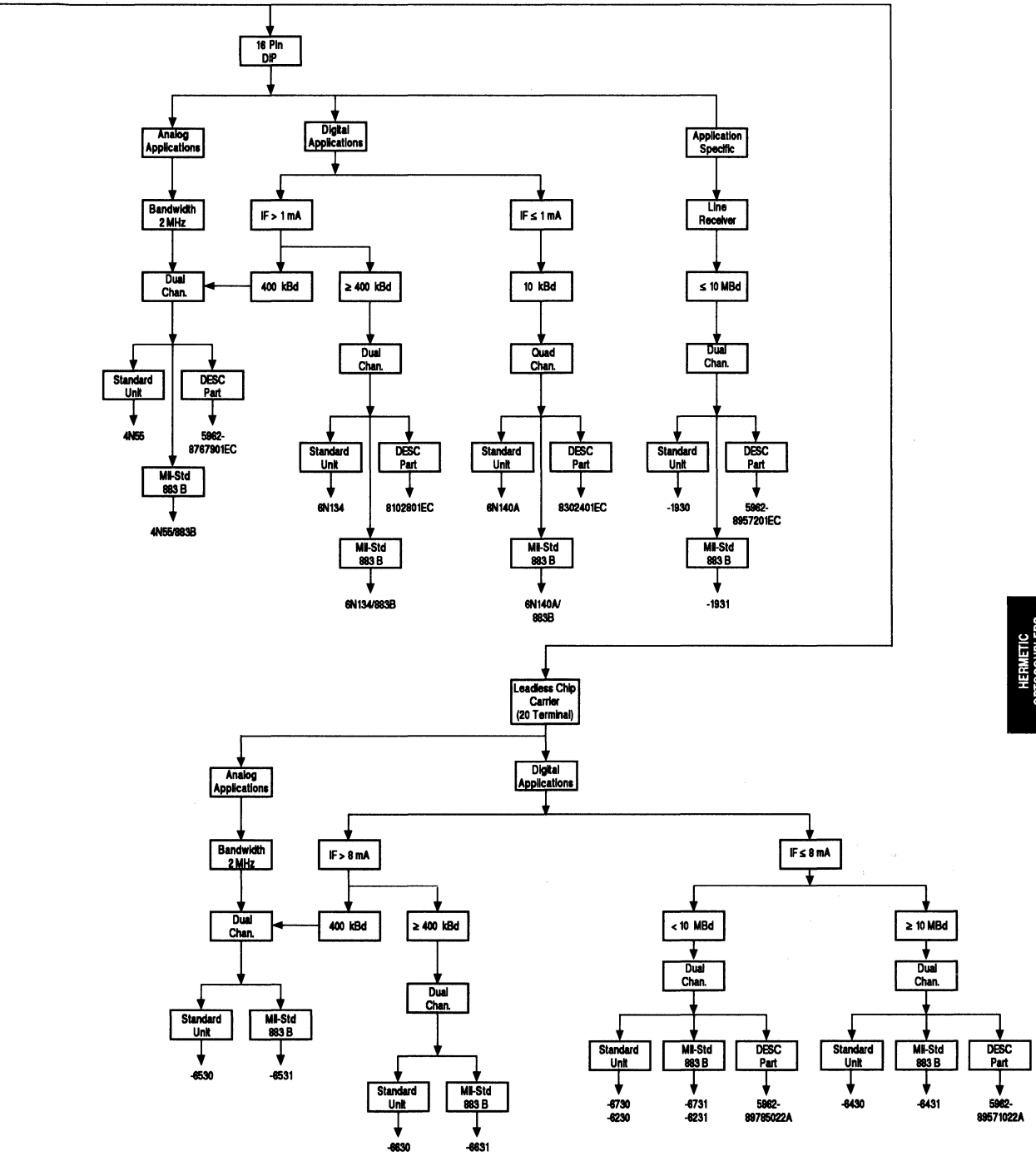
One Part - One Part Number System[3]



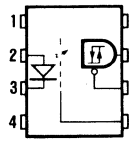
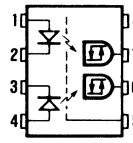
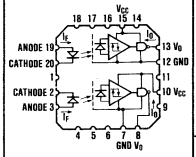
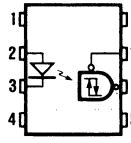
Notes:
1. The numbering system used was current when any particular part was numbered.
2. DESC Drawings do not contain the prefix 5962.
3. Class Designators H, and K of MIL-H-38534 are equivalent to class levels B and S of MIL-M-38510 respectively.

Hermetic Optocoupler Selection Flowchart



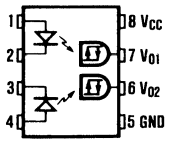
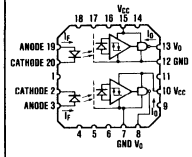
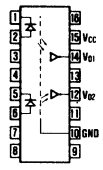
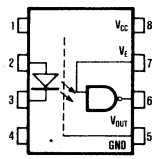

16 Pin DIP
Analog Applications
Digital Applications
Application Specific
Bandwidth 2 MHz
IF > 1 mA
IF ≤ 1 mA
Line Receiver
Dual Chan.
400 kBd
≥ 400 kBd
10 kBd
≤ 10 MBd
Dual Chan.
Quad Chan.
Dual Chan.
Standard Unit
DESC Part
4N55
5962-8767901EC
Mil-Std 883 B
4N55/883B
Standard Unit
DESC Part
6N134
8102801EC
Mil-Std 883 B
6N134/883B
Standard Unit
DESC Part
6N140A
8302401EC
Mil-Std 883 B
6N140A/883B
Standard Unit
DESC Part
-1930
5962-8957201EC
Mil-Std 883 B
-1931
Leadless Chip Carrier (20 Terminal)
Analog Applications
Digital Applications
Bandwidth 2 MHz
IF > 8 mA
IF ≤ 8 mA
Dual Chan.
400 kBd
≥ 400 kBd
< 10 MBd
≥ 10 MBd
Dual Chan.
Dual Chan.
Dual Chan.
Standard Unit
Mil-Std 883 B
-6530
-6531
Standard Unit
Mil-Std 883 B
-6630
-6631
Standard Unit
Mil-Std 883 B
DESC Part
-6730
-6230
-6731
-6231
5962-89785022A
Standard Unit
Mil-Std 883 B
DESC Part
-6430
-6431
5962-89571022A

High-Speed Logic Gate Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Common Mode	Specified Input Current	Withstand Test Voltage*	Page No.
 8 pin DIP	HCPL-5200	Single Channel, Hermetically Sealed Wide Supply Voltage Optocoupler	High Speed Logic Ground Isolation, LSTTL, TTL, CMOS Logic Interface	5 M bit/s	1000 V/µs at Vcm = 50 V	2-8 mA	1500 Vdc	6-222
	HCPL-5201	MIL-STD-883 Class B	Military/High Reliability					
	5962-8876801PC	DESC Approved HCPL-5201						
 8 pin DIP	HCPL-5230	Dual Channel, Hermetically Sealed Wide Supply Voltage Optocoupler	High Speed Logic Ground Isolation, LSTTL, TTL, CMOS Logic Interface					
	HCPL-5231	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-8876901PC	DESC Approved HCPL-5231						
 20 Terminal LCC	**HCPL-6230**	Dual Channel, Hermetically Sealed Wide Supply Voltage Optocoupler	High Speed Logic Ground Isolation, LSTTL, TTL, CMOS Logic Interface					
	HCPL-6231	MIL-STD-883 Class B Part	Military/High Reliability					
	TBD	DESC Approved HCPL-6231						
 8 pin DIP	HCPL-5400	Single Channel, Hermetically Sealed High Speed Optocoupler	High Speed Logic Isolation, A/D and Parallel/Serial Conversion	40 M bit/s	500 V/µs at Vcm = 50 V	6-10 mA	1500 Vdc	6-236
	HCPL-5401	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-8957001PC	DESC Approved HCPL-5401						

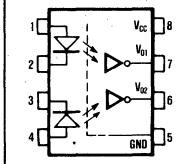
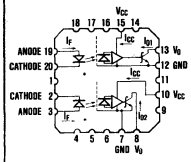
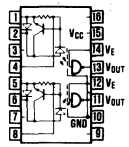
Bold Type – New Product

High-Speed Logic Gate Optocouplers (Continued)

Device		Description	Application	Typical Data Rate [NRZ]	Common Mode	Specified Input Current	Withstand Test Voltage*	Page No.
 8 pin DIP	HCPL-5430	Dual Channel, Hermetically Sealed High Speed Optocoupler	High Speed Logic Isolation, Communications, Networks, Computers	40 Mbit/s	500 V/µs at Vcm = 50 V	6-10 mA	1500 Vdc	6-236
	HCPL-5431	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-8957101PC	DESC Approved HCPL-5431						
 20 Terminal LCC	**HCPL-6430**	Dual Channel, Hermetically Sealed High Speed Optocoupler	High Speed Logic Isolation, Communications, Networks, Computers					
	HCPL-6431	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-89571022A	DESC Approved HCPL-6431						
 16 pin DIP	6N134	Dual Channel, Hermetically Sealed Optically Coupled Logic Gate	Line Receiver, Ground Isolation for High Reliability Systems	10 M bit/s	1000 V/µs at Vcm = 50 V	10 mA	1500 Vdc	6-251
	6N134/883B	MIL-STD-883 Class B Part	Military/High Reliability					
	8102801EC	DESC Approved 6N134/883B						
 8 pin DIP	**HCPL-5600**	Single Channel, Hermetically Sealed Optically Coupled Logic Gate	Line Receiver, Ground Isolation for High Reliability Systems					6-257
	HCPL-5601	MIL-STD-883 Class B Part	Military/High Reliability					
	TBD	DESC Approved HCPL-5601						

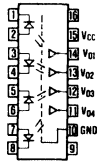
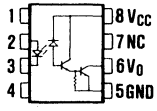
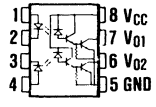
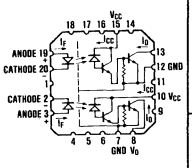
Bold Type – New Product

High-Speed Logic Gate Optocouplers (Continued)

Device		Description	Application	Typical Data Rate [NRZ]	Common Mode	Specified Input Current	Withstand Test Voltage*	Page No.
 8 pin DIP	**HCPL-5630**	Dual Channel, Hermetically Sealed Optically Coupled Logic Gate	Line Receiver, Ground Isolation for High Reliability Systems	10 M bit/s	1000 V/μs at Vcm = 50 V	10 mA	1500 Vdc	6-257
	HCPL-5631	MIL-STD-883 Class B Part	Military/High Reliability					
	TBD	DESC Approved HCPL-5631						
 20 Terminal LCC	**HCPL-6630**	Dual Channel, Hermetically Sealed Optically Coupled Logic Gate	Line Receiver, Ground Isolation for High Reliability Systems					
	HCPL-6631	MIL-STD-883 Class B Part	Military/High Reliability					
	TBD	DESC Approved HCPL-6631						
 16 pin DIP	HCPL-1930	Dual Channel, Hermetically Sealed High CMR Line Receiver Optocoupler	Line Receiver, High Speed Logic Ground Isolation in High Ground or Induced Noise Environments	10M bit/s	1000 V/μs at Vcm = 50 V	10 mA	1500 Vdc	6-265
	HCPL-1931	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-8957201EC	DESC Approved HCPL-1931						

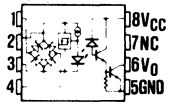
Bold Type – New Product

High Gain Optocouplers

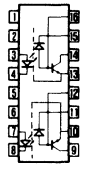
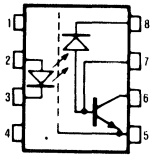
Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
 16 pin DIP	6N140A	Hermetically Sealed Package Containing 4 Low Input Current High Gain Optocouplers	Line Receiver, Low Power Ground Isolation for High Reliability Systems	100k bit/s	300% Min.	0.5 mA to 5.0 mA	1500 Vdc	6-273
	6N140A/883B	MIL-STD-883 Class B Part	Military/High Reliability					
	8302401EC	DESC Approved 6N140A/883B						
 8 pin DIP	HCPL-5700	Single Channel, Hermetically Sealed High Gain Optocoupler	Line Receiver, Low Current Ground Isolation. TTL/TTL, LSTTL/TTL, CMOS/TTL					6-280
	HCPL-5701	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-8981001PC	DESC Approved HCPL-5701						
 8 pin DIP	HCPL-5730	Dual Channel, Hermetically Sealed, High Gain Optocoupler	Line Receiver, Polarity Sensing, Low Current Ground Isolation					
	HCPL-5731	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-8978501PC	DESC Approved HCPL-5731						
 20 Terminal LCC	**HCPL-6730**	Dual Channel, Hermetically Sealed High Gain Optocoupler	Line Receiver, Polarity Sensing, Low Current Ground Isolation					
	HCPL-6731	MIL-STD-883 Class B Part	Military/High Reliability					
	5962-89785022A	DESC Approved HCPL-6731						

Bold Type - New Product

AC/DC to Logic Interface Optocoupler

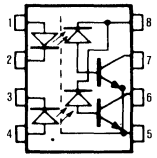
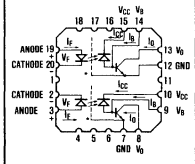
Device		Description	Application	Typical Data Rate	Input Threshold Current	Output Current	Withstand Test Voltage	Page No.
	HCPL-5760	Single Channel Hermetically Sealed Threshold Sensing Optocoupler	Limit Switch Sensing, Low Voltage Detector Relay Contact Monitor	10 kHz	2.5 mA TH+ 1.3 mA TH–	2.6 mA	1500 Vdc	6-290
	HCPL-5761	MIL-STD-883 Class B Part	Military/High Reliability					
8 pin DIP	5962-8947701PC	DESC Approved HCPL-5761						

High Speed Transistor Optocouplers

Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
	4N55	Dual Channel Hermetically Sealed Analog Optical Coupler	Line Receiver, Analog Signal Ground Isolation, Switching Power Supply Feedback Element	700k bit/s	9% Min.	16 mA	1500 Vdc	6-298
	4N55/883B	MIL-STD-883 Class B Part	Military/High Reliability					
16 pin DIP	5962-8767901EC	DESC Approved 4N55/883B						
	HCPL-5500	Single Channel Hermetically Sealed Analog Optical Coupler	Line Receiver, Analog Signal Ground Isolation, Switching Power Supply Feedback Element					6-305
	HCPL-5501	MIL-STD-883 Class B Part	Military/High Reliability					
8 pin DIP	TBD	DESC Approved HCPL-5501						

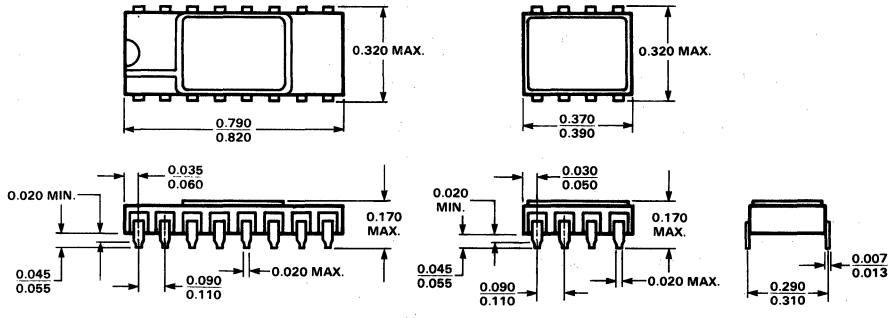
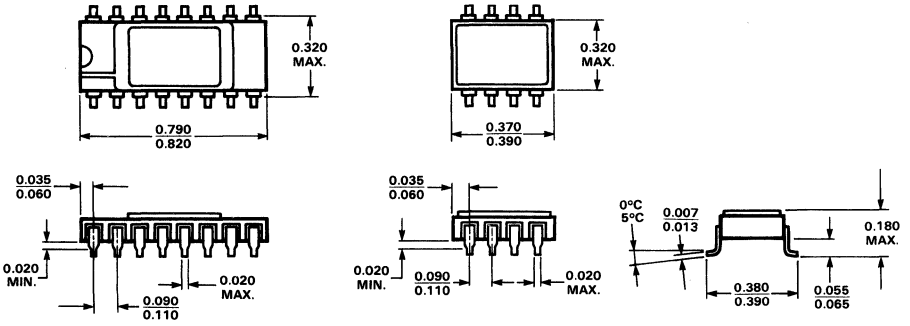
Bold Type – New Product

High Speed Transistor Optocouplers (Continued)

Device		Description	Application	Typical Data Rate [NRZ]	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
 8 pin DIP	**HCPL-5530**	Dual Channel, Hermetically Sealed Analog Optical Coupler	Line Receiver, Analog Signal Ground Isolation, Switching Power Supply Feedback Element	700k bit/s	9% Min.	16 mA	1500 Vdc	6-305
	HCPL-5531	MIL-STD-883 Class B Part	Military/High Reliability					
	TBD	DESC Approved HCPL-5531						
 20 Terminal LCC	**HCPL-6530**	Dual Channel, Hermetically Sealed Analog Optical Coupler	Line Receiver, Analog Signal Ground Isolation, Switching Power Supply Feedback Element					
	HCPL-6531	MIL-STD-883 Class B Part	Military/High Reliability					
	TBD	DESC Approved HCPL-6531						

Bold Type – New Product

Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on standard product and /883B hi-rel product in 8 and 16 pin DIP (see drawings below for details). Contact factory for the availability of this option on DESC part types. 
200	Lead finish is solder dipped rather than gold plated. This option is available on standard product and /883B product in 8 and 16 pin DIP. DESC Drawing part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder dipped terminals as a standard feature.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on standard product and /883B product in 8 and 16 pin DIP (see drawings below for details). Contact factory for the availability of this option on DESC part types. This option has solder dipped leads. 

Hermetic High Performance Optocouplers
Functionally Equivalent Part Types

Package Style	16 PIN DIP		8 PIN DIP		20 Terminal LCC	Closest Equivalent Plastic
# of Channels / Function	Quad (4)	Dual (2)	Dual (2)	Single (1)	Dual (2)	Single (1)
High Gain Output, Low Input Current	6N140A **6N140A/883B** *8302401EC*		HCPL-5730 **HCPL-5731** *5962-8978501PC*	HCPL-5700 **HCPL-5701** *5962-8981001PC*	HCPL-6730 **HCPL-6731** *5962-89785022A*	6N138 6N139
Transistor Output		4N55 **4N55/883B** *5962-8767901EC*	HCPL-5530 **HCPL-5531**	HCPL-5500 **HCPL-5501**	HCPL-6530 **HCPL-6531**	6N135 6N136
High Speed Logic Output, 10 Mbaud	Special P/N	6N134 **6N134/883B** *8102801EC*	HCPL-5630 **HCPL-5631**	HCPL-5600 **HCPL-5601**	HCPL-6630 **HCPL-6631**	HCPL-2601 6N137
High Speed Logic, Input Regulation		HCPL-1930 **HCPL-1931** *5962-8957201EC*	Special P/N	Special P/N	Special P/N	HCPL-2602
Wide Vcc from 4.5 to 20 Volts			HCPL-5230 **HCPL-5231** *5962-8876901PC*	HCPL-5200 **HCPL-5201** *5962-8876801PC*	HCPL-6230 **HCPL-6231**	HCPL-2200
Very High Speed Logic, 20 Mbaud			HCPL-5430 **HCPL-5431** *5962-8957101PC*	HCPL-5400 **HCPL-5401** *5962-8957001PC*	HCPL-6430 **HCPL-6431** *5962-89571022A*	HCPL-2400
AC/DC Logic Interface				HCPL-5760 **HCPL-5761** *5962-8947701PC*	Special P/N Single	HCPL-3700

Standard type refers to standard parts
Bold type refers to 883B parts
Italic type refers to DESC Drawing parts

3/90
HIGHOC5

HEWLETT PACKARD

Wide Supply Voltage, High CMR, Hermetically Sealed Optocoupler

Technical Data

8 Pin Dual In-Line Package
- **HCPL-5200**
- **HCPL-5201 (883B)**
- **5962 8876801PC**
- **HCPL-5230**
- **HCPL-5231 (883B)**
- **5962 8876901PC**

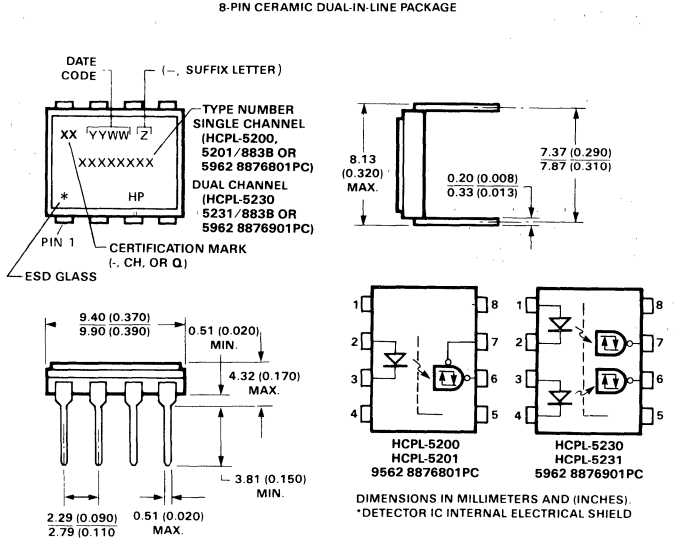
20 Terminal Leadless Chip Carrier
- **HCPL-6230**
- **HCPL-6231 (883B)**

Features
- DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534
- Hermetically Sealed Packages
- Performance Guaranteed over -55°C to +125°C Ambient Temperature Range
- MIL-STD-883 Class B Testing
- Wide V_{CC} Range (4.5 to 20 V)
- 300 ns Maximum Propagation Delay
- Compatible with LSTTL, TTL, and CMOS Logic
- High Common Mode Rejection – 1000 V/μs Guaranteed
- 1500 Vdc Withstand Test Voltage
- Three State Output Available
- HCPL-2200 Function Compatibility

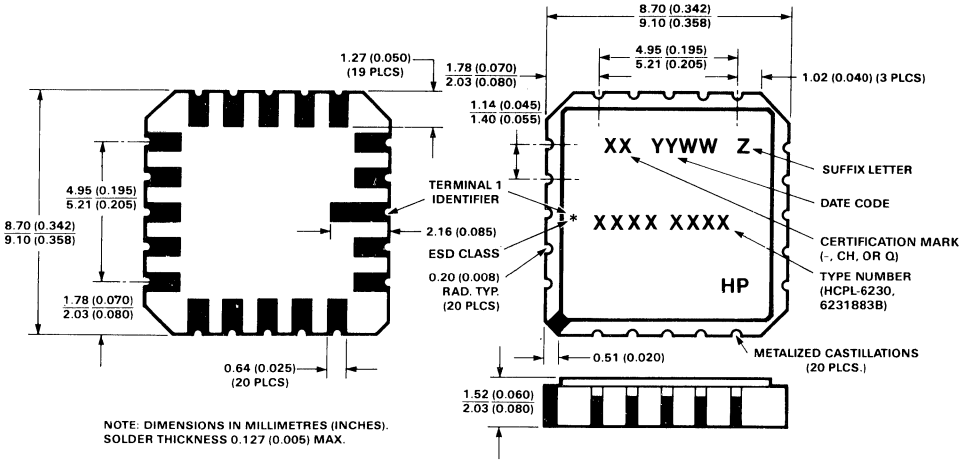
Applications
- Military/High Reliability Systems
- Isolation of High Speed Logic Systems
- Computer-Peripheral Interfaces
- Microprocessor System Interfaces
- Ground Loop Elimination
- Pulse Transformer Replacement
- Isolated Bus Driver (Single Channel)
- High Speed Line Receiver

Outline Drawings

8 PIN CERAMIC DUAL IN-LINE PACKAGE



20 TERMINAL CERAMIC LEADLESS CHIP CARRIER



Description

The HCPL-5200, HCPL-5201, and 5962 8876801PC are single channel, logic gate optocouplers. The HCPL-5230, HCPL-5231 and 5962 8876901PC are dual channel units made from the same chip sets. All six products are in eight pin hermetic dual in-line packages. These units are capable of operation and storage over the full military temperature ranges and can be purchased as either single or dual channel standard product (HCPL-5200 and HCPL-5230 respectively), with full MIL-STD-883 Class Level B testing (HCPL-5201 and HCPL-5231 respectively), or from the DESC Standard Military Drawings (SMDs) 5962-88768 and 5962-88769 as (5962 8876801PC or 5962 8876901PC respectively). All parts are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the SMD part #, or by adding option #200 to the part number for non-SMD parts.

The HCPL-6230 and HCPL-6231 parts are in twenty terminal hermetic, ceramic, leadless chip carriers. The standard part is HCPL-6230. The product with full MIL-STD-883 Class Level B testing is HCPL-6231. These dual channel devices are configured and function as two independent single channels. Devices are delivered with solder dipped terminals as a standard feature. Units may also be purchased with gold-plated terminals.

Each channel contains an AlGaAs light emitting diode optically coupled to an integrated high gain photon detector. The detector has a threshold with hysteresis. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter. The detector in the single channel units has a three state output stage which allows for direct connection to data buses. The detector IC has an electric shield that provides a guaranteed common mode transient immunity of 1,000 Volts/μsec. Improved power supply rejection eliminates the need for special power supply bypass precautions.

All devices are guaranteed to operate over a V_{CC} range of 4.5 Volts to 20 Volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS. Logic low I_F and low I_{CC} result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a typical propagation delay of 100 nsec when used in the circuit of Figure 11.

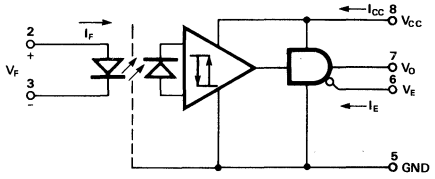
These units are useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

The test programs on the 5962 8876801PC and 5962 8876901PC are in compliance with DESC (SMDs) 5962-88768 and 5962-88769 respectively. The electrical characteristics table shows Group A Subgroup testing requirements from these drawings.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

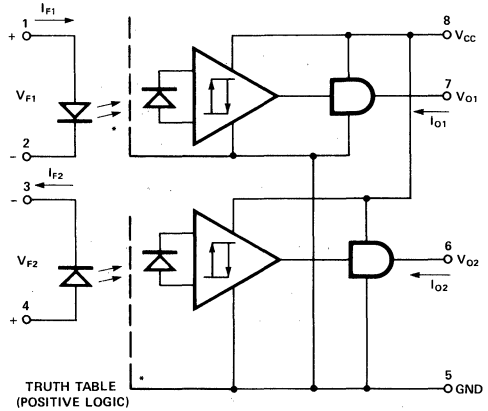
Schematics

8 PIN CERAMIC DIP SINGLE CHANNEL SCHEMATIC



DETECTOR IC INTERNAL ELECTRICAL SHIELD

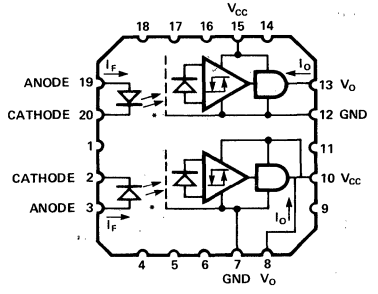
8 PIN CERAMIC DIP DUAL CHANNEL SCHEMATIC



TRUTH TABLE
(POSITIVE LOGIC)

INPUT	OUTPUT
H	H
L	L

20 TERMINAL CERAMIC LEADLESS CHIP CARRIER SCHEMATIC



TRUTH TABLE
(POSITIVE LOGIC)

INPUT	OUTPUT
H	H
L	L

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Input Current (High)	$I_{F(ON)}$	2	8	mA
Input Voltage (Low)	$V_{F(OFF)}$	0	0.8	Volts
Fan Out	N		4	TTL Loads

Single Channel Product Only

Enable Voltage High	V_{EH}	2.0	20	Volts
Enable Voltage Low	V_{EL}	0	0.8	Volts

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Case Temperature – T_C ..... +170°C
Lead Solder Temperature ..... 260°C for 10 s
Junction Temperature (T_J) ..... +175°C
Average Forward Current – $I_{F\,AVG}$ ..... 8 mA
Peak Input Current – $I_{F\,PK}$ ..... 20 mA[1]
Reverse Input Voltage – V_R ..... 5 V
Supply Voltage – V_{CC} ..... -0.0 V min., 20 V max.
Average Output Current – I_O (per channel) ..... 15 mA
Output Voltage – V_O ..... -0.3 V min., 20 V max.
Total Package Power Dissipation – P_d (per channel) ..... 200 mW
Single Channel Product Only
Three State Enable Voltage – V_E ..... -0.3 V min., 20 V max.

Electrical Characteristics

T_A = -55°C to 125°C, unless otherwise specified. For 4.75 V ≤ V_{CC} ≤ 20 V, 2 mA ≤ $I_{F(ON)}$ ≤ 8 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V

Parameter		Sym.	Test Conditions		Group A Subgroups[11]	Min.	Typ.*	Max.	Units	Fig.	Notes
Logic Low Output Voltage		V_{OL}	I_{OL} = 6.4 mA (4 TTL Loads)		1, 2, 3			0.5	Volts	1, 3	2
Logic High Output Voltage		V_{OH}	I_{OH} = -2.6 mA (**V_{OH} = V_{CC} - 2.1 V)		1, 2, 3	2.4	**		Volts	2, 3	2
			I_{OH} = -0.32 mA		NA		31		Volts		
Output Leakage Current (V_{OUT} > V_{CC})		I_{OHH}	V_O = 5.5 V	I_F = 8 mA, V_{CC} = 4.5 V	1, 2, 3			100	µA		2
			V_O = 20 V					500	µA		
Logic Low Supply Current	Single Channel (5962-88768)	I_{CCL}	V_{CC} = 5.5 V	V_F = 0 V, V_E = Don't Care	1, 2, 3		4.5	6.0	mA		
			V_{CC} = 20 V				5.3	7.5	mA		
	Dual Channel (5962-88769)		V_{CC} = 5.5 V	V_{F1} = V_{F2} = 0 V	1, 2, 3		9.0	12.0	mA		
			V_{CC} = 20 V				10.6	15	mA		
Logic High Supply Current	Single Channel (5962-88768)	I_{CCH}	V_{CC} = 5.5 V	I_F = 8 mA, V_E = Don't Care	1, 2, 3		2.9	4.5	mA		
			V_{CC} = 20 V				3.3	6.0	mA		
	Dual Channel (5962-88769)		V_{CC} = 5.5 V	I_{F1} = I_{F2} = 8 mA	1, 2, 3		5.8	9.0	mA		
			V_{CC} = 20 V				6.6	12.0	mA		
Logic Low Short Circuit Output Current		I_{OSL}	V_O = V_{CC} = 5.5 V	V_F = 0 V	1, 2, 3	20			mA		2, 3
			V_O = V_{CC} = 20 V			35			mA		
Logic High Short Circuit Output Current		I_{OSH}	V_{CC} = 5.5 V	I_F = 8 mA, V_O = GND	1, 2, 3			-10	mA		2, 3
			V_{CC} = 20 V					-25	mA		
Input Forward Voltage		V_F	I_F = 8 mA		1, 2, 3	1.0	1.3	1.8	Volts	4	2
Input Reverse Breakdown Voltage		V_R	I_R = 10 µA		1, 2, 3	3			Volts		2
Input-Output Insulation		I_{I-O}	45% RH, t = 5 s, V_{I-O} = 1500 Vdc		1			1	µA		4, 5
Propagation Delay Time to Logic Low Output Level		t_{PHL}			9, 10, 11		173	300	ns	5, 6,	2, 6
Propagation Delay Time to Logic High Output Level		t_{PLH}			9, 10, 11		118	300	ns	5, 6,	2, 6
Logic High Common Mode Transient Immunity		$\|CM_H\|$	I_F = 2 mA, V_{CM} = 50 V_{P-P}		9	1000	10,000		V/µs	9	2, 7
Logic Low Common Mode Transient Immunity		$\|CM_L\|$	I_F = 0 mA, V_{CM} = 50 V_{P-P}		9	1000	10,000		V/µs	9	2, 7

Electrical Characteristics Single Channel Product Only

T_A = -55°C to 125°C, unless otherwise specified.
For 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, 4.5 V ≤ V_{CC} ≤ 20 V, 2 mA ≤ $I_{F(ON)}$ ≤ 8 mA, 2.0 V ≤ V_{EH} ≤ 20 V, 0 V ≤ V_{EL} ≤ 0.8 V unless otherwise specified.

Parameter	Sym.	Test Conditions		Group A Subgroups	Min.	Typ.*	Max.	Units	Fig.	Notes
High Impedance State Output Current	I_{OZL}	V_O = 0.4 V	V_{EN} = 2 V, V_F = 0 V	1, 2, 3			-20	µA		
	I_{OZH}	V_O = 2.4 V	V_{EN} = 2 V, I_F = 8 mA	1, 2, 3			20	µA		
		V_O = 5.5 V					100	µA		
		V_O = 20 V					500	µA		
Logic High Enable Voltage	V_{EH}			1, 2, 3	2.0			Volts		
Logic Low Enable Voltage	V_{EL}			1, 2, 3			0.8	Volts		
Logic High Enable Current	I_{EH}	V_{EN} = 2.7 V		1, 2, 3			20	µA		
		V_{EN} = 5.5 V					100	µA		
		V_{EN} = 20 V				0.004	250	µA		
Logic Low Enable Current	I_{EL}	V_{EN} = 0.4 V		1, 2, 3			-0.32	mA		

*All typical values are at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 5 mA unless otherwise specified.

Typical Characteristics

All typical values are at V_{CC} = 5 V, T_A = 25°C), $I_{F(ON)}$ = 5 mA unless otherwise specified.

Parameter	Symbol	Test Conditions	Typ.	Units	Fig.	Notes
Input Current Hysteresis	I_{HYS}	V_{CC} = 5 V	0.07	mA	3	2
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	I_F = 8 mA	-1.25	mV/°C		2
Input-Output Resistance	R_{I-O}	V_{I-O} = 500 Vdc	10^{13}	Ω		2, 8
Input-Output Capacitance	C_{I-O}	f = 1 MHz	2.0	pF		2, 8
Input Capacitance	C_{IN}	f = 1 MHz, V_F = 0 V	20	pF		2, 10
Output Rise Time (10-90%)	t_r		45	ns	5, 7	2
Output Fall Time (90-10%)	t_f		10	ns	5, 7	2

Single Channel Product Only

Output Enable Time to Logic High	t_{PZH}		30	ns	8	
Output Enable Time to Logic Low	t_{PZL}		30	ns	8	
Output Disable Time from Logic High	t_{PHZ}		45	ns	8	
Output Disable Time from Logic Low	t_{PLZ}		55	ns	8	

Dual Channel Product Only

Input-Input Insulation Leakage Current	I_{I-I}	45% Relative Humidity, V_{I-I} = 500 Vdc, T_A = 25°C, t = 5 s	0.5	nA		9
Resistance (Input-Input)	R_{I-I}	V_{I-I} = 500 Vdc	10^{13}	Ω		9
Capacitance (Input-Input)	C_{I-I}	f = 1 MHz	1.5	pF		9

Notes:

1. Peak Forward Input Current pulse width < 50 μs at 1 KHz maximum repetition rate.
2. Each channel.
3. Duration of output short circuit time not to exceed 10 ms.
4. Device considered a two terminal device: for 8 pin DIP, pins 1 through 4 are shorted together, and pins 5 through 8 are shorted together; for LCC, terminals 19, 20, 1, 2, 3 are shorted together, and terminals 7 through 15 are shorted together.
5. This is a momentary withstand test, not an operating condition.
6. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
7. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).
8. Measured between each input pair shorted together and all outputs for that channel shorted together.
9. Measured between adjacent input pairs shorted together; i.e., for 8 pin DIP, between pins 1 and 2 shorted together and pins 3 and 4 shorted together; for LCC, between terminals 19 and 20 shorted together, and terminals 2 and 3 shorted together.
10. Zero-bias capacitance measured between the LED anode and cathode.
11. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

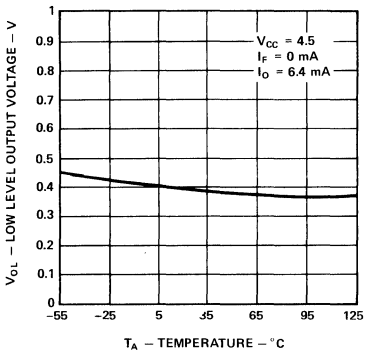


Figure 1. Typical Logic Low Output Voltage vs. Temperature

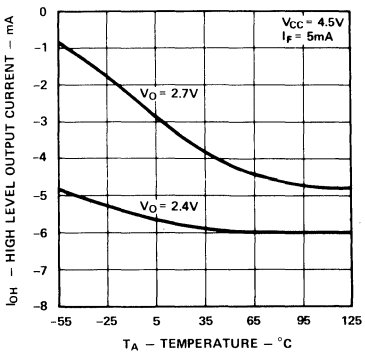


Figure 2. Typical Logic High Output Current vs. Temperature

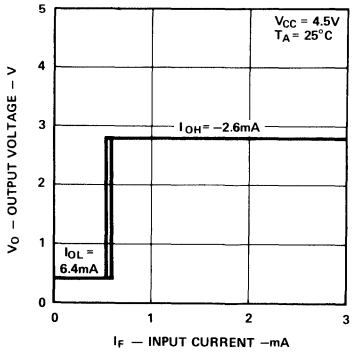


Figure 3. Output Voltage vs. Forward Input Current

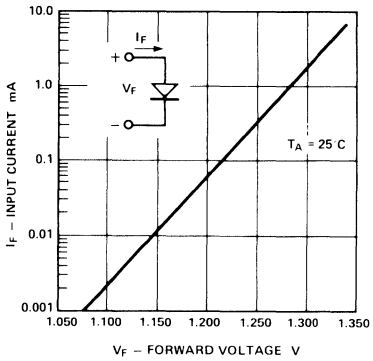


Figure 4. Typical Diode Input Forward Characteristic

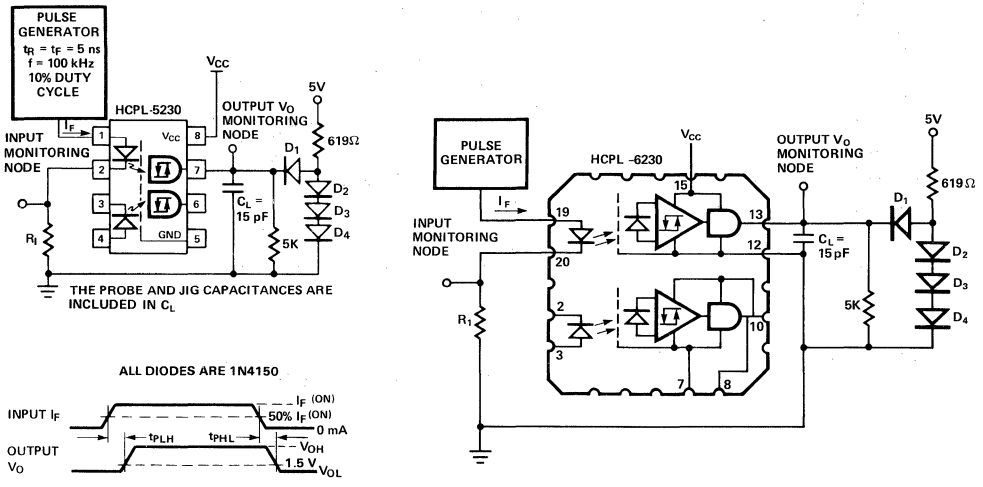


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

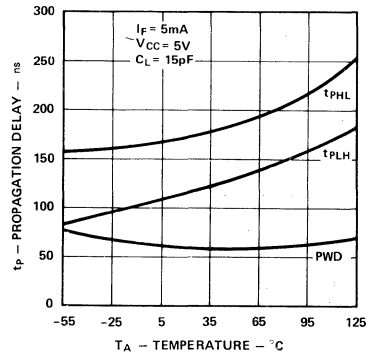


Figure 6. Typical Propagation Delay vs. Temperature

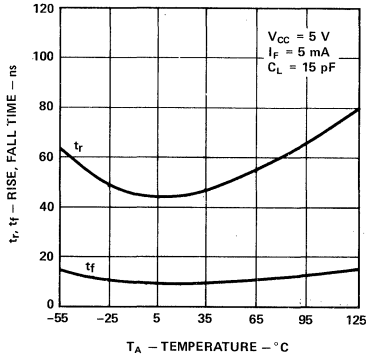


Figure 7. Typical Rise, Fall Time vs. Temperature

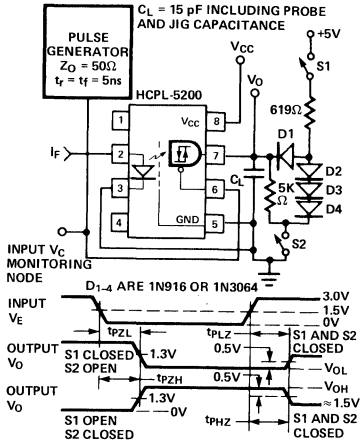


Figure 8. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}

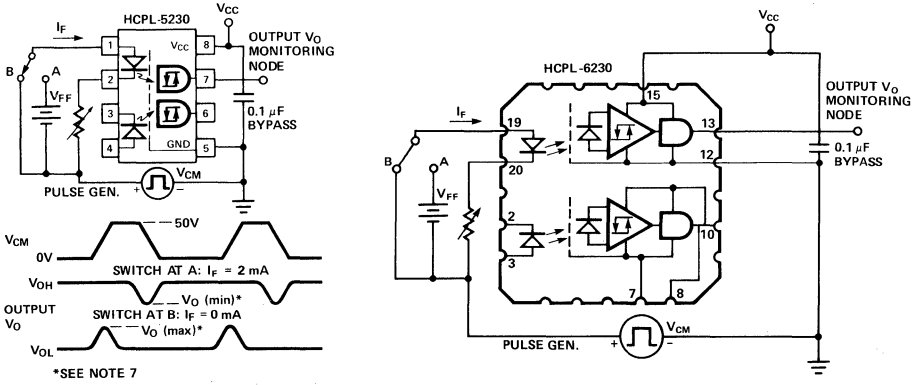


Figure 9. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

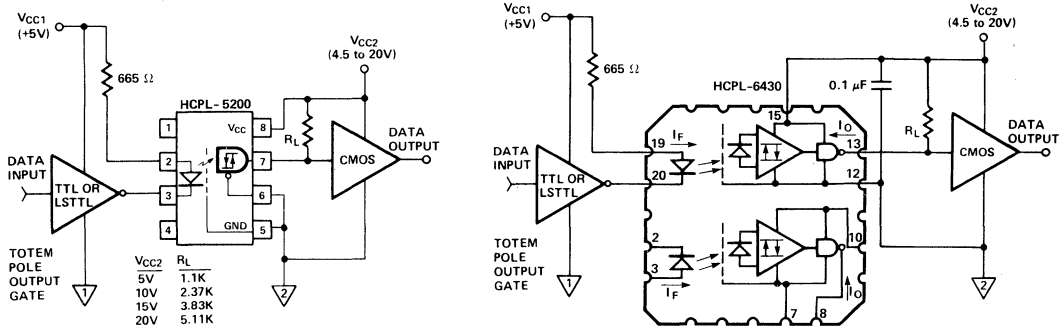


Figure 10. LSTTL to CMOS Interface Circuit.

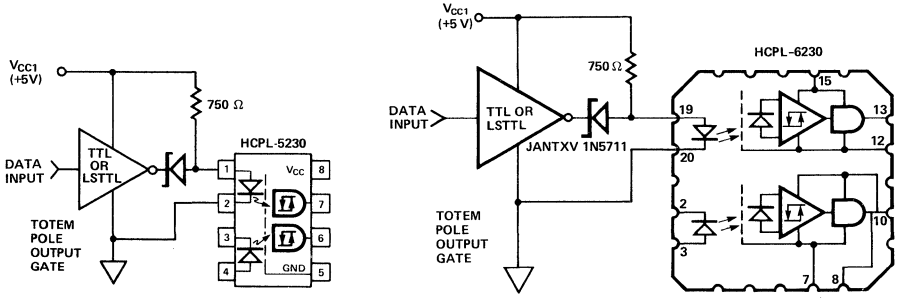


Figure 11. Recommended LED Drive Circuit.

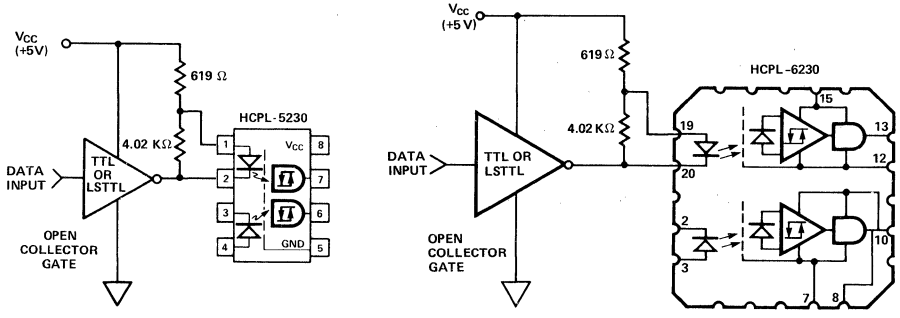


Figure 12. Series LED Drive with Open Collector Gate (4.02 kΩ Resistor Shunts I_{OH} from the LED)

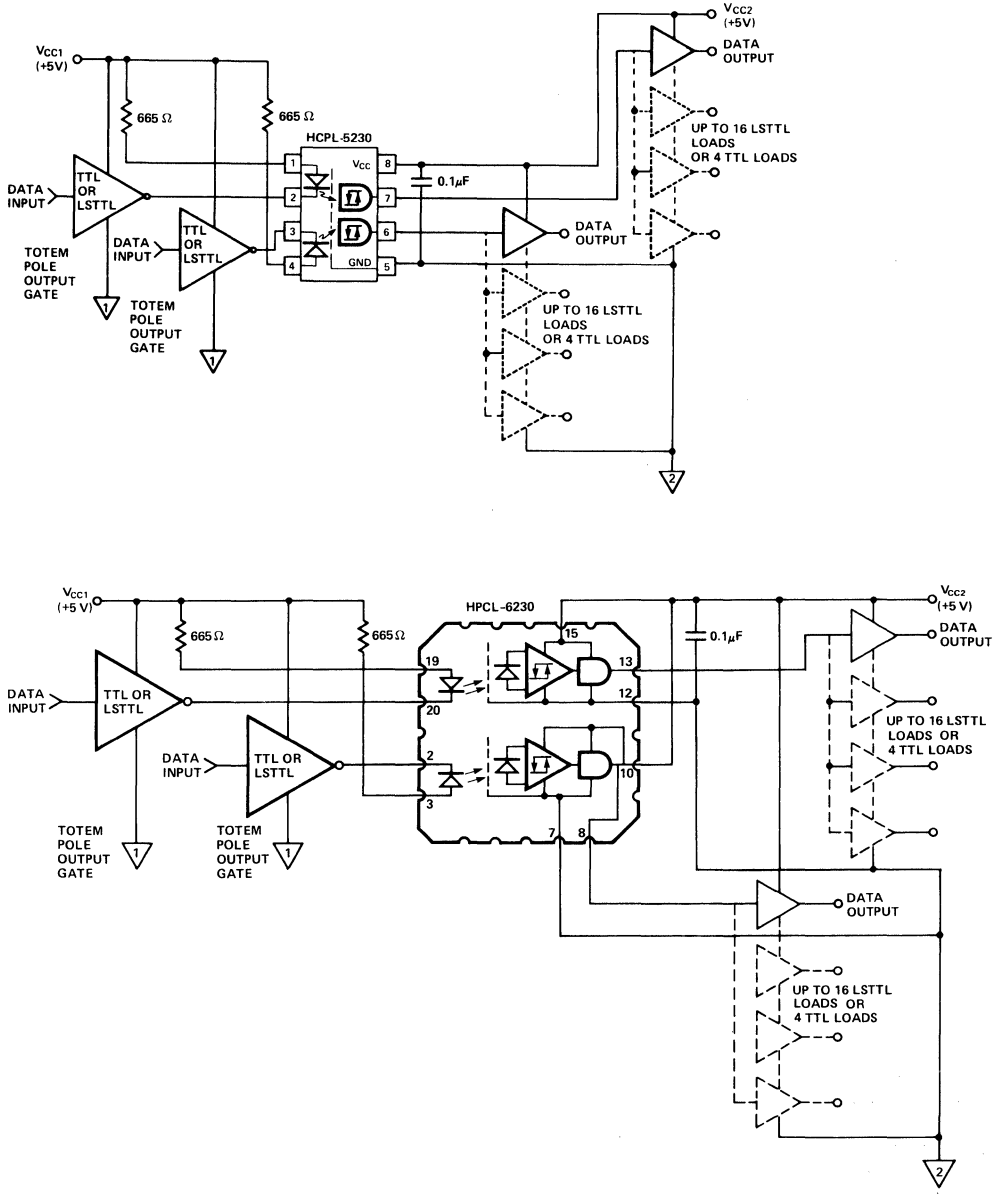


Figure 13. Recommended LSTTL to LSTTL Circuit

Part Numbering System

Commercial Product	Class B Product	SMD Product
HCPL-5200	HCPL-5201	5962 8876801PC
HCPL-5230	HCPL-5231	5962 8876901PC
HCPL-6230	HCPL-6231	By Request

SMD 5962 8876801PC, SMD 5962 8876901PC, and MIL-STD-883 Class B Test Program

Hewlett-Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC SMD 5962-88768 for an H.P. Optocoupler from the same generic family using the same manufacturing process, design rules and elements of the same microcircuit group.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883.

Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration–Condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C, and D.
Group A–See Electrical Characteristics Table.
Group B–No change.
Group C–No change.
Group D–Constant Acceleration – Condition A not E.

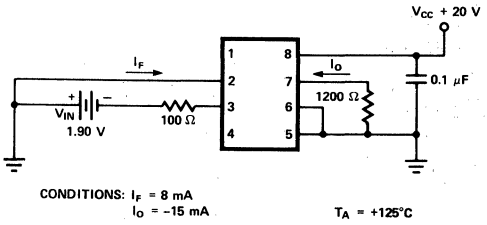


Figure 14. Single Channel Operating Circuit for Burn-in and Steady State Life Tests

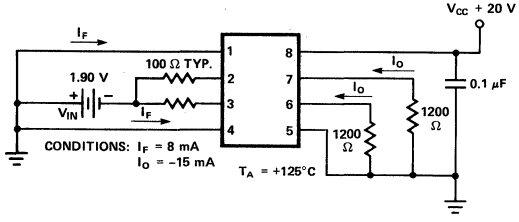


Figure 15. Dual Channel Operating Circuit for Burn-in and Steady State Life Tests

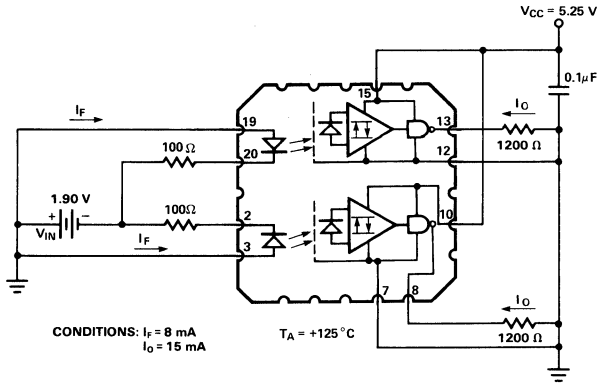


Figure 16. Operating Circuit for Burn-In and Steady State Life Tests

HEWLETT PACKARD

Very High Speed, Hermetically Sealed Optocoupler

Technical Data

8- pin Dual In-Line Package
HCPL-5400
HCPL-5401 (883B)
5962-8957001PC

HCPL-5430
HCPL-5431 (883B)
5962-8957101PC

20 Terminal Leadless Chip Carrier
HCPL-6430
HCPL-6431 (883B)
5962-89571022A

Features

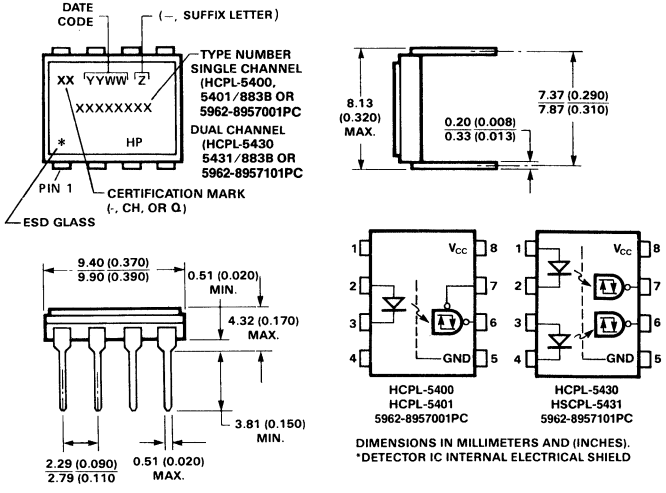
- DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534
- Hermetically Sealed Packages
- Performance Guaranteed Over -55°C to +125°C Ambient Temperature Range
- MIL-STD-883 Class B Testing
- High Speed Guaranteed Over Temperature
- 60 ns Maximum Propagation Delay
- 35 ns Maximum Pulse Width Distortion
- High Common Mode Rejection – 500 V/μs Guaranteed
- Compatible with TTL, STTL, LSTTL and HCMOS Logic Families
- Three State Output (No Pull-Up Resistor Required) – (5400/1 Only)
- HCPL-2400 Function Compatibility
- 1500 Vdc Withstand Test Voltage

Applications

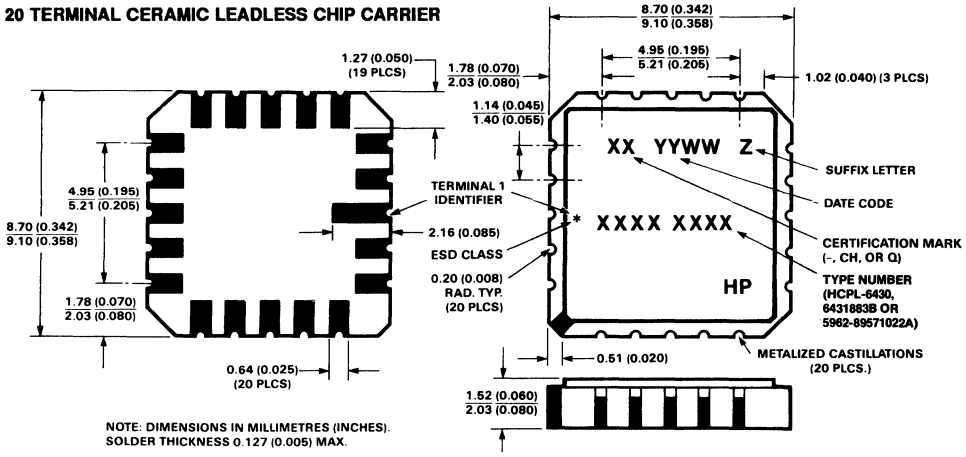
- Military/High Reliability Systems
- Isolation of High Speed Logic Systems
- Computer-Peripheral Interfaces
- Isolated Bus Driver (Networking Applications) – (5400/1 Only)
- Switching Power Supplies
- Ground Loop Elimination
- High Speed Disk Drive I/O
- Digital Isolation for A/D, D/A Conversion
- Pulse Transformer Replacement

Outline Drawings

8 PIN CERAMIC DUAL-IN-LINE PACKAGE



20 TERMINAL CERAMIC LEADLESS CHIP CARRIER



NOTE: DIMENSIONS IN MILLIMETRES (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

Description

The HCPL-5400, HCPL-5401, and 5962-8957001PC are single channel, logic gate optocouplers. The HCPL-5430, HCPL-5431, and 5962-8957101PC are dual channel units made from the same chip sets. All six products are in 8 pin hermetic dual in-line packages. These units are capable of operation and storage over the full military temperature ranges and can be purchased as either single or dual channel standard product (HCPL-5400 and HCPL-5430 respectively), with full MIL-STD-883 Class Level B testing (HCPL-5401 and HCPL-5431 respectively), or from the DESC Standard Military Drawings (SMDs) 5962-89570 and 5962-89571 as (5962-8957001PC or 5962-8957101PC respectively). All parts are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the SMD part #, or by adding option #200 to the part number for non-SMD parts.

The HCPL-6430, HCPL-6431, and 5962-89571022A are dual channel parts in twenty terminal hermetic, ceramic, leadless chip carriers. The standard part is HCPL-6430. The product with full MIL-STD-883 Class Level B testing is HCPL-6431. The DESC SMD part is 5962-89571022A. All three products are configured and function as two independent single channels without enable. Devices are delivered with solder-dipped terminals as a standard feature. Units may also be purchased with gold-plated terminals.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

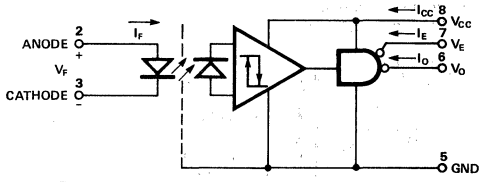
Each channel contains an AlGaAs light emitting diode which is optically coupled to an integrated high gain photon detector. This combination results in very high data rate capability. The detector has a threshold with hysteresis. The hysteresis provides typically 0.25 mA of differential mode noise immunity and minimizes the potential for output signal chatter. The detector in the single channel units has a three state output stage which eliminates the need for a pull-up resistor and allows for direct drive of a data bus.

All nine units are compatible with TTL, STTL, LSTTL, and HCMOS logic families. The 35 ns pulse width distortion specification guarantees a 10 mBaud signaling rate at +125°C with 35% pulse width distortion. Figures 11 through 16 show recommended circuits for reducing pulse width distortion and optimizing the signal rate of the product.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Schematics

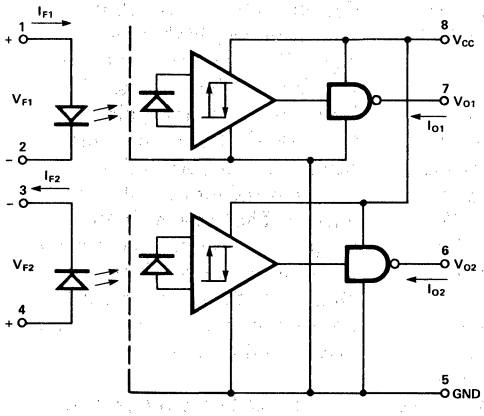
8 PIN CERAMIC DIP SINGLE CHANNEL SCHEMATIC



TRUTH TABLE
(POSITIVE LOGIC)

INPUT	ENABLE	OUTPUT
H (ON)	L	L
L (OFF)	L	H
H (ON)	H	Z
L (OFF)	H	Z

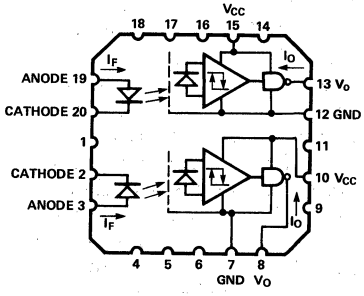
8 PIN CERAMIC DIP DUAL CHANNEL SCHEMATIC



TRUTH TABLE
(POSITIVE LOGIC)

INPUT	OUTPUT
H (ON)	L
L (OFF)	H

20 TERMINAL CERAMIC LEADLESS CHIP CARRIER SCHEMATIC



TRUTH TABLE
(POSITIVE LOGIC)

INPUT	OUTPUT
H (ON)	L
L (OFF)	H

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.75	5.25	Volts
Input Current (High)	$I_{F(ON)}$	6	10	mA
Input Voltage (Low)	$V_{F(OFF)}$	–	0.7	Volts
Fan Out (each channel)	N	–	5	TTL Loads

Single Channel Product Only

Enable Voltage (Low)	V_{EL}	0	0.8	Volts
Enable Voltage (High)	V_{EH}	2.0	V_{CC}	Volts

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Case Temperature – T_C ..... +170°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Forward Current – $I_{F\,AVG}$ ..... 10 mA
Peak Input Current – $I_{F\,PK}$ ..... 20 mA[1]
Reverse Input Voltage – V_R ..... 5 V
Supply Voltage – V_{CC} ..... 0 V min., 7.0 V max.
Average Output Current – I_O ..... -25 mA min., 25 mA max.
Output Voltage – V_O ..... -0.5 V min., 10 V max.
Output Power Dissipation – P_O (per channel) ..... 130 mW
Total Package Power Dissipation P_d ..... 400 mW
Single Channel Product Only
Three State Enable Voltage – V_E ..... -0.5 V min., 10 V max.

Electrical Characteristics

T_A = -55°C to 125°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, 6 mA ≤ $I_{F(ON)}$ ≤ 10 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.7 V, unless otherwise specified.

Parameter		Sym.	Test Conditions	Group A[10] Subgroup	Min.	Typ.*	Max.	Units	Fig.	Notes
Logic Low Output Voltage		V_{OL}	I_{OL} = 8.0 mA (5 TTL Loads)	1, 2, 3			0.5	Volts	1	9
Logic High Output Voltage		V_{OH}	I_{OH} = -4.0 mA	1, 2, 3	2.4			Volts	2	9
Output Leakage Current		I_{OHH}	V_O = 5.25 V, V_F = 0.7 V	1, 2, 3			100	µA		9
Logic Low Supply Current	Single Channel	I_{CCL}	V_{CC} = 5.25 V V_E = 0 V (Single Channel Only)	1, 2, 3		19	26	mA		
	Dual Channel					38	52			14
Logic High Supply Current	Single Channel	I_{CCH}		1, 2, 3		17	26	mA		
	Dual Channel					34	52			14
Input Forward Voltage		V_F	I_F = 10 mA	1, 2, 3	1.0	1.35	1.85	Volts	4	9
Input Reverse Breakdown Voltage		V_R	I_R = 10 µA	1, 2, 3	3.0	7.0		Volts		9
Input-Output Insulation Leakage Current		I_{I-O}	45% RH, t = 5 s, V_{I-O} = 1500 Vdc	1			1	µA		2, 3
Propagation Delay Time Logic Low Output Level		t_{PHL}		9, 10, 11		33	60	ns	5, 6, 7	4, 9
Propagation Delay Time Logic High Output Level		t_{PLH}		9, 10, 11		30	60	ns	5, 6, 7	4, 9
Pulse Width Distortion		PWD		9, 10, 11		3	35	ns	5, 6, 7	4, 9
Logic High Common Mode Transient Immunity		$\|CM_H\|$	I_F = 0 V_{CM} = 50 V_{P-P}	9, 10, 11	500	3000		V/µs	11	5, 9, 11
Logic Low Common Mode Transient Immunity		$\|CM_L\|$	I_F = 6 mA V_{CM} = 50 V_{P-P}	9, 10, 11	500	3000		V/µs	11	5, 9, 11

Guaranteed Performance

T_A = -55°C to 125°C

Propagation Delay Skew	t_{PSK}				30		ns	10	12, 13

Electrical Characteristics (continued)

T_A = -55°C to 125°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, 6 mA ≤ $I_{F(ON)}$ ≤ 10 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.7 V, unless otherwise specified.

Single Channel Product Only

Parameter	Sym.	Test Conditions		Group A[10] Subgroup	Min.	Typ.*	Max.	Units	Fig.	Notes
Logic High Enable Voltage	V_{EH}			1, 2, 3	2.0			Volts		
Logic Low Enable Voltage	V_{EL}			1, 2, 3			0.8	Volts		
Logic High Enable Current	I_{EH}	V_E = 2.4 V		1, 2, 3			20	µA		
		V_E = 5.25 V,		1, 2, 3			100	µA		
Logic Low Enable Current	I_{EL}	V_E = 0.4 V		1, 2, 3		-0.28	-0.4	mA		
High Impedance State Supply Current	I_{CCZ}	V_{CC} = 5.25 V V_E = 5.25 V		1, 2, 3		22	28	mA		
High Impedance State Output Current	I_{OZL}	V_O = 0.4 V, V_E = 2 V		1, 2, 3			-20	µA		
	I_{OZH}	V_O = 2.4 V	V_E = 2 V	1, 2, 3			20	µA		
		V_O = 5.25 V					100	µA		

*All typical values are at V_{CC} = 5 V, T_A = 25°C, I_F = 8 mA except where noted.

Typical Characteristics

All typical values are at V_{CC} = 5 V, T_A = 25°C, I_F = 8 mA unless otherwise specified.

Parameter	Symbol	Typical	Units	Test Conditions	Figure	Note
Input Current Hysteresis	I_{HYS}	0.25	mA	V_{CC} = 5 V	3	
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	-1.11	mV/°C	I_F = 10 mA	4	
Input-Output Resistance	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 Vdc		2
Input-Output Capacitance	C_{I-O}	0.6	pF	f = 1 MHz, V_{I-O} = 0 Vdc		2
Logic Low Short Circuit Output Current	I_{OSL}	65	mA	V_O = V_{CC} = 5.25 V, I_F = 10 mA		6, 9
Logic High Short Circuit Output Current	I_{OSH}	-50	mA	V_{CC} = 5.25 V, I_F = 0 mA, V_O = GND		6, 9
Output Rise Time (10-90%)	t_r	15	ns		5	
Output Fall Time (90-10%)	t_f	10	ns		5	
Power Supply Noise Immunity	PSNI	0.5	V_{P-P}	48 Hz ≤ f_{ac} ≤ 50 MHz		7
Single Channel Product Only						
Input Capacitance	C_{IN}	15	pF	f = 1 MHz, V_F = 0 V, Pins 2 and 3		
Output Enable Time to Logic High	t_{PZH}	15	ns		8, 9	
Output Enable Time to Logic Low	t_{PZL}	30	ns		8, 9	
Output Disable Time from Logic High	t_{PHZ}	20	ns		8, 9	
Output Disable Time from Logic Low	t_{PLZ}	15	ns		8, 9	
Dual Channel Product Only						
Input Capacitance	C_{IN}	15	pF	f = 1 MHz, V_O = 0 V, Pins 1 and 2, Pins 3 and 4		
Input-Input Capacitance	C_{I-I}	1.3	pF	f = 1 MHz, V_F = 0 V		8
Input-Input Leakage Current	I_{I-I}	0.5	nA	V_{I-I} = 500 Vdc, 45% RH		8
Input-Input Resistance	R_{I-I}	10^{12}	ohms	V_{I-I} = 500 Vdc		8

Notes:

1. Not to exceed 5% duty factor, not to exceed 50 µsec pulse width.
2. Device considered a two terminal device: for 8 pin DIP, pins 1 through 4 are shorted together, and pins 5 through 8 are shorted together; for LCC, terminals 19, 20, 1, 2, 3 are shorted together, and terminals 7 through 15 are shorted together.
3. This is a momentary withstand test, not an operating condition.
4. t_{PHL} propagation delay is measured from the 50% level on the rising edge of the input current pulse to the 1.5 V level on the falling edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% level on the falling edge of the input current pulse to the 1.5 V level on the rising edge of the output pulse. Pulse width distortion, PWD = $|t_{PHL}-t_{PLH}|$.
5. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_{O(MIN)}$ > 2.0 V). CM_L is the maximum slew rate of common mode voltage that can be sustained with the output voltage in the logic low state ($V_{O(MAX)}$ < 0.8 V).
6. Duration of output short circuit time not to exceed 10 ms.
7. Power Supply Noise Immunity is the peak to peak amplitude of the ac ripple voltage on the V_{CC} line that the device will withstand and still remain in the desired logic state. For desired logic high state, $V_{OH(MIN)}$ > 2.0 V, and for desired logic low state, $V_{OL(MAX)}$ < 0.8 volts.
8. Measured between adjacent input pairs shorted together; i.e., for 8 pin DIP, between pins 1 and 2 shorted together and pins 3 and 4 shorted together; for LCC, between terminals 19 and 20 shorted together, and terminals 2 and 3 shorted together.
9. Each channel.
10. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and/883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
11. Subgroups 10 and 11 shall be tested as part of device initial characterization and after design and process changes. Subgroups 10 and 11 shall be guaranteed to the limits specified for all lots not specifically tested. Subgroup 9 shall be tested with every lot.
12. Propagation delay skew is defined as the difference between the minimum and maximum propagation delays for any given group of HCPL-540X, HCPL-543X, and HCPL-643X optocouplers that are all switching at the same time under the same operating conditions. The minimum propagation delay is the shortest delay, either t_{PLH} or t_{PHL}, of any of the optocouplers; the maximum delay is the longest delay, either t_{PLH} or t_{PHL}, of any of the optocouplers. For more application information see HCPL-2430 data sheet.
13. Propagation delay skew is indirectly tested and guaranteed through guardbanding of the minimum and maximum t_{PHL} and t_{PLH} limits.
14. The HCPL-6430 and HCPL-6431 dual channel parts function as two independent single channel units. Use the single channel parameter limits.

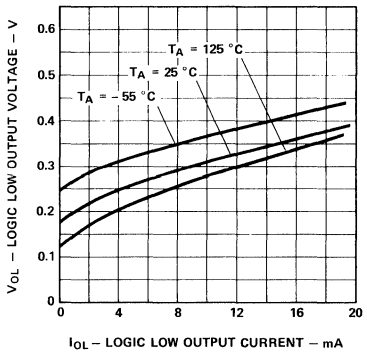


Figure 1. Typical Logic Low Output Voltage vs. Logic Low Output Current.

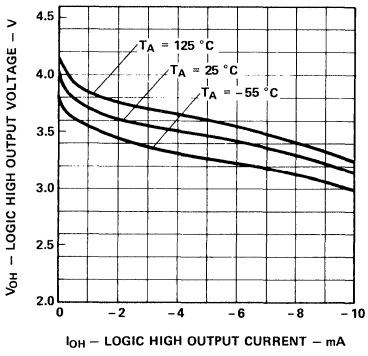


Figure 2. Typical Logic High Output Voltage vs. Logic High Output Current.

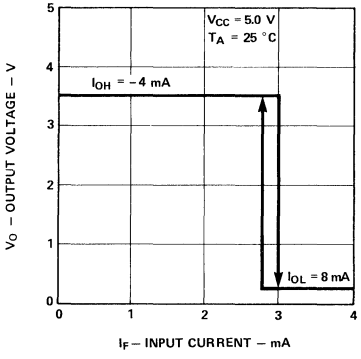


Figure 3. Typical Output Voltage vs. Input Forward Current.

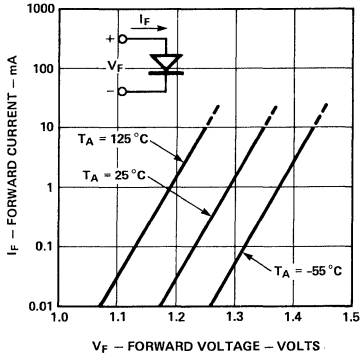


Figure 4. Typical Diode Input Forward Current Characteristic.

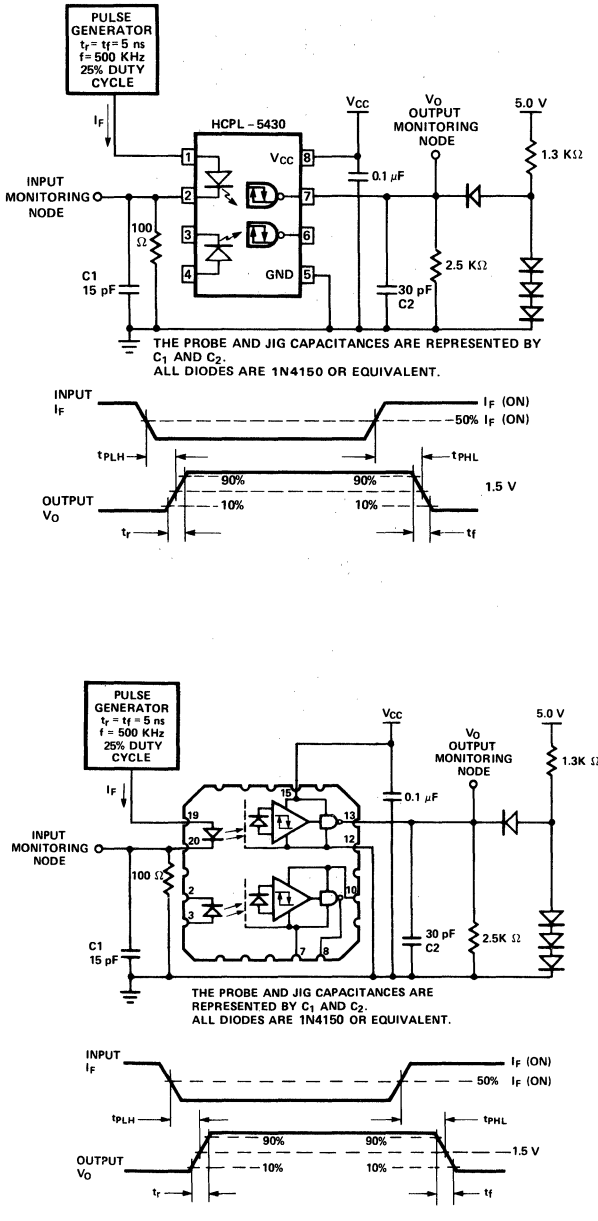


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f.

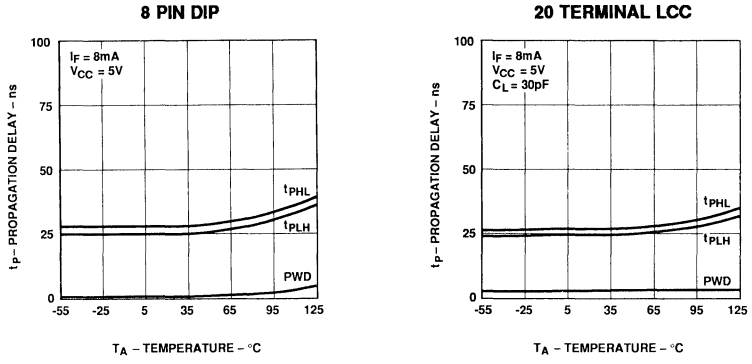


Figure 6. Typical Propagation Delay vs. Ambient Temperature.

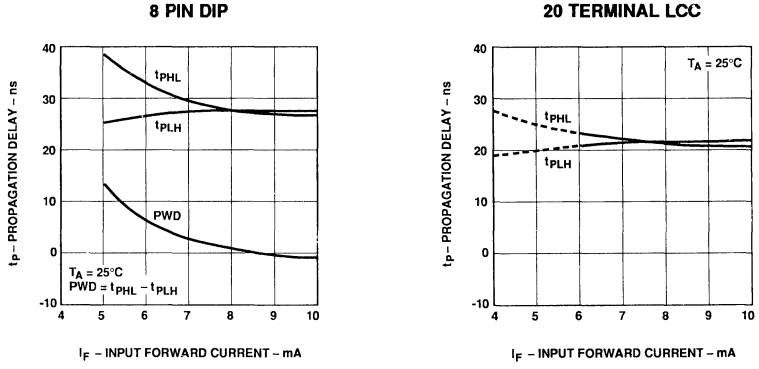
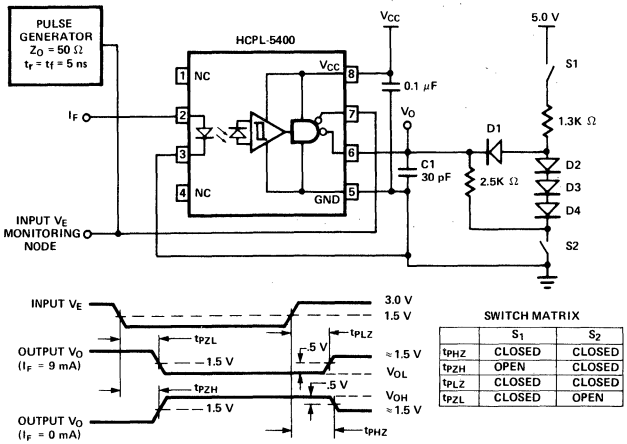


Figure 7. Typical Propagation Delay vs. Input Forward Current.



	S_1	S_2
t_{PHZ}	CLOSED	CLOSED
t_{PZH}	OPEN	CLOSED
t_{PLZ}	CLOSED	CLOSED
t_{PZL}	CLOSED	OPEN

Figure 8. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}. (Single Channel Product Only).

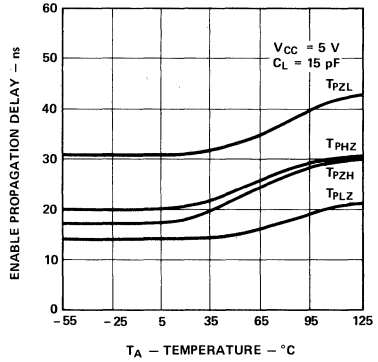


Figure 9. Typical Enable Propagation Delay vs. Ambient Temperature. (Single Channel Product Only).

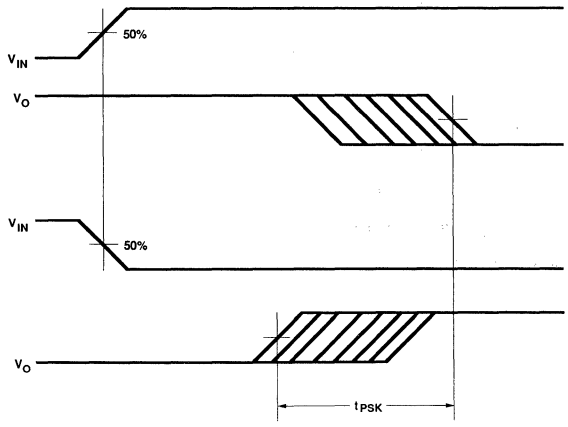
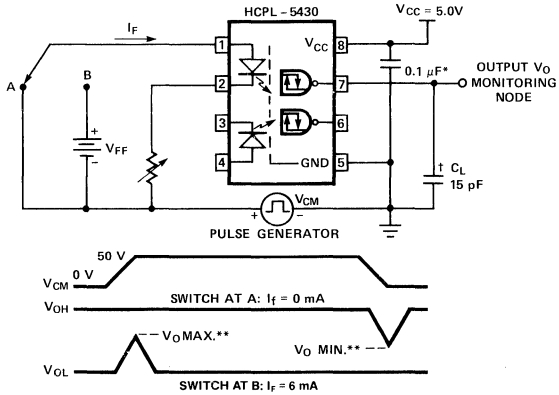
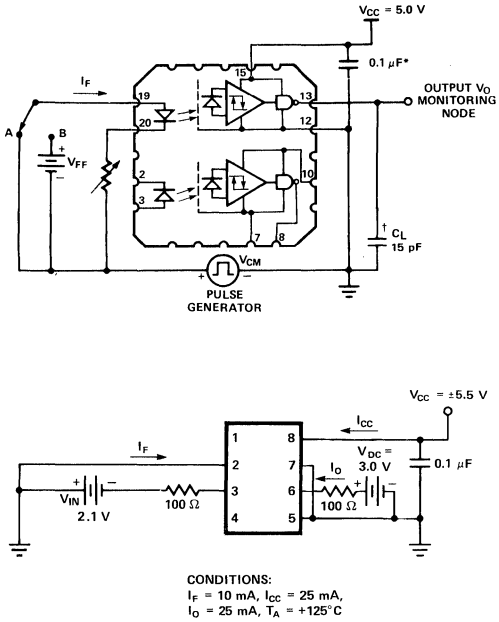


Figure 10. Propagation Delay Skew, t_{PSK}, Waveform.



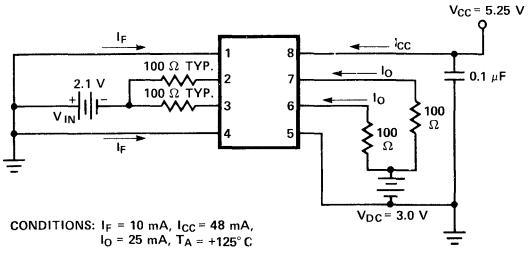
*TOTAL LEAD LENGTH < 10 mm FROM DEVICE UNDER TEST.
**SEE NOTE 5.
†C_L IS APPROXIMATELY 15 pF, WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

Figure 11. Test Diagram for Common Mode Transient Immunity and Typical Waveforms.



CONDITIONS:
I_F = 10 mA, I_{CC} = 25 mA,
I_O = 25 mA, T_A = +125°C

Figure 12. Single Channel Operating Circuit for Burn-In and Steady State Life Tests.



CONDITIONS: I_F = 10 mA, I_{CC} = 48 mA,
I_O = 25 mA, T_A = +125° C

Figure 13. Dual Channel Operating Circuit for Burn-In and Steady State Life Tests.

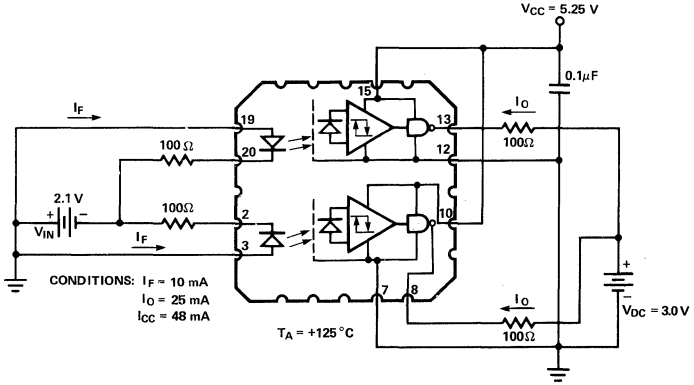


Figure 14. Operating Circuit for Burn-In and Steady State Life Tests.

Part Numbering System

Commercial Product	Class B Product	SMD Product
HCPL-5400	HCPL-5401	5962-8957001PC
HCPL-5430	HCPL-5431	5962-8957101PC
HCPL-6430	HCPL-6431	5962-89571022A

SMD 5962-8957001PC, SMD 5962-8957101PC, SMD 5962-89571022A, and MIL-STD-883 Class B Test Programs

Hewlett-Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC SMDs 5962-89570 and 5962-89571 for Hewlett-Packard Optocouplers from the same generic families using the same manufacturing processes, design rules and elements of the same microcircuit groups.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883.

Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration–Condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C, and D.
Group A–See Electrical Characteristics Table.
Group B–No change.
Group C–No change.
Group D–Constant Acceleration – Condition A not E.

Data Rate and Pulse-Width Distortion Definitions

Propagation delay is a figure of merit which describes the finite amount of time required for a system to translate information from input to output when shifting logic levels. Propagation delay from low to high (t_{PLH}) specifies the amount of time required for a system's output to change from a Logic 0 to a Logic 1, when given a stimulus at the input. Propagation delay from high to low (t_{PHL}) specifies the amount of time required for a system's output to change from a Logic 1 to a Logic 0, when given a stimulus at the input (see Figure 5).

When t_{PLH} and t_{PHL} differ in value, pulse width distortion results. Pulse width distortion is defined as $|t_{PHL}-t_{PLH}|$ and determines the maximum data rate capability of a distortion-limited system. Maximum pulse width distortion on the order of 25-35% is typically used when specifying the maximum data rate capabilities of systems. The exact figure depends on the particular application (RS-232, PCM, T-1, etc.).

These high performance optocouplers offer the advantages of specified propagation delay (t_{PLH}, t_{PHL}), and pulse-width distortion ($|t_{PLH}, t_{PHL}|$) over temperature and power supply voltage ranges.

Applications

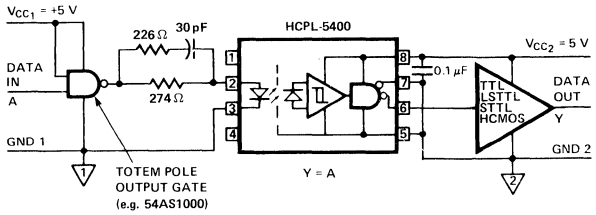


Figure 15. Recommended HCPL-5400 Interface Circuit.

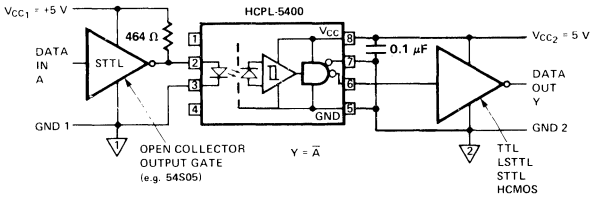


Figure 16. Alternative HCPL-5400 Interface Circuit.

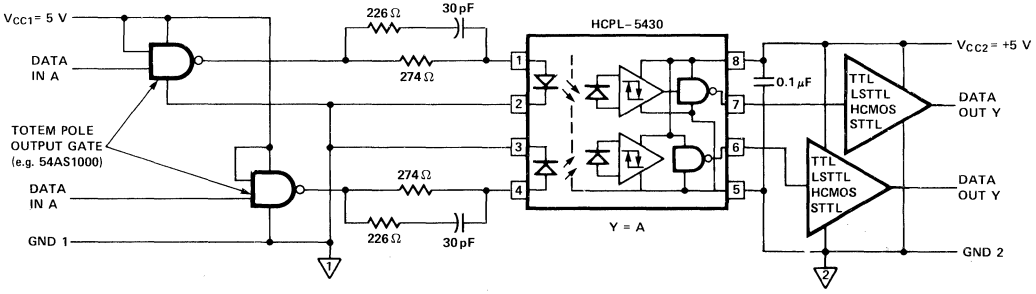


Figure 17. Recommended HCPL-5430 Interface Circuit.

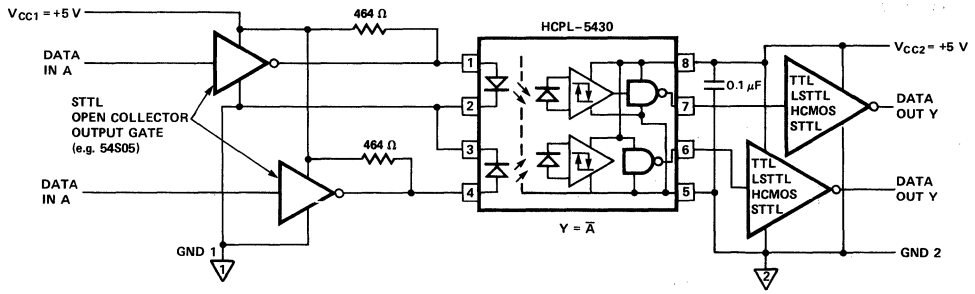


Figure 18. Alternative HCPL-5430 Interface Circuit.

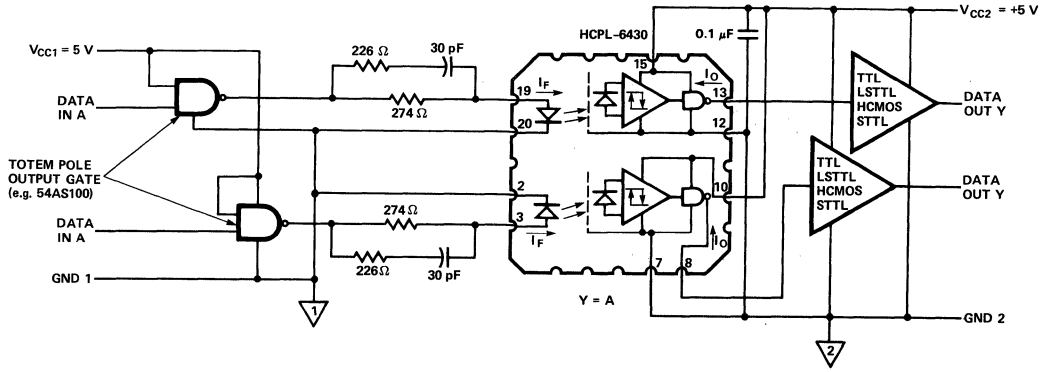


Figure 19. Recommended HCPL-6430 Interface Circuit.

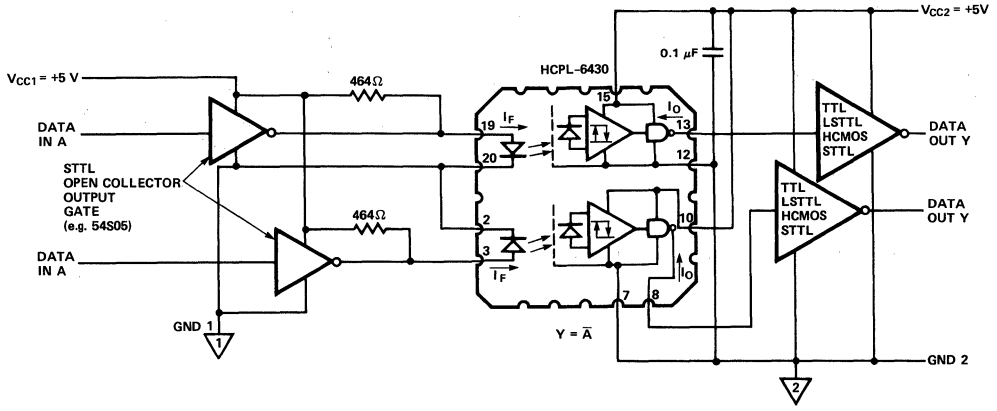


Figure 20. Alternative HCPL-6430 Interface Circuit.

HEWLETT PACKARD

Dual Channel High CMR High Speed Hermetically Sealed Optocouplers

Technical Data

6N134
6N134/883B
8102801EC

Features

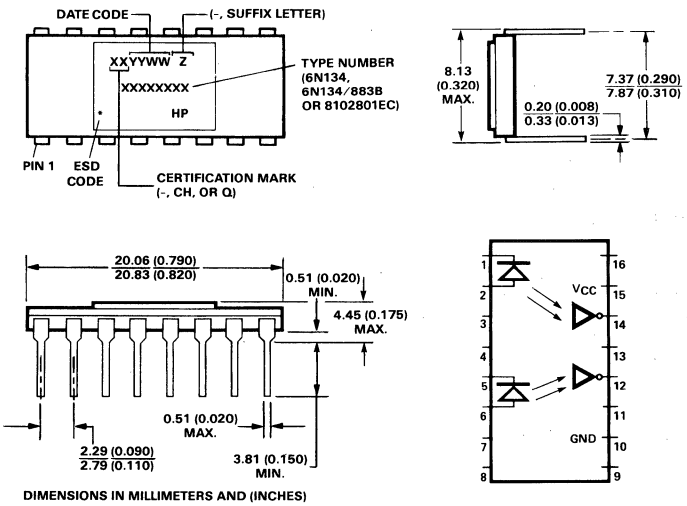
- **DESC Standard Military Drawing**
- **Manufactured and Tested on a MIL-STD-1772 Certified Line**
- **QML-MIL-H-38534**
- **Hermetically Sealed 8-pin Dual In-Line Package**
- **Performance Guaranteed Over -55°C to +125°C Ambient Temperature Range**
- **MIL-STD-883 Class B Testing**
- **Internal Shield for Higher CMR**
- **1500 Vdc Withstand Test Voltage**
- **High Radiation Immunity**
- **HCPL-2631, HCPL-56XX, 66XX Function Compatibility**

Description

The 6N134, 6N134/883B, and 8102801EC units are hermetically sealed, high CMR, high speed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product (6N134), with full MIL-STD-883 Class Level B testing (6N134/883B) or from the DESC Drawing 81028 as (8102801EC). All three products are dual channel in sixteen pin hermetic dual in-line packages. These parts are normally shipped with gold platted leads. They are also available with solder dipped leads by replacing C with A in the DESC part #, or by adding option #200 to the part number for non-DESC parts.

Each channel contains a GaAsP light emitting diode which is optically coupled to an integrated high speed photon detector. The output of the detector is an open collector Schottky clamped transistor. Internal shields provide a guaranteed common mode transient immunity specification of 1000 V/μs. Selection for higher CMR values are available by special request.

Outline Drawing



DIMENSIONS IN MILLIMETERS AND (INCHES)

This unique optocoupler design provides maximum dc and ac circuit isolation between each input and output while achieving TTL circuit compatibility. These optocouplers operate such that a minimum input current of 10 mA in each channel will sink a six gate fanout (10 mA) at the output with 4.5 to 5.5 V V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 55 nsec.

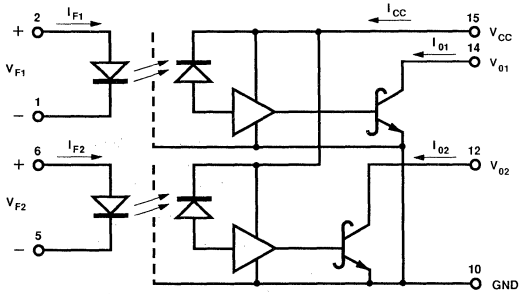
The test program performed on the 8102801EC is in compliance with DESC Drawing 81028. The electrical characteristics table shows Group A Subgroup testing requirements from this drawing.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Applications

- **Military/High Reliability Systems**
- **Logic Ground Isolation**
- **Line Receiver**
- **Computer-Peripheral Interface**
- **Vehicle Command/Control Isolation**
- **Harsh Industrial Environments**
- **System Test Equipment Isolation**

Schematic



NOTE:
A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 15 AND 10.

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Temperature (soldering, 10 seconds) ..... +260°C
Junction Temperature (T_J) ..... +175°C
Peak Forward Input Current
(each channel) ..... 40 mA (≤1 ms Duration)
Average Input Forward Current (each channel) ..... 20 mA
Input Power Dissipation (each channel) ..... 35 mW
Reverse Input Voltage (each channel) ..... 5 V
Supply Voltage – V_{CC} ..... 7 V (1 minute max.)
Output Current – I_O (each channel) ..... 25 mA
Output Power Dissipation (each channel) ..... 40 mW
Output Voltage – V_O (each channel) ..... 7 V*
Total Power Dissipation (both channels) ..... 350 mW

*Selection for higher output voltages up to 20 V is available.

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Input Current, Low Level, Each Channel	I_{FL}	0	250	μA
Input Current, High Level, Each Channel	I_{FH}	12.5*	16	mA
Supply Voltage	V_{CC}	4.5	5.5	V
Fan Out (TTL Load), Each Channel	N		6	
Operating Temperature	T_A	-55	125	°C

*12.5 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 10 mA or less.

Electrical Specifications

Test	Symbol	Conditions	Group A Sub-groups[11]	Limits			Unit	Fig.	Note
				Min.	Typ.**	Max.			
Low Level Output Voltage	V_{OL}*	V_{CC} = 5.5 V; I_F = 10 mA I_{OL} = 10 mA	1, 2, 3	–	0.4	0.6	V	4	1, 9
Current Transfer Ratio	h_F CTR	V_O = 0.6 V; I_F = 10 mA V_{CC} = 5.5 V	1, 2, 3	100		–	%		1
High Level Output Current	I_{OH}*	V_{CC} = 5.5 V; V_O = 5.5 V I_F = 250 µA	1, 2, 3	–	5	250	µA dc		1
High Level Supply Current	I_{CCH}*	V_{CC} = 5.5 V; I_{F1} = I_{F2} = 0 mA	1, 2, 3	–	18	28	mA dc		
Low Level Supply Current	I_{CCL}*	V_{CC} = 5.5 V; I_{F1} = I_{F2} = 20 mA	1, 2, 3	–	26	36	mA dc		
Input Forward Voltage	V_F*	I_F = 20 mA	1, 2	–	1.55	1.75	V dc	1	1
			3	–		1.85			
Input Reverse Breakdown Voltage	V_{BR}*	I_R = 10 mA	1, 2, 3	5.0		–	V dc		1
Input to Output Insulation Leakage Current	I_{I-O}*	V_{IO} = 1500 V dc Relative Humidity = 45% t = 5 seconds	1	–		1.0	µA dc		2, 10
Capacitance Between Input/Output	C_{I-O}	f = 1 MHz; T_C = 25°C	4	–		4.0	pF		3
Propagation Delay Time, Low to High Output Level	t_{PLH}*	R_L = 510 Ω; C_L = 50 pF I_F = 13 mA	9	–		100	ns	2, 3	1, 5
			10, 11	–		140			
Propagation Delay Time, High to Low Output Level	t_{PHL}*	R_L = 510 Ω; C_L = 50 pF I_F = 13 mA	9	–		100	ns	2, 3	1, 6
			10, 11	–		120			
Output Rise Time	t_{LH}	R_L = 510 Ω C_L = 50 pF; I_F = 13 mA	9, 10, 11	–		90	ns		
Output Fall Time	t_{HL}			–		40			
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	V_{CM} = 50 V (peak); V_O = 2 V minimum; R_L = 510 Ω; I_F = 0 mA	9, 10, 11	1000	10000	–	V µs	6	1, 7, 11, 12
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	V_{CM} = 50 V (peak); V_O = 0.8 V minimum; R_L = 510 Ω; I_F = 10 mA	9, 10, 11	1000	10000	–	V µs	6	1, 8, 11, 12

*For JEDEC registered parts. **All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Specifications T_A = 25°C), V_{CC} = 5 V each channel

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz		1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.5		mV/°C	I_F = 20 mA		1
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Input-Input Leakage Current	I_{I-I}		0.5		nA	Relative Humidity = 45% V_{I-I} = 500 V, t = 5 s		4
Resistance (Input-Input)	R_{I-I}		10^{12}		Ω	V_{I-I} = 500 V		4
Capacitance (Input-Input)	C_{I-I}		0.55		pF	f = 1 MHz		4
Output Rise Time (10-90%)	t_r		35		ns	R_L = 510 Ω, C_L = 15 pF I_F = 13 mA		1
Output Fall Time (90-10%)	t_f		35		ns			

Notes:

1. Each channel.
2. Measured between pins 1 through 8 shorted together and pins 9 through 16 shorted together.
3. Measured between pins 1 and 2 or 5 and 6 shorted together, and pins 10, 12, 14 and 15 shorted together.
4. Measured between pins 1 and 2 shorted together, and pins 5 and 6 shorted together.
5. The t_{PLH} propagation delay is measured form the 6.5 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. The t_{PHL} propagation delay is measured from the 6.5 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
7. CM_H is the max. tolerable common mode transient to assure that the output will remain in a high logic state (i.e., V_o > 2.0 V).
8. CM_L is the max. tolerable common mode transient to assure that the output will remain in a low logic state (i.e., V_o < 0.8 V).
9. It is essential that a bypass capacitor (0.1 µF, ceramic) be connected from pin 10 to pin 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.
10. This is a momentary withstand test, not an operating condition.
11. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
12. Subgroups 10 and 11 shall be tested as part of device initial characterization and after design and process changes. Subgroups 10 and 11 shall be guaranteed to the limits specified in table I for all lots not specifically tested. Subgroup 9 shall be tested with every lot.

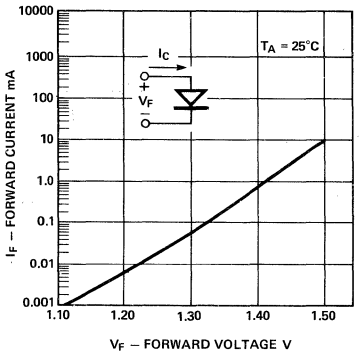
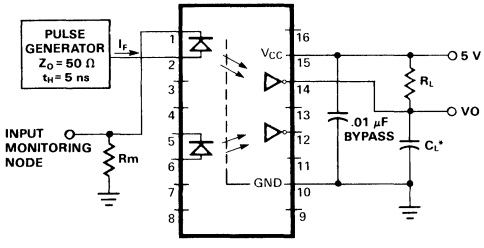


Figure 1. Input Diode Forward Current vs. Forward Voltage



*C_1 INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

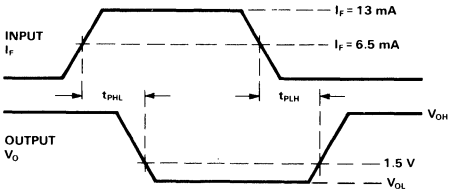


Figure 2. Test Circuit for t_{PHL} and t_{PLH}*

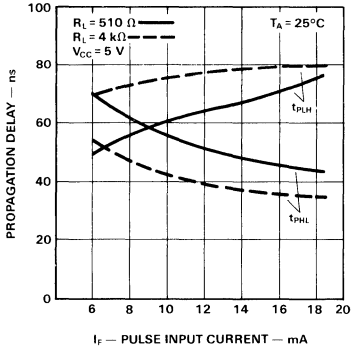
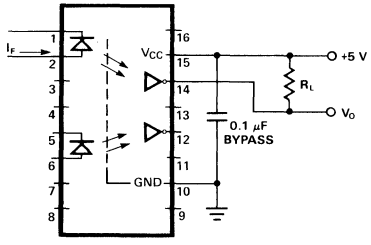


Figure 3. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}



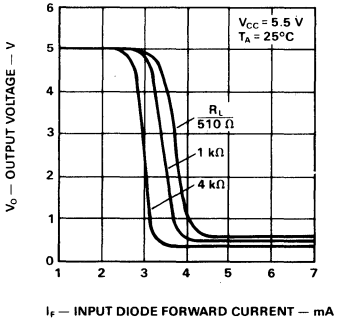


Figure 4. Input-Output Characteristics

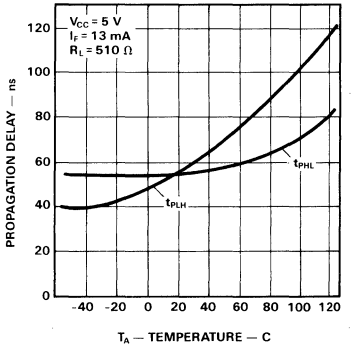


Figure 5. Propagation Delay vs. Temperature

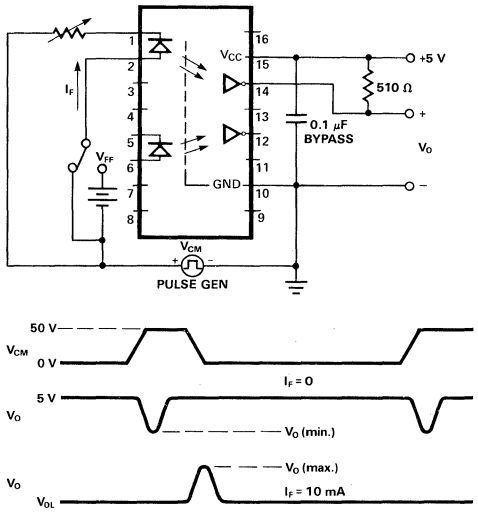


Figure 6. Typical Common Mode Rejection Characteristics/Circuit

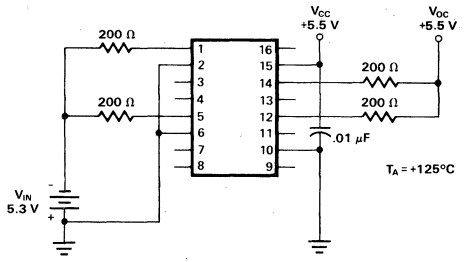


Figure 7. Operating Circuit for Burn-In and Steady State Life Tests

SMD 8102801EC and MIL-STD-883 Class B Test Program

Hewlett-Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC drawing 81028 for an H.P. Optocoupler from the same generic family using the same manufacturing process, design rules and elements of the same microcircuit group.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883.

6N134/883B Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration – Condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C, and D.
- Group A – See Electrical Characteristics Table.
- Group B – No change.
- Group C – No change.
- Group D – Constant Acceleration – Condition A not E.

Part Numbering System

Commercial Product	Class B Product	SMD Product
6N134	6N134/883B	8102801EC

For more information call:

United States: 1-800-752-0900*

Or write:
Hewlett-Packard Components
Customer Information Center
Building 49 AV
19310 Pruneridge Avenue
Cupertino, California 95014

Canada: (416) 678-9430*

Europe: (49) 7031/14-0*

Far East: (65) 271-9444*

Japan: (81) 03-331-6111*

Elsewhere in the world: (415) 857-5027*

*Or call your local HP sales office listed in your telephone directory. Ask for a Components representative.

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HEWLETT PACKARD

High CMR High Speed Hermetically Sealed Optocouplers

Technical Data

HCPL-5600
HCPL-5601 (883B)
HCPL-5630
HCPL-5631 (883B)
(8-pin Dual In-Line Package)
HCPL-6630
HCPL-6631 (883B)
(20 Terminal Leadless Chip Carrier)

Features

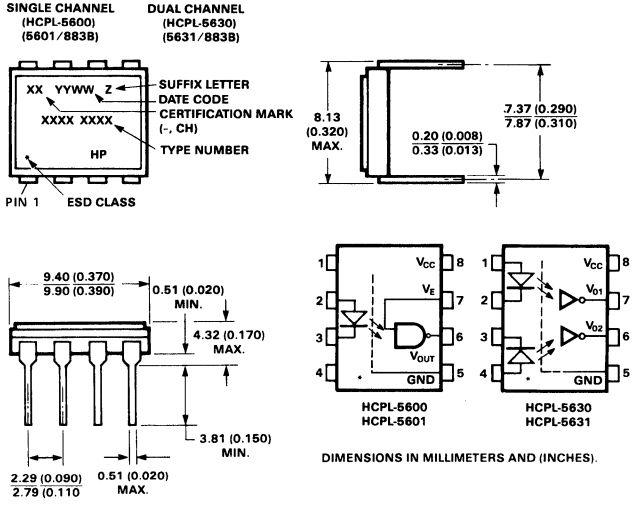
- **Manufactured and Tested on a MIL-STD-1772 Certified Line**
- **QML-MIL-H-38534**
- **Performance Guaranteed Over -55°C to +125°C Ambient Temperature Range**
- **MIL-STD-883 Class B Testing**
- **High Speed: 10M Bit/s**
- **Internal Shield for High CMR**
- **Open Collector Outputs**
- **1500 Vdc Withstand Test Voltage**
- **High Radiation Immunity**
- **6N134, 6N137, HCPL-2601, HCPL-2630/31 Function Compatibility**

Applications

- **Military/High Reliability Systems**
- **Isolated Input Line Receiver**
- **Isolated Output Line Driver**
- **System Test Equipment Isolation**
- **Digital Logic Ground Isolation**
- **Computer-Peripheral Interface**
- **Level Shifting**
- **Vehicle Command/Control Isolation**

Outline Drawings

8-pin Ceramic Dual In-Line Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

Description

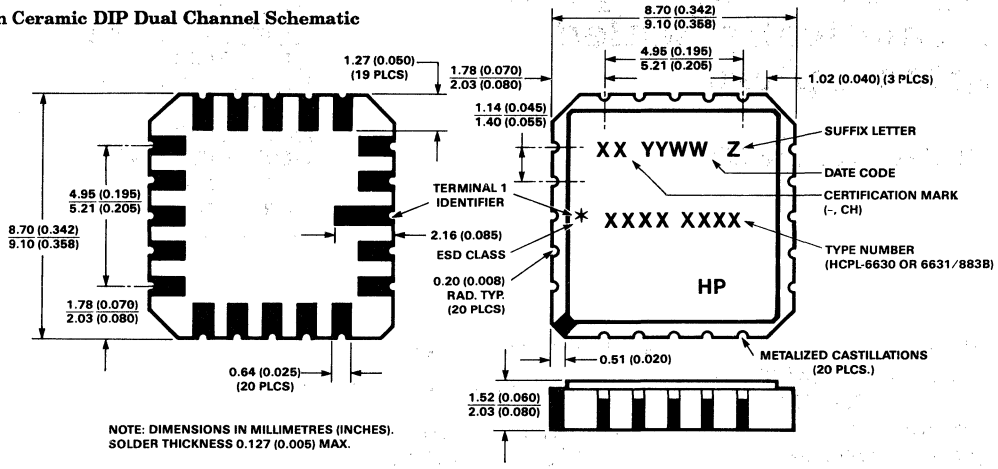
These units are single and dual channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product or with full MIL-STD-883 Class Level B testing. All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

The HCPL-5600, 5601, 5630 and 5631 are in 8 Pin ceramic DIPs configured as either single or dual channel devices. The standard products are HCPL-5600 and HCPL-5630. The products with full MIL-STD-883 Class Level B testing are HCPL-5601 and HCPL-5631.

HERMETIC OPTOCOUPLERS

Outline Drawings

8 Pin Ceramic DIP Dual Channel Schematic

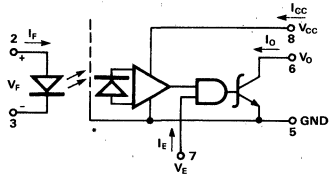


NOTE: DIMENSIONS IN MILLIMETRES (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

The HCPL-6630 and HCPL-6631 parts are in twenty terminal hermetic, ceramic, leadless chip carriers. The standard part is HCPL-6630. The product with full MIL-STD-883 Class Level B testing is HCPL-6631. These dual channel devices are configured and function as two independent single channels. Devices are delivered with solder dipped terminals as a standard feature. Units may also be purchased with gold plated terminals.

Each channel contains a light emitting diode optically coupled to an inverting gate providing 1500 Vdc electrical isolation between input and output. The output of the detector is an open collector schottky clamped transistor. Internal shields provide a guaranteed common mode transient immunity specification of 1000 V/μs at VCM = 50 V. Selection for higher CMR values are available by special request. Contact your local HP field sales engineer for ordering information.

8 Pin Ceramic DIP



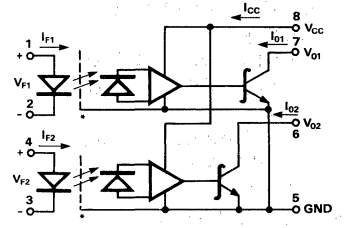
NOTE:
A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5.

SEE NOTE 10.

TRUTH TABLE
(POSITIVE LOGIC)

INPUT	ENABLE	OUTPUT
H (on)	H	L
L (off)	H	H
H (on)	L	H
L (off)	L	H

8 Pin Ceramic DIP

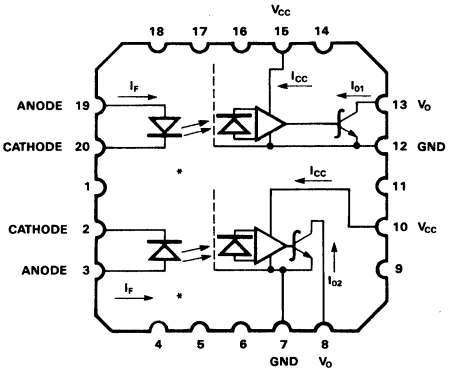


NOTE:
A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5.

This unique design provides maximum D.C. and A.C. circuit isolation while achieving TTL circuit compatibility. The optocoupler operational parameters are guaranteed from -55°C to +125°C, such that a minimum input current of 10 mA per channel will sink a six gate fanout (10 mA) at the output with 4.5 to 5.5 V V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 55 nsec.

External to the unit, a 0.01 μF bypass capacitor must be connected between V_{CC} and ground. A capacitor immediately adjacent to each optocoupler is necessary. The power supply bus for the optocoupler(s) should be separate from the bus for any active loads, otherwise a larger value of the bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.

20 Terminal Ceramic Leadless Chip Carrier Schematic



NOTE:
A .01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN TERMINALS 7 AND 10 AND BETWEEN 12 AND 15.

TRUTH TABLE (POSITIVE LOGIC)

INPUT	OUTPUT
H (on)	L
L (off)	H

*DETECTOR IC INTERNAL ELECTRICAL SHIELD

Recommended Operating Conditions

Parameter	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	12.5†	16	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		6	

Single Channel Product Only (see note 10)

High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V

† 12.5 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 10 mA or less.

Absolute Maximum Ratings

(No derating required up to +125° C)

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Junction Temperature ..... 175°C
Lead Solder Temperature ..... 260°C for 10s
Peak Foward Input Current
(each channel) ..... 40 mA (≤ 1 ms Duration)
Average Input Foward Current
(each channel) ..... 20 mA
Input Power Dissipation
(each channel) ..... 35 mW
Reverse Input Voltage
(each channel) ..... 5 V
Supply Voltage - V_{CC} .... 7 V (1 minute maximum)
Output Current, I_O (each channel) ..... 25 mA
Output Power Dissipation
(each channel) ..... 40 mW
Output Voltage, V_O (each channel) ..... 7 V
Total Package Power Dissipation ..... 350 mW

Single Channel Product Only

Enable Input Voltage - V_E ..... 5.5 V
ESD Classification HCPL-5600/01 ..... Class 1
HCPL-5630/31 and 6630/31
(MIL-STD-883, Method 3015) ..... Class 3

Electrical Characteristics T_A = -55°C to +125°C, unless otherwise specified

Parameter		Sym.	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
High Level Output Current		I_{OH}		20	250	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 µA		3	1
Low Level Output Voltage		V_{OL}		0.3	0.6	V	V_{CC} = 5.5 V, I_F = 10 mA I_{OL} (Sinking) = 10 mA		1	1,9
Logic High Supply Current	Single Channel	I_{CCH}		9	14	mA	V_{CC} = 5.5 V, I_F = 0			1
	Dual Channel			18	28	mA	V_{CC} = 5.5 V, I_F = 0			6
Logic Low Supply Current	Single Channel	I_{CCL}		13	18	mA	V_{CC} = 5.5 V, I_F = 20 mA			1
	Dual Channel			26	36	mA	V_{CC} = 5.5 V, I_F = 20 mA			6
Input Forward Voltage		V_F		1.5	1.9	V	I_F = 20 mA		2	1
Input Reverse Breakdown Voltage		BV_R	5			V	I_R = 10 µA			1
Input-Output Leakage Current		I_{I-O}			1.0	µA	V_{I-O} = 1500 Vdc Relative Humidity = 45% T_A = 25°C, t = 5 s			2,8
Propagation Delay Time to High Output Level		t_{PLH}		60	100	ns	T_A = 25°C	R_L = 510 Ω, C_L = 50 pF, I_F = 13 mA, V_{CC} = 5 V	4,5	1,5
					140		-55 to +125°C			
Propagation Delay Time to Low Output Level		t_{PHL}		55	100	ns	T_A = 25°C			
					120		-55 to +125°C			
Common Mode Transient Immunity at High Output Level		$\|CM_H\|$	1000	>10000		V/µs	V_{CM} = 50 V (peak), T_A = 25°C, V_O (min.) = 2 V, R_L = 510 Ω, I_F = 0 mA		8	1, 7
Common Mode Transient Immunity at High Output Level		$\|CM_L\|$	1000	>10000		V/µs	V_{CM} = 50 V (peak), T_A = 25°C, V_O (min.) = 0.8 V, R_L = 510 Ω, I_F = 10 mA		8	1, 7

Single Channel Product Only

Low Level Enable Current	I_{EL}		-1.45	-2.0	mA	V_{CC} = 5.5 V, V_E = 0.5 V		
High Level Enable Voltage	V_{EH}	2.0			V			10
Low Level Enable Voltage	V_{EL}			0.8	V			

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics $T_A = 25°C$, $V_{CC} = 5$ V

Parameter	Sym.	Typ.	Units	Test Conditions	Fig.	Note
Input Capacitance	C_{IN}	60	pF	$V_F = 0$, f = 1 MHz		1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	-1.5	mV/°C	$I_F = 20$ mA		1
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	$V_{I-O} = 500$ V		2
Capacitance (Input-Output)	C_{I-O}	1.0	pF	f = 1 MHz		1, 3
Output Rise Time (10-90%)	t_r	35	ns	$R_L = 510\Omega$, $C_L = 50$ pF $I_F = 13$ mA		1
Output Fall Time (90-10%)	t_f	35	ns			

Single Channel Product Only

Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	35	ns	$R_L = 510\Omega$, $C_L = 50$ pF, $I_F = 13$ mA, $V_{EH} = 3$ V, $V_{EL} = 0$ V	6,7	1,11
Propagation Delay time of Enable from V_{EL} to V_{EH}	t_{EHL}	35	ns		6,7	1,12

Dual Channel Products Only

Input-Input Leakage Current	I_{I-I}	0.5	nA	Relative Humidity = 45% $V_{I-I} = 500$ V, t = 5 s		4
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	$V_{I-I} = 500$ V		4
Capacitance (Input-Input)	C_{I-I}	0.55	pF	f = 1 MHz		4

Notes:

1. Each channel of a dual channel device.
2. Device considered a two-terminal device: for 8 pin DIP, pins 1 through 4 are shorted together, and pins 5 through 8 are shorted together; for LCC, terminals 19, 20, 1, 2, 3 are shorted together, and terminals 7 through 15 are shorted together.
3. Measured between each input pair shorted together and all outputs for that channel shorted together.
4. Measured between adjacent input pairs shorted together; i.e., for 8 pin DIP, between pins 1 and 2 shorted together and pins 3 and 4 shorted together; for LCC, between terminals 19 and 20 shorted together, and terminals 2 and 3 shorted together.
5. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. The HCPL-6630 and HCPL-6631 dual channel parts function as two independent single channel units. Use the single channel parameter limits.
7. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8$ V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0$ V).
8. This is a momentary withstand test, not an operating condition.
9. It is essential that a bypass capacitor (.01 to 0.1μF, ceramic) be connected from V_{CC} to ground. Total lead length between both ends of this external capacitor and the isolator pins should not exceed 20mm.
10. No external pull up is required for a high logic state on the enable input.
11. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
12. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.

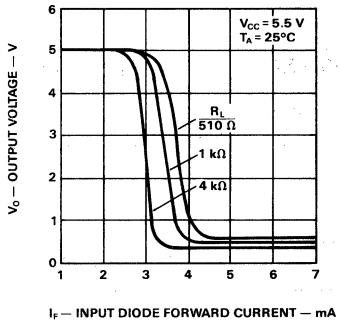


Figure 1. Input-Output Characteristics.

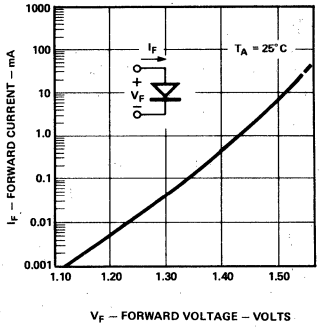


Figure 2. Input Diode Forward Characteristic.

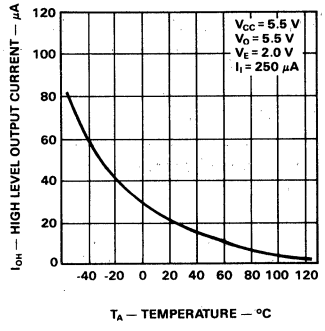


Figure 3. High Level Output Current vs. Temperature.

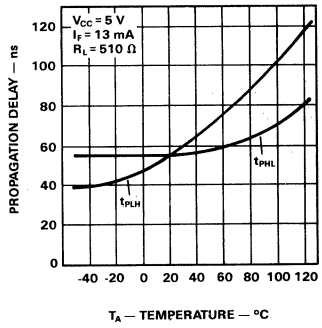
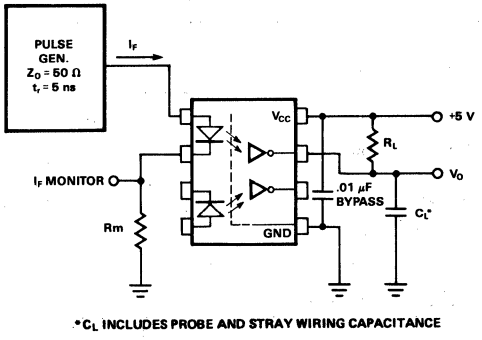


Figure 4. Propagation Delay vs. Temperature.



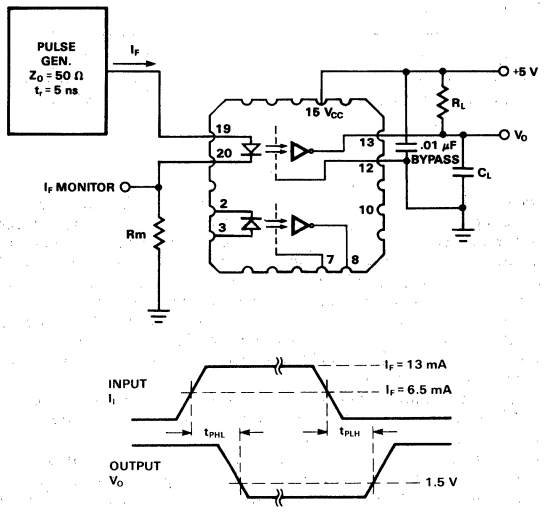


Figure 5. Test Circuit for t_{PHL} and t_{PLH}.

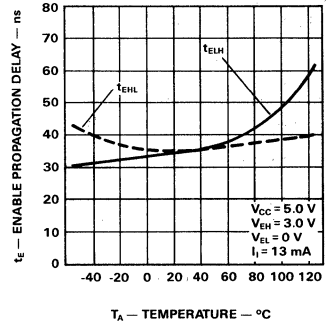
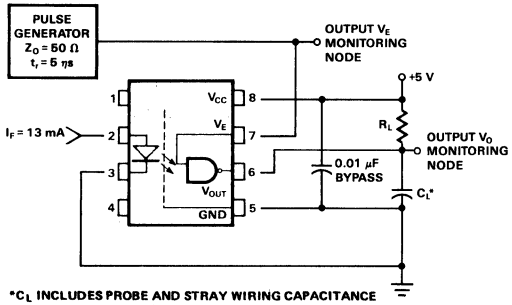


Figure 6. Enable Propagation Delay vs. Temperature.



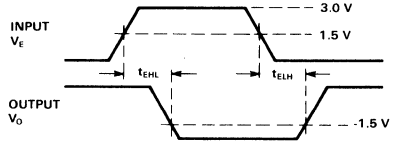
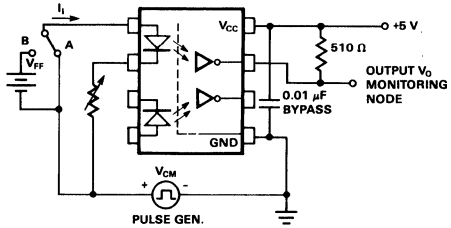


Figure 7. Test Circuit for t_{EHL} and t_{ELH}.



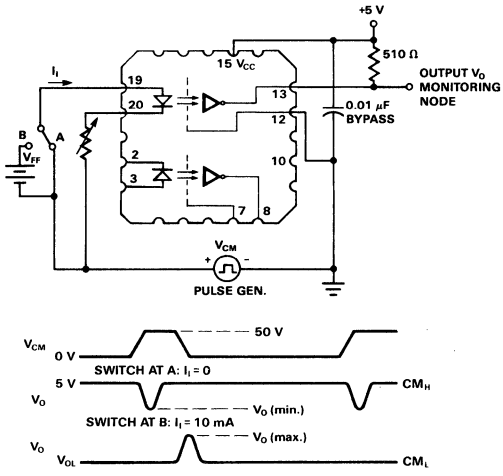


Figure 8. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

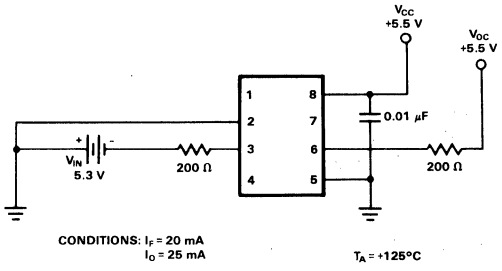


Figure 9. Single Channel Operating Circuit for Burn-In and Steady State Life Tests.

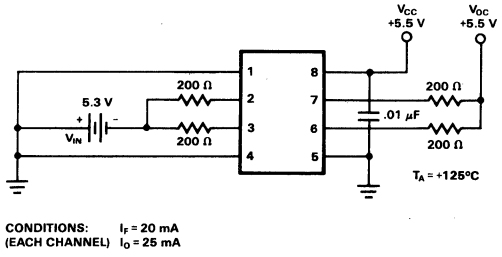


Figure 10. Dual Channel Operating Circuit for Burn-In and Steady-State Life Tests.

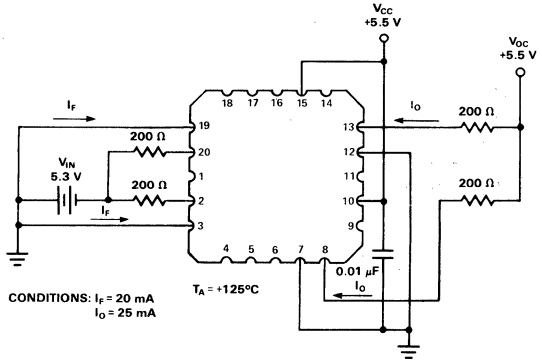


Figure 11. Operating Circuit for Burn-In and Steady State Life Tests.

MIL-STD-883 Class B Test Program

Hewlett-Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC drawing 81028 for the equivalent H.P. Optocoupler.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883.

Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration - Condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C, and D.
Group A - See table for specific electrical tests.
Group B - No change.
Group C - No change.
Group D - Constant Acceleration - Condition A not E.

Part Numbering System

Commercial Product	Class B Product
HCPL-5600	HCPL-5601
HCPL-5630	HCPL-5631
HCPL-6630	HCPL-6631

Group A – Electrical Tests Quantity/Accept No. = 116/0

Single and Dual Channel Product	Single Channel Product
Subgroup 1 *Static tests at T_A = 25°C – V_{OL}, BV_R, I_{OH}, I_{CCL}, I_{CCH}, V_F, I_{I-O}	I_{EL}, V_{EH}, V_{EL}
Subgroup 2 *Static tests at T_A = +125°C – V_{OL}, BV_R, I_{OH}, I_{CCL}, I_{CCH}, V_F	I_{EL}, V_{EH}, V_{EL}
Subgroup 3 *Static tests at T_A = -55°C – V_{OL}, BV_R, I_{OH}, I_{CCL}, I_{CCH}, V_F	I_{EL}, V_{EH}, V_{EL}
Subgroup 4, 5, 6, 7, 8A and 8B These subgroups are not applicable to this device type.	
Subgroup 9 *Switching tests at T_A = 25°C – t_{PHL}, t_{PLH} $\lvert CM_H \rvert$, $\lvert CM_L \rvert$	
Subgroup 10 *Switching tests at T_A = +125°C – t_{PHL}, t_{PLH}	
Subgroup 11 *Switching tests at T_A = -55°C – t_{PHL}, t_{PLH}	

*Limits and conditions per Electrical Characteristics.

HEWLETT PACKARD

Dual Channel Line Receiver Hermetic Optocoupler

Technical Data

HCPL-1930
HCPL-1931 (883B)
5962-8957201EC

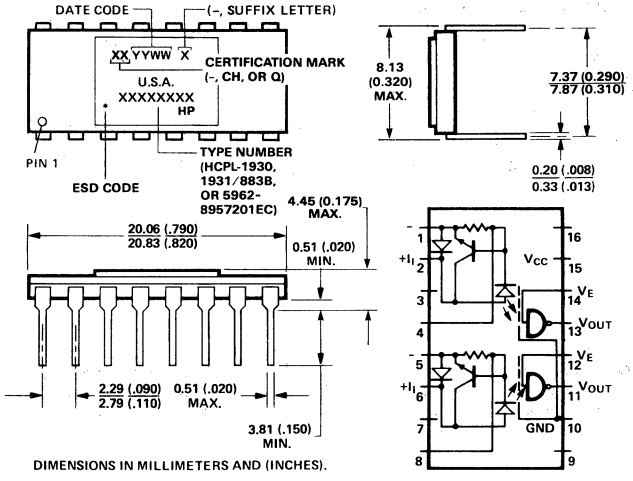
Features

- **DESC Standard Military Drawing**
- **Manufactured and Tested on a MIL-STD-1772 Certified Line**
- **QML-MIL-H-38534**
- **Hermetically Sealed 8-pin Dual In-Line Package**
- **Performance Guaranteed Over -55°C to +125°C Ambient Temperature Range**
- **MIL-STD-883 Class B Testing**
- **High Speed – 10 Mb/s**
- **Accepts a Broad Range of Drive Conditions**
- **Adaptive Line Termination Included**
- **Internal Shield Provides Excellent Common Mode Rejection**
- **External Base Lead Allows "LED Peaking" and LED Current Adjustment**
- **1500 Vdc Withstand Test Voltage**
- **High Radiation Immunity**
- **HCPL-2602 Function Compatibility**

Description

The HCPL-1930, HCPL-1931, and 5962-8957201EC units are dual channel, hermetically sealed, high CMR, line receiver optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product (HCPL-1930), with full MIL-STD-883 Class Level B testing (HCPL-1931), or from the DESC Standard Military Drawing (SMD) 5962-89572 as (5962-8957201EC). All three products are sixteen pin hermetic dual in-line packages. They are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in

Outline Drawing



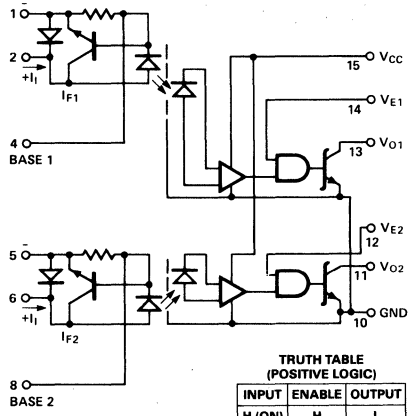
HERMETIC OPTOCOUPLERS

the SMD part #, or by adding option #200 to the part number for non-DESC parts.

Each unit contains two independent channels, consisting of a GaAsP light emitting diode, an input current regulator, and an integrated high gain photon detector. The input regulator serves as a line termination for line receiver applications. It clamps the line voltage and regulates the LED current so line reflections do not interfere with circuit performance. The regulator allows a typical LED current of 12.5 mA before it starts to shunt excess current. The output of the detector IC is an open collector Schottky clamped transistor. An enable input gates the detector. The internal detector shield provides a guaranteed common mode transient immunity specification of +1000 V/μsec.

DC specifications are compatible with TTL logic and are guaranteed from -55°C to +125°C allowing trouble-free interfacing with digital logic circuits. An input current of 10 mA will sink a six gate fan-out (TTL) at the output with a typical propagation delay from input to output of only 45 nsec.

Schematic



A 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 10 AND 15 (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

INPUT	ENABLE	OUTPUT
H (ON)	H	L
L (OFF)	H	H
H (ON)	L	H
L (OFF)	L	H

The test program performed on the 5962-8957201EC is in compliance with DESC (SMD) 5962-89572. The electrical characteristics table shows Group A Subgroup testing requirements from this drawing.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Applications

- **Military/High Reliability Systems**
- **Isolated Line Receiver**
- **Simplex/Multiplex Data Transmission**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Current Sensing**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{IL}	0	250	μA
Input Current, High Level*	I_{IH}	12.5	60	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (TTL Load)	N		6	
Operating Temperature	T_A	-55	125	°C

*12.5 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 10 mA or less.

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10 s
1.6 mm below seating plane
Forward Input Current – I_I (each channel) ..... 60 mA[2]
Reverse Input Current ..... 60 mA
Supply Voltage – V_{CC} ..... 7 V 1 Minute Maximum
Enable Input Voltage – V_E (each channel) ..... 5.5 V
Not to exceed V_{CC} by more than 500 mV
Output Collector Current – I_O (each channel) ..... 25 mA
Output Collector Power Dissipation (each channel) ..... 40 mW
Output Collector Voltage – V_O (each channel) ..... 7 V
Total Package Power Dissipation ..... 564 mW
Total Input Power Dissipation (each channel) ..... 168 mW

Electrical Specifications

Parameter	Symbol	Test Conditions	Group A Sub-groups[15]	Limits			Units	Fig.	Note
				Min.	Typ.*	Max.			
High Level Output Current	I_{OH}	V_{CC} = 5.5 V, V_O = 5.5 V I_I = 250 µA, V_E = 2.0 V	1, 2, 3		20	250	µA	3	3
Low Level Output Voltage	V_{OL}	V_{CC} = 5.5 V; I_I = 10 mA V_E = 2.0 V, I_{OL} (Sinking) = 10 mA	1, 2, 3		0.3	0.6	V	1	3
Input Voltage	V_I	I_I = 10 mA	1, 2, 3		2.2	2.6	V	2	3
		I_I = 60 mA			2.35	2.75			
Input Reverse Voltage	V_R	I_R = 10 mA	1, 2, 3		0.8	1.10	V		3
Low Level Enable Current	I_{EL}	V_{CC} = 5.5 V, V_E = 0.5 V	1, 2, 3		-1.45	-2.0	mA		3
High Level Enable Voltage	V_{EH}		1, 2, 3	2.0			V		3, 12
Low Level Enable Voltage	V_{EL}		1, 2, 3			0.8	V		3
High Level Supply Current	I_{CCH}	V_{CC} = 5.5 V; I_I = 0, V_E = 0.5 V both channels	1, 2, 3		21	28	mA		
Low Level Supply Current	I_{CCL}	V_{CC} = 5.5 V; I_I = 60 mA, V_E = 0.5 V both channels	1, 2, 3		27	36	mA		
Input-Output Insulation Leakage Current	I_{I-O}	Relative Humidity = 45% t = 5 s, V_{I-O} = 1500 Vdc	1			1	µA		4
Propagation Delay Time to High Output Level	t_{PLH}	R_L = 510 Ω; C_L = 50 pF, I_I = 13 mA	9		55	100	ns	4, 5	3, 5
			10, 11			140			
Propagation Delay Time to Low Output Level	t_{PHL}	R_L = 510 Ω; C_L = 50 pF, I_I = 13 mA	9		60	100	ns	4, 5	3, 6
			10, 11			120			
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	V_{CM} = 50 V (peak), V_O (min.) = 2 V, R_L = 510 Ω; I_I = 0 mA	9, 10, 11	1000	10,000		V/µs	8, 9	3, 9, 14
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	V_{CM} = 50 V (peak), V_O (max.) = 0.8 V, R_L = 510 Ω; I_I = 10 mA	9, 10, 11	1000	10,000		V/µs	8, 9	3, 10, 14

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Specifications

$T_A = 25°C$, $V_{CC} = 5$ V

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Note
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	$V_{I-O} = 500$ V dc		3, 13
Capacitance (Input-Output)	C_{I-O}	1.7	pF	f = 1 MHz		3, 13
Input-Input Insulation Leakage Current	I_{I-I}	0.5	nA	45% Relative Humidity, $V_{I-I} = 500$ Vdc, t = 5 s		11
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	$V_{I-I} = 500$ Vdc		11
Capacitance (Input-Input)	C_{I-I}	0.55	pF	f = 1 MHz		11
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	35	ns	$R_L = 510$ Ω, $C_L = 15$ pF, $I_I = 13$ mA, $V_{EH} = 3$ V, $V_{EL} = 0$ V	6, 7	3, 7
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	35	ns		6, 7	3, 8
Output Rise Time (10-90%)	t_r	30	ns	$R_L = 510$ Ω, $C_L = 15$ pF, $I_I = 13$ mA		3
Output Fall Time (90-10%)	t_f	24	ns			3
Input Capacitance	C_I	60	pF	f = 1 MHz, $V_I = 0$, PINS 1 to 2 or 5 to 6		3

Notes:

1. Bypassing of the power supply line is required, with a 0.1 µF ceramic disc capacitor adjacent to each isolator. The power supply bus for the isolators should be separate from the bus for any active loads, otherwise additional bypass capacitance may be needed to suppress regenerative feedback via the power supply.
2. Derate linearly at 1.2 mA/°C above $T_A = 100°C$.
3. Each channel.
4. Device considered a two terminal device: pins 1 through 8 are shorted together, and pins 9 through 16 are shorted together.
5. The t_{PLH} propagation delay is measured form the 6.5 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. The t_{PHL} propagation delay is measured from the 6.5 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
7. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
8. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
9. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state, i.e. $V_{OUT} > 2.0$ V.
10. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state, i.e. $V_{OUT} < 0.8$ V.
11. Measured between adjacent input leads shorted together, i.e. between 1, 2 and 4 shorted together and pins 5, 6 and 8 shorted together.
12. No external pull up is required for a high logic state on the enable input.
13. Measured between pins 1 and 2 or 5 and 6 shorted together, and pins 10 through 15 shorted together.
14. Subgroups 10 and 11 shall be tested as part of device initial characterization and after design and process changes. Subgroup 9 shall be tested with every lot.
15. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and/883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

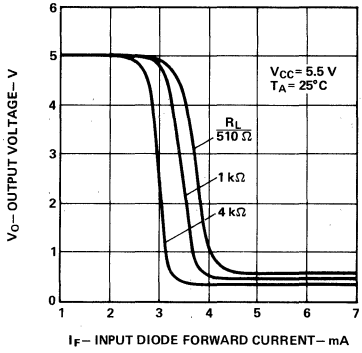


Figure 1. Input-Output Characteristics.

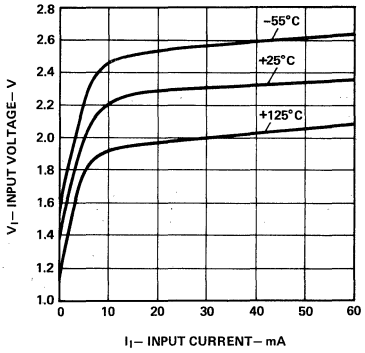


Figure 2. Input Characteristics.

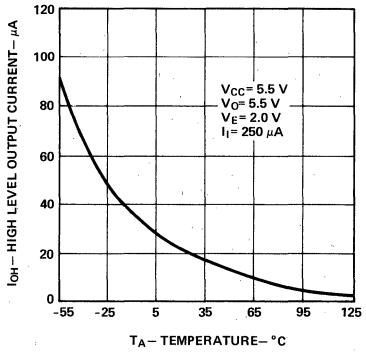


Figure 3. High Level Output Current vs. Temperature.

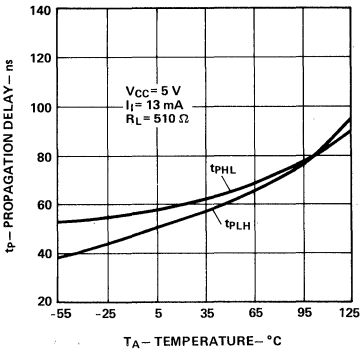


Figure 4. Propagation Delay vs. Temperature.

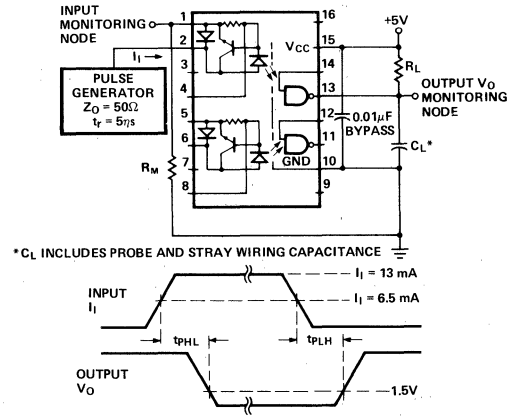


Figure 5. Test Circuit for t_{PHL} and t_{PLH}.

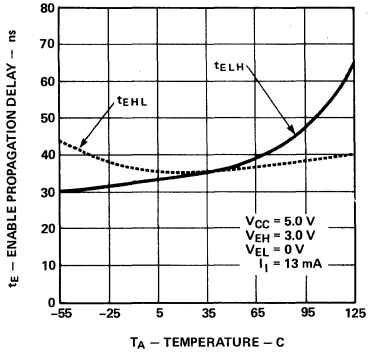


Figure 6. Enable Propagation Delay vs. Temperature.

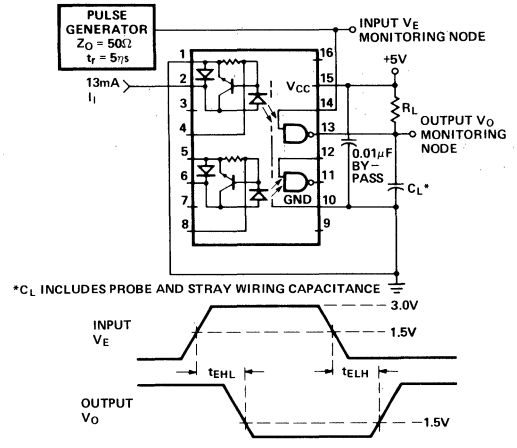


Figure 7. Test Circuit for t_{EHL} and t_{ELH}.

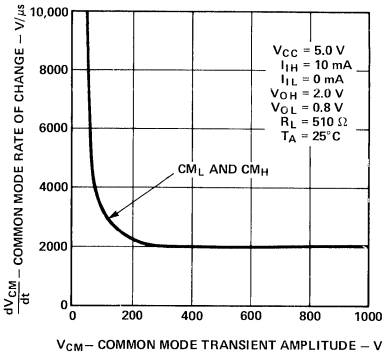


Figure 8. Typical Common Mode Transient Immunity.

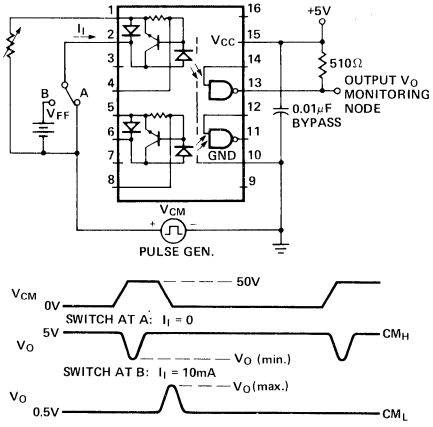


Figure 9. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

SMD 5962-8957201EC and MIL-STD-883 Class B Test Program

Hewlett-Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC SMD 5962-89572 for an H.P. Optocoupler from the same generic family using the same manufacturing process, design rules and elements of the same microcircuit group.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883.

1931/883B Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration – Condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C, and D.
Group A – See Electrical Characteristics Table.
Group B – No change.
Group C – No change.
Group D – Constant Acceleration – Condition A not E.

Part Numbering System

Commercial Product	Class B Product	SMD Product
HCPL-1930	HCPL-1931	5962-8957201EC

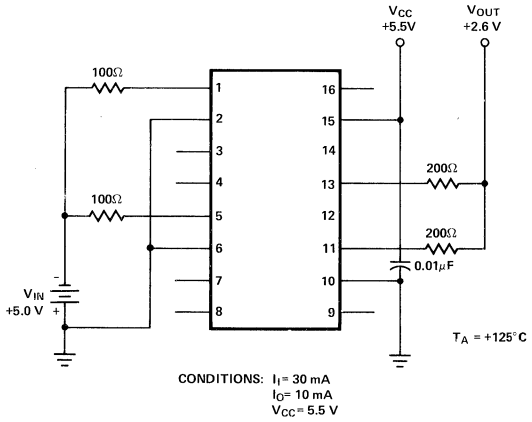
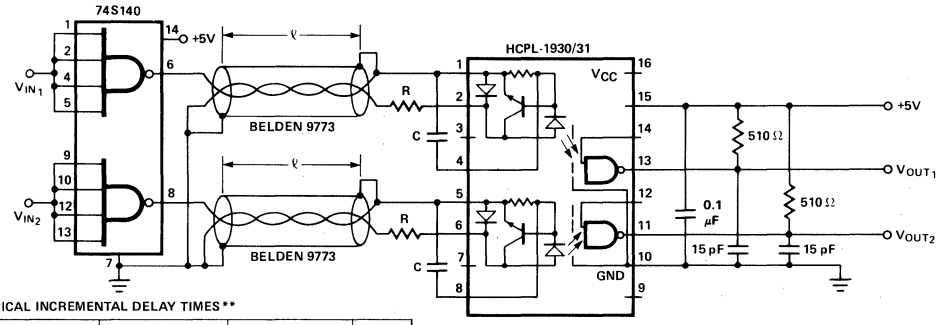


Figure 10. Burn In Circuit.

Application Circuits*

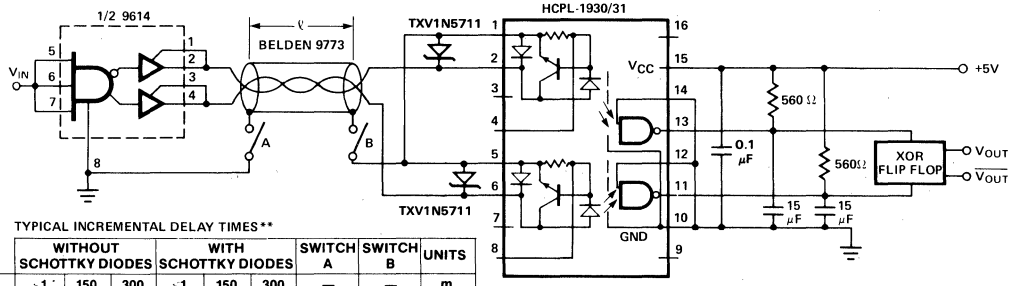


TYPICAL INCREMENTAL DELAY TIMES**

	R = 0, C = OPEN			R =33Ω, C = OPEN			R=33Ω, C = 390pF			UNITS
ℓ	<1	150	300	<1	150	300	<1	150	300	m
t_{PHL}	42	27	121	43	47	171	28	37	146	nsec
t_{PLH}	31	121	296	31	31	71	26	11	46	nsec

PROPAGATION DELAY TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

Figure A_1, Polarity Non-Reversing.

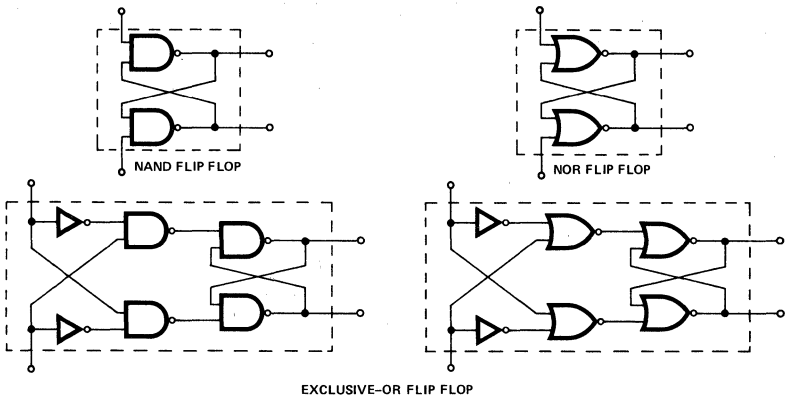


TYPICAL INCREMENTAL DELAY TIMES**

	WITHOUT SCHOTTKY DIODES			WITH SCHOTTKY DIODES			SWITCH A	SWITCH B	UNITS
ℓ	<1	150	300	<1	150	300	—	—	m
tp	112	455	820	78	365	700	OPEN	OPEN	nsec
	52	410	730	54	305	580	OPEN	CLOSED	nsec
	52	410	490	54	395	490	CLOSED	CLOSED	nsec

PROPAGATION DELAY TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS
USING 1/3 74LS04 INVERTERS AND 74LS00 QUAD NAND

Figure A_2. Polarity Reversing, Split Phase.



NAND flip flop tolerates simultaneously HIGH inputs; NOR flip flop tolerates simultaneously LOW inputs; EXCLUSIVE-OR flip flop tolerates simultaneously HIGH OR LOW inputs without causing either of the outputs to change.

*FOR A DESCRIPTION OF THESE CIRCUITS SEE HCPL-2602 DATA SHEET.

Figure A_3. Flop-Flop Configurations.

HEWLETT PACKARD

Hermetically Sealed Four Channel Low Input Current Optocoupler

Technical Data

6N140A
6N140A/883B
8302401EC

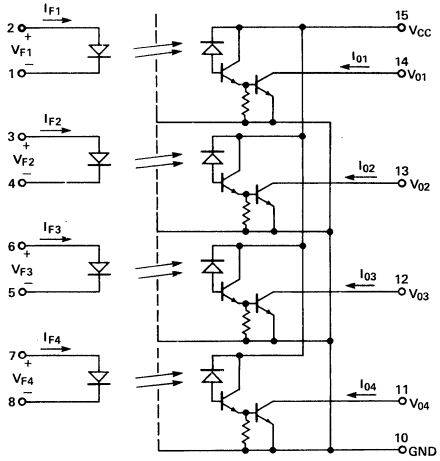
Features

- DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534
- Hermetically Sealed 8-Pin Dual In-Line Package
- Performance Guaranteed Over -55°C to +125°C Ambient Temperature Range
- MIL-STD-883 Class B Testing
- Internal Shield for Higher CMR
- Low Input Current Requirement: 0.5 mA
- High Current Transfer Ratio: 1500% Typical
- Low Output Saturation Voltage: 0.1 V Typical
- Low Power Consumption
- 1500 VDC Withstand Test Voltage
- High Radiation Immunity
- 6N138/9, HCPL-57XX, 67XX Function Compatibility

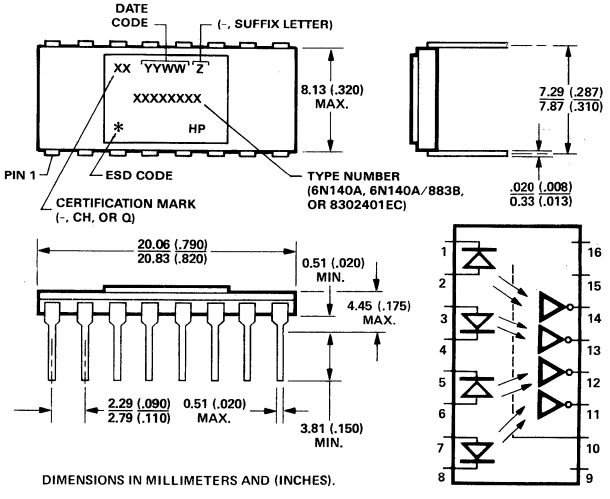
Applications

- Military/High Reliability Systems
- Isolated Input Line Receiver
- System Test Equipment Isolation
- Digital Logic Ground Isolation
- EIA RS-232C Line Receiver
- Microprocessor System Interface
- Current Loop Receiver
- Level Shifting
- Process Control Input/ Output Isolation

Schematic



Outline Drawing



DIMENSIONS IN MILLIMETERS AND (INCHES).

HERMETIC OPTOCOUPLERS

Description

The 6N140A is an EIA registered hybrid microcircuit which is capable of operation over the full military temperature range from -55°C to +125°C and is electrically and functionally identical to the 6N140 part. It is an advanced replacement unit for the 6N140. The better performance results from an improved integrated bypass resistor which shunts photodiode and first stage leakage currents. All products within this family have this advanced feature and can be purchased as either a standard product (6N140A), with full MIL-STD-883 Class Level B testing (6N140A/883B) or as parts compliant to DESC Drawing 83024 as (8302401EC). All parts are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the DESC part number, or by adding Option 200 to the part number for non-DESC parts.

All three products are in sixteen-pin hermetic dual in-line packages. Each part contains four GaAsP light emitting diodes, each of which is optically coupled to a corresponding integrated high gain photon detector. The high gain output stage features an open collector output providing both lower output saturation voltage and higher speed operation than possible with conventional photodarlington type optocouplers. Also, the separate V_{CC} pin can be strobed low as an output disable or operated with supply voltages as low as 2.0 V without adversely affecting the parametric performance.

The high current transfer ratio at very low input currents permits circuit designs in which adequate margin can be allowed for the effects of CTR degradation over time.

These products have a 300% minimum CTR at an input current of only 0.5 mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing or RS-232C data transmission systems. Compatibility with high voltage CMOS logic systems is assured by the 18 V V_{CC} and by the guaranteed maximum output leakage (IOH) at 18 V. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor optocouplers.

The test program performed on the 8302401EC is in compliance with DESC Drawing 83024. The electrical characteristics table shows Group A Subgroup testing requirements from this drawing.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Voltage, Low Level (Each Channel)	$V_{F,OFF}$		0.8	V
Input Current, High Level (Each Channel)	$I_{F,ON}$	0.5	5	mA
Supply Voltage	V_{CC}	2.0	18	V

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Output Current, I_O (each channel) ..... 40 mA
Output Voltage, V_O (each channel) ..... -0.5 to 20 V[1]
Supply Voltage ,V_{CC} ..... -0.5 to 20 V[1]
Output Power Dissipation (each channel) ..... 50 mW[2]
Peak Input Current (each channel, ≤ 1 ms duration) ..... 20 mA
Average Input Current, I_F (each channel) ..... 10 mA[3]
Reverse Input Voltage, V_R (each channel) ..... 5 V

Electrical Characteristics

Parameter	Sym.	Test Conditions	Group A[14] Sub-groups	Limits Min.	Limits Typ.**	Limits Max.	Unit	Fig.	Note
Current Transfer Ratio	$h_{F(CTR)}$*	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1, 2, 3	300	1500		%	3	4, 5
		I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1, 2, 3	300	1000		%		4, 5
		I_F = 5 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1, 2, 3	200	500		%		4, 5
Logic Low Output Voltage	V_{OL}	I_F = 0.5 mA, I_{OL} = 1.5 mA, V_{CC} = 4.5 V	1, 2, 3		0.1	0.4	V	2	4
		I_F = 5 mA, I_{OL} = 10 mA, V_{CC} = 4.5 V	1, 2, 3		0.2	0.4	V		4
Logic High Output Current	I_{OH}*	I_F = 2 µA	1, 2, 3		0.001	250	µA		4
	I_{OHX}	V_O = V_{CC} = 18 V	1, 2, 3			250	µA		4, 6
Logic Low Supply Current	I_{CCL}*	I_{F1} = I_{F2} = I_{F3} = I_{F4} = 1.6 mA, V_{CC} = 18 V	1, 2, 3		1.7	4	mA		
Logic High Supply Current	I_{CCH}*	I_{F1} = I_{F2} = I_{F3} = I_{F4} = 0 mA, V_{CC} = 18 V	1, 2, 3		0.001	40	µA		
Input Forward Voltage	V_F*	I_F = 1.6 mA	1, 2		1.44	1.7	V	1	4
			3			1.8	V		4
Input Reverse Breakdown Voltage	BV_R*	I_R = 10 µA	1, 2, 3	5			V		4
Input-Output Insulation Leakage Current	I_{I-O}*	45% Relative Humidity, T = 25°C, t = 5 s, V_{I-O} = 1500 VDC	1			1.0	µA		7, 12
Capacitance Between Input-Output	C_{I-O}	f = 1 MHz, T_C = 25°C	4			4	pF		4, 8
Propagation Delay Time To Logic High At Output	t_{PLH}*	I_F = 0.5 mA, R_L = 4.7 kΩ, V_{CC} = 5.0 V	9, 10, 11		6	60	µs	8	4
		I_F = 5 mA, R_L = 680 Ω, V_{CC} = 5.0 V	9		4	20	µs		4
			10, 11			30	µs		4
Propagation Delay Time To Logic Low At Output	t_{PHL}*	I_F = 0.5 mA, R_L = 4.7 kΩ, V_{CC} = 5.0 V	9, 10, 11		30	100	µs	8	4
		I_F = 5 mA, R_L = 680 Ω, V_{CC} = 5.0 V	9		2	5	µs		4
			10, 11			10	µs		4
Common Mode Transient Immunity At Logic High Level Output	$\|CM_H\|$	I_F = 0, R_L = 1.5 kΩ $\|V_{CM}\|$ = 25 V_{P-P}, V_{CC} = 5.0 V	9, 10, 11	500	1000		V/µs	9	4, 9, 11, 15
Common Mode Transient Immunity At Logic Low Level Output	$\|CM_L\|$	I_F = 1.6 mA, R_L = 1.5 kΩ $\|V_{CM}\|$ = 25 V_{P-P}, V_{CC} = 5.0 V	9, 10, 11	500	1000		V/µs	9	4, 10, 11, 15

*JEDEC Registered Data.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics

T_A = 25°C, V_{CC} = 5 V Each Channel

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 VDC, T_A = 25°C		4, 8
Input-Input Insulation Leakage Current	I_{I-I}		0.5		nA	45% Relative Humidity, V_{I-I} = 500 VDC T_A = 25°C, t = 5 s		13
Resistance (Input-Input)	R_{I-I}		10^{12}		Ω	V_{I-I} = 500 VDC, T_A = 25°C		13
Capacitance (Input-Input)	C_{I-I}		1		pF	f = 1 MHz, T_A = 25°C		13
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$		-1.8		mV/°C	I_F = 1.6 mA		4
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0, T_A = 25°C		4

Notes:

1. Pin 10 should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0 volts, will provide lowest total I_{OH} over temperature.
2. Output power is collector output power plus one fourth of total supply power. Derate at 1.66 mW/°C above 110°C.
3. Derate I_F at 0.33 mA/°C above 110°C.
4. Each channel.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. I_{OHX} is the leakage current resulting from channel to channel optical crosstalk. I_F = 2 μA for channel under test. For all other channels, I_F = 10 mA.
7. Device considered a two-terminal device: Pins 1 through 8 are shorted together and pins 9 through 16 are shorted together.
8. Measured between the LED anode and cathode shorted together and pins 10 through 15 shorted together.
9. CM_H is the maximum tolerable common mode transient to assure that the output will remain in a high logic state (i.e., V_O > 2.0 V).
10. CM_L is the maximum tolerable common mode transient to assure that the output will remain in a low logic state (i.e., V_O < 0.8 V).
11. In applications where dV/dt may exceed 50,000 V μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector ICs from destructively high surge currents. The recommended value is

$$R_{CC} \approx \frac{1\ V}{0.6\ I_F\ (mA)}\ k\Omega$$

12. This is a momentary withstand test, not an operating condition.
13. Measured between adjacent input pairs shorted together, i.e., between pins 1 and 2 shorted together, and pins 3 and 4 shorted together, etc.
14. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
15. Subgroups 10 and 11 shall be tested as part of device initial characterization and after design and process changes. Subgroups 10 and 11 shall be guaranteed to the limits specified in Table I for all lots not specifically tested. Subgroup 9 shall be tested with every lot.

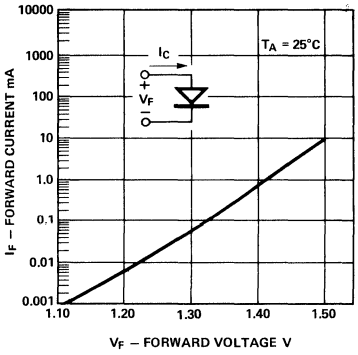


Figure 1. Input Diode Forward Current vs Forward Voltage.

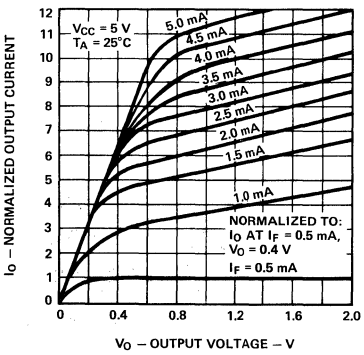


Figure 2. Normalized DC Transfer Characteristics.

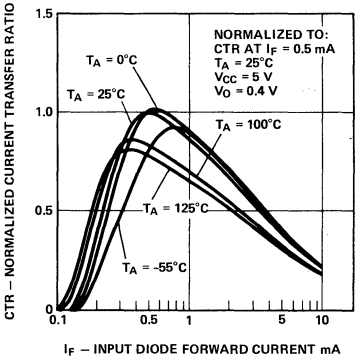


Figure 3. Normalized Current Transfer Ratio vs Input Diode Forward Current.

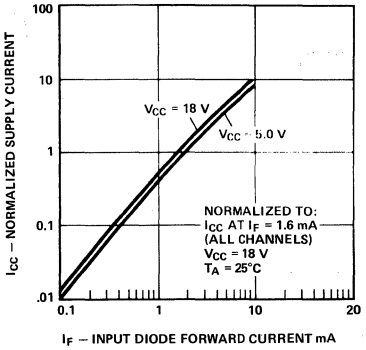


Figure 4. Normalized Supply Current vs Input Diode Forward Current.

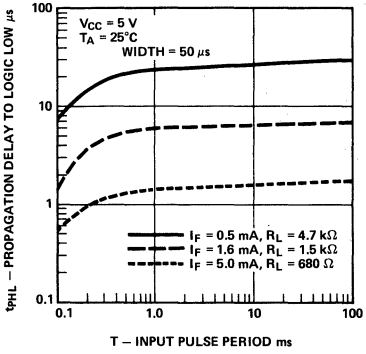


Figure 5. Propagation Delay to Logic Low vs Input Pulse Period.

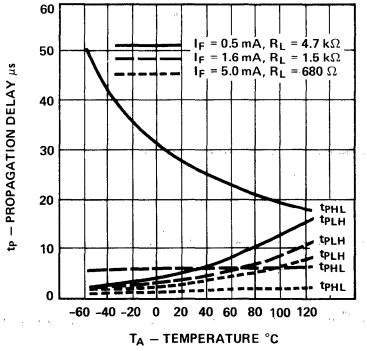


Figure 6. Propagation Delay vs Temperature.

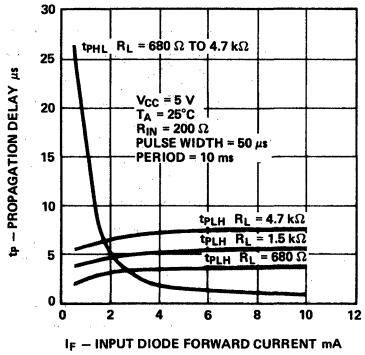


Figure 7. Propagation Delay vs Input Diode Forward Current.

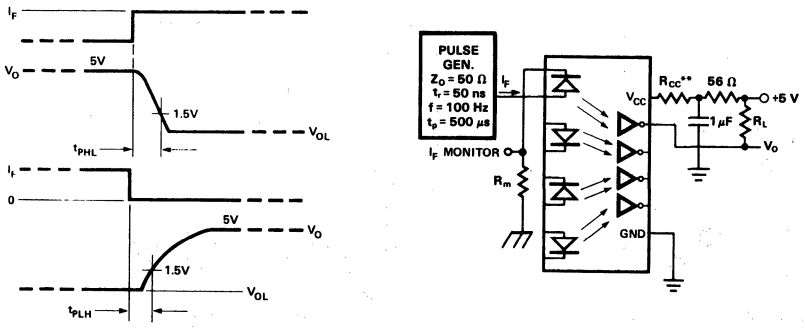


Figure 8. Switching Test Circuit (f, t_p not JEDEC registered).*

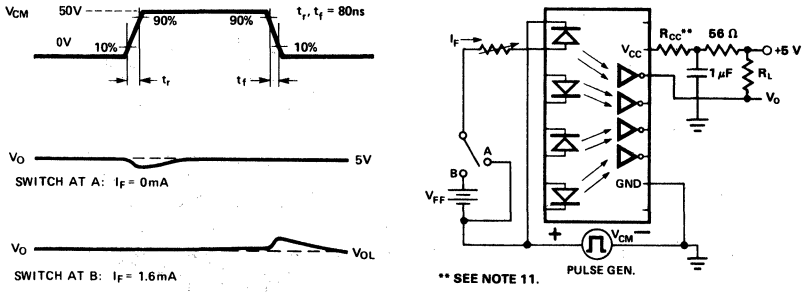


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

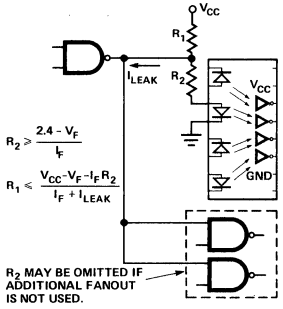


Figure 10. Recommended Drive Circuitry Using TTL Open-Collector Logic.

SMD 8302401EC and MIL-STD-883 Class B Test Program

Hewlett-Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC drawings 83024 for an H.P. Optocoupler from the same generic family using the same manufacturing process, design rules and elements of the same microcircuit group.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883.

6N140A/883B Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration–condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C, and D.

Group A–See Electrical Characteristics Table.
Group B–No change.
Group C–No change.
Group D–Constant Acceleration–Condition A not E.

Part Numbering System

Commercial Product	Class B Product	SMD Product
6N140A	6N140A/883B	8302401EC

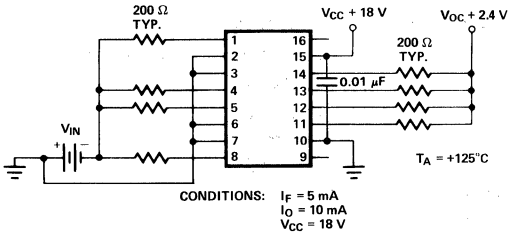


Figure 11. Operating Circuit for Burn-In and Steady State Life Tests.

HEWLETT PACKARD

Low Input Current, High Gain, Hermetically Sealed Optocoupler

Technical Data

8-pin Dual In-Line Package
HCPL-5700
HCPL-5701 (883B)
5962-8981001PC
HCPL-5730
HCPL-5731 (883B)
5962-8978501PC
20 Terminal Leadless Chip Carrier
HCPL-6730
HCPL-6731 (883B)
5962-89785022A

Features

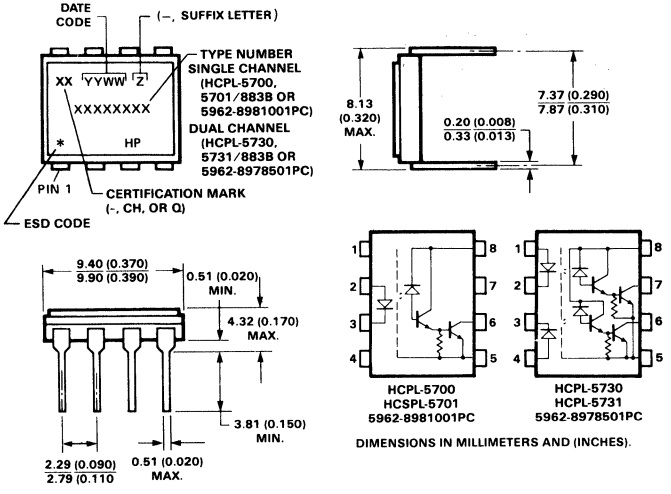
- DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534
- Hermetically Sealed Packages
- Performance Guaranteed Over -55°C to +125°C Ambient Temperature Range
- MIL-STD-883 Class B Testing
- Low Input Current Requirement: 0.5 mA
- High Current Transfer Ratio: 1500% Typical
- Low Output Saturation Voltage: 0.11 V Typical
- 1500 Vdc Withstand Test Voltage
- Low Power Consumption
- High Radiation Immunity
- Function Compatibility with 6N138/9, HCPL-2730/31, and 6N140A
- 2-18 Volt V_{CC} Range

Applications

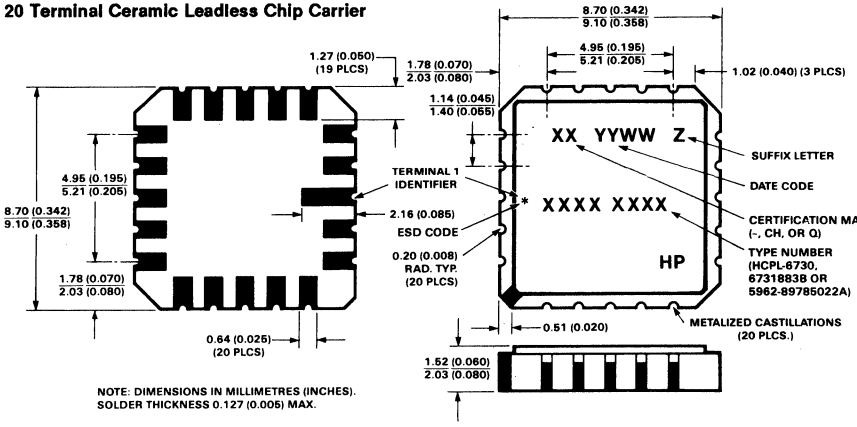
- Military/High Reliability Systems
- Telephone Ring Detection
- Microprocessor System Interface
- EIA RS-232-C Line Receiver
- Level Shifting
- Digital Logic Ground Isolation
- Current Loop Receiver
- Isolated Input Line Receiver
- System Test Equipment Isolation
- Process Control Input/Output Isolation

Outline Drawings

8-PIN CERAMIC DUAL IN-LINE PACKAGE



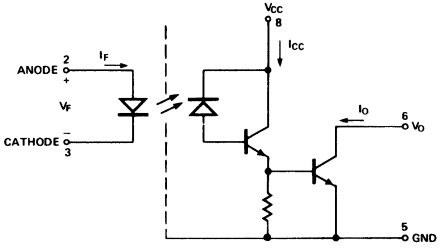
20 Terminal Ceramic Leadless Chip Carrier



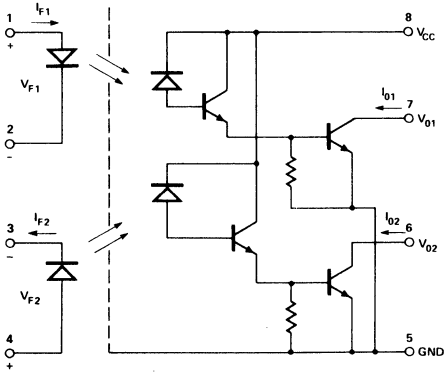
NOTE: DIMENSIONS IN MILLIMETRES (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

Description

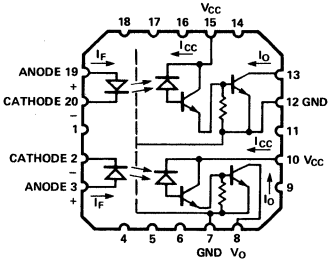
The HCPL-5700, HCPL-5701, and 5962-8981001PC are single channel, low input current, high gain optocouplers. The HCPL-5730, HCPL-5731 and 5962-8978501PC are dual channel units made from the same chip sets. All six products are in eight pin hermetic dual in-line packages. These units are capable of operation and storage over the full military temperature ranges and can be purchased as either single or dual channel standard product (HCPL-5700 and HCPL-5730 respectively), with full MIL-STD-883 Class Level B testing (HCPL-5701 and HCPL-5731 respectively), or from the DESC Standard Military Drawings (SMDs) 5962-89810 and 5962-89785 as (5962-8981001PC or 5962-8978501PC respectively). All parts are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the SMD part number, or by adding Option 200 to the part number for non-SMD parts.



8 PIN CERAMIC DIP SINGLE CHANNEL SCHEMATIC



8 PIN CERAMIC DIP DUAL CHANNEL SCHEMATIC



20 TERMINAL CERAMIC LEADLESS CHIP CARRIER SCHEMATIC

The HCPL-6730, HCPL-6731, and 8962-89785022A are dual channel parts in twenty terminal hermetic, ceramic, leadless chip carriers. The standard part is HCPL-6730. The product with full MIL-STD-883 Class Level B testing is HCPL-6731. The DESC SMD part is 5962-89785022A. All three products are configured and function as two independent single channels. Devices are delivered with solder dipped terminals as a standard feature. Units may also be purchased with gold plated terminals.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Each channel contains a GaAsP light emitting diode optically coupled to an integrated high gain photon detector. The high gain output stage features an open collector output providing both lower saturation voltage and higher signaling speed than possible with conventional photo-Darlington optocouplers.

The supply voltage can be operated as low as 2.0 V without adversely affecting the parametric performance.

These devices have a 300% minimum CTR at an input current of only 0.5 mA making them ideal for use in low input current applications such as MOS, CMOS, low power logic interfaces or line receivers.

Compatibility with high voltage CMOS logic systems is assured by the 18V VCC, VOH current and the guaranteed maximum output leakage current at 18 V. The shallow depth and small junctions offered by the IC process provides better radiation immunity than conventional phototransistor optocouplers.

Upon special request, the following device selections can be made: CTR minimum of up to 600% at 0.5 mA, lower drive currents to 0.1 mA, and lower output leakage current levels to 100 μA.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Voltage, Low Level (Each Channel)	$V_{F,OFF}$		0.8	V
Input Current, High Level (Each Channel)	$I_{F,ON}$	0.5	5	mA
Supply Voltage	V_{CC}	2.0	18	V

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10 s
Output Current, I_O (each channel) ..... 40 mA
Output Voltage, V_O (each channel) ..... -0.5 to 20 V[1]
Supply Voltage ,V_{CC} ..... -0.5 to 20 V[1]
Output Power Dissipation (each channel) ..... 50 mW[2]
Peak Input Current (each channel, ≤ 1 ms duration) ..... 20 mA
Average Input Current, I_F (each channel) ..... 10 mA[3]
Reverse Input Voltage, V_R (each channel) ..... 5 V

Electrical Characteristics T_A = -55°C to +125°C, unless otherwise specified

Parameter		Sym.	Test Conditions	Group A[14] Subgroups	Min.	Typ.*	Max.	Units	Fig.	Notes
Current Transfer Ratio		CTR	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1, 2, 3	300	1500		%	3	4, 5
			I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V		300	1000				
			I_F = 5 mA, V_O = 0.4 V, V_{CC} = 4.5 V		200	500				
Logic Low Output Voltage		V_{OL}	I_F = 0.5 mA, I_O = 1.5 mA, V_{CC} = 4.5 V	1, 2, 3		0.11	0.4	V	2	4
			I_F = 1.6 mA, I_O = 4.8 mA, V_{CC} = 4.5 V			0.13	0.4			
			I_F = 5.0 mA, I_O = 10 mA, V_{CC} = 4.5 V			0.16	0.4			
Logic High Output Current		I_{OHX} / I_{OH}	I_F = 2 µA (Channel Under Test) I_F = 10 mA (Other Channel) V_O = V_{CC} = 18 V	1, 2, 3		0.001	250	µA		6
Logic Low Supply Current	Single Channel	I_{CCL}	I_F = 1.6 mA, V_{CC} = 18 V	1, 2, 3		1.0	2	mA		
	Dual Channel		I_{F1} = I_{F2} = 1.6 mA, V_{CC} = 18 V				4		4	16
Logic High Supply Current	Single Channel	I_{CCH}	I_F = 0, V_{CC} = 18 V	1, 2, 3		0.001	20	µA		
	Dual Channel		I_{F1} = I_{F2} = 0, V_{CC} = 18 V				40			16
Input Forward Voltage	8 Pin DIP Devices	V_F	I_F = 1.6 mA	1	1.0	1.44	1.7	V	1	4
				2			1.7			
				3			1.8			
	20 Terminal Devices			1, 2, 3	1.0		1.8			
Input Reverse Breakdown Voltage		BV_R	I_R = 10 µA	1, 2, 3	5			V		4
Input-Output Insulation Leakage Current		I_{I-O}	45% Relative Humidity, t = 5 s, V_{I-O} = 1500 Vdc	1			1.0	µA		7, 13

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Electrical Characteristics (continued)

Parameter	Sym.	Test Conditions	Group A[14] Subgroups	Min.	Typ.*	Max.	Units	Fig.	Notes
Propagation Delay Time to Logic High at Output	t_{PLH}	I_F = 0.5 mA, R_L = 4.7 kΩ, V_{CC} = 5 V	9, 10, 11		17	60	µs	7, 8	4
		I_F = 1.6 mA, R_L = 1.5 kΩ, V_{CC} = 5 V			14	50			
		I_F = 5.0 mA, R_L = 680 Ω, V_{CC} = 5 V			8	30			
Propagation Delay Time to Logic Low at Output	t_{PHL}	I_F = 0.5 mA, R_L = 4.7 kΩ, V_{CC} = 5 V	9, 10, 11		10	100	µs	7, 8	4
		I_F = 1.6 mA, R_L = 1.5 kΩ, V_{CC} = 5 V			5	30			
		I_F = 5.0 mA, R_L = 680 Ω, V_{CC} = 5 V			2	10			
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	I_F = 0, R_L = 1.5 kΩ $\|V_{CM}\|$ = 50 V_{P-P}, V_{CC} = 5.0 V	9, 10, 11	500	≥2000		V/µs	9	4, 10, 12, 15
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	I_F = 1.6 mA, R_L = 1.5 kΩ $\|V_{CM}\|$ = 50 V_{P-P}, V_{CC} = 5.0 V	9, 10, 11	500	≥1000		V/µs	9	4, 11, 12, 15

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics

T_A = 25°C, V_{CC} = 5 V

Parameter	Symbol	Typical	Units	Test Conditions	Figure	Note
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 Vdc		4, 8
Capacitance (Input-Input)	C_{I-O}	2.0	pF	f = 1 MHz		4, 8
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	-1.8	mV/°C	I_F = 1.6 mA		4
Input Capacitance	C_{IN}	60	pF	f = 1 MHz, V_F = 0		4

Dual Channel Product Only

Input-Output Insulation Leakage Current	I_{I-I}	0.5	nA	45% Relative Humidity, V_{I-I} = 500 Vdc T_A = 25°C, t = 5 s		9
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	V_{I-I} = 500 Vdc		9
Capacitance (Input-Input)	C_{I-I}	1.0	pF	f = 1 MHz		9

Notes:

1. GND Pin should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0 V, will provide lowest total I_{OH} over temperature.
2. Output power is collector output power plus total supply power for the single channel device. For the dual channel device, output power is collector output power plus one half the total supply power. Derate at 1.66 mW/°C above 110°C.
3. Derate I_F at 0.33 mA/°C above 110°C.
4. Each channel.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. I_{OHX} is the leakage current resulting from channel to channel optical crosstalk. I_F = 2 μA for channel under test. For all other channels, I_F = 10 mA.
7. Device considered a two-terminal device: For 8 pin DIP, pins 1 through 4 are shorted together, and pins 5 through 8 are shorted together; for LCC, terminals 19, 20, 1, 2, 3 are shorted together, and terminals 7 through 15 are shorted together.
8. Measured between each input pair shorted together, and all outputs for that channel shorted together.
9. Measured between adjacent input pairs shorted together; i.e., for 8 pin DIP, between pins 1 and 2 shorted together and pins 3 and 4 shorted together; for LCC, between terminals 19 and 20 shorted together, and terminals 2 and 3 shorted together.
10. CM_H is the maximum tolerable common mode transient to assure that the output will remain in a high logic state (i.e., V_O > 2.0 V).
11. CM_L is the maximum tolerable common mode transient to assure that the output will remain in a low logic state (i.e., V_O < 0.8 V).
12. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector ICs from destructively high surge currents. The recommended value is

$$R_{CC} \approx \frac{1\ V}{0.15\ I_F\ (mA)}\ k\Omega$$

for single channel;

$$R_{CC} \approx \frac{1\ V}{0.3\ I_F\ (mA)}\ k\Omega$$

for dual channel.

13. This is a momentary withstand test, not an operating condition.
14. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
15. Subgroups 10 and 11 shall be tested as part of device initial characterization and after design and process changes. Subgroups 10 and 11 shall be guaranteed to the limits specified in Table I for all lots not specifically tested. Subgroup 9 shall be tested with every lot.
16. The HCPL-6730 and HCPL-6731 dual channel parts function as two independent single channel units. Use the single channel parameter limits.

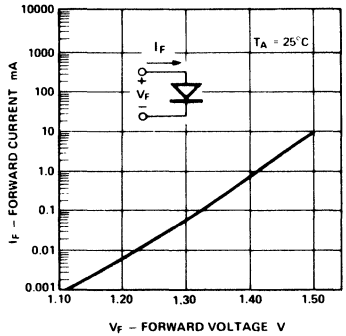


Figure 1. Input Diode Forward Current vs. Forward Voltage.

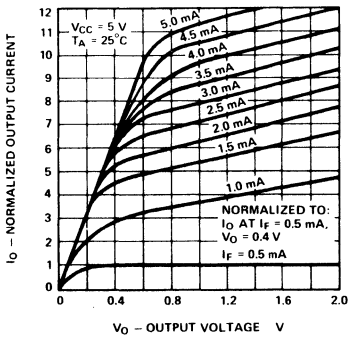


Figure 2. Normalized DC Transfer Characteristics.

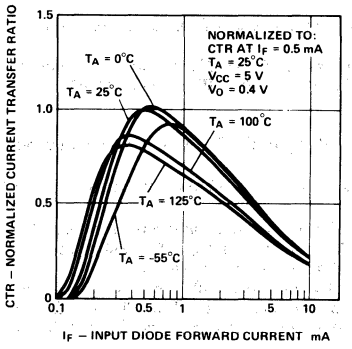


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

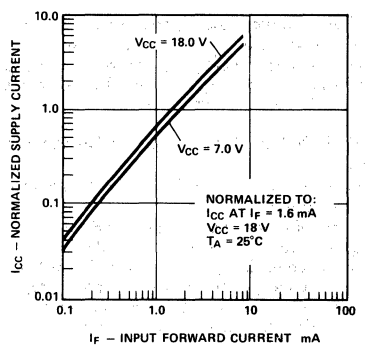


Figure 4. Normalized Supply Current vs. Input Diode Forward Current.

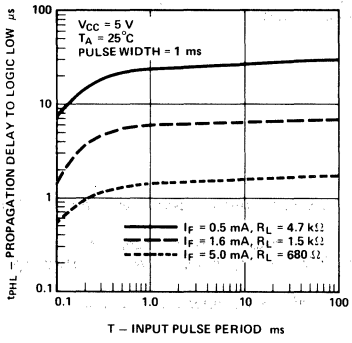


Figure 5. Propagation Delay to Logic Low vs. Input Pulse Period.

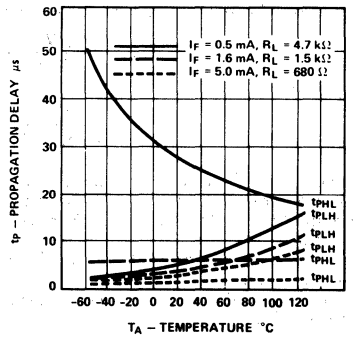


Figure 6. Propagation Delay vs. Temperature.

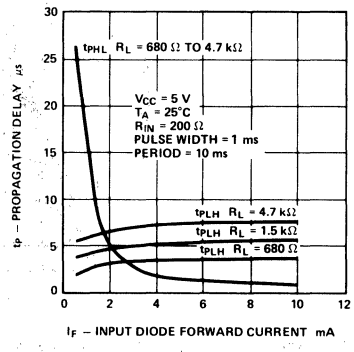
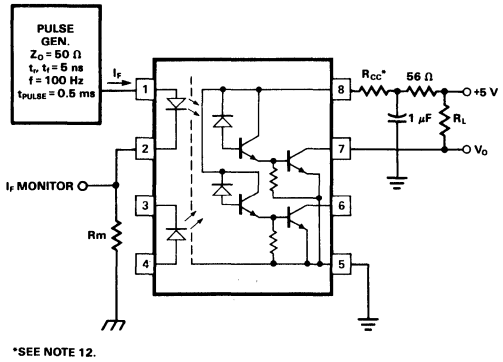
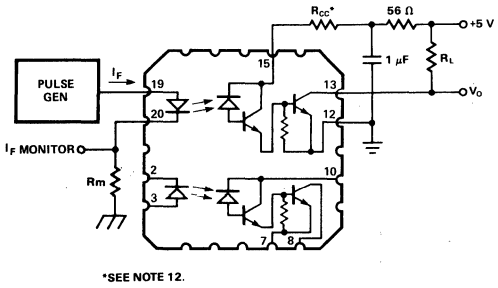


Figure 7. Propagation Delay vs. Input Diode Forward Current.





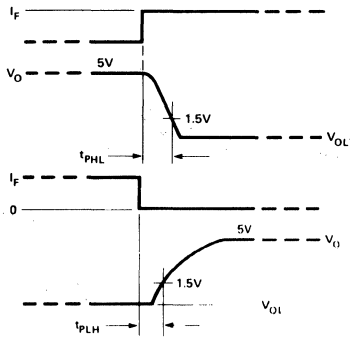
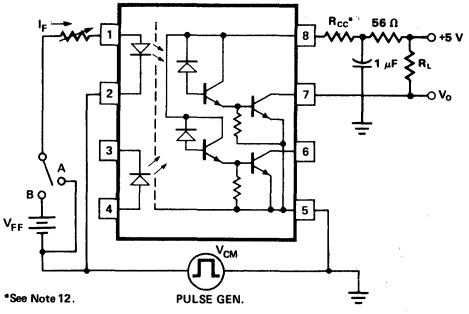
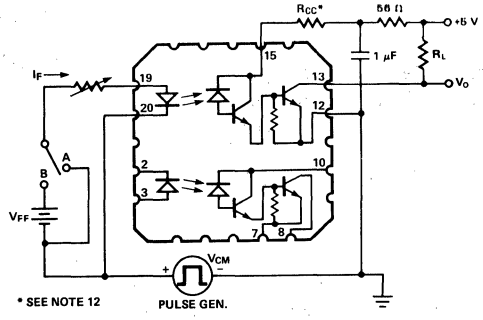


Figure 8. Switching Test Circuit.





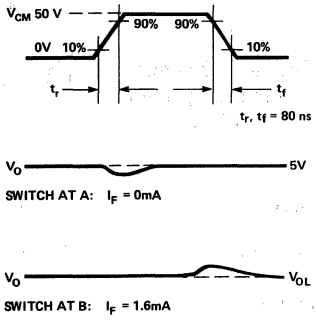


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

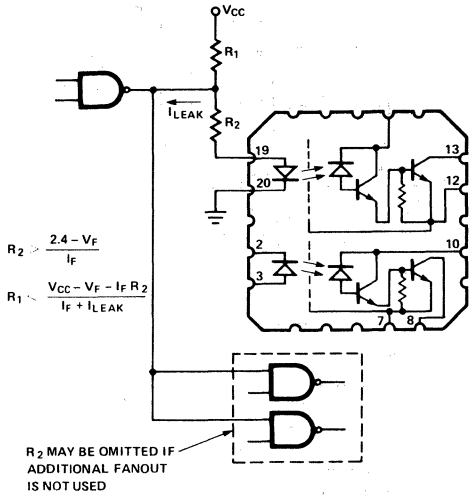


Figure 10. Recommended Drive Circuitry Using TTL Open-Collector Logic.

Condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C, and D.

Group A–See Electrical Characteristics Table.

Group B–No change.

Group C–No change.

Group D–Constant Acceleration–Condition A not E.

SMD 5962-8981001PC SMD 5962-8978501PC SMD 5962-89785022A and MIL-STD-883 Class B Test Programs

Hewlett-Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC SMDs 5962-89810 and 5962-89785 for Hewlett-Packard Optocouplers from the same generic families using the same manufacturing processes, design rules and elements of the same microcircuit groups.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883.

Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration–

Part Numbering System

Commercial Product	Class B Product	SMD Product
HCPL-5700	HCPL-5701	5962-8981001PC
HCPL-5730	HCPL-5731	5962-8978501PC
HCPL-6730	HCPL-6731	5962-89785022A

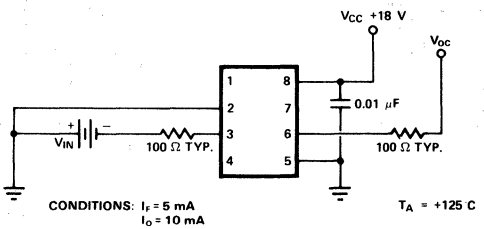


Figure 11. Single Channel Operating Circuit for Burn-In and Steady State Life Tests.

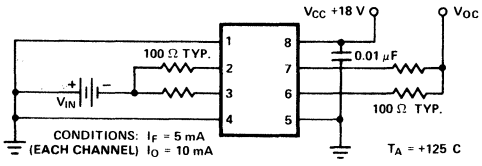


Figure 12. Dual Channel Operating Circuit for Burn-in and Steady State Life Tests.

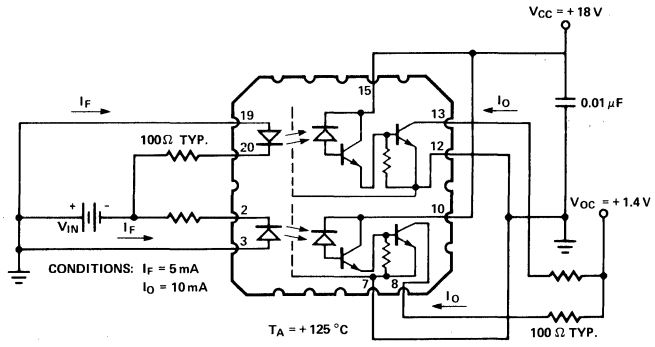


Figure 13. Operating Circuit for Burn-in and Steady State Life Tests.

HEWLETT PACKARD

AC/DC to Logic Interface Hermetically Sealed Optocouplers

Technical Data

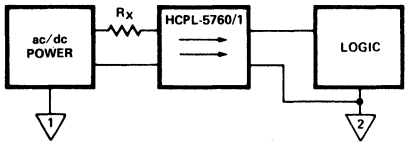
HCPL-5760
HCPL-5761 (883B)
5962-8947701PC

Features

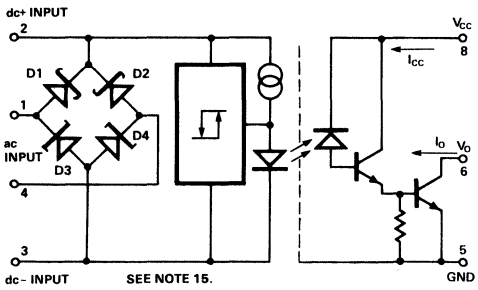
- DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534
- Hermetically Sealed 8-pin Dual In-Line Packages
- Performance Guaranteed Over -55°C to +125°C Ambient Temperature Range
- MIL-STD-883 Class B Testing
- ac or dc Input
- Programmable Sense Voltage
- Hysteresis
- HCPL-3700 Operating Compatibility
- Logic Compatible Output
- 1500 Vdc Withstand Test Voltage
- Thresholds Guaranteed Over Temperature
- Thresholds Independent of LED Characteristics

Applications

- Military/High Reliability Systems
- Limit Switch Sensing
- Low Voltage Detector
- ac/dc Voltage Sensing
- Relay Contact Monitor
- Relay Coil Voltage Monitor
- Current Sensing
- Microprocessor Interface
- Telephone Ring Detection



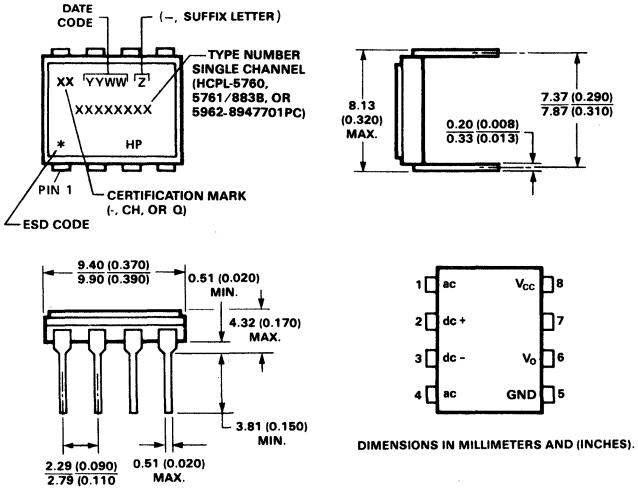
Schematic



TRUTH TABLE

INPUT	OUTPUT
$H(V_{TH+} < V_{dc})$(on)	L
$L(V_{dc} < V_{TH-})$(off)	H

Outline Drawing



DIMENSIONS IN MILLIMETERS AND (INCHES).

Description

The HCPL-5760, HCPL-5761, and 5962-8947701PC are single channel, hermetically sealed, voltage/current threshold detection optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product (HCPL-5760), with full MIL-STD-883 Class Level B testing (HCPL-5761), or from the DESC Standard Military Drawings (SMD) 5962-89477 as (5962-8947701PC). All three products are in eight pin hermetic dual in-line packages. They are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the SMD part #, or by adding option #200 to the part number for non-SMD parts.

Each unit contains a light emitting diode (LED), a threshold sensing input buffer IC, and a high gain photon detector to provide an optocoupler which permits adjustable external threshold levels. The input buffer circuit has a nominal turn on threshold of 2.5 mA (I_{TH+}) and 3.6 volts (V_{TH+}). The addition of one or more external attenuation resistors permits the use of this device over a wide range of input voltages and currents. Threshold sensing prior to the LED and detector elements minimizes effects of different optical gain and LED variations over operating life (CTR degradation). Hysteresis is also provided in the buffer for extra noise immunity and switching stability.

The buffer circuit is designed with internal clamping diodes to protect the circuitry and LED from a wide range of over-voltage and over-current transients while the diode bridge enables easy use with ac voltage input.

These units combine several unique functions in a single package, providing the user with an ideal component for computer input boards and other applications where a predetermined input threshold optocoupler level is desirable.

The high gain output stage features an open collector output providing both TTL compatible saturation voltages and CMOS compatible breakdown voltages.

The test program performed on the 5962-8947701PC is in compliance with DESC (SMD) 5962-89477. The electrical characteristcis table shows Group A Subgroup testing requirements from this drawing.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply	V_{CC}	3.0	18	V
Operating Frequency[1]	f	0	10	KHz

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to 125°C
Lead Solder Temperature ..... 260°C for 10 s[2]
Average Input Current – I_{IN} ..... 15 mA[3]
Surge Input Current – $I_{IN,SG}$ ..... 140 mA[3,4]
Peak Transient Input Current – $I_{IN,PK}$ ..... 500 mA[3,4]
Input Power Dissipation – P_{IN} ..... 195 mW[5]
Total Package Power Dissipation – P_d ..... 260 mW
Output Power Dissipation – P_O ..... 65 mW
Average Output Current – I_O ..... 40 mA
Supply Voltage ,V_{CC} (Pins 8-5) ..... -0.5 min., 20 V max.
Output Voltage, V_O (Pins 6-5) ..... -0.5 min., 20 V max.

Electrical Characteristics T_A = -55°C to 125°C, unless otherwise specified.

Parameter		Symbol	Conditions	Group A[16] Subgroup	Min.	Typ.*	Max.	Units	Fig.	Note
Input Threshold Current		I_{TH+}	$V_{IN} = V_{TH+}$; V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 2.6 mA	1, 2, 3	1.75	2.5	3.20	mA		
		I_{TH-}	$V_{IN} = V_{TH-}$; V_{CC} = 4.5 V; V_O = 2.4 V; $I_{OH} \leq$ 250 µA	1, 2, 3	0.93	1.3	1.62	mA		
Input Threshold Voltage	dc (Pins 2, 3)	V_{TH+}	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 2.6 mA	1, 2, 3	3.18	3.6	4.10	V		7
		V_{TH-}	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 250 µA	1, 2, 3	1.90	2.5	3.00	V	1, 2	
	ac (Pins 1, 4)	V_{TH+}	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 2.6 mA	1, 2, 3	3.79	5.0	5.62	V		7, 8
		V_{TH-}	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 250 µA	1, 2, 3	2.57	3.7	4.52	V		
Input Clamp Voltage		V_{IHC1}	$V_{IHC1} = V_2 - V_3$; V_3 = GND; I_{IN} = 10 mA; Pin 1 & 4 Connected to Pin 3	1, 2, 3	5.3	5.9	6.7	V	3	15
		V_{IHC2}	$V_{IHC2} = \lvert V_1 - V_4 \rvert$; $\lvert I_{IN} \rvert$ = 10 mA; Pins 2 & 3 Open	1, 2, 3	6.0	6.6	7.4	V		
		V_{IHC3}	$V_{IHC3} = V_2 - V_3$; V_3 = GND; I_{IN} = 15 mA; Pins 1 & 4 Open	1, 2, 3		12.0	13.0	V		
Input Current		I_{IN}	$V_{IN} = V_2 - V_3$ = 5.0 V; Pins 1 & 4 Open	1, 2, 3	3.0	3.9	4.5	mA	4	
Logic Low Output Voltage		V_{OL}	V_{CC} = 4.5 V; I_{OL} = 2.6 mA	1, 2, 3		0.05	0.4	V	4	7
Logic High Output Current		I_{OH}	$V_{OH} = V_{CC}$ = 18 V	1, 2, 3			250	µA		
Logic Low Supply Current		I_{CCL}	$V_2 - V_3$ = 5.0 V; V_O = Open; V_{CC} = 18 V	1, 2, 3		0.8	3.0	mA		
Logic High Supply Current		I_{CCH}	V_{CC} = 18 V; V_O = Open	1, 2, 3		0.001	20	µA	5	
Input-Output Insulation		I_{I-O}	45% RH, t = 5 s; V_{I-O} = 1500 Vdc; T_A = 25°C	1			1	µA		9, 10

Electrical Characteristics T_A = -55°C to 125°C, unless otherwise specified (continued).

Parameter	Symbol	Conditions		Group A[16] Subgroup	Min.	Typ.*	Max.	Units	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}	R_L =1.8 kΩ, C_L = 15 pF		9, 10, 11		4	20	µs	6, 7	6, 11
Propagation Delay Time to Logic High Output Level	t_{PLH}	R_L =1.8 kΩ, C_L = 15 pF		9, 10, 11		8	40	µs		6, 12
Logic High Common Mode Transient Immunity	$\|CM_H\|$	V_{CM} = 50 V	T_A = 25°C, I_{IN} = 0 mA	9	1000	≥10,000		V/µs	8	13, 14
		V_{CM} = 450 V				≥10,000				
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	V_{CM} = 50 V	T_A = 25°C, I_{IN} = 4 mA	9	1000	≥5,000		V/µs		
		V_{CM} = 250 V				≥5,000				

*All typical values are at T_A = 25°C, V_{CC} = 5 V unless otherwise noted.

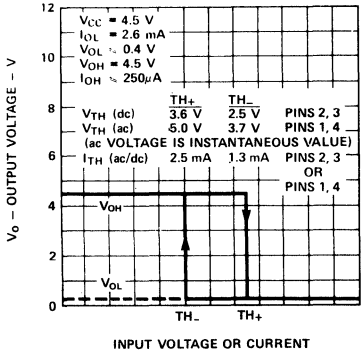


Figure 1. Typical Transfer Characteristics.

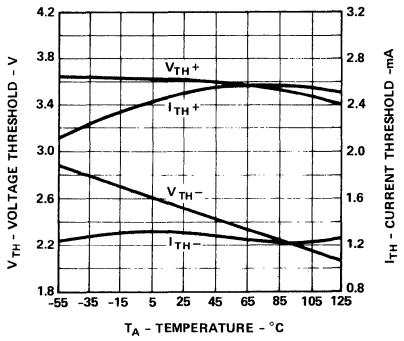


Figure 2. Typical dc Threshold Levels vs. Temperature

HERMETIC OPTOCOUPLERS

Typical Characteristics All typical values are at $T_A = 25°C$, $V_{CC} = 5$ V, unless otherwise specified.

Parameter	Symbol	Typ.	Units	Conditions	Fig.	Note
Hysteresis	I_{HYS}	1.2	mA	$I_{HYS} = I_{TH+} - I_{TH-}$	1	
	V_{HYS}	1.1	V	$V_{HYS} = V_{TH+} - V_{TH-}$		
Input Clamp Voltage	V_{ILC}	-0.76	V	$V_{ILC} = V_2 - V_3$; V_3 = GND; I_{IN} = -10 mA		
Bridge Diode Forward Voltage	$V_{D1,2}$	0.62		I_{IN} = 3 mA (see schematic)		
	$V_{D3,4}$	0.73				
Input-Output Resistance	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 Vdc		9
Input-Output Capacitance	C_{I-O}	2.0	pF	f = 1 MHz, V_{I-O} = 0 Vdc		
Input Capacitance	C_{IN}	50	pF	f = 1 MHz; V_{IN} = 0 V, Pins 2 & 3, Pins 1 & 4 Open		
Output Rise Time (10-90%)	t_r	10	µs		7	
Output Fall Time (90-10%)	t_f	0.5	µs		7	

Notes:

1. Maximum operating frequency is defined when output waveform (Pin 6) attains only 90% of V_{CC} with R_L = 1.8 kΩ, C_L = 15 pF using a 5 V square wave input signal.
2. Measured at a point 1.6 mm below seating plane.
3. Current into/out of any single lead.
4. Surge input current duration is 3 ms at 120 Hz pulse repetition rate. Transient input current duration is 10 µs at 120 Hz pulse repetition rate. Note that maximum input power, P_{IN}, must be observed.
5. Derate linearly above 100°C free-air temperature at a rate of 4.26 mW/°C. Maximum input power dissipation of 195 mW allows an input IC junction temperature of 150°C at an ambient temperature of T_A = 125°C with a typical thermal resistance from junction to ambient of θ_{JA} = 235°C/W. The typical thermal resistance from junction to case is equal to 170°C/W. Excessive P_{IN} and T_J may result in device degradation.
6. The 1.8 kΩ load represents 1 TTL unit load of 1.6 mA and the 4.7 kΩ pull-up resistor.
7. Logic low output level at Pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH}$ – once V_{IN} has exceeded V_{TH+}. Logic high output level at Pin 6 occurs under the conditions of $V_{IN} \leq V_{TH-}$ as well as the range of $V_{IN} < V_{TH+}$ once V_{IN} has decreased below V_{TH-}.
8. The ac voltage is instantaneous voltage.
9. Device considered a two terminal device: Pins 1, 2, 3, 4 connected together, Pins 5, 6, 7 8 connected together.
10. This is a momentary withstand test, not an operating condition.
11. The t_{PHL} propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 µs rise time) to the 1.5 V level on the leading edge of the output pulse (see Figure 7).
12. The t_{PLH} propagation delay is measured from the 2.5 V level of the trailing edge of a 5.0 V input pulse (1 µs fall time) to the 1.5 V level on the trailing edge of the output pulse (see Figure 7).
13. Common mode transient immunity in Logic High level is the maximum tolerable $dV_{CM/dt}$ of the common mode voltage, V_{CM}, to ensure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in Logic Low level is the maximum tolerable $dV_{CM/dt}$ of the common mode voltage, V_{CM}, to ensure that the output will remain in a Logic Low state (i.e., $V_O < 0.8$ V). See figure 8.
14. In applications were $dV_{CM/dt}$ may exceed 50,000 V/µs (such as static discharge), a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value for R_{CC} is 240 Ω per volt of allowable drop in V_{CC} (between Pin 8 and V_{CC}) with a minimum value of 240 Ω.
15. D_1 and D_2 are Schottky diodes; D_3 and D_4 are zener diodes.
16. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10 ,3 and 11, respectively.)

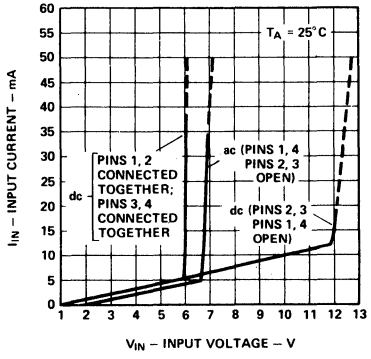


Figure 3. Typical Input Characteristics, I_{IN} vs. V_{IN} (ac Voltage Is Instantaneous Value.)

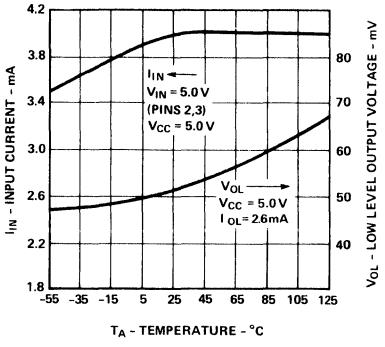


Figure 4. Typical Input Current, I_{IN}, and Low Level Output Voltage, V_{OL}, vs. Temperature.

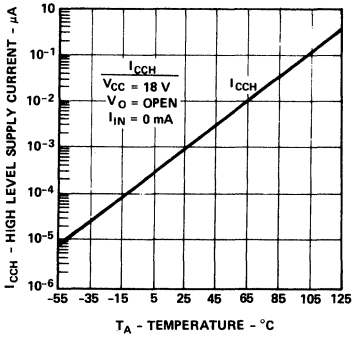


Figure 5. Typical High Level Supply Current, I_{CCH} vs. Temperature.

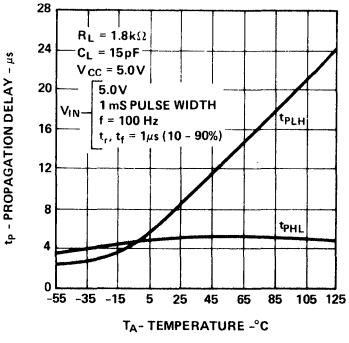
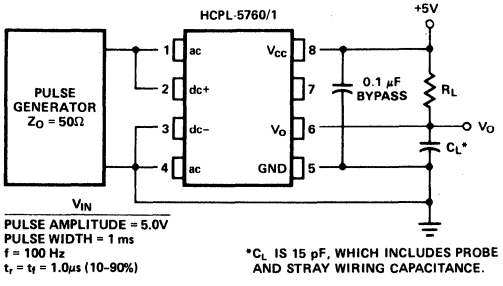


Figure 6. Typical Propagation Delay vs. Temperature.



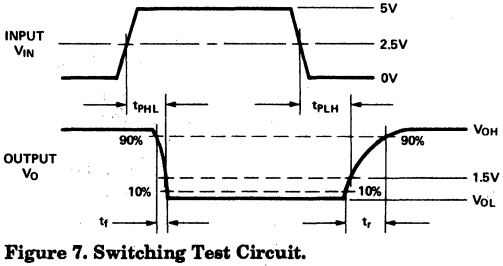
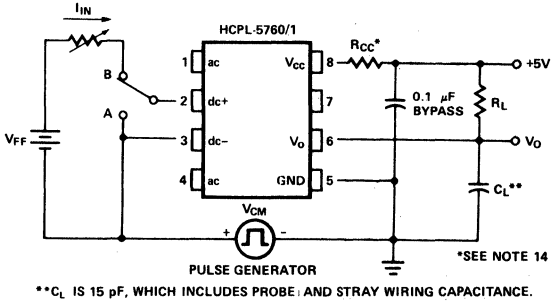


Figure 7. Switching Test Circuit.



**C_L IS 15 pF, WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

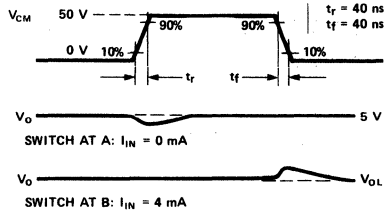


Figure 8. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

SMD 5962-8947701PC and MIL-STD-883 Class B Test Program

Hewlett-Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC SMD 5962-89477 for an H. P. Optocoupler from the same generic family using the same manufacturing process, design rules and elements of the same microcircuit group.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883.

5761/883B Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration–Condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C, and D.
- Group A– See Electrical Characteristics Table.
- Group B– No change.
- Group C– No change.
- Group D– Constant Acceleration– Condition A not E.

Part Numbering System

Commercial Product	Class B Product	SMD Product
HCPL-5760	HCPL-5761	5962-8947701PC

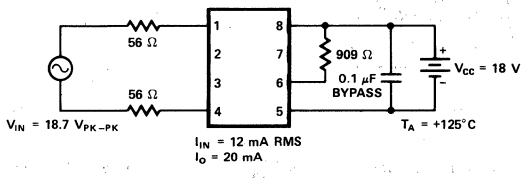


Figure 9. Operating Circuit for Burn-In and Steady State Life Tests

Electrical Considerations

The HCPL-5760, HCPL-5761, or 5962-8947701PC optocoupler has internal temperature compensated, predictable voltage and current threshold points which allow selection of an external resistor, R_x, to determine larger external threshold voltage levels. For a desired external threshold voltage, $V_{\pm}$, a corresponding typical value of Rx can be obtained from Figure 10. Specific calculation of R_x can be obtained from Equation (1) of Figure 11. Specification of both V_+ and V_- voltage threshold levels simultaneously can be obtained by the use of R_x and R_p as shown in Figure 11 and determined by Equations (2) and (3).

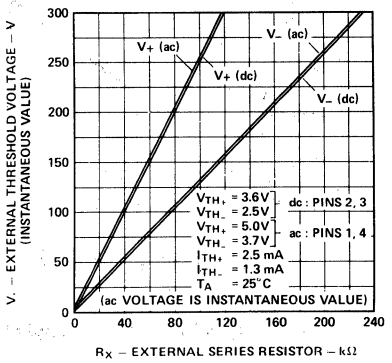


Figure 10. Typical External Threshold Characteristic, $V_{\pm}$ vs. R_x

Rx can provide over-current transient protection by limiting input current during a transient condition. For monitoring contacts with a relay or switch, the HCPL-5760/1, or 5962-8947701PC combination with R_x and R_p can be used to allow a specific current to be conducted through the contacts for cleaning purposes (wetting current).

The choice of which input voltage clamp level to choose depends upon the application of this device (see Figure 3). It is recommended that the low clamp condition be used when possible to lower the input power dissipation as well as the LED current, which minimizes LED degradation over time.

In applications where $dV_{CM/dt}$ may be extremely large (such as static discharge), a series resistor, R_{CC}, should be connected in series with V_{CC} and Pin 8 to protect the detector IC from destructively high surge currents. See note 14 for determination of R_{CC}. In addition, it is recommended that a ceramic disc bypass capacitor of 0.01 μF to 0.1 μF be placed between Pins 8 and 5 to reduce the effect of power supply noise.

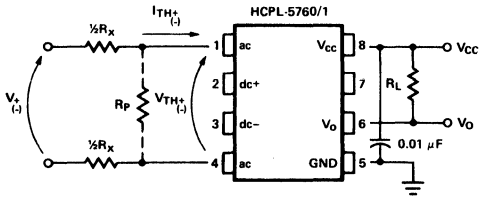


Figure 11. External Threshold Voltage Level Selection

For interfacing ac signals to TTL systems, output low pass filtering can be performed with a pullup resistor of 1.5 kΩ and 20 µF capacitor. This application requires a Schmitt trigger gate to avoid slow rise time chatter problems. For ac input applications, a filter capacitor can be placed across the dc input terminals for either signal or transient filtering.

Either ac (Pins 1, 4) or dc (Pins 2, 3) input can be used to determine external threshold levels.

For one specifically selected external threshold voltage level V_+ or V_-, R_x can be determined without use of R_p via

$$R_x = \frac{V_+ - V_{TH+}}{I_{TH+}} \quad (1)$$

For two specifically selected external threshold voltage levels, V_+ and V_-, the use of R_x and R_p will permit this selection via equations (2), (3) provided the following conditions are met:

$$\frac{V_+}{V_-} \geq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}}$$

$$R_x = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_{TH-}) - I_{TH-}(V_{TH+})} \quad (2)$$

$$R_P = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_- - V_{TH-}) + I_{TH-}(V_{TH+} - V_+)} \quad (3)$$

See Application Note 1004 for more information.

HEWLETT PACKARD

Dual Channel Hermetically Sealed Transistor Output Optocoupler

Technical Data

4N55
4N55/883B
5962-8767901EC

Features

- DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534
- Hermetically Sealed 8-pin Dual In-Line Package
- Performance Guaranteed Over -55°C to +125°C Ambient Temperature Range
- MIL-STD-883 Class B Testing
- Dual Isolated Channels
- High Speed: Typically 400kBit/s
- 2-MHz Bandwidth
- Open Collector Outputs
- 2-18 Volt V_{CC} Range
- 1500 Vdc Withstand Test Voltage
- High Radiation Immunity
- HCPL-2530/2531, HCPL-55XX, 65XX Function Compatibility

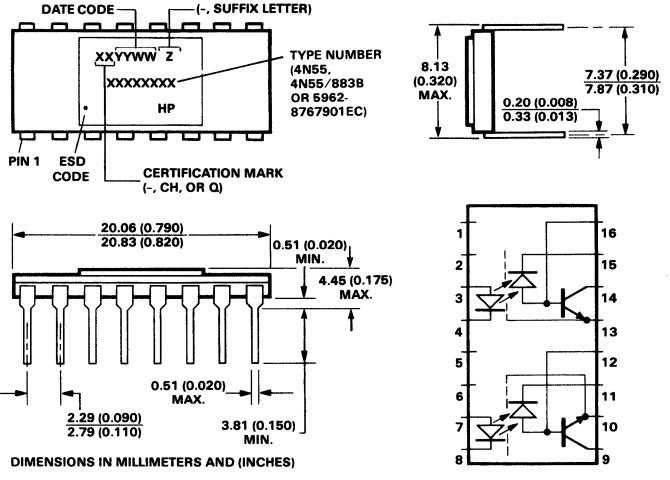
Applications

- Military/High Reliability Systems
- Line Receivers
- Digital Logic Ground Isolation
- Analog Signal Ground Isolation
- Switching Power Supply Feedback Element
- Vehicle Command/Control
- System Test Equipment
- Level Shifting

Description

The 4N55, 4N55/883B, and 5962-8767901EC units consist of two completely independent transistor output optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product (4N55), with full MIL-STD-883 Class Level B testing (4N55/883B) or from the DESC Standard Military Drawing (SMD) 5962-87679 as (5962-8767901EC). All three products are assembled in hermetic, sixteen pin dual in-line packages. These parts are

Outline Drawing



normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the DESC part #, or by adding option #200 to the part number for non DESC parts.

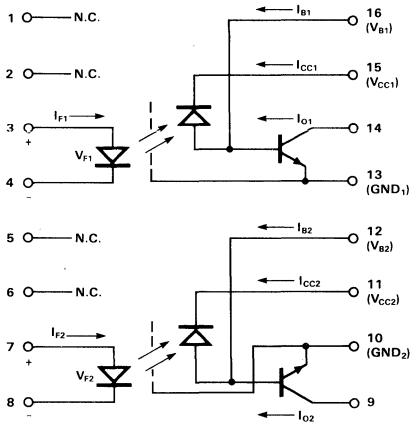
Each channel has a GaAsP light emitting diode which is optically coupled to an integrated photon detector. Separate connections for the photodiodes and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor optocoupler by reducing the base-collector capacitance.

These devices are suitable for wide bandwidth analog applications, as well as for interfacing TTL to LSTTL or CMOS. Current Transfer Ratio (CTR) is 9% minimum at I_F = 16 mA. The 18 V V_{CC} capability will enable the designer to interface any TTL family to CMOS. The availability of the base lead allows optimized gain/bandwidth adjustment in analog applications. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor couplers.

The test program performed on the 5962-8767901EC is in compliance with DESC (SMD) 5962-87679. The Electrical Characteristics Table shows Group A Subgroup testing requirements from this drawing.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Schematic



CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}		250	µA
Supply Voltage	V_{CC}	2	18	V
Operating Temperature	T_C	-55	+125	°C
Input Current, High Level	$I_{F,H}$	12	20	mA

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Lead Solder Temperature ..... 260°C for 10 s.
(1.6 mm below seating plane)
Average Input Current – I_F (each channel) ..... 20 mA
Peak Input Current – I_F (each channel,
≤ 1 ms duration) ..... 40 mA
Reverse Input Voltage — V_R (each channel) ..... 5 V
Input Power Dissipation (each channel) ..... 36 mW
Average Output Current — I_O (each channel) ..... 8 mA
Peak Output Current — I_O (each channel) ..... 16 mA
Supply Voltage — V_{CC} (each channel) ..... -0.5 V to 20 V
Output Voltage — V_O (each channel) ..... -0.5 V to 20 V
Emitter Base Reverse Voltage – V_{EBO} ..... 3.0 V
Base Current – I_B (each channel) ..... 5 mA
Output Power Dissipation (each channel) ..... 50 mW
Derate linearly above 100°C free air temperature
at a rate of 1.4 mW/°C.

Electrical Characteristics

Parameter	Sym.	Test Conditions[3]	Group A Subgroups[10]	Limits			Units	Fig.	Note
				Min.	Typ.**	Max.			
Input Forward Voltage	V_F*	I_F = 20 mA	1, 2, 3		1.55	1.80	Vdc	1	1
Reverse Breakdown Voltage	BV_R*	I_R = 10 µA	1, 2, 3	5.0			Vdc		1
Coupled High Level Output Current	I_{OH}	I_F = 0, I_F (other channel) = 20 mA V_O = V_{CC} = 18 V	1, 2, 3		10	100	µA dc	4	1
Output Leakage Current	I_{OLEAK}*	I_F = 250 µA, I_F (other channel) = 20 mA, V_O = V_{CC} = 18 V	1, 2, 3		30	250	µA dc	4	1
Current Transfer Ratio	CTR*	V_{CC} = 4.5 V; V_O = 0.4 V; I_F = 16 mA	1, 2, 3	9	20		%	2, 3	1, 2
Input to Output Insulation Leakage Current	$I_{I/O}$*	T_C = +25°C; $V_{I/O}$ = 1500 Vdc Relative humidity = 45%; t = 5 s	1			1.0	µA dc		3, 9
Supply Current High Level	I_{CCH}*	I_F = 0 mA, I_F (other channel) = 20 mA, V_{CC} = 18 V	1, 2, 3		0.1	10	µA dc		1
Supply Current Low Level	I_{CCL}*	I_{F1} = I_{F2} = 20 mA, V_{CC} = 18 V	1, 2, 3		35	200	µA dc	5	1
Propagation Delay Time									
HIGH to LOW	t_{PHL}*	I_F = 16 mA; R_L = 8.2 kΩ V_{CC} = 5.0 V; C_L = 50 pF	9, 10, 11		0.4	2	µs	6, 9	1
LOW to HIGH	t_{PLH}*				1.0	6			

*JEDEC Registered Data.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Note
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	-1.5	mV/°C	I_F = 20 mA		1
Input Capacitance	C_{IN}	60	pF	f = 1 MHz, V_F = 0 Vdc		1
Input-Output Resistance	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 Vdc		1
Input-Output Capacitance	C_{I-O}	1.0	pF	f = 1 MHz		1, 4
Input-Input Insulation Leakage Current	I_{I-I}	1	pA	45% Relative Humidity, V_{I-I} = 500 Vdc, t = 5 s		5
Input-Input Capacitance	C_{I-I}	0.55	pF	f = 1 MHz		5
Transistor DC Current Gain	h_{FE}	150	–	V_O = 5 V, I_O = 3 mA		1
Small Signal Current Transfer Ratio	$\frac{\Delta I_O}{\Delta I_F}$	21	%	V_{CC} = 5 V, V_O = 2 V	7	1
Common Mode Transient Immunity at Logic High Level Output	$\lvert CM_H \rvert$	1000	V/μs	I_F = 0, R_L = 8.2 kΩ V_{CM} = 10 V_{p-p} V_O (min.) = 2.0 V	10	1, 6
Common Mode Transient Immunity at Logic Low Level Output	$\lvert CM_L \rvert$	1000	V/μs	I_F = 16 mA, R_L = 8.2 kΩ V_{CM} = 10 V_{p-p} V_O (max.) = 0.8 V	10	1, 7
Bandwidth	BW	9	MHz		8	8

Notes:

1. Each channel.
2. Current Transfer Ratio is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%. CTR is known to degrade slightly over the unit's lifetime as a function of input current, temperature, signal duty cycle and system on time. Refer to Application Note 1002 for more detail. In short it is recommended that designers allow at least 20-25% guardband for CTR degradation.
3. Measured between pins 1 through 8 shorted together and pins 9 through 16 shorted together.
4. Measured between each input pair shorted together and the output pins for that channel shorted together.
5. Measured between pins 3 and 4 shorted together and pins 7 and 8 shorted together.
6. CM_H is the steepest slope (dV/dt) on the leading edge of the common mode pulse, V_{CM}, for which the output will remain in the logic high state (i.e., V_O > 2.0 V).
7. CM_L is the steepest slope (dV/dt) on the trailing edge of the common mode pulse, V_{CM}, for which the output will remain in the logic low state (i.e., V_O < 0.8 V).
8. Bandwidth is the frequency at which the ac output voltage is 3 dB below the low frequency asymptote.
9. This is a momentary withstand test, not an operating condition.
10. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

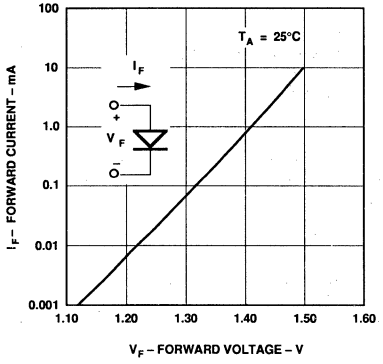


Figure 1. Input Diode Forward Current vs. Forward Voltage.

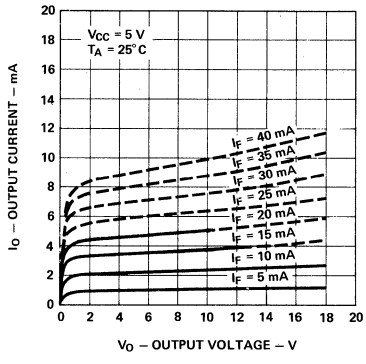


Figure 2. DC and Pulsed Transfer Characteristic.

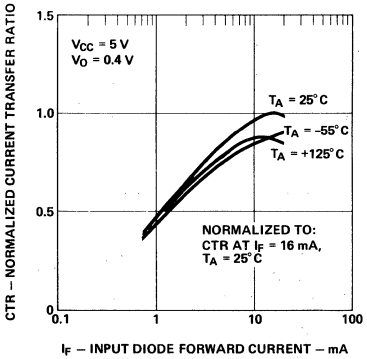


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

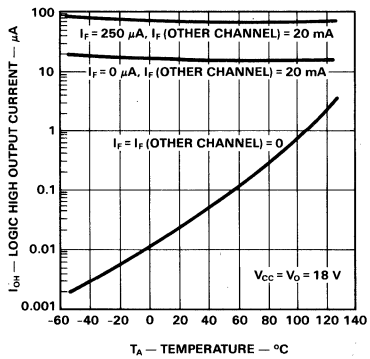


Figure 4. Logic High Output Current vs. Temperature.

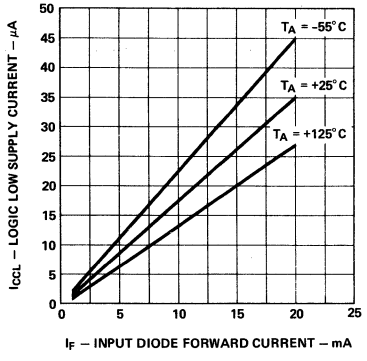


Figure 5. Logic Low Supply Current vs. Input Diode Forward Current.

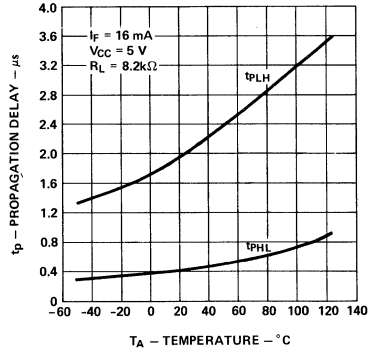


Figure 6. Propagation Delay vs. Temperature.

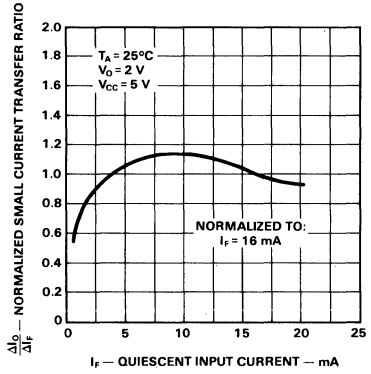


Figure 7. Normalized Small Signal Current Transfer Ratio vs. Quiescent Input Current.

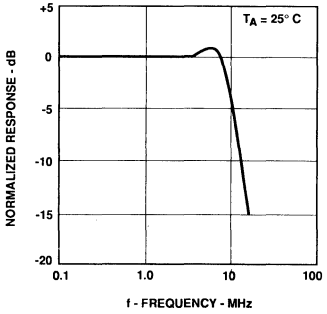


Figure 8a. Frequency Response.

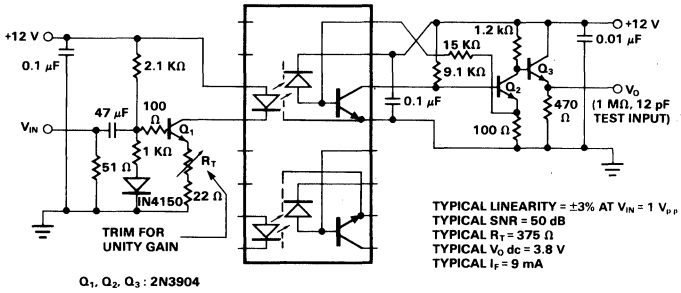


Figure 8b. Frequency Response.

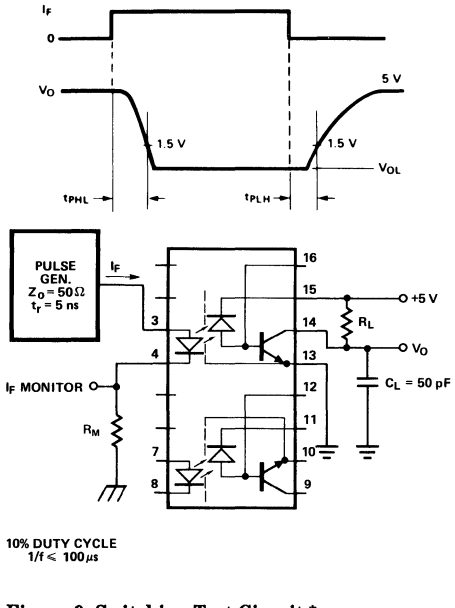


Figure 9. Switching Test Circuit.*
*JEDEC Registered Data.

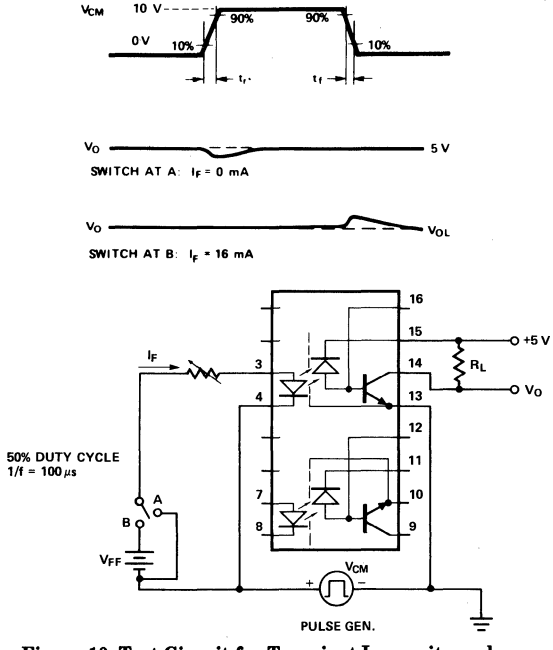
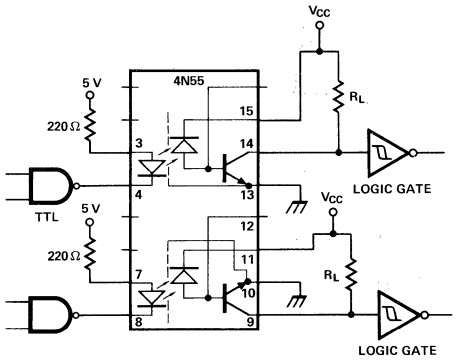


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.



LOGIC FAMILY	LSTTL	CMOS	
DEVICE NO.	54LS14	CD40106BM	
V_{cc}	5 V	5 V	15 V
R_L 5% TOLERANCE	18 kΩ*	8.2 kΩ	22 kΩ

***THE EQUIVALENT OUTPUT LOAD RESISTANCE IS AFFECTED BY THE LSTTL INPUT CURRENT AND IS APPROXIMATELY 8.2 kΩ.**

This is a worst case design which takes into account 25% degradation of CTR. See App. Note 1002 to assess actual degradation and lifetime.

Figure 11. Recommended Logic Interface.

SMD 5962-8767901EC and MIL-STD-883 Class B Test Program

Hewlett-Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC SMD 5962-87679 for an HP Optocoupler from the same generic family using the same manufacturing process, design rules, and elements of the same microcircuit group.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883.

4N55/883B Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration–Condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C, and D.

Group A–See Electrical Characteristics Table.
Group B–No change.
Group C–No change.
Group D–Constant Acceleration–Condition A not E.

Part Numbering System

Commercial Product	Class B Product	SMD Product
4N55	4N55/883B	5962-8767901EC

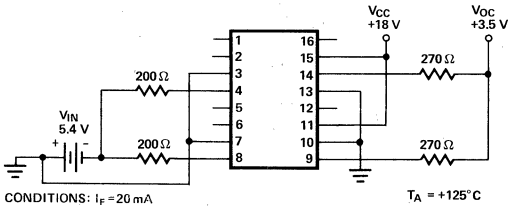


Figure 12. Operating Circuit for Burn-in and Steady State Life Tests.

HEWLETT PACKARD

Transistor Output, Hermetically Sealed Optocoupler

Technical Data

HCPL-5500
HCPL-5501 (883B)
HCPL-5530
HCPL-5531 (883B)
(8-pin Dual In-Line Package)
HCPL-6530
HCPL-6531 (883B)
(20 Terminal Leadless Chip Carrier)

Features

- **Manufactured and Tested on a MIL-STD-1772 Certified Line**
- **QML-MIL-H-38534**
- **Performance Guaranteed Over -55°C to +125°C Ambient Temperature Range**
- **MIL-STD-883 Class B Testing**
- **High Speed: Typically 400 kbit/s**
- **9 MHz Bandwidth**
- **Open Collector Outputs**
- **1500 Vdc Withstand Test Voltage**
- **High Radiation Immunity**
- **4N55, 6N135/6, HCPL-2530/31 Function Compatibility**
- **2-18 Volt V_{CC} Range**

Applications

- **Military/High Reliability Systems**
- **Isolated Input Line Receiver**
- **Isolated Output Line Driver**
- **System Test Equipment Isolation**
- **Digital Logic Ground Isolation**
- **Current Loop Receiver**
- **Level Shifting**
- **Analog Signal Ground Isolation**
- **Vehicle Command/Control**
- **Switching Power Supply Feedback Element**

Description

These units are single and dual channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product or with full MIL-STD-883 Class Level B testing. All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

The HCPL-5500, 5501, 5530 and 5531 are in a 8 Pin ceramic DIP configured as either single or dual channel devices. The standard products are HCPL-5500 and HCPL-5530. The products with full MIL-STD-883 Class Level B testing are HCPL-5501 and HCPL-5531.

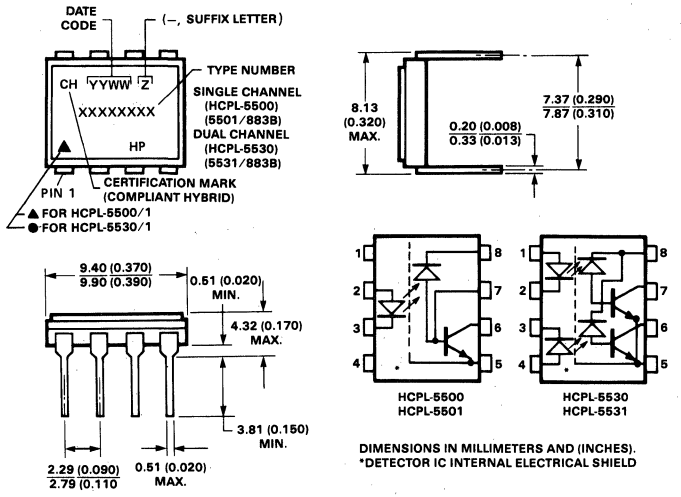
The HCPL-6530 and HCPL-6531 parts are in twenty terminal hermetic, ceramic, leadless chip carriers. The standard part is HCPL-6530. The product with full MIL-STD-883 Class Level B testing is HCPL-6531. These dual channel devices are configured and function as two independent single channels. Devices are delivered with solder dipped terminals as a standard feature. Units may also be purchased with gold plated terminals.

Each channel contains a light emitting diode optically coupled to an integrated photon detector providing 1500 Vdc electrical isolation between input and output. Separate connections for the photodiodes and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor optocoupler by reducing the base-collector capacitance. These devices are suitable for wide bandwidth analog applications, as well as for interfacing TTL to LSTTL or CMOS. Current Transfer Ratio (CTR) is 9% minimum at I_F = 16 mA over the full military operating temperature range, -55°C to +125°C. The 18 V V_{CC} capability will enable the designer to interface any TTL family to CMOS. The availability of the base lead allows optimized gain/bandwidth adjustment in analog applications. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor couplers.

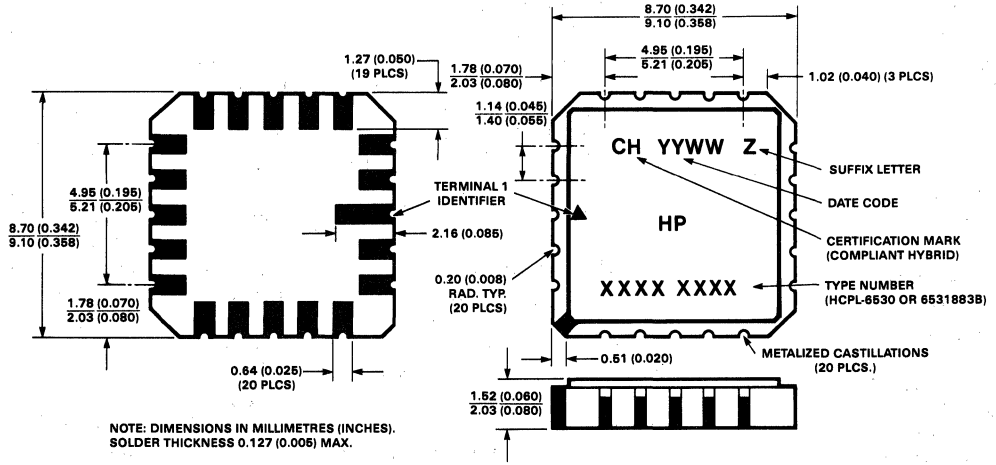
These products are also available with the transistor base node unconnected to improve common mode noise immunity and ESD susceptibility. In addition, higher CTR minimums are available by special request. Contact your local HP Field Sales Engineer for ordering information.

Outline Drawings

8-pin Ceramic Dual In-Line Package

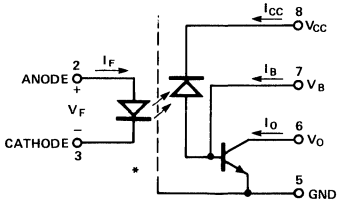


20 Terminal Ceramic Leadless Chip Carrier



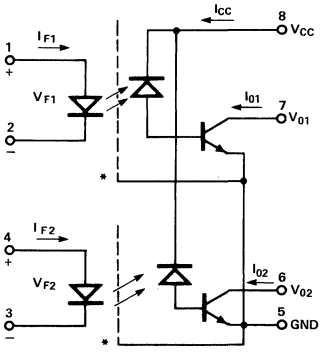
8 PIN Ceramic DIP

SINGLE CHANNEL SCHEMATIC

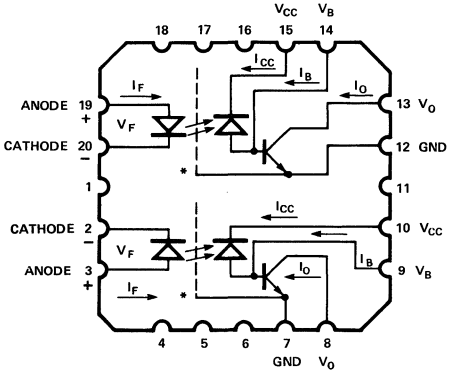


8 PIN Ceramic DIP

DUAL CHANNEL SCHEMATIC



20 Terminal Ceramic Leadless Chip Carrier Schematic



* DETECTOR IC INTERNAL ELECTRICAL SHIELD

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}		250	μA
Supply Voltage	V_{CC}	2	18	V

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10 s
Average Input Current, I_F each channel ..... 20 mA
Peak Input Current, I_F each channel,
≤1 ms duration ..... 40 mA
Reverse Input Voltage, V_R each channel ..... 3 V
Average Output Current, I_O each channel ..... 8 mA
Peak Output Current, I_O each channel ..... 16 mA
Supply Voltage, V_{CC} each channel ..... -0.5 V to 20 V
Output Voltage, V_O each channel ..... -0.5 V to 20 V
Input Power Dissipation, each channel ..... 36 mW
Output Power Dissipation, each channel ..... 50 mW
ESD Classification ..... Class 1
ESD Classification (HCPL-5530/1) ..... Class 3
(MIL-STD-883, Method 3015)

Single Channel Product Only

Emitter Base Reverse Voltage. V_{EBO} ..... 3.0 V
Base Current, I_B each channel ..... 5 mA

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and degradation which may be induced by ESD.

Electrical Characteristics TA = -55°C to +125°C, unless otherwise specified

Parameter		Sym.	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio		CTR	9	20		%	I_F = 16 mA, V_O = 0.4 V, V_{CC} = 4.5 V	2, 3	1, 2, 10
Logic High Output Current		I_{OH}		5	100	µA	I_F = 0, I_F (other channel) = 20 mA V_O = V_{CC} = 18 V	4	1
Output Leakage Current Dual Channel		I_{OH1}		30	250	µA	I_F = 250 µA, I_F (other channel) = 20 mA, V_O = V_{CC} = 18 V	4	1
Logic Low Supply Current	Single Channel	I_{CCL}		35	200	µA	I_F = 20 mA, V_{CC} = 18 V	5	1
	Dual Channel			70	400		I_{F1} = I_{F2} = 20 mA, V_{CC} = 18 V		4
Logic High Supply Current	Single Channel	I_{CCH}		0.1	10	µA	I_F = 0 mA, V_{CC} = 18 V		1
	Dual Channel			0.2	20		I_F = 0 mA, I_F (other channel) = 20 mA, V_{CC} = 18 V		4
Input Forward Voltage		V_F		1.55	1.9	V	I_F = 20 mA	1	1
Input Reverse Breakdown Voltage		B_{VR}	3			V	I_R = 10 µA		1
Input-Output Insulation Leakage Current		I_{I-O}			1.0	µA	45% Relative Humidity, T_A = 25°C, t = 5 s, V_{I-O} = 1500 Vdc		3, 9
Propagation Delay Time to Logic High at Output		t_{PLH}		1.0	6.0	µs	R_L = 8.2 kΩ, C_L = 50 pF I_F = 16 mA, V_{CC} = 5 V	6, 9	1, 6
Propagation Delay Time to Logic Low at Output		t_{PHL}		0.4	2.0	µs	R_L = 8.2 kΩ, C_L = 50 pF I_F = 16 mA, V_{CC} = 5 V	6, 9	1, 6

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics $T_A = 25°C$, $V_{CC} = 5$ V

Parameter	Sym.	Typ.	Units	Test Conditions	Fig.	Note
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	-1.5	mV/°C	$I_F = 20$ mA		1
Input Capacitance	C_{in}	60	pF	f = 1 MHz, $V_F = 0$		1
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	$V_{I-O} = 500$ Vdc		3
Capacitance (Input-Output)	C_{I-O}	1.0	pF	f = 1 MHz		1, 11
Transistor DC Current Gain	h_{FE}	250	–	$V_O = 5$ V, $I_O = 3$ mA		1
Small Signal Current Transfer Ratio	$\frac{\Delta I_O}{\Delta I_F}$	21	%	$V_{CC} = 5$ V, $V_O = 2$ V	7	1
Bandwidth	BW	9	MHz		8	8
Common Mode Transient Immunity At Logic High Level Output	$\lvert CM_H \rvert$	1000	V/μs	$I_F = 0$ mA, $R_L = 8.2$ kΩ $V_{CM} = 10$ V_{p-p}	10	1, 7
Common Mode Transient Immunity At Logic Low Level Output	$\lvert CM_L \rvert$	-1000	V/μs	$I_F = 16$ mA, $R_L = 8.2$ kΩ $V_{CM} = 10$ V_{p-p}	10	1, 7

Dual Channel Product Only

Input-Input Insulation Leakage Current	I_{I-I}	1	pA	45% Relative Humidity, $V_{I-I} = 500$ Vdc, t = 5 s		5, 9
Capacitance (Input-Input)	C_{I-I}	0.8	pF	f = 1 MHz		5
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	$V_{I-I} = 500$ Vdc		5

Notes:

1. Each channel of a dual channel device.
2. Current Transfer Ratio is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%. CTR is known to degrade slightly over the unit's lifetime as a function of input current, temperature, signal duty cycle, and system on time. Refer to Application Note 1002 for more detail. In short, it is recommended that designers allow at least 20-25% guardband for CTR degradation.
3. Device considered a two-terminal device: for 8 pin DIP, pins 1 through 4 are shorted together, and pins 5 through 8 are shorted together; for LCC, terminals 19, 20, 1, 2, 3 are shorted together, and terminals 7 through 15 are shorted together.
4. The HCPL-6530 and HCPL-6531 dual channel parts function as two independent single channel units. Use the single channel parameter limits.
5. Measured between adjacent input pairs shorted together; i.e., for 8 pin DIP, between pins 1 and 2 shorted together and pins 3 and 4 shorted together; for LCC, between terminals 19 and 20 shorted together, and terminals 2 and 3 shorted together.
6. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.

7. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8$ V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0$ V).
8. Bandwidth is the frequency at which the ac output voltage is 3 dB below the low frequency asymptote. For the HCPL-5530 the typical bandwidth is 2 MHz.
9. This is a momentary withstand test, not an operating condition.
10. Higher CTR minimums are available to support special applications.
11. Measured between each input pair shorted together and all outputs for that channel shorted together.

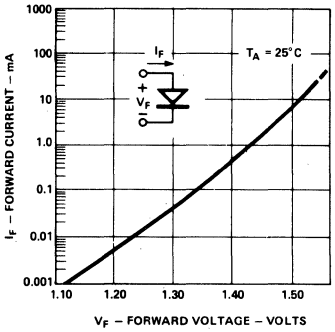


Figure 1. Input Diode Forward Characteristic.

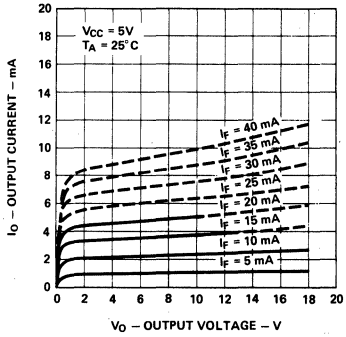


Figure 2. DC and Pulsed Transfer Characteristic.

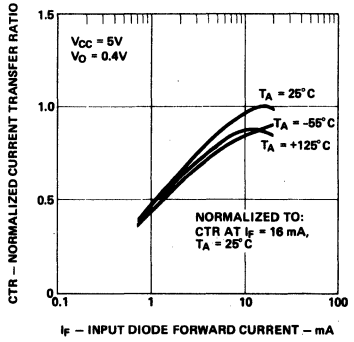


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

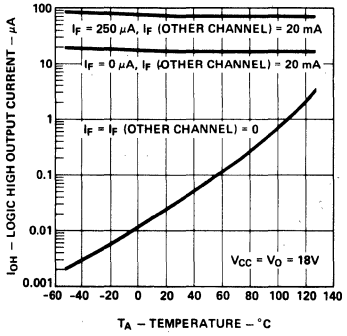


Figure 4. Logic High Output Current vs. Temperature.

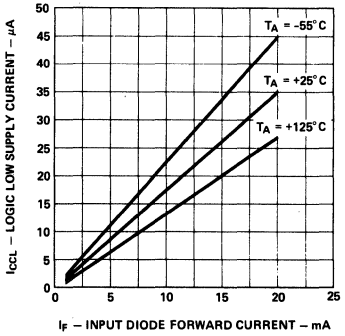


Figure 5. Logic Low Supply Current vs. Input Diode Forward Current.

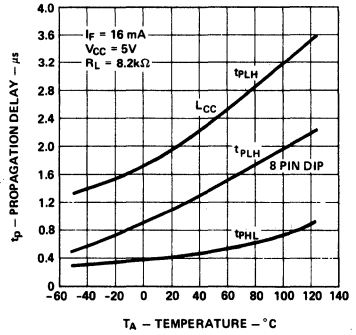


Figure 6. Propagation Delay vs. Temperature.

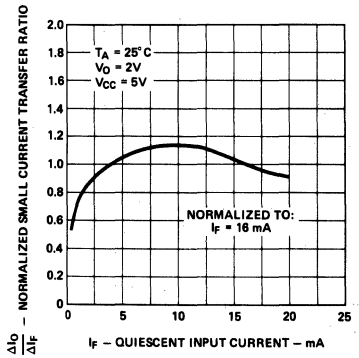
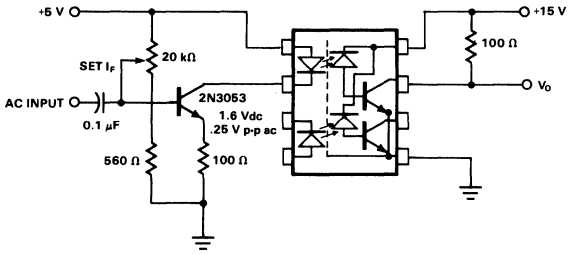
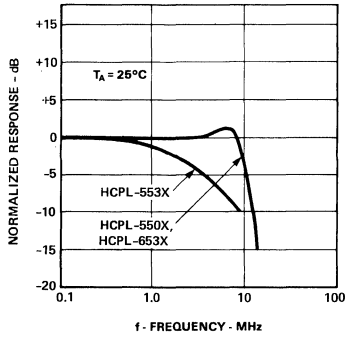


Figure 7. Normalized Small Signal Current Transfer Ratio vs. Quiescent Input Current.





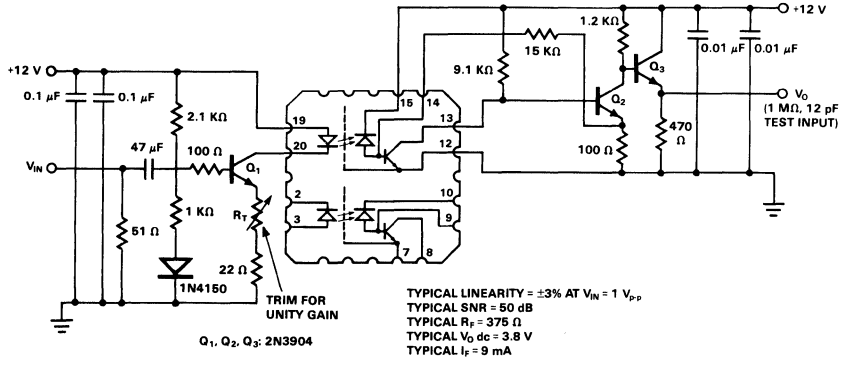


Figure 8. Frequency Response.

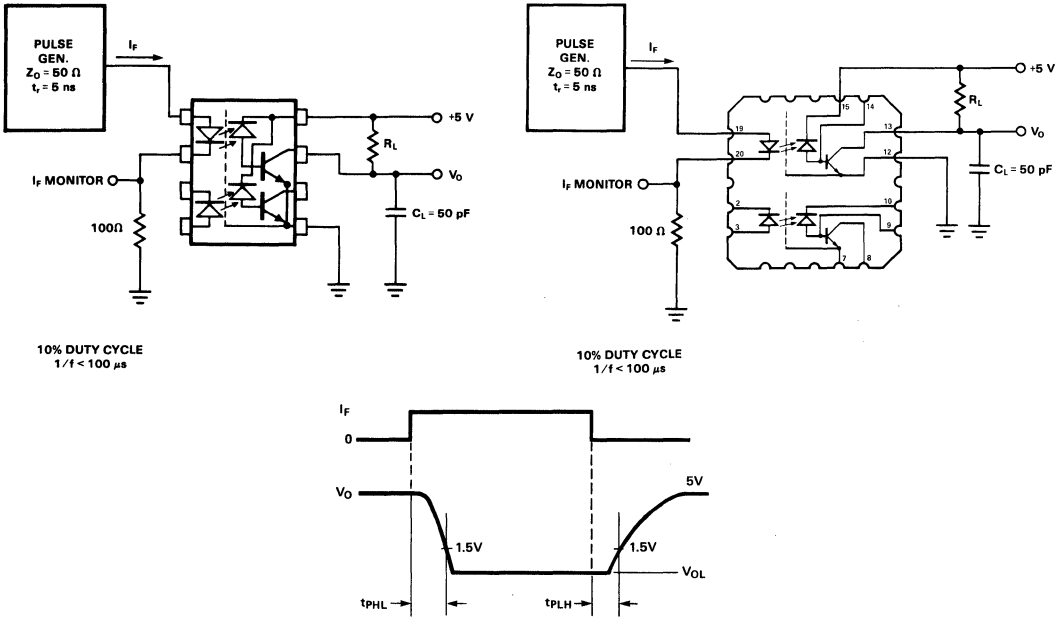


Figure 9. Switching Test Circuit.

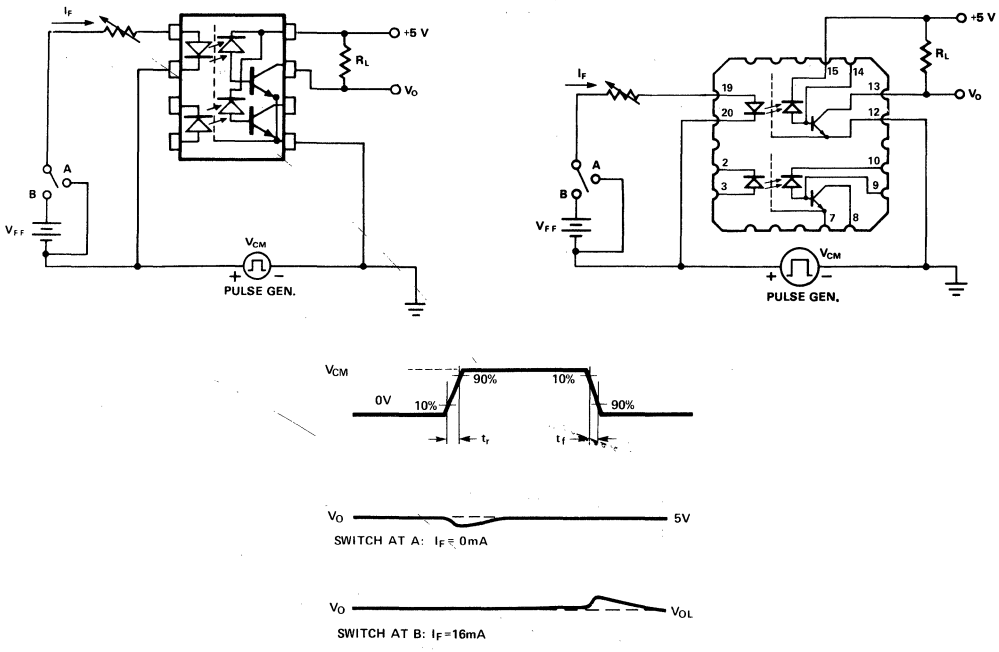
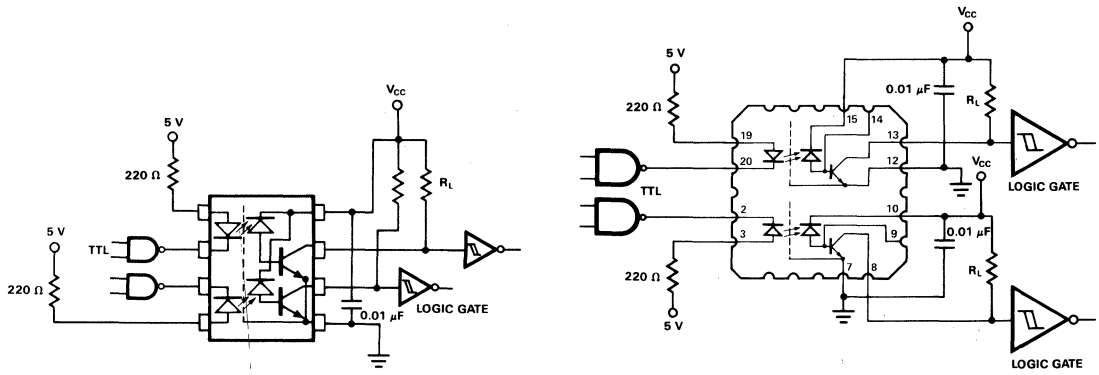


Figure. 10. Test Circuit for Transient Immunity and Typical Waveforms.



LOGIC FAMILY	LSTTL	CMOS	
DEVICE NO.	54LS14	CD40106BM	
V_{CC}	5V	5V	15 V
R_L 5% TOLERANCE	18 KΩ*	8.2 KΩ	22 KΩ

*THE EQUIVALENT OUTPUT LOAD RESISTANCE IS AFFECTED BY THE LSTTL INPUT CURRENT AND IS APPROXIMATELY 8.2 KΩ

This is a worst case design which takes into account 25% degradation of CTR. See App. Note 1002 to assess actual degradation and lifetime.

Figure 11. Recommended Logic Interface.

MIL-STD-883 Class B Test Program

Hewlett-Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC drawing 5962-87679 for the equivalent H.P. Optocoupler.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883.

Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration–Condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C, and D.
Group A–See table below for specific electrical tests.
Group B–No change.
Group C–No change.
Group D–Constant Acceleration–Condition A not E.

Part Numbering System

Commercial Product	Class B Product
HCPL-5500	HCPL-5501
HCPL-5530	HCPL-5531
HCPL-6530	HCPL-6531

Group A – Electrical Tests Quantity/Accept No. = 116/0

Single and Dual Channel Product	Dual Channel Product
Subgroup 1 Static tests at T_A = 25°C – I_{OH}, I_{CCL}, I_{CCH}, B_{VR}, V_F, I_{I-O} and CTR*	I_{OH1}
Subgroup 2 Static tests at T_A = +125°C – I_{OH}, V_F, I_{CCL}, I_{CCH}, B_{VR} and CTR*	I_{OH1}
Subgroup 3 Static tests at T_A = -55°C – I_{OH}, V_F, I_{CCL}, I_{CCH}, B_{VR} and CTR*	I_{OH1}
Subgroup 4, 5, 6, 7, 8A and 8B These subgroups are not applicable to this device type.	
Subgroup 9 Switching tests at T_A = 25°C – t_{PHL}, t_{PLH}*	
Subgroup 10 Switching tests at T_A = +125°C – t_{PHL}, t_{PLH}*	
Subgroup 11 Switching tests at T_A = -55°C – t_{PHL}, t_{PLH}*	

*Limits and conditions per Electrical Characteristics

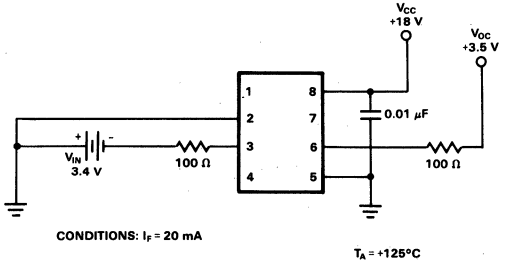


Figure 12. Single Channel Operating Circuit for Burn-In and Steady State Life Tests.

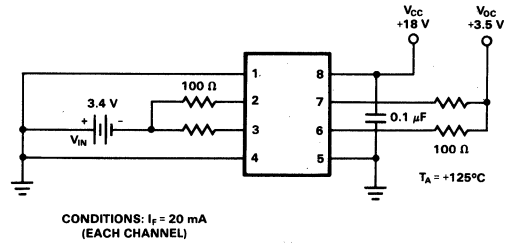


Figure 13. Dual Channel Operating Circuit for Burn-In and Steady State Life Tests.

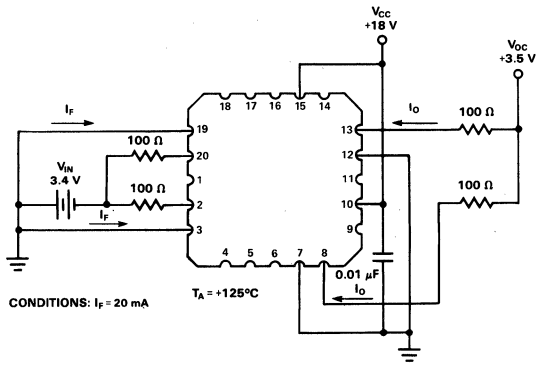
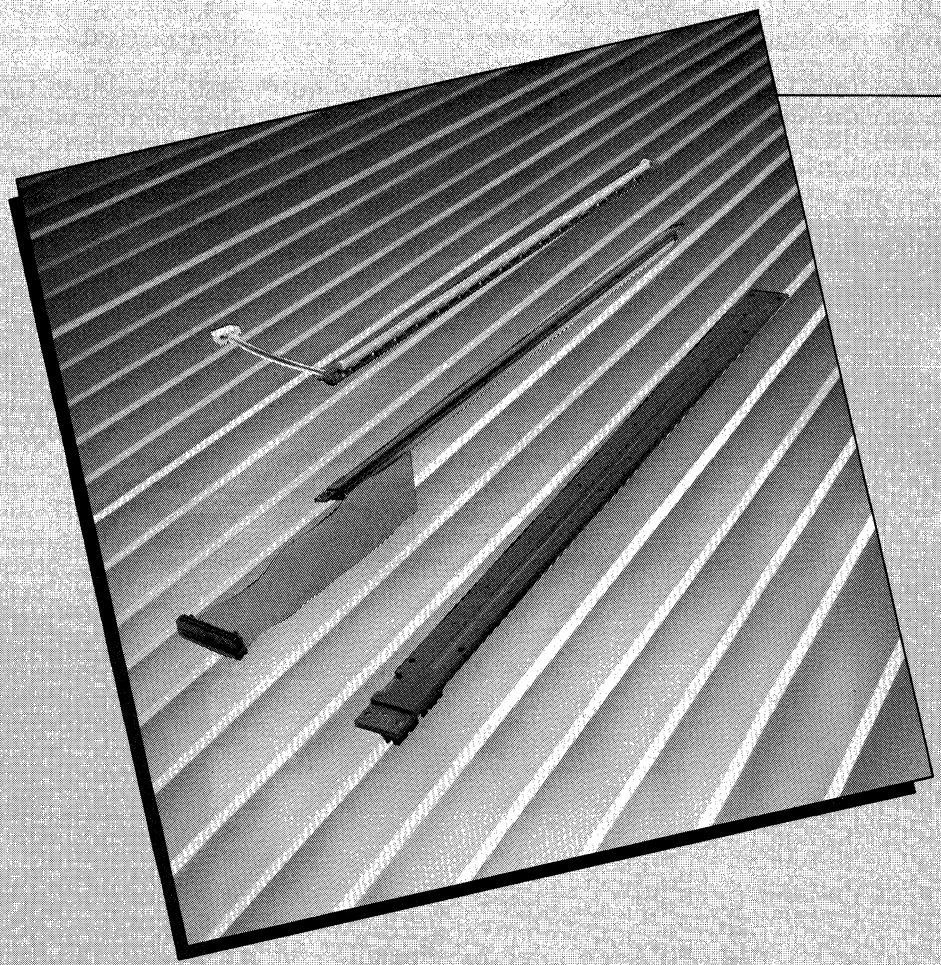


Figure 14. Operating Circuit for Burn-In and Steady State Life Tests.

HEWLETT PACKARD

Electrophotographic Products



Electrophotographic Products

Hewlett-Packard's Electrophotographic Products consist of LED Printheads and LED Erase Bars which are used to expose the image and to erase the image, respectively, on the photoreceptor in Non-Impact Plain Paper Printers, Copiers, and FAX machines using the Electrophotographic process.

LED Printheads

The LED Printhead can replace the Laser which is the principal part of the Raster Output Scanner (ROS) system of the electrophotographic non-impact printers (NIP). The choice of using either a laser or a LED Printhead is dictated by the speed, cost, and performance trade-offs. Some of the advantages of LED Printheads include:

1. Compact size
2. High speed, high power capability
3. No moving parts, solid state reliability
4. Wavelength can be modified as a special option to match the photoreceptor characteristics
5. Precise pixel placement, registration

Hewlett-Packard's binary LED Printheads are a series of compact, efficient, uniform, linear LED arrays with on-board integrated data registers and precise LED drivers. These HP printheads are suitable for use in electrophotographic NIPs, digital copiers, universal office machines, and FAX machines. HP offers its binary LED Printheads in common LED array lengths of 8.5 inches (A4 size) and 12 inches (A3 size).

The resolution choices are 300 DPI (8.5 and 12 inch LED array lengths), 406 DPI (12 inch length), and 480 DPI (12 inch length) where DPI is Dots Per Inch. For these LED Printheads, HP uses a modular design construction consisting of tiles aligned and mounted on a mother substrate to form a single LED row of thousands of pixels. The exact number of pixels depends on the length and resolution (DPI) of the printhead. A precision aligned SELFOC® array lens can be rigidly mounted over the LED linear array of thousands of pixels to focus the LED light output power (LOP) onto the photoreceptor of the electrophotographic machine. The A4 size 300 DPI printhead is supplied with a mounted SLA-20 SELFOC®lens. The A3 size 300 DPI, 406 DPI and 480 DPI printheads are supplied without a SELFOC®lens, but the lenses can be added as a special option.

Table 1 gives some of the optical/electrical parameters and characteristics of HP's LED Printheads.

*SELFOC® is a registered trademark of Nippon Sheet Glass Co., Ltd.

Table 1. Optical/Electrical Characteristics at T_A = 25°C.

Type of LED Printhead	Length of LED Array (mm)	Number of LED Pixels	Light Peak Wavelength (nm) (See Note 1)	Radiant Output Intensity (see Note 2) (μW/sr/pixel)	Radiant Output Intensity Variation	Max. Clock Frequency (MHz)	LED Supply Voltage (volts)	Nominal Operating Current (mA/pixel)
300 DPI	219	2592	660 ± 10	3-6	See Note 3	10	5 ± 5%	5
300 DPI	303	3584	685 ± 8	6-8	See Note 4	10	5 ± 5%	4
406 DPI	304	4864	685 ± 8	6-8	See Note 4	10	5 ± 5%	4
480 DPI	298	5632	685 ± 8	6-8	See Note 4	10	5 ± 5%	4

[SELFOC® – Registered trademark of Nippon Sheet Glass Co. Ltd.]

Notes:

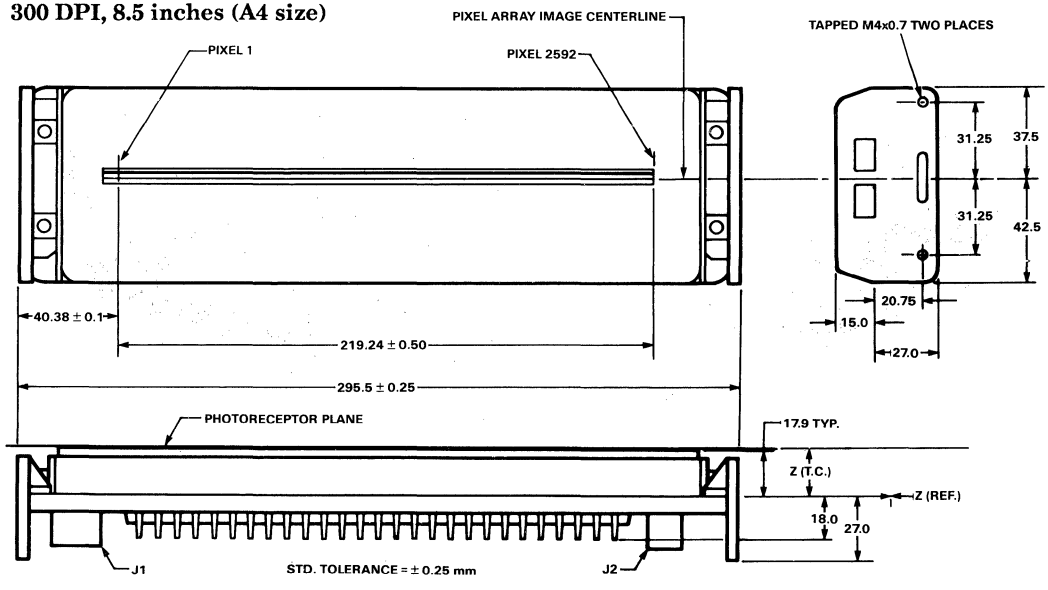
1. The wavelength can be changed in special options.
2. Far-field measurement with a glass cover over the LED array but without a mounted SELFOC® lens.
3. **Intensity Variation** — **Max Values**
   (a) Pixel intensity variation ±20%
   (b) Group intensity variation ±10%
   (average of 4 pixels versus adjacent group of 4)
   Eg. LED 1, 2, 3, 4, vs. 5, 6, 7, 8
   vs. 9, 10, 11, 12 ...
4. **Intensity Variation** — **Max Values**
   (a) Pixel intensity variation ±20%
   (b) Group intensity variation ±8%
   (average of 8 pixels versus adjacent group of 8)
   Eg. LED 1, 2, 3, 4, 5, 6, 7, 8
   vs. 9, 10, 11, 12, 13, 14, 15, 16
   vs. 17, 18, 19, 20, 21, 22, 23, 24

Custom Options Available

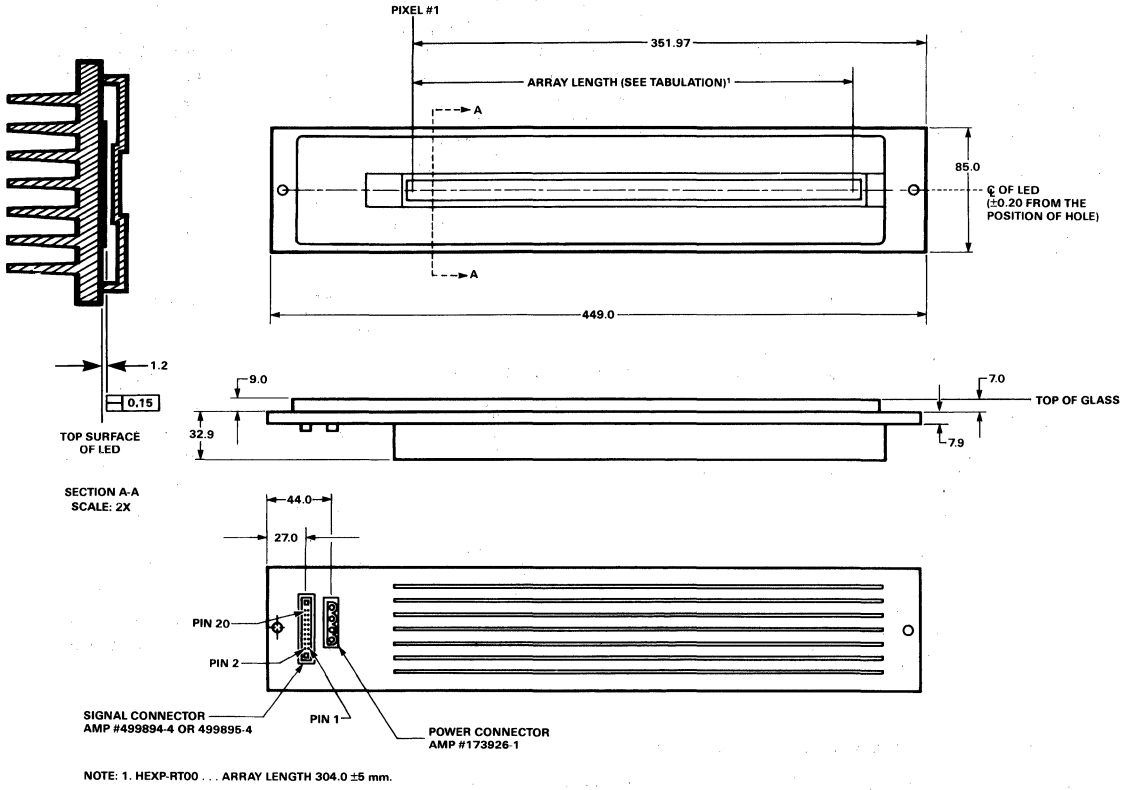
1. Upon request, the following wavelengths are available: 660 nm and 710 nm for the A4 size 300 DPI; 660 nm, 685 nm and 710 nm for the A3 size 300 DPI, 406 DPI and 480 DPI LED Printheads.
2. "With/without" lens options and different types of lens options (SLA-20, SLA-12) are offered upon request for the LED Printheads.

Outline Drawings of LED Printheads

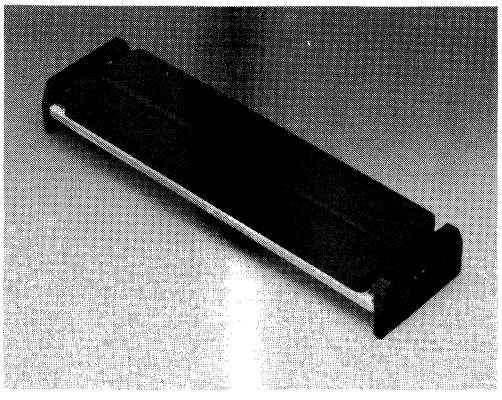
300 DPI, 8.5 inches (A4 size)



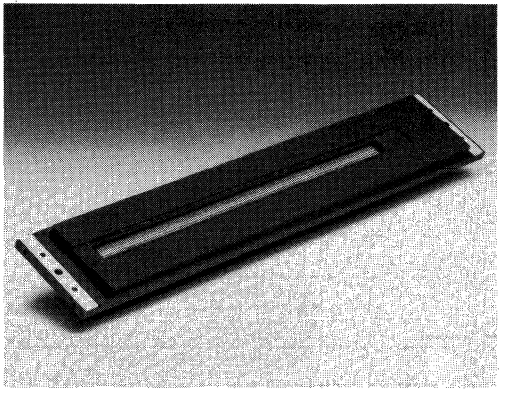
300 DPI, 406 DPI, 480 DPI (All are 12 inches – A3 size)



NOTE: 1. HEXP-RT00 . . . ARRAY LENGTH 304.0 ±5 mm.



300 DPI, 8.5 inches (A4 size)



300 DPI, 406 DPI, 480 DPI
12 inches (A3 size)

Future LED Printheads

The following types of LED Printheads are in product development at Hewlett-Packard. Please contact your local Hewlett-Packard field sales engineer for more information.

1. Large format: 2 foot and 3 foot binary LED Printheads.
2. Grayscale 400 DPI LED Printheads with the following features:
   a. 64 levels of gray (6 bits)
   b. ±2% accuracy of exposure
   c. Exposed length of 306 mm (12 inches) or 4820 pixels
   d. Built in Light Output Power Monitor
3. Narrow Profile Options

LED Erase Bars

The LED Erase Bar is an ideal illuminator source which is finding widespread application in the copiers and printers which use the electrophotographic process. Some of the advantages of LED Erase Bars include:

1. High reliability.
2. Uniformity of light output
3. Compact size
4. Low voltage/low power
5. Addressability – Segmented and fully addressable erase bars allow precise, electronic control of which pixels are illuminated.
6. Patented optical design – HP's design tailors the pixel's beam profile for optimal performance.
7. Variety of wavelengths – The LED wavelength can be chosen to best match a photoreceptor's sensitivity.
8. On-Board electronics – For high-density addressable erase bars, on-board custom LED driver ICs simplify the electronics interface.

HP offers 3 families of LED Erase Bars:

Type of Erase Bar	Erase Function	Choices of Wavelength Emitted by Erase Bar (nm)
1. On/Off	Pre-clean, Pre-transfer, Interdocument	655, 635, 610, 565
2. Addressable, Segmented, 10 DPI	Interdocument, Edge Fade Out, Edit	655, 635, 610, 565
3. High Resolution, 25 DPI, OBIC	Edit, Color highlight	655

Hewlett-Packard LED Erase Bars employ a hybrid construction consisting of LED dice, electronic components and optical elements in a compact assembly. The light from each LED pixel is focused to a sharp image at the specified working distance. This HP patented optical technique maintains high uniformity and very low stray light.

Table 2 gives some of the optical/electrical parameters and characteristics of HP's LED Erase Bars.

Table 2. Optical/Electrical Characteristics at T_A = 25°C.

Type of LED Erase Bar	Length of LED Array (mm)	Number of LED Pixels	Light Peak Wavelength (nm) (See Note 1)	Typical Light Output (see Notes 2 & 3)	Transverse Beam Width (mm)	Detector Height Above LED Array (mm)	Radiant Output Intensity Variation	LED Drive Condition	Test Current per LED mA/LED
On/Off	312	120	655 635 610 565	1700 µW/cm 450 µW/cm 130 µW/cm 95 µW/cm	3	4	±10%	22.5 Vdc	25 dc
10 DPI Addressable	310	124	655 635 610 565	500 µW/cm 175 µW/cm 50 µW/cm 40 µW/cm	2.7	1.05	±30%	Multiplex	12 avg.
25 DPI Addressable	358	352	655	800 µW/cm²	1.1	1.5	±45%	Digital	5 dc

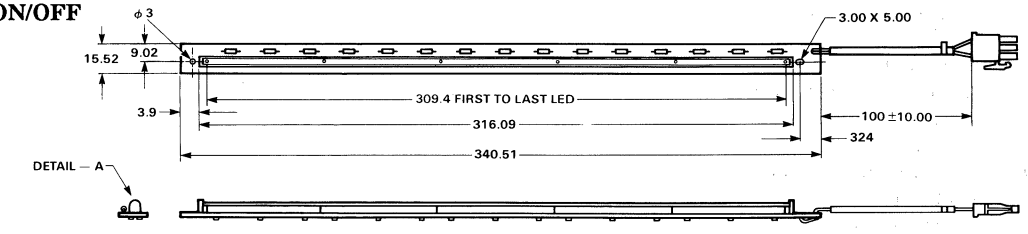
Notes:
1. As of this writing, not all products are released in all the wavelengths shown.
2. The light output figures for on/off and 10 DPI addressable bars are given in µW/cm. This is the total radiometric flux emitted per unit of length of the bar. It is typically measured using a 1 mm x 20 mm slit detector oriented perpendicular to the length of the erase bar.
3. The light output figure for 25 DPI addressable bars is an irradiance measurement, specified in µW/cm². This figure is computed by dividing the total flux emitted from a pixel by the area of its square projected image. That image area is defined by the 50% peak power points at the specified detector height above the LED array.

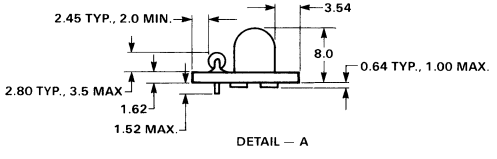
Custom Options Available

HP can design and manufacture custom LED Erase Bars to different optical/electrical specifications and/or different mechanical designs from the ones shown. Please furnish a drawing and specification to your local HP field sales engineer.

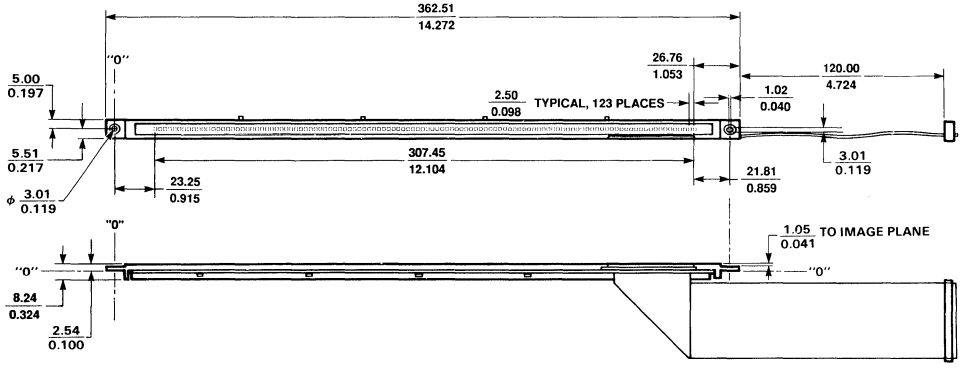
Outline Drawings of LED Erase Bars

ON/OFF

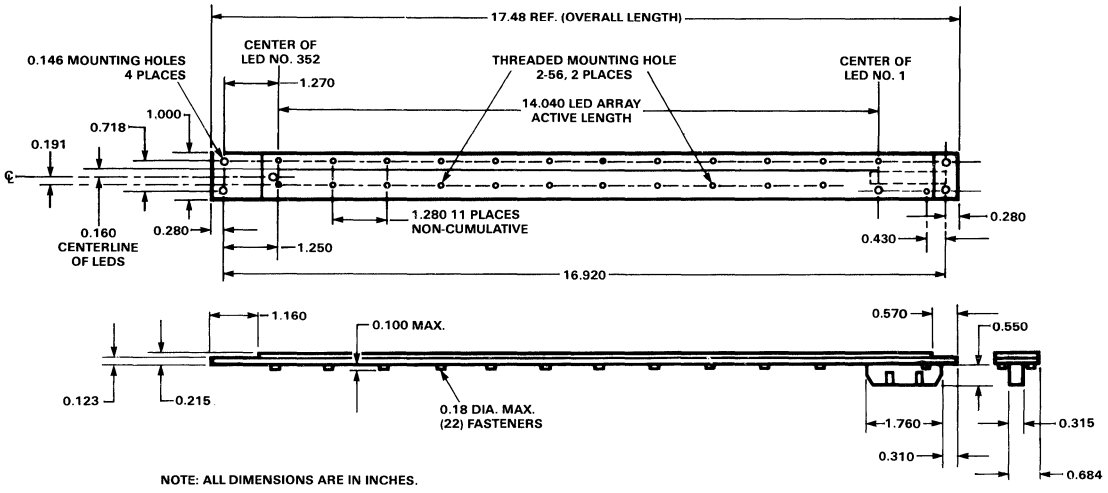




10 DPI Addressable



25 DPI Addressable

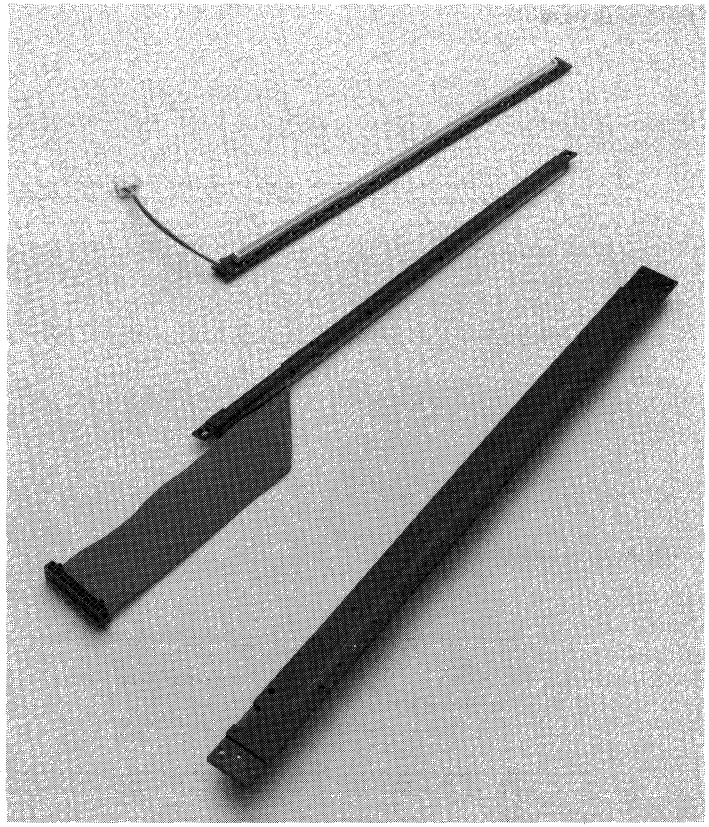


NOTE: ALL DIMENSIONS ARE IN INCHES.

Future LED Erase Bars

The following types of LED Erase Bars are in product development at Hewlett-Packard. Please contact your local Hewlett-Packard field sales engineer for more information.

1. Future LED Erase Bar designs driven by customers' needs.
2. Anticipated variations including length, on-board electronics, optical performance, narrower mechanical profiles.



HEWLETT PACKARD

406 DPI LED Optical Printhead

Technical Data

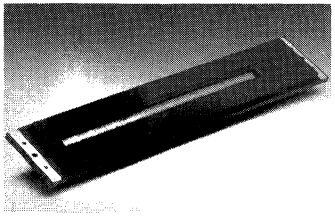
HEXP-RT00

Features

- **High Optical Power and Efficiency**
- **Electronically Trimmed and Programmed to Guarantee Excellent Uniformity**
- **Designed to Write Image or Background**
- **Noise Tolerant Interface**
- **High Data Input Rates**
- **Custom Wavelengths Available**

Applications

- **Electrophotographic printers to over 100 pages/ minute**
- **High performance editing copiers**
- **Universal printer/copiers**
- **High performance facsimile printers**
- **General purpose optical Raster Output Systems**



Description

The HEXP-RT00 represents a 12" LED optical binary printhead. Each printhead consists of:

- A 4864 x 1 array of LED pixels at a 406 dpi resolution
- Four serial data line inputs
- A differential line interface

Special Options:

- 660 nm and 710 nm peak wavelengths are available upon request
- A selfoc lens can be provided upon request

Reliable operation in high speed applications is achieved by a combination of conservative thermal design, efficient LED materials, careful design of power distribution, and use of individual precision current source drivers.

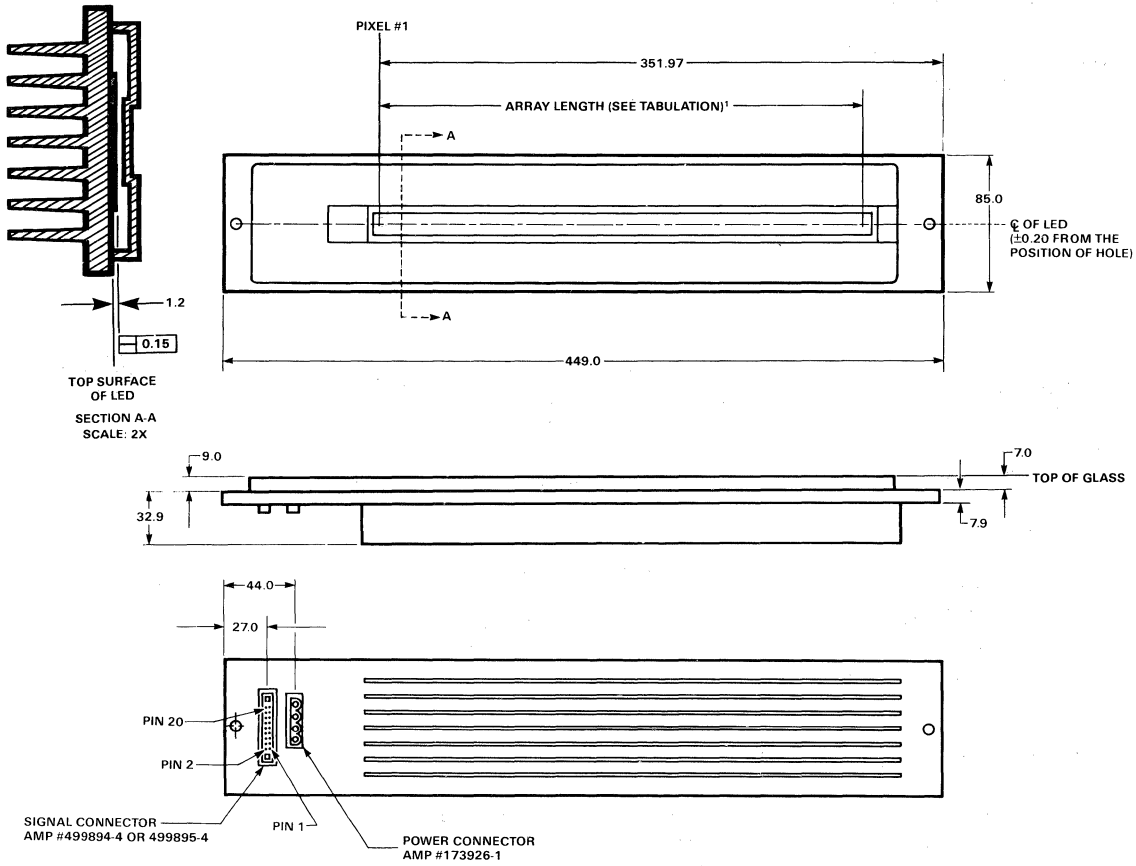
Selection Guide

406 dpi (16 dots/mm) Resolution
11.97 inches (304 mm) Image Width

685 nm Wavelength	HEXP-RT00

ELECTROPHOTOGRAPHIC PRODUCTS

Mechanical Drawing



NOTE: 1. HEXP-RT00 . . . ARRAY LENGTH 304.0 ±5 mm.

Mechanical Characteristics

Emitter Parameters	
Emitter Size	40 µm ± 6 µm x 50 µm ± 6 µm
Emitter Pitch	62.5 µm ± 5 µm
Number of Emitters	4864
Emitter Tolerances	
Emitter Pitch Error	
a. Xe Chip to Chip	± 10 µm
b. Ye Chip to Chip	25 µm Max
c. Ye Over Entire Head	150 µm Max
Emitter Height Error	
a. Ze Chip to Adjacent Chip	25 µm
b. Ze Max to Min Over Entire Head	150 µm

Orientation and Conventions

A. Printhead Orientation

CONNECTOR J1: DIGITAL SIGNALS
CONNECTOR J2: POWER AND GROUND

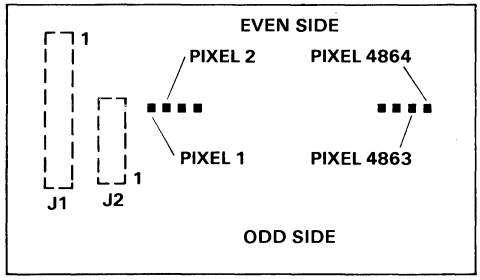


Figure 1: Printhead Top Side View

B. Connector Location and Orientation

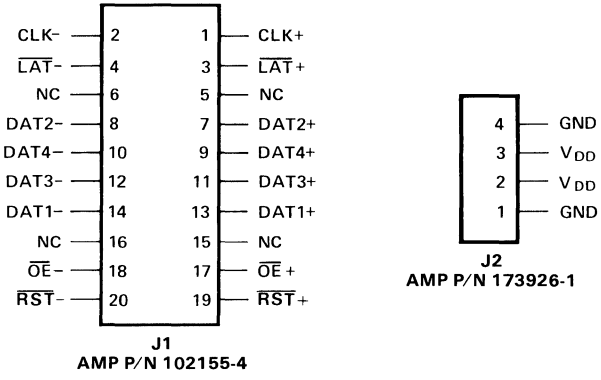


Figure 2: Connector Pinout Top Side View

Specifications Summary

Absolute Maximum Ratings*

All voltages referenced to Gnd. Driver Outputs Not Enabled.

Supply Voltage, V_{DD} ..... -0.3 to 6.0 V
Input Voltage, Any Pin to Ground ..... -0.3 to V_{DD} + 0.3 V
Maximum Operating Duty Factor 38%
Free Air Operating Temperature Range, T_A ..... +15°C to +43°C
Operating Humidity (Non-condensing) ..... 5% to 90% RH
Storage Temperature Range, T_S ..... -30°C to +65°C at 50% max RH

*Permanent device failure may occur if parts are stressed beyond these limits. Device reliability may be affected by extended exposure to absolute maximum ratings. Functionality at or above these limits is not guaranteed.

Recommended Operating Conditions*

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage[1]	V_{DD}	4.75	5.0	5.25	V

*Recommended operating conditions define the limits between which the functionality of the product is guaranteed.

Note:
1. Power supply rise time to be less than 10 ms.

Optical Characteristics*

Output Characteristics (V_{DD} = 5.0 V)	HEXP-RT00
Light Wavelength	685 ± 8 nm
Average Printhead Intensity	6.0 µW/sr/pixel Min 8.0 µW/sr/pixel Typical

*Unless specified otherwise, T_A = 25°C and V_{DD} = 5.0 volts.

Intensity Variation	Max Values
Pixel Intensity Variation	±20%
Group Intensity Variation (Average of 8 pixels vs. adjacent group of 8)	±8%
Maximum Load Intensity Variation (One pixel on to same pixel with all pixels on at time = 0^+)	±2%
Thermally Induced Average Intensity Variation (Average intensity at time = 0^+ and T_A = 25°C, compared to average intensity at thermal equilibrium, 1/3 on, 38% DF, T_A = 43°C, and minimum air flow = 600 liters/min)	±10%

*Unless specified otherwise, T_A = 25°C and V_{DD} = 5.0 volts.

DC Characteristics Over Operating Range*

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Supply Current (All pixels on)	I_{DD}			35[1]	A, peak
Pixel Current	I_{pix}		4	7	mA, peak
Input Differential Voltage (CLK±, $\overline{\text{LAT}}$±, $\overline{\text{OE}}$± and DATA±) and RST±					
Hi Level (V+ - V-)	V_{TH}			200	mV
Lo Level (V- - V+)	V_{TL}	-200			mV
Input Current into V+ (CLK±, $\overline{\text{LAT}}$±, and DATA±)					
V+ = V_{CC}, V- = Gnd	Iih	44	50	56	mA
V+ = Gnd, V- = V_{CC}	Iil	-56	-50	-44	mA
Input Current into V+ $\overline{\text{OE}}$					
V+ = V_{CC}, V- = Gnd	Iih	44	50	56	mA
V+ = Gnd, V- = V_{CC}	Iil	-61	-55	-49	mA
Input Current into V+ RST					
V+ = V_{CC}, V- = Gnd	Iih	.1	.25	.6	mA
V+ = Gnd, V- = V_{CC}	Iil	-3	-5	-7	mA
Hysteresis	Vhys		50		mV

*Unless specified otherwise, min/max limits apply across the temperature range and supply voltage range. All typical values are for T_A = 25°C and V_{DD} = 5.0 volts.

Note:

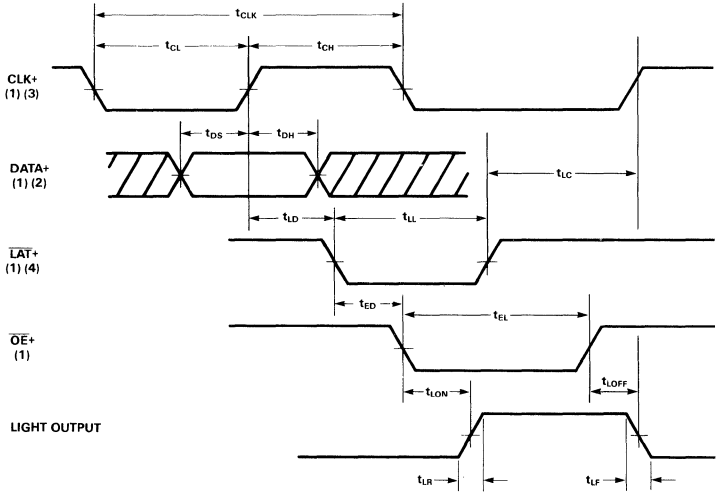
1. Maximum peak current at thermal equilibrium (T_A = 43°C, DF = 38%, 1/3 pixels on and a minimum air flow of 600 liters/minute.

AC Switching Characteristics Over Operating Range*

Parameter	Symbol	Minimum	Typical	Maximum	Units
CLK Period	t_{CLK}	100			ns
CLK Frequency	f_{CLK}			10	MHz
CLK Hold High Time	t_{CH}	45	50	55	ns
CLK Hold Low Time	t_{CL}	45	50	55	ns
Data Setup Time Prior to CLK	t_{DS}	25			ns
Data Hold Time After CLK	t_{DH}	25			ns
$\overline{\text{LAT}}$ Active Delay After CLK	t_{LD}	25			ns
$\overline{\text{LAT}}$ Inactive Before CLK	t_{LC}	25			ns
$\overline{\text{LAT}}$ Hold Low Time	t_{LL}	50			ns
$\overline{\text{OE}}$ Active Delay After LAT	t_{ED}	25			ns
$\overline{\text{OE}}$ Active Low Time	t_{EL}			50	ms
Light Output Delay After $\overline{\text{OE}}$ Active	t_{LON}			300	ns
Light Output Delay After $\overline{\text{OE}}$ Disable	t_{LOFF}			300	ns
Light Output Rise Time	t_{LR}			200	ns
Light Output Fall Time	t_{LF}			200	ns

*Unless specified otherwise, min/max limits apply across the temperature range and supply voltage range. All typical values are for T_A = 25°C and V_{DD} = 5.0 volts.

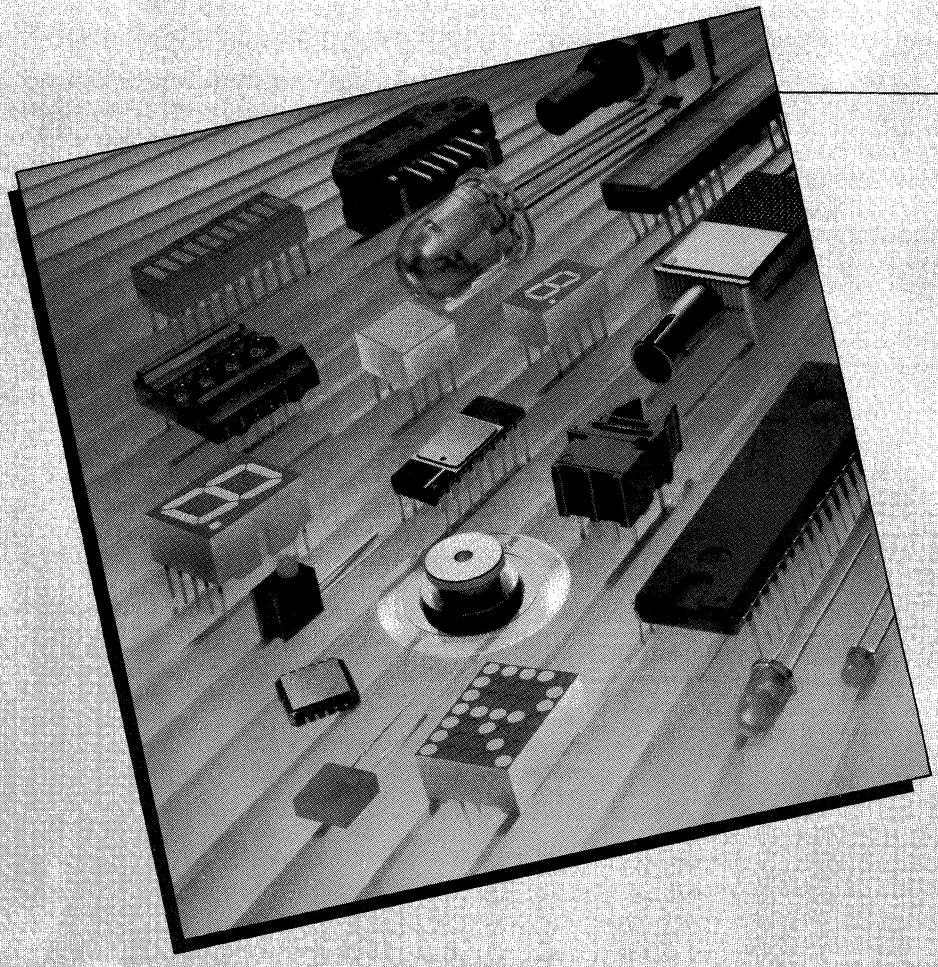
Timing Diagram



(1) CLK-, DATA-, $\overline{\text{LAT}}$- AND $\overline{\text{OE}}$- HAVE INVERTED WAVEFORMS.
(2) DATA+ IS REPRESENTATIVE OF DAT1+, DAT2+, DAT3+ AND DAT4+.
(3) POSITIVE EDGE-TRIGGERED SIGNAL.
(4) LEVEL-SENSITIVE SIGNAL.

HEWLETT PACKARD

Applications



Applications

Because technology is growing and changing so rapidly, HP's commitment to customers includes an extensive applications department. In an effort to anticipate design needs and answer design questions, this team of engineers has published a complete library of applications literature.

All of the Application Notes, Bulletins and Technical Briefs listed here, are available from your local HP Sales Office or nearest HP Components Authorized Distributor or Representative (see section 9), or by calling our Customer Information Center at 1-800-752-0900.

Motion Sensing & Control Products

AN 1011
Design and Operational Considerations for the HEDS-5000 Incremental Shaft Encoder
This application note is directed toward the system designer using the HEDS-5000 and HEDS-6000 modular incremental shaft encoders. First the note briefly analyzes the theory of design and operation of the HEDS-5000 and HEDS-6000. A practical approach to design considerations and an error analysis provide an in depth treatment of the relationship between motor mechanical parameters and encoding error accumulation. Several design examples demonstrate the analysis techniques presented. Operation considerations for assembly, test, trouble shooting and repair are presented. Finally, some circuits and software concepts are introduced which will be useful in interfacing the shaft encoder to a digital or microprocessor based system. Appendix A summarizes the uses and advantages of various encoder technologies while Appendix B provides guidance for selecting DC motors suitable for use with the HEDS-5000 and HEDS-6000.

Ordering No. 5953-9393

AN 1025
Applications and Circuit Design for the HEDS-7500 Series Digital Potentiometer
This application note demonstrates some of the uses for the Hewlett-Packard HEDS-7500 series digital potentiometer, explains how a digital potentiometer works, and explains some of the advantages of a digital potentiometer over a standard resistive potentiometer. In addition, this application note provides some examples of circuitry which will interface the digital potentiometer to a microprocessor, and provides mechanical design considerations and available options for the HEDS-7500 series digital potentiometer.

Ordering No. 5954-8485

AN 1032
Design of the HCTL-1000's Digital Filter Parameters by the Combination Method
Digital closed loop motion control systems employing a dedicated IC as a controller are becoming increasingly popular as a solution to the need for controlled velocity and positioning systems. Hewlett-Packard's HCTL-1000 is a general purpose motion control IC which has been designed for this type of closed loop systems. A digital compensator has been designed into the HCTL-1000 to provide a stable response to an input command. This application note explains how the combination method can be used for calculation of the HCTL-1000's digital compensation filter parameters to provide a stable, closed loop position control system.

Ordering No. 5954-8455

Light Bars & Bar Graph Arrays

AN 1007
Bar Graph Array Applications
This application note begins with a description of the manufacturing process used to construct the 10 element array. Next is a discussion of the package design and basic electrical configuration and how they affect designing with the bar graph array. Mechanical information including pin spacing and wave soldering recommendations are made.

Display interface techniques of two basic types are thoroughly discussed. The first of these two drive schemes is applicable in systems requiring display of analog signals in a bar graph format. The second major drive technique interfaces bar graph arrays in systems where the data is of a digital nature. Examples of microprocessor controlled bar graph arrays are presented.

Summarized for the design engineer are tables of available integrated circuits for use with bar graph arrays. Finally, a list of recommended filters is included.

Ordering No. 5953-0452

AN 1012
Methods of Legend Fabrication
Hewlett-Packard LED Light Bar Modules inscribed with fixed messages or symbols can be used as economical annunciators. Annunciators are often used in front panels to convey the status of a system, to indicate a selected mode of operation, or to indicate the next step in a sequence. This application note discusses alternative ways the message or symbols (legends) can be designed. A selection matrix is provided to assist in the selection of the most appropriate method of legend fabrication. Each fabrication method is explained in detail along with mounting and attachment techniques. Finally, prevention of cross-talk is discussed for legend areas of a multi-segmented light bar.

Ordering No. 5953-0478

Solid State Lamps

AB 74
Option 002 Tape and Reel LED Lamps
Hewlett-Packard Option 002 tape and reel LED lamps have straight leads on standard 2.54 mm (0.100 inch) center spacing. These lamps may be auto-inserted into printed circuit boards with most radial auto-insertion equipment. However, it is important to have the proper plated through hole size and spacing, in the printed circuit to assure high insertion yields.

This application bulletin details the specific information on the printed board plated through hole size, spacing, and tolerances necessary to assure high insertion yields of Option 002 LED lamps with 0.46 mm (0.018 inch) square leads.

Ordering No. 5954-8402

AN 1005
Operational Considerations for LED Lamps and Display Devices
In the design of a display system which incorporates LED lamps and display devices, the objective is to achieve an optimum between light output, power dissipation, reliability, and operating life. The performance characteristics and capabilities of each LED device must be known and understood so that an optimum design can be achieved. The primary source for this information is the LED device data sheet. The data sheet typically contains Electrical/Optical Characteristics that list the performance of the device and Absolute Maximum Ratings in conjunction with characteristic curves and other data which describe the capabilities of the device. A thorough understanding of this information and its intended use provides the basis for achieving an optimum design. This application note presents an in-depth discussion of the theory and use of the electrical and optical information contained within a data sheet. Two designs using this information in the form of numerical examples are presented, one for dc operation and one for pulsed (strobed) operation.

Ordering No. 5953-0419

AN 1017
LED Solid State Reliability
Light emitting diode display technology offers many attractive features including multiple display colors, sunlight readability, and a continuously variable intensity adjustment. One of the most common reasons that LED displays are designed into an application, however, is the high level of reliability of the LED display. Hewlett-Packard has taken a leadership role in setting reliability standards for LED displays and documenting reliability performance.

This note explains how to use the reliability data sheets published for HP LED indicators and displays. It describes the LED indicator and display

packages, defines device failures, and discusses parameters affecting useful life, failure rates, and mechanical test performance.

Ordering Number 5953-7784

AN 1021
Utilizing LED Lamps Packaged on Tape and Reel
Hewlett-Packard offers many of its LED lamps packaged on tape and reel for radial insertion by automatic equipment during high volume production of PC board assemblies.

This application note is a guide to the use of tape and reel LED lamps in the automatic insertion process. Discussed are the LED lamp tape and reel configuration, the radial lead insertion process, PC board design considerations, a method to maintain LED lamp alignment during soldering, and lamp stand-off height information.

AN 1027
Soldering LED Components
The modern printed circuit board is assembled with a wide variety of semiconductor components. These components may include LED lamps and displays in combination with other components. The quantity of solder connections will be many times the component count. Therefore, the solder connections must be good on the first pass through the soldering process. The effectiveness of the soldering process is a function of the care and attention paid to the details of the process. It is important for display system designers and PC board assembly engineers to understand the aspects of the soldering process and how they relate to LED components to assure high yields.

This application note provides an in-depth discussion on the aspects of the soldering process and how they relate to LED lamps and display components, with the objective of being to serve as a guide towards achieving high yields for solder connections.

Ordering No. 5954-0893

AN 1028
Surface Mount Subminiature LED Lamps
Modern printed circuit boards are being assembled with surface mounted components, replacing through hole mounted components in many traditional applications. Hewlett-Packard has surface mount options for its HLMP-6000/7000 series of subminiature LED lamps, Options 011 and 013 for "gull wing" leads, and Option 021 for "yoke" leads, for inverted mounting.

This application note provides information on how to surface mount and vapor phase reflow solder these surface mount subminiature LED lamps.

Ordering No. 5954-0902

Solid State Displays

AN 1006
Seven Segment LED Display Applications
This application note begins with a detailed explanation of the two basic product lines that Hewlett-Packard offers in the seven segment display market. This discussion includes mechanical construction techniques, character heights, and typical areas of application. The two major display drive techniques, dc and strobed, are covered. The resultant tradeoffs of cost, power, and ease of use are discussed. This is followed by several typical instrument applications including counters, digital voltmeters, and microprocessor interface applications. Several different microprocessor based drive techniques are presented incorporating both the monolithic and the large seven segment LED displays.

The application note contains a discussion of intensity and color considerations made necessary if the devices are to be end stacked. Hewlett-Packard has made several advances in the area of sunlight viewability of LED displays. The basic theory is discussed and recommendations made for achieving viewability in direct sunlight. Information concerning display mounting, soldering, and cleaning is presented. Finally, an extensive set of tables has been compiled to aid the designer in choosing the correct hardware to match a particular application. These tables include seven segment decoder/drivers, digit drivers, LSI chips designed for use with LEDs, printed circuit board edge connectors, and filtering materials.

Ordering No. 5953-0439

AN 1015
Contrast Enhancement Techniques for LED Displays
Contrast enhancement is essential to assure readability of LED displays in a variety of indoor and outdoor ambients. Plastic filters are typically used for contrast enhancement with indoor lighting and glass circular polarized filters are typically used to achieve readability in sunlight ambients.

This application note discusses contrast enhancement technology for both indoor and outdoor ambients, the theory of Discrimination Index and provides a list of tested contrast enhancement filters and filter manufacturers.

Ordering No. 5953-7788

AN 1016
Using the HDSP-2000 Alphanumeric Display Family
The HDSP-2000 family of alphanumeric display products provides the designer with a variety of easy-to-use display modules with on board integrated circuit drivers. The HDSP-2000 family has been expanded to provide three display sizes with character heights ranging from 3.8 mm (0.15 in.) to 6.9 mm (0.27 in.), four display colors, and both commercial and military versions. These displays can be arranged to create both single line and multiple line alphanumeric panels.

This note is intended to serve as a design and application guide for users of the HDSP-2000 family of alphanumeric display devices. It covers the theory of the device design and operation, considerations for specific circuit designs, thermal management, power derating and heat sinking, and intensity modulation techniques.

Ordering No. 5953-7787

AN 1026
Designing with Hewlett-Packard's Smart Display – the HPDL-2416
The trend in LED Alphanumeric displays is to simplify a designer's job as much as possible by incorporating on board character storage, ASCII character generation, and multiplexing within the display. The HPDL-2416 is a four character alphanumeric display which incorporates a 64 character ASCII decoder and an on board CMOS IC to perform these functions. This application note is intended to serve as a design and application guide for users of the HPDL-2416. The information presented will cover electrical description, electrical design considerations, interfacing to micro-processors, preprogrammed message systems, mechanical and electrical handling, and contrast enhancement.

Ordering No. 5954-0886

AN 1029
Luminous Contrast and Sunlight Readability of the HDSP-238X Series LED Alphanumeric Displays for Military Applications
Military specifications for avionics and other kinds of electronics that require readability in sunlight use specific definitions for luminous contrast. The concept of chrominance contrast and the theory of Discrimination Index (see Hewlett-Packard Application Note 1015) are not used by the military as a means of determining readability in sunlight. Thus, the military requirements for readability in sunlight are based solely on luminous contrast measurements. This application note discusses the luminous contrasts used by military specifications, describes anti-reflection/circular polarized filters designed for use with the HDSP-238X series sunlight viewable LED displays, and presents luminous contrast data for various HDSP-238X display/filter combinations.

Ordering No. 5954-0923

AN1030
LED Displays and Indicators and Night Vision Imaging System Lighting
This application note introduces the concept of night vision imaging. It discusses GEN II and GEN III ANVIS and Cat's Eyes night vision goggles. NVG compatibility problems and compatible lighting objectives for aircraft cockpits are discussed. It illustrates the use of NVG filters with high performance green and yellow LEDs to obtain NVG compatibility. Various aspects of MIL-L-85762A, as they apply to LEDs, are discussed. Calculated NVIS Radiance values are presented for high performance green and yellow LED/NVG/DV filter combinations. A discussion of the U.S. Army's NVG Secure Lighting Program and the objectives of the CECOM SOW are included. Information on dimming LED displays is presented. Daylight readability with NVG/DV filters is also discussed.

Ordering No. 5954-2245

AN 1031
Front Panel Design
In many applications designers are faced with the problem of how to match the perceived brightness of an assortment of seven segment displays, light bars, linear arrays, and lamps on the same front panel. To simplify this problem Hewlett-Packard has introduced S02 option selected parts. S02 option selected parts provide a restricted range of luminous intensity for a given part number. This application note is written as a design guide to matching the perceived brightness of LED displays and lamps on a front panel. The procedure shown in the application note will enable the designer to calculate the needed display drive currents (either dc or pulsed) for a given ambient light level and specified filter. Two technques are explained. The first is how to calculate the drive currents to insure minimum acceptable brightness. The second is how to calculate the drive currents to match the display on the front panel to a known display.

Ordering No. 5954-0933

AN 1033
Designing with the HDSP-211X Smart Display Family
Hewlett-Packard's smart alphanumeric display, the HDSP-211X, is built to simplify the user's display design. Each HDSP-211X has an onboard CMOS IC which displays eight characters. All of the IC features are software driven. These features include 128 character ASCII decoder, 16 user-defined symbols, seven brightness levels, flashing characters, a self test, and all of the circuitry needed to decode, drive, and refresh eight 5 x 7 dot matrix characters.

This application note discusses how to interface the HDSP-211X display to either a Motorola 6808 or an Intel 8085 microprocessor. A 32 character display interface is explained for each microprocessor. The note includes a detailed description of the hardware and software. The software illustrates how the user-defined symbols and a string of ASCII characters are loaded into the display.

Ordering No. 5954-8424

AN 1039
Dimming HDSP-213X Displays to Meet Night Vision Lighting Levels
Abstract
For normal operation, the seven programmable dimming levels available with the HDSP-213X military grade displays are sufficient. However, the displays must be dimmed well below the lowest available on-board programmable dimming level to meet the requirements for night vision imaging system (NVIS) lighting. This application note describes a circuit that will dim HDSP-213X displays to luminance levels sufficient to meet NVIS lighting requirements.

Ordering No. 5952-0708

Fiber Optics

AB 65
Using 50/125 μm Optical Fiber with Hewlett-Packard Components
Applications Bulletin 65 explains factors that influence the power coupled into various fiber diameters and numerical apertures. Test results showing coupled power from HP LED sources into 100/140 μ metre and 50/125 μ metre fiber are included.

Ordering No. 5953-9370

AB 71
200-μm PCS Fiber with Hewlett-Packard Fiber-Optic Transmitters and Receivers
A description of the properties of 200-μm PCS fiber is given and the performance when used with Hewlett-Packard fiber optic components is described in the form of graphs and tables.

Ordering No. 5954-1021

AB 73
Low-cost Fiber-Optic Transmitter and Receiver Interface Circuits
This bulletin provides assistance in designing circuits to interface Hewlett-Packard HFBR-0400 low-cost miniature fiber-optic components with TTL I/O for applications at data rates up to 35 MBD. The TTL T_X/R_X circuits presented in this applications bulletin have been designed, built, and tested. They are suitable for a wide range of applications. The HFBR-0400 fiber-optic components are compatible with either SMA or ST style connectors. The concepts illustrated in this bulletin are applicable to both types.

Ordering No. 5954-8415

AB78
Low-Cost Fiber-Optic Links for Digital Applications up to 150 MBd
The HFBR-2406 and HFBR-2416 are high-speed, low-cost linear light-to-voltage converters with typical bandwidths of 125 MHz. These components can be used to make fiber-optic links for both analog and digital applications. Since the range of possible uses is so varied, this Application Bulletin concentrates on a specific digital application. The application is one of the most prevalent for the HFBR-24X6: the transmission of encoded digital signals, otherwise known as run-length limited* data.

Ordering No. 5954-8478

AN 1022
High Speed Fiber-Optic Link Design with Discrete Components
As the technology of fiber-optic communication matures, design considerations for large volume applications focus as much on cost and reliability as bandwidth and bit-error-rate. This application note describes a 100 MBd fiber-optic communication link which was implemented with low-cost, non-exotic technology, including LED transmitter, PIN photodiode detector, off-the-shelf ICs, and discrete components, laid out on epoxy-glass circuit boards.

Ordering No. 5954-0979

AN 1035
Versatile Link
The Versatile Link Application Note describes how fiber optics can be used to solve different types of application problems, introduces Hewlett-Packard's Versatile Link plastic fiber-optic components, and shows how to design a working fiber-optic link using the Versatile Link. It also includes several additional application circuits to help the designer obtain maximum performance from the Versatile Link

Ordering No. 5954-2191

AN 1038
Low Cost Components for IEEE 802.3 Fiber-Optic Inter-Repeater Links
The HFBR-0400 family of low cost high performance components can be combined with inexpensive support circuits to construct the Fiber-Optic Inter-Repeater Links (FOIRL) described in the IEEE 802.3 standard. The recommendations shown in this Application Note can also be used to construct 20 MBd optical links which are suited for a variety of point-to-point data communication applications.

Ordering No. 5954-2215

TB 101
Fiber-Optic SMA Connector Technology
Technical Brief 101 discusses tradeoffs between various SMA connector techniques and provides a contact matrix of manufacturers versus SMA connector type.

Ordering No. 5954-1004

TB 102
Fiber/Cable Selection for LED Based Local Communications Systems
Technical Brief 102 is intended to assist the first time user of fiber optics with the selection of a fiber cable that best meets desired system requirements. Issues discussed in Technical Brief 102 include: Tradeoffs between various fiber types, the effect of LED emitters on fiber performance, coupled power versus numerical aperture and factors that influence cable selection. A contact matrix that lists fiber cable manufacturers versus cable type is also included.

Ordering No. 5954-1004

TB 104
Baseband Video Transmission with Low Cost Fiber-Optic Components
The transmission of video signals over fiber-optic links offers several advantages relative to comparable wire distribution systems. Technical Brief 104 describes simple T_x/R_x circuits providing 20 MHz, 3 dB bandwidth for high resolution analog video transmission.

Ordering No. 5954-1025

TB 105
ST Connector/Cable Guide
A fairly recent development by AT&T is the ST* Connector, and its rapid acceptance by users of fiber-optic components is an indication that it may soon become a standard connector.

Technical Brief 105 provides a quick comparison between the SMA and the ST style connector. A table at the end lists some suppliers of the ST style connectored cables.

Ordering No. 5954-8436

Optocouplers

AN 69
CMOS Circuit Design Using Hewlett-Packard Optocouplers
Within this application bulletin are CMOS isolation interface circuits for use with the various low input current, Hewlett-Packard optocouplers, specifically, the HCPL-2200/ 2300/2731 and 6N139 devices. Advantages of and recommendations for different input and output circuit configurations are given in tabular form for low power operation at various signalling rates.

Ordering No. 5953-9384

AN 947
Digital Data Transmission Using Optically Coupled Isolators
Optocouplers make ideal line receivers for digital data transmission applications. They are especially useful for elimination of common mode interference between two isolated data transmission systems. This application note describes design considerations and circuit techniques with special emphasis on selection of line drivers, transmission lines, and line receiver termination for optimum data rate and common mode rejection. Both resistive and active terminations are described in detail. Specific techniques are described for multiplexing applications, and for common mode rejection and data rate enhancement.

Ordering No. 5954-7759

AN 951-1
Applications for Low Input Current, High Gain Optocouplers
Optocouplers are useful in line receivers, logic isolation, power lines, medical equipment, and telephone lines. This note discusses use of the 6N138/9 series high CTR optocouplers in each of these areas.

Ordering No. 5953-8430

AN 951-2
Linear Applications of Optocouplers
Although optocouplers are not inherently linear, the separate photodiodes used in Hewlett-Packard optocouplers provide better linearity as well as higher speed of response than phototransistor detectors.

Linearity enhancement by use of paired optocouplers is described with specific circuit examples offering DC-to-25 KHz response. These examples illustrate the relative merits of differential and servo techniques.

A circuit with linear AC response to 10 MHz is also described for analog optocouplers having the photodiode terminals externally accessible.

Digital techniques of voltage-to-frequency conversion and pulse width modulation are discussed. Their linearity is quite independent of optocoupler linearity but require use of high speed optocouplers for low distortion.

Ordering No. 5954-8430

AN 1002
Consideration of CTR Variations in Optocoupler Circuit Designs
A persistent, and sometimes crucial, concern of designers using optocouplers is that of the current transfer ratio, CTR, changing with time. The change, or CTR degradation, must be accounted for if long, functional lifetime of a system is to be guaranteed. This application note will discuss a number of different sources for this degradation.

Ordering No. 5953-7799

AN 1004
Threshold Sensing for Industrial Control Systems with the HCPL-3700 Interface Optocoupler
Interfacing from industrial control systems to logic systems is a necessary operation in order to monitor system progress. This interfacing is found if process control systems, programmable controllers, microprocessor subsystems which monitor limit and proximity switches, environmental sensors and ac line status; in switching power supplies for detection of ac power loss; in power back up systems which need an early warning of power loss in order to save special microprocessor memory information or switch to battery operation, etc. Applications of the HCPL-3700 interface optocoupler are addressed in this note. The isolation and threshold detection capability of the HCPL-3700 allows it to provide unique features which no other optocoupler can provide. Addressed in this note are the advantages of using this optocoupler for isolating systems as well as the device characteristics, dc/ac operational performance with

and without filtering, simple calculations for setting desired thresholds, and four typical application examples for the HCPL-3700. Additional coverage is given to protection considerations for the optocoupler from the standpoint of power transients, thermal conditions, and electrical safety requirements of the industrial control environment.

Ordering No. 5953-0406

AN 1018
Designing with the HCPL-4100 and HCPL-4200 Current Loop Optocoupler
Digital current loops provide unique advantages of large noise immunity and long distance communication at low cost. Applications are wide and varied for current loops, but one of the critical concerns of a loop system is to provide a predictable, reliable, and isolated interface with the loop. The HCPL-4100 (transmitter) and HCPL-4200 (receiver) optocouplers provide for easy interfacing to and from a current loop with minimal design effort. Within this application note a complete description of the HCPL-4100/4200 devices is given along with applications for digital, 20 mA, simplex, half duplex, and full duplex loops. These loops can be either point-to-point or multidrop configurations. Factors which affect data performance are discussed. Circuit arrangements with specific data performance are given in graphical and tabular form.

Ordering No. 5953-9359

AN 1023
Radiation Immunity of Hewlett-Packard Optocouplers
Opening with a quotation from MIL-HDBK-279 describing optocouplers containing photodiodes as superior to optocouplers containing phototransistors, the text describes the properties of ionizing radiation (particles and photons) and how it affects the performance of optocouplers. Graphs show degradation of CTR (Current Transfer Ratio) in the 6N140 as a function of gamma total dose (up to 1000 rad [Si] and as a function of total neutron fluence (up to 6 x 1012 n/cm2). A table gives radiation hardness requirements for various military requirements.

Ordering No. 5954-1003

AN 1024
Ring Detection with the HCPL-3700 Optocoupler
With the increased use of modems, automatic phone answering equipment, private automatic branch exchange (PABX) systems, etc., low-cost, reliable, isolated ring detection becomes important to many electronic equipment manufacturers. This application note addresses the definition of ringing requirements (U.S.A. and Europe), applications of the HCPL-3700 optocoupler as a simple, but effective, ring detector. A design example is shown with calculations to illustrate proper use of the HCPL-3700. Features which are integrated into the HCPL-3700 provide for predictable detection, protection and isolation when compared to other optocoupler techniques.

Ordering No. 5954-1006

AN 1036
Solid State Relay Introduction and Applications
A brief opening describes SSRs (Solid State Relays), their advantages relative to EMRs (Electro Magnetic Relays); and their classification according to contact characteristics. There follows a description of HSSR-8200 "control" and "contact" properties. Arrangement of the contacts for signal switching, multiplexing, gain switching, and low-level sensing are discussed. Circuit suggestions and design rules are given for operation of the "control" LED. Schematics and design rules for overvoltage protection of the open contacts are presented.

Ordering No. 5954-2200

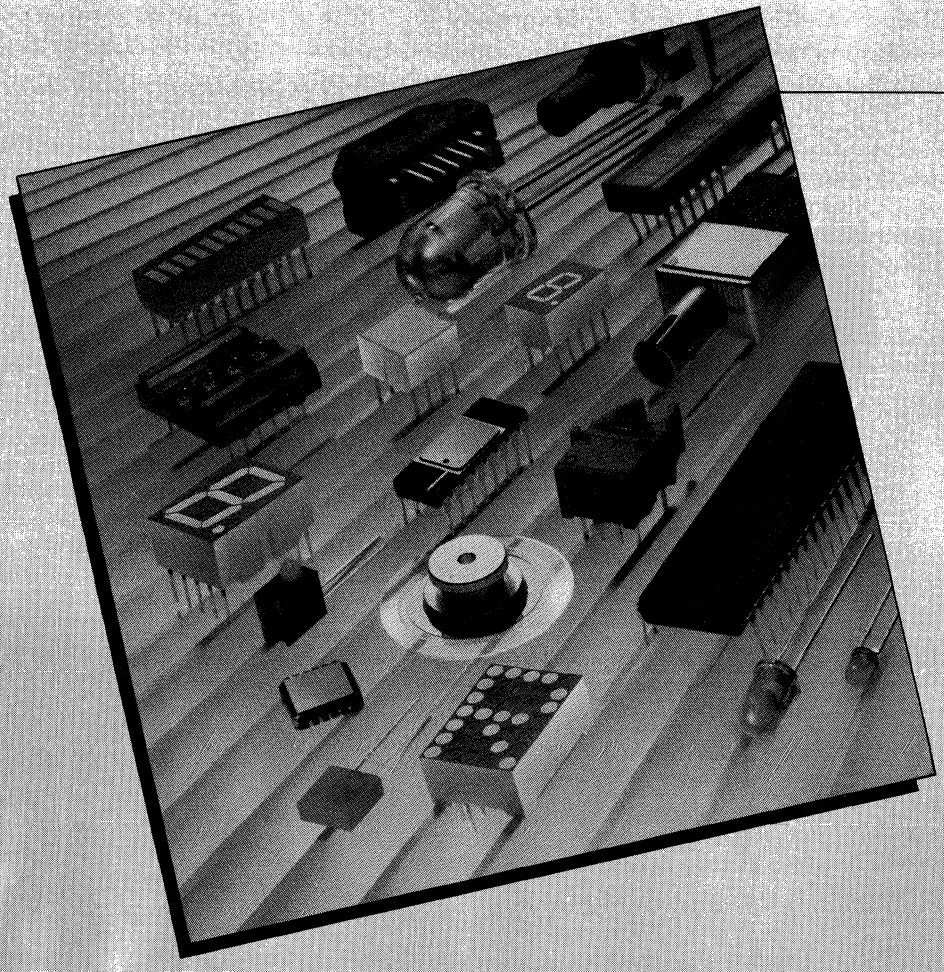
TB 103
High Speed Optocouplers vs. Pulse Transformers
For high speed signaling with Ground loop isolation, pulse transformers are often used. Here are summarized briefly the difficulties encountered in the use of pulse transformers, such as rise-time, sag, and interwinding capacitance. A table summarizes the parameters of Hewlett-Packard optocouplers designed for high speed signaling. A second table summarizes the advantages of using these optocouplers instead of pulse transformers.

Ordering No. 5954-1017

HEWLETT PACKARD

Appendix

- Ordering Information
- HP Components Authorized Distributor and Representative Directory
- HP Components U.S. Sales and Service Offices
- HP International Sales and Service Offices



Ordering Information, After Sales Service

How to Order

To order any component in this catalog or additional applications information, call the HP office nearest you and ask for a Components representative. A complete listing of the U.S. sales offices is on page 9-7; offices located outside of the U.S. are listed on page 9-8.

A world-wide listing of HP authorized distributors is on page 9-3. These distributors can offer off-the-shelf delivery for most HP components.

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Hall-Mark Electronics
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(516) 737-0600 (Long Island)

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933 Motor Park Way
Hauppauge 11788
(516) 434-7421

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2060 Town Line Road
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(716) 272-2729

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103 Twin Oaks Drive
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1065 Old Country Road
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120 Commerce Drive
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(716) 383-8020

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P.O. Box 1032
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Berkshire.
SL1 6LN
(0628-604422)

Farnell Electronic Components Limited,
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Leeds.
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Anglia Microwave,
Radford Way Business Centre,
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