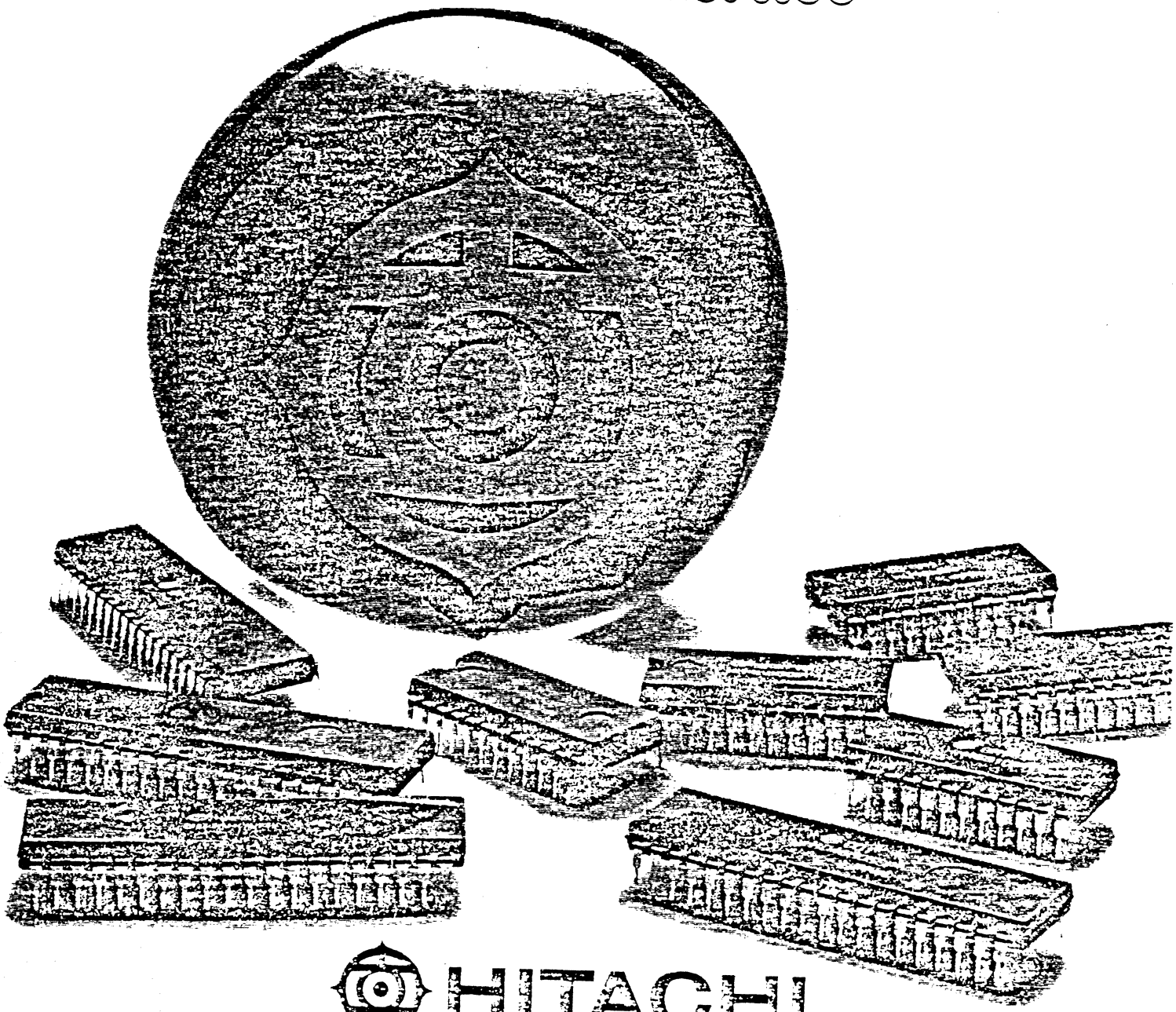
HLN 014

HD 46505R CRT CONTROLLER (CRTC) USERS MANUAL

- HITACHI MICROCOMPUTER SYSTEM HMCS 6800



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ABBREVIATIONS

AB	Address Bus
AR	Address Register
CG	Character Generator
CLK	Clock
CMP	Comparator
CRT	Cathode Ray Tube
CRTC	Cathode Ray Tube Controller
CUDISP	Cursor Display
DB	Data Bus
DEC	Decoder
DISPTMG	Display Timing
HSYNC	Horizontal Synchronization
LPSTB	Light Pen Strobe
MA	Refresh Memory Address
MPU	Micro Processor Unit
MPX	Multiplexer
RA	Raster Address
RM	Refresh Memory
RS	Register Select
VSYNC	Vertical Synchronization
P — S	Parallel-Serial Converter

1. Abstract

The CRTC is a LSI controller which is designed to provide an interface for microcomputers to raster scan type CRT displays. The CRTC belongs to the HMCS6800 LSI Family and has full compatibility with MPU in both data lines and control lines. Its primary function is to generate timing signal which is necessary for raster scan type CRT display according to the specification programmed by MPU. The CRTC is also designed as a programmable controller, so applicable to wide-range CRT display from small low-functioning character display up to raster type full graphic display as well as large high-functioning limited graphic display.

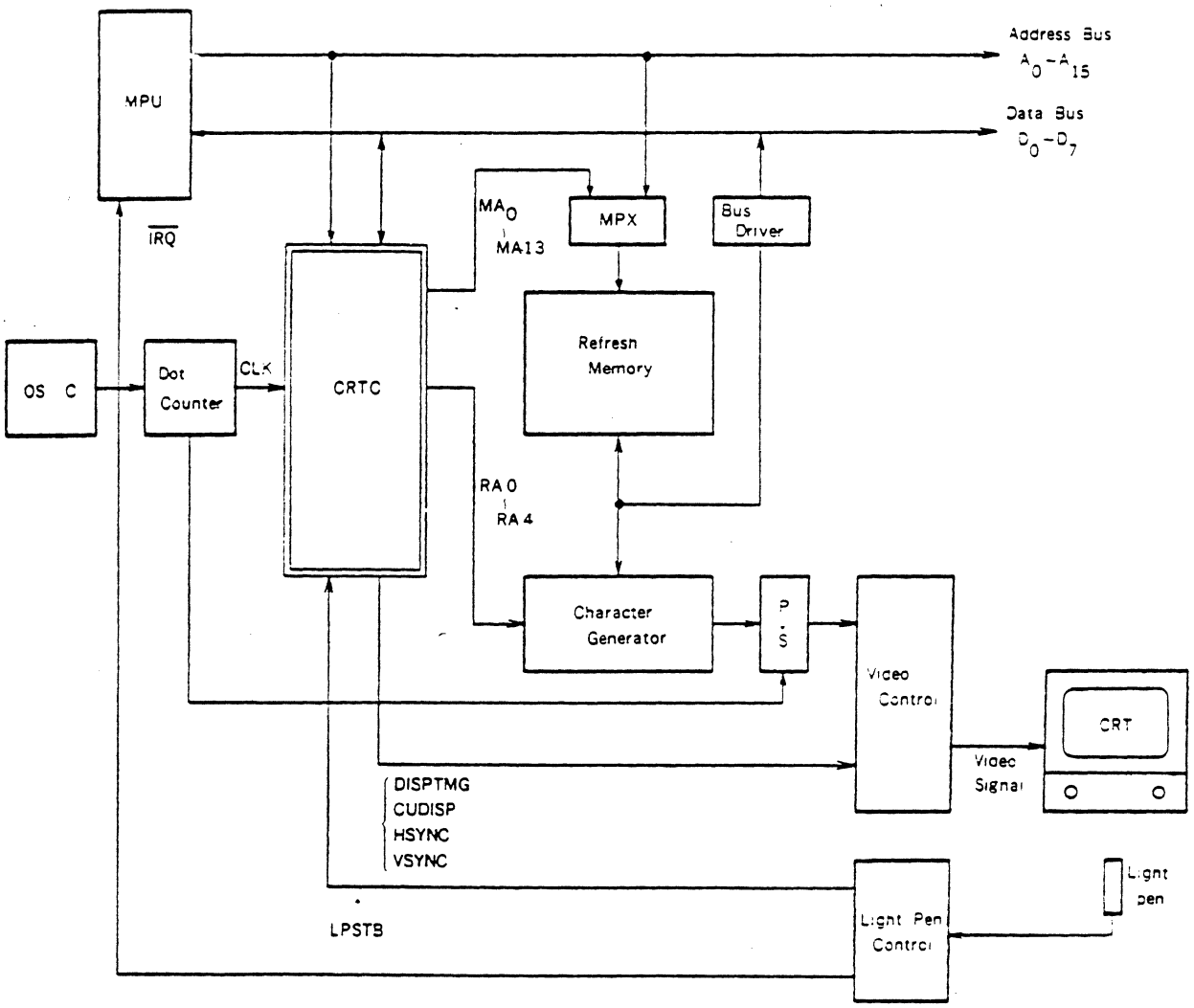


Fig. 1—1 Example of the CRTC Character Display System

2. Feature and Function

2.1 Features of the CRTC

(1) Number of displayed characters on the screen, vertical dot format of one character, horizontal and verzical sync signal, display timing signal are programmable.
(2) Line buffer-less refreshing.
(3) 14-bit refresh memory address output. (16K words max. access)
(4) Programmable interlace Non-interlace scan mode.
(5) Built-in cursor control function.
(6) Programmable cursor height and its blink.
(7) Built-in light pen detection function.
(8) Paging and scrolling capability.
(9) TTL compatible.
(10) Single + 5V power supply.

2.2 Function of the CRTC

Fig.2—1 Function of the CRTC

Item	Sub-item	Function	Remark
Function of the CRTC	Programmable screen format	Horizontal scan period	Programmable per one character period
		Vertical scan period(per.line)	Programmable perd one line period
		Vertical scan period(fine adjustment)	Progammable per one raster
		Number of characters per line	
		Number of lines per screen	
		Number of rasters per line	Vertical dot number of one character + line space
		Horizontal display position on CRT	Programmble output timing of sync signal
		Vertical display position on CRT	
		Pulse width of horizontal sync signal	
	Programmable cursor display	Cursor display position on screen	Built-in 14-bit cursor register
		Cursor height	
		Cursor blink and its Period	One choice between 16 fisld penod and 32 fisld penod
	Scan mode	Non-interlace mode	One choice
		Interlace mode	
		Interlace sync and video mode	
	Light pen	Built-in 14-bit light pen register	
	Refresh Memory Addressing	14-bit refresh memory address output	16K words max.refresh memory access
	Programmable Start Address	Built-in programmable 14-bit start address register on refresh memory	Paging & scrolling
Structure of the CRTC LSI		Single + 5V power supply	
		TTL compatible input/output	
		Directly connected bus with the HMCS 6800 Family	
		N-channel, Silicon-Gate E/D MOS	
		Full static operation of internal logic	
		40 pin DIL package	
Application of the CRTC (Expansibility)		Character display	Alphanumeric, kanji & other characters
		Limited(simple)graphic display	Figure display(raster scan display)
		Full graphic display	
		Color display, blink of displayed characters	
		Cluster control	

3. CRT Display System

3.1 Principle of Raster Scan System

Raster scan system is the system where an electron beam, which is deflected according to a certain rule, hits against the fluorescent screen of CRT and forms a frame. An ordinary CRT display device forms a frame by deflection of an electron beam by saw wave electric current (or voltage) like a common TV set. This system is shown in Fig. 3-1.

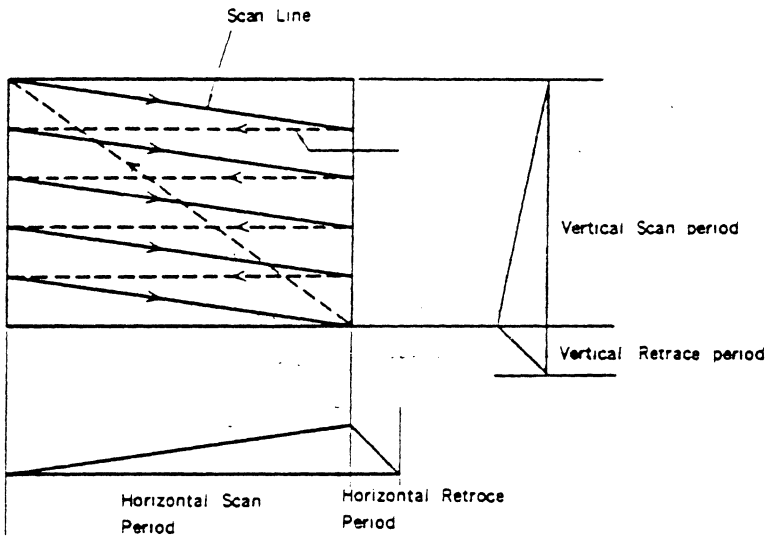


Fig. 3—1 Raster Scan System(Non-interlace)

One frame is composed both of horizontal scan from left to right and of vertical scan from top to bottom to move vertical position. Solid lines in Fig. 3-1 are called scan period (or display period), and broken lines are called retrace period. In this system, increase in frame number per sec enables to lessen its flickering. Increase in scan line per frame enables a high resolution. In an ordinary display device, frame number between 50 and 60 per sec is used. Besides the scan system shown in Fig. 3-1, there is another scan system called interlace scan system, which is used for a TV set, etc. As shown in Fig. 3-2, each latter half scan is located in the middle of its former scans. Two-time vertical scans (odd and even number fields) form one frame. The CRTC is designed to be able to deal with the scan system (interlace mode) shown in Fig. 3-2 as well as the scan system shown in Fig. 3-1 (non-interlace mode).

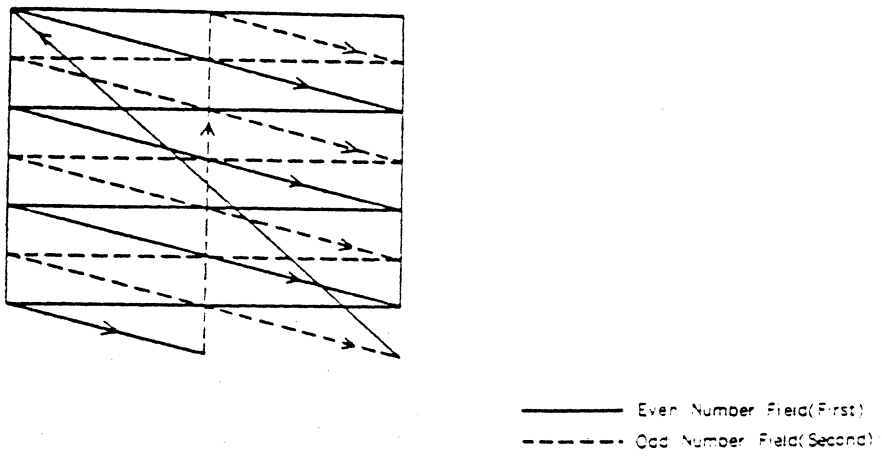


Fig. 3—2 Raster Scan System(Interlace)

3.2 Principle of Character Display System

Principle of character display is shown in Fig. 3-3. In order to keep characters displayed on CRT screen, it is always necessary to repeat scans and refresh them. To do this, an ordinary CRT display device adopts a method that data to be displayed is stored in memory and screen is refreshed according to its contents. Here, the memory which stores data for display is called Refresh Memory. Data is written on Refresh Memory by data processing system including MPU. The data is written in ASCII code, so it cannot be displayed as characters. It is necessary to convert the character code into the character pattern. The converter is called Character Generator. Fig. 3-4 shows the principle on which the character code is converted into the character pattern. Character Generator is a kind of ROM which generates the character pattern from the character code and the scan line number as address. Normally one dot period of characters is only several ten ns. To generate the character pattern, it is necessary to read the character dot per row or per column in parallel and to convert into serial. Now 5 x 7, or 7 x 9 dot matrix format is widely used for display of alphanumeric.

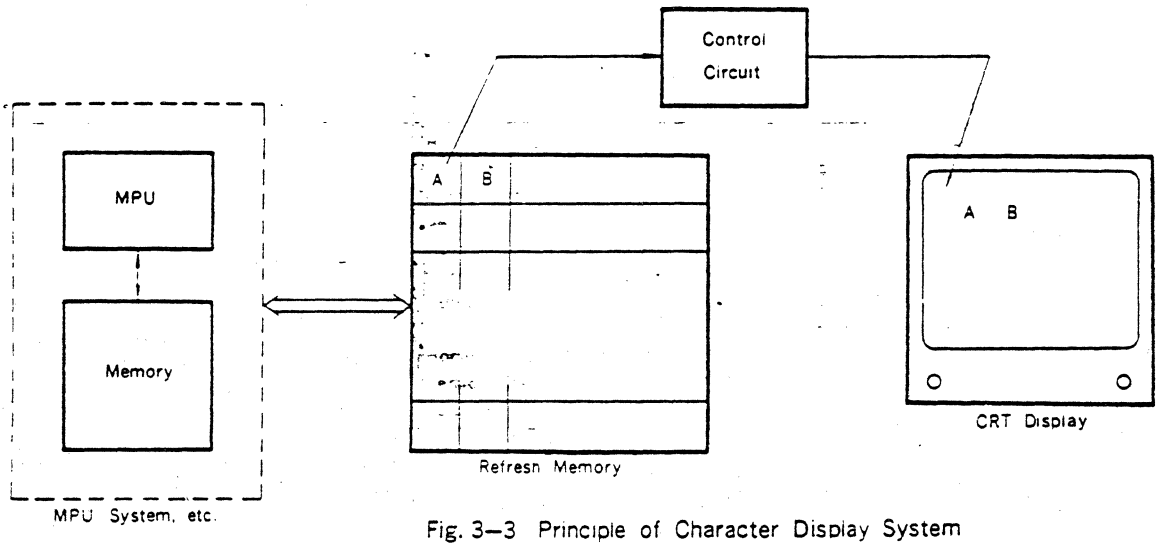


Fig. 3—3 Principle of Character Display System

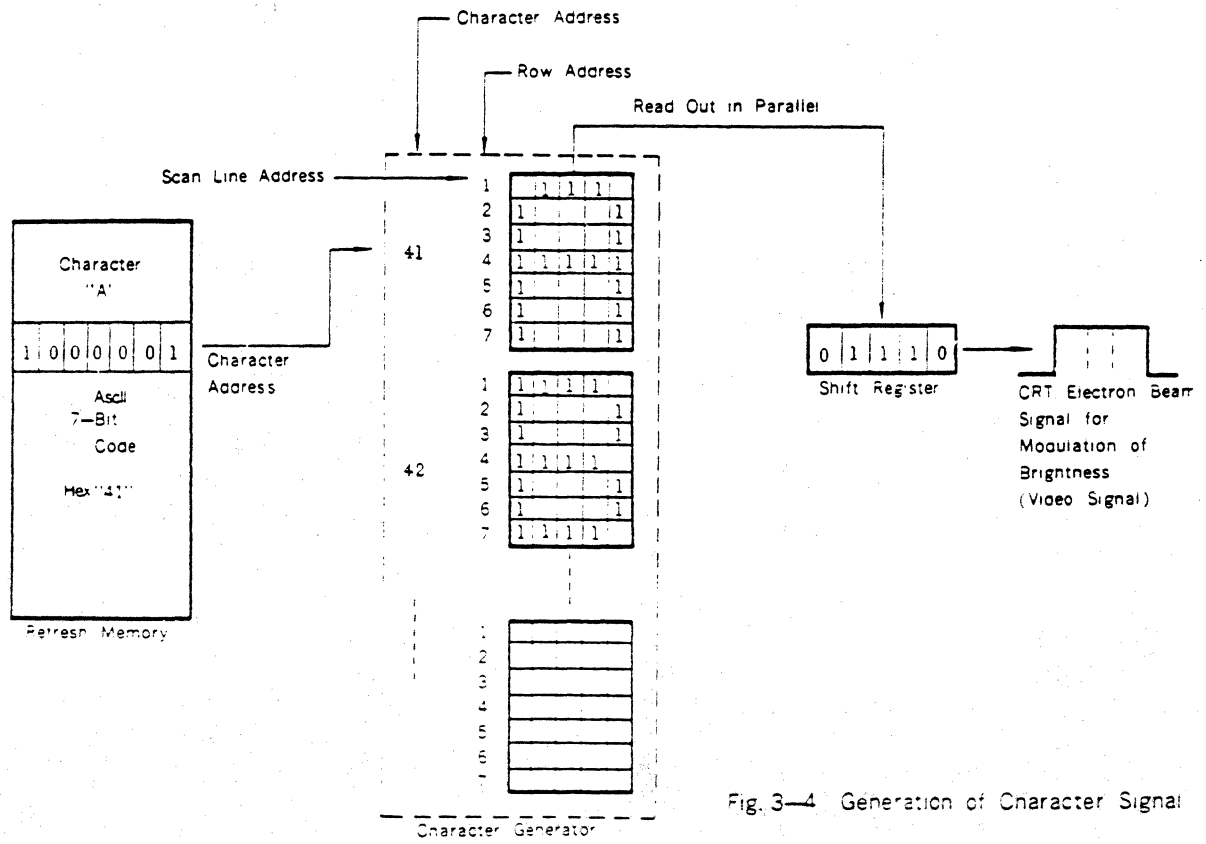


Fig. 3—4 Generation of Character Signal

Fig. 3-5 shows an example of character patterns displayed on the screen. Being shown in Fig. 3-1, as an electron beam scans both horizontally and vertically on the screen, the data of refresh memory correspondent to its position of scanning is read out successively. Then the character pattern of each scan line is generated according to the signal indicating position of the line. This video signal modulates an electron beam current to control brightness so as to display characters on the screen.

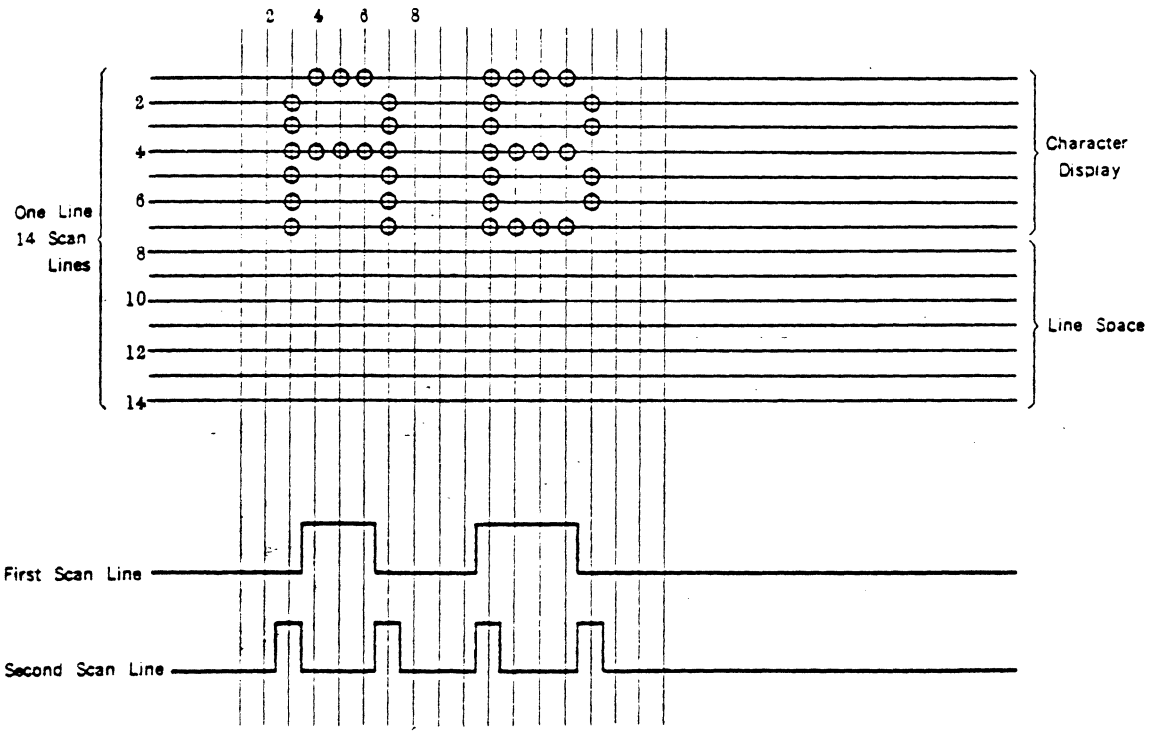


Fig. 3—5 Character Display on the Screen & Video Signal

4.1 Structure of the CRTC

As shown in Fig. 1-1, the CRTC is a LSI which is connected with MPU and CRT display device to control CRT display. The CRTC consists of internal register group, horizontal and vertical timing circuits, linear address generator, cursor control circuit, and light pen detection circuit. Horizontal and vertical timing circuit generate $RA_0 \sim RA_4$, DISPTMG, HSYNC, and VSYNC. $RA_0 \sim RA_4$ are raster address signals and used as input signals for Character Generator. DISPTMG, HSYNC, and VSYNC signals are received by video control circuit. This horizontal and vertical timing circuit consists of internal counter and comparator circuit. Linear address generator generates refresh memory address $MA_0 \sim MA_{13}$ to be used for refreshing the screen. By these address signals, refresh memory is accessed periodically. As 14 refresh memory address signals are prepared, 16K words max are accessible. Moreover, the use of start address register enables paging and scrolling shown in Fig. 9-11 and 9.12. Light pen detection circuit detects light pen position on the screen. When light pen strobe signal is received, light pen register memorizes linear address generated by linear address generator in order to memorize where light pen is on the screen. Cursor control circuit controls the position of cursor, its height, and its blink.

4.2 Pin Assignment

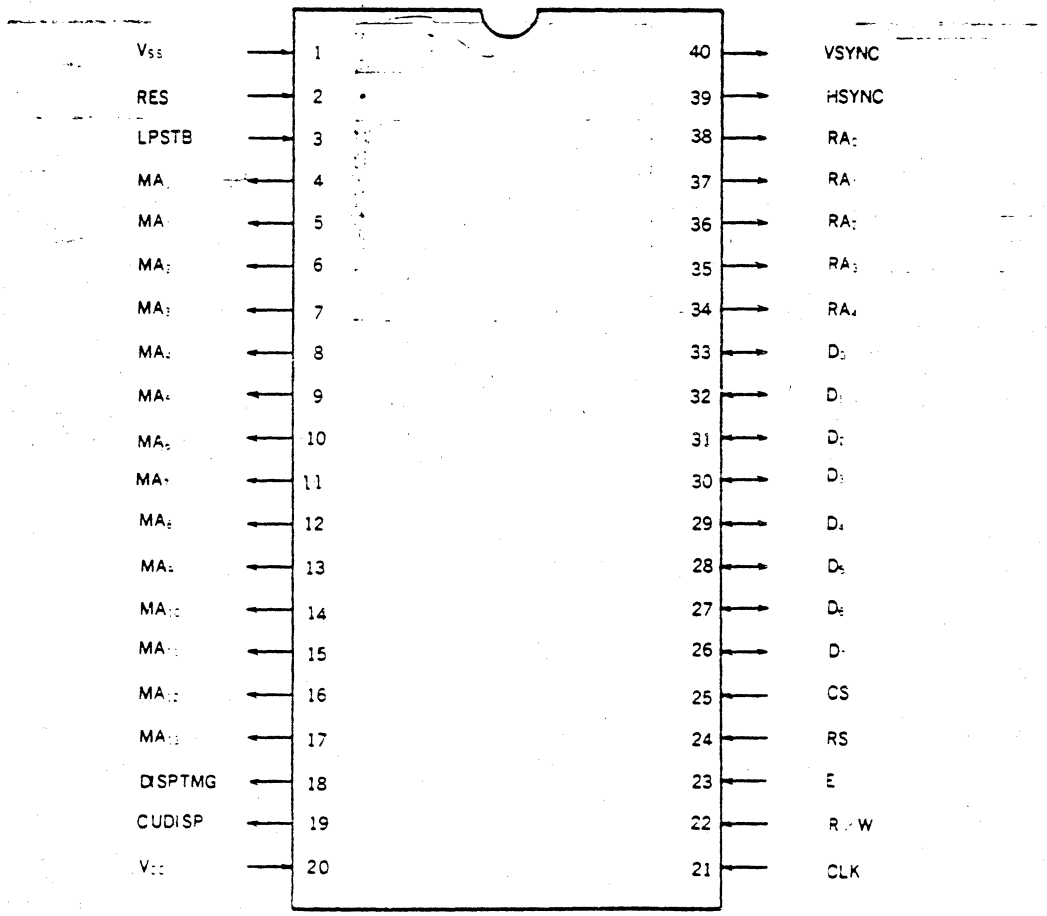


Fig. 4—1 Pin Assignment of the CRTC

4.3 Internal Block Diagram

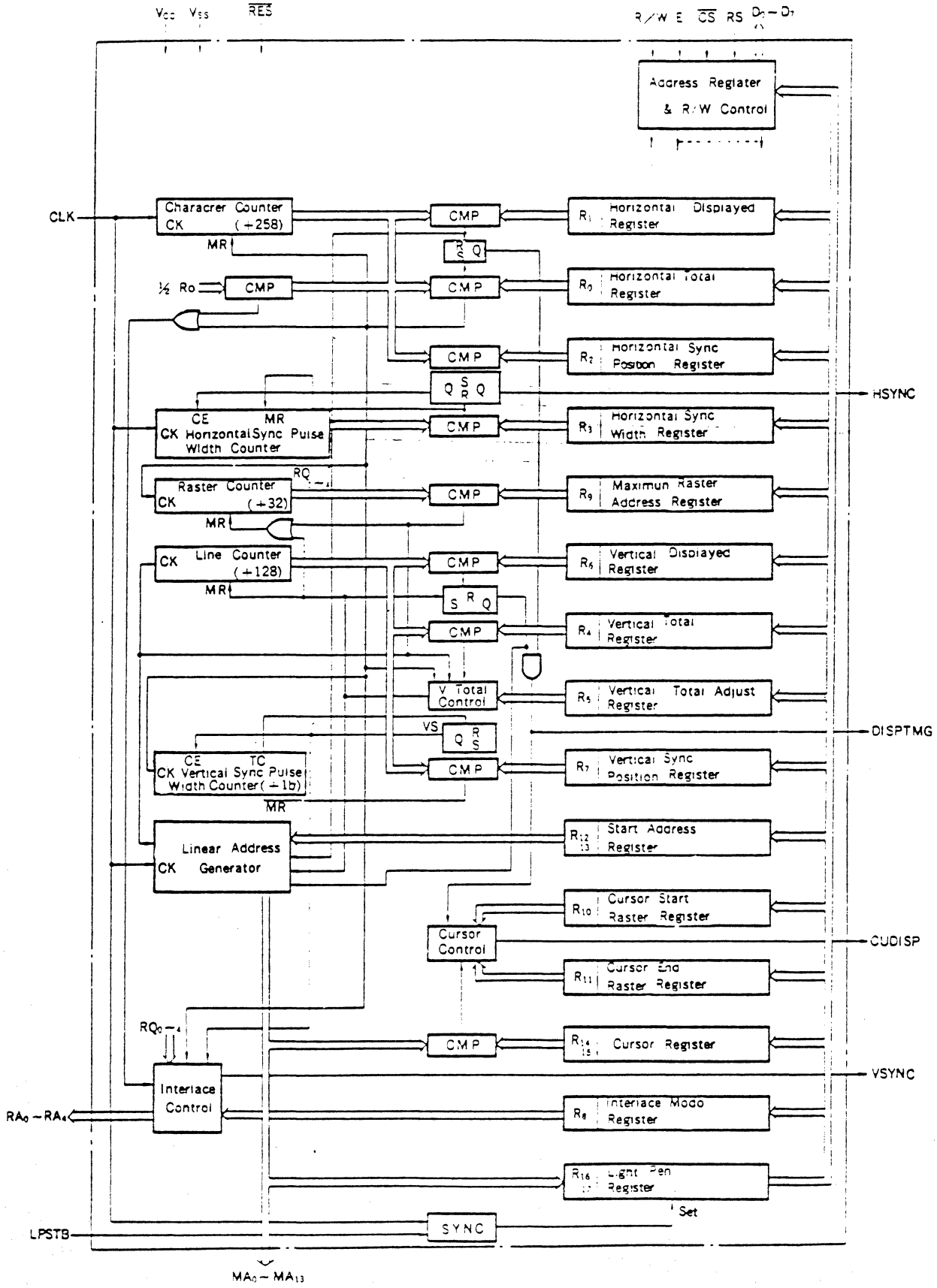


Fig. 1—2 Internal Block Diagram of the CRTC

5. Function of Signal Line

As shown in Fig. 4-1, the CRTC provides 13 interface signals to MPU and 25 interface signals to CRT display.

5.1 Interface Signals to MPU

(1) Bi-directional Data Bus (D_0~D-)

Bi-directional data bus(D_0~D-) are used for data transfer between the CRTC and MPU. The data bus output are 3-state buffers and remain in the high-impedance state except when MPU performs a CRTC read operation.

(2) Read/Write (R/W)

R/W signal controls the direction of data transfer between the CRTC and MPU. When R/W is at "High" level, data of CRTC is transfered to MPU. When R/W is at "Low" level, data of MPU is transfered to CRTC.

(3) Chip Select($\overline{CS}$)

Chip Select signal ($\overline{CS}$) is used to address the CRTC. When $\overline{CS}$ is at "Low" level, it enables R/W operation to CRTC internal registers. Normally this signal is derived from decoded address signal of MPU under the condition that VMA signal of MPU is at "High" level.

(4) Register Select(RS)

Register Select signal (RS) is used to select the address register and 18 control registers of the CRTC. When RS is at "Low" level, the address register is selected and when RS is at "High" level, control registers are selected. This signal is normally a derivative of the lowest bis (A_0) of MPU address bus.

(5) Enable(E)

Enable signal (E) is used as strobe signal in MPU R/W operation with the CRTC internal registers. This signal is normally a derivative of the HMCS6800 System ϕ_2 clock.

(6) Reset ($\overline{RES}$)

Reset signal ($\overline{RES}$) is an input signal used to reset the CRTC. When $\overline{RES}$ is at "Low" level, it forces the CRTC into the following status.

1. All the counters in the CRTC are cleared and the device stops the display operation.
2. All the outputs go down to "Low" level.
3. Control registers in the CRTC are not affected and remain unchanged.

This signal is different from other HMCS6800 family LSIs in the following functions and has restrictions for usage.

1. $\overline{RES}$ signal has capability of reset function only when LPSTB is at "Low" level.
2. After $\overline{RES}$ has gone down to "Low" level, output signals of MA_0~MA_{13} and RA_0~RA_4 synchronize with CLK low level and go down to "Low" level (At least, 1 cycle CLK signal is necessary for reset.)
3. The CRTC starts the display operation immediately after $\overline{RES}$ signal goes high.

5.2 Interface Signals to CRT Display Device

(1) Character Clock(CLK)

CLK is a standard clock input signal which defines character timing for the CRTC display operation. This signal is normally derived from the external high-speed dot timing logic.

(2) Horizontal Sync (HSYNC)

HSYNC is an active high level signal which provides horizontal synchronization for display device.

(3) Vertical Sync(VSYNC)

VSYNC is an active high level signal which provides vertical synchronization for display device. The pulse width is fixed at 16 horizontal scans (16H).

(4) Display Timing(DISPTMG)

DISPTMG is an active high level signal which defines the display period in horizontal and vertical raster scanning. It is necessary to enable video signal only when DISPTMG is at high level.

(5) Refresh Memory Address(MA_0~MA_{13})

MA_0~MA_{13} are refresh memory address signals which are used to access to refresh memory in order to refresh the CRT screen periodically. These outputs enables 16K words max. refresh memory access. So, for instance, these are applicable up to 2000 characters/screen and 8-page system.

(6) Raster Address(RA_0~RA_4)

RA_0~RA_4 are raster address signals which are used to select the raster of the character generator or graphic pattern generator etc.

(7) Cursor Display(CUDISP)

CUDISP is an active high level video signal which is used to display the cursor on the CRT screen. This output is inhibited while DISPTMG is at low level. Normally this output is mixed with video signal and provided to the CRT display device.

(8) Light Pen Strobe(LPSTB)

LPSTB is an active high level input signal which accepts strobe pulse detected by the light pen and control circuit. When this signal is activated, the refresh memory address (MA_0~MA_{13}) which are shown in Fig.8-2 are stored in the 14-bit light pen register. The stored refresh memory address need to be corrected in software, taking the delay time of the display device, light pen, and light pen control circuits into account.

6. Structure & Function of Internal Registers

6.1 Structure of Internal Registers

Table 6—1 Internal Registers of the CRTC

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Register #	Register Name	Program Unit	READ	WRITE	Data Bit 7	6	5	4	3	2	1	0	
1	×	×	×	×	×	×	A		—	—	—									
0	0	×	×	×	×	×	RR	Address Register	—	×	O									
0	1	0	0	0	0	0	R_0	Horizontal Total *7	character	×	O									*1
0	1	0	0	0	0	1	R_1	Horizontal Displayed	"	×	O									
0	1	0	0	0	1	0	R_2	Horizontal Sync Position *7	"	×	O									
0	1	0	0	0	1	1	R_3	Horizontal Sync Width	"	×	O									
0	1	0	0	1	0	0	R_4	Vertical Total *7	line	×	O									
0	1	0	0	1	0	1	R_5	Vertcal Total Adjust	raster	×	O									*2
0	1	0	0	1	1	0	R_6	Vertical Displayed	line	×	O									
0	1	0	0	1	1	1	R_7	Vertical Sync Position *7	"	×	O									
0	1	0	1	0	0	0	R_8	Interlace Mode	—	×	O							V	S	*3
0	1	0	1	0	0	1	R_9	Maximum Raster Address *7	raster	×	O									*4
0	1	0	1	0	1	0	R_{10}	Cursor Start Raster	"	×	O		B	P						*5
0	1	0	1	0	1	1	R_{11}	Cursor End Raster	"	×	O									*6
0	1	0	1	1	0	0	R_{12}	Start Address(H)	—	×	O									
0	1	0	1	1	0	1	R_{13}	Start Address(L)	—	×	O									
0	1	0	1	1	1	0	R_{14}	Cursor(H)	—	O	O									
0	1	0	1	1	1	1	R_{15}	Cursor(L)	—	O	O									
0	1	1	0	0	0	0	R_{16}	Light Pen(H)	—	O	×									
0	1	1	0	0	0	1	R_{17}	Light Pen(L)	—	O	×									

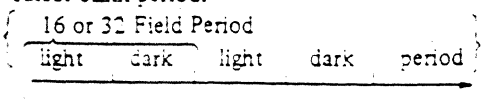
NOTE: 1 When R_8 is 1 or 3 (Interlace Mode), programmed data must be odd.

2 When R_8 is 3, N/2 (N: total number of lines)

3 When S is 1, V specifies video mode. S specifies interlace sync mode.

4 When R_8 is 3, programmed data must be odd.

5 B specifies the cursor blink. P specifies the cursor blink period.



6 When R_8 is 3, the cursor start and the cursor end raster registers must be both even or both odd.

7 Programmed Value = Specified Value - 1
In the following explanation, for instance, total number of horizontal characters means "Specified Value"

6.2 Function of Internal Registers

(1) **Address Register(AR)**
This is a 5-bit register used to select 18 internal control registers ($R_0 \sim R_{17}$). Its contents are the address of one of 18 internal control registers. Programming the data from 18 to 31 produces no results. Access to $R_0 \sim R_{17}$ requires, first of all, to write the address of corresponding control register into this register. When RS and $\overline{CS}$ are at low level, this register is selected.

(2) **Horizontal Total Register(R_0)**
This is a register used to program total number of horizontal characters per line including the retrace period. The data is 8-bit and its value should be programmed according to the specification of the CRT. When M is total number of characters, (M-1) shall be programmed to this register. When programming for interlace mode, M must be even. How to decide total number of characters is shown in 9.5.1.

(3) **Horizontal Displayed Register(R_1)**
This is a register used to program the number of horizontal displayed characters per line. Data is 8-bit and any number that is smaller than that of horizontal total characters can be programmed.

(4) **Horizontal Sync Position Register(R_2)**
This is a register used to program horizontal sync position in unit of horizontal character time. Data is 8-bit and any number that is under the following condition (Horizontal Sync Position + Horizontal Pulse Width < Horizontal Total Characters) can be programmed. When H is character number of horizontal Sync Position, (H-1) shall be programmed to this register. When programmed value of this register is increased, the display position on the CRT screen is shifted to the left. When programmed value is decreased, the position is shifted to the right. Therefore, the optimum horizontal position can be determined by this value.

(5) **Horizontal Sync Width Register(R_3)**
This is a register used to program horizontal sync pulse width from 1 to 15 in unit of horizontal character time. Note that when 0 is programmed, HSYNC is not provided.

(6) **Vertical Total Register(R_4)**
This is a register used to program total number of lines per frame including vertical retrace period. The data is within 7-bit and its value should be programmed according to the specification of the CRTC. When N is total number of lines, (N-1) shall be programmed to this register. How to decide total number of lines is shown in 9.5.1.

(7) **Vertical Total Adjust Register(R_5)**
This is a register used to program the optimum number from 0 to 31 to adjust total number of rasters per frame. This register enables to decide the number of vertical deflection frequency more strictly.

(8) **Vertical Displayed Register(R_6)**
This is a register used to program the number of displayed character rows on the CRT screen. Data is 7-bit and any number that is smaller than that of vertical total characters can be programmed.

(9) **Vertical Sync Position Register(R_7)**
This is a register used to program the vertical sync position on the screen in unit of horizontal character time. Data is 7-bit and any number that is equal to or less than vertical total characters can be programmed. When V is character number of vertical sync position, (V-1) shall be programmed to this register. When programmed value of this register is increased, the display position is shifted up. When programmed value is decreased, the position is shifted down. Therefore, the optimum vertical position may be determined by this value.

(10) **Interlace Mode Register(R_8)**
This is a 2-bit register used to control the raster scan mode. (See Table.6-2)

Table.6—2 Interlace Mode

2^1	2^0	Mode
0	0	Non-Interlace Mode
1	0	Non-Interlace Mode
0	1	Interlace Sync Mode
1	1	Interlace Sync & Video Mode

In non-interlace mode, the rasters of even number field and odd number field are scanned duplicatedly. In interlace sync mode, the rasters of odd number field are scanned in the middle of even number field. Then it is controlled to display the same character pattern in two fields. In interlace sync and video mode, the raster scan method is the same as that in interlace sync mode, but it is controlled to display different character pattern in two fields.

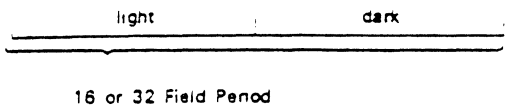
(11) **Maximum Raster Address Register (R_9)**
This is a register used to program maximum raster address within 5-bit. This register defines total number of rasters per character including spacing. When total number of rasters is RN, (RN-1) shall be programmed to this register. Moreover, when programmed value of R_8 is "3", RN must be even.

(12) **Cursor Start Raster Register(R_{10})**
This is a register used to program the cursor start raster address by lower 5 bits ($2^0 \sim 2^4$) and the cursor display mode by higher 2 bits (2^5,2^6).

Table.6-3 Cursor Display Mode

2^6	2^5	Cursor Display Mode
0	0	Non-Blink
0	1	Cursor Non-Display
1	0	Blink, 16 Field Period
1	1	Blink, 32 Field Period

Blink Period



(13) Cursor End Raster Register (R11)

This is a register used to program the cursor end raster address. When programmed value of R_8 is "3" (Interlace sync & video mode), both the cursor start raster register and the cursor end raster register must be even or odd.

(14) Start Address Register(R_{12},R_{13})

These are used to program initial address of refresh memory to read out. Changing the contents of these registers dynamically enables paging and scrolling easily.

(15) Cursor Register(R_{14},R_{15})

These are used to program the cursor display address and R/W operation from MPU is possible. When R_{14} is read, the higher 2 bits (2^6,2^7) are always "0".

(16) Light Pen Register(R_{16},R_{17})

These are used to catch the detection address of light pen and only a read operation from MPU is possible. When R_{16} is read, the higher 2 bits (2^6, 2^7) are always "0". Its vlaue needs to be corrected in software because there is time delay from address output of the CRTC to signal input to LPSTB pin of the CRTC in the process that raster is lit after address output and light pen detects it. Moreover, delay time shown in Fig. 8-2 needs to be taken into account.

7. Operation of the CRTC

7.1 Time Chart of CRT Interface Signals

The following example shows the display operation in which values of Table. 7-1 are programmed to the CRTC internal registers. Fig. 7-1 shows the CRT screen format Fig. 7-4 shows the time chart of signals output from the CRTC.

Table. 7—1 Programmed Values into the Registers

Reg	Register Name	Value	Reg	Register Name	Value
R_0	Horizotal Total	N_{ht}	R_9	Max Raster Address	N_r
R_1	Horizontal Displayed	N_{hd}	R_{10}	Cursor Start Raster	
R_2	Horizontal Sync Position	N_{hsp}	R_{11}	Cursor End Raster	
R_3	Horizontal Sync Width	N_{hsw}	R_{12}	Start Address(H)	0
R_4	Vertical Total	N_{vt}	R_{13}	Start Address(L)	0
R_5	Vertical Total Adjust	N_{adj}	R_{14}	Cursor(H)	
R_6	Vertical Displayed	N_{vd}	R_{15}	Cursor(L)	
R_7	Vertical Sync Position	N_{vsp}	R_{16}	Light Pen(H)	
R_8	Interlace Mode		R_{17}	Light Pen(L)	

NOTE: $N_{hd} < N_{ht}$, $N_{vd} < N_{vt}$

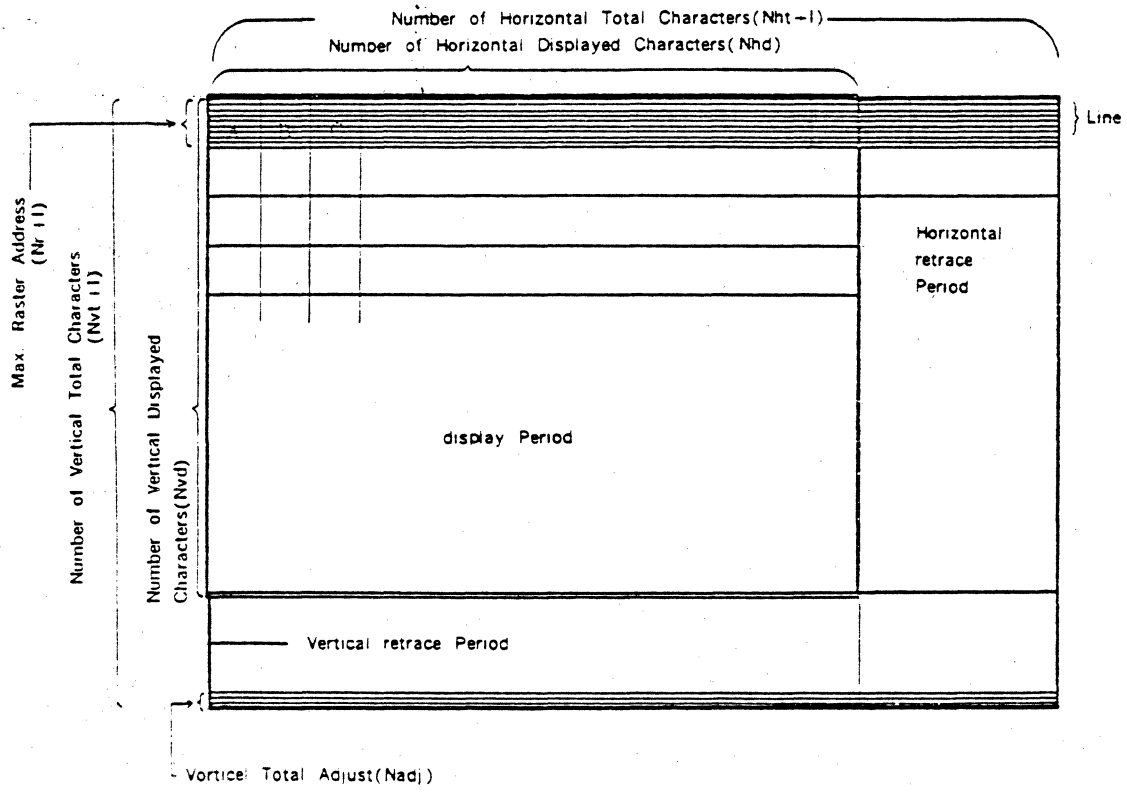


Fig. 7—1 CRT Screen Format

The relation between values of Refresh Memory Address (MA_0~MA_{13}) and Raster Address (RA_0~RA_4) and the display position on the screen is shown in Fig. 7-10. Fig. 7-10 shows the case where the value of Start Address is 0.

7.2 Interlace Control

Fig. 7-2 shows an example where the same character is displayed in non-interlace mode, interlace sync mode, and video mode.

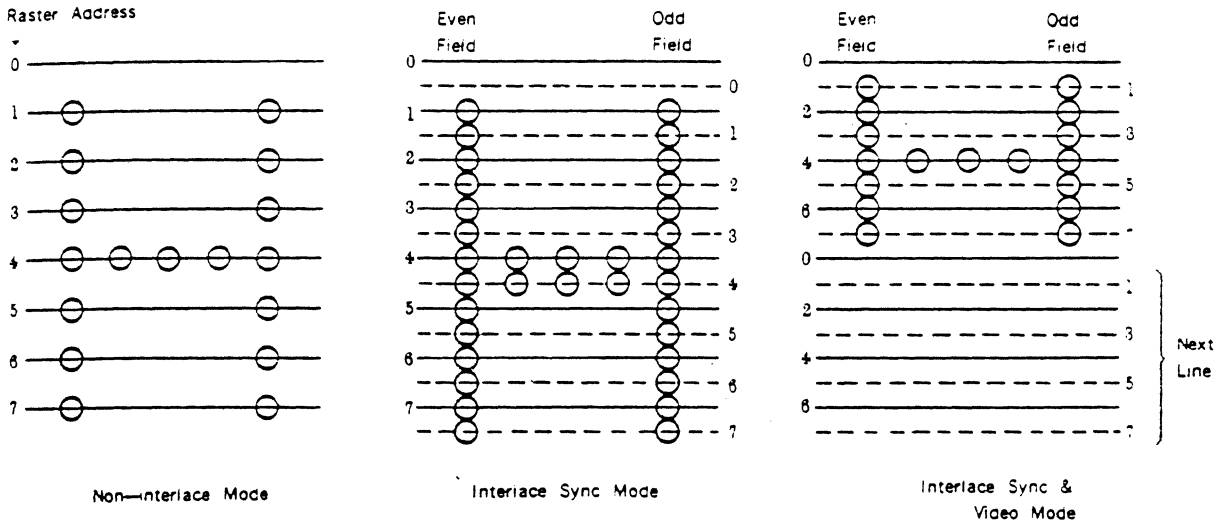


Fig. 7—2 Interlace Control

In interlace sync mode, the raster address of even field and odd field are the same and display the same character pattern. In interlace sync & video mode, the character pattern of even number raster address is displayed in even field. The character pattern of odd number raster address is displayed in odd field. Therefore, compared with the characters in non-interlace mode and interlace sync mode, the size is one-half of them vertically. Fig. 7-7 shows the output wave form of vertical sync in interlacing.

7.3 Cursor Control

Fig. 7-3 shows the display patterns where each value is programmed to the cursor start raster register and the cursor end raster register. Programmed values to the cursor start raster register and the cursor end raster register need to be under the following condition.

Cursor Start Raster Register≤Cursor End Raster Register≤Maximum Raster Address Register

Time chart of CUDISP output signal is shown in Fig. 7-8 and Fig. 7-9.

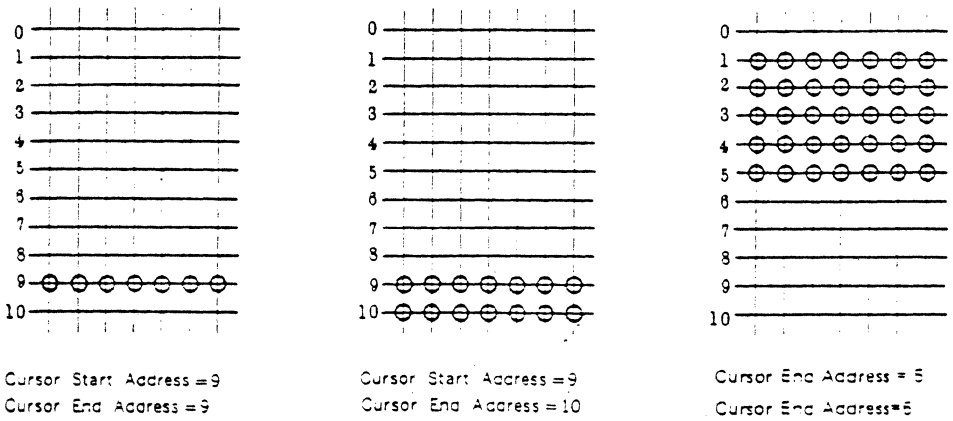


Fig. 7—3 Cursor Control

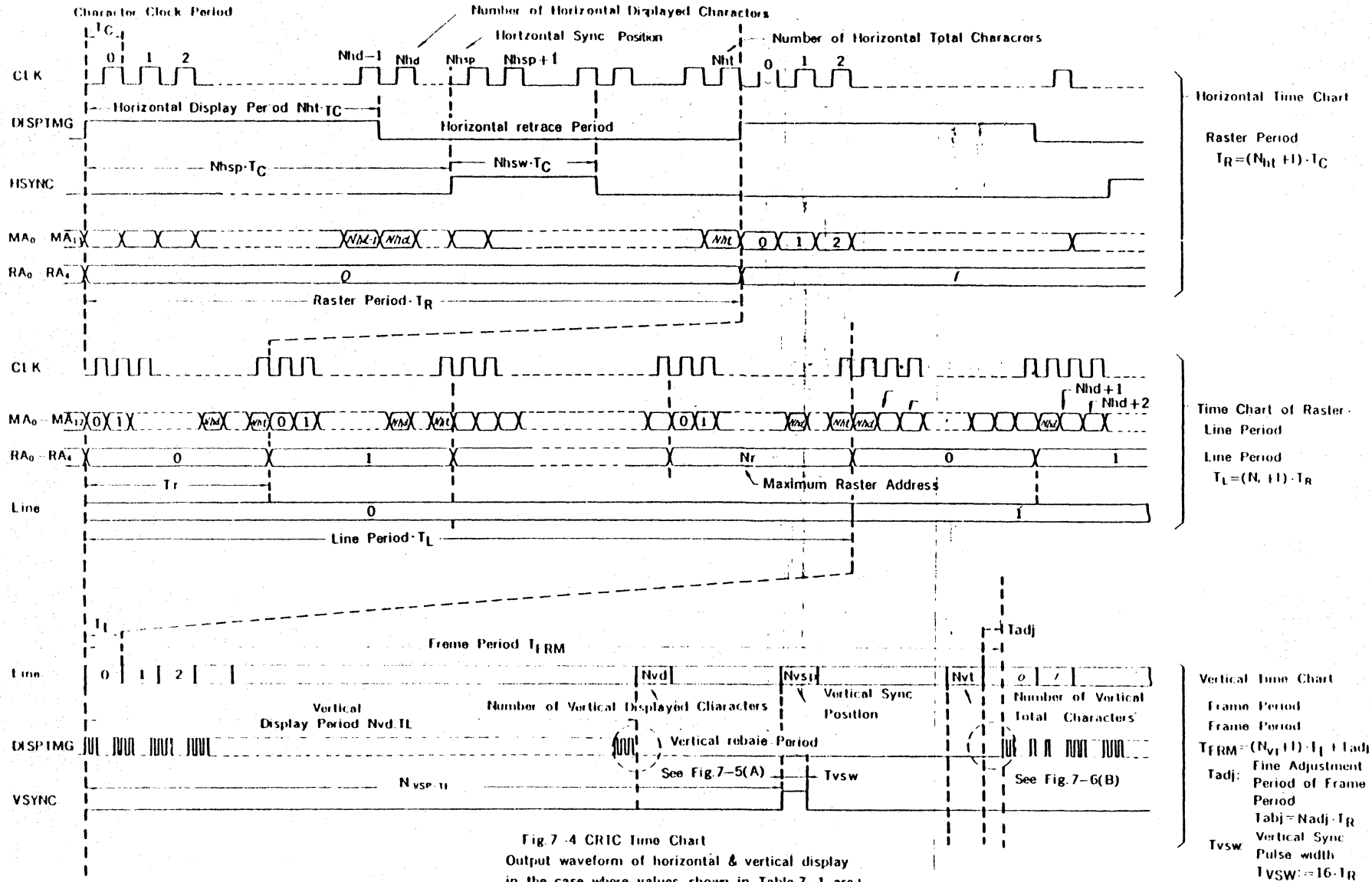


Fig.7-4 CRTC Time Chart
Output waveform of horizontal & vertical display in the case where values shown in Table.7-1 are Programmed to each register.

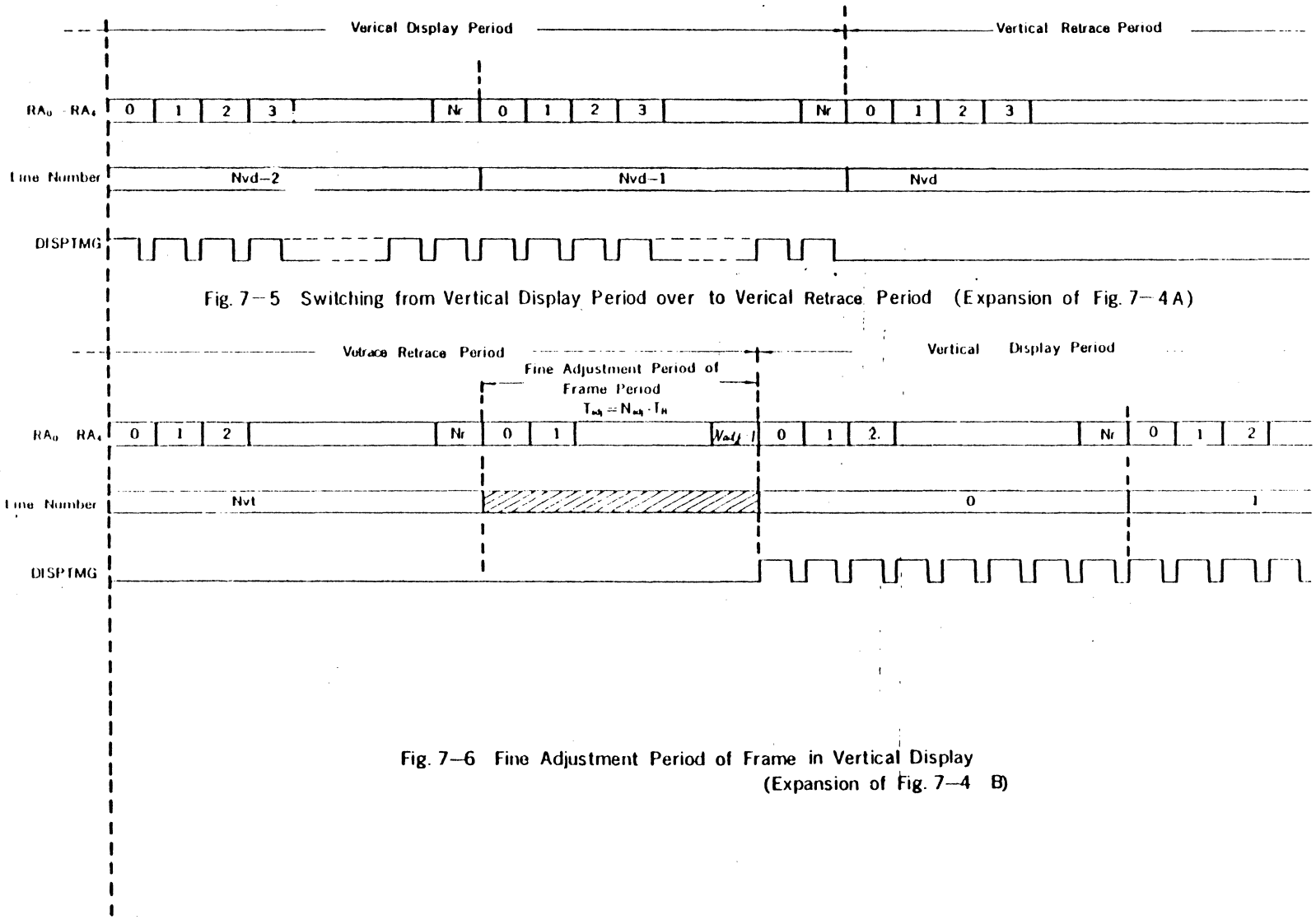


Fig. 7−5 Switching from Vertical Display Period over to Verical Retrace Period (Expansion of Fig. 7−4A)

Fig. 7−6 Fine Adjustment Period of Frame in Vertical Display
(Expansion of Fig. 7−4 B)

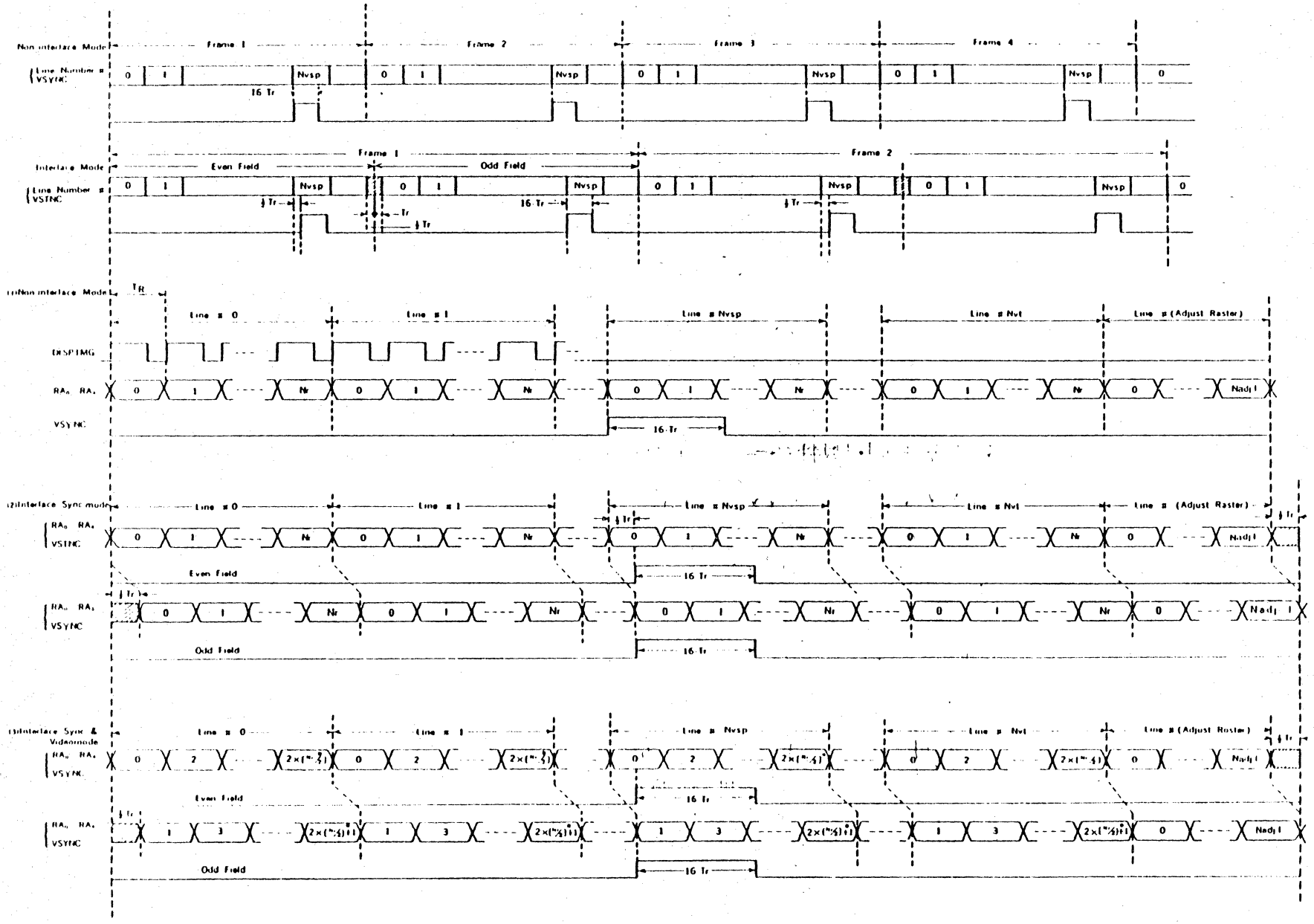


図 Fig. 7—7 Interlace Control

NOTE1 In interlace sync & video mode, maximum raster address(Nr))shall be odd
2 In interlaee mode, Nht shall be odd

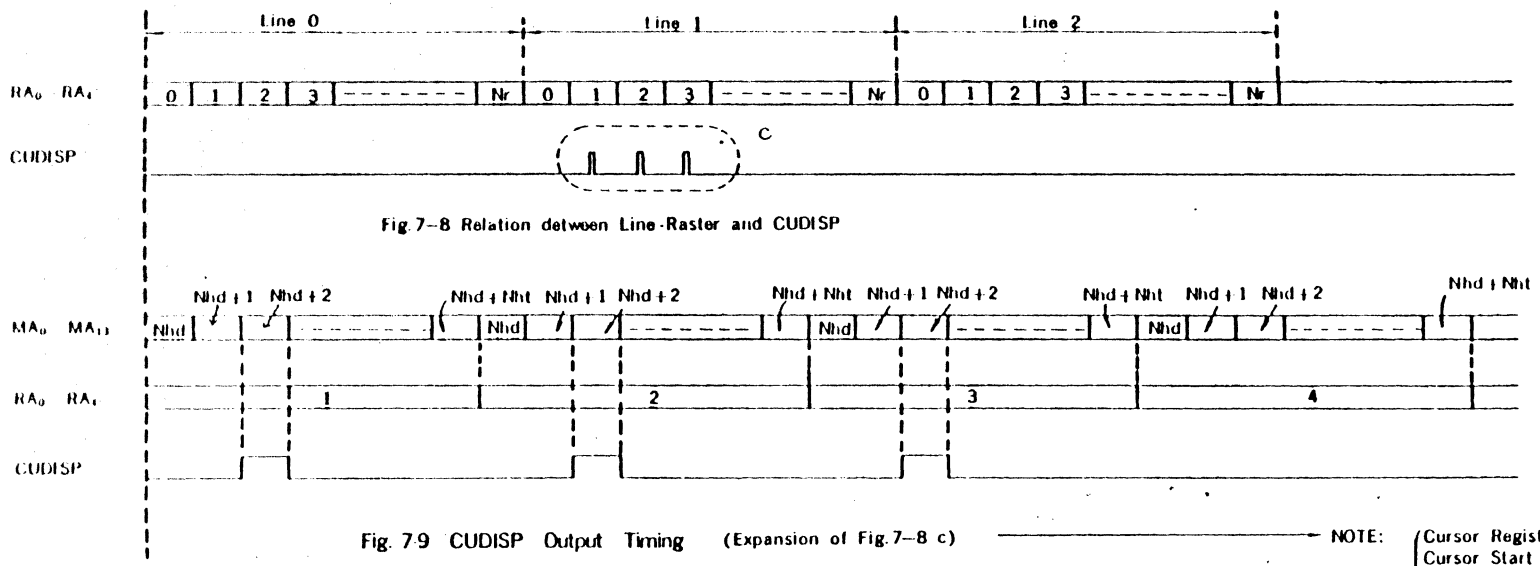


Fig. 7-8 Relation between Line-Raster and CUDISP

Fig. 7-9 CUDISP Output Timing (Expansion of Fig. 7-8 c)

NOTE: (Cursor Register = N_{hd} + 2, Cursor Start Raster Register = 1, Cursor End Raster Register = 3) are Programmed in cursor display mode

In blink mode, it is changed into display mode when frame period is 16 or 32 time period.

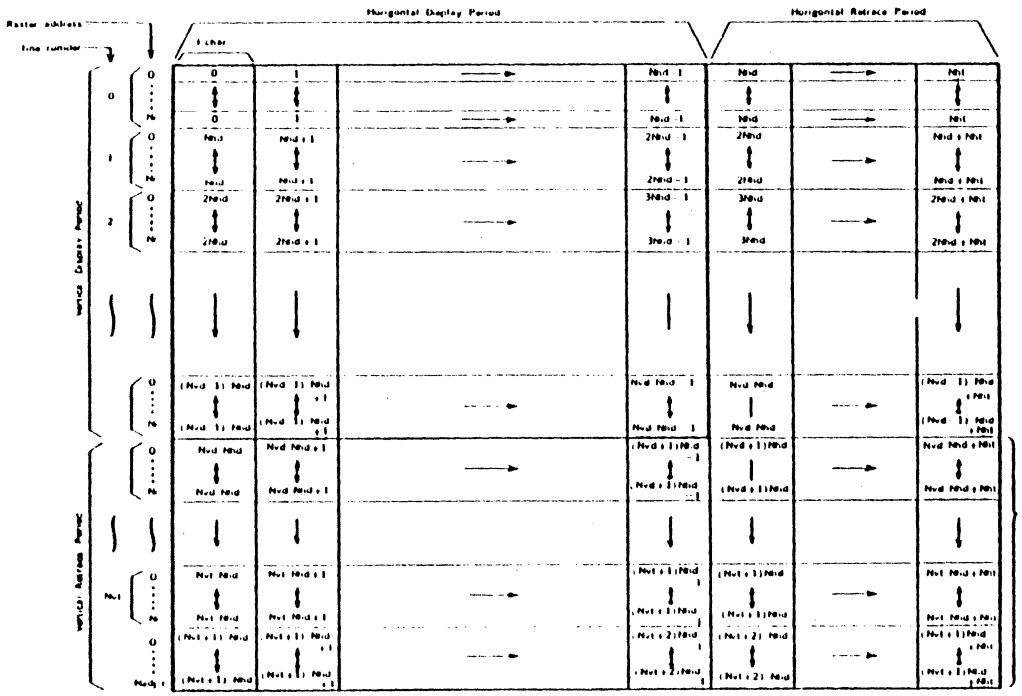


Fig. 7-10 Refresh Memory Address (MA_0-MA_{13})

Valid refresh memory address (0 N_{vd}-N_{hd}-1) are shown within the thick line square. Refresh memory address are provided even during horizontal and Vertical retrace period. This is an example in the case where the programmed value of start address register is 0.

8. Electrical Characteristics of the CRTC

8-1 Maximum Ratings

Table. 8—1 Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	V_{CC} *	−0.3 ~ +7.0	V
Input Voltage	V_{IN} *	−0.3 ~ +7.0	V
Operating Temperature Range	Ta	−20 ~ +75	°C
Storage Temperature Range	Tstg	−55 ~ +150	°C

[NOTE] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

* With respect to V_{SS}(SYSTEM GND)

8-2 Recommended Operating Conditions

Table. 8—2 Recommended Operating Conditions

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.75	5	5.25	V
Input Voltage	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.0	—	V_{CC}	V
Operating Temperature Range	Ta	−20	25	75	°C

8-3 Electrical Characteristics

Table. 8—3 DC Characteristics

V_{CC}=5V±5%, V_{SS}=0 V, Ta=−20 ~ +75°C

Item	Symbol	min	typ	max	Unit
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Input Leak Current	I_{IN}	—	1.0	2.5	μA
Three-State Input Current V_{IN}=0.4~2.4V V_{CC}=5.25V	I_{TSI}	—	2.0	10	μA
Output High Voltage I_{LOAD}=−205μA D_0~D_7 I_{LOAD}=−100μA All Other Outputs	V_{OH}	2.4	—	—	V
Output Low Voltage I_{LOAD}=1.6mA	V_{OL}	—	—	0.4	V
Input Capacitance D_0~D_7	C_{IN}	—	—	12.5	pF
All Other Inputs				10.0	
Output Capacitance	C_{OUT}	—	—	10.0	pF
Power Dissipation	P_D	—	600	1000	mW

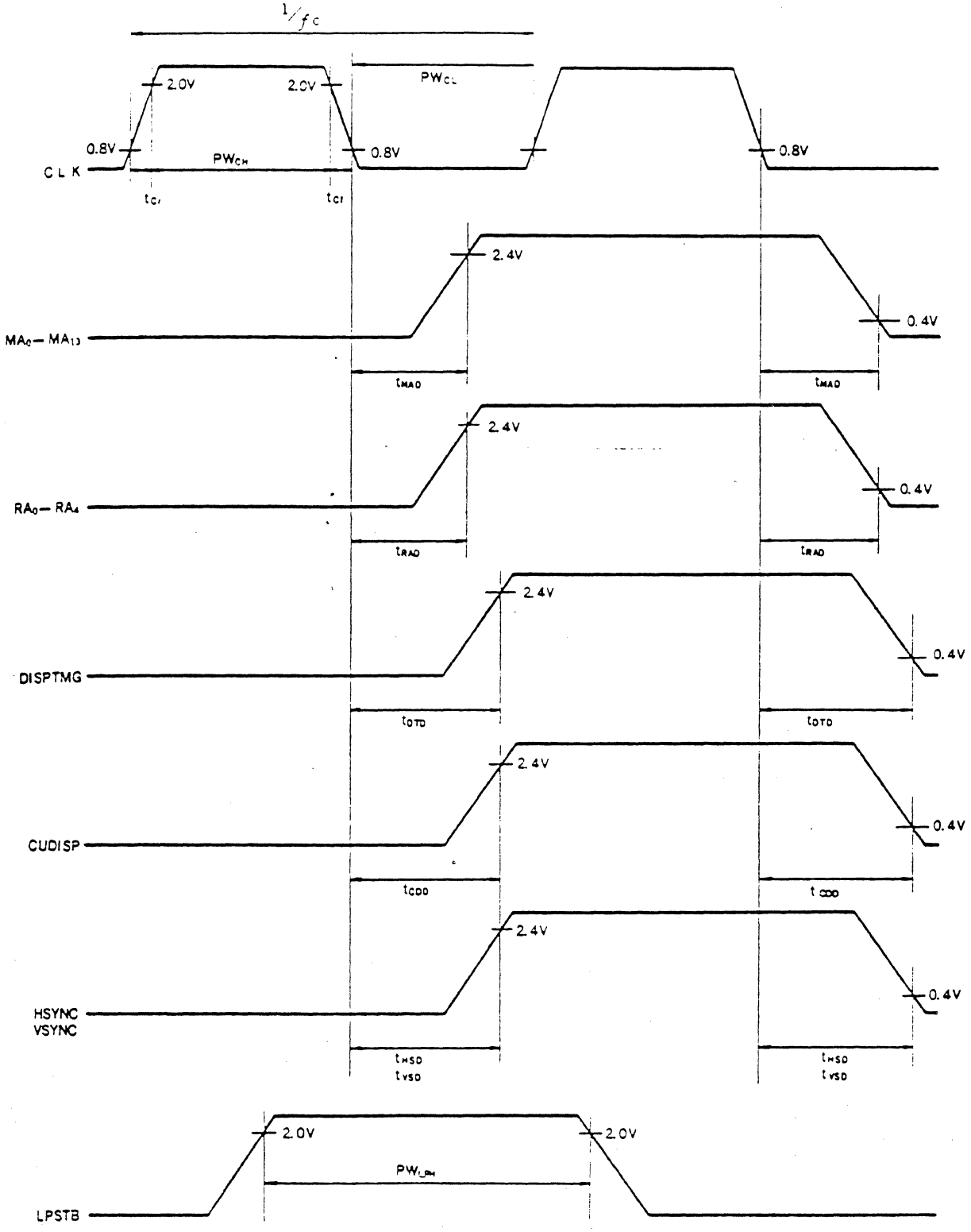
Table 8—4 AC Characteristics

Item	Symbol	min	typ	max	Unit
Clock Frequency	f_c	—	—	3.0	MHz
Clock Pulse Width, Low	PW_{CL}	150	—	—	ns
Clock Pulse Width, High	PW_{CH}	150	—	—	ns
Rise and Fall Time For Clock Input	t_{CR}	—	—	15	ns
	t_{CF}	—	—	15	
Memory Address Delay Time	t_{MAD}	—	—	160	ns
Raster Address Delay Time	t_{RAD}	—	—	160	ns
Display Timing Delay Time	t_{DTD}	—	—	250	ns
Horizontal Sync Delay Time	t_{HSD}	—	—	250	ns
Vertical Sync Delay Time	t_{VSD}	—	—	250	ns
Cursor Display Delay Time	t_{CDD}	—	—	250	ns
Light Pen Strobe Pulse Width	PW_{LPH}	80	—	—	ns
Light Pen Strobe Uncertain Time of Acceptance (Fig. 8-2)	t_{LPD1}	—	—	80	ns
	t_{LPD2}	—	—	10	

8-4 Bus Timing Characteristics

Table. 8—5 Read Sepuence

Item	Symbol	Test condition	min	typ	max	Unit
Enable Cycle Time	t_{CYCE}	—	1.0	—	—	μs
Enable Pulse Width ("High"level time)	PW_{EH}	—	0.45	—	—	μs
Enable Pulse Width ("Low"level time)	PW_{EL}		0.40			
Set Up Time ADDRESS-ENABLE	t_{AS}	—	140	—	—	ns
Data Delay Time	t_{DDR}	—	—	—	320	ns
Data Hold Time	t_H	—	10	—	—	ns
Rise & Fall Time for Enable Input	t_{Er} / t_{Ef}	—	—	—	25	ns
Address Hold Time	t_{AH}	—	10	—	—	ns
Data Access Time	t_{ACC}	—	—	—	460	ns



This Figure snows the relation in time between CLK signal and each output signals. Output secuence is snown in Fig. 7—4 — Fig. 7— 9.

Fig. 8—1 Time Chart of the CRTC

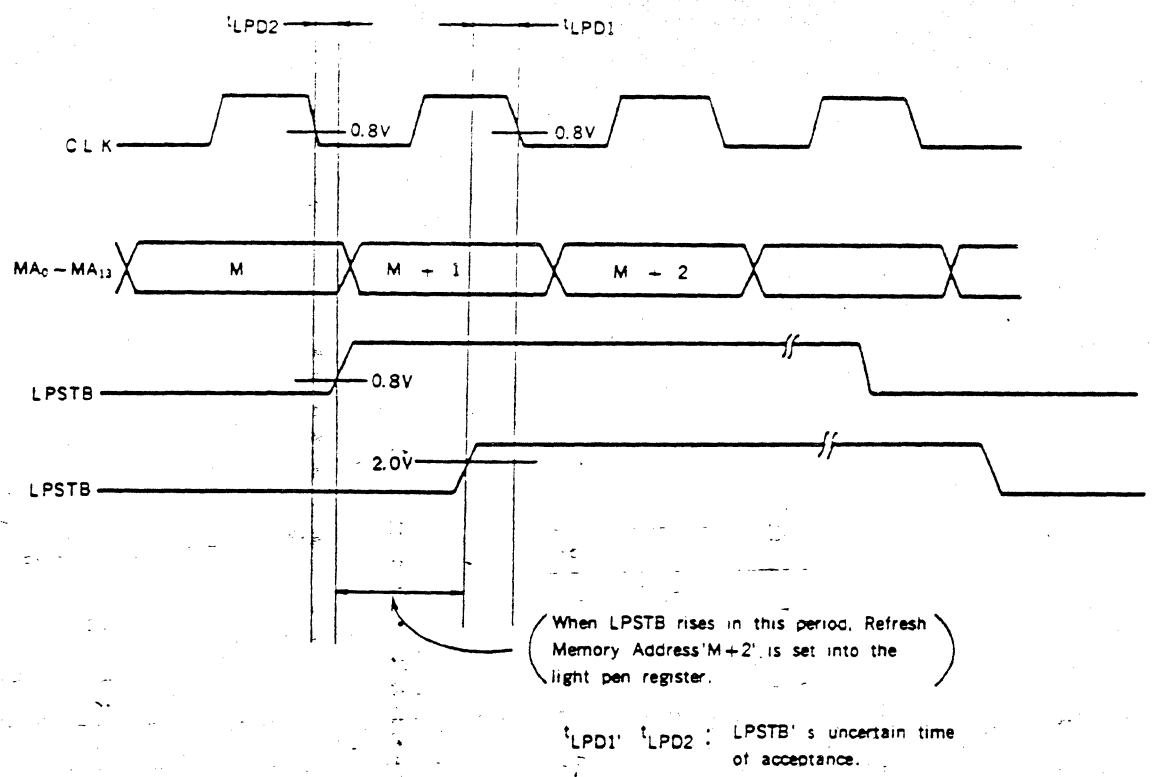


Fig. 8—2 LPSTB Input Timing & Refresh Memory Address that is set into the light pen register.

Table. 8—6 Write Sequence

Item	Symbol	Test condition	min	typ	max	Unit
Enable Cycle Time	t_{CYCE}	—	1.0	—	—	μs
Enable Pulse Width ("High"level time)	PW_{EH}	—	0.45	—	—	μs
Enable Pulse Width ("Low"level time)	PW_{EL}	—	0.40	—	—	μs
Set Up Time	t_{AS}	—	140	—	—	ns
Data Set Up Time	t_{DSW}	—	195	—	—	ns
Data Hold Time	t_H	—	10	—	—	ns
Rise & Fall Time for Enable Input	t_{Er}/t_{Ef}	—	—	—	25	ns
Address Hold Time	t_{AH}	—	10	—	—	ns

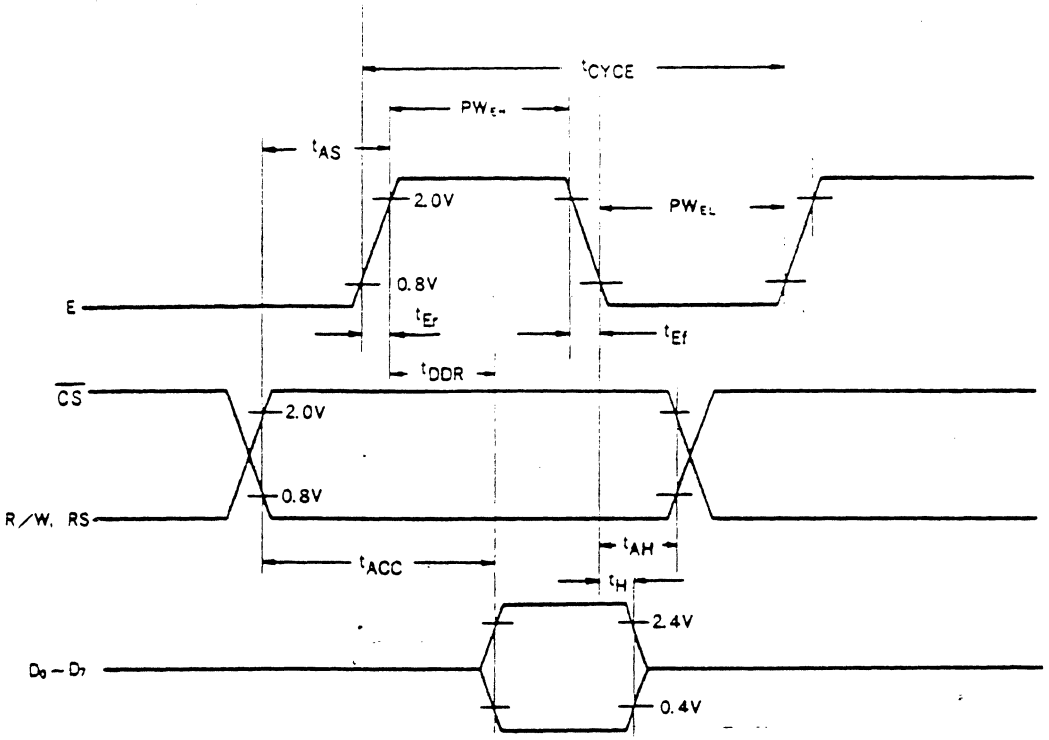


Fig. 8—3 Read Sequence

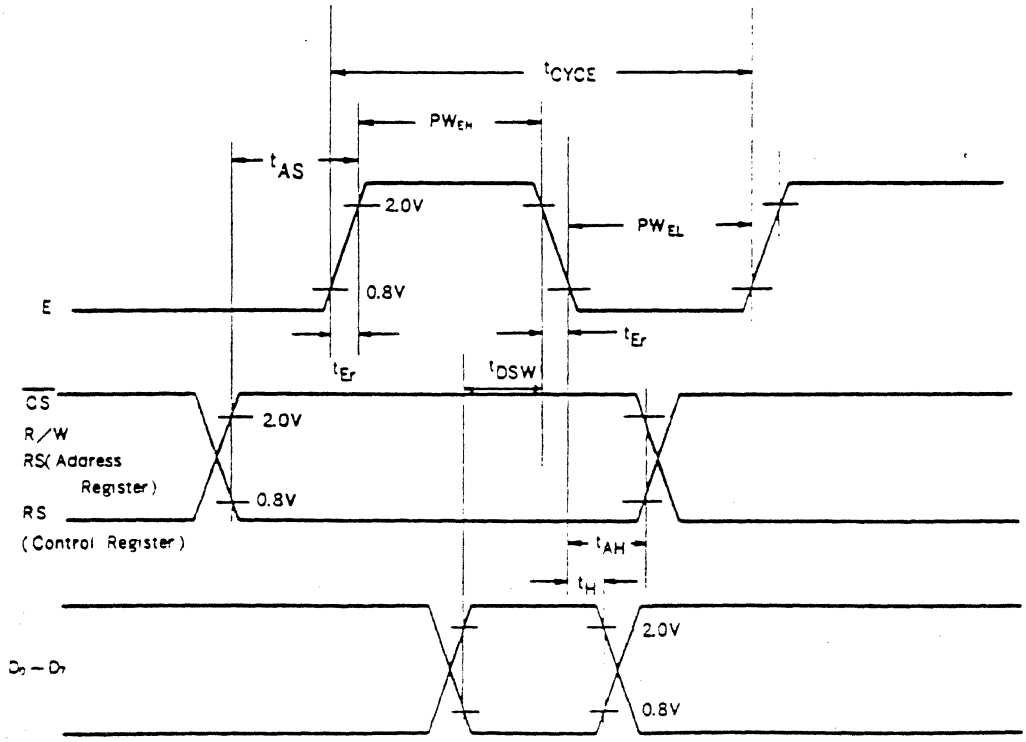


Fig. 8—4 Write Sequence

9. How to Use the CRTC

9-1 Interface to MPU

As shown in Fig. 9-1, the CRTC is connected with the standard bus of MPU to control the data transfer between them. The CRTC address is determined by $\overline{CS}$ and RS, and the R/W operation is controlled by R/W and Enable signals. When $\overline{CS}$ is "Low" and RS is also "Low", the CRTC address register is selected. When $\overline{CS}$ is "Low" and RS is "High" one of 18 internal registers is selected.

$\overline{RES}$ is the system reset signal. When $\overline{RES}$ becomes "Low", the CRTC internal control logic is reset. But internal registers shown in Table 6-1($R_0 \sim R_{17}$) are not affecteb by $\overline{RES}$ signal and remain unchanged.

The CRTC is designed so as to provide an interface to microcomputers, but adding some external circuits enables an interface to other data sources.

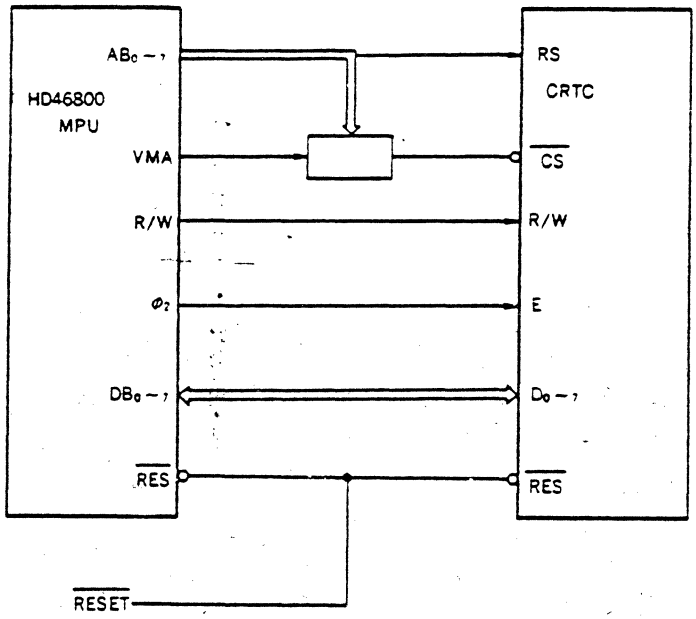


Fig. 9—1 Interface to MPU

9-2 Dot Timing Generating Circuit

CRTC's CLK input (21 pin) is provided with CLK signal which defines horizontal character time period from the outside. This CLK signal is generated by dot counter shown in Fig. 9-2. Fig. 9-2 shows a example of circuit where horizontal dot number of the character is "9". Fig. 9-3 shows the operation time chart of dot counter shown in Fig. 9-2. As this example shows explicitly, CLK signal is at "Low" level in the former half of horizontal character time and at "High" level in the latter half. It is necessary to be careful so as not to mistake this polarity.

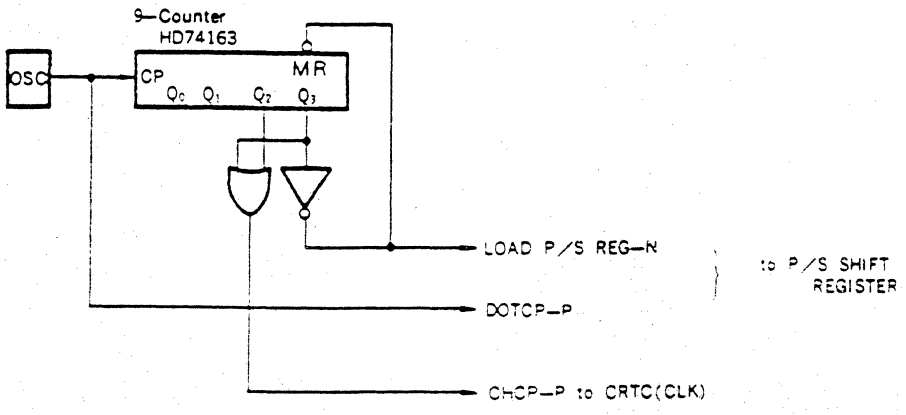


Fig. 9—2 Dot Counter

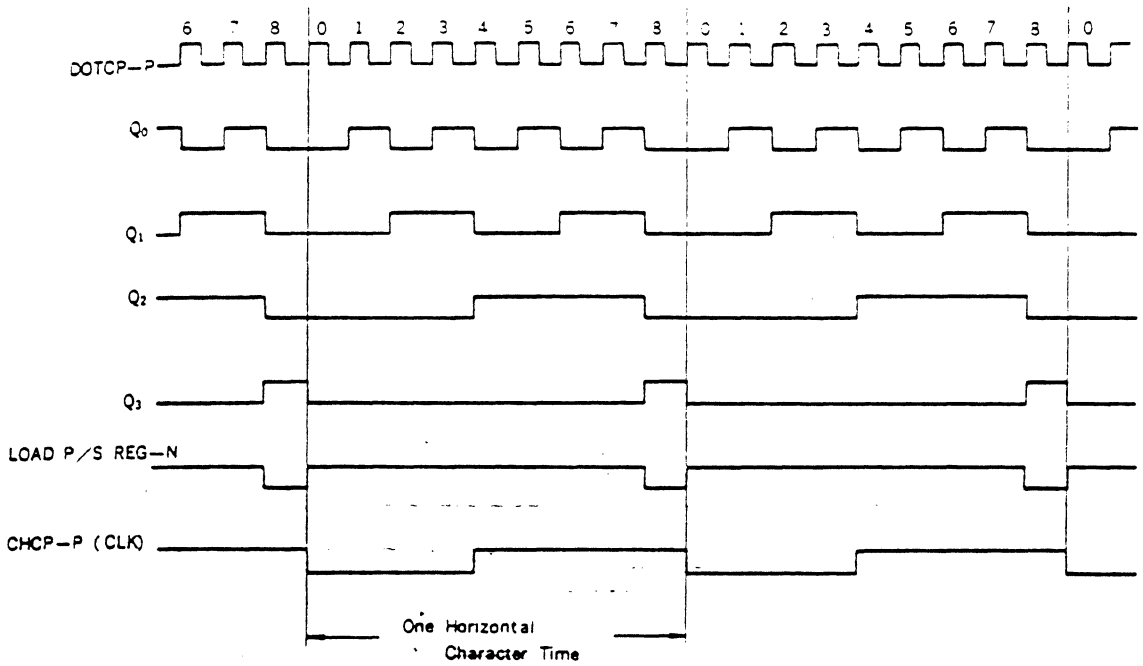


Fig. 9—3 Time Chart of Dot Counter

9·3 Interface to Display Control Unit

Fig. 9-4 shows the interface between the CRTC and display control unit. Display control unit is mainly composed of Refresh Memory, Character Generator, and Video Control circuit For refresh memory, 14 Memory Address line (0—16383) max are provided and for character generator, 5 Raster Address line (0—31) max are provided. For video control circuit, DISPTMG, CUDISP, HSYNC, and VSYNC signals are sent out. DISPTMG signal is used to control the blank period of video signal. CUDISP signal is used as video signal to display the cursor on the CRT screen. Moreover, HSYNC and VSYNC signals are used as drive signals respectively for CRT horizontal and vertical deflection circuits.

Outputs from video control circuit, (video signals and sync signals) are provided to CRT display unit to control the deflection and brightness of CRT, thus characters are displayed on the screen.

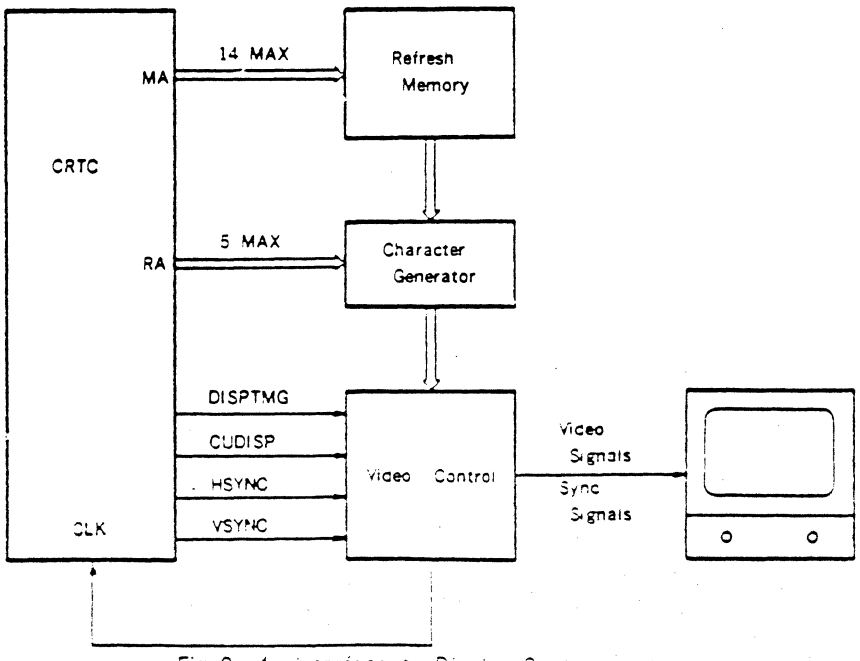
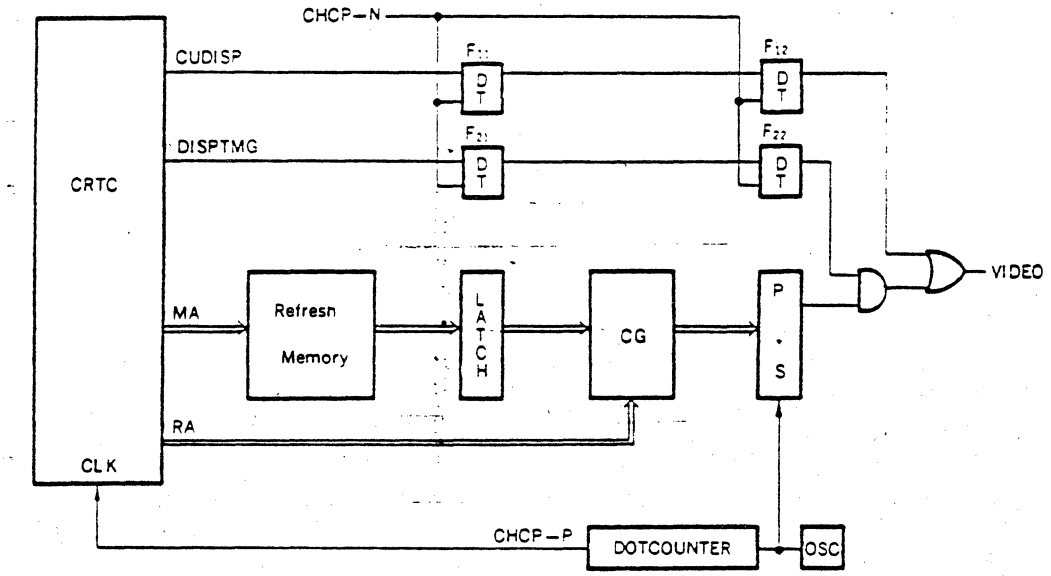


Fig. 9—4 Interface to Display Control Unit

Fig. 9-5 shows more detailed block diagram of display control unit. This shows how to use DISPTMG and CUDISP signals. By delaying for one or two-character time, DISPTMG signal synchronizes with output timing of parallel-serial converter to control blanking of character video signal. By delaying for one or two-character time, CUDISP signal is mixed with character video signal. Whether delay time of DISPTMG and CUDISP signals should be one or two-character time, moreover, whether LATCH register is necessary for output from refresh memory or not, are determined, as shown in Fig. 9-5 by the relations among one horizontal character time, delay time of Memory Address, access time of refresh memory, and access time of character generator.

For reference, time chart from refresh memory address MA to video signal in the case of two-character time delay is shown in Fig. 9-6.



Case	Aceess Time of RM and CG	LATCH	F_{11}	F_{21}	F_{12}	F_{22}
1	RM Access—CG Access $>t_{CH}-t_{MAD}$	N	N	N	N	N
2	RM Access+CG Access $<t_{CH}-t_{MAD}$	UN	N	N	UN	UN

[NOTE] N : Necessary
UN : Unnecessary
t_{CH} : Cycle time of CHCP
t_{MAD} : Delay time of MA

Fig. 9—5 Display Control unit

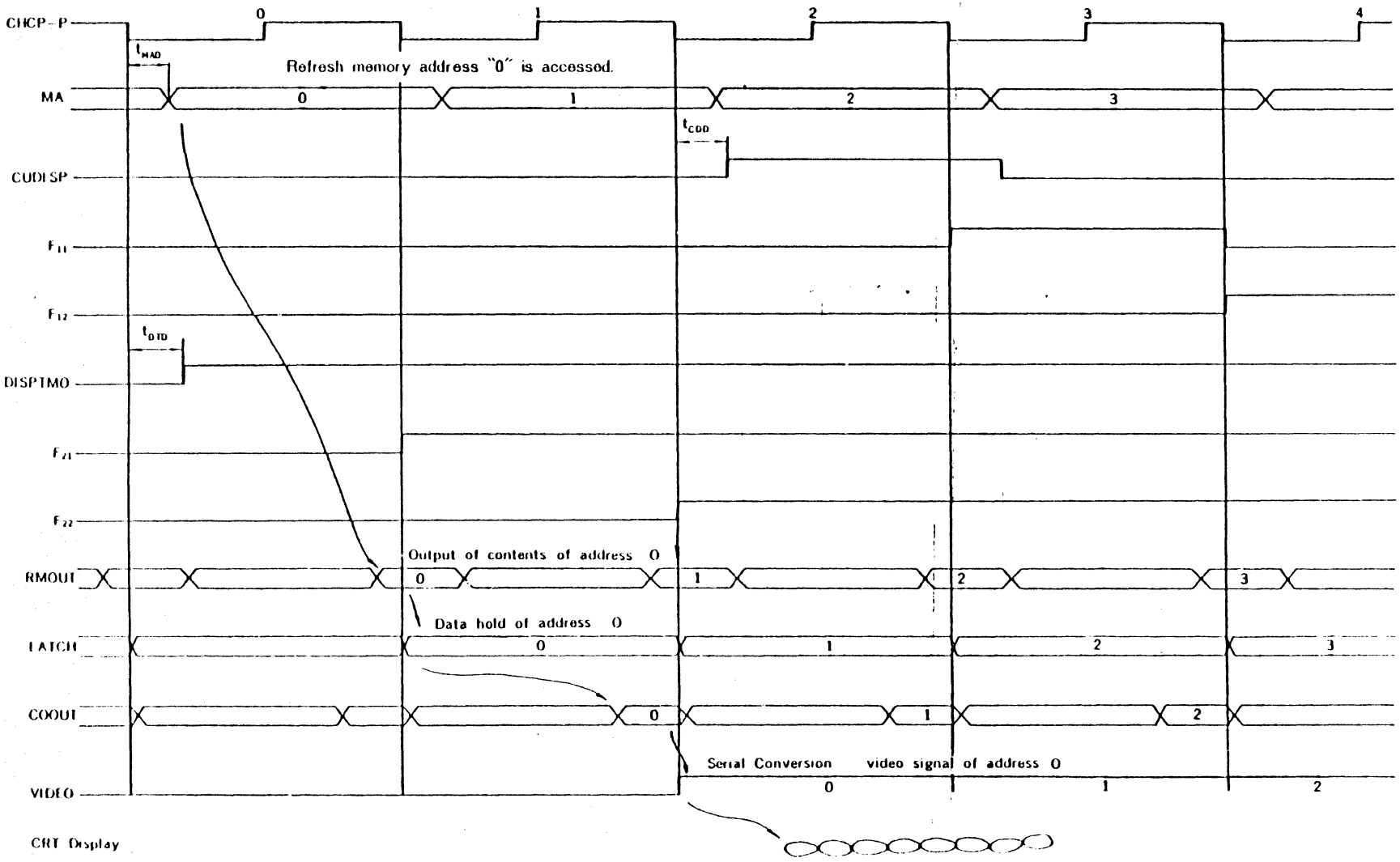


Fig. 9 - 6 Time Chart of Display Control unit

9-4 Interface to CRT

To display video signals such as characters on the CRT, sync signals which drive the deflection circuit of CRT display unit and video signals which modulate brightness of an electron beam are needed. The ways in which these signals are interfaced are different according to the CRT display devices.

Fig. 9-7 shows four typical types of interfaces to CRT display unit. Fig. 9-7(A) shows the way in which HSYNC, VSYNC, and VIDEO signals are interfaced separately to CRT display unit. Fig. 9-7(B) shows the way in which the mixed signal of HSYNC and VSYNC signals by EXCLUSIVE-OR GATE and VIDEO signal are interfaced to CRT display unit. Fig. 9-7(C) shows the way in which composite video signal of HSYNC, VSYNC, and VIDEO signals by Mixer is solely interfaced to CRT display unit. Fig. 9-7(D) shows the way in which composite video signal is modulated into high-fre quency signal by RF modulator and connected with antenna terminal of TV. This way is used in video game machines.

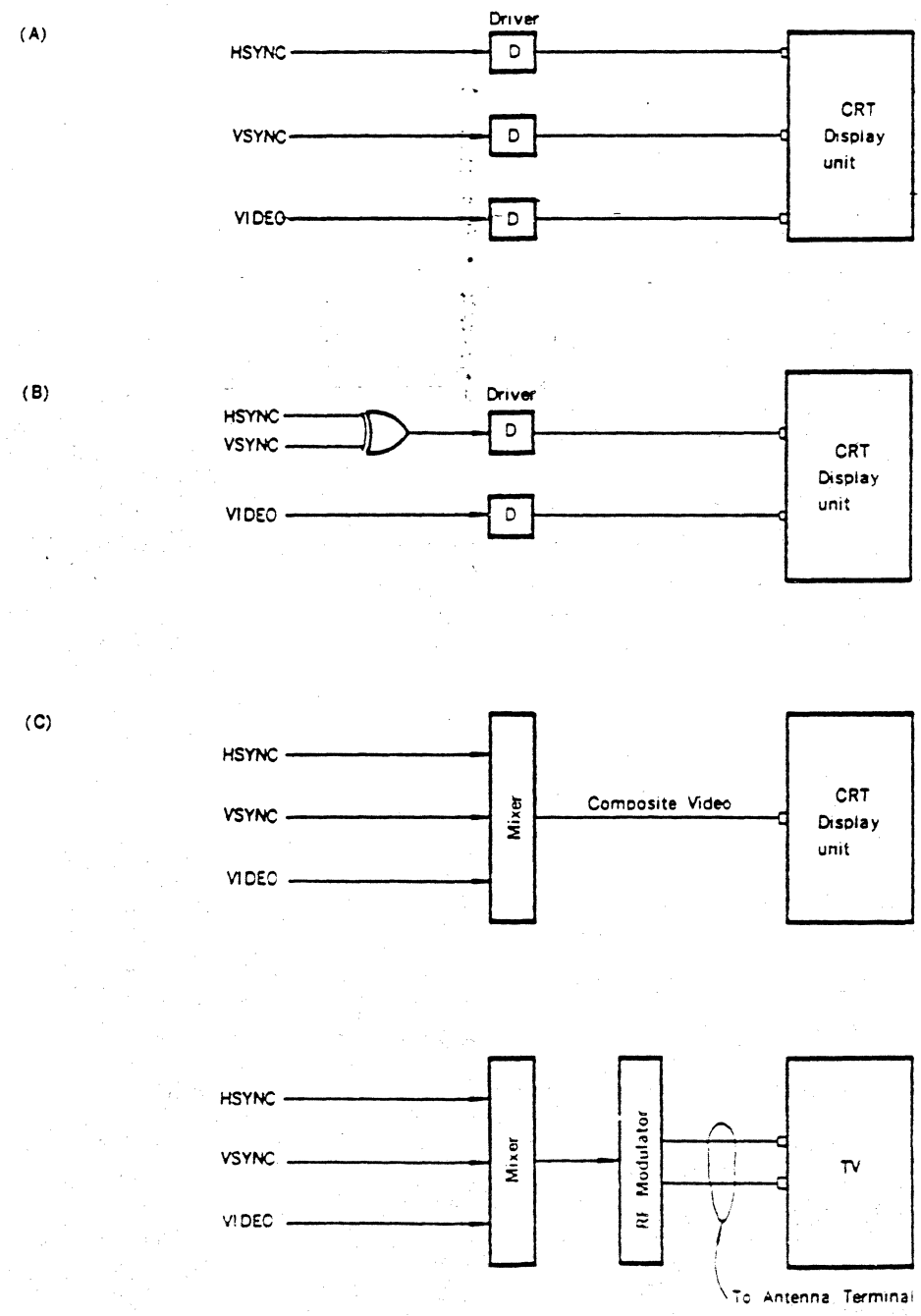


Fig. 9—7 Interface to CRT Display unit

9·5 How to Decide Parameters Set on the CRTC

Tadle. 9-1 shows parameters which are necessary for CRT display. Some of them are decided by the specification of CRT display unit (Monitor) and others are decided by the display format on the screen. Moreover, CRTC internal registers which are related to setting these parameters are shown in this Table.

Table. 9—1 Parameters For CRT Display

Item	Specification of Monitor	Screen Format	CRTC Registers
Dot Number of Characters (Horizontal)		○	External Circuits
Dot Number of Characters (Vertical)		○	R_9
Number of Horizontal Total Characters	○		R_0
Number of Horizontal Displayed Characters	△	○	R_1
Horizontal Sync Position	○		R_2
Horizontal Sync Pulse Width	○		R_3
Number of Vertical Total Characters	○		R_4
Number of Vertical Displayed Characters	△	○	R_6
Vertical Sync Position	○		R_7
Scan Mode		○	R_8
Cursor Display Method		○	R_{10}, R_{11}
Start Address		○	R_{12}, R_{13}
Cursor Address		○	R_{14}, R_{15}

△……Under the restriction of specification of CRT display unit. (Monitor)

9·5·1 How to Decide Parameters Based on Specification of CRT Display Unit (Monitor)

(1) Number of Horizontal Total Characters

Horizontal deflection frequency f_h is given by specification of CRT display unit. Number of horizontal Total characters is determined by the following equation. (Ref. 9·5·2(3))

$$f_h = \frac{1}{t_c(N_{ht}-1)}$$

where,

t_c : Cycle Time of CLK (Character Clock)

N_{ht} : Programmed Value of Horizontal Total Register (R_0)

(2) Number of Vertical Total Characters

Vertical deflection frequency is given by specification of CRT display unit. Number of vertical Total characters is determined by the following equation. (Ref. 9·5·2(4))

$$f_v = \frac{f_h}{R_t} = \frac{f_h}{(N_{vt}+1)(N_r+1)+N_{adj}}$$

where,

R_t : Number of Total Rasters per frame (Including retrace period)

N_{vt} : Programmed Value of Vertical Total Register (R_4)

N_r : Programmed Value of Maximum Raster Address Register (R_9)

N_{adj} : Programmed Value of Vertical Total Adjust Register (R_5)

(3) Horizontal Sync Pulse Width

Horizontal sync pulse width is programmed to horizontal sync width register (R_3) in unit of horizontal character time. R_3 is a 4-bit register, so programmed value can be selected within from 1 to 15.

(4) Horizontal Sync Position

As shown in Fig. 9-3, horizontal sync position is normally selected to be in the middle of horizontal blank period. But there are some cases where its optimum sync position is not located in the middle of horizontal blank period according to specification of CRT. Therefore, horizontal sync position should be determined by specification of CRT. Horizontal sync pulse position is programmed in unit of horizontal character time.

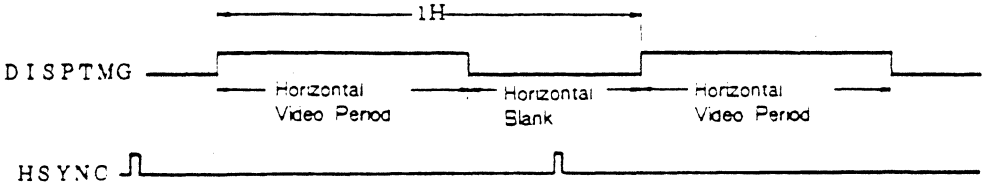


Fig. 9—8 Time Chart of HSYNC

(5) Vertical Sync Position

As shown in Fig. 9-9, vertical sync position is normally selected to be in the middle of vertical blank period. But there are some cases where its optimum sync position is not located in the middle of vertical blank period according to specification of CRT. Therefore, vertical sync position should be determined by specification of CRT. Vertical sync pulse position is programmed to vertical sync position register (R-) in unit of line period.

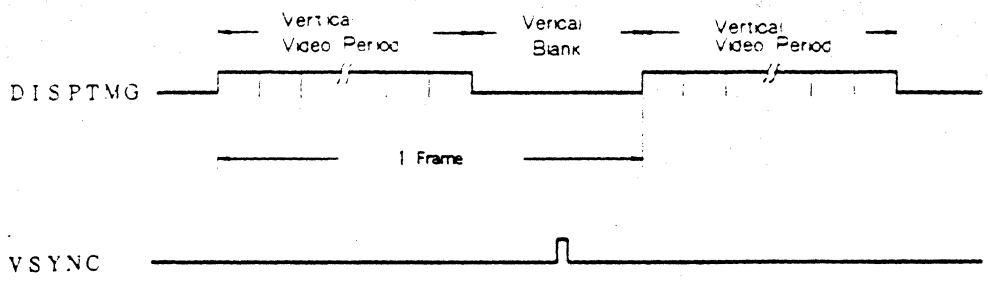


Fig. 9-9 Time chart of VSYNC

9·5·2 How to Decide Parameters Based on Screen Format

(1) Dot Number of Characters (Horizontal)

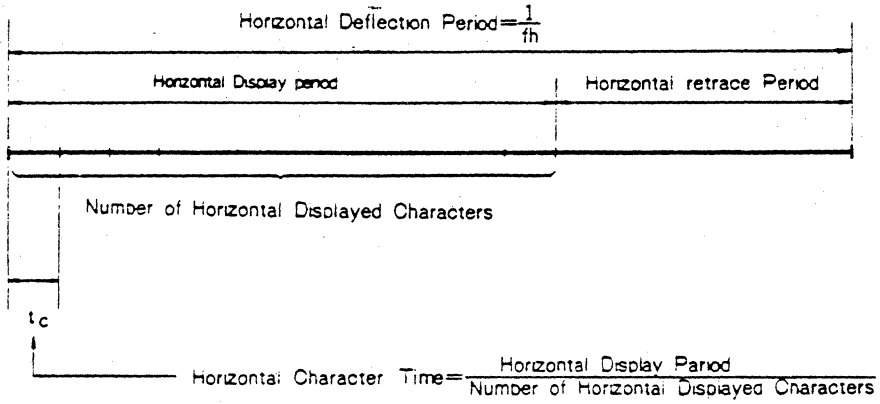
Dot number of characters (horizontal) is determined by character font and character space. More strictly, as shown in Fig. 9-2, dot number of characters (horizontal) N is determined by external N-counter.

(2) Dot Number of Characters (Vertical)

Dot number of characters (vertical) is determined by character font and line space. Dot number of characters (vertical) is programmed to maximum raster address register (R_9) of the CRTC. When N_r is programmed value of R_9, dot number of characters (vertical) is (N_r+1).

(3) Number of Horizontal Displayed Characters

Number of horizontal displayed characters is programmed to horizontal displayed register (R_1) of the CRTC. Programmed value is based on screen format. Horizontal display period, which is given by specification of horizontal deflection frequency and horizontal retrace period of CRT display unit, determines horizontal character time, being divided by number of horizontal displayed characters. Moreover, as Fig. 9-10 shows the access method of refresh memory, its cycle time and access time which are necessary for CRT display system are determined by horizontal character time.



(4) Number of Vertical Displayed Characters

Number of vertical displayed characters is programmed to vertical displayed register (R_6). Programmed value is based on screen format. As specification of vertical deflection frequency of CRT determines number of total rasters (R_7) including vertical retrace period. CRT which is suitable for desired screen format should be selected. The relation between number of vertical displayed characters and number of total rasters per frame shown in 9·5·2(2) is shown in the following equation.

$$R_7=(N_{vt}-1)(N_r-1)+N_{adj} \quad \text{(Non Interlace Mode)}$$

Number of Vertical Total Characters = Number of Vertical Displayed Characters (N_{vd}) + Number of Characters during vertical retrace period

$$R_7=(N_{vt}-1)(N_r+1)+N_{adj}+0.5 \quad \text{(Interlace Mode)}$$

For optimum screen format, it is necessary to adjust number of rasters per line, number of vertical displayed characters, and total adjust raster (N_{adj}) within specification of vertical deflection frequency.

(5) Scan Mode

The CRTC can program three scan modes shown in Table. 9-2 to interlace mode register (R_8). An example of character display in each scan mode is shown in Fig. 7-2.

Table. 9—2 Program of Scan Mode

2^1	2^0	Scan Mode	Main Usage
0	0	Non-Interlace	Normal Display of Characters & Figures
1	0		
0	1	Interlace Sync	Fine Display of Characters & Figures
1	1	Interlace Sync & Video	Display of Many Characters & Figures Without Using High-Resolution CRT

[NOTE] In interlace mode, the number of times per sec. in raster scanning on one spot on the screen is half as many as that in non-interlace mode. Therefore, when persistence of luminescence is short, flickering may happen. It is necessary to select optimum scan mode for the system, taking characteristics of CRT, raster scan speed, and number of displayed characters and figures into account.

(6) Cursor Display Method

Cursor start raster register and cursor end raster register (R_{10}, R_{11}) enable programming the display modes shown in Table 6-3 and display patterns shown in Fig. 7-3. Therefore, it is possible to change the method of cursor display dynamically according to the system conditions as well as to realize the cursor display that meets the system requirements.

(7) Start Address

Start address registers (R_{12}, R_{13}) give an offset to the address of refresh memory to read out. This enables paging and scrolling easily.

(8) Cursor Register

Cursor registers (R_{14}, R_{15}) enable programming the cursor display position on the screen. As for cursor address, it is not X, Y address but linear address that is programmed.

9·6 Relation Between Number of Displayed Characters and Memory Address

Refresh memory address of the CRTC (MA_0—MA_{13}) is linear address which starts from the value of start address. It does not need the address conversion circuit in wide use that determines the address of refresh memory to read out by line address and row address and can be used without change.

Moreover, as start address registers (R_{12}, R_{13}) enable to change the initial address of refresh memory dynamically, paging and scrolling are easily possible.

Fig. 9-10 shows memory address in the case where start address is "0" and number of displayed characters is 640 (40 characters/line x 16 lines).

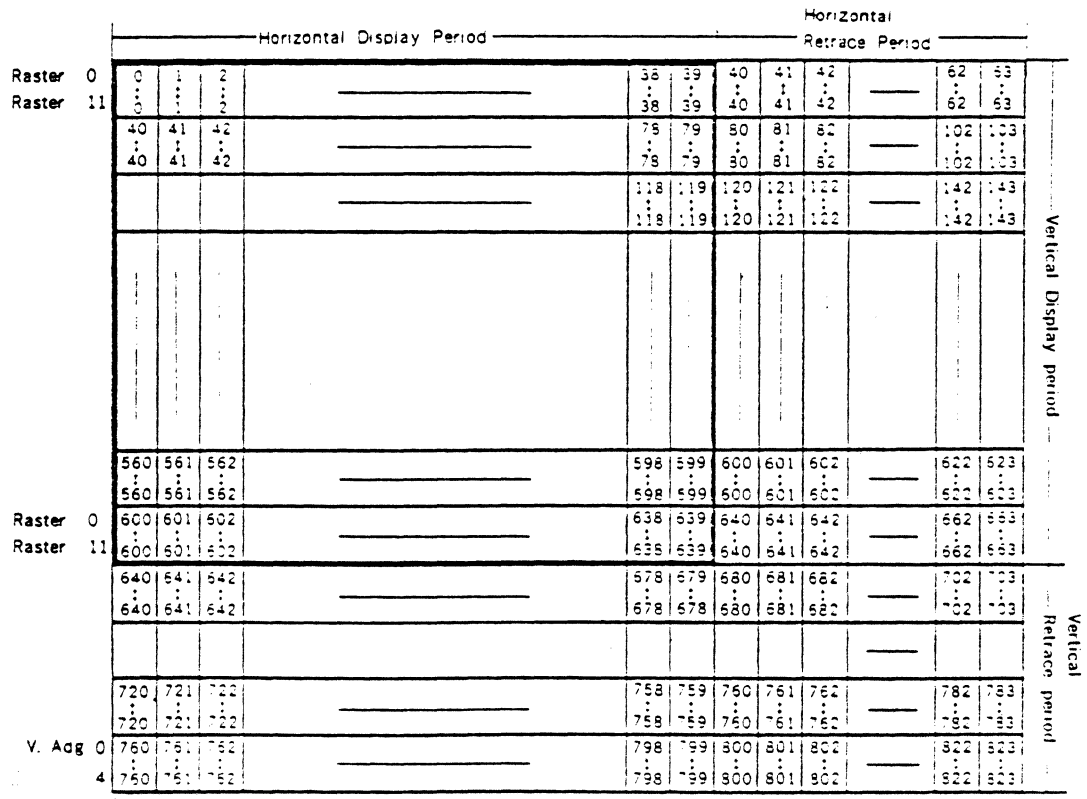


Fig. 9—10 Relation between Number of Displayed Characters and Memory Address

9·7 How to Use Start Address

Start address controls the initial address of refresh memory to read out and gives an offset to refresh memroy address within 14-bit.

Fig. 9-11 shows an example of paging to which start address is applied. In Fig. 9-11, there are refresh memories for 8 pages. Setting initial address of each page to start address registers (R_{12}, R_{13}) enables to display an optional page in a moment.

Fig 9-12 shows an example of scrolling to which start address is applied. In Fig 9-12, changing start address periodically enables to move the data to be displayed for plural pages successively on the CRT screen.

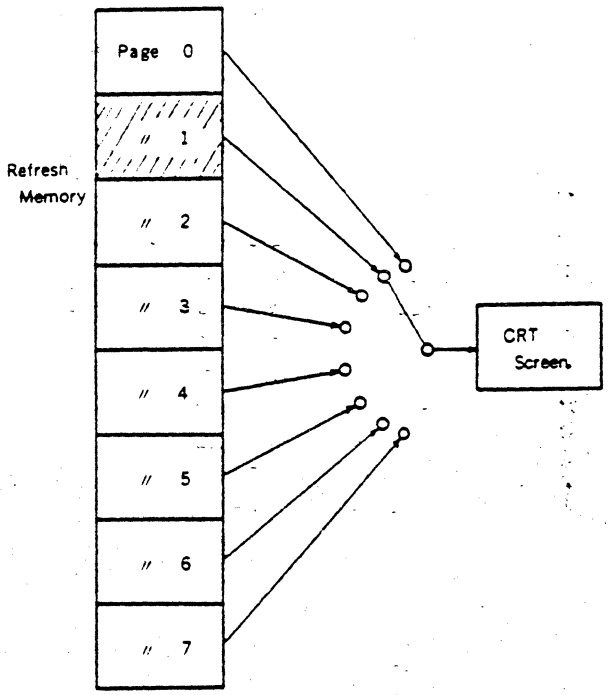


Fig. 9—11 Paging

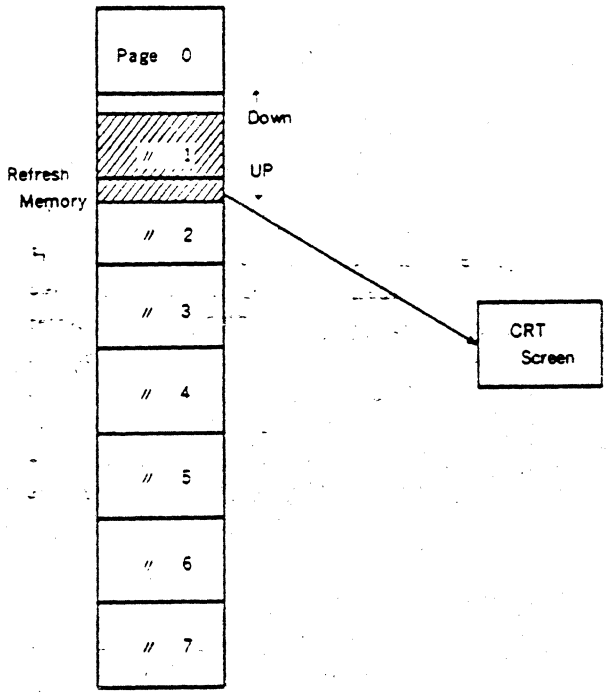


Fig. 9—12 Scrolling

9·8 How to Use Cursor Register

Cursor register is a register used to specify cursor display position on the screen and its contents are controlled by MPU. Cursor address is linear address and is itself refresh memory address of the character displayed in the cursor position.

In changing start address to $=\Delta$ x for paging and scrolling, it is necessary to change cursor address to $=\Delta$ x.

9·9 How to Use Light Pen Register

The CRTC adopts a 14-bit light pen register. When light pen detection pulse is added to LPSTB (3 pins), the values of memory address ($MA_0 \sim MA_{13}$) are stored. As Light pen detection pulse is asynchronous with memory address timing, so its internal synchronization circuit makes the detection operation certain. The detection address involves the delay time of the system (from pulse output of light pen after a character is displayed on the screen and light pen detects it to LPSTB input of the CRTC), so its value needs to be corrected in software. Light pen detection address is itself refresh memory address. When cursor is moved to light pen detection position, the value corrected in software is written into cursor register. When the character indicated by light pen is read out, the corrected value is used as refresh memory address to read out. As for frame address that light pen indicates, start address needs to be excluded from the corrected value because the corrected value is also modified with start adress.

Fig. 9-13 shows a typical example of light pen control circuit. As shown in Fig. 9-13, some external circuits enable to use light pen. There are some ways of interfacing between light pen and MPU. These are:

(a) Interrupt Method
(b) Program Scan Method etc.

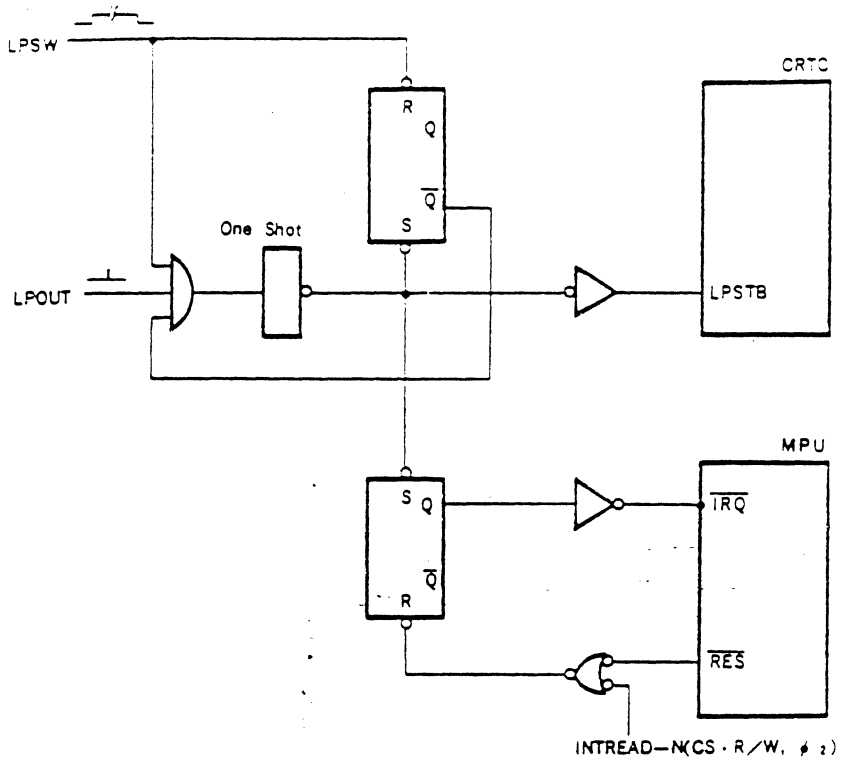


Fig. 9—13 Light Pen Control Circuit

Fig. 9-14 shows an interrupt method of interfacing. When light pen detects light, LPSTB signal and an interrupt signal $\overline{IRQ}$ are respectively provided to the CRTC and MPU. Fig. 9-15 shows the program of this interrupt method.

Fig. 9-16 shows a program scan method of interfacing. When LPSTB signal is provided to the CRTC, light pen sets up a detection FLAG. MPU reads out this FLAG periodically and when FLAG is "1", the contents of light pen register are read out. Table. 9-17 shows the program of this program scan method.

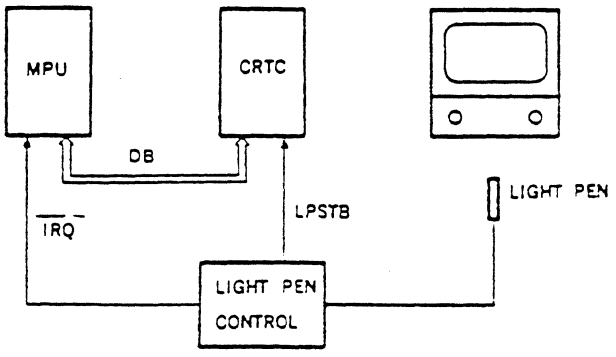


Fig. 9—14 Interfacing of Light Pen

```
INTERRUPT  LDA A  #16    LOAB LPH ADDRESS
                         INTO ACCA
           STA A  A0     STORE ACCA INTO
                         ADDRESS REGISTER
           LDA A  A0+1   LOAD LPH DATA
                         INTO ACCA
           LDA B  #17    LOAD LPL ADDRESS
                         INTO ACCB
           STA B  A0     STORE ACCB INTO
                         ADDRESS REGISTER
           LDA B  A0+1   LOAD LPL DATA
                         INTO ACCB
           ---
           ---
           ---
           ---
           RTI           RETURN FROM
                         INTERRUPT
```

Fig. 9-15 Read Operation of Light Pen Register

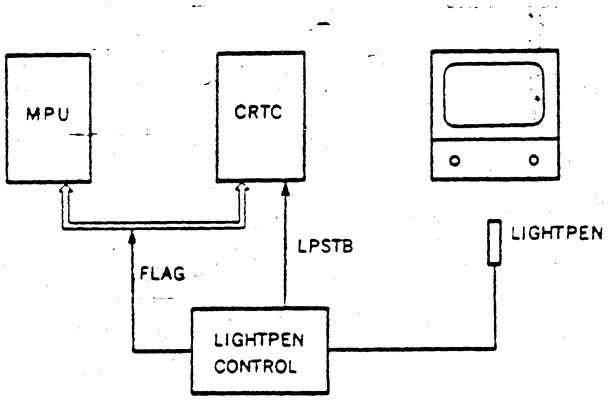


Fig. 9—16 Interfacing of Light Pen

```
---
---
LDA  A  LPFLAG   LOAD LPFLAG INTO ACCA
BIT  A  #1       BIT TEST
BEQ     *-5      TRY AGAIN IF LPPLAG=0
LDA  A  #16      LOAD LPH ADDRESS INTO
                 ACCA
STA  A  A0       STORE ACCA INTO ADDRESS
                 REGISTER
LDA  A  A0+1     LOAD LPH DATA INTO ACCA
LDA  B  #17      LOAD LPL ADDRESS INTO
                 ACCB
STA  B  A0       STORE ACCB INTO ADDRESS
                 REGISTER
LDA  B  A0+1     LOAD LPL DATA INTO ACCB
CLR     LPFLAG   CLEAR LPFLAG
---
---
```

Fig. 9-17 Read Operation of Light Pen Register

9 10 Access Method to Refresh Memory

For CRT display with the CRTC, refresh memory is accessed by CRTC's memory address (MA_0~MA_{13}) to refresh the screen periodically and also accessed by MPU in changing the contents to be displayed. As for access method by MPU, there are asynchronous access method that has no relation to the display condition and synchronous access method that avoids the display period. Fig. 9-18 shows an example of asynchronous access methods. In this case, MPU address specifies refresh memory address and the output of address multiplexer is switched over to address bus side. Therefore, a part of the screen may flash in a moment. Fig. 9-19 shows a program of asynchronous access method.

Fig. 9-20 shows an example of synchronous access methods. In this case, MPU reads out DISPTMG output of CRTC and only when DISPTMG is "Low"(horizontal and vertical retrace periods), refresh memory is accessed by MPU. In synchronous access method, there is no competition between MPU access and display access, the screen doesn't flash. Fig. 9-21 shows a program in this case.

Fig. 9-22 shows another example of synchronous access methods. In this case, a character time is devided into MPU access time and display accesstime. In MPU access time MPU is synchronized by stretching MPU clock ϕ_2 by $\overline{\text{READY}}$ signal till its access is finished. Fig. 9-23 shows a program of this case.

Moreover, as there are many other access methods including these typical examples, the most reasonable method should be selected according to each system.

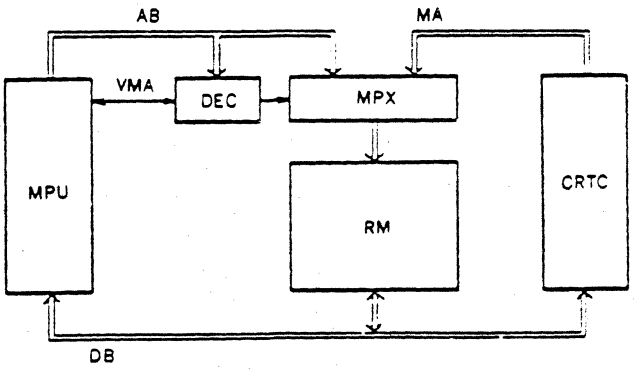


Fig. 9—18 Asynchronous Access to RM

```
STA   A   RM    STORE ACCA INTO RM LOCATION
LDA   A   RM    LOAD RM LOCATION INTO ACCA
```

Fig. 9-19 Program of Asynchronous Access to RM

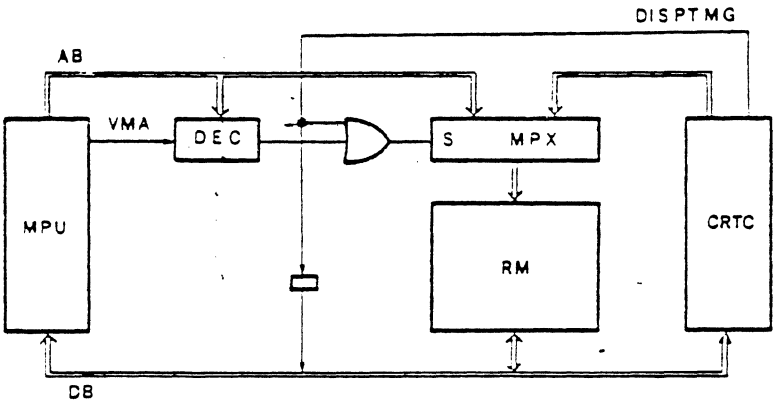


Fig. 9—20 Synchronous Access to RM (1)

```
LDA   A   DT    LOAD DISPTMG INTO ACCA
BIT   A   #1    BIT TEST
BGT       *-5   TRY AGAIN IF DT=1
STA   B   RM    STORE ACCB INTO RM LOCATION
LDA   A   DT    LOAD DISPTMG INTO ACCA
BIT   A   #1    BIT TEST
BEQ       *-5   SKIP IF ACCA=0
LDA   B   RM    LOAD RM LOCATION INTO ACCB
```

Fig. 9-21 Program of Synchronous Access to RM(1)

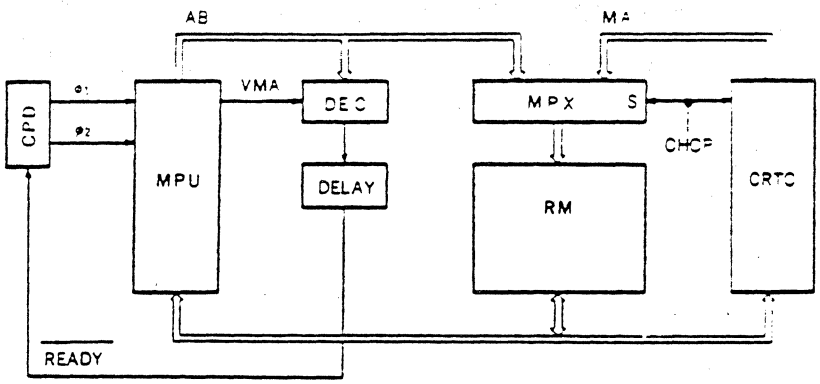


Fig. 9—22 Synchronous Access to RM (2)

```
      ---
      ---
      ---
STA   A   RM    STORE ACCA INTO RM LOCATION
      ---
      ---
      ---
      ---
LDA   A   RM    LOAD RM LOCATION INTO ACCA
      ---
      ---
```

Fig. 9-23 Program of Synchronous Access to RM (2)

10. Program of the CRTC

10-1 READ/WRITE Operation of Internal Registers

As shown in Table. 6-1, the CRTC has 18 internal registers and 1 address register that specifies address of these registers.

Therefore, READ/WRITE operation of internal registers should be done through 2 steps in a pair.

STEP 1. Register address is written into address register by STORE command.

STEP 2. The contents of the specified register are read by LOAD command, or are written into the specified register by STORE command.

READ/WRITE procedure of internal registers is shown in Fig. 10-1 and an example of its program is shown in Fig. 10-2.

When address register is accessed, it is necessary to assign address so that RS may be "Low" (pin 24). When an internal register is accessed, it is necessary to assign address so that RS may be "High".

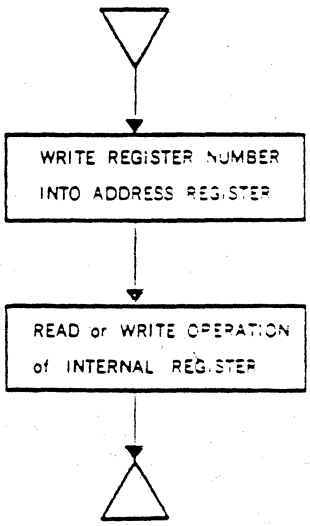


Fig. 10—1 READ/WRITE Procedure of Internal Register

```
        —
LDA   A   #15     LOAD REGISTER NUMBER INTO ACCA
STA   A   A0      STORE ACCA INTO ADDRESS REGISTER
LDA   A   A0+1    LOAD CURSOR LOWER BYTE INTO ACCA
        —
        —
LDA   A   #15     LOAD REGISTER NUMBER INTO ACCA
STA   A   A0      STORE ACCA INTO ADDRESS REGISTER
LDA   A   DATA    LOAD WRITE DATA INTO ACCA
STA   A   A0+1    STORE ACCA INTO CURSOR LOWER BYTE
                  REGISTER
        —
        —
```

Fig.10-2 READ/WRITE Program of Internal Register

10.2 Initializing Program of the CRTC

For desirable display control function of the CRTC, it is necessary to initialize 16 internal registers except light pen register after the system power supply is established by power on.

Fig.10-3 shows a flow chart of initializing program and Fig.10-4 shows the program based on this flow chart. In this example, the number of program steps is decreased by looping the program storing the initializing data in order of register address in a table.

Table.10-1 shows an example of initializing values for character display. In this case, there no paging and scrolling. So start address should be always "0". Cursor's initializing position shall be usually in home position, though it can be anywhere within valid memory address of system(0~639 in Table.10-1).

When cursor address is out of valid memory address, it is necessary to be careful because cursor display position is not guaranteed. Table. 10-3 and Table.10-4 show an example of initializing values for full graphic display.

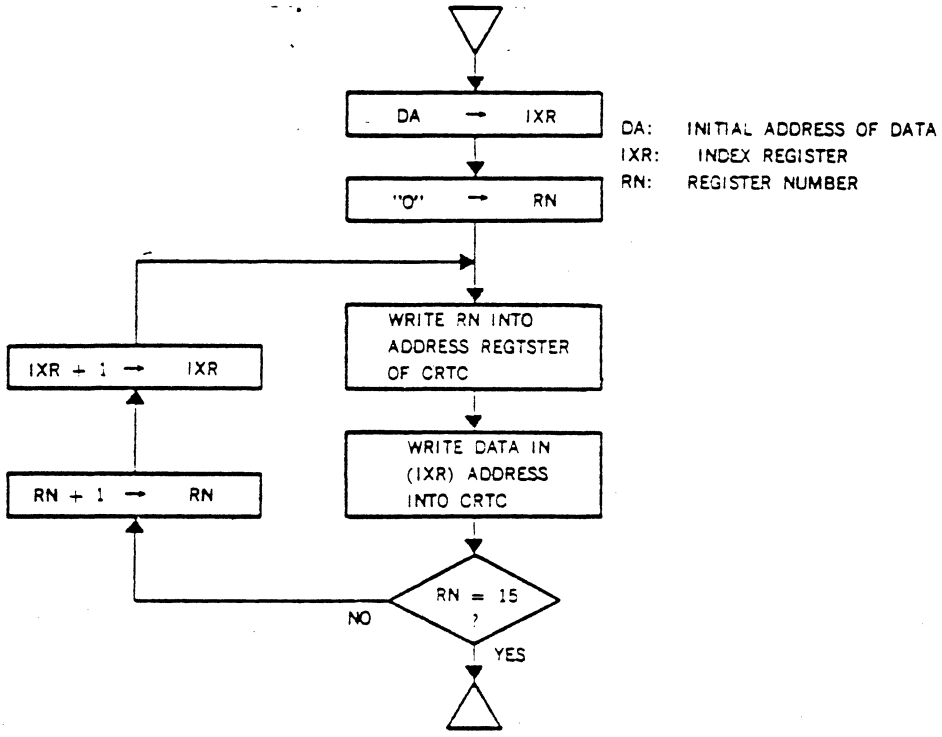


Fig. 10—3 Initializing Flow Chart of The CRTC

```
      LDX   #DA    LOAD DATA ADDRESS INTO INDEX
                   REGISTER
      CLR   A      CLEAR ACCA
ILRI  STA   A  A0  STORE REGISTER NUMBER INTO ADDRESS
                   REGISTER
      LDA   B  0,X LOAD INITAL DATA INTO ACCB
      STA   B  A0+1 STORE ACCB INTO CRTC REGISTER
      CMP   A  #15
      BEQ      ILR2 BRANCH IF COMPLETE
      INC   A      INCREMENT ACCA
      INX          INCREMENT INDEX REGISTER
      BRA      ILRI BRANCH TO ILRI
ILR2  —
      —
```

Fig. 10—4 Initializing Program of the CRTC

Table.10-1 Specification of Character Display Example

Item	Specificaton
Scan Mode	Non-Interlace
Horizontal Deflection Frequency	15.625 KHz
Vertical Deflection Frequency	60.1 Hz
Dot Frequency	8 MHz
Character Dot(Horizontal x Vertical)	8 x 12
Number of Displayed Characters (Row x Line)	40 x 16
HSYNC Width	4 μs
Cursor Display	Raster 9—10, Blink:16Field Period
Paging, Scrolling	——

Table.10-2 Initializing Values for Character Display

Register No.	Name	Initializing Value (Decimal)
R_0	Horizontal Total	63
R_1	Horizontal Displayed	40
R_2	Horizontal Sync Position	52
R_3	Horizontal Sync Width	4
R_4	Vertical Total	20
R_5	Vertical Total Adjust	8
R_6	Vertical Displayed	16
R_7	Vertical Sync Position	19
R_8	Interlace Mode	0
R_9	Maximum Raster Address	11
R_{10}	Cursor Start Raster	73
R_{11}	Cursor End Raster	10
R_{12}	Start Address (H)	0
R_{13}	Start Address(L)	0
R_{14}	Cursor (H)	0
R_{15}	Cursor (L)	0

Table.10-3 Specification of Full Graphic Display (Example)

Item	Specification
Scan Mode	Non-Interlace
Horizontal Deflection Frequency	15.625 KHz
Vertical Deflection Frequency	60.1 Hz
Dot Frequency	8 MHz
Character Dot(Horizontal x Vertical)	8 x 8
Number of Displayed Characters (Row x Line)	32 x 24
Number of Display Dot(Horizontal x Vertical)	256 x 192
HSYNC Width	4 μs
Cursor Display	—
Paging, Scrolling	—

Table.10-4 Initializing Values for Full Graphic Display

Register No.	Name	Initializing Value (Decimal)
R_0	Horizontal Total	63
R_1	Horizontal Displayed	32
R_2	Horizontal Sync Position	47
R_3	Horizontal Sync Width	4
R_4	Vertical Total	31
R_5	Vertical Total Adjust	4
R_6	Vertical Displayed	24
R_7	Vertical Sync Position	28
R_8	Interlace Mode	0
R_9	Maximum Raster Address	7
R_{10}	Cursor Start Raster	—
R_{11}	Cursor End Raster	—
R_{12}	Start Address (H)	0
R_{13}	Start Address (L)	0
R_{14}	Cursor (H)	—
R_{15}	Cursor (L)	—

10.3 Program of Paging

As shown in Fig.9-11, paging is to select a desired page from refresh memories for plural pages. Fig.10-5 shows a flow chart of paging. In this example, input for selecting a page is derived from page KEY. This is a very easy program where initial address of refresh memory corresponding to the selected page is set to start address register.

Then, as shown in 9.8, cursor address should be modified by the same number which start address is changed by.

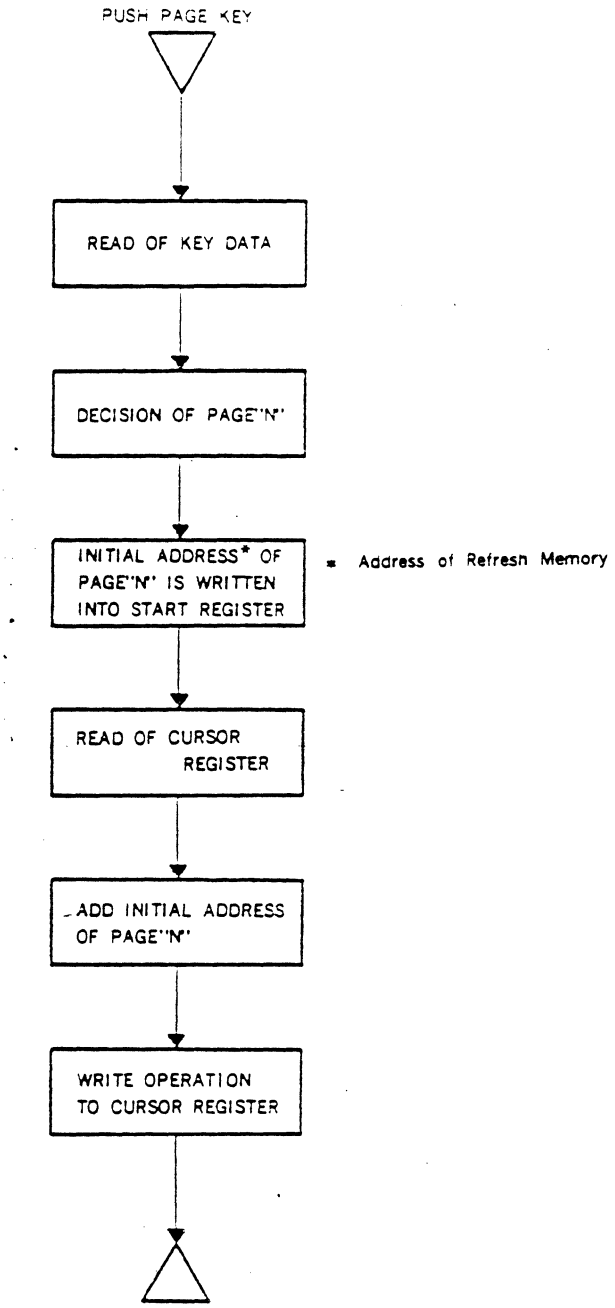


Fig. 10—5 Program of Paging

10.4 Program of Scrolling

There are two kinds of scrolling. One is page scrolling shown in Fig.9-12. In this case, the data of refresh memories for plural pages are moved up and down. The other is teletype scrolling. In this case, refresh memories are for only one page, so new data is displayed at the bottom line, scrolling up one line by scroll up command.

Fig.10-6 shows a flow chart of page scrolling. In this example, scroll key controls up and down of scrolling. In scrolling up, when start address is the same as initial address of the last page, scrolling up is ignored. When start address is the same as address of initial page, scrolling down is ignored.

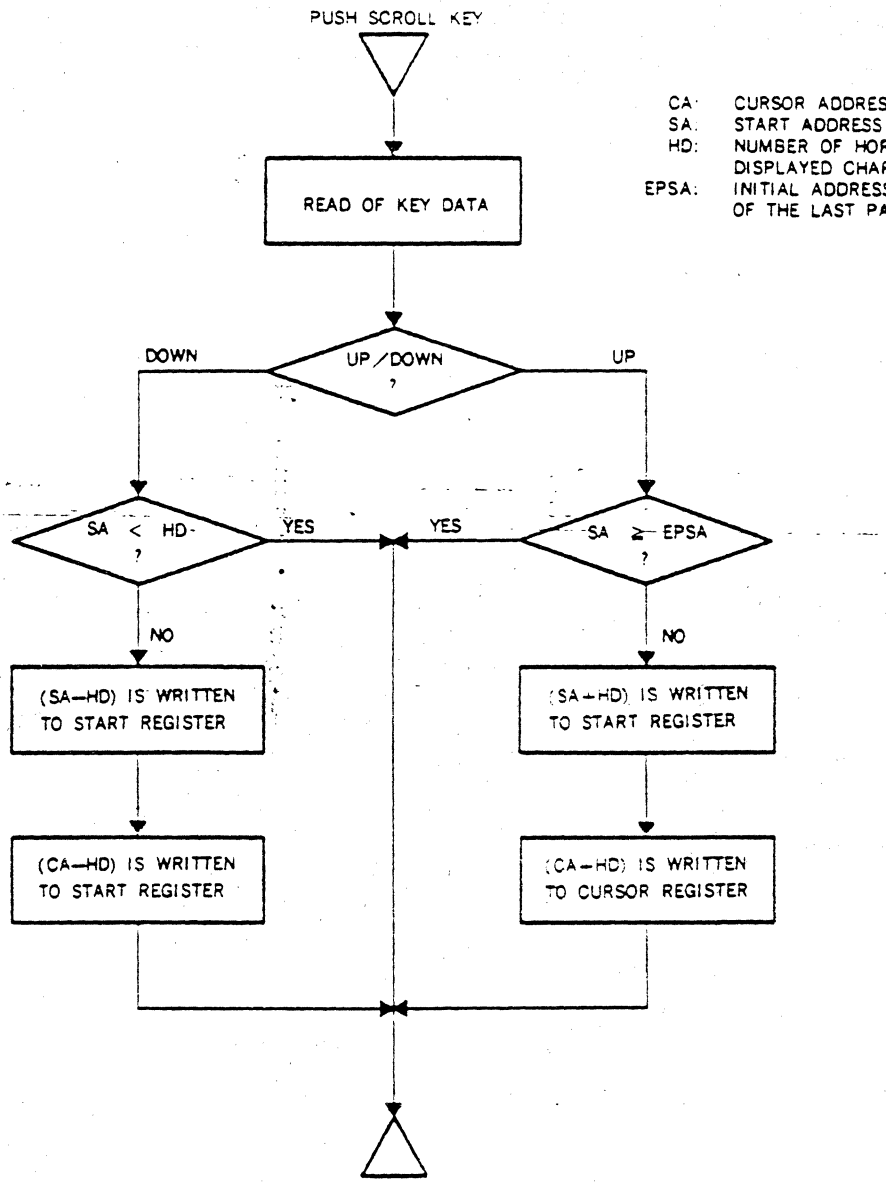


Fig. 10—6 Page Scrolling

Another scrolling is teletype scrolling where a program controls start address etc. Fig.10-7 shows a flow chart of teletype scrolling. After scroll command has changed the line under the bottom line to space to display new data, only one line is scrolled up. Fig.10-8 shows an example of addressing of teletype scrolling.(Scroll up). In this example, the number of displayed characters is 1920 and refresh memory is 2048 bytes. Refresh memory has an excess by 128 bytes, and address above 2048 is ignored in the hardware and the software to do teletype scrolling shown in Fig.10-8. Its higher 3 address bits being ignored, refresh memory is wrapped around and the address next to 2047 becomes "0". As refresh memory size is more than the number of displayed characters by 128 bytes, a boundary of data in it moves successively. Therefore, READ/WRITE address of data is determined relatively by start address under the control of a program and other basic address. Whether it is page scrolling or teletype scrolling, start address is changed in unit of the number of horizontal displayed characters. Then the contents of cursor register should be also changed by the same number.

Moreover, increment or decrement of start address easily enables scrolling in unit of a character as well as in unit of a line shown in this example.

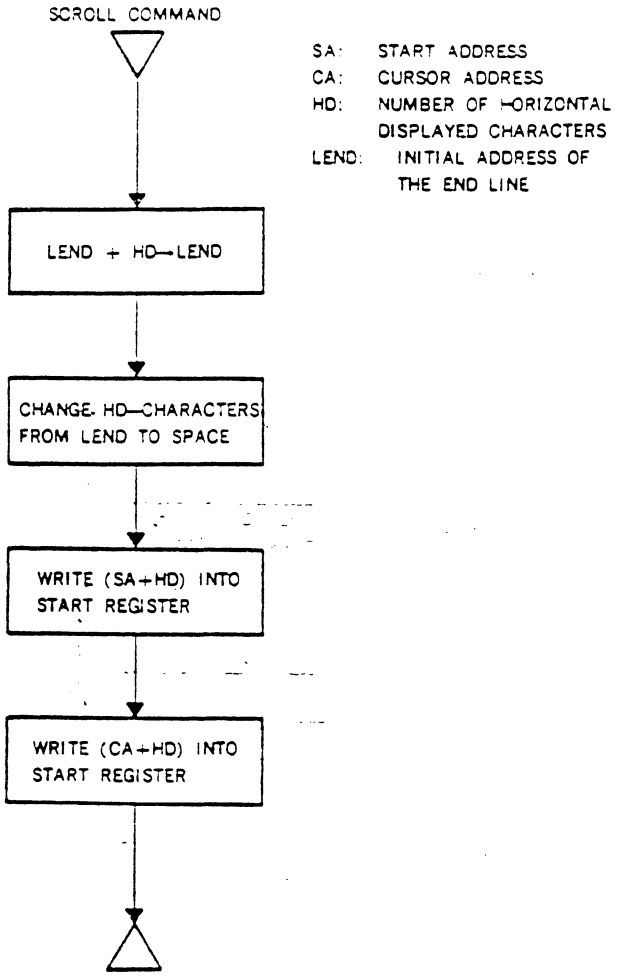


Fig. 10—7 Teletype Scrolling (Procedure of Scroll Command)

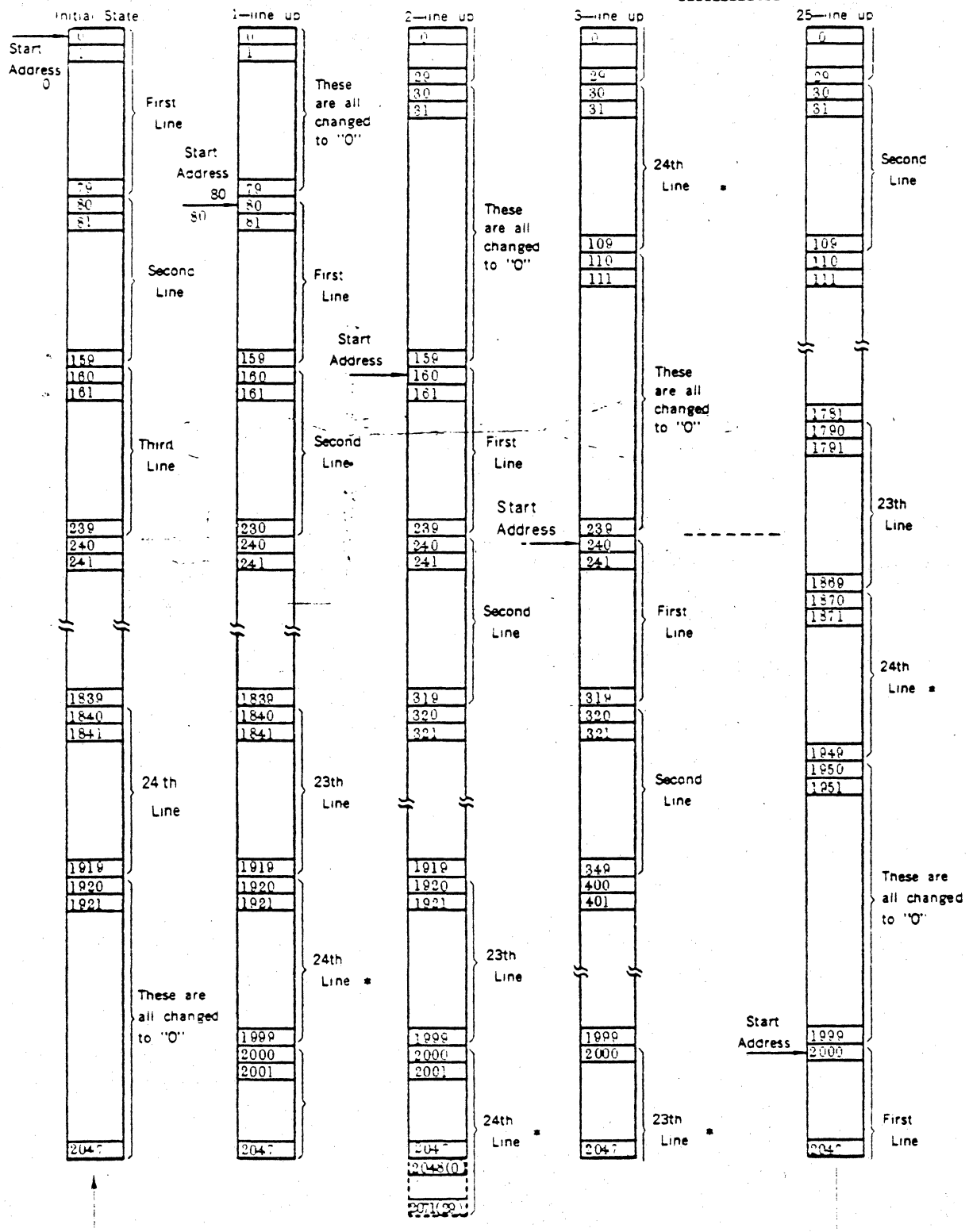


Fig. 10—8 Example of Addressing in Teletype Scrolling (2048—Word memory is used for 80 characters x 24 lings.)

10.5 Program of Cursor Control

Cursor is used as a pointer to indicate the data input position on the screen. It can be located anywhere on the screen and is usually controlled by cursor keys. These keys are the followings:

- → shift cursor one place to the right
- ← shift cursor one place to the left
- ↑ shift cursor one place up
- ↓ shift cursor one place down
- HM shift cursor to home position

Fig.10-9 shows an example of cursor's right shift and down shift. In this example, when cursor is located at the end of a line, pushing → key shifts it to the beginning of next line. When cursor is located at the end of bottom line, pushing → key shifts it to home position. Moreover, when cursor is located at bottom line, pushing ↓ key shifts it to top line of the same row.

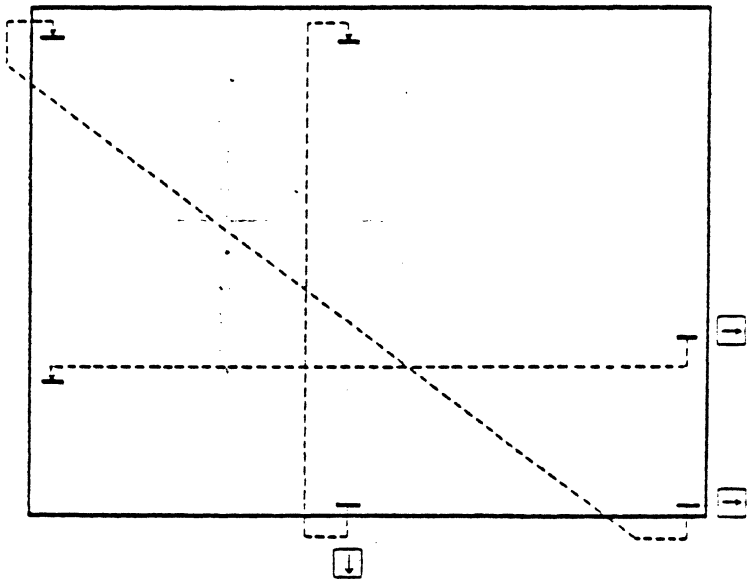


Fig. 10—9 Cursor Control

Fig.10-10 shows a flow chart of cursor's right shift and Fig.10-11 shows a flow chart of cursor's down shift.

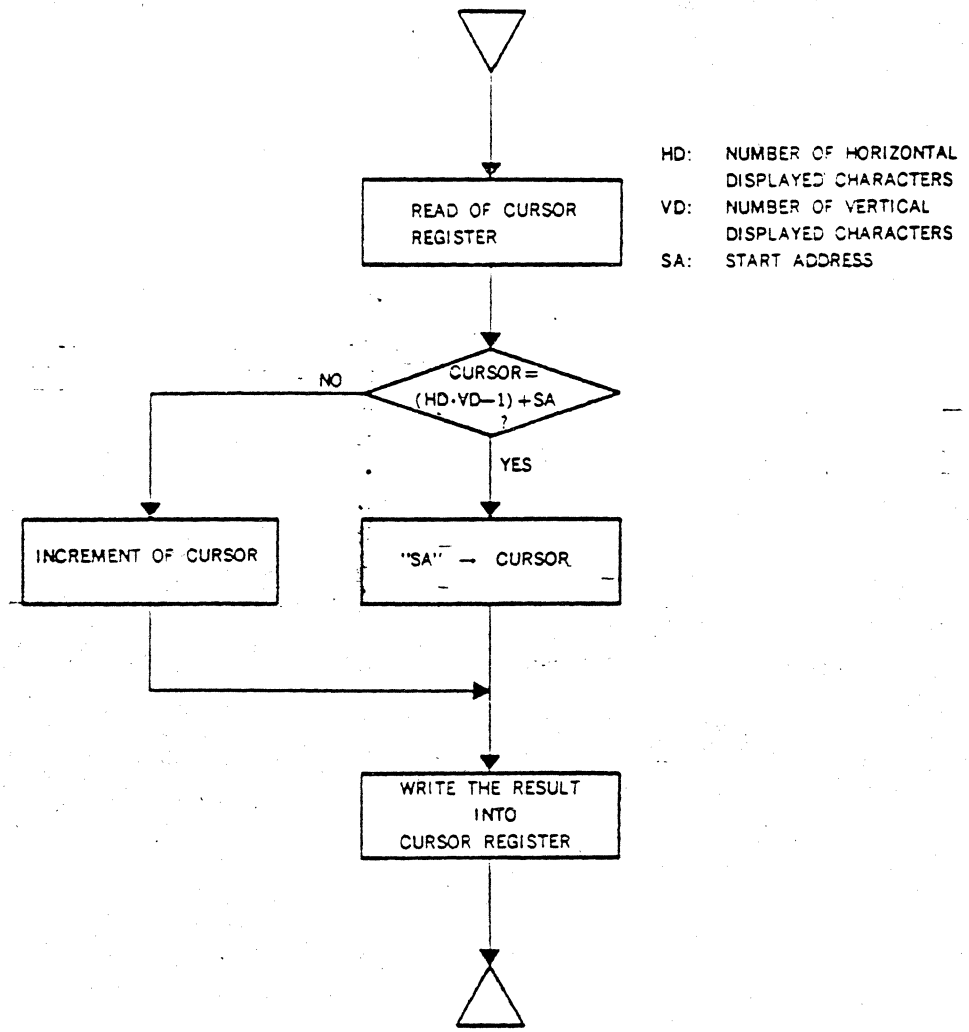


Fig. 10—10 Cursor's Right Shift

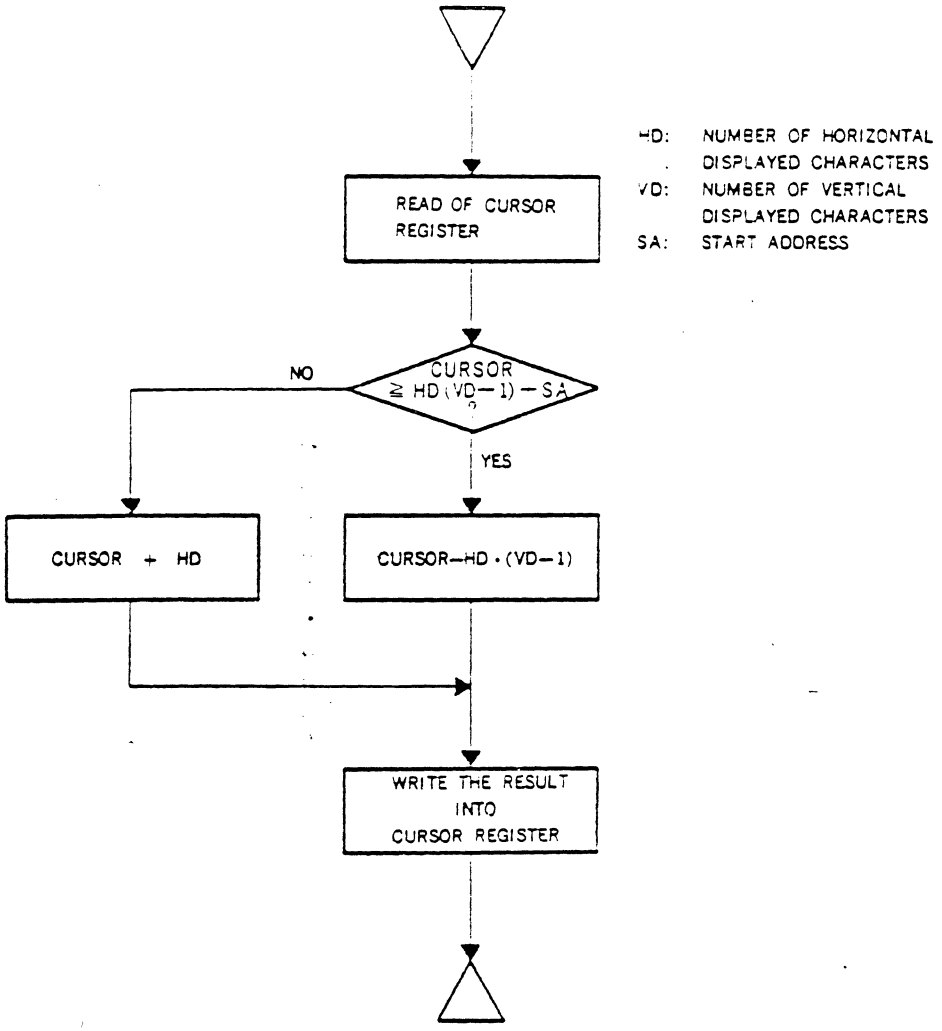


Fig. 10—11 Cursor's Down Shift

10.6 Program of Light Pen Control

Combination of light pen with CRT display enables various functions such as the followings.

(1) Shift cursor to light pen position
(2) Input of address of light pen position to CPU
(3) Input of data of light pen position to CPU
(4) Move the data of light pen position to other display position etc.

Fig.10-12 shows a flow chart of cursor shift using light pen. In this example, light pen and CPU are interfaced by an interrupt method and a program of light pen starts with this interrupt.

Light pen detection address is linear address and writing the corrected result of system delay into cursor register without change enables cursor shift to light pen position.

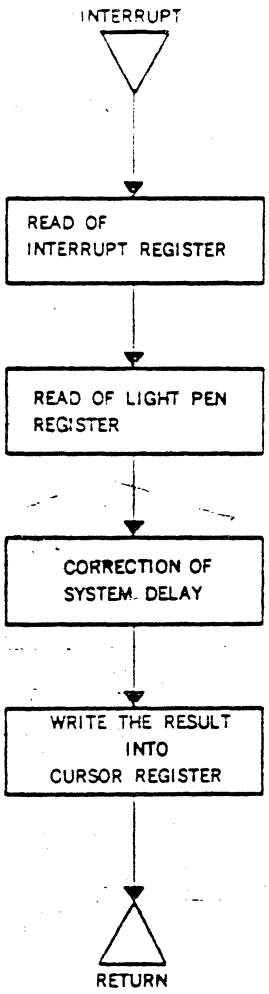


Fig. 10—12 Program of Light Pen

11. Applications of the CRTC

11.1 Monochrome Character Display

Fig. 11-1 shows a system of monochrome character display. Character clock signal(CLK) is provided to the CRTC through OSC and dot counter. It is used as basic clock which drives internal control circuits. MPU is connected with the CRTC by standard bus and controls the CRTC initialization and READ/WRITE of internal registers.

Refresh memory is composed of RAM which has capacity of one frame at least and the data to be displayed is coded and stored. The data to refresh memory is changed through MPU bus, while refresh memory is read out successively by the CRTC to display a static pattern on the screen. Refresh memory is accessed by both MPU and the CRTC, so it needs to change its address selectively by multiplexer. The CRTC has 14 MA(Memory Address output), but in fact some of them that are needed are used according to capacity of refresh memory.

Code output of refresh memory is provided to character generator. Character generator reads out a dot pattern of a specified raster of a specified character in parallel by code output of refresh memory and RA(Raster Address output) of the CRTC and provids it out to parallel-serial converter(P→S). Parallel-serial converter is normally composed of shift register to convert output of character generator into a serial dot pattern. Moreover, DISPTMG, CUDISP, HSYNC, and VSYNC signals are provided to video control circuit. It controls blanking for output of parallel-serial converter, mixes these signals with cursor video signal, and generates sync signals for an interface to monitor.

11.2 Color Character Display

Fig.11-2 shows a system of color character display. In this example, a 3-bit color control bit(R,G,B) is added to refresh memory in parallel with character code and provided to video control circuit. Video control circuit controls coloring as well as blanking and provids three primary color video signals(R,G,B signals) to CRT display device to display characters in seven kinds of color on the screen.

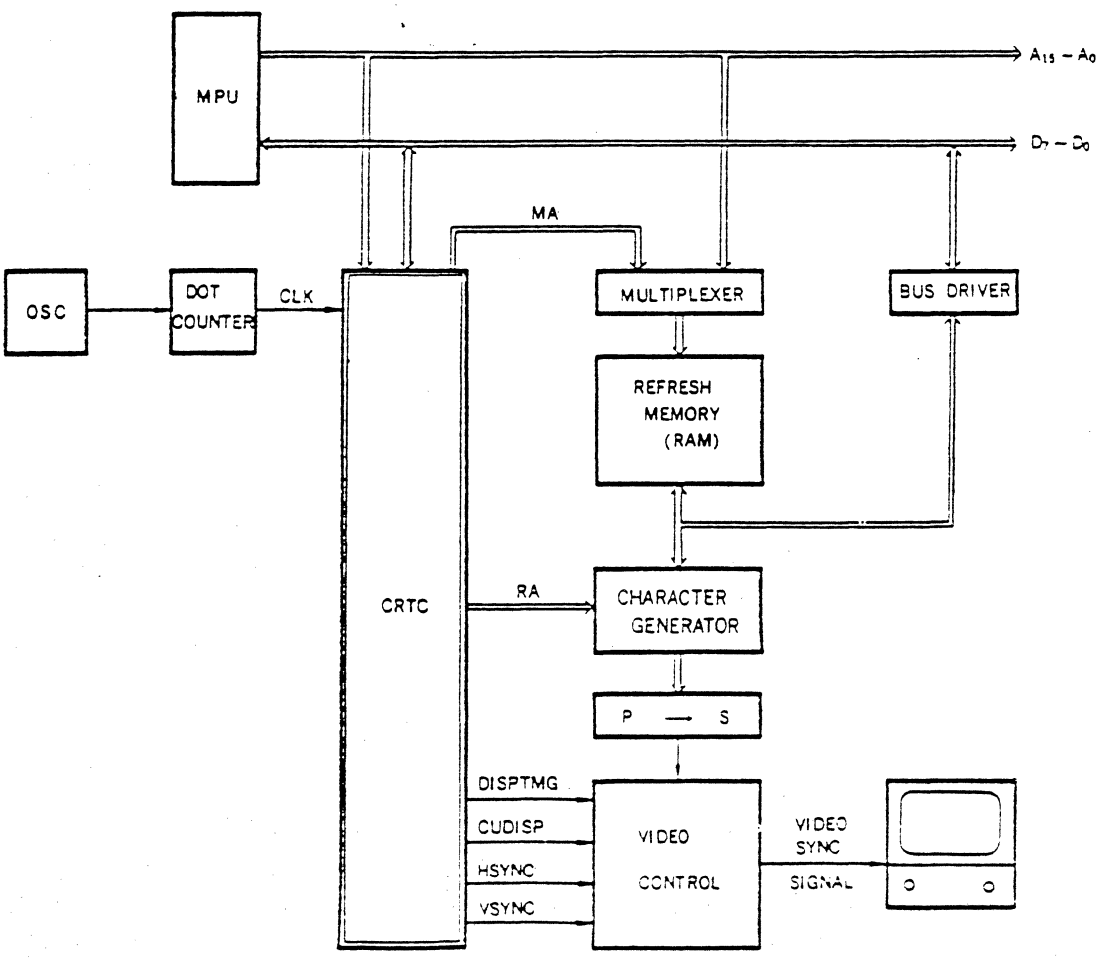


Fig. 11—1 Monochrome Charater Display

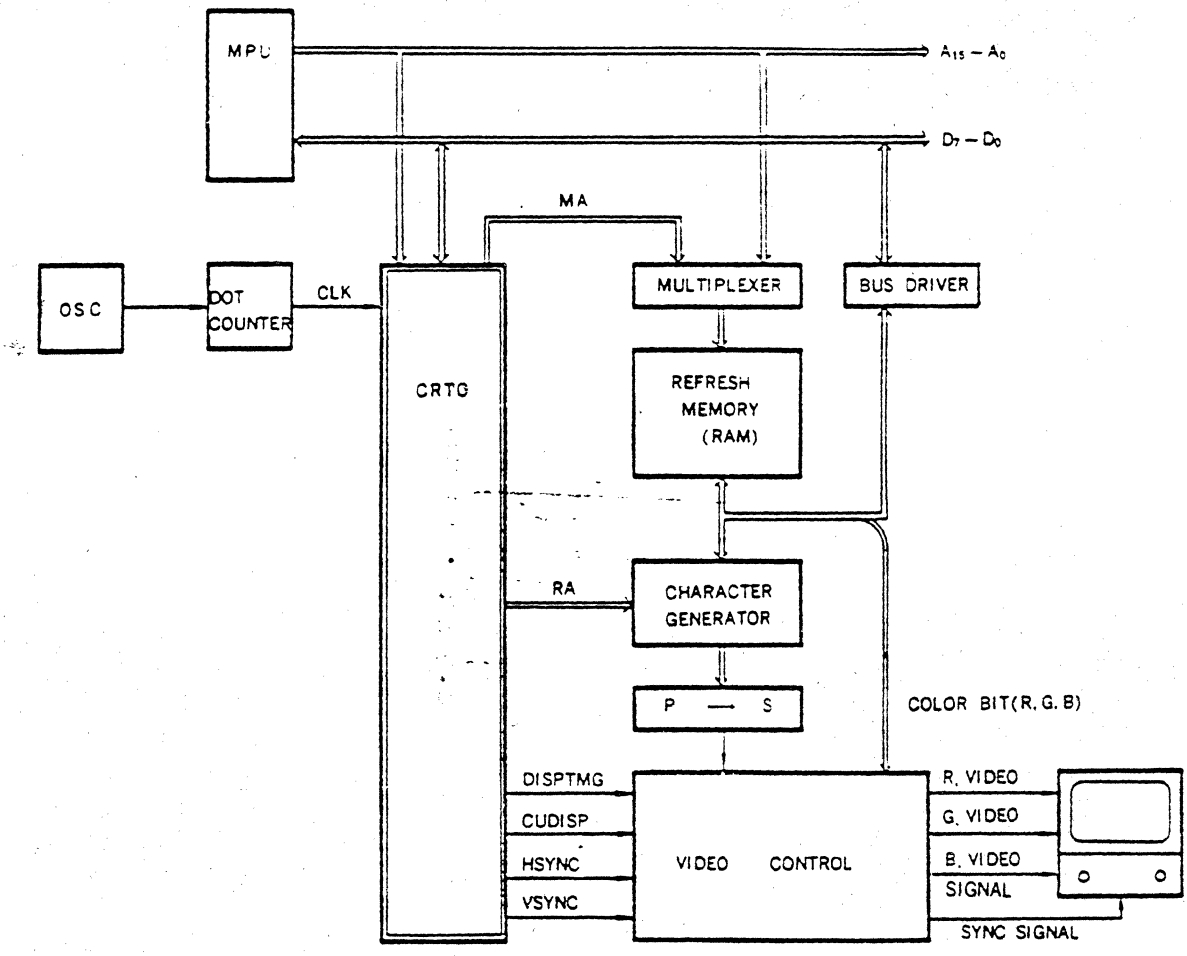


Fig. 11—2 Color Character Display

11.3 Color limited Graphic Display

Limited graphic display is to display simple figures as well as character display by combination of writable symbols which are defined in unit of one character.

As shown in Fig.11-3, graphic pattern generator is set up in parallel with character generator and output of these generators are wire-ORed. Which generator is accessed depends on coded output of refresh memory.

In this example, graphic pattern generator adopts ROM, so only the combination of writable symbols which are programmed to it is possible. Adopting RAM instead of ROM enables dynamically writable symbols in any combination on one display by changing the contents of them.

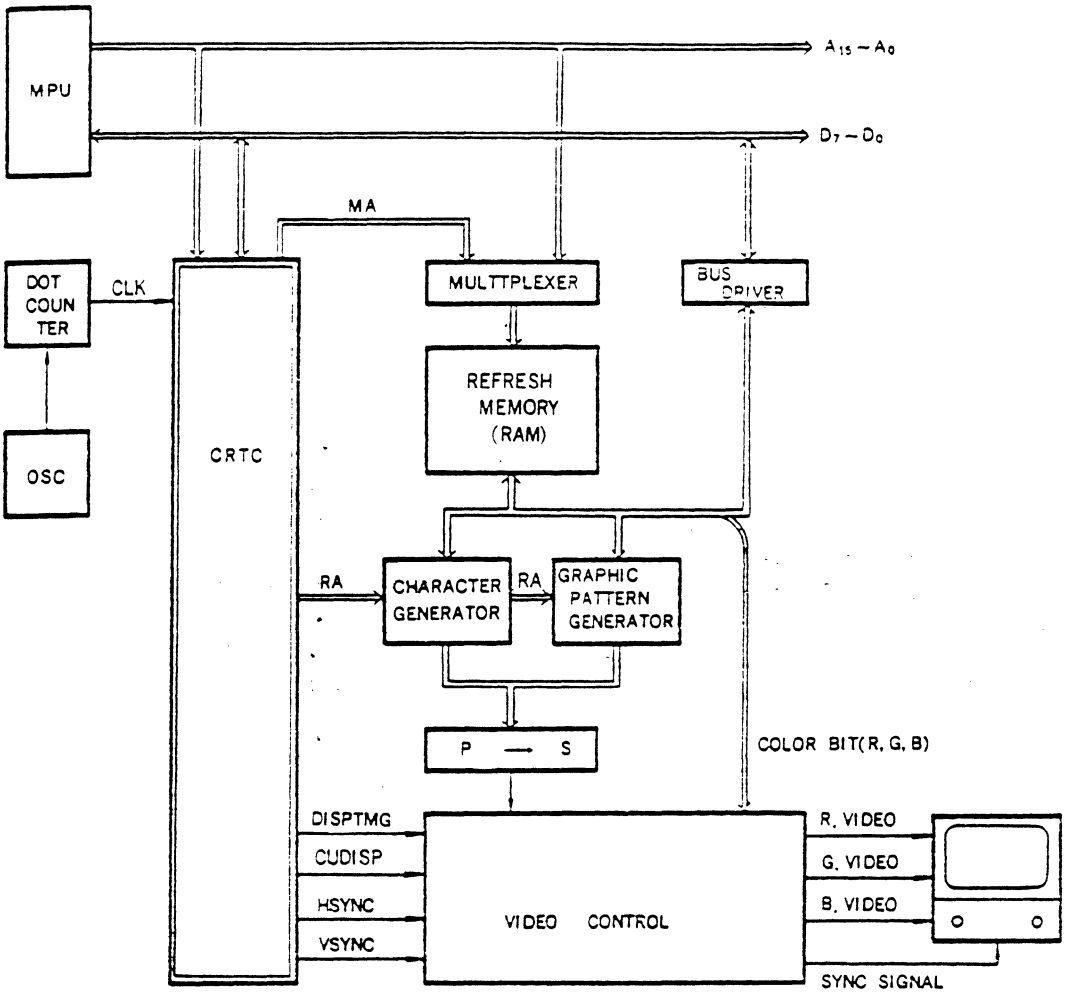


Fig. 11—3 Color Limited Graphic Display

11.4 Monochrome Full Graphic Display

Fig.11-4 shows a system of monochrome full graphic display. While simple graphic display is figure display by combination of picture elements in unit of 1 picture elements, full graphic display is display of any figures in unit of 1 dot. In this case, refresh memory is dot memory that stores all the dot patterns, so its output is directly provided to parallel-serial converter to be displayed. Dot memory address to refresh the screen is set up by combination of MA output and RA output of CRTC.

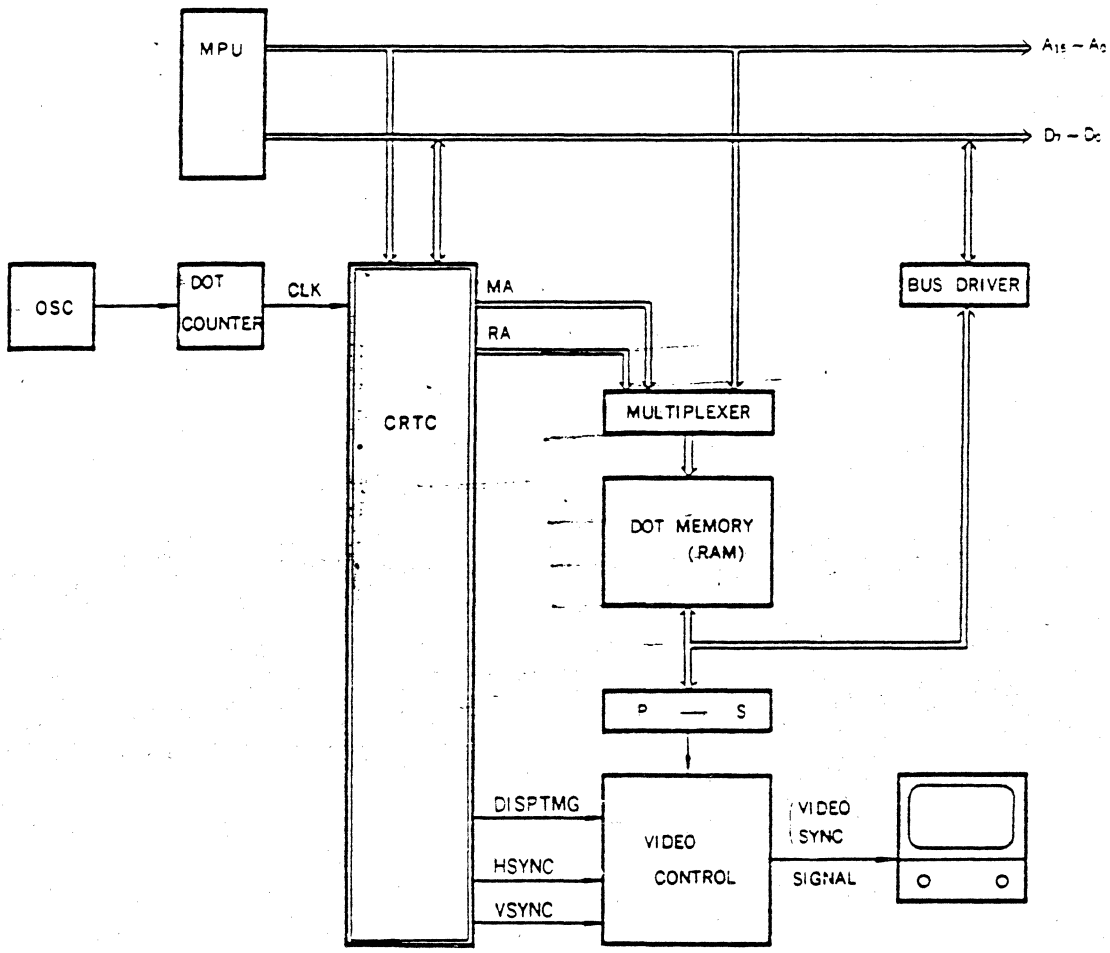


Fig. 11—4 Monochrome Full Graphic Display

Fig.11-5 shows an example of access to refresh memory by combination of MA output and RA output. Fig.11-5 shows a refresh memory address method for full graphic display which has specification shown in Table.10-3. In this case, the values shown in Table.10-4 are initially programmed to CRTC internal registers. Correspondence between dot on the CRT screen and refresh memory address is shown in Fig.11-6.

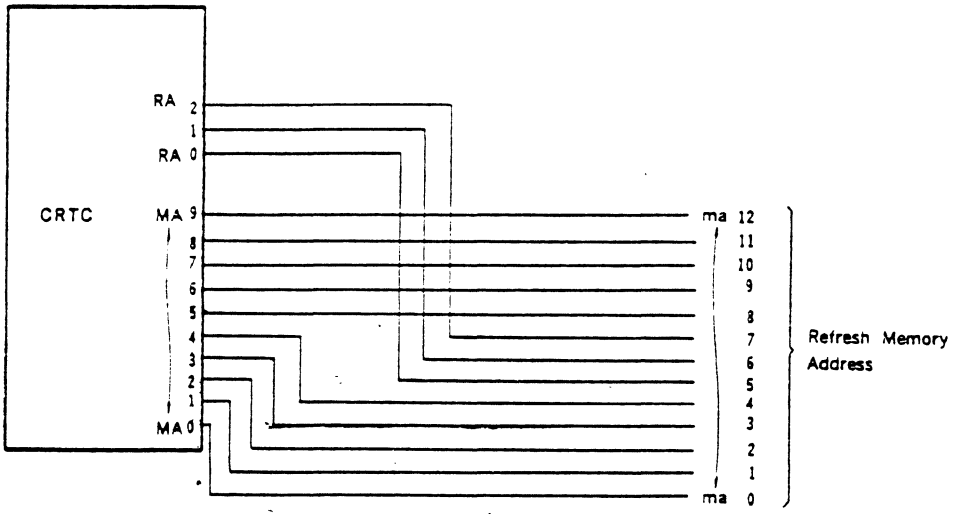


Fig. 11—5 Refresh Memory Address Method for Full Graphic Display

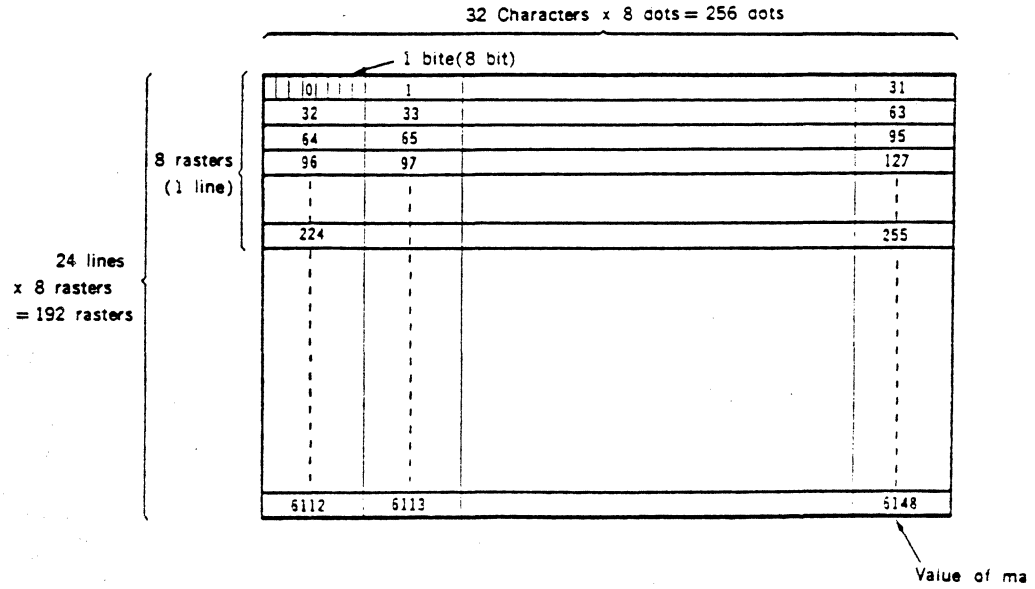


Fig. 11—6 Memory Address and Dot Display position on the Screen for Full Graphic Display

11.5 Color Full Graphic Display

Fig.11-7 shows a system of color full graphic display by 7-color display. Refresh memory is composed of three dot memories which are respectively used for red, green, and blue. These dot memories are read out in parallel at one time and their output is provided to three parallel-serial converters. Then video control circuit adds the blanking control to output of these converters and provids it to CRT display device as red, green, and blue video signals with sync signals.

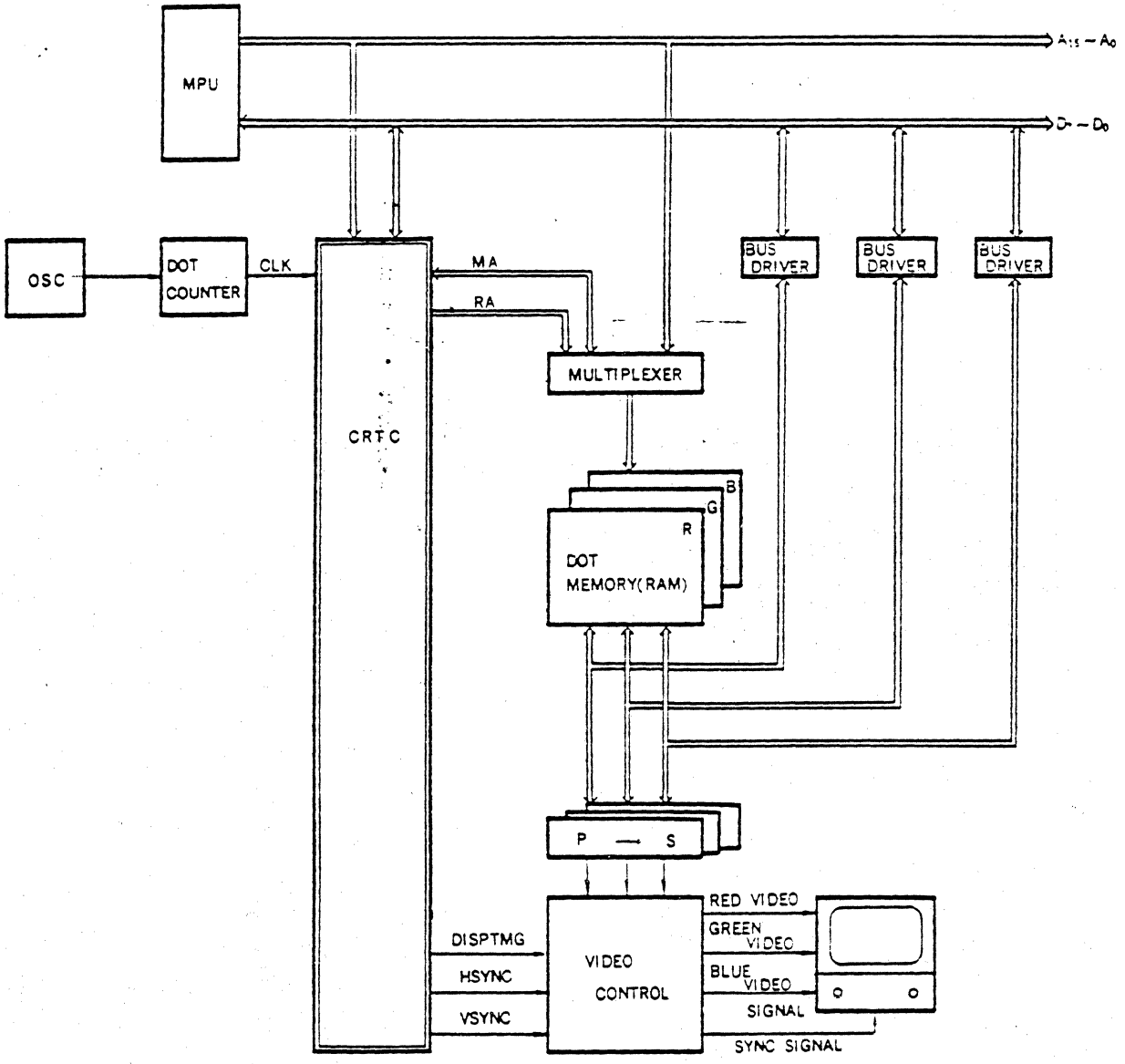


Fig. 11—7 Color Full Graphic Display

11.6 Cluster Control of CRT Display

The CRTC enables cluster control that is to control CRT display of plural devices by one CRTC. Fig.11-8 shows a system of cluster control. Each display control unit has refresh memory, character generator, parallel-serial converter, and video control circuit separately, but these are controlled together by the CRTC.

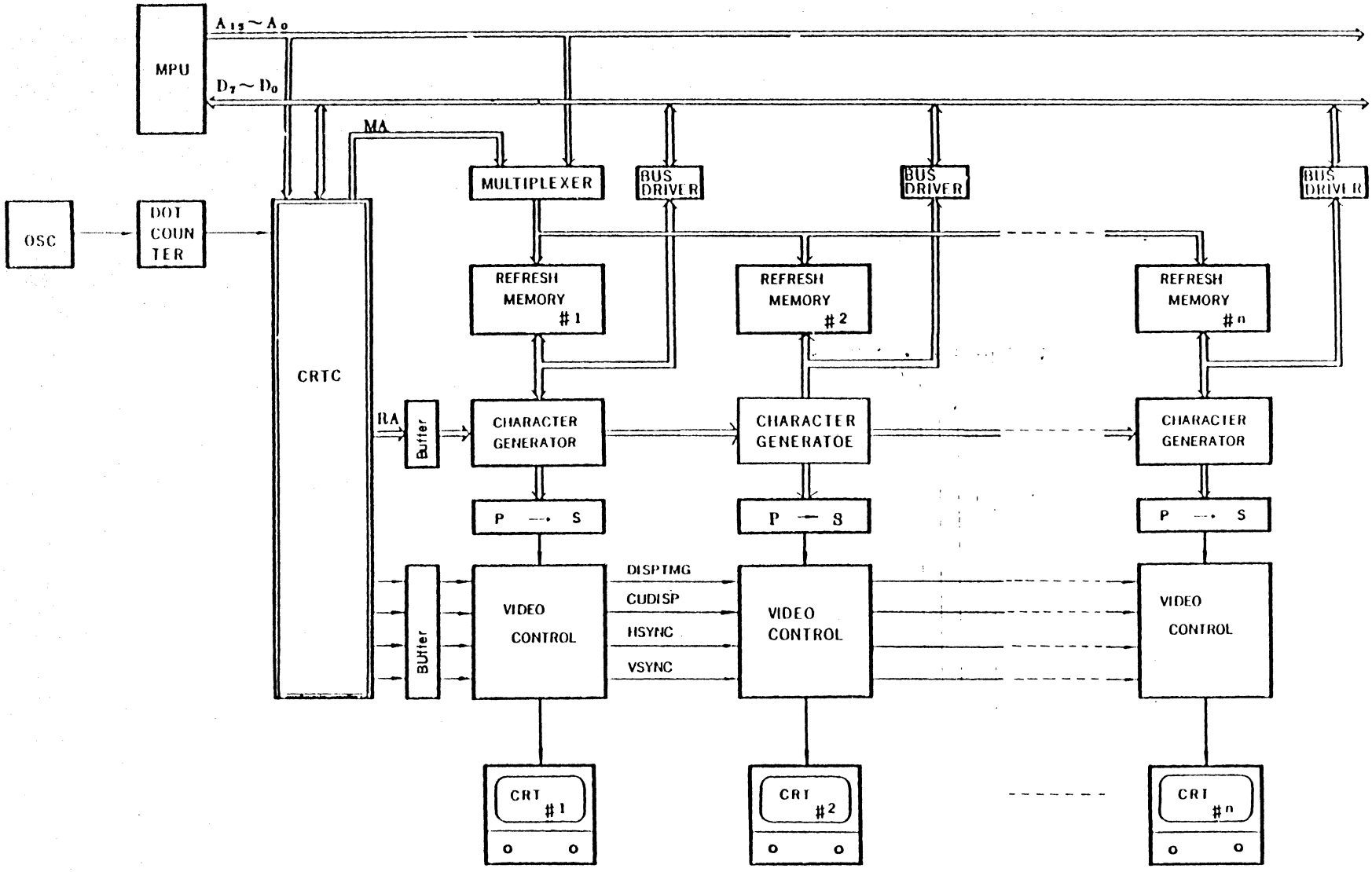


Fig. 11--8 Cluster Control by the CRTC

In this system it is possible for plural CRT display devices to have their own display separately

12. Examples of Applied Circuit of the CRTC

12.1 Monochrome Character Display

Fig.12-1 shows an example of application of the CRTC to monochrome character display. Its specification is shown in Table.12-1. Moreover, specification of CRT display unit is shown in Table.10-1 and initializing values for the CRTC are shown in Table.10-2.

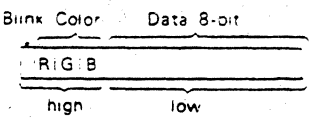
Table. 12-1 Specification of Example 1 of Applied Circuit

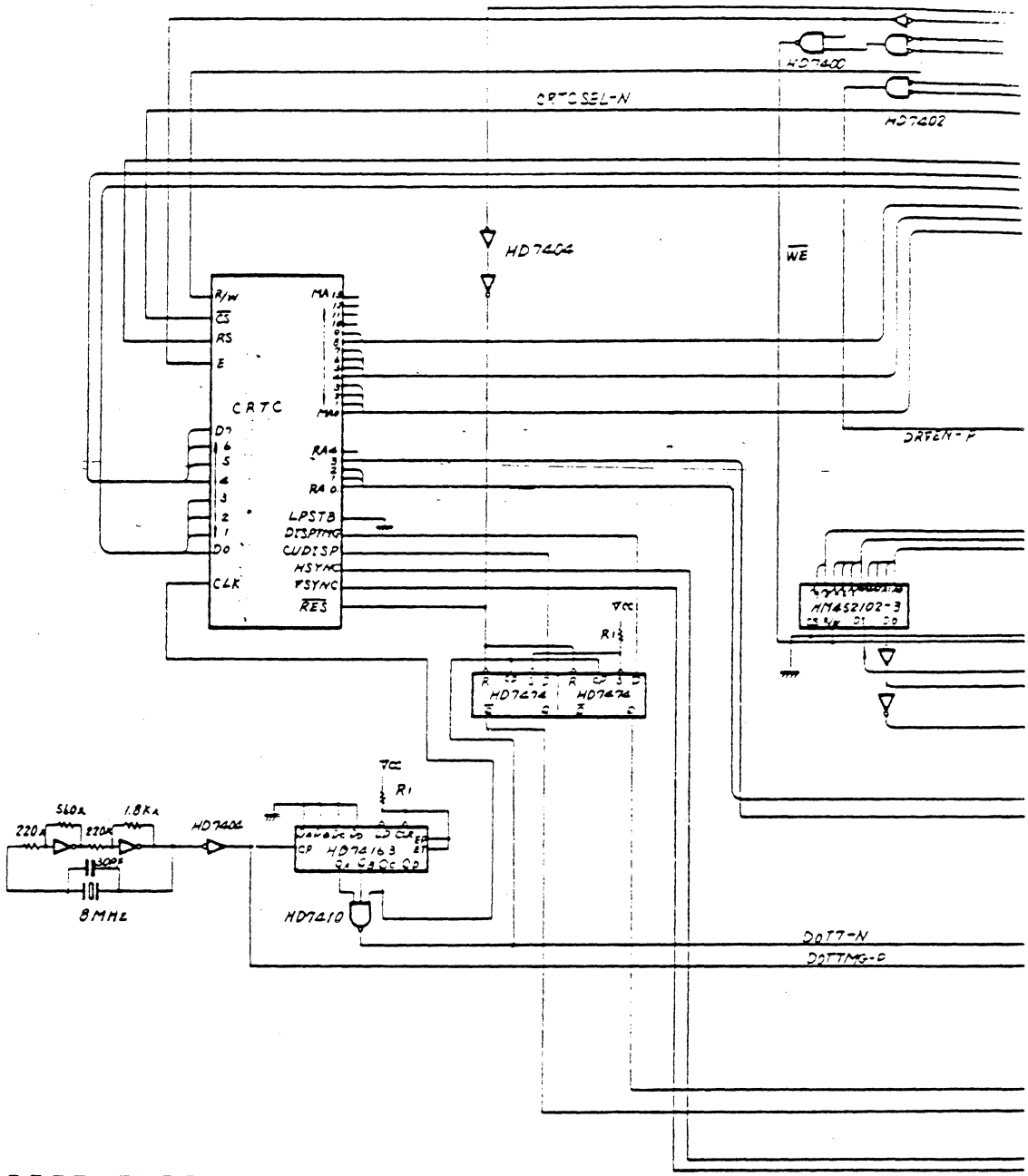
Item	Specification
Character Format	5 x 7 Dot
Character Space	Horizontal:3 Dot Vertical:5 Dot
One Character Time	1 μS
Number of Displayed Characters	40 characters x 16 lines =640 characters
Access Method to Refresh Memory	Asynchronous Method
Refresh Memory	1 kB
Address Map	AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0 Refresh Memory 0 0 0 0 0 0 * * * * * * * * * * CRTC Address Register 0 0 0 1 0 0 x x x x x x x x x 0 CRTC Control Register 0 0 0 1 0 0 x x x x x x x x x 1 x···don't care, *···0 or 1
Synchronization Method	HVSYNC Method

12.2 Color Character Display

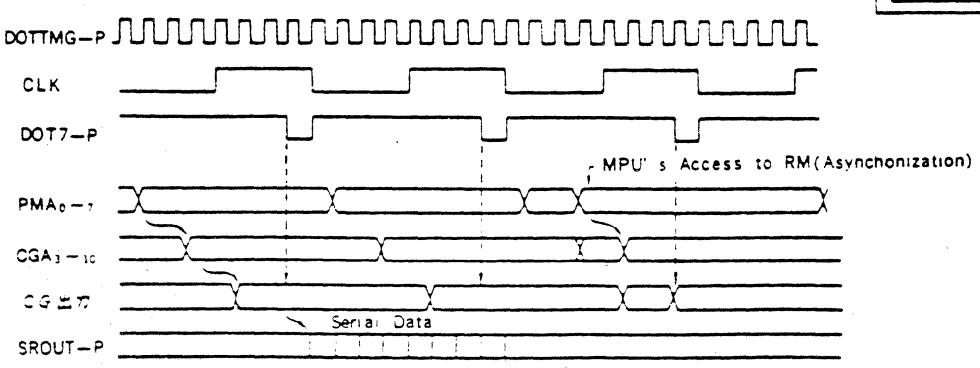
Fig.12-2 shows an example of application of the CRTC to color character display. Its specification is shown in Table.12-2. Moreover, CRT for color display shall be used and its specification is shown in Table.10-1. Initializing values for the CRTC are shown in Table.10-2.

Table. 12-2 Specification of Example 2 of Applied Circuit

Item	Specification
Character Format	5 x 7 Dot
Character Space	Horizontal:3 Dot Vertical:5 Dot
Number of Displayed Characters	40 characters x 16 lines = 640 characters(seven color)
One Character Time	1 μS
Access Method to Refresh Memory	Synchronous Method (Time Division) 
Refresh Memory	2 kW(for 2 pages) Structure of One Word 
Address Map	AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0 Refresh Memory L 0 0 0 0 x * * * * * * * * * * Refresh Memory H 0 0 0 1 x * * * * * * * * * * CRTC Address Register 0 0 1 0 x x x x x x x x x x 0 CRTC Control Register 0 0 1 0 x x x x x x x x x x 1 x···don't care *···0 or 1
Cursor	Displayed in Green
Blink of A Displayed Character	Higher Blink Bits of Refresh Memory: 0:Normal Character Display(Non-Blink) 1:Blink(16 Field Period)
Synchronization Method	HVSYNC Method


HD7400
CRTCSEL-N
HD7402
HD7404
WE
R/W
CS
RS
E
CRTC
D7
6
5
4
3
2
1
D0
CLK
MA
MA0
RA4
RA3
RA0
LPSTB
DISPTMG
CUDISP
HSYNC
VSYNC
RES
DRTEN-P
HM4S2102-3
Vcc
R1
HD7474
HD7474
220Ω
560Ω
1.8KΩ
820Ω
300Ω
8MHz
HD7404
HD74163
HD7410
DOT7-N
DOTTMG-P

Time Chart


DOTTMG—P
CLK
DOT7—P
MPU's Access to RM(Asynchonization)
PMA0—7
CGA3—10
CG ﾃﾞｰﾀ
Serial Data
SROUT—P

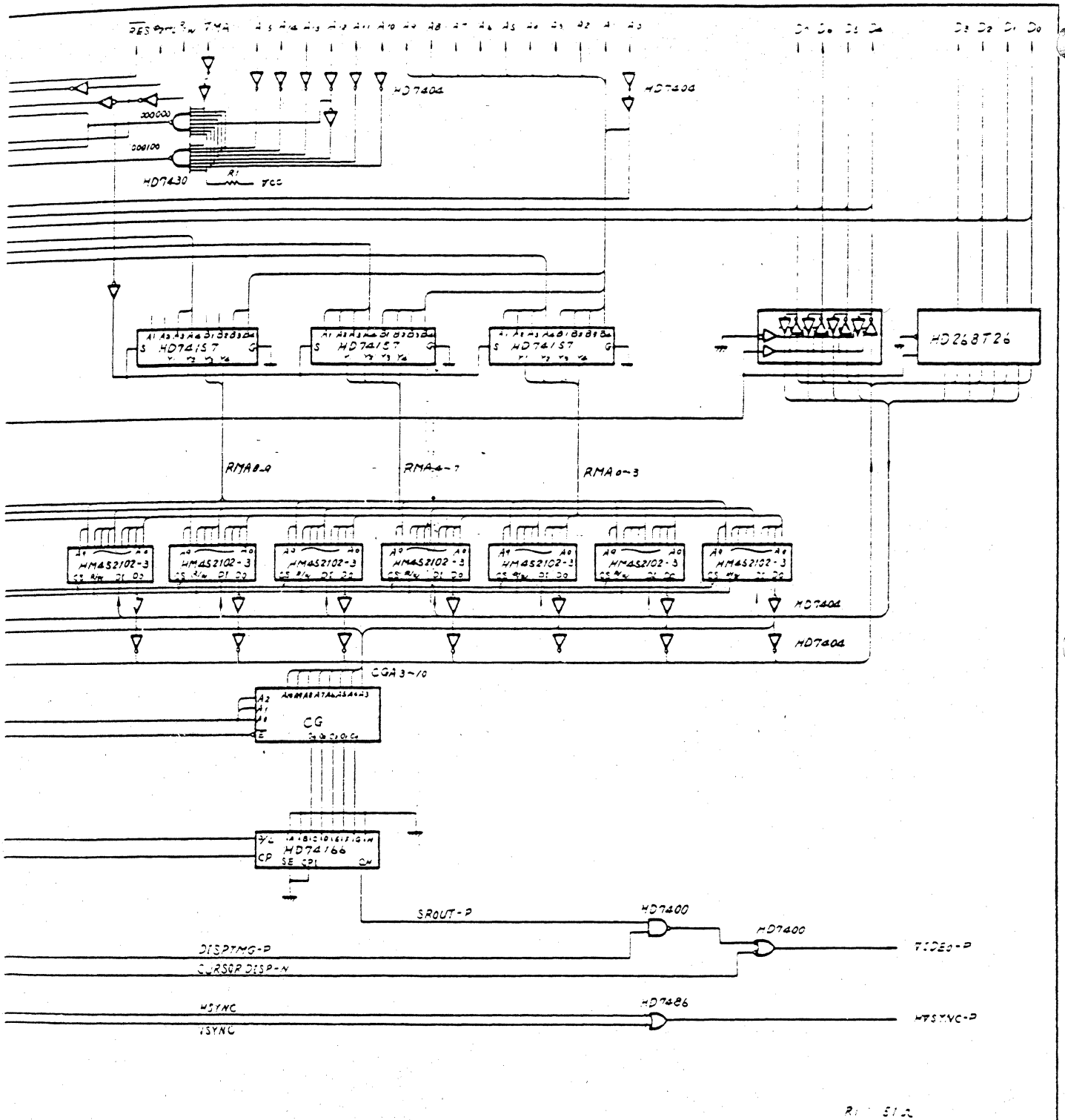
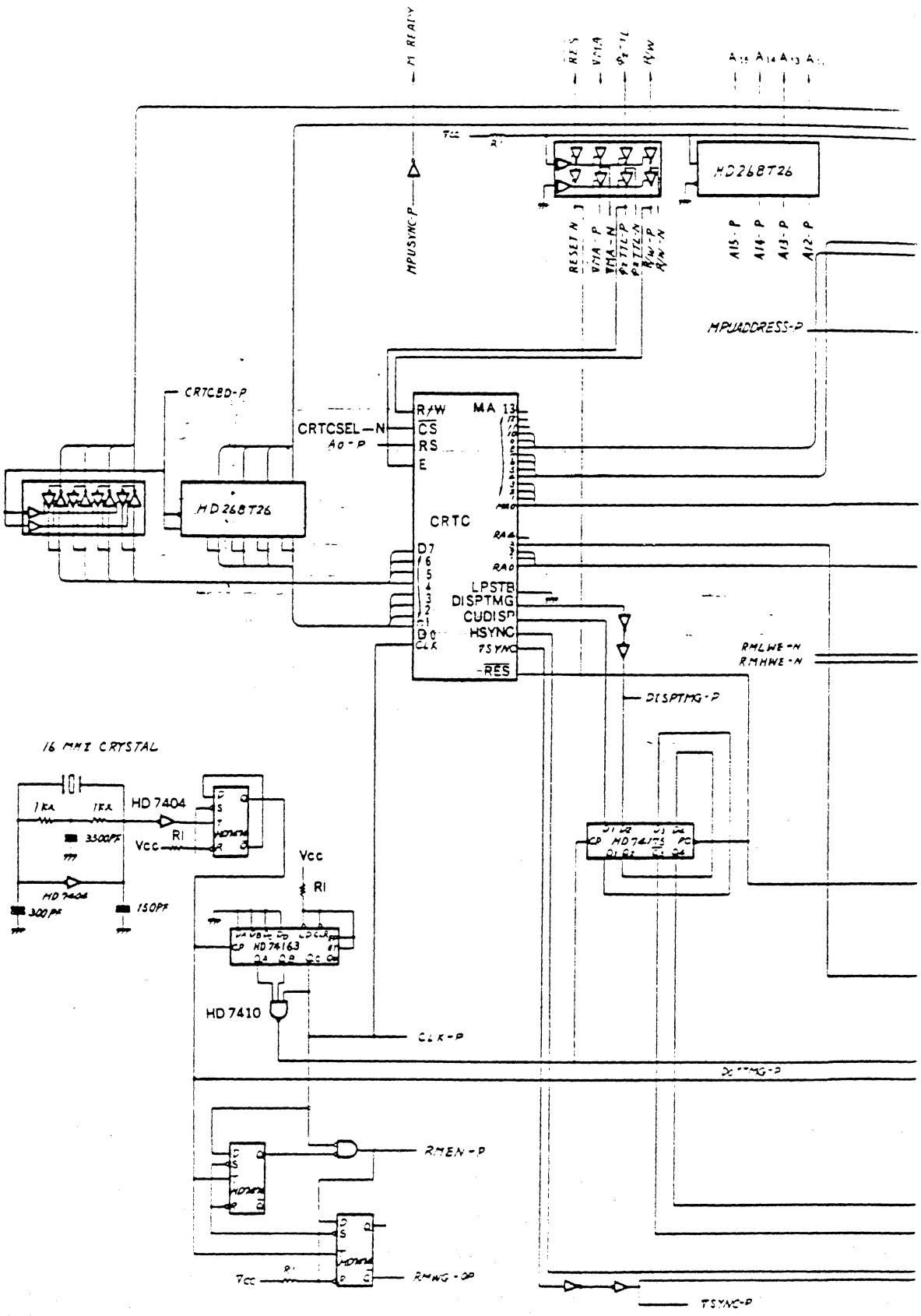


Fig. 12—1 Example of Applied Circuit of the CRTC (Monochrome Character Display)


MPUSYNC-P
HD26BT26
MPUADDRESS-P
CRTCBD-P
CRTCSEL-N
A0-P
R/W
CS
RS
E
MA 13
CRTC
D7
6
5
4
3
2
1
D0
CLK
RA4
RA0
LPSTB
DISPTMG
CUDISP
HSYNC
TSYNC
-RES
RMLWE-N
RMHWE-N
DISPTMG-P
16 MHz CRYSTAL
1KΩ
1KΩ
HD 7404
3300PF
Vcc
RI
150PF
HD 74163
HD 7410
CLK-P
RMEN-P
RMWG-P
TSYNC-P

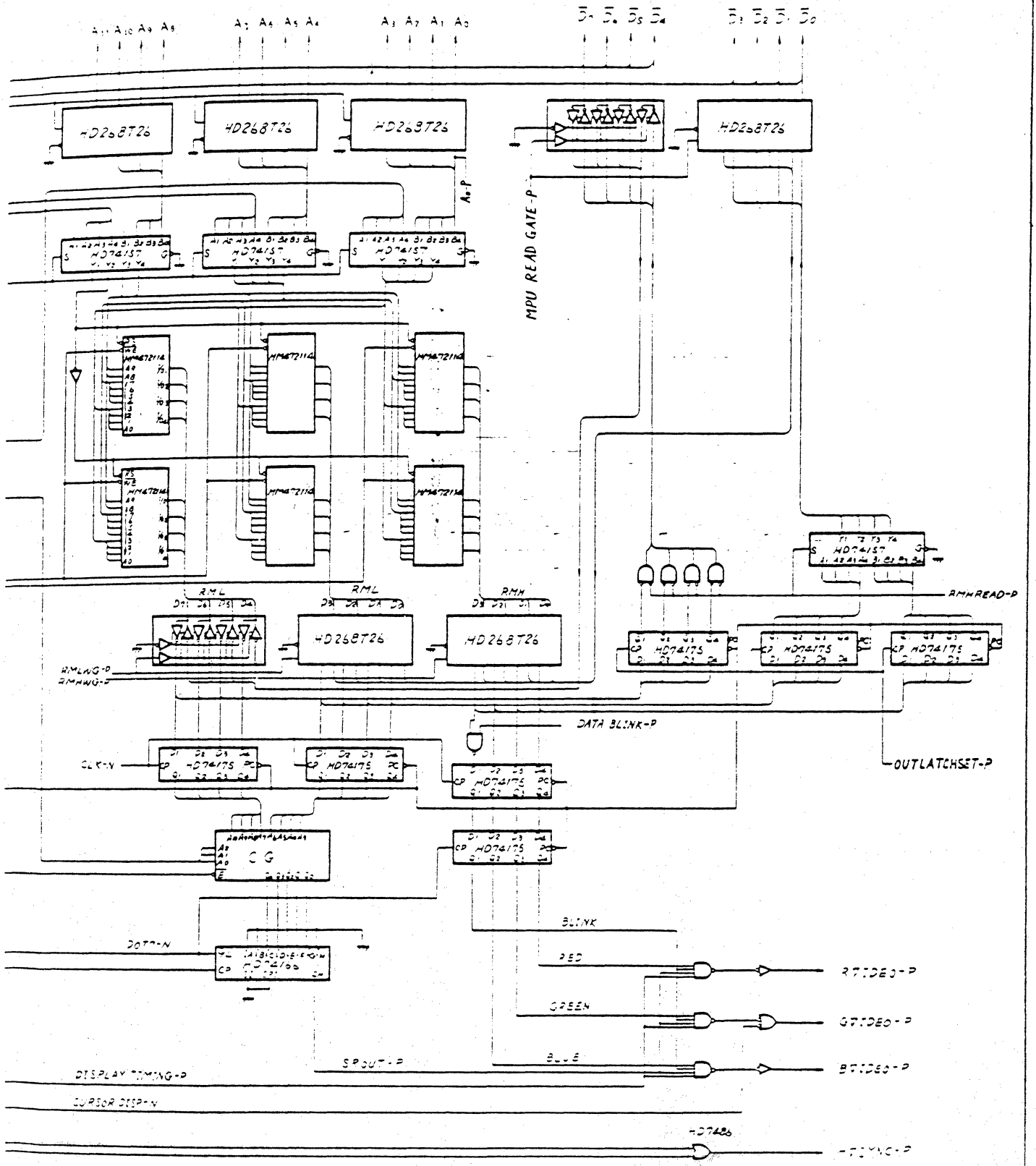
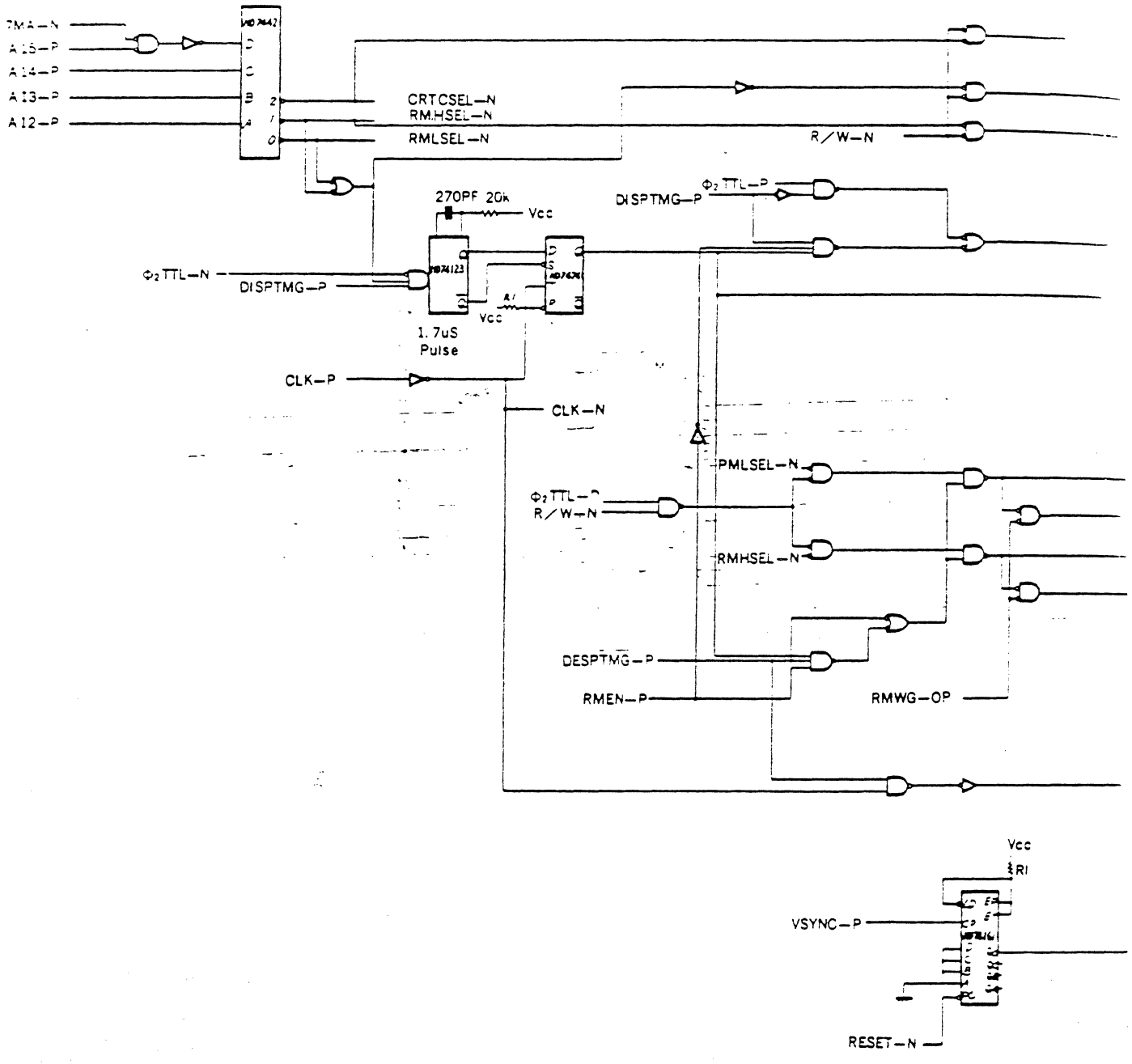


Fig. 12—2(1) Example of Applied Circuit of the CRTC Color Character Display


TMA—N
A15—P
A14—P
A13—P
A12—P
CRTCSEL—N
RMHSEL—N
RMLSEL—N
R/W—N
270PF 20k
Vcc
DISPTMG—P
Φ2 TTL—P
Φ2 TTL—N
DISPTMG—P
1.7uS
Pulse
CLK—P
CLK—N
PMLSEL—N
Φ2 TTL—P
R/W—N
RMHSEL—N
DESPTMG—P
RMEN—P
RMWG—OP
Vcc
VSYNC—P
RESET—N

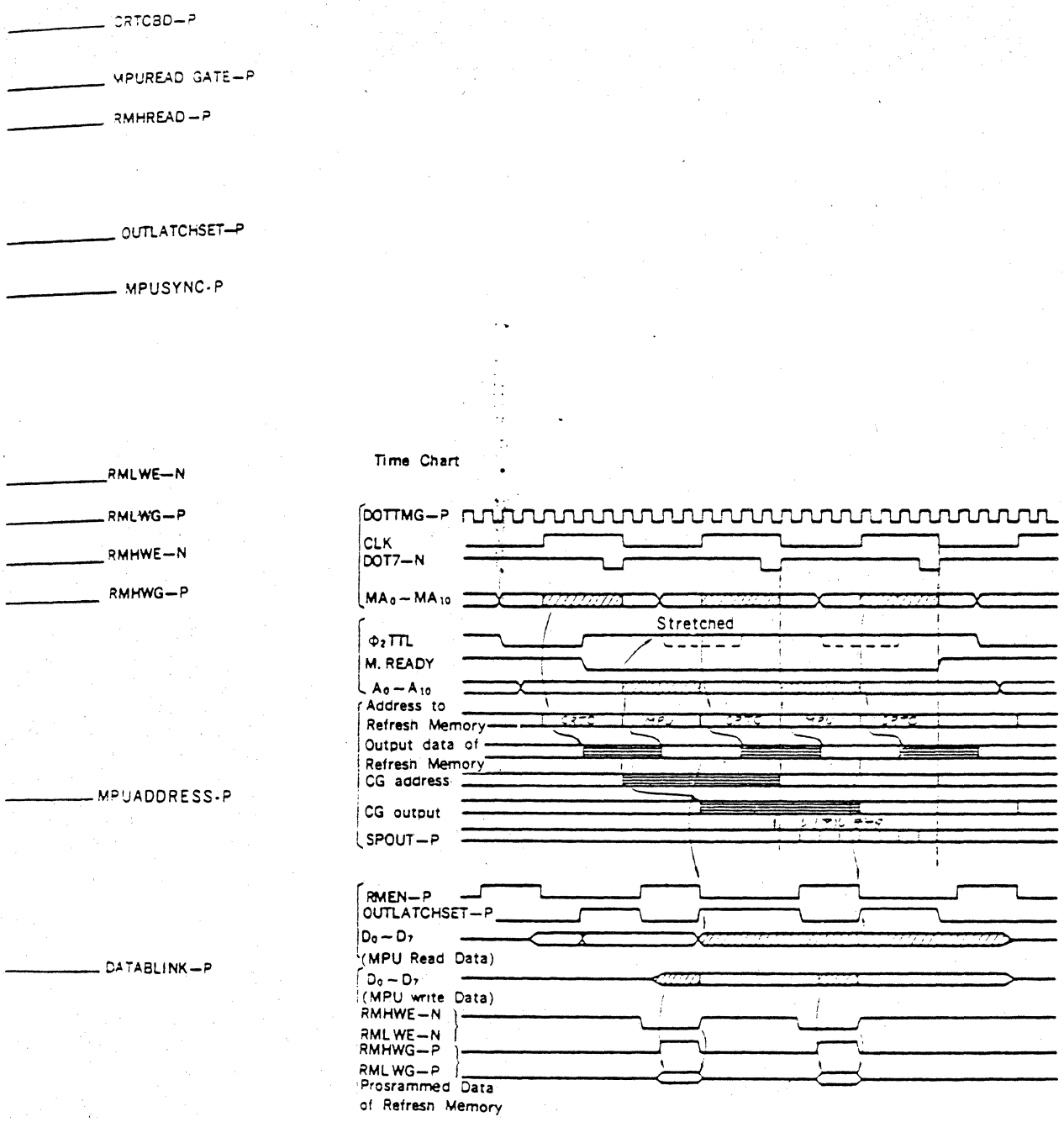


Fig. 12—2(2) Example of Applied Circuit of the CRTC (Color Character Display) 2/2

APPENDIX

Internal Registers of the CRTC

Register No	Name	Hexadecimal Programmed Values of AR	Data Bit 7 6 5 4 3 2 1 0	Range of Programmed Values
AR	Address Register	—		0～17
R_0	Horizontal Total	00		0～255
R_1	Horizontal Displayed	01		0～255 *
R_2	Horizontal Sync Position	02		0～255 *
R_3	Horizontal Sync Width	03		0～15
R_4	Vertical Total	04		0～127
R_5	VERTICAL Total Adjust	05		0～31
R_6	Vertical Displayed	06		0～127 *
R_7	Vertical Sync Position	07		0～127 *
R_8	Interlace Mode	08	V S	0～3
R_9	Maximum Raster Address	09		0～31
R_{10}	Cursor Start Raster	0A	B P	0～4 0～31 Bit *
R_{11}	Cursor End Raster	0B		0 31 *
R_{12}	Start Address (H)	0C		0～
R_{13}	Start Address (L)	0D		16383
R_{14}	Cursor (H)	0E		0～
R_{15}	Cursor (L)	0F		16383
R_{16}	Light Pen (H)	10		
R_{17}	Light Pen (L)	11		

* These values shall be programmed according to restriction shown in next page.

Interlace Mode

V	S	Mode
0	0	Non-Interlace Mode
1	0	
0	1	Interlace Sync Mode
1	1	Interlace Sync & Video Mode

Cursor Display

B	P	Display Mode
0	0	Non-Blink
0	1	Non-Display
1	0	Blink, 16 Field Period
1	1	Blink, 32 Field Period

Restriction On Programmed Values of the CRTC

Programmed values of the CRTC internal registers shall be restricted like the the followings:

i) $0 < N_{hd} < N_{ht} - 1 \leq 256$

ii) N_{ht} : Odd Number (in the case of interlace sync mode or interlace sync & video mode)

iii) $0 < N_{vd} < N_{vt} - 1 \leq 128$

iv) $N_{hsp} + N_{hsw} < N_{ht} - 1$

v) $N_{vsp} \leq N_{vt}$

vi) $0 \leq N_{CSTART} \leq N_{CEND} \leq N_r$

vii) In the case of interlace sync & video mode, either of the followings shall be selected.

(1) N_{CSTART}, N_{CEND} : Even Number

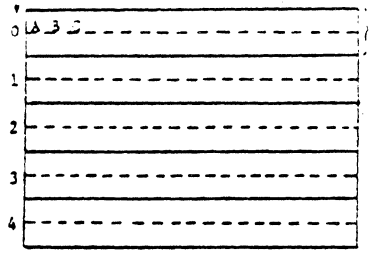
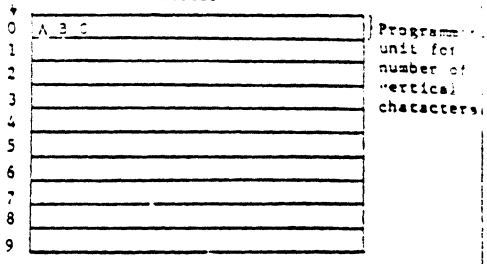
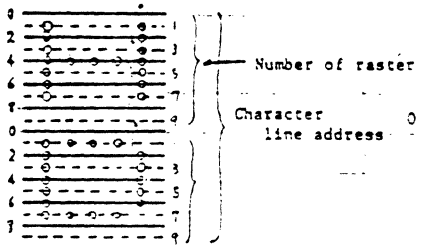
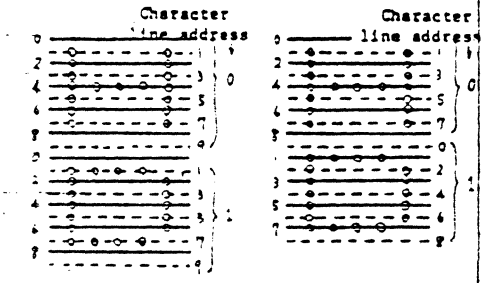
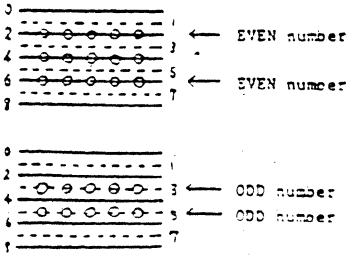
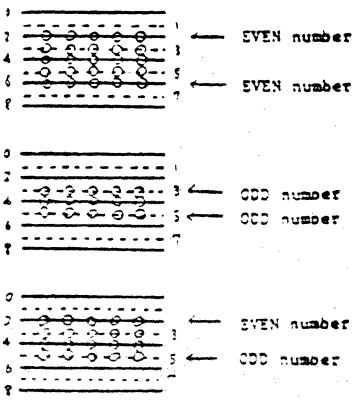
(2) N_{CSTART}, N_{CEND} : Odd Number

Meaning of Symbols in i) ~ vii)

Programmed Values of Registers

- N_{ht} : (Number of Horizontal Total Characters) − 1
- N_{hd} : Number of Horizontal Displayed Characters
- N_{vt} : Number of Vertical Total Characters) − 1
- N_{vd} : Number of Vertical Displayed Characters
- N_{hsp} : (Horizontal Sync Position) − 1
- N_{vsp} : (Vertical Sync Position) − 1
- N_{CSTART} : Cursor Start Raster Address
- N_{CEND} : Cursor End Raster Address
- N_r : Maximum Raster Address

Table of Functional Differences between HD46505R and HD46505S

No.	Functional Difference		HD46505R	HD46505S
1	Interlace Sync & Video Mode Display	Programming Method of number of vertical character	Character line address  In HD46505R, number of characters is vertically programmed in unit of two lines, as illustrated above. (Number of vertical total characters, Number of vertical displayed characters, Vertical Sync Position) Example of above figure Programmed number into Vertical Displayed Register = 5	Character line address  In HD46505S, number of characters is vertically programmed in unit of one line, as illustrated above. (Number of vertical total characters, Number of vertical displayed characters, Vertical Sync Position) Example of above figure Programmed number into Vertical Displayed Register = 10
		Number of raster per character line	Only even-number can be specified.  Number of raster = 10 scanline (specified) However, number which is programmed into register is caluculated as follows. Programmed number (Nr) = (Number specified) - 1	Both even number and odd number can be specified.  When number of raster per character line is EVEN. Number of raster = 10 scan line (specified) When number of raster per character line is ODD. Number of raster = 9 scan line (specified) However, number which is programmed into register is caluculated as follows. Programmed number (Nr) = (Number specified) - 2
		Cursor Display	Cursor is displayed in either EVEN field or ODD field.  	Cursor is displayed in both EVEN field and ODD field. 

Continued

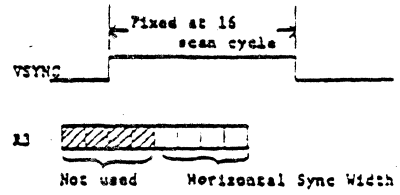
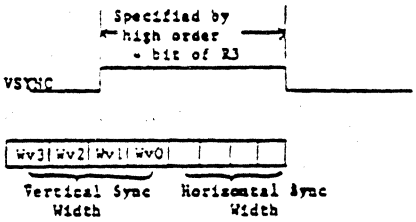
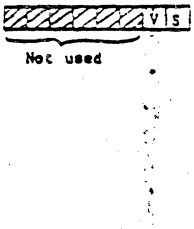
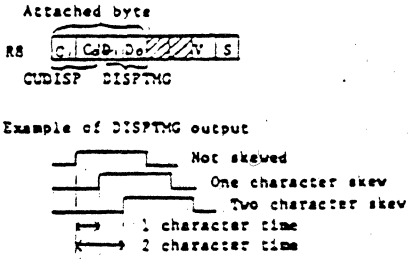
No.	Functional Differen	HD46505R	HD46505S
2	Vertical Sync Pulse Width (VSYNC output)	Fixed at 16 raster scan cycle (16H) 	Programmable (1 - 16 raster scan cycle) 
3	SKEW Function	Not included 	SKEW function is newly included in DISPTMG, CUDISP signals. 
4	Start Address Register	Impossible to READ	Possible to READ
5	RESET Signal ($\overline{RES}$)	$MA_0 \sim MA_{13}$ Output, $RA_0 \sim RA_4$ Output ---Synchronous reset Other Outputs ------Asynchronous reset Output signals of $MA_0 \sim MA_{13}$, $RA_0 \sim RA_4$, synchronizing with DLK "LOW" level, go to "LOW" level, after $\overline{RES}$ has gone to "LOW". Other outputs go to "LOW" immediately after $\overline{RES}$ has gone to "LOW" level.	$MA_0 \sim MA_{13}$ Output, $RA_0 \sim RA_4$ Output, Other Outputs ---Asynchronous reset Output signals of $MA_0 \sim MA_{13}$, $RA_0 \sim RA_4$ and others go to "LOW" level immediately after $\overline{RES}$ has gone to "LOW" level.

Table of Characteristic Difference between HD46505R and HD46505S

No.	Characteristic Difference	Symbol	HD46505R min	HD46505R typ	HD46505R max	HD46505S min	HD46505S typ	HD46505S max	Unit
1	Clock Cycle Time	t_{CYCC}	330	—	—	270	—	—	ns
2	Clock Pulse Width "High"	PW_{CH}	150	—	—	130	—	—	ns
3	Clock Pulse Width "Low"	PW_{CL}	150	—	—	130	—	—	ns
4	Rise and Fall Time for Clock Input	t_{CR}, t_{CF}	—	—	15	—	—	20	ns
5	Horizontal Sync Delay Time	T_{HSD}	—	—	250	—	—	200	ns
6	Light Pen Strobe Pulse Width	PW_{LPH}	80	—	—	60	—	—	ns
7	Light Pen Strobe Uncertain Time of Acceptance	T_{LPD1}	—	—	80	—	—	70	ns
		T_{LPD2}	—	—	10	—	—	0	ns