1997

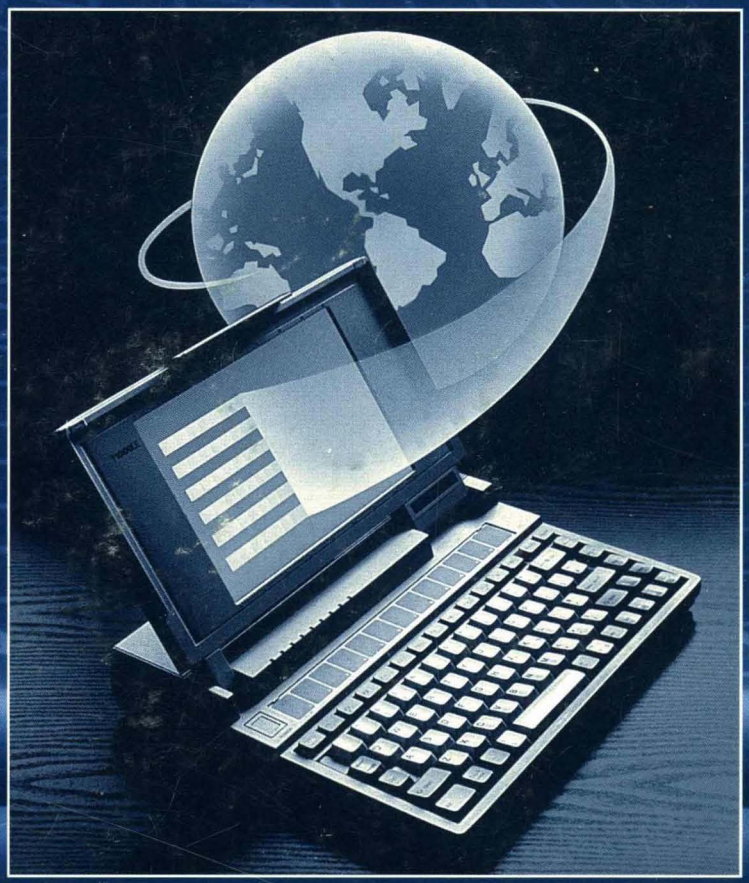
COMMUNICATIONS DATA BOOK

HARRIS

DB
317

Wireless and Wired Communications Products

COMMUNICATIONS DATA BOOK 1997



HARRIS
SEMICONDUCTOR

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HARRIS SEMICONDUCTOR

TECHNICAL ASSISTANCE

Harris Marketing Support Services (HMSS)

HMSS provides world-class service to customers requiring information on all products offered by Harris Semiconductor. Ask Harris Marketing Support Services for answers concerning:

- Product Identification
- Availability
- Competitive and Obsolete Cross-Reference
- Distributor Stocking Levels
- Requests for Literature and Samples

HMSS services are available from 8:00am to 8:00pm EST. Within the United States, call 1-800-4HARRIS. Callers from outside the United States, dial (407) 727-9207.

HMSS is the initial contact for customers who need technical assistance with the selection and use of our products. Callers have the option to be connected directly to the Central Applications Group.

Central Applications

Ask our experienced staff of engineers for assistance with:

- Device Selection
- Specification Interpretation
- Applications for Any Harris Product

Central Applications serves you Monday through Thursday 8:00am to 7:00pm and Friday 8:00am to 5:00pm EST. Within the United States, call 1-800-4HARRIS. Callers from outside the United States dial (407) 727-9207.

Central Applications' knowledge of our portfolio can provide you with a total system design solution using the latest Harris devices!

Electronic Technical Support

Electronic services from Harris Semiconductor offer you the most current information possible.

http://www.semi.harris.com

- Latest Literature Revisions
- New Product Listing
- Product Information
- Design Support
- Contact Information

HARRIS SEMICONDUCTOR

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(407) 724-7800

- Latest Literature Revisions
- New Product Listing
- Data Book Request Form

CENTRAL APPLICATIONS EMAIL

centapp@harris.com, or 1-800-4HARRIS

- Technical Application Assistance

See our specs in CAPS

Printed in USA, 1/1997

HARRIS COMMUNICATIONS PRODUCTS

As one millennium comes to a close and a new one approaches, a revolution is upon us. The telecommunications industry is experiencing rapid social and regulatory change throughout the world. Fueled by advancing technology, the upsurge of change is gaining momentum. Consumers now have access to technology that less than a decade ago only the military could afford. From Internet access to personal communications systems, consumers are demanding higher data rates and more bandwidth at lower costs. To address these needs Harris Semiconductor is developing highly integrated chip set solutions targeted for the communications market.

This book is organized to help the reader quickly find solutions for their particular needs and applications. Section 1 contains a listing of new products and Section 2 contains the table of contents and general information. Section 3 is dedicated to wireless communications products. In Section 3, you will find highly integrated solutions for applications such as wireless LAN and wireless local loop systems. Section 4 is dedicated to wired communications products. Here you will find integrated solutions for applications such as ISDN modems, cable telephony, wireless local loop, PABX, and key telephone systems.

Section 5, our Standard Products Section, contains a broad range of communications products including Data Acquisition, Digital Signal Processing, Linear and Power Products. The breadth of this product line is so large only the first page of each data sheet is included in this section. Complete data sheets for Standard Products can be obtained from our Internet web site, **http://www.harris.com/**, AnswerFax, the Harris Fulfillment Center, or your local sales office or authorized distributor. (See Section 10).

Section 6 contains a listing of Development Tools including SPICE models, evaluation boards, macromodels, etc. Complete information about these tools is available from any of the above referenced sources. Section 7 is our application note section where we have reprinted in full a selection of our more popular application notes and tech briefs.

Section 8 contains information about Harris' world class Quality and Reliability Program. Section 9 is where you will find packaging information on the products contained herein. Section 10 contains information on how to use Harris' on-line services to obtain data sheets and application notes. And last but not least, Section 11 contains a listing of our world wide sales offices.

For complete, current and detailed technical specifications on any Harris devices, please contact the nearest Harris sales, representative or distributor office, listed in Section 11; or direct literature requests to:

Harris Semiconductor Data Services Department
P.O. Box 883, MS 53-204
Melbourne, FL 32902
Phone: 1-800-442-7747
Fax: 407-724-7240

This catalog is an invaluable reference for engineers and technicians in the communications field. Please contact your local sales office listed in Section 11 for further assistance.

For a complete listing of all Harris Semiconductor products, please refer to the Product Selection Guide (PSG201; ordering information above).

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

HARRIS SEMICONDUCTOR

COMMUNICATIONS

FOR COMMERCIAL APPLICATIONS

COMMUNICATIONS 1

NEW PRODUCTS

PART NUMBER	DESCRIPTION	AnswerFAX℠ DOCUMENT NO.
WIRELESS, Section 3		
PRISM™ Full Duplex Radio Front End Chip Set	For Voice and Data	4238
WIRED, Section 4		
HC5515	SLIC Subscriber Line Interface Circuit	4235
HC5519	SLIC Subscriber Line Interface Circuit	4232
HC5520	SLIC Subscriber Line Interface Circuit	4148
HC5523	SLIC Subscriber Line Interface Circuit	4144
HC5526	SLIC Subscriber Line Interface Circuit	4151
DATA ACQUISITION, Section 5		
HI5805	12-Bit, 5 MSPS A/D Converter	3984
HI5808	12-Bit, 10 MSPS A/D Converter	4233
HI5731	12-Bit, 100 MSPS High Speed D/A Converter	4070
HI5741	14-Bit, 100 MSPS High Speed D/A Converter	4071
DIGITAL SIGNAL PROCESSING, Section 5		
HSP50110	Digital Quadrature Tuner	3651
HSP50210	Digital Costas Loop	3652
HSP50214	Programmable Downconverter	4266
HSP50215 (Note)	Digital Up Converter	
HSP50306	Digital QPSK Demodulator	4162
HSP50307	Burst QPSK Modulator	4219

NOTE: Coming soon.

COMMUNICATIONS 2

TABLE OF CONTENTS AND GENERAL INFORMATION

Alpha Numeric Product Index

Alpha Numeric Product Index (Continued)

Alpha Numeric Product Index (Continued)

Alpha Numeric Product Index (Continued)

Alpha Numeric Product Index (Continued)

PRISM™ and LittleFET™ are trademarks of Harris Corporation.

Product Index by Family

Product Index by Family (Continued)

Product Index by Family (Continued)

WIRED COMMUNICATIONS

Product Index by Family (Continued)

WIRELESS COMMUNICATIONS

Communications Cross-Reference Guide

COMPETITOR PART NUMBER	COMPETITOR NAME	HARRIS PART NUMBER	(NOTE) CROSS TYPE	COMMENTS
KT8592N	SAMSUNG	CD22100E	P	
SSI22100CP	SILICON SYSTEMS	CD22100E	P	
SSI22100IP	SILICON SYSTEMS	CD22100E	P	
SSI22100MD	SILICON SYSTEMS	CD22100E	P	
KT8592N	SAMSUNG	CD22100F	P	
SSI22100CP	SILICON SYSTEMS	CD22100F	P	
SSI22100IP	SILICON SYSTEMS	CD22100F	P	
SSI22100MD	SILICON SYSTEMS	CD22100F	P	
SSI22101IP	SILICON SYSTEMS	CD22101E	D	
SSI22101CP	SILICON SYSTEMS	CD22101E	P	
SSI22101MD	SILICON SYSTEMS	CD22101E	P	
SSI22101MD	SILICON SYSTEMS	CD22101F	D	
SSI22101CP	SILICON SYSTEMS	CD22101F	P	
SSI22101IP	SILICON SYSTEMS	CD22101F	P	
SSI22102IP	SILICON SYSTEMS	CD22102E	D	
SSI22102CP	SILICON SYSTEMS	CD22102E	P	
SSI22102MD	SILICON SYSTEMS	CD22102E	P	
MT8816AE	MITEL SEMI	CD22M3494E	D	
MT8816AC	MITEL SEMI	CD22M3494E	P	
MT8816AP	MITEL SEMI	CD22M3494MQ	D	
MT8816AP	MITEL SEMI	CD22M3494SQ	D	
SSI22301CP	SILICON SYSTEMS	CD22301E	P	
SSI22301IP	SILICON SYSTEMS	CD22301E	P	
SSI75T204-IP	SILICON SYSTEMS	CD22204E	H	
CXD2306Q	SONY	HI5780JCQ	H	Local Technical Support
CX20201A-1	SONY	HI20201JCB	H	Local Technical Support
CX20201A-2	SONY	HI20201JCB	P	Extra Bit of Resolution
CX20202A-1	SONY	HI20201JCP	H	Local Technical Support

NOTE: D = Direct Replacement, E = Functionally Equivalent Pin-for-Pin Replacement. Electrical specification review required, H = Harris Recommended Replacement, P = Pin-for-Pin Replacement

COMPETITOR PART NUMBER	COMPETITOR NAME	HARRIS PART NUMBER	(NOTE) CROSS TYPE	COMMENTS
CX20202A-2	SONY	HI20201JCP	P	Extra Bit of Resolution
CXD2310AR	SONY	HI5710AJCQ	H	Local Technical Support
CA3046	SGS-THOMSON	CA3045	P	
LM3045J	NATIONAL SEMI	CA3045F	H	
SG3045J	SILICON GENERAL	CA3045F	H	
SL3045C-DG	GEC PLESSEY	CA3045F	H	
CA3046	SGS-THOMSON	CA3045F	P	
SL3145C-DC	GEC PLESSEY	CA3045F	P	Greater Breakdown Voltages
LM3046N	NATIONAL SEMI	CA3046	H	
CA3046	SGS-THOMSON	CA3046	P	
MC3346P	MOTOROLA SEMI	CA3046	P	Full -55°C to 125°C Operation
LM3046D	NATIONAL SEMI	CA3046M	H	
MC3346D	MOTOROLA SEMI	CA3046M	P	Full -55°C to 125°C Operation
SG3083	SILICON GENERAL	CA3083	H	
ULN2083A	SPRAGUE	CA3083	P	Full -55°C to 125°C Operation
ULN2083L	SPRAGUE	CA3083M	P	Full -55°C to 125°C Operation
LM3086N	NATIONAL SEMI	CA3086	H	
CA3046	SGS-THOMSON	CA3086	P	
ULN2086A	SPRAGUE	CA3086	P	Full -55°C to 125°C Operation
LM3086M	NATIONAL SEMI	CA3086M	H	
LM3086J	NATIONAL SEMI	CA3086F	H	
CA3046	SGS-THOMSON	CA3086F	P	
SL3127C-DP	GEC PLESSEY	CA3127E	H	
CA3146P	MOTOROLA SEMI	CA3146E	H	
LM3146N	NATIONAL SEMI	CA3146E	P	Enhanced "A" Version Offered
ULN2046A-1	SPRAGUE	CA3146E	P	Full -40°C to 85°C Operation
ULN2046L-1	SPRAGUE	CA3146M	H	
LM3146M	NATIONAL SEMI	CA3146M	P	Enhanced "A" Version Offered
SG3183N	SILICON GENERAL	CA3183E	P	Identical Specs at 25°C

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COMPETITOR PART NUMBER	COMPETITOR NAME	HARRIS PART NUMBER	(NOTE) CROSS TYPE	COMMENTS
ULN2083A-1	SPRAGUE	CA3183E	P	Full -40°C to 85°C Operation
SG3183D	SILICON GENERAL	CA3183M	P	Identical Specs at 25°C
SL3227-DP	GEC PLESSEY	CA3227E	P	Greater Breakdown Voltages
SL3227/DC	GEC PLESSEY	CA3227E	P	
SL3227/DP	GEC PLESSEY	CA3227E	P	
SL3227NADC	GEC PLESSEY	CA3227E	P	
SL3227NADP	GEC PLESSEY	CA3227E	P	
SL3227-MP	GEC PLESSEY	CA3227M	P	Greater Breakdown Voltages
SL3227/MP	GEC PLESSEY	CA3227M	P	
SL3227NAMP	GEC PLESSEY	CA3227M	P	
SL3227/MP	GEC PLESSEY	CA3227M96	P	
SL3227NAMP	GEC PLESSEY	CA3227M96	P	
SL3245-DP	GEC PLESSEY	CA3246E	P	Programmable Biasing Current
SL3245-MP	GEC PLESSEY	CA3246M	P	Faster Acquisition/Lower Droop
AD9621SQ	ANALOG DEVICES	HFA1100MJ/883	H	Better Specs, VFB vs CFB
AD9622SQ	ANALOG DEVICES	HFA1100MJ/883	H	Better Specs, VFB vs CFB
AD9623SQ	ANALOG DEVICES	HFA1100MJ/883	H	Higher Speed, VFB vs CFB
AD9624SQ	ANALOG DEVICES	HFA1100MJ/883	H	Higher Speed, VFB vs CFB
CLC401A8B	COMLINEAR	HFA1100MJ/883	H	Better Performance
CLC402A8B	COMLINEAR	HFA1100MJ/883	H	Better Performance
CLC404A8B	COMLINEAR	HFA1100MJ/883	H	Better Performance
CLC406A8B	COMLINEAR	HFA1100MJ/883	H	Better Performance
CLC409A8B	COMLINEAR	HFA1100MJ/883	H	Better Performance
EL2171J/883B	ELANTEC	HFA1100MJ/883	H	Better ACs
AD8001AN	ANALOG DEVICES	HFA1100MJ/883	P	
AD8001SMD	ANALOG DEVICES	HFA1100MJ/883	P	
CLC402AID	COMLINEAR	HFA1100MJ/883	P	
CLC402AJP	COMLINEAR	HFA1100MJ/883	P	
CLC402A8D	COMLINEAR	HFA1100MJ/883	P	

NOTE: D = Direct Replacement, E = Functionally Equivalent Pin-for-Pin Replacement. Electrical specification review required, H = Harris Recommended Replacement, P = Pin-for-Pin Replacement

COMPETITOR PART NUMBER	COMPETITOR NAME	HARRIS PART NUMBER	(NOTE) CROSS TYPE	COMMENTS
CLC406AIB	COMLINEAR	HFA1100MJ/883	P	
CLC406AID	COMLINEAR	HFA1100MJ/883	P	
CLC406AJP	COMLINEAR	HFA1100MJ/883	P	
CLC406A8D	COMLINEAR	HFA1100MJ/883	P	
CLC409AID	COMLINEAR	HFA1100MJ/883	P	
CLC409AJP	COMLINEAR	HFA1100MJ/883	P	
CLC409A8D	COMLINEAR	HFA1100MJ/883	P	
CLC446AJP	COMLINEAR	HFA1100MJ/883	P	
CLC446A8B	COMLINEAR	HFA1100MJ/883	P	
CLC446SMD	COMLINEAR	HFA1100MJ/883	P	
CLC449AJP	COMLINEAR	HFA1100MJ/883	P	
CLC449A8B	COMLINEAR	HFA1100MJ/883	P	
CLC449SMD	COMLINEAR	HFA1100MJ/883	P	
OPA648H	BURR-BROWN CORP	HFA1100MJ/883	P	
OPA648P	BURR-BROWN CORP	HFA1100MJ/883	P	
OPA658P	BURR-BROWN CORP	HFA1100MJ/883	P	
OPA658PB	BURR-BROWN CORP	HFA1100MJ/883	P	
5962-9200401MPX	COMLINEAR	HFA1100MJ/883	P	
5962-9203301MPX	COMLINEAR	HFA1100MJ/883	P	
5962-9203401MPX	COMLINEAR	HFA1100MJ/883	P	
5962-9459301MPA	ANALOG DEVICES	HFA1100MJ/883	P	
AD9621AQ	ANALOG DEVICES	HFA1100IJ	H	Better Specs, VFB vs CFB
AD9622AQ	ANALOG DEVICES	HFA1100IJ	H	Better Specs, VFB vs CFB
AD9623AQ	ANALOG DEVICES	HFA1100IJ	H	Higher Speed, VFB vs CFB
AD9624AQ	ANALOG DEVICES	HFA1100IJ	H	Higher Speed, VFB vs CFB
CLC401AIB	COMLINEAR	HFA1100IJ	H	Better Performance
CLC402AIB	COMLINEAR	HFA1100IJ	H	Better Performance
CLC404AIB	COMLINEAR	HFA1100IJ	H	Better Performance
CLC406AIB	COMLINEAR	HFA1100IJ	H	Better Performance

NOTE: D = Direct Replacement, E = Functionally Equivalent Pin-for-Pin Replacement. Electrical specification review required, H = Harris Recommended Replacement, P = Pin-for-Pin Replacement

COMPETITOR PART NUMBER	COMPETITOR NAME	HARRIS PART NUMBER	(NOTE) CROSS TYPE	COMMENTS
CLC409AIB	COMLINEAR	HFA1100IJ	H	Better Performance
OPA644H	BURR-BROWN CORP	HFA1100IJ	H	Better Bandwidth
OPA644HB	BURR-BROWN CORP	HFA1100IJ	H	Better Bandwidth
OPA648H	BURR-BROWN CORP	HFA1100IJ	H	
AD8001AN	ANALOG DEVICES	HFA1100IJ	P	
AD8001SMD	ANALOG DEVICES	HFA1100IJ	P	
CLC402AID	COMLINEAR	HFA1100IJ	P	
CLC402AJP	COMLINEAR	HFA1100IJ	P	
CLC402A8D	COMLINEAR	HFA1100IJ	P	
CLC406AID	COMLINEAR	HFA1100IJ	P	
CLC406AJP	COMLINEAR	HFA1100IJ	P	
CLC406A8B	COMLINEAR	HFA1100IJ	P	
CLC406A8D	COMLINEAR	HFA1100IJ	P	
CLC409AID	COMLINEAR	HFA1100IJ	P	
CLC409AJP	COMLINEAR	HFA1100IJ	P	
CLC409A8D	COMLINEAR	HFA1100IJ	P	
CLC446AJP	COMLINEAR	HFA1100IJ	P	
CLC446A8B	COMLINEAR	HFA1100IJ	P	
CLC446SMD	COMLINEAR	HFA1100IJ	P	
CLC449AJP	COMLINEAR	HFA1100IJ	P	
CLC449A8B	COMLINEAR	HFA1100IJ	P	
CLC449SMD	COMLINEAR	HFA1100IJ	P	
OPA648P	BURR-BROWN CORP	HFA1100IJ	P	
OPA658P	BURR-BROWN CORP	HFA1100IJ	P	
OPA658PB	BURR-BROWN CORP	HFA1100IJ	P	
5962-9200401MPX	COMLINEAR	HFA1100IJ	P	
5962-9203301MPX	COMLINEAR	HFA1100IJ	P	
5962-9203401MPX	COMLINEAR	HFA1100IJ	P	
5962-9459301MPA	ANALOG DEVICES	HFA1100IJ	P	

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COMPETITOR PART NUMBER	COMPETITOR NAME	HARRIS PART NUMBER	(NOTE) CROSS TYPE	COMMENTS
CLC425AJP	COMLINEAR	HFA1100IP	H	VFB vs CFB
CLC449AJP	COMLINEAR	HFA1100IP	H	
EL2171CN	ELANTEC	HFA1100IP	H	Better Performance
OPA644P	BURR-BROWN CORP	HFA1100IP	H	Better Bandwidth
OPA644PB	BURR-BROWN CORP	HFA1100IP	H	Better Bandwidth
OPA648P	BURR-BROWN CORP	HFA1100IP	H	
OPA658P	BURR-BROWN CORP	HFA1100IP	H	Harris is Higher I_{CC}
OPA658PB	BURR-BROWN CORP	HFA1100IP	H	Harris is Higher I_{CC}
AD8001AN	ANALOG DEVICES	HFA1100IP	P	
AD8001SMD	ANALOG DEVICES	HFA1100IP	P	
CLC402AID	COMLINEAR	HFA1100IP	P	
CLC402AJP	COMLINEAR	HFA1100IP	P	
CLC402A8D	COMLINEAR	HFA1100IP	P	
CLC406AIB	COMLINEAR	HFA1100IP	P	
CLC406AID	COMLINEAR	HFA1100IP	P	
CLC406AJP	COMLINEAR	HFA1100IP	P	
CLC406A8B	COMLINEAR	HFA1100IP	P	
CLC406A8D	COMLINEAR	HFA1100IP	P	
CLC409AID	COMLINEAR	HFA1100IP	P	
CLC409AJP	COMLINEAR	HFA1100IP	P	
CLC409A8D	COMLINEAR	HFA1100IP	P	
CLC446AJP	COMLINEAR	HFA1100IP	P	
CLC446A8B	COMLINEAR	HFA1100IP	P	
CLC446SMD	COMLINEAR	HFA1100IP	P	
CLC449A8B	COMLINEAR	HFA1100IP	P	
CLC449SMD	COMLINEAR	HFA1100IP	P	
OPA648H	BURR-BROWN CORP	HFA1100IP	P	
5962-9200401MPX	COMLINEAR	HFA1100IP	P	
5962-9203301MPX	COMLINEAR	HFA1100IP	P	

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COMPETITOR PART NUMBER	COMPETITOR NAME	HARRIS PART NUMBER	(NOTE) CROSS TYPE	COMMENTS
5962-9203401MPX	COMLINEAR	HFA1100IP	P	
5962-9459301MPA	ANALOG DEVICES	HFA1100IP	P	
CLC425AJE	COMLINEAR	HFA1100IB	H	VFB vs CFB
CLC449AJE	COMLINEAR	HFA1100IB	H	
EL2171CS	ELANTEC	HFA1100IB	H	Better Performance
OPA644U	BURR-BROWN CORP	HFA1100IB	H	Better Bandwidth
OPA644UB	BURR-BROWN CORP	HFA1100IB	H	Better Bandwidth
OPA648U	BURR-BROWN CORP	HFA1100IB	H	
OPA658U	BURR-BROWN CORP	HFA1100IB	H	Harris is Higher I_{CC}
OPA658UB	BURR-BROWN CORP	HFA1100IB	H	Harris is Higher I_{CC}
AD8001AR	ANALOG DEVICES	HFA1100IB	P	
AD8001AR-REEL	ANALOG DEVICES	HFA1100IB	P	
AD8001AR-REEL7	ANALOG DEVICES	HFA1100IB	P	
CLC402AJE	COMLINEAR	HFA1100IB	P	
CLC406AJE	COMLINEAR	HFA1100IB	P	
CLC409AJE	COMLINEAR	HFA1100IB	P	
CLC446AJE	COMLINEAR	HFA1100IB	P	
AD9620AD	ANALOG DEVICES	HFA1110IJ	H	Performance
AD9630AQ	ANALOG DEVICES	HFA1110IJ	H	Performance
CLC109AJB	COMLINEAR	HFA1110IJ	H	Better AC and Video Specs
CLC110AIB	COMLINEAR	HFA1110IJ	H	Better Performance
CLC111AIB	COMLINEAR	HFA1110IJ	H	Better Video Specs
AD9630AN	ANALOG DEVICES	HFA1110IP	H	Performance
CLC109AJP	COMLINEAR	HFA1110IP	H	Better AC and Video Specs
CLC110AJP	COMLINEAR	HFA1110IP	H	Better Performance
CLC111AJP	COMLINEAR	HFA1110IP	H	Better Video Specs
EL2072CN	ELANTEC	HFA1110IP	H	Better Performance
MAX405CPA	MAXIM	HFA1110IP	H	Better AC Specs, Lower Power
MAX405EPA	MAXIM	HFA1110IP	H	Better AC Specs, Lower Power

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COMPETITOR PART NUMBER	COMPETITOR NAME	HARRIS PART NUMBER	(NOTE) CROSS TYPE	COMMENTS
AD9630AR	ANALOG DEVICES	HFA1110IB	H	Performance
CLC109AJE	COMLINEAR	HFA1110IB	H	Better AC and Video Specs
CLC111AJE	COMLINEAR	HFA1110IB	H	Better Video Specs
EL2072CS	ELANTEC	HFA1110IB	H	Better Performance
MAX405CSA	MAXIM	HFA1110IB	H	Better AC Specs, Lower Power
MAX405ESA	MAXIM	HFA1110IB	H	Better AC Specs, Lower Power
CLC501A8B	COMLINEAR	HFA1130MJ/883	H	Better Performance
CLC502A8B	COMLINEAR	HFA1130MJ/883	H	Better Performance
CLC501AID	COMLINEAR	HFA1130MJ/883	P	
CLC501AJP	COMLINEAR	HFA1130MJ/883	P	
CLC501AMD	COMLINEAR	HFA1130MJ/883	P	
CLC501A8D	COMLINEAR	HFA1130MJ/883	P	
CLC502AID	COMLINEAR	HFA1130MJ/883	P	
CLC502AJP	COMLINEAR	HFA1130MJ/883	P	
CLC502A8D	COMLINEAR	HFA1130MJ/883	P	
5962-8997401PX	COMLINEAR	HFA1130MJ/883	P	
5962-9174301MPX	COMLINEAR	HFA1130MJ/883	P	
CLC501AIB	COMLINEAR	HFA1130IJ	H	Better Performance
CLC502AIB	COMLINEAR	HFA1130IJ	H	Better Performance
CLC501AID	COMLINEAR	HFA1130IJ	P	
CLC501AJP	COMLINEAR	HFA1130IJ	P	
CLC501AMD	COMLINEAR	HFA1130IJ	P	
CLC501A8D	COMLINEAR	HFA1130IJ	P	
CLC502AID	COMLINEAR	HFA1130IJ	P	
CLC502AJP	COMLINEAR	HFA1130IJ	P	
CLC502A8D	COMLINEAR	HFA1130IJ	P	
5962-8997401PX	COMLINEAR	HFA1130IJ	P	
5962-9174301MPX	COMLINEAR	HFA1130IJ	P	
CLC501AJP	COMLINEAR	HFA1130IP	H	Better Performance

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COMPETITOR PART NUMBER	COMPETITOR NAME	HARRIS PART NUMBER	(NOTE) CROSS TYPE	COMMENTS
CLC502AJP	COMLINEAR	HFA1130IP	H	Better Performance
CLC501AID	COMLINEAR	HFA1130IP	P	
CLC501AMD	COMLINEAR	HFA1130IP	P	
CLC501A8D	COMLINEAR	HFA1130IP	P	
CLC502AID	COMLINEAR	HFA1130IP	P	
CLC502A8D	COMLINEAR	HFA1130IP	P	
5962-8997401PX	COMLINEAR	HFA1130IP	P	
5962-9174301MPX	COMLINEAR	HFA1130IP	P	
CLC501AJE	COMLINEAR	HFA1130IB	H	Better Performance
CLC502AJE	COMLINEAR	HFA1130IB	H	Better Performance
UPA103G	NEC	HFA3046B	H	
UPA101G	NEC	HFA3101B	H	
UPA102G	NEC	HFA3102B	H	
UPA102G	NEC	HFA3102B96	P	
MMSF5N02HD	MOTOROLA	RF1K49157	E	The Harris RF1K49157 has a 25% lower (better) $r_{DS(ON)}$ and a 50% higher (better) breakdown voltage.
MMSF5N03HD	MOTOROLA	RF1K49157	E	The Harris RF1K49157 has a 25% lower (better) $r_{DS(ON)}$.
MMDF3N03HD	MOTOROLA	RF1K49086	E	The Harris RF1K49086 has a 15% lower (better) $r_{DS(ON)}$.
MMDF3N02HD	MOTOROLA	RF1K49086	E	The Harris RF1K49086 has a 30% lower (better) $r_{DS(ON)}$ and a 50% higher (better) breakdown voltage.
MMSF6N01HD	MOTOROLA	RF1K49157	E	The RF1K49157 has a 150% (higher) breakdown voltage.
MMDF4N01HD	MOTOROLA	RF1K49090	D	
MMDF2P01HD	MOTOROLA	RF1K49093	E	The Harris RF1K49093 has a 30% lower (better) $r_{DS(ON)}$.
MMDF2C01HD	MOTOROLA	RF1K49092	E	The Harris RF1K49092 has a 30% lower (better) $r_{DS(ON)}$ for the P-channel MOS and a 40% lower (better) $r_{DS(ON)}$ for the N-channel MOS.
IRF7102	INT'L RECTIFIER	RF1K49154	E	The Harris RF1K49154 has a 20% higher (better) breakdown voltage.

NOTE: D = Direct Replacement, E = Functionally Equivalent Pin-for-Pin Replacement. Electrical specification review required,
H = Harris Recommended Replacement, P = Pin-for-Pin Replacement

COMPETITOR PART NUMBER	COMPETITOR NAME	HARRIS PART NUMBER	(NOTE) CROSS TYPE	COMMENTS
IRF7201	INT'L RECTIFIER	RF1K49157	D	
NDS9410	NATIONAL SEMI	RF1K49157	D	
NDS9945	NATIONAL SEMI	RF1K49154	D	
NDS9955	NATIONAL SEMI	RF1K49154	E	The Harris RF1K49154 has a 20% higher (better) breakdown voltage.
SI9410DY	SILICONIX	RF1K49157	D	
SI9925DY	SILICONIX	RF1K49090	E	The Harris RF1K49090 has a 40% lower (not as good as) breakdown voltage.
		RF1K49088	E	The RF1K49088 has a 50% higher (better) breakdown voltage and a 20% higher (not as good as) $r_{DS(ON)}$.
SI9928DY	SILICONIX	RF1K49092	E	The Harris RF1K49092 has a 40% lower (not as good as) breakdown voltage.
SI9933DY	SILICONIX	RF1K49093	E	The Harris RF1K49093 has a 40% lower (not as good as) breakdown voltage and a 20% higher (not as good as) $r_{DS(ON)}$.
SI9936DY	SILICONIX	RF1K49086	E	The RF1K49086 has a 20% higher (not as good as) $r_{DS(ON)}$.
SI9945DY	SILICONIX	RF1K49154	D	
SI9955DY	SILICONIX	RF1K49154	E	The Harris RF1K49154 has a 20% higher (better) breakdown voltage.

NOTE: D = Direct Replacement, E = Functionally Equivalent Pin-for-Pin Replacement. Electrical specification review required,
H = Harris Recommended Replacement, P = Pin-for-Pin Replacement

COMMUNICATIONS 3

WIRELESS COMMUNICATIONS

AN9640 "Glossary of Communication Terms" (32 pages) is not included in this data book, but is available on the net at *http://www.semi.harris.com/appnotes/an9640/* and Harris AnswerFAX (407-724-7800) document # 99640.

WIRELESS BUILDING BLOCKS

PART NUMBER	FUNCTION	FEATURES	PACKAGE	AnswerFAX DOCUMENT NUMBER
HFA3424	2.4GHz Low Noise Amplifier	14dB Gain, 1.9dB Noise Figure	SOIC, T&R	4131
HFA3524	2.5GHz/600MHz Dual Synthesizer	Dual Modulus Prescaler 32/33 or 64/65	TSSOP, T&R	4062
HFA3624	2.4GHz Up/Down Converter	10MHz to 400MHz IF Range	SSOP, T&R	4066
HFA3724	400MHz Quadrature IF Modulator/Demodulator	84dB gain, Programmable Low Pass Filter	TQFP, T&R	4067
HSP3824	Direct Sequence Spread Spectrum Baseband Processor	16-Bit PN Code, 12dB Processing Gain, Data Rate up to 4 MBPS	TQFP, T&R	4064
HFA3925	2.4GHz RF Power Amplifier	P(1dB): +24dBm, Integrated T/R Switch	SSOP, T&R	4132

HARRIS SEMICONDUCTOR

PRISM™ 2.4GHz Chip Set

Direct Sequence Spread Spectrum Wireless Transceiver Chip Set

October 1996

Features

- Provides Antenna-to-Bits™ Data Stream
- Low Voltage Operation from 2.7V to 5.5V
- 2.4GHz - 2.5GHz ISM Band Operation
- Single Heterodyne Conversion
- Programmable Antialiasing and Shaping Filters
- 10MHz to 400MHz IF Operation with RSSI
- Autonomous Half Duplex Direct Sequence Modem
- Selectable DBPSK, DQPSK Signalling
- Antenna Diversity Selection
- Direct Sequence Physical Layer (DS-PHY)
- Differential Data Encoding/Decoding
- Programmable 16-Bit PN Code
- Data Rates up to 4 MBPS DQPSK
- Power Management Control
- Low Profile PCMCIA-Compatible Surface Mount Packaging

Applications

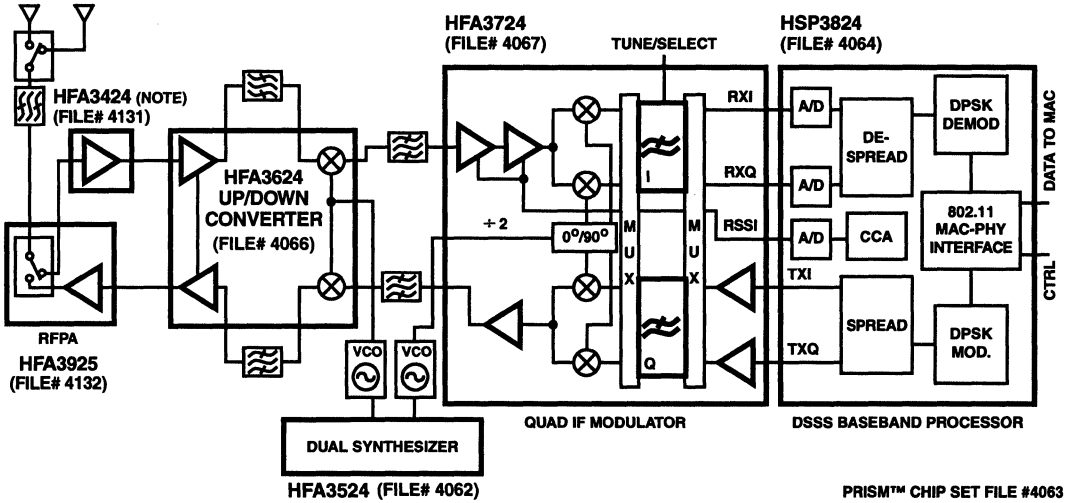
- Systems Targeting IEEE 802.11 Standard
- PCMCIA Wireless Transceiver
- WLAN RF Modems
- TDMA Packet Protocol Radios
- Part 15 Compliant Radio Links

Description

The Harris 2.4GHz PRISM™ chip set is a highly integrated five-chip solution for RF modems employing Direct Sequence Spread Spectrum (DSSS) signaling. Significant integration of transmit and receive functions employ the following ICs: complete integrated DSSS engine, the HSP3824; a quadrature modulator/demodulator, integrated with an IF limiter amplifier with RSSI, the HFA3724; a combined LNA/Mixer and upconverter/preamplifier, the HFA3624; a high performance, low noise amplifier for increased receiver sensitivity, the HFA3424; a dual synthesizer, the HFA3524 and a monolithic RF power amplifier, the HFA3925. Each of the functions may be used individually or in any combination in support of a variety of RF modem applications.

The PRISM™ chip set is intended to support various data rates including systems targeting the proposed IEEE 802.11 standard "Direct Sequence Physical layer (DS-PHY)". Differential BPSK and QPSK signaling is employed with differential encoding and decoding of packetized data. A PN sequence rate of up to 22 MCPS is supported for up to a 16 chip PN code. Integrated programmable low pass filters are used on the HFA3724 to allow chip rates from 2.75 MCPS to 22 MCPS. A flexible general purpose data and control interface is provided for parameter configuration and for transferring data packets between the PHY and Media Access Control (MAC) layers. Data rates of up to 2 MBPS for DBPSK and 4 MBPS for DQPSK are supported.

Typical Application Diagram



NOTE: Required for systems targeting 802.11 specifications.

PRISM™, the PRISM™ logo and Antenna-to-Bits™ are trademarks of Harris Corporation.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4063.4**

Typical 802.11 DS-PHY System Level Performance (Note 5) (Measured at a diversity antenna port)

Receiver

- Frequency Range ..... 2.4GHz - 2.4835GHz
- Step Size 1MHz
- Cascaded Noise Figure 6.8dB
- Sensitivity..... -93dBm, 1 MBPS, 8E-2 FER (Note 1)
  -90dBm, 2 MBPS, 8E-2 FER (Note 1)
- Input Intercept Point.....-17dBm
- IF Frequency 280MHz
- IF Bandwidth 17MHz
- Image Rejection.....80dB
- Adjacent Channel Rejection..... >35dB
- Supply Voltage.....2.7V - 5.5V

Transmitter

- Frequency Range .....2.4GHz - 2.4835GHz
- Step Size.....1MHz
- Output Power .....+18dBm
- Spurious Outputs ..... Targeting ISM/802.11
- Transmit Spectral Mask..... -32dBr at First Side-Lobe
- IF Frequency.....280MHz
- Supply Voltage ..... 2.7V - 5.5V

General Specifications

- Targeted Standard..... IEEE 802.11
- Data Rate ..... 1 MBPS DBPSK
  2 MBPS DQPSK
- Range .....400ft Indoor (Note 2)
  3700ft Outdoor (Note 2)
- RX/TX Switching Speed 2µs
- Standby Current
  - Mode 1: 240mA at 1µs Recovery (Notes 3, 4)
  - Mode 2: 58mA at 25µs Recovery (Notes 3, 4)
  - Mode 3: 47mA at 2ms Recovery (Notes 3, 4)
  - Mode 4: 33mA at 25ms Recovery (Notes 3, 4)
- Active Mode Current 304mA

NOTES:

1. FER = Frame Error Rate or Packet Error Rate.
2. Range Test using AND-C-107 omnidirectional antenna.
3. Supply current includes AM79C930 MAC Processor.
4. Recovery time is for the PRISM™ 2.4GHz Chip Set only and does not include programming latency of the AM79C930 MAC Processor.
5. Refer to Application Note AN9624 for more information on the "PRISM™ DSSS PC Card Wireless LAN Description".

HARRIS SEMICONDUCTOR

HFA3424

2.4GHz - 2.5GHz Low Noise Amplifier

January 1997

Features

- Low Noise Figure 1.90dB
- High Gain 14dB
- Low Power Consumption . . . . . 3V to 5V, 5mA
- High Dynamic Range
- DC Decoupled RF Input and Output
- No External RF Tuning Elements Necessary
- Low Cost SOIC 8 Lead Plastic Package

Applications

- Systems Targeting IEEE 802.11 Standard
- TDD Quadrature-Modulated Communication Systems
- Wireless Local Area Networks
- PCMCIA Wireless Transceivers
- ISM Systems
- TDMA Packet Protocol Radios
- PCS/Wireless PBX
- Wireless Local Loop

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HFA3424IB	-40 to 85	8 Ld SOIC	M8.15
HFA3424IB96	-40 to 85	Tape and Reel	

Description

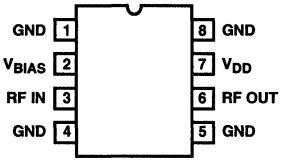
The Harris 2.4GHz PRISM™ chip set is a highly integrated five-chip solution for RF modems employing Direct Sequence Spread Spectrum (DSSS) signaling. The HFA3424 2.4GHz - 2.5GHz low noise amplifier is an optional chip that can be added to the five chips in the PRISM™ chip set. The HFA3424 offers increased sensitivity for systems targeting 802.11 specifications. (See Figure 1, the Typical Application Diagram.)

The Harris HFA3424 PRISM™ is a high performance low noise amplifier in a low cost SOIC 8 lead surface mount plastic package. The HFA3424 employs a fully monolithic design which eliminates the need for external tuning networks. It can be biased using 3V or 5V supplies and has an option for biasing at higher currents for increased dynamic range.

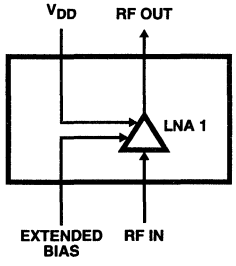
The HFA3424 is ideally suited for use where low noise figure, high gain, high dynamic range and low power consumption required. Typical applications include receiver front ends in the Wireless Local Area Network (WLAN) and wireless data collection markets in the 2.4GHz Industrial, Scientific and Medical (ISM) band, as well as standard gain blocks, buffer amps, driver amps and IF amps in both fixed and portable systems.

Pinout

HFA3424
(SOIC)
TOP VIEW



Functional Block Diagram



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File Number 4131.2

Typical Application Diagram

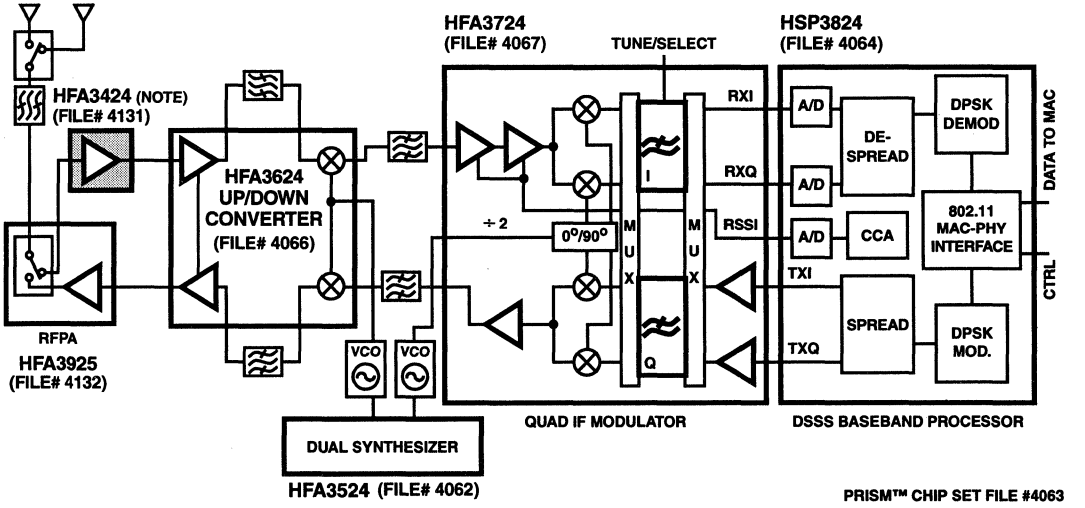


FIGURE 1. TYPICAL TRANSCEIVER AMPLIFIER APPLICATIONS CIRCUIT USING THE HFA3424

NOTE: Required for systems targeting 802.11 specifications.

For additional information on the PRISM™ chip set, call (407) 724-7800 to access Harris' AnswerFAX system. When prompted, key in the four-digit document number (File #) of the datasheets you wish to receive.

The four-digit file numbers are shown in Typical Application Diagram, and correspond to the appropriate circuit.

Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . +10V_{DC}
Input Power . . . . . +17dBm
Supply Current (Note 1) 30mA

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
SOIC Package 165
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Only if Pin 2 is used to increase current.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = 25°C, Z_0 = 50Ω, V_{DD} = +5V, P_{IN} = -30dBm, f = 2.45GHz, V_{BIAS} = Open Circuit Unless Otherwise Specified

PARAMETER	MIN	TYP	MAX	UNITS
LNA Input Frequency Range	2.4	-	2.5	GHz
Gain	12	14	16	dB
Noise Figure	-	1.90	2.30	dB
Input VSWR	-	1.5:1	-	
Output VSWR	-	1.5:1	-	
Input Return Loss	-	-14.0	-	dB
Output Return Loss	-	-14.0	-	dB
Output 1dB Compression	-	3	-	dBm
Input IP_3	-	1	-	dBm
Reverse Isolation	-	30	-	dB
Supply Current at V_{DD} = 5V	3	5	7	mA
Supply Range	2.7	-	5.5	V

Typical Performance Curves

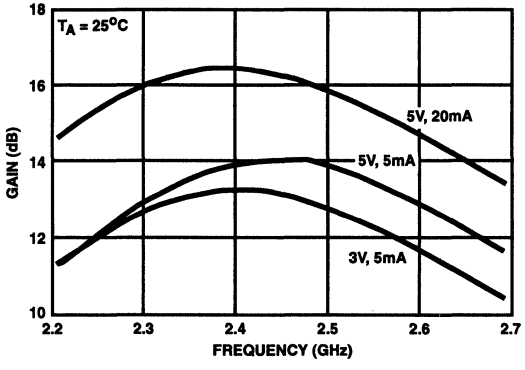


FIGURE 2. GAIN vs FREQUENCY

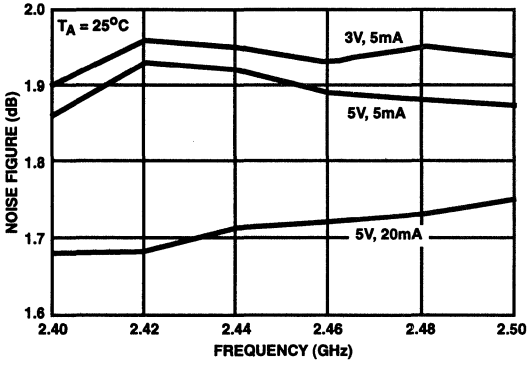


FIGURE 3. NOISE FIGURE vs FREQUENCY

Typical Performance Curves (Continued)

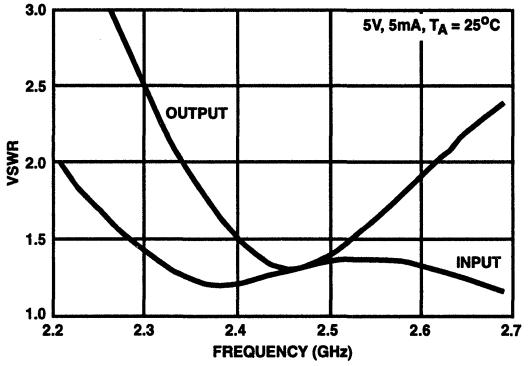


FIGURE 4. VSWR vs FREQUENCY

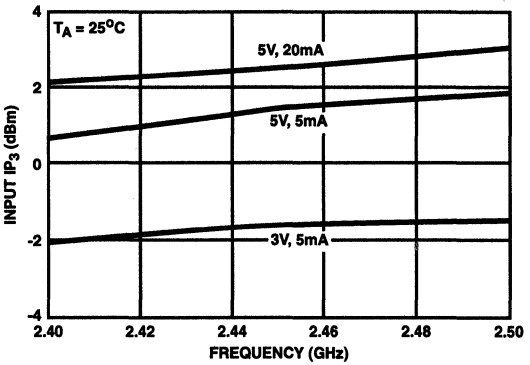


FIGURE 5. INPUT IP_3 vs FREQUENCY

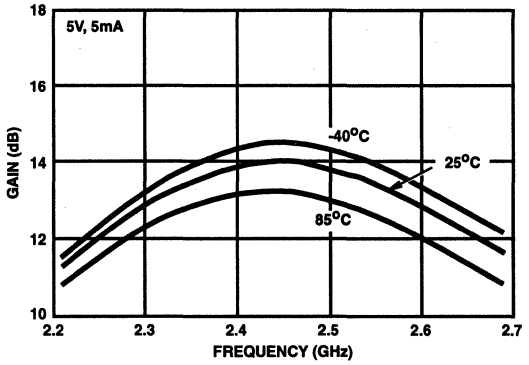


FIGURE 6. GAIN vs FREQUENCY

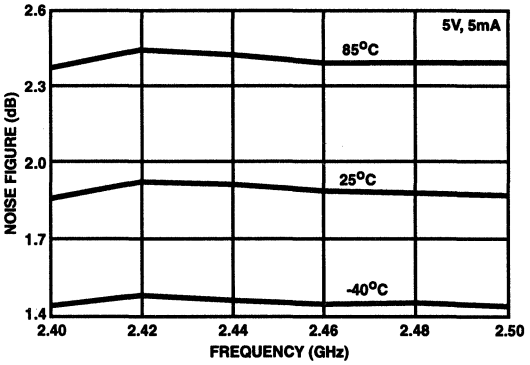
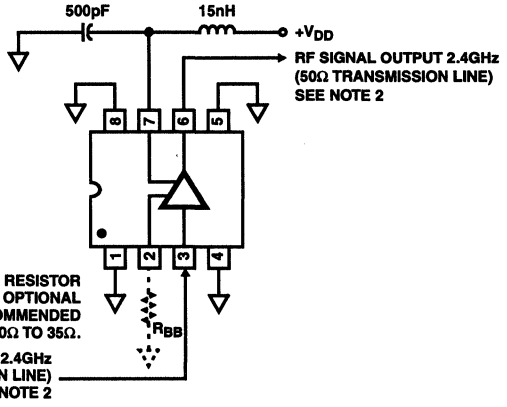


FIGURE 7. NOISE FIGURE vs FREQUENCY

Typical Application Circuit

V_{BIAS} (PIN 2)

NORMAL BIAS	EXTENDED BIAS
Open	30Ω To 35Ω To Ground



NOTE:

3. No DC blocking capacitor required on LNA input or output transmission lines.

FIGURE 8. REFERENCE APPLICATION/TEST DESIGN SETUP SCHEMATIC: LOW NOISE AMPLIFIER

HARRIS SEMICONDUCTOR

HFA3524

January 1997

2.5GHz/600MHz Dual Frequency Synthesizer

Features

- 2.7V to 5.5V Operation
- Low Current Consumption
- Selectable Powerdown Mode I_{CC} = 1μA Typical at 3V
- Dual Modulus Prescaler, 32/33 or 64/65
- Selectable Charge Pump High Z State Mode

Applications

- Systems Targeting IEEE 802.11 Standard
- PCMCIA Wireless Transceiver
- Wireless Local Area Network Modems
- TDMA Packet Protocol Radios
- Part 15 Compliant Radio Links
- Portable Battery Powered Equipment

Description

The Harris 2.4GHz PRISM™ chip set is a highly integrated five-chip solution for RF modems employing Direct Sequence Spread Spectrum (DSSS) signaling. The HFA3524 600MHz Dual Frequency Synthesizer is one of the five chips in the PRISM™ chip set (see the Typical Application Diagram).

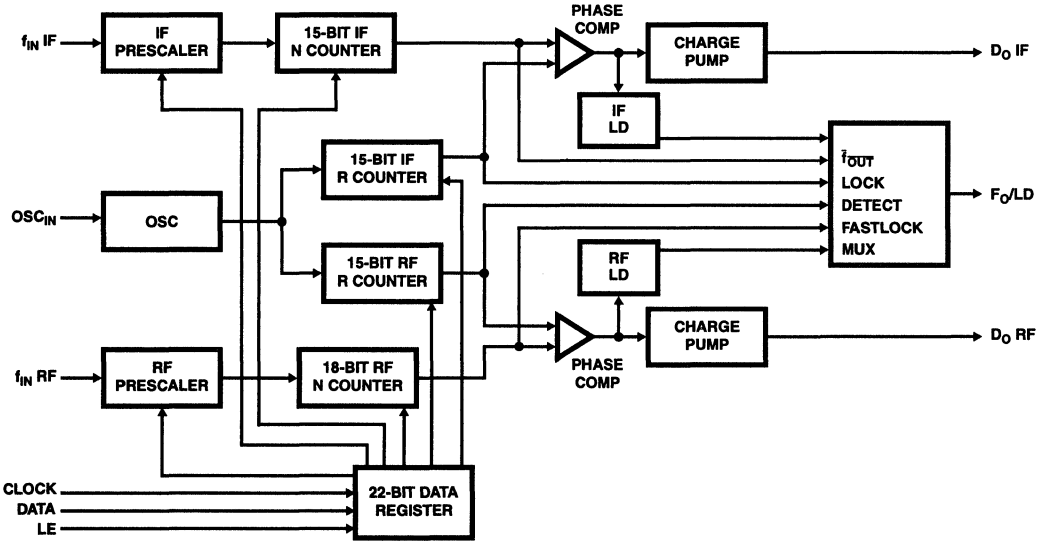
The HFA3524 is a monolithic, integrated dual frequency synthesizer, including prescaler, is to be used as a local oscillator for RF and first IF of a dual conversion transceiver.

The HFA3524 contains a dual modulus prescaler. A 32/33 or 64/65 prescaler can be selected for the RF synthesizer and a 8/9 or a 16/17 prescaler can be selected for the IF synthesizer. Using a digital phase locked loop technique, the HFA3524 can generate a very stable, low noise signal for the RF and IF local oscillator. Serial data is transferred into the HFA3524 via a three wire interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The HFA3524 features very low current consumption of 13mA at 3V.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA3524IA	-40 to 85	20 Ld TSSOP	M20.173
HFA3524IA96	-40 to 85	Tape and Reel	

Functional Block Diagram



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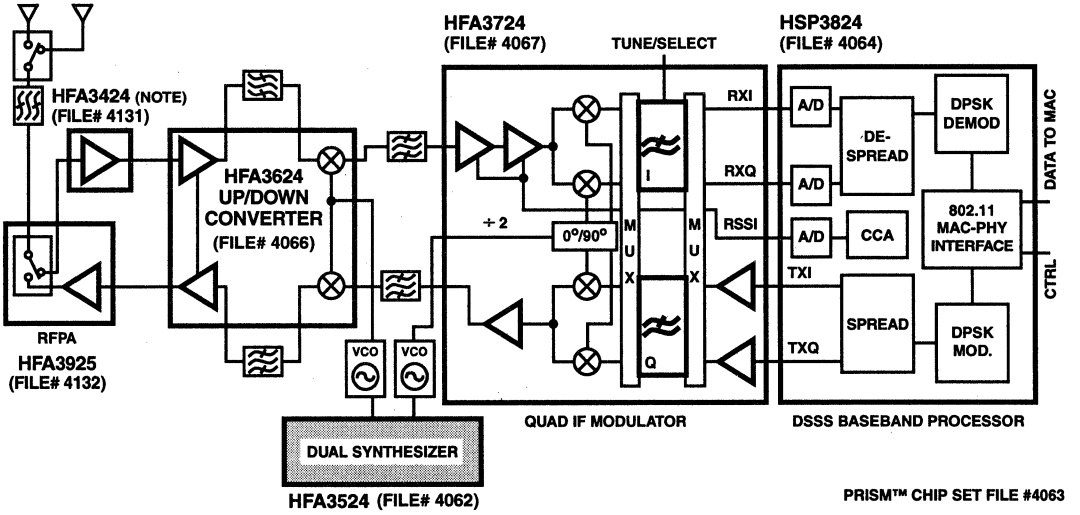
File Number **4062.4**

Typical Application Diagram



TYPICAL TRANSCEIVER APPLICATION CIRCUIT USING THE HFA3524

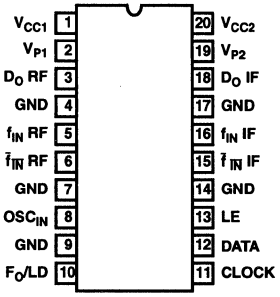
NOTE: Required for systems targeting 802.11 specifications.

For additional information on the PRISM™ chip set, call (407) 724-7800 to access Harris' AnswerFAX system. When prompted, key in the four-digit document number (File #) of the datasheets you wish to receive.

The four-digit file numbers are shown in Typical Application Diagram, and correspond to the appropriate circuit.name a

Pinout

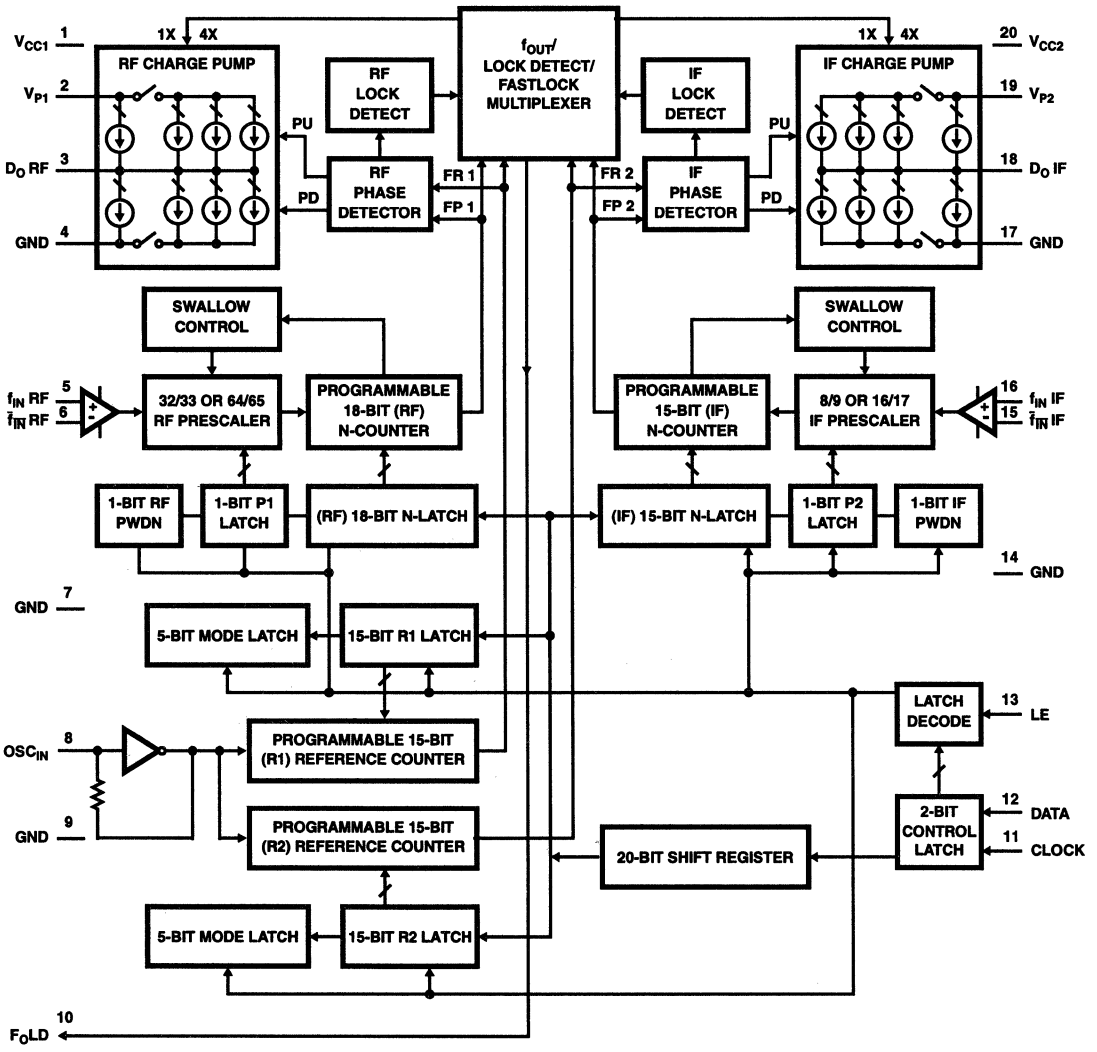
HFA3524 (TSSOP)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	I/O	DESCRIPTION
1	V_{CC1}	-	Power supply voltage input. Input may range from 2.7V to 5.5V. V_{CC1} must equal V_{CC2}. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
2	V_{P1}	-	Power Supply for RF charge pump. Must be > V_{CC}.
3	D_O RF	O	Internal charge pump output. For connection to a loop filter for driving the input of an external V_{CO}.
4	GND	-	Ground.
5	f_{IN} RF	I	RF prescaler input. Small signal input from the V_{CO}.
6	$\overline{f}_{IN}$ RF	I	RF prescaler complimentary input. A bypass capadtor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with some loss of sensitivity.
7	GND	-	Ground.
8	OSC_{IN}	I	Oscillator input. The input has a V_{CC}/2 input threshold and can be driven from an external CMOS or TTL logic gate.
9	GND	-	Ground.
10	F_O/LD	O	Multiplexed output of the RF/IF progrannmable or reference dividers, RF/IF lock detect signals and Fastlock mode. CMOS output (see Programmable Modes).
11	Clock	I	High impedance CMOS Clock input. Data for the various counters is clocked in on the rising edge, into the 22-bit shift register.
12	Data	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
13	LE	I	Load enable CMOS input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 4 appropriate latches (control bit dependent).
14	GND	-	Ground.
15	$\overline{f}_{IN}$ IF	I	IF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with some loss of sensitivity.
16	f_{IN} IF	I	IF prescaler input. Small signal input from the V_{CO}.
17	GND	-	Ground.
18	D_O IF	O	IF charge pump output. For connection to a loop filter for driving the input of an external V_{CO}.
19	V_{P2}	-	Power Supply for IF charge pump. Must be >V_{CC}.
20	V_{CC2}	-	Power supply voltage input Input may range from 2.7V to 5.5V. V_{CC2} must equal V_{CC1}. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.

Block Diagram



NOTES:

1. V_{CC1} supplies power to the RF prescaler, N-counter and phase detector. V_{CC2} supplies power to the IF prescaler, N-counter and phase detector, RF and IF R-counters along with the OSC_{IN} buffer and all digital circuitry. V_{CC1} and V_{CC2} are separated by a diode and must be run at the same voltage level.
2. V_{P1} and V_{P2} can be run independently as long as $V_P \geq V_{CC}$.

Absolute Maximum Ratings

Power Supply Voltage
- V_{CC} ..... -0.3V to +6.5V
- V_P ..... -0.3V to +6.5V

Voltage on Any Pin with GND = 0V (V_I) ..... -0.3V to +6.5V

Operating Conditions

Power Supply Voltage
- V_{CC} ..... 2.7V to 5.5V
- V_P ..... V_{CC} to +5.5V

Temperature (T_A) ..... -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
- TSSOP Package 130

Maximum Storage Temperature Range (T_S) ..... -65°C to 150°C

Maximum Lead Temperature (Soldering 4s) (T_L) ..... 260°C
(TSSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{CC} = 3.0V, V_P = 3.0V, -40°C < T_A < 85°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CC}					
RF + IF		V_{CC} = 2.7V to 5.5V	-	13	-	mA
RF Only		V_{CC} = 2.7V to 5.5V	-	10	-	mA
Powerdown Current	$I_{CC-PWDN}$	V_{CC} = 3.0V	-	1	25	µA
Operating Frequency	f_{IN} RF		500	-	2.5	GHz
Operating Frequency	f_{IN} IF		45	-	600	MHz
Maximum Oscillator Frequency	f_{OSC}		44	-	-	MHz
Maximum Phase Detector Frequency	f_ϕ		10	-	-	MHz
RF Input Sensitivity	Pf_{IN} RF	V_{CC} = 3.0V	-15	-	+4	dBm
		V_{CC} = 5.0V	-10	-	+4	dBm
IF Input Sensitivity	Pf_{IN} IF	V_{CC} = 2.7V to 5.5V	-10	-	+4	dBm
Oscillator Sensitivity	V_{OSC}	OSC_{IN}	0.5	-	-	V_{P-P}
High Level Input Voltage	V_{IH}	(Note)	$0.8V_{CC}$	-	-	V
Low Level Input Voltage	V_{IL}	(Note)	-	-	$0.2V_{CC}$	V
High Level Input Current	I_{IH}	V_{IH} = V_{CC} = 5.5V (Note)	-1.0	-	1.0	µA
Low Level Input Current	I_{IL}	V_{IL} = 0V, V_{CC} = 5.5V (Note)	-1.0	-	1.0	µA
Oscillator Input Current	I_{IH}	V_{IH} = V_{CC} = 5.5V	-	-	100	µA
Oscillator Input Current	I_{IL}	V_{IL} = 0V, V_{CC} = 5.5V	-100	-	-	µA
High Level Output Voltage	V_{OH}	I_{OH} = -500µA	V_{CC} -0.4	-	-	V
Low Level Output Voltage	V_{OL}	I_{OL} = 500µA	-	-	0.4	V
Data to Clock Set Up Time	t_{CS}	See Data Input Timing	50	-	-	ns
Data to Clock Hold Time	t_{CH}	See Data Input Timing	10	-	-	ns
Clock Pulse Width High	t_{CWH}	See Data Input Timing	50	-	-	ns
Clock Pulse Width Low	t_{CWL}	See Data Input Timing	50	-	-	ns
Clock to Load Enable Set Up Time	t_{ES}	See Data Input Timing	50	-	-	ns
Load Enable Pulse Width	t_{EW}	See Data Input Timing	50	-	-	ns

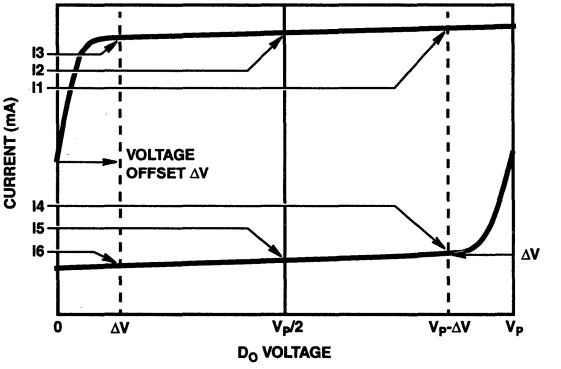
NOTE: Clock, Data and LE does not include f_{IN} RF, f_{IN} IF and OSC_{IN}.

Charge Pump Specifications V_{CC} = 3.0V, V_P = 3.0V, -40°C < T_A < 85°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Charge Pump Output Current	$I_{DO-SOURCE}$	$V_{DO} = V_P/2$, I_{CPO} = HIGH (Note 4)	-	-5.0	-	mA
	$I_{DO-SINK}$	$V_{DO} = V_P/2$, I_{CPO} = HIGH (Note 4)	-	5.0	-	mA
	$I_{DO-SOURCE}$	$V_{DO} = V_P/2$, I_{CPO} = LOW (Note 4)	-	-1.25	-	mA
	$I_{DO-SINK}$	$V_{DO} = V_P/2$, I_{CPO} = LOW (Note 4)	-	1.25	-	mA
Charge Pump High Z State Current	$I_{DO-HIGH\ Z}$	0.5V ≤ V_{DO} ≤ V_P - 0.5, -40°C < T < 85°C	-2.5	-	2.5	nA
CP Sink vs Source Mismatch (Note 5)	$I_{DO-SINK}$ vs $I_{DO-SOURCE}$	$V_{DO} = V_P/2$, T_A = 25°C	-	3	10	%
CP Current vs Voltage (Note 6)	I_{DO} vs V_{DO}	0.5V ≤ V_{DO} ≤ V_P - 0.5, T < 25°C	-	10	15	%
CP Current vs Temperature (Note 7)	I_{DO} vs T	$V_{DO} = V_P/2$, -40°C < T < 85°C	-	10	-	%

NOTES:

4. See Programmable Modes for ICP) description.
5. I_{DO} vs V_{DO} = Charge Pump Output Current magnitude variation vs Voltage = $[1/2 \cdot \{|I1| - |I3|\}]/[1/2 \cdot \{|I1| + |I3|\}] \cdot 100\%$ and $[1/2 \cdot |I4| - |I6|]/[1/2 \cdot \{|I4| + |I6|\}] \cdot 100\%$.
6. $I_{DO-SINK}$ vs $I_{DO-SOURCE}$ = Charge Pump Output Current Sink vs Source Mismatch = $[|I2| - |I5|]/[1/2 \cdot \{|I2| + |I5|\}] \cdot 100\%$.
7. I_{DO} vs T_A = Charge Pump Output Current magnitude variation vs Temperature = $[|I2 \text{ at temp}| - |I2 \text{ at } 25°C|]/|I2 \text{ at } 25°C| \cdot 100\%$ and $[|I5 \text{ at temp}| - |I5 \text{ at } 25°C|]/|I5 \text{ at } 25°C| \cdot 100\%$.



I1 = CP sink current at $V_{DO} = V_P - \Delta V$
I2 = CP sink current at $V_{DO} = V_P/2$
I3 = CP sink current at $V_{DO} = \Delta V$
I4 = CP source current at $V_{DO} = V_P - \Delta V$
I5 = CP source current at $V_{DO} = V_P/2$
I6 = CP source current at $V_{DO} = \Delta V$

FIGURE 1. CHARGE PUMP CURRENT SPECIFICATION DEFINITIONS

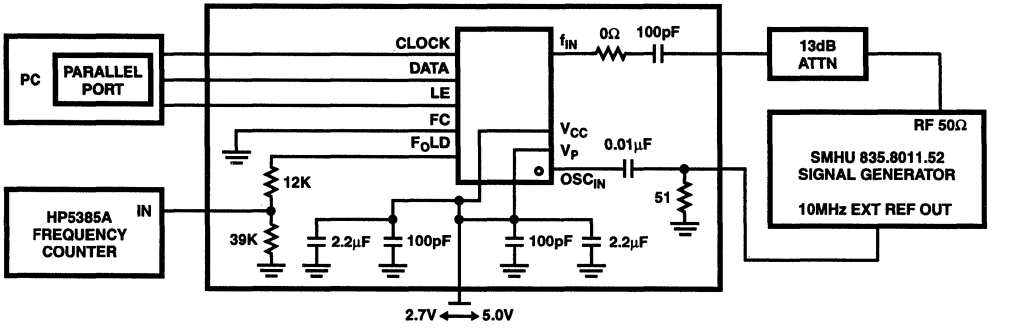


FIGURE 2. RF SENSITIVITY TEST BLOCK DIAGRAM

Typical Performance Curves

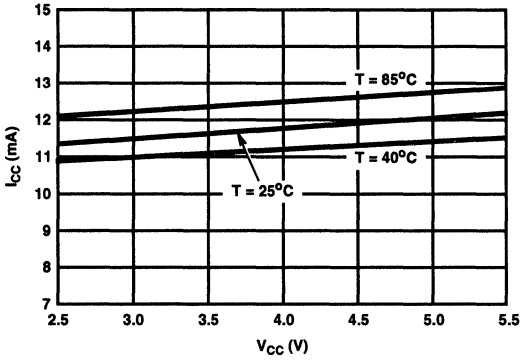


FIGURE 3. I_{CC} vs V_{CC}

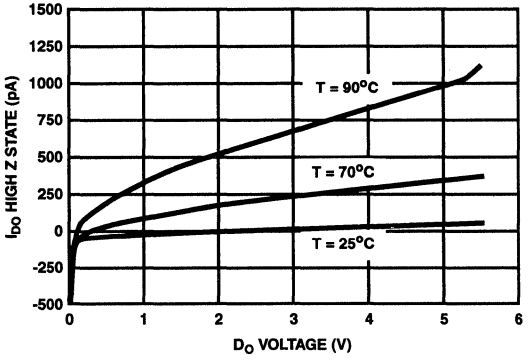


FIGURE 4. I_{DO} HIGH Z STATE vs D_O VOLTAGE

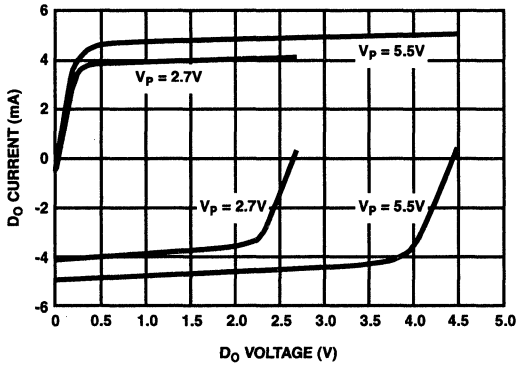


FIGURE 5. CHARGE PUMP CURRENT vs D_O VOLTAGE
I_{CP} = HIGH

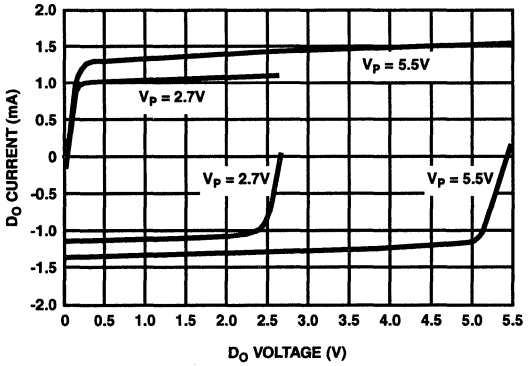
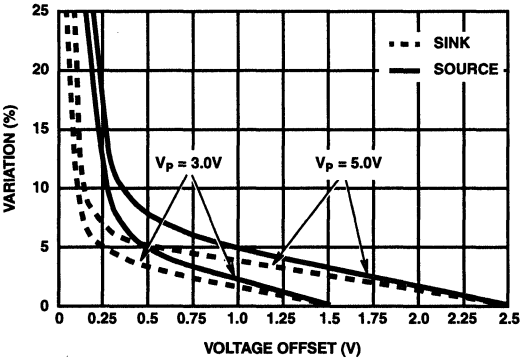


FIGURE 6. CHARGE PUMP CURRENT vs D_O VOLTAGE
I_{CP} = LOW



NOTE: See charge pump current specification definitions.

FIGURE 7. CHARGE PUMP CURRENT VARIATION

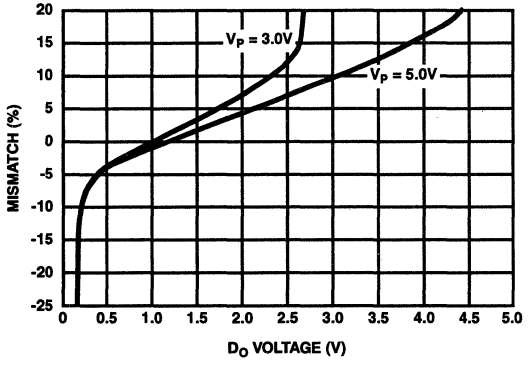
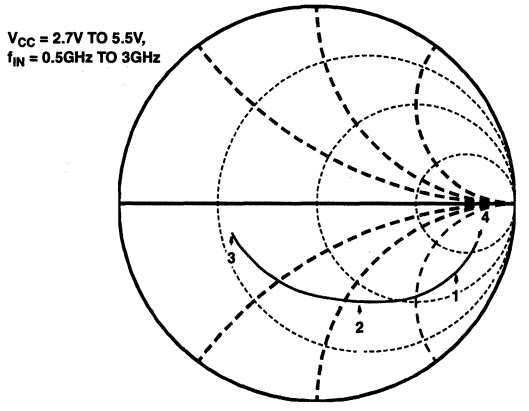


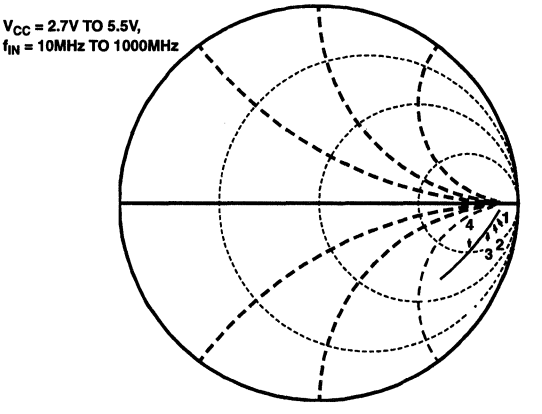
FIGURE 8. SINK vs SOURCE MISMATCH vs D_O VOLTAGE

Typical Performance Curves (Continued)



Marker 1 = 1GHz, Real = 101, Imaginary = -144
Marker 2 = 2GHz, Real = 37, Imaginary = -54
Marker 3 = 3GHz, Real = 22, Imaginary = -2
Marker 4 = 500MHz, Real = 209, Imaginary = -232

FIGURE 9. RF INPUT IMPEDANCE



Marker 1 = 100MHz, Real = 589, Imaginary = -209
Marker 2 = 200MHz, Real = 440, Imaginary = -286
Marker 3 = 300MHz, Real = 326, Imaginary = -287
Marker 4 = 500MHz, Real = 202, Imaginary = -234

FIGURE 10. IF INPUT IMPEDANCE

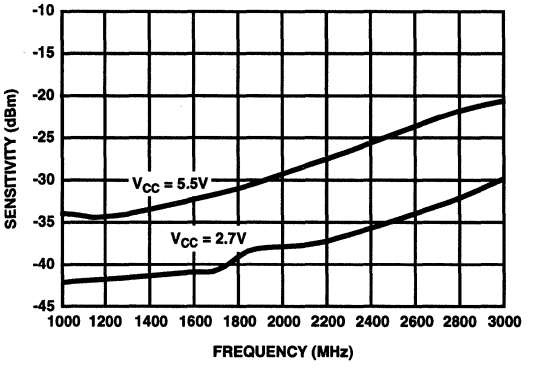


FIGURE 11. RF SENSITIVITY vs FREQUENCY

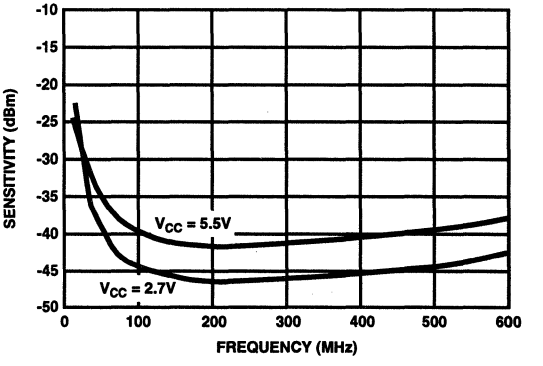


FIGURE 12. IF INPUT SENSITIVITY vs FREQUENCY

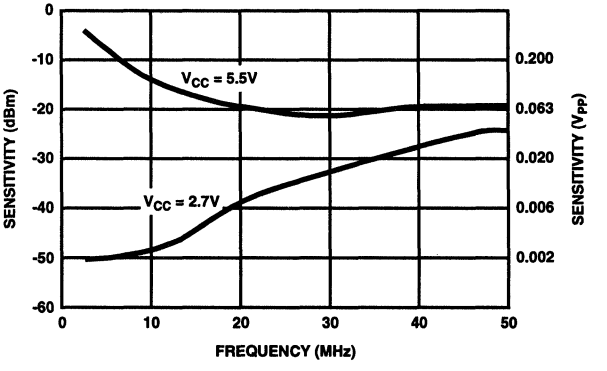


FIGURE 13. OSCILLATOR INPUT SENSITIVITY vs FREQUENCY

Functional Description

The simplified block diagram in Figure 14 shows the 22-bit data register, two 15-bit R Counters and the 15-bit and 18-bit N Counters (intermediate latches are not shown). The data stream is clocked (on the rising edge of Clock) into the DATA input, MSB first. The last two bits are the Control Bus. The DATA is transferred into the counters as follows:

CONTROL BITS		DATA LOCATION
C1	C2	
0	0	IR R Counter
0	1	RF R Counter
1	0	IF N Counter
1	1	RF N Counter

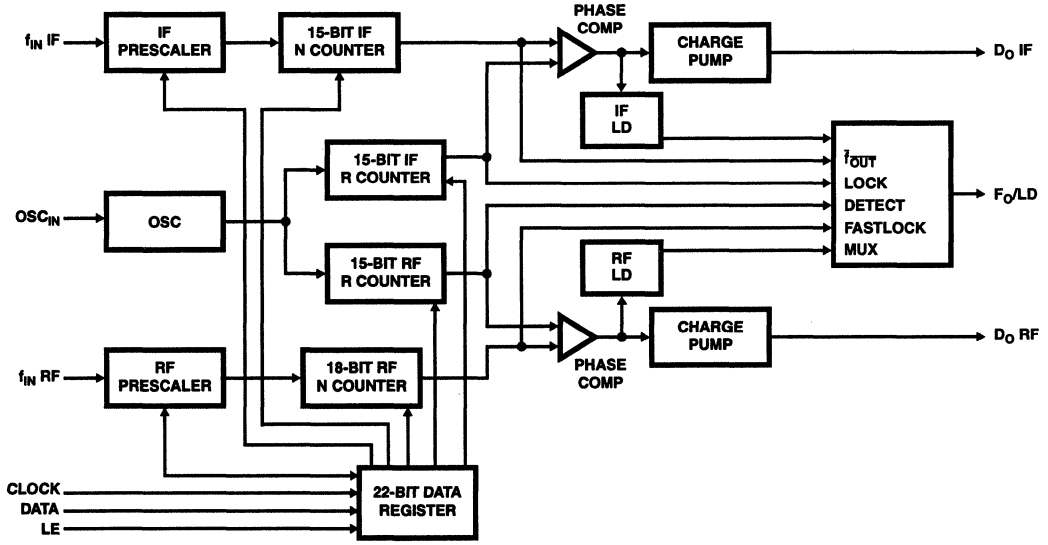
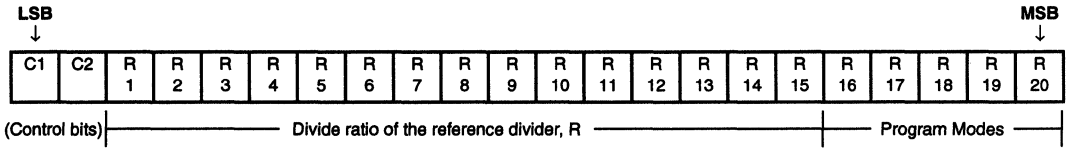


FIGURE 14. SIMPLIFIED BLOCK DIAGRAM

Programmable Reference Dividers (IF and RF R Counters)

If the Control Bits are 00 or 01 (00 for IF and 01 for RF) data is transferred from the 22-bit shift register into a latch which sets the 15-bit R Counter. Serial data format is shown below.



15-Bit Programmable Reference Divider Ratio (R Counter)

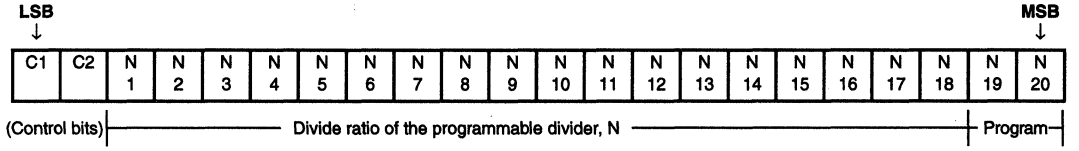
DIVIDE RATIO	R 15	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES:

8. Divide ratios less than 3 are prohibited.
9. Divide ratio: 3 to 32767.
10. R1 to R15: These bits select the divide ratio of the programmable reference divider.
11. Data is shifted in MSB first.

Programmable Divide (N Counter)

The N counter consists of the 7-bit swallow counter (A counter) and the 11-bit programmable counter (B counter). If the Control Bits are 10 or 11 (10 for IF counter and 11 for RF counter) data is transferred from the 22-bit shift register into a 4-bit or 7-bit latch (which sets the Swallow (A) Counter) and an 11-bit latch (which sets the 11-bit programmable (B) Counter), MSB first. Serial data format is shown below. For the IF N counter bits 5, 6, and 7 are don't care bits. The RF N counter does not have don't care bits.



7-Bit Swallow Counter Divide Ratio (A Counter)

RF

DIVIDE RATIO A	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

NOTES:

12. Divide ratio 0 to 127
13. B ≥ A

IF

DIVIDE RATIO A	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	X	X	X	0	0	0	0
1	X	X	X	0	0	0	1
•	•	•	•	•	•	•	•
15	X	X	X	1	1	1	1

X = Don't care condition

11-Bit Programmable Counter Divide Ratio (B Counter)

DIVIDE RATIO B	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

NOTES:

14. Divide ratio 3 to 2047 (divide ratios less than 3 are prohibited).
15. B ≥ A

Pulse Swallow Function

$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)

B: Preset divide ratio of binary 11-bit programmable counter (3 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \le A \le 127$ {RF}, $0 \le A \le 15$ {IF}, $A \le B$)

f_{OSC}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 15-bit programmable reference counter (3 to 32767)

P: Preset modulus of dual modulus prescaler (for IF: P = 8 or 16; for RF: P = 32 or 64)

Programmable Modes

Several modes of operation can be programmed with bits R16-R19 including the phase detector polarity, charge pump High Z State and the output of the F_O/LD pin. The prescaler and powerdown modes are selected with bits N19 and N20. The programmable modes are shown in Table 1. Truth table for the programmable modes and F_O/LD output are shown in Table 2 and Table 3.

TABLE 1. PROGRAMMABLE MODES

C1	C2	R16	R17	R18	R19	R20
0	0	IF Phase Detector Polarity	IF I_{CPO}	IF D_O High Z	IF LD	IF F_O
0	1	RF Phase Detector Polarity	RF I_{CPO}	RF D_O High Z	RF LD	RF F_O

C1	C2	N19	N20
1	0	IF Prescaler	Powerdown IF
1	1	RF Prescaler	Powerdown RF

TABLE 2. MODE SELECT TRUTH TABLE

	ΦD POLARITY	D_O HIGH Z STATE	(NOTE 16) I_{CPO}	IF PRESCALER	RF PRESCALER	(NOTE 17) POWERDOWN
0	Negative	Normal Operation	LOW	8/9	32/33	Powered Up
1	Positive	High Z State	HIGH	16/17	64/65	Powered Down

NOTES:

16. The I_{CPO} LOW current state = 1/4 x I_{CPO} HIGH current.
17. Activation of the IF PLL or RF PLL powerdown modes result in the disabling of the respective N counter divider and debiasing of its respective f_{IN} inputs (to a high impedance state). Powerdown forces the respective charge pump and phase comparator logic to a High Z State condition. The R counter functionality does not become disabled until both IF and RF powerdown bits are activated. The OSC_{IN} pin reverts to a high impedance state when this condition exists. The control register remains active and capable of loading and latching in data during all of the powerdown modes.

TABLE 3. THE F_O/LD (PIN 10) OUTPUT TRUTH TABLE

RF R [19] (RF LD)	IF R [19] (IF LD)	RF R [20] (RF F_O)	IF R [20] (IF F_O)	F_O OUTPUT STATE
0	0	0	0	Disabled (Note 18)
0	1	0	0	IF Lock Detect (Note 19)
1	0	0	0	RF Lock Detect (Note 19)
1	1	0	0	RF/IF Lock Detect (Note 19)
X	0	0	1	IF Reference Divider Output
X	0	1	0	RF Reference Divider Output
X	1	0	1	IF Programmable Divider Output
X	1	1	0	RF Programmable Divider Output
0	0	1	1	Fastlock (Note 20)
0	1	1	1	For Internal Use Only
1	0	1	1	For Internal Use Only
1	1	1	1	For Internal Use Only
1	1	1	1	Counter Reset (Note 21)

X = Don't care condition

NOTES:

18. When the F_OLD output is disabled, it is actively pulled to a low logic state.
19. Lock detect output provided to indicate when the VCO frequency is in "lock". When the loop is locked and a lock detect mode is selected, the pins output is HIGH, with narrow pulses LOW. In the RF/IF lock detect mode a locked condition is indicated when RF and IF are both locked.
20. The Fastlock mode utilizes the F_OLD output pin to switch a second loop filter damping resistor to ground during fastlock operation. Activation of Fastlock occurs whenever the RF loop's Icpo magnitude bit #17 is selected HIGH (while the #19 and #20 mode bits are set for Fastlock).
21. The Counter Reset mode bits R19 and R20 when activated reset all counters. Upon removal of the Reset bits, the N counter resumes counting in "close" alignment with the R counter. (The maximum error is one prescaler cycle.) If the Reset bits are activated, the R counter is also forced to Reset, allowing smooth acquisition upon powering up.

Phase Detector Polarity

Depending upon VCO characteristics, R16 bit should be set accordingly, (see Figure 15).

- When VCO characteristics are positive like (1), R16 should be set HIGH.
- When VCO characteristics are negative like (2), R16 should be set LOW.

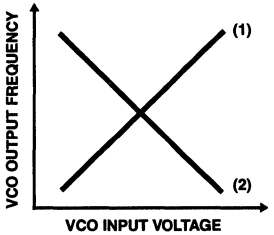
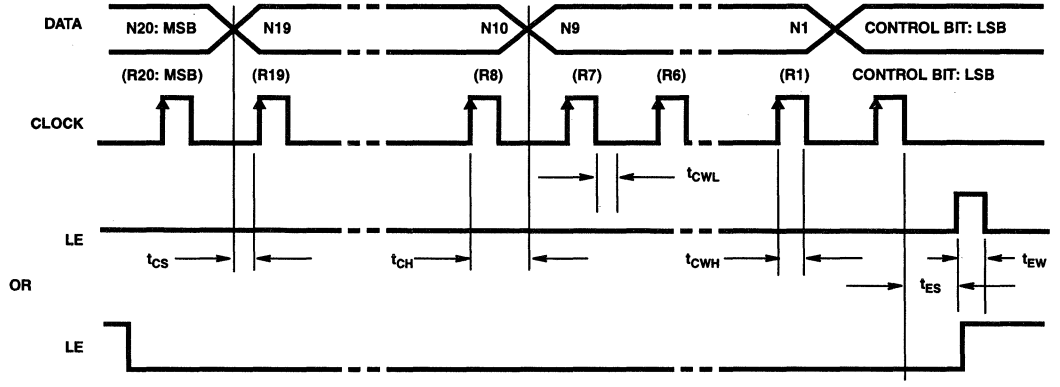


FIGURE 15. VCO CHARACTERISTICS

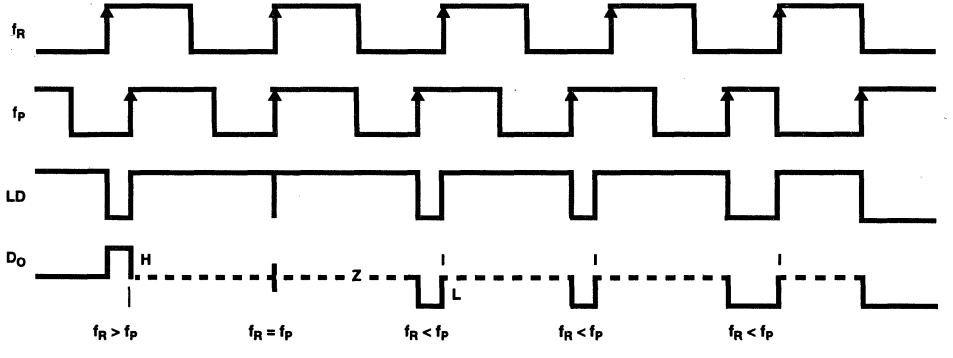


NOTES:

22. Parenthesis data indicates programmable reference divider data.
23. Data shifted into register on clock rising edge.
24. Data is shifted in MSB first.

Test Conditions: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6V/ns with amplitudes of 2.2V at V_{CC} = 2.7V and 2.6V at V_{CC} = 5.5V.

FIGURE 16. SERIAL DATA INPUT TIMING



NOTES:

25. Phase difference detection range: -2π to $+2\pi$
26. The minimum width pump up and pump down current pulses occur at the D_O pin when the loop is locked.
27. R16 = HIGH.

FIGURE 17. PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS

Typical Application Example

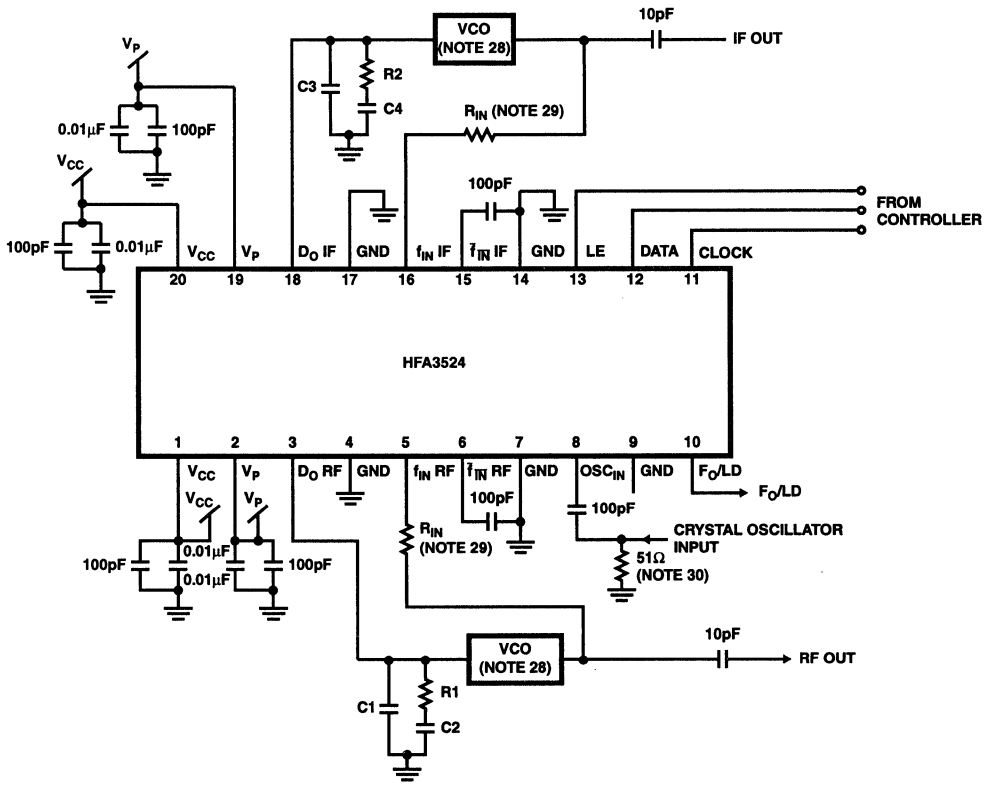


FIGURE 18.

NOTES:

28. VCO is assumed AC coupled.
29. R_{IN} increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10Ω to 200Ω depending on the VCO power level. f_{IN} RF impedance ranges from 40Ω to 100Ω. f_{IN} IF impedances are higher.
30. 50Ω termination is often used on test boards to allow use of external reference oscillator. For most typical products a CMOS clock is used and no terminating resistor is required. OSC_{IN} may be AC or DC coupled. AC coupling is recommended because the input circuit provides its own bias (see Figure 16).
31. Proper use of grounds and bypass capacitors is essential to achieve a high level of performance. Crosstalk between pins can be reduced by careful board layout.
32. This is a static sensitive device. It should be handled only at static free work stations.

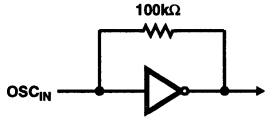


FIGURE 19.

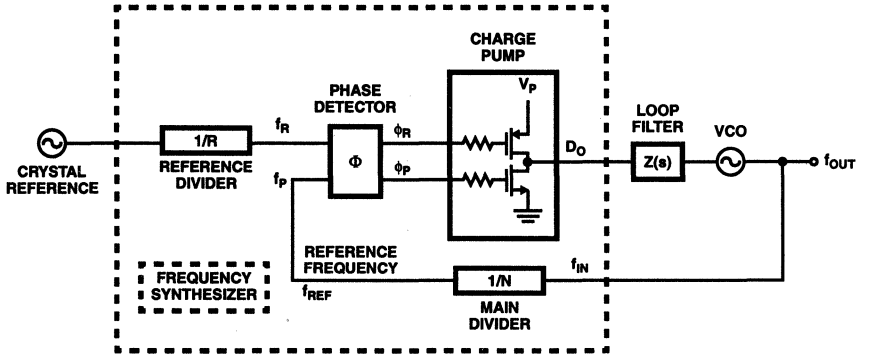


FIGURE 20. BASIC CHARGE PUMP PHASE LOCKED LOOP

Application Information

A block diagram of the basic phase locked loop is shown in Figure 20.

Loop Gain Equations

A linear control system model of the phase feedback for a PLL in the locked state is shown in Figure 21. The open loop gain is the product of the phase comparator gain (Kϕ), the VCO gain (K_{VCO}/s), and the loop filter gain Z(s) divided by the gain of the feedback counter modulus (N). The passive loop filter configuration used is displayed in Figure 22, while the complex impedance of the filter is given in Equation 2.

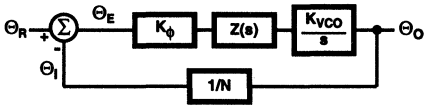


FIGURE 21. PLL LINEAR MODEL

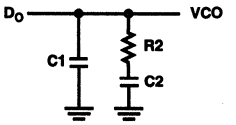


FIGURE 22. PASSIVE LOOP FILTER

$$\text{Open loop gain} = H(s)\,G(s) = \Theta_I/\Theta_E = K_\phi\,Z(s)\,K_{VCO}/Ns \quad \text{(EQ. 1)}$$

$$Z(s) = \frac{s(C2 \bullet R2) + 1}{s^2(C1 \bullet C2 \bullet R2) + sC1 + sC2} \quad \text{(EQ. 2)}$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as:

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad \text{(EQ. 3A)}$$

and

$$T2 = R2 \bullet C2 \quad \text{(EQ. 3B)}$$

The 3rd order PLL Open Loop Gain can be calculated in terms of frequency, ω, the filter time constants T1 and T2, and the design constants K_ϕ, K_{VCO}, and N.

$$|G(s) \bullet H(s)|_{s=j \bullet w} = \frac{-K\phi \bullet K_{VCO}(1 + j\omega \bullet T2)}{\omega^2 C1 \bullet N(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \quad \text{(EQ. 4)}$$

From Equation 3 we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in Equation 5.

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180^o \quad \text{(EQ. 5)}$$

A plot of the magnitude and phase of G(s)H(s) for a stable loop, is shown in Figure 23 with a solid trace. The parameter ϕ_P shows the amount of phase margin that exists at the point the gain drops below zero (the cutoff frequency wp of the loop). In a critically damped system, the amount of phase margin would be approximately 45 degrees.

If we were now to redefine the cut off frequency, wp', as double the frequency which gave us our original loop bandwidth, wp, the loop response time would be approximately halved. Because the filter attenuation at the comparison frequency also diminishes, the spurs would have increased by approximately 6dB. In the proposed Fastlock scheme, the higher spur levels and wider loop filter conditions would exist only during the initial lock-on phase - just long enough to reap the benefits of locking faster. The objective would be to open up the loop bandwidth but not introduce any additional complications or compromises related to our original design criteria. We would ideally like to momentarily shift the curve of Figure 23 over to a different cutoff frequency, illustrated by the dotted line, without affecting the relative open loop gain and phase relationships. To maintain the same gain/phase relationship at twice the original cutoff frequency, other terms in the gain and phase Equations 4 and 5 will have to compensate by the corresponding "1/w" or "$1/w^2$" factor. Examination of Equations 3 and 5 indicates the damping resistor variable R2 could be chosen to compensate the "w"

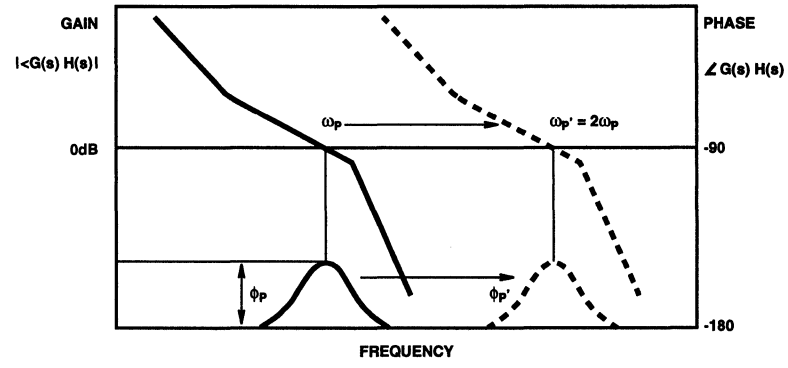


FIGURE 23. OPEN LOOP RESPONSE BODE PLOT

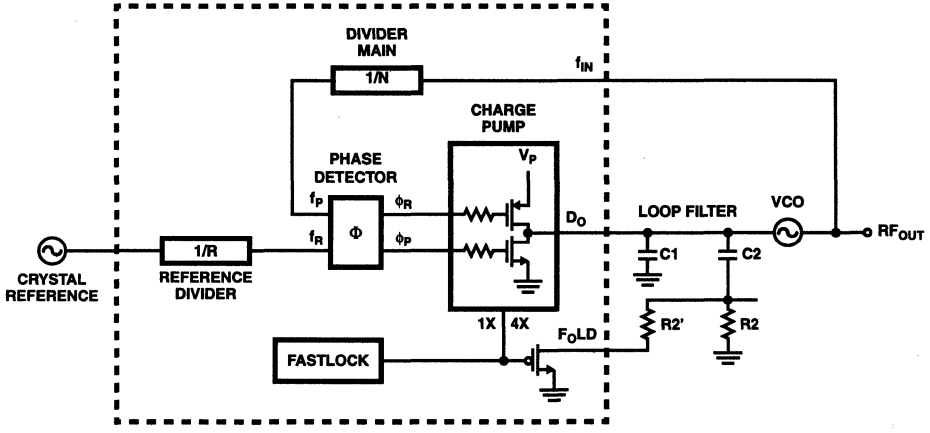


FIGURE 24. FASTLOCK PLL ARCHITECTURE

terms for the phase margin. This implies that another resistor of equal value to R2 will need to be switched in parallel with R2 during the initial lock period. We must also insure that the magnitude of the open loop gain, H(s)G(s) is equal to zero at wp' = 2wp. K_{VCO}, Kϕ, N, or the net product of these terms can be changed by a factor of 4, to counteract the w^2 term present in the denominator of Equation 3. The Kϕ term was chosen to complete the transformation because it can readily be switched between 1X and 4X values. This is accomplished by increasing the charge pump output current from 1mA in the standard mode to 4mA in Fastlock.

Fastlock Circuit Implementation

A diagram of the Fastlock scheme as implemented in Harris Semiconductors HFA3524 PLL is shown in Figure 24. When a new frequency is loaded, and the RF Icp_O bit is set high, the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error while an open drain NMOS on chip device switches in a second R2 resistor element to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second identical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations to account for. Once locked on the correct frequency, the user can return the PLL to standard low noise operation by sending an instruction with the RF Icp_O bit set low. This transition does not affect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless change between Fastlock and standard mode.

HARRIS SEMICONDUCTOR

HFA3624

January 1997

2.4GHz Up/Down Converter

Features

- Complete Receive/Transmit Front End
- RF Frequency Range . . . . . 2.4GHz to 2.5GHz
- IF Operation . . . . . 10MHz to 400MHz
- Single Supply Battery Operation . . . . . 2.7V to 5.5V
- Independent Receive/Transmit Power Enable Mode

Applications

- Systems Targeting IEEE 802.11 Standard
- PCMCIA Wireless Transceiver
- Wireless Local Area Network Modems
- TDMA Packet Protocol Radios
- Part 15 Compliant Radio Links
- Portable Battery Powered Equipment

Description

The Harris 2.4GHz PRISM™ chip set is a highly integrated five-chip solution for RF modems employing Direct Sequence Spread Spectrum (DSSS) signaling. The HFA3624 RF/IF converter is one of the five chips in the PRISM™ chip set (see Figure 1 for the typical application circuit).

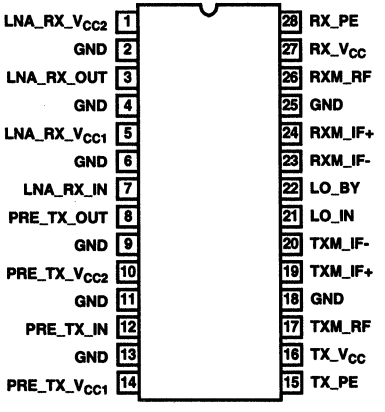
The HFA3624 Up/Down converter is a monolithic bipolar device for up/down conversion applications in the 2.4GHz to 2.5GHz range. Manufactured in the Harris UHF1X process, the device consists of a low noise amplifier and down conversion mixer in the receive section and an up conversion mixer with power preamp in the transmit section. An energy saving power enable control feature assures isolation between the receive and transmit circuits for time division multiplexed systems. The device requires low drive levels from the local oscillator and is housed in a small outline 28 lead SSOP package ideally suited for PCMCIA card applications.

Ordering Information

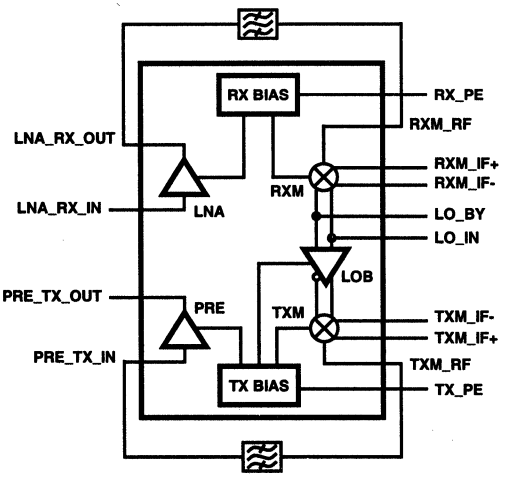
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA3624IA	-40 to 85	28 Ld SSOP	M28.15
HFA3624IA96	-40 to 85	Tape and Reel	

Pinout

HFA3624
(SSOP)
TOP VIEW



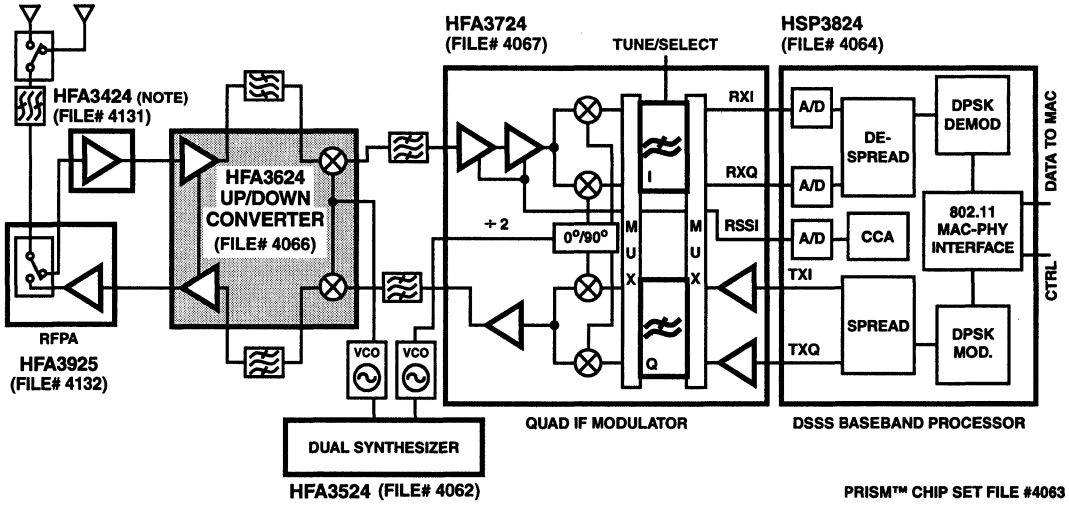
Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

PRISM™ and the PRISM™ logo are trademarks of Harris Corporation.

File Number 4066.6



NOTE: Required for systems targeting 802.11 specifications.

FIGURE 1. TYPICAL TRANSCEIVER APPLICATION CIRCUIT USING THE HFA3624

For additional information on the PRISM™ chip set, call (407) 724-7800 to access Harris' AnswerFAX system. When prompted, key in the four-digit document number (File #) of the datasheets you wish to receive. The four-digit file numbers are shown in Figure 1, and correspond to the appropriate circuit.

Absolute Maximum Ratings

Supply Voltage ..... -0.3V to +6.0V
Voltage on Any Other Pin ..... -0.3 to V_{CC} +0.3V

Operating Conditions

Supply Voltage Range ..... 2.7V to 5.5V
Temperature Range ..... $-40^{o}C \le T_A \le 85^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^{o}C/W$)
28 Lead Plastic SSOP	88

Package Power Dissipation at 70°C
28 Lead Plastic SSOP 0.9W
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... $-65^{o}C \le T_A \le 150^{o}C$
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{CC} = +2.7V, LO = 2170MHz, IF = 280MHz, RF = 2450MHz, Z_O = 50Ω, Unless Otherwise Specified

PARAMETER	SYMBOL	TEMP (°C)	ALL GRADES MIN	ALL GRADES TYP	ALL GRADES MAX	UNITS
LO INPUT CHARACTERISTICS (LO_IN = 2170MHz/-3dBm, RS_{LO} = 50Ω, tested in both RX and TX modes, all unused inputs and outputs are terminated into 50Ω)						
LO Input Frequency Range	LO_f	25	2.0	-	2.49	GHz
LO Input Drive Level	LO_dr	25	-6	-3	3	dBm
LO Input VSWR	LO_SWR	25	-	1.18:1	2.0:1	-
RECEIVE LNA CHARACTERISTICS (LNA_RX_IN = 2450MHz/-25dBm, RS = RL = 50Ω, Receive Mode)						
Receive LNA Frequency Range	LNA_f	25	2.4	-	2.5	GHz
LNA Noise Figure	LNA_NF	25	-	3.5	-	dB
LNA Power Gain	LNA_PG	25	13.5	15.5	-	dB
LNA Reverse Isolation (Source = 2450MHz/-25dBm)	LNA_ISO	25	-	30	-	dB
LNA Output 3rd Order Intercept (LNA_RX_IN = 2449.9MHz, 2450.1MHz / -35dBm)	LNA_IP3	25	-	18	-	dBm
LNA Output 1dB Compression	LNA_P1D	25	-	5.5	-	dBm
LNA Input VSWR	LNA_ISWR	25	-	1.85:1	2.2:1	-
LNA Input Return Loss	LNA_IRL	25	-	10.5	8.5	dB
LNA Output VSWR	LNA_OSWR	25	-	1.33:1	2.0:1	-
LNA Output Return Loss	LNA_ORL	25	-	17.0	9.5	dB
RECEIVE MIXER CHARACTERISTICS (LO_IN = 2170MHz/-3dBm, RXM_RF = 2450MHz/-25dBm, RS_{LO} = 50Ω, RS_{RF} = 50Ω, RL_{IF} = 50Ω with external matching network (Note 2), Receive Mode)						
Mixer RF Frequency Range	RXM_RFf	25	2.4	-	2.5	GHz
Mixer IF Frequency Range	RXM_IFf	25	10	-	400	MHz
SSB Noise Figure (Note 3)	RXM_NF	25	-	15	-	dB
Mixer Power Conversion Gain (Note 2)	RXM_PG	25	4	6	-	dB
Mixer IF Output 3rd Order Intercept (RXM_RF = 2449.9MHz, 2450.1MHz/-30dBm)	RXM_IP3	25	-	4.0	-	dBm
Mixer IF Output 1dB Compression	RXM_P1D	25	-	-5	-	dBm
Mixer RF Input VSWR (2.4GHz to 2.5GHz)	RXM_SWR	25	-	1.5:1	2.0:1	-
Mixer RF Input Return Loss	RXM_IRL	25	-	14.0	9.5	dB

Electrical Specifications V_{CC} = +2.7V, LO = 2170MHz, IF = 280MHz, RF = 2450MHz, Z_O = 50Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEMP (°C)	ALL GRADES			UNITS
			MIN	TYP	MAX	
IF Open Collector Output Resistance (IF = 280MHz)	RXM_ROUT	25	-	1.5	-	kΩ
IF Open Collector Output Capacitance	RXM_COUT	25	-	0.4	-	pF
Mixer LO to RF Isolation	RXA_LOR	25	-	22	-	dB
RECEIVE LNA/MIXER CASCADED CHARACTERISTICS (-3dB Loss RF Image Filter between LNA and Mixer, LNA_RX_IN = 2450MHz/-25dBm, RL_{IF} = 250Ω external matching network, (Note 6))						
Cascaded Noise Figure	CRX_NF	25	-	6.24	-	dB
Cascaded Power Gain	CRX_PG	25	15	18	-	dB
Cascaded Input IP3	CRX_IP3	25	-	-14.1	-	dBm
Cascaded Input Compression Point	CRX_P1D	25	-	-23.2	-	dBm
Maximum Input Power (Output may be gain compressed, but functional)	CRX_dr	25	-	-4	-	dBm
TRANSMIT MIXER CHARACTERISTICS (LO_IN = 2170MHz/-3dBm, TXM_IF+ = 280MHz/-13dBm, RS_{IF} = 50Ω, RS_{LO} = 50Ω, RL_{RF} = 50Ω, Transmit Mode)						
IF Input Frequency Range	TXM_IFf	25	10	-	400	MHz
IF Input Resistance (IF = 280MHz)	TXM_RIN	25	-	3	-	kΩ
IF Input Capacitance (IF = 280MHz)	TXM_CIN	25	-	0.5	-	pF
Power Conversion Gain (RS_{IF} = 50Ω)	TXM_PG50	25	-6	-3.4	-	dB
Power Conversion Gain (RS_{IF} = 250Ω) (Notes 4, 5)	TXM_PG250	25	-0.5	2.1	-	dB
Transmit Mixer LO Leakage	TXM_LEAK	25	-	-20	-18	dBm
RF Output Frequency Range	TXM_RFf	25	2.4	-	2.5	GHz
TXM_RF VSWR (2.4GHz to 2.5GHz)	TXM_OSWR	25	-	1.25:1	2.0:1	-
TXM_RF Return Loss	TXM_ORL	25	-	19.0	9.5	dB
Mixer Output 1dB Compression	TXM_P1D	25	-	-10.5	-	dBm
Output SSB Noise Figure (RS_{IF} = 50Ω)	TXM_NF50	25	-	18.3	-	dB
Output 3rd Order Intercept (RS_{IF} = 50Ω)	TXM_IP3_50	25	-	1.1	-	dBm
Output SSB Noise Figure (RS_{IF} = 250Ω)	TXM_NF250	25	-	14.5	-	dB
Output 3rd Order Intercept (RS_{IF} = 250Ω)	TXM_IP3_250	25	-	-1.5	-	dBm
TRANSMIT POWER PRE-AMP CHARACTERISTICS (PRE_IN = 2450MHz/-13dBm, RS = RL = 50Ω, Transmit Mode)						
Power Pre-Amp Frequency Range	PRE_f	25	2.4	-	2.5	GHz
Power Gain	PRE_PG	25	10.8	12.3	-	dB
PRE_AMP Output 1dB Compression	PRE_P1D	25	-	5.6	-	dBm
PRE_AMP Noise Figure	PRE_NF	25	-	5.7	-	dB
PRE_AMP Output 3rd Order Intercept	PRE_IP3	25	-	15.3	-	dBm
PRE_AMP Input VSWR (2.4GHz to 2.5GHz)	PRE_ISWR	25	-	1.3:1	2.0:1	-
PRE_AMP Input Return Loss	PRE_IRL	25	-	17.7	9.5	dB
PRE_AMP Output VSWR (2.4GHz to 2.5GHz)	PRE_OSWR	25	-	1.3:1	2.0:1	-
PRE_AMP Output Return Loss	PRE_ORL	25	-	17.7	9.5	dB

Electrical Specifications V_{CC} = +2.7V, LO = 2170MHz, IF = 280MHz, RF = 2450MHz, Z_O = 50Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEMP (°C)	ALL GRADES MIN	ALL GRADES TYP	ALL GRADES MAX	UNITS
TRANSMIT MIXER/POWER PRE-AMP CASCADED CHARACTERISTICS (TXM_IF+ = 280MHz/-13dBm, -3dB Loss RF Image Filter with no LO suppression between Mixer and Transmit Amp, RL = 50Ω, RS_{IF} = 250Ω (Note 6))						
Cascaded Power Gain	CTX_PG	25	8	11.4	-	dB
Cascaded Output P1dB	CTX_P1D	25	-	-2.0	-	dBm
Cascaded Output NF	CTX_NF	25	-	15	-	dB
Cascaded Output 3rd Order Intercept	CTX_IP3	25	-	7.1	-	dBm
Cascaded LO Leakage	CTX_LEAK	25	-	-8.7	-	dBm
POWER SUPPLY AND LOGIC CHARACTERISTICS						
Voltage Supply Range	V_{CC}	25	2.7	-	5.5	V
Transmit Mode Supply Current (V_{CC} = 2.7V)	$TX\_2.7I_{CC}$	25	46	49	52	mA
		Full	-	64	-	mA
Receive Mode Supply Current (V_{CC} = 2.7V)	RX_I_{CC}	25	15.5	18	20.5	mA
		Full	-	22.5	-	mA
Power Down Current (V_{CC} = 5.5V)	I_{CC}_PD	Full	-	0.3	10	µA
Logic Input Low Level	V_{IL}	Full	-0.2	-	0.8	V
Logic Input High Level	V_{IH}	Full	2.0	-	V_{CC}	V
Logic Low Input Bias Current (V_{PE} = 0V, V_{CC} = 5.5V)	I_B_LO	Full	-	-	1	µA
Logic High Input Bias Current (V_{PE} = 5.5V, V_{CC} = 5.5V)	I_B_HI	Full	-	50	150	µA
TX/RX Power Enable Time (Note 7)	PEt	Full	-	0.25	1	µs
TX/RX Power Disable Time (Note 7)	PDt	Full	-	0.25	1	µs

NOTES:

2. See Figure 5 Test Circuit for 50Ω IF matching network component values.
3. SSB (Single Side Band) Noise Figure measurement requires the use of an IF Reject/Highpass Filter between the Noise Source and the RXM_RF port. This filter prevents IF input noise from interfering with the Mixer IF output Noise Figure Measurement.
4. Transmit mixer measured with Impedance Transform Network 250Ω at device to 50Ω at the source. Refer to Figure 5, pin 19.
5. Implied limit, production measurement uses 50Ω termination at pin 19 (RS_{IF} = 50Ω). Typical transmit conversion gain increase of 5.5dB with application circuit Figure 5 (RS_{IF} = 250Ω).
6. See Figure 2 for Typical Application Circuit.
7. Enable/Disable Time Specifications are tested with the external component values shown in the Figure 5 Test Circuit, with an IF frequency of 280MHz. Specifically the AC coupling capacitors on the TXM_IF+ and TXM_IF- pins are biased up to operating voltage from a fixed internal current source at power up. Increasing these AC coupling capacitors above 1000pF will slow Enable Time proportionately.

POWER CONTROL TRUTH TABLE

STATE	RX_PE	TX_PE
Power Down (Receive/Transmit Channels Power Down)	Low	Low
Transmit Mode (Receive Channel Power Down)	Low	High
Receive Mode (Transmit Channel Power Down)	High	Low
Not Recommended	High	High

Pin Description

PINS	SYMBOL	DESCRIPTION
1	LNA_RX_V_{CC2}	Receive Channel Low Noise Amplifier Output Stage Positive Power Supply. Use high quality decoupling capacitors right at the pin. A 5pF chip capacitor is recommended.
3	LNA_RX_OUT	Receive Channel Low Noise Amplifier Output (2400MHz to 2500MHz). The nominal impedance of 50Ω, over the operating frequency range, is achieved with an on chip narrowband tuned circuit. This pin requires AC coupling.
5	LNA_RX_V_{CC1}	Receive Channel Low Noise Amplifier Input Stage Positive Power Supply. Use high quality decoupling capacitors right at the pin. A 200pF chip capacitor is recommended.
7	LNA_RX_IN	Receive Channel Low Noise Amplifier Input (2400MHz to 2500MHz). The nominal impedance of 50Ω, over the operating frequency range, is achieved with an on chip narrowband tuned circuit. This pin requires AC coupling.
8	PRE_TX_OUT	Transmit Channel Power Pre-Amplifier Output (2400MHz to 2500MHz). The nominal impedance of 50Ω, over the operating frequency range, is achieved with on chip narrowband tuned circuit. This pin requires AC coupling.
10	PRE_TX_V_{CC2}	Transmit Channel Power Pre-Amplifier Output Stage Positive Power Supply. Use high quality decoupling capacitors right at the pin. A 200pF chip capacitor is recommended.
12	PRE_TX_IN	Transmit Channel Power Pre-Amplifier Input (2400MHz to 2500MHz). The nominal impedance of 50Ω, over the operating frequency range, is achieved with an on chip narrowband tuned circuit. This pin requires AC coupling.
14	PRE_TX_V_{CC1}	Transmit Channel Power Pre-Amplifier Input Stage Positive Power Supply. Use high quality decoupling capacitors right at the pin. A 200pF chip capacitor is recommended.
15	TX_PE	Transmit Channel Power Enable Control Input. TTL compatible input. Refer to "Power Control Truth Table" on previous page.
16	TX_V_{CC}	Transmit Channel Positive Power Supply. Use high quality decoupling capacitors right at the pin. A 200pF chip capacitor is recommended.
17	TXM_RF	Transmit Channel Mixer RF Output (2400MHz to 2500MHz). The nominal impedance of 50Ω, over the operating frequency range, is achieved with an on chip narrowband tuned circuit. This pin requires AC coupling.
19	TXM_IF+	Transmit Channel Mixer IF+ Input (10MHz to 400MHz). The TXM_IF+ and TXM_IF- pins form a high input impedance differential pair. Either input (or both inputs for special applications) may be used for the IF signal. Typically the TXM_IF- pin is bypassed to ground with a 470pF capacitor and the TXM_IF+ pin is AC coupled to the transmit IF signal. The high impedance input requires external termination. The specified input impedance is modeled as a resistor in parallel with a capacitor derived from S parameters at 280MHz. The input Impedance will increase at lower IF frequencies. This pin requires AC coupling. Increasing the AC coupling capacitor to larger than 1000pF will degrade Transmit Enable Time.
20	TXM_IF-	Transmit Channel Mixer IF- Input (10MHz to 400MHz). The TXM_IF+ and TXM_IF- pins form a high input impedance differential pair. Either input (or both for special applications) may be used for the IF signal. Typically the TXM_IF- pin is bypassed to ground with a 470pF capacitor and the TXM_IF+ pin is AC coupled to the transmit IF signal. The high impedance input requires external termination. The specified input impedance is modeled as a resistor in parallel with a capacitor derived from S parameters at 280MHz. The input impedance will increase at lower IF frequencies. This pin requires AC coupling. Increasing the AC coupling capacitor to larger than 1000pF will degrade Transmit Enable Time.
21	LO_IN	Local Oscillator Input (2000MHz to 2490MHz). The LO_IN and LO_BY pins form a differential pair with a mutual broadband 50Ω impedance. Refer to the LO_BY pin for details. The recommended LO power is -3dBm, however usable performance is obtained for the range -6dBm to +3dBm. The LO_IN pin requires AC coupling.
22	LO_BY	Local Oscillator Input Bypass (2000MHz to 2490MHz). The LO_IN and LO_BY pins form a differential pair with a mutual broadband 50Ω input impedance. The LO_BY pin can be used as a signal input, but may have slightly degraded performance due to a clamp circuit to GND. Typically the LO_BY pin is bypassed to GND with a 5pF capacitor. The LO_BY pin requires AC coupling.

Pin Description (Continued)

PINS	SYMBOL	DESCRIPTION
23	RXM_IF-	Receive Channel Mixer IF- Output (10MHz to 400MHz). The RXM_IF+ and RXM_IF- pins form a complimentary open collector output driver pair. The open collector outputs require an external load to V_{CC} not to exceed 500Ω, for the Single Ended IF case shown in Figure 3, or 1kΩ for the Differential IF cases shown in Figures 2 and 4. This pin requires AC coupling.
24	RXM_IF+	Receive Channel Mixer IF+ Output (10MHz to 400MHz) The RXM_IF+ and RXM_IF- pins form a complimentary open collector output driver pair. The open collector outputs require an external load to V_{CC} not to exceed 500Ω, for the Single Ended IF case shown in Figure 3, or 1kΩ for the Differential IF cases shown in Figures 2 and 4. This pin requires AC coupling.
26	RXM_RF	Receive Channel Mixer RF Input (2400MHz to 2500MHz). The nominal impedance of 50Ω, over the operating frequency range, is achieved with an on chip narrowband tuned circuit. This pin requires AC coupling.
27	RX_V_{CC}	Receive Channel Positive Power Supply. Use high quality decoupling capacitors right at the pin. A 200pF chip capacitor is recommended.
28	RX_PE	Receive Channel Power Enable Control Input. TTL compatible input. Refer to "Power Control Truth Table" on previous page.
2, 4, 6, 9, 11, 13, 18, 25	GND	Circuit Ground Pins (Qty 8). Internally connected.

Typical Application Circuits

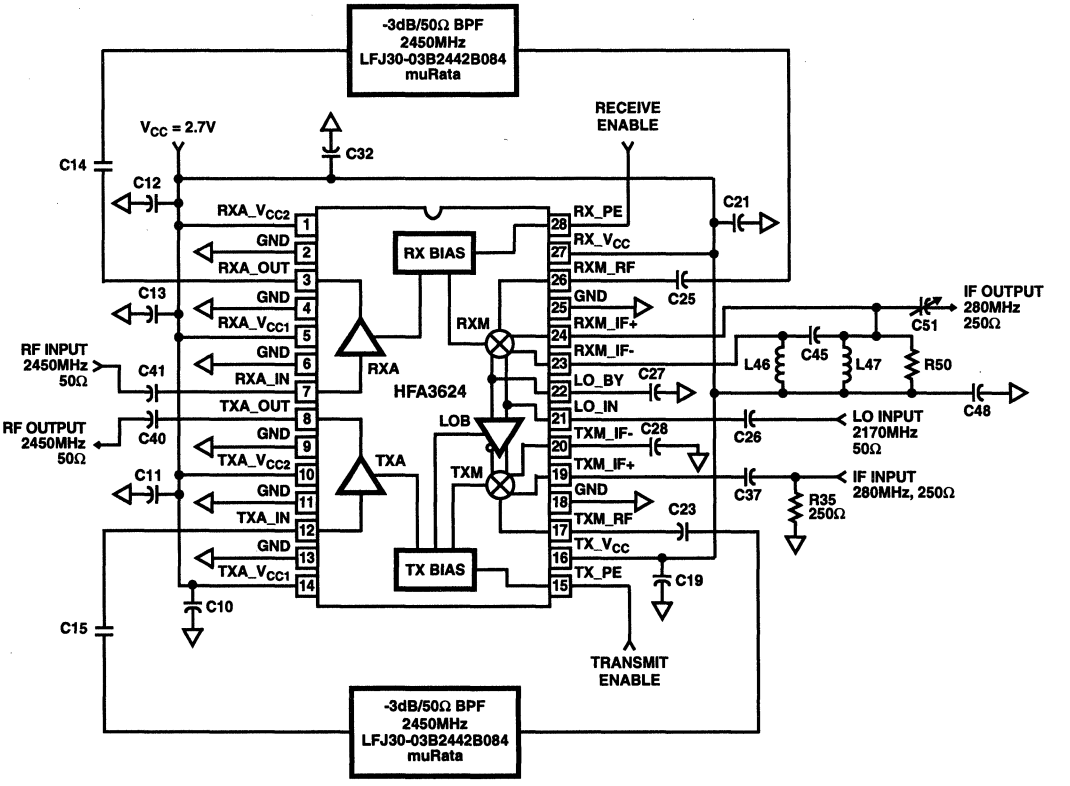


FIGURE 2. DIFFERENTIAL TO SINGLE ENDED IF OUTPUT TRANSLATION WITH 250Ω IF IMPEDANCE

Typical Application Circuits (Continued)

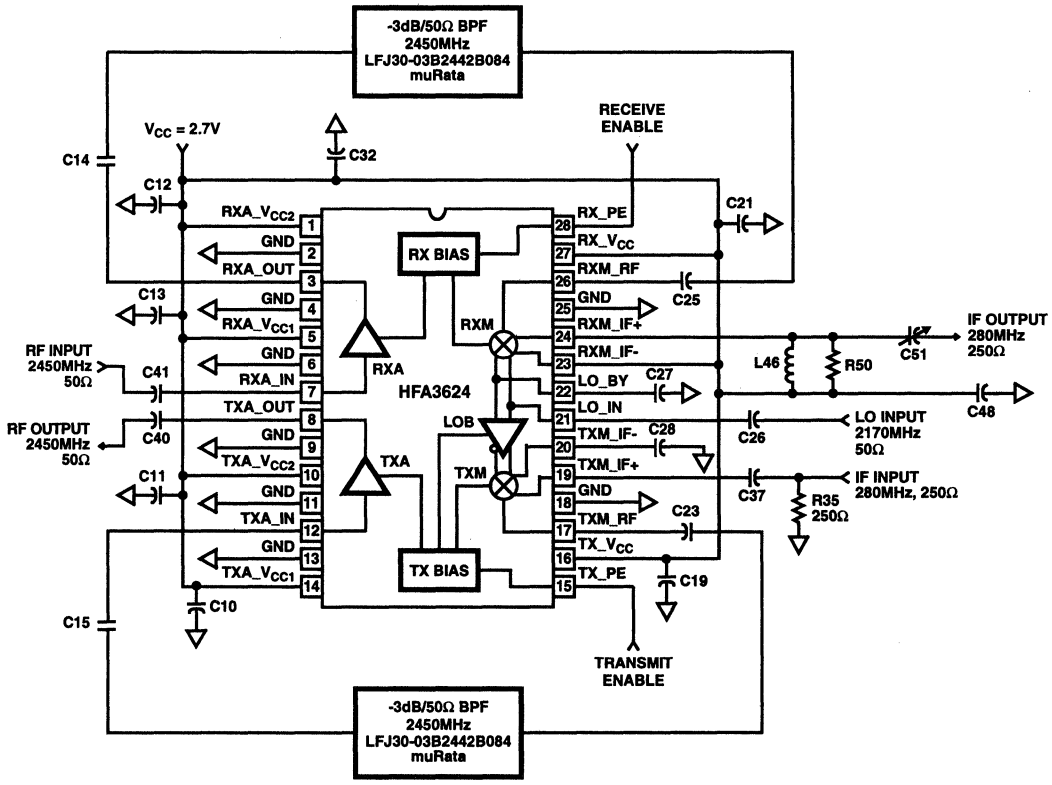


FIGURE 3. SINGLE ENDED IF OUTPUT WITH 250Ω IF IMPEDANCE

Typical Application Circuits (Continued)

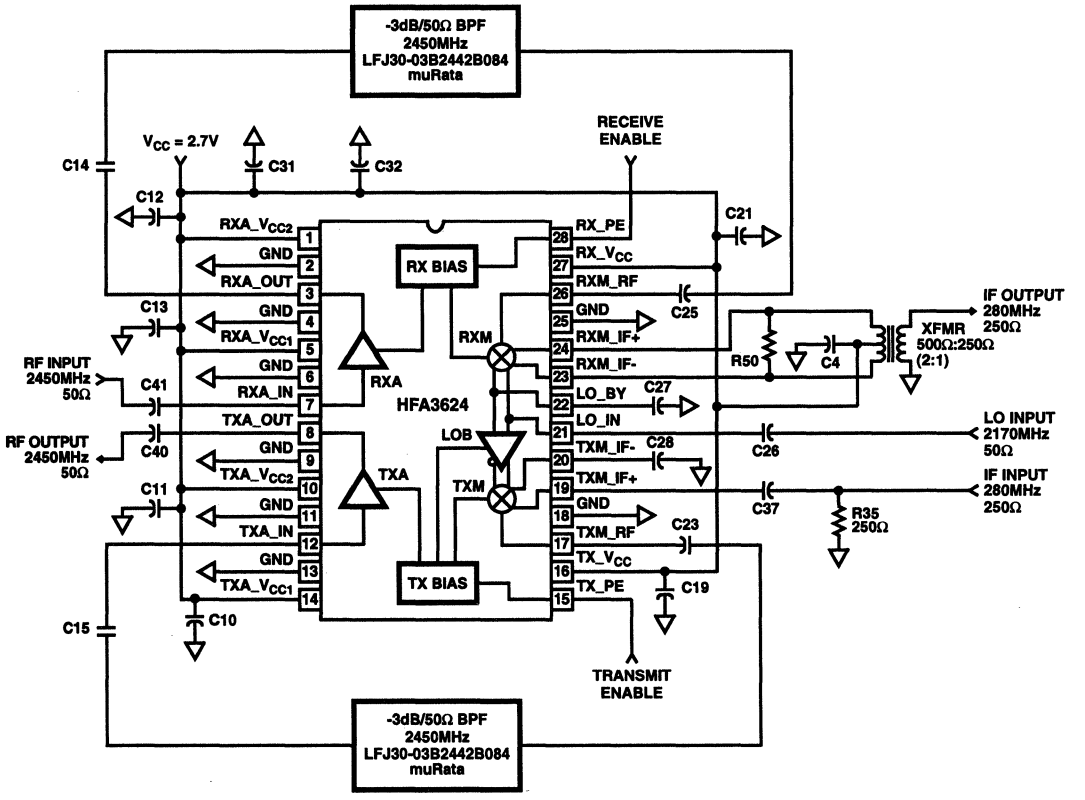


FIGURE 4. DIFFERENTIAL TO SINGLE ENDED IF OUTPUT TRANSLATION USING TRANSFORMER INTO 250Ω

Typical Application Circuits (Continued)

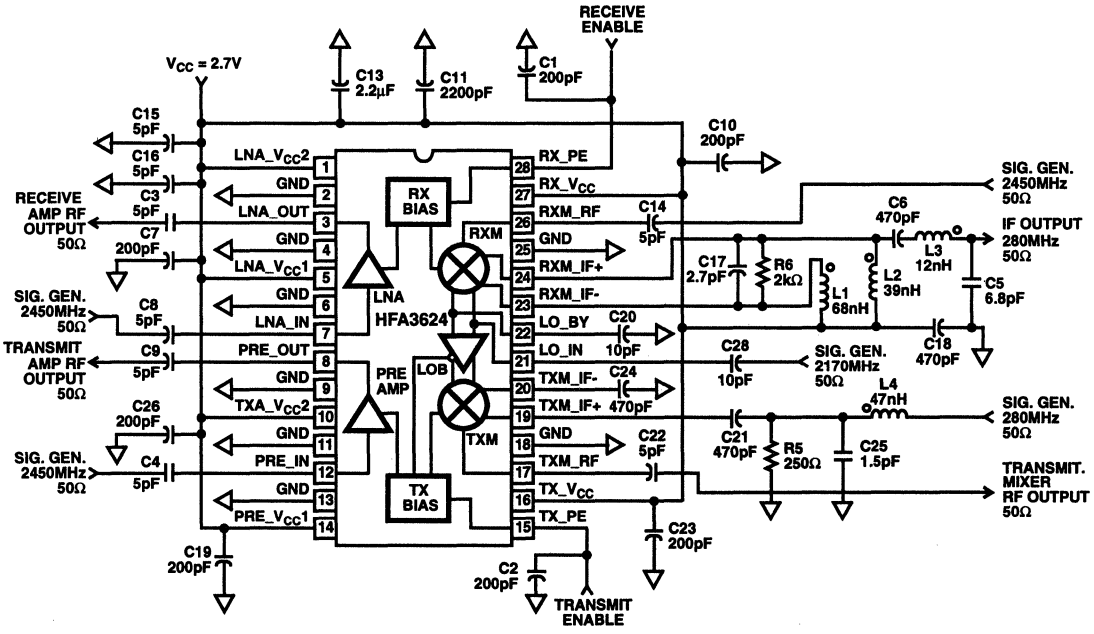


FIGURE 5. OPTIMIZED LAB EVALUATION CIRCUIT

Typical Performance Curves

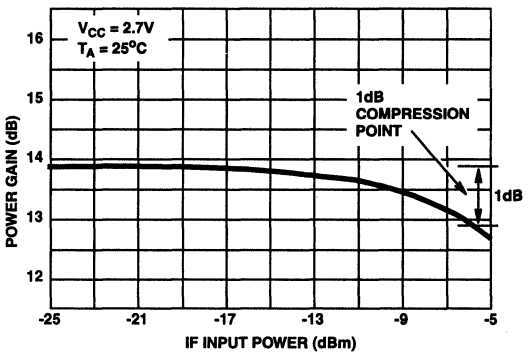


FIGURE 6. TRANSMIT PRE-AMP 1dB COMPRESSION

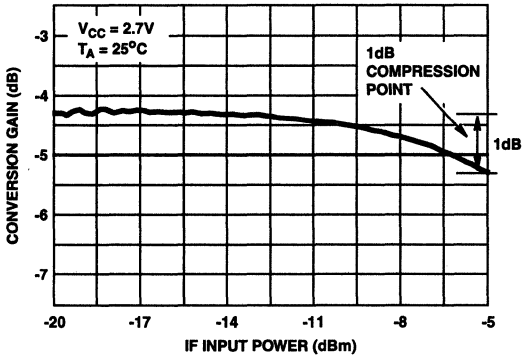


FIGURE 7. TRANSMIT MIXER 1dB COMPRESSION

Typical Performance Curves (Continued)

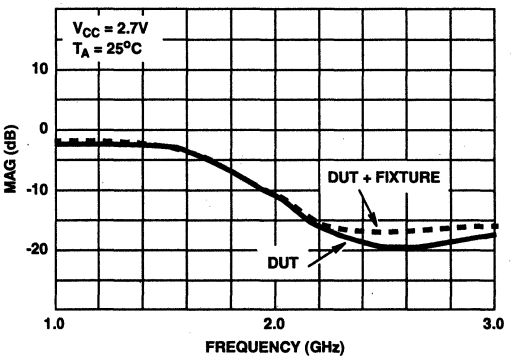


FIGURE 8. PRE-AMPLIFIER S_{11} LOG MAG INPUT RETURN LOSS

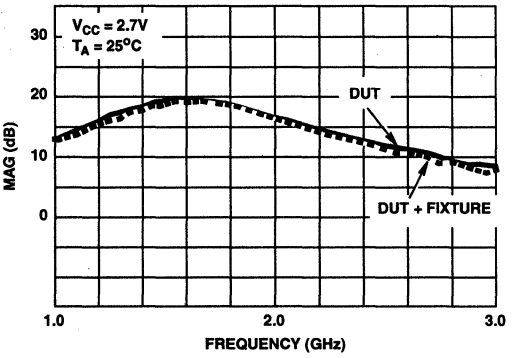


FIGURE 9. PRE-AMPLIFIER S_{21} LOG MAG FORWARD GAIN

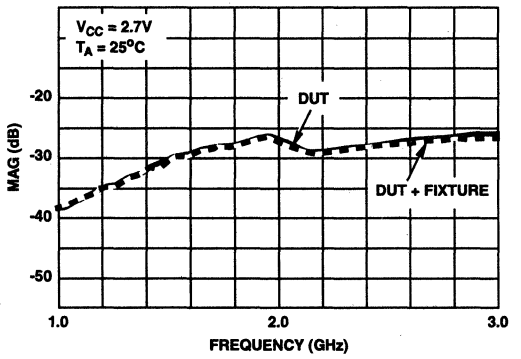


FIGURE 10. PRE-AMPLIFIER S_{12} LOG MAG REVERSE ISOLATION

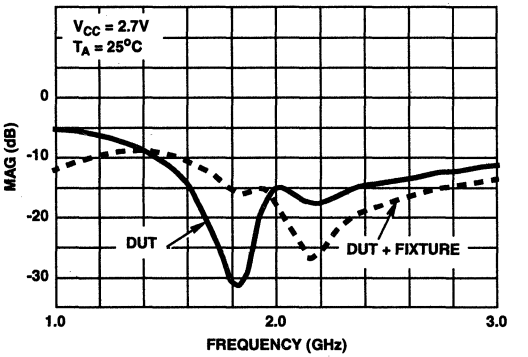


FIGURE 11. PRE-AMPLIFIER S_{22} LOG MAG OUTPUT RETURN LOSS

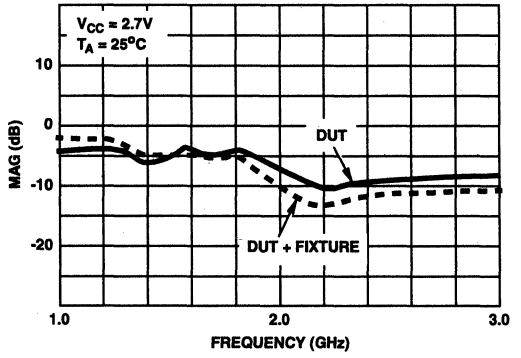


FIGURE 12. LNA S_{11} LOG MAG INPUT RETURN LOSS

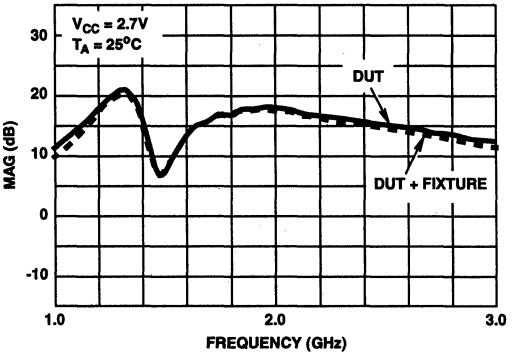


FIGURE 13. LNA S_{21} LOG MAG FORWARD GAIN

Typical Performance Curves (Continued)

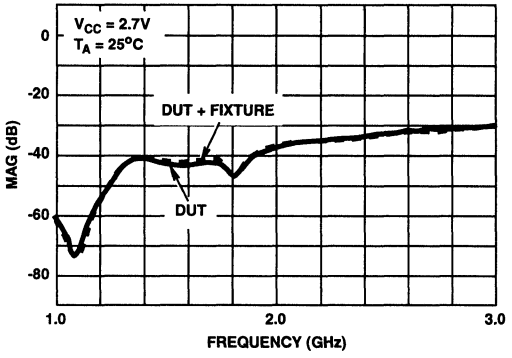


FIGURE 14. LNA S_{12} LOG MAG REVERSE ISOLATION

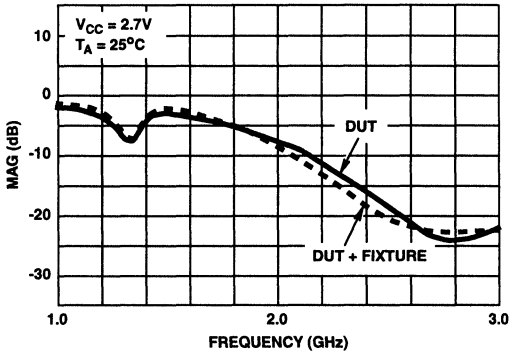


FIGURE 15. LNA S_{22} LOG MAG OUTPUT RETURN LOSS

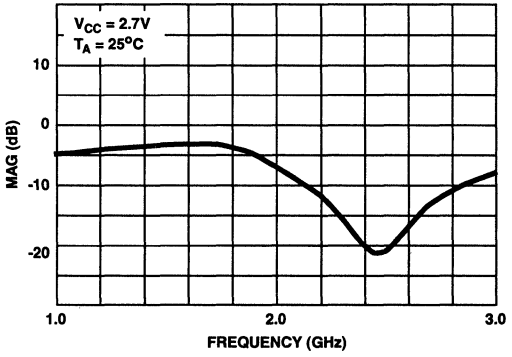
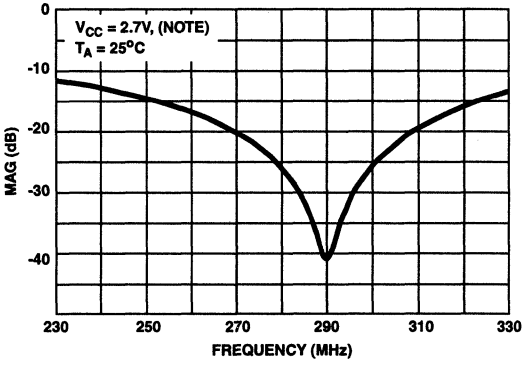
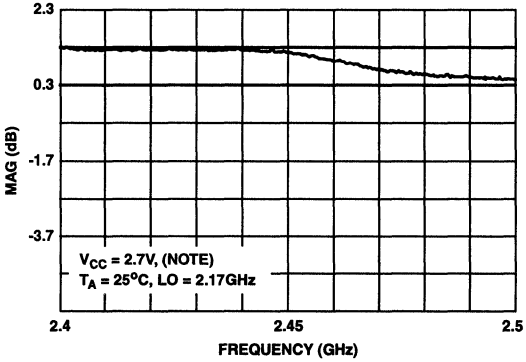


FIGURE 16. TRANSMIT MIXER S_{22} LOG MAG RF OUTPUT RETURN LOSS



NOTE: Transmit mixer measured with Impedance Transform Network 250Ω at device to 50Ω at the source. Refer to Figure 5, pin 19.

FIGURE 17. TRANSMIT MIXER S_{11} LOG MAG IF INPUT RETURN LOSS



NOTE: Transmit mixer measured with Impedance Transform Network 250Ω at device to 50Ω at the source. Refer to Figure 5, pin 19.

FIGURE 18. TRANSMIT MIXER CONVERSION GAIN vs IF FREQUENCY SWEEP

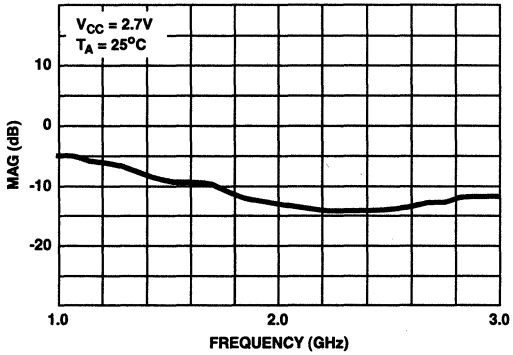


FIGURE 19. RECEIVE MIXER S_{11} LOG MAG RF INPUT RETURN LOSS

Typical Performance Curves (Continued)

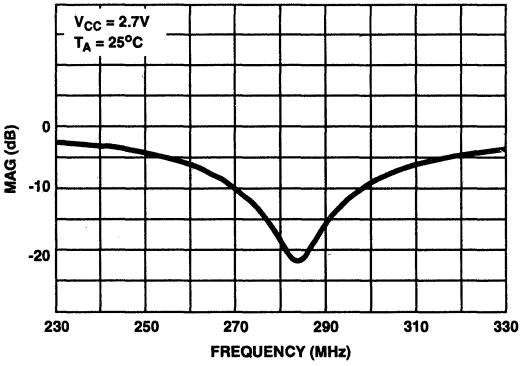


FIGURE 20. RECEIVE MIXER S_{22} LOG MAG IF OUTPUT RETURN LOSS

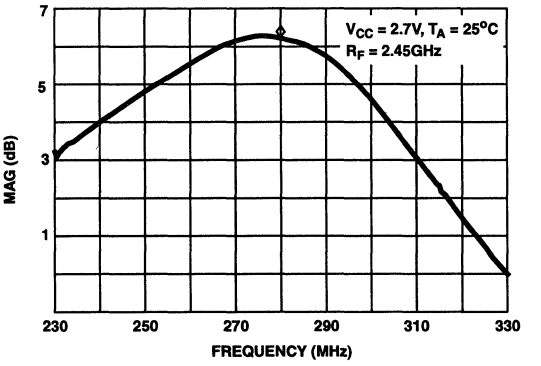


FIGURE 21. RECEIVE MIXER CONVERSION GAIN vs LO FREQUENCY SWEEP

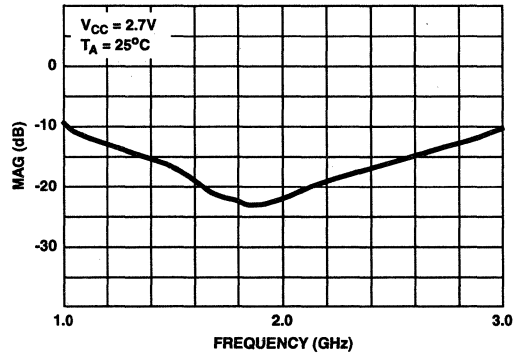


FIGURE 22. LO_IN S_{11} LOG MAG RECEIVE MODE LO INPUT RETURN LOSS

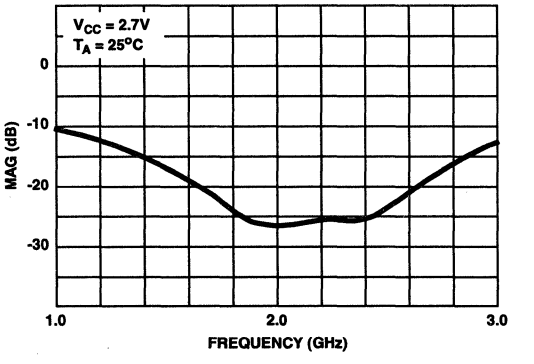


FIGURE 23. LO_IN S_{11} LOG MAG TRANSMIT MODE LO INPUT RETURN LOSS

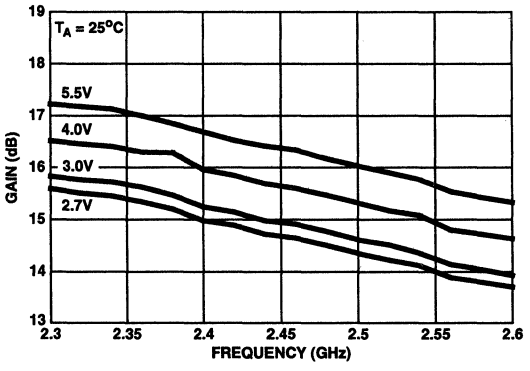


FIGURE 24. LOW NOISE AMPLIFIER GAIN vs FREQUENCY

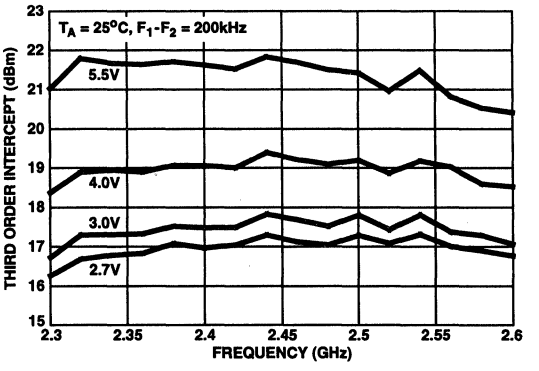


FIGURE 25. LOW NOISE AMPLIFIER IP3 vs FREQUENCY

Typical Performance Curves (Continued)

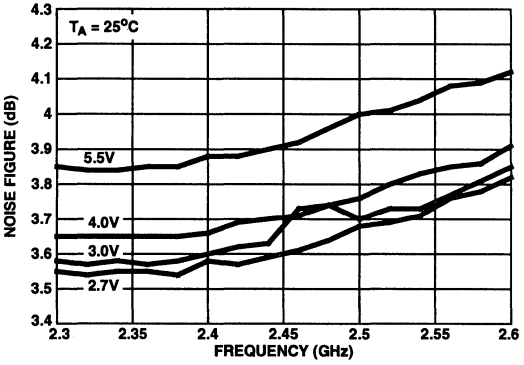


FIGURE 26. LOW NOISE AMPLIFIER NOISE FIGURE vs FREQUENCY

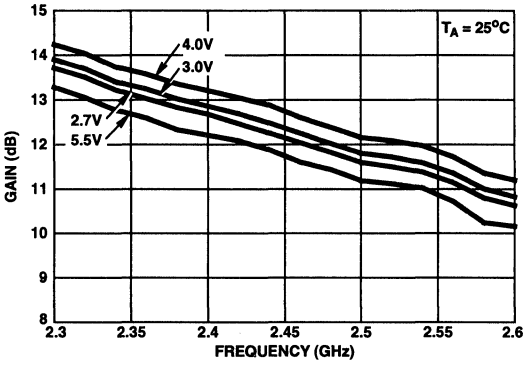


FIGURE 27. PRE-AMPLIFIER GAIN vs FREQUENCY

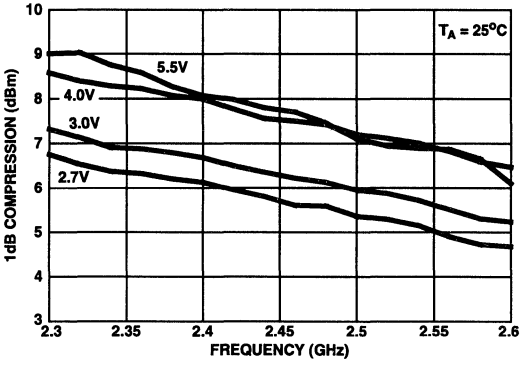


FIGURE 28. PRE-AMPLIFIER RF OUTPUT 1dB COMPRESSION vs FREQUENCY

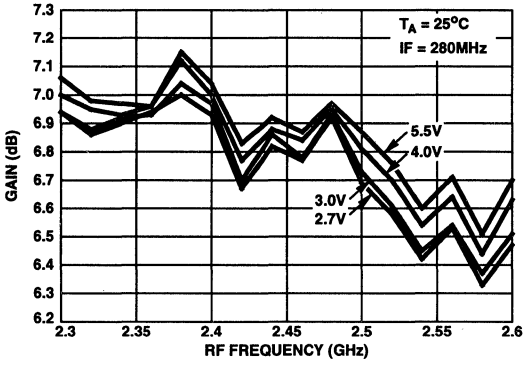


FIGURE 29. RECEIVE MIXER GAIN vs RF FREQUENCY FOR FIXED IF FREQUENCY

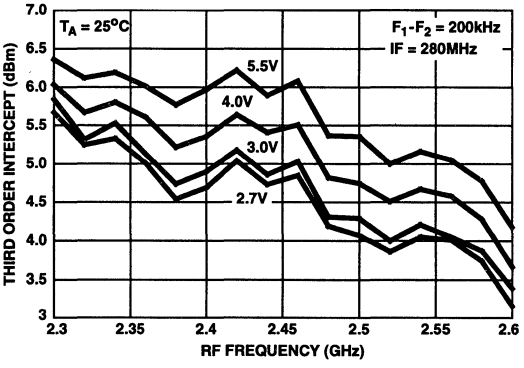


FIGURE 30. RECEIVE MIXER IP3 vs RF FREQUENCY

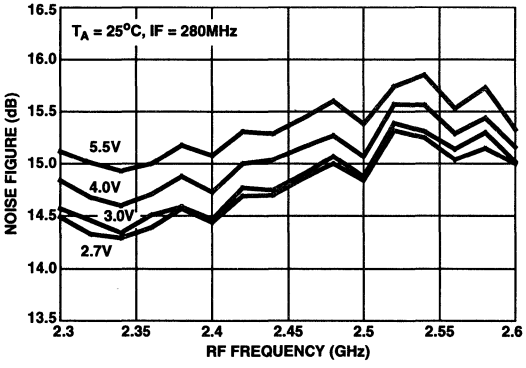


FIGURE 31. RECEIVE MIXER SSB NOISE FIGURE vs RF FREQUENCY

Typical Performance Curves (Continued)

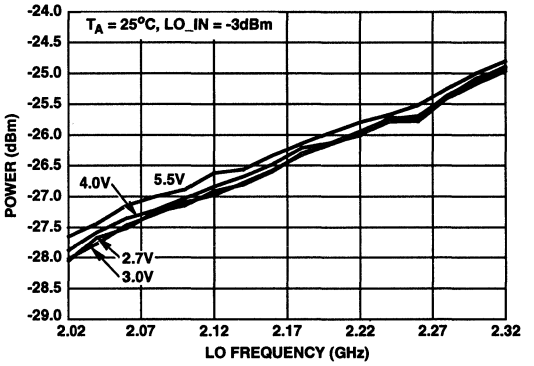


FIGURE 32. RECEIVE MIXER LO TO RF PORT LEAKAGE vs LO FREQUENCY

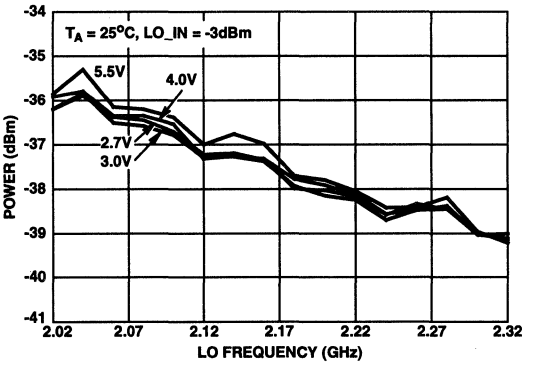
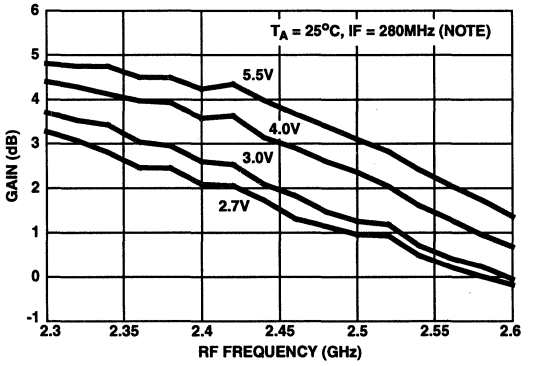
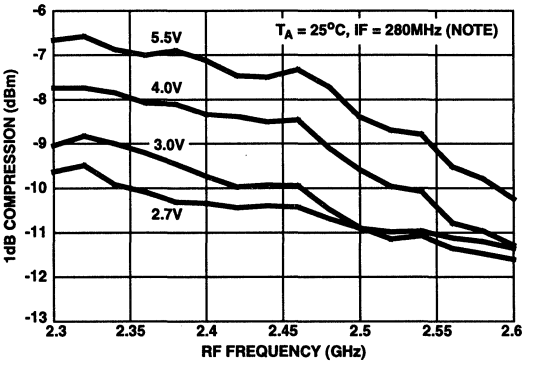


FIGURE 33. RECEIVE MIXER LO TO IF PORT LEAKAGE vs LO FREQUENCY



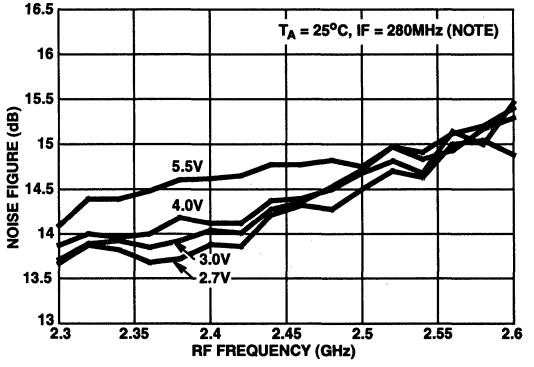
NOTE: Transmit mixer measured with Impedance Transform Network 250Ω at device to 50Ω at the source. Refer to Figure 5, pin 19.

FIGURE 34. TRANSMIT MIXER GAIN vs RF FREQUENCY



NOTE: Transmit mixer measured with Impedance Transform Network 250Ω at device to 50Ω at the source. Refer to Figure 5, pin 19.

FIGURE 35. TRANSMIT MIXER OUTPUT 1dB COMPRESSION vs RF FREQUENCY



NOTE: Transmit mixer measured with Impedance Transform Network 250Ω at device to 50Ω at the source. Refer to Figure 5, pin 19.

FIGURE 36. TRANSMIT MIXER SSB NOISE FIGURE vs RF FREQUENCY

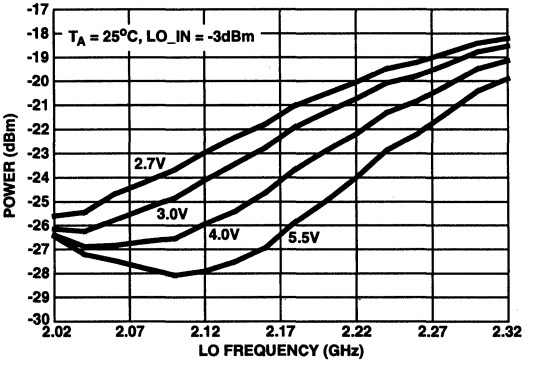


FIGURE 37. TRANSMIT MIXER LO TO RF PORT LEAKAGE vs LO FREQUENCY

Typical Performance Curves (Continued)

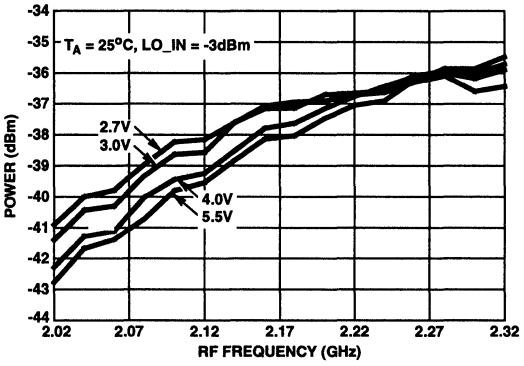


FIGURE 38. TRANSMIT MIXER LO TO IF PORT LEAKAGE vs LO FREQUENCY

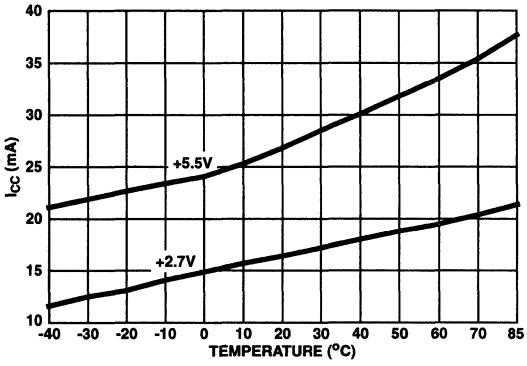


FIGURE 39. RECEIVE MODE I_{CC} vs TEMPERATURE

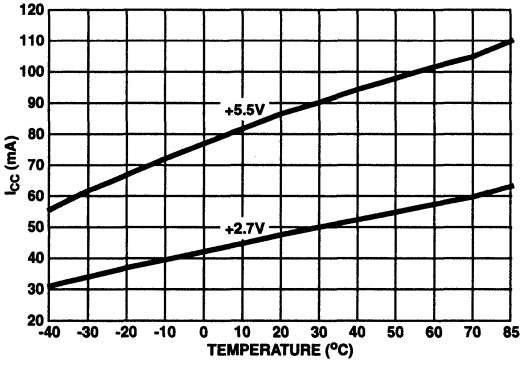


FIGURE 40. TRANSMIT MODE I_{CC} vs TEMPERATURE

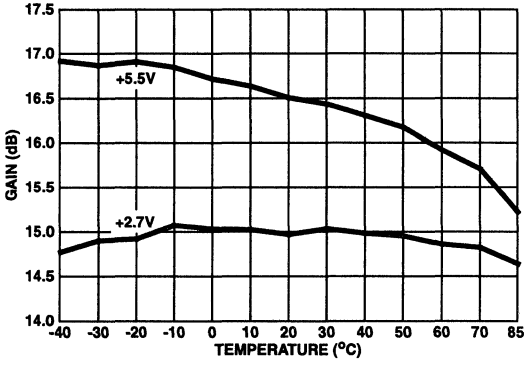


FIGURE 41. LOW NOISE AMPLIFIER GAIN vs TEMPERATURE

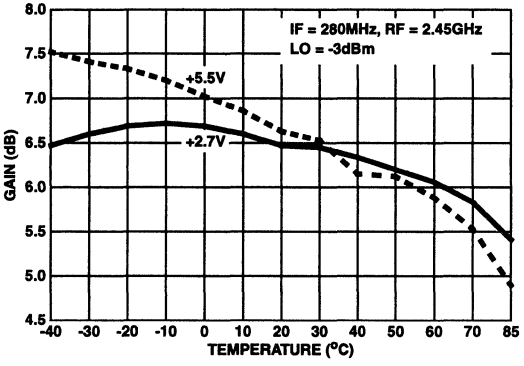


FIGURE 42. RECEIVE MIXER GAIN vs TEMPERATURE

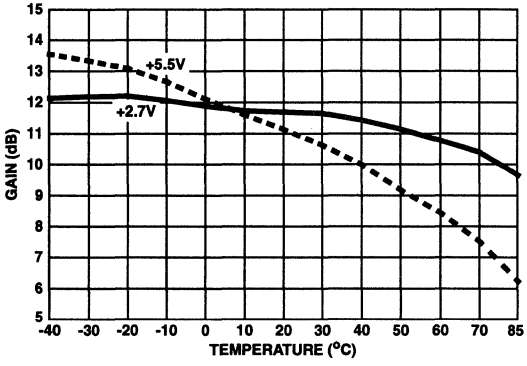


FIGURE 43. PRE-AMPLIFIER GAIN vs TEMPERATURE

Typical Performance Curves (Continued)

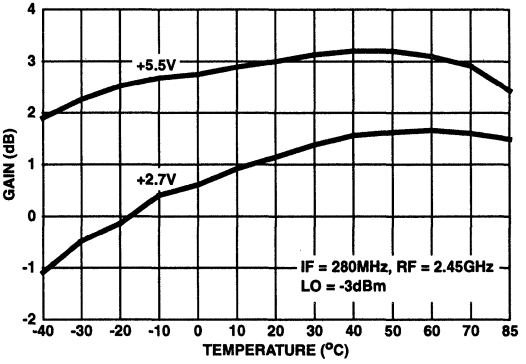


FIGURE 44. TRANSMIT MIXER GAIN vs TEMPERATURE

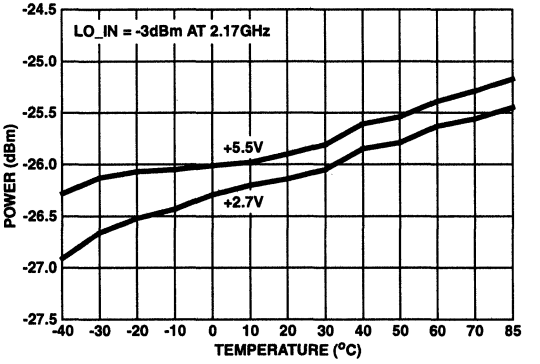


FIGURE 45. RECIEVE MIXER LO TO RF PORT LEAKAGE vs TEMPERATURE

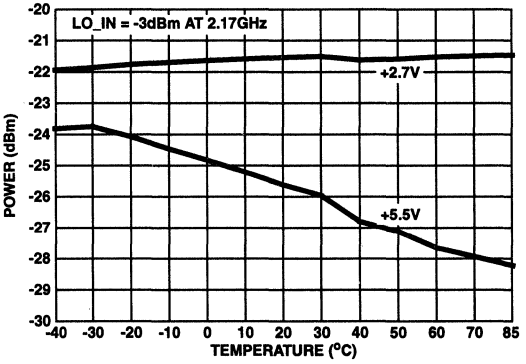


FIGURE 46. TRANSMIT MIXER LO TO RF PORT LEAKAGE vs TEMPERATURE

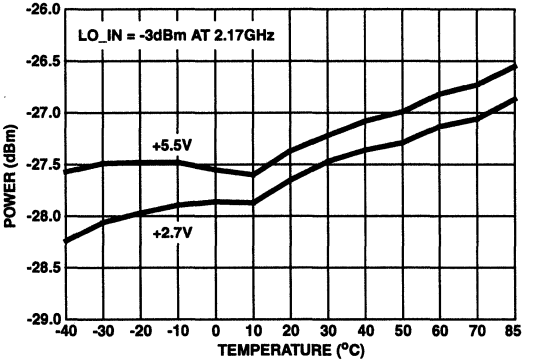


FIGURE 47. RECEIVE MIXER LO TO IF PORT LEAKAGE vs TEMPERATURE

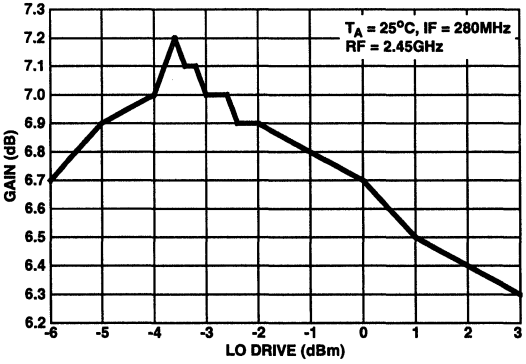


FIGURE 48. RECEIVE MIXER GAIN vs LO DRIVE

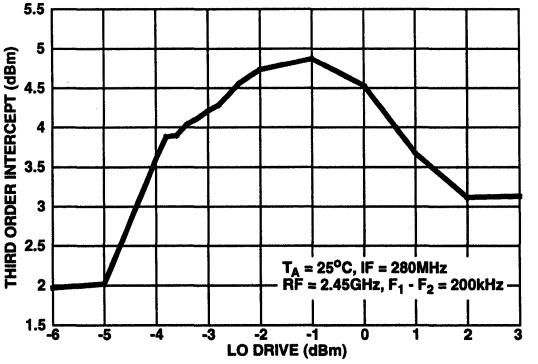


FIGURE 49. RECEIVE MIXER IP3 vs LO DRIVE

Typical Performance Curves (Continued)

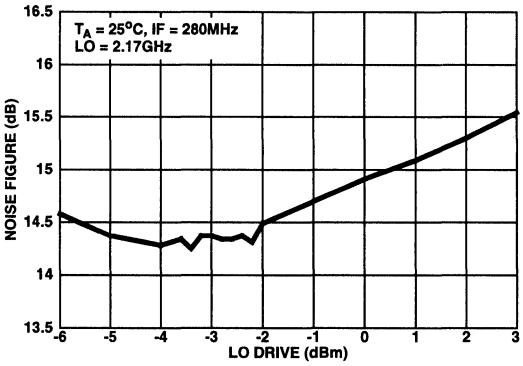
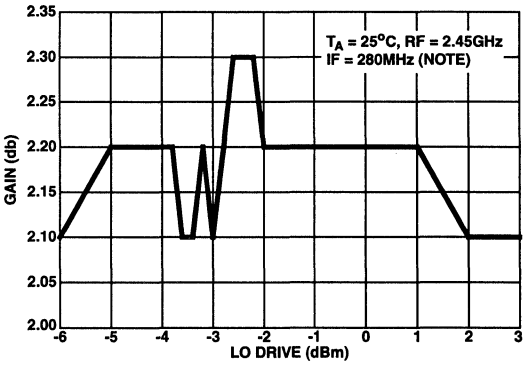
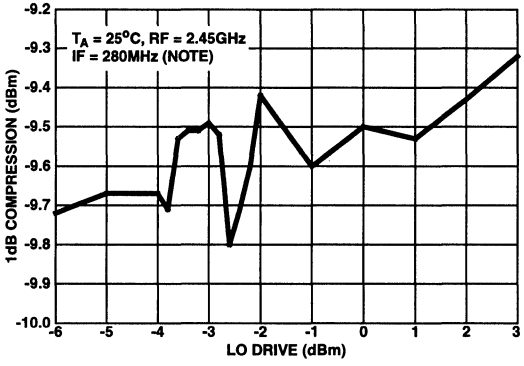


FIGURE 50. RECEIVE MIXER SSB NOISE FIGURE vs LO DRIVE



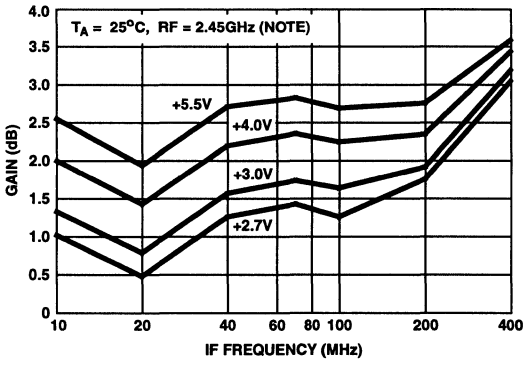
NOTE: Transmit mixer measured with Impedance Transform Network 250Ω at device to 50Ω at the source. Refer to Figure 5, pin 19.

FIGURE 51. TRANSMIT MIXER GAIN vs LO DRIVE



NOTE: Transmit mixer measured with Impedance Transform Network 250Ω at device to 50Ω at the source. Refer to Figure 5, pin 19.

FIGURE 52. TRANSMIT MIXER OUTPUT 1dB COMPRESSION vs LO DRIVE



NOTE: TXM_IF input matching network modified for each IF frequency as described in Table 1.

FIGURE 53. TRANSMIT MIXER GAIN vs IF FREQUENCY

TABLE 1. TXM_IF INPUT 50Ω TO 250Ω IMPEDANCE TRANSFORM CIRCUIT

	COMPONENT VALUES			
IF FREQ	LO CAPACITORS C20, C28	IF BYPASS C24, C21	IF SHUNT C C25	IF SERIES L L4
10MHz	5pF	0.1µF	150pF	1.2µH
20MHz	5pF	0.022µF	68pF	680nH
40MHz	5pF	0.012µF	33pF	330nH
70MHz	5pF	0.0068mF	18pF	180nH
100MHz	7pF	0.0033mF	12pF	120nH
200MHz	7pF	1000pF	3.9pF	68nH
280MHz	10pF	470pF	1.5pF	47nH
400MHz	10pF	330pF	0	33nH

NOTE: Refer to Figure 5, pin 19.

HARRIS SEMICONDUCTOR

HFA3724

400MHz Quadrature IF Modulator/Demodulator

January 1997

Features

- Integrates all IF Transmit and Receive Functions
- Broad Frequency Range .....10MHz to 400MHz
- I/Q Amplitude and Phase Balance ..... 0.2dB, 2°
- 5th Order Programmable Low Pass Filter.....2.2MHz - 17.6MHz
- 400MHz Limiting IF Gain Strip with RSSI 84dB
- Low LO Drive Level .....-15dBm
- Fast Transmit-Receive Switching..... 1µs
- Power Management/Standby Mode
- Single Supply 2.7V to 5.5V Operation

Applications

- Systems Targeting IEEE 802.11 Standard
- TDD Quadrature-Modulated Communication Systems
- Wireless Local Area Networks
- PCMCIA Wireless Transceivers
- ISM Systems
- TDMA Packet Protocol Radios
- PCS/Wireless PBX
- Wireless Local Loop

Description

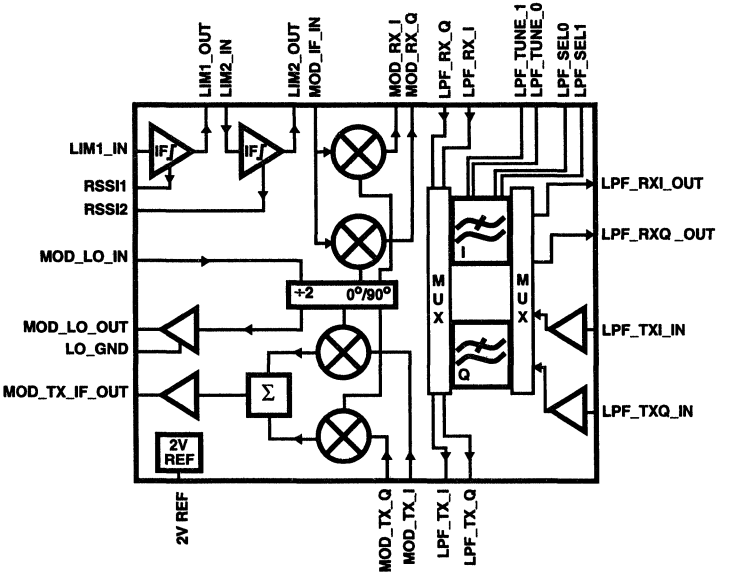
The Harris 2.4GHz PRISM™ chip set is a highly integrated five-chip solution for RF modems employing Direct Sequence Spread Spectrum (DSSS) signaling. The HFA3724 400MHz Quadrature IF Modulator/Demodulator is one of the five chips in the PRISM™ chip set (see the Typical Application Diagram).

The HFA3724 is a highly integrated baseband converter for quadrature modulation applications. It features all the necessary blocks for baseband modulation and demodulation of I and Q signals. It has a two stage integrated limiting IF amplifier with 84db of gain with a built in Receive Signal Strength Indicator (RSSI). Baseband antialiasing and shaping filters are integrated in the design. Four filter bandwidths are programmable via a two bit digital control interface. In addition, these filters are continuously tunable over a ±20% frequency range via one external resistor. The modulator channel receives digital I and Q data for processing. To achieve broadband operation, the Local Oscillator frequency input is required to be twice the desired frequency of modulation/demodulation. A selectable buffered divide by 2 LO output and a stable reference voltage are provided for convenience of the user. The device is housed in a thin 80 lead TQFP package well suited for PCMCIA board applications.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA3724IN	-40 to 85	80 Ld TQFP	Q80.14x14
HFA3724IN96	-40 to 85	Tape and Reel	

Simplified Block Diagram



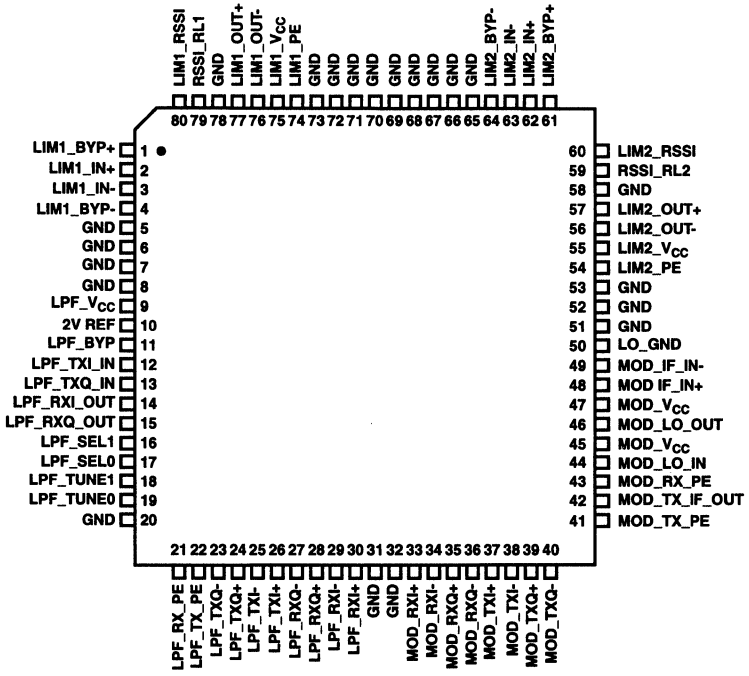
PRISM™ and the PRISM™ logo are trademarks of Harris Corporation.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

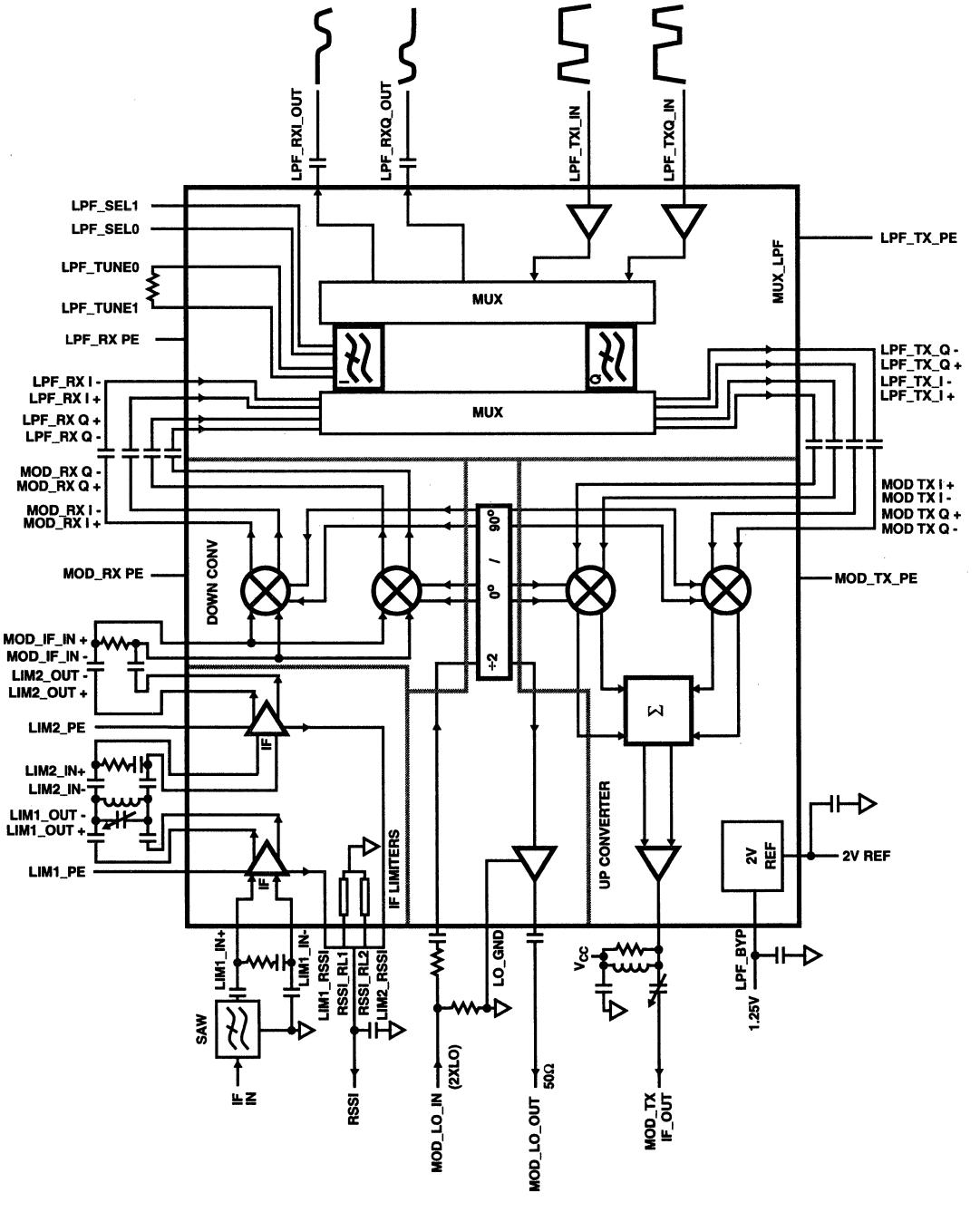
File Number **4067.4**

Pinout

80 LEAD TQFP
TOP VIEW

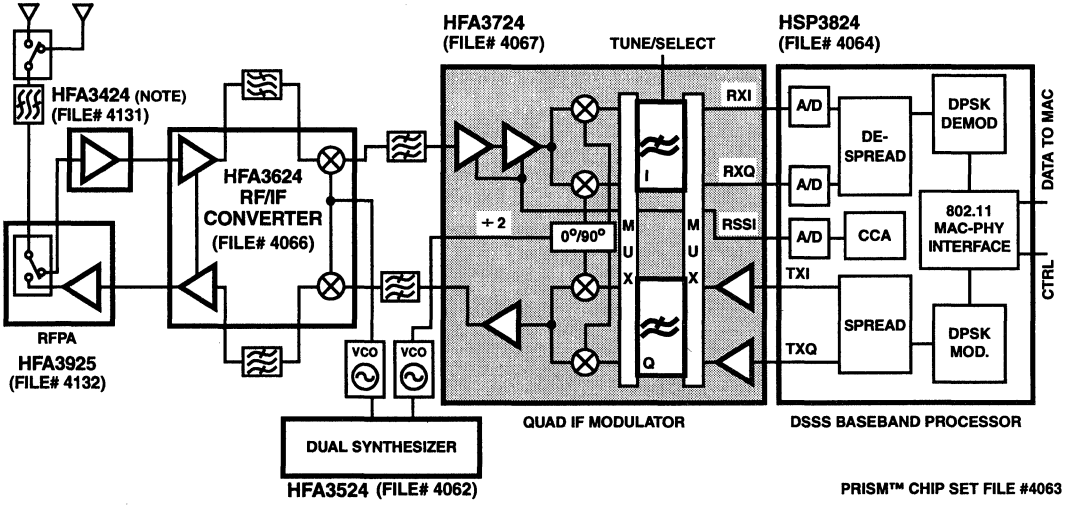


Block Diagram



NOTE: V_{CC}, GND and Bypass capacitors not shown.

Typical Application Diagram



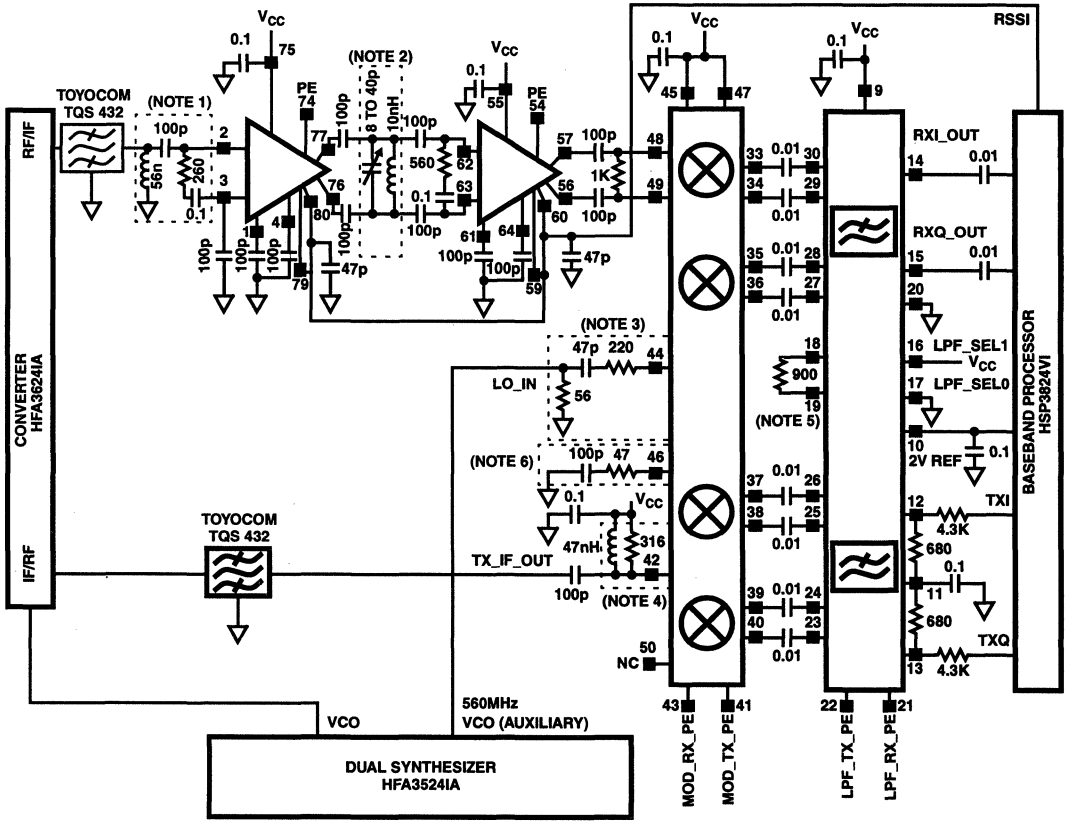
TYPICAL TRANSCEIVER APPLICATION USING THE HFA3724

NOTE: Required for systems targeting 802.11 specifications.

For additional information on the PRISM™ chip set, call (407) 724-7800 to access Harris' AnswerFAX system. When prompted, key in the four-digit document number (File #) of the datasheets you wish to receive.

The four-digit file numbers are shown in Typical Application Diagram, and correspond to the appropriate circuit.

Typical Application Diagram (Targeting IEEE 802.11 Standard)



TYPICAL APPLICATION DIAGRAM (TARGETING IEEE 802.11 STANDARD)

NOTES:

1. Input termination used to match a SAW filter.
2. Typical bandpass filter for 280MHz, BW = 47MHz, Q = 6. Can also be used if desired after the second stage.
3. Network shown for a typical -10dBm input at 50Ω.
4. Output termination used to match a SAW filter.
5. R_{TUNE} value for a 7.7MHz cutoff frequency setting.
6. LO buffer output termination is needed only when the buffer is enabled by pin 50 connected to GND, otherwise tie pin 46 to pin 47.

Pin Description

PIN	SYMBOL	DESCRIPTION
1	LIM1_BYP+	DC feedback pin for Limiter amplifier 1. Requires good decoupling and minimum wire length to a solid signal ground.
2	LIM1_In+	Non inverting analog input of Limiter amplifier 1.
3	LIM1_In-	Inverting input of Limiter amplifier 1.
4	LIM1_BYP-	DC feedback pin for Limiter amplifier 1. Requires good decoupling and minimum wire length to a solid signal ground.
5, 6, 7, 8	GND	Ground. Connect to a solid ground plane.
9	LPF_V_{CC}	Supply pin for the Low pass filter. Use high quality decoupling capacitors right at the pin.
10	2V REF	Stable 2V reference voltage output for external applications. Loading must be higher than 10kΩ. A bypass capacitor of at least 0.1µF is required.
11	LPF_BYP	Internal reference bypass pin. This is the common voltage (V_{CM}) used for the LPF digital thresholds. Requires 0.1µF decoupling capacitor.
12	LPF_TXI_In	Low pass filter in phase (I) channel transmit input. Conventional or attenuated direct coupling is required for digital inputs. (Note 7)
13	LPF_TXQ_In	Low pass filter quadrature (Q) channel transmit input. Conventional or attenuated direct coupling is required for digital inputs. (Note 7)
14	LPF_RXI_Out	Low pass filter in phase (I) channel receive output. Requires AC coupling. (Note 8)
15	LPF_RXQ_Out	Low pass filter quadrature (Q) channel receive output. Requires AC coupling. (Note 8)
16 17	LPF_Sel1 LPF_Sel0	Digital control input pins. Selects four programed cut off frequencies for both receive and transmit channels. Tuning speed from one cutoff to another is less than 1µs. SEL1 SEL0 Cutoff Frequency — SEL1 SEL0 Cutoff Frequency LO LO 2.2MHz — HI LO 8.8MHz LO HI 4.4MHz — HI HI 17.6MHz
18 19	LPF_Tune1 LPF_Tune0	These two pins are used to fine tune the Low pass filter cutoff frequency. A resistor connected between the two pins (R_{TUNE}) will fine tune both transmit and receive filters. Refer to the tuning equation in the LPF AC specifications.
20	GND	Ground. Connect to a solid ground plane.
21	LPF_RX_PE	Digital input control pin to enable the LPF receive mode of operation. Enable logic level is High.
22	LPF_TX_PE	Digital input control pin to enable the LPF transmit mode of operation. Enable logic level is High.
23	LPF_TXQ-	Negative output of the transmit Low pass filter, quadrature channel. AC coupling is required. Normally connects to the inverting input of the quadrature Modulator (Mod_TXQ-), pin 40.
24	LPF_TXQ+	Positive output of the transmit Low pass filter, quadrature channel. AC coupling is required. Normally connects to the non inverting input of the quadrature Modulator (Mod_TXQ+), pin 39.
25	LPF_TXI-	Negative output of the transmit Low pass filter, in phase channel. AC coupling is required. Normally connects to the inverting input of the in phase Modulator (Mod_TXI-), pin 38.
26	LPF_TXI+	Positive output of the transmit Low pass filter, in phase channel. AC coupling is required. Normally connects to the non inverting input of the in phase Modulator (Mod_TXI+), pin 37.
27	LPF_RXQ-	Low pass filter inverting input of the receive quadrature channel. AC coupling is required. This input is normally coupled to the negative output of the quadrature demodulator (Mod_RXQ-), pin 36.
28	LPF_RXQ+	Low pass filter non inverting input of the receive quadrature channel. AC coupling is required. This input is normally coupled to the positive output of the quadrature demodulator (Mod_RXQ+), pin 35.
29	LPF_RXI-	Low pass filter inverting input of the receive in phase channel. AC coupling is required. This input is normally coupled to the negative output of the in phase demodulator (Mod_RXI-), pin 34.

Pin Description (Continued)

PIN	SYMBOL	DESCRIPTION
30	LPF_RXI+	Low pass filter non inverting input of the receive in phase channel. AC coupling is required. This input is normally coupled to the positive output of the in phase demodulator (Mod_RXI-), pin 33.
31, 32	GND	Ground. Connect to a solid ground plane.
33	Mod_RXI+	In phase demodulator positive output. AC coupling is required. Normally connects to the non inverting input of the Low pass filter (LPF_RXI+), pin 30.
34	Mod_RXI-	In phase demodulator negative output. AC coupling is required. Normally connects to the inverting input of the Low pass filter (LPF_RXI-), pin 29.
35	Mod_RXQ+	Quadrature demodulator positive output. AC coupling is required. Normally connects to the non inverting input of the Low pass filter (LPF_RXQ+), pin 28.
36	Mod_RXQ-	Quadrature demodulator negative output. AC coupling is required. Normally connects to the inverting input of the Low pass filter (LPF_RXQ+), pin 27.
37	Mod_TXI+	In phase modulator non inverting input. AC coupling is required. This input is normally coupled to the Low pass filter positive output (LPF_TXI+), pin 26.
38	Mod_TXI-	In phase modulator inverting input. AC coupling is required. This input is normally coupled to the Low pass filter negative output (LPF_TXI-), pin 25.
39	Mod_TXQ+	Quadrature modulator non inverting input. AC coupling is required. This input is normally coupled to the Low pass filter positive output (LPF_TXQ+), pin 24.
40	Mod_TXQ-	Quadrature modulator inverting input. AC coupling is required. This input is normally coupled to the Low pass filter negative output (LPF_TXQ-), pin 23.
41	Mod_TX_PE	Digital input control to enable the Modulator section. Enable logic level is High for transmit.
42	Mod_TX_IF_Out	Modulator open collector output, single ended. Termination resistor to V_{CC} with a typical value of 316Ω.
43	Mod_RX_PE	Digital input control to enable the demodulator section. Enable logic level is High for receive.
44	Mod_LO_In (2XLO)	Single ended local oscillator current input. Frequency of input signal must be twice the required modulator carrier and demodulator LO frequency. Input current is optimum at 200μA_{RMS}. Input matching networks and filters can be designed for a wide range of power and impedances at this port. Typical input impedance is 130Ω.This pin requires AC coupling. (Note 9) NOTE: High second harmonic content input waveforms may degrade I/Q phase accuracy.
45	Mod_V_{CC}	Modulator/Demodulator supply pin. Use high quality decoupling capacitors right at the pin.
46	Mod_LO_Out	Divide by 2 buffered output reference from "Mod_LO_in" input. Used for external applications where the modulating and demodulating carrier reference frequency is required. 50Ω single end driving capability.This output can be disabled by use of pin 50. AC coupling is required, otherwise tie to pin 47 (V_{CC}).
47	Mod_V_{CC}	Modulator/Demodulator supply pin. Use high quality decoupling capacitors right at the pin.
48	Mod_IF_In+	Demodulator non inverting input. Requires AC coupling.
49	Mod_IF In-	Demodulator inverting input. Requires AC coupling.
50	LO_GND	When grounded, this pin enables the LO buffer (Mod_LO_Out). When open (NC) it disables the LO buffer.
51,52, 53	GND	Ground. Connect to a solid ground plane.
54	LIM2_PE	Digital input control to enable the limiter amplifier 2. Enable logic level is High.
55	LIM2_V_{CC}	Limiter amplifier 2 supply pin. Use high quality decoupling capacitors right at the pin.
56	LIM2_Out-	Positive output of limiter amplifier 2. Requires AC coupling.
57	LIM2_Out+	Negative output of limiter amplifier 2. Requires AC coupling.
58	GND	Ground. Connect to a solid ground plane.

Pin Description (Continued)

PIN	SYMBOL	DESCRIPTION
59	RSSI_RL2	Load resistor to ground. Nominal value is 6kΩ. This load is used to terminate the LIM RSSI current output and maintain temperature and process variation to a minimum.
60	LIM2_RSSI	Current output of RSSI for the limiter amplifier 2. Connect in parallel with the RSSI output of the amplifier limiter 1 for cascaded response.
61	LIM2_BYP+	DC feedback pin for Limiter amplifier 2. Requires good decoupling and minimum wire length to a solid signal ground.
62	LIM2_In+	Non inverting analog input of Limiter amplifier 2.
63	LIM2_In-	Inverting input of Limiter amplifier 2.
64	LIM2_BYP-	DC feedback pin for Limiter amplifier 2. Requires good decoupling and minimum wire length to a solid signal ground.
65, 66, 67, 68, 69, 70, 71, 72, 73	GND	Ground. Connect to a solid ground plane.
74	LIM1_PE	Digital input control to enable the limiter amplifier 1. Enable logic level is High.
75	LIM1_V_{CC}	Limiter amplifier 1 supply pin. Use high quality decoupling capacitors right at the pin.
76	LIM1_Out-	Negative output of limiter amplifier 1. Requires AC coupling.
77	LIM1_Out+	Positive output of limiter amplifier 1. Requires AC coupling.
78	GND	Ground. Connect to a solid ground plane.
79	RSSI_RL1	Load resistor to ground. Nominal value is 6kΩ. This load is used to terminate the LIM RSSI current output and maintain temperature and process variation to a minimum.
80	LIM1_RSSI	Current output of RSSI for the limiter amplifier 1. Connect in parallel with the RSSI output of the amplifier limiter 2 for cascaded response.

NOTES:

7. The HFA3724 generates a lower sideband signal when the "I" input leads the "Q" input by 90 degrees.
8. For a reference LO frequency higher than a CW IF signal input, the "I" channel leads the "Q" channel by 90 degrees.
9. The in-phase reference LO transitions occur at the rising edges of the 2XLO clock signal. Quadrature LO transitions occur at the falling edges. 180 degrees phase ambiguity is expected for carrier locked systems without differential encoding.

TABLE 1. POWER MANAGEMENT

	TRANSMIT	RECEIVE	POWER DOWN
LIM1_PE	0	1	0
LIM2_PE	0	1	0
LPF_RX_PE	0	1	0
MOD_RX_PE	0	1	0
MOD_TX_PE	1	0	0
LPF_TX_PE	1	0	0

Absolute Maximum Ratings

Supply Voltage . . . . . -0.3V to +6.0V
Voltage on Any Other Pin . . . . . -0.3V to V_{CC} +0.3V

Operating Conditions

Supply Voltage Range . . . . . +2.7V to +5.5V
Temperature Range . . . . . $-40^{o}C \le T_A \le 85^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 10) θ_{JA} ($^{o}C/W$)
TQFP Package 75
Package Power Dissipation at 70°C
TQFP Package 1.1W
Maximum Junction Temperature (Plastic Package . . . . . 150°C
Maximum Storage Temperature Range . . . . . $-65^{o}C \le T_A \le 150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(TQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

10. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 2.7V to 5.5V, Unless Otherwise Specified

PARAMETER	SYMBOL	(NOTE 11) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
Total Supply Current, RX Mode at 5.5V	RXI_{CC}	A	Full	-	70	105	mA
Total Supply Current, TX Mode at 5.5V	TXI_{CC}	A	Full	-	60	80	mA
Shutdown Current at 5.5V	I_{CCOFF}	A	Full	-	0.8	2.0	mA
All Digital Inputs V_{IH} (TTL Threshold for All V_{CC})	V_{IH}	A	Full	2.0		V_{CC}	V
All Digital Inputs V_{IL} (TTL Threshold for All V_{CC})	V_{IL}	A	Full	-0.2		0.8	V
High Level Input Current at 2.7V V_{CC}, V_{IN} = 2.4V	I_{IHl}	A	25	-	-	80	µA
High Level Input Current at 5.5V V_{CC}, V_{IN} = 4.0V	I_{IHh}	A	25	-	-	400	µA
Low Level Input Current, V_{IN} = 0.8V	I_{IL}	A	25	-20	-	+20	µA
RX to TX/TX to RX Switching Speed (Figure 23)	PEt	B	25	-	2	-	µs
Power Down/Up Switching Speed (Figure 23)	PEtpd	B	25	-	10	-	µs
Reference Voltage	V_{REF}	A	Full	1.87	2.0	2.13	V
Reference Voltage Variation Over Temperature	V_{REFT}	B	25	-	800	-	µV/°C
Reference Voltage Variation Over Supply Voltage	V_{REFV}	B	25	-	1.6	-	mV/V
Reference Voltage Minimum Load Resistance	V_{REFRL}	C	25	10	-	–	kΩ

NOTE:

11. A = Production Tested, B = Based on Characterization, C = By Design

AC Electrical Specifications, Demodulator Performance

Application Targeting IEEE 802.11, V_{CC} = 3V, Figure 23 Unless Otherwise Specified

PARAMETER	SYMBOL	(NOTE 12) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
IF Demodulator 3dB Limiting Sensitivity (Note 13)	D3db	B	25	-	-84	-	dBm
IF Demodulator I and Q Outputs Voltage Swing	DIQsw	A	Full	350	500	700	mV_{P-P}
IF Demodulator I and Q Channels Output Drive Capability (Z_{OUT} = 50Ω) C_{MAX} = 10pF	Doutz	C	25	1.2	2	-	kΩ
IF Demodulator I/Q Amplitude Balance, IFin = -70dbm at 50Ω	Dabal	A	Full	-1.0	0	+1.0	dB
IF Demodulator I/Q Phase Balance, IFin = -70dbm at 50Ω	Dphbal	A	Full	-4.0	0	+4.0	Degrees
IF Demodulator Output Variation at -70dbm to 0dbm input	Dovar	A	Full	-0.5	0	+0.5	dB
IF Demodulator RSSI Noise Induced Offset Voltage (Note 14)	Drssio	B	25	-	580	-	mV_{DC}
IF Demodulator RSSI Voltage Output Slope (Note 15)	Drssis	B	25	-	15	-	mV/dB

AC Electrical Specifications, Demodulator Performance

Application Targeting IEEE 802.11, V_{CC} = 3V, Figure 23 Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	(NOTE 12) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
IF Demodulator RSSI DC Level, Pin = -30dBm (Note 15)	Drssi_30	A	Full	1.13	1.46	1.71	V_{DC}
IF Demodulator RSSI DC Level, Pin = -70dBm (Note 15)	Drssi_70	A	Full	0.57	0.86	0.99	V_{DC}
IF Demodulator RSSI Linear Dynamic Range (Note 16)	Drssidr	B	25	-	60	-	dB
IF Demodulator RSSI Rise and Fall Time from -30dBm to -50dBm Input at 100pF Load	Drssitr	B	25	-	0.3	-	µs

NOTES:

12. A = Production Tested, B = Based on Characterization, C = By Design
13. 2XLO input = 572MHz, measure IF input level required to drop the I and Q output at 6MHz by 3dB from a reference output generated at IF input = -30dBm (hard limiting). LPF selected for 8.8MHz. This is a noise limited case with a BW of 47MHz. Please refer to the Overall Device Description, IF limiter.
14. The residual DC voltage generated by the RSSI circuit due to a noise limited stage at the end of the chain with no IF input. IF port terminated into 50Ω. Please referred to the Overall Device Description, IF limiter.
15. Both limiter RSSI current outputs are summed by on chip 6KΩ resistors in parallel.
16. Range is defined where the indicated received input strength by the RSSI is ±3dBm accurate.

AC Electrical Specifications, Modulator Performance

Application Targeting IEEE 802.11, V_{CC} = 3V, Figure 23 Unless Otherwise Specified

PARAMETER	SYMBOL	(NOTE 17) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
IF Modulator I/Q Amplitude Balance (Note 18)	Mabal	B	25	-1.0	0	+1.0	dB
IF Modulator I/Q Phase Balance (Note 18)	Mphbal	B	25	-4.0	0	+4.0	Degrees
IF modulator SSB Output Power (Note 19)	Mssbpw	A	Full	-12	-7	-4	dBm
IF Modulator Side Band Suppression (Note 19)	Mssbss	A	Full	26	33	-	dBc
IF Mod Carrier Suppression (LO Buffer Enabled) (Note 19)	Mssbcs	A	Full	28	30	-	dBc
IF Mod Carrier Suppression (LO Buffer Disabled) (Note 19)	Mssbcs1	B	25	28	36	-	dBc
IF Modulator Output Noise Floor (Out of Band)	Moutn0	B	25	-	-132	-	dBm/Hz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 2.2MHz (Note 20)	Msel1f	A	Full	1.8	2.2	2.5	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 4.4MHz (Note 20)	Msel2f	A	Full	3.6	4.4	5.0	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 8.8MHz (Note 20)	Msel3f	A	Full	7.3	8.8	9.8	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 17.6MHz (Note 20)	Msel4f	A	Full	14.6	17.6	19.6	MHz
IF Modulator Spread Spectrum Output Power (Note 21)	Mdsspw	B	25	-12	-7	-4	dBm
IF Modulator Side Lobe to Main Lobe Ratio, LPF = 8.8MHz (Note 21)	Mdsssl	A	Full	32	35	-	dB

NOTES:

17. A = Production Tested, B = Based on Characterization, C = By Design
18. Data is characterized by DC levels applied to MOD TXI and Q pins for 4 quadrants with LO output as reference or indirectly by the SSB characteristics.
19. Power at the fundamental SSB frequency of two 6MHz, 90 degrees apart square waves applied at TXI and TXQ inputs. V_{IH} = 3.0V, V_{IL} = 0.5V. LPF selected to 8.8MHz cutoff.
20. Cutoff frequencies are specified for both modulator and demodulator as the filter bank is shared and multiplexed for Transmit and Receive. Data is characterized by observing the attenuation of the fundamental of a square wave digital input swept at each channel separately. The IF output is down converted by an external wideband mixer with a coherent LO input for each of quadrature signals separately.
21. Typical ratio characterization with R_{TUNE} set to 7.7MHz, LPF selected for 8.8MHz. TXI and TXQ Digital Inputs at two independent and aligned 11M chip/s, 2^{23}-1 sequence code signals.

Typical Performance Curves, Demodulator (See Figure 23 Test Diagram)

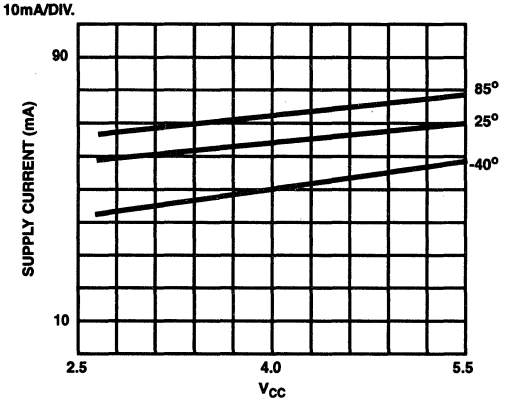


FIGURE 1. DEMODULATOR SUPPLY CURRENT vs V_{CC} AND TEMPERATURE

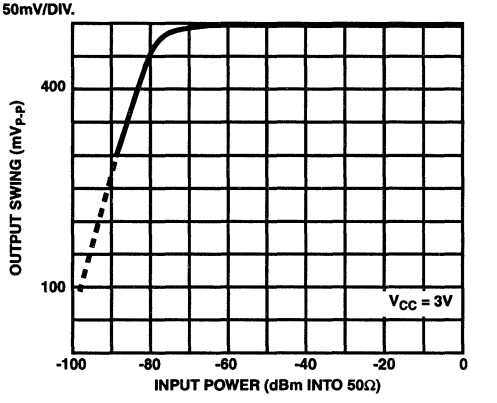


FIGURE 2. DEMODULATOR I/Q OUTPUT SWING vs INPUT POWER

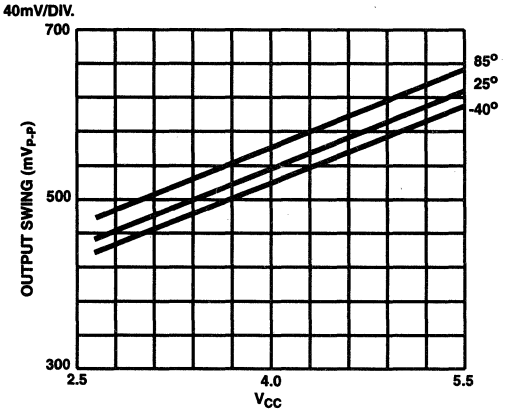


FIGURE 3. DEMOD I/Q OUTPUT SWING vs V_{CC} AND TEMPERATURE

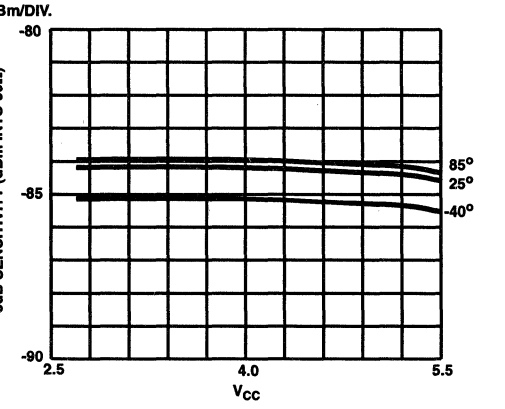


FIGURE 4. CASCADED LIMITER -3dB INPUT SENSITIVITY RESPONSE vs V_{CC} AND TEMPERATURE

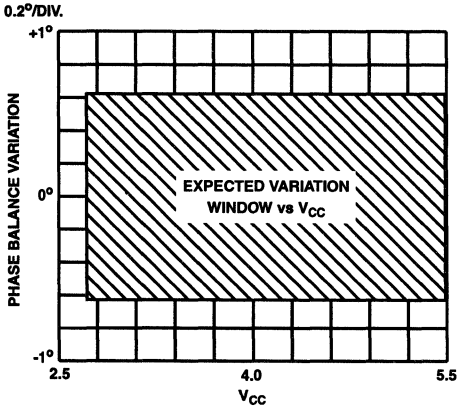


FIGURE 5. DEMOD I/Q PHASE BALANCE VARIATION vs V_{CC}

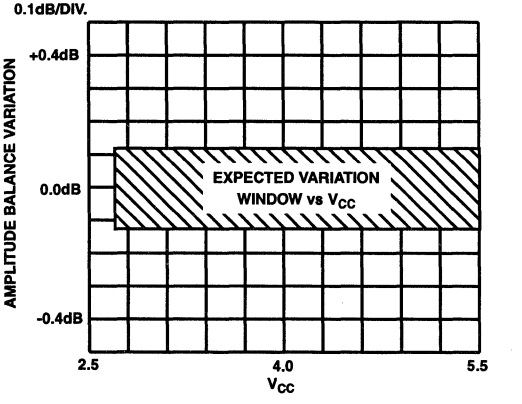


FIGURE 6. DEMOD I/Q AMPLITUDE BALANCE VARIATION vs V_{CC}

Typical Performance Curves, Demodulator (See Figure 23 Test Diagram) (Continued)

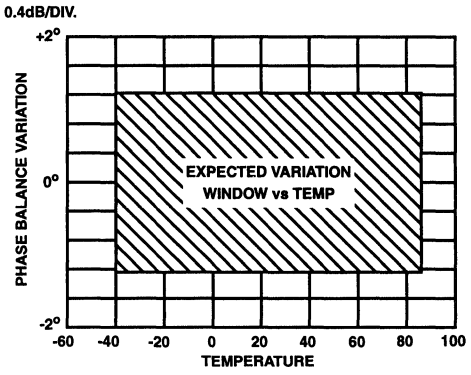


FIGURE 7. DEMOD I/Q PHASE BALANCE VARIATION vs TEMPERATURE

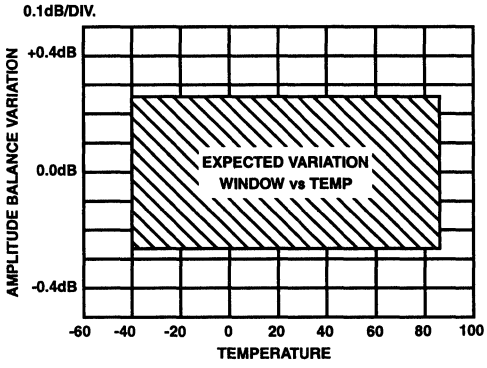


FIGURE 8. DEMOD I/Q AMPLITUDE BALANCE VARIATION vs TEMPERATURE

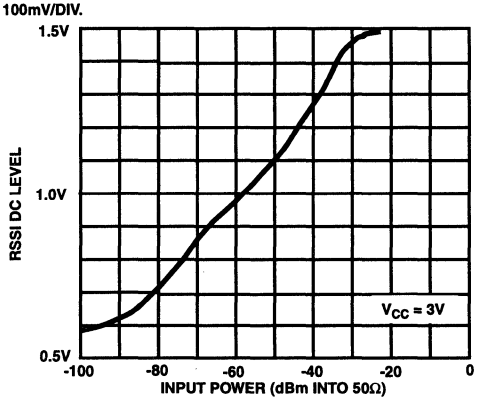


FIGURE 9. DEMOD RSSI DC LEVEL vs INPUT POWER

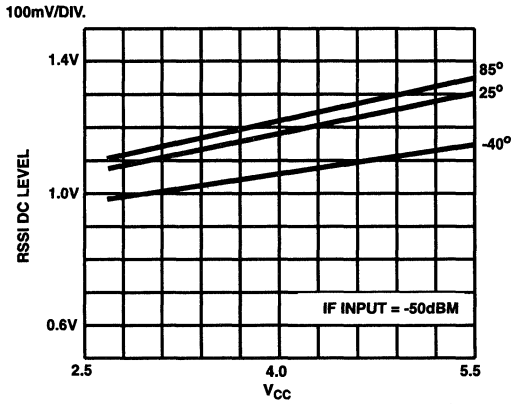


FIGURE 10. DEMOD RSSI DC LEVEL vs V_{CC} AND TEMPERATURE

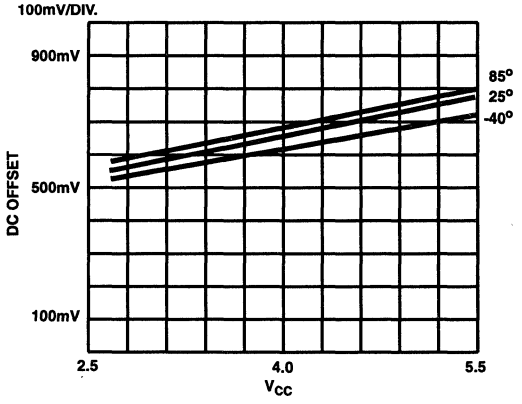


FIGURE 11. DEMODULATOR RSSI DC OFFSET vs V_{CC} AND TEMPERATURE

Typical Performance Curves, Modulator (See Figure 23 Test Diagram)

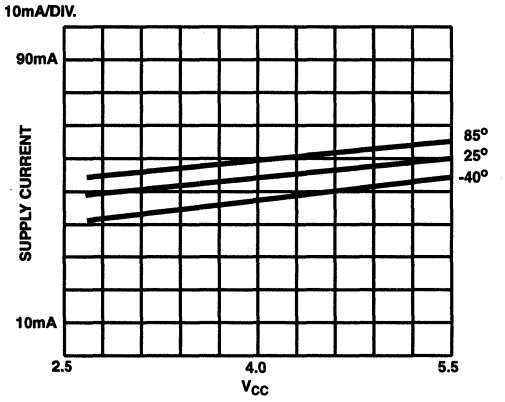


FIGURE 12. MODULATOR SUPPLY CURRENT vs V_{CC} AND TEMPERATURE

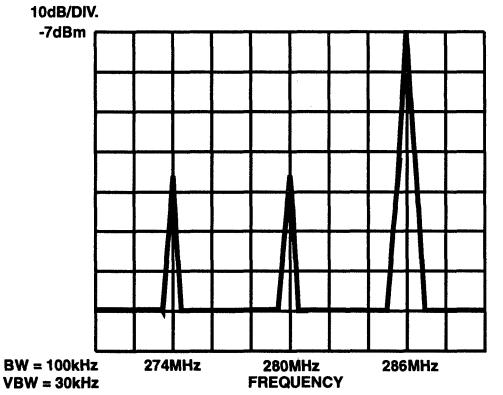


FIGURE 13. TYPICAL SSB MODULATOR RESPONSE (NOTE 3 ON AC ELECTRICAL SPECIFICATIONS, MODULATOR PERFORMANCE TABLE, LO BUFFER ENABLED)

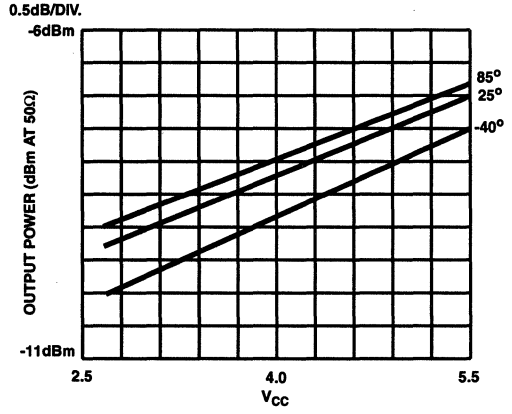


FIGURE 14. MODULATOR SSB OUTPUT POWER vs V_{CC} AND TEMPERATURE

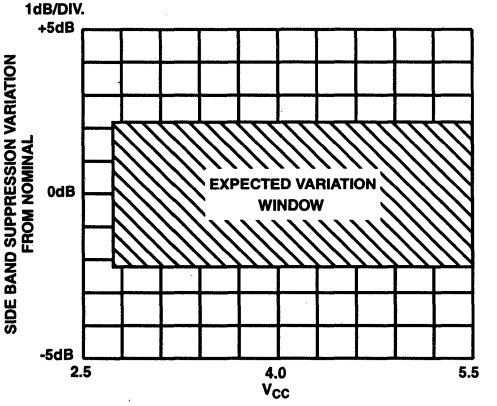


FIGURE 15. MODULATOR SSB SIDE BAND SUPPRESSION VARIATION vs V_{CC} AND TEMPERATURE

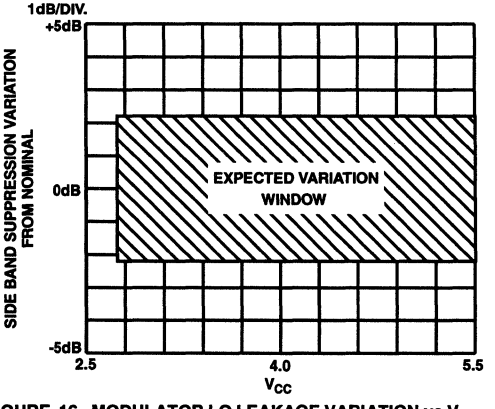


FIGURE 16. MODULATOR LO LEAKAGE VARIATION vs V_{CC} AND TEMPERATURE

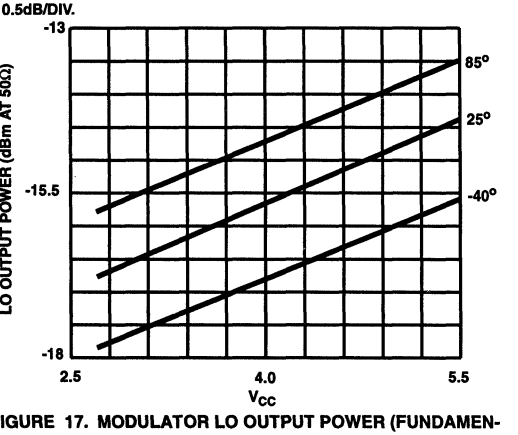


FIGURE 17. MODULATOR LO OUTPUT POWER (FUNDAMENTAL) vs V_{CC} AND TEMPERATURE

Typical Performance Curves, Modulator (See Figure 23 Test Diagram) (Continued)

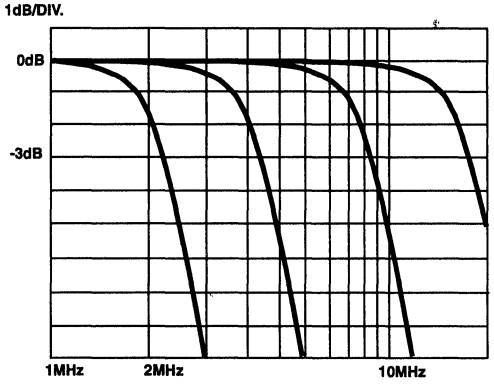


FIGURE 18. TYPICAL MODULATOR I/Q 3dB CUTOFF FREQUENCY CURVES

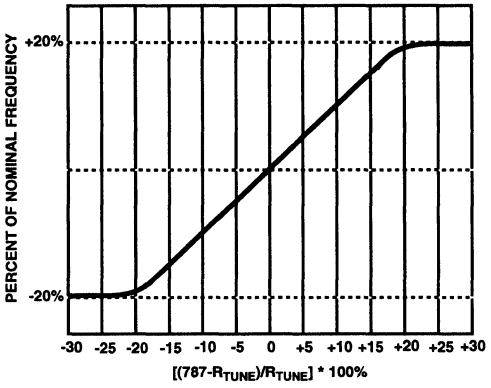


FIGURE 19. LPF CUTOFF FREQUENCY vs R_{TUNE}, V_{CC} = 3V, T_A = 25°C

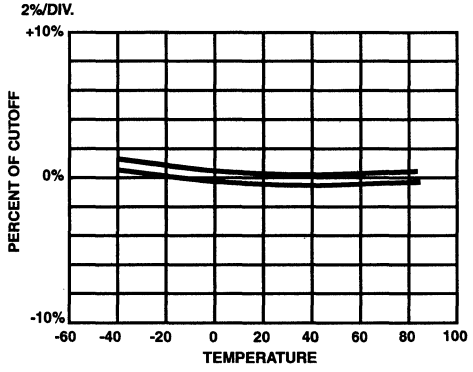


FIGURE 20. LPF CUTOFF FREQUENCY vs TEMPERATURE AND V_{CC} (NOTE 4 ON AC ELECTRICAL SPECIFICATIONS, MODULATOR PERFORMANCE TABLE)

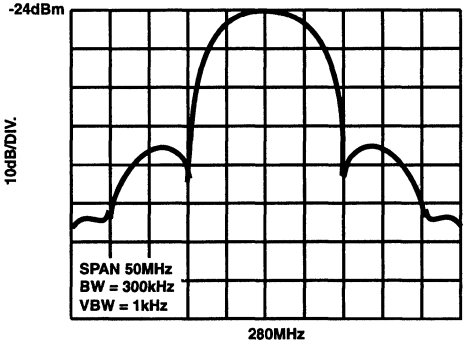


FIGURE 21. TYPICAL MODULATOR SPREAD SPECTRUM OUTPUT 11M CHIPS/s, QPSK. R_{TUNE} TO 7.7MHz, 8.8MHz SETTING

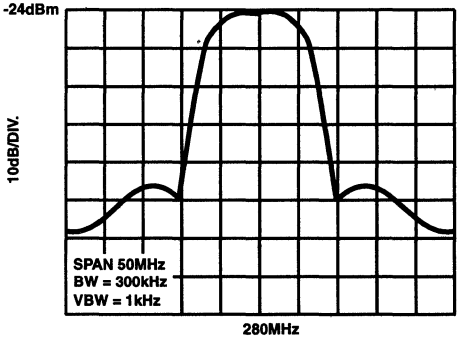


FIGURE 22. TYPICAL MODULATOR SPREAD SPECTRUM OUTPUT WITH R_{TUNE} TO +20% OF 4.4MHz SETTING FOR ILLUSTRATION PURPOSES ONLY

Test Diagram (280MHz IF)

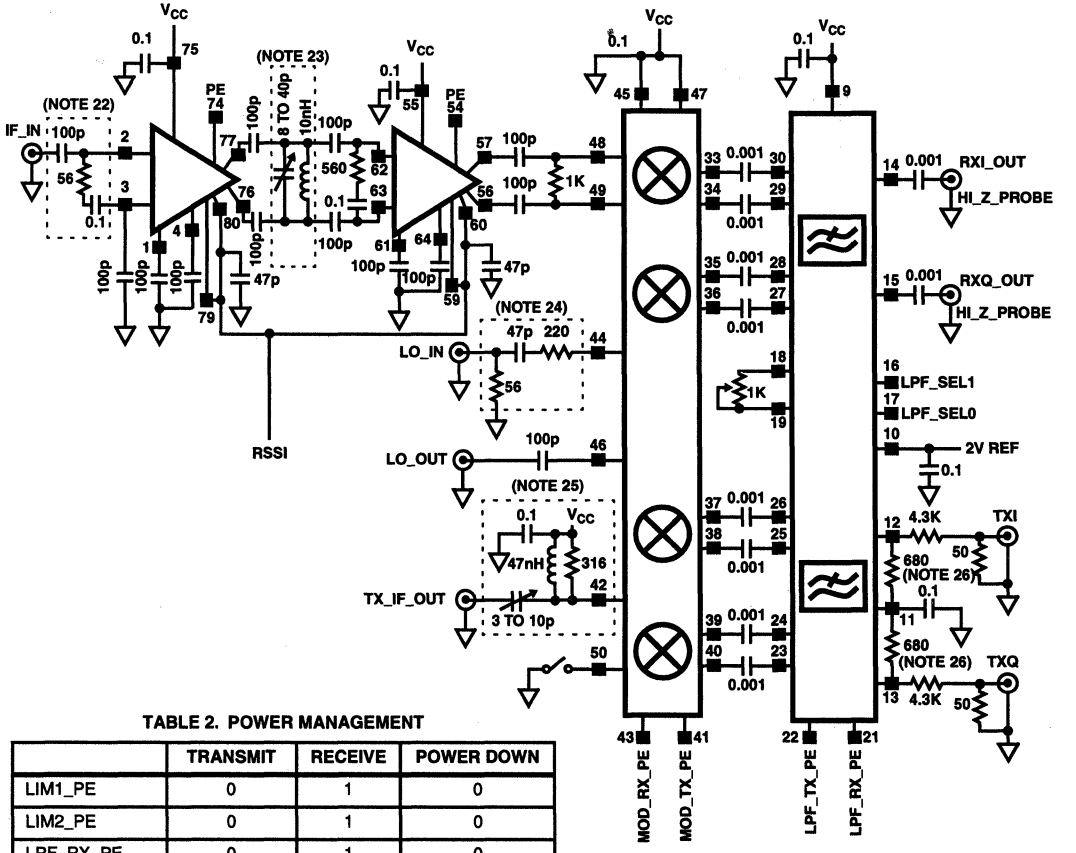


TABLE 2. POWER MANAGEMENT

	TRANSMIT	RECEIVE	POWER DOWN
LIM1_PE	0	1	0
LIM2_PE	0	1	0
LPF_RX_PE	0	1	0
MOD_RX_PE	0	1	0
MOD_TX_PE	1	0	0
LPF_TX_PE	1	0	0

FIGURE 23. TEST DIAGRAM (280MHz IF)

NOTES:

22. Input termination used to provide a 50Ω impedance. Limiter Noise Figure ≡ 9dB for this configuration.
23. Bandpass filter for 280MHz, BW = 47MHz, Q = 6.
24. Network shown for a typical -10dBm input at 50Ω.
25. Matching network from 250Ω to 50Ω at 280MHz.
26. Attenuator is optional if TTL driver can drive 50Ω.

Overall Device Description

The HFA3724 is a highly integrated baseband converter for half duplex wireless data applications. It features all the necessary blocks for baseband modulation and demodulation of "I" and "Q" quadrature multiplexing signals. It targets applications using all phase shift types of modulation (PSK) due to its hard limiting receiving front end. Four fully independent blocks adds flexibility for numerous applications covering a wide range of IF frequencies. A differential design architecture, device pin out and layout have been chosen to improve system RF properties like common mode signal immunity (noise, crosstalk), reduce relevant parasitics and settling times and optimize dynamic range for low power requirements. Single power supply requirements from $2.7V_{DC}$ to $5.5V_{DC}$ makes the HFA3724 a good choice for portable transceiver designs.

The HFA3724 has a two stage integrated limiting IF amplifier with frequency response to 400MHz. These amplifiers exhibit a -84dbm, -3db cascaded limiting sensitivity with a built in Receive Signal Strength Indicator (RSSI) covering 60db of dynamic range with excellent linearity. An up conversion and down conversion pair of quadrature doubly balanced mixers are available for "I" and "Q" baseband IF processing. These converters are driven by an internal quadrature LO generator which exhibits a broadband response with excellent quadrature properties. To achieve broadband operation, the Local Oscillator frequency input is required to be twice the desired frequency for modulation/demodulation. Duty cycle and signal purity requirements for the 2X LO input using this type of quadrature architecture are less restrictive for the HFA3724. Ground reference input signals as low as -15dBm and frequencies up to 900MHz (2XLO) can be used and tailored by the user. A buffered, divide by 2, LO single ended 50Ω selectable output is provided for convenience of PLL designs. The receive channel mixers "I" and "Q" quadrature outputs have a frequency response up to 30MHz for baseband signals and the transmit mixers are summed and amplified to a single ended open collector output with frequency response up to 400MHz.

Multiplexed or half duplex baseband 5th order Butterworth low pass filters are also included in the design. The "I" and "Q" filters address applications requiring low pass and antialiasing filtering for external baseband threshold comparison or simple analog to digital conversion in the receive channel. During transmission, the filter is used for pulse shaping or control of spectral mask.

Four filter bandwidths are programmable, (2.2MHz, 4.4MHz, 8.8MHz and 17.6MHz) via a two bit digital or hardwired control interface. These cut off frequencies are selected for optimization of spectrum output responses for 2.25M, 5.5M, 11M and 22M chips/sec respectively for spread spectrum applications (These rates can also be interpreted as symbol rates for conventional data transmission). External processing correlators in the receive channel as in the Harris HSP3824 baseband converter, will bring the demodulation to lower effective data rates. As an example, the use of 11M chips/sec, 11 chip Barker code using the 8.8MHz low pass filter in a QPSK type of modulation scheme will bring a post processed effective data rate to 1M symbol/sec or 2M bits/sec. Likewise, the use of a 2.4M chips/sec, 16 chip spreading code and the use of 2.2MHz filter can process an effective data rate of 150K symbols/sec or 300K bits/sec. In addition, these filters are continuously tunable over a ±20% frequency range via one external resistor. This feature gives the user the ability to reshape the spectrum of a transmitted signal at the antenna port which takes into account any spectral regrowth along the transmitter chain. The modulator "I" and "Q" filter inputs accept digital signal levels data for modulation and their phase and gain characteristics, including I / Q matching and group delay are well suitable for reliable data transmission. In the Receive mode and over the full input limiting dynamic range, both low pass filters outputs swing a $500mV_{P-P}$ baseband signal.

Each block has its own independent power enable control for power management and half duplex transmit/receive operation. A stable 2V DC output and a buffered band gap reference voltage are also provided for an external analog to digital conversion reference.

Detailed Description

(Refer to Block Diagram)

IF Limiter

Two independent limiting amplifiers are available in the HFA3724. Each one exhibits a broadband response to 400MHz with 45dB of gain. The low frequency response is limited by external components because the device has no internal coupling capacitors. The differential limiting output swing with a 500Ω load is typically $200mV_{P-P}$ at the fundamental frequency and is temperature stable.

Both amplifiers are very stable within their passband and the cascaded performance also exhibits very good stability for any input source impedance. Wide bandwidth SAW filters for spread spectrum applications or any desired source impedance filter implementation can be used for IF filtering before the cascaded amplifiers. The stability is remarkable for such an integrated solution. In fact, in many applications it is possible to remove the bypass pin capacitors with no degradation in stability. The cascaded -1dB and -3dB input limiting sensitivity have been characterized as -79dbm and 84dbm respectively, for a 50Ω single ended input at 280MHz and with a 47MHz bandwidth interstage bandpass LC filter (refer to Figure 23, Test Diagram). The input sensitivity is determined to a large extent by the bandwidth of the interstage filter and input source impedance.

The noise figure for each stage has been characterized at 6dB for a 250Ω single end input impedance and 9dB for a 50Ω input impedance. These low noise figures combined with their high gain, eliminate the need for additional IF gain components. The use of interstage bandpass filtering is suggested to decrease the noise bandwidth of the signal driving the second stage. Excessive broadband noise energy amplified by the first stage will force the last limiting stage to lose some of its effective gain or "limit on the noise". The use of interstage filters with narrower bandwidths will further improve the sensitivity of the cascaded limiter chain.

The amplifier differential output impedance is 140Ω (70Ω single ended) which gives the user, the ability to design simple wide or narrow LC bandwidth interstage filters, or tailor a desired cascaded gain by using differential attenuators. The filter can be designed with a desired "Q" by using the followIng relationship: Q = Rp/X; where Rp is the parallel combination of 140Ω source resistance and the load (approximately 500Ω when using 560Ω termination as in Figure 23, Test Diagram), and X is the reactance of either L or C at the desired center frequency.

Another independent feature of the limiting amplifier is its Receive Signal Strength Indicator (RSSI). A Log-Amp design was developed which resulted in a current output proportional to the input power. The RSSI output voltage is set by summing the two stages output currents, which are full wave rectified signals, to a common resistor to ground. This full wave rectified voltage can then be converted to DC by the use of a filter capacitor in parallel with the resistor (The larger the capacitor value, the less the AC ripple with the expense of longer RSSI settling times). This arrangement gives the user the flexibility to set the dynamic voltage swing to any desired level by an appropriate resistance choice. Each stage has an available on chip 6KΩ low temperature coefficient resistor to ground for current output termination that can be used for convenience. The RSSI gives a ±3dBm accurate indication of the receive input power. This accuracy is across a 60dB input dynamic range. The cascaded HFA3724 RSSI slope is of 5.0μA/dB.

Quadrature Down Converter

The quadrature down converter mixers are based in a Gilbert cell design. The input signal is routed to both mixers in parallel. With full balanced differential architecture, these mixers are driven by an accurate internal Local Oscillator (LO) chain as described later. Phase and gain accuracy of the output baseband signals are excellent and are a function of the combination of LO accuracy, balanced device design and layout characteristics. Mainly used for down conversion, its input frequency response exceeds 400MHz with a differential voltage gain of 2.5. With a differential input impedance of 1KΩ, the input compression point exceeds $2V_{P-P}$, which makes it suitable for use with the hard limiting output from the limiter amplifier chain or any low power external AGC application. The output frequency response is limited to 30MHz for "I" and "Q" baseband signals driving a 4KΩ differential load.

The HFA3724 down conversion mixers can generate two 10MHz, 90° apart signals, with the use of proper low pass filtering, and exhibits ±4° and ±0.5dB of phase and amplitude match for a input CW IF signal of 400MHz and a 2XLO input of 780MHz.

LO Quadrature Generator

The In Phase and Quadrature reference signals are generated by a divide by two chain internal to the device which drives both the up and down conversion mixers. With a fully balanced approach, the phase relationship between the two quadrature signals is within 90° ±4° for a wide 10 to 400MHz frequency range. The reference signal input frequency needs to be twice the desired internal reference frequency. The ground referenced 2XLO input is current driven, which makes the input power requirement a function of external components that can be calculated assuming the input impedance of 130Ω. A typical input current value of $200\mu A_{RMS}$ is the only requirement for reliable LO generation. Figure 25 shows a typical 2XLO input network.

Divide by two flip flop architectures for LO generation often require tight control of signal purity or duty cycles. The HFA3724 has an internal duty cycle compensation scheme which eases the requirements of tight controlled duty cycles.

In addition, a 50Ω LO buffer is available to the user for PLL's design reference. It substitutes a divide by two prescaler needed to bring the 2X LO frequency reference down. It is capable to drive $100mV_{P-P}$ into 50Ω and its frequency response is from 10MHz to 400MHz corresponding to a 2XLO input frequency response of 20MHz to 800MHz. The LO buffer can be disabled by removing the ground connection to the pin LO GND. The quadrature generator is always enabled for either transmit or receive modes.

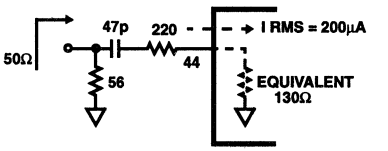


FIGURE 25. MOD LO IN (2XLO) EQUIVALENT CIRCUIT

Quadrature Up Converter

The Quadrature up converter mixers are also based on a doubly balanced Gilbert Cell design. "I" and "Q" Up converter signals are summed and buffered together through a single end open collector stage. As with the demodulators, both modulator mixers are driven from the same quadrature LO generator. It features a ±4° and 0.5dB of phase and amplitude balance up to 400MHz which are reflected into its SSB characteristics. For "I" and "Q" differential inputs of $500mV_{P-P}$, 90° apart, the carrier feedthrough or LO leakage is typical -30dBc into 250Ω with a sideband suppression of minimum 26dBc at 400MHz. Carrier feedthrough can be further improved by disabling the LO output port (please refer to pin#50 description) or using a DC bias network as in Figure 26. Featuring an output compression level of $1V_{P-P}$, the modulator output can generate a CW signal of typical -10dbm into 250Ω ($158mV_{RMS}$) when differential DC inputs of $500mV_{P-P}$ (equivalent to applying ±125mV ground referenced levels from the DC bias quiescent point of the device input) are applied to both "I" and "Q" inputs. Four quadrant phase shifts of the carrier output, like in Vector Modulator applications, can be set by proper choice of "I" and "Q" DC differential inputs, such that the square root of the sum of the squares of I and Q is constant.

Although specified to drive a 250Ω load, the HFA3724 modulator open collector output enables user designed output matching networks to suit any application interface.

The nominal AC current capability of this port is of $1.3mA_{RMS}$, which is shared between the termination resistor and the load for I and Q differential DC inputs of $500mV_{P-P}$ as explained above. (Use 70.7% of this AC capability for I and Q quadrature signals in case of SSB generation).

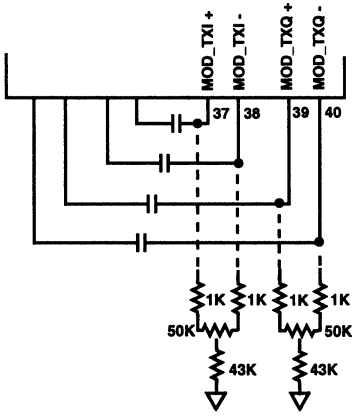


FIGURE 26. CARRIER NULL BIASING

Programmable Low Pass Filters

These filters are implemented using a 5th order Butterworth architecture. They are multiplexed, i.e., the same filter bank is used for both transmit and receive modes.

The filter block, in the transmit mode is set to accept digital (TTL threshold) input data for "I" and "Q" signals and is programmable with 4 frequency cutoffs: (2.2MHz, 4.4MHz, 8.8MHz and 17.8MHz). Digital control pins are used to switch all programmed cutoff modes. The user can design a multi data rate transceiver or simply hardwire these inputs. An external resistor is used to fine tune the cut off frequencies for each setting within ±20% of the nominal value. This feature is often needed to fulfill requirements of spectral mask compliance at the antenna output.

The "I" and "Q" filter matching is within 2^o for phase and 0.25dB for amplitude at the passband. Group delay characteristics follow closely a theoretical 5th order Butterworth design.

When in the receive mode, the filters exhibit a 0dB of gain with differential inputs and single ended outputs.

In the transmit mode, the digital ground referenced "I" and "Q" input signals are level shifted, shaped and buffered with constant driving differential outputs of $550mV_{P-P}$.

Baseband Digital Interfacing

Special precautions must be taken when interfacing the HFA3724 to a digital baseband processor: Large TTL signal swings, overshoots and current spikes, must be carefully considered when dealing with the generation of analog spread spectrum signals which are relatively much smaller in energy per bandwidth.

In order to avoid distortion or spurious tones on the analog transmit path, it may be necessary to decrease and/or limit digital excursions as much as possible without compromising the specifications. Figure 27 shows a simplified block diagram of the Transmit digital inputs.

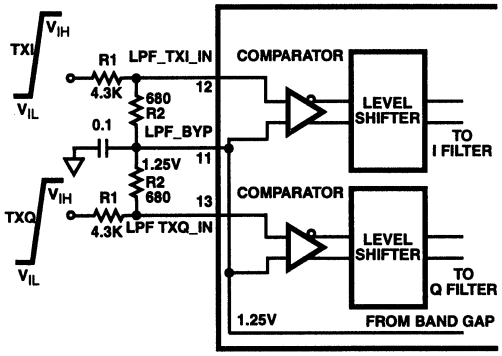


FIGURE 27. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT DIGITAL INPUTS

Because of the input comparators high gain, a small overdrive of about ±150mV from the reference level of 1.25V is all what is needed to reliably switch and level shift the "I" and "Q" digital signals. An external attenuator comprising of R1 and R2 with termination in the available 1.25V reference voltage pin (LPF BYP) can be calculated based on expected V_{IH} and V_{IL} inputs from a digital interface. Capacitive coupling must be avoided which could affect rise and fall times needed for proper overdrive speed of the comparators. Limiting the digital excursion on those pins greatly reduce the possibility of signal corruption at the transmit chain.

Coupling Capacitors

Capacitor coupling is used to tie all HFA3724 blocks together. Special bias is used to maintain the DC levels on both ends of coupling pins (capacitors) when the device is changes from Transmitter to a Receiver and vice versa. The capacitance values must be chosen as a compromise to maintain proper frequency response and settling times (when the device is brought up from sleep mode or power down).

AC Electrical Specifications, IF Limiter, Single Stage Individual Performance Full Supply Range, $T_A = 25^oC$

PARAMETER	SYMBOL	(NOTE 27) TEST LEVEL	MIN	TYP	MAX	UNITS
IF Frequency Range (Min Limited by Bypass Capacitors)	IFf	A	-	-	400	MHz
IF Voltage Gain	IFvG	A	39	45	-	dB
IF Amp. Noise Figure at 250Ω Source Input	IFNF	B	-	-	7	dB
Maximum IF Input, Single Ended	IFinmax	B	-	-	500	mV_{P-P}
IF Differential Limiting Output (1st Harmonic at 500Ω Load)	IFVpp	A	160	200	260	mV_{P-P}
IF Voltage Output Variation at -40dBm to -10dBm Input Range, 500Ω Load	IFVppl	A	-0.5	-	+0.5	dB
RSSI Slope, Current Output	IFRSSIsi	B		5.7	-	µA/dB
RSSI Slope, Voltage Output at 6K Load	IFRSSIv	A	25	34	45	mV/dB
RSSI Output Voltage Compliance	IFRSSIvc	B	-	-	V_{CC}- 0.7	V
RSSI DC Offset and Noise Induced Voltage at 6K Load	IFRSSIof	A	200	400	600	mV
RSSI Absolute Accuracy, V_{IN} = -40dBm	IFRSSIa	A	-10	-	+10	%
RSSI Rise and Fall Time at 50pF Load (-20dBm to -40dBm Input)	IFRSSIt	B	-	-	1	µs

NOTE:

27. A = Production Tested, B = Based on Characterization, C = By Design

TABLE 3. IF LIMITER S11, S22 PARAMETER

FREQUENCY	S11 (SINGLE ENDED)		S22 (DIFFERENTIAL)	
50MHz	0.96	-4.0°	0.45	0.0°
100MHz	0.95	-8.0°	0.45	3.0°
200MHz	0.91	-17.0°	0.47	7.0°
300MHz	0.84	-26.0°	0.50	9.0°
400MHz	0.80	-33.0°	0.53	10.0°

AC Electrical Specifications, I/Q Down Converter Individual Performance Full Supply Range, $T_A = 25^oC$

PARAMETER	SYMBOL	(NOTE 28) TEST LEVEL	MIN	TYP	MAX	UNITS
Quadrature Demodulator Input Frequency Range	QDf	B	10	-	400	MHz
Demodulator Baseband I/Q Frequency Range	QDIQf	C	-	-	30	MHz
Demodulator Voltage Gain at Frequency Range	QDg	A	6	8	9	dB
Demodulator Differential Input Resistance	Drin	C	-	1	-	kΩ
Demodulator Differential Input Capacitance	Dcin	C	-	0.5	-	pF

AC Electrical Specifications, I/Q Down Converter Individual Performance Full Supply Range, $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	(NOTE 28) TEST LEVEL	MIN	TYP	MAX	UNITS
Demodulator Differential Output Level at 4K Load, Input = $200mV_{P-P}$	QDdo	A	400	500	560	mV_{P-P}
Demodulator Amplitude Balance	QDab	A	-0.5	-	0.5	dB
Demodulator Phase Balance at 200MHz	QDpb	A	-1.85	-	1.85	Degrees
Demodulator Phase Balance at 400MHz	QDPb1	B	-4	-	4	Degrees
Demodulator Output Compression Voltage at 4K Load	QDoc	B	-	1.25	-	V_{P-P}

NOTE:

28. A = Production Tested, B = Based on Characterization, C = By Design

AC Electrical Specifications, I/Q Up Converter and LO Individual Performance Full Supply Range, $T_A = 25^oC$

PARAMETER	SYMBOL	(NOTE 29) TEST LEVEL	MIN	TYP	MAX	UNITS
2XLO Input Frequency Range (2 X Input Range)	LOinf	B	20	-	800	MHz
2XLO Input Current Range	LOinz	C	50	200	300	μA_{RMS}
2XLO Input Impedance	LOz	C	-	130	-	Ω
Buffered LO Output Voltage, Single Ended	BLOout	A	80	100	-	mV_{P-P}
Buffered LO Output Impedance	BLOoutZ	C	-	50	-	Ω
Quadrature IF Modulator Output Frequency Range	QMLOf	B	10	-	400	MHz
IF Modulator I/Q Input Frequency Range	QMIQf	C	-	-	30	MHz
IF Modulator Differential I/Q Max Input Voltage	QMdi	C	-	2.25	-	V_{P-P}
IF Modulator Differential I/Q Input Impedance	QMIQdz	C	-	4	-	kΩ
IF Modulator Differential Input Capacitance	Mcin	C	-	0.5	-	pF
IF Modulator I/Q Amplitude Balance	QMIQac	A	-0.5	-	0.5	dB
IF Modulator I/Q Phase Balance at 200MHz	QMIQpac	A	-2	-	2	Degrees
IF Modulator I/Q Phase Balance at 400MHz	QMIQp1	B	-4	-	4	Degrees
IF Modulator Output at SSB Into 50Ω, I and Q, $500mV_{P-P}$	QMIFo	A	-22	-	-10.0	dBm
IF Modulator Carrier Suppression (LO Buffer Enabled)	QMCs	A	28	30	-	dBc
IF Modulator Carrier Suppression (LO Buffer Disabled)	QMCs1	A	28	36	-	dBc
IF Modulator SSB Sideband Suppression at 200MHz	QMSSBs	A	28	-	-	dBc
IF Modulator SSB Sideband Suppression at 400MHz	QMSSBs	B	26	-	-	dBc
IF Output Level Compression Point	QMIFP1	C	-	1.0	-	V_{P-P}
IF Modulator Intermodulation Suppression	QMIMsup	B	26	-	-	dBc

NOTE:

29. A = Production Tested, B = Based on Characterization, C = By Design

TABLE 4. QUADRATURE MODULATOR S22 PARAMETER

FREQUENCY	S22	
50MHz	0.99	-2.8°
100MHz	0.98	-6.5°
200MHz	0.96	-12.3°
300MHz	0.87	-25.1°
400MHz	0.82	-30.8°

AC Electrical Specifications, TX Buffer Individual Performance Full Supply Range, $T_A = 25°C$

PARAMETER	SYMBOL	(NOTE 30) TEST LEVEL	MIN	TYP	MAX	UNITS
TX LPF Buffer Serial Data Rate	TXBrat	A	-	11	22	MBPS
TX LPF Buffer Digital Input Impedance	LPFDz	C	10	12.5	-	kΩ

NOTE:

30. A = Production Tested, B = Based on Characterization, C = By Design

AC Electrical Specifications, RX/TX 5TH Order LPF Individual Performance Full Supply Range, $T_A = 25°C$

PARAMETER	SYMBOL	(NOTE 31) TEST LEVEL	MIN	TYP	MAX	UNITS
TX/RX LPF 3dB Bandwidth, Sel0 = 0, Sel1 = 0	LPF3db0	A	1.8	2.20	2.4	MHz
TX/RX LPF 3dB Bandwidth, Sel0 = 1, Sel1 = 0	LPF3db1	A	3.6	4.40	4.8	MHz
TX/RX LPF 3dB Bandwidth, Sel0 = 0, Sel1 = 1	LPF3db2	A	7.4	8.80	9.6	MHz
TX/RX LPF 3dB Bandwidth, Sel0 = 1, Sel1 = 1	LPF3db3	A	14.8	17.60	19.2	MHz
TX/RX LPF Sel0, Sel1 Tuning Speed	LPFsp	B	-	-	1	µs
TX/RX LPF 3dB Bandwidth Tuning	LPFtu	A	-20	-	+20	%
LPF Tune Nominal Resistance	LPFTr	B	-	787	-	Ω
RX LPF Voltage Gain	LPFg	A	-1.0	0	1.0	dB
RX LPF Single Ended Output Voltage Swing at 2kΩ Load	LPFRXar	B	-	500	-	mV_{P-P}
RX LPF Differential Input Impedance	LPFRXzi	A	4	5	-	kΩ
TX LPF Differential Digital Output Voltage Swing at 4kΩ Load	LPFTXo	A	450	550	670	mV_{P-P}
TX/RX I/Q Channel Amplitude Match	LPFIQm	A	-0.5	-	0.5	dB
TX/RX I/Q Channel Phase Match	LPFIQpm	A	-3	-	3	Degrees
TX/RX LPF Total Harmonic Distortion	LPFTHD	B	-	3	-	%

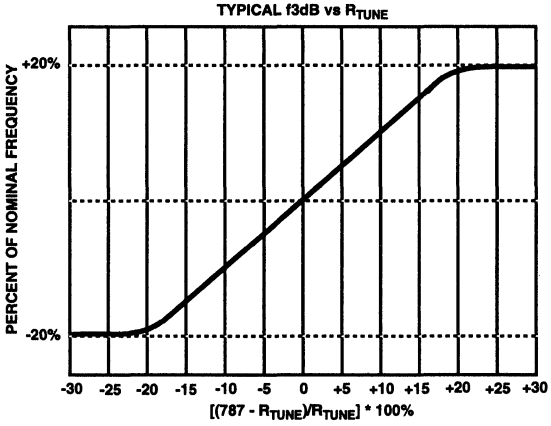
NOTE:

31. A = Production Tested, B = Based on Characterization, C = By Design

TABLE 5. LOW PASS FILTER PROGRAMMING AND TUNING INFORMATION

MODE	LPF SEL1	LPF SEL0	f_{3dB} (NOMINAL R_{TUNE})
BW0	0	0	2.2MHz
BW1	0	1	4.4MHz
BW2	1	0	8.8MHz
BW3	1	1	17.6MHz

$$f_{TUNED3dB} = \frac{f_{3dBNOMINAL} * 787}{R_{TUNE}}$$



FREQUENCY	R_{TUNE}
20% Low	984Ω
Nominal	787Ω
20% High	656Ω

FIGURE 28.

Typical Performance Curves, Individual Blocks

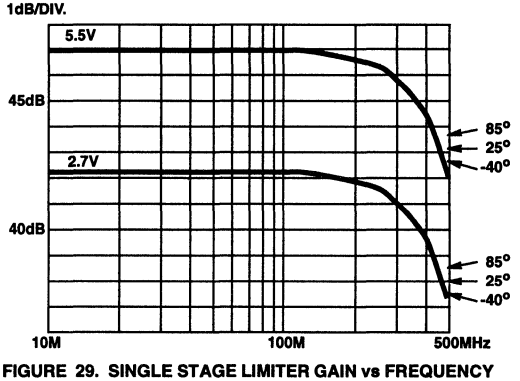


FIGURE 29. SINGLE STAGE LIMITER GAIN vs FREQUENCY AND TEMPERATURE, V_{CC} = 2.7V, 5.5V

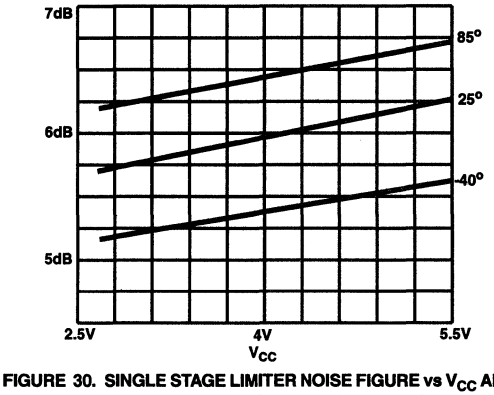


FIGURE 30. SINGLE STAGE LIMITER NOISE FIGURE vs V_{CC} AND TEMPERATURE, RS = 250Ω, FREQUENCY = 300MHz

HARRIS SEMICONDUCTOR

HSP3824

Direct Sequence Spread Spectrum Baseband Processor

January 1997

Features

- Complete DSSS Baseband Processor
- High Data Rate.....up to 4 MBPS
- Processing Gain .....up to 12dB
- Programmable PN Code ..... up to 16 Bits
- Ultra Small Package .....7 x 7 x 1mm
- Single Supply Operation (33MHz Max) . . 2.7V to 5.5V
- Single Supply Operation (44MHz Max) . . 3.3V to 5.0V
- Modulation Method.....DBPSK or DQPSK
- Supports Full or Half Duplex Operations
- On-Chip A/D Converters for I/Q Data (3-Bit, 44 MSPS) and RSSI (6-Bit, 2 MSPS)

Applications

- Systems Targeting IEEE802.11 Standard
- DSSS PCMCIA Wireless Transceiver
- Spread Spectrum WLAN RF Modems
- TDMA Packet Protocol Radios
- Part 15 Compliant Radio Links
- Portable Bar Code Scanners/POS Terminal
- Portable PDA/Notebook Computer
- Wireless Digital Audio
- Wireless Digital Video
- PCN/Wireless PBX

Description

PRISM™

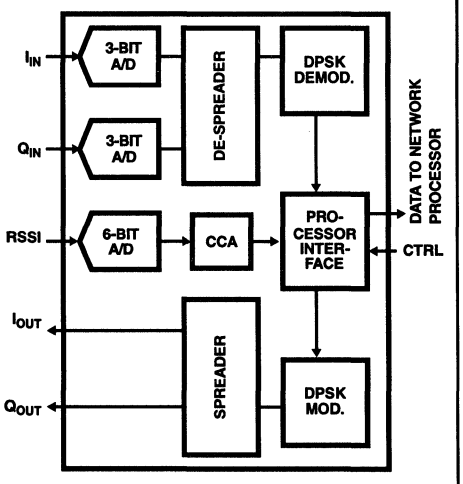
The Harris HSP3824 Direct Sequence (DSSS) baseband processor is part of the PRISM™ 2.4GHz radio chipset, and contains all the functions necessary for a full or half duplex packet baseband transceiver.

The HSP3824 has on-board ADC's for analog I and Q inputs, for which the HFA3724 IF QMODEM is recommended. Differential phase shift keying modulation schemes DBPSK and DQPSK, with optional data scrambling capability, are combined with a programmable PN sequence of up to 16 bits. Built-in flexibility allows the HSP3824 to be configured through a general purpose control bus, for a wide range of applications. A Receive Signal Strength Indicator (RSSI) monitoring function with on-board 6-bit 2 MSPS ADC provides Clear Channel Assessment (CCA) to avoid data collisions and optimize network throughput. The HSP3824 is housed in a thin plastic quad flat package (TQFP) suitable for PCMCIA board applications.

Ordering Information

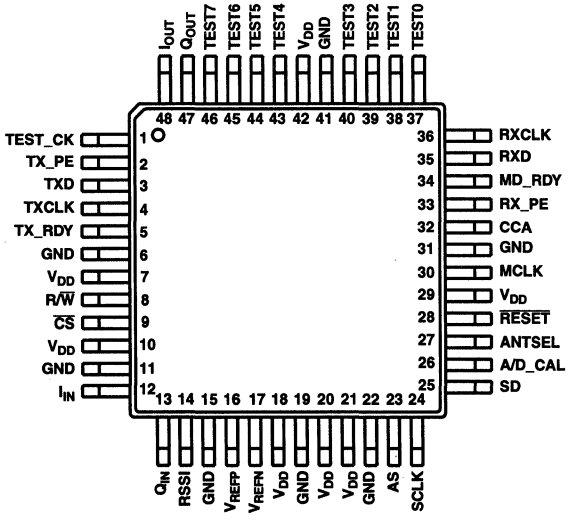
PART NO.	TEMP. RANGE (°C)	PKG. TYPE	PKG. NO.
HSP3824VI	-40 to 85	48 Ld TQFP	Q48.7x7
HFA3824VI96	-40 to 85	Tape and Reel	

Simplified Block Diagram



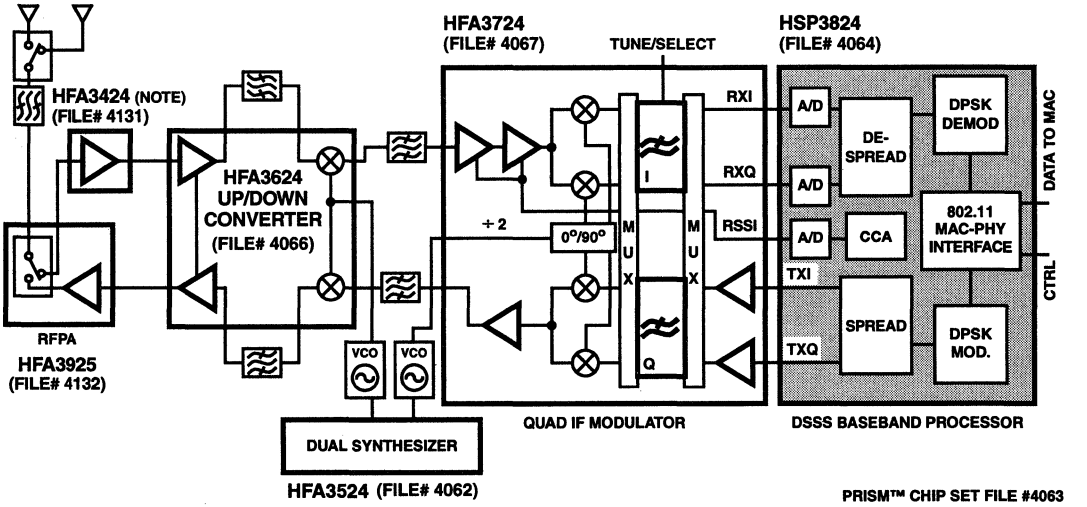
Pinout

HSP3824 (TQFP)



List of Contents

Typical Application Diagram



TYPICAL TRANSCEIVER APPLICATION CIRCUIT USING THE HSP3824

NOTE: Required for systems targeting 802.11 specifications.

For additional information on the PRISM™ chip set, call (407) 724-7800 to access Harris' AnswerFAX system. When prompted, key in the four-digit document number (File #) of the datasheets you wish to receive.

The four-digit file numbers are shown in Typical Application Diagram, and correspond to the appropriate circuit.

Pin Description

NAME	PIN	TYPE I/O	DESCRIPTION
V_{DD} (Analog)	10, 18, 20	Power	DC power supply 2.7V - 5.5V
V_{DD} (Digital)	7, 21, 29, 42	Power	DC power supply 2.7V - 5.5V
GND (Analog)	11, 15, 19	Ground	DC power supply 2.7V - 5.5V, ground.
GND (Digital)	6, 22, 31, 41	Ground	DC power supply 2.7V - 5.5V, ground.
V_{REFN}	17	I	"Negative" voltage reference for ADC's (I and Q) [Relative to V_{REFP}]
V_{REFP}	16	I	"Positive" voltage reference for ADC's (I, Q and RSSI)
I_{IN}	12	I	Analog input to the internal 3-bit A/D of the In-phase received data.
Q_{IN}	13	I	Analog input to the internal 3-bit A/D of the Quadrature received data.
RSSI	14	I	Receive Signal Strength Indicator Analog input.
A/D_CAL	26	O	This signal is used internally as part of the I and Q ADC calibration circuit. When the ADC calibration circuit is active, the voltage references of the ADCs are adjusted to maintain the outputs of the ADCs in their optimum range. A logic 1 on this pin indicates that one or both of the ADC outputs are at their full scale value. This signal can be integrated externally as a control voltage for an external AGC.
TX_PE	2	I	When active, the transmitter is configured to be operational, otherwise the transmitter is in standby mode. TX_PE is an input from the external Media Access Controller (MAC) or network processor to the HSP3824. The rising edge of TX_PE will start the internal transmit state machine and the falling edge will inhibit the state machine. TX_PE envelopes the transmit data.
TXD	3	I	TXD is an input, used to transfer serial Data or Preamble/Header information bits from the MAC or network processor to the HSP3824. The data is received serially with the LSB first. The data is clocked in the HSP3824 at the falling edge of TXCLK.
TXCLK	4	O	TXCLK is a clock output used to receive the data on the TXD from the MAC or network processor to the HSP3824, synchronously. Transmit data on the TXD bus is clocked into the HSP3824 on the falling edge. The clocking edge is also programmable to be on either phase of the clock. The rate of the clock will be depending upon the modulation type and data rate that is programmed in the signalling field of the header.
TX_RDY	5	O	When the HSP3824 is configured to generate the preamble and Header information internally, TX_RDY is an output to the external network processor indicating that Preamble and Header information has been generated and that the HSP3824 is ready to receive the data packet from the network processor over the TXD serial bus. The TX_RDY returns to the inactive state when the TX_PE goes inactive indicating the end of the data transmission. TX_RDY is an active high signal. This signal is meaningful only when the HSP3824 generates its own preamble.
CCA	32	O	Clear Channel Assessment (CCA) is an output used to signal that the channel is clear to transmit. The CCA algorithm is user programmable and makes its decision as a function of RSSI, Energy detect (ED), Carrier Sense (CRS) and the CCA watch dog timer. The CCA algorithm and its programmable features are described in the data sheet. Logic 0 = Channel is clear to transmit. Logic 1 = Channel is NOT clear to transmit (busy). NOTE: This polarity is programmable and can be inverted.
RXD	35	O	RXD is an output to the external network processor transferring demodulated Header information and data in a serial format. The data is sent serially with the LSB first. The data is frame aligned with MD_RDY.
RXCLK	36	O	RXCLK is the clock output bit clock. This clock is used to transfer Header information and data through the RXD serial bus to the network processor. This clock reflects the bit rate in use.RXCLK will be held to a logic "0" state during the acquisition process. RXCLK becomes active when the HSP3824 enters in the data mode. This occurs once bit sync is declared and a valid signal quality estimate is made, when comparing the programmed signal quality thresholds.

Pin Description (Continued)

NAME	PIN	TYPE I/O	DESCRIPTION
MD_RDY	34	O	MD_RDY is an output signal to the network processor, indicating a data packet is ready to be transferred to the processor. MD_RDY is an active high signal and it envelopes the data transfer over the RXD serial bus. MD_RDY returns to its inactive state when there is no more receiver data, when the programmable data length counter reaches its value or when the link has been interrupted. MD_RDY remains inactive during preamble synchronization.
RX_PE	33	I	When active, receiver is configured to be operational, otherwise receiver is in standby mode. This is an active high input signal.
ANTSEL	27	O	The antenna select signal changes state as the receiver switches from antenna to antenna during the acquisition process in the antenna diversity mode.
SD	25	I/O	SD is a serial bi-directional data bus which is used to transfer address and data to/from the internal registers. The bit ordering of an 8-bit word is MSB first. The first 8 bits during transfers indicate the register address immediately followed by 8 more bits representing the data that needs to be written or read at that register.
SCLK	24	I	SCLK is the clock for the SD serial bus.The data on SD is clocked at the rising edge. SCLK is an input clock and it is asynchronous to the internal master clock (MCLK)The maximum rate of this clock is 10MHz or the master clock frequency, whichever is lower.
AS	23	I	AS is an address strobe used to envelope the Address or the data on SD. Logic 1 = envelopes the address bits. Logic 0 = envelopes the data bits.
R/$\overline{W}$	8	I	R/$\overline{W}$ is an input to the HSP3824 used to change the direction of the SD bus when reading or writing data on the SD bus. R/$\overline{W}$ must be set up prior to the rising edge of SCLK. A high level indicates read while a low level is a write.
$\overline{CS}$	9	I	$\overline{CS}$ is a Chip select for the device to activate the serial control port.The $\overline{CS}$ doesn't impact any of the other interface ports and signals, i.e. the TX or RX ports and interface signals. This is an active low signal. When inactive SD, SCLK, AS and R/$\overline{W}$ become "don't care" signals.
TEST 0-7	37, 38, 39, 40, 43, 44, 45, 46	O	This is a data port that can be programmed to bring out internal signals or data for monitoring. This data includes: Correlator phase and magnitude, NCO frequency offset estimate, and signal quality estimates. Some of the discrete signals available include: Carrier Sense (CRS), which becomes active when initial PN acquisition has been declared. Energy Detect (ED) which becomes active when the integrated RSSI value exceeds the programmable threshold. Both ED and CRS are active high signals.These bits are primarily reserved by the manufacturer for testing. A further description of the test port is given at the appropriate section of this data sheet.
TEST_CK	1	O	This is the clock that is used in conjunction with the data that is being output from the test bus (TEST 0-7).
$\overline{RESET}$	28	I	Master reset for device. When active TX and RX functions are disabled. If $\overline{RESET}$ is kept low the HSP3824 goes into the power standby mode. $\overline{RESET}$ does not alter any of the configuration register values nor it presets any of the registers into default values. Device requires programming upon power-up. $\overline{RESET}$ must be inactive during programming of the device.
MCLK	30	I	Master Clock for device. The maximum frequency of this clock is 44MHz. This is used internally to generate all other internal necessary clocks and is divided by 1, 2, 4, or 8 for the transceiver clocks.
I_{OUT}	48	O	TX Spread baseband I digital output data. Data is output at the programmed chip rate.
Q_{OUT}	47	O	TX Spread baseband Q digital output data. Data is output at the programmed chip rate.

NOTE: Total of 48 pins; ALL pins are used.

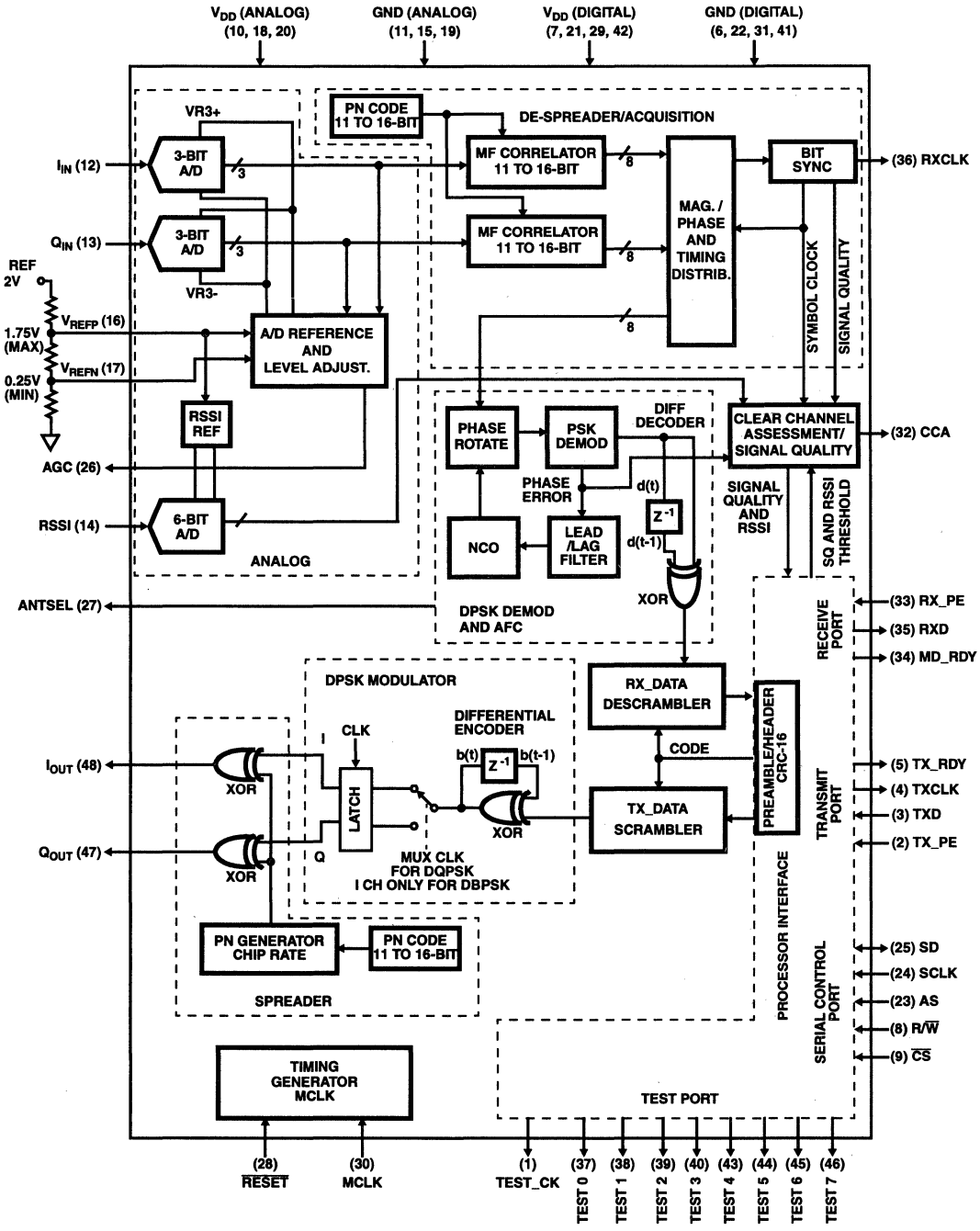


FIGURE 1. DSSS BASEBAND PROCESSOR

External Interfaces

There are three primary digital interface ports for the HSP3824 that are used for configuration and during normal operation of the device. These ports are:

- The **TX Port**, which is used to accept the data that needs to be transmitted from the network processor.
- The **RX Port**, which is used to output the received demodulated data to the network processor.
- The **Control Port**, which is used to configure, write and/or read the status of the internal HSP3824 registers.

In addition to these primary digital interfaces the device includes a byte wide parallel **Test Port** which can be configured to output various internal signals and/or data (i.e. PN acquisition indicator, Correlator magnitude output etc.). The device can also be set into various power consumption modes by external control. The HSP3824 contains three Analog to Digital (A/D) converters. The analog interfaces to the HSP3824 include, the In phase (I) and quadrature (Q) data component inputs, and the RF signal strength indicator input. A reference voltage divider is also required external to the device.

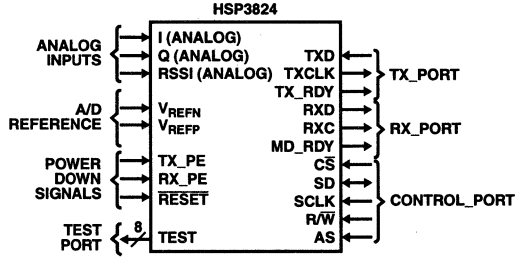
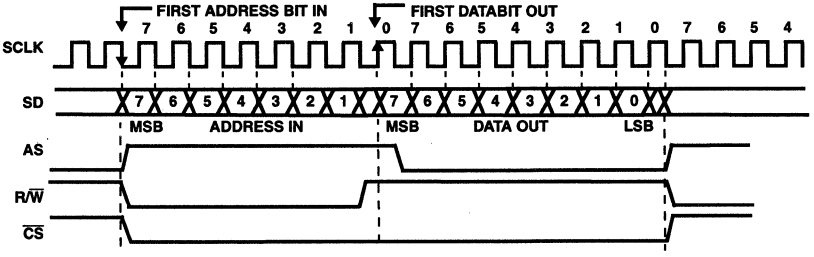


FIGURE 2. EXTERNAL INTERFACES

Control Port

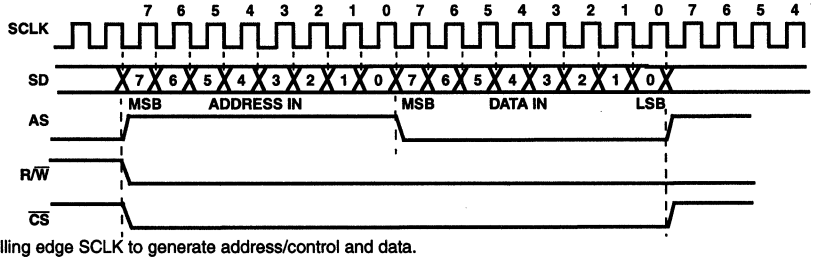
The serial control port is used to serially write and read data to/from the device. This serial port can operate up to a 10MHz rate or the maximum master clock rate of the device, MCLK (whichever is lower). MCLK must be running and $\overline{RESET}$ inactive during programming. This port is used to program and to read all internal registers. The first 8 bits always represent the address followed immediately by the 8 data bits for that register. The two LSBs of address are don't care. The serial transfers are accomplished through the serial data pin (SD). SD is a bidirectional serial data bus. An Address Strobe (AS), Chip Select ($\overline{CS}$), and Read/$\overline{Write}$ (R/$\overline{W}$) are also required as handshake signals for this port. The clock used in conjunction with the address and data on SD is SCLK. This clock is provided by the external source and it is an input to the HSP3824. The timing relationships of these signals are illustrated on Figure 3 and 4. AS is active high during the clocking of the address bits. R/$\overline{W}$ is high when data is to be read, and low when it is to be written. $\overline{CS}$ must be active (low) during the entire data transfer cycle. $\overline{CS}$ selects the device. The serial control port operates asynchronously from the TX and RX ports and it can accomplish data transfers independent of the activity at the other digital or analog ports. $\overline{CS}$ does not effect the TX or RX operation of the device; impacting only the operation of the Control port. The HSP3824 has 57 internal registers that can be configured through the control port. These registers are listed in the Configuration and Control Internal Register table. Table 1 lists the configuration register number, a brief name describing the register, and the HEX address to access each of the registers. The type indicates whether the corresponding register is Read only (R) or Read/Write (R/W). Some registers are two bytes wide as indicated on the table (high and low bytes).



NOTES:

1. Using falling edge SCLK to generate address/control and capture read data.
2. The $\overline{CS}$ is a synchronous interface in reference to SCLK. There is at least one clock required before $\overline{CS}$ transitions to its active state.

FIGURE 3. CONTROL PORT READ TIMING



NOTE: Using falling edge SCLK to generate address/control and data.

FIGURE 4. CONTROL PORT WRITE TIMING

TABLE 1. CONFIGURATION AND CONTROL INTERNAL REGISTER LIST

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX
CR0	Modem Config. Register A	R/W	00
CR1	Modem Config. Register B	R/W	04
CR2	Modem Config. Register C	R/W	08
CR3	Modem Config. Register D	R/W	0C
CR4	Internal Test Register A	R/W	10
CR5	Internal Test Register B	R/W	14
CR6	Internal Test Register C	R	18
CR7	Modem Status Register A	R	1C
CR8	Modem Status Register B	R	20
CR9	I/O Definition Register	R/W	24
CR10	RSSI Value Register	R	28
CR11	ADC_CAL_POS Register	R/W	2C
CR12	ADC_CAL_NEG Register	R/W	30
CR13	TX_Spread Sequence (High)	R/W	34
CR14	TX_Spread Sequence (Low)	R/W	38
CR15	Scramble_Seed	R/W	3C
CR16	Scramble_Tap (RX and TX)	R/W	40
CR17	CCA_Timer_TH	R/W	44
CR18	CCA_Cycle_TH	R/W	48
CR19	RSSI_TH	R/W	4C
CR20	RX_Spread Sequence (High)	R/W	50
CR21	RX_Spread Sequence (Low)	R/W	54
CR22	RX_SQ1_ ACQ (High) Threshold	R/W	58
CR23	RX-SQ1_ ACQ (Low) Threshold	R/W	5C
CR24	RX-SQ1_ ACQ (High) Read	R	60
CR25	RX-SQ1_ ACQ (Low) Read	R	64
CR26	RX-SQ1_ Data (High) Threshold	R/W	68
CR27	RX-SQ1-SQ1_ Data (Low) Threshold	R/W	6C
CR28	RX-SQ1_ Data (High) Read	R	70
CR29	RX-SQ1_ Data (Low) Read	R	74
CR30	RX-SQ2_ ACQ (High) Threshold	R/W	78
CR31	RX-SQ2- ACQ (Low) Threshold	R/W	7C
CR32	RX-SQ2_ ACQ (High) Read	R	80

TABLE 1. CONFIGURATION AND CONTROL INTERNAL REGISTER LIST (Continued)

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX
CR33	RX-SQ2_ ACQ (Low) Read	R	84
CR34	RX-SQ2_Data (High) Threshold	R/W	88
CR35	RX-SQ2_Data (Low) Threshold	R/W	8C
CR36	RX-SQ2_Data (High) Read	R	90
CR37	RX-SQ2_Data (Low) Read	R	94
CR38	RX_SQ_Read; Full Protocol	R	98
CR39	Reserved (must load 00h)	W	9C
CR40	Reserved (must load 00h)	W	A0
CR41	UW_Time Out_Length	R/W	A4
CR42	SIG_DBPSK Field	R/W	A8
CR43	SIG_DQPSK Field	R/W	AC
CR44	RX_SER_Field	R	B0
CR45	RX_LEN Field (High)	R	B4
CR46	RX_LEN Field (Low)	R	B8
CR47	RX_CRC16 (High)	R	BC
CR48	RX_CRC16 (Low)	R	C0
CR49	UW (High)	R/W	C4
CR50	UW (Low)	R/W	C8
CR51	TX_SER_F	R/W	CC
CR52	TX_LEN (High)	R/W	D0
CR53	TX_LEN (LOW)	R/W	D4
CR54	TX_CRC16 (HIGH)	R	D8
CR55	TX_CRC16 (LOW)	R	DC
CR56	TX_PREM_LEN	R/W	E0

TX Port

The transmit data port accepts the data that needs to be transmitted serially from an external data source. The data is modulated and transmitted as soon as it is received from the external data source. The serial data is input to the HSP3824 through TXD using the falling edge of TXCLK to clock it in the HSP3824. TXCLK is an output from the HSP3824. A timing scenario of the transmit signal handshakes and sequence is shown on timing diagram Figures 5 and 6.

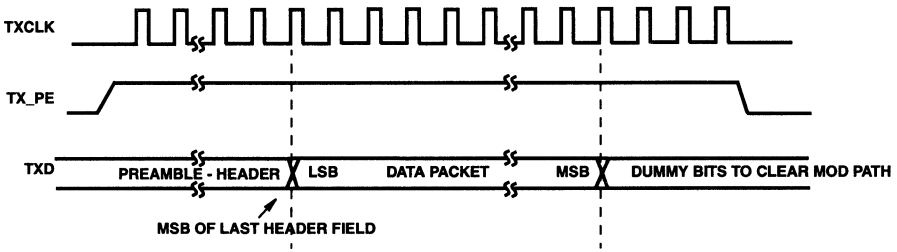
The external processor initiates the transmit sequence by asserting TX_PE. TX_PE envelopes the transmit data packet on TXD. The HSP3824 responds by generating TXCLK to input the serial data on TXD. TXCLK will run until TX_PE goes back to its inactive state indicating the end of the data packet. There are two possible transmit scenarios.

One scenario is when the HSP3824 internally generates the preamble and header information. During this mode the external source needs to provide only the data portion of the packet. The timing diagram of this mode is illustrated on Figure 6. When the HSP3824 generates the preamble internally, assertion of TX_PE will initialize the generation of the preamble and header. TX_RDY, which is an output from the HSP3824, is used to indicate to the external processor that the preamble has been generated and the device is ready to receive the data packet to be transmitted from the external processor. The TX_RDY timing is programmable in case the external processor needs several clocks of advanced notice before actual data transmission is to begin.

The second transmit scenario supported by the HSP3824 is when the preamble and header information are provided by the external data source. During this mode TX_RDY is not required as part of the TX handshake. The HSP3824 will immediately start transmitting the data available on TXD upon assertion of TX_PE. The timing diagram of this TX scenario, where the preamble and header are generated external to the HSP3824, is illustrated on Figure 5.

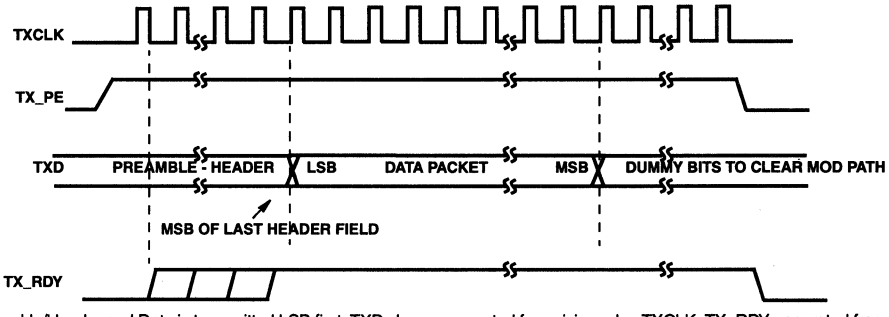
One other signal that can be used for certain applications as part of the TX interface is the Clear Channel Assessment (CCA) signal which is an output from the HSP3824. The CCA is programmable and it is described with more detail in the Transmitter section of this document. CCA provides the indication that the channel is clear of energy and the transmission will not be subject to collisions. CCA can be monitored by the external processor to assist in deciding when to initiate transmissions. The CCA indication can bypassed or ignored by the external processor. The state of the CCA does not effect the transmit operation of the HSP3824. TX_PE alone will always initiate the transmit state independent of the state of CCA. Signals TX_RDY, TX_PE and TXCLK can be set individually, by programming Configuration Register (CR) 9, as either active high or active low signals.

The transmit port is completely independent from the operation of the other interface ports including the RX port, therefore supporting a full duplex mode.



NOTE: Preamble/Header and Data is transmitted LSB first TX_RDY is inactive Logic 0 when generated externally. TXD shown generated from rising edge TXCLK.

FIGURE 5. TX PORT TIMING (EXTERNAL PREAMBLE)



NOTE: Preamble/Header and Data is transmitted LSB first. TXD shown generated from rising edge TXCLK. TX_RDY generated from falling edge.

FIGURE 6. TX PORT TIMING (INTERNAL PREAMBLE)

RX Port

The timing diagram Figure 7 illustrates the relationships between the various signals of the RX port. The receive data port serially outputs the demodulated data from RXD. The data is output as soon as it is demodulated by the HSP3824. RX_PE must be at its active state throughout the receive operation. When RX_PE is inactive the device's receive functions, including acquisition, will be in a stand by mode.

RXCLK is an output from the HSP3824 and is the clock for the serial demodulated data on RXD. MD_RDY is an output from the HSP3824 and it envelopes the valid data on RXD. The HSP3824 can be also programmed to ignore error detections during the CCITT - CRC 16 check of the header fields. If programmed to ignore errors the device continues to output the demodulated data in its entirety regardless of the CCITT - CRC 16 check result. This option is programmed through CR 2, bit 5.

Note that RXCLK becomes active after acquisition, well before valid data begins to appear on RXD and MD_RDY is asserted. MD_RDY returns to its inactive state under the following conditions:

- The number of data symbols, as defined by the length field in the protocol, has been received and output through RXD in its entirety (normal condition).
- PN tracking is lost during demodulation.
- RX_PE is deactivated by the external controller.

MD_RDY can be configured through CR 9, bit 6 to be active low, or active high. Energy Detect (ED) pin 45 (Test port), and Carrier Sense (CRS) pin 46 (Test port), are available outputs from the HSP3824 and can be useful signals for an effective RX interface design. Use of these signals is optional. CRS and ED are further described within this document. The receive port is completely independent from the operation of the other interface ports including the TX port, supporting therefore a full duplex mode.

I/Q ADC Interface

The PRISM baseband processor chip (HSP3824) includes two 3-bit Analog to Digital converters (ADCs) that sample the analog input from the IF down converter. The I/Q ADC clock, MCLK, samples at twice the chip rate. The maximum sampling rate is 44MHz (power supply: 3.3V to 5.0V) or 33MHz (power supply 2.7V to 5.5V).

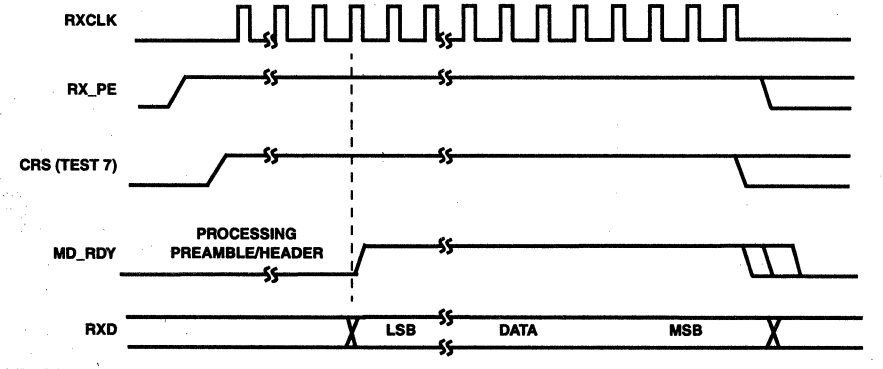
The interface specifications for the I and Q ADCs are listed on Table 2 below.

TABLE 2. I, Q, ADC SPECIFICATIONS

PARAMETER	MIN	TYP	MAX
Full Scale Input Voltage (V_{P-P})	0.25	0.50	1.0
Input Bandwidth (-0.5dB)	-	20MHz	-
Input Capacitance (pF)	-	5	-
Input Impedance (DC)	5kΩ	-	-
FS (Sampling Frequency)	-	-	44MHz

The voltages applied to pin 16, V_{REFP} and pin 17, V_{REFN} set the references for the internal I and Q ADC converters. In addition, V_{REFP} is also used to set the RSSI ADC converter reference. For a nominal 500mV_{P-P}, the suggested V_{REFP} voltage is 1.75V, and the suggested V_{REFN} is 0.93V. V_{REFN} should never be less than 0.25V. Since these ADCs are intended to sample AC voltages, their inputs are biased internally and they should be capacitively coupled.

The ADC section includes a compensation (calibration) circuit that automatically adjusts for temperature and component variations of the RF and IF strips. The variations in gain of limiters, AGC circuits, filters etc. can be compensated for up to ±4dB. Without the compensation circuit, the ADCs could see a loss of up to 1.5 bits of the 3 bits of quantization. The ADC calibration circuit adjusts the ADC reference voltages to maintain optimum quantization of the IF input over this variation range. It works on the principle of setting the reference to insure that the signal is at full scale (saturation) a certain percentage of the time. Note that this is not an AGC and it will compensate only for slow variations in signal levels (several seconds).



NOTE: MD_RDY active after CRC16.

FIGURE 7. RX PORT TIMING

The procedure for setting the ADC references to accommodate various input signal voltage levels is to set the reference voltages so that the ADC calibration circuit is operating at half scale. This leaves the maximum amount of adjustment room for circuit tolerances.

Figure 8 illustrates the suggested interface configuration for the ADCs and the reference circuits.

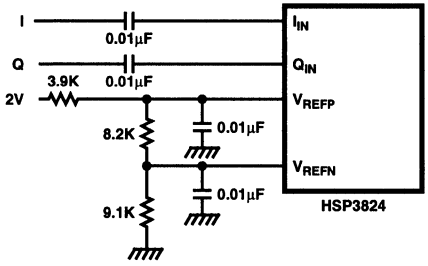


FIGURE 8. INTERFACES

ADC Calibration Circuit and Registers

The ADC compensation or calibration circuit is designed to optimize ADC performance for the I and Q inputs by maintaining the full 3-bit resolution of the outputs. There are two registers (CR 11 AD_CAL_POS and CR 12 AD_CAL_NEG) that set the parameters for the internal I and Q ADC calibration circuit.

Both I and Q ADC outputs are monitored by the ADC calibration circuit and if either has a full scale value, a 24-bit accumulator is incremented as defined by parameter AD_CAL_POS. If neither has a full scale value, the accumulator is decremented as defined by parameter AD_CAL_NEG.

A loop gain reduction is accomplished by using only the 5 MSBs out of the 24 bits to drive a D/A converter that adjusts the ADCs reference. The compensation adjustment is updated at 2kHz rate for a 2 MBPS operation. The ADC calibration circuit is only intended to remove slow component variations.

The ratio of the values from the two registers CR11 and CR12 set the probability that either the I or Q ADC converter will be at the saturation. The probability is set by (AD_CAL_POS)/(AD_CAL_NEG).

This also sets the levels so that operation with either NOISE or DPSK is approximately the same. It is assumed that the RF and IF sections of the receiver have enough gain to cause limiting on thermal noise. This will keep the levels at the ADC approximately same regardless of whether signal is present or not.

The ADC calibration voltage is automatically held during transmit in half duplex operation.

The ADC calibration circuit operation can be defined through CR 1, bits 1 and 0. Table 3 illustrates the possible configurations.

TABLE 3. ADC CALIBRATION

CR 1 BIT 0	CR 1 BIT 1	ADC CALIBRATION CIRCUIT CONFIGURATION
0	0	Automatic real time adjustment of reference.
0	1	Reference set at mid scale.
1	0	Reference held at most recent value.
1	1	Reference set at mid scale.

RSSI ADC Interface

The Receive Signal Strength Indication (RSSI) analog signal is input to a 6-bit ADC, indicating 64 discrete levels of received signal strength. This ADC measures a DC voltage, so its input must be DC coupled. Pin 16 (V_{REFP}) sets the reference for the RSSI ADC converter. V_{REFP} is common for the I and Q and RSSI ADCs. The RSSI signal is used as an input to the programmable Clear Channel Assessment algorithm of the HSP3824. The RSSI ADC output is stored in an 8-bit register (CR10) and it is updated at the symbol rate for access by the external processor to assist in network management.

The interface specifications for the RSSI ADC are listed on Table 4 below (V_{REFP} = 1.75V).

TABLE 4. RSSI ADC SPECIFICATIONS

PARAMETER	MIN	TYP	MAX
Full Scale Input Voltage	-	-	1.15
Input Bandwidth (0.5dB)	1MHz	-	-
Input Capacitance	-	7pF	-
Input Impedance (DC)	1M	-	-

Test Port

The HSP3824 provides the capability to access a number of internal signals and/or data through the Test port, pins TEST 0-7. In addition pin 1 (TEST_CK) is an output clock that can be used in conjunction with the data coming from the test port outputs. The test port is programmable through configuration register (CR5).

There are 9 test modes assigned to the PRISM test port listed in the Test Modes Table 5.

TABLE 5. TEST MODES

MODE	DESCRIPTION	TEST_CLK	TEST (7:0)
0	Normal Operation	TXCLK	CRS, ED, "000", Initial Detect, Reserved (1:0)
1	Correlator Test Mode	TXCLK	Mag (7:0)
2	Frequency Test Mode	DCLK	Frq Reg (7:0)
3	Phase Test Mode	DCLK	Phase (7:0)
4	NCO Test Mode	DCLK	NCO Phase Accum Reg
5	SQ Test Mode	LoadSQ	SQ2 (15:8) Phase Variance
6	Bit Sync Test Mode 1	RXCLK	Bit Sync Accum (7:0)
7	Bit Sync Test Mode 2	LoadSQ	SQ (14:7) Bit Sync Ref-Data

TABLE 5. TEST MODES (Continued)

MODE	DESCRIPTION	TEST_CLK	TEST (7:0)
8	A/D Cal Test Mode	A/D CAL_CK	CRS, ED, "0", ADCal (4:0)
9	Reserved		
10 (0Ah)	Reserved		
11	Reserved		
12	Reserved		
13	Reserved		
14	Reserved		
15	Reserved		

Definitions

Normal - Device in the full protocol mode (Mode 3).

TXCLK - Transmit clock (PN rate).

Initial Detect - Indicates that Signal Quality 1 and 2 (SQ1 and SQ2) exceed their programmed thresholds. Signal qualities are a function of phase error and correlator magnitude outputs.

ED - energy detect indicates that the RSSI value exceeds its programmed threshold.

CRS - indicates that a signal has been acquired (PN acquisition).

Mag - Magnitude output from the correlator.

DCLK - Data symbol clock.

FrqReg - Contents of the NCO frequency register.

Phase - phase of signal after carrier loop correction.

NCO PhaseAccumReg - Contents of the NCO phase accumulation register.

LoadSQ - Strobe that samples and updates Signal Quality, SQ1 and SQ2 values.

SQ2 - Signal Quality measure #2. Signal phase variance after removal of data, 8 MSBs of most recent 16-bit stored value.

RXCLK - Receive clock (RX sample clock). Nominally 22MHz.

BitSyncAccum - Real time monitor of the bit synchronization accumulator contents, mantissa only.

SQ1 - Signal Quality measure #1. Contents of the bit sync accumulator 8 MSBs of most recent 16-bit stored value.

A/D_Cal_ck - Clock for applying A/D calibration corrections.

ADCal - 5-bit value that drives the D/A adjusting the A/D reference.

External AGC Control

The ADC cal output (pin 26) is a binary signal that fluctuates between logic levels as the signals in the I and Q channels are either at full scale or not. If the input level is too high, this output will have a higher duty cycle, and visa versa. Thus, this signal could be integrated with an R-C filter to develop an AGC control voltage. The AGC feedback should be designed to drive it to 50% duty cycle. In the case that an external AGC is in use then the ADC calibration circuit must not be programmed for automatic level adjustment.

Power Down Modes

The power consumption modes of the HSP3824 are controlled by the following control signals.

Receiver Power Enable (RX_PE,pin 33), which disables the receiver when inactive.

Transmitter Power Enable (TX_PE, pin 2), which disables the transmitter when inactive.

Reset ($\overline{\text{RESET}}$, pin 28), which puts the receiver in a sleep mode when it is asserted at least 2 MCLKs after RX_PE is set at its inactive state. The power down mode where, both RESET and RX_PE are used is the lowest possible power consumption mode for the receiver. Exiting this mode requires a maximum of 10µs before the device is back at its operational mode.

The contents of the Configuration Registers is not effected by any of the power down modes. The external processor does not have access and cannot modify any of the CRs during the power down modes. No reconfiguration is required when returning to operational modes.

Table 6 describes the power down modes available for the HSP3824 (V_{CC} = 3.5V). The table values assume that all other inputs to the part (MCLK, SCLK, etc.) continue to run except as noted.

TABLE 6. POWER DOWN MODES

RX_PE	TX_PE	RESET	22MHz	44MHz	DEVICE STATE
Inactive	Inactive	Active	3.5mA	7mA	Both transmit and receive functions disabled. Device in sleep mode. Control Interface is still active. Register values are maintained. Device will return to its active state within 10µs.
Inactive	Inactive	Inactive	37mA	50mA	Both transmit and receive operations disabled. Device will become in its active state within 1µs.
Inactive	Active	Inactive	37mA	50mA	Receiver operations disabled. Receiver will return in its active state within 1µs.
Active	Inactive	Inactive	42mA	62mA	Transmitter operations disabled. Transmitter will return to its active state within 2 MCLKs.
I_{CC} Standby			300µA		All inputs at V_{CC} or GND.

Reset

The $\overline{\text{RESET}}$ signal is used during the power down mode as described in the Power Down Mode section. The $\overline{\text{RESET}}$ does not impact any of the internal configuration registers when asserted. Reset does not set the device in a default configuration, the HSP3824 must always be programmed on power up. The HSP3824 must be programmed with RESET inactive.

Transmitter Description

The HSP3824 transmitter is designed as a Direct Sequence Spread Spectrum DBPSK/DQPSK modulator. It can handle data rates of up to 4 MBPS (refer to AC and DC specifications). The major functional blocks of the transmitter include a network processor interface, DBPSK/DQPSK modulator, a data scrambler and a PN generator, as shown on Figure 9.

The transmitter has the capability to either generate its own synchronization preamble and header or accept the preamble and header information from an external source. In the first case, the transmitter knows when to make the DBPSK to DQPSK switchover, as required.

The preamble and header are always transmitted as DBPSK waveforms while the data packets can be configured to be either DBPSK or DQPSK. The preamble is used by the receiver to achieve initial PN synchronization while the header includes the necessary data fields of the communications protocol to establish the physical layer link. There is a choice of four potential preamble/header formats that the HSP3824 can generate internally. These formats are referred to as mode 0, 1, 2 and 3. Mode 0 uses the minimum number of available header fields while mode 3 is a full protocol mode utilizing all available header fields. The number of the synchronization preamble bits is programmable.

The transmitter accepts data from the external source, scrambles it, differentially encodes it as either DBPSK or DQPSK, and mixes it with the BPSK PN spreading. The baseband digital signals are then output to the external IF modulator.

The transmitter includes a programmable PN generator that can provide 11, 13, 15 or 16 chip sequences. The transmitter also contains a programmable clock divider circuit that allows for various data rates. The master clock (MCLK) can be a maximum of 44MHz.

The chip rates are programmed through CR3 for TX and CR2 for RX. In addition the data rate is a function of the sample clock rate (MCLK) and the number of PN bits per symbol.

The following equations show the Symbol rate for both TX and RX as a function of MCLK, Chips per symbol and N.

N is a programmable parameter through configuration registers CR 2and CR 3. The value of N is 2, 4, 8 or 16. N is used internally to divide the MCLK to generate other required clocks for proper operation of the device.

Symbol Rate = MCLK/(N x Chips per Symbol).

The bit rate Table 7 shows examples of the relationships expressed on the symbol rate equation.

The modulator is capable of switching rate automatically in the case where the preamble and header information are DBPSK modulated, and the data is DQPSK modulated.

The modulator is completely independent from the demodulator, allowing the PRISM baseband processor to be used in full duplex operation.

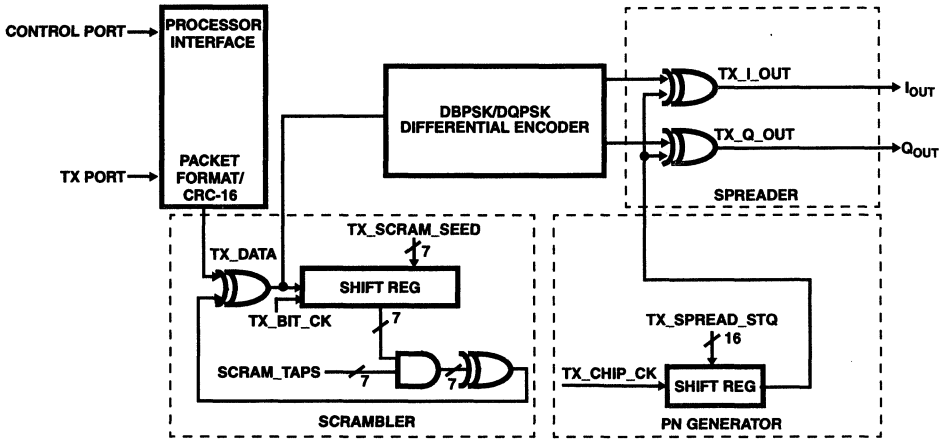


FIGURE 9. MODULATOR DIAGRAM

TABLE 7. BIT RATE TABLE EXAMPLES FOR MCLK = 44MHz

DATA MODULATION	ADC SAMPLE CLOCK (MHz)	TX SETUP CR 3 BITS 4, 3	RX SET UP CR 2 BITS 4, 3	DATA RATE FOR 11 CHIPS/BIT (MBPS)	DATA RATE FOR 13 CHIPS/BIT (MBPS)	DATA RATE FOR 15 CHIPS/BIT (MBPS)	DATA RATE FOR 16 CHIPS/BIT (MBPS)
DQPSK	44	00 (N = 2)	00	4	3.385	2.933	2.75
DQPSK	22	01 (N = 4)	01	2	1.692	1.467	1.375
DQPSK	11	10 (N = 8)	10	1	0.846	0.733	0.688
DQPSK	5.5	11 (N = 16)	11	0. 5	0.423	0.367	0.344
DBPSK	44	00 (N = 2)	00	2	1.692	1.467	1.375
DBPSK	22	01 (N = 4)	01	1	0.846	0.733	0.688
DBPSK	11	10 (N = 8)	10	0.5	0.423	0.367	0.344
DBPSK	5.5	11 (N = 16)	11	0.25	0.212	0.183	0.171

Header/Packet Description

The HSP3824 is designed to handle continuous or packetized Direct Sequence Spread Spectrum (DSSS) data transmissions. The HSP3824 can generate its own preamble and header information or it can accept them from an external source.

When preamble and header are internally generated the device supports a synchronization preamble up to 256 symbols, and a header that can include up to five fields. The preamble size and all of the fields are programmable. When internally generated the preamble is all 1's (before entering the scrambler). The actual transmitted pattern of the preamble will be randomized by the scrambler if the user chooses to utilize the data scrambling option.

When the preamble is externally generated the user can choose any desirable bit pattern. Note though, that if the preamble bits will be processed by the scrambler which will alter the original pattern unless it is disabled.

The preamble is always transmitted as a DBPSK waveform with a programmable length of up to 256 symbols long. The HSP3824 requires at least 126 preamble symbols to acquire in a dual antenna configuration (diversity), or a minimum of 78 preamble symbols to acquire under a single antenna configuration. The exact number of necessary preamble symbols should be determined by the system designer, taking into consideration the noise and interference requirements in conjunction with the desired probability of detection vs probability of false alarm for signal acquisition.

The five available fields for the header are:

SFD Field (16 Bits) - This field carries the ID to establish the link. This is a mandatory field for the HSP3824 to establish communications. The HSP3824 will not declare a valid data packet, even if it PN acquires, unless it detects the specific SFD. The SFD field is required for both Internal preamble/header generation and External preamble/header generation. The HSP3824 receiver can be programmed to time out searching for the SFD. The timer starts counting the moment that initial PN synchronization has been established from the preamble.

Signal Field (8 Bits) - This field indicates whether the data packet that follows the header is modulated as DBPSK or DQPSK. In mode 3 the HSP3824 receiver looks at the signal field to determine whether it needs to switch from DBPSK demodulation into DQPSK demodulation at the end of the always DBPSK preamble and header fields.

Service Field (8 Bits) - This field can be utilized as required by the user.

Length Field (16 Bits - This field indicates the number of data symbols contained in the data packet. The receiver can be programmed to check the length field in determining

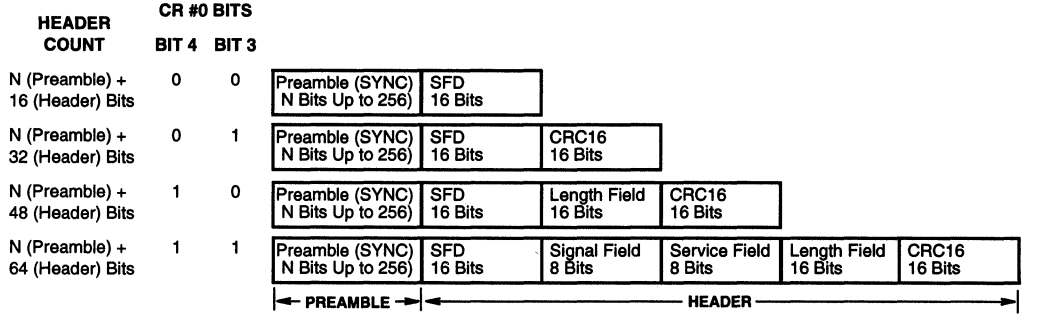


FIGURE 10. PREAMBLE/HEADEAR MODES

when it needs to de-assert the MD_RDY interface signal. MD_RDY envelopes the received data packet as it is being output to the external processor.

CCITT - CRC 16 Field (16 Bits) - This field includes the 16-bit CCITT - CRC 16 calculation of the five header fields. This value is compared with the CCITT - CRC 16 code calculated at the receiver. The HSP3824 receiver can be programmed to drop the link upon a CCITT - CRC 16 error or it can be programmed to ignore the error and to continue with data demodulation.

The CRC or cyclic Redundancy Check is a CCITT CRC-16 FCS (frame check sequence). It is the ones compliment of the remainder generated by the modulo 2 division of the protected bits by the polynominal:

$X^{16} + x^{12} + x^5 + 1$

The protected bits are processed in transmit order. All CRC calculations are made prior to data scrambling. A shift register with two taps is used for the calculation. It is preset to all ones and then the protected fields are shifted through the register. The output is then complimented and the residual shifted out MSB first.

When the HSP3824 generates the preamble and header internally it can be configured into one of four link protocol modes.

Mode 0 - In this mode the preamble is programmable up to 256 bits (all 1's) and the SFD field is the only field utilized for the header. This mode only supports DBPSK transmissions for the entire packet (preamble/header and data).

Mode 1 - In this mode the preamble is programmable up to 256 bits (all 1's) and the SFD and CCITT - CRC 16 fields are used for the header. The data that follows the header can be either DBPSK or DQPSK. The receiver and transmitter must be programmed to the proper modulation type.

Mode 2 - In this mode the preamble is programmable up to 256 bits (all 1's) and the SFD, Length Field, and CCITT - CRC 16 fields are used for the header. The data that follows the header can be either DBPSK or DQPSK. The receiver and transmitter must be programmed to the proper modulation type.

Mode 3 - In this mode the preamble is programmable up to 256 bits (all 1's). The header in this mode is using all available fields. In mode 3 the signal field defines the modulation type of the data packet (DBPSK or DQPSK) so the receiver does not need to be preprogrammed to anticipate one or the other. In this mode the device checks the Signal field for the data packet modulation and it switches to DQPSK if it is defined as such in the signal field. Note that the preamble and header are always DBPSK the modulation definition applies only for the data packet. This mode is called the full protocol mode in this document.

Figure 10 summarizes the four preamble/head or modes. In the case that the device is configured to accept the preamble and header from an external source it still needs to be configured in one of the four modes (0:3). Even though the HSP3824 transmitter does not generate the preamble and header information the receiver needs to know the mode in use so it can proceed with the proper protocol and demodulation decisions.

The following Configuration Registers (CR)are used to program the preamble/header functions, more programming details about these registers can be found in the Control Registers section of this document:

CR 0 - Defines one of the four modes (bits 4, 3) for the TX. Defines whether the SFD timer is active (bit 2). Defines whether the receiver should stop demodulating after the number of symbols indicated in the Length field has been met.

CR 2 - Defines to the receiver one of the four protocol modes (bits 1, 0). Indicates whether any detected CCITT - CRC 16 errors need to reset the receiver (return to acquisition) or to ignore them and continue with demodulation (bit 5). Specifies a 128-bit preamble or an 80-bit preamble (bit 2).

CR 3 - Defines internal or external preamble generation (bit 2). Indicates to the receiver the data packet modulation (bit 0), note that in mode 3 the contents of this register are overwritten by the information in the received signal field of the header. CR 3 specifies the data modulation type used to the transmitter (bit 1). Bit 1 defines the contents of the signaling field in the header to indicate either DBPSK or DQPSK modulation.

CR 41 - Defines the length of time that the demodulator searches for the SFD before returning to acquisition.

CR 42 - The contents of this register indicate that the transmitted data is DBPSK. If CR 4-bit 1 is set to indicate DBPSK modulation then the contents of this register are transmitted in the signal field of the header.

CR 43 - The contents of this register indicates that the transmitted data is DQPSK. If CR 4-bit 1 is set to indicate DQPSK modulation then the contents of this register are transmitted in the signal field of the header.

CR 44, 45, 46, 47, 48 - Status, read only, registers that indicate the service field, data length field and CCITT - CRC 16 field values of the received header.

CR 49, 50 - Defines the transmit SFD field value of the header. The receiver will always search to detect this value before it declares a valid data packet.

CR 51 - Defines the contents of the transmit service field.

CR 52, 53 - Defines the value of the transmit data length field. This value includes all symbols following the last header field symbol.

CR 54,55 - Status, read only, registers indicating the calculated CCITT - CRC 16 value of the most recently transmitted header.

CR 56 - Defines the number of preamble synchronization bits that need to be transmitted when the preamble is internally generated. These symbols are used by the receiver for initial PN acquisition and they are followed by the header fields.

The full protocol requires a setting of 128d = 80h. For other applications, in general increasing the preamble length will improve low signal to noise acquisition performance at the cost of greater link overhead. For dual receive antenna operation, the minimum suggested value is 128d = 80h. For single receive antenna operation, the minimum suggested value is 80d = 50h. These suggested values include a 2 symbol TX power amplifier ramp up. If an AGC is used, its worst case settling time in symbols should be added to these values.

PN Generator Description

The spread function for this radio uses short sequences. The same sequence is applied to every bit. All transmitted symbols, preamble/header and data are always spread by the PN sequence at the chip rate. The PN sequence sets the Processing Gain (PG) of the Direct Sequence receiver. The HSP3824 can be programmed to utilize 11,13,15 and 16 bit sequences. Given the length of these programmable sequences the PG range of the HSP3824 is:

From 10.41dB (10 LOG(11)) to 12.04dB (10 LOG(16))

The transmitter and receiver PN sequences can are programmed independently. This provides additional flexibility to the network designer.

The TX sequence is set through CR 13 and CR 14 while the RX PN sequence is set through CR 20 and CR 21. A maximum of 16 bits can be programmed between the pairs of these configuration registers. For TX Registers CR13 and CR14 contain the high and low bytes of the sequence for the transmitter. In addition Bits 5 and 6 of CR 4 define the sequence length in chips per bit. CR 13, CR 14 and CR 4 must all be programmed for proper functionality of the PN generator. The sequence is transmitted MSB first. When fewer than 16 bits are in the sequence, the MSBs are truncated.

Scrambler and Data Encoder Description

The data coder the implements the desired DQPSK coding as shown in the DQPSK Data Encoder table. This coding scheme results from differential coding of the dibits. When used in the DBPSK modes, only the 00 and 11 dibits are used. Vector rotation is counterclockwise.

TABLE 8. DQPSK DATA ENCODER

PHASE SHIFT	DIBITS
0	00
+90	01
+180	11
-90	10

The data scrambler is a self synchronizing circuit. It consist of a 7-bit shift register with feedback from specified taps of the register, as programmed through CR 16. Both transmitter and receiver use the same scrambling algorithm. All of the bits transmitted are scrambled, including data header and preamble. The scrambler can be disabled.

Scrambling provides additional spreading to each of the spectral lines of the spread DS signal. The additional spreading due to the scrambling will have the same null to null bandwidth, but it will further smear the discrete spectral lines from the PN code sequence. Scrambling might be necessary for certain allocated frequencies to meet transmission waveform requirements as defined by various regulatory agencies.

In the absence of scrambling, the data patterns could contain long strings of ones or zeros. This is definitely the case with the a DS preamble which has a stream of up to 256 continuous ones. The continuous ones would cause the spectrum to be concentrated at the discrete lines defined by the spreading code and potentially cause interference with other narrow band users at these frequencies. Additionally, the DS system itself would be moderately more susceptible to interference at these frequencies. With scrambling, the spectrum is more uniform and these negative effects are reduced, in proportion with the scrambling code length.

Figure 11 illustrates an example of a non scrambled transmission using an 11-bit code with DBPSK modulation with alternate 1's and 0's as data. The data rate is 2 MBPS while the spread rate or chip rate is at 11 MCPS. The 11 spectral lines resulting from the PN code can be clearly seen in Figure 11. In Figure 12, the same signal is transmitted but with the scrambler being on. In this case the spectral lines have been smeared.

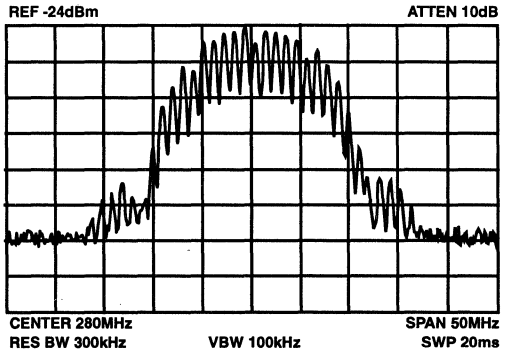


FIGURE 11. UNSCRAMBLED DBPSK DATA OF ALTERNATE 1's/0's SPREAD WITH AN 11-BIT SEQUENCE

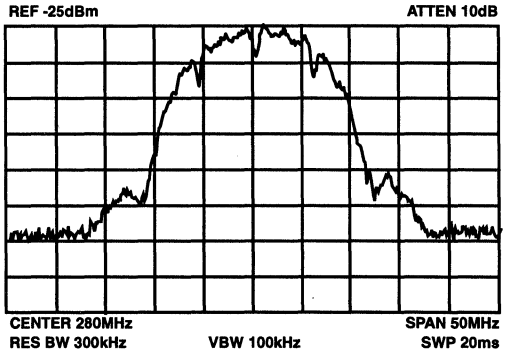


FIGURE 12. SCRAMBLED DBPSK DATA OF ALTERNATE 1's/0's SPREAD WITH AN 11-BIT SEQUENCE

Another reason to scramble is to gain a small measure of privacy. The DS nature of the signal is easily demodulated with a correlating receiver. Indeed, the data modulation can be recovered from one of the discrete spectral lines with a narrow band receiver (with a 10dB loss in sensitivity). This means that the signal gets little security from the DS spreading code alone. Scrambling adds a privacy feature to the waveform that would require the listener to know the scrambling parameters in order to listen in. When the data is scrambled it cannot be

defeated by listening to one of the scrambling spectral lines since the unintentional receiver in this case is too narrow band to recover the data modulation. This assumes though that each user can set up different scrambling patterns There are 9 maximal length codes that can be utilized with a generator of length 7. The different codes can be used to implement a basic privacy scheme. It needs to be clear though that this scrambling code length and the actual properties of such codes are not a major challenge for a sophisticated intentional interceptor to be listening in. This is why we refer to this scrambling advantage as a communications privacy feature as opposed to a secure communications feature.

Scrambling is done by a polynomial division using a prescribed polynomial. A shift register holds the last quotient and the output is the exclusive-or of the data and the sum of taps in the shift register. The taps and seed are programmable. The transmit scrambler seed is programmed by CR 15 and the taps are set with CR 16. Setting the seed is optional, since the scrambler is self-synchronizing and it will eventually synchronize with the incoming data after flashing the 7 bits stored from the previous transmission.

Modulator Description

The modulator is designed to support both DBPSK and DQPSK signals. The modulator is capable of automatically switching its rate in the case where the preamble and header are DBPSK modulated, and the data is DQPSK modulated. The modulator can support date rates up to 4 MBPS. The programming details of the modulator are given at the introductory paragraph of this section. The HSP3824 can support data rates of up to 4 MBPS (DQPSK) with power supply voltages between 3.3V and 5.0V and data rates of up to 3 MBPS with supply voltages between 2.7V and 5.5V.

Clear Channel Assessment (CCA) and Energy Detect (ED) Description

The clear channel assessment (CCA) circuit implements the carrier sense portion of a carrier sense multiple access (CSMA) networking scheme. The Clear Channel Assessment (CCA) monitors the environment to determine when it is feasible to transmit. The result of the CCA algorithm is available in real time through output pin 32 of the device. The CCA state machine in the HSP3824 can be programmed as a function of RSSI, energy detected on the channel, carrier detection, and a number of on board watchdog timers to time-out under certain conditions. The CCA can be also completely by-passed allowing transmissions independent of any channel conditions. The programmable CCA in combination with the visibility of the various internal parameters (i.e. Energy Detection measurement results), can assist an external processor in executing algorithms that can adapt to the environment. These algorithms can increase network throughput by minimizing collisions and reducing transmissions liable to errors.

There are two measures that are used in the CCA assessment. The receive signal strength (RSSI) which measures the energy at the antenna and the carrier sense (CS), which is triggered upon valid PN correlation of the baseband processor (HSP3824). Both indicators are used since interference can trigger the signal strength indication, but it will not trigger the carrier sense. The carrier sense, however, is slower to respond than the signal strength and it becomes active only when a spread signal with identical PN code has been detected, so it is not adequate in itself. Note that the CS is also vulnerable to false alarms. The CCA looks for changes in these measurements and decides its state based on these measures and the time that has elapsed since the

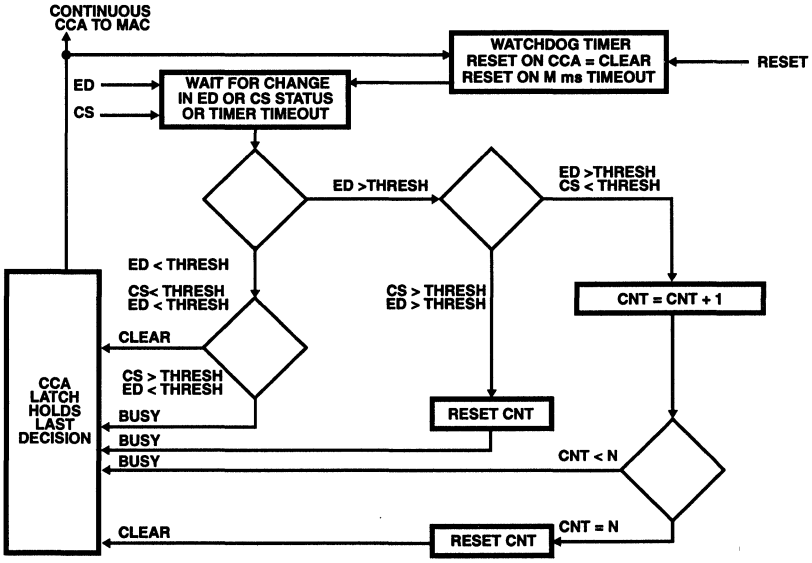


FIGURE 13. CCA FUNCTIONAL FLOW DIAGRAM

channel was last clear. If a source of interference makes it look like the channel is occupied, the circuit will detect a signal without carrier and will wait a proscribed time before deciding to transmit over the interference.

The receive signal strength indication (RSSI) measurement is an analog input to the HSP3824 from the successive IF stage of the radio. The RSSI ADC converts it within the baseband processor and it compares it to a programmable threshold. This threshold is normally set to between -70 and -80dBm. This measure is used in the acquisition decision and is also passed to the clear channel assessment logic. The state diagram in Figure 13 shows the operation of the clear channel assessment state machine.

The energy detection (ED) signal is the digitized RSSI signal. The carrier sense (CS) input is derived from a combination of the Signal Quality 2 (SQ2) based on phase error and the Signal Quality 1(SQ1) based on PN correlator magnitude outputs. Both Signal Quality measures and the ED input are differentiated to sense when they change. These change detectors and the watchdog timer TIME OUT output are combined to initiate a clear channel assessment decision.

The CCA algorithm will always declare the channel busy if CS is active. If only ED is active the state machine will initially declare a busy channel and at the same time it will start timing ED until it meets the programmed time out count. When the time out expires the state machine will declare the channel as being clear even if the ED is still active. This will prevent the transmitter locking out permanently on some persisting interference. This time out period is programmable by 2 parameters that define an inner count M and an outer count N. The total time out period is determined by the time corresponding to the product of MxN. The value of the inner counter M is programmable through CR 17 while the value of the outer counter N is programmable through CR 18. The state machine cycles M times the N count before it asserts CCA, declaring the channel as clear for transmission. Note that the counters are automatically reset to restart the count when CS is detected to be active. In summary the CCA state machine has four basic states. The first state clears the CCA when both the CS and ED are inactive. This indicates that the channel is truly clear.

The second state sets the CCA to BUSY when the CS is active and the ED is inactive. This corresponds to a channel where the signal just went away or dropped below threshold but the carrier is still being sensed. The third state sets the CCA to BUSY and resets the cycle counter when the ED and CS are both active. This is an obviously busy channel.

The fourth state increments the cycle counter if the CS is inactive and the ED is active, and sets the CCA to BUSY if the count is less than N. This is where the channel has just had a new signal come up and the carrier has not yet been acquired or where an interferer turns on.

If the cycle counter reaches N, the counter is reset and the CCA is set to CLEAR. This happens on interference that persists. If the channel has interference, it may be low enough to allow communications. ***The CCA state machine does not influence any of the receive or transmit operations within the HSP3824. The CCA algorithm output is an indication to the network processor. The processor can ignore this indicator and decide to have the HSP3824 transmit regardless of the state of CCA.***

The Configuration registers effecting the CCA algorithm operation are summarized below (more programming details on these registers can be found under the Control Registers section of this document).

The CCA output from pin 32 of the device can be defined as active high or active low through CR 9 (bit 5). The RSSI threshold is set through CR19. If the actual RSSI value from the ADC exceeds this threshold then ED becomes active.

The instantaneous RSSI value can be monitored by the external network processor by reading CR 10. The programmable thresholds on the two signal quality measurements are set through CR22, 23, 30, and 31. Signal Quality 1 and 2 thresholds derive the state of the Carrier Sense. More details on SQ are included under the receiver section of this document.

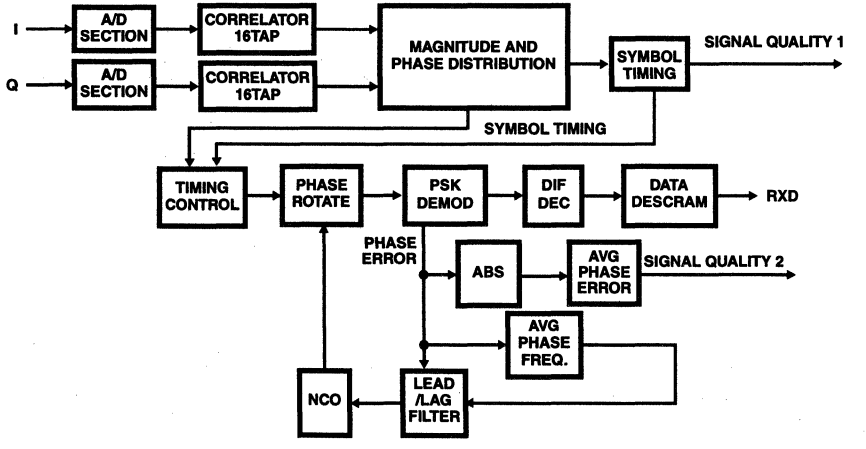


FIGURE 14. DEMODULATOR BLOCK DIAGRAM

Finally, CR 17 and CR 18 are used to set the time out parameters before the CCA algorithm declares permission for transmission.

Receiver Description

The receiver portion of the baseband processor, performs ADC conversion and demodulation of the spread spectrum signal. It correlates the PN spread symbols, then demodulates the DBPSK or DQPSK symbols. The demodulator includes a frequency loop that tracks and removes the carrier frequency offset. In addition it tracks the symbol timing, and differentially decodes and descrambles the data. The data is output through the RX Port to the external processor.

A common practice for burst mode communications systems is to differentially modulate the signal, so that a DPSK demodulator can be used for data recovery. This form of demodulator uses each symbol as a phase reference for the next one. It offers rapid acquisition and tolerance to rapid phase fluctuations at the expense of lower bit error rate (BER) performance.

The PRISM baseband processor, HSP3824 uses differential demodulation for the initial acquisition portion of the processing and then switches to coherent demodulation for the rest of the acquisition and data demodulation. The HSP3824 is designed to achieve rapid settling of the carrier tracking loop during acquisition. Coherent processing substantially improves the BER performance margin. Rapid phase fluctuations are handled with a relatively wide loop bandwidth.

The baseband processor uses time invariant correlation to strip the PN spreading and polar processing to demodulate the resulting signals. These operations are illustrated in Figure 14 which is an overall block diagram of the receiver processor. Input samples from the I and Q ADC converters are correlated to remove the spreading sequence. The magnitude of the correlation pulse is used to determine the symbol timing. The sample stream is decimated to the symbol rate and the phase is corrected for frequency offset prior to PSK demodulation. Phase errors from the demodulator are fed to the NCO through a lead/lag filter to achieve phase lock. The variance of the phase errors is used to determine signal quality for acquisition and lock detection.

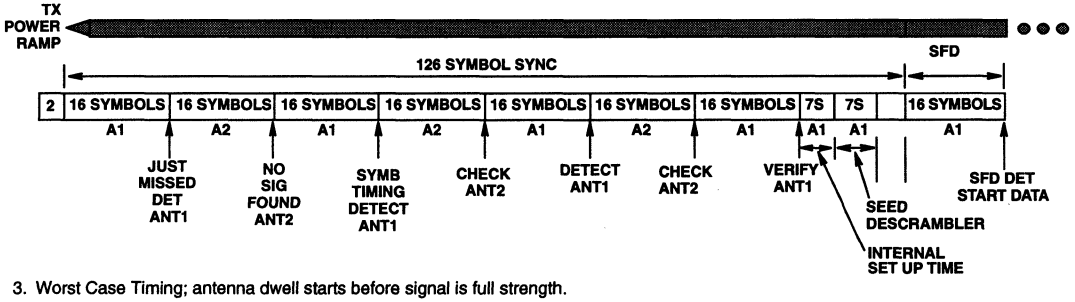
Acquisition Description

The PRISM baseband processor uses either a dual antenna mode of operation for compensation against multipath interference losses or a single antenna mode of operation with faster acquisition times.

Two Antenna Acquisition

During the 2 antenna (diversity) mode the two antennas are scanned in order to find the one with the best representation of the signal. This scanning is stopped once a suitable signal is found and the best antenna is selected.

A projected worst case time line for the acquisition of a signal in the two antenna case is shown in Figure 15. The synchronization part of the preamble is 128 symbols long followed by a 16-bit SFD. The receiver must scan the two antennas to determine if a signal is present on either one and, if so, which has the better signal. The timeline is broken into 16 symbol blocks (dwells) for the scanning process. This length of time is necessary to allow enough integration of the signal to make a good



3. Worst Case Timing; antenna dwell starts before signal is full strength.
4. Time line shown assumes that antenna 2 gets insufficient signal.

FIGURE 15. DUAL ANTENNA ACQUISITION TIMELINE

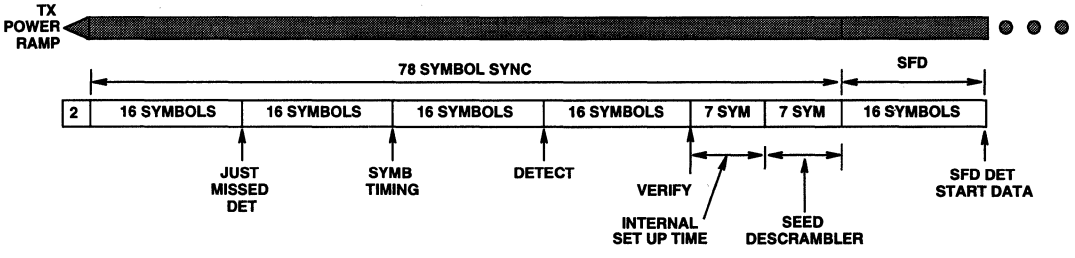


FIGURE 16. SINGLE ANTENNA ACQUISITION TIMELINE

acquisition decision. This worst case time line example assumes that the signal is present on antenna A1 only (A2 is blocked). It further assumes that the signal arrives part way into the first A1 dwell such as to just barely miss detection. The signal and the scanning process are asynchronous and the signal could start anywhere. In this timeline, it is assumed that all 16 symbols are present, but they were missed due to power amplifier ramp up. Since A2 has insufficient signal, the first A2 dwell after the start of the preamble also fails detection. The second A1 dwell after signal start is successful and a symbol timing measurement is achieved.

Meanwhile signal quality and signal frequency measurements are made simultaneous with symbol timing measurements. When the bit sync level, SQ1, and Phase variance SQ2 are above their user programmable thresholds, the signal is declared present for the antenna with the best signal. More details on the Signal Quality estimates and their programmability are given in the Acquisition Signal Quality Parameters section of this document.

At the end of each dwell, a decision is made based on the relative values of the signal qualities of the signals on the two antennas. In the example, antenna A1 is the one selected, so the recorded symbol timing and carrier frequency for A1 are used thereafter for the symbol timing and the PLL of the NCO to begin carrier de-rotation and demodulation.

Prior to initial acquisition the NCO was inactive and DPSK demodulation processing was used. Carrier phase measurement are done on a symbol by symbol basis afterward and coherent DPSK demodulation is in effect. After a brief setup time as illustrated on the timeline of Figure 15, the signal begins to emerge from the demodulator.

If the descrambler is used it takes 7 more symbols to seed the descrambler before valid data is available. This occurs in time for the SFD to be received. At this time the demodulator is tracking and in the coherent PSK demodulation mode it will no longer scan antennas.

One Antenna Acquisition

When only one antenna is being used, the user can delete the antenna switch and shorten the acquisition sequence. Figure 16 shows the single antenna acquisition timeline. It uses a 78 symbol sequence with 2 more for power ramping of the RF front of the radio. This scheme deletes the second antenna dwells but performs the same otherwise. It verifies the signal after initial detection for lower false alarm probability.

Acquisition Signal Quality Parameters

Two measures of signal quality are used to determine acquisition and drop lock decisions. The first method of determining signal presence is to measure the correlator output (or bit sync) amplitude. This measure, however, flattens out in the range of high BER and is sensitive to signal amplitude. The second measure is phase noise and in most BER scenarios it is a better indication of good signals plus it is insensitive to signal amplitude. The bit sync amplitude and phase noise are integrated over each block of 16 symbols used in acquisition or over blocks of 128 symbols in the data demodulation mode. The bit sync amplitude measurement represents the peak of the correlation out of the PN correlator. Figure 17 shows the correlation process. The signal is sampled at twice the chip rate (i.e. 22 MSPS). The one sample that falls closest to the peak is used for a bit sync amplitude sample for each symbol. This sample is called the on-time sample. High bit sync amplitude means a good signal. The early and late samples are the two adjacent samples and are used for tracking.

The other signal quality measurement is based on phase noise and that is taken by sampling the correlator output at the correlator peaks. The phase changes due to scrambling are removed by differential demodulation during initial acquisition. Then the phase, the phase rate and the phase variance are measured and integrated for 16 symbols. The phase variance is used for the phase noise signal quality measure. Low phase noise means a stronger received signal.

Procedure to Set Acq. Signal Quality Parameters (Example)

There are four registers that set the acquisition signal quality thresholds, they are: CR 22, 23, 30, and 31 (RX_SQX_IN_ACQ). Each threshold consists of two bytes, high and low that hold a 16-bit number.

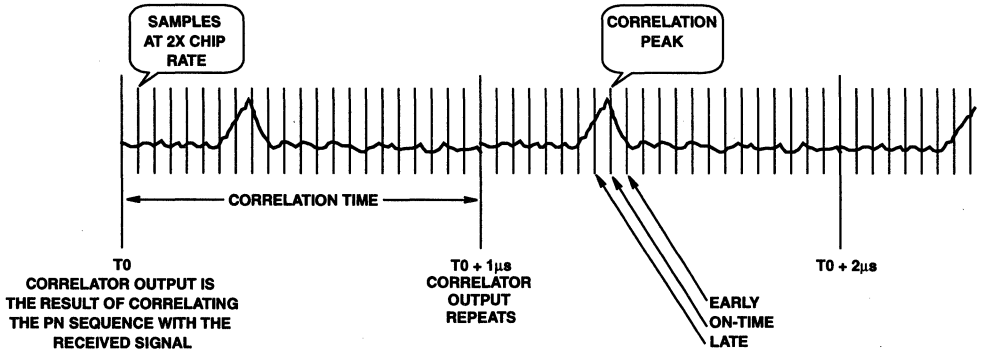


FIGURE 17. CORRELATION PROCESS

These two thresholds, bit sync amplitude CR (22 and 23) and phase error CR (30 and 31) are used to determine if the desired signal is present. If the thresholds are set too "low", there is the probability of missing a high signal to noise detection due to processing a false alarm. If they are set too "high", there is the probability of missing a low signal to noise detection. For the bit sync amplitude, "high" actually means high amplitude while for phase noise "high" means high SNR or low noise.

A recommended procedure is to set these thresholds individually optimizing each one of them to the same false alarm rate with no desired signal present. Only the background environment should be present, usually additive gaussian white noise (AGWN). When programming each threshold, the other threshold is set so that it always indicates that the signal is present. Set register CR22 to 00h while trying to determine the value of the phase error signal quality threshold for registers CR 30 and 31. Set register CR30 to FFh while trying to determine the value of the Bit sync. amplitude signal quality threshold for registers 22 and 23. Monitor the Carrier Sense (CRS) output (TEST 7, pin 46) and adjust the threshold to produce the desired rate of false detections. CRS indicates valid initial PN acquisition. After both thresholds are programmed in the device the CRS rate is a logic "and" of both signal qualities rate of occurrence over their respective thresholds and will therefore be much lower than either.

PN Correlator Description

The PN correlator is designed to handle BPSK spreading with carrier offsets up to ±50ppm and 11,13,15 or 16 chips per symbol. Since the spreading is BPSK, the correlator is implemented with two real correlators, one for the I and one for the Q channel.The same sequence is always used for both I an Q correlators. The TX sequence can be programmed as a different sequence from the RX sequence. This allows a full duplex link with different spreading parameters for each direction.

The correlators are time invariant matched filters otherwise known as parallel correlators. They use two samples per chip. The correlator despreads the samples from the chip rate back to the original data rate giving 10.4dB processing gain for 11 chips per bit. While despreading the desired signal, the correlator spreads the energy of any non correlating interfering signal.

Based on the fact that correlator output pulse is used for bit timing, the HSP3824 can not be used for any non spread applications.

In programming the correlator functions, there are two sets of configuration registers that are used to program the spread sequences of the transmitter and the receiver. They are CR 13 and 14 for transmitter and CR 20 and 21 for the receiver. In addition, CR2 and CR3 define the sequence length or chips per symbol for the receiver and transmitter respectively. These are carried in bits 6 and 7 of CR2 and bits 5 and 6 of CR3. More programming details are given in the Control Registers section of this document.

Data Demodulation and Tracking Description

The signal is demodulated from the correlation peaks tracked by the symbol timing loop (bit sync). The frequency and phase of the signal is corrected from the NCO that is driven by the phase locked loop. Demodulation of the DPSK data in the early stages of acquisition is done by delay and subtraction of the phase samples. Once phase locked loop tracking of the carrier is established, coherent demodulation is enabled for better performance. Averaging the phase errors over 16 symbols gives the necessary frequency information for proper NCO operation. The signal quality is taken as the variance in this estimate.

There are two signal quality measurements that are performed in real time by the device and they set the demodulator performance. The thresholds for these signal quality measurements are user programmable. The same two signal quality measures, phase error and bit sync. amplitude, that are used in acquisition are also used for the data drop lock decision. The data thresholds, though, are programmed independently from the acquisition thresholds. If the radio uses the network processor to determine when to drop the signal, the thresholds for these decisions should be set to their limits allowing data demodulation even with poor signal reception. Under this configuration the HSP3824 data monitor mechanism is essentially bypassed and data monitoring becomes the responsibility of the network processor.

These signal quality measurements are integrated over 128 symbols as opposed to 16 symbol intervals for acquisition, so the minimum time to drop lock based with these thresholds is 128 symbols or 128ms at 1 MSPS. Note that other than the data thresholds, non-detection of the SFD can cause the HSP3824 to drop lock and return its acquisition mode.

Configuration Register 41 sets the search timer for the SFD. This register sets this time-out length in symbols for the receiver. If the time out is reached, and no SFD is found, the receiver resets to the acquisition mode. The suggested value is preamble symbols + 16 symbols. If several transmit preamble lengths are used by various transmitters in a network, the longest value should be used for the receiver settings.

Procedure to Set Signal Quality Registers

CR 26, 27, 34, AND 35 (RX_SQX_IN_DATA) are programmed to hold the threshold values that are used to drop lock if the signal quality drops below their values. These can be set to their limit values if the external network processor is used for drop lock decisions instead of the HSP3824 demodulator. The signal quality values are averaged over 128 symbols and if the bit sync amplitude value drops below its threshold or the phase noise rises over its threshold, the link is dropped and the receiver returnes to the acquisition mode. These values should typically be different for BPSK and QPSK since the operating point in SNR differs by 3dB. If the receiver is intended to receive both BPSK and QPSK modulations, a compromise value must be used or the network processor can control them as appropriate.

The suggested method of optimization is to set the transmitter in a continuous transmit mode. Then, measure the time until the receiver drops lock at low signal to noise ratio. Each of the 2 thresholds should be set individually to the same drop lock time. While setting thresholds for one of the signal qualities the other should be configured at its limit so it does not influence the drop lock decisions. Set CR 26 to 00h while determining the value of CR 34 and 35 for phase error threshold. Set CR 34 to FFh while determining the value of CR 26 and 27 for bit sync. amplitude threshold.

Assuming a 10e-6 BER operating point, it is suggested that the drop lock thresholds are set at 10e-3 BER, with each threshold adjusted individually.

Note that the bit sync amplitude is linearly proportional to the signal amplitude at the ADC converters. If an AGC system is being used instead of a limiter, the bit sync amplitude threshold should be set at or below the minimum amplitude that the radio will see at its sensitivity level.

Data Decoder and Descrambler Description

The data decoder that implements the desired DQPSK coding/decoding as shown in DQPSK Data Decoder Table 9. This coding scheme results from differential coding of the dibits. When used in the DBPSK modes, only the 00 and 11 dibits are used. Vector rotation is counterclockwise.

TABLE 9. DQPSK DATA DECODER

PHASE SHIFT	DIBITS
0	00
+90	01
+180	11
-90	10

The data scrambler and de-scrambler are self synchronizing circuits. They consist of a 7-bit shift register with feedback of some of the taps of the register. The scrambler can be disabled for measuring RF carrier suppression. The scrambler is designed to insure smearing of the discrete spectrum lines produced by the PN code.

One thing to keep in mind is that both the differential decoding and the descrambling when used cause error extension. This causes the errors to occur in groups of 4 and 6. This is due to two properties of the processing. First, the differential decoding process causes errors to occur in pairs. When a symbol error is made, it is usually a single bit error even in QPSK mode. When a symbol is in error, the next symbol will also be decoded wrong since the data is encoded in the change from one symbol to the next. Thus, two errors are made on two successive symbols. In QPSK mode, these may be next to one another or separated by up to 2 bits. Secondly, when the bits are processed by the descrambler, these errors are further extended. The descrambler is a 7-bit shift register with one or more taps exclusive ored with the bit stream. If for example the scrambler polynomial uses 2 taps that are summed with the data, then each error is extended by a factor of three. Since the DPSK errors are close together, however, some of them can be canceled in the descrambler. In this case, two wrongs do make a right, so the observed errors can be in groups of 4 instead of 6.

Descrambling is done by a polynomial division using a prescribed polynomial. A shift register holds the last quotient and the output is the exclusive-or of the data and the sum of taps in the shift register. The taps and seed are programmable. The transmit scrambler seed is programmed by CR 15 and the taps are set with CR 16. One reason for setting the seed is that it can be used to make the SFD scrambling the same every packet so that it can be recognized in its scrambled state.

Demodulator Performance

This section indicates the theoretical performance and typical performance measures for a radio design. The performance data below should be used as a guide. The actual performance depends on the application, interference environment, RF/IF implementation and radio component selection in general.

Overall Eb/N0 Versus BER Performance

The PRISM chip set has been designed to be robust and energy efficient in packet mode communications. The demodulator uses coherent processing for data demodulation. Figure 18 below shows the performance of the baseband processor when used in conjunction with the HSP3724 IF limiter and the PRISM recommended IF filters. Off the shelf test equipment are used for the RF processing. The curves should be used as a guide to assess performance in a complete implementation.

Factors for carrier phase noise, multipath, and other degradations will need to be considered on an implementation by implementation basis in order to predict the overall performance of each individual system.

Figure 18 shows the curve for theoretical DBPSK/DQPSK demodulation with coherent demodulation as well as the PRISM performance measured for DBPSK and DQPSK. The losses include RF and IF radio losses; they do not reflect the HSP3824 losses alone. These are more realistic measurements. The HSP3824 baseband losses from theoretical by themselves are a small percentage of the overall loss.

The PRISM demodulator performs at less than 3dB from theoretical in a AWGN environment with low phase noise local oscillators. The observed errors occurred in groups of 4 and 6 errors and rarely singly. This is because of the error extension properties of differential decoding and descrambling.

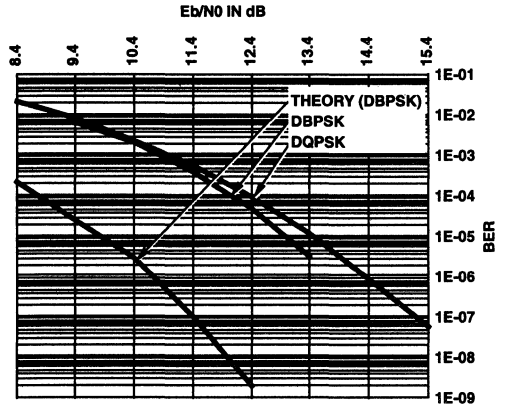


FIGURE 18. BER vs EB/N0 PERFORMANCE

Clock Offset Tracking Performance

The PRISM baseband processor is designed to accept data clock offsets of up to ±25ppm for each end of the link (TX and RX). This effects both the acquisition and the tracking performance of the demodulator. The budget for clock offset error is 0.75dB at ±50ppm as shown in Figure 19.

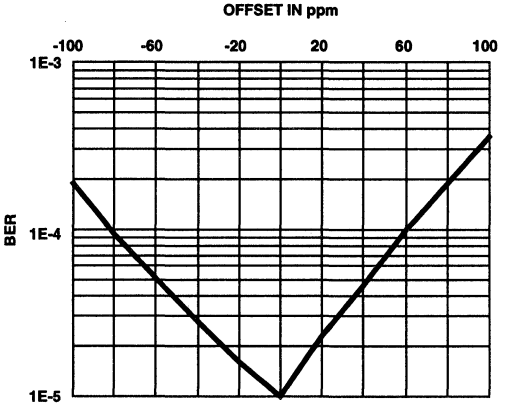


FIGURE 19. BER vs CLOCK OFFSET

Carrier Offset Frequency Performance

The correlators in the baseband processor are time invariant matched filter correlators otherwise known as parallel correlators. They use two samples per chip and are tapped at every other shift register stage. Their performance with carrier frequency offsets is determined by the phase roll rate due to the offset. For an offset of +50ppm (combined for both TX and RX) will cause the carrier to phase roll 22.5 degrees over the length of the correlator. This causes a loss of 0.22dB in correlation magnitude which translates directly to Eb/N0 performance loss. In the PRISM chip design, the correlator is not included in the carrier phase locked loop correction, so this loss occurs for both acquisition and data. Figure 20 shows the loss versus carrier offset taken out to +350kHz (120kHz is 50ppm at 2.4GHz).

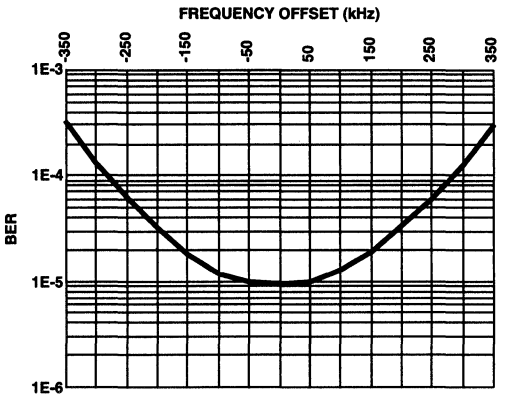


FIGURE 20. BER vs CARRIER OFFSET

I/Q Amplitude Imbalance

Imbalances in the signal cause differing effects depending on where they occur. In a system using a limiter, if the imbalances are in the transmitter, that is, before the limiter, amplitude imbalances translate into phase imbalances between the I and Q symbols. If they occur in the receiver after the limiter, they are not converted to phase imbalances in the symbols, but into vector phase imbalances on the composite signal plus noise. The following curve shows data taken with amplitude imbalances in the transmitter. Starting at the balanced condition, I = 100% of Q, the bit error rate degrades by two orders of magnitude for a 3dB drop in I (70%).

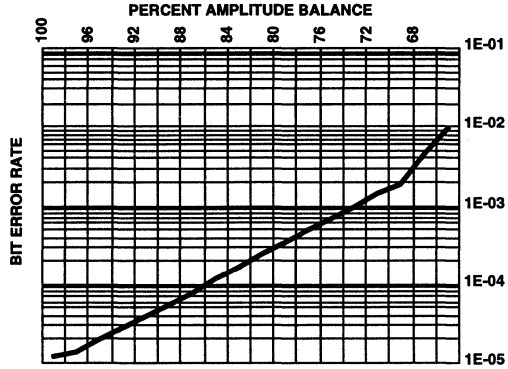


FIGURE 21. I/Q IMBALANCE EFFECTS

A Default Register Configuration

The registers in the HSP3824 are addressed with 14-bit numbers where the lower 2 bits of a 16-bit hexadecimal address are left as unused. This results in the addresses being in increments of 4 as shown in the table below. Table 10 shows the register values for a default Full Protocol configuration (Mode 3) with a single antenna. The data is transmitted as DQPSK. This is a recommended configuration for initial test and verification of the device and /or the radio design. The user can later modify the CR contents to reflect the system and the required performance of each specific application.

TABLE 10. CONTROL REGISTER VALUES FOR SINGLE ANTENNA ACQUISITION

REGISTER	NAME	TYPE	REG ADDR IN HEX	QPSK	BPSK
CR0	MODEM CONFIG. REG A	R/W	00	3C	64
CR1	MODEM CONFIG. REG B	R/W	04	00	00
CR2	MODEM CONFIG. REG C	R/W	08	07	24
CR3	MODEM CONFIG. REG D	R/W	0C	04	07
CR4	INTERNAL TEST REGISTER A	R/W	10	00	00
CR5	INTERNAL TEST REGISTER B	R/W	14	00	00
CR6	INTERNAL TEST REGISTER C	R	18	X	X
CR7	MODEM STATUS REGISTER A	R	1C	X	X
CR8	MODEM STATUS REGISTER B	R	20	X	X
CR9	I/O DEFINITION REGISTER	R/W	24	00	00
CR10	RSSI VALUESTATUS REGISTER	R	28	X	X
CR11	ADC_CAL_POS REGISTER	R/W	2C	01	01
CR12	ADC_CAL_NEG REGISTER	R/W	30	FD	FD
CR13	TX_SPREAD SEQUENCE(HIGH)	R/W	34	05	05
CR14	TX_SPREAD SEQUENCE (LOW)	R/W	38	B8	B8
CR15	SCRAMBLE_SEED	R/W	3C	00	00
CR16	SCRAMBLE_TAP (RX AND TX)	R/W	40	48	48
CR17	CCA_TIMER_TH	R/W	44	2C	2C
CR18	CCA_CYCLE_TH	R/W	48	03	03
CR19	RSSI_TH	R/W	4C	1E	1E
CR20	RX_SPREAD SEQUENCE (HIGH)	R/W	50	05	05
CR21	RX_SREAD SEQUENCE (LOW)	R/W	54	B8	B8
CR22	RX_SQ1_ IN_ACQ (HIGH) THRESHOLD	R/W	58	01	01
CR23	RX-SQ1_ IN_ACQ (LOW) THRESHOLD	R/W	5C	E8	E8
CR24	RX-SQ1_ OUT_ACQ (HIGH) READ	R	60	X	X
CR25	RX-SQ1_ OUT_ACQ (LOW) READ	R	64	X	X
CR26	RX-SQ1_ IN_DATA (HIGH) THRESHOLD	R/W	68	0F	0F
CR27	RX-SQ1-SQ1_ IN_DATA (LOW) THRESHOLD	R/W	6C	FF	FF
CR28	RX-SQ1_ OUT_DATA (HIGH)READ	R	70	X	X
CR29	RX-SQ1_ OUT_DATA (LOW) READ	R	74	X	X
CR30	RX-SQ2_ IN_ACQ (HIGH) THRESHOLD	R/W	78	00	00

TABLE 10. CONTROL REGISTER VALUES FOR SINGLE ANTENNA ACQUISITION (Continued)

REGISTER	NAME	TYPE	REG ADDR IN HEX	QPSK	BPSK
CR31	RX-SQ2- IN-ACQ (LOW) THRESHOLD	R/W	7C	CA	CA
CR32	RX-SQ2_ OUT_ACQ (HIGH) READ	R	80	X	X
CR33	RX-SQ2_ OUT_ACQ (LOW) READ	R	84	X	X
CR34	RX-SQ2_IN_DATA (HIGH)THRESHOLD	R/W	88	09	09
CR35	RX-SQ2_ IN_DATA (LOW) THRESHOLD	R/W	8C	80	80
CR36	RX-SQ2_ OUT_DATA (HIGH) READ	R	90	X	X
CR37	RX-SQ2_ OUT_DATA (LOW) READ	R	94	X	X
CR38	RX_SQ_READ; FULL PROTOCOL	R	98	X	X
CR39	RESERVED	W	9C	00	00
CR40	RESERVED	W	A0	00	00
CR41	UW_Time Out_LENGTH	R/W	A4	90	90
CR42	SIG_DBPSK Field	R/W	A8	0A	0A
CR43	SIG_DQPSK Field	R/W	AC	14	14
CR44	RX_SER_Field	R	B0	X	X
CR45	RX_LEN Field (HIGH)	R	B4	X	X
CR46	RX_LEN Field (LOW)	R	B8	X	X
CR47	RX_CRC16 (HIGH)	R	BC	X	X
CR48	RX_CRC16 (LOW)	R	C0	X	X
CR49	UW -(HIGH)	R/W	C4	F3	F3
CR50	UW _(LOW)	R/W	C8	A0	A0
CR51	TX_SER_F	R/W	CC	00	00
CR52	TX_LEN (HIGH)	R/W	D0	FF	FF
CR53	TX_LEN(LOW)	R/W	D4	FF	FF
CR54	TX_CRC16 (HIGH)	R	D8	X	X
CR55	TX_CRC16 (LOW)	R	DC	X	X
CR56	TX_PREM_LEN	R/W	E0	80	80

Control Registers

The following tables describe the function of each control register along with the associated bits in each control register.

CONFIGURATION REGISTER 0 ADDRESS (0h) MODEM CONFIGURATION REGISTER A

Bit 7	This bit selects the transmit antenna, controlling the output ANT_SEL pin. It is only used in half duplex mode. (Bit 5 = 0) Logic 1 = Antenna A. Logic 0 = Antenna B.
Bit 6	In single antenna operation this bit is used as the output of the ANT_SEL pin. In dual antenna mode this bit is ignored. Logic 1 = Antenna A. Logic 0 = Antenna B.
Bit 5	This control bit is used to select between full duplex and half duplex operation. If set for full duplex operation, the ANT_SEL pin reflects the setting of CR0 bit 7 when TX_PE is active and reflects the receiver's choice when TX_PE is inactive. In full duplex operation, the ANT_SEL pin always reflects the receiver's choice antenna. Logic 1 = full duplex. Logic 0 = half duplex.
Bit 4, 3	These control bits are used to select one of the four input Preamble Header modes for transmitting data. The preamble and header are DBPSK for all modes of operation. Mode 0 is followed by DBPSK data. For modes 1-3, the data can be configured as either DBPSK or DQPSK. This is a "don't care" if the header is generated externally.

MODE	BIT 4	BIT 3	MODE DESCRIPTION
0	0	0	Preamble with SFD Field.
1	0	1	Preamble with SFD, and CRC16.
2	1	0	Preamble with SFD, Length, and CRC16.
3	1	1	Full preamble and header.

Bit 2	This control bit is used to enable the SFD (Start Frame Delimiter) timer. If the time is set and expires before the SFD has been detected, the HSP3824 will return to its acquisition mode. Logic 1: Enables the SFD timer to start counting once the PN acquisition has been achieved. Logic 0: Disables the SFD Timer.
Bit 1	This control bit enables counting the number of data bits per the length field embedded in the header. Only used in header modes 2 and 3. Then according to the count it returns the processor into its acquisition mode at the end of the count. If length field is 0000h, modem will reset at end of SFD regardless of this bit setting. Logic 1 = Enable Length Time Out. Logic 0 = Disabled.
Bit 0	Unused don't care.

CONFIGURATION REGISTER 1 ADDRESS (04h) MODEM CONFIGURATION REGISTER B

Bit 7	When active this bit maintains the RXCLK and TXLK rates constant for preamble and data transfers even if the data is modulated in DQPSK. This bit is used if the external processor can not accommodate rate changes. This is an active high signal. The rate used is the QPSK rate and the BPSK header bits are double clocked.
Bit 6, 5, 4, 3, 2	These control bits are used to define a binary count (N) from 0 - 31. This count is used to assert TX_RDY N - clocks (TXCLK) before the beginning of the first data bit. If this is set to zero, then the TX_RDY will be asserted immediately after the last bit of the Preamble Header.
Bit 1	When active the internal A/D calibration circuit sets the reference to mid-scale. When inactive then the calibration circuit adjusts the reference voltage in real time to optimize I, Q levels. Logic 1 = Reference set at mid-scale (fixed). Logic 0 = Real time reference adjustment.
Bit 0	When active the A/D calibration circuit is held at its last value. Logic 1 = Reference held at the most recent value. Logic 0 = Real time reference level adjustment.

CONFIGURATION REGISTER 2 ADDRESS (08h) MODEM CONFIGURATION REGISTER C

Bit 7, 6

These control bits are used to select the number of chips per symbol used in the I and Q paths of the receiver matched filter correlators (see table below).

CHIPS PER SYMBOL	BIT 7	BIT 6
11	0	0
13	0	1
15	1	0
16	1	1

Bit 5

This control bit is used to disable the CRC16 check. When this bit is set, the processor will accept the received packet and any packet error checks have to be detected externally. The HSP3824 will remain in the receive mode until either the carrier is lost or the network processor resets the device to the acquisition mode, or if, in modes 2 or 3, the length times out.
Logic 1 = Disable receiver error checks.
Logic 0 = Enable receiver checks.

Bit 4, 3

These control bits are used to select the divide ratio for the demodulators receive chip clock timing.The value of N is determined by the following equation:
Symbol Rate = MCLK/(N x Chips per symbol).

MASTER CLOCK/N	BIT 4	BIT 3
N = 2	0	0
N = 4	0	1
N = 8	1	0
N = 16	1	1

Bit 2

This control bit sets the receiver into single or dual antenna mode. The Preamble acquisition processing length and whether the modem scans antennas is controlled by this bit. If in single antenna mode, the ANT_SEL pin reflects CR0 bit 6 otherwise it reflects the receiver's choice of antenna.
Logic 0 = Acquisition processing is for dual antenna acquisition.
Logic 1 = Acquisition processing is for single antenna acquisition.

Bit 1, 0

These control bits are used to indicate one of the four Preamble Header modes for receiving data. Each of the modes includes different combinations of Header fields. Users can choose the mode with the fields that are more appropriate for their networking requirements. The Header fields that are combined to form the various modes are:

- SFD field
- CRC16 field
- Data length field (indicates the number of data bits that follow the Header information)
- Full protocol Header

INPUT MODE	BIT 1	BIT 0	RECEIVE PREAMBLE - HEADER FIELDS
0	0	0	Preamble, with SFD Field
1	0	1	Preamble, with SFD, CRC16
2	1	0	Preamble, with SFD Length, CRC16
3	1	1	Preamble, with Full Protocol Header

CONFIGURATION REGISTER 3 ADDRESS (0Ch) MODEM CONFIGURATION REGISTER D

Bit 7

Reserved (must set to "0").

CONFIGURATION REGISTER 3 ADDRESS (0Ch) MODEM CONFIGURATION REGISTER D (Continued)

Bit 6, 5	These control bits combined are used to select the number of chips per symbol used in the I and Q transmit paths (see table below).

CHIPS PER	BIT 6	BIT 5
11	0	0
13	0	1
15	1	0
16	1	1

Bit 4, 3	These control bits are used to select the divide ratio for the transmit chip clock timing. NOTE: The value of N is determined by the following equation: Symbol Rate = MCLK/(N x Chips per symbol)

MASTER	BIT 4	BIT 3
N = 2	0	0
N = 4	0	1
N = 8	1	0
N = 16	1	1

Bit 2	This control bit is used to select the origination of Preamble/Header information. Logic 1: The HSP3824 generates the Preamble and Header internally by formatting the programmed header information and generating a TX_RDY to indicate the beginning of the data packet. Logic 0: Accepts the Preamble/Header information from an externally generated source.
Bit 1	This control bit is used to indicate the signal modulation type for the transmitted data packet. When configured for mode 0 header, or mode 3 and external header, this bit is ignored. See Register 0 bits 4 and 3. Logic 1 = DBPSK modulation for data packet. Logic 0 = DQPSK modulation for data packet.
Bit 0	This control bit is used to indicate the signal modulation type for the received data packet Used only with header modes 1 and 2. See register 2 bits 1 and 0. Logic 1 = DBPSK. Logic 0 = DQPSK.

CONFIGURATION REGISTER 4 ADDRESS (10h) INTERNAL TEST REGISTER A

Bit 7 - 0	These control bits are used to direct various internal signals to test port output pins. These internal signals are monitored to fault isolate the device at manufacturing testing. During normal operation, the value 0h is recommended. This will result to the following signals becoming available at the output test pins of the device: Pin 46 (TEST7): Carrier Sense (CRS), a Logic 1 indicates PN lock. Pin 45 (TEST6): Energy Detect (ED), a Logic 1 indicates that there is energy detected in the channel. The ED goes active when the RSSI exceeds the threshold level programmed by the user. Pin 1 (TEST_CK): PN clock.

CONFIGURATION REGISTER 5 ADDRESS (14h,18h) INTERNAL TEST REGISTER B

Bits 7 - 0	These bits need to be programmed to 0h. They are used for manufacturing test only.

CONFIGURATION REGISTER 7 ADDRESS (1Ch) MODEM STATUS REGISTER A

Bit 7	This bit indicates the status of the TX_RDY output pin. TX_RDY is used only when the HSP3824 generates the Preamble/Header data internally. Logic 1: Indicates that the HSP3824 has completed transmitting Preamble header information and is ready to accept data from the external source (i.e. MAC) to transmit. Logic 0: Indicates that the HSP3824 is in the process of transmitting Preamble Header information.
Bit 6	This status bit indicates the antenna selected by the device. Logic 0: Antenna A is selected. Logic 1: Antenna B is selected.

CONFIGURATION REGISTER 7 ADDRESS (1Ch) MODEM STATUS REGISTER A (Continued)

Bit 5	This status bit indicates the present state of clear channel assessment (CCA) which is output pin 32. The CCA is being asserted as a result of a channel energy monitoring algorithm that is a function of RSSI, carrier sense, and time out counters that monitor the channel activity.
Bit 4	This status bit, when active indicates Carrier Sense, or PN lock. Logic 1: Carrier present. Logic 0: No Carrier Sense.
Bit 3	This status bit indicates whether the RSSI signal is above or below the programmed RSSI 6-bit threshold setting. This signal is referred as Energy Detect (ED). Logic 1: RSSI is above the programmed threshold setting. Logic 0: RSSI is below the programmed threshold setting.
Bit 2	This bit indicates the status of the output control pin MD_RDY (pin 34). It signals that a valid Preamble/Header has been received and that the next available bit on the TXD bus will be the first data packet bit. Logic 1: Envelopes the data packet as it becomes available on pin 3 (TXD). Logic 0: No data packet on TXD serial bus.
Bit 1	This status bit indicates whether the external device has acknowledged that the channel is clear for transmission. This is the same as the input signal TX_PE on pin 2. Logic 1 = Acknowledgment that channel is clear to transmit. Logic 0 = Channel is NOT clear to transmit.
Bit 0	This status bit indicates that a valid CRC16 has been calculated. The CRC16 is calculated on the Header information. The CRC16 does not cover the preamble bits. Logic 1 = Valid CRC16 check. Logic 0 = Invalid CRC16 check.

CONFIGURATION REGISTER 8 ADDRESS (20h) MODEM STATUS REGISTER B

Bit 7	This status bit is meaningful only when the device operates under the full protocol mode. Errors imply CRC errors of the header fields. Logic 0 = Valid packet received. Logic 1 = Errors in received packet.
Bit 6	This bit is used to indicate the status of the SFD search timer. The device monitors the incoming Header for the SFD. If the timer, times out the HSP3824 returns to its signal acquisition mode looking to detect the next Preamble and Header. Logic 1 = SFD not found, return to signal acquisition mode. Logic 0 = No time out during SFD search.
Bit 5	This status bit is used to indicate the modulation type for the data packet. This signal is generated by the header detection circuitry in the receive interface. Logic 0 = DBPSK. Logic 1 = DQPSK.
Bit 4	Unused, don't care.
Bit 3	Unused, don't care.
Bit 2	Unused, don't care.
Bit 1	Unused, don't care.
Bit 0	Unused, don't care.

CONFIGURATION REGISTER 9 ADDRESS (24h) I/O DEFINITION REGISTER

	This register is used to define the phase of clocks and other interface signals.
Bit 7	This bit needs to always be set to logic 0.
Bit 6	This control bit selects the active level of the MD_RDY output pin 34. Logic 1 = MD_RDY is active 0. Logic 0 = MD_RDY is active 1.

CONFIGURATION REGISTER 9 ADDRESS (24h) I/O DEFINITION REGISTER

Bit 5	This control bit selects the active level of the Clear Channel Assessment (CCA) output pin 32. Logic 1 = CCA active 1. Logic 0 = CCA active 0.
Bit 4	This control bit selects the active level of the Energy Detect (ED) output which is an output pin at the test port, pin 45. Logic 1 = ED active 0. Logic 0 = ED active 1.
Bit 3	This control bit selects the active level of the Carrier Sense (CRS) output pin which is an output pin at the test port, pin 46. Logic 1 = CRS active 0. Logic 0 = CRS active 1.
Bit 2	This control bit selects the active level of the transmit ready (TX_RDY) output pin 5. Logic 1 = TX_RDY active 0. Logic 0 = TX_RDY active 1.
Bit 1	This control bit selects the active level of the transmit enable (TX_PE) input pin 2. Logic 1 = TX_PE active 0. Logic 0 = TX_PE active 1.
Bit 0	This control bit selects the phase of the transmit output clock (TXCLK) pin 4. Logic 1 = Inverted TXCLK. Logic 0 = NON-Inverted TXCLK

CONFIGURATION REGISTER 10 ADDRESS (28h) RSSI VALUE REGISTER

Bits 0 - 7

This is a read only register reporting the value of the RSSI analog input signal from the on chip 6-bit ADC. This register is updated at (chip rate/11). Bits 7 and 6 are not used and set to Logic 0.
Example:

	BITS (0:7)	RANGE
RSSI_STAT	7 6 5 4 3 2 1 0	
	0 0 0 0 0 0 0 0	00h (Min)
	0 0 1 1 1 1 1 1	3Fh (Max)

CONFIGURATION REGISTER 11 ADDRESS (2ch) A/D CAL POS REGISTER

Bits 0 - 7	This 8-bit control register contains a binary value used for positive increment for the level adjusting circuit of the A/D reference. The larger the step the faster the level reaches saturation.

CONFIGURATION REGISTER 12 ADDRESS (30h) A/D CAL NEG REGISTER

Bits 0 - 7	This 8-bit control register contains a binary value used for the negative increment for the level adjusting reference of the A/D. The number is programmed as 256 - the value wanted since it is a negative number.

CONFIGURATION REGISTER 13 ADDRESS (34h) TX SPREAD SEQUENCE (HIGH)

Bits 0 - 7

This 8-bit register is programmed with the upper byte of the transmit spreading code. This code is used for both the I and Q signalling paths of the transmitter. This register combined with the lower byte TX_SPREAD(LOW) generates a transmit spreading code programmable up to 16 bits. Code lengths permitted are 11, 13, 15, and 16. Right justified MSB first.

SOME SUITABLE CODES

LENGTH	CR13	CR14	TYPE
11	05	B8	Barker
13	1F	35	Barker
15	1F	35	Modified Barker
16	1F	35	Modified Barker

CONFIGURATION REGISTER 14 ADDRESS (38h) TX SPREAD SEQUENCE (LOW)

Bits 0 - 7

This 8-bit register is programmed with the lower byte of the transmit spreading code. This code is used for the I and Q signalling paths of the transmitter. This register combined with the higher byte TX_SPREAD(HIGH) generates the transmit spreading code programmable up to 16 bits.
The example below illustrates the bit positioning for one of the 11 bit Barker PN codes.
Example:

Transmit Spreading Code 11-Bit Barker Word Right Justified MSB First.

	MSB	LSB
TX_SPREAD(HIGH)	15 14 13 12 11 10 9 8	
TX_SPREAD(LOW)		7 6 5 4 3 2 1 0
11-bit Barker code	X X X X X 1 0 1	1 0 1 1 1 0 0 0

CONFIGURATION REGISTER 15 ADDRESS (3Ch) SCRAMBLER SEED

Bits 0 - 7

This register contains the 7-bit (seed) value for the transmit scrambler which is used to preset the transmit scrambler to a known starting state. The MSB bit position (7) is unused and must be programmed to a Logic 0. The example below illustrates the bit positioning of seed.

CONFIGURATION REGISTER 16 ADDRESS (40h) SCRAMBLER TAP

Bits 0 - 7

This register is used to configure the transmit scrambler with a 7-bit polynomial tap configuration. The transmit scrambler is a 7-bit shift register, with 7 configurable taps. A logic 1 is the respective bit position enables that particular tap. The MSB bit 7 is not used and it is set to a Logic 0. The example below illustrates the register configuration for the polynomial $F(x) = 1 + X^{-4}+X^{-7}$. Each clock is a shift left

		LSB
Bits (0:7)		7 6 5 4 3 2 1 0
		$XZ^{-7}Z^{-6}Z^{-5}Z^{-4}Z^{-3}Z^{-2}Z^{-1}$
Scrambler Taps	$F(x) = 1 + X^{-4}+X^{-7}$	0 1 0 0 1 0 0 0

CONFIGURATION REGISTER 17 ADDRESS (44h)CCA TIMER THRESHOLD

Bits 0 - 7

This 8-bit register is used to configure the period of the time-out threshold of the CCA watchdog timer. If the channel is busy the timer counts until it reaches the programmed value and at that point it declares that the channel is clear independent of the actual energy measured within the channel. This register is programmable up to 8 bits.

$$\text{Time (ms)} = 1000 \bullet \frac{N \bullet 5632}{\text{Chip Rate}}, \text{ where N is the programmable value of CR17.}$$

For example, for a chip rate of 11 MCPS and a desired timeout of ~11ms, N = 2ch.

	LSB	
Bits (0:7)	7 6 5 4 3 2 1 0	
	0 0 0 0 0 0 1 0	02h (Min)
CCA_TIMER_TH	1 1 1 1 1 1 1 1	FFh (Max)

CONFIGURATION REGISTER 18 ADDRESS (48h) CCA CYCLE THRESHOLD

Bits 0 - 7

This 8-bit register is used to configure how many times the CCA timer is allowed to reach its maximum count before the channel is declared clear for transmission independent of the actual energy in the channel. This is an outer counter loop of the CCA timer. Each increment represents a time out of the CCA timer. Use a value of 03h for a time out of 2 CCA timer counts.

	MSB LSB	
Bits (0:7)	7 6 5 4 3 2 1 0	
	0 0 0 0 0 0 1 0	2h; 1 CCA timer (Min)
CCA_TIMER_TH	1 1 1 1 1 1 1 1	FFh; 256 CCA timer (Max)

CONFIGURATION REGISTER 19 ADDRESS (4Ch) RSSI THRESHOLD, ENERGY DETECT

Bits 0 - 7	This register contains the value for the RSSI threshold for measuring and generating energy detect (ED). When the RSSI exceeds the threshold ED is declared. ED indicates the presence of energy in the channel. The threshold that activates ED is programmable. Bits 7 an 6 of this register are not used and set to Logic 0.

	MSB LSB	
Bits (0:7)	7 6 5 4 3 2 1 0	
	0 0 0 0 0 0 0 0	00h (Min)
RSSI_STAT	0 0 1 1 1 1 1 1	3Fh (Max)

CONFIGURATION REGISTER 20 ADDRESS (50h) RX SPREAD SEQUENCE (HIGH)

Bits 0 - 7	This 8-bit register is programmed with the upper byte of the receive despreading code. This code is used for both the I and Q signalling paths of the receiver. This register combined with the lower byte RX_SPRED(LOW) generates a receive despreading code programmable up to 16 bits. Right justified MSB first. See address 13 and 14 for example.

CONFIGURATION REGISTER 21 ADDRESS (54h) RX SPREAD SEQUENCE (LOW)

Bits 0 - 7	This 8-bit register is programmed with the lower byte of the receiver despreading code. This code is used for both the I and Q signalling paths of the receiver. This register combined with the upper byte RX_SPRED(HIGH) generates a receive despreading code programmable up to 16 bits.

CONFIGURATION REGISTER 22 ADDRESS (58h) RX SIGNAL QUALITY 1 ACQ (HIGH) THRESHOLD

Bits 0 - 7	This control register contains the upper byte bits (8 - 14) of the bit sync amplitude signal quality threshold used for acquisition. This register combined with the lower byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements made during acquisition at each antenna dwell. This threshold comparison is added with the SQ2 threshold in registers 30 and 31 for acquisition. A lower value on this threshold will increase the probability of detection and the probability of false alarm. Set the threshold according to instructions in the text.

CONFIGURATION REGISTER 23 ADDRESS (5Ch) RX SIGNAL QUALITY 1 ACQ THRESHOLD (LOW)

Bits 0 - 7	This control register contains the lower byte bits (0 - 7) of the bit sync amplitude signal quality threshold used for acquisition. This register combined with the upper byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurement made during acquisition at each antenna dwell.

CONFIGURATION REGISTER 24 ADDRESS (60h) RX SIGNAL QUALITY 1 ACQ READ (HIGH)

Bits 0 - 7	This status register contains the upper byte bits (8 - 14) of the measured signal quality threshold for the bit sync amplitude used for acquisition. This register combined with the lower byte represents a 15-bit value, representing the measured bit sync amplitude. This measurement is made at each antenna dwell and is the result of the best antenna.

CONFIGURATION REGISTER 25 ADDRESS (64h) RX SIGNAL QUALITY 1 ACQ READ (LOW)

Bits 0 - 7	This register contains the lower byte bits (0 - 7) of the measured signal quality threshold for the bit sync amplitude used for acquisition. This register combined with the higher byte represents a 15-bit value, of the measured bit sync amplitude. This measurement is made at each antenna dwell and is the result of the best antenna.

CONFIGURATION REGISTER 26 ADDRESS (68h) RX SIGNAL QUALITY 1 DATA THRESHOLD (HIGH)

Bits 0 - 7	This control register contains the upper byte bits (8-14) of the bit sync amplitude signal quality threshold used for drop lock decisions. This register combined with the lower byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements, made every 128 symbols. These thresholds set the drop lock probability. A higher value will increase the probability of dropping lock.

CONFIGURATION REGISTER ADDRESS 27 (6Ch) RX SIGNAL QUALITY 1 DATA THRESHOLD (LOW)

Bits 0 - 7	This control register contains the lower byte bits (0 - 7) of the bit sync amplitude signal quality threshold used for drop lock decisions. This register combined with the upper byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements, made every 128 symbols.

CONFIGURATION REGISTER 28 ADDRESS (70h) RX SIGNAL QUALITY 1 DATA (high) THRESHOLD READ (HIGH)

Bits 0 - 7	This status register contains the upper byte bits (8-14) of the measured signal quality of bit sync amplitude used for drop lock decisions. This register combined with the lower byte represents a 15-bit value, representing the measured signal quality for the bit sync amplitude. This measurement is made every 128 symbols.

CONFIGURATION REGISTER 29 ADDRESS (74h) RX SIGNAL QUALITY 1 DATA THRESHOLD READ (LOW)

Bits 0 - 7	This register contains the lower byte bits (0-7) of the measured signal quality of bit sync amplitude used for drop lock decisions. This register combined with the lower byte represents a 16-bit value, representing the measured signal quality for the bit sync amplitude. This measurement is made every 128 symbols.

CONFIGURATION REGISTER 30 ADDRESS (78h) RX SIGNAL QUALITY 2 ACQ THRESHOLD (HIGH)

Bits 0 - 7	This control register contains the upper byte bits (8-15) of the carrier phase variance threshold used for acquisition. This register combined with the lower byte represents a 16-bit threshold value for carrier phase variance measurement made during acquisition at each antenna dwell and is based on the choice of the best antenna. This threshold is used with the bit sync threshold in registers 22 and 23 to declare acquisition. A higher value in this threshold will increase the probability of acquisition and false alarm.

CONFIGURATION REGISTER 31 ADDRESS (7Ch) RX SIGNAL QUALITY 2 ACQ THRESHOLD (LOW)

Bits 0 - 7	This control register contains the lower byte bits (0-7) of the carrier phase variance threshold used for acquisition.

CONFIGURATION REGISTER 32 ADDRESS (80h) RX SIGNAL QUALITY 2 ACQ READ (HIGH)

Bits 0 - 7	This status register contains the upper byte bits (8-15) of the measured signal quality of the carrier phase variance used for acquisition. This register combined with the lower byte generates a 16-bit value, representing the measured signal quality of the carrier phase variance. This measurement is made during acquisition at each antenna dwell and is based on the selected best antenna.

CONFIGURATION REGISTER 33 ADDRESS (84h) RX SIGNAL QUALITY 2 ACQ READ (LOW)

Bits 0 - 7	This status register contains the lower byte bits (0-7) of the measured signal quality of the carrier phase variance used for acquisition. This register combined with the lower byte generates a 16-bit value, representing the measured signal quality of the carrier phase variance. This measurement is made during acquisition at each antenna dwell and is based on the selected best antenna

CONFIGURATION REGISTER 34 ADDRESS (88h) RX SIGNAL QUALITY 2 DATA THRESHOLD (HIGH)

Bits 0-7	This control register contains the upper byte bits (8-15) of the carrier phase variance threshold. This register combined with the lower byte represents a 16-bit threshold value for the carrier phase variance signal quality measurements made every 128 symbols.

CONFIGURATION REGISTER 35 ADDRESS (8Ch) RX SIGNAL QUALITY 2 DATA THRESHOLD (LOW)

Bits 0-7	This control register contains the lower byte bits (0-7) of the carrier phase variance threshold. This register combined with the upper byte) represents a 16-bit threshold value for the carrier phase variance signal quality measurements made every 128 symbols.

CONFIGURATION REGISTER 36 ADDRESS (90h) RX SIGNAL QUALITY 2 DATA READ (HIGH)

Bits 0-7	This status register contains the upper byte bits (8-15) of the measured signal quality of the carrier phase variance. This register combined with the lower byte represents a 16-bit value, of the measured carrier phase variance. This measurement is made every 128 symbols.

CONFIGURATION REGISTER 37 ADDRESS (94h) RX SIGNAL QUALITY 2 DATA READ (LOW)

Bits 0-7	This register contains the lower byte bits (0-7) of the measured signal quality of the carrier phase variance. This register combined with the represents a 16-bit value, of the measured carrier phase variance. This measurement is made every 128 symbols.

CONFIGURATION REGISTER ADDRESS 38 (98h) RX SIGNAL QUALITY 8-BIT READ

Bits 0 - 7	This 8-bit register contains the bit sync amplitude signal quality measurement derived from the 16-bit Bit Sync signal quality value stored in the CR28-29 registers. This value is the result of the signal quality measurement for the best antenna dwell. The signal quality measurement provides 256 levels of signal to noise measurement.

CONFIGURATION REGISTER 39 ADDRESS RESERVED

	Reserved

CONFIGURATION REGISTER 40 ADDRESS RESERVED

	Reserved

CONFIGURATION REGISTER 41 ADDRESS (A4h) SFD SEARCH TIME

Bits 0 - 7	This register is programmed with an 8-bit value which represents the length of time for the demodulator to search for a SFD in a receive Header. Each bit increment represents 1 symbol period.

CONFIGURATION REGISTER 42 ADDRESS (A8h) DSBPSK SIGNAL

Bits 0 - 7	This register contains an 8-bit value indicating the data packet modulation is DBPSK. This value will be a OAH for full protocol operation at a data rate of 1 MBPS, and is used in the transmitted Signalling Field of the header. This value will also be used for detecting the modulation type on the received Header.

CONFIGURATION REGISTER 43 ADDRESS (ACh) DQPSK SIGNAL

Bits 0 - 7	This register contains the 8-bit value indicating the data packet modulation is DQPSK. This value will be a 14h for full protocol operation at a data rate of 2 MBPS and is used in the transmitted Signalling Field of the header. This value will also be used for detecting the modulation type on the received header.

CONFIGURATION REGISTER 44 ADDRESS (B0h) RX SERVICE FIELD (RESERVED)

Bits 0 - 7	This register contains the detected received 8-bit value of the Service Field for the Header. This field is reserved for the full protocol mode for future use and should be always a 00h.

CONFIGURATION REGISTER 45 ADDRESS (B4h) RX DATA LENGTH (HIGH)

Bits 0 - 7	This register contains the detected higher byte (bits 8-15) of the received Length Field contained in the Header. This byte combined with the lower byte indicates the number of transmitted bits in the data packet.

CONFIGURATION REGISTER 46 ADDRESS (B8h) RX DATA LENGTH (LOW)

Bits 0 - 7	This register contains the detected lower byte of the received Length Field contained in the Header. This byte combined with the upper byte indicates the number of transmitted bits in the data packet.

CONFIGURATION REGISTER 47 ADDRESS (BCh) RX CRC16 (HIGH)

Bits 0 - 7	This register contains the upper byte bits (8 -15) of the received CRC16 field Header. This register combined with the lower byte represents a 16-bit CRC16 value protecting transmitted header. The fields protected are selected by configuring the header control bits at configuration register 2.

CONFIGURATION REGISTER 48 ADDRESS (C0h) RX CRC16 (LOW)

Bits 0 - 7	This register contains the lower byte bits (0-7) of the received CRC16 field Header. This register combined with the upper byte represents a 16-bit CRC16 value protecting transmitted header. The fields protected are selected by configuring the header control bits at configuration register 2.

	MSB LSB
RX_CRC16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RX_CRC16(HIGH)	7 6 5 4 3 2 1 0
RX_CRC16(LOW)	7 6 5 4 3 2 1 0

NOTE: The receive CRC16 Field protects the following fields depending upon the mode selection, as defined in configuration register 2.

Mode 0 CRC16 not used
Mode 1 CRC16 protects SFD
Mode 2 CRC16 protects SFD, and Length Field
Mode 3 CRC16 protects Signalling Field, Service Field, and Length Field

CONFIGURATION REGISTER 49 ADDRESS (C4h) SFD (HIGH)

Bits 0 - 7	This 8-bit register contains the upper byte bits (8-15) of the SFD used for both the Transmit and Receive header. This register combined with the lower byte represents the 16-bit value for the SFD field.

CONFIGURATION REGISTER 50 ADDRESS (C8h) SFD (LOW)

Bits 0 - 7	This 8-bit register contains the upper byte bits (0-7) of the SFD used for both the Transmit and Receive header. This register combined with the lower byte represents the 16-bit value for the SFD field.

CONFIGURATION REGISTER 51 ADDRESS (CCh) TX SERVICE FIELD

Bits 0 - 7	This 8-bit register is programmed with the 8-bit value of the Service Field to be transmitted in a Header. This field is reserved for future use and should be always a 00h.

CONFIGURATION REGISTER 52 ADDRESS (D0h) TX DATA LENGTH FIELD (HIGH)

Bits 0 - 7	This 8-bit register contains the higher byte (bits 8-15) of the transmit Length Field described in the Header. This byte combined with the lower byte indicates the number of bits to be transmitted in the data packet. CR 52/53 should not be set to 0000h. This value would cause the modem to reset after SFD.

CONFIGURATION REGISTER 53 ADDRESS (D4h) TX DATA LENGTH FIELD (LOW)

Bits 0 - 7	This 8-bit register contains the lower byte bits (0-7) of the transmit Length Field described in the Header. This byte combined with the higher byte indicates the number of bits to be transmitted in the data packet, including the MAC payload header. CR 52/53 should not be set to 0000h. This value would cause the modem to reset after SFD.

CONFIGURATION REGISTER 54 ADDRESS (D8h) TX CRC16 (HIGH)

Bits 0 - 7	This 8-bit register contains the upper byte (bits 8-15) of the transmitted CRC16 Field for the Header. This register combined with the lower byte represents a 16-bit CRC16 value calculated by the HSP3824 to protect the transmitted header. The fields protected are selected by configuring the header mode control bits at register address 02.

CONFIGURATION REGISTER 55 ADDRESS (DCh) TX CRC16 (LOW)

Bits 0 - 7

This 8-bit register contains the lower byte (bits 0-7) of the transmitted CRC16 Field for the Header. This register combined with the higher byte represents a 16-bit CRC16 value calculated by the HSP3824 to protect the transmitted header. The fields protected are selected by configuring the header mode control bits at register address 02.
configuration register 2

	MSB LSB
RX_CRC16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RX_CRC16(HIGH)	7 6 5 4 3 2 1 0
RX_CRC16(LOW)	7 6 5 4 3 2 1 0

NOTE: The receive CRC16 Field protects the following fields depending upon the mode selection. as defined in register address 02.

Mode 0 CRC16 not used
Mode 1 CRC16 protects SFD
Mode 2 CRC16 protects SFD, and Length Field
Mode 3 CRC16 protects Signalling Field, Service Field, and Length Field

CONFIGURATION REGISTER 56 ADDRESS (E0h) TX PREAMBLE LENGTH

Bits 0 - 7	This register contains the count for the Preamble length counter. This counter is programmable up to 8 bits and represents the number of preamble bits. This should be set at 50h for 1 antenna and 80h for dual antennas.

Absolute Maximum Ratings

Supply Voltage 7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC}+0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +2.70V to +5.50V
Operating Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 5) θ_{JA} (°C/W)
TQFP Package 80
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Junction Temperature . . . . . 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

Die Characteristics

Gate Count . . . . . 25,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 3.0V to 5.0V ±10%, T_A = -40°C to 85°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = 3.5V, CLK Frequency 22MHz (Notes 6, 7)	-	42	50	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = Max, Outputs Not Loaded	-	1	2.5	mA
Input Leakage Current	I_I	V_{CC} = Max, Input = 0V or V_{CC}	-10	1	10	µA
Output Leakage Current	I_O	V_{CC}= Max, Input = 0V or V_{CC}	-10	1	10	µA
Logical One Input Voltage	V_{IH}	V_{CC} = Max, Min	0.7 V_{CC}		-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = Min, Max	-		V_{CC}/3	V
Logical One Output Voltage	V_{OH}	I_{OH} = -1mA, V_{CC} = Min	V_{CC}-0.4	V_{CC}-.2	-	V
Logical Zero Output Voltage	V_{OL}	I_{OL} = 2mA, V_{CC} = Min	-	.2	0.4	V
Input Capacitance	C_{IN}	CLK Frequency 1MHz. All measurements referenced to GND. T_A = 25°C, Note 7	-	5	10	pF
Output Capacitance	C_{OUT}		-	5	10	pF

NOTES:

6. Output load 30pF. I_{CCOP} = 5.5 + 4.7(V) + 3.7E - 7 (V)(f); V = Volts, f = Freq. Example: 5.5 + 4.7(5.5) + 3.7E - 7(5.5)(22E6) = 77
7. Not tested, but characterized at initial design and at major process/design changes.

AC Electrical Specifications

V_{CC} = 3.0V to 5.0V ±10%, T_A = -40°C to 85°C, (Note 8)

PARAMETER	SYMBOL	33MHz		UNITS
		MIN	MAX	
CLK Period (MCLK)	t_{CP}	30	-	ns
CLK High (MCLK)	t_{CH}	9	-	ns
CLK Low (MCLK)	t_{CL}	9	-	ns
Setup Time to MCLK (TXD)	t_{S2}	10	-	ns
Hold Time from MCLK (TXD)	t_{H2}	20	-	ns
SCLK Clock Period	t_P	100ns or MCLK	-	ns
SCLK High	t_H	20	-	ns
SCLK Low	t_L	20	-	ns
Set up to SCLK (SD, AS, R/$\overline{W}$, $\overline{CS}$)	t_{S1}	20	-	ns
Hold Time from SCLK (SD, AS, R/$\overline{W}$, $\overline{CS}$)	t_{H1}	20	-	ns
SD_{OUT} from SCLK	t_{D1}	-	30	ns
Output Enable of Sd from R/$\overline{W}$ High	t_{E1}	-	20	ns (Note 9)
Output disable of SD after R/$\overline{W}$ Low	t_{F1}	-	20	ns (Note 9)
TXCLK, TXRDY, I, Q from MCLK	t_{D2}	-	35	ns
RXCLK, MD_RDY, RXD from MCLK	t_{D3}	-	35	ns
TEST 0-7, CCA, AGC, from MCLK	t_{D4}	-	40	ns
ANSTEL, TEST_CK	-	-	-	-
OUTPUT Rise/Fall		-	10	ns (Note 9, 10)

NOTES:

8. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -1mA. Input reference level all inputs 1.5V. Test $V_{IH} = V_{CC}$, V_{IL} = 0V; $V_{OH} = V_{OL} = V_{CC}/2$.
9. Not tested, but characterized at initial design and at major process/design changes.
10. Measured from V_{IL} to V_{IH}.

I and Q A/D AC Electrical Specifications

PARAMETER	MIN	TYP	MAX	UNITS
Full Scale Input Voltage (V_{P-P})	0.25	0.50	1.0	V
Input Bandwidth (-0.5dB)	-	20	-	MHz
Input Capacitance	-	5	-	pF
Input Impedance (DC)	5	-	-	kΩ
FS (Sampling Frequency)	-	-	44	MHz

RSSI A/D Electrical Specifications

PARAMETER	MIN	TYP	MAX	UNITS
Full Scale Input Voltage (V_{P-P})	-	-	1.15	V
Input Bandwidth (0.5dB)	1MHz	-	-	MHz
Input Capacitance (DC)	-	7pF	-	pF
Input Impedance	1M	-	-	MΩ

Absolute Maximum Ratings

Supply Voltage 7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +3.3V to +5.0V
Operating Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 11) θ_{JA} (°C/W)
TQFP Package 80
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Junction Temperature . . . . . 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

Die Characteristics

Gate Count . . . . . 25,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
11. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 3.3V to 5.0V T_A = -40° to 85°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = 3.5V, CLK Frequency 44MHz (Notes 12, 13)	-	62	79	mA
See previous DC table for remaining DC specifications						

NOTES:
12. Output load 30pF, I_{CCOP} = 5.5 + 4.7(V) + 3.7E - 7 (V)(f); V = Volts, f = Freq. Example: 5.5 + 4.7(5.0) + 3.7E - 7(5.0)(44E6) = 111
13. Not tested, but characterized at initial design and major process/design changes.

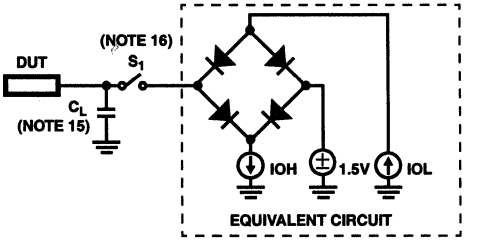
AC Electrical Specifications

V_{CC} = 3.3V to 5.0V, T_A = -40° to 85°, (Note 14)

PARAMETER	SYMBOL	44MHz		UNITS
		MIN	MAX	
CLK Period (MCLK)	t_{CP}	22.5	-	ns
CLK High (MCLK)	t_{CH}	9	-	ns
CLK Low (MCLK)	t_{CL}	9	-	ns
TXCLK, TXRDY, I, Q from MCLK	t_{D2}	-	25	ns
RXCLK, MD_RDY, RXD from MCLK	t_{D3}	-	25	ns
TEST 0-7, CCA, AGC, from MCLK	t_{D4}	-	27	ns
ANSTEL, TEST_CK	-	-	-	-
See previous AC table for remaining AC specifications				

NOTE:
14. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -1mA. Input reference level all inputs 1.5V. Test V_{IH} = Vcc, V_{IL} = 0V; $V_{OH} = V_{OL} = V_{CC}/2$.

Test Circuit



NOTES:
15. Includes Stray and JIG Capacitance
16. Switch S1 Open for I_{CCSB} and I_{CCOP}

FIGURE 22. TEST LOAD CIRCUIT

Waveforms

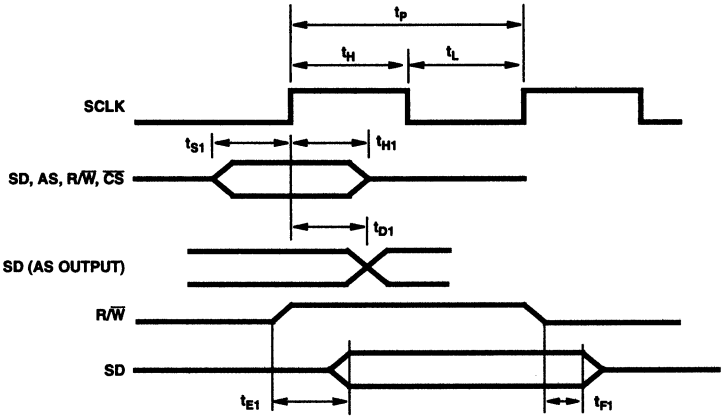


FIGURE 23. SERIAL CONTROL PORT SIGNAL TIMING

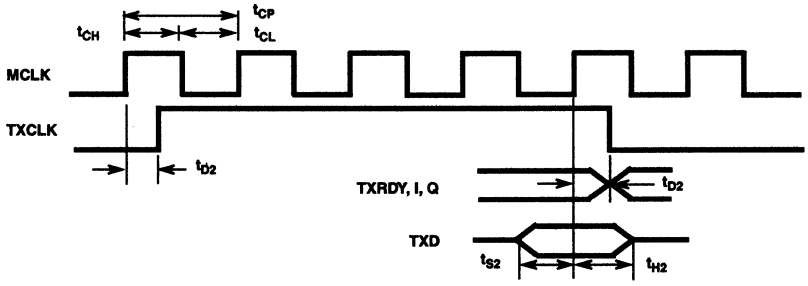
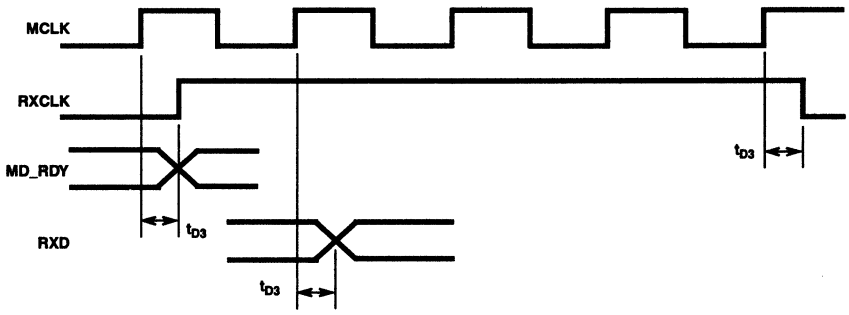


FIGURE 24. TX PORT SIGNAL TIMING



NOTE: RXD is output one MCLK after RXCLK rising to provide data hold time.

FIGURE 25. RX PORT SIGNAL TIMING

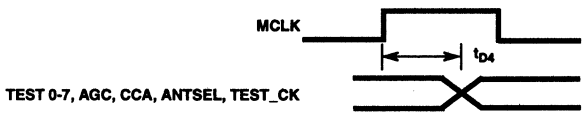


FIGURE 26. MISCELLANEOUS SIGNAL TIMING

HARRIS SEMICONDUCTOR

HFA3925

2.4GHz - 2.5GHz 250mW Power Amplifier

January 1997

Features

- Highly Integrated Power Amplifier with T/R Switch
- Operates Over 2.7V to 6V Supply Voltage
- High Linear Output Power (P_{1dB}: +24dBm)
- Individual Gate Control for Each Amplifier Stage
- Low Cost SSOP-28 Plastic Package

Applications

- Systems Targeting IEEE 802.11 Standard
- TDD Quadrature-Modulated Communication Systems
- Wireless Local Area Networks
- PCMCIA Wireless Transceivers
- ISM Systems
- TDMA Packet Protocol Radios
- PCS/Wireless PBX
- Wireless Local Loop

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA3925IA	-40 to 85	28 Ld SSOP	M28.15
HFA3925IA96	-40 to 85	Tape and Reel	

Description

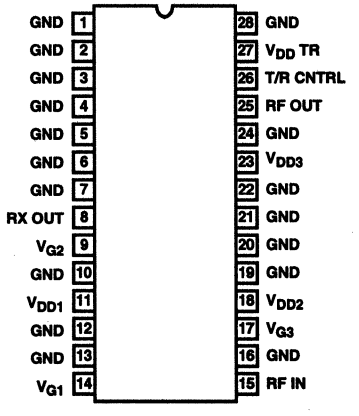
The Harris 2.4GHz PRISM™ chip set is a highly integrated five-chip solution for RF modems employing Direct Sequence Spread Spectrum (DSSS) signaling. The HFA3925 2.4GHz-2.5GHz, 250mW power amplifier is one of the five chips in the PRISM™ chip set (see the Typical Application Diagram).

The Harris HFA3925 is an integrated power amplifier with transmit/receive switch in a low cost SSOP 28 plastic package. The power amplifier delivers +27dB of gain with high efficiency and can be operated with voltages as low as 2.7V. The power amplifier switch is fully monolithic and can be controlled with CMOS logic levels.

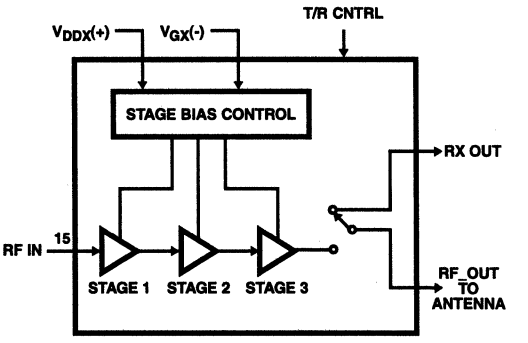
The HFA3925 is ideally suited for QPSK, BPSK or other linearly modulated systems in the 2.4GHz Industrial, Scientific, and Medical (ISM) frequency band. It can also be used in GFSK systems where levels of +25dBm are required. Typical applications include Wireless Local Area Network (WLAN) and wireless portable data collection.

Pinout

HFA3925
(SSOP)
TOP VIEW



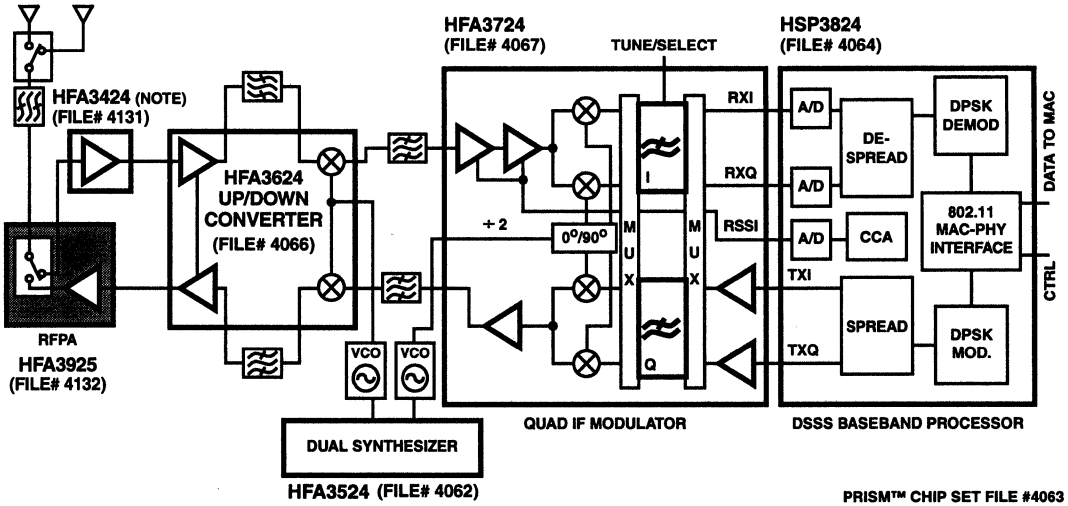
Functional Block Diagram



PRISM™ and the PRISM™ logo are trademarks of Harris Corporation.

File Number 4132.3

Typical Application Diagram



TYPICAL TRANSCEIVER APPLICATION USING THE HFA3925

NOTE: Required for systems targeting 802.11 specifications.

For additional information on the PRISM™ chip set, call (407) 724-7800 to access Harris' AnswerFAX system. When prompted, key in the four-digit document number (File #) of the datasheets you wish to receive.

The four-digit file numbers are shown in the Typical Application Diagram, and correspond to the appropriate circuit.

Absolute Maximum Ratings

Maximum Input Power (Note 2) . . . . . +23dBm
Operating Voltages (Notes 2, 3) . . . . . V_{DD} = 8V, V_{GG} = -8V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
SSOP Package 88
Maximum Storage Temperature Range . . . . . -65°C to 150°C

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = 25°C, Z_0 = 50Ω, V_{DD} = +5V, P_{IN} = -30dBm, f = 2.45GHz, Unless Otherwise Specified

PARAMETER	MIN	TYP	MAX	UNITS
POWER AMPLIFIER				
Linear Gain	27	28	32	dB
VSWR In/Out	-	1.75:1	-	
Input Return Loss	-	-11.3	-	dB
Output Return Loss	-	-11.3	-	dB
Output Power at P_{1dB}	22.5	24.5	-	dBm
Second Harmonic at P_{1dB}	-	-20	0	dBc
Third Harmonic at P_{1dB}	-	-30	-10	dBc
IDD at P1dB (VDD1 + VDD2 + VDD3)	-	270	375	mA

NOTES:

2. Ambient temperature (T_A) = 25°C.
3. $|V_{DD}| + |V_{GG}|$ not to exceed 12V.

Pin Description

PINS	SYMBOL	DESCRIPTION
1	GND	DC and RF Ground.
2	GND	DC and RF Ground.
3	GND	DC and RF Ground.
4	GND	DC and RF Ground.
5	GND	DC and RF Ground.
6	GND	DC and RF Ground.
7	GND	DC and RF Ground.
8	RX OUT	Output of T/R Switch for receive mode.
9	V_{G2}	Negative bias control for the second PA stage, adjusted to set V_{DD2} quiescent bias current, which is typically 53mA. Typical voltage at pin = -0.75V. Input impedance: > 1MΩ.
10	GND	DC and RF Ground.
11	V_{DD1}	Positive bias for the first stage of the PA, 2.7V to 6V.
12	GND	DC and RF Ground.
13	GND	DC and RF Ground.
14	V_{G1}	Negative bias control for the first PA stage, adjusted to set V_{DD1} quiescent bias current, which is typically 20mA. Typical voltage at pin = -0.75V. Input impedance: > 1MΩ.
15	RF IN	RF Input of the Power Amplifier.
16	GND	DC and RF Ground.

Pin Description (Continued)

PINS	SYMBOL	DESCRIPTION
17	V_{G3}	Negative bias control for the third PA stage, adjusted to set V_{DD3} quiescent bias current, which is typically 90mA. Typical voltage at pin = -0.95V. Input impedance: > 1MΩ.
18	V_{DD2}	Positive bias for the second stage of the PA. 2.7V to 6V.
19-22	GND	DC and RF Ground.
23	V_{DD3}	Positive bias for the third stage of the PA. 2.7V to 6V.
24	GND	DC and RF Ground.
25	RF OUT	RF output of T/R switch and power amplifier for transmit mode.
26	T/R CTRL	0V for transmit mode, +5V for receive mode.
27	V_{DD} TR	V_{DD} for T/R switch.
28	GND	DC and RF Ground.

NOTE: Process variation will effect V_{G3} voltage requirement to develop 90mA stage 3 quiescent current, typical range = -0.75V to -1.14V.

Typical Performance Curves

Power Amplifier Small Signal Performance NOTE: All data measured at $T_A = 25^oC$ and V_{G1}, V_{G2} and V_{G3} adjusted for first stage quiescent current of 20mA, second stage current of 53mA and third stage current of 90mA, respectively

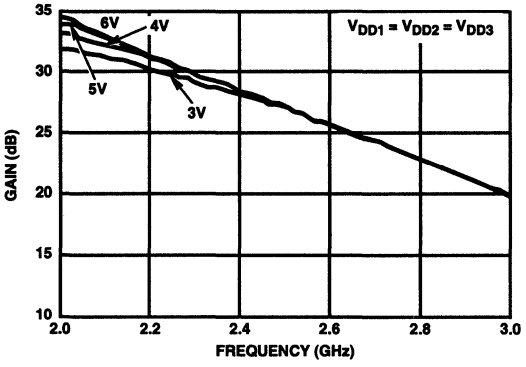


FIGURE 1. LINEAR GAIN

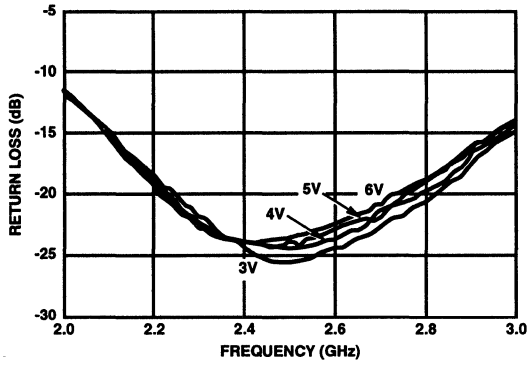


FIGURE 2. INPUT MATCH

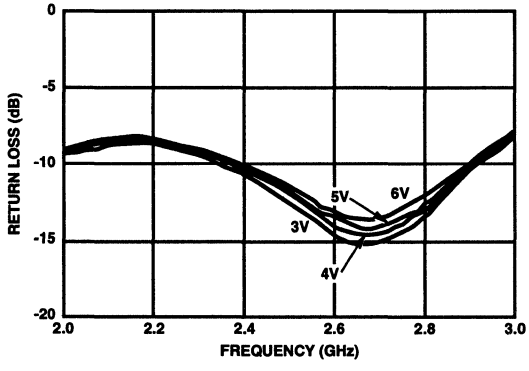


FIGURE 3. OUTPUT MATCH

Power Amplifier CW Performance at Various Supply Voltages NOTE: All data measured at $T_A = 25^oC$ and V_{G1}, V_{G2} and V_{G3} adjusted for first stage quiescent current of 53mA, second stage current of 70mA and third stage current of 90mA, respectively.

Typical Performance Curves (Continued)

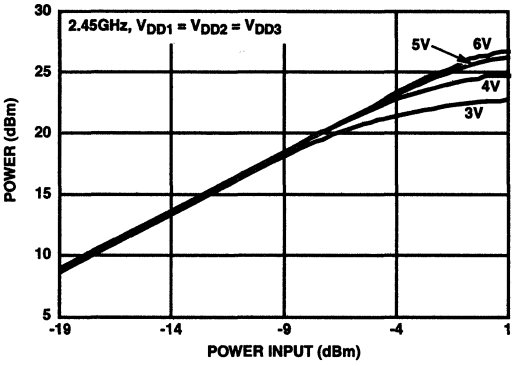


FIGURE 4. POWER OUTPUT

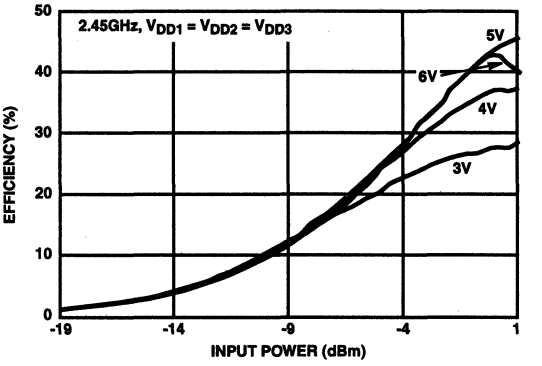


FIGURE 5. POWER ADDED EFFICIENCY

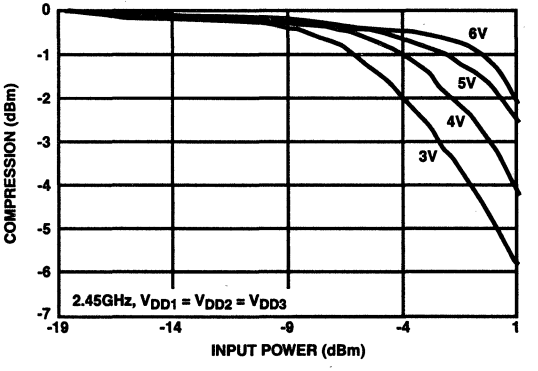


FIGURE 6. GAIN COMPRESSION

Power Amplifier Temperature Performance NOTE: All data measured at $T_A = 25^oC$ and V_{G1}, V_{G2} and V_{G3} adjusted for first stage quiescent current of 20mA, second stage current of 53mA and third stage current of 90mA, respectively.

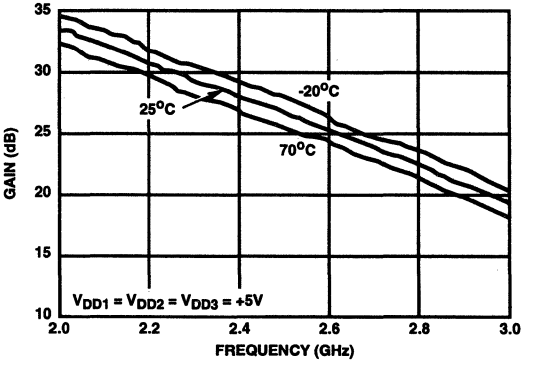


FIGURE 7. LINEAR GAIN

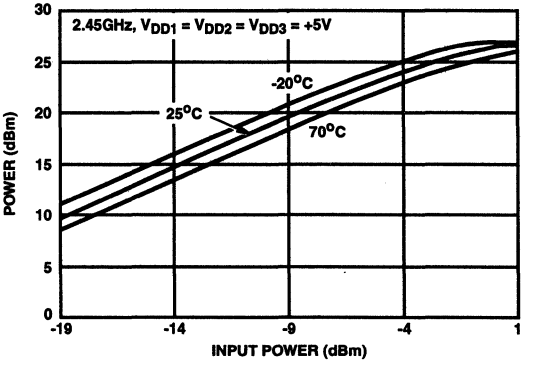


FIGURE 8. POWER OUTPUT

Typical Performance Curves (Continued)

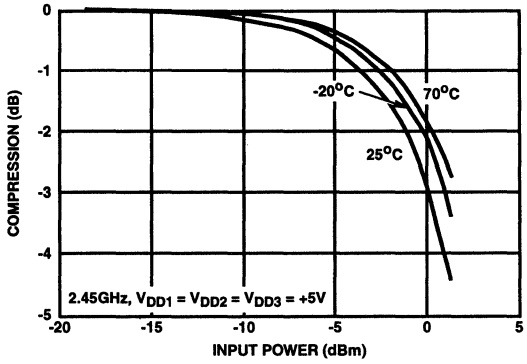


FIGURE 9. GAIN COMPRESSION

Power Amplifier Spurious Response at Various Supply Voltages NOTE: All data measured at $T_A = 25^oC$ and V_{G1}, V_{G2} and V_{G3} adjusted for first stage quiescent current of 20mA, second stage current of 53mA and third stage current of 90mA, respectively.

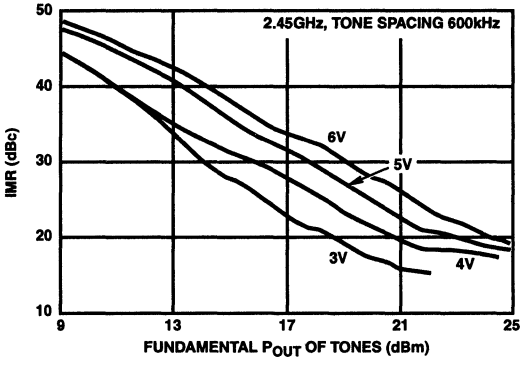


FIGURE 10. THIRD ORDER INTERMODULATION RATIO

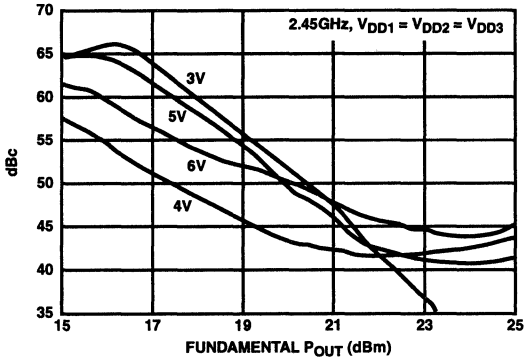


FIGURE 11. SECOND HARMONIC RATIO

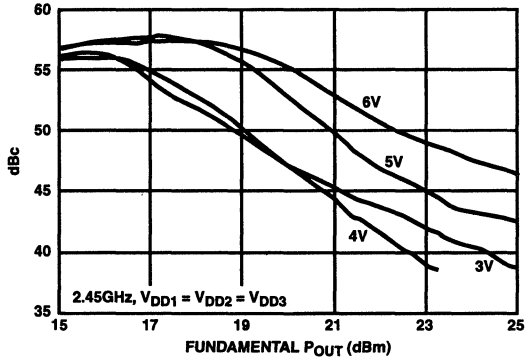


FIGURE 12. THIRD HARMONIC RATIO

Typical Performance Curves (Continued)

Transmit/Receive Switch Performance NOTE: All data measured with V_{DD} TR = +5V, T_A = 25°C.

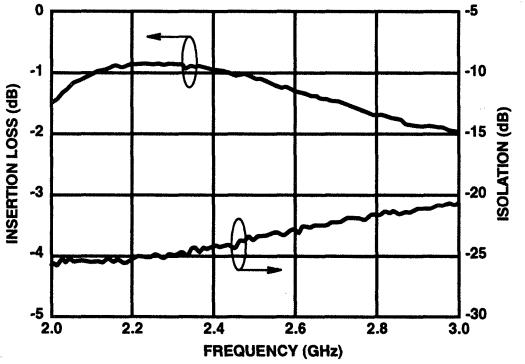


FIGURE 13. RECEIVE MODE T/R INSERTION LOSS/ISOLATION

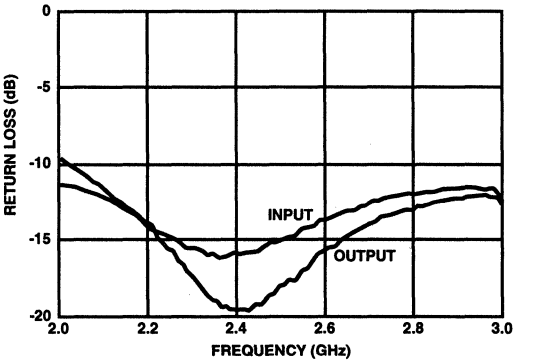
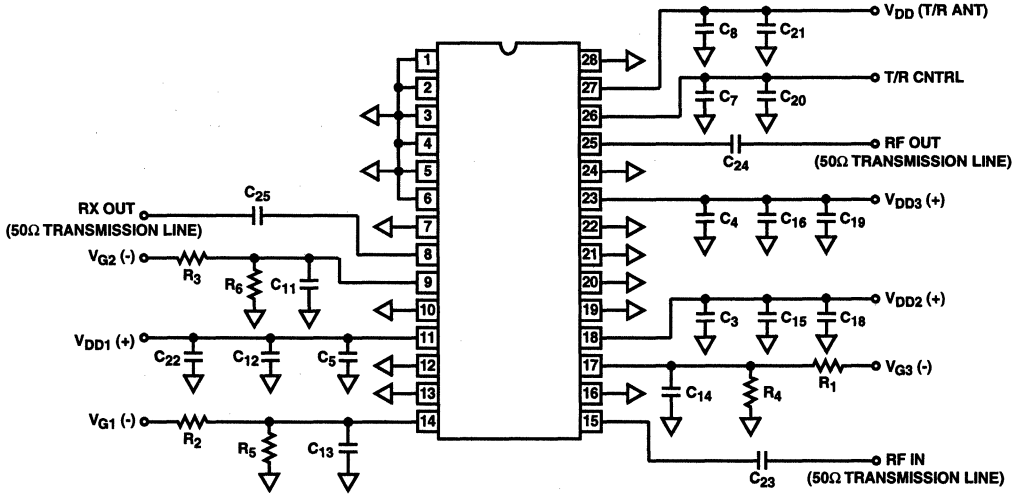


FIGURE 14. RECEIVE MODE T/R SWITCH MATCH

Typical Application Example



EXTERNAL CIRCUITRY PARTS LIST

LABEL	VALUE	PURPOSE
C_3-C_5	22pF	Bypass (GHz)
C_{23}-C_{25}	22pF	DC Block
C_{11}-C_{16}	1000pF	Bypass (MHz)
C_{18}-C_{22}	0.01µF	Bypass (kHz)
R_1, R_6	1.5kΩ	FET Gate Divider Network
R_3, R_5	5kΩ	
R_2	12kΩ	
R_4	1kΩ	

NOTE: All off-chip components are low cost surface mount components obtainable from multiple sources. (0.020in x 0.040in or 0.030in x 0.050in.)

HARRIS SEMICONDUCTOR

PRISM™ Full Duplex Radio Front End

PRELIMINARY

November 1996

For Voice and Data

Features

- Provides Antenna-to-I/Q Baseband Stream
- Low Voltage Operation from 2.7V to 5.5V
- 1.7GHz - 2.7GHz ISM Band Operation
- Single Heterodyne Conversion
- Programmable Antialiasing and Shaping Filters
- 10MHz to 400MHz IF Operation with AGC
- Transmit Variable Gain Range 60dB
- Receive AGC Range 76dB
- Chip Rates to 22M Chip/s
- Power Management Control
- Low Profile PCMCIA-Compatible Surface Mount Packaging

Applications

- Wireless Local Loop Systems
- PCMCIA Wireless Transceivers
- WLAN RF Modems
- TDMA/CDMA Radios
- Part 15 Compliant Radio Links
- Full Duplex Point To Point Transceivers
- PCM Repeater/Transceivers

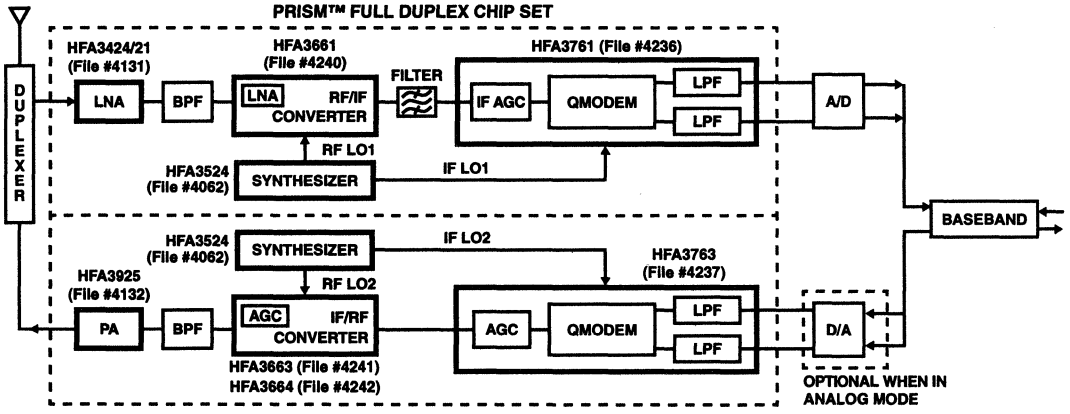
Description

The Harris PRISM™ Full Duplex Radio Front End Chip Set is a highly integrated 7 chip solution for RF modems or transceivers employing quadrature modulation and demodulation. Significant integration of independent transmit and receive functions employ seven ICs. The Receive chain consists of: The HFA3424/21, two high performance, low noise LNA's which cover the 1.7GHz to 2.7GHz range; the HFA3661, a full frequency range combined second LNA/down converter mixer with an LNA bypass mode; the HFA3761, a 10MHz to 400MHz, 82dB IF AGC amplifier with 76dB of dynamic range, integrated with a quadrature demodulator and selectable low pass filters.

The Transmit chain includes: The HFA3763, a 10MHz to 400MHz quadrature modulator integrated with selectable low pass shaping filters and an output stage with a gain control range from 8dB to -35dB; the HFA3663/64 are two IF to RF upconverters integrated with an output RF AGC amplifier with gain control range of 20dB to -10dB; and the HFA3925, a monolithic RF power amplifier. To complete the set, Harris offers a dual synthesizer for RF and IF local oscillator applications, the HFA3524. Each of these functions may be used individually or in any combination of a variety of RF modem applications.

This chip set is intended to support a variety of full duplex radio applications that employ modulation and demodulation architectures requiring highly linear analog processing schemes. Harris also offers a complete line of high speed A/D and D/A converters that can interface with this Full Duplex Chip Set.

Typical Application Diagram



PRISM™ FULL DUPLEX RADIO CHIP SET, FILE #4238

PRISM™ and the PRISM™ logo are trademarks of Harris Corporation.

File Number **4238**

COMMUNICATIONS 4

WIRED COMMUNICATIONS

Wired Communications (Continued)

AN9640 "Glossary of Communication Terms" (32 pages) is not included in this data book, but is available on the net at *http://www.semi.harris.com/appnotes/an9640/* and Harris AnswerFAX (407-724-7800) document # 99640.

ANALOG INTERFACE AT CENTRAL OFFICE SWITCH OR PBX SWITCH END

SLIC SUBSCRIBER LINE INTERFACE CIRCUITS													
PART NUMBER	**HC-5502B/1**	**HC-5504B/1**	**HC-5524**	**HC-5509B**	**HC5509A1R3060**	**HC5513B**	**HC5523**	**HC5526**	**HC5515**	**HC5517**	**HC5519**	**HC5520**	**HC5521**
Status	Released	Released	Released	Released	Released	Released	Released	Released	Released	Released	Sampling	Sampling	Sampling
Replacement for					PBL3764	PBL3764/A		PBL3860 PBL3860A					
Application	PABX	PABX	PABX	Central Office	Central Office Loop Carrier			Central Office Loop Carrier PABX		ISDN Modems Cable Telephony WLL	Central Office Includes Combo	Central Office	Central Office PABX
Longitudinal Balance	58dB	58dB	58dB	58dB	58dB	55dB	58dB	53dB	53dB	58dB	48dB	48dB	48dB
Relay Drivers	Ring	Ring	Ring + 1	Ring + 1	Ring + 1	Ring	Ring	Ring	Ring	1	Ring + 2	Ring + 2	Ring + 2
Ringing Schemes	Ext.	Ext.	Ext.	Ext.	Ext.	Ext.	Ext.	Ext.	Ext.	Ext.	Ext.	Ext.	Ext.
High, Low Voltage Op.			X			X	X	X	X	X			
Constant Voltage Feed	X	X	X	X	X					X	X	X	X
Constant Current Feed			X	X	X	X	X	X	X				
Programmable Feed			X	X	X	X	X	X	X	X			
Loop Current (mA)	30	40	20 to 60	20 to 60	20 to 60	20 to 60	20 to 60	20 to 60	20 to 60	20 to 60	30	30	30
Rloop 20mA at 48V	1400	1400	1800	1800	1800	2000	2000	2000	2000	Short Loop	1710	1710	1710
Thermal Management											X	X	X
Tip and Ring Open			X	X	X	X	X	X	X	X	X	X	X
Loop Current Detector	X	X	X	X	X	X	X	X	X	X	X	X	X
Ground Key Detector	X	X	X	X	X	X	X	X					
Ring Trip Detector	X	X	X	X	X	X	X	X	X	X	X	X	X
Zero Crossing Detection											X	X	X
Thermal Shutdown			X	X	X	X	X	X	X	X	X	X	X
Thermal Shutdown Detector			X	X	X					X	X	X	X
On Hook Transmission	X	X	X	X	X	X	X	X	X	X	X	X	X
Saturation Guard	X	X	X	X	X	X	X	X	X	X	X	X	X
On-Chip Transhybrid Bal.											X		
-40°C to 85°C	X	X	X	X		X	X	X	X	X			
Standard Packages	PDIP	PDIP	PDIP	PDIP	PLCC	PDIP	PDIP	PDIP	PDIP	PLCC	MQFP	MQFP	MQFP
	PLCC	PLCC	PLCC	PLCC		PLCC	PLCC	PLCC	PLCC	SO		PLCC	PLCC
	SO	SO	SO	SO									
AnswerFAX Doc#	2884/4127	2886/4125	2798	2799	3675	3963	4144	4151	4235	4147	4232	4148	4265

ANALOG INTERFACE AT CENTRAL OFFICE SWITCH OR PBX SWITCH END

CMOS CODECs
COMPLEMENTARY METAL-OXIDE SEMICONDUCTOR

PART NUMBER	FEATURES	CLOCK RATES	SUPPLY VOLTAGE	PACKAGE
NON-LINEAR ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTER FOR VOICE AND PCM (PULSE CODE MODULATION) SIGNALS				
CD22354A (μ-Law) CD22357A (A-Law)	• Meets or Exceeds All AT&T D3/D4 Specs CCITT Recommendations • Complete CODEC and Filtering Systems - No External Components for Sample-and-Hold and Auto-Zero - Receive Output Filter with SIN X/X Correction and Additional 8kHz Suppression • Variable Data Clocks - From 64kHz to 2.1MHz • Synchronous and Asynchronous Operation • TTL or CMOS Compatible Logic • ESD Protection on All Inputs and Outputs • Adjustable Gain for Transmit Input	64kHz to 2.1MHz	±5V ±5% at 90mW (Max)	16 Lead DIP (E)

CROSSPOINT SWITCHES

TYPE	FEATURES	CONFIGURATION	R_{ON} TYP at 12V	Δ R_{ON} TYP at 12V	FREQ. RESPONSE TYP -3dB 14V	CROSSTALK TYP -40dB 14V	SUPPLY VOLTAGE	PACKAGE
BIMOS-E CROSSPOINT SWITCHES WITH CONTROL INPUT MEMORY								
CD22M3493 CD22M3494	• Independent Address Latches • Manual and Automatic Power-On Resets • Crosstalk: -90dB (Min) at 10kHz • Parallel Input Addressing • HC/HCT Ground-Referenced Inputs Available • 2kV Minimum ESD Protection • Latch-Up Current: 50mA Min • Pin and Functionally Compatible with the SGS M3493/M3494 and Mitel MT8812/MT8816	12 x 8 x 1 16 x 8 x 1	36Ω	6Ω	45MHz	3MHz	4V to 16V CD22M3493 4V to 15V CD22M3494	40 Lead DIP (E) 44 Lead PLCC (N)
CMOS CROSSPOINT SWITCHES WITH CONTROL MEMORY								
CD22100	• "Built-In" Control Latches • Large Analog Signal Capability $\pm V_{DD}/2$ • 10MHz Switch Bandwidth • High Linearity - 0.5% Distortion Typ at f = 1kHz, $V_{IN} = 5V_{P-P}$, $V_{DD} = 10V$, and $R_L = 1k\Omega$ • Standard CMOS Noise Immunity • 100% Tested for Maximum Quiescent Current at 20V	4 x 4 x 1	75Ω	18Ω	40MHz	1.5MHz	3V to 18V	16 Lead DIP (E or F)

CROSSPOINT SWITCHES (Continued)								
TYPE	FEATURES	CONFIGURATION	R_{ON} TYP at 12V	Δ R_{ON} TYP at 12V	FREQ. RESPONSE TYP -3dB 14V	CROSSTALK TYP -40dB 14V	SUPPLY VOLTAGE	PACKAGE
CD22101	• Strobed Control Input • "Built-In" Latched Inputs • Large Analog Signal Capability $\pm V_{DD}/2$ • 10MHz Switch Bandwidth • High Linearity - 0.25% Distortion Typ at f = 1kHz, $V_{IN} = 5V_{P-P}$, $V_{DD} - V_{SS} = 10V$, and $R_L = 1k\Omega$ • Standard CMOS Noise Immunity	4 x 4 x 2	75Ω	8Ω	40MHz	2.5MHz	3V to 18V	24 Lead DIP (E or F)
CD22102	• Same as CD22101, but has Set/Reset Flip-Flop Control Input Instead of Strobed Control Input	4 x 4 x 2	75Ω	8Ω	40MHz	2.5MHz	3V to 18V	24 Lead DIP (E or F)
CD54/74HC(T) 22106	• 64 Analog Switches in an 8 x 8 x 1 Array • On-Chip Line Decoder and Control Latches • Automatic Power-Up Reset by Using a 0.1μF Capacitor at the MR Pin • R_{ON} Resistance 95Ω Max at $V_{CC} = 4.5V$ • Analog Signal Capability $V_{DD}/2$	8 x 8 x 1	64Ω	25Ω	6MHz	7MHz	2V to 10V	28 Lead DIP (E)

NOTE: High Performance Analog Switches Matrix for PBX, Studio, Audio Switching, and Multisystem Bus Interconnects.

ANALOG INTERFACE AT SUBSCRIBER END

CMOS DTMF RECEIVERS				
TYPE	FEATURES	OUTPUT 3-STATE OUTPUT CODE	SUPPLY VOLTAGE	PACKAGE
CD22202	• Detects Either 12 or 16 Standard DTMF Signals • Central-Office Quality • No Front-End Band Splitting Filters Required • Single, Low-Tolerance, 5V Supply • Uses Inexpensive 3.579545MHz Crystal for Reference • Excellent Speech Immunity • Synchronous or Handshake Interface • Three-State Outputs	4-Bit Hexadecimal or Binary Coded 2-of-8	5V ±10%	18 Lead DIP (E)
CD22203	• Same as CD22202, but also has Early Detect Output	4-Bit Hexadecimal or Binary Coded 2-of-8	5V ±10%	18 Lead DIP (E)

ANALOG INTERFACE AT SUBSCRIBER END

CMOS DTMF RECEIVERS

TYPE	FEATURES	OUTPUT 3-STATE OUTPUT CODE	SUPPLY VOLTAGE	PACKAGE
CD22204	• No Front-End Band Splitting Filters Required • Single, Low-Tolerance, 5V Supply • Three-State Outputs for Microprocessor-Based Systems • Detects all 16 Standard DTMF Digits • Uses Inexpensive 3.579545MHz Crystal for Reference • Excellent Speech Immunity • Outputs in 4-Bit Hexadecimal Code	4-Bit Hexadecimal Only	5V ±10%	14 Lead DIP (E) 24 SOIC (M)

CMOS DTMF TRANSMITTERS

TYPE	FEATURES	OUTPUT (MIN)	SUPPLY VOLTAGE	PACKAGE
CD22859	• Mute Drivers on Chip • Device Power Can Either be Regulated DC or Phone Loop Current • Use of an Inexpensive 3.579545MHz TV Crystal Provides High Accuracy and Stability for All Frequencies	350mV into 82Ω	2.5V to 10V	16 Lead DIP (E)

NOTE: Detects and Generates Special Tones for Standard Telephone Touch Tone Dialing Keypad.

DIGITAL INTERFACE

PCM LINE REPEATERS

TYPE	FEATURES	OUTPUT	SUPPLY VOLTAGE	PACKAGE
BIPOLAR				
CD22301	• Automatic Line Buildout • For T1 1.544Mbits/s Bipolar Carrier System • For T148 2.37Mbits/s Ternary Carrier System • For CCITT 2.048Mbits/s Bipolar Carrier System	Buffered	5.1V ±5%, 30mA Max	18 Lead DIP (E)

NOTE: Digital to Digital Converter to Bolster and Reshape Digital PCM Signals Distorted by Long Transmission Over PCM Bus Lines.

PCM TRANSCODERS

TYPE	FEATURES	OUTPUT	CODES	SUPPLY VOLTAGE	PACKAGE
HC-5560	• Mode Selectable Coding • North American and European Compatibility • Simultaneous Encoding and Decoding • Asynchronous Operation • Loop-Back Control • Transmission Error Detection • Alarm Indication Signal • Replaces MJ1440, MJ1471, and TCM2201 Transcoders	3.2mA at 0.4V	AMI (T1 and T1C) B6ZS (T2) B8ZS (T1) HDB3 (PCM30)	5V at 10mA Typ	20 Lead DIP (E)
CD22103A	• Simultaneous Encoding and Decoding • HDB3 Coding and Decoding for Data Rates from 50kbits/s to 10Mbits/s in a Manner Consistent with CCITT G703 Recommendations • HDB3/AMI Transmission Coding/Reception Decoding with Code Error Detection is Performed in Independent Coder and Decoder Sections • All Transmitter and Receiver Inputs/Outputs are TTL Compatible • Internal Loop Test Capability	1.6mA at 0.5V	HDB3/AMI per CCITT G703 Annex Recommendation	5V ±10% at 100mA Max	16 Lead DIP (E)

NOTE: Unipolar to Bipolar Digital to Digital Converter for More Efficient Long Line Transmission of digital PCM signals.

GENERAL INTERFACE

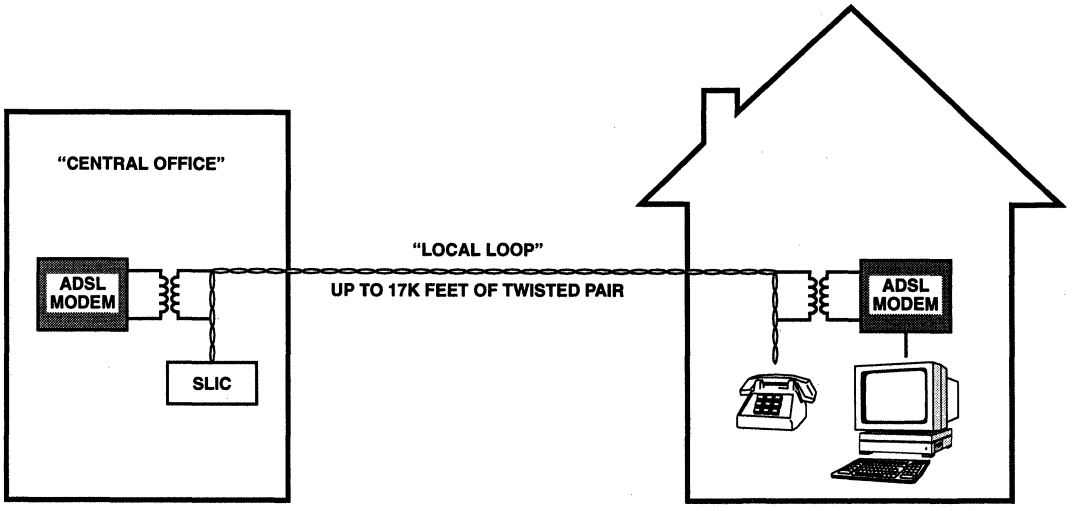
CVSD
CONTINUOUS VARIABLE SLOPE DELTA MODULATOR

TYPE	FEATURES	CLOCK RATES	SUPPLY VOLTAGE	PACKAGE
HC-55564	• Modulator/Demodulator Functions • All Digital • Requires Few External Parts • Low Power Drain: 1.5mW Typical from Single 3V - 7V Supply • Time Constants Determined by Clock Frequency; No Calibration or Drift Problems; Automatic Offset Adjustment • Half Duplex Operation Under Digital Control • Filter Reset Under Digital Control • Automatic Overload Recovery • Automatic "Quiet" Pattern Generation • AGC Control Signal Available	9kHz to 64kHz	3.3V to 6V at 1.5mA Max	16 Lead SOIC (M) 14 Lead DIP (E and F)

NOTE: A Real Time Voice to Digital (Encoder) and Digital to Voice (Decoder) Converter.

Digital Subscriber Line

ADSL APPLICATION



- **ADSL (Asymmetrical Digital Subscriber Line) Provides POTS and High Speed Data on ONE Existing Line**
- **Does NOT Tie Up a Switched Circuit at Central Office**
- **Data Rates to 8Mbits (Downstream) and to 256kbits (Upstream)**

HARRIS SEMICONDUCTOR

HC6094

ADVANCE INFORMATION

January 1997

ADSL Analog Front End Chip

Features

- 14-Bit DAC
- Programmable Gain Stages
  - 48dB Programmable Gain on Receive Channel
  - 12dB Programmable Gain on Transmit Channel
- Precision Laser Tuned Onboard Anti-Aliasing and Reconstruction Filters
- High Impedance MOS Inputs on Receive Channel
- Transmit Channel Output Capable of Driving 200Ω Load at up to $12V_{P-P}$

Applications

- DMT/CAPS ADSL
- High Resolution Communications Applications Requiring up to 1MHz Bandwidth

Description

The AFE chip performs the Analog processing for the ADSL chip set. The transmitter side has a 14-bit DAC as well as reconstruction filters and a programmable gain stage. The receiver side has programmable gain stages and anti-aliasing filters for driving the off chip A/D.

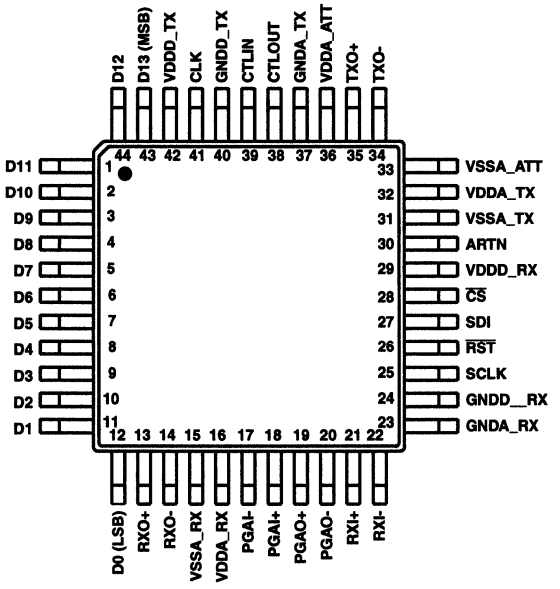
The DAC and the filters are laser trimmed to ensure accuracy.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC6094IN	-40 to 85	44 Ld MQFP	Q44.10x10

Pinout

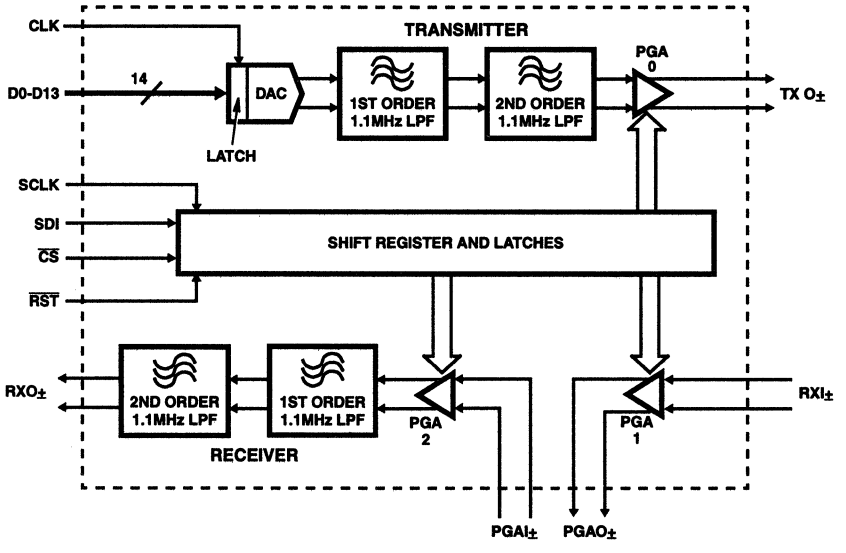
HC6094
(MQFP)
TOP VIEW



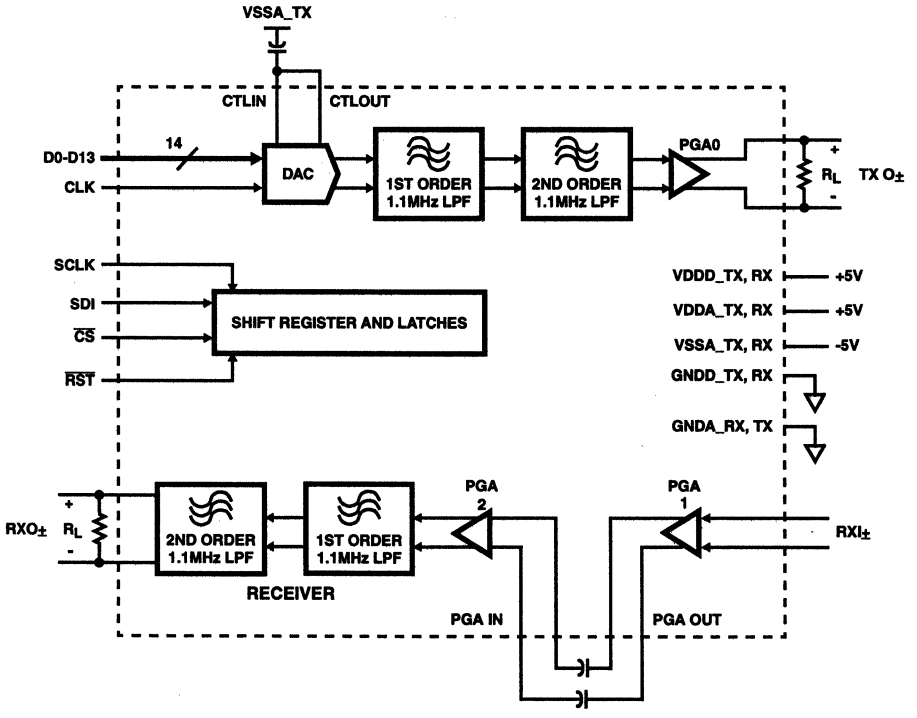
4 WIRED COMMUNICATIONS

File Number **4260**

Functional Block Diagram



Typical Setup



HARRIS SEMICONDUCTOR

HI5905

ADVANCE INFORMATION

January 1997

14-Bit, 5 MSPS A/D Converter

Features

- 5 MSPS Sampling Rate
- Low Power 350mW at 5 MSPS
- Internal Sample and Hold
- Fully Differential Architecture
- 100MHz Full Power Input Bandwidth
- Typical SINAD >70dB at 1MHz
- Low Latency
- Internal Voltage Reference
- TTL Compatible Clock Input
- CMOS Compatible Digital Data Outputs

Applications

- Asymmetric Digital Subscriber Line (ADSL)
- Digital Communication Systems
- Undersampling Digital IF
- Document Scanners
- Reference Literature
  - AN9214 Using Harris High Speed A/D Converters

Description

The HI5905 is a monolithic, 14-bit, Analog-to-Digital Converter fabricated in Harris' HBC10 BiCMOS process. It is designed for high speed, high resolution applications where wide bandwidth, low power consumption and excellent SINAD performance are essential. With a 100MHz full power input bandwidth the converter is ideal for many types of communication systems and document scanner applications.

The HI5905 is designed in a fully differential pipelined architecture with a front end differential-in-differential-out sample-and-hold (S/H). The HI5905 has excellent dynamic performance while consuming 350mW power at 5 MSPS.

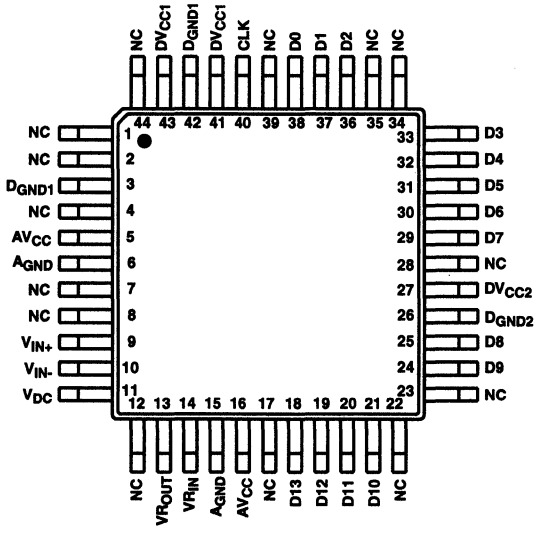
Data output latches are provided which present valid data to the output bus with a latency of 4 clock cycles. The digital data outputs have a separate supply pin which can be powered from a 5.0V supply.

Ordering Information

PART NUMBER	SAMPLE RATE	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5905BIB	5 MSPS	-40 to 85	44 Ld MQFP	Q44.10x10

Pinout

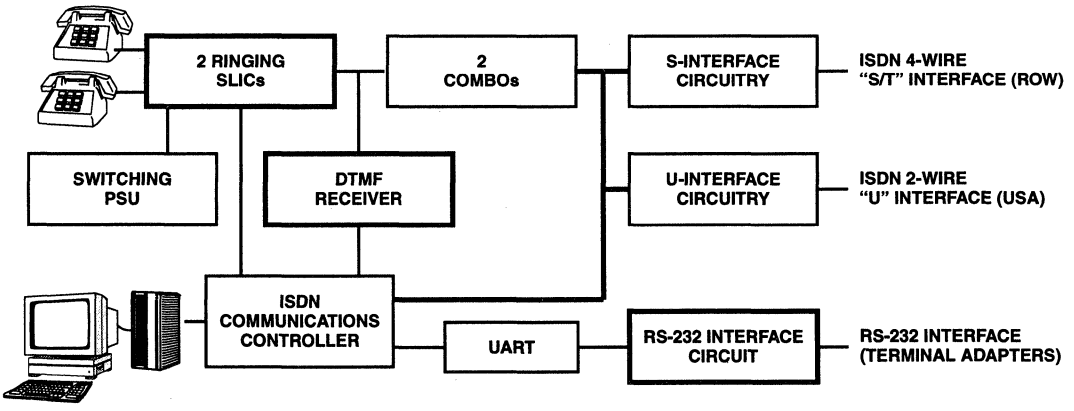
HI5905 (MQFP)
TOP VIEW



4 WIRED COMMUNICATIONS

File Number 4259

ISDN MODEM/TERMINAL ADAPTER



	USA	ROW
SLICs	HC5517	HC5517
COMBOs	CD22354A	CD22357A
MOSFETs	IRF9110	IRF9110
Interface	HIN207	HIN207
DTMF Receiver	CD22204	CD22204

HARRIS SEMICONDUCTOR

HC5517

Ringing SLIC Subscriber Line Interface Circuit

January 1997

Features

- Thru-SLIC Open Circuit Ringing Voltage up to $77V_{PEAK}/54V_{RMS}$, 3 REN Capability at $44V_{RMS}$
- Sinusoidal Ringing Capability
- DI Process Provides Substrate Latch Up Immunity when Driving Inductive Ringers
- Adjustable On-Hook Voltage for Fax and Answering Machine Compatibility
- Resistive and Complex Impedance Matching
- Programmable Loop Current Limit
- Switch Hook and Adjustable Ring Trip Detection
- Pulse Metering Capability
- Single Low Voltage Positive Supply (+5V)

Applications

- Solid State Line Interface Circuit for Wireless Local Loop, Hybrid Fiber Coax, Set Top Box, Voice/Data Modems
- Related Literature
  - AN9606, Operation of the HC5517 Evaluation Board
  - AN9607, Impedance Matching Design Equations
  - AN9628, AC Voltage Gain
  - AN9608, Implementing Pulse Metering
  - AN9636, Implementing an Analog Port for ISDN Using the HC5517
  - AN549, The HC-5502S/4X Telephone Subscriber Line Interface Circuits (SLIC)

Description

The HC5517 is a ringing SLIC designed to accommodate a wide variety of local loop applications. The various applications include, basic POTS lines with answering machines and fax capabilities, ISDN networks, wireless local loop, and hybrid fiber coax (HFC) terminals. The HC5517 provides a high degree of flexibility with open circuit tip to ring DC voltages, user defined ringing waveforms (sinusoidal to square wave), ring trip detection thresholds and loop current limits that can be tailored for many applications. Additional features of the HC5517 are complex impedance matching, pulse metering and transhybrid balance. The HC5517 is designed for use in systems where a separate ring generator is not economically feasible.

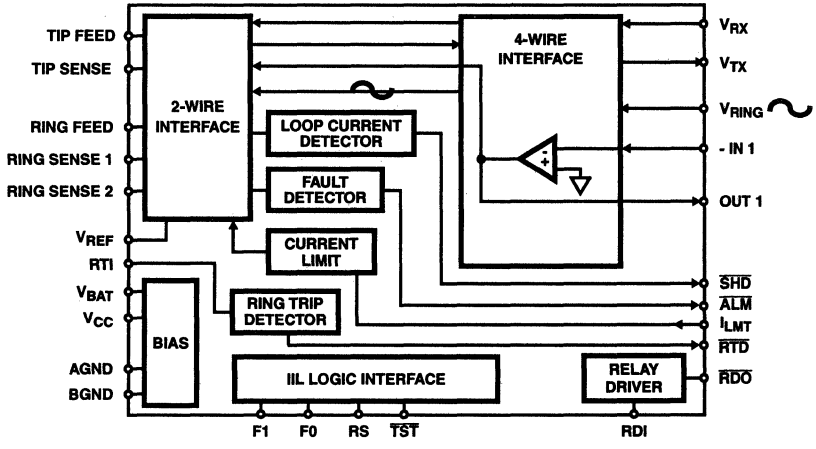
The device is manufactured in a high voltage Dielectric Isolation (DI) process with an operating voltage range from -16V, for off-hook operation and -80V for ring signal injection. The DI process provides substrate latch up immunity, resulting in a robust system design. Together with a secondary protection diode bridge and "feed" resistors, the device will withstand 1000V lightning induced surges, in a plastic package.

A thermal shutdown with an alarm output and line fault protection are also included for operation in harsh environments.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC5517IM	-40 to 85	28 Ld PLCC	N28.45
HC5517CM	0 to 75	28 Ld PLCC	N28.45
HC5517IB	-40 to 85	28 SOIC	M28.3
HC5517CB	0 to 75	28 SOIC	M28.3

Block Diagram



4 WIRED COMMUNICATIONS

File Number 4147

Absolute Maximum Ratings $T_A = 25^oC$

Maximum Supply Voltages
- (V_{CC}) ..... -0.5V to +7V
- (V_{CC})-(V_{BAT}) 90V

Relay Drivers ..... -0.5V to +15V

Operating Conditions

Operating Temperature Range
- HC5517IM, HC5517IB ..... -40^oC to 85^oC
- HC5517CM, HC5517CB ..... 0^oC to 75^oC

Relay Drivers ..... +5V to +12V
Positive Power Supply (V_{CC}) ..... +5V ±5%
Negative Power Supply (V_{BAT}) ..... -16V to -80V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PLCC	67
SOIC	70

Maximum Junction Temperature Plastic ..... 150^oC
Maximum Storage Temperature Range ..... -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) ..... 300^oC
(SOIC, PLCC - Lead Tips Only)

Die Characteristics

Transistor Count 224
Diode Count 28
Die Dimensions ..... 174 x 120
Substrate Potential ..... V_{BAT}
Process ..... Bipolar-DI
ESD (Human Body Model) 500V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. All grounds (AGND, BGND) must be applied before V_{CC} or V_{BAT}. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Electrical Specifications

Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are over Operating Temperature Range, V_{BAT} = -24V, V_{CC} = +5V, AGND = BGND = 0V. All AC Parameters are specified at 600Ω 2-Wire terminating impedance.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RINGING TRANSMISSION PARAMETERS					
V_{RING} Input Impedance	(Note 3)	-	5.4	-	kΩ
4-Wire to 2-Wire Gain	V_{RING} to Vt-r (Note 3)	-	40	-	V/V
AC TRANSMISSION PARAMETERS					
RX Input Impedance	300Hz to 3.4kHz (Note 3)	-	108	-	kΩ
TX Output Impedance	300Hz to 3.4kHz (Note 3)	-	-	20	Ω
4-Wire Input Overload Level	300Hz to 3.4kHz R_L = 1200Ω, 600Ω Reference (Note 3)	+1.0	-	-	V_{PEAK}
2-Wire Return Loss	Matched for 600Ω (Note 3)				
SRL LO		26	35	-	dB
ERL		30	40	-	dB
SRL HI		30	40	-	dB
2-Wire Longitudinal to Metallic Balance Off Hook	Per ANSI/IEEE STD 455-1976 (Note 3) 300Hz to 3400Hz	58	63	-	dB
4-Wire Longitudinal Balance Off Hook	300Hz to 3400Hz (Note 3)	50	55	-	dB
Low Frequency Longitudinal Balance	I_{LINE} = 40mA $T_A = 25^oC$ (Note 3)	-	10	23	dBrnC
Longitudinal Current Capability	I_{LINE} = 40mA $T_A = 25^oC$ (Note 3)	-	-	40	mA_{RMS}
Insertion Loss	0dBm at 1kHz, Referenced 600Ω				
2-Wire/4-Wire (Includes external transhybrid amplifier with a gain of 3)		-	±0.05	±0.2	dB
4-Wire/2-Wire		-	±0.05	±0.2	dB
4-Wire/4-Wire (Includes external transhybrid amplifier with a gain of 3)		-	-	±0.25	dB

Electrical Specifications Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are over Operating Temperature Range, $V_{BAT} = -24V$, $V_{CC} = +5V$, AGND = BGND = 0V. All AC Parameters are specified at 600Ω 2-Wire terminating impedance. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Response	300Hz to 3400Hz (Note 3) Referenced to Absolute Level at 1kHz, 0dBm Referenced 600Ω	-	±0.02	±0.06	dB
Level Linearity	Referenced to -10dBm (Note 3)				
2-Wire to 4-Wire and 4-Wire to 2-Wire	+3 to -40dBm	-	-	±0.08	dB
	-40 to -50dBm	-	-	±0.12	dB
	-50 to -55dBm	-	-	±0.3	dB
Absolute Delay	(Note 3)				
2-Wire/4-Wire	300Hz to 3400Hz	-	-	1.0	µs
4-Wire/2-Wire	300Hz to 3400Hz	-	-	1.0	µs
4-Wire/4-Wire	300Hz to 3400Hz	-	0.95	1.5	µs
Transhybrid Loss	$V_{IN} = 1V_{P-P}$ at 1kH (Notes 3, 4)	30	40		dB
Total Harmonic Distortion 2-Wire/4-Wire, 4-Wire/2-Wire, 4-Wire/4-Wire	Reference Level 0dBm at 600Ω 300Hz to 3400Hz (Note 3)	-	-	-50	dB
Idle Channel Noise 2-Wire and 4-Wire	(Note 3) C-Message	-	3	-	dBrnC
	Psophometric (Note 3)	-	-87	-	dBmp
Power Supply Rejection Ratio	(Note 3)				
V_{CC} to 2-Wire	30Hz to 200Hz, R_L = 600Ω	20	40	-	dB
V_{CC} to 4-Wire		20	40	-	dB
V_{BAT} to 2-Wire		20	40	-	dB
V_{BAT} to 4-Wire		20	50	-	dB
V_{CC} to 2-Wire	(Note 3) 200Hz to 16kHz, R_L = 600Ω	30	40	-	dB
V_{CC} to 4-Wire		20	28	-	dB
V_{BAT} to 2-Wire		20	50	-	dB
V_{BAT} to 4-Wire		20	50	-	dB
DC PARAMETERS					
Loop Current Programming Limit Range		20 (Note 5)	-	60	mA
Accuracy		10	-	-	%
Loop Current During Power Denial	R_L = 200Ω	-	±4	±7	mA
Fault Currents					
TIP to Ground (Note 3)		-	30	-	mA
RING to Ground		-	120	-	mA
TIP and RING to Ground (Note 3)		-	150	-	mA
Switch Hook Detection Threshold		-	12	15	mA
Ring Trip Comparator Threshold		7.2	-	25	mA
Thermal $\overline{\text{ALARM}}$ Output (Note 3)	Safe Operating Die Temperature Exceeded	140	-	160	°C

Electrical Specifications Unless Otherwise Specified, Typical Parameters are at T_A = 25°C, Min-Max Parameters are over Operating Temperature Range, V_{BAT} = -24V, V_{CC} = +5V, AGND = BGND = 0V. All AC Parameters are specified at 600Ω 2-Wire terminating impedance. **(Continued)**

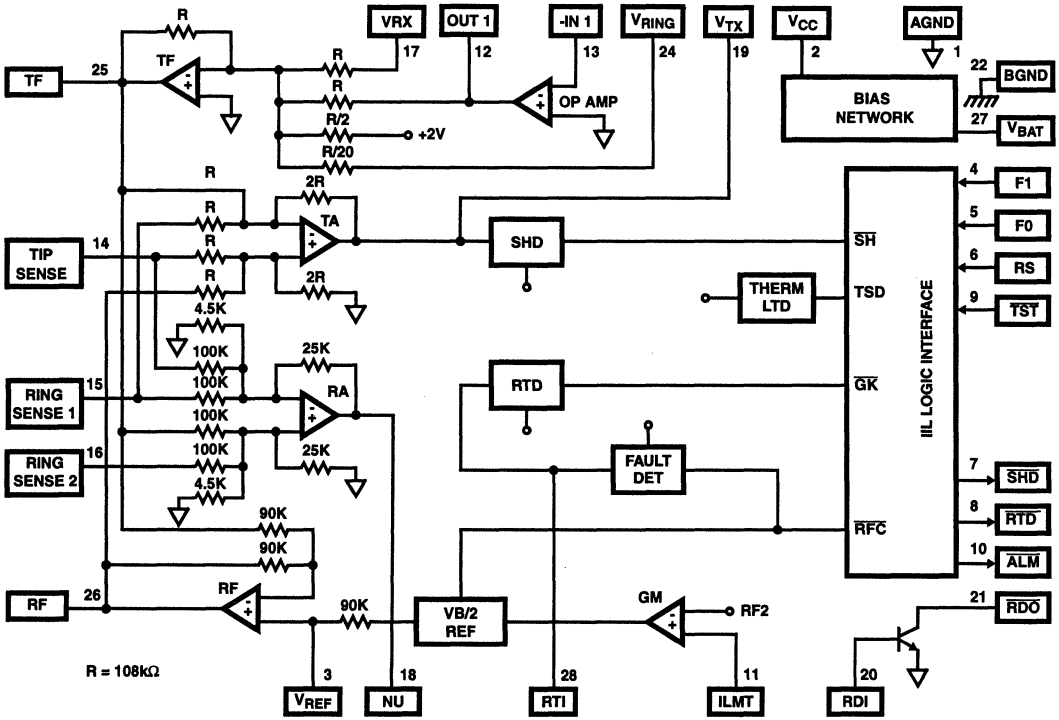
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Dial Pulse Distortion (Note 3)		-	0.1	0.5	ms
Uncommitted Relay Driver					
On Voltage V_{OL}	I_{OL} ($\overline{RDO}$) = 30mA	-	0.2	0.5	V
Off Leakage Current		-	±10	±100	µA
TTL/CMOS Logic Inputs (F0, F1, RS, $\overline{TST}$, RDI)					
Logic '0' V_{IL}		0	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Input Current (F0, F1, RS, $\overline{TST}$, RDI)	IIH, 0V ≤ V_{IN} ≤ 5V	-	-	-1	µA
Input Current (F0, F1, RS, $\overline{TST}$, RDI)	IIL, 0V ≤ V_{IN} ≤ 5V	-	-	-100	µA
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} = 800µA	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} = 40µA	2.7	-	-	V
Power Dissipation On Hook	V_{CC} = +5V, V_{BAT} = -80V, R_{LOOP} = ∞	-	300	-	mW
	V_{CC} = +5V, V_{BAT} = -48V, R_{LOOP} = ∞	-	150	-	mW
Power Dissipation Off Hook	V_{CC} = +5V, V_{BAT} = -24V, R_{LOOP} = 600Ω, I_L = 25mA	-	280	-	mW
I_{CC}	V_{CC} = +5V, V_{BAT} = -80V, R_{LOOP} = ∞	-	3	6	mA
	V_{CC} = +5V, V_{BAT} = -48V, R_{LOOP} = ∞	-	2	5	mA
	V_{CC} = +5V, V_{BAT} = -24V, R_{LOOP} = ∞	-	1.9	4	mA
I_{BAT}	V_{CC} = +5V, V_{B-} = -80V, R_{LOOP} = ∞	-7	-3.6	-	mA
	V_{CC} = +5V, V_{B-} = -48V, R_{LOOP} = ∞	-5	-2.6	-	mA
	V_{CC} = +5V, V_{B-} = -24V, R_{LOOP} = ∞	-4	-1.8	-	mA
UNCOMMITTED OP AMP PARAMETERS					
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Differential Input Resistance (Note 3)		-	1	-	MΩ
Output Voltage Swing (Note 3)	R_L = 10kΩ	-	±3	-	V_{P-P}
Small Signal GBW (Note 3)		-	1	-	MHz

NOTES:

3. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.
4. For transhybrid circuit as shown in Figure 10.
5. Application limitation based on maximum switch hook detect limit and metallic currents. Not a part limitation.

Functional Diagram

PLCC/SOIC



HC5517 TRUTH TABLE

F1	F0	ACTION
0	0	Loop power Denial Active
0	1	Power Down Latch RESET
0	1	Power on RESET
1	0	$\overline{RD}$ Active
1	1	Normal Loop feed

Over Voltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or $30mA_{RMS}$, $15mA_{RMS}$ per leg, without any performance degradation

TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic)	PEAK
50/60Hz Current T/GND R/GND	 11 Cycles Limited to $10A_{RMS}$	700 (Plastic)	V_{RMS}

Circuit Operation and Design Information

The HC5517 is a voltage feed current sense Subscriber Line Interface Circuit (SLIC). This means that for long loop applications the SLIC provides a constant voltage to the tip and ring terminals while sensing the tip to ring current. For short loops, where the loop current limit is exceeded, the tip to ring voltage decreases as a function of loop resistance.

The following discussion separates the SLIC's operation into its DC and AC path, then follows up with additional circuit design and application information.

DC Operation of Tip and Ring Amplifiers

SLIC in the Active Mode

The tip and ring amplifiers are voltage feedback op amps that are connected to generate a differential output (e.g. if tip sources 20mA then ring sinks 20mA). Figure 1 shows the connection of the tip and ring amplifiers. The tip DC voltage is set by an internal +2V reference, resulting in -4V at the output. The ring DC voltage is set by the tip DC output voltage and an internal $V_{BAT}/2$ reference, resulting in V_{BAT} +4V at the output. (See Equation 1, Equation 2 and Equation 3.)

$$V_{TIPFEED} = V_C = -2V\left(\frac{R}{R/2}\right) = -4V \quad \text{(EQ. 1)}$$

$$V_{RINGFEED} = V_D = \frac{V_{BAT}}{2}\left(1+\frac{R}{R}\right) - V_{TIPFEED}\left(\frac{R}{R}\right) \quad \text{(EQ. 2)}$$

$$V_{RINGFEED} = V_D = V_{BAT} + 4 \quad \text{(EQ. 3)}$$

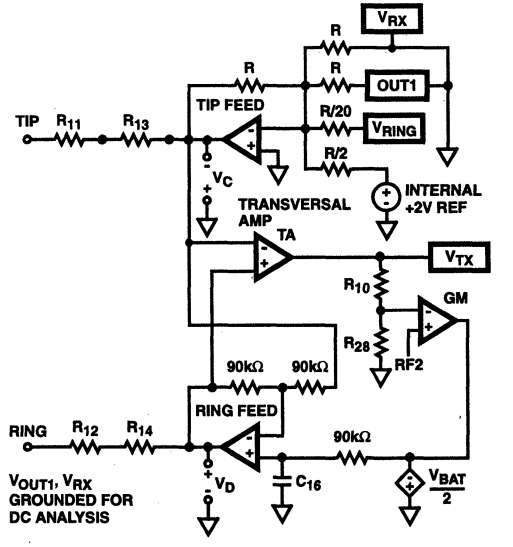


FIGURE 1. OPERATION OF THE TIP AND RING AMPLIFIERS

Current Limit

The tip feed to ring feed voltage (Equation 1 minus Equation 3) is equal to the battery voltage minus 8V. Thus, with a 48 (24) volt battery and a 600Ω loop resistance, including the feed resistors, the loop current is 66.6mA (26.6mA). On short loops the line resistance often approaches zero and the need exists to control the maximum DC loop current.

Current limiting is achieved by a feedback network (Figure 1) that modifies the ring feed voltage (V_D) as a function of the loop current. The output of the Transversal Amplifier (TA) has a DC voltage that is directly proportional to the loop current. This voltage is scaled by R_{10} and R_{28}. The scaled voltage is the input to a transconductance amplifier (GM) that compares it to an internal reference level. When the scaled voltage exceeds the internal reference level, the transconductance amplifier sources current. This current charges C_{16} in the positive direction causing the ring feed voltage (V_D) to approach the tip feed voltage (V_C). This effectively reduces the tip feed to ring feed voltage (V_{T-R}), and holds the maximum loop current constant.

The maximum loop current is programed by resistors R_{10} and R_{28} as shown in Equation 4 (Note: R_{10} is typically 100kΩ).

$$I_{LIMIT} = \frac{(0.6)(R_{10}+R_{28})}{(200xR_{28})} \quad \text{(EQ. 4)}$$

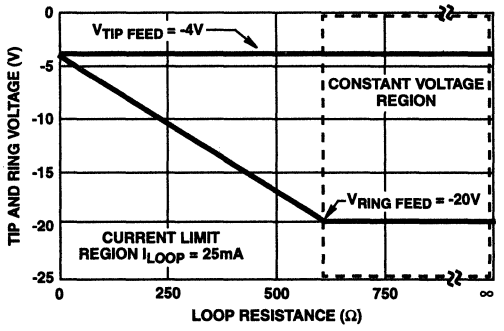


FIGURE 2. V_{T-R} vs R_L (V_{BAT} = -24V, I_{LIMIT} = 25mA)

Figure 2 illustrates the relationship between V_{T-R} and the loop resistance. The conditions are shown for a battery voltage of -24V and the loop current limit set to 25mA. For a infinite loop resistance both tip feed and ring feed are at -4V and -20V respectively. When the loop resistance decreases from infinity to about 640Ω the loop current (obeying Ohm's Law) increases from 0mA to the set loop current limit. As the loop resistance continues to decrease, the ring feed voltage approaches the tip feed voltage as a function of the programed loop current limit (Equation 4).

AC Voltage Gain Design Equations

The HC5517 uses feedback to synthesize the impedance at the 2-wire tip and ring terminals. This feedback network defines the AC voltage gains for the SLIC.

The 4-wire to 2-wire voltage gain (V_{RX} to V_{TR}) is set by the feedback loop shown in Figure 3. The feedback loop senses the loop current through resistors R_{13} and R_{14}, sums their voltage drop and multiplies it by 2 to produce an output voltage at the V_{TX} pin equal to $+4R_S\Delta I_L$. The V_{TX} voltage is then fed into the -IN1 input of the SLIC's internal op amp. This signal is multiplied by the ratio R_8/R_9 and fed into the tip current summing node via the OUT1 pin. (Note: the internal $V_{BAT}/2$ reference (ring feed amplifier) and the internal +2V reference (tip feed amplifier) are grounded for the AC analysis.)

The current into the OUT1 pin is equal to:

$$I_{OUT1} = -\frac{4R_S\Delta I_L}{R}\left(\frac{R_8}{R_9}\right) \quad \text{(EQ. 5)}$$

Equation 6 is the node equation for the tip amplifier summing node. The current in the tip feedback resistor (I_R) is given in Equation 7.

$$-I_R - \frac{4R_S\Delta I_L}{R}\left(\frac{R_8}{R_9}\right) + \frac{V_{RX}}{R} = 0 \quad \text{(EQ. 6)}$$

$$I_R = -\frac{4R_S\Delta I_L}{R}\left(\frac{R_8}{R_9}\right) + \frac{V_{RX}}{R} \quad \text{(EQ. 7)}$$

The AC voltage at V_C is then equal to:

$$V_C = (I_R)(R) \quad \text{(EQ. 8)}$$

$$V_C = -4R_S\Delta I_L\left(\frac{R_8}{R_9}\right) + V_{RX} \quad \text{(EQ. 9)}$$

and the AC voltage at V_D is:

$$V_D = 4R_S\Delta I_L\left(\frac{R_8}{R_9}\right) - V_{RX} \quad \text{(EQ. 10)}$$

The values for R_8 and R_9 are selected to match the impedance requirements on tip and ring, for more information reference AN9607 "Impedance Matching Design Equations for the HC5509 Series of SLICs". The following loop current calculations will assume the proper R_8 and R_9 values for matching a 600Ω load.

The loop current (ΔI_L) with respect to the feedback network, is calculated in Equations 11 through 14. Where R_8 = 40kΩ, R_9 = 40kΩ, R_L = 600Ω, $R_{11} = R_{12} = R_{13} = R_{14}$ = 50Ω.

$$\Delta I_L = \frac{V_C - V_D}{R_L + R_{11} + R_{12} + R_{13} + R_{14}} \quad \text{(EQ. 11)}$$

Substituting the expressions for V_C and V_D

$$\Delta I_L = \frac{2\times\left(-4R_S\Delta I_L\left(\frac{R_8}{R_9}\right) + V_{RX}\right)}{R_L + R_{11} + R_{12} + R_{13} + R_{14}} \quad \text{(EQ. 12)}$$

Equation 12 simplifies to

$$\Delta I_L = \frac{2V_{RX} - 400\Delta I_L}{800} \quad \text{(EQ. 13)}$$

Solving for ΔI_L results in

$$\Delta I_L = \frac{V_{RX}}{600} \quad \text{(EQ. 14)}$$

Equation 14 is the loop current with respect to the feedback network. From this, the 4-wire to 2-wire and the 2-wire to 4-wire AC voltage gains are calculated. Equation 15 shows the 4-wire to 2-wire AC voltage gain is equal to one.

$$A_{4W-2W} = \frac{V_{TR}}{V_{RX}} = \frac{\Delta I_L(R_L)}{V_{RX}} = \frac{\frac{V_{RX}}{600}(600)}{V_{RX}} = 1 \quad \text{(EQ. 15)}$$

Equation 16 shows the 2-wire to 4-wire AC voltage gain is equal to negative one-third.

$$A_{2W-4W} = \frac{V_{OUT1}}{V_{TR}} = \frac{-4R_S\Delta I_L\left(\frac{R_8}{R_9}\right)}{\Delta I_L(R_L)} = \frac{-200\frac{V_{RX}}{600}(1)}{\frac{V_{RX}}{600}(600)} = -\frac{1}{3} \quad \text{(EQ. 16)}$$

Impedance Matching

The feedback network, described above, is capable of synthesizing both resistive and complex loads. Matching the SLIC's 2-wire impedance to the load is important to maximize power transfer and minimize the 2-wire return loss. The 2-wire return loss is a measure of the similarity of the impedance of a transmission line (tip and ring) and the impedance at it's termination. It is a ratio, expressed in decibels, of the power of the outgoing signal to the power of the signal reflected back from an impedance discontinuity.

Requirements for Impedance Matching

Impedance matching of the HC5517 application circuit to the transmission line requires that the impedance be matched to points "A" and "B" in Figure 3. To do this, the sense resistors R_{11}, R_{12}, R_{13} and R_{14} must be accounted for by the feedback network to make it appear as if the output of the tip and ring amplifiers are at points "A" and "B". The feedback network takes a voltage that is equal to the voltage drop across the sense resistors and feeds it into the summing node of the tip amplifier. The effect of this is to cause the tip feed voltage to become more negative by a value that is proportional to the voltage drop across the sense resistors R_{11} and R_{13}. At the same time the ring amplifier becomes more positive by the same amount to account for resistors R_{12} and R_{14}.

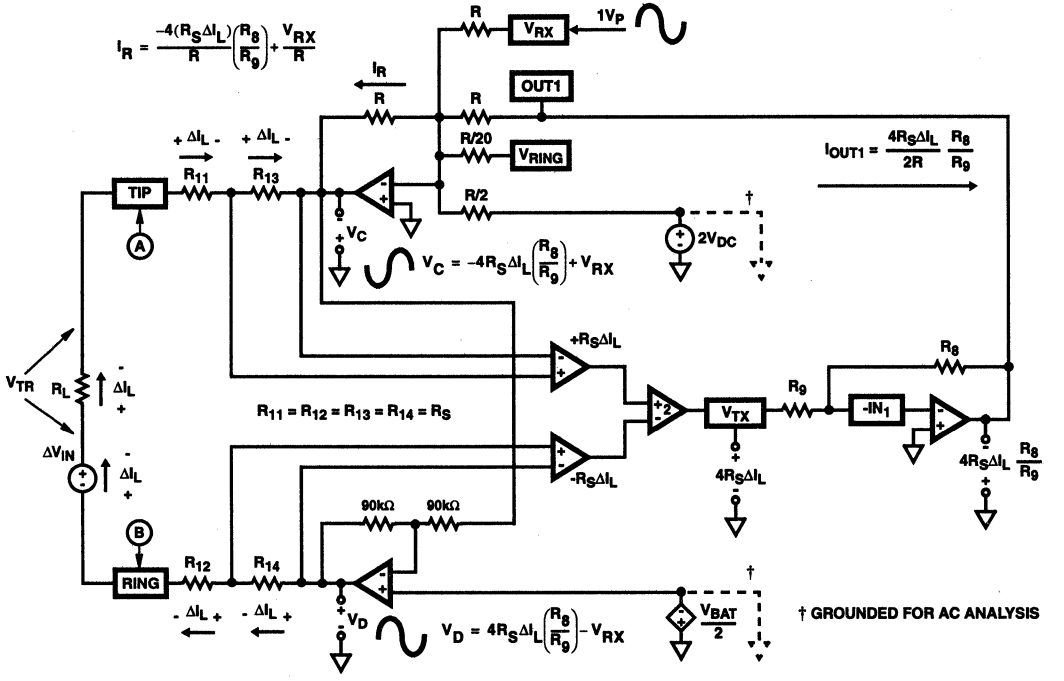


FIGURE 3. AC VOLTAGE GAIN AND IMPEDANCE MATCHING

The net effect cancels out the voltage drop across the feed resistors. By nullifying the effects of the feed resistors the feedback circuitry becomes relatively easy to match the impedance at points "A" and "B".

IMPEDANCE MATCHING DESIGN EQUATIONS

Matching the impedance of the SLIC to the load is accomplished by writing a loop equation starting at V_D and going around the loop to V_C. The loop equation to match the impedance of any load is as follows (note: $V_{RX} = 0$ for this analysis):

$$-4R_S\Delta I_L\left(\frac{R_8}{R_9}\right) + 2R_S\Delta I_L - \Delta V_{IN} +$$

$$R_L\Delta I_L + 2R_S\Delta I_L - 4R_S\Delta I_L\left(\frac{R_8}{R_9}\right) = 0 \quad \text{(EQ. 17)}$$

$$\Delta V_{IN} = -8R_S\Delta I_L\left(\frac{R_8}{R_9}\right) + 4R_S\Delta I_L + R_L\Delta I_L \quad \text{(EQ. 18)}$$

$$\Delta V_{IN} = \Delta I_L\left[-8R_S\left(\frac{R_8}{R_9}\right) + 4R_S + R_L\right] \quad \text{(EQ. 19)}$$

Equation 19 can be separated into two terms, the feedback ($-8R_S(R_8/R_9)$) and the loop impedance ($+4R_S+R_L$).

$$\frac{\Delta V_{IN}}{\Delta I_L} = -8R_S\left(\frac{R_8}{R_9}\right) + 4R_S + R_L \quad \text{(EQ. 20)}$$

The result is shown in Equation 20. Figure 4 is a schematic representation of Equation 15.

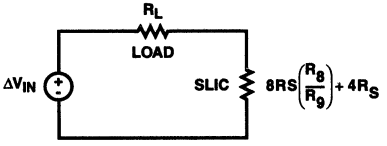


FIGURE 4. SCHEMATIC REPRESENTATION OF EQUATION 20

To match the impedance of the SLIC to the impedance of the load, set

$$R_L = 8R_S\left(\frac{R_8}{R_9}\right) + 4R_S \quad \text{(EQ. 21)}$$

If R_9 is made to equal $8R_S$ then:

$$R_L = R_8 + 4R_S \quad \text{(EQ. 22)}$$

Therefore to match the HC5517, with R_S equal to 50Ω, to a 600Ω load:

$$R_9 = 8R_S = 8(50\Omega) = 400\Omega \quad \text{(EQ. 23)}$$

and

$$R_8 = R_L - 4R_S = 600\Omega - 200\Omega = 400\Omega \quad \text{(EQ. 24)}$$

To prevent loading of the V_{TX} output, the value of R_8 and R_9 are typically scaled by a factor of 100:

$$KR_8 = 40k\Omega \qquad KR_9 = 40k\Omega \quad \text{(EQ. 25)}$$

Since the impedance matching is a function of the voltage gain, scaling of the resistors to achieve a standard value is recommended.

For complex impedances the above analysis is the same.

$$KR_9 = 40k\Omega \qquad KR_8 = 100(\text{Resistive} - 200) + \frac{\text{Reactive}}{100} \quad \text{(EQ. 26)}$$

Reference application note AN9607 ("Impedance Matching Design Equations for the HC5509 Series of SLICs") for the values of KR_9 and KR_8 for several worldwide Typical line impedances.

Tip-to-Ring Open-Circuit Voltage

The tip-to-ring open-circuit voltage, V_{OC}, of the HC5517 is programmable to meet a variety of applications. The design of the HC5517 defaults the value of V_{OC} to

$$V_{OC} \cong |V_{BAT}| - 8$$

The HC5517 application circuit overrides the default V_{OC} operation when operating from a -80V battery. While operating from a -80V battery, the SLIC will be in either the ringing mode or on-hook standby mode. In the ringing mode, V_{OC} is designed to switch from 0V (centering voltage) to -47V (Maintenance Termination Unit voltage). The centering voltage is active during the ringing portion of the ringing waveform and the Maintenance Termination Unit (MTU) voltage is active during the silent portion of the ringing signal. In the on-hook standby mode, the application circuit is designed to maintain V_{OC} at the MTU voltage.

Centering Voltage Application Circuit Overview

The centering voltage is used during ringing to center the DC outputs of the tip feed and ring feed amplifiers. Centering the amplifier outputs allows for the maximum undistorted voltage swing of the ringing signal. Without centering, the output of each amplifier would saturate at ground or V_{BAT}, minimizing the ringing capability of the HC5517. The required centering voltage, V_C, is $+1.8V_{DC}$ when operating from a -80V battery.

Centering Voltage Application Circuit Operation

The circuit used to generate the centering voltage is shown in Figure 5.

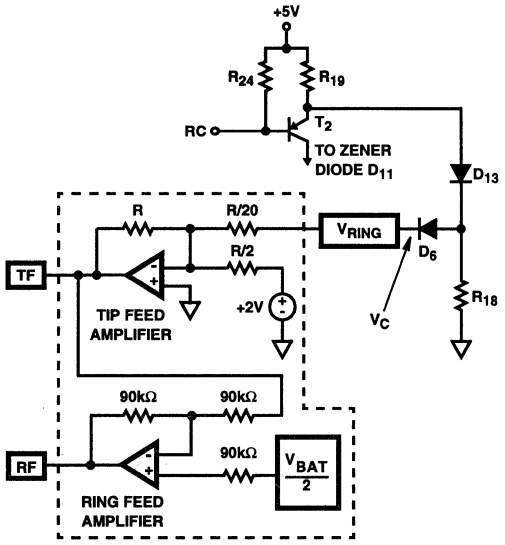


FIGURE 5. CENTERING VOLTAGE APPLICATION CIRCUIT

The circuitry within the dotted lines is internal to the HC5517. The value of the resistor designated as R is 108kΩ and the resistor R/20 is 5.4kΩ. The tip amplifier gain of 20V/V amplifies the $+1.8V_{DC}$ at V_C to $+36V_{DC}$ and adds it to the internal $4V_{DC}$ offset, generating $-40V_{DC}$ at the tip amplifier output. The $-40V_{DC}$ offset also sums into the ring amplifier, adding to the battery voltage, achieving -40V at the ring amplifier output.

Centering Voltage Design Equations

The centering voltage (V_C) is dependent on the battery voltage. A battery voltage of -80V requires a $+1.8V_{DC}$ centering voltage. The equation used to calculate the centering voltage is shown below.

$$V_C = \left(\left|\frac{V_{BAT}}{2}\right| - 4\right)/20 \quad \text{(EQ. 27)}$$

The DC voltage at the outputs of the centered tip and ring amplifiers can be calculated from Equation 28 and Equation 29.

$$V_{TC} = -(20V_C + 4) \quad \text{(EQ. 28)}$$

$$V_{RC} = V_{BAT} + (20V_C + 4) \quad \text{(EQ. 29)}$$

The shunt resistor of the divider network, R_{18}, is not determined from a design equation. It is selected based on the trade-off of power dissipation in the voltage divider (low value of R_{18}) and loading affects of the internal R/20 resistor

(high value of R_{18}). The suggested range of R_{18} is between 1.0kΩ and 2.0kΩ. The application circuit design equation used to calculate the value of R_{19} of the divider network is as follows:

$$R_{19} = \frac{(V_{CC} - V_{D13} - V_{D6} - V_C)(R_{18} \bullet R_{IN})}{(V_C + V_{D6})R_{IN} + V_C R_{18}} \quad \text{(EQ. 30)}$$

where: V_{D13} forward drop of D_{13}, 0.63V.

V_{D6} forward drop of D_6, 0.54V.

R_{18} is the shunt resistor of the divider, 1.1kΩ.

R_{IN} is the input impedance of V_{RING}, 5.4kΩ.

V_C is the required centering voltage, 1.8V, V_{BAT} = -80V.

V_{CC} is the +5V supply.

Centering Voltage Logic Control

The pnp transistor T_2 is used to defeat the voltage divider formed by R_{19}, R_{18}, D_{13} and D_6. When T_2 is off (RC is logic high), +5V_{DC} is divided to produce +1.8V_{DC} at the V_{RING} input. When T_2 is on (RC is logic low), its emitter base voltage of +0.9V_{DC} is divided resulting in +0.2V at the anode of D_6, hence reverse biasing the diode (D_6) and floating the V_{RING} pin.

MTU Voltage Application Circuit Overview

According to Bellcore specification TR-NWT-000057, an MTU voltage may be required by some operating companies. The minimum allowable voltage to meet MTU requirements is -42.75V, which is used by measurement equipment to verify an active line. Also, some facsimile and answering machines use the MTU voltage as an indication that the telephone is on-hook or not answered. In addition to the Bellcore specification, FCC Part 68.306 requires that the maximum tip to ground or ring to ground voltage not exceed -56.5V for hazardous voltage limitations. These two requirements have been combined and the resulting range is defined as the MTU voltage. The HC5517 application circuit can be programmed to any voltage within this range using the zener clamping circuit.

MTU Voltage Application Circuit Operation

The circuit used to generate the MTU voltage is shown in Figure 6.

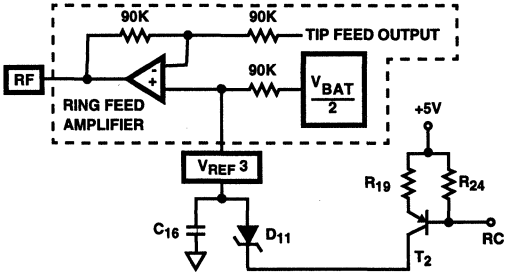


FIGURE 6. RING FEED AMPLIFIER CIRCUIT CONNECTIONS

The ring feed amplifier DC output voltage, V_{RDC}, is a function of the internal $V_{BAT}/2$ reference and external zener diode D_{11}. When the magnitude of $V_{BAT}/2$ is less then the zener voltage, the zener is off and the input to the ring feed amplifier is $V_{BAT}/2$. When the magnitude of $V_{BAT}/2$ is greater than the zener voltage, the zener conducts and clamps the noninverting terminal of the ring amplifier to the zener voltage.

Internal to the HC5517 are connections to the tip feed amplifier output and $V_{BAT}/2$ reference. The DC voltage at the tip feed output, V_{TDC}, is a constant -4V during on-hook standby.

MTU Voltage Design Equations

The following equations are used to predict the DC output of the ring feed amplifier, V_{RDC}.

$$\left|\frac{V_{BAT}}{2}\right| < V_Z \qquad V_{RDC} = 2\left(\frac{V_{BAT}}{2}\right) + 4 \quad \text{(EQ. 31)}$$

$$\left|\frac{V_{BAT}}{2}\right| \geq V_Z \qquad V_{RDC} = 2(-V_Z + (V_{CE} - V_{BE})) + 4 \quad \text{(EQ. 32)}$$

Where V_Z is the zener diode voltage of D_{11} and V_{CE} and V_{BE} are the saturation voltages of T_2. Using Equations 31 and 32, the tip-to-ring open-circuit voltage can be calculated for any value of zener diode and battery voltage.

$$\left|\frac{V_{BAT}}{2}\right| < V_Z \qquad V_{OC} = V_{TDC} - 2\left(\frac{V_{BAT}}{2}\right) - 4 \quad \text{(EQ. 33)}$$

$$\left|\frac{V_{BAT}}{2}\right| \geq V_Z \qquad V_{OC} = V_{TDC} - 2(-V_Z + (V_{CE} - V_{BE})) - 4 \quad \text{(EQ. 34)}$$

Figure 7 plots V_{OC} as a function of battery voltage. The graph illustrates the clamping function of the zener circuitry.

FIGURE 7. V_{OC} AS A FUNCTION OF BATTERY VOLTAGE

MTU Voltage Logic Control

The same pnp transistor, T_2, that is used to control the centering voltage is also used to control the MTU voltage. The application circuit uses T_2 to ground or float the anode of the zener diode D_{11}. When RC is a logic low (T_2 on) the anode of D_{11} is referenced to ground through the collector base junction of the transistor. Current then flows through the zener, allowing the ring amplifier input to be clamped. When RC is a logic high (T_2 off) the anode of D_{11} floats, inhibiting the clamping action of the zener.

HC5517 Modes of Operation

The four modes of operation of the HC5517 Ringing SLIC are ringing, on-hook standby, off-hook active and power denial. Three control signals select the operating mode of the SLIC. The signals are Battery Switch, F1 and Ring Cadence (RC). The active application circuit and active supervisory function are different for each mode, as shown in the Table 2.

Mode Control Signals

The Battery Switch selects between the -80V and -24V supplies. The Battery Switch circuitry is described in the "Operation of the Battery Switch" section. A system alternative to the battery switch signal is to use a buffered version of the $\overline{SHD}$ output to select the battery voltage. Another alternative is to control the output of a programmable battery supply, removing the battery switch entirely from the application circuit. F1 is used to put the SLIC in the power denial mode. RC drives the base of T_2, which is the transistor used to control the centering voltage and MTU voltage. The three control signals can be driven from a TTL logic source or an open collector output

RINGING MODE

The ringing state, as the name indicates, is used to ring the telephone with a -80V battery supply. The SLIC is designed for balanced ringing with a differential gain of 40V/V across tip and ring. Voltage feed amplifiers operating in the linear mode are used to amplify the ringing signal. The linear amplifier approach allows the system designer to define the shape and amplitude of the ringing waveform. Both supervisory function outputs, $\overline{SHD}$ and $\overline{RTD}$, are active during ringing.

Spectral Content of the Ringing Signal

The shape of the waveform can range from sinusoidal to trapezoidal. Sinusoidal waveforms are spectrally cleaner than trapezoidal waveforms, although the latter does result in lower power dissipation across the SLIC for a given rms amplitude. Systems where the ringing signal will be in proximity to digital data lines will benefit from the sinusoidal ringing capability of the HC5517. The slow edge rates of a sinusoid will minimize coupling of the large amplitude ringing signal. The linear amplifier architecture of the HC5517 allows the system designer to optimize the design for power dissipation and spectral purity.

Amplitude of the Ringing Signal

Amplitude control is another benefit of the linear amplifier architecture. Systems that require less ringing amplitude are able to do so by driving the HC5517 with a lower level ringing waveform. Solutions that use saturated amplifiers can only vary the amplitude of the ringing signal by changing the negative battery voltage to the SLIC.

HC5517 Through SLIC Ringing

The HC5517 is designed with a high gain input, V_{RING}, that the system drives while ringing the phone. V_{RING} is one of many signals summed at the inverting input to the tip feed amplifier. The gain of the V_{RING} signal through the tip feed amplifier is set to 20V/V. The output of the tip feed amplifier is summed at the inverting input of the ring feed amplifier, configured for unity gain. The result is a differential gain of 40V/V across tip and ring of the ringing signal.

The ringing function requires an input ringing waveform and a centering voltage. The ringing waveform is the signal from the 4-wire side that is amplified by the SLIC to ring the telephone. The centering voltage, as previously discussed, is a positive DC offset that is applied to the V_{RING} input along with the ringing waveform. The HC5517 application circuit provides the centering voltage, simplifying the system interface to an AC coupled ringing waveform.

Ringer Equivalence Number

Before any further discussion, the Ringer Equivalence Number or REN must be discussed. Based on FCC Part 68.313 a single REN can be defined as 5kΩ, 7kΩ or 8kΩ of AC impedance at the ringing frequency. The ringing frequency is based on the ringing types listed in Table 1 of the FCC specification. The impedance of multiple REN is the paralleling of a single REN. Therefore 5 REN can either be 1kΩ, 1.4kΩ or 1.6kΩ. The 7kΩ model of a single REN will be used throughout the remainder of the data sheet.

Ringing Waveform

An amplitude of $1.2V_{RMS}$ will deliver approximately $46V_{RMS}$ to a 1 REN load, and $42V_{RMS}$ to a 3 REN load. The amplitude is REN dependent and is slightly attenuated by the feedback scheme used for impedance matching. The ringing waveform is cadenced, alternating between a 20Hz burst and a silent portion between bursts. Bellcore specification TR-NWT-000057 defines seven distinct ringing waveforms or alerting (ringing) patterns. The following table lists each type.

TABLE 1. DISTINCTIVE ALERTING PATTERNS

	INTERVAL DURATION IN SECONDS					
PATTERN	RINGING	SILENT	RINGING	SILENT	RINGING	SILENT
A	0.4	0.2	0.4	0.2	0.8	4.0
B	0.2	0.1	0.2	0.1	0.6	4.0
C	0.8	0.4	0.8	0.4		
D	0.4	0.2	0.6	4.0		
E	1.2	4.0				
F	1 ± 0.2	3 ± 0.3				
G	0.3	0.2	1.0	0.2	0.3	4.0

Figure 8 shows the relationship of the cadenced ringing waveform and the Battery Switch and RC control signals. Also shown are the states of the MTU voltage and the centering voltage.

The state of Battery Switch is indicated by the desired battery voltage to the SLIC. The RC signal is used to enable and disable the centering voltage and MTU voltage. RC follows the ring signal in that it is high during the 20Hz burst and low during the static part of the waveform.

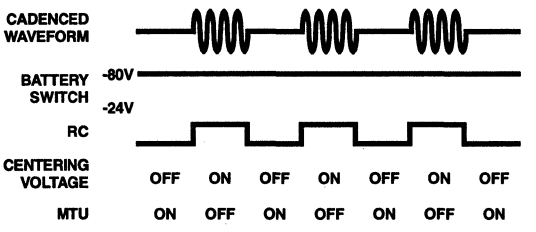


FIGURE 8. RINGING WAVEFORM AND CONTROL SIGNALS

Open Circuit Voltage During the Ringing Mode

The mutually exclusive relationship of the centering voltage and MTU implies that both functions will not exist at the same time. During the silent portion of the ringing waveform the HC5517 application circuit meets the hazardous voltage requirements of FCC Part 68.306 by forcing the MTU voltage. Without the zener clamping solution, a programmable power supply would have to be designed. The intervals listed in Table 1 would require the power supply to switch voltages and settle to stable operation well within 100ms. The design of such a power supply may prove quite a challenge. The zener solution provides a cost effective, low impact to meeting a wide variety of tip to ring open circuit voltages.

Ringing Design Equations

The differential tip to ring voltage during ringing, as a function of REN, can be approximated from Equation 35.

$$V_{TR}(R_L) \cong 2 \times \left[\frac{V_{RING}}{5.4e3} - \frac{(0.702)(200)V_{TRO}}{(108e3)R_L}\right] \bullet 108e3 \quad \text{(EQ. 35)}$$

The voltage V_{RING} is defined as the rms amplitude of the input ringing signal. V_{TRO} is the open circuit tip to ring differential output voltage, calculated as V_{RING} multiplied by the differential gain of 40V/V. The REN impedance is shown as R_L. Figure 9 shows the relationship of REN load to maximum differential tip to ring rms voltage during ringing. The maximum ringing signal amplitude herein assumes an infinite source and sink capability of the tip feed and ring feed amplifiers. Due to the amplifier output design, the HC5517 is limited to 3 REN ringing capability for this reason.

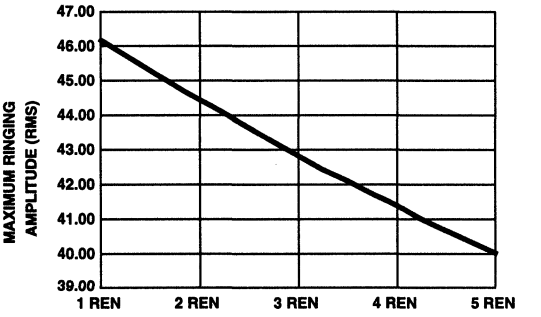


FIGURE 9. MAXIMUM RINGING OUTPUT VOLTAGE ($V_{RING} = 1.2V_{RMS}$)

ON-HOOK STANDBY MODE

On-hook standby mode is with the phone on-hook (i.e., not answered) and ready to accept an incoming voice signal or electronic data. The HC5517 application circuit is designed to maintain the MTU voltage during this mode of operation. During this mode, the $\overline{SHD}$ output is valid and the $\overline{RTD}$ output is invalid.

OFF-HOOK ACTIVE MODE

Off-hook active accommodates voice and data communications, including pulse metering, with a battery voltage of -24V. The MTU voltage during this mode is defeated by the zener clamp design regardless of the state of RC. It is important to have RC low to disable the ringing voltage. Only the $\overline{SHD}$ output is valid during this mode.

POWER DENIAL MODE

The HC5517 will enter the power denial mode whenever F1 is a logic low. During power denial, the tip and ring amplifiers are active. The DC voltages of both amplifiers are near ground, resulting in a maximum loop current of 7mA. Both the $\overline{SHD}$ and the $\overline{RTD}$ detector output are invalid.

Table 2 summarizes the operating modes of the HC5517 application circuit. The table indicates the valid detectors in each mode as well as valid application circuit operation.

TABLE 2. HC5517 APPLICATION CIRCUIT OPERATING MODES SUMMARY

BATTERY SWITCH	F1	RC	MODE	DETECTORS VALID		APPLICATION CIRCUIT VALID	
				$\overline{SHD}$	$\overline{RTD}$	MTU	CENTERING
-24V	0	0	Power Denial				
-24V	0	1	Invalid				
-24V	1	0	Off-Hook Active	√			
-24V	1	1	Invalid				
-80V	0	0	Power Denial			√	
-80V	0	1	Invalid				
-80V	1	0	On-Hook Standby	√		√	
-80V	1	1	Ringing	(Note)	√		√

NOTE: During Ringing, the $\overline{SHD}$ output will be active for both on-hook and off-hook conditions. The AC current, for the on-hook condition, exceeds the $\overline{SHD}$ threshold of 12mA. Valid off-hook detection during ringing is provided by the $\overline{RTD}$ output only.

Operation of the Battery Switch

The battery switch is used to select between the off-hook battery of -24V and the ringing/standby battery of -80V. When T_1 is off (battery switch is logic low) the MOSFET T_3 is off and the -24V battery is supplied to the SLIC through D_{10}. When T_1 is on (battery switch is logic high) current flows through the collector of T_1 turning on the zener D_9. When D_9 turns on, the gate of the MOSFET is positive with respect to the drain (-80V) and T_3 turns on. Turning T_3 on connects the -80V battery to the SLIC through D_7. This in turn reverse biases D_{10}, isolating the two supplies.

Transhybrid Balance (Voice Signal)

The purpose of the transhybrid circuit is to remove the receive signal (V-REC) from the transmit signal (V-XMIT), thereby preventing an echo on the transmit side. This is accomplished by using an external op amp (usually part of the CODEC) and by the inversion of the signal from the SLIC's 4-wire receive port (V_{RX}) to the SLIC's 4-wire transmit port (OUT1).

The external transhybrid circuit is shown in Figure 10. The effects of capacitors C_5, C_7 and C_8 are negligible and therefore omitted from the analysis. The input signal (V-REC) will be subtracted from the output signal (V-XMIT) if I_1 equals I_2 are equal and opposite in phase. A node analysis yields the following equation:

$$\frac{V\text{-REC}}{R_2} + \frac{OUT1}{R_3} = 0 \qquad \text{(EQ. 36)}$$

The value of R_2 is then

$$R_2 = -R_3 \bullet \frac{V\text{-REC}}{OUT1} \qquad \text{(EQ. 37)}$$

Given that OUT1 is equal to -1/3 of V-REC (Equation 16) and V-REC is equal to VTR ($A_{4\text{-Wire-2-Wire}} = 1$, Equation 15), then $R_2 = 3R_3$. A transhybrid balance greater than 30dB can be achieved by using 1% resistors values.

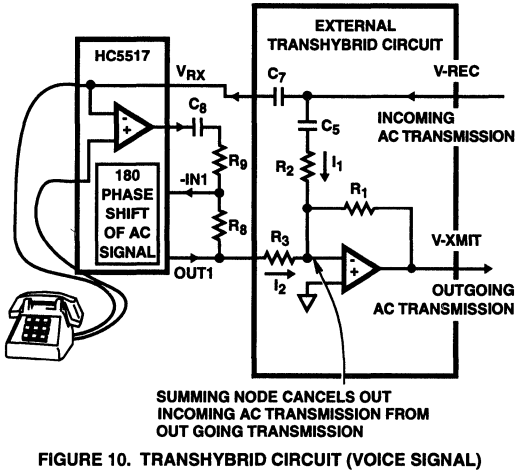


FIGURE 10. TRANSHYBRID CIRCUIT (VOICE SIGNAL)

Transhybrid Balance (Pulse Metering)

Transhybrid balance of the pulse metering signal is accomplished in 2 stages. The first stage uses the SLIC's internal op amp to invert the phase of the pulse metering signal. The second stage sums the inverted pulse metering signal with the incoming signal for cancellation in the transhybrid amplifier. A third network can be added to offset both tip and ring by the peak amplitude of the pulse metering signal. This will allow both the maximum voice and pulse metering signals to occur at the same time with no distortion.

Pulse Metering

Pulse metering or Teletax is used outside the United States for billing purposes at pay phones. A 12kHz or 16kHz burst is injected into the 4-wire side of the SLIC and transmitted across the tip and ring lines from the central office to the pay phone. For more information about pulse metering than covered here reference application note AN9608 "Implementing Pulse Metering for the HC5509 Series of SLICs".

Inverting Amplifier (A1)

The pulse metering signal is injected in the -IN1 pin of the SLIC. This pin is the inverting input of the internal amplifier (A_1) that is used to invert the pulse metering signal for later cancellation. The components required for pulse metering are C_6 and R_5, are shown in Figure 11. The pulse metering signal is AC coupled to prevent a DC offset on the input of the internal amplifier. The value of C_6 should be 10µF. The expression for the voltage at OUT1 is given in Equation 38.

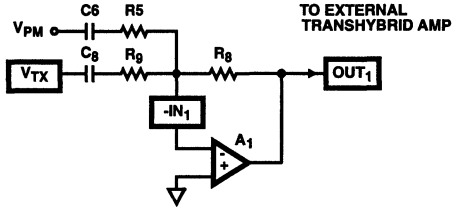


FIGURE 11. PULSE METERING PHASE SHIFT AMPLIFIER DESIGN

$$V_{OUT1} = -V_{TX} \bullet \frac{R_8}{R_9} - V_{PM} \bullet \frac{R_8}{R_5} \qquad \text{(EQ. 38)}$$

The first term is the gain of the feedback voltage from the 2-wire side and the second term is the gain of the injected pulse metering signal. The effects of C_6 and C_8 are negligible and therefore omitted from the analysis.

The injected pulse metering output term of Equation 38 is shown below in Equation 39 and rearranged to solve for R_5 in Equation 40.

$$V_{OUT1}(\text{injected}) = V_{PM} \bullet \frac{R_8}{R_5} = 1 \qquad \text{(EQ. 39)}$$

$$R_5 = R_8 \qquad \text{(EQ. 40)}$$

The ratio of R_8 to R_5 is set equal to one and results in unity gain of the pulse metering signal from 4-wire side to 2-wire side. The value of R_8 is considered to be a constant since it is selected based on impedance matching requirements.

Cancellation of the Pulse Metering Signal

The transhybrid cancellation technique that is used for the voice signal is also implemented for pulse metering. The technique is to drive the transhybrid amplifier with the signal that is injected on the 4-wire side, then adjust its level to match the amplitude of the feedback signal, and cancel the signals at the summing node of an amplifier.

NOTE: The CA741C operational amplifier is used in the application as a "stand in" for the operational amplifier that is traditionally located in the CODEC, where transhybrid cancellation is performed.

Referring to Figure 3, V_{TX} is the 2-wire feedback used to drive the internal amplifier (A1) which in turn drives the OUT1 pin of the SLIC. The voltage measured at V_{TX} is related to the loop impedance as follows:

$$V_{TX} = \frac{-200}{R_L} \bullet V_{PM} \bullet G_{PM} \qquad \text{(EQ. 41)}$$

For a 600Ω termination and a pulse metering gain (G_{PM}) of 1, the feedback voltage (V_{TX}) is equal to one third the injected pulse metering signal of the 4-wire side. Note, depending upon the line impedance characteristics and the degree of impedance matching, the pulse metering gain may differ from the voice gain. The pulse metering gain (G_{PM}) must be accounted for in the transhybrid balance circuit.

The polarity of the signal at OUT1 (Equation 38) is opposite of V_{PM} allowing the circuit of Figure 12 to perform the final stage of transhybrid cancellation.

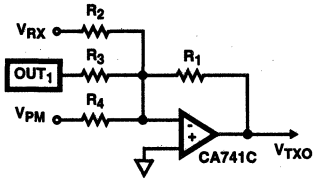


FIGURE 12. CANCELLATION OF THE PULSE METERING SIGNAL

The following equations do not require much discussion. They are based on inverting amplifier design theory. The voice path V_{RX} signal has been omitted for clarity. All reference designators refer to components of Figures 11 and 12.

$$V_{TXO} = -R_8 \bullet \left(-\frac{V_{TX}}{R_9} - \frac{V_{PM}}{R_5}\right) \bullet \frac{R_1}{R_3} - \left(V_{PM} \bullet \frac{R_1}{R_4}\right) \qquad \text{(EQ. 42)}$$

The first term refers to the signal at OUT1 and the second term refers to the 4-wire side pulse metering signal. Since ideal transhybrid cancellation implies V_{TXO} equals zero when a signal is injected on the 4-wire side, V_{TXO} is set to zero and the resulting equation is shown below.

$$0 = R_8 \bullet \left(\frac{V_{TX}}{R_9} + \frac{V_{PM}}{R_5}\right) \bullet \frac{R_1}{R_3} - \left(V_{PM} \bullet \frac{R_1}{R_4}\right) \qquad \text{(EQ. 43)}$$

Rearranging terms of Equation 43 and solving for R_4 results in Equation 44. This is the only value to be calculated for the transhybrid cancellation. All other values either exist in the application circuit or have been calculated in previous sections of this data sheet.

$$R_4 = \left(\frac{R_8}{R_3} \bullet \left(\frac{-200 \bullet G_{PM}}{R_L \bullet R_9} + \frac{1}{R_5}\right)\right)^{-1} \qquad \text{(EQ. 44)}$$

The value of R_4 (Figure 12) is 12.37kΩ given the following set of values:

$R_8 = 40k\Omega$

$R_9 = 40k\Omega$

$R_L = 600\Omega$

$R_3 = 8.25k\Omega$

$R_5 = 40k\Omega$

$G_{PM} = 1$

Substituting the same values into Equation 41 and Equation 42, it can be shown that the signal at OUT_1 is equal to $-2/3V_{PM}$. This result, along with Equation 44 where R_3 equals to 2/3R4, indicates the signal levels into the transhybrid amplifier are equalized by the amplifier gains and opposite in polarity, thereby achieving transhybrid balance at V_{TXO}.

Additional Tip and Ring Offset Voltage

A DC offset is required to level shift tip and ring from ground and V_{BAT} respectively. By design, the tip amplifier is offset 4V below ground and the ring amplifier is offset 4V above V_{BAT}. The 4V offset was designed so that the peak voice signal could pass through the SLIC without distortion. Therefore, to maintain distortion free transmission of pulse metering and voice, an additional offset equal to the peak of the pulse metering signal is required.

The tip and ring voltages are offset by a voltage divider network on the V_{RX} pin. The V_{RX} pin is a unity gain input designed as the 4-wire side voice input for the SLIC. Figure 13 details the circuit used to generate the additional offset voltage.

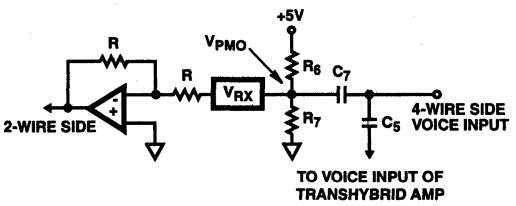


FIGURE 13. PULSE METERING OFFSET GENERATION

The amplifier shown is the tip amplifier. Other signals are connected to the summing node of the amplifier but only those components used for the offset generation are shown. The offset generated at the output of the tip amplifier is summed at the ring amplifier inverting input to provide a positive offset from the battery voltage. The connection to the ring amplifier was omitted from Figure 13 for clarity, refer to Figure 3 for details.

The term V_{PMO} is defined to be the offset required for the pulse metering signal. The value of the offset voltage is calculated as the peak value of the pulse metering signal. Equation 45 assumes the amplitude of the pulse metering signal is expressed as an rms voltage.

$$V_{PMO} = \sqrt{2} \bullet V_{PM} \quad \text{(EQ. 45)}$$

The value of R_6 can be calculated from the following equation:

$$R_6 = \left(\frac{R_7 R}{R_7 + R}\right)\left(\frac{5 - V_{PMO}}{V_{PMO}}\right) \quad \text{(EQ. 46)}$$

The component labeled R is the internal summing resistor of the tip amplifier and has a typical value of 108kΩ. The value of R_7 should be selected in the range of 4.99kΩ and 10kΩ. Staying within these limits will minimize the parallel loading effects of the internal resistor R on R_7 as well as minimize the constant power dissipation introduced by the divider.

Solving Equation 45 for $1V_{RMS}$ results in a 1.414V requirement for V_{PMO}. Setting R_7 of Equation 46 to 10kΩ and substituting the values for V_{PMO} and R yields 23.2kΩ for R_6. The value of R_6 can be rounded to the nearest standard value without significantly changing the offset voltage.

Single Low Voltage Supply Operation

The application circuit shown Figure 15 requires 2 low voltage supplies (+5V, -5V). The following application offers away to make use of a 2.5V reference, provided with some CODEC, to operate the transhybrid balance amplifier from a single +5V supply. The implementation is shown in Figure 14. Notice that the three inputs from the SLIC must all be AC coupled to insure the proper DC gain through the CODECs internal op amp. The resistor Ra is not used for gain setting and is only intended to balance the DC offsets generated by the input bias current of the CODEC amplifier. If the DC offsets generated by the input bias currents are negligible, then Ra may be omitted from the circuit. Ca may be required for decoupling of the voltage reference pin and does not contribute to the response of the amplifier.

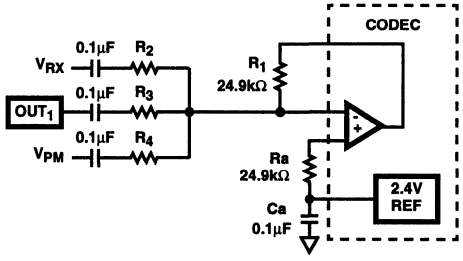


FIGURE 14. SINGLE LOW VOLTAGE SUPPLY OPERATION

Layout Guidelines and Considerations

The printed circuit board trace length to all high impedance nodes should be kept as short as possible. Minimizing length will reduce the risk of noise or other unwanted signal pickup. The short lead length also applies to all high gain inputs. The set of circuit nodes that can be categorized as such are:

- V_{RX} pin 27, the 4-wire voice input.
- -IN1 pin 13, the inverting input of the internal amplifier.
- V_{REF} pin 3, the noninverting input to ring feed amplifier.
- V_{RING} pin 24, the 20V/V input for the ringing signal
- U1 pin 2, inverting input of external amplifier.

For multi layer boards, the traces connected to tip should not cross the traces connected to ring. Since they will be carrying high voltages, and could be subject to lightning or surge depending on the application, using a larger than minimum trace width is advised.

The 4-wire transmit and receive signal paths should not cross. The receive path is any trace associated with the V_{RX} input and the transmit path is any trace associated with V_{TX} output. The physical distance between the two signal paths should be maximized to reduce crosstalk.

The mode control signals and detector outputs should be routed away from the analog circuitry. Though the digital signals are nearly static, care should be taken to minimize coupling of the sharp digital edges to the analog signals.

The part has two ground pins, one is labeled AGND and the other BGND. Both pins should be connected together as close as possible to the SLIC. If a ground plane is available, then both AGND and BGND should be connected directly to the ground plane.

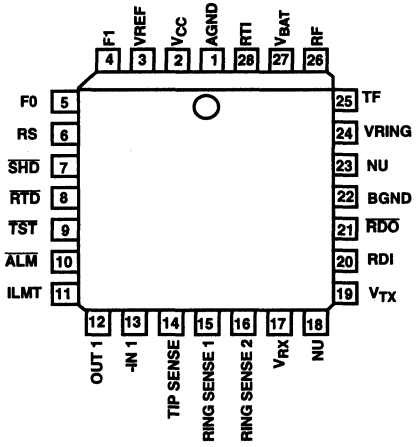
A ground plane that provides a low impedance return path for the supply currents should be used. A ground plane provides isolation between analog and digital signals. If the layout density does not accommodate a ground plane, a single point grounding scheme should be used.

Application Pin Descriptions

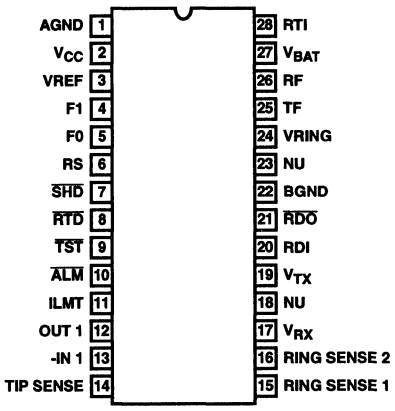
PLCC	SYMBOL	DESCRIPTION
1	AGND	Analog Ground - To be connected to zero potential. Serves as a reference for the transmit output and receive input terminals.
2	V_{CC}	Positive Voltage Source - Most Positive Supply.
3	V_{REF}	Ring amplifier reference override. An external voltage connected to this pin will override the internal $V_{BAT}/2$ reference.
4	F1	Power Denial -A low active TTL compatible logic control input. When enabled, the output of the ring amplifier will ramp close to the output voltage of the tip amplifier.
5	F0	TTL compatible logic control input that must be tied high for proper SLIC operation.
6	RS	TTL compatible logic control input that must be tied high for proper SLIC operation.
7	$\overline{SHD}$	Switch Hook Detection - An active low TTL compatible logic output. Indicates an offhook condition.
8	RTD	Ring Trip Detection - An active low TTL compatible logic output. Indicates an off-hook condition when the phone is ringing.
9	$\overline{TST}$	TTL compatible logic control input that must be tied high for proper SLIC operation.
10	$\overline{ALM}$	A TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded.
11	I_{LMT}	Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions using a resistive voltage divider.
12	OUT1	The analog output of the spare operational amplifier.
13	-IN1	The inverting analog input of the spare operational amplifier. Note that the non-inverting input of the amplifier is internally connected to AGND.
14	TIP SENSE	An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor and ring relay contact. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purpose.
15	RING SENSE 1	An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.
16	RING SENSE 2	This is an internal sense mode that must be tied to RING SENSE 1 for proper SLIC operation.
17	V_{RX}	Receive Input, 4-Wire Side - A high impedance analog input. AC signals appearing at this input drive the Tip Feed and Ring Feed amplifiers deferentially.
18	NU	Not used in this application.This pin should be left floating.
19	V_{TX}	Transmit Output, 4-Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is necessary.
20	RDI	TTL compatible input to drive the uncommitted relay driver.
21	$\overline{RDO}$	This is the output of the uncommitted relay driver.
22	BGND	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this terminal.
23	NU	Not used in this application. This pin should be either grounded or left floating.
24	V_{RING}	Ring signal input (0V to $3V_{PEAK}$ at 20Hz).
25	TF	This is the output of the tip amplifier.
26	RF	This is the output of the ring amplifier.
27	V_{BAT}	The negative battery source.
28	RTI	Ring Trip Input - This pin is connected to the external negative peak detector output for ring trip detection.

Pinouts

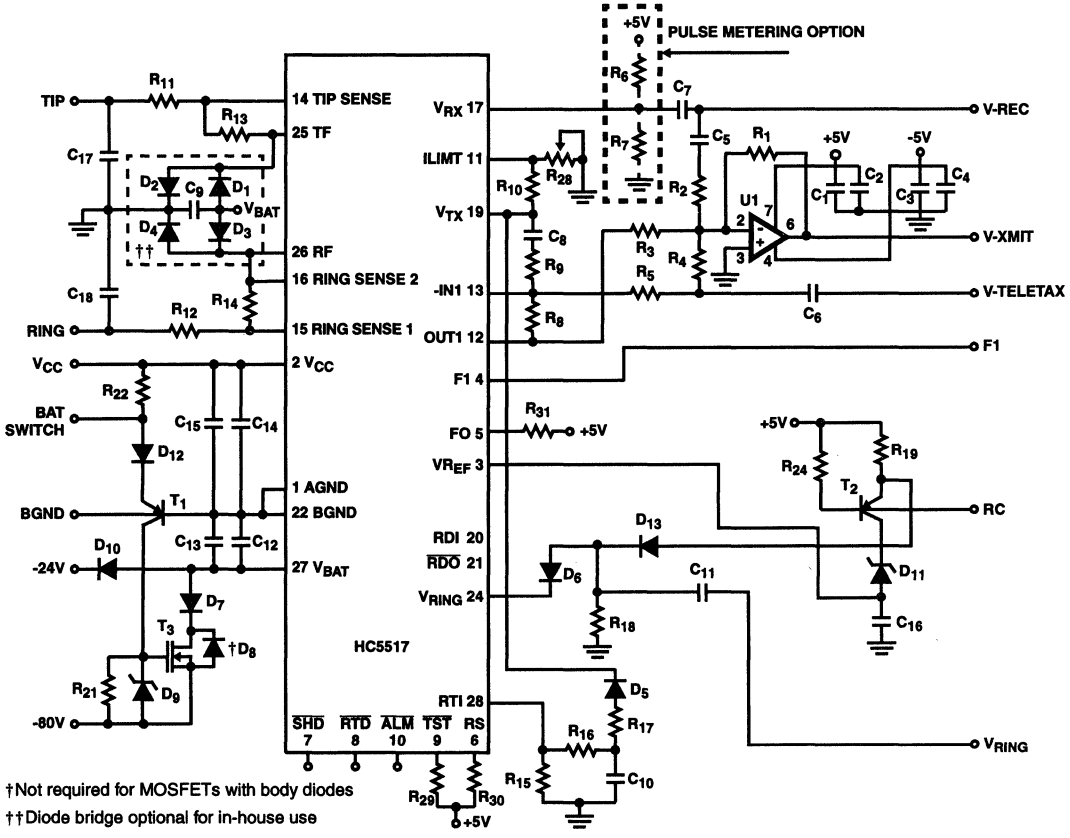
HC5517 (PLCC)
TOP VIEW



HC5517 (SOIC)
TOP VIEW



Applications Circuit



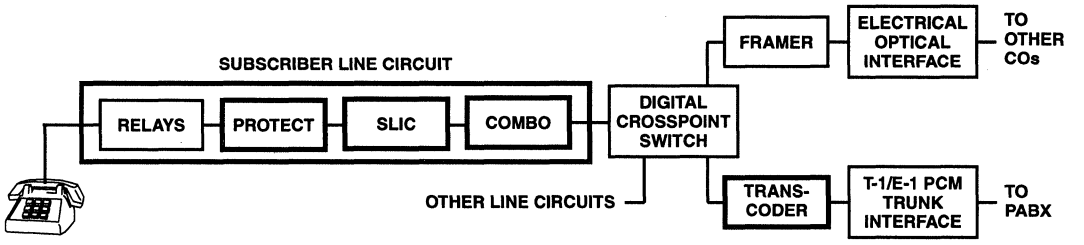
†Not required for MOSFETs with body diodes
††Diode bridge optional for in-house use

FIGURE 15. APPLICATION CIRCUIT

HC5517EVAL Evaluation Board Parts List

COMPONENT	VALUE	TOLERANCE	RATING	COMPONENT	VALUE	TOLERANCE	RATING
SLIC	HC5517	n/a	n/a	C_2, C_4, C_{15}	0.1µF	20%	50V
R_1, R_2	24.9kΩ	1%	1/4W	C_5, C_7	10µF	20%	20V
R_3	8.25kΩ	1%	1/4W	C_6, C_8	0.47µF	20%	20V
R_4	12.1kΩ	1%	1/4W	C_9, C_{12}	0.01µF	20%	100V
R_5, R_8, R_9	40kΩ	1%	1/4W	C_{10}	1.0µF	20%	50V
R_6 (not provided)	23.2kΩ	1%	1/4W	C_{11}	100µF	20%	5V
R_7 (not provided)	10kΩ	1%	1/4W	C_{13}	0.1µF	20%	100V
R_{10}	100kΩ	5%	1/4W	C_{16}	0.5µF	20%	50V
R_{11-14}	50Ω	1%	1/4W	C_{17},C_{18}	3300pF	20%	100V
R_{15}	47kΩ	1%	1/4W	D_{1-4}, D_7, D_8, D_{10}	1N4007		100V, 1A
R_{16}	1.5MΩ	1%	1/4W	D_5, D_6,D_{12}, D_{13}	1N914		100V, 1A
R_{17}	56.2kΩ	1%	1/4W	D_9	1N4744		15V, 1W
R_{18}	1.1kΩ	1%	1/4W	D_{11}	1N5255		28V, 1/2-Wire
R_{19}	825Ω	1%	1/4W	T_1	NTE 383		100V, 1A
R_{22}, R_{29}, R_{30}, R_{31}	10kΩ	5%	1/4W	T_2	2N2907		60V,150mA
R_{24}	47kΩ	5%	1/4W	T_3	RFP2N10 or equivalent		100V, 2A
R_{25-27}	560Ω	5%	1/4W	F1, RC, BATTERY	SPDT Toggle switches, center off.		
R_{28}	20kΩ Potentiometer		1/4W	U1	CA741C OpAmp		
R_{21}	47kΩ	5%	1/4W	Textool Socket	228-5523		
C_1, C_3, C_{14}	0.01µF	20%	50V				

CENTRAL OFFICE SWITCH



	USA	ROW
SLICs	HC5523 HC5513 (Note)	HC5519 HC5520 HC5521 HC5526 HC5515 HC-5509B
COMBOs	CD22354A	CD22357A
Transcoder	HC5560	CD22103A
Protection	SGT06U13	SGT06U13

NOTE: When used in fiber loop carrier applications.

HARRIS SEMICONDUCTOR

HC5519

ADVANCE INFORMATION

January 1997

SLIC
Subscriber Line Interface Circuit

Features

- **Complete A-Law Codec, Filter, and SLIC Functions with Serial Digital Control and Status Monitoring**
- **30mA Current Limit on Normal or Reverse Loop Feed**
- **Constant Voltage (Resistance) Feed on Long Loops**
- **On-Hook Transmission**
- **Switch Hook Detection**
- **User Selectable 2-Wire Complex Impedance**
- **User Selectable Receive Gain**
- **User Selectable Transmit Gain**
- **Ringing, Test-In, and Test-Out Relay Drivers**
- **Zero Crossing Ring Trip Detection and Ring Relay Release**
- **Thermal Shutdown Protection**
- **Meets CCITT/China Transmission Requirements**

Applications

- **CO/PABX Line Circuits**

Description

The HC5519 SLIC is designed to meet the technical requirements of the China Telecommunications network. It provides many of the BORSCHT functions associated with a Central Office line circuit.

The HC5519 consists of an A-Law Codec/Filter, a 2-wire interface circuit, an impedance control circuit, a ringing control circuit, a power management circuit, and a serial control interface circuit which is used to program and monitor the operation of the device.

The integration of the line interface and coder/decoder functions into a 80 pin MQFP surface mount package and standard value surface mount components avoids the need for costly hybrid packaging techniques and offers the superior reliability of an integrated solution for dense circuit board layouts.

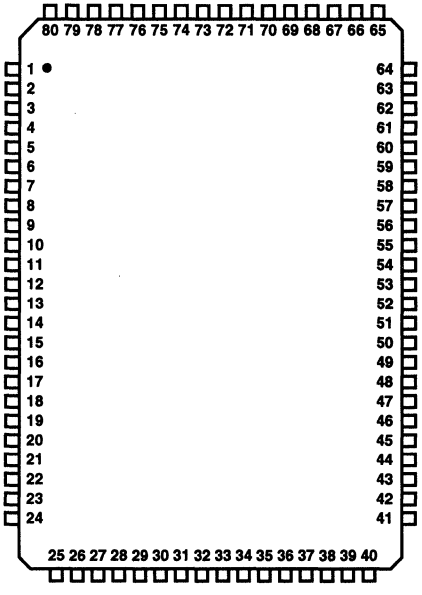
The SLIC combines Harris' patented Bonded Wafer Dielectrically Isolated fabrication techniques with a state of the art CMOS process to produce the world's most compact line circuit signal processing solution.

Ordering Information

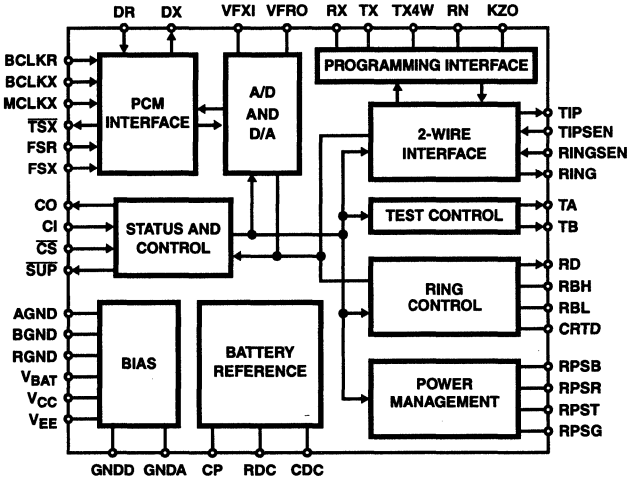
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC5519CQ	0 to 70	80 Ld MQFP	Q80.14x20

Pinout

HC5519 (MQFP)
TOP VIEW



Block Diagram



4 WIRED COMMUNICATIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4232**

HARRIS SEMICONDUCTOR

HC5520

ADVANCE INFORMATION

January 1997

SLIC
Subscriber Line Interface Circuit

Features

- Normal and Reversed DC Feed
- 30mA Current Limit
- Ringing, Test-In, and Test-Out Relay Drivers
- Thermal Shutdown Protection with Alert Signal
- On-Hook Transmission
- Selectable Transmit and Receive Gain Setting
- Selectable 2-Wire Impedance Matching
- Zero Crossing Ring Trip Detection and Ring Relay Release
- Parallel Digital Control and Status Monitoring
- Protection Resistors Inside Feedback Loop Allows the Use of PTC Devices Without Impact on Longitudinal Balance

Applications

- PABX/CO Line Circuits

Description

The HC5520 is a Monolithic Subscriber Line Interface Circuit (SLIC) for Analog Subscriber Line cards in Central Office and PABX switches.

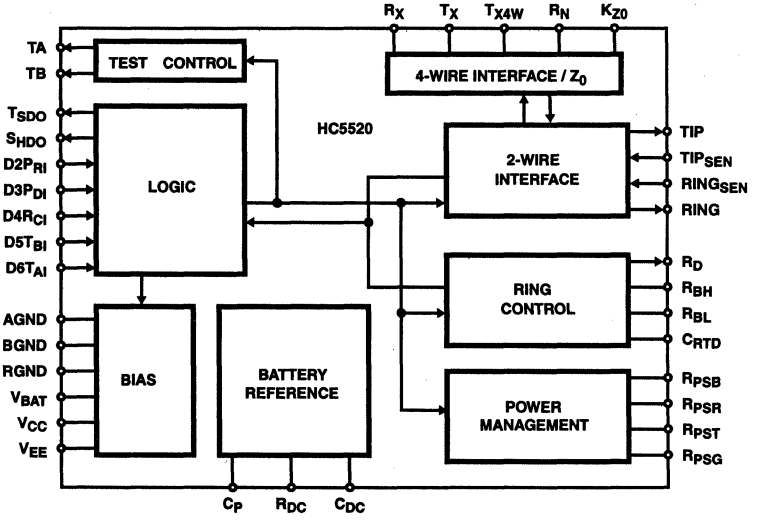
The HC5520 provides a comprehensive set of features for these applications including loop reversal, zero crossing ringing relay operation, long loop drive and a mutually independent setting of the receive and transmit gains, and the two wire impedance synthesis. An option is also provided for eliminating transhybrid balance on-chip. Advanced power management features combined with a small 44 lead MQFP package allow significant board space to be freed up for additional line circuits.

The HC5520 is fabricated in a Harris state-of-the-art Bonded Wafer High Voltage process, providing freedom from traditional JI latch-up phenomena without the use of additional power supply filtering components or substrate tie connections. The very low parasitics and leakages associated with this process provide an exceptionally flat performance over frequency and temperature.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC5520CQ	0 to 70	44 Ld MQFP	Q44.10x10
HC5520CM	0 to 70	44 Ld PLCC	N44.65

Block Diagram



File Number **4148**

HARRIS SEMICONDUCTOR

HC5521

ADVANCE INFORMATION

January 1997

SLIC
Subscriber Line Interface Circuit

Features

- Normal and Reversed DC Feed
- 30mA Current Limit
- Ringing, Test-In, and Test-Out Relay Drivers
- Ground Key Detector with Seperate Logic Output
- Thermal Shutdown Protection with Alert Signal
- On-Hook Transmission
- Selectable Transmit and Receive Gain Setting
- Selectable 2-Wire Impedance Matching
- Zero Crossing Ring Trip Detection and Ring Relay Release
- Parallel Digital Control and Status Monitoring
- Protection Resistors inside Feedback Loop allows the use of PTC Devices without Impact on Longitudinal Balance

Applications

- PABX/CO Line Circuits

Description

The HC5521 is a Monolithic Subscriber Line Interface Circuit (SLIC) for Analog Subscriber Line cards in Central Office and PABX switches.

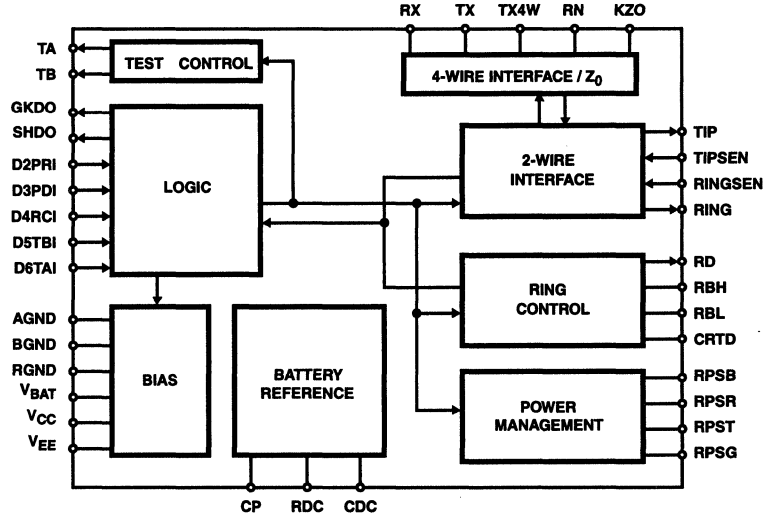
The HC5521 provides a comprehensive set of features for these applications including loop reversal, ground key detection, zero crossing ring relay operation, long loop drive and a mutually independent setting of the receive and transmit gains, and the two-wire impedance synthesis. An option is also provided for eliminating transhybrid balance on-chip. Advanced power management features combined with a small 44 lead MQFP package allow significant board space to be freed up for additional line circuits.

The HC5521 is fabricated in a Harris state of the art Bonded Wafer High Voltage process, providing freedom from traditional JI latch-up phenomena without the use of additional power supply filtering components or substrate tie connections. The very low parasitics and leakages associated with this process provide an exceptionally flat performance over frequency and temperature.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HC5521CQ	0 to 70	44 Ld MQFP	Q44.10x10
HC5521CM	0 to 70	44 Ld PLCC	N44.65

Block Diagram



4 WIRED COMMUNICATIONS

File Number **4265**

HARRIS SEMICONDUCTOR

HC5513

SLIC
Subscriber Line Interface Circuit

January 1997

Features

- DI Monolithic High Voltage Process
- Programmable Current Feed (20mA to 60mA)
- Programmable Loop Current Detector Threshold and Battery Feed Characteristics
- Ground Key and Ring Trip Detection
- Compatible with Ericsson's PBL3764
- Thermal Shutdown
- On-Hook Transmission
- Wide Battery Voltage Range (-24V to -58V)
- Low Standby Power
- Meets TR-NWT-000057 Transmission Requirements
- -40°C to 85°C Ambient Temperature Range

Applications

- Digital Loop Carrier Systems
- Fiber-In-The-Loop ONUs
- Wireless Local Loop
- Hybrid Fiber Coax
- Pair Gain
- POTS
- PABX
- Related Literature
  - AN9537, Operation of the HC5513/26 Evaluation Board

Description

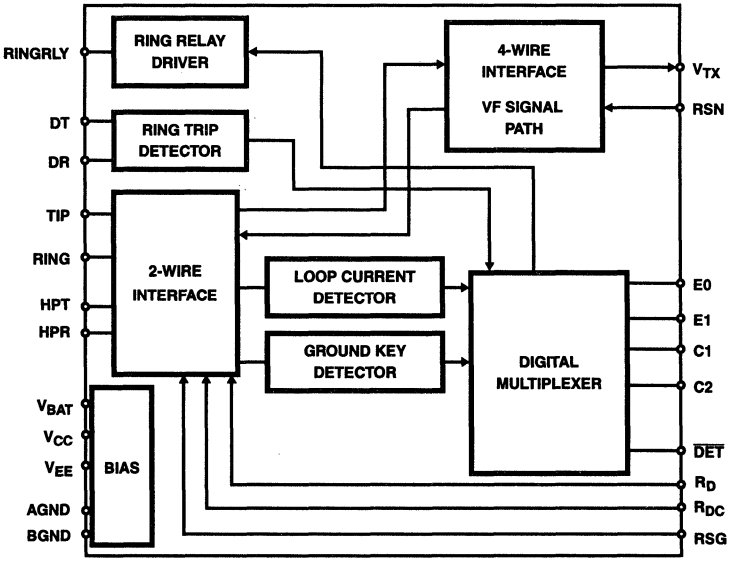
The HC5513 is a subscriber line interface circuit which is interchangeable with Ericsson's PBL3764 for distributed central office applications. Enhancements include immunity to circuit latch-up during hot plug and absence of false signaling in the presence of longitudinal currents.

The HC5513 is fabricated in a High Voltage Dielectrically Isolated (DI) Bipolar Process that eliminates leakage currents and device latch-up problems normally associated with Junction Isolated (JI) ICs. The elimination of the leakage currents results in improved circuit performance for wide temperature extremes. The latch free benefit of the DI process guarantees operation under adverse transient conditions. This process feature makes the HC5513 ideally suited for use in harsh outdoor environments.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC5513BIM	-40 to 85	28 Ld PLCC	N28.45
HC5513BIP	-40 to 85	22 Ld PDIP	E22.4

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3963.7**

Absolute Maximum Ratings

Operating Temperature Range . . . . . -40°C to 110°C
Power Supply (-40°C ≤ T_A ≤ 85°C)
  Supply Voltage V_{CC} to GND . . . . . 0.5V to 7V
  Supply Voltage V_{EE} to GND . . . . . -7V to 0.5V
  Supply Voltage V_{BAT} to GND . . . . . -70V to 0.5V
Ground
  Voltage between AGND and BGND . . . . . -0.3V to 0.3V
Relay Driver
  Ring Relay Supply Voltage . . . . . 0V to V_{BAT} 75V
  Ring Relay Current 50mA
Ring Trip Comparator
  Input Voltage . . . . . V_{BAT} to 0V
  Input Current . . . . . -5mA to 5mA
Digital Inputs, Outputs (C1, C2, E0, E1, $\overline{DET}$)
  Input Voltage . . . . . 0V to V_{CC}
  Output Voltage ($\overline{DET}$ Not Active) . . . . . 0V to V_{CC}
  Output Current ($\overline{DET}$) 5mA
Tipx and Ringx Terminals (-40°C ≤ T_A ≤ 85°C)
  Tipx or Ringx Voltage, Continuous (Referenced to GND) . V_{BAT} to 2V
  Tipx or Ringx, Pulse < 10ms, T_{REP} > 10s . . . . . V_{BAT} -20V to 5V
  Tipx or Ringx, Pulse < 10µs, T_{REP} > 10s . . . . . V_{BAT} -40V to 10V
  Tipx or Ringx, Pulse < 250ns, T_{REP} > 10s . . . . V_{BAT} -70V to 15V
  Tipx or Ringx Current 70mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}°C/W
22 Lead PDIP Package	53
28 Lead PLCC Package	53

Continuous Dissipation at 70°C
  22 Lead PDIP Package 1.5W
  28 Lead PLCC Package 1.5W
Package Power Dissipation at 70°C, t < 100ms, t_{REP} > 1s
  22 Lead PDIP Package 4W
  28 Lead PLCC Package 4W
Derate above . . . . . 70°C
  Plastic DIP Package . . . . . 18.8mW/°C
  PLCC Package . . . . . 18.8mW/°C
Maximum Junction Temperature Range . . . . . -40°C to 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 543 Transistors, 51 Diodes

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Typical Operating Conditions

These represent the conditions under which the part was developed and are suggested as guidelines.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Case Temperature		-40	-	100	°C
V_{CC} with Respect to AGND	-40°C to 85°C	4.75	-	5.25	V
V_{EE} with Respect to AGND	-40°C to 85°C	-5.25	-	-4.75	V
V_{BAT} with Respect to BGND	-40°C to 85°C	-58	-	-24	V

Electrical Specifications

T_A = -40°C to 85°C, V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Overload Level	1% THD, Z_L = 600Ω, (Note 2, Figure 1)	3.1	-	-	V_{PEAK}
Longitudinal Impedance (Tip/Ring)	0 < f < 100Hz (Note 3, Figure 2)	-	20	35	Ω/Wire

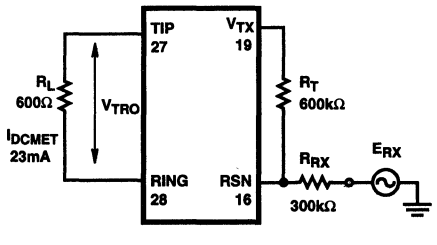


FIGURE 1. OVERLOAD LEVEL (TWO-WIRE PORT)

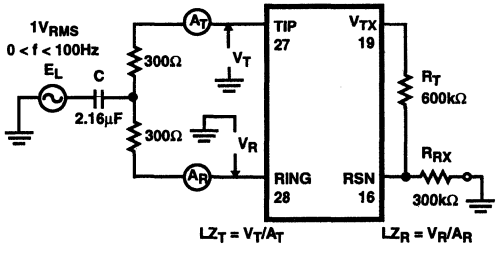


FIGURE 2. LONGITUDINAL IMPEDANCE

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LONGITUDINAL CURRENT LIMIT (TIP/RING)					
Off-Hook (Active)	No False Detections, (Loop Current), LB > 45dB (Note 4, Figure 3A)	-	-	20	mA_{PEAK}/ Wire
On-Hook (Standby), R_L = ∞	No False Detections (Loop Current) (Note 5, Figure 3B)	-	-	5	mA_{PEAK}/ Wire

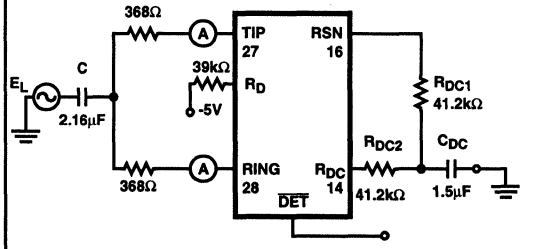


FIGURE 3A. OFF-HOOK

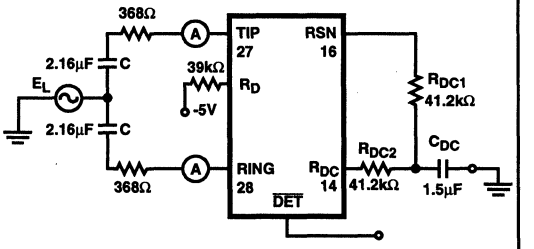


FIGURE 3B. ON-HOOK

FIGURE 3. LONGITUDINAL CURRENT LIMIT

OFF-HOOK LONGITUDINAL BALANCE					
Longitudinal to Metallic	IEEE 455 - 1985, R_{LR}, R_{LT} = 368Ω 0.2kHz < f < 4.0kHz (Note 6, Figure 4)	55	70	-	dB
Longitudinal to Metallic	R_{LR}, R_{LT} = 300Ω, 0.2kHz < f < 4.0kHz (Note 6, Figure 4)	55	70	-	dB
Metallic to Longitudinal	FCC Part 68, Para 68.310 0.2kHz < f < 1.0kHz	50	55	-	dB
	1.0kHz < f < 4.0kHz (Note 7)	50	55	-	dB
Longitudinal to 4-Wire	0.2kHz < f < 4.0kHz (Note 8, Figure 4)	55	70	-	dB
Metallic to Longitudinal	R_{LR}, R_{LT} = 300Ω, 0.2kHz < f < 4.0kHz (Note 9, Figure 5)	50	55	-	dB
4-Wire to Longitudinal	0.2kHz < f < 4.0kHz (Note 10, Figure 5)	50	55	-	dB

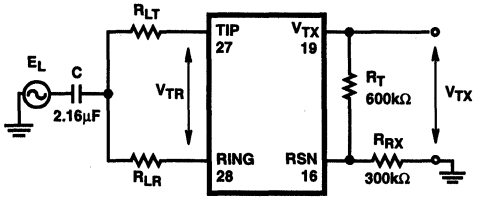


FIGURE 4. LONGITUDINAL TO METALLIC AND LONGITUDINAL TO 4-WIRE BALANCE

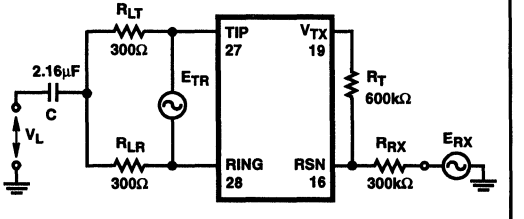


FIGURE 5. METALLIC TO LONGITUDINAL AND 4-WIRE TO LONGITUDINAL BALANCE

2-Wire Return Loss C_{HP} = 20nF	0.2kHz to 0.5kHz (Note 11, Figure 6)	25	-	-	dB
	0.5kHz to 1.0kHz (Note 11, Figure 6)	27	-	-	dB
	1.0kHz to 3.4kHz (Note 11, Figure 6)	23	-	-	dB

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TIP IDLE VOLTAGE					
Active, I_L = 0		-	-4	-	V
Standby, I_L = 0		-	<0	-	V
RING IDLE VOLTAGE					
Active, I_L = 0		-	-24	-	V
Standby, I_L = 0		-	>-28	-	V
4-WIRE TRANSMIT PORT (V_{TX})					
Overload Level	(Z_L > 20kΩ, 1% THD) (Note 12, Figure 7)	3.1	-	-	V_{PEAK}
Output Offset Voltage	E_G = 0, Z_L = ∞, (Note 13, Figure 7)	-60	-	60	mV
Output Impedance (Guaranteed by Design)	0.2kHz < f < 03.4kHz	-	5	20	Ω
2- to 4-Wire (Metallic to V_{TX}) Voltage Gain	0.3kHz < f < 03.4kHz (Note 14, Figure 7)	0.98	1.0	1.02	V/V

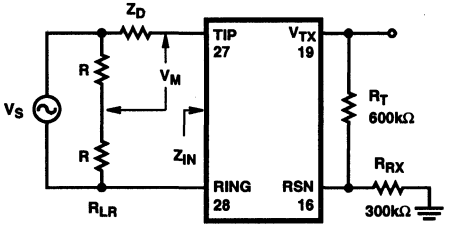


FIGURE 6. TWO-WIRE RETURN LOSS

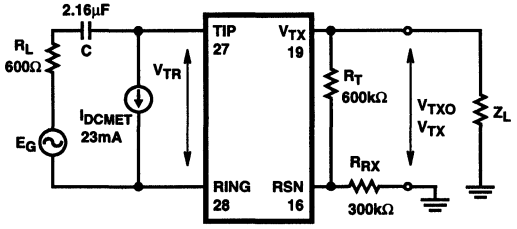


FIGURE 7. OVERLOAD LEVEL (4-WIRE TRANSMIT PORT), OUTPUT OFFSET VOLTAGE, 2-WIRE TO 4-WIRE VOLTAGE GAIN AND HARMONIC DISTORTION

4-WIRE RECEIVE PORT (RSN)					
DC Voltage	I_{RSN} = 0mA	-	0	-	V
R_X Sum Node Impedance (Guaranteed by Design)	0.3kHz < f < 3.4kHz	-	-	20	Ω
Current Gain-RSN to Metallic	0.3kHz < f < 3.4kHz (Note 15, Figure 8)	980	1000	1020	Ratio
FREQUENCY RESPONSE (OFF-HOOK)					
2-Wire to 4-Wire	0dBm at 1.0kHz, E_{RX} = 0V 0.3kHz < f < 3.4kHz (Note 16, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm at 1.0kHz, E_G = 0V 0.3kHz < f < 3.4kHz (Note 17, Figure 9)	-0.2	-	0.2	dB
4-Wire to 4-Wire	0dBm at 1.0kHz, E_G = 0V 0.3kHz < f < 3.4kHz (Note 18, Figure 9)	-0.2	-	0.2	dB
INSERTION LOSS					
2-Wire to 4-Wire	0dBm, 1kHz (Note 19, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm, 1kHz (Note 20, Figure 9)	-0.2	-	0.2	dB
GAIN TRACKING (Ref = -10dBm, at 1.0kHz)					
2-Wire to 4-Wire	-40dBm to +3dBm (Note 21, Figure 9)	-0.1	-	0.1	dB
2-Wire to 4-Wire	-55dBm to -40dBm (Note 21, Figure 9)	-	±0.03	-	dB

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
4-Wire to 2-Wire	-40dBm to +3dBm (Note 22, Figure 9)	-0.1	-	0.1	dB
4-Wire to 2-Wire	-55dBm to -40dBm (Note 22, Figure 9)	-	±0.03	-	dB

GRX = $((V_{TR1} - V_{TR2})(300k))/(-3)(600)$

Where: V_{TR1} is the Tip to Ring Voltage with V_{RSN} = 0V
and V_{TR2} is the Tip to Ring Voltage with V_{RSN} = -3V

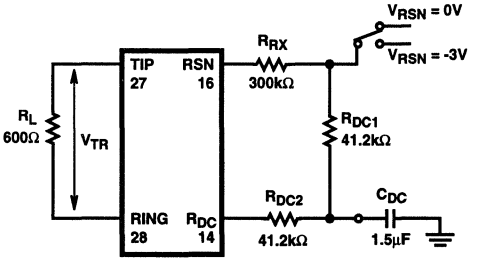


FIGURE 8. CURRENT GAIN-RSN TO METALLIC

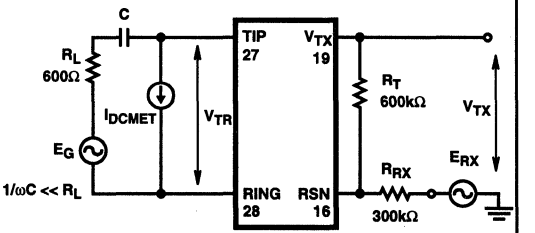
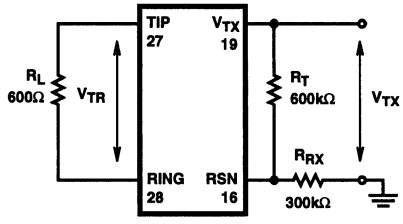
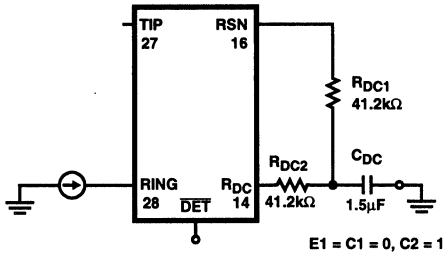


FIGURE 9. FREQUENCY RESPONSE, INSERTION LOSS, GAIN TRACKING AND HARMONIC DISTORTION

NOISE					
Idle Channel Noise at 2-Wire	C-Message Weighting (Note 23, Figure 10)	-	12	-	dBrnC
Idle Channel Noise at 4-Wire	C-Message Weighting (Note 24, Figure 10)	-	12	-	dBrnC
HARMONIC DISTORTION					
2-Wire to 4-Wire	0dBm, 1kHz (Note 25, Figure 7)	-	-65	-54	dB
4-Wire to 2-Wire	0dBm, 0.3kHz to 3.4kHz (Note 26, Figure 9)	-	-65	-54	dB
BATTERY FEED CHARACTERISTICS					
Constant Loop Current Tolerance R_{DCX} = 41.2kΩ	$I_L = 2500/(R_{DC1} + R_{DC2})$, -40°C to 85°C (Note 27)	$0.9I_L$	I_L	$1.1I_L$	mA
Loop Current Tolerance (Standby)	$I_L = (V_{BAT}-3)/(R_L +1800)$, -40°C to 85°C (Note 28)	$0.8I_L$	I_L	$1.2I_L$	mA
Open Circuit Voltage (V_{TIP} - V_{RING})	-40°C to 85°C, (Active)	14	-	20	V
LOOP CURRENT DETECTOR					
On-Hook to Off-Hook	R_D = 39kΩ, -40°C to 85°C	$372/R_D$	$465/R_D$	$558/R_D$	mA
Off-Hook to On-Hook	R_D = 39kΩ, -40°C to 85°C	$325/R_D$	$405/R_D$	$485/R_D$	mA
Loop Current Hysteresis	R_D = 39kΩ, -40°C to 85°C	$25/R_D$	$60/R_D$	$95/R_D$	mA
GROUND KEY DETECTOR					
Tip/Ring Current Difference - Trigger	(Note 29, Figure 11)	8	12	17	mA
Tip/Ring Current Difference - Reset	(Note 29, Figure 11)	3	7	12	mA
Hysteresis	(Note 29, Figure 11)	0	5	9	mA

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
 FIGURE 10. IDLE CHANNEL NOISE					
 FIGURE 11. GROUND KEY DETECT					
RING TRIP DETECTOR (DT, DR)					
Offset Voltage	Source Res = 0	-20	-	20	mV
Input Bias Current	Source Res = 0	-500	-	500	nA
Input Common-Mode Range	Source Res = 0	V_{BAT} +1	-	0	V
Input Resistance	Source Res = 0, Balanced	3	-	-	MΩ
RING RELAY DRIVER					
V_{SAT} at 25mA	I_{OL} = 25mA	-	1.0	1.5	V
Off-State Leakage Current	V_{OH} = 12V	-	-	10	µA
DIGITAL INPUTS (E0, E1, C1, C2)					
Input Low Voltage, V_{IL}		0	-	0.8	V
Input High Voltage, V_{IH}		2	-	V_{CC}	V
Input Low Current, I_{IL}: C1, C2	V_{IL} = 0.4V	-200	-	-	µA
Input Low Current, I_{IL}: E0, E1	V_{IL} = 0.4V	-100	-	-	µA
Input High Current	V_{IH} = 2.4V	-	-	40	µA
DETECTOR OUTPUT ($\overline{DET}$)					
Output Low Voltage, V_{OL}	I_{OL} = 2mA	-	-	0.45	V
Output High Voltage, V_{OH}	I_{OH} = 100µA	2.7	-	-	V
Internal Pull-Up Resistor		10	15	20	kΩ
POWER DISSIPATION					
Open Circuit State	C1 = C2 = 0	-	-	23	mW
On-Hook, Standby	C1 = C2 = 1	-	-	30	mW
On-Hook, Active	C1 = 0, C2 = 1, R_L = High Impedance	-	-	150	mW
Off-Hook, Active	R_L = 0Ω	-	-	1.1	W
	R_L = 300Ω	-	-	0.75	W
	R_L = 600Ω	-	-	0.5	W
TEMPERATURE GUARD					
Thermal Shutdown		150	-	180	°C

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENTS (V_{BAT} = -28V)					
I_{CC}, On-Hook	Open Circuit State (C1, 2 = 0, 0)	-	-	1.5	mA
	Standby State (C1, 2 = 1, 1)	-	-	1.7	mA
	Active State (C1, 2 = 0,1)	-	-	5.5	mA
I_{EE}, On-Hook	Open Circuit State (C1, 2 = 0, 0)	-	-	0.8	mA
	Standby State (C1, 2 = 1, 1)	-	-	0.8	mA
	Active State (C1, 2 = 0, 1)	-	-	2.2	mA
I_{BAT}, On-Hook	Open Circuit State (C1, 2 = 0, 0)	-	-	0.4	mA
	Standby State (C1, 2 = 1, 1)	-	-	0.6	mA
	Active State (C1, 2 = 0, 1)	-	-	3.9	mA
PSRR					
V_{CC} to 2 or 4-Wire Port	(Note 30, Figure 12)	-	40	-	dB
V_{EE} to 2 or 4-Wire Port	(Note 30, Figure 12)	-	40	-	dB
V_{BAT} to 2 or 4-Wire Port	(Note 30, Figure 12)	-	40	-	dB

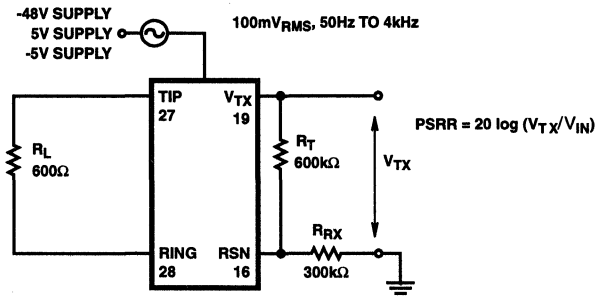


FIGURE 12. POWER SUPPLY REJECTION RATIO

Circuit Operation and Design Information

The HC5513 is a current feed voltage sense Subscriber Line Interface Circuit (SLIC). This means that for short loop applications the SLIC provides a programed constant current to the tip and ring terminals while sensing the tip to ring voltage.

The following discussion separates the SLIC's operation into its DC and AC path, then follows up with additional circuit and design information.

Constant Loop Current (DC) Path

SLIC in the Active Mode

The DC path establishes a constant loop current that flows out of tip and into the ring terminal. The loop current is programmed by resistors R_{DC1}, R_{DC2} and the voltage on the R_{DC} pin (Figure 13). The R_{DC} voltage is determined by the voltage across R_1 in the saturation guard circuit. Under

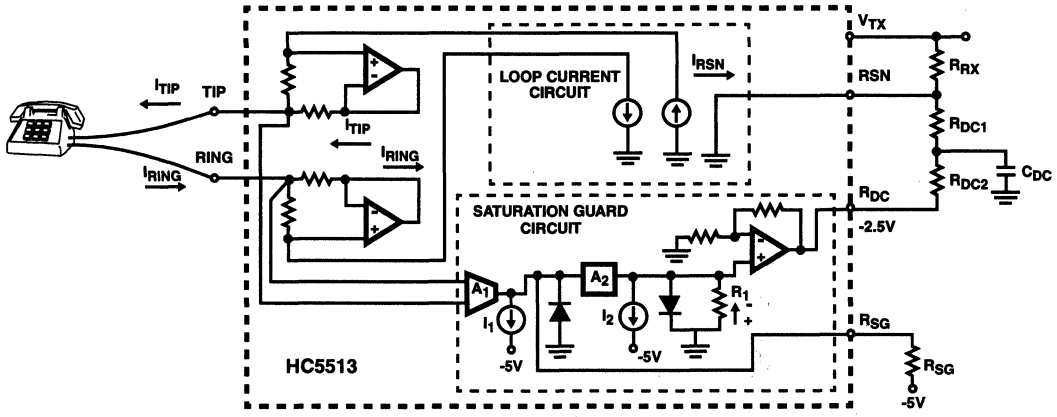


FIGURE 13. DC LOOP CURRENT

constant current feed conditions, the voltage drop across R_1 sets the R_{DC} voltage to -2.5V. This occurs when current flows through R_1 into the current source I_2. The R_{DC} voltage establishes a current (I_{RSN}) that is equal to $V_{RDC}/(R_{DC1}+R_{DC2})$. This current is then multiplied by 1000, in the loop current circuit, to become the tip and ring loop currents.

For the purpose of the following discussion, the saturation guard voltage is defined as the maximum tip to ring voltage at which the SLIC can provide a constant current for a given battery and overhead voltage.

For loop resistances that result in a tip to ring voltage less than the saturation guard voltage the loop current is defined as:

$$I_L = \frac{2.5V}{R_{DC1}+R_{DC2}} \times 1000 \qquad \text{(EQ. 1)}$$

where: I_L = Constant loop current.

R_{DC1} and R_{DC2} = Loop current programming resistors.

Capacitor C_{DC} between R_{DC1} and R_{DC2} removes the VF signals from the battery feed control loop. The value of C_{DC} is determined by Equation 2:

$$C_{DC} = T \times \left(\frac{1}{R_{DC1}} + \frac{1}{R_{DC2}}\right) \qquad \text{(EQ. 2)}$$

where T = 30ms

NOTE: The minimum C_{DC} value is obtained if $R_{DC1} = R_{DC2}$

Figure 14 illustrates the relationship between the tip to ring voltage and the loop resistance. For a 0Ω loop resistance both tip and ring are at $V_{BAT}/2$. As the loop resistance increases, so does the voltage differential between tip and ring. When this differential voltage becomes equal to the saturation guard voltage, the operation of the SLIC's loop feed changes from a constant current feed to a resistive feed. The loop current in the resistive feed region is no longer constant but varies as a function of the loop resistance.

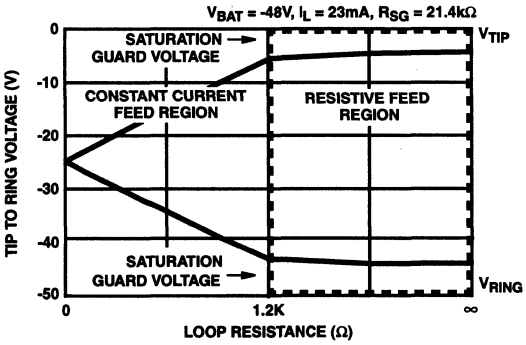
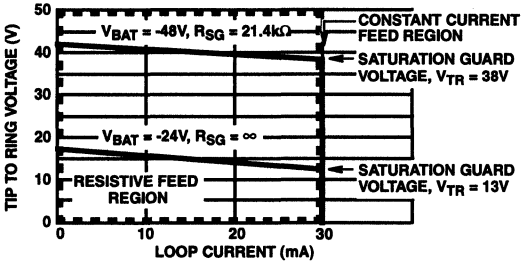


FIGURE 14. V_{TR} vs R_L

Figure 15 shows the relationship between the saturation guard voltage, the loop current and the loop resistance. Notice from Figure 15 that for a loop resistance <1.2kΩ (R_{SG} = 21.4kΩ) the SLIC is operating in the constant current feed region and for resistances >1.2kΩ the SLIC is operating in the resistive feed region. Operation in the resistive feed region allows long loop and off-hook transmission by keeping the tip and ring voltages off the rails. Operation in this region is transparent to the customer.



R_L	100kΩ	4kΩ	2kΩ	<1.2kΩ	R_{RSG} = 21.4kΩ
R_L	100kΩ	1.5kΩ	700Ω	<400Ω	R_{RSG} = ∞Ω

FIGURE 15. V_{TR} vs I_L and R_L

The Saturation Guard circuit (Figure 13) monitors the tip to ring voltage via the transconductance amplifier A_1. A_1 generates a current that is proportional to the tip to ring voltage difference. I_1 is internally set to sink all of A_1's current until the tip to ring voltage exceeds 12.5V. When the tip to ring voltage exceeds 12.5V (with no R_{SG} resistor) A_1 supplies more current than I_1 can sink. When this happens A_2 amplifies its input current by a factor of 12 and the current through R_1 becomes the difference between I_2 and the output current from A_2. As the current from A_2 increases, the voltage across R_1 decreases and the output voltage on R_{DC} decreases. This results in a corresponding decrease in the loop current. The R_{SG} pin provides the ability to increase the saturation guard reference voltage beyond 12.5V. Equation 3 gives the relationship between the R_{SG} resistor value and the programmable saturation guard reference voltage:

$$V_{SGREF} = 12.5 + \frac{5 \bullet 10^5}{R_{SG}} \quad \text{(EQ. 3)}$$

where:

V_{SGREF} = Saturation Guard reference voltage.

R_{SG} = Saturation Guard programming resistor.

When the Saturation guard reference voltage is exceeded, the tip to ring voltage is calculated using Equation 4:

$$V_{TR} = R_L \times \frac{16.66 + 5 \bullet 10^5 / R_{SG}}{R_L + (R_{DC1} + R_{DC2})/600} \quad \text{(EQ. 4)}$$

where:

V_{TR} = Voltage differential between tip and ring.

R_L = Loop resistance.

For on-hook transmission $R_L = \infty$, Equation 4 reduces to:

$$V_{TR} = 16.66 + \frac{5 \bullet 10^5}{R_{SG}} \quad \text{(EQ. 5)}$$

The value of R_{SG} should be calculated to allow maximum loop length operation. This requires that the saturation guard reference voltage be set as high as possible without clipping the incoming or outgoing VF signal. A voltage margin of -4V on tip and -4V on ring, for a total of -8V margin, is recommended as a general guideline. The value of R_{SG} is calculated using Equation 6:

$$R_{SG} = \frac{5 \bullet 10^5}{(|V_{BAT}| - V_{MARGIN}) \times \left(1 + \frac{(R_{DC1} + R_{DC2})}{600 R_L}\right) - 16.66V} \quad \text{(EQ. 6)}$$

where:

V_{BAT} = Battery voltage.

V_{MARGIN} = Recommended value of -8V to allow a maximum overload level of 3.1V peak.

For on-hook transmission $R_L = \infty$, Equation 6 reduces to:

$$R_{SG} = \frac{5 \bullet 10^5}{|V_{BAT}| - V_{MARGIN} - 16.66V} \quad \text{(EQ. 7)}$$

SLIC in the Standby Mode

Overall system power is saved by configuring the SLIC in the standby state when not in use. In the standby state the tip and ring amplifiers are disabled and internal resistors are connected between tip to ground and ring to V_{BAT}. This connection enables a loop current to flow when the phone goes off-hook. The loop current detector then detects this current and the SLIC is configured in the active mode for voice transmission. The loop current in standby state is calculated as follows:

$$I_L \approx \frac{|V_{BAT}| - 3V}{R_L + 1800\Omega} \quad \text{(EQ. 8)}$$

where:

I_L = Loop current in the standby state.

R_L = Loop resistance.

V_{BAT} = Battery voltage.

(AC) Transmission Path

SLIC in the Active Mode

Figure 16 shows a simplified AC transmission model. Circuit analysis yields the following design equations:

$$V_{TR} = V_{TX} + I_M \bullet 2R_F \quad \text{(EQ. 9)}$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_M}{1000} \quad \text{(EQ. 10)}$$

$$V_{TR} = E_G - I_M \bullet Z_L \quad \text{(EQ. 11)}$$

where:

V_{TR} = Is the AC metallic voltage between tip and ring, including the voltage drop across the fuse resistors R_F.

V_{TX} = Is the AC metallic voltage. Either at the ground referenced 4-wire side or the SLIC tip and ring terminals.

I_M = Is the AC metallic current.

R_F = Is a fuse resistor.

Z_T = Is used to set the SLIC's 2-wire impedance.

V_{RX} = Is the analog ground referenced receive signal.

Z_{RX} = Is used to set the 4-wire to 2-wire gain.

E_G = Is the AC open circuit voltage.

Z_L = Is the line impedance.

(AC) 2-Wire Impedance

The AC 2-wire impedance (Z_{TR}) is the impedance looking into the SLIC, including the fuse resistors, and is calculated as follows:

Let $V_{RX} = 0$. Then from Equation 10

$$V_{TX} = Z_T \bullet \frac{I_M}{1000} \quad \text{(EQ. 12)}$$

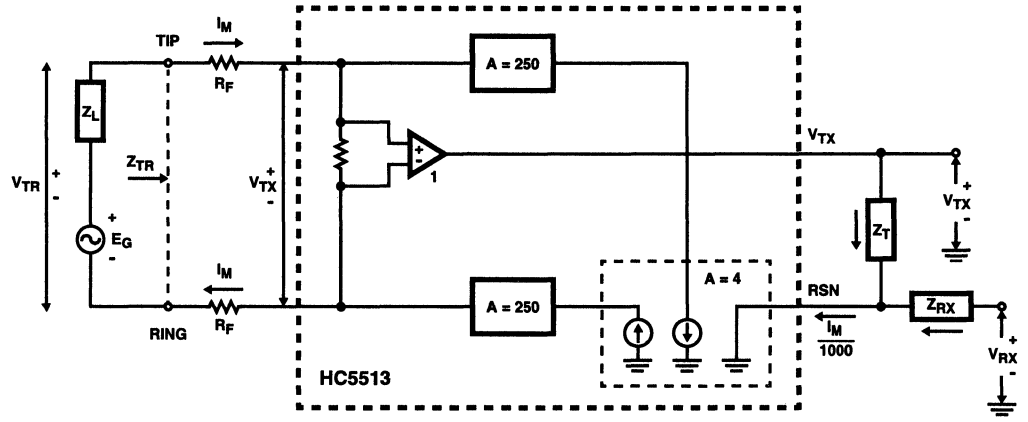


FIGURE 16. SIMPLIFIED AC TRANSMISSION CIRCUIT

Z_{TR} is defined as:

$$Z_{TR} = \frac{V_{TR}}{I_M} \quad \text{(EQ. 13)}$$

Substituting in Equation 9 for V_{TR}

$$Z_{TR} = \frac{V_{TX}}{I_M} + \frac{2R_F \bullet I_M}{I_M} \quad \text{(EQ. 14)}$$

Substituting in Equation 12 for V_{TX}

$$Z_{TR} = \frac{Z_T}{1000} + 2R_F \quad \text{(EQ. 15)}$$

Therefore

$$Z_T = 1000 \bullet (Z_{TR} - 2R_F) \quad \text{(EQ. 16)}$$

Equation 16 can now be used to match the SLIC's impedance to any known line impedance (Z_{TR}).

EXAMPLE:

Calculate Z_T to make $Z_{TR} = 600\Omega$ in series with 2.16µF. $R_F = 20\Omega$.

$$Z_T = 1000 \bullet \left(600 + \frac{1}{j\omega \bullet 2.16 \bullet 10^{-6}} - 2 \bullet 20\right)$$

$Z_T = 560k\Omega$ in series with 2.16nF

(AC) 2-Wire to 4-Wire Gain

The 2-wire to 4-wire gain is equal to V_{TX}/V_{TR}

From Equations 9 and 10 with $V_{RX} = 0$

$$A_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/1000}{Z_T/1000 + 2R_F} \quad \text{(EQ. 17)}$$

(AC) 4-Wire to 2-Wire Gain

The 4-wire to 2-wire gain is equal to V_{TR}/V_{RX}

From Equations 9, 10 and 11 with $E_G = 0$

$$A_{4-2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L}{\frac{Z_T}{1000} + 2R_F + Z_L} \quad \text{(EQ. 18)}$$

For applications where the 2-wire impedance (Z_{TR}, Equation 15) is chosen to equal the line impedance (Z_L), the expression for A_{4-2} simplifies to:

$$A_{4-2} = -\frac{Z_T}{Z_{RX}} \bullet \frac{1}{2} \quad \text{(EQ. 19)}$$

(AC) 4-Wire to 4-Wire Gain

The 4-wire to 4-wire gain is equal to V_{TX}/V_{RX}

From Equations 9, 10 and 11 with $E_G = 0$

$$A_{4-4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L + 2R_F}{\frac{Z_T}{1000} + 2R_F + Z_L} \quad \text{(EQ. 20)}$$

Transhybrid Circuit

The purpose of the transhybrid circuit is to remove the receive signal (V_{RX}) from the transmit signal (V_{TX}), thereby preventing an echo on the transmit side. This is accomplished by using an external op amp (usually part of the CODEC) and by the inversion of the signal from the 4-wire receive port (RSN) to the 4-wire transmit port (V_{TX}). Figure 17 shows the transhybrid circuit. The input signal will be subtracted from the output signal if I_1 equals I_2. Node analysis yields the following equation:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \quad \text{(EQ. 21)}$$

The value of Z_B is then

$$Z_B = -R_{TX} \bullet \frac{V_{RX}}{V_{TX}} \quad \text{(EQ. 22)}$$

Where V_{RX}/V_{TX} equals $1/A_{4-4}$

Therefore

$$Z_B = R_{TX} \bullet \frac{Z_{RX}}{Z_T} \bullet \frac{\frac{Z_T}{1000} + 2R_F + Z_L}{Z_L + 2R_F} \quad \text{(EQ. 23)}$$

Example:

Given: R_{TX} = 20kΩ, Z_{RX} = 280kΩ, Z_T = 562kΩ (standard value), R_F = 20Ω and Z_L = 600Ω

The value of Z_B = 18.7kΩ

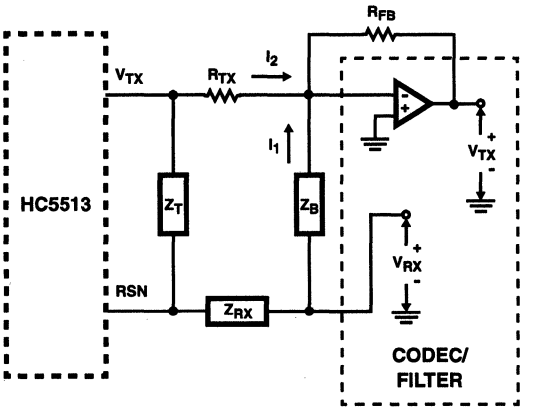


FIGURE 17. TRANSHYBRID CIRCUIT

Supervisory Functions

The loop current, ground key and the ring trip detector outputs are multiplexed to a single logic output pin called $\overline{DET}$. See Table 1 to determine the active detector for a given logic input. For further discussion of the logic circuitry see section titled "Digital Logic Inputs".

Before proceeding with an explanation of the loop current detector, ground key detector and later the longitudinal impedance, it is important to understand the difference between a "metallic" and "longitudinal" loop currents. Figure 18 illustrates 3 different types of loop current encountered.

Case 1 illustrates the metallic loop current. The definition of a metallic loop current is when **equal** currents flow out of tip and into ring. Loop current is a metallic current.

Cases 2 and 3 illustrate the longitudinal loop current. The definition of a longitudinal loop current is a common mode current, that flows either out of or into tip and ring simultaneously. Longitudinal currents in the on-hook state result in **equal** currents flowing through the sense resistors R_1 and R_2 (Figure 18). And longitudinal currents in the off-hook state result in **unequal** currents flowing through the sense resistors R_1 and R_2. Notice that for case 2, longitudinal currents flowing away from the SLIC, the current through R_1 is the metallic loop current plus the longitudinal current; whereas the current through R_2 is the metallic loop current minus the longitudinal current. Longitudinal currents are generated when the phone line is influenced by magnetic fields (e.g. power lines).

Loop Current Detector

Figure 18 shows a simplified schematic of the loop current and ground key detectors. The loop current detector works by sensing the metallic current flowing through resistors R_1 and R_2. This results in a current (I_{RD}) out of the transconductance amplifier (gm_1) that is equal to the product of gm_1 and the metallic loop current. I_{RD} then flows out the R_D pin and through resistor R_D to V_{EE}. The value of I_{RD} is equal to:

$$I_{RD} = \frac{|I_{TIP} - I_{RING}|}{600} = \frac{I_L}{300} \quad \text{(EQ. 24)}$$

The I_{RD} current results in a voltage drop across R_D that is compared to an internal 1.25V reference voltage. When the voltage drop across R_D exceeds 1.25V, and the logic is configured for loop current detection, the $\overline{DET}$ pin goes low.

The hysteresis resistor R_H adds an additional voltage effectively across R_D, causing the on-hook to off-hook threshold to be slightly higher than the off-hook to on-hook threshold.

Taking into account the hysteresis voltage, the typical value of R_D for the on-hook to off-hook condition is:

$$R_D = \frac{465}{I_{ON-HOOK\ to\ OFF-HOOK}} \quad \text{(EQ. 25)}$$

Taking into account the hysteresis voltage, the typical value of R_D for the off-hook to on-hook condition is:

$$R_D = \frac{375}{I_{OFF-HOOK\ to\ ON-HOOK}} \quad \text{(EQ. 26)}$$

A filter capacitor (C_D) in parallel with R_D will improve the accuracy of the trip point in a noisy environment. The value of this capacitor is calculated using the following Equation:

$$C_D = \frac{T}{R_D} \quad \text{(EQ. 27)}$$

where: T = 0.5ms

Ground Key Detector

A simplified schematic of the ground key detector is shown in Figure 18. Ground key, is the process in which the ring terminal is shorted to ground for the purpose of signaling an Operator or seizing a phone line (between the Central Office and a Private Branch Exchange). The Ground Key detector is activated when unequal current flow through resistors R_1 and R_2. This results in a current (I_{GK}) out of the transconductance amplifier (gm_2) that is equal to the product of gm_2 and the differential (I_{TIP} -I_{RING}) loop current. If I_{GK} is less than the internal current source (I_1), then diode D_1 is on and the output of the ground key comparator is low. If I_{GK} is greater than the internal current source (I_1), then diode D_2 is on and the output of the ground key comparator is high. With the output of the ground key comparator high, and the logic configured for ground key detect, the $\overline{DET}$ pin goes low. The ground key detector has a built in hysteresis of typically 5mA between its trigger and reset values.

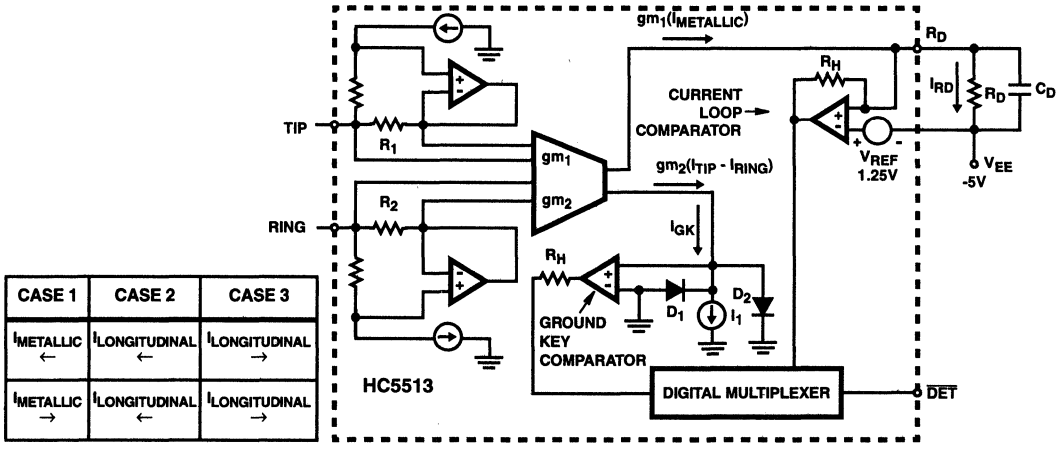


FIGURE 18. LOOP CURRENT AND GROUND KEY DETECTORS

Ring Trip Detector

Ring trip detection is accomplished with the internal ring trip comparator and the external circuitry shown in Figure 19. The process of ring trip is initiated when the logic input pins are in the following states: E0 = 0, E1 = 1/0, C1 = 1 and C2 = 0. This logic condition connects the ring trip comparator to the $\overline{DET}$ output, and causes the Ringrly pin to energize the ring relay. The ring relay connects the tip and ring of the phone to the external circuitry in Figure 19. When the phone is on-hook the DT pin is more positive than the DR pin and the $\overline{DET}$ output is high. For off-hook conditions DR is more positive than DT and $\overline{DET}$ goes low. When $\overline{DET}$ goes low, indicating that the phone has gone off-hook, the SLIC is commanded by the logic inputs to go into the active state. In the active state, tip and ring are once again connected to the phone and normal operation ensues.

Figure 19 illustrates battery backed unbalanced ring injected ringing. For tip injected ringing just reverse the leads to the phone. The ringing source could also be balanced.

NOTE: The $\overline{DET}$ output will toggle at 20Hz because the DT input is not completely filtered by C_{RT}. Software can examine the duty cycle and determine if the $\overline{DET}$ pin is low for more that half the time, if so the off-hook condition is indicated.

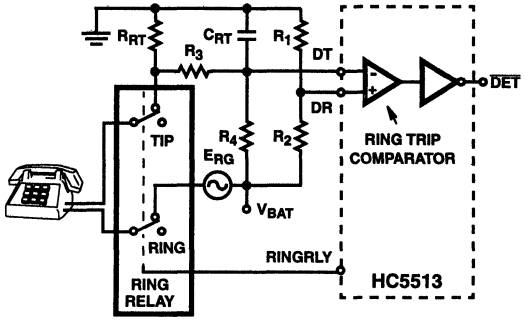


FIGURE 19. RING TRIP CIRCUIT FOR BATTERY BACKED RINGING

Longitudinal Impedance

The feedback loop described in Figure 20(A, B) realizes the desired longitudinal impedances from tip to ground and from ring to ground. Nominal longitudinal impedance is resistive and in the order of 22Ω.

In the presence of longitudinal currents this circuit attenuates the voltages that would otherwise appear at the tip and ring terminals, to levels well within the common mode range of the SLIC. In fact, longitudinal currents may exceed the programmed DC loop current without disturbing the SLIC's VF transmission capabilities.

The function of this circuit is to maintain the tip and ring voltages symmetrically around $V_{BAT}/2$, in the presence of longitudinal currents. The differential transconductance amplifiers G_T and G_R accomplish this by sourcing or sinking the required current to maintain V_C at $V_{BAT}/2$.

When a longitudinal current is injected onto the tip and ring inputs, the voltage at V_C moves from it's equilibrium value $V_{BAT}/2$. When V_C changes by the amount ΔV_C, this change appears between the input terminals of the differential transconductance amplifiers G_T and G_R. The output of G_T and G_R are the differential currents ΔI_1 and ΔI_2, which in turn feed the differential inputs of current sources I_T and I_R respectively. I_T and I_R have current gains of 250 single ended and 500 differentially, thus leading to a change in I_T and I_R that is equal to $500(\Delta I)$ and $500(\Delta I_2)$.

The circuit shown in Figure 20(B) illustrates the tip side of the longitudinal network. The advantages of a differential input current source are: improved noise since the noise due to current source $2I_O$ is now correlated, power savings due to differential current gain and minimized offset error at the Operational Amplifier inputs via the two 5kΩ resistors.

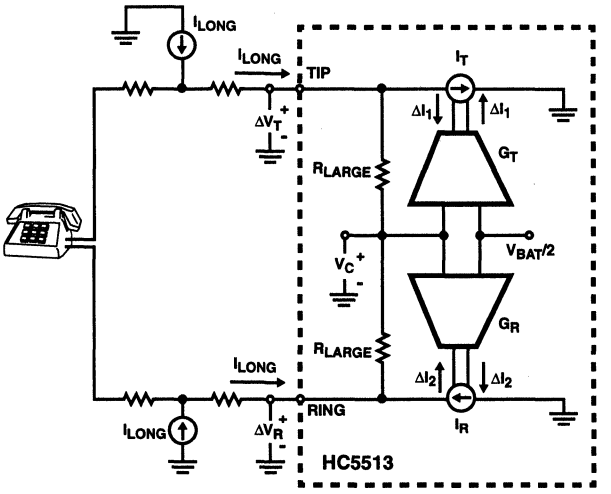


FIGURE 20A.

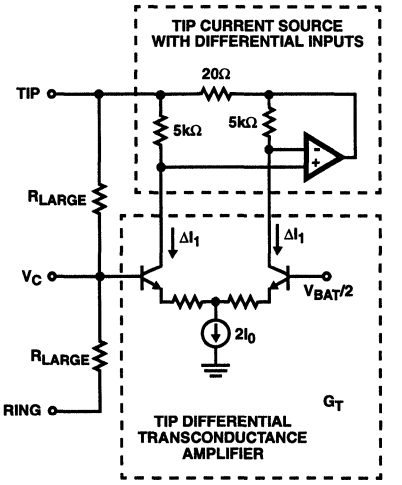


FIGURE 20B.

FIGURE 20. LONGITUDINAL IMPEDANCE NETWORK

Digital Logic Inputs

Table 1 is the logic truth table for the TTL compatible logic input pins. The HC5513 has two enable inputs pins (E0, E1) and two control inputs pins (C1, C2).

The enable pin E0 is used to enable or disable the $\overline{DET}$ output pin. The $\overline{DET}$ pin is enabled if E0 is at a logic level 0 and disabled if E0 is at a logic level 1.

The enable pin E1 gates the ground key detector to the $\overline{DET}$ output with a logic level 0, and gates the loop or ring trip detector to the $\overline{DET}$ output with a logic level 1.

A combination of the control pins C1 and C2 is used to select 1 of the 4 possible operating states. A description of each operating state and the control logic follow:

Open Circuit State (C1 = 0, C2 = 0)

In this state the SLIC is effectively off. All detectors and both the tip and ring line drive amplifiers are powered down, presenting a high impedance to the line. Power dissipation is at a minimum.

Active State (C1 = 0, C2 = 1)

The tip output is capable of sourcing loop current and for open circuit conditions is about -4V from ground. The ring output is capable of sinking loop current and for open circuit conditions is about V_{BAT} + 4V. VF signal transmission is normal. The loop current and ground key detectors are both active, E0 and E1 determine which detector is gated to the $\overline{DET}$ output.

Ringing State (C1 = 1, C2 = 0)

The ring relay driver and the ring trip detector are activated. Both the tip and ring line drive amplifiers are powered down. Both tip and ring are disconnected from the line via the external ring relay.

Standby State (C1 = 1, C2 = 1)

Both the tip and ring line drive amplifiers are powered down. Internal resistors are connected between tip to ground and ring to V_{BAT} to allow loop current detect in an off-hook condition. The loop current and ground key detectors are both active, E0 and E1 determine which detector is gated to the $\overline{DET}$ output.

AC Transmission Circuit Stability

To ensure stability of the AC transmission feedback loop two compensation capacitors C_{TC} and C_{RC} are required. Figure 21 (Application Circuit) illustrates their use. Recommended value is 2200pF.

AC-DC Separation Capacitor, C_{HP}

The high pass filter capacitor connected between pins HPT and HPR provides the separation between circuits sensing tip to ring DC conditions and circuits processing AC signals. A 10nf C_{HP} will position the low end frequency response 3dB break point at 48Hz. Where:

$$f_{3dB} = \frac{1}{(2 \bullet \pi \bullet R_{HP} \bullet C_{HP})} \quad \text{(EQ. 28)}$$

where R_{HP} = 330kΩ

SLIC Operating States

TABLE 1. LOGIC TRUTH TABLE

E0	E1	C1	C2	SLIC OPERATING STATE	ACTIVE DETECTOR	$\overline{\text{DET}}$ OUTPUT
0	0	0	0	Open Circuit	No Active Detector	Logic Level High
0	0	0	1	Active	Ground Key Detector	Ground Key Status
0	0	1	0	Ringing	No Active Detector	Logic Level High
0	0	1	1	Standby	Ground Key Detector	Ground Key Status
0	1	0	0	Open Circuit	No Active Detector	Logic Level High
0	1	0	1	Active	Loop Current Detector	Loop Current Status
0	1	1	0	Ringing	Ring Trip Detector	Ring Trip Status
0	1	1	1	Standby	Loop Current Detector	Loop Current Status
1	0	0	0	Open Circuit	No Active Detector	Logic Level High
1	0	0	1	Active	Ground Key Detector	
1	0	1	0	Ringing	No Active Detector	
1	0	1	1	Standby	Ground Key Detector	
1	1	0	0	Open Circuit	No Active Detector	
1	1	0	1	Active	Loop Current Detector	
1	1	1	0	Ringing	Ring Trip Detector	
1	1	1	1	Standby	Loop Current Detector	

Thermal Shutdown Protection

The HC5513's thermal shutdown protection is invoked if a fault condition on the tip or ring causes the temperature of the die to exceed 160°C. If this happens, the SLIC goes into a high impedance state and will remain there until the temperature of the die cools down by about 20°C. The SLIC will return back to its normal operating mode, providing the fault condition has been removed.

Surge Voltage Protection

The HC5513 must be protected against surge voltages and power crosses. Refer to "Maximum Ratings" TIPX and RINGX terminals for maximum allowable transient tip and ring voltages. The protection circuit shown in Figure 20 utilizes diodes together with a clamping device to protect tip and ring against high voltage transients.

Positive transients on tip or ring are clamped to within a couple of volts above ground via diodes D_1 and D_2. Under normal operating conditions D_1 and D_2 are reverse biased and out of the circuit.

Negative transients on tip and ring are clamped to within a couple of volts below ground via diodes D_3 and D_4 with the help of a Surgector. The Surgector is required to block conduction through diodes D_3 and D_4 under normal operating conditions and allows negative surges to be returned to system ground.

In applications where only low energy transients (<300V) are possible, diodes D_3 and D_4 could be connected to V_{BAT}, eliminating the requirement of the Surgector. Caution should be used with this application. Be aware that: surge protection is for low level transients only and will subject the batteries to negative voltage surges.

The fuse resistors (R_F) serve a dual purpose of being non-destructive power dissipaters during surge and fuses when the line in exposed to a power cross.

Power-Up Sequence

The HC5513 has **no** required power-up sequence. This is a result of the **D**ielectrically **I**solated (DI) process used in the fabrication of the part. By using the DI process, care is no longer required to insure that the substrate be kept at the most negative potential as with junction isolated ICs.

Printed Circuit Board Layout

Care in the printed circuit board layout is essential for proper operation. All connections to the RSN pin should be made as close to the device pin as possible, to limit the interference that might be injected into the RSN terminal. It is good practice to surround the RSN pin with a ground plane.

The analog and digital grounds should be tied together at the device.

NOTES:

2. **Overload Level (Two-Wire port)** - The overload level is specified at the 2-wire port (V_{TR0}) with the signal source at the 4-wire receive port (E_{RX}). I_{DCMET} = 23mA, increase the amplitude of E_{RX} until 1% THD is measured at V_{TRO}. Reference Figure 1.

3. **Longitudinal Impedance** - The longitudinal impedance is computed using the following equations, where TIP and RING voltages are referenced to ground. L_{ZT}, L_{ZR}, V_T, V_R, A_R and A_T are defined in Figure 2.

   (TIP) $L_{ZT} = V_T/A_T$

   (RING) $L_{ZR} = V_R/A_R$

   where: $E_L = 1V_{RMS}$ (0Hz to 100Hz)

4. **Longitudinal Current Limit (Off-Hook Active)** - Off-Hook (Active, $C_1 = 1$, $C_2 = 0$) longitudinal current limit is determined by increasing the amplitude of E_L (Figure 3A) until the 2-wire longitudinal balance drops below 45dB. $\overline{DET}$ pin remains low (no false detection).

5. **Longitudinal Current Limit (On-Hook Standby)** - On-Hook (Active, $C_1 = 1$, $C_2 = 1$) longitudinal current limit is determined by increasing the amplitude of E_L (Figure 3B) until the 2-wire longitudinal balance drops below 45dB. $\overline{DET}$ pin remains high (no false detection).

6. **Longitudinal to Metallic Balance** - The longitudinal to metallic balance is computed using the following equation:

   BLME = 20 • log (E_L/V_{TR}), where: E_L and V_{TR} are defined in Figure 4.

7. **Metallic to Longitudinal FCC Part 68, Para 68.310** - The metallic to longitudinal balance is defined in this spec.

8. **Longitudinal to Four-Wire Balance** - The longitudinal to 4-wire balance is computed using the following equation:

   BLFE = 20 • log (E_L/V_{TX}),: E_L and V_{TX} are defined in Figure 4.

9. **Metallic to Longitudinal Balance** - The metallic to longitudinal balance is computed using the following equation:

   BMLE = 20 • log (E_{TR}/V_L), E_{RX} = 0

   where: E_{TR}, V_L and E_{RX} are defined in Figure 5.

10. **Four-Wire to Longitudinal Balance** - The 4-wire to longitudinal balance is computed using the following equation:

    BFLE = 20 • log (E_{RX}/V_L), E_{TR} = source is removed.

    where: E_{RX}, V_L and E_{TR} are defined in Figure 5.

11. **Two-Wire Return Loss** - The 2-wire return loss is computed using the following equation:

    r = -20 • log ($2V_M/V_S$)

    where: Z_D = The desired impedance; e.g., the characteristic impedance of the line, nominally 600Ω. (Reference Figure 6).

12. **Overload Level (4-Wire port)** - The overload level is specified at the 4-wire transmit port (V_{TXO}) with the signal source (E_G) at the 2-wire port, I_{DCMET} = 23mA, Z_L = 20kΩ (Reference Figure 7). Increase the amplitude of E_G until 1% THD is measured at V_{TXO}. Note that the gain from the 2-wire port to the 4-wire port is equal to 1.

13. **Output Offset Voltage** - The output offset voltage is specified with the following conditions: E_G = 0, I_{DCMET} = 23mA, $Z_L = \infty$ and is measured at V_{TX}. E_G, I_{DCMET}, V_{TX} and Z_L are defined in Figure 7. Note: I_{DCMET} is established with a series 600Ω resistor between tip and ring.

14. **Two-Wire to Four-Wire (Metallic to V_{TX}) Voltage Gain** - The 2-wire to 4-wire (metallic to V_{TX}) voltage gain is computed using the following equation.

    $G_{2-4} = (V_{TX}/V_{TR})$, E_G = 0dBm0, V_{TX}, V_{TR}, and E_G are defined in Figure 7.

15. **Current Gain RSN to Metallic** - The current gain RSN to Metallic is computed using the following equation:

    $K = I_M [(R_{DC1} + R_{DC2})/(V_{RDC} - V_{RSN})]$ K, I_M, R_{DC1}, R_{DC2}, V_{RDC} and V_{RSN} are defined in Figure 8.

16. **Two-Wire to Four-Wire Frequency Response** - The 2-wire to 4-wire frequency response is measured with respect to E_G = 0dBm at 1.0kHz, E_{RX} = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    F_{2-4} = 20 • log (V_{TX}/V_{TR}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TX}, V_{TR}, and E_G are defined in Figure 9.

17. **Four-Wire to Two-Wire Frequency Response** - The 4-wire to 2-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    F_{4-2} = 20 • log (V_{TR}/E_{RX}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TR} and E_{RX} are defined in Figure 9.

18. **Four-Wire to Four-Wire Frequency Response** - The 4-wire to 4-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    F_{4-4} = 20 • log (V_{TX}/E_{RX}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TX} and E_{RX} are defined in Figure 9.

19. **Two-Wire to Four-Wire Insertion Loss** - The 2-wire to 4-wire insertion loss is measured with respect to E_G = 0dBm at 1.0kHz input signal, E_{RX} = 0, I_{DCMET} = 23mA and is computed using the following equation:

    $L_{2-4} = 20 \bullet \log (V_{TX}/V_{TR})$

    where: V_{TX}, V_{TR}, and E_G are defined in Figure 9. (Note: The fuse resistors, R_F, impact the insertion loss. The specified insertion loss is for R_F = 0).

20. **Four-Wire to Two-Wire Insertion Loss** - The 4-wire to 2-wire insertion loss is measured based upon E_{RX} = 0dBm, 1.0kHz input signal, E_G = 0, I_{DCMET} = 23mA and is computed using the following equation:

    $L_{4-2} = 20 \bullet \log (V_{TR}/E_{RX})$

    where: V_{TR} and E_{RX} are defined in Figure 9.

21. **Two-Wire to Four-Wire Gain Tracking** - The 2-wire to 4-wire gain tracking is referenced to measurements taken for E_G = -10dBm, 1.0kHz signal, E_{RX} = 0, I_{DCMET} = 23mA and is computed using the following equation.

    $G_{2-4} = 20 \bullet \log (V_{TX}/V_{TR})$ vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

    V_{TX} and V_{TR} are defined in Figure 9.

22. **Four-Wire to Two-Wire Gain Tracking** - The 4-wire to 2-wire gain tracking is referenced to measurements taken for E_{RX} = -10dBm, 1.0kHz signal, E_G = 0, I_{DCMET} = 23mA and is computed using the following equation:

    $G_{4-2} = 20 \bullet \log (V_{TR}/E_{RX})$ vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

    V_{TR} and E_{RX} are defined in Figure 9. The level is specified at the 4-wire receive port and referenced to a 600Ω impedance level.

23. **Two-Wire Idle Channel Noise** - The 2-wire idle channel noise at V_{TR} is specified with the 2-wire port terminated in 600Ω (R_L) and with the 4-wire receive port grounded (Reference Figure 10).

24. **Four-Wire Idle Channel Noise** - The 4-wire idle channel noise at V_{TX} is specified with the 2-wire port terminated in 600Ω (R_L). The noise specification is with respect to a 600Ω impedance level at V_{TX}. The 4-wire receive port is grounded (Reference Figure 10).

25. **Harmonic Distortion (2-Wire to 4-Wire)** - The harmonic distortion is measured with the following conditions. E_G = 0dBm at 1kHz, I_{DCMET} = 23mA. Measurement taken at V_{TX}. (Reference Figure 7).

26. **Harmonic Distortion (4-Wire to 2-Wire)** - The harmonic distortion is measured with the following conditions. E_{RX} = 0dBm0. Vary frequency between 300Hz and 3.4kHz, I_{DCMET} = 23mA. Measurement taken at V_{TR}. (Reference Figure 9).

27. **Constant Loop Current** - The constant loop current is calculated using the following equation:

    $I_L = 2500 / (R_{DC1} + R_{DC2})$

28. **Standby State Loop Current** - The standby state loop current is calculated using the following equation:

    $I_L = [|V_{BAT}| - 3] / [R_L + 1800]$, $T_A = 25^oC$

29. **Ground Key Detector** - (TRIGGER) Increase the input current to 8mA and verify that $\overline{DET}$ goes low.

    (RESET) Decrease the input current from 17mA to 3mA and verify that $\overline{DET}$ goes high.

    (Hysteresis) Compare difference between trigger and reset.

30. **Power Supply Rejection Ratio** - Inject a $100mV_{RMS}$ signal (50Hz to 4kHz) on V_{BAT}, V_{CC} and V_{EE} supplies. PSRR is computed using the following equation:

    PSRR = 20 • log (V_{TX}/V_{IN}). V_{TX} and V_{IN} are defined in Figure 12.

Pin Descriptions

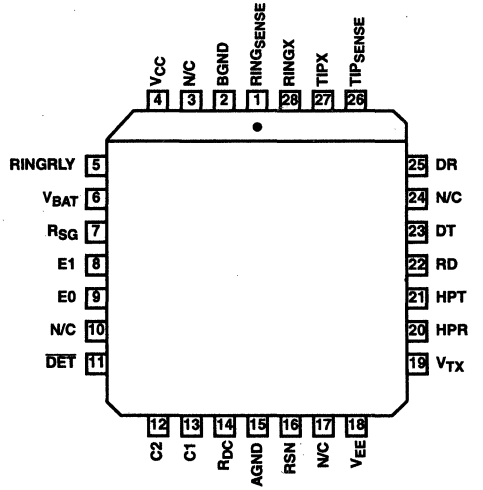
PLCC	PDIP	SYMBOL	DESCRIPTION
1		$RING_{SENSE}$	Internally connected to output of RING power amplifier.
2	7	BGND	Battery Ground - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from AGND but it is recommended that it is connected to the same potential as AGND.
4	8	V_{CC}	5V power supply.
5	9	RINGRLY	Ring relay driver output.
6	10	V_{BAT}	Battery supply voltage, -24V to -56V.
7	11	R_{SG}	Saturation guard programming resistor pin.
8	12	E1	TTL compatible logic input. The logic state of E1 in conjunction with the logic state of C1 determines which detector is gated to the $\overline{DET}$ output.
9	13	E0	TTL compatible logic input. Enables the $\overline{DET}$ output when set to logic level zero and disables $\overline{DET}$ output when set to a logic level one.
11	14	$\overline{DET}$	Detector output. TTL compatible logic output. A zero logic level indicates that the selected detector was triggered (see Truth Table for selection of Ground Key detector, Loop Current detector or the Ring Trip detector). The $\overline{DET}$ output is an open collector with an internal pull-up of approximately 15kΩ to V_{CC}.
12	15	C2	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
13	16	C1	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
14	17	R_{DC}	DC feed current programming resistor pin. Constant current feed is programmed by resistors R_{DC1} and R_{DC2} connected in series from this pin to the receive summing node (RSN). The resistor junction point is decoupled to AGND to isolate the AC signal components.
15	18	AGND	Analog ground.
16	19	RSN	Receive Summing Node. The AC and DC current flowing into this pin establishes the metallic loop current that flows between tip and ring. The magnitude of the metallic loop current is 1000 times greater than the current into the RSN pin. The constant current programming resistors and the networks for program receive gain and 2-wire impedance all connect to this pin.
18	20	V_{EE}	-5V power supply.
19	21	V_{TX}	Transmit audio output. This output is equivalent to the TIP to RING metallic voltage. The network for programming the 2-wire input impedance connects between this pin and RSN.

Pin Descriptions (Continued)

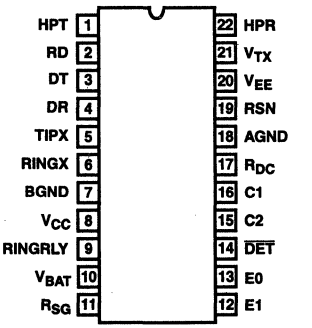
PLCC	PDIP	SYMBOL	DESCRIPTION
20	22	HPR	RING side of AC/DC separation capacitor C_{HP}. C_{HP} is required to properly separate the ring AC current from the DC loop current. The other end of C_{HP} is connected to HPT.
21	1	HPT	TIP side of AC/DC separation capacitor C_{HP}. C_{HP} is required to properly separate the tip AC current from the DC loop current. The other end of C_{HP} is connected to HPR.
22	2	RD	Loop current programming resistor. Resistor R_D sets the trigger level for the loop current detect circuit. A filter capacitor C_D is also connected between this pin and V_{EE}.
23	3	DT	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR.
25	4	DR	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR.
26		TIP_{SENSE}	Internally connected to output of tip power amplifier.
27	5	TIPX	Output of tip power amplifier.
28	6	RINGX	Output of ring power amplifier.
3, 10 17, 24		N/C	No internal connection.

Pinouts

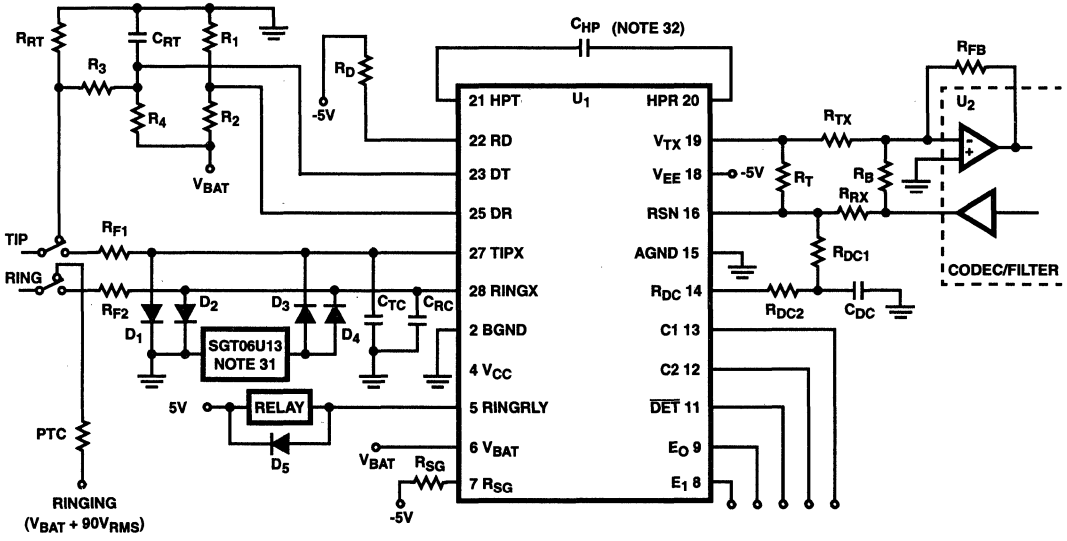
HC5513
(PLCC)
TOP VIEW



HC5513
(PDIP)
TOP VIEW



Application Circuit



U1 SLIC (Subscriber Line Interface Circuit) HC5513

U2 Combination CODEC/Filter e.g. CD22354A or Programmable CODEC/ Filter, e.g. SLAC

C_{DC} 1.5µF, 20%, 10V

C_{HP} 10nF, 20%, 100V (Note 2)

C_{RT} 0.39µF, 20%, 100V

C_{TC}, C_{RC} 2200pF, 20%, 100V

Relay Relay, 2C Contacts, 5V Coil

D_1 - D_4 Diode, 100V, 3A

Surgector SGT06U13

D_5 Diode, 1N4454

R_{F1}, R_{F2} Line Resistor, 20Ω, 1% Match

R_1, R_3 200kΩ, 5%, 1/4W

R_2 910kΩ, 5%, 1/4W

R_4 1.2MΩ, 5%, 1/4W

R_B 18.7kΩ,1%, 1/4W

R_D 39kΩ, 5%, 1/4W

R_{DC1}, R_{DC2} 41.2kΩ, 5%, 1/4W

R_{FB} 20.0kΩ, 1%, 1/4W

R_{RX} 280kΩ, 1%, 1/4W

R_T 562kΩ, 1%, 1/4W

R_{TX} 20kΩ, 1%, 1/4W

R_{RT} 150Ω, 5%, 2W

R_{SG} V_{BAT} = -28V, R_{SG} = ∞
V_{BAT} = -48V, R_{SG} = 21.4kΩ, 1/4W 5%

NOTES:

31. The anodes of D_3 and D_4 may be connected directly to the V_{BAT} supply if the application is exposed to only low energy transients. For harsher environments it is recommended that the anodes of D_3 and D_4 be shorted to ground through a transzorb or surgector.
32. To meet the specified 25dB 2-wire return loss at 200Hz, C_{HP} needs to be 20nF, 20%, 100V.

FIGURE 21. APPLICATION CIRCUIT

HARRIS SEMICONDUCTOR

HC5515

SLIC
Subscriber Line Interface Circuit

January 1997

Features

- DI Monolithic High Voltage Process
- Programmable Current Feed (20mA to 60mA)
- Programmable Loop Current Detector Threshold and Battery Feed Characteristics
- Ring Trip Detection
- Compatible with Ericsson's PBL3860
- Thermal Shutdown
- On-Hook Transmission
- Wide Battery Voltage Range (-24V to -58V)
- Low Standby Power
- -40°C to 85°C Ambient Temperature Range

Applications

- Digital Loop Carrier Systems
- Fiber-In-The-Loop ONUs
- Wireless Local Loop
- Hybrid Fiber Coax
- Related Literature
  - AN9632, Operation of the HC5523/15 Evaluation Board
- Pair Gain
- POTS
- PABX

Description

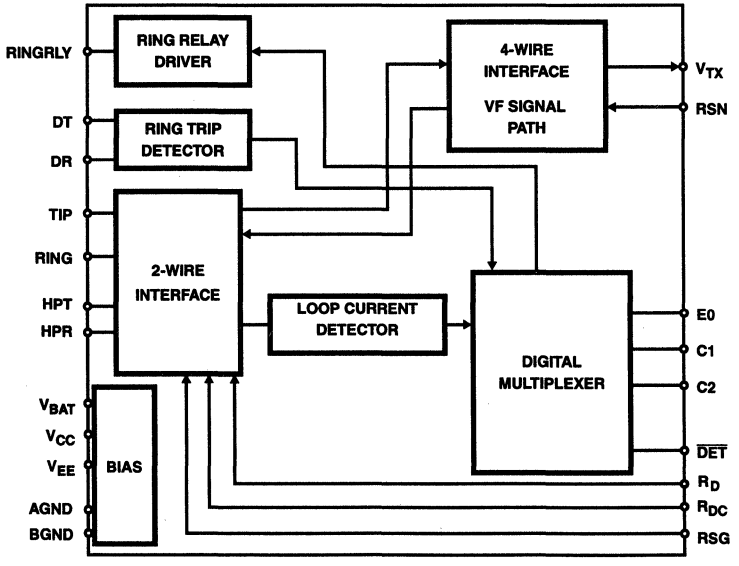
The HC5515 is a subscriber line interface circuit which is interchangeable with Ericsson's PBL3860 for distributed central office applications. Enhancements include immunity to circuit latch-up during hot plug and absence of false signaling in the presence of longitudinal currents.

The HC5515 is fabricated in a High Voltage Dielectrically Isolated (DI) Bipolar Process that eliminates leakage currents and device latch-up problems normally associated with junction isolated ICs. The elimination of the leakage currents results in improved circuit performance for wide temperature extremes. The latch free benefit of the DI process guarantees operation under adverse transient conditions. This process feature makes the HC5515 ideally suited for use in harsh outdoor environments.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC5515CM	0 to 70	28 Ld PLCC	N28.45
HC5515CP	0 to 70	22 Ld PDIP	E22.4
HC5515IM	-40 to 85	28 Ld PLCC	N28.45
HC5515IP	-40 to 85	22 Ld PDIP	E22.4

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4235.1**

Absolute Maximum Ratings

Temperature, Humidity
- Storage Temperature Range . . . . . -65°C to 150°C
- Operating Temperature Range . . . . . -40°C to 110°C
- Operating Junction Temperature Range . . . . . -40°C to 150°C

Power Supply (-40°C ≤ T_A ≤ 85°C)
- Supply Voltage V_{CC} to GND . . . . . 0.5V to 7V
- Supply Voltage V_{EE} to GND . . . . . -7V to 0.5V
- Supply Voltage V_{BAT} to GND . . . . . -80V to 0.5V

Ground
- Voltage between AGND and BGND . . . . . -0.3V to 0.3V

Relay Driver
- Ring Relay Supply Voltage . . . . . 0V to V_{BAT} +75V
- Ring Relay Current 50mA

Ring Trip Comparator
- Input Voltage . . . . . V_{BAT} to 0V
- Input Current . . . . . -5mA to 5mA

Digital Inputs, Outputs (C1, C2, E0, $\overline{DET}$)
- Input Voltage . . . . . 0V to V_{CC}
- Output Voltage ($\overline{DET}$ Not Active) . . . . . 0V to V_{CC}
- Output Current ($\overline{DET}$) 5mA

Tipx and Ringx Terminals (-40°C ≤ T_A ≤ +85°C)
- Tipx or Ringx Voltage, Continuous (Referenced to GND) V_{BAT} to +2V
- Tipx or Ringx, Pulse < 10ms, T_{REP} > 10s . . . . V_{BAT} -20V to +5V
- Tipx or Ringx, Pulse < 10µs, T_{REP} > 10s . . . . V_{BAT} -40V to +10V
- Tipx or Ringx, Pulse < 250ns, T_{REP} > 10s . . . V_{BAT} -70V to +15V
- Tipx or Ringx Current 70mA

ESD Rating 500V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}
22 Lead PDIP Package	53°C/W
28 Lead PLCC Package	53°C/W

Continuous Power Dissipation at 70°C
- 22 Lead PDIP Package 1.5W
- 28 Lead PLCC Package 1.5W

Package Power Dissipation at 70°C, t < 100ms, t_{REP} > 1s
- 22 Lead PDIP Package 4W
- 28 Lead PLCC Package 4W

Derate above . . . . . 70°C
- Plastic DIP . . . . . 18.8mW/°C
- PLCC . . . . . 18.8mW/°C

Maximum Junction Temperature Range . . . . . -40°C to 150°C
Maximum Storage Temeprature Range . . . . . -65°C to 150°C
Maximum Lead Temperature . . . . . 300°C
(Soldering 10s, PLCC Lead Tips Only)

Die Characteristics

Gate Count . . . . . 543 Transistors, 51 Diodes

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Typical Operating Conditions

These represent the conditions under which the part was developed and are suggested as guidelines.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Case Temperature		-40	-	100	°C
V_{CC} with Respect to AGND	-40°C to +85°C	4.75	-	5.25	V
V_{EE} with Respect to AGND	-40°C to +85°C	-5.25	-	-4.75	V
V_{BAT} with Respect to BGND	-40°C to +85°C	-58	-	-24	V

Electrical Specifications

T_A = -40°C to +85°C, V_{CC} = +5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -48V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 33kΩ, R_{SG} = 0Ω, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Overload Level	1% THD, Z_L = 600Ω, (Note 2, Figure 1)	3.1	-	-	V_{PEAK}
Longitudinal Impedance (Tip/Ring)	0 < f < 100Hz (Note 3, Figure 2)	-	20	35	Ω/Wire

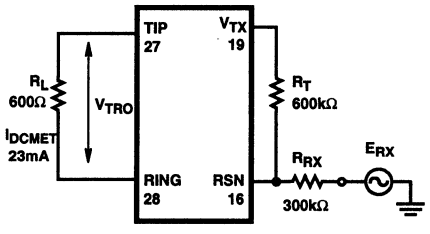


FIGURE 1. OVERLOAD LEVEL (TWO-WIRE PORT)

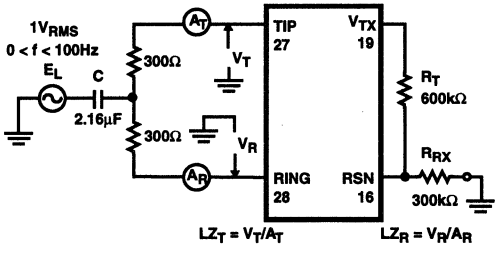


FIGURE 2. LONGITUDINAL IMPEDANCE

Electrical Specifications $T_A = -40^oC$ to $+85^oC$, $V_{CC} = +5V \pm 5\%$, $V_{EE} = -5V \pm 5\%$, $V_{BAT} = -48V$, AGND = BGND = 0V, $R_{DC1} = R_{DC2} = 41.2k\Omega$, $R_D = 33k\Omega$, $R_{SG} = 0\Omega$, $R_{F1} = R_{F2} = 0\Omega$, $C_{HP} = 10nF$, $C_{DC} = 1.5\mu F$, $Z_L = 600\Omega$, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LONGITUDINAL CURRENT LIMIT (TIP/RING)					
Off-Hook (Active)	No False Detections, (Loop Current), LB > 45dB (Note 4, Figure 3A)	20	-	-	mA_{PEAK}/ Wire
On-Hook (Standby), $R_L = \infty$	No False Detections (Loop Current) (Note 5, Figure 3B)	5	-	-	mA_{PEAK}/ Wire

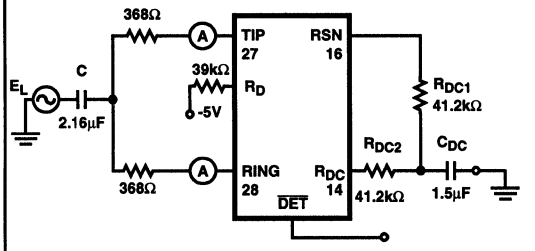


FIGURE 3A. OFF-HOOK

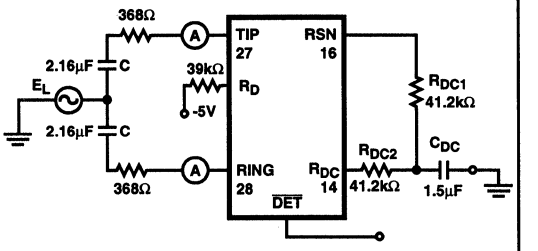


FIGURE 3B. ON-HOOK

FIGURE 3. LONGITUDINAL CURRENT LIMIT

OFF-HOOK LONGITUDINAL BALANCE					
Longitudinal to Metallic	IEEE 455 - 1985, R_{LR}, $R_{LT} = 368\Omega$ 0.2kHz < f < 4.0kHz (Note 6, Figure 4)	53	70	-	dB
Longitudinal to Metallic	R_{LR}, $R_{LT} = 300\Omega$, 0.2kHz < f < 4.0kHz (Note 6, Figure 4)	53	70	-	dB
Metallic to Longitudinal	FCC Part 68, Para 68.310 0.2kHz < f < 1.0kHz	50	55	-	dB
	1.0kHz < f < 4.0kHz (Note 7)	50	55	-	dB
Longitudinal to 4-Wire	0.2kHz < f < 4.0kHz (Note 8, Figure 4)	53	70	-	dB
Metallic to Longitudinal	R_{LR}, $R_{LT} = 300\Omega$, 0.2kHz < f < 4.0kHz (Note 9, Figure 5)	50	55	-	dB
4-Wire to Longitudinal	0.2kHz < f < 4.0kHz (Note 10, Figure 5)	50	55	-	dB

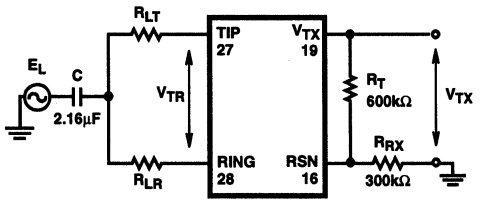


FIGURE 4. LONGITUDINAL TO METALLIC AND LONGITUDINAL TO 4-WIRE BALANCE

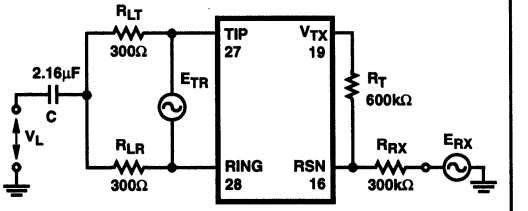


FIGURE 5. METALLIC TO LONGITUDINAL AND 4-WIRE TO LONGITUDINAL BALANCE

2-Wire Return Loss $C_{HP} = 20nF$	0.2kHz to 0.5kHz (Note 11, Figure 6)	25	-	-	dB
	0.5kHz to 1.0kHz (Note 11, Figure 6)	27	-	-	dB
	1.0kHz to 3.4kHz (Note 11, Figure 6)	23	-	-	dB

Electrical Specifications T_A = -40°C to +85°C, V_{CC} = +5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -48V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 33kΩ, R_{SG} = 0Ω, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TIP IDLE VOLTAGE					
Active, I_L = 0		-	-1.5	-	V
Standby, I_L = 0		-	<0	-	V
RING IDLE VOLTAGE					
Active, I_L = 0		-	-46.5	-	V
Standby, I_L = 0		-	>-48	-	V
TIP-RING Open Loop Metallic Voltage, V_{TR}	V_{BAT} = -52V, R_{SG} = 0Ω	43	-	47	V
4-WIRE TRANSMIT PORT (V_{TX})					
Overload Level	(Z_L > 20kΩ, 1% THD) (Note 12, Figure 7)	3.1	-	-	V_{PEAK}
Output Offset Voltage	E_G = 0, Z_L = ∞, (Note 13, Figure 7)	-60	-	60	mV
Output Impedance (Guaranteed by Design)	0.2kHz < f < 03.4kHz	-	5	20	Ω
2- to 4-Wire (Metallic to V_{TX}) Voltage Gain	0.3kHz < f < 03.4kHz (Note 14, Figure 7)	0.98	1.0	1.02	V/V

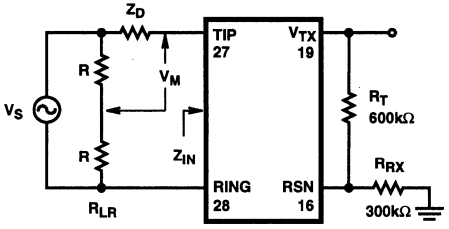


FIGURE 6. TWO-WIRE RETURN LOSS

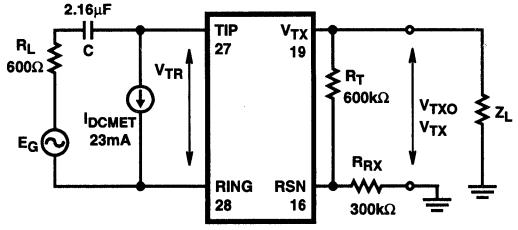


FIGURE 7. OVERLOAD LEVEL (4-WIRE TRANSMIT PORT), OUTPUT OFFSET VOLTAGE, 2-WIRE TO 4-WIRE VOLTAGE GAIN AND HARMONIC DISTORTION

4-WIRE RECEIVE PORT (RSN)					
DC Voltage	I_{RSN} = 0mA	-	0	-	V
R_X Sum Node Impedance (Gtd by Design)	0.2kHz < f < 3.4kHz	-	-	20	Ω
Current Gain-RSN to Metallic	0.3kHz < f < 3.4kHz (Note 15, Figure 8)	900	1000	1100	Ratio
FREQUENCY RESPONSE (OFF-HOOK)					
2-Wire to 4-Wire	0dBm at 1.0kHz, E_{RX} = 0V 0.3kHz < f < 3.4kHz (Note 16, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm at 1.0kHz, E_G = 0V 0.3kHz < f < 3.4kHz (Note 17, Figure 9)	-0.2	-	0.2	dB
4-Wire to 4-Wire	0dBm at 1.0kHz, E_G = 0V 0.3kHz < f < 3.4kHz (Note 18, Figure 9)	-0.2	-	0.2	dB
INSERTION LOSS					
2-Wire to 4-Wire	0dBm, 1kHz (Note 19, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm, 1kHz (Note 20, Figure 9)	-0.2	-	0.2	dB
GAIN TRACKING (Ref = -10dBm, at 1.0kHz)					
2-Wire to 4-Wire	+3dBm to +7dBm (Note 21, Figure 9)	-0.15	-	0.15	dB
2-Wire to 4-Wire	-40dBm to +3dBm (Note 21, Figure 9)	-0.1	-	0.1	dB

Electrical Specifications $T_A = -40^oC$ to $+85^oC$, $V_{CC} = +5V \pm 5\%$, $V_{EE} = -5V \pm 5\%$, $V_{BAT} = -48V$, AGND = BGND = 0V, $R_{DC1} = R_{DC2} = 41.2k\Omega$, $R_D = 33k\Omega$, $R_{SG} = 0\Omega$, $R_{F1} = R_{F2} = 0\Omega$, $C_{HP} = 10nF$, $C_{DC} = 1.5\mu F$, $Z_L = 600\Omega$, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2-Wire to 4-Wire	-55dBm to -40dBm (Note 21, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	-40dBm to +7dBm (Note 22, Figure 9)	-0.1	-	0.1	dB
4-Wire to 2-Wire	-55dBm to -40dBm (Note 22, Figure 9)	-0.2	-	0.2	dB

$GRX = ((V_{TR1} - V_{TR2})(300k))/(-3)(600)$

Where: V_{TR1} is the Tip to Ring Voltage with $V_{RSN} = 0V$
and V_{TR2} is the Tip to Ring Voltage with $V_{RSN} = -3V$

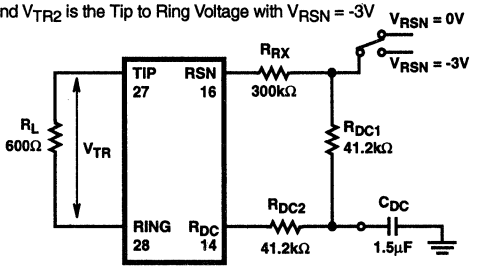


FIGURE 8. CURRENT GAIN-RSN TO METALLIC

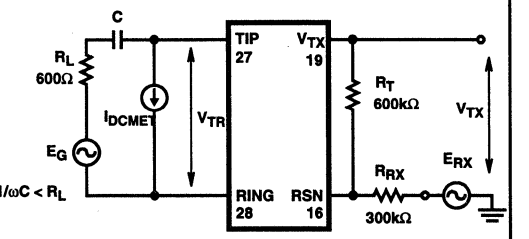


FIGURE 9. FREQUENCY RESPONSE, INSERTION LOSS, GAIN TRACKING AND HARMONIC DISTORTION

NOISE					
Idle Channel Noise at 2-Wire	C-Message Weighting (Note 23, Figure 10)	-	8.5	-	dBrnC
	Psophometrical Weighting (Note 23, Figure 10)	-	-81.5	-	dBrnp
Idle Channel Noise at 4-Wire	C-Message Weighting (Note 24, Figure 10)	-	8.5	-	dBrnC
	Psophometrical Weighting (Note 23, Figure 10)	-	-81.5	-	dBrnp
HARMONIC DISTORTION					
2-Wire to 4-Wire	0dBm, 1kHz (Note 25, Figure 7)	-	-65	-54	dB
4-Wire to 2-Wire	0dBm, 0.3kHz to 3.4kHz (Note 26, Figure 9)	-	-65	-54	dB
BATTERY FEED CHARACTERISTICS					
Constant Loop Current Tolerance $R_{DCX} = 41.2k\Omega$	$I_L = 2500/(R_{DC1} + R_{DC2})$, -40^oC to 85^oC (Note 27)	$0.85I_L$	I_L	$1.15I_L$	mA
Loop Current Tolerance (Standby)	$I_L = (V_{BAT}-3)/(R_L+1800)$, -40^oC to 85^oC (Note 28)	$0.75I_L$	I_L	$1.25I_L$	mA
Open Circuit Voltage ($V_{TIP} - V_{RING}$)	-40^oC to 85^oC, (Active) $R_{SG} = \infty$	14	16.67	20	V
LOOP CURRENT DETECTOR					
On-Hook to Off-Hook	$R_D = 33k\Omega$, -40^oC to 85^oC	11	$465/R_D$	17.2	mA
Off-Hook to On-Hook	$R_D = 33k\Omega$, -40^oC to 85^oC	9.5	$405/R_D$	15.0	mA
Loop Current Hysteresis	$R_D = 33k\Omega$, -40^oC to 85^oC	-	$60/R_D$	-	mA

Electrical Specifications T_A = -40°C to +85°C, V_{CC} = +5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -48V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 33kΩ, R_{SG} = 0Ω, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS

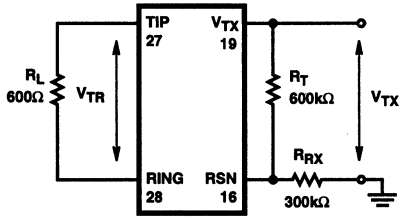



FIGURE 10. IDLE CHANNEL NOISE					
RING TRIP DETECTOR (DT, DR)					
Offset Voltage	Source Res = 0	-20	-	20	mV
Input Bias Current	Source Res = 0	-360	-	360	nA
Input Common-Mode Range	Source Res = 0	V_{BAT} +1	-	0	V
Input Resistance	Source Res = 0, Unbalanced	1	-	-	MΩ
	Source Res = 0, Balanced	3	-	-	MΩ
RING RELAY DRIVER					
V_{SAT} at 25mA	I_{OL} = 25mA	-	0.2	0.6	V
Off-State Leakage Current	V_{OH} = 12V	-	-	10	µA
DIGITAL INPUTS (E0, C1, C2)					
Input Low Voltage, V_{IL}		0	-	0.8	V
Input High Voltage, V_{IH}		2	-	V_{CC}	V
Input Low Current, I_{IL}: C1, C2	V_{IL} = 0.4V	-200	-	-	µA
Input Low Current, I_{IL}: E0	V_{IL} = 0.4V	-100	-	-	µA
Input High Current	V_{IH} = 2.4V	-	-	40	µA
DETECTOR OUTPUT ($\overline{DET}$)					
Output Low Voltage, V_{OL}	I_{OL} = 2mA	-	-	0.45	V
Output High Voltage, V_{OH}	I_{OH} = 100µA	2.7	-	-	V
Internal Pull-Up Resistor		8	15	25	kΩ
POWER DISSIPATION (V_{BAT} = -48V)					
Open Circuit State	C1 = C2 = 0	-	26.3	70	mW
On-Hook, Standby	C1 = C2 = 1	-	37.5	85	mW
On-Hook, Active	C1 = 0, C2 = 1, R_L = High Impedance	-	110	300	mW
Off-Hook, Active	C1 = 0, C2 = 1, R_L = 600Ω	-	1.1	1.4	W
TEMPERATURE GUARD					
Thermal Shutdown		150	-	180	°C

Electrical Specifications $T_A = -40^oC$ to $+85^oC$, $V_{CC} = +5V \pm 5\%$, $V_{EE} = -5V \pm 5\%$, $V_{BAT} = -48V$, AGND = BGND = 0V, $R_{DC1} = R_{DC2} = 41.2k\Omega$, $R_D = 33k\Omega$, $R_{SG} = 0\Omega$, $R_{F1} = R_{F2} = 0\Omega$, $C_{HP} = 10nF$, $C_{DC} = 1.5\mu F$, $Z_L = 600\Omega$, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENTS (V_{BAT} = -28V)					
Open Circuit State (C1, 2 = 0, 0) On-Hook	I_{CC}	-	1.3	2.8	mA
	I_{EE}	-	0.6	2.0	mA
	I_{BAT}	-	0.35	1.2	mA
Standby State (C1, 2 = 1, 1) On-Hook	I_{CC}	-	1.6	3.5	mA
	I_{EE}	-	0.62	2.0	mA
	I_{BAT}	-	0.55	1.6	mA
Active State (C1, 2 = 0, 1) On-Hook	I_{CC}	-	3.7	9.5	mA
	I_{EE}	-	1.1	4.0	mA
	I_{BAT}	-	2.2	5.2	mA
PSRR					
V_{CC} to 2 or 4-Wire Port	(Note 29, Figure 11)	-	40	-	dB
V_{EE} to 2 or 4-Wire Port	(Note 29, Figure 11)	-	40	-	dB
V_{BAT} to 2 or 4-Wire Port	(Note 29, Figure 11)	-	40	-	dB

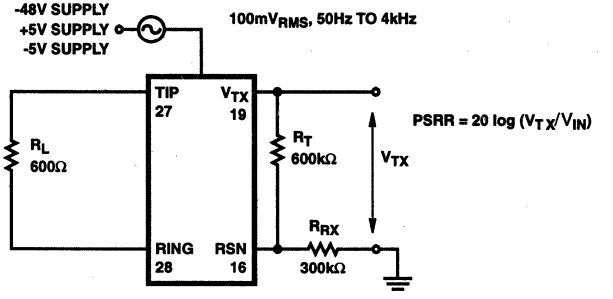


FIGURE 11. POWER SUPPLY REJECTION RATIO

Circuit Operation and Design Information

The HC5515 is a current feed voltage sense Subscriber Line Interface Circuit (SLIC). This means that for short loop applications the SLIC provides a programed constant current to the tip and ring terminals while sensing the tip to ring voltage.

The following discussion separates the SLIC's operation into its DC and AC path, then follows up with additional circuit and design information.

Constant Loop Current (DC) Path

SLIC In the Active Mode

The DC path establishes a constant loop current that flows out of tip and into the ring terminal. The loop current is programmed by resistors R_{DC1}, R_{DC2} and the voltage on the R_{DC} pin (Figure 12). The R_{DC} voltage is determined by the voltage across R_1 in the saturation guard circuit. Under constant current feed conditions, the voltage drop across R_1

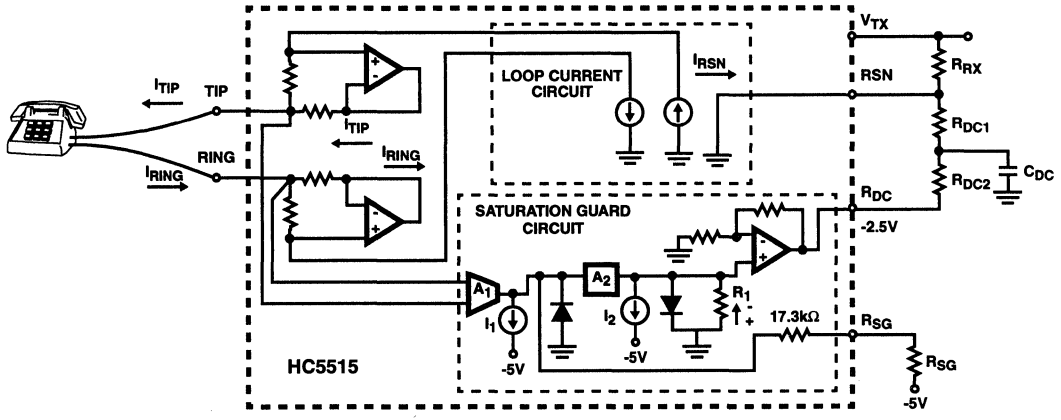


FIGURE 12. DC LOOP CURRENT

sets the R_{DC} voltage to -2.5V. This occurs when current flows through R_1 into the current source I_2. The R_{DC} voltage establishes a current (I_{RSN}) that is equal to $V_{RDC}/(R_{DC1}+R_{DC2})$. This current is then multiplied by 1000, in the loop current circuit, to become the tip and ring loop currents.

For the purpose of the following discussion, the saturation guard voltage is defined as the maximum tip to ring voltage at which the SLIC can provide a constant current for a given battery and overhead voltage.

For loop resistances that result in a tip to ring voltage less than the saturation guard voltage the loop current is defined as:

$$I_L = \frac{2.5V}{R_{DC1}+R_{DC2}} \times 1000 \qquad \text{(EQ. 1)}$$

where: I_L = Constant loop current.

R_{DC1} and R_{DC2} = Loop current programming resistors.

Capacitor C_{DC} between R_{DC1} and R_{DC2} removes the VF signals from the battery feed control loop. The value of C_{DC} is determined by Equation 2:

$$C_{DC} = T \times \left(\frac{1}{R_{DC1}} + \frac{1}{R_{DC2}}\right) \qquad \text{(EQ. 2)}$$

where T = 30ms

NOTE: The minimum C_{DC} value is obtained if $R_{DC1} = R_{DC2}$

Figure 13 illustrates the relationship between the tip to ring voltage and the loop resistance. For a 0Ω loop resistance both tip and ring are at $V_{BAT}/2$. As the loop resistance increases, so does the voltage differential between tip and ring. When this differential voltage becomes equal to the saturation guard voltage, the operation of the SLIC's loop feed changes from a constant current feed to a resistive feed. The loop current in the resistive feed region is no longer constant but varies as a function of the loop resistance.

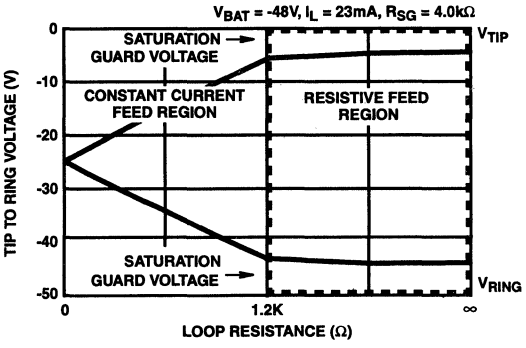
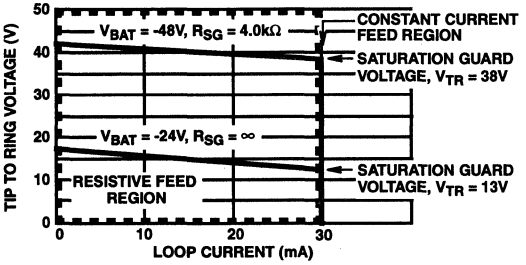


FIGURE 13. V_{TR} vs R_L

Figure 14 shows the relationship between the saturation guard voltage, the loop current and the loop resistance. Notice from Figure 14 that for a loop resistance <1.2kΩ (R_{SG} = 4.0kΩ) the SLIC is operating in the constant current feed region and for resistances >1.2kΩ the SLIC is operating in the resistive feed region. Operation in the resistive feed region allows long loop and off-hook transmission by keeping the tip and ring voltages off the rails. Operation in this region is transparent to the customer.



R_L	100kΩ	4kΩ	2kΩ	<1.2kΩ	R_{SG} = 4.0kΩ
R_L	100kΩ	1.5kΩ	700Ω	<400Ω	R_{SG} = ∞Ω

FIGURE 14. V_{TR} vs I_L and R_L

The Saturation Guard circuit (Figure 12) monitors the tip to ring voltage via the transconductance amplifier A_1. A_1 generates a current that is proportional to the tip to ring voltage difference. I_1 is internally set to sink all of A_1's current until the tip to ring voltage exceeds 12.5V. When the tip to ring voltage exceeds 12.5V (with no R_{SG} resistor) A_1 supplies more current than I_1 can sink. When this happens A_2 amplifies its input current by a factor of 12 and the current through R_1 becomes the difference between I_2 and the output current from A_2. As the current from A_2 increases, the voltage across R_1 decreases and the output voltage on R_{DC} decreases. This results in a corresponding decrease in the loop current. The R_{SG} pin provides the ability to increase the saturation guard reference voltage beyond 12.5V. Equation 3 gives the relationship between the R_{SG} resistor value and the programmable saturation guard reference voltage:

$$V_{SGREF} = 12.5 + \frac{5 \bullet 10^5}{R_{SG} + 17300} \quad \text{(EQ. 3)}$$

where:

V_{SGREF} = Saturation Guard reference voltage.

R_{SG} = Saturation Guard programming resistor.

When the Saturation guard reference voltage is exceeded, the tip to ring voltage is calculated using Equation 4:

$$V_{TR} = R_L \times \frac{16.66 + 5 \bullet 10^5/(R_{SG} + 17300)}{R_L + (R_{DC1} + R_{DC2})/600} \quad \text{(EQ. 4)}$$

where:

V_{TR} = Voltage differential between tip and ring.

R_L = Loop resistance.

For on-hook transmission $R_L = \infty$, Equation 4 reduces to:

$$V_{TR} = 16.66 + \frac{5 \bullet 10^5}{R_{SG} + 17300} \quad \text{(EQ. 5)}$$

The value of R_{SG} should be calculated to allow maximum loop length operation. This requires that the saturation guard reference voltage be set as high as possible without clipping the incoming or outgoing VF signal. A voltage margin of -4V on tip and -4V on ring, for a total of -8V margin, is recommended as a general guideline. The value of R_{SG} is calculated using Equation 6:

$$R_{SG} = \left(\frac{5 \bullet 10^5}{(|V_{BAT}| - V_{MAR}) \times \left(1 + \frac{(R_{DC1} + R_{DC2})}{600 R_L}\right) - 16.66V} - 17300 \right) \quad \text{(EQ. 6)}$$

where:

V_{BAT} = Battery voltage.

V_{MAR} = Voltage Margin. Recommended value of -8V to allow a maximum overload level of 3.1V peak.

For on-hook transmission $R_L = \infty$, Equation 6 reduces to:

$$R_{SG} = \frac{5 \bullet 10^5}{|V_{BAT}| - V_{MAR} - 16.66V} - 17300 \quad \text{(EQ. 7)}$$

SLIC in the Standby Mode

Overall system power is saved by configuring the SLIC in the standby state when not in use. In the standby state the tip and ring amplifiers are disabled and internal resistors are connected between tip to ground and ring to V_{BAT}. This connection enables a loop current to flow when the phone goes off-hook. The loop current detector then detects this current and the SLIC is configured in the active mode for voice transmission. The loop current in standby state is calculated as follows:

$$I_L \approx \frac{|V_{BAT}| - 3V}{R_L + 1800\Omega} \quad \text{(EQ. 8)}$$

where:

I_L = Loop current in the standby state.

R_L = Loop resistance.

V_{BAT} = Battery voltage.

(AC) Transmission Path

SLIC in the Active Mode

Figure 15 shows a simplified AC transmission model. Circuit analysis yields the following design equations:

$$V_{TR} = V_{TX} + I_M \bullet 2R_F \quad \text{(EQ. 9)}$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_M}{1000} \quad \text{(EQ. 10)}$$

$$V_{TR} = E_G - I_M \bullet Z_L \quad \text{(EQ. 11)}$$

where:

V_{TR} = Is the AC metallic voltage between tip and ring, including the voltage drop across the fuse resistors R_F.

V_{TX} = Is the AC metallic voltage. Either at the ground referenced 4-wire side or the SLIC tip and ring terminals.

I_M = Is the AC metallic current.

R_F = Is a fuse resistor.

Z_T = Is used to set the SLIC's 2-wire impedance.

V_{RX} = Is the analog ground referenced receive signal.

Z_{RX} = Is used to set the 4-wire to 2-wire gain.

E_G = Is the AC open circuit voltage.

Z_L = Is the line impedance.

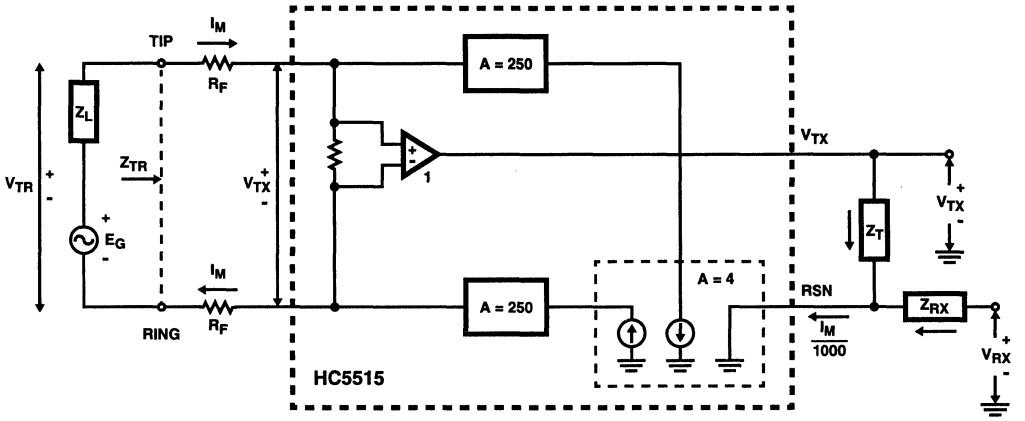


FIGURE 15. SIMPLIFIED AC TRANSMISSION CIRCUIT

(AC) 2-Wire Impedance

The AC 2-wire impedance (Z_{TR}) is the impedance looking into the SLIC, including the fuse resistors, and is calculated as follows:

Let $V_{RX} = 0$. Then from Equation 10

$$V_{TX} = Z_T \bullet \frac{I_M}{1000} \quad \text{(EQ. 12)}$$

Z_{TR} is defined as:

$$Z_{TR} = \frac{V_{TR}}{I_M} \quad \text{(EQ. 13)}$$

Substituting in Equation 9 for V_{TR}

$$Z_{TR} = \frac{V_{TX}}{I_M} + \frac{2R_F \bullet I_M}{I_M} \quad \text{(EQ. 14)}$$

Substituting in Equation 12 for V_{TX}

$$Z_{TR} = \frac{Z_T}{1000} + 2R_F \quad \text{(EQ. 15)}$$

Therefore

$$Z_T = 1000 \bullet (Z_{TR} - 2R_F) \quad \text{(EQ. 16)}$$

Equation 16 can now be used to match the SLIC's impedance to any known line impedance (Z_{TR}).

Example:

Calculate Z_T to make $Z_{TR} = 600\Omega$ in series with 2.16µF. $R_F = 20\Omega$.

$$Z_T = 1000 \bullet \left(600 + \frac{1}{j\omega \bullet 2.16 \bullet 10^{-6}} - 2 \bullet 20\right)$$

$Z_T = 560k\Omega$ in series with 2.16nF

(AC) 2-Wire to 4-Wire Gain

The 2-wire to 4-wire gain is equal to V_{TX}/V_{TR}

From Equations 9 and 10 with $V_{RX} = 0$

$$A_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/1000}{Z_T/1000 + 2R_F} \quad \text{(EQ. 17)}$$

(AC) 4-Wire to 2-Wire Gain

The 4-wire to 2-wire gain is equal to V_{TR}/V_{RX}

From Equations 9, 10 and 11 with $E_G = 0$

$$A_{4-2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L}{\frac{Z_T}{1000} + 2R_F + Z_L} \quad \text{(EQ. 18)}$$

For applications where the 2-wire impedance (Z_{TR}, Equation 15) is chosen to equal the line impedance (Z_L), the expression for A_{4-2} simplifies to:

$$A_{4-2} = -\frac{Z_T}{Z_{RX}} \bullet \frac{1}{2} \quad \text{(EQ. 19)}$$

(AC) 4-Wire to 4-Wire Gain

The 4-wire to 4-wire gain is equal to V_{TX}/V_{RX}

From Equations 9, 10 and 11 with $E_G = 0$

$$A_{4-4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L + 2R_F}{\frac{Z_T}{1000} + 2R_F + Z_L} \quad \text{(EQ. 20)}$$

Transhybrid Circuit

The purpose of the transhybrid circuit is to remove the receive signal (V_{RX}) from the transmit signal (V_{TX}), thereby preventing an echo on the transmit side. This is accomplished by using an external op amp (usually part of the CODEC) and by the inversion of the signal from the 4-wire receive port (RSN) to the 4-wire transmit port (V_{TX}). Figure 16 shows the transhybrid circuit. The input signal will

be subtracted from the output signal if I_1 equals I_2. Node analysis yields the following equation:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \quad \text{(EQ. 21)}$$

The value of Z_B is then

$$Z_B = -R_{TX} \bullet \frac{V_{RX}}{V_{TX}} \quad \text{(EQ. 22)}$$

Where V_{RX}/V_{TX} equals $1/A_{4-4}$

Therefore

$$Z_B = R_{TX} \bullet \frac{Z_{RX}}{Z_T} \bullet \frac{\frac{Z_T}{1000} + 2R_F + Z_L}{Z_L + 2R_F} \quad \text{(EQ. 23)}$$

Example:

Given: R_{TX} = 20kΩ, Z_{RX} = 280kΩ, Z_T = 562kΩ (standard value), R_F = 20Ω and Z = 600Ω

The value of Z_B = 18.7kΩ

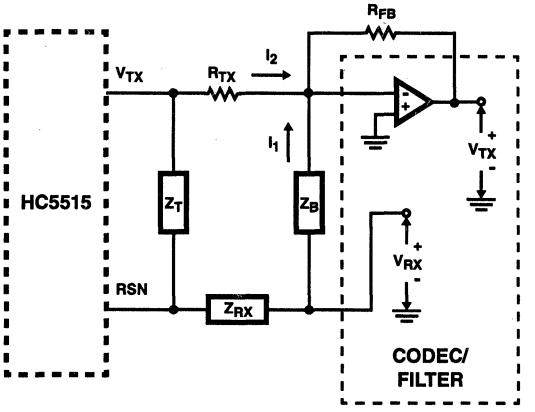


FIGURE 16. TRANSHYBRID CIRCUIT

Supervisory Functions

The loop current and the ring trip detector outputs are multiplexed to a single logic output pin called $\overline{DET}$. See Table 1 to determine the active detector for a given logic input. For further discussion of the logic circuitry see section titled "Digital Logic Inputs".

Before proceeding with an explanation of the loop current detector and the longitudinal impedance, it is important to understand the difference between a "metallic" and "longitudinal" loop currents. Figure 17 illustrates 3 different types of loop current encountered.

Case 1 illustrates the metallic loop current. The definition of a metallic loop current is when **equal** currents flow out of tip and into ring. Loop current is a metallic current.

Cases 2 and 3 illustrate the longitudinal loop current. The definition of a longitudinal loop current is a common mode current, that flows either out of or into tip and ring simultaneously. Longitudinal currents in the on-hook state result in **equal** currents flowing through the sense resistors R_1 and R_2 (Figure 17). And longitudinal currents in the off-hook state result in **unequal** currents flowing through the sense resistors R_1 and R_2. Notice that for case 2, longitudinal currents flowing away from the SLIC, the current through R_1 is the metallic loop current plus the longitudinal current; whereas the current through R_2 is the metallic loop current minus the longitudinal current. Longitudinal currents are generated when the phone line is influenced by magnetic fields (e.g. power lines).

Loop Current Detector

Figure 17 shows a simplified schematic of the loop current detector. The loop current detector works by sensing the metallic current flowing through resistors R_1 and R_2. This results in a current (I_{RD}) out of the transconductance amplifier (gm_1) that is equal to the product of gm_1 and the metallic loop current. I_{RD} then flows out the R_D pin and through resistor R_D to V_{EE}. The value of I_{RD} is equal to:

$$I_{RD} = \frac{|I_{TIP} - I_{RING}|}{600} = \frac{I_L}{300} \quad \text{(EQ. 24)}$$

The I_{RD} current results in a voltage drop across R_D that is compared to an internal 1.25V reference voltage. When the voltage drop across R_D exceeds 1.25V, and the logic is configured for loop current detection, the $\overline{DET}$ pin goes low.

The hysteresis resistor R_H adds an additional voltage effectively across R_D, causing the on-hook to off-hook threshold to be slightly higher than the off-hook to on-hook threshold.

Taking into account the hysteresis voltage, the typical value of R_D for the on-hook to off-hook condition is:

$$R_D = \frac{465}{I_{ON-HOOK\ to\ OFF-HOOK}} \quad \text{(EQ. 25)}$$

Taking into account the hysteresis voltage, the typical value of R_D for the off-hook to on-hook condition is:

$$R_D = \frac{375}{I_{OFF-HOOK\ to\ ON-HOOK}} \quad \text{(EQ. 26)}$$

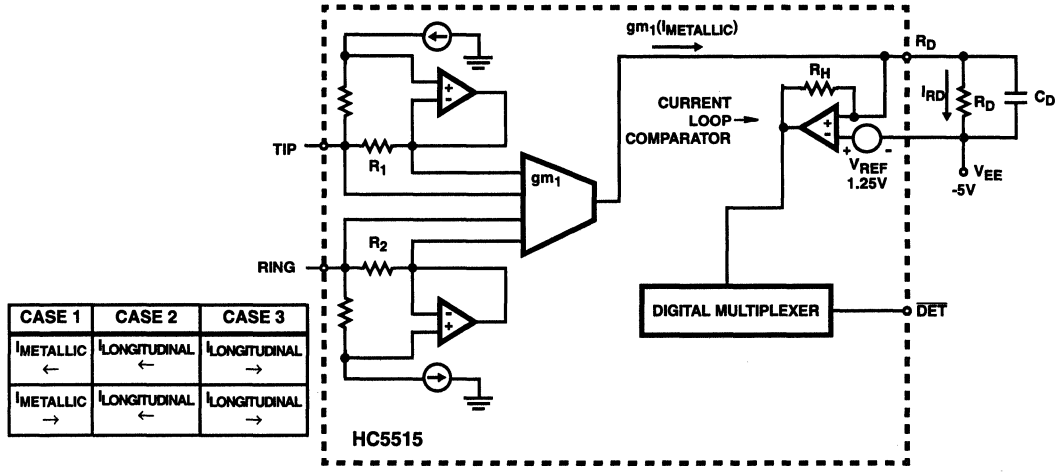
A filter capacitor (C_D) in parallel with R_D will improve the accuracy of the trip point in a noisy environment. The value of this capacitor is calculated using the following Equation:

$$C_D = \frac{T}{R_D} \quad \text{(EQ. 27)}$$

where: T = 0.5ms

Ring Trip Detector

Ring trip detection is accomplished with the internal ring trip comparator and the external circuitry shown in Figure 18. The process of ring trip is initiated when the logic input pins are in the following states: E0 = 0, C1 = 1 and C2 = 0. This logic condition connects the ring trip comparator to the $\overline{DET}$ output, and causes the Ringrly pin to energize the ring relay.



CASE 1	CASE 2	CASE 3
$I_{METALLIC}$ ←	$I_{LONGITUDINAL}$ ←	$I_{LONGITUDINAL}$ →
$I_{METALLIC}$ →	$I_{LONGITUDINAL}$ ←	$I_{LONGITUDINAL}$ →

FIGURE 17. LOOP CURRENT DETECTOR

The ring relay connects the tip and ring of the phone to the external circuitry in Figure 18. When the phone is on-hook the DT pin is more positive than the DR pin and the $\overline{DET}$ output is high. For off-hook conditions DR is more positive than DT and $\overline{DET}$ goes low. When $\overline{DET}$ goes low, indicating that the phone has gone off-hook, the SLIC is commanded by the logic inputs to go into the active state. In the active state, tip and ring are once again connected to the phone and normal operation ensues.

Figure 18 illustrates battery backed unbalanced ring injected ringing. For tip injected ringing just reverse the leads to the phone. The ringing source could also be balanced.

NOTE: The $\overline{DET}$ output will toggle at 20Hz because the DT input is not completely filtered by C_{RT}. Software can examine the duty cycle and determine if the $\overline{DET}$ pin is low for more that half the time, if so the off-hook condition is indicated.

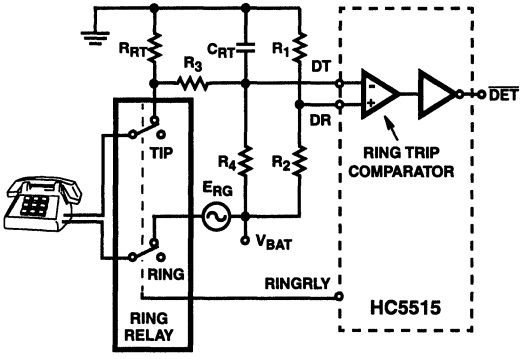


FIGURE 18. RING TRIP CIRCUIT FOR BATTERY BACKED RINGING

Longitudinal Impedance

The feedback loop described in Figure 19(A, B) realizes the desired longitudinal impedances from tip to ground and from ring to ground. Nominal longitudinal impedance is resistive and in the order of 22Ω.

In the presence of longitudinal currents this circuit attenuates the voltages that would otherwise appear at the tip and ring terminals, to levels well within the common mode range of the SLIC. In fact, longitudinal currents may exceed the programmed DC loop current without disturbing the SLIC's VF transmission capabilities.

The function of this circuit is to maintain the tip and ring voltages symmetrically around $V_{BAT}/2$, in the presence of longitudinal currents. The differential transconductance amplifiers G_T and G_R accomplish this by sourcing or sinking the required current to maintain V_C at $V_{BAT}/2$.

When a longitudinal current is injected onto the tip and ring inputs, the voltage at VC moves from it's equilibrium value VBAT/2. When VC changes by the amount DVC, this change appears between the input terminals of the differential transconductance amplifiers GT and GR. The output of GT and GR are the differential currents DI1 and DI2, which in turn feed the differential inputs of current sources IT and IR respectively. IT and IR have current gains of 250 single ended and 500 differentially, thus leading to a change in IT and IR that is equal to 500(DI) and 500(DI2).

The circuit shown in Figure 19(B) illustrates the tip side of the longitudinal network. The advantages of a differential input current source are: improved noise since the noise due to current source $2I_O$ is now correlated, power savings due to differential current gain and minimized offset error at the Operational Amplifier inputs via the two 5kΩ resistors.

Digital Logic Inputs

Table 1 is the logic truth table for the TTL compatible logic input pins. The HC5515 has an enable input pin (E0) and two control inputs pins (C1, C2).

The enable pin E0 is used to enable or disable the $\overline{DET}$ output pin. The $\overline{DET}$ pin is enabled if E0 is at a logic level 0 and disabled if E0 is at a logic level 1.

A combination of the control pins C1 and C2 is used to select 1 of the 4 possible operating states. A description of each operating state and the control logic follow:

Open Circuit State (C1 = 0, C2 = 0)

In this state the SLIC is effectively off. All detectors and both the tip and ring line drive amplifiers are powered down, presenting a high impedance to the line. Power dissipation is at a minimum.

Active State (C1 = 0, C2 = 1)

The tip output is capable of sourcing loop current and for open circuit conditions is about -4V from ground. The ring output is capable of sinking loop current and for open circuit conditions is about V_{BAT} +4V. VF signal transmission is normal. The loop current detector is active, E0 determines if the detector is gated to the $\overline{DET}$ output.

Ringing State (C1 = 1, C2 = 0)

The ring relay driver and the ring trip detector are activated. Both the tip and ring line drive amplifiers are powered down. Both tip and ring are disconnected from the line via the external ring relay.

Standby State (C1 = 1, C2 = 1)

Both the tip and ring line drive amplifiers are powered down. Internal resistors are connected between tip to ground and ring to V_{BAT} to allow loop current detect in an off-hook condition. The loop current and ground key detectors are both active, E0 determines if the detector is gated to the $\overline{DET}$ output.

AC Transmission Circuit Stability

To ensure stability of the AC transmission feedback loop two compensation capacitors C_{TC} and C_{RC} are required. Figure 20 (Application Circuit) illustrates their use. Recommended value is 2200pF.

SLIC Operating States

TABLE 1. LOGIC TRUTH TABLE

E0	C1	C2	SLIC OPERATING STATE	ACTIVE DETECTOR	$\overline{DET}$ OUTPUT
0	0	0	Open Circuit	No Active Detector	Logic Level High
0	0	1	Active	Loop Current Detector	Loop Current Status
0	1	0	Ringing	Ring Trip Detector	Ring Trip Status
0	1	1	Standby	Loop Current Detector	Loop Current Status
1	0	0	Open Circuit	No Active Detector	Logic Level High
1	0	1	Active	Loop Current Detector	
1	1	0	Ringing	Ring Trip Detector	
1	1	1	Standby	Loop Current Detector	

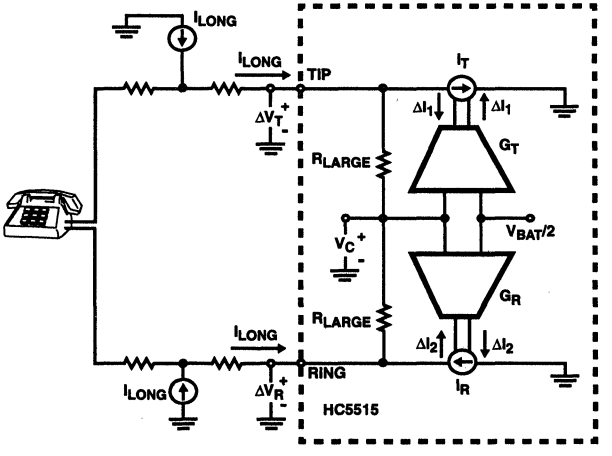


FIGURE 19A.

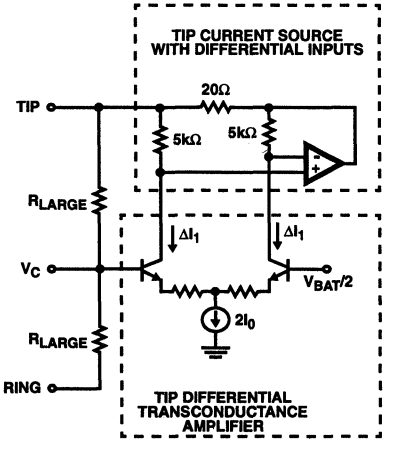


FIGURE 19B.

FIGURE 19. LONGITUDINAL IMPEDANCE NETWORK

AC-DC Separation Capacitor, C_{HP}

The high pass filter capacitor connected between pins HPT and HPR provides the separation between circuits sensing tip to ring DC conditions and circuits processing AC signals. A 10nf C_{HP} will position the low end frequency response 3dB break point at 48Hz. Where:

$$f_{3dB} = \frac{1}{(2 \bullet \pi \bullet R_{HP} \bullet C_{HP})} \quad \text{(EQ. 28)}$$

where R_{HP} = 330kΩ

Thermal Shutdown Protection

The HC5515's thermal shutdown protection is invoked if a fault condition on the tip or ring causes the temperature of the die to exceed 160°C. If this happens, the SLIC goes into a high impedance state and will remain there until the temperature of the die cools down by about 20°C. The SLIC will return back to its normal operating mode, providing the fault condition has been removed.

Surge Voltage Protection

The HC5515 must be protected against surge voltages and power crosses. Refer to "Maximum Ratings" TIPX and RINGX terminals for maximum allowable transient tip and ring voltages. The protection circuit shown in Figure 20 utilizes diodes together with a clamping device to protect tip and ring against high voltage transients.

Positive transients on tip or ring are clamped to within a couple of volts above ground via diodes D_1 and D_2. Under normal operating conditions D_1 and D_2 are reverse biased and out of the circuit.

Negative transients on tip and ring are clamped to within a couple of volts below ground via diodes D_3 and D_4 with the help of a Surgector. The Surgector is required to block conduction through diodes D_3 and D_4 under normal operating conditions and allows negative surges to be returned to system ground.

In applications where only low energy transients (<300V) are possible, diodes D_3 and D_4 could be connected to V_{BAT}, eliminating the requirement of the Surgector. Caution should be used with this application. Be aware that: surge protection is for low level transients only and will subject the batteries to negative voltage surges.

The fuse resistors (R_F) serve a dual purpose of being non-destructive power dissipaters during surge and fuses when the line in exposed to a power cross.

Power-Up Sequence

The HC5515 has **no** required power-up sequence. This is a result of the **D**ielectrically **I**solated (DI) process used in the fabrication of the part. By using the DI process, care is no longer required to insure that the substrate be kept at the most negative potential as with junction isolated ICs.

Printed Circuit Board Layout

Care in the printed circuit board layout is essential for proper operation. All connections to the RSN pin should be made as close to the device pin as possible, to limit the interference that might be injected into the RSN terminal. It is good practice to surround the RSN pin with a ground plane.

The analog and digital grounds should be tied together at the device.

Notes

2. **Overload Level (Two-Wire port)** - The overload level is specified at the 2-wire port (V_{TR0}) with the signal source at the 4-wire receive port (E_{RX}). I_{DCMET} = 23mA, R_{SG} = 4kΩ, increase the amplitude of E_{RX} until 1% THD is measured at V_{TRO}. Reference Figure 1.

3. **Longitudinal Impedance** - The longitudinal impedance is computed using the following equations, where TIP and RING voltages are referenced to ground. L_{ZT}, L_{ZR}, V_T, V_R, A_R and A_T are defined in Figure 2.

   (TIP) $L_{ZT} = V_T/A_T$

   (RING) $L_{ZR} = V_R/A_R$

   where: $E_L = 1V_{RMS}$ (0Hz to 100Hz)

4. **Longitudinal Current Limit (Off-Hook Active)** - Off-Hook (Active, C_1 = 1, C_2 = 0) longitudinal current limit is determined by increasing the amplitude of E_L (Figure 3A) until the 2-wire longitudinal balance drops below 45dB. $\overline{DET}$ pin remains low (no false detection).

5. **Longitudinal Current Limit (On-Hook Standby)** - On-Hook (Active, C_1 = 1, C_2 = 1) longitudinal current limit is determined by increasing the amplitude of E_L (Figure 3B) until the 2-wire longitudinal balance drops below 45dB. $\overline{DET}$ pin remains high (no false detection).

6. **Longitudinal to Metallic Balance** - The longitudinal to metallic balance is computed using the following equation:

   $BLME = 20 \bullet \log (E_L/V_{TR})$, where: E_L and V_{TR} are defined in Figure 4.

7. **Metallic to Longitudinal FCC Part 68, Para 68.310** - The metallic to longitudinal balance is defined in this spec.

8. **Longitudinal to Four-Wire Balance** - The longitudinal to 4-wire balance is computed using the following equation:

   $BLFE = 20 \bullet \log (E_L/V_{TX})$,: E_L and V_{TX} are defined in Figure 4.

9. **Metallic to Longitudinal Balance** - The metallic to longitudinal balance is computed using the following equation:

   $BMLE = 20 \bullet \log (E_{TR}/V_L)$, $E_{RX} = 0$

   where: E_{TR}, V_L and E_{RX} are defined in Figure 5.

10. **Four-Wire to Longitudinal Balance** - The 4-wire to longitudinal balance is computed using the following equation:

    $BFLE = 20 \bullet \log (E_{RX}/V_L)$, E_{TR} = source is removed.

    where: E_{RX}, V_L and E_{TR} are defined in Figure 5.

11. **Two-Wire Return Loss** - The 2-wire return loss is computed using the following equation:

    $r = -20 \bullet \log (2V_M/V_S)$

    where: Z_D = The desired impedance; e.g., the characteristic impedance of the line, nominally 600Ω. (Reference Figure 6).

12. **Overload Level (4-Wire port)** - The overload level is specified at the 4-wire transmit port (V_{TXO}) with the signal source (E_G) at the 2-wire port, I_{DCMET} = 23mA, Z_L = 20kΩ, R_{SG} = 4kΩ (Reference Figure 7). Increase the amplitude of E_G until 1% THD is measured at V_{TXO}. Note that the gain from the 2-wire port to the 4-wire port is equal to 1.

13. **Output Offset Voltage** - The output offset voltage is specified with the following conditions: E_G = 0, I_{DCMET} = 23mA, Z_L = ∞ and is measured at V_{TX}. E_G, I_{DCMET}, V_{TX} and Z_L are defined in Figure 7. Note: I_{DCMET} is established with a series 600Ω resistor between tip and ring.

14. **Two-Wire to Four-Wire (Metallic to V_{TX}) Voltage Gain** - The 2-wire to 4-wire (metallic to V_{TX}) voltage gain is computed using the following equation.

    $G_{2-4} = (V_{TX}/V_{TR})$, E_G = 0dBm0, V_{TX}, V_{TR}, and E_G are defined in Figure 7.

15. **Current Gain RSN to Metallic** - The current gain RSN to Metallic is computed using the following equation:

    $K = I_M [(R_{DC1} + R_{DC2})/(V_{RDC} - V_{RSN})]$ K, I_M, R_{DC1}, R_{DC2}, V_{RDC} and V_{RSN} are defined in Figure 8.

16. **Two-Wire to Four-Wire Frequency Response** - The 2-wire to 4-wire frequency response is measured with respect to E_G = 0dBm at 1.0kHz, E_{RX} = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    $F_{2-4} = 20 \bullet \log (V_{TX}/V_{TR})$, vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TX}, V_{TR}, and E_G are defined in Figure 9.

17. **Four-Wire to Two-Wire Frequency Response** - The 4-wire to 2-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    $F_{4-2} = 20 \bullet \log (V_{TR}/E_{RX})$, vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TR} and E_{RX} are defined in Figure 9.

18. **Four-Wire to Four-Wire Frequency Response** - The 4-wire to 4-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    $F_{4-4} = 20 \bullet \log (V_{TX}/E_{RX})$, vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TX} and E_{RX} are defined in Figure 9.

19. **Two-Wire to Four-Wire Insertion Loss** - The 2-wire to 4-wire insertion loss is measured with respect to E_G = 0dBm at 1.0kHz input signal, E_{RX} = 0, I_{DCMET} = 23mA and is computed using the following equation:

    $L_{2-4} = 20 \bullet \log (V_{TX}/V_{TR})$

    where: V_{TX}, V_{TR}, and E_G are defined in Figure 9. (Note: The fuse resistors, R_F, impact the insertion loss. The specified insertion loss is for R_F = 0).

20. **Four-Wire to Two-Wire Insertion Loss** - The 4-wire to 2-wire insertion loss is measured based upon E_{RX} = 0dBm, 1.0kHz input signal, E_G = 0, I_{DCMET} = 23mA and is computed using the following equation:

    $L_{4-2} = 20 \bullet \log (V_{TR}/E_{RX})$

    where: V_{TR} and E_{RX} are defined in Figure 9.

21. **Two-Wire to Four-Wire Gain Tracking** - The 2-wire to 4-wire gain tracking is referenced to measurements taken for E_G = -10dBm, 1.0kHz signal, E_{RX} = 0, I_{DCMET} = 23mA and is computed using the following equation.

    $G_{2-4} = 20 \bullet \log (V_{TX}/V_{TR})$ vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

    V_{TX} and V_{TR} are defined in Figure 9.

22. **Four-Wire to Two-Wire Gain Tracking** - The 4-wire to 2-wire gain tracking is referenced to measurements taken for E_{RX} = -10dBm, 1.0kHz signal, E_G = 0, I_{DCMET} = 23mA and is computed using the following equation:

    $G_{4-2} = 20 \bullet \log (V_{TR}/E_{RX})$ vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

    V_{TR} and E_{RX} are defined in Figure 9. The level is specified at the 4-wire receive port and referenced to a 600Ω impedance level.

23. **Two-Wire Idle Channel Noise** - The 2-wire idle channel noise at V_{TR} is specified with the 2-wire port terminated in 600Ω (R_L) and with the 4-wire receive port grounded (Reference Figure 10).

24. **Four-Wire Idle Channel Noise** - The 4-wire idle channel noise at V_{TX} is specified with the 2-wire port terminated in 600Ω (R_L). The noise specification is with respect to a 600Ω impedance level at V_{TX}. The 4-wire receive port is grounded (Reference Figure 10).

25. **Harmonic Distortion (2-Wire to 4-Wire)** - The harmonic distortion is measured with the following conditions. E_G = 0dBm at 1kHz, I_{DCMET} = 23mA. Measurement taken at V_{TX}. (Reference Figure 7).

26. **Harmonic Distortion (4-Wire to 2-Wire)** - The harmonic distortion is measured with the following conditions. E_{RX} = 0dBm0. Vary frequency between 300Hz and 3.4kHz, I_{DCMET} = 23mA. Measurement taken at V_{TR}. (Reference Figure 9).

27. **Constant Loop Current** - The constant loop current is calculated using the following equation:

    $I_L = 2500 / (R_{DC1} + R_{DC2})$

28. **Standby State Loop Current** - The standby state loop current is calculated using the following equation:

    $I_L = [|V_{BAT}| - 3] / [R_L + 1800]$, $T_A = 25^oC$

29. **Power Supply Rejection Ratio** - Inject a 100mV_{RMS} signal (50Hz to 4kHz) on V_{BAT}, V_{CC} and V_{EE} supplies. PSRR is computed using the following equation:

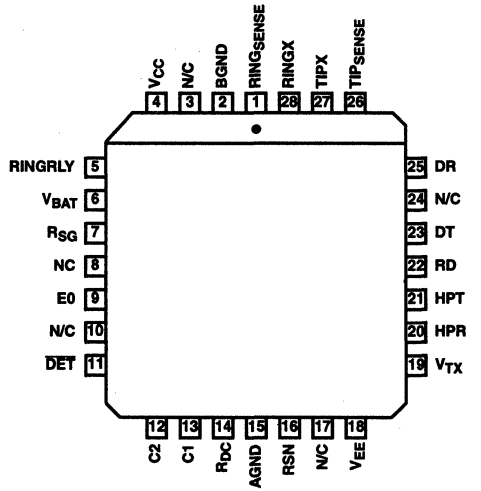
    $PSRR = 20 \bullet \log (V_{TX}/V_{IN})$. V_{TX} and V_{IN} are defined in Figure 11.

Pin Descriptions

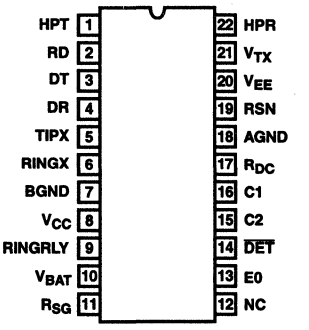
PLCC	PDIP	SYMBOL	DESCRIPTION
1		$RING_{SENSE}$	Internally connected to output of RING power amplifier.
2	7	BGND	Battery Ground - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from AGND but it is recommended that it is connected to the same potential as AGND.
4	8	V_{CC}	+5V power supply.
5	9	RINGRLY	Ring relay driver output.
6	10	V_{BAT}	Battery supply voltage, -24V to -56V.
7	11	R_{SG}	Saturation guard programming resistor pin.
8	12	NC	This pin is used during manufacturing.This pin is to be left open for proper SLIC operation .
9	13	E0	TTL compatible logic input. Enables the $\overline{DET}$ output when set to logic level zero and disables $\overline{DET}$ output when set to a logic level one.
11	14	$\overline{DET}$	Detector output. TTL compatible logic output. A zero logic level indicates that the selected detector was triggered (see Truth Table for selection of Ground Key detector, Loop Current detector or the Ring Trip detector). The $\overline{DET}$ output is an open collector with an internal pull-up of approximately 15kΩ to V_{CC}.
12	15	C2	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
13	16	C1	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
14	17	R_{DC}	DC feed current programming resistor pin. Constant current feed is programmed by resistors R_{DC1} and R_{DC2} connected in series from this pin to the receive summing node (RSN). The resistor junction point is decoupled to AGND to isolate the AC signal components.
15	18	AGND	Analog ground.
16	19	RSN	Receive Summing Node. The AC and DC current flowing into this pin establishes the metallic loop current that flows between tip and ring. The magnitude of the metallic loop current is 1000 times greater than the current into the RSN pin. The constant current programming resistors and the networks for program receive gain and 2-wire impedance all connect to this pin.
18	20	V_{EE}	-5V power supply.
19	21	V_{TX}	Transmit audio output. This output is equivalent to the TIP to RING metallic voltage. The network for programming the 2-wire input impedance connects between this pin and RSN.
20	22	HPR	RING side of AC/DC separation capacitor C_{HP}. C_{HP} is required to properly separate the ring AC current from the DC loop current. The other end of C_{HP} is connected to HPT.
21	1	HPT	TIP side of AC/DC separation capacitor C_{HP}. C_{HP} is required to properly separate the tip AC current from the DC loop current. The other end of C_{HP} is connected to HPR.
22	2	RD	Loop current programming resistor. Resistor R_D sets the trigger level for the loop current detect circuit. A filter capacitor C_D is also connected between this pin and V_{EE}.
23	3	DT	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR.
25	4	DR	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR.
26		TIP_{SENSE}	Internally connected to output of tip power amplifier.
27	5	TIPX	Output of tip power amplifier.
28	6	RINGX	Output of ring power amplifier.
3, 10 17, 24		N/C	No internal connection.

Pinouts

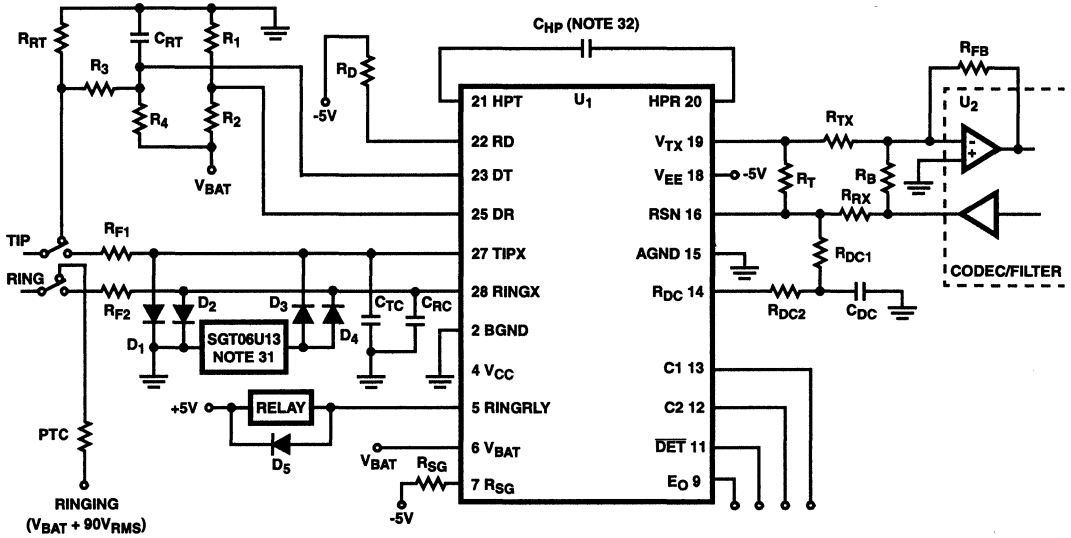
HC5515
(PLCC)
TOP VIEW



HC5515
(PDIP)
TOP VIEW



Application Circuit



U1	SLIC (Subscriber Line Interface Circuit) HC5515	R_1, R_3	200kΩ, 5%, 1/4W
U2	Combination CODEC/Filter e.g. CD22354A or Programmable CODEC/ Filter, e.g. SLAC	R_2	910kΩ, 5%, 1/4W
		R_4	1.2MΩ, 5%, 1/4W
C_{DC}	1.5µF, 20%, 10V	R_B	18.7kΩ,1%, 1/4W
C_{HP}	10nF, 20%, 100V (Note 2)	R_D	39kΩ, 5%, 1/4W
C_{RT}	0.39µF, 20%, 100V	R_{DC1}, R_{DC2}	41.2kΩ, 5%, 1/4W
C_{TC}, C_{RC}	2200pF, 20%, 100V	R_{FB}	20.0kΩ, 1%, 1/4W
Relay	Relay, 2C Contacts, 5V Coil	R_{RX}	280kΩ, 1%, 1/4W
D_1 - D_4	Diode, 100V, 3A	R_T	562kΩ, 1%, 1/4W
Surgector	SGT06U13	R_{TX}	20kΩ, 1%, 1/4W
D_5	Diode, 1N4454	R_{RT}	150Ω, 5%, 2W
R_{F1}, R_{F2}	Line Resistor, 20Ω, 1% Match	R_{SG}	V_{BAT} = -28V, R_{SG} = ∞ V_{BAT} = -48V, R_{SG} = 4.0kΩ, 1/4W 5%

NOTE:

30. The anodes of D_3 and D_4 may be connected directly to the V_{BAT} supply if the application is exposed to only low energy transients. For harsher environments it is recommended that the anodes of D_3 and D_4 be shorted to ground through a transzorb or surgector.
31. To meet the specified 25dB 2-wire return loss at 200Hz, C_{HP} needs to be 20nF, 20%, 100V.

FIGURE 20. APPLICATION CIRCUIT

HARRIS SEMICONDUCTOR

HC5523

SLIC
Subscriber Line Interface Circuit

January 1997

Features

- DI Monolithic High Voltage Process
- Programmable Current Feed (20mA to 60mA)
- Programmable Loop Current Detector Threshold and Battery Feed Characteristics
- Ground Key and Ring Trip Detection
- Compatible with Ericsson's PBL3764A/4
- Thermal Shutdown
- On-Hook Transmission
- Wide Battery Voltage Range (-24V to -58V)
- Low Standby Power
- Meets TR-NWT-000057 Transmission Requirements
- -40°C to 85°C Ambient Temperature Range

Applications

- Digital Loop Carrier Systems
- Fiber-In-The-Loop ONUs
- Wireless Local Loop
- Hybrid Fiber Coax
- Pair Gain
- POTS
- PABX
- Related Literature
  - AN9632, Operation of the HC5523/15 Evaluation Board

Description

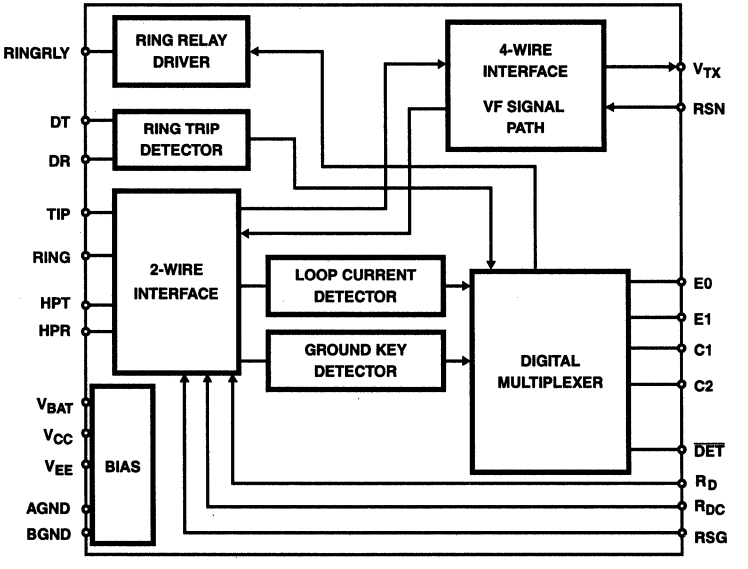
The HC5523 is a subscriber line interface circuit which is interchangeable with Ericsson's PBL3764A/4 for distributed central office applications. Enhancements include immunity to circuit latch-up during hot plug and absence of false signaling in the presence of longitudinal currents.

The HC5523 is fabricated in a High Voltage Dielectrically Isolated (DI) Bipolar Process that eliminates leakage currents and device latch-up problems normally associated with junction isolated ICs. The elimination of the leakage currents results in improved circuit performance for wide temperature extremes. The latch free benefit of the DI process guarantees operation under adverse transient conditions. This process feature makes the HC5523 ideally suited for use in harsh outdoor environments.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC5523IM	-40 to 85	28 Ld PLCC	N28.45
HC5523IP	-40 to 85	22 Ld PDIP	E22.4

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4144.1**

Absolute Maximum Ratings

Temperature, Humidity
- Storage Temperature Range . . . . . -65°C to 150°C
- Operating Temperature Range . . . . . -40°C to 110°C
- Operating Junction Temperature Range . . . . . -40°C to 150°C

Power Supply (-40°C ≤ T_A ≤ 85°C)
- Supply Voltage V_{CC} to GND . . . . . 0.5V to 7V
- Supply Voltage V_{EE} to GND . . . . . -7V to 0.5V
- Supply Voltage V_{BAT} to GND . . . . . -80V to 0.5V

Ground
- Voltage between AGND and BGND . . . . . -0.3V to 0.3V

Relay Driver
- Ring Relay Supply Voltage . . . . . 0V to V_{BAT} +75V
- Ring Relay Current 50mA

Ring Trip Comparator
- Input Voltage . . . . . V_{BAT} to 0V
- Input Current . . . . . -5mA to 5mA

Digital Inputs, Outputs (C1, C2, E0, E1, $\overline{DET}$)
- Input Voltage . . . . . 0V to V_{CC}
- Output Voltage ($\overline{DET}$ Not Active) . . . . . 0V to V_{CC}
- Output Current ($\overline{DET}$) 5mA

Tipx and Ringx Terminals (-40°C ≤ T_A ≤ +85°C)
- Tipx or Ringx Voltage, Continuous (Referenced to GND) V_{BAT} to +2V
- Tipx or Ringx, Pulse < 10ms, T_{REP} > 10s . . . . V_{BAT} -20V to +5V
- Tipx or Ringx, Pulse < 10µs, T_{REP} > 10s . . . . V_{BAT} -40V to +10V
- Tipx or Ringx, Pulse < 250ns, T_{REP} > 10s . . . V_{BAT} -70V to +15V
- Tipx or Ringx Current 70mA

ESD Rating 500V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}
22 Lead PDIP Package	53°C/W
28 Lead PLCC Package	53°C/W

Continuous Power Dissipation at 70°C
- 22 Lead PDIP Package 1.5W
- 28 Lead PLCC Package 1.5W

Package Power Dissipation at 70°C, t < 100ms, t_{REP} > 1s
- 22 Lead PDIP Package 4W
- 28 Lead PLCC Package 4W

Derate above . . . . . 70°C
- Plastic DIP . . . . . 18.8mW/°C
- PLCC . . . . . 18.8mW/°C

Maximum Junction Temperature Range . . . . . -40°C to 150°C
Maximum Storage Temeprature Range . . . . . -65°C to 150°C
Maximum Lead Temperature . . . . . 300°C
(Soldering 10s, PLCC Lead Tips Only)

Die Characteristics

Gate Count . . . . . 543 Transistors, 51 Diodes

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Typical Operating Conditions

These represent the conditions under which the part was developed and are suggested as guidelines.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Case Temperature		-40	-	100	°C
V_{CC} with Respect to AGND	-40°C to 85°C	4.75	-	5.25	V
V_{EE} with Respect to AGND	-40°C to 85°C	-5.25	-	-4.75	V
V_{BAT} with Respect to BGND	-40°C to 85°C	-58	-	-24	V

Electrical Specifications

T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -48V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = 0Ω, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Overload Level	1% THD, Z_L = 600Ω, (Note 2, Figure 1)	3.1	-	-	V_{PEAK}
Longitudinal Impedance (Tip/Ring)	0 < f < 100Hz (Note 3, Figure 2)	-	20	35	Ω/Wire

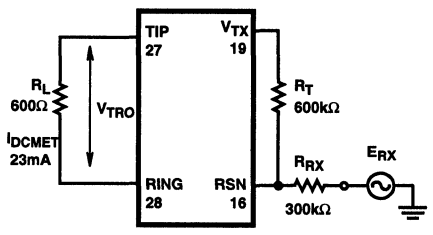


FIGURE 1. OVERLOAD LEVEL (TWO-WIRE PORT)

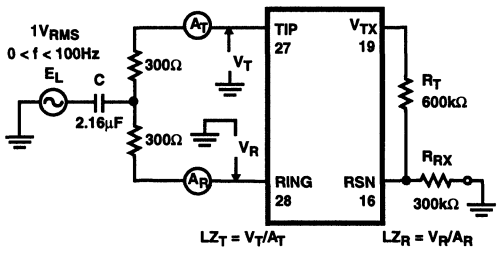


FIGURE 2. LONGITUDINAL IMPEDANCE

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -48V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = 0Ω, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LONGITUDINAL CURRENT LIMIT (TIP/RING)					
Off-Hook (Active)	No False Detections, (Loop Current), LB > 45dB (Note 4, Figure 3A)	27	-	-	mA_{PEAK}/ Wire
On-Hook (Standby), R_L = ∞	No False Detections (Loop Current) (Note 5, Figure 3B)	8.5	-	-	mA_{PEAK}/ Wire

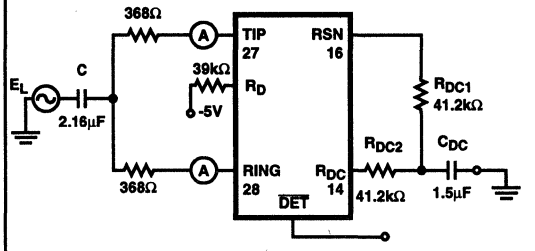


FIGURE 3A. OFF-HOOK

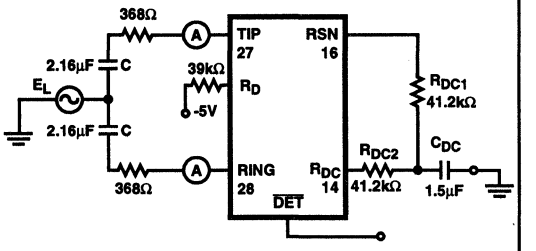


FIGURE 3B. ON-HOOK

FIGURE 3. LONGITUDINAL CURRENT LIMIT

OFF-HOOK LONGITUDINAL BALANCE					
Longitudinal to Metallic	IEEE 455 - 1985, R_{LR}, R_{LT} = 368Ω 0.2kHz < f < 4.0kHz (Note 6, Figure 4)	58	70	-	dB
Longitudinal to Metallic	R_{LR}, R_{LT} = 300Ω, 0.2kHz < f < 4.0kHz (Note 6, Figure 4)	58	70	-	dB
Metallic to Longitudinal	FCC Part 68, Para 68.310 0.2kHz < f < 1.0kHz	50	55	-	dB
	1.0kHz < f < 4.0kHz (Note 7)	50	55	-	dB
Longitudinal to 4-Wire	0.2kHz < f < 4.0kHz (Note 8, Figure 4)	58	70	-	dB
Metallic to Longitudinal	R_{LR}, R_{LT} = 300Ω, 0.2kHz < f < 4.0kHz (Note 9, Figure 5)	50	55	-	dB
4-Wire to Longitudinal	0.2kHz < f < 4.0kHz (Note 10, Figure 5)	50	55	-	dB

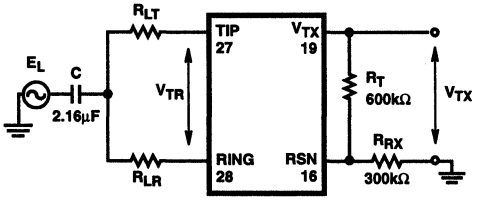


FIGURE 4. LONGITUDINAL TO METALLIC AND LONGITUDINAL TO 4-WIRE BALANCE

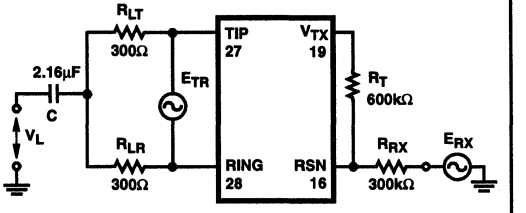


FIGURE 5. METALLIC TO LONGITUDINAL AND 4-WIRE TO LONGITUDINAL BALANCE

2-Wire Return Loss C_{HP} = 20nF	0.2kHz to 0.5kHz (Note 11, Figure 6)	25	-	-	dB
	0.5kHz to 1.0kHz (Note 11, Figure 6)	27	-	-	dB
	1.0kHz to 3.4kHz (Note 11, Figure 6)	23	-	-	dB

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -48V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = 0Ω, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TIP IDLE VOLTAGE					
Active, I_L = 0		-	-4	-	V
Standby, I_L = 0		-	<0	-	V
RING IDLE VOLTAGE					
Active, I_L = 0		-	-44	-	V
Standby, I_L = 0		-	>-48	-	V
TIP-RING Open Loop Metallic Voltage, V_{TR}	V_{BAT} = -52V, R_{SG} = 0Ω	43	-	47	V
4-WIRE TRANSMIT PORT (V_{TX})					
Overload Level	(Z_L > 20kΩ, 1% THD) (Note 12, Figure 7)	3.1	-	-	V_{PEAK}
Output Offset Voltage	E_G = 0, Z_L = ∞, (Note 13, Figure 7)	-60	-	60	mV
Output Impedance (Guaranteed by Design)	0.2kHz < f < 03.4kHz	-	5	20	Ω
2- to 4-Wire (Metallic to V_{TX}) Voltage Gain	0.3kHz < f < 03.4kHz (Note 14, Figure 7)	0.98	1.0	1.02	V/V

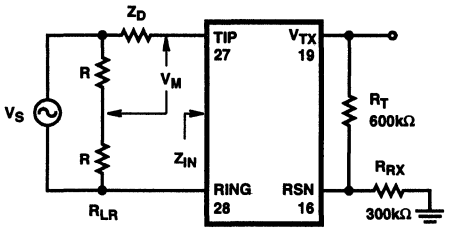


FIGURE 6. TWO-WIRE RETURN LOSS

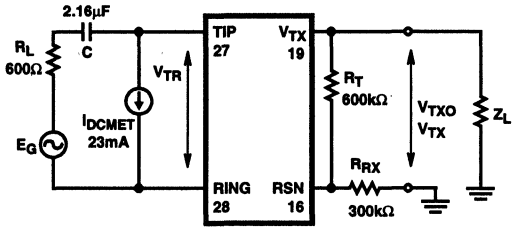


FIGURE 7. OVERLOAD LEVEL (4-WIRE TRANSMIT PORT), OUTPUT OFFSET VOLTAGE, 2-WIRE TO 4-WIRE VOLTAGE GAIN AND HARMONIC DISTORTION

4-WIRE RECEIVE PORT (RSN)					
DC Voltage	I_{RSN} = 0mA	-	0	-	V
R_X Sum Node Impedance (Gtd by Design)	0.2kHz < f < 3.4kHz	-	-	20	Ω
Current Gain-RSN to Metallic	0.3kHz < f < 3.4kHz (Note 15, Figure 8)	980	1000	1020	Ratio
FREQUENCY RESPONSE (OFF-HOOK)					
2-Wire to 4-Wire	0dBm at 1.0kHz, E_{RX} = 0V 0.3kHz < f < 3.4kHz (Note 16, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm at 1.0kHz, E_G = 0V 0.3kHz < f < 3.4kHz (Note 17, Figure 9)	-0.2	-	0.2	dB
4-Wire to 4-Wire	0dBm at 1.0kHz, E_G = 0V 0.3kHz < f < 3.4kHz (Note 18, Figure 9)	-0.2	-	0.2	dB
INSERTION LOSS					
2-Wire to 4-Wire	0dBm, 1kHz (Note 19, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm, 1kHz (Note 20, Figure 9)	-0.2	-	0.2	dB
GAIN TRACKING (Ref = -10dBm, at 1.0kHz)					
2-Wire to 4-Wire	+3dBm to +7dBm (Note 21, Figure 9)	-0.15	-	0.15	dB
2-Wire to 4-Wire	-40dBm to +3dBm (Note 21, Figure 9)	-0.1	-	0.1	dB

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -48V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = 0Ω, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2-Wire to 4-Wire	-55dBm to -40dBm (Note 21, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	-40dBm to +7dBm (Note 22, Figure 9)	-0.1	-	0.1	dB
4-Wire to 2-Wire	-55dBm to -40dBm (Note 22, Figure 9)	-0.2	-	0.2	dB

$GRX = ((V_{TR1} - V_{TR2})(300k))/(-3)(600)$

Where: V_{TR1} is the Tip to Ring Voltage with V_{RSN} = 0V
and V_{TR2} is the Tip to Ring Voltage with V_{RSN} = -3V

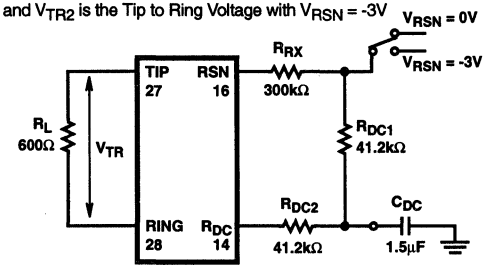


FIGURE 8. CURRENT GAIN-RSN TO METALLIC

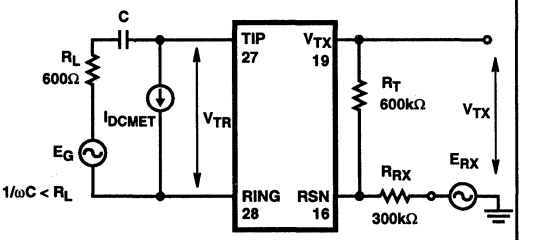
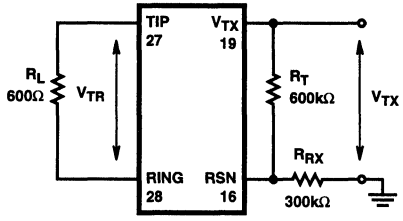
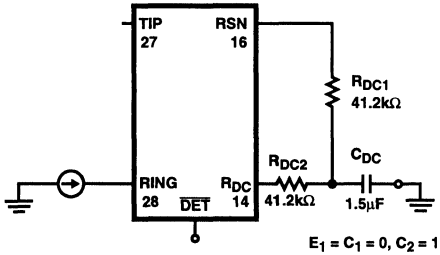


FIGURE 9. FREQUENCY RESPONSE, INSERTION LOSS, GAIN TRACKING AND HARMONIC DISTORTION

NOISE					
Idle Channel Noise at 2-Wire	C-Message Weighting (Note 23, Figure 10)	-	8.5	-	dBrnC
	Psophometrical Weighting (Note 23, Figure 10)	-	-81.5	-	dBrnp
Idle Channel Noise at 4-Wire	C-Message Weighting (Note 24, Figure 10)	-	8.5	-	dBrnC
	Psophometrical Weighting (Note 23, Figure 10)	-	-81.5	-	dBrnp
HARMONIC DISTORTION					
2-Wire to 4-Wire	0dBm, 1kHz (Note 25, Figure 7)	-	-65	-54	dB
4-Wire to 2-Wire	0dBm, 0.3kHz to 3.4kHz (Note 26, Figure 9)	-	-65	-54	dB
BATTERY FEED CHARACTERISTICS					
Constant Loop Current Tolerance R_{DCX} = 41.2kΩ	$I_L = 2500/(R_{DC1} + R_{DC2})$, -40°C to 85°C (Note 27)	$0.92I_L$	I_L	$1.08I_L$	mA
Loop Current Tolerance (Standby)	$I_L = (V_{BAT}-3)/(R_L+1800)$, -40°C to 85°C (Note 28)	$0.8I_L$	I_L	$1.2I_L$	mA
Open Circuit Voltage (V_{TIP} - V_{RING})	-40°C to 85°C, (Active) R_{SG} = ∞	14	16.67	20	V
LOOP CURRENT DETECTOR					
On-Hook to Off-Hook	R_D = 39kΩ, -40°C to 85°C	$372/R_D$	$465/R_D$	$558/R_D$	mA
Off-Hook to On-Hook	R_D = 39kΩ, -40°C to 85°C	$325/R_D$	$405/R_D$	$485/R_D$	mA
Loop Current Hysteresis	R_D = 39kΩ, -40°C to 85°C	$25/R_D$	$60/R_D$	$95/R_D$	mA
GROUND KEY DETECTOR					
Tip/Ring Current Difference - Trigger	(Note 29, Figure 11)	8	12	17	mA
Tip/Ring Current Difference - Reset	(Note 29, Figure 11)	3	7	12	mA
Hysteresis	(Note 29, Figure 11)	0	5	9	mA

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -48V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = 0Ω, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
 FIGURE 10. IDLE CHANNEL NOISE					
 FIGURE 11. GROUND KEY DETECT					
RING TRIP DETECTOR (DT, DR)					
Offset Voltage	Source Res = 0	-20	-	20	mV
Input Bias Current	Source Res = 0	-360	-	360	nA
Input Common-Mode Range	Source Res = 0	V_{BAT} +1	-	0	V
Input Resistance	Source Res = 0, Unbalanced	1	-	-	MΩ
	Source Res = 0, Balanced	3	-	-	MΩ
RING RELAY DRIVER					
V_{SAT} at 25mA	I_{OL} = 25mA	-	0.2	0.6	V
Off-State Leakage Current	V_{OH} = 12V	-	-	10	µA
DIGITAL INPUTS (E0, E1, C1, C2)					
Input Low Voltage, V_{IL}		0	-	0.8	V
Input High Voltage, V_{IH}		2	-	V_{CC}	V
Input Low Current, I_{IL}: C1, C2	V_{IL} = 0.4V	-200	-	-	µA
Input Low Current, I_{IL}: E0, E1	V_{IL} = 0.4V	-100	-	-	µA
Input High Current	V_{IH} = 2.4V	-	-	40	µA
DETECTOR OUTPUT ($\overline{DET}$)					
Output Low Voltage, V_{OL}	I_{OL} = 2mA	-	-	0.45	V
Output High Voltage, V_{OH}	I_{OH} = 100µA	2.7	-	-	V
Internal Pull-Up Resistor		10	15	20	kΩ
POWER DISSIPATION (V_{BAT} = -48V)					
Open Circuit State	C1 = C2 = 0	-	26.3	41	mW
On-Hook, Standby	C1 = C2 = 1	-	37.5	57	mW
On-Hook, Active	C1 = 0, C2 = 1, R_L = High Impedance	-	110	216	mW
Off-Hook, Active	C1 = 0, C2 = 1, R_L = 600Ω	-	1.1	1.4	W
TEMPERATURE GUARD					
Thermal Shutdown		150	-	180	°C

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -48V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = 0Ω, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENTS (V_{BAT} = -28V)					
Open Circuit State (C1, 2 = 0, 0) On-Hook	I_{CC}	-	1.3	2.0	mA
	I_{EE}	-	0.6	0.9	mA
	I_{BAT}	-	0.35	0.55	mA
Standby State (C1, 2 = 1, 1) On-Hook	I_{CC}	-	1.6	2.25	mA
	I_{EE}	-	0.62	0.9	mA
	I_{BAT}	-	0.55	0.85	mA
Active State (C1, 2 = 0, 1) On-Hook	I_{CC}	-	3.7	5.8	mA
	I_{EE}	-	1.1	1.8	mA
	I_{BAT}	-	2.2	3.7	mA
PSRR					
V_{CC} to 2 or 4-Wire Port	(Note 30, Figure 12)	-	40	-	dB
V_{EE} to 2 or 4-Wire Port	(Note 30, Figure 12)	-	40	-	dB
V_{BAT} to 2 or 4-Wire Port	(Note 30, Figure 12)	-	40	-	dB

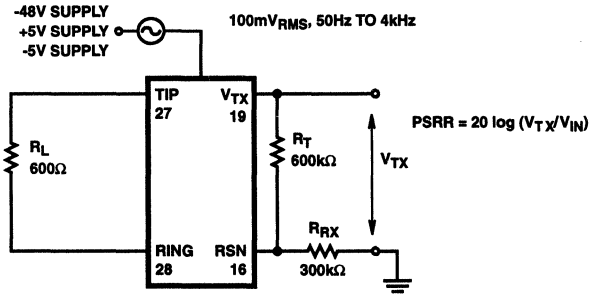


FIGURE 12. POWER SUPPLY REJECTION RATIO

Circuit Operation and Design Information

The HC5523 is a current feed voltage sense Subscriber Line Interface Circuit (SLIC). This means that for short loop applications the SLIC provides a programed constant current to the tip and ring terminals while sensing the tip to ring voltage.

The following discussion separates the SLIC's operation into its DC and AC path, then follows up with additional circuit and design information.

Constant Loop Current (DC) Path

SLIC in the Active Mode

The DC path establishes a constant loop current that flows out of tip and into the ring terminal. The loop current is programmed by resistors R_{DC1}, R_{DC2} and the voltage on the R_{DC} pin (Figure 13). The R_{DC} voltage is determined by the voltage across R_1 in the saturation guard circuit. Under constant current feed conditions, the voltage drop across R_1

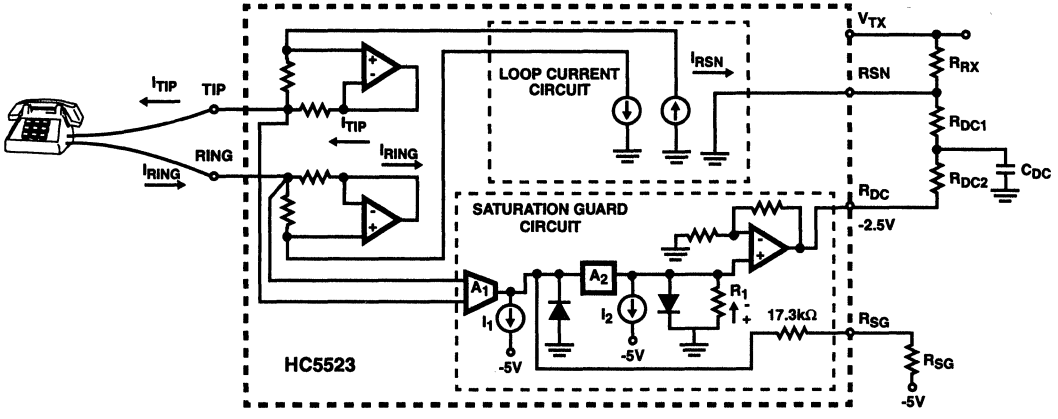


FIGURE 13. DC LOOP CURRENT

sets the R_{DC} voltage to -2.5V. This occurs when current flows through R_1 into the current source I_2. The R_{DC} voltage establishes a current (I_{RSN}) that is equal to $V_{RDC}/(R_{DC1}+R_{DC2})$. This current is then multiplied by 1000, in the loop current circuit, to become the tip and ring loop currents.

For the purpose of the following discussion, the saturation guard voltage is defined as the maximum tip to ring voltage at which the SLIC can provide a constant current for a given battery and overhead voltage.

For loop resistances that result in a tip to ring voltage less than the saturation guard voltage the loop current is defined as:

$$I_L = \frac{2.5V}{R_{DC1}+R_{DC2}} \times 1000 \qquad \text{(EQ. 1)}$$

where: I_L = Constant loop current.

R_{DC1} and R_{DC2} = Loop current programming resistors.

Capacitor C_{DC} between R_{DC1} and R_{DC2} removes the VF signals from the battery feed control loop. The value of C_{DC} is determined by Equation 2:

$$C_{DC} = T \times \left(\frac{1}{R_{DC1}} + \frac{1}{R_{DC2}}\right) \qquad \text{(EQ. 2)}$$

where T = 30ms

NOTE: The minimum C_{DC} value is obtained if $R_{DC1} = R_{DC2}$

Figure 14 illustrates the relationship between the tip to ring voltage and the loop resistance. For a 0Ω loop resistance both tip and ring are at $V_{BAT}/2$. As the loop resistance increases, so does the voltage differential between tip and ring. When this differential voltage becomes equal to the saturation guard voltage, the operation of the SLIC's loop feed changes from a constant current feed to a resistive feed. The loop current in the resistive feed region is no longer constant but varies as a function of the loop resistance.

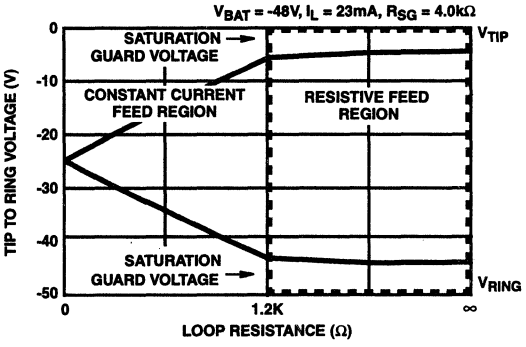
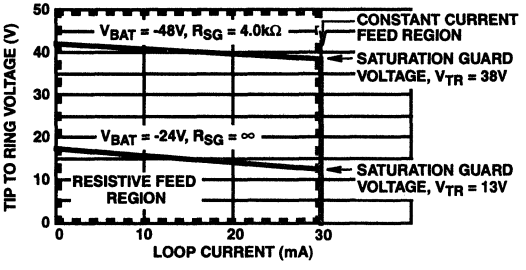


FIGURE 14. V_{TR} vs R_L

Figure 15 shows the relationship between the saturation guard voltage, the loop current and the loop resistance. Notice from Figure 15 that for a loop resistance <1.2kΩ (R_{SG} = 4.0kΩ) the SLIC is operating in the constant current feed region and for resistances >1.2kΩ the SLIC is operating in the resistive feed region. Operation in the resistive feed region allows long loop and off-hook transmission by keeping the tip and ring voltages off the rails. Operation in this region is transparent to the customer.



R_L	100kΩ	4kΩ	2kΩ	<1.2kΩ	R_{SG} = 4.0kΩ
R_L	100kΩ	1.5kΩ	700Ω	<400Ω	R_{SG} = ∞Ω

FIGURE 15. V_{TR} vs I_L and R_L

The Saturation Guard circuit (Figure 13) monitors the tip to ring voltage via the transconductance amplifier A_1. A_1 generates a current that is proportional to the tip to ring voltage difference. I_1 is internally set to sink all of A_1's current until the tip to ring voltage exceeds 12.5V. When the tip to ring voltage exceeds 12.5V (with no R_{SG} resistor) A_1 supplies more current than I_1 can sink. When this happens A_2 amplifies its input current by a factor of 12 and the current through R_1 becomes the difference between I_2 and the output current from A_2. As the current from A_2 increases, the voltage across R_1 decreases and the output voltage on R_{DC} decreases. This results in a corresponding decrease in the loop current. The R_{SG} pin provides the ability to increase the saturation guard reference voltage beyond 12.5V. Equation 3 gives the relationship between the R_{SG} resistor value and the programmable saturation guard reference voltage:

$$V_{SGREF} = 12.5 + \frac{5 \bullet 10^5}{R_{SG} + 17300} \quad \text{(EQ. 3)}$$

where:

V_{SGREF} = Saturation Guard reference voltage.

R_{SG} = Saturation Guard programming resistor.

When the Saturation guard reference voltage is exceeded, the tip to ring voltage is calculated using Equation 4:

$$V_{TR} = R_L \times \frac{16.66 + 5 \bullet 10^5/(R_{SG} + 17300)}{R_L + (R_{DC1} + R_{DC2})/600} \quad \text{(EQ. 4)}$$

where:

V_{TR} = Voltage differential between tip and ring.

R_L = Loop resistance.

For on-hook transmission $R_L = \infty$, Equation 4 reduces to:

$$V_{TR} = 16.66 + \frac{5 \bullet 10^5}{R_{SG} + 17300} \quad \text{(EQ. 5)}$$

The value of R_{SG} should be calculated to allow maximum loop length operation. This requires that the saturation guard reference voltage be set as high as possible without clipping the incoming or outgoing VF signal. A voltage margin of -4V on tip and -4V on ring, for a total of -8V margin, is recommended as a general guideline. The value of R_{SG} is calculated using Equation 6:

$$R_{SG} = \left(\frac{5 \bullet 10^5}{(|V_{BAT}| - V_{MAR}) \times \left(1 + \frac{(R_{DC1} + R_{DC2})}{600 R_L}\right) - 16.66V} - 17300 \right) \quad \text{(EQ. 6)}$$

where:

V_{BAT} = Battery voltage.

V_{MAR} = Voltage Margin. Recommended value of -8V to allow a maximum overload level of 3.1V peak.

For on-hook transmission $R_L = \infty$, Equation 6 reduces to:

$$R_{SG} = \frac{5 \bullet 10^5}{|V_{BAT}| - V_{MAR} - 16.66V} - 17300 \quad \text{(EQ. 7)}$$

SLIC in the Standby Mode

Overall system power is saved by configuring the SLIC in the standby state when not in use. In the standby state the tip and ring amplifiers are disabled and internal resistors are connected between tip to ground and ring to V_{BAT}. This connection enables a loop current to flow when the phone goes off-hook. The loop current detector then detects this current and the SLIC is configured in the active mode for voice transmission. The loop current in standby state is calculated as follows:

$$I_L \approx \frac{|V_{BAT}| - 3V}{R_L + 1800\Omega} \quad \text{(EQ. 8)}$$

where:

I_L = Loop current in the standby state.

R_L = Loop resistance.

V_{BAT} = Battery voltage.

(AC) Transmission Path

SLIC in the Active Mode

Figure 16 shows a simplified AC transmission model. Circuit analysis yields the following design equations:

$$V_{TR} = V_{TX} + I_M \bullet 2R_F \quad \text{(EQ. 9)}$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_M}{1000} \quad \text{(EQ. 10)}$$

$$V_{TR} = E_G - I_M \bullet Z_L \quad \text{(EQ. 11)}$$

where:

V_{TR} = Is the AC metallic voltage between tip and ring, including the voltage drop across the fuse resistors R_F.

V_{TX} = Is the AC metallic voltage. Either at the ground referenced 4-wire side or the SLIC tip and ring terminals.

I_M = Is the AC metallic current.

R_F = Is a fuse resistor.

Z_T = Is used to set the SLIC's 2-wire impedance.

V_{RX} = Is the analog ground referenced receive signal.

Z_{RX} = Is used to set the 4-wire to 2-wire gain.

E_G = Is the AC open circuit voltage.

Z_L = Is the line impedance.

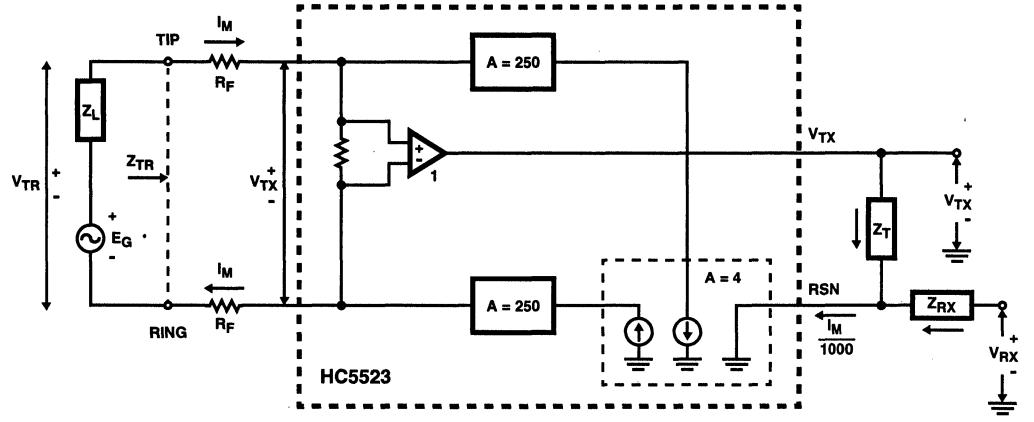


FIGURE 16. SIMPLIFIED AC TRANSMISSION CIRCUIT

(AC) 2-Wire Impedance

The AC 2-wire impedance (Z_{TR}) is the impedance looking into the SLIC, including the fuse resistors, and is calculated as follows:

Let $V_{RX} = 0$. Then from Equation 10

$$V_{TX} = Z_T \bullet \frac{I_M}{1000} \quad \text{(EQ. 12)}$$

Z_{TR} is defined as:

$$Z_{TR} = \frac{V_{TR}}{I_M} \quad \text{(EQ. 13)}$$

Substituting in Equation 9 for V_{TR}

$$Z_{TR} = \frac{V_{TX}}{I_M} + \frac{2R_F \bullet I_M}{I_M} \quad \text{(EQ. 14)}$$

Substituting in Equation 12 for V_{TX}

$$Z_{TR} = \frac{Z_T}{1000} + 2R_F \quad \text{(EQ. 15)}$$

Therefore

$$Z_T = 1000 \bullet (Z_{TR} - 2R_F) \quad \text{(EQ. 16)}$$

Equation 16 can now be used to match the SLIC's impedance to any known line impedance (Z_{TR}).

Example:

Calculate Z_T to make $Z_{TR} = 600\Omega$ in series with 2.16µF. $R_F = 20\Omega$.

$$Z_T = 1000 \bullet \left(600 + \frac{1}{j\omega \bullet 2.16 \bullet 10^{-6}} - 2 \bullet 20\right)$$

$Z_T = 560k\Omega$ in series with 2.16nF

(AC) 2-Wire to 4-Wire Gain

The 2-wire to 4-wire gain is equal to V_{TX}/V_{TR}

From Equations 9 and 10 with $V_{RX} = 0$

$$A_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/1000}{Z_T/1000 + 2R_F} \quad \text{(EQ. 17)}$$

(AC) 4-Wire to 2-Wire Gain

The 4-wire to 2-wire gain is equal to V_{TR}/V_{RX}

From Equations 9, 10 and 11 with $E_G = 0$

$$A_{4-2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L}{\frac{Z_T}{1000} + 2R_F + Z_L} \quad \text{(EQ. 18)}$$

For applications where the 2-wire impedance (Z_{TR}, Equation 15) is chosen to equal the line impedance (Z_L), the expression for A_{4-2} simplifies to:

$$A_{4-2} = -\frac{Z_T}{Z_{RX}} \bullet \frac{1}{2} \quad \text{(EQ. 19)}$$

(AC) 4-Wire to 4-Wire Gain

The 4-wire to 4-wire gain is equal to V_{TX}/V_{RX}

From Equations 9, 10 and 11 with $E_G = 0$

$$A_{4-4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L + 2R_F}{\frac{Z_T}{1000} + 2R_F + Z_L} \quad \text{(EQ. 20)}$$

Transhybrid Circuit

The purpose of the transhybrid circuit is to remove the receive signal (V_{RX}) from the transmit signal (V_{TX}), thereby preventing an echo on the transmit side. This is accomplished by using an external op amp (usually part of the CODEC) and by the inversion of the signal from the 4-wire receive port (RSN) to the 4-wire transmit port (V_{TX}). Figure 17 shows the transhybrid circuit. The input signal will

be subtracted from the output signal if I_1 equals I_2. Node analysis yields the following equation:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \quad \text{(EQ. 21)}$$

The value of Z_B is then

$$Z_B = -R_{TX} \bullet \frac{V_{RX}}{V_{TX}} \quad \text{(EQ. 22)}$$

Where V_{RX}/V_{TX} equals $1/A_{4-4}$

Therefore

$$Z_B = R_{TX} \bullet \frac{Z_{RX}}{Z_T} \bullet \frac{\frac{Z_T}{1000} + 2R_F + Z_L}{Z_L + 2R_F} \quad \text{(EQ. 23)}$$

Example:

Given: R_{TX} = 20kΩ, Z_{RX} = 280kΩ, Z_T = 562kΩ (standard value), R_F = 20Ω and Z = 600Ω

The value of Z_B = 18.7kΩ

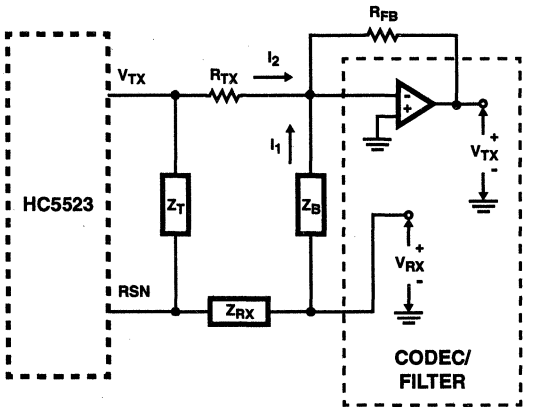


FIGURE 17. TRANSHYBRID CIRCUIT

Supervisory Functions

The loop current, ground key and the ring trip detector outputs are multiplexed to a single logic output pin called $\overline{DET}$. See Table 1 to determine the active detector for a given logic input. For further discussion of the logic circuitry see section titled "Digital Logic Inputs".

Before proceeding with an explanation of the loop current detector, ground key detector and later the longitudinal impedance, it is important to understand the difference between a "metallic" and "longitudinal" loop currents. Figure 18 illustrates 3 different types of loop current encountered.

Case 1 illustrates the metallic loop current. The definition of a metallic loop current is when **equal** currents flow out of tip and into ring. Loop current is a metallic current.

Cases 2 and 3 illustrate the longitudinal loop current. The definition of a longitudinal loop current is a common mode current, that flows either out of or into tip and ring simultaneously. Longitudinal currents in the on-hook state result in **equal** currents flowing through the sense resistors R_1 and R_2 (Figure 18). And longitudinal currents in the off-hook state result in **unequal** currents flowing through the sense resistors R_1 and R_2. Notice that for case 2, longitudinal currents flowing away from the SLIC, the current through R_1 is the metallic loop current plus the longitudinal current; whereas the current through R_2 is the metallic loop current minus the longitudinal current. Longitudinal currents are generated when the phone line is influenced by magnetic fields (e.g. power lines).

Loop Current Detector

Figure 18 shows a simplified schematic of the loop current and ground key detectors. The loop current detector works by sensing the metallic current flowing through resistors R_1 and R_2. This results in a current (I_{RD}) out of the transconductance amplifier (gm_1) that is equal to the product of gm_1 and the metallic loop current. I_{RD} then flows out the R_D pin and through resistor R_D to V_{EE}. The value of I_{RD} is equal to:

$$I_{RD} = \frac{|I_{TIP} - I_{RING}|}{600} = \frac{I_L}{300} \quad \text{(EQ. 24)}$$

The I_{RD} current results in a voltage drop across R_D that is compared to an internal 1.25V reference voltage. When the voltage drop across R_D exceeds 1.25V, and the logic is configured for loop current detection, the $\overline{DET}$ pin goes low.

The hysteresis resistor R_H adds an additional voltage effectively across R_D, causing the on-hook to off-hook threshold to be slightly higher than the off-hook to on-hook threshold.

Taking into account the hysteresis voltage, the typical value of R_D for the on-hook to off-hook condition is:

$$R_D = \frac{465}{I_{ON-HOOK\ to\ OFF-HOOK}} \quad \text{(EQ. 25)}$$

Taking into account the hysteresis voltage, the typical value of R_D for the off-hook to on-hook condition is:

$$R_D = \frac{375}{I_{OFF-HOOK\ to\ ON-HOOK}} \quad \text{(EQ. 26)}$$

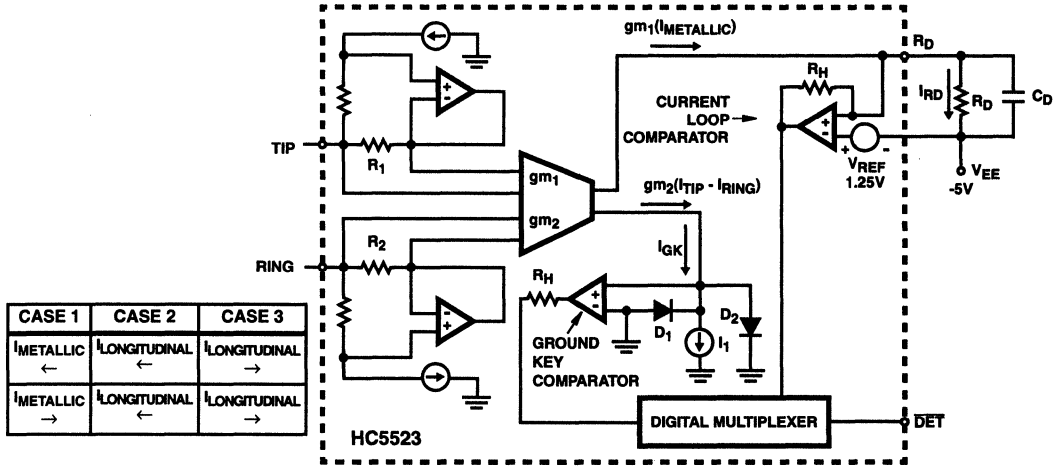
A filter capacitor (C_D) in parallel with R_D will improve the accuracy of the trip point in a noisy environment. The value of this capacitor is calculated using the following Equation:

$$C_D = \frac{T}{R_D} \quad \text{(EQ. 27)}$$

where: T = 0.5ms

Ground Key Detector

A simplified schematic of the ground key detector is shown in Figure 18. Ground key, is the process in which the ring terminal is shorted to ground for the purpose of signaling an Operator or seizing a phone line (between the Central Office and a Private Branch Exchange). The Ground Key detector is activated when unequal current flow through resistors R_1



CASE 1	CASE 2	CASE 3
$I_{METALLIC}$ ←	$I_{LONGITUDINAL}$ ←	$I_{LONGITUDINAL}$ →
$I_{METALLIC}$ →	$I_{LONGITUDINAL}$ ←	$I_{LONGITUDINAL}$ →

FIGURE 18. LOOP CURRENT AND GROUND KEY DETECTORS

and R_2. This results in a current (I_{GK}) out of the transconductance amplifier (gm_2) that is equal to the product of gm_2 and the differential (I_{TIP} -I_{RING}) loop current. If I_{GK} is less than the internal current source (I_1), then diode D_1 is on and the output of the ground key comparator is low. If I_{GK} is greater than the internal current source (I_1), then diode D_2 is on and the output of the ground key comparator is high. With the output of the ground key comparator high, and the logic configured for ground key detect, the $\overline{DET}$ pin goes low. The ground key detector has a built in hysteresis of typically 5mA between its trigger and reset values.

Ring Trip Detector

Ring trip detection is accomplished with the internal ring trip comparator and the external circuitry shown in Figure 19. The process of ring trip is initiated when the logic input pins are in the following states: E0 = 0, E1 = 1/0, C1 = 1 and C2 = 0. This logic condition connects the ring trip comparator to the $\overline{DET}$ output, and causes the Ringrly pin to energize the ring relay. The ring relay connects the tip and ring of the phone to the external circuitry in Figure 19. When the phone is on-hook the DT pin is more positive than the DR pin and the $\overline{DET}$ output is high. For off-hook conditions DR is more positive than DT and $\overline{DET}$ goes low. When $\overline{DET}$ goes low, indicating that the phone has gone off-hook, the SLIC is commanded by the logic inputs to go into the active state. In the active state, tip and ring are once again connected to the phone and normal operation ensues.

Figure 19 illustrates battery backed unbalanced ring injected ringing. For tip injected ringing just reverse the leads to the phone. The ringing source could also be balanced.

NOTE: The $\overline{DET}$ output will toggle at 20Hz because the DT input is not completely filtered by C_{RT}. Software can examine the duty cycle and determine if the $\overline{DET}$ pin is low for more that half the time, if so the off-hook condition is indicated.

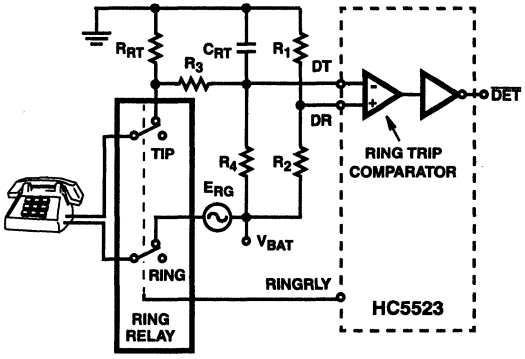


FIGURE 19. RING TRIP CIRCUIT FOR BATTERY BACKED RINGING

Longitudinal Impedance

The feedback loop described in Figure 20(A, B) realizes the desired longitudinal impedances from tip to ground and from ring to ground. Nominal longitudinal impedance is resistive and in the order of 22Ω.

In the presence of longitudinal currents this circuit attenuates the voltages that would otherwise appear at the tip and ring terminals, to levels well within the common mode range of the SLIC. In fact, longitudinal currents may exceed the programmed DC loop current without disturbing the SLIC's VF transmission capabilities.

The function of this circuit is to maintain the tip and ring voltages symmetrically around $V_{BAT}/2$, in the presence of longitudinal currents. The differential transconductance amplifiers G_T and G_R accomplish this by sourcing or sinking the required current to maintain V_C at $V_{BAT}/2$.

When a longitudinal current is injected onto the tip and ring inputs, the voltage at V_C moves from it's equilibrium value $V_{BAT}/2$. When V_C changes by the amount DVC, this change appears between the input terminals of the differential transconductance amplifiers G_T and G_R. The output of G_T and G_R are the differential currents ΔI_1 and ΔI_2, which in turn feed the differential inputs of current sources I_T and I_R respectively. I_T and I_R have current gains of 250 single ended and 500 differentially, thus leading to a change in I_T and I_R that is equal to 500(ΔI) and 500(ΔI_2).

The circuit shown in Figure 20(B) illustrates the tip side of the longitudinal network. The advantages of a differential input current source are: improved noise since the noise due to current source $2I_O$ is now correlated, power savings due to differential current gain and minimized offset error at the Operational Amplifier inputs via the two 5kΩ resistors.

Digital Logic Inputs

Table 1 is the logic truth table for the TTL compatible logic input pins. The HC5523 has two enable inputs pins (E0, E1) and two control inputs pins (C1, C2).

The enable pin E0 is used to enable or disable the $\overline{DET}$ output pin. The $\overline{DET}$ pin is enabled if E0 is at a logic level 0 and disabled if E0 is at a logic level 1.

The enable pin E1 gates the ground key detector to the $\overline{DET}$ output with a logic level 0, and gates the loop or ring trip detector to the $\overline{DET}$ output with a logic level 1.

A combination of the control pins C1 and C2 is used to select 1 of the 4 possible operating states. A description of each operating state and the control logic follow:

Open Circuit State (C1 = 0, C2 = 0)

In this state the SLIC is effectively off. All detectors and both the tip and ring line drive amplifiers are powered down, presenting a high impedance to the line. Power dissipation is at a minimum.

Active State (C1 = 0, C2 = 1)

The tip output is capable of sourcing loop current and for open circuit conditions is about -4V from ground. The ring output is capable of sinking loop current and for open circuit conditions is about V_{BAT} +4V. VF signal transmission is normal. The loop current and ground key detectors are both active, E0 and E1 determine which detector is gated to the $\overline{DET}$ output.

Ringing State (C1 = 1, C2 = 0)

The ring relay driver and the ring trip detector are activated. Both the tip and ring line drive amplifiers are powered down. Both tip and ring are disconnected from the line via the external ring relay.

Standby State (C1 = 1, C2 = 1)

Both the tip and ring line drive amplifiers are powered down. Internal resistors are connected between tip to ground and ring to V_{BAT} to allow loop current detect in an off-hook condition. The loop current and ground key detectors are both active, E0 and E1 determine which detector is gated to the $\overline{DET}$ output.

AC Transmission Circuit Stability

To ensure stability of the AC transmission feedback loop two compensation capacitors C_{TC} and C_{RC} are required. Figure 21 (Application Circuit) illustrates their use. Recommended value is 2200pF.

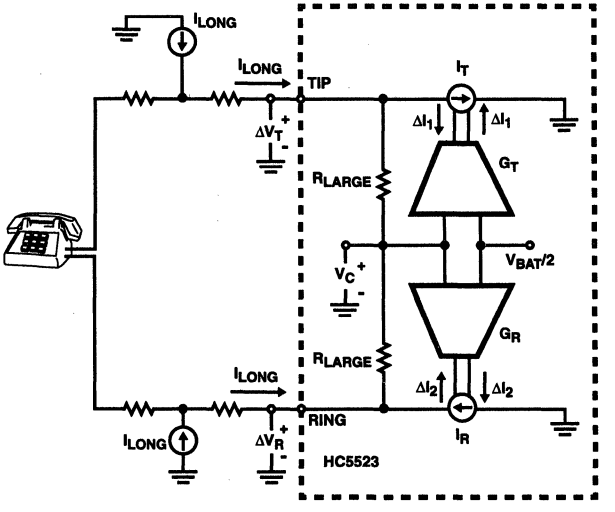


FIGURE 20A.

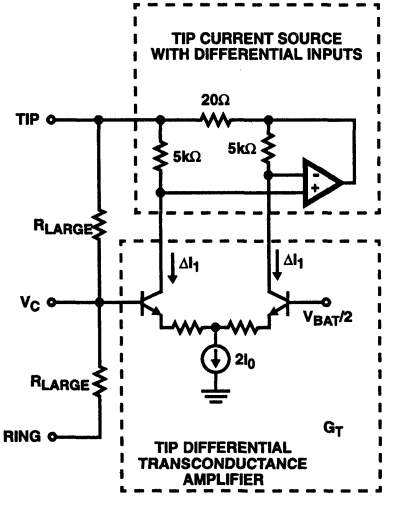


FIGURE 20B.

FIGURE 20. LONGITUDINAL IMPEDANCE NETWORK

SLIC Operating States

TABLE 1. LOGIC TRUTH TABLE

E0	E1	C1	C2	SLIC OPERATING STATE	ACTIVE DETECTOR	DET OUTPUT
0	0	0	0	Open Circuit	No Active Detector	Logic Level High
0	0	0	1	Active	Ground Key Detector	Ground Key Status
0	0	1	0	Ringing	No Active Detector	Logic Level High
0	0	1	1	Standby	Ground Key Detector	Ground Key Status
0	1	0	0	Open Circuit	No Active Detector	Logic Level High
0	1	0	1	Active	Loop Current Detector	Loop Current Status
0	1	1	0	Ringing	Ring Trip Detector	Ring Trip Status
0	1	1	1	Standby	Loop Current Detector	Loop Current Status
1	0	0	0	Open Circuit	No Active Detector	Logic Level High
1	0	0	1	Active	Ground Key Detector	
1	0	1	0	Ringing	No Active Detector	
1	0	1	1	Standby	Ground Key Detector	
1	1	0	0	Open Circuit	No Active Detector	
1	1	0	1	Active	Loop Current Detector	
1	1	1	0	Ringing	Ring Trip Detector	
1	1	1	1	Standby	Loop Current Detector	

AC-DC Separation Capacitor, C_{HP}

The high pass filter capacitor connected between pins HPT and HPR provides the separation between circuits sensing tip to ring DC conditions and circuits processing AC signals. A 10nf C_{HP} will position the low end frequency response 3dB break point at 48Hz. Where:

$$f_{3dB} = \frac{1}{(2 \bullet \pi \bullet R_{HP} \bullet C_{HP})} \quad \text{(EQ. 28)}$$

where $R_{HP} = 330k\Omega$

Thermal Shutdown Protection

The HC5523's thermal shutdown protection is invoked if a fault condition on the tip or ring causes the temperature of the die to exceed 160°C. If this happens, the SLIC goes into a high impedance state and will remain there until the temperature of the die cools down by about 20°C. The SLIC will return back to its normal operating mode, providing the fault condition has been removed.

Surge Voltage Protection

The HC5523 must be protected against surge voltages and power crosses. Refer to "Maximum Ratings" TIPX and RINGX terminals for maximum allowable transient tip and ring voltages. The protection circuit shown in Figure 20 utilizes diodes together with a clamping device to protect tip and ring against high voltage transients.

Positive transients on tip or ring are clamped to within a couple of volts above ground via diodes D_1 and D_2. Under normal operating conditions D_1 and D_2 are reverse biased and out of the circuit.

Negative transients on tip and ring are clamped to within a couple of volts below ground via diodes D_3 and D_4 with the help of a Surgector. The Surgector is required to block conduction through diodes D_3 and D_4 under normal operating conditions and allows negative surges to be returned to system ground.

In applications where only low energy transients (<300V) are possible, diodes D_3 and D_4 could be connected to V_{BAT}, eliminating the requirement of the Surgector. Caution should be used with this application. Be aware that: surge protection is for low level transients only and will subject the batteries to negative voltage surges.

The fuse resistors (R_F) serve a dual purpose of being non-destructive power dissipaters during surge and fuses when the line in exposed to a power cross.

Power-Up Sequence

The HC5523 has **no** required power-up sequence. This is a result of the Dielectrically Isolated (DI) process used in the fabrication of the part. By using the DI process, care is no longer required to insure that the substrate be kept at the most negative potential as with junction isolated ICs.

Printed Circuit Board Layout

Care in the printed circuit board layout is essential for proper operation. All connections to the RSN pin should be made as close to the device pin as possible, to limit the interference that might be injected into the RSN terminal. It is good practice to surround the RSN pin with a ground plane.

The analog and digital grounds should be tied together at the device.

Notes

2. **Overload Level (Two-Wire port)** - The overload level is specified at the 2-wire port (V_{TR0}) with the signal source at the 4-wire receive port (E_{RX}). I_{DCMET} = 23mA, R_{SG} = 4kΩ, increase the amplitude of E_{RX} until 1% THD is measured at V_{TRO}. Reference Figure 1.

3. **Longitudinal Impedance** - The longitudinal impedance is computed using the following equations, where TIP and RING voltages are referenced to ground. L_{ZT}, L_{ZR}, V_T, V_R, A_R and A_T are defined in Figure 2.

   (TIP) $L_{ZT} = V_T/A_T$

   (RING) $L_{ZR} = V_R/A_R$

   where: $E_L = 1V_{RMS}$ (0Hz to 100Hz)

4. **Longitudinal Current Limit (Off-Hook Active)** - Off-Hook (Active, C_1 = 1, C_2 = 0) longitudinal current limit is determined by increasing the amplitude of E_L (Figure 3A) until the 2-wire longitudinal balance drops below 45dB. $\overline{DET}$ pin remains low (no false detection).

5. **Longitudinal Current Limit (On-Hook Standby)** - On-Hook (Active, C_1 = 1, C_2 = 1) longitudinal current limit is determined by increasing the amplitude of E_L (Figure 3B) until the 2-wire longitudinal balance drops below 45dB. $\overline{DET}$ pin remains high (no false detection).

6. **Longitudinal to Metallic Balance** - The longitudinal to metallic balance is computed using the following equation:

   BLME = 20 • log (E_L/V_{TR}), where: E_L and V_{TR} are defined in Figure 4.

7. **Metallic to Longitudinal FCC Part 68, Para 68.310** - The metallic to longitudinal balance is defined in this spec.

8. **Longitudinal to Four-Wire Balance** - The longitudinal to 4-wire balance is computed using the following equation:

   BLFE = 20 • log (E_L/V_{TX}),: E_L and V_{TX} are defined in Figure 4.

9. **Metallic to Longitudinal Balance** - The metallic to longitudinal balance is computed using the following equation:

   BMLE = 20 • log (E_{TR}/V_L), E_{RX} = 0

   where: E_{TR}, V_L and E_{RX} are defined in Figure 5.

10. **Four-Wire to Longitudinal Balance** - The 4-wire to longitudinal balance is computed using the following equation:

    BFLE = 20 • log (E_{RX}/V_L), E_{TR} = source is removed.

    where: E_{RX}, V_L and E_{TR} are defined in Figure 5.

11. **Two-Wire Return Loss** - The 2-wire return loss is computed using the following equation:

    r = -20 • log ($2V_M/V_S$)

    where: Z_D = The desired impedance; e.g., the characteristic impedance of the line, nominally 600Ω. (Reference Figure 6).

12. **Overload Level (4-Wire port)** - The overload level is specified at the 4-wire transmit port (V_{TXO}) with the signal source (E_G) at the 2-wire port, I_{DCMET} = 23mA, Z_L = 20kΩ, R_{SG} = 4kΩ (Reference Figure 7). Increase the amplitude of E_G until 1% THD is measured at V_{TXO}. Note that the gain from the 2-wire port to the 4-wire port is equal to 1.

13. **Output Offset Voltage** - The output offset voltage is specified with the following conditions: E_G = 0, I_{DCMET} = 23mA, Z_L = ∞ and is measured at V_{TX}. E_G, I_{DCMET}, V_{TX} and Z_L are defined in Figure 7. Note: I_{DCMET} is established with a series 600Ω resistor between tip and ring.

14. **Two-Wire to Four-Wire (Metallic to V_{TX}) Voltage Gain** - The 2-wire to 4-wire (metallic to V_{TX}) voltage gain is computed using the following equation.

    $G_{2-4} = (V_{TX}/V_{TR})$, E_G = 0dBm0, V_{TX}, V_{TR}, and E_G are defined in Figure 7.

15. **Current Gain RSN to Metallic** - The current gain RSN to Metallic is computed using the following equation:

    $K = I_M [(R_{DC1} + R_{DC2})/(V_{RDC} - V_{RSN})]$ K, I_M, R_{DC1}, R_{DC2}, V_{RDC} and V_{RSN} are defined in Figure 8.

16. **Two-Wire to Four-Wire Frequency Response** - The 2-wire to 4-wire frequency response is measured with respect to E_G = 0dBm at 1.0kHz, E_{RX} = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    F_{2-4} = 20 • log (V_{TX}/V_{TR}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TX}, V_{TR}, and E_G are defined in Figure 9.

17. **Four-Wire to Two-Wire Frequency Response** - The 4-wire to 2-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    F_{4-2} = 20 • log (V_{TR}/E_{RX}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TR} and E_{RX} are defined in Figure 9.

18. **Four-Wire to Four-Wire Frequency Response** - The 4-wire to 4-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    F_{4-4} = 20 • log (V_{TX}/E_{RX}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TX} and E_{RX} are defined in Figure 9.

19. **Two-Wire to Four-Wire Insertion Loss** - The 2-wire to 4-wire insertion loss is measured with respect to E_G = 0dBm at 1.0kHz input signal, E_{RX} = 0, I_{DCMET} = 23mA and is computed using the following equation:

    $L_{2-4} = 20 • \log (V_{TX}/V_{TR})$

    where: V_{TX}, V_{TR}, and E_G are defined in Figure 9. (Note: The fuse resistors, R_F, impact the insertion loss. The specified insertion loss is for R_F = 0).

20. **Four-Wire to Two-Wire Insertion Loss** - The 4-wire to 2-wire insertion loss is measured based upon E_{RX} = 0dBm, 1.0kHz input signal, E_G = 0, I_{DCMET} = 23mA and is computed using the following equation:

    $L_{4-2} = 20 • \log (V_{TR}/E_{RX})$

    where: V_{TR} and E_{RX} are defined in Figure 9.

21. **Two-Wire to Four-Wire Gain Tracking** - The 2-wire to 4-wire gain tracking is referenced to measurements taken for E_G = -10dBm, 1.0kHz signal, E_{RX} = 0, I_{DCMET} = 23mA and is computed using the following equation.

    $G_{2-4} = 20 • \log (V_{TX}/V_{TR})$ vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

    V_{TX} and V_{TR} are defined in Figure 9.

22. **Four-Wire to Two-Wire Gain Tracking** - The 4-wire to 2-wire gain tracking is referenced to measurements taken for E_{RX} = -10dBm, 1.0kHz signal, E_G = 0, I_{DCMET} = 23mA and is computed using the following equation:

    $G_{4-2} = 20 • \log (V_{TR}/E_{RX})$ vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

V_{TR} and E_{RX} are defined in Figure 9. The level is specified at the 4-wire receive port and referenced to a 600Ω impedance level.

23. **Two-Wire Idle Channel Noise** - The 2-wire idle channel noise at V_{TR} is specified with the 2-wire port terminated in 600Ω (R_L) and with the 4-wire receive port grounded (Reference Figure 10).

24. **Four-Wire Idle Channel Noise** - The 4-wire idle channel noise at V_{TX} is specified with the 2-wire port terminated in 600Ω (R_L). The noise specification is with respect to a 600Ω impedance level at V_{TX}. The 4-wire receive port is grounded (Reference Figure 10).

25. **Harmonic Distortion (2-Wire to 4-Wire)** - The harmonic distortion is measured with the following conditions. E_G = 0dBm at 1kHz, I_{DCMET} = 23mA. Measurement taken at V_{TX}. (Reference Figure 7).

26. **Harmonic Distortion (4-Wire to 2-Wire)** - The harmonic distortion is measured with the following conditions. E_{RX} = 0dBm0. Vary frequency between 300Hz and 3.4kHz, I_{DCMET} = 23mA. Measurement taken at V_{TR}. (Reference Figure 9).

27. **Constant Loop Current** - The constant loop current is calculated using the following equation:

    $I_L = 2500 / (R_{DC1} + R_{DC2})$

28. **Standby State Loop Current** - The standby state loop current is calculated using the following equation:

    $I_L = [|V_{BAT}| - 3] / [R_L + 1800]$, $T_A = 25^oC$

29. **Ground Key Detector** - (TRIGGER) Increase the input current to 8mA and verify that $\overline{DET}$ goes low.

    (RESET) Decrease the input current from 17mA to 3mA and verify that $\overline{DET}$ goes high.

    (Hysteresis) Compare difference between trigger and reset.

30. **Power Supply Rejection Ratio** - Inject a $100mV_{RMS}$ signal (50Hz to 4kHz) on V_{BAT}, V_{CC} and V_{EE} supplies. PSRR is computed using the following equation:

    PSRR = 20 • log (V_{TX}/V_{IN}). V_{TX} and V_{IN} are defined in Figure 12.

Pin Descriptions

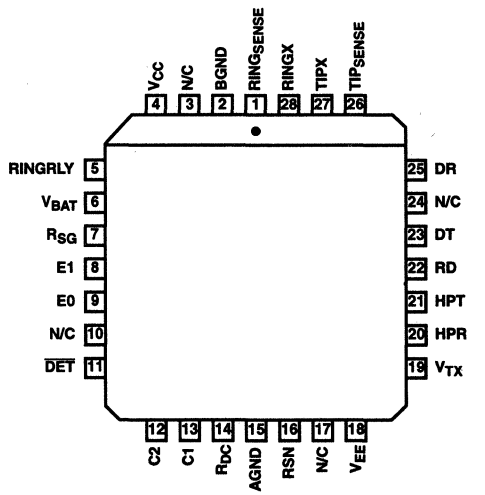
PLCC	PDIP	SYMBOL	DESCRIPTION
1		$RING_{SENSE}$	Internally connected to output of RING power amplifier.
2	7	BGND	Battery Ground - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from AGND but it is recommended that it is connected to the same potential as AGND.
4	8	V_{CC}	+5V power supply.
5	9	RINGRLY	Ring relay driver output.
6	10	V_{BAT}	Battery supply voltage, -24V to -56V.
7	11	R_{SG}	Saturation guard programming resistor pin.
8	12	E1	TTL compatible logic input. The logic state of E1 in conjunction with the logic state of C1 determines which detector is gated to the $\overline{DET}$ output.
9	13	E0	TTL compatible logic input. Enables the $\overline{DET}$ output when set to logic level zero and disables $\overline{DET}$ output when set to a logic level one.
11	14	$\overline{DET}$	Detector output. TTL compatible logic output. A zero logic level indicates that the selected detector was triggered (see Truth Table for selection of Ground Key detector, Loop Current detector or the Ring Trip detector). The $\overline{DET}$ output is an open collector with an internal pull-up of approximately 15kΩ to V_{CC}.
12	15	C2	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
13	16	C1	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
14	17	R_{DC}	DC feed current programming resistor pin. Constant current feed is programmed by resistors R_{DC1} and R_{DC2} connected in series from this pin to the receive summing node (RSN). The resistor junction point is decoupled to AGND to isolate the AC signal components.
15	18	AGND	Analog ground.
16	19	RSN	Receive Summing Node. The AC and DC current flowing into this pin establishes the metallic loop current that flows between tip and ring. The magnitude of the metallic loop current is 1000 times greater than the current into the RSN pin. The constant current programming resistors and the networks for program receive gain and 2-wire impedance all connect to this pin.
18	20	V_{EE}	-5V power supply.
19	21	V_{TX}	Transmit audio output. This output is equivalent to the TIP to RING metallic voltage. The network for programming the 2-wire input impedance connects between this pin and RSN.
20	22	HPR	RING side of AC/DC separation capacitor C_{HP}. C_{HP} is required to properly separate the ring AC current from the DC loop current. The other end of C_{HP} is connected to HPT.
21	1	HPT	TIP side of AC/DC separation capacitor C_{HP}. C_{HP} is required to properly separate the tip AC current from the DC loop current. The other end of C_{HP} is connected to HPR.

Pin Descriptions (Continued)

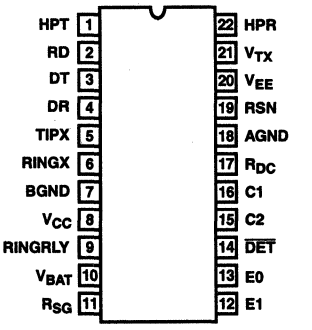
PLCC	PDIP	SYMBOL	DESCRIPTION
22	2	RD	Loop current programming resistor. Resistor R_D sets the trigger level for the loop current detect circuit. A filter capacitor C_D is also connected between this pin and V_{EE}.
23	3	DT	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR.
25	4	DR	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR.
26		TIP_{SENSE}	Internally connected to output of tip power amplifier.
27	5	TIPX	Output of tip power amplifier.
28	6	RINGX	Output of ring power amplifier.
3, 10, 17, 24		N/C	No internal connection.

Pinouts

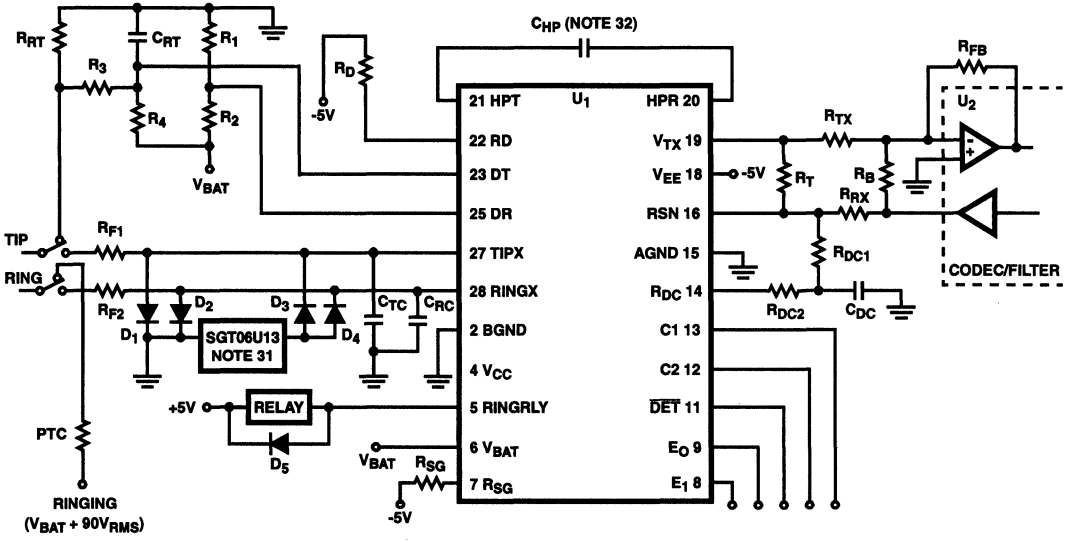
HC5523
(PLCC)
TOP VIEW



HC5523
(PDIP)
TOP VIEW



Application Circuit



U1 SLIC (Subscriber Line Interface Circuit) HC5523

U2 Combination CODEC/Filter e.g. CD22354A or Programmable CODEC/ Filter, e.g. SLAC

C_{DC} 1.5µF, 20%, 10V

C_{HP} 10nF, 20%, 100V (Note 2)

C_{RT} 0.39µF, 20%, 100V

C_{TC}, C_{RC} 2200pF, 20%, 100V

Relay Relay, 2C Contacts, 5V Coil

D_1 - D_4 Diode, 100V, 3A

Surgector SGT06U13

D_5 Diode, 1N4454

R_{F1}, R_{F2} Line Resistor, 20Ω, 1% Match

R_1, R_3 200kΩ, 5%, 1/4W

R_2 910kΩ, 5%, 1/4W

R_4 1.2MΩ, 5%, 1/4W

R_B 18.7kΩ,1%, 1/4W

R_D 39kΩ, 5%, 1/4W

R_{DC1}, R_{DC2} 41.2kΩ, 5%, 1/4W

R_{FB} 20.0kΩ, 1%, 1/4W

R_{RX} 280kΩ, 1%, 1/4W

R_T 562kΩ, 1%, 1/4W

R_{TX} 20kΩ, 1%, 1/4W

R_{RT} 150Ω, 5%, 2W

R_{SG} V_{BAT} = -28V, R_{SG} = ∞
V_{BAT} = -48V, R_{SG} = 4.0kΩ, 1/4W 5%

NOTES:

31. The anodes of D_3 and D_4 may be connected directly to the V_{BAT} supply if the application is exposed to only low energy transients. For harsher environments it is recommended that the anodes of D_3 and D_4 be shorted to ground through a transzorb or surgector.
32. To meet the specified 25dB 2-wire return loss at 200Hz, C_{HP} needs to be 20nF, 20%, 100V.

FIGURE 21. APPLICATION CIRCUIT

HARRIS SEMICONDUCTOR

HC5526

SLIC
Subscriber Line Interface Circuit

January 1997

Features

- DI Monolithic High Voltage Process
- Programmable Current Feed (20mA to 60mA)
- Programmable Loop Current Detector Threshold and Battery Feed Characteristics
- Ground Key and Ring Trip Detection
- Compatible with Ericsson's PBL3764
- Thermal Shutdown
- On-Hook Transmission
- Wide Battery Voltage Range (-24V to -58V)
- Low Standby Power
- Meets CCITT Transmission Requirements
- -40°C to 85°C Ambient Temperature Range

Applications

- On-Premises (ONS)
- Key Systems
- PBX
- Related Literature
  - AN9537, Operation of the HC5513/26 Evaluation Board

Description

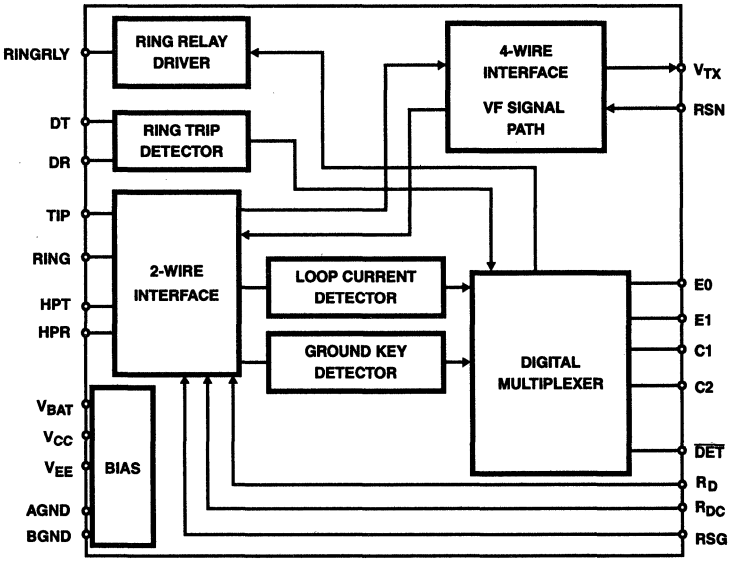
The HC5526 is a subscriber line interface circuit is compliant with CCITT standards. Enhancements include immunity to circuit latch-up during hot plug and absence of false signaling in the presence of longitudinal currents.

The HC5526 is fabricated in a High Voltage Dielectrically Isolated (DI) Bipolar Process that eliminates leakage currents and device latch-up problems normally associated with Junction Isolated (JI) ICs. The elimination of the leakage currents results in improved circuit performance for wide temperature extremes. The latch free benefit of the DI process guarantees operation under adverse transient conditions. This process feature makes the HC5526 ideally suited for use in harsh outdoor environments.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC5526CM	0 to 70	28 Ld PLCC	N28.45
HC5526CP	0 to 70	22 Ld PDIP	E22.4
HC5526IM	-40 to 85	28 Ld PLCC	N28.45
HC5526IP	-40 to 85	22 Ld PDIP	E22.4

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4151.1**

Absolute Maximum Ratings

Operating Temperature Range ..... -40°C to 110°C
Power Supply (-40°C ≤ T_A ≤ 85°C)
  Supply Voltage V_{CC} to GND ..... 0.5V to 7V
  Supply Voltage V_{EE} to GND ..... -7V to 0.5V
  Supply Voltage V_{BAT} to GND ..... -70V to 0.5V
Ground
  Voltage between AGND and BGND ..... -0.3V to 0.3V
Relay Driver
  Ring Relay Supply Voltage ..... 0V to V_{BAT} 75V
  Ring Relay Current 50mA
Ring Trip Comparator
  Input Voltage ..... V_{BAT} to 0V
  Input Current ..... -5mA to 5mA
Digital Inputs, Outputs (C1, C2, E0, E1, $\overline{DET}$)
  Input Voltage ..... 0V to V_{CC}
  Output Voltage ($\overline{DET}$ Not Active) ..... 0V to V_{CC}
  Output Current ($\overline{DET}$) 5mA
Tipx and Ringx Terminals (-40°C ≤ T_A ≤ 85°C)
  Tipx or Ringx Voltage, Continuous (Referenced to GND) V_{BAT} to 2V
  Tipx or Ringx, Pulse < 10ms, T_{REP} > 10s ..... V_{BAT} -20V to 5V
  Tipx or Ringx, Pulse < 10µs, T_{REP} > 10s ..... V_{BAT} -40V to 10V
  Tipx or Ringx, Pulse < 250ns, T_{REP} > 10s .... V_{BAT} -70V to 15V
  Tipx or Ringx Current 70mA
ESD Rating 500V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
22 Lead PDIP Package	53
28 Lead PLCC Package	53

Continuous Dissipation at 70°C
  22 Lead PDIP Package 1.5W
  28 Lead PLCC Package 1.5W
Package Power Dissipation at 70°C, t < 100ms, t_{REP} > 1s
  22 Lead PDIP Package 4W
  28 Lead PLCC Package 4W
Derate above ..... 70°C
  PDIP Package ..... 18.8mW/°C
  PLCC Package ..... 18.8mW/°C
Maximum Junction Temperature Range ..... -40°C to 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
  (PLCC - Lead Tips Only)

Die Characteristics

Gate Count ..... 543 Transistors, 51 Diodes

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Typical Operating Conditions

These represent the conditions under which the part was developed and are suggested as guidelines.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Case Temperature		-40	-	100	°C
V_{CC} with Respect to AGND	0°C to 70°C	4.75	-	5.25	V
V_{EE} with Respect to AGND	0°C to 70°C	-5.25	-	-4.75	V
V_{BAT} with Respect to BGND	0°C to 70°C	-58	-	-24	V

Electrical Specifications

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, R_{F1} = R_{F2} = 0Ω, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Overload Level	1% THD, Z_L = 600Ω, (Note 2, Figure 1)	3.1	-	-	V_{PEAK}
Longitudinal Impedance (Tip/Ring)	0 < f < 100Hz (Note 3, Figure 2)	-	20	35	Ω/Wire

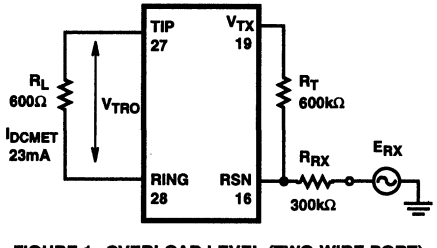


FIGURE 1. OVERLOAD LEVEL (TWO-WIRE PORT)

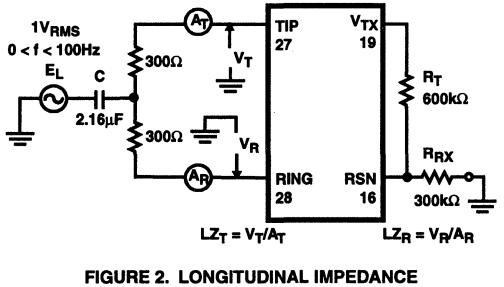


FIGURE 2. LONGITUDINAL IMPEDANCE

Electrical Specifications $T_A = 0^oC$ to 70^oC, $V_{CC} = 5V \pm 5\%$, $V_{EE} = -5V \pm 5\%$, $V_{BAT} = -28V$, AGND = BGND = 0V, $R_{DC1} = R_{DC2} = 41.2k\Omega$, $R_D = 39k\Omega$, $R_{SG} = \infty$, $R_{F1} = R_{F2} = 0\Omega$, $C_{HP} = 10nF$, $C_{DC} = 1.5\mu F$, $Z_L = 600\Omega$, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LONGITUDINAL CURRENT LIMIT (TIP/RING)					
Off-Hook (Active)	No False Detections, (Loop Current), LB > 45dB (Note 4, Figure 3A)	-	-	20	mA_{PEAK}/ Wire
On-Hook (Standby), $R_L = \infty$	No False Detections (Loop Current) (Note 5, Figure 3B)	-	-	5	mA_{PEAK}/ Wire

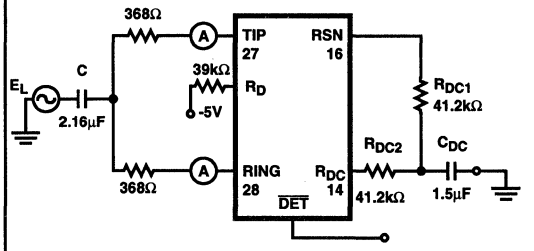


FIGURE 3A. OFF-HOOK

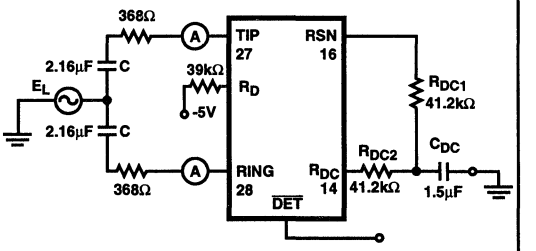


FIGURE 3B. ON-HOOK

FIGURE 3. LONGITUDINAL CURRENT LIMIT

OFF-HOOK LONGITUDINAL BALANCE					
Longitudinal to Metallic	IEEE 455 - 1985, R_{LR}, $R_{LT} = 368\Omega$ 0.2kHz < f < 4.0kHz (Note 6, Figure 4)	53	60	-	dB
Longitudinal to Metallic	R_{LR}, $R_{LT} = 300\Omega$, 0.2kHz < f < 4.0kHz (Note 6, Figure 4)	53	60	-	dB
Metallic to Longitudinal	FCC Part 68, Para 68.310 0.2kHz < f < 1.0kHz	50	55	-	dB
	1.0kHz < f < 4.0kHz (Note 7)	50	55	-	dB
Longitudinal to 4-Wire	0.2kHz < f < 4.0kHz (Note 8, Figure 4)	53	60	-	dB
Metallic to Longitudinal	R_{LR}, $R_{LT} = 300\Omega$, 0.2kHz < f < 4.0kHz (Note 9, Figure 5)	50	55	-	dB
4-Wire to Longitudinal	0.2kHz < f < 4.0kHz (Note 10, Figure 5)	50	55	-	dB

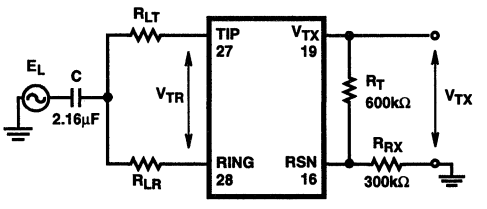


FIGURE 4. LONGITUDINAL TO METALLIC AND LONGITUDINAL TO 4-WIRE BALANCE

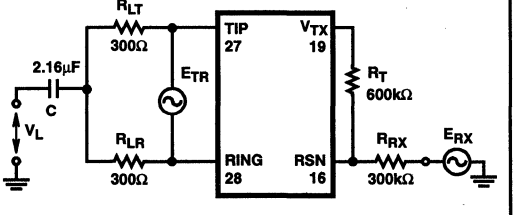


FIGURE 5. METALLIC TO LONGITUDINAL AND 4-WIRE TO LONGITUDINAL BALANCE

2-Wire Return Loss $C_{HP} = 20nF$	0.2kHz to 0.5kHz (Note 11, Figure 6)	25	-	-	dB
	0.5kHz to 1.0kHz (Note 11, Figure 6)	27	-	-	dB
	1.0kHz to 3.4kHz (Note 11, Figure 6)	23	-	-	dB

Electrical Specifications $T_A = 0^oC$ to 70^oC, $V_{CC} = 5V \pm 5\%$, $V_{EE} = -5V \pm 5\%$, $V_{BAT} = -28V$, AGND = BGND = 0V, $R_{DC1} = R_{DC2} = 41.2k\Omega$, $R_D = 39k\Omega$, $R_{SG} = \infty$, $R_{F1} = R_{F2} = 0\Omega$, $C_{HP} = 10nF$, $C_{DC} = 1.5\mu F$, $Z_L = 600\Omega$, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TIP IDLE VOLTAGE					
Active, $I_L = 0$		-	-4	-	V
Standby, $I_L = 0$		-	<0	-	V
RING IDLE VOLTAGE					
Active, $I_L = 0$		-	-24	-	V
Standby, $I_L = 0$		-	>-28	-	V
4-WIRE TRANSMIT PORT (V_{TX})					
Overload Level	($Z_L > 20k\Omega$, 1% THD) (Note 12, Figure 7)	3.1	-	-	V_{PEAK}
Output Offset Voltage	$E_G = 0$, $Z_L = \infty$, (Note 13, Figure 7)	-60	-	60	mV
Output Impedance (Guaranteed by Design)	0.2kHz < f < 03.4kHz	-	5	20	Ω
2- to 4-Wire (Metallic to V_{TX}) Voltage Gain	0.3kHz < f < 03.4kHz (Note 14, Figure 7)	0.98	1.0	1.02	V/V

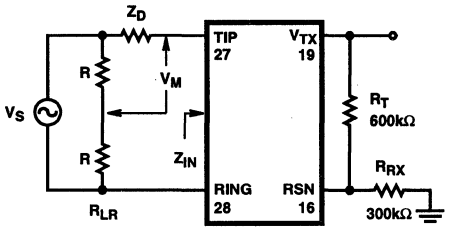


FIGURE 6. TWO-WIRE RETURN LOSS

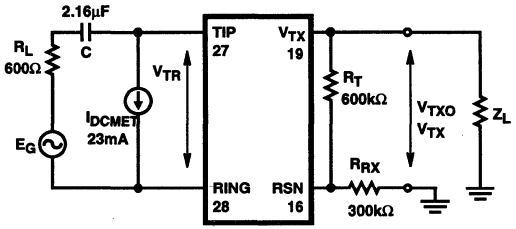


FIGURE 7. OVERLOAD LEVEL (4-WIRE TRANSMIT PORT), OUTPUT OFFSET VOLTAGE, 2-WIRE TO 4-WIRE VOLTAGE GAIN AND HARMONIC DISTORTION

4-WIRE RECEIVE PORT (RSN)					
DC Voltage	$I_{RSN} = 0mA$	-	0	-	V
R_X Sum Node Impedance (Guaranteed by Design)	0.3kHz < f < 3.4kHz	-	-	20	Ω
Current Gain-RSN to Metallic	0.3kHz < f < 3.4kHz (Note 15, Figure 8)	980	1000	1020	Ratio
FREQUENCY RESPONSE (OFF-HOOK)					
2-Wire to 4-Wire	0dBm at 1.0kHz, $E_{RX} = 0V$ 0.3kHz < f < 3.4kHz (Note 16, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm at 1.0kHz, $E_G = 0V$ 0.3kHz < f < 3.4kHz (Note 17, Figure 9)	-0.2	-	0.2	dB
4-Wire to 4-Wire	0dBm at 1.0kHz, $E_G = 0V$ 0.3kHz < f < 3.4kHz (Note 18, Figure 9)	-0.2	-	0.2	dB
INSERTION LOSS					
2-Wire to 4-Wire	0dBm, 1kHz (Note 19, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm, 1kHz (Note 20, Figure 9)	-0.2	-	0.2	dB
GAIN TRACKING (Ref = -10dBm, at 1.0kHz)					
2-Wire to 4-Wire	-40dBm to +3dBm (Note 21, Figure 9)	-0.1	-	0.1	dB
2-Wire to 4-Wire	-55dBm to -40dBm (Note 21, Figure 9)	-	±0.03	-	dB

Electrical Specifications $T_A = 0^oC$ to 70^oC, $V_{CC} = 5V \pm 5\%$, $V_{EE} = -5V \pm 5\%$, $V_{BAT} = -28V$, AGND = BGND = 0V, $R_{DC1} = R_{DC2} = 41.2k\Omega$, $R_D = 39k\Omega$, $R_{SG} = \infty$, $R_{F1} = R_{F2} = 0\Omega$, $C_{HP} = 10nF$, $C_{DC} = 1.5\mu F$, $Z_L = 600\Omega$, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
4-Wire to 2-Wire	-40dBm to +3dBm (Note 22, Figure 9)	-0.1	-	0.1	dB
4-Wire to 2-Wire	-55dBm to -40dBm (Note 22, Figure 9)	-	±0.03	-	dB

$GRX = ((V_{TR1} - V_{TR2})(300k))/(-3)(600)$

Where: V_{TR1} is the Tip to Ring Voltage with $V_{RSN} = 0V$
and V_{TR2} is the Tip to Ring Voltage with $V_{RSN} = -3V$

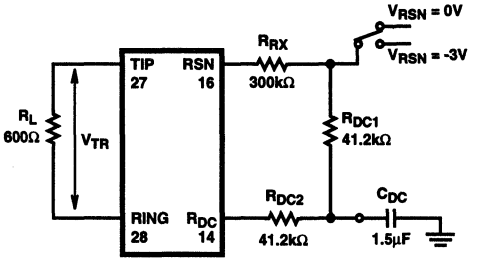


FIGURE 8. CURRENT GAIN-RSN TO METALLIC

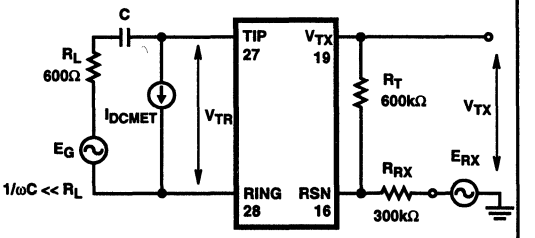
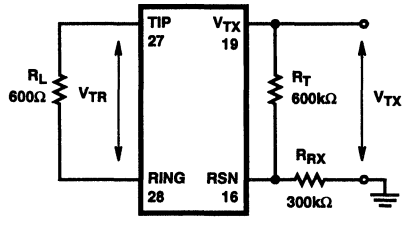
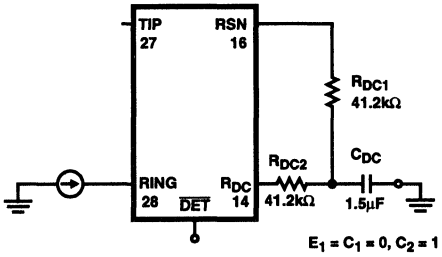


FIGURE 9. FREQUENCY RESPONSE, INSERTION LOSS, GAIN TRACKING AND HARMONIC DISTORTION

NOISE					
Idle Channel Noise at 2-Wire	C-Message Weighting (Note 23, Figure 10)	-	10	-	dBrnC
Idle Channel Noise at 4-Wire	C-Message Weighting (Note 24, Figure 10)	-	10	-	dBrnC
HARMONIC DISTORTION					
2-Wire to 4-Wire	0dBm, 1kHz (Note 25, Figure 7)	-	-65	-54	dB
4-Wire to 2-Wire	0dBm, 0.3kHz to 3.4kHz (Note 26, Figure 9)	-	-65	-54	dB
BATTERY FEED CHARACTERISTICS					
Constant Loop Current Tolerance $R_{DCX} = 41.2k\Omega$	$I_L = 2500/(R_{DC1} + R_{DC2})$, 0^oC to 70^oC (Note 27)	$0.9I_L$	I_L	$1.1I_L$	mA
Loop Current Tolerance (Standby)	$I_L = (V_{BAT}-3)/(R_L+1800)$, 0^oC to 70^oC (Note 28)	$0.8I_L$	I_L	$1.2I_L$	mA
Open Circuit Voltage ($V_{TIP} - V_{RING}$)	0^oC to 70^oC, (Active)	14	-	20	V
LOOP CURRENT DETECTOR					
On-Hook to Off-Hook	$R_D = 39k\Omega$, 0^oC to 70^oC	$372/R_D$	$465/R_D$	$558/R_D$	mA
Off-Hook to On-Hook	$R_D = 39k\Omega$, 0^oC to 70^oC	$325/R_D$	$405/R_D$	$485/R_D$	mA
Loop Current Hysteresis	$R_D = 39k\Omega$, 0^oC to 70^oC	$25/R_D$	$60/R_D$	$95/R_D$	mA
GROUND KEY DETECTOR					
Tip/Ring Current Difference - Trigger	(Note 29, Figure 11)	8	12	17	mA
Tip/Ring Current Difference - Reset	(Note 29, Figure 11)	3	7	12	mA
Hysteresis	(Note 29, Figure 11)	0	5	9	mA

Electrical Specifications $T_A = 0^oC$ to 70^oC, $V_{CC} = 5V \pm 5\%$, $V_{EE} = -5V \pm 5\%$, $V_{BAT} = -28V$, AGND = BGND = 0V, $R_{DC1} = R_{DC2} = 41.2k\Omega$, $R_D = 39k\Omega$, $R_{SG} = \infty$, $R_{F1} = R_{F2} = 0\Omega$, $C_{HP} = 10nF$, $C_{DC} = 1.5\mu F$, $Z_L = 600\Omega$, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
 FIGURE 10. IDLE CHANNEL NOISE					
 FIGURE 11. GROUND KEY DETECT					
RING TRIP DETECTOR (DT, DR)					
Offset Voltage	Source Res = 0	-20	-	20	mV
Input Bias Current	Source Res = 0	-500	-	500	nA
Input Common-Mode Range	Source Res = 0	V_{BAT} +1	-	0	V
Input Resistance	Source Res = 0, Balanced	3	-	-	MΩ
RING RELAY DRIVER					
V_{SAT} at 25mA	I_{OL} = 25mA	-	1.0	1.5	V
Off-State Leakage Current	V_{OH} = 12V	-	-	10	µA
DIGITAL INPUTS (E0, E1, C1, C2)					
Input Low Voltage, V_{IL}		0	-	0.8	V
Input High Voltage, V_{IH}		2	-	V_{CC}	V
Input Low Current, I_{IL}: C1, C2	V_{IL} = 0.4V	-200	-	-	µA
Input Low Current, I_{IL}: E0, E1	V_{IL} = 0.4V	-100	-	-	µA
Input High Current	V_{IH} = 2.4V	-	-	40	µA
DETECTOR OUTPUT ($\overline{DET}$)					
Output Low Voltage, V_{OL}	I_{OL} = 2mA	-	-	0.45	V
Output High Voltage, V_{OH}	I_{OH} = 100µA	2.7	-	-	V
Internal Pull-Up Resistor		10	15	20	kΩ
POWER DISSIPATION					
Open Circuit State	C1 = C2 = 0	-	-	23	mW
On-Hook, Standby	C1 = C2 = 1	-	-	30	mW
On-Hook, Active	C1 = 0, C2 = 1, R_L = High Impedance	-	-	150	mW
Off-Hook, Active	$R_L = 0\Omega$	-	-	1.1	W
	$R_L = 300\Omega$	-	-	0.75	W
	$R_L = 600\Omega$	-	-	0.5	W

Electrical Specifications $T_A = 0^oC$ to 70^oC, $V_{CC} = 5V \pm 5\%$, $V_{EE} = -5V \pm 5\%$, $V_{BAT} = -28V$, AGND = BGND = 0V, $R_{DC1} = R_{DC2} = 41.2k\Omega$, $R_D = 39k\Omega$, $R_{SG} = \infty$, $R_{F1} = R_{F2} = 0\Omega$, $C_{HP} = 10nF$, $C_{DC} = 1.5\mu F$, $Z_L = 600\Omega$, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TEMPERATURE GUARD					
Thermal Shutdown		150	-	180	°C
SUPPLY CURRENTS (V_{BAT} = -28V)					
I_{CC}, On-Hook	Open Circuit State (C1, 2 = 0, 0)	-	-	1.5	mA
	Standby State (C1, 2 = 1, 1)	-	-	1.7	mA
	Active State (C1, 2 = 0,1)	-	-	5.5	mA
I_{EE}, On-Hook	Open Circuit State (C1, 2 = 0, 0)	-	-	0.8	mA
	Standby State (C1, 2 = 1, 1)	-	-	0.8	mA
	Active State (C1, 2 = 0, 1)	-	-	2.2	mA
I_{BAT}, On-Hook	Open Circuit State (C1, 2 = 0, 0)	-	-	0.4	mA
	Standby State (C1, 2 = 1, 1)	-	-	0.6	mA
	Active State (C1, 2 = 0, 1)	-	-	3.9	mA
PSRR					
V_{CC} to 2 or 4-Wire Port	(Note 30, Figure 12)	-	40	-	dB
V_{EE} to 2 or 4-Wire Port	(Note 30, Figure 12)	-	40	-	dB
V_{BAT} to 2 or 4-Wire Port	(Note 30, Figure 12)	-	40	-	dB

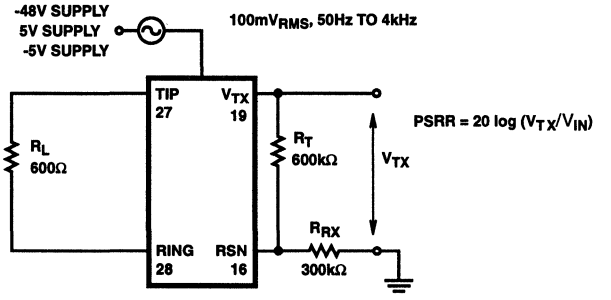


FIGURE 12. POWER SUPPLY REJECTION RATIO

Circuit Operation and Design Information

The HC5526 is a current feed voltage sense Subscriber Line Interface Circuit (SLIC). This means that for short loop applications the SLIC provides a programmed constant current to the tip and ring terminals while sensing the tip to ring voltage.

The following discussion separates the SLIC's operation into its DC and AC path, then follows up with additional circuit and design information.

Constant Loop Current (DC) Path

SLIC in the Active Mode

The DC path establishes a constant loop current that flows out of tip and into the ring terminal. The loop current is programmed by resistors R_{DC1}, R_{DC2} and the voltage on the R_{DC} pin (Figure 13). The R_{DC} voltage is determined by the voltage across R_1 in the saturation guard circuit. Under

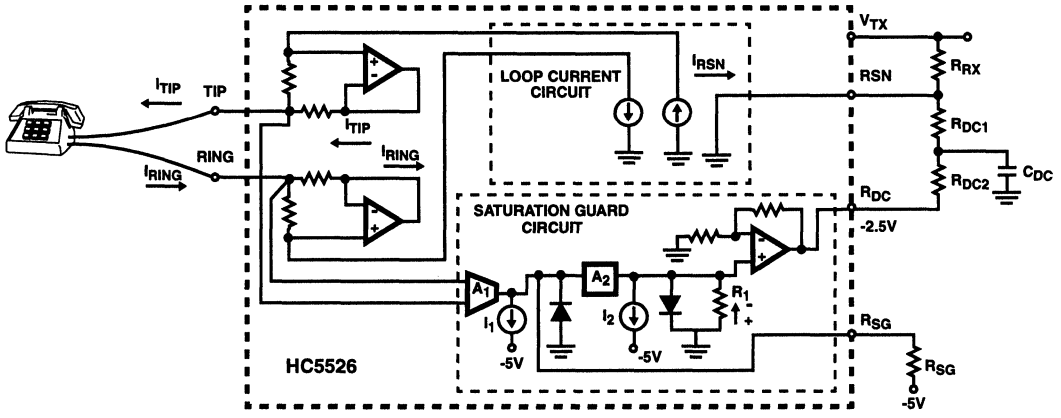


FIGURE 13. DC LOOP CURRENT

constant current feed conditions, the voltage drop across R_1 sets the R_{DC} voltage to -2.5V. This occurs when current flows through R_1 into the current source I_2. The R_{DC} voltage establishes a current (I_{RSN}) that is equal to $V_{RDC}/(R_{DC1}+R_{DC2})$. This current is then multiplied by 1000, in the loop current circuit, to become the tip and ring loop currents.

For the purpose of the following discussion, the saturation guard voltage is defined as the maximum tip to ring voltage at which the SLIC can provide a constant current for a given battery and overhead voltage.

For loop resistances that result in a tip to ring voltage less than the saturation guard voltage the loop current is defined as:

$$I_L = \frac{2.5V}{R_{DC1}+R_{DC2}} \times 1000 \qquad \text{(EQ. 1)}$$

where: I_L = Constant loop current.

R_{DC1} and R_{DC2} = Loop current programming resistors.

Capacitor C_{DC} between R_{DC1} and R_{DC2} removes the VF signals from the battery feed control loop. The value of C_{DC} is determined by Equation 2:

$$C_{DC} = T \times \left(\frac{1}{R_{DC1}} + \frac{1}{R_{DC2}}\right) \qquad \text{(EQ. 2)}$$

where T = 30ms

The minimum C_{DC} value is obtained if $R_{DC1} = R_{DC2}$

Figure 14 illustrates the relationship between the tip to ring voltage and the loop resistance. For a 0Ω loop resistance both tip and ring are at $V_{BAT}/2$. As the loop resistance increases, so does the voltage differential between tip and ring. When this differential voltage becomes equal to the saturation guard voltage, the operation of the SLIC's loop feed changes from a constant current feed to a resistive feed. The loop current in the resistive feed region is no longer constant but varies as a function of the loop resistance.

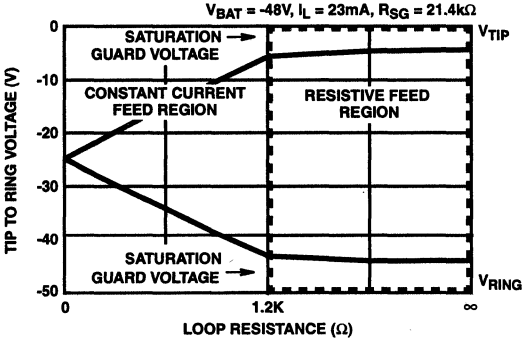
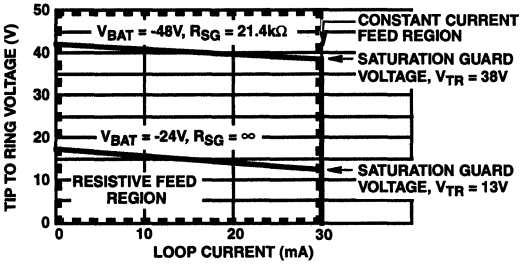


FIGURE 14. V_{TR} vs R_L

Figure 15 shows the relationship between the saturation guard voltage, the loop current and the loop resistance. Notice from Figure 15 that for a loop resistance <1.2kΩ (R_{SG} = 21.4kΩ) the SLIC is operating in the constant current feed region and for resistances >1.2kΩ the SLIC is operating in the resistive feed region. Operation in the resistive feed region allows long loop and off-hook transmission by keeping the tip and ring voltages off the rails. Operation in this region is transparent to the customer.



R_L	100kΩ	4kΩ	2kΩ	<1.2kΩ	R_{RSG} = 21.4kΩ
R_L	100kΩ	1.5kΩ	700Ω	<400Ω	R_{RSG} = ∞Ω

FIGURE 15. V_{TR} vs I_L and R_L

The Saturation Guard circuit (Figure 13) monitors the tip to ring voltage via the transconductance amplifier A_1. A_1 generates a current that is proportional to the tip to ring voltage difference. I_1 is internally set to sink all of A_1's current until the tip to ring voltage exceeds 12.5V. When the tip to ring voltage exceeds 12.5V (with no R_{SG} resistor) A_1 supplies more current than I_1 can sink. When this happens A_2 amplifies its input current by a factor of 12 and the current through R_1 becomes the difference between I_2 and the output current from A_2. As the current from A_2 increases, the voltage across R_1 decreases and the output voltage on R_{DC} decreases. This results in a corresponding decrease in the loop current. The R_{SG} pin provides the ability to increase the saturation guard reference voltage beyond 12.5V. Equation 3 gives the relationship between the R_{SG} resistor value and the programmable saturation guard reference voltage:

$$V_{SGREF} = 12.5 + \frac{5 \bullet 10^5}{R_{SG}} \quad \text{(EQ. 3)}$$

where:

V_{SGREF} = Saturation Guard reference voltage.

R_{SG} = Saturation Guard programming resistor.

When the Saturation guard reference voltage is exceeded, the tip to ring voltage is calculated using Equation 4:

$$V_{TR} = R_L \times \frac{16.66 + 5 \bullet 10^5 / R_{SG}}{R_L + (R_{DC1} + R_{DC2})/600} \quad \text{(EQ. 4)}$$

where:

V_{TR} = Voltage differential between tip and ring.

R_L = Loop resistance.

For on-hook transmission $R_L = \infty$, Equation 4 reduces to:

$$V_{TR} = 16.66 + \frac{5 \bullet 10^5}{R_{SG}} \quad \text{(EQ. 5)}$$

The value of R_{SG} should be calculated to allow maximum loop length operation. This requires that the saturation guard reference voltage be set as high as possible without clipping the incoming or outgoing VF signal. A voltage margin of -4V on tip and -4V on ring, for a total of -8V margin, is recommended as a general guideline. The value of R_{SG} is calculated using Equation 6:

$$R_{SG} = \frac{5 \bullet 10^5}{(|V_{BAT}| - V_{MARGIN}) \times \left(1 + \frac{(R_{DC1} + R_{DC2})}{600 R_L}\right) - 16.66V} \quad \text{(EQ. 6)}$$

where:

V_{BAT} = Battery voltage.

V_{MARGIN} = Recommended value of -8V to allow a maximum overload level of 3.1V peak.

For on-hook transmission $R_L = \infty$, Equation 6 reduces to:

$$R_{SG} = \frac{5 \bullet 10^5}{|V_{BAT}| - V_{MARGIN} - 16.66V} \quad \text{(EQ. 7)}$$

SLIC in the Standby Mode

Overall system power is saved by configuring the SLIC in the standby state when not in use. In the standby state the tip and ring amplifiers are disabled and internal resistors are connected between tip to ground and ring to V_{BAT}. This connection enables a loop current to flow when the phone goes off-hook. The loop current detector then detects this current and the SLIC is configured in the active mode for voice transmission. The loop current in standby state is calculated as follows:

$$I_L \approx \frac{|V_{BAT}| - 3V}{R_L + 1800\Omega} \quad \text{(EQ. 8)}$$

where:

I_L = Loop current in the standby state.

R_L = Loop resistance.

V_{BAT} = Battery voltage.

(AC) Transmission Path

SLIC in the Active Mode

Figure 16 shows a simplified AC transmission model. Circuit analysis yields the following design equations:

$$V_{TR} = V_{TX} + I_M \bullet 2R_F \quad \text{(EQ. 9)}$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_M}{1000} \quad \text{(EQ. 10)}$$

$$V_{TR} = E_G - I_M \bullet Z_L \quad \text{(EQ. 11)}$$

where:

V_{TR} = Is the AC metallic voltage between tip and ring, including the voltage drop across the fuse resistors R_F.

V_{TX} = Is the AC metallic voltage. Either at the ground referenced 4-wire side or the SLIC tip and ring terminals.

I_M = Is the AC metallic current.

R_F = Is a fuse resistor.

Z_T = Is used to set the SLIC's 2-wire impedance.

V_{RX} = Is the analog ground referenced receive signal.

Z_{RX} = Is used to set the 4-wire to 2-wire gain.

E_G = Is the AC open circuit voltage.

Z_L = Is the line impedance.

(AC) 2-Wire Impedance

The AC 2-wire impedance (Z_{TR}) is the impedance looking into the SLIC, including the fuse resistors, and is calculated as follows:

Let $V_{RX} = 0$. Then from Equation 10

$$V_{TX} = Z_T \bullet \frac{I_M}{1000} \quad \text{(EQ. 12)}$$

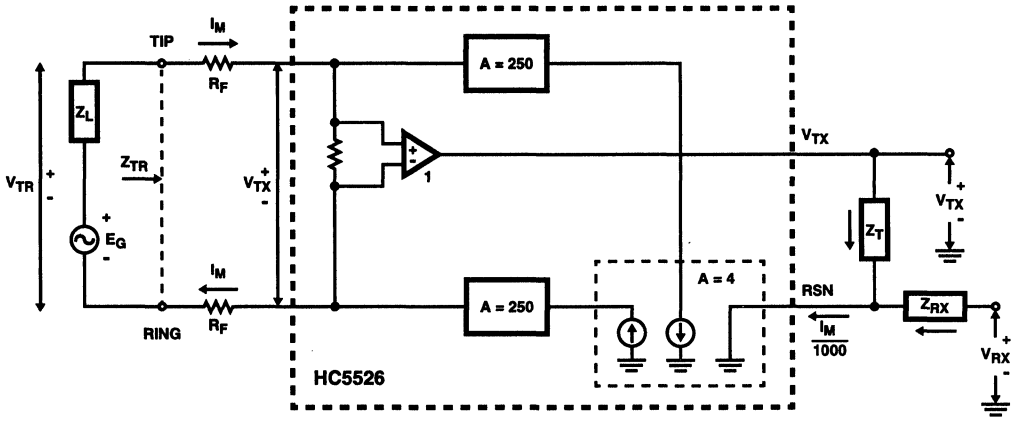


FIGURE 16. SIMPLIFIED AC TRANSMISSION CIRCUIT

Z_{TR} is defined as:

$$Z_{TR} = \frac{V_{TR}}{I_M} \quad \text{(EQ. 13)}$$

Substituting in Equation 9 for V_{TR}

$$Z_{TR} = \frac{V_{TX}}{I_M} + \frac{2R_F \bullet I_M}{I_M} \quad \text{(EQ. 14)}$$

Substituting in Equation 12 for V_{TX}

$$Z_{TR} = \frac{Z_T}{1000} + 2R_F \quad \text{(EQ. 15)}$$

Therefore

$$Z_T = 1000 \bullet (Z_{TR} - 2R_F) \quad \text{(EQ. 16)}$$

Equation 16 can now be used to match the SLIC's impedance to any known line impedance (Z_{TR}).

EXAMPLE:

Calculate Z_T to make $Z_{TR} = 600\Omega$ in series with 2.16µF. $R_F = 20\Omega$

$$Z_T = 1000 \bullet \left(600 + \frac{1}{j\omega \bullet 2.16 \bullet 10^{-6}} - 2 \bullet 20\right)$$

$Z_T = 560k\Omega$ in series with 2.16nF

(AC) 2-Wire to 4-Wire Gain

The 2-wire to 4-wire gain is equal to V_{TX}/V_{TR}

From Equations 9 and 10 with $V_{RX} = 0$

$$A_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/1000}{Z_T/1000 + 2R_F} \quad \text{(EQ. 17)}$$

(AC) 4-Wire to 2-Wire Gain

The 4-wire to 2-wire gain is equal to V_{TR}/V_{RX}

From Equations 9, 10 and 11 with $E_G = 0$

$$A_{4-2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L}{\frac{Z_T}{1000} + 2R_F + Z_L} \quad \text{(EQ. 18)}$$

For applications where the 2-wire impedance (Z_{TR}, Equation 15) is chosen to equal the line impedance (Z_L), the expression for A_{4-2} simplifies to:

$$A_{4-2} = -\frac{Z_T}{Z_{RX}} \bullet \frac{1}{2} \quad \text{(EQ. 19)}$$

(AC) 4-Wire to 4-Wire Gain

The 4-wire to 4-wire gain is equal to V_{TX}/V_{RX}

From Equations 9, 10 and 11 with $E_G = 0$

$$A_{4-4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L + 2R_F}{\frac{Z_T}{1000} + 2R_F + Z_L} \quad \text{(EQ. 20)}$$

Transhybrid Circuit

The purpose of the transhybrid circuit is to remove the receive signal (V_{RX}) from the transmit signal (V_{TX}), thereby preventing an echo on the transmit side. This is accomplished by using an external op amp (usually part of the CODEC) and by the inversion of the signal from the 4-wire receive port (RSN) to the 4-wire transmit port (V_{TX}). Figure 17 shows the transhybrid circuit. The input signal will be subtracted from the output signal if I_1 equals I_2. Node analysis yields the following equation:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \quad \text{(EQ. 21)}$$

The value of Z_B is then

$$Z_B = -R_{TX} \bullet \frac{V_{RX}}{V_{TX}} \quad \text{(EQ. 22)}$$

Where V_{RX}/V_{TX} equals $1/A_{4-4}$

Therefore

$$Z_B = R_{TX} \bullet \frac{Z_{RX}}{Z_T} \bullet \frac{\frac{Z_T}{1000} + 2R_F + Z_L}{Z_L + 2R_F} \quad \text{(EQ. 23)}$$

Example:

Given: R_{TX} = 20kΩ, Z_{RX} = 280kΩ, Z_T = 562kΩ (standard value), R_F = 20Ω and Z_L = 600Ω

The value of Z_B = 18.7kΩ

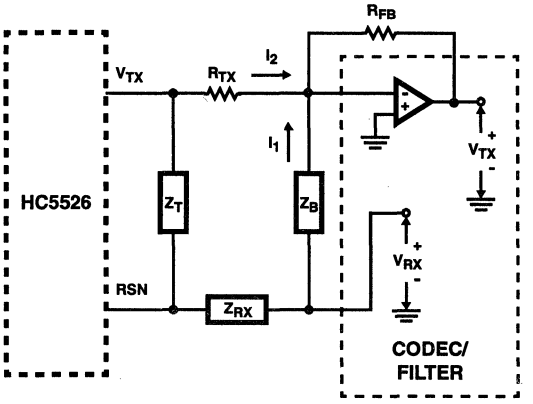


FIGURE 17. TRANSHYBRID CIRCUIT

Supervisory Functions

The loop current, ground key and the ring trip detector outputs are multiplexed to a single logic output pin called $\overline{DET}$. See Table 1 to determine the active detector for a given logic input. For further discussion of the logic circuitry see section titled "Digital Logic Inputs".

Before proceeding with an explanation of the loop current detector, ground key detector and later the longitudinal impedance, it is important to understand the difference between a "metallic" and "longitudinal" loop currents. Figure 18 illustrates 3 different types of loop current encountered.

Case 1 illustrates the metallic loop current. The definition of a metallic loop current is when **equal** currents flow out of tip and into ring. Loop current is a metallic current.

Cases 2 and 3 illustrate the longitudinal loop current. The definition of a longitudinal loop current is a common mode current, that flows either out of or into tip and ring simultaneously. Longitudinal currents in the on-hook state result in **equal** currents flowing through the sense resistors R_1 and R_2 (Figure 18). And longitudinal currents in the off-hook state result in **unequal** currents flowing through the sense resistors R_1 and R_2. Notice that for case 2, longitudinal currents flowing away from the SLIC, the current through R_1 is the metallic loop current plus the longitudinal current; whereas the current through R_2 is the metallic loop current minus the longitudinal current. Longitudinal currents are generated when the phone line is influenced by magnetic fields (e.g. power lines).

Loop Current Detector

Figure 18 shows a simplified schematic of the loop current and ground key detectors. The loop current detector works by sensing the metallic current flowing through resistors R_1 and R_2. This results in a current (I_{RD}) out of the transconductance amplifier (gm_1) that is equal to the product of gm_1 and the metallic loop current. I_{RD} then flows out the R_D pin and through resistor R_D to V_{EE}. The value of I_{RD} is equal to:

$$I_{RD} = \frac{|I_{TIP} - I_{RING}|}{600} = \frac{I_L}{300} \quad \text{(EQ. 24)}$$

The I_{RD} current results in a voltage drop across R_D that is compared to an internal 1.25V reference voltage. When the voltage drop across R_D exceeds 1.25V, and the logic is configured for loop current detection, the $\overline{DET}$ pin goes low.

The hysteresis resistor R_H adds an additional voltage effectively across R_D, causing the on-hook to off-hook threshold to be slightly higher than the off-hook to on-hook threshold.

Taking into account the hysteresis voltage, the typical value of R_D for the on-hook to off-hook condition is:

$$R_D = \frac{465}{I_{ON-HOOK\ to\ OFF-HOOK}} \quad \text{(EQ. 25)}$$

Taking into account the hysteresis voltage, the typical value of R_D for the off-hook to on-hook condition is:

$$R_D = \frac{375}{I_{OFF-HOOK\ to\ ON-HOOK}} \quad \text{(EQ. 26)}$$

A filter capacitor (C_D) in parallel with R_D will improve the accuracy of the trip point in a noisy environment. The value of this capacitor is calculated using the following Equation:

$$C_D = \frac{T}{R_D} \quad \text{(EQ. 27)}$$

where: T = 0.5ms

Ground Key Detector

A simplified schematic of the ground key detector is shown in Figure 18. Ground key, is the process in which the ring terminal is shorted to ground for the purpose of signaling an Operator or seizing a phone line (between the Central Office and a Private Branch Exchange). The Ground Key detector is activated when unequal current flow through resistors R_1 and R_2. This results in a current (I_{GK}) out of the transconductance amplifier (gm_2) that is equal to the product of gm_2 and the differential (I_{TIP} -I_{RING}) loop current. If I_{GK} is less than the internal current source (I_1), then diode D_1 is on and the output of the ground key comparator is low. If I_{GK} is greater than the internal current source (I_1), then diode D_2 is on and the output of the ground key comparator is high. With the output of the ground key comparator high, and the logic configured for ground key detect, the $\overline{DET}$ pin goes low. The ground key detector has a built in hysteresis of typically 5mA between its trigger and reset values.

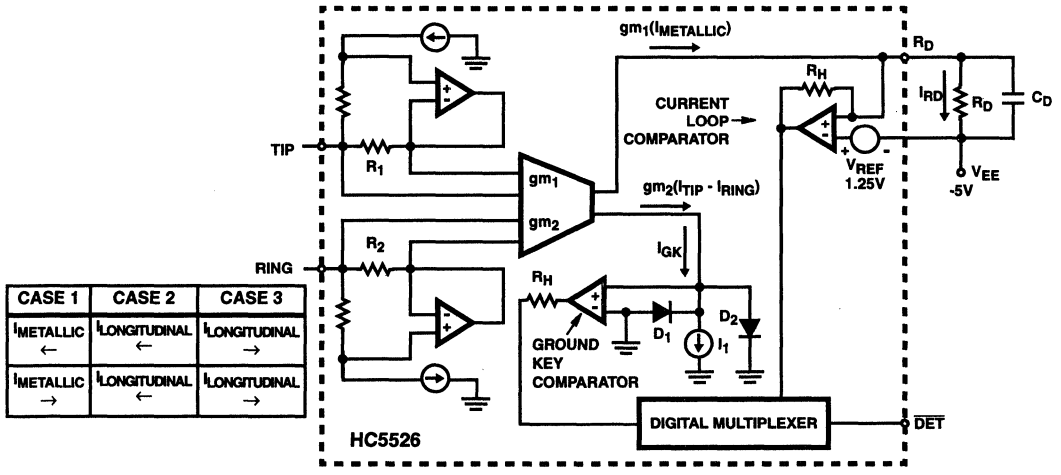


FIGURE 18. LOOP CURRENT AND GROUND KEY DETECTORS

Ring Trip Detector

Ring trip detection is accomplished with the internal ring trip comparator and the external circuitry shown in Figure 19. The process of ring trip is initiated when the logic input pins are in the following states: E0 = 0, E1 = 1/0, C1 = 1 and C2 = 0. This logic condition connects the ring trip comparator to the $\overline{DET}$ output, and causes the Ringrly pin to energize the ring relay. The ring relay connects the tip and ring of the phone to the external circuitry in Figure 19. When the phone is on-hook the DT pin is more positive than the DR pin and the $\overline{DET}$ output is high. For off-hook conditions DR is more positive than DT and $\overline{DET}$ goes low. When $\overline{DET}$ goes low, indicating that the phone has gone off-hook, the SLIC is commanded by the logic inputs to go into the active state. In the active state, tip and ring are once again connected to the phone and normal operation ensues.

Figure 19 illustrates battery backed unbalanced ring injected ringing. For tip injected ringing just reverse the leads to the phone. The ringing source could also be balanced.

NOTE: The $\overline{DET}$ output will toggle at 20Hz because the DT input is not completely filtered by C_{RT}. Software can examine the duty cycle and determine if the $\overline{DET}$ pin is low for more that half the time, if so the off-hook condition is indicated.

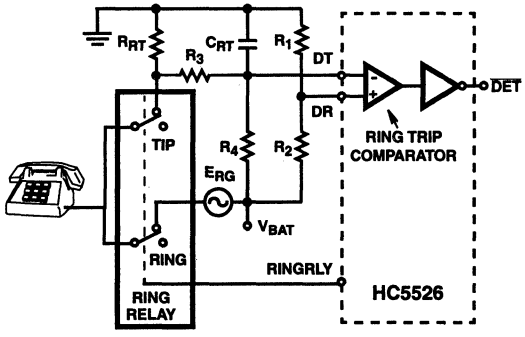


FIGURE 19. RING TRIP CIRCUIT FOR BATTERY BACKED RINGING

Longitudinal Impedance

The feedback loop described in Figure 20(A, B) realizes the desired longitudinal impedances from tip to ground and from ring to ground. Nominal longitudinal impedance is resistive and in the order of 22Ω.

In the presence of longitudinal currents this circuit attenuates the voltages that would otherwise appear at the tip and ring terminals, to levels well within the common mode range of the SLIC. In fact, longitudinal currents may exceed the programmed DC loop current without disturbing the SLIC's VF transmission capabilities.

The function of this circuit is to maintain the tip and ring voltages symmetrically around $V_{BAT}/2$, in the presence of longitudinal currents. The differential transconductance amplifiers G_T and G_R accomplish this by sourcing or sinking the required current to maintain V_C at $V_{BAT}/2$.

When a longitudinal current is injected onto the tip and ring inputs, the voltage at V_C moves from it's equilibrium value $V_{BAT}/2$. When V_C changes by the amount ΔV_C, this change appears between the input terminals of the differential transconductance amplifiers G_T and G_R. The output of G_T and G_R are the differential currents ΔI_1 and ΔI_2, which in turn feed the differential inputs of current sources I_T and I_R respectively. I_T and I_R have current gains of 250 single ended and 500 differentially, thus leading to a change in I_T and I_R that is equal to $500(\Delta I)$ and $500(\Delta I_2)$.

The circuit shown in Figure 20(B) illustrates the tip side of the longitudinal network. The advantages of a differential input current source are: improved noise since the noise due to current source $2I_O$ is now correlated, power savings due to differential current gain and minimized offset error at the Operational Amplifier inputs via the two 5kΩ resistors.

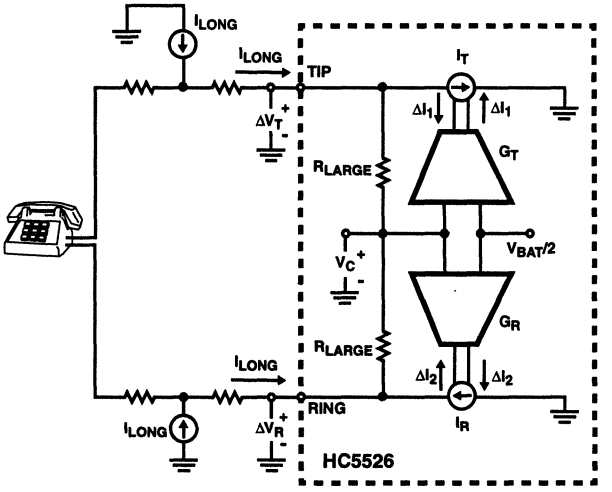


FIGURE 20A.

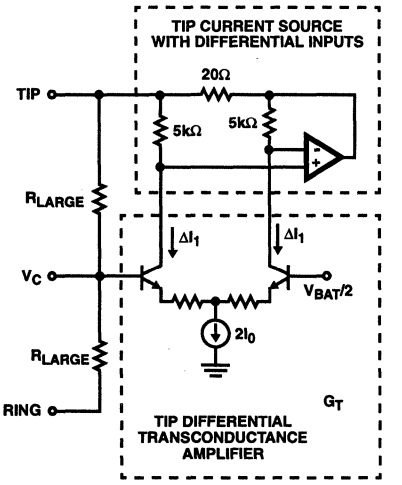


FIGURE 20B.

FIGURE 20. LONGITUDINAL IMPEDANCE NETWORK

Digital Logic Inputs

Table 1 is the logic truth table for the TTL compatible logic input pins. The HC5526 has two enable inputs pins (E0, E1) and two control inputs pins (C1, C2).

The enable pin E0 is used to enable or disable the $\overline{DET}$ output pin. The $\overline{DET}$ pin is enabled if E0 is at a logic level 0 and disabled if E0 is at a logic level 1.

The enable pin E1 gates the ground key detector to the $\overline{DET}$ output with a logic level 0, and gates the loop or ring trip detector to the $\overline{DET}$ output with a logic level 1.

A combination of the control pins C1 and C2 is used to select 1 of the 4 possible operating states. A description of each operating state and the control logic follow:

Open Circuit State (C1 = 0, C2 = 0)

In this state the SLIC is effectively off. All detectors and both the tip and ring line drive amplifiers are powered down, presenting a high impedance to the line. Power dissipation is at a minimum.

Active State (C1 = 0, C2 = 1)

The tip output is capable of sourcing loop current and for open circuit conditions is about -4V from ground. The ring output is capable of sinking loop current and for open circuit conditions is about V_{BAT} +4V. VF signal transmission is normal. The loop current and ground key detectors are both active, E0 and E1 determine which detector is gated to the $\overline{DET}$ output.

Ringing State (C1 = 1, C2 = 0)

The ring relay driver and the ring trip detector are activated. Both the tip and ring line drive amplifiers are powered down. Both tip and ring are disconnected from the line via the external ring relay.

Standby State (C1 = 1, C2 = 1)

Both the tip and ring line drive amplifiers are powered down. Internal resistors are connected between tip to ground and ring to V_{BAT} to allow loop current detect in an off-hook condition. The loop current and ground key detectors are both active, E0 and E1 determine which detector is gated to the $\overline{DET}$ output.

AC Transmission Circuit Stability

To ensure stability of the AC transmission feedback loop two compensation capacitors C_{TC} and C_{RC} are required. Figure 21 (Application Circuit) illustrates their use. Recommended value is 2200pF.

AC-DC Separation Capacitor, C_{HP}

The high pass filter capacitor connected between pins HPT and HPR provides the separation between circuits sensing tip to ring DC conditions and circuits processing AC signals. A 10nf C_{HP} will position the low end frequency response 3dB break point at 48Hz. Where:

$$f_{3dB} = \frac{1}{(2 \bullet \pi \bullet R_{HP} \bullet C_{HP})} \quad \text{(EQ. 28)}$$

where R_{HP} = 330kΩ

SLIC Operating States

TABLE 1. LOGIC TRUTH TABLE

E0	E1	C1	C2	SLIC OPERATING STATE	ACTIVE DETECTOR	$\overline{DET}$ OUTPUT
0	0	0	0	Open Circuit	No Active Detector	Logic Level High
0	0	0	1	Active	Ground Key Detector	Ground Key Status
0	0	1	0	Ringing	No Active Detector	Logic Level High
0	0	1	1	Standby	Ground Key Detector	Ground Key Status
0	1	0	0	Open Circuit	No Active Detector	Logic Level High
0	1	0	1	Active	Loop Current Detector	Loop Current Status
0	1	1	0	Ringing	Ring Trip Detector	Ring Trip Status
0	1	1	1	Standby	Loop Current Detector	Loop Current Status
1	0	0	0	Open Circuit	No Active Detector	Logic Level High
1	0	0	1	Active	Ground Key Detector	
1	0	1	0	Ringing	No Active Detector	
1	0	1	1	Standby	Ground Key Detector	
1	1	0	0	Open Circuit	No Active Detector	
1	1	0	1	Active	Loop Current Detector	
1	1	1	0	Ringing	Ring Trip Detector	
1	1	1	1	Standby	Loop Current Detector	

Thermal Shutdown Protection

The HC5526's thermal shutdown protection is invoked if a fault condition on the tip or ring causes the temperature of the die to exceed 160°C. If this happens, the SLIC goes into a high impedance state and will remain there until the temperature of the die cools down by about 20°C. The SLIC will return back to its normal operating mode, providing the fault condition has been removed.

Surge Voltage Protection

The HC5526 must be protected against surge voltages and power crosses. Refer to "Maximum Ratings" TIPX and RINGX terminals for maximum allowable transient tip and ring voltages. The protection circuit shown in Figure 20 utilizes diodes together with a clamping device to protect tip and ring against high voltage transients.

Positive transients on tip or ring are clamped to within a couple of volts above ground via diodes D_1 and D_2. Under normal operating conditions D_1 and D_2 are reverse biased and out of the circuit.

Negative transients on tip and ring are clamped to within a couple of volts below ground via diodes D_3 and D_4 with the help of a Surgector. The Surgector is required to block conduction through diodes D_3 and D_4 under normal operating conditions and allows negative surges to be returned to system ground.

In applications where only low energy transients (<300V) are possible, diodes D_3 and D_4 could be connected to V_{BAT}, eliminating the requirement of the Surgector. Caution should be used with this application. Be aware that: surge protection is for low level transients only and will subject the batteries to negative voltage surges.

The fuse resistors (R_F) serve a dual purpose of being non-destructive power dissipaters during surge and fuses when the line in exposed to a power cross.

Power-Up Sequence

The HC5526 has **no** required power-up sequence. This is a result of the **D**ielectrically **I**solated (DI) process used in the fabrication of the part. By using the DI process, care is no longer required to insure that the substrate be kept at the most negative potential as with junction isolated ICs.

Printed Circuit Board Layout

Care in the printed circuit board layout is essential for proper operation. All connections to the RSN pin should be made as close to the device pin as possible, to limit the interference that might be injected into the RSN terminal. It is good practice to surround the RSN pin with a ground plane.

The analog and digital grounds should be tied together at the device.

NOTES:

2. **Overload Level (Two-Wire port)** - The overload level is specified at the 2-wire port (V_{TR0}) with the signal source at the 4-wire receive port (E_{RX}). I_{DCMET} = 23mA, increase the amplitude of E_{RX} until 1% THD is measured at V_{TRO}. Reference Figure 1.

3. **Longitudinal Impedance** - The longitudinal impedance is computed using the following equations, where TIP and RING voltages are referenced to ground. L_{ZT}, L_{ZR}, V_T, V_R, A_R and A_T are defined in Figure 2.

   (TIP) $L_{ZT} = V_T/A_T$

   (RING) $L_{ZR} = V_R/A_R$

   where: $E_L = 1V_{RMS}$ (0Hz to 100Hz)

4. **Longitudinal Current Limit (Off-Hook Active)** - Off-Hook (Active, $C_1 = 1$, $C_2 = 0$) longitudinal current limit is determined by increasing the amplitude of E_L (Figure 3A) until the 2-wire longitudinal balance drops below 45dB. $\overline{DET}$ pin remains low (no false detection).

5. **Longitudinal Current Limit (On-Hook Standby)** - On-Hook (Active, $C_1 = 1$, $C_2 = 1$) longitudinal current limit is determined by increasing the amplitude of E_L (Figure 3B) until the 2-wire longitudinal balance drops below 45dB. $\overline{DET}$ pin remains high (no false detection).

6. **Longitudinal to Metallic Balance** - The longitudinal to metallic balance is computed using the following equation:

   BLME = 20 • log (E_L/V_{TR}), where: E_L and V_{TR} are defined in Figure 4.

7. **Metallic to Longitudinal FCC Part 68, Para 68.310** - The metallic to longitudinal balance is defined in this spec.

8. **Longitudinal to Four-Wire Balance** - The longitudinal to 4-wire balance is computed using the following equation:

   BLFE = 20 • log (E_L/V_{TX}),: E_L and V_{TX} are defined in Figure 4.

9. **Metallic to Longitudinal Balance** - The metallic to longitudinal balance is computed using the following equation:

   BMLE = 20 • log (E_{TR}/V_L), E_{RX} = 0

   where: E_{TR}, V_L and E_{RX} are defined in Figure 5.

10. **Four-Wire to Longitudinal Balance** - The 4-wire to longitudinal balance is computed using the following equation:

    BFLE = 20 • log (E_{RX}/V_L), E_{TR} = source is removed.

    where: E_{RX}, V_L and E_{TR} are defined in Figure 5.

11. **Two-Wire Return Loss** - The 2-wire return loss is computed using the following equation:

    r = -20 • log ($2V_M/V_S$)

    where: Z_D = The desired impedance; e.g., the characteristic impedance of the line, nominally 600Ω. (Reference Figure 6).

12. **Overload Level (4-Wire port)** - The overload level is specified at the 4-wire transmit port (V_{TXO}) with the signal source (E_G) at the 2-wire port, I_{DCMET} = 23mA, Z_L = 20kΩ (Reference Figure 7). Increase the amplitude of E_G until 1% THD is measured at V_{TXO}. Note that the gain from the 2-wire port to the 4-wire port is equal to 1.

13. **Output Offset Voltage** - The output offset voltage is specified with the following conditions: E_G = 0, I_{DCMET} = 23mA, $Z_L = \infty$ and is measured at V_{TX}. E_G, I_{DCMET}, V_{TX} and Z_L are defined in Figure 7. Note: I_{DCMET} is established with a series 600Ω resistor between tip and ring.

14. **Two-Wire to Four-Wire (Metallic to VTX) Voltage Gain** - The 2-wire to 4-wire (metallic to V_{TX}) voltage gain is computed using the following equation.

    $G_{2-4} = (V_{TX}/V_{TR})$, E_G = 0dBm0, V_{TX}, V_{TR}, and E_G are defined in Figure 7.

15. **Current Gain RSN to Metallic** - The current gain RSN to Metallic is computed using the following equation:

    $K = I_M [(R_{DC1} + R_{DC2})/(V_{RDC} - V_{RSN})]$ K, I_M, R_{DC1}, R_{DC2}, V_{RDC} and V_{RSN} are defined in Figure 8.

16. **Two-Wire to Four-Wire Frequency Response** - The 2-wire to 4-wire frequency response is measured with respect to E_G = 0dBm at 1.0kHz, E_{RX} = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    F_{2-4} = 20 • log (V_{TX}/V_{TR}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TX}, V_{TR}, and E_G are defined in Figure 9.

17. **Four-Wire to Two-Wire Frequency Response** - The 4-wire to 2-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    F_{4-2} = 20 • log (V_{TR}/E_{RX}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TR} and E_{RX} are defined in Figure 9.

18. **Four-Wire to Four-Wire Frequency Response** - The 4-wire to 4-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation:

    F_{4-4} = 20 • log (V_{TX}/E_{RX}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TX} and E_{RX} are defined in Figure 9.

19. **Two-Wire to Four-Wire Insertion Loss** - The 2-wire to 4-wire insertion loss is measured with respect to E_G = 0dBm at 1.0kHz input signal, E_{RX} = 0, I_{DCMET} = 23mA and is computed using the following equation:

    L_{2-4} = 20 • log (V_{TX}/V_{TR})

    where: V_{TX}, V_{TR}, and E_G are defined in Figure 9. (Note: The fuse resistors, R_F, impact the insertion loss. The specified insertion loss is for R_F = 0).

20. **Four-Wire to Two-Wire Insertion Loss** - The 4-wire to 2-wire insertion loss is measured based upon E_{RX} = 0dBm, 1.0kHz input signal, E_G = 0, I_{DCMET} = 23mA and is computed using the following equation:

    L_{4-2} = 20 • log (V_{TR}/E_{RX})

    where: V_{TR} and E_{RX} are defined in Figure 9.

21. **Two-Wire to Four-Wire Gain Tracking** - The 2-wire to 4-wire gain tracking is referenced to measurements taken for E_G = -10dBm, 1.0kHz signal, E_{RX} = 0, I_{DCMET} = 23mA and is computed using the following equation.

    G_{2-4} = 20 • log (V_{TX}/V_{TR}) vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

    V_{TX} and V_{TR} are defined in Figure 9.

22. **Four-Wire to Two-Wire Gain Tracking** - The 4-wire to 2-wire gain tracking is referenced to measurements taken for E_{RX} = -10dBm, 1.0kHz signal, E_G = 0, I_{DCMET} = 23mA and is computed using the following equation:

    G_{4-2} = 20 • log (V_{TR}/E_{RX}) vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

    V_{TR} and E_{RX} are defined in Figure 9. The level is specified at the 4-wire receive port and referenced to a 600Ω impedance level.

23. **Two-Wire Idle Channel Noise** - The 2-wire idle channel noise at V_{TR} is specified with the 2-wire port terminated in 600Ω (R_L) and with the 4-wire receive port grounded (Reference Figure 10).

24. **Four-Wire Idle Channel Noise** - The 4-wire idle channel noise at V_{TX} is specified with the 2-wire port terminated in 600Ω (R_L). The noise specification is with respect to a 600Ω impedance level at V_{TX}. The 4-wire receive port is grounded (Reference Figure 10).

25. **Harmonic Distortion (2-Wire to 4-Wire)** - The harmonic distortion is measured with the following conditions. E_G = 0dBm at 1kHz, I_{DCMET} = 23mA. Measurement taken at V_{TX}. (Reference Figure 7).

26. **Harmonic Distortion (4-Wire to 2-Wire)** - The harmonic distortion is measured with the following conditions. E_{RX} = 0dBm0. Vary frequency between 300Hz and 3.4kHz, I_{DCMET} = 23mA. Measurement taken at V_{TR}. (Reference Figure 9).

27. **Constant Loop Current** - The constant loop current is calculated using the following equation:

    $I_L = 2500 / (R_{DC1} + R_{DC2})$

28. **Standby State Loop Current** - The standby state loop current is calculated using the following equation:

    $I_L = [|V_{BAT}| - 3] / [R_L + 1800]$, $T_A = 25^oC$

29. **Ground Key Detector** - (TRIGGER) Increase the input current to 8mA and verify that $\overline{DET}$ goes low.

    (RESET) Decrease the input current from 17mA to 3mA and verify that $\overline{DET}$ goes high.

    (Hysteresis) Compare difference between trigger and reset.

30. **Power Supply Rejection Ratio** - Inject a 100mV_{RMS} signal (50Hz to 4kHz) on V_{BAT}, V_{CC} and V_{EE} supplies. PSRR is computed using the following equation:

    PSRR = 20 • log (V_{TX}/V_{IN}). V_{TX} and V_{IN} are defined in Figure 12.

Pin Descriptions

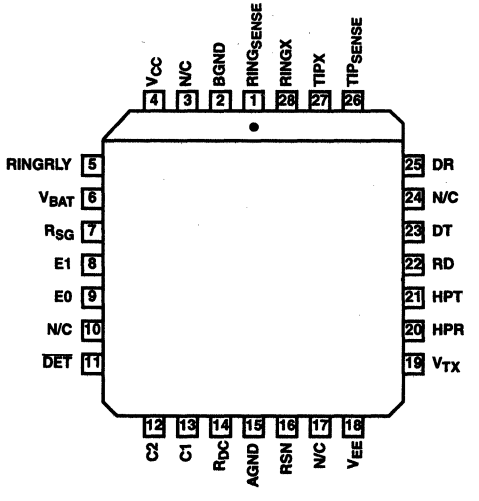
PLCC	PDIP	SYMBOL	DESCRIPTION
1		$RING_{SENSE}$	Internally connected to output of RING power amplifier.
2	7	BGND	Battery Ground - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from AGND but it is recommended that it is connected to the same potential as AGND.
4	8	V_{CC}	5V power supply.
5	9	RINGRLY	Ring relay driver output.
6	10	V_{BAT}	Battery supply voltage, -24V to -56V.
7	11	R_{SG}	Saturation guard programming resistor pin.
8	12	E1	TTL compatible logic input. The logic state of E1 in conjunction with the logic state of C1 determines which detector is gated to the $\overline{DET}$ output.
9	13	E0	TTL compatible logic input. Enables the $\overline{DET}$ output when set to logic level zero and disables $\overline{DET}$ output when set to a logic level one.
11	14	$\overline{DET}$	Detector output. TTL compatible logic output. A zero logic level indicates that the selected detector was triggered (see Truth Table for selection of Ground Key detector, Loop Current detector or the Ring Trip detector). The $\overline{DET}$ output is an open collector with an internal pull-up of approximately 15kΩ to V_{CC}.
12	15	C2	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
13	16	C1	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
14	17	R_{DC}	DC feed current programming resistor pin. Constant current feed is programmed by resistors R_{DC1} and R_{DC2} connected in series from this pin to the receive summing node (RSN). The resistor junction point is decoupled to AGND to isolate the AC signal components.
15	18	AGND	Analog ground.
16	19	RSN	Receive Summing Node. The AC and DC current flowing into this pin establishes the metallic loop current that flows between tip and ring. The magnitude of the metallic loop current is 1000 times greater than the current into the RSN pin. The constant current programming resistors and the networks for program receive gain and 2-wire impedance all connect to this pin.
18	20	V_{EE}	-5V power supply.
19	21	V_{TX}	Transmit audio output. This output is equivalent to the TIP to RING metallic voltage. The network for programming the 2-wire input impedance connects between this pin and RSN.
20	22	HPR	RING side of AC/DC separation capacitor C_{HP}. C_{HP} is required to properly separate the ring AC current from the DC loop current. The other end of C_{HP} is connected to HPT.

Pin Descriptions (Continued)

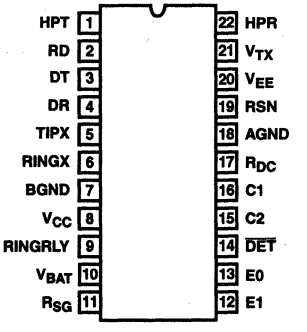
PLCC	PDIP	SYMBOL	DESCRIPTION
21	1	HPT	TIP side of AC/DC separation capacitor C_{HP}. C_{HP} is required to properly separate the tip AC current from the DC loop current. The other end of C_{HP} is connected to HPR.
22	2	RD	Loop current programming resistor. Resistor R_D sets the trigger level for the loop current detect circuit. A filter capacitor C_D is also connected between this pin and V_{EE}.
23	3	DT	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR.
25	4	DR	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR.
26		TIP_{SENSE}	Internally connected to output of tip power amplifier.
27	5	TIPX	Output of tip power amplifier.
28	6	RINGX	Output of ring power amplifier.
3, 10, 17, 24		N/C	No internal connection.

Pinouts

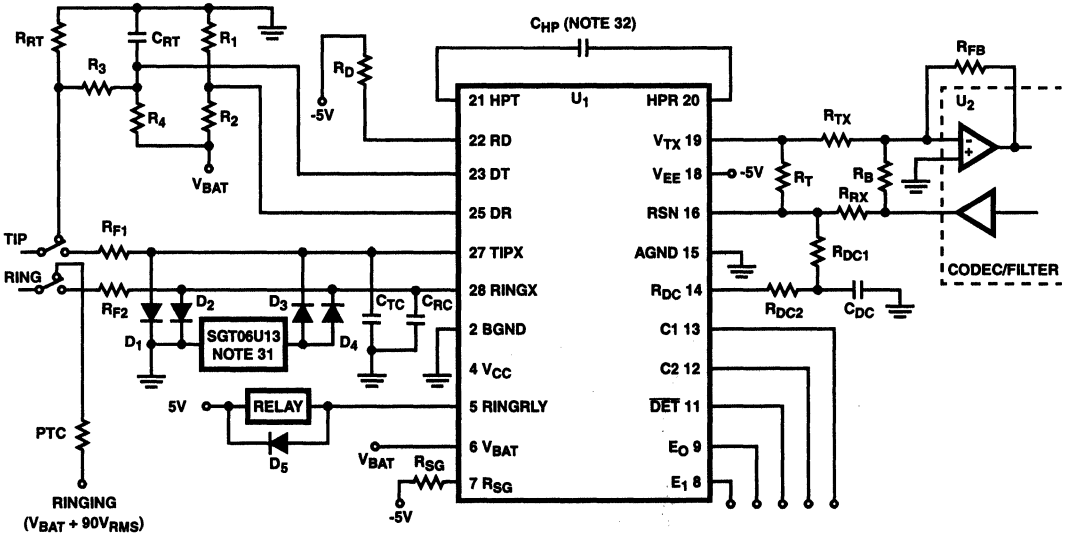
HC5526
(PLCC)
TOP VIEW



HC5526
(PDIP)
TOP VIEW



Application Circuit



U1 SLIC (Subscriber Line Interface Circuit) HC5526

U2 Combination CODEC/Filter e.g. CD22354A or Programmable CODEC/ Filter, e.g. SLAC

C_{DC} 1.5µF, 20%, 10V

C_{HP} 10nF, 20%, 100V (Note 2)

C_{RT} 0.39µF, 20%, 100V

C_{TC}, C_{RC} 2200pF, 20%, 100V

Relay Relay, 2C Contacts, 5V Coil

D_1 - D_4 Diode, 100V, 3A

Surgector SGT06U13

D_5 Diode, 1N4454

R_{F1}, R_{F2} Line Resistor, 20Ω, 1% Match

R_1, R_3 200kΩ, 5%, 1/4W

R_2 910kΩ, 5%, 1/4W

R_4 1.2MΩ, 5%, 1/4W

R_B 18.7kΩ,1%, 1/4W

R_D 39kΩ, 5%, 1/4W

R_{DC1}, R_{DC2} 41.2kΩ, 5%, 1/4W

R_{FB} 20.0kΩ, 1%, 1/4W

R_{RX} 280kΩ, 1%, 1/4W

R_T 562kΩ, 1%, 1/4W

R_{TX} 20kΩ, 1%, 1/4W

R_{RT} 150Ω, 5%, 2W

R_{SG} V_{BAT} = -28V, R_{SG} = ∞
V_{BAT} = -48V, R_{SG} = 21.4kΩ, 1/4W 5%

NOTES:

31. The anodes of D_3 and D_4 may be connected directly to the V_{BAT} supply if the application is exposed to only low energy transients. For harsher environments it is recommended that the anodes of D_3 and D_4 be shorted to ground through a transzorb or surgector.

32. To meet the specified 25dB 2-wire return loss at 200Hz, C_{HP} needs to be 20nF, 20%, 100V.

FIGURE 21. APPLICATION CIRCUIT

HARRIS SEMICONDUCTOR

HC5509A1R3060

SLIC
Subscriber Line Interface Circuit

January 1997

Features

- DI Monolithic High Voltage Process
- Compatible with Worldwide PBX and CO Performance Requirements
- Controlled Supply of Battery Feed Current with Programmable Current Limit
- Operates with 5V Positive Supply (V_{B+})
- Internal Ring Relay Driver and a Utility Relay Driver
- High Impedance Mode for Subscriber Loop
- High Temperature Alarm Output
- Low Power Consumption During Standby Functions
- Switch Hook, Ground Key, and Ring Trip Detection
- Selective Power Denial to Subscriber
- Voice Path Active During Power Denial
- On Chip Op Amp for 2-Wire Impedance Matching

Applications

- Solid State Line Interface Circuit for PBX or Central Office Systems, Digital Loop Carrier Systems
- Hotel/Motel Switching Systems
- Direct Inward Dialing (DID) Trunks
- Voice Messaging PBXs
- High Voltage 2-Wire/4-Wire, 4-Wire/2-Wire Hybrid
- Related Literature
  - AN9607, Impedance Matching Design Equations
  - AN9628, AC Voltage Gain
  - AN9608, Implementing Pulse Metering
  - AN549, The HC-5502S/4X Telephone Subscriber Line Interface Circuits (SLIC)

Description

The HC4P5509A1R3060 telephone Subscriber Line Interface Circuit integrates most of the BORSCHT functions on a monolithic IC. The device is manufactured in a Dielectric Isolation (DI) process and is designed for use as a high voltage interface between the traditional telephone subscriber pair (Tip and Ring) and the low voltage filtering and coding/decoding functions of the line card. Together with a secondary protection diode bridge and "feed" resistors, the device will withstand 1000V lightning induced surges, in plastic packages. The SLIC also maintains specified transmission performance in the presence of externally induced longitudinal currents. The BORSCHT functions that the SLIC provides are:

- Battery Feed with Subscriber Loop Current Limiting
- Overvoltage Protection
- Ring Relay Driver
- Supervisory Signaling Functions
- Hybrid Functions (with External Op Amp)
- Test (or Battery Reversal) Relay Driver

In addition, the SLIC provides selective denial of power to subscriber loops, a programmable subscriber loop current limit from 20mA to 60mA, a thermal shutdown with an alarm output and line fault protection. Switch hook detection, ring trip detection and ground key detection functions are also incorporated in the SLIC device.

The HC4P5509A1R3060 SLIC is ideally suited for line card designs in PBX and CO systems, replacing traditional transformer solutions.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC4P5509A1R3060	0 to 75	28 Ld PLCC	N28.45

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3675.1**

Absolute Maximum Ratings $T_A = 25^oC$

Relay Drivers ..... -0.5V to +15V
Maximum Supply Voltages
(V_{B+}) ..... -0.5V to +7V
(V_{B+})-(V_{B-}) ..... +75V
Junction Temperature Plastic ..... 150°C
Lead Temperature (Soldering 10s) ..... 300°C

Operating Conditions

Operating Temperature Range
HC4P5509A1R3060 ..... 0°C to 75°C
Storage Temperature Range ..... -65°C to 150°C
Relay Drivers ..... +5V to +12V
Positive Power Supply (V_{B+}) ..... +5V ±5%
Negative Power Supply (V_{B-}) ..... -42V to -58V
Loop Resistance (R_L) ..... 200Ω to 1750Ω (Note 2)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PLCC Package	67

Die Characteristics

Transistor Count 224
Diode Count 28
Die Dimensions ..... 174 x 120
Substrate Potential ..... Connected
Process ..... Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. May be extended to 1900Ω with application circuit.

Electrical Specifications

Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are over Operating Temperature Range, $V_{B-} = -48V$, $V_{B+} = +5V$, AG = BG = 0V. All AC Parameters are specified at 600Ω 2-Wire terminating impedance.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC TRANSMISSION PARAMETERS					
RX Input Impedance	300Hz to 3.4kHz (Note 3)	-	100	-	kΩ
TX Output Impedance	300Hz to 3.4kHz (Note 3)	-	-	20	Ω
4-Wire Input Overload Level	300Hz to 3.4kHz R_L = 1200Ω, 600Ω Reference	+1.5	-	-	V_{PEAK}
2-Wire Return Loss	Matched for 600Ω (Note 3)				
SRL LO		26	35	-	dB
ERL		30	40	-	dB
SRL HI		30	40	-	dB
2-Wire Longitudinal to Metallic Balance Off Hook	Per ANSI/IEEE STD 455-1976 (Note 3) 300Hz to 3400Hz	58	63	-	dB
4-Wire Longitudinal Balance Off Hook	300Hz to 3400Hz (Note 3)	50	55	-	dB
Low Frequency Longitudinal Balance	R.E.A. Test Circuit	-	-	-67	dBmp
	I_{LINE} = 40mA $T_A = 25^oC$ (Note 3)	-	-	23	dBrnC
Longitudinal Current Capability	I_{LINE} = 40mA $T_A = 25^oC$ (Note 3)	-	-	30	mA_{RMS}
Insertion Loss	0dBm at 1kHz, Referenced 600Ω				
2-Wire/4-Wire		-6.22	-6.02	-5.82	dB
4-Wire/2-Wire		-	±0.05	±0.2	dB
4-Wire/4-Wire		-6.22	-6.02	-5.82	dB

Electrical Specifications Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are over Operating Temperature Range, $V_{B-} = -48V$, $V_{B+} = +5V$, AG = BG = 0V. All AC Parameters are specified at 600Ω 2-Wire terminating impedance. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Response	300Hz to 3400Hz (Note 3) Referenced to Absolute Level at 1kHz, 0dBm Referenced 600Ω	-	±0.02	±0.05	dB
Level Linearity	Referenced to -10dBm (Note 3)				
2-Wire to 4-Wire and 4-Wire to 2-Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
Absolute Delay	(Note 3)				
2-Wire/4-Wire	f_{IN} - 1kHz	-	0.7	1.2	µs
4-Wire/2-Wire	f_{IN} - 1kHz	-	0.3	1.0	µs
4-Wire/4-Wire	f_{IN} - 1kHz	-	1.5	2.0	µs
Transhybrid Loss	$V_{IN} = 1V_{P-P}$ at 1kHz (Note 3)	32	40	-	dB
Total Harmonic Distortion 2-Wire/4-Wire, 4-Wire/2-Wire, 4-Wire/4-Wire	Reference Level 0dBm at 600Ω 300Hz to 3400Hz (Note 3)	-	-	-52	dB
Idle Channel Noise					
2-Wire and 4-Wire	C-Message (Note 3)	-	-	5	dBrnC
	Psophometric	-	-	-85	dBmp
	3kHz Flat	-	-	15	dBrn
Power Supply Rejection Ratio	(Note 3) 30Hz to 200Hz, $R_L = 600Ω$				
V_{B+} to 2-Wire		25	29	-	dB
V_{B+} to 4-Wire		25	29	-	dB
V_{B-} to 2-Wire		25	29	-	dB
V_{B-} to 4-Wire		25	29	-	dB
V_{B+} to 4-Wire	(Note 3) 200Hz to 16kHz, $R_L = 600Ω$	25	-	-	dB
V_{B+} to 2-Wire		25	-	-	dB
V_{B-} to 4-Wire		25	25	-	dB
V_{B-} to 2-Wire		25	25	-	dB
Ring Sync Pulse Width		50	-	500	µs
DC PARAMETERS					
Loop Current Programming Limit Range	(Note 4)	20 (Note 4)	-	60	mA
Accuracy		10	-	-	%
Loop Current During Power Denial	$R_L = 200Ω$	-	±3	±5	mA

Electrical Specifications Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are over Operating Temperature Range, $V_{B-} = -48V$, $V_{B+} = +5V$, AG = BG = 0V. All AC Parameters are specified at 600Ω 2-Wire terminating impedance. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Fault Currents					
TIP to Ground		-	38	45	mA
RING to Ground		-	54	60	mA
TIP and RING to Ground		-	85	95	mA
Switch Hook Detection Threshold		-	12	15	mA
Ground Key Detection Threshold		9.5	13.5	17.5	mA
Thermal $\overline{ALARM}$ Output	Safe Operating Die Temperature Exceeded	140	-	160	^oC
Ring Trip Comparator Threshold	See Typical Applications for more information	9.5	13.5	17.5	mA
Dial Pulse Distortion		-	0.1	0.5	ms
Relay Driver Outputs					
On Voltage V_{OL}	I_{OL} ($\overline{PR}$) = 60mA, I_{OL} ($\overline{RD}$) = 60mA	-	0.2	0.5	V
Off Leakage Current	V_{OH} = 13.2V	-	±10	±100	µA
TTL/CMOS Logic Inputs ($\overline{RC}$, $\overline{PD}$, RS, $\overline{TST}$, PRI)					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Input Current ($\overline{RC}$, $\overline{PD}$, RS, $\overline{TST}$, PRI)	$0V \le V_{IN} \le 5V$	-	-	±100	µA
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} = 800µA	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} = 40µA	2.7	-	-	V
Power Dissipation On Hook	Relay Drivers Off	-	200	-	mW
I_{B+}	V_{B+} = +5.25V, V_{B-} = -58V, $R_{LOOP} = \infty$	-	-	6	mA
I_{B-}	V_{B+} = +5.25V, V_{B-} = -58V, $R_{LOOP} = \infty$	-6	-	-	mA
UNCOMMITTED OP AMP PARAMETERS					
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Differential Input Resistance	(Note 2)	-	1	-	MΩ
Output Voltage Swing	R_L = 10kΩ	-	±3	-	V_{P-P}
Small Signal GBW		-	1	-	MHz

NOTES:

3. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
4. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.
5. Application limitation based on maximum switch hook detect limit and metallic currents. Not a part limitation.

Pin Descriptions

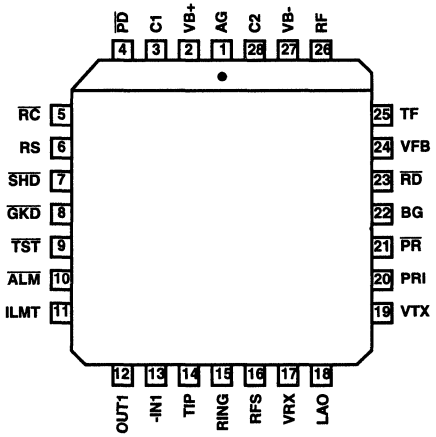
SOIC	SYMBOL	DESCRIPTION
1	AG	Analog Ground - To be connected to zero potential. Serves as a reference for the transmit output and receive input terminals.
2	VB+	Positive Voltage Source - Most Positive Supply.
3	C1	Capacitor #C1 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function.
4	$\overline{PD}$	Power Denial - A low active TTL-compatible logic input. When enabled, the output of the ring amplifier will ramp to close to the output voltage of the tip amplifier.
5	$\overline{RC}$	Ring Command - A low active TTL-compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power down mode ($\overline{TST}$ = 0) or the subscriber is not already off-hook ($\overline{SHD}$ = 0).
6	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive pulse (50 - 500µs) occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring delay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5.
7	$\overline{SHD}$	Switch Hook Detection - An active low LS TTL compatible logic output. A line supervisory output.
8	$\overline{GKD}$	Ground Key Detection - An active low LS TTL compatible logic output. A line supervisory output.
9	$\overline{TST}$	A TTL logic input. A low on this pin will keep the SLIC in a power down mode.
10	$\overline{ALM}$	A LS TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded. The $\overline{ALM}$ can be tied directly to the $\overline{TST}$ pin to power down the part when a thermal fault is detected. It is possible to ignore transient thermal overload conditions in the SLIC by delaying the response to the $\overline{TST}$ pin from the $\overline{ALM}$. Care must be exercised in attempting this as continued thermal overstress may reduced component life.
11	ILMT	Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions using a resistive voltage divider.
12	OUT1	The analog output of the spare operational amplifier.
13	-IN1	The inverting analog input of the spare operational amplifier.
14	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor and ring relay contact. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purpose.
15	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.
16	RFS	Ring Feed Sense - Senses RING side of the loop for Ground Key Detection. During Ring injected ringing the ring signal at this node is isolated from RF via the ring relay. For Tip injected ringing, the RF and RFS pins must be shorted.
17	VRX	Receive Input, 4-Wire Side - A high impedance analog input. AC signals appearing at this input drive the Tip Feed and Ring Feed amplifiers differentially.
18	LAO	Longitudinal Amplifier Output - A low impedance output to be connected to C2 through a low pass filter. Output is proportional to the difference in I_{TIP} and I_{RING}.

Pin Descriptions (Continued)

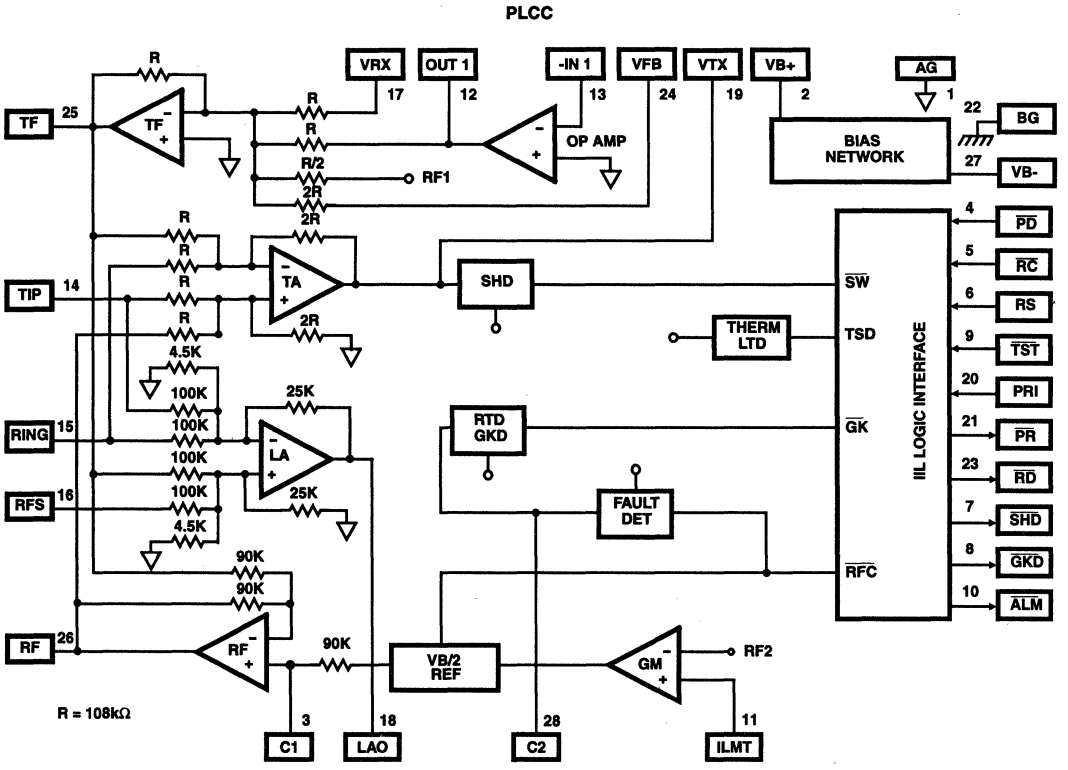
SOIC	SYMBOL	DESCRIPTION
19	VTX	Transmit Output, 4-Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Transhybrid balancing must be performed beyond this output to completely implement two to four wire conversion. This output is referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is necessary.
20	PRI	A TTL compatible input used to control $\overline{PR}$. PRI active High = $\overline{PR}$ active low.
21	$\overline{PR}$	An active low open collector output. Can be used to drive a Polarity Reversal Relay.
22	BG	Battery Ground - Tube connected to zero potential. All loop current and some quiescent current flows into this terminal.
23	$\overline{RD}$	Ring Relay Driver - An active low open collector output. Used to drive a relay that switches ringing signals onto the 2-Wire line.
24	VFB	Feedback input to the tip feed amplifier; may be used in conjunction with transmit output signal and the spare op amp to accommodate 2-Wire line impedance matching.
25	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a feed resistor. Functions with the RF terminal to provide loop current, and to feed voice signals to the telephone set and to sink longitudinal currents.
26	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and to sink longitudinal currents.
27	VB-	The battery voltage source. The most negative supply.
28	C2	Capacitor #2 - An external capacitor to be connected between this terminal and ground. It prevents false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from power lines and other noise sources. This capacitor should be nonpolarized.

Pinout

HC4P5509A1R3060 (PLCC)
TOP VIEW



Functional Diagram



Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

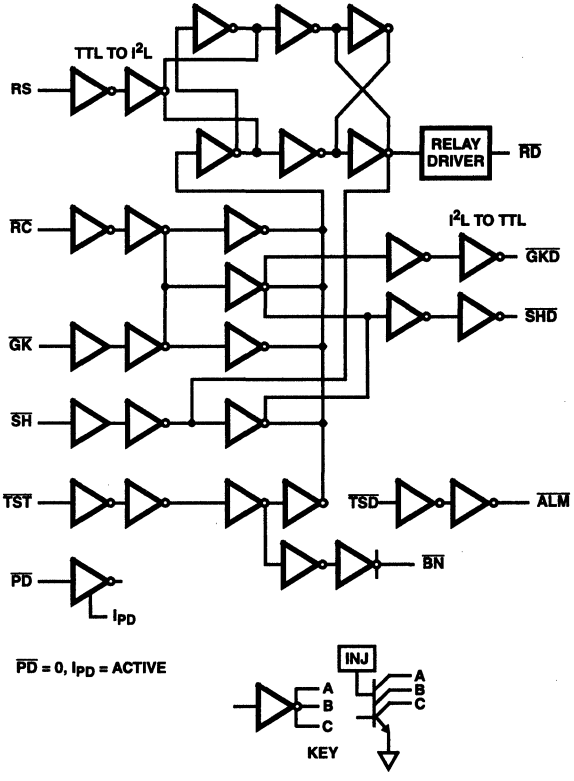
High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or $30mA_{RMS}$, $15mA_{RMS}$ per leg, without any performance degradation.

TABLE 1.

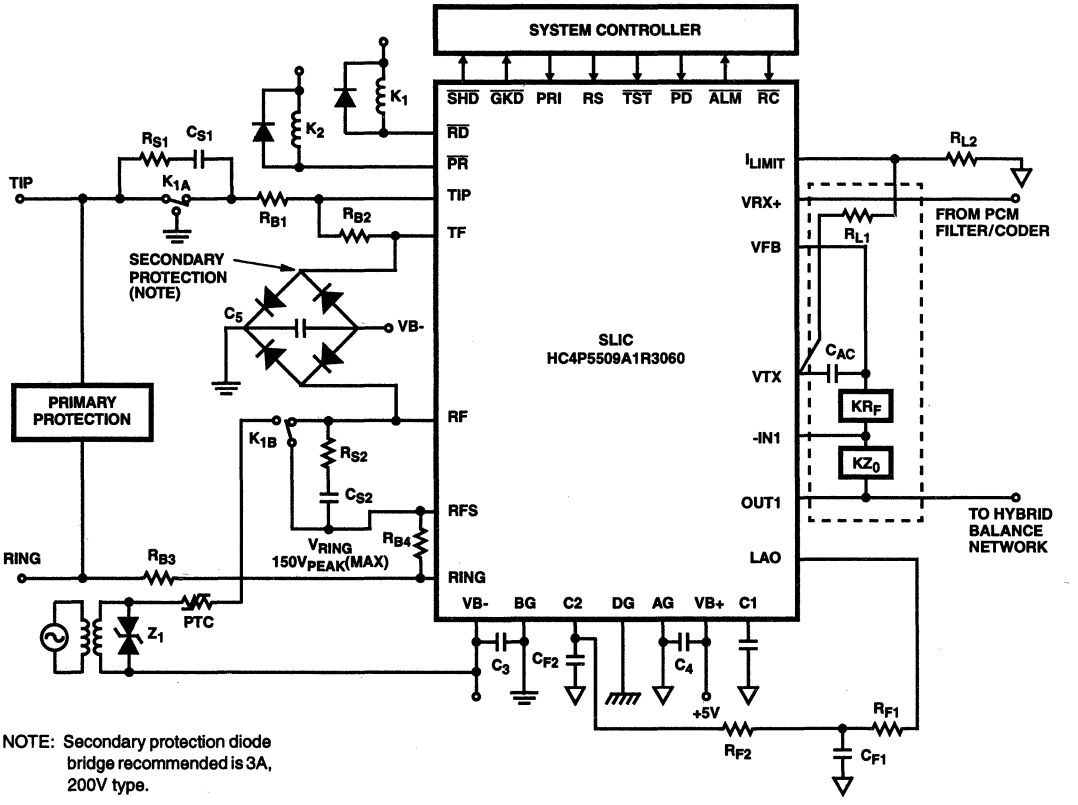
PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
50/60Hz Current T/GND R/GND	11 Cycles Limited to $10A_{RMS}$	700 (Plastic)	V_{RMS}

Logic Diagram



NOTE: PRI and $\overline{PD}$ are independent switch driven by TTL input levels.

Applications Diagram



NOTE: Secondary protection diode bridge recommended is 3A, 200V type.

FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

TYPICAL COMPONENT VALUES

C_1 = 0.5µF, 30V

$R_{F1} = R_{F2}$ = 210kΩ, 1%

$C_{F1} = C_{F2}$ = 0.22µF, 10%, 20V Nonpolarized

C_3 = 0.01µF, 100V, ±20%

C_4 = 0.01µF, 100V, ±20%

C_5 = 0.01µF, 100V, ±20%

C_{AC} = 0.5µF, 20V

KZ_0 = 30kΩ, (Z_0 = 600Ω)

R_{L1}, R_{L2}; Current Limit Setting Resistors:

$I_{LIMIT} = (0.6)\ (R_{L1} + R_{L2})/(200 \times R_{L2})$, R_{L1} typically 100kΩ

KR_F = 20kΩ

$R_{B1} = R_{B2} = R_{B3} = R_{B4}$ = 50Ω 0.1% absolute matching

$R_{S1} = R_{S2}$ = 1kΩ typically

$C_{S1} = C_{S2}$ = 0.1µF, 200V typically, depending on V_{Ring} and line length.

Z_1 = 150V to 200V transient protector. PTC used as ring generator ballast.

NOTES:

1. All grounds (AG, BG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
2. Application shows Ring Injected Ringing, a Balanced or Tip injected configuration may be used.

HARRIS SEMICONDUCTOR

HC-5509B

SLIC
Subscriber Line Interface Circuit

January 1997

Features

- DI Monolithic High Voltage Process
- Compatible with Worldwide PBX and CO Performance Requirements
- Controlled Supply of Battery Feed Current with Programmable Current Limit
- Operates with 5V Positive Supply (V_{B+})
- Internal Ring Relay Driver and a Utility Relay Driver
- High Impedance Mode for Subscriber Loop
- High Temperature Alarm Output
- Low Power Consumption During Standby Functions
- Switch Hook, Ground Key, and Ring Trip Detection
- Selective Power Denial to Subscriber
- Voice Path Active During Power Denial
- On-Chip Op Amp for 2-Wire Impedance Matching

Applications

- Solid State Line Interface Circuit for PBX or Central Office Systems, Digital Loop Carrier Systems
- Hotel/Motel Switching Systems
- Direct Inward Dialing (DID) Trunks
- Voice Messaging PBXs
- High Voltage 2-Wire/4-Wire, 4-Wire/2-Wire Hybrid
- Related Literature
  - AN9607, Impedance Matching Design Equations
  - AN9628, AC Voltage Gain
  - AN9608, Implementing Pulse Metering
  - AN549, The HC-5502S/4X Telephone Subscriber Line Interface Circuits (SLIC)

Description

The HC-5509B telephone Subscriber Line Interface Circuit integrates most of the BORSCHT functions on a monolithic IC. The device is manufactured in a Dielectric Isolation (DI) process and is designed for use as a high voltage interface between the traditional telephone subscriber pair (Tip and Ring) and the low voltage filtering and coding/decoding functions of the line card. Together with a secondary protection diode bridge and "feed" resistors, the device will withstand 1000V lightning induced surges, in plastic packages. The SLIC also maintains specified transmission performance in the presence of externally induced longitudinal currents. The BORSCHT functions that the SLIC provides are:

- Battery Feed with Subscriber Loop Current Limiting
- Overvoltage Protection
- Ring Relay Driver
- Supervisory Signaling Functions
- Hybrid Functions (with External Op-Amp)
- Test (or Battery Reversal) Relay Driver

In addition, the SLIC provides selective denial of power to subscriber loops, a programmable subscriber loop current limit from 20mA to 60mA, a thermal shutdown with an alarm output and line fault protection. Switch hook detection, ring trip detection and ground key detection functions are also incorporated in the SLIC device.

The HC-5509B SLIC is ideally suited for line card designs in PBX and CO systems, replacing traditional transformer solutions.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC3-5509B-5	0 to 75	28 Ld Plastic DIP	E28.6
HC3-5509B-9	-40 to 85	28 Ld Plastic DIP	E28.6
HC4P5509B-5	0 to 75	44 Ld PLCC	N44.65
HC4P5509B-9	-40 to 85	44 Ld PLCC	N44.65
HC9P5509B-5	0 to 75	28 Ld Plastic SOIC	M28.3
HC9P5509B-9	-40 to 85	28 Ld Plastic SOIC	M28.3

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2799.4**

Absolute Maximum Ratings (Note 1)

Relay Drivers ..... -0.5V to 15V
Maximum Supply Voltages
(V_{B+}) ..... -0.5V to 7V
(V_{B+})-(V_{B-}) 75V

Operating Conditions

Operating Temperature Range
HC-5509B-5 ..... 0°C to 75°C
HC-5509B-9 ..... -40°C to 85°C
Relay Drivers ..... 5V to 12V
Positive Power Supply (V_{B+}) ..... 5V ±5%
Negative Power Supply (V_{B-}) ..... -42V to -58V
Loop Resistance (R_L) ..... 200Ω to 1750Ω (Note 2)

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	48	12
Plastic DIP Package	51	N/A
PLCC Package	47	N/A
SOIC Package	72	N/A

Maximum Junction Temperature Ceramic ..... 175°C
Maximum Junction Temperature Plastic ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(For SMD; PLCC and SOIC - Lead Tips Only)

Die Characteristics

Transistor Count 224
Diode Count 28
Die Dimensions ..... 174 x 120
Substrate Potential ..... Connected
Process ..... Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. May Be Extended to 1900Ω With Application Circuit.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Unless Otherwise Specified, Typical Parameters are at T_A = 25°C, Min-Max Parameters are Over Operating Temperature Range, V_{B-} = -48V, V_{B+} = 5V, AG = DG = BG = 0V. All AC Parameters are specified at 600Ω 2-Wire Terminating Impedance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC TRANSMISSION PARAMETERS					
RX Input Impedance	300Hz to 3.4kHz (Note 4)	-	100	-	kΩ
TX Output Impedance	300Hz to 3.4kHz (Note 4)	-	-	20	Ω
4-Wire Input Overload Level	300Hz to 3.4kHz R_L = 1200Ω, 600Ω Reference	1.5	-	-	V_{PEAK}
2-Wire Return Loss	Matched for 600Ω (Note 4)				
SRL LO		26	35	-	dB
ERL		30	40	-	dB
SRL HI		30	40	-	dB
2-Wire Longitudinal to Metallic Balance Off Hook	Per ANSI/IEEE STD 455-1976 (Note 4) 300Hz to 3400Hz	58	63	-	dB
4-Wire Longitudinal Balance Off Hook	300Hz to 3400Hz (Note 4)	50	55	-	dB
Low Frequency Longitudinal Balance	R.E.A. Test Circuit	-	-	-67	dBmp
	I_{LINE} = 40mA T_A = 25°C (Note 4)	-	-	23	dBrnC
Longitudinal Current Capability	I_{LINE} = 40mA T_A = 25°C (Note 4)	-	-	30	mA_{RMS}
Insertion Loss	0dBm at 1kHz, Referenced 600Ω				
2-Wire/4-Wire		-	±0.05	±0.2	dB
4-Wire/2-Wire		-	±0.05	±0.2	dB
4-Wire/4-Wire		-	-	±0.2	dB

Electrical Specifications Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are Over Operating Temperature Range, $V_{B-} = -48V$, $V_{B+} = 5V$, AG = DG = BG = 0V. All AC Parameters are specified at 600Ω 2-Wire Terminating Impedance **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Response	300Hz to 3400Hz (Note 4) Referenced to Absolute Level at 1kHz, 0dBm Referenced 600Ω	-	±0.02	±0.05	dB
Level Linearity	Referenced to -10dBm (Note 4)				
2-Wire to 4-Wire and 4-Wire to 2-Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
Absolute Delay	(Note 4)				
2-Wire/4-Wire	300Hz to 3400Hz	-	-	1	µs
4-Wire/2-Wire	300Hz to 3400Hz	-	-	1	µs
4-Wire/4-Wire	300Hz to 3400Hz	-	-	1.5	µs
Transhybrid Loss, THL	(Note 4) See Figure 1	-	40	-	dB
Total Harmonic Distortion 2-Wire/4-Wire, 4-Wire/2-Wire, 4-Wire/4-Wire	Reference Level 0dBm at 600Ω 300Hz to 3400Hz (Note 4)	-	-	-52	dB
Idle Channel Noise	(Note 4)				
2-Wire and 4-Wire	C-Message	-	-	5	dBrnC
	Psophometric	-	-	-85	dBmp
	3kHz Flat	-	-	15	dBrn
Power Supply Rejection Ratio	(Note 4)				
V_{B+} to 2-Wire	30Hz to 200Hz, $R_L = 600Ω$	20	29	-	dB
V_{B+} to 4-Wire		20	29	-	dB
V_{B-} to 2-Wire		20	29	-	dB
V_{B-} to 4-Wire		20	29	-	dB
V_{B+} to 4-Wire	(Note 4)	30	-	-	dB
V_{B-} to 2-Wire	200Hz to 16kHz, $R_L = 600Ω$	30	-	-	dB
V_{B-} to 4-Wire		20	25	-	dB
V_{B-} to 4-Wire		20	25	-	dB
Ring Sync Pulse Width		50	-	500	µs
DC PARAMETERS					
Loop Current Programming					
Limit Range		20	-	60	mA
Accuracy		10	-	-	%
Loop Current During Power Denial	$R_L = 200Ω$	-	±3	±5	mA
Fault Currents					
TIP to Ground		-	30	-	mA
RING to Ground		-	60	-	mA
TIP and RING to Ground		-	90	-	mA

Electrical Specifications Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are Over Operating Temperature Range, $V_{B-} = -48V$, $V_{B+} = 5V$, AG = DG = BG = 0V. All AC Parameters are specified at 600Ω 2-Wire Terminating Impedance **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Switch Hook Detection Threshold		-	12	15	mA
Ground Key Detection Threshold		-	10	-	mA
Thermal $\overline{ALARM}$ Output	Safe Operating Die Temperature Exceeded	140	-	160	°C
Ring Trip Detection Threshold	$V_{RING} = 105V_{RMS}$, $f_{RING} = 20Hz$	-	10	-	mA
Ring Trip Detection Period		-	100	150	ms
Dial Pulse Distortion		-	0.1	0.5	ms
Relay Driver Outputs					
On Voltage V_{OL}	I_{OL} ($\overline{PR}$) = 60mA, I_{OL} ($\overline{RD}$) = 30mA	-	0.2	0.5	V
Off Leakage Current	$V_{OH} = 13.2V$	-	±10	±100	µA
TTL/CMOS Logic Inputs (F0, F1, RS, TEST, PRI)					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Input Current (F0, F1, RS, $\overline{TEST}$, PRI)	$0V \le V_{IN} \le 5V$	-	-	±100	µA
Logic Outputs					
Logic '0' V_{OL}	$I_{LOAD} = 800\mu A$	-	0.1	0.5	V
Logic '1' V_{OH}	$I_{LOAD} = 40\mu A$	2.7	-	-	V
Power Dissipation On Hook	Relay Drivers Off	-	200	-	mW
I_{B+}	$V_{B+} = 5.25V$, $V_{B-} = -58V$, $R_{LOOP} = \infty$	-	-	6	mA
I_{B-}	$V_{B+} = 5.25V$, $V_{B-} = -58V$, $R_{LOOP} = \infty$	-6	-	-	mA
UNCOMMITTED OP AMP PARAMETERS					
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Differential Input Resistance	(Note 4)	-	1	-	MΩ
Output Voltage Swing	$R_L = 10k\Omega$	-	±3	-	V_{P-P}
Small Signal GBW	(Note 4)	-	1	-	MHz

NOTE:

4. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Pin Descriptions

DIP/SOIC	PLCC	SYMBOL	DESCRIPTION
1	2	AG (Note 5)	Analog Ground - To be connected to zero potential. Serves as a reference for the transmit output and receive input terminals.
2	3	V_B+	Positive Voltage Source - most positive supply.
3	4	C_1	Capacitor #C_1 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function.
4	8	F1	Function Address #1 - A TTL and CMOS compatible input used with F0 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table. F1 should be toggled high after power is applied.
5	9	F0	Function Address #0 - A TTL and CMOS compatible input used with F1 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table.
6	10	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive pulse (50µs - 500µs) occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring delay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to 5.
7	11	$\overline{SHD}$	Switch Hook Detection - An active low LS TTL compatible logic output. A line supervisory output.
8	12	$\overline{GKD}$	Ground Key Detection - An active low LS TTL compatible logic output. A line supervisory output.
9	13	$\overline{TST}$	A TTL logic input. A low on this pin will set a latch and keep the SLIC in a power down mode until the proper F1, F0 state is set and will keep $\overline{ALM}$ low. See Truth Table.
10	17	$\overline{ALM}$	A LS TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded. When $\overline{TST}$ is forced low by an external control signal, $\overline{ALM}$ is latched low until the proper F1, F0 state and $\overline{TST}$ input is brought high. The $\overline{ALM}$ can be tied directly to the $\overline{TST}$ pin to power down the part when a thermal fault is detected and then reset with F0, F1. See Truth Table. It is possible to ignore transient thermal overload conditions in the SLIC by delaying the response to the $\overline{TST}$ pin from the $\overline{ALM}$. Care must be exercised in attempting this as continued thermal overstress may reduced component life.
11	18	I_{LMT}	Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions using a resistive voltage divider.
12	19	OUT1	The analog output of the spare operational amplifier.
13	20	-IN1	The inverting analog input of the spare operational amplifier.
14	22	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor and ring relay contact. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purpose.
15	24	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.
16	25	RFS	Ring Feed Sense - Senses RING side of the loop for Ground Key Detection. During Ring injected ringing the ring signal at this node is isolated from RF via the ring relay. For Tip injected ringing, the RF and RFS pins must be shorted.
17	27	V_{RX}	Receive Input, 4-Wire Side - A high impedance analog input. AC signals appearing at this input drive the Tip Feed and Ring Feed amplifiers differentially.
18	31	C_2	Capacitor #C_2 - An external capacitor to be connected between this terminal and ground. It prevents false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from power lines and other noise sources. This capacitor should be nonpolarized.
19	32	V_{TX}	Transmit Output, 4-Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Transhybrid balancing must be performed beyond this output to completely implement 2-Wire to 4-Wire conversion. This output is referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is necessary.

Pin Descriptions (Continued)

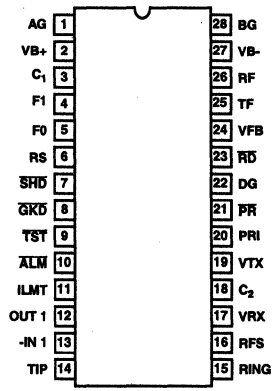
DIP/SOIC	PLCC	SYMBOL	DESCRIPTION
20	33	PRI	A TTL compatible input used to control $\overline{PR}$. PRI active High = $\overline{PR}$ active low.
21	34	$\overline{PR}$	An active low open collector output. Can be used to drive a Polarity Reversal Relay.
22	35	DG (Note 5)	Digital Ground - To be connected to zero potential. Serves as a reference for all digital inputs and outputs on the SLIC.
23	36	$\overline{RD}$	Ring Relay Driver - An active low open collector output. Used to drive a relay that switches ringing signals onto the 2-Wire line.
24	37	V_{FB}	Feedback input to the tip feed amplifier; may be used in conjunction with transmit output signal and the spare op amp to accommodate 2-Wire line impedance matching.
25	38	TF_2	Tip Feed - A low impedance analog output connected to the TIP terminal through a feed resistor. Functions with the RF terminal to provide loop current, and to feed voice signals to the telephone set and to sink longitudinal currents. Must be tied to TF_1.
NA	39	TF_1	Tie directly to TF_2 in the PLCC application.
26	41	RF_1	Ring Feed - A low impedance analog output connected to the RING terminal through a feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and to sink longitudinal currents. Tie directly to RF_2.
NA	42	RF_2	Tie directly to RF_1 in the PLCC application.
27	43	V_{B}-	The battery voltage source. The most negative supply.
28	44	BG (Note 5)	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
	1, 5, 6, 7, 14, 15, 16, 21, 23, 26, 28, 29, 30, 40	NC	No internal connection.

NOTE:

5. All grounds (AG, BG, and DG) must be applied before V_{B+} or V_{B-}. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Pinouts

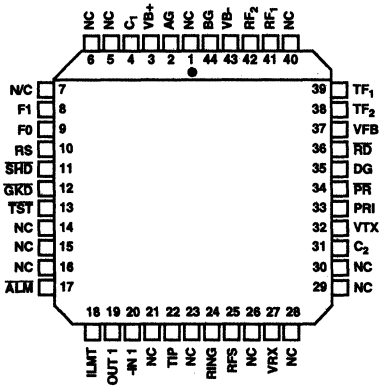
HC-5509B (PDIP, SOIC)
TOP VIEW



TRUTH TABLE

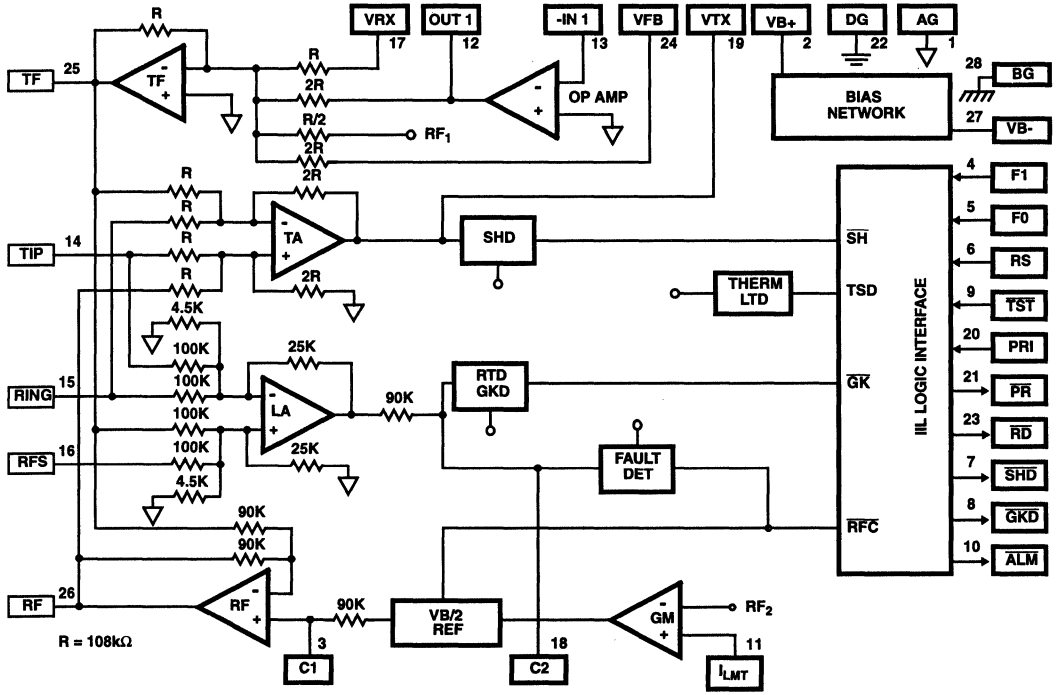
F1	F0	ACTION
0	0	Normal Loop Feed
0	1	$\overline{RD}$ Active (Ringing)
1	0	Power Down Latch RESET
1	0	Power On RESET
1	1	Loop Power Denial Active

HC-5509B (PLCC)
TOP VIEW



Functional Diagram

DIP OR SOIC



Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or $30mA_{RMS}$, $15mA_{RMS}$ per leg, without any performance degradation.

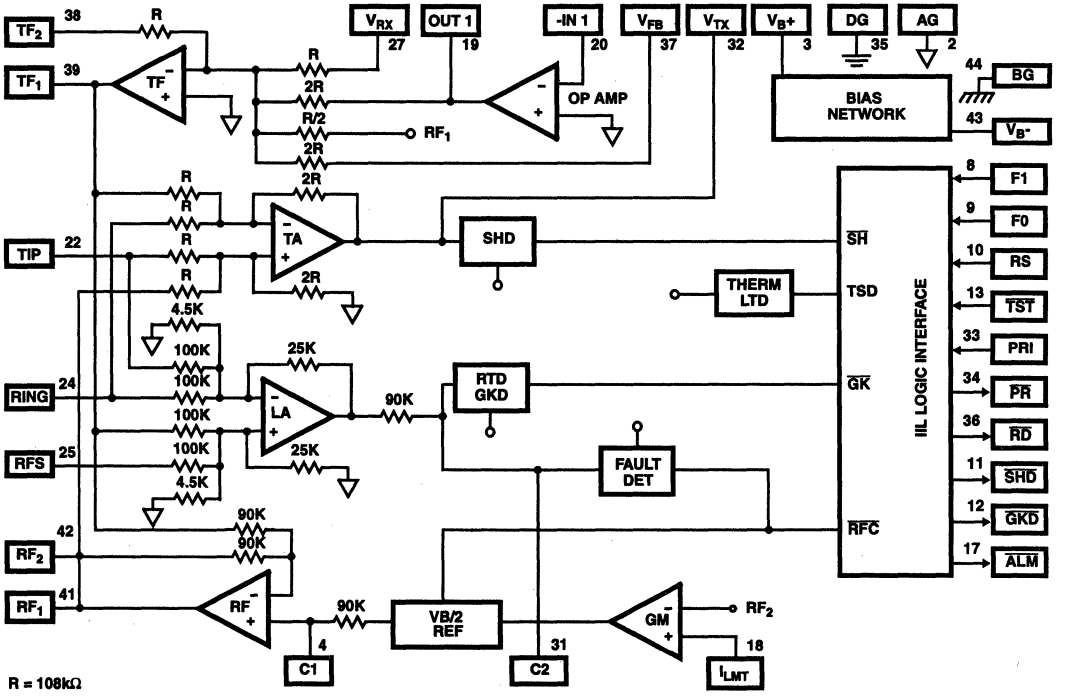
TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
T/GND, R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
50/60Hz Current T/GND, R/GND	11 Cycles, Limited to $10A_{RMS}$	700 (Plastic)	V_{RMS}

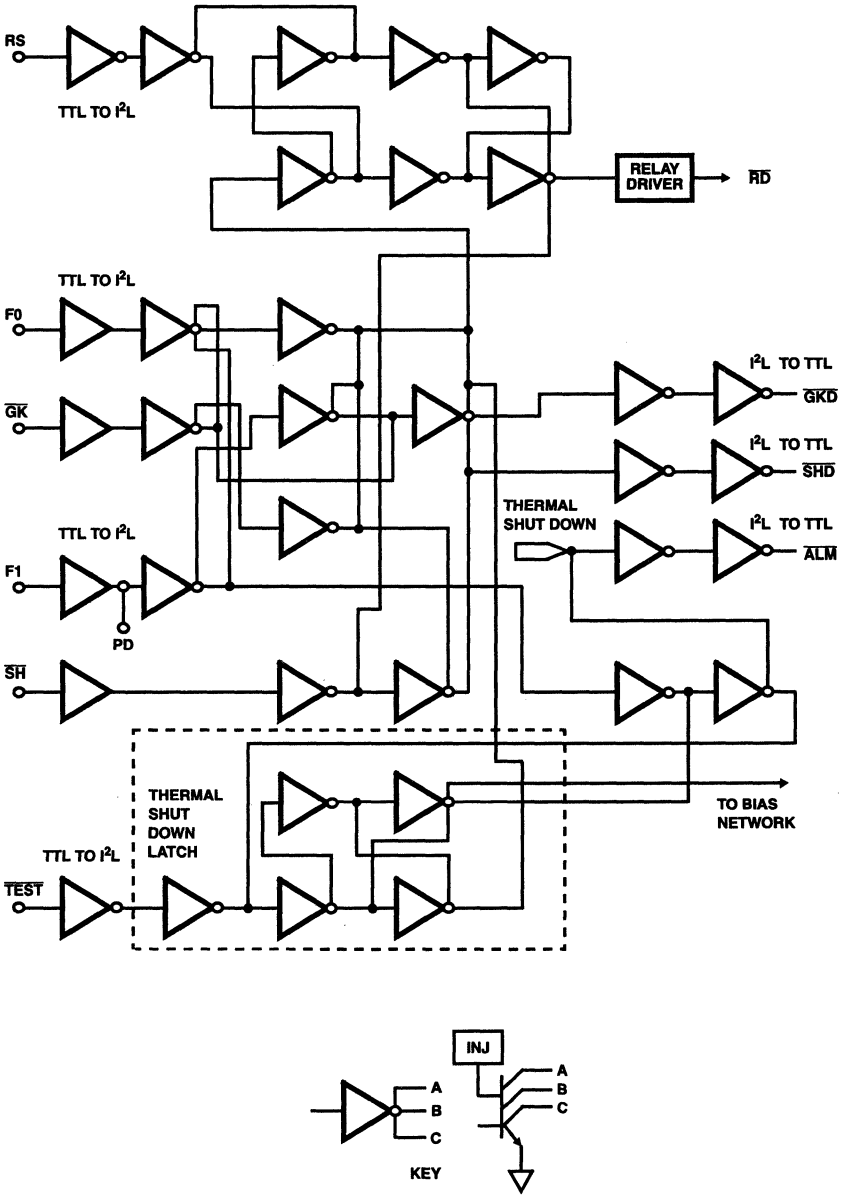
4 WIRED COMMUNICATIONS

Functional Diagram (Continued)

PLCC



Logic Diagram



Typical Applications

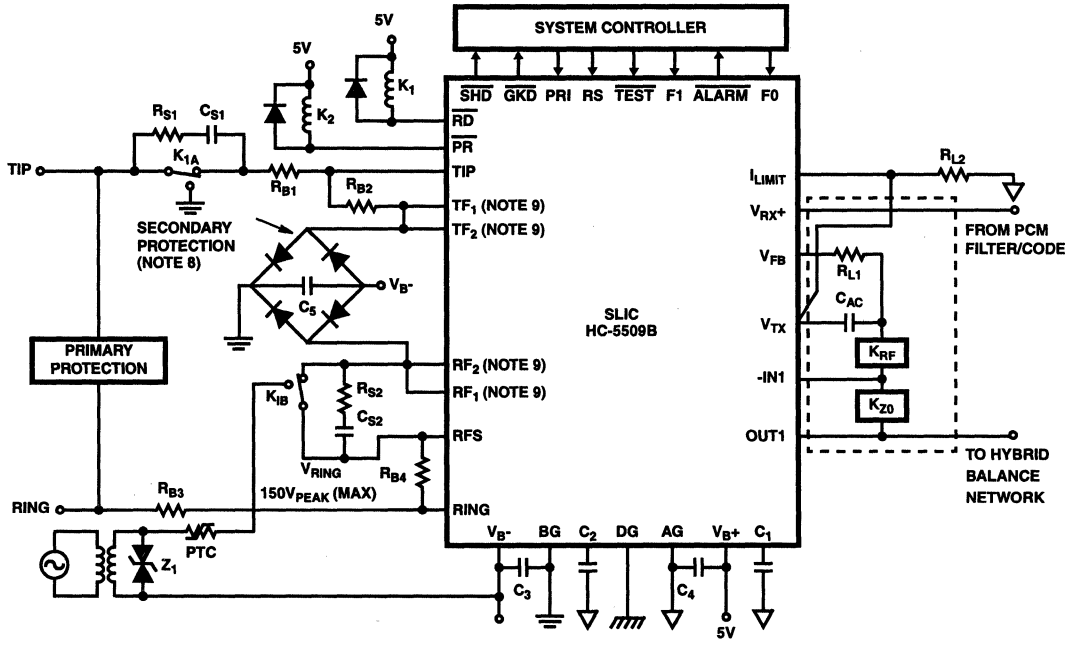


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values

C_1 = 0.5µF, 30V

C_2 = 1.0µF ±10%, 20V (for other values of C2, refer to AN9667)

C_3 = 0.01µF, 100V, ±20%

C_4 = 0.01µF, 100V, ±20%

C_5 = 0.01µF, 100V, ±20%

C_{AC} = 0.5µF, 20V

KZ_0 = 60kΩ, (Z_0 = 600Ω, K = Scaling Factor = 100)

R_{L1}, R_{L2}; Current Limit Setting Resistors:

$R_{L1} + R_{L2} > 90k\Omega \rightarrow$ offset

$I_{LIMIT} = (0.6)\ (R_{L1} + R_{L2})/(200 \times R_{L2})$, R_{L1} typically 100kΩ

K_{RF} = 20kΩ, RF = 2(R_{B2} + R_{B4}), K = Scaling Factor = 100)

$R_{B1} = R_{B2} = R_{B3} = R_{B4}$ = 50Ω (1% absolute, matching requirements covered in a Tech Brief)

$R_{S1} = R_{S2}$ = 1kΩ typically

$C_{S1} = C_{S2}$ = 0.1µF, 200V typically, depending on V_{Ring} and line length.

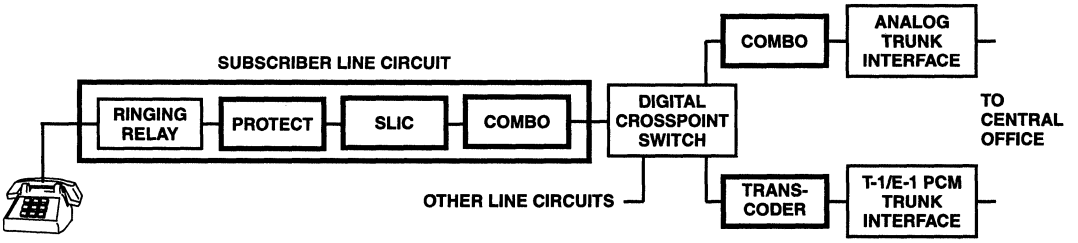
Z_1 = 150V to 200V transient protector. PTC used as ring generator ballast.

NOTES:

6. All grounds (AG, BG, and DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
7. Application shows Ring Injected Ringing, a Balanced or Tip injected configuration may be used.
8. Secondary protection diode bridge recommended is 3A, 200V type.
9. TF_1, TF_2 and RF_1, RF_2 are on PLCC only and should be connected together as shown.

Private Automatic Branch Exchange (PABX)

PABX SWITCH



	USA	ROW
SLICs	HC-5502B(1) HC5526 HC5515 HC-5524	HC-5504B(1) HC5526 HC5515 HC-5524
Combos	CD22354A	CD22357A
Transcoder	HC5560	CD22103A
Protection	SGT06U13	SGT06U13

HARRIS SEMICONDUCTOR

HC-5504B1

SLIC
Subscriber Line Interface Circuit

January 1997

Features

- Low Cost Version of the HC-5504B
- Capable of 5V or 12V (V_B+) Operation
- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (41mA)
- Internal Ring Relay Driver
- Allows Interfacing With Negative Superimposed Ringing Systems
- Low Power Consumption During Standby
- Switch Hook Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBXs
- Related Literature
  - AN549, The HC-5502S/4X Telephone Subscriber Line Interface Circuits (SLIC)
  - AN571, Using Ring Sync with HC-5502A and HC-5504 SLICs

Description

The Harris SLIC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Harris dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

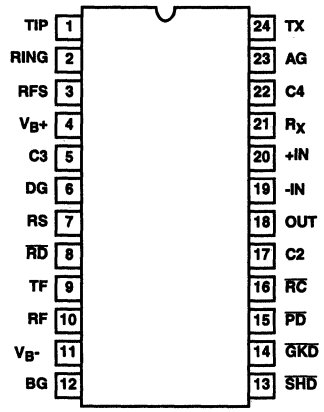
The Harris SLIC is ideally suited for the design of new digital PBX systems by eliminating bulky hybrid transformers.

Ordering Information

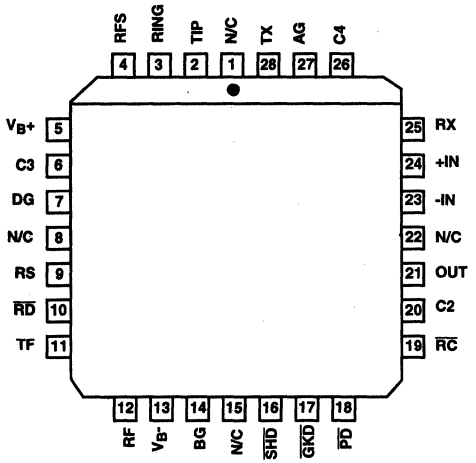
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC3-5504B1-5	0 to 75	24 Ld PDIP	E24.6
HC4P5504B1-5	0 to 75	28 Ld PLCC	N28.45
HC9P5504B1-5	0 to 75	24 Ld SOIC	M24.3

Pinouts

HC-5504B1 (PDIP, SOIC)
TOP VIEW



HC-5504B1 (PLCC)
TOP VIEW



4 WIRED COMMUNICATIONS

File Number 4125.1

Absolute Maximum Ratings (Note 1)

Maximum Continuous Supply Voltages
- (V_{B-}) ..... -60 to 0.5V
- (V_{B+}) ..... -0.5 to 15V
- (V_{B+} - V_{B-}) 75V

Relay Drive Voltage (V_{RD}) ..... -0.5 to 15V

Operating Conditions

Operating Temperature Range
- HC-5504B1-5 ..... 0°C to 75°C

Relay Driver Voltage (V_{RD}) ..... 5V to 12V
Positive Supply Voltage (V_{B+}) ... 4.75V to 5.25V or 10.8V to 13.2V
Negative Supply Voltage (V_{B-}) ..... -36V to -58V
High Level Logic Input Voltage 2.4V
Low Level Logic Input Voltage 0.6V
Loop Resistance (R_L) ..... 200Ω to 1200Ω

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
24 Lead PDIP	65
24 Lead SOIC	75
28 Lead PLCC	65

Maximum Junction Temperature Plastic ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(PLCC and SOIC - Lead Tips Only)

Die Characteristics

Transistor Count 185
Diode Count 36
Die Dimensions ..... 137 x 102
Substrate Potential ..... Connected
Process ..... Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Unless Otherwise Specified, V_{B-} = -48V, V_{B+} = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I_{LONG} = 0 (Note 2), V_{B+} = 12V	-	170	235	mW
Off Hook Power Dissipation	R_L = 600Ω, I_{LONG} = 0 (Note 3), V_{B+} = 12V	-	425	550	mW
Off Hook I_{B+}	R_L = 600Ω, I_{LONG} = 0 (Note 3), T_A = -40°C	-	-	6.0	mA
Off Hook I_{B+}	R_L = 600Ω, I_{LONG} = 0 (Note 3), T_A = 25°C	-	-	5.3	mA
Off Hook I_{B-}	R_L = 600Ω, I_{LONG} = 0 (Note 3)	-	35	41	mA
Off Hook Loop Current	R_L = 1200Ω, I_{LONG} = 0 (Note 3)	-	21	-	mA
Off Hook Loop Current	R_L = 1200Ω, V_{B-} = -42V, I_{LONG} = 0 (Note 3) T_A = 25°C	17.5	-	-	mA
Off Hook Loop Current	R_L = 200Ω, I_{LONG} = 0 (Note 3)	36	41	48	mA
Fault Currents					
TIP to Ground		-	14	-	mA
RING to Ground		-	55	-	mA
TIP to RING		-	41	-	mA
TIP and RING to Ground		-	55	-	mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	V_{RD} = 12V, $\overline{RC}$ = 1 = HIGH, T_A = 25°C	-	-	100	µA
Ring Trip Detection Period	R_L = 600Ω	-	2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD}$ = V_{OL}	10	-	-	mA
	$\overline{SHD}$ = V_{OH}	-	-	5	mA

Electrical Specifications Unless Otherwise Specified, V_{B-} = -48V, V_{B+} = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Ground Key Detection Threshold	$\overline{GKD}$ = V_{OL}	20	-	-	mA
	$\overline{GKD}$ = V_{OH}	-	-	10	mA
Loop Current During Power Denial	R_L = 200Ω	-	±2	-	mA
Dial Pulse Distortion		0	-	5	ms
Receive Input Impedance	(Note 4)	-	110	-	kΩ
Transmit Output Impedance	(Note 4)	-	10	20	Ω
2-Wire Return Loss	(Referenced to 600Ω + 2.16µF), (Note 4)				
SR_L LO		-	15.5	-	dB
ER_L		-	24	-	dB
SR_L HI		-	31	-	dB
Longitudinal Balance	$1V_{RMS}$ 200Hz - 3400Hz, (Note 4) IEEE Method				
2-Wire Off Hook	0°C ≤ T_A ≤ 75°C	53	58	-	dB
2-Wire On Hook		53	58	-	dB
4-Wire Off Hook		50	58	-	dB
Low Frequency Longitudinal Balance	R.E.A. Method, (Note 4), R_L = 600Ω	-	-	23	dBrnC
	0°C ≤ T_A ≤ 75°C	-	-	-67	dBm0p
Insertion Loss	At 1kHz, 0dBm Input Level, Referenced 600Ω				
2-Wire to 4-Wire, 4-Wire to 2-Wire		-	±0.05	±0.2	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 4)	-	±0.02	±0.05	dB
Idle Channel Noise	(Note 4)				
2-Wire to 4-Wire, 4-Wire to 2-Wire		-	1	5	dBrnC
		-	-89	-85	dBm0p
Absolute Delay	(Note 4)				
2-Wire to 4-Wire, 4-Wire to 2-Wire		-	-	2	ms
Trans Hybrid Loss	Balance Network Set Up for 600Ω Termination at 1kHz	30	40	-	dB
Overload Level	V_{B+} = +5V	1.5	-	-	Vpeak
2-Wire to 4-Wire, 4-Wire to 2-Wire	V_{B+} = 12V	1.75	-	-	Vpeak
Level Linearity	At 1kHz, (Note 4) Referenced to 0dBm Level				
2-Wire to 4-Wire, 4-Wire to 2-Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB

Electrical Specifications Unless Otherwise Specified, V_{B-} = -48V, V_{B+} = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio	(Note 4)				
V_{B+} to 2-Wire	30 - 60Hz, R_L = 600Ω	15	-	-	dB
V_{B+} to Transmit		15	-	-	dB
V_{B-} to 2-Wire		15	-	-	dB
V_{B-} to Transmit		15	-	-	dB
V_{B+} to 2-Wire	200 - 16kHz, R_L = 600Ω	30	-	-	dB
V_{B+} to Transmit		30	-	-	dB
V_{B-} to 2-Wire		30	-	-	dB
V_{B-} to Transmit		30	-	-	dB
Logic Input Current (RS, $\overline{RC}$, $\overline{PD}$)	$0V \le V_{IN} \le 5V$	-	-	±100	µA
Logic Inputs					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} 800µA, V_{B+} = 12V, 5V	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} 80µA, V_{B+} = 12V	2.7	5.0	5.5	V
	I_{LOAD} 40µA, V_{B+} = 5V	2.7	-	5.0	V

Uncommitted Op Amp Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Input Bias Current		-	20	-	nA
Differential Input Resistance	(Note 4)	-	1	-	MΩ
Output Voltage Swing	R_L = 10K, V_{B+} = 12V	-	±5	-	Vpeak
	R_L = 10K, V_{B+} = 5V	-	±3	-	Vpeak
Output Resistance	A_{VCL} = 1 (Note 4)	-	10	-	Ω
Small Signal GBW	(Note 4)	-	1	-	MHz

NOTES:

3. I_{LONG} = Longitudinal Current
4. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Pin Descriptions

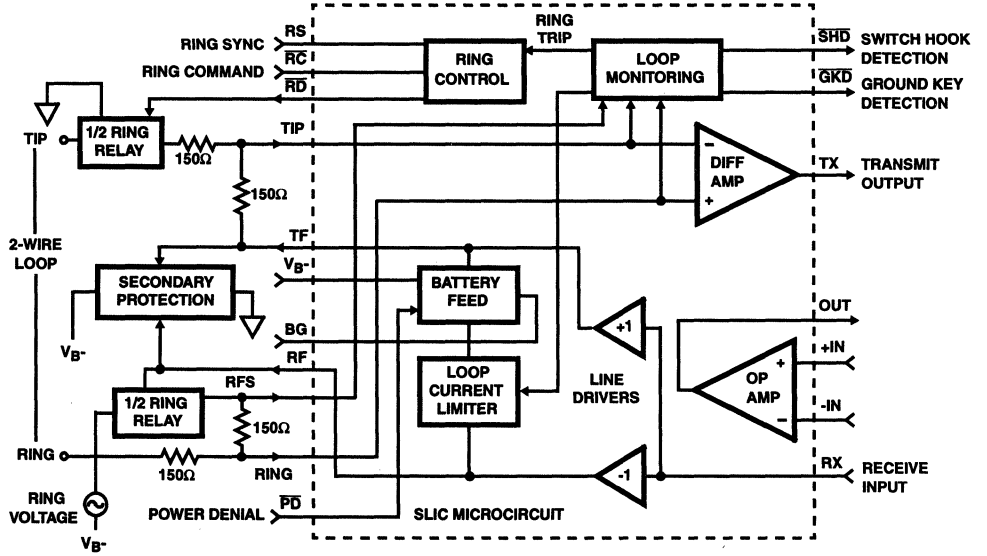
28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
2	1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring purposes.
3	2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
4	3	RFS	Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.
5	4	$V_{B}+$	Positive Voltage Source - Most positive supply. $V_{B}+$ is typically 12V or 5V.
6	5	C_3	Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering $V_{B}-$. Typical value is 0.3µF, 30V.
7	6	DG	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
9	7	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock should be arranged such that a positive pulse transition occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring relay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to 5V.
10	8	$\overline{RD}$	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
11	9	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
12	10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
13	11	$V_{B}-$	Negative Voltage Source - Most negative supply. $V_{B}-$ is typically -48V with an operational range of -42V to -58V. Frequently referred to as "battery".
14	12	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
16	13	$\overline{SHD}$	Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
17	14	$\overline{GKD}$	Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.
18	15	$\overline{PD}$	Power Denial - A low active TTL - Compatible logic input. When enabled, the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.
19	16	$\overline{RC}$	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off- hook ($\overline{SHD}$ = 0).
20	17	C_2	Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15µF, 10V. This capacitor is not used if ground key function is not required and (Pin 17) may be left open or connected to digital ground.
21	18	OUT	The analog output of the spare operational amplifier. The output voltage swing is typically ±5V.
23	19	-IN	The inverting analog input of the spare operational amplifier.
24	20	+IN	The non-inverting analog input of the spare operational amplifier.

Pin Descriptions (Continued)

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
25	21	RX	Receive Input, Four Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed terminals, which in turn drive tip and ring through 300Ω of feed resistance on each side of the line.
26	22	C_4	Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near by power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5µF, to 1.0µF, 20V. This capacitor should be nonpolarized.
27	23	AG	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
28	24	TX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
1, 8, 15, 22		NC	No internal connection.

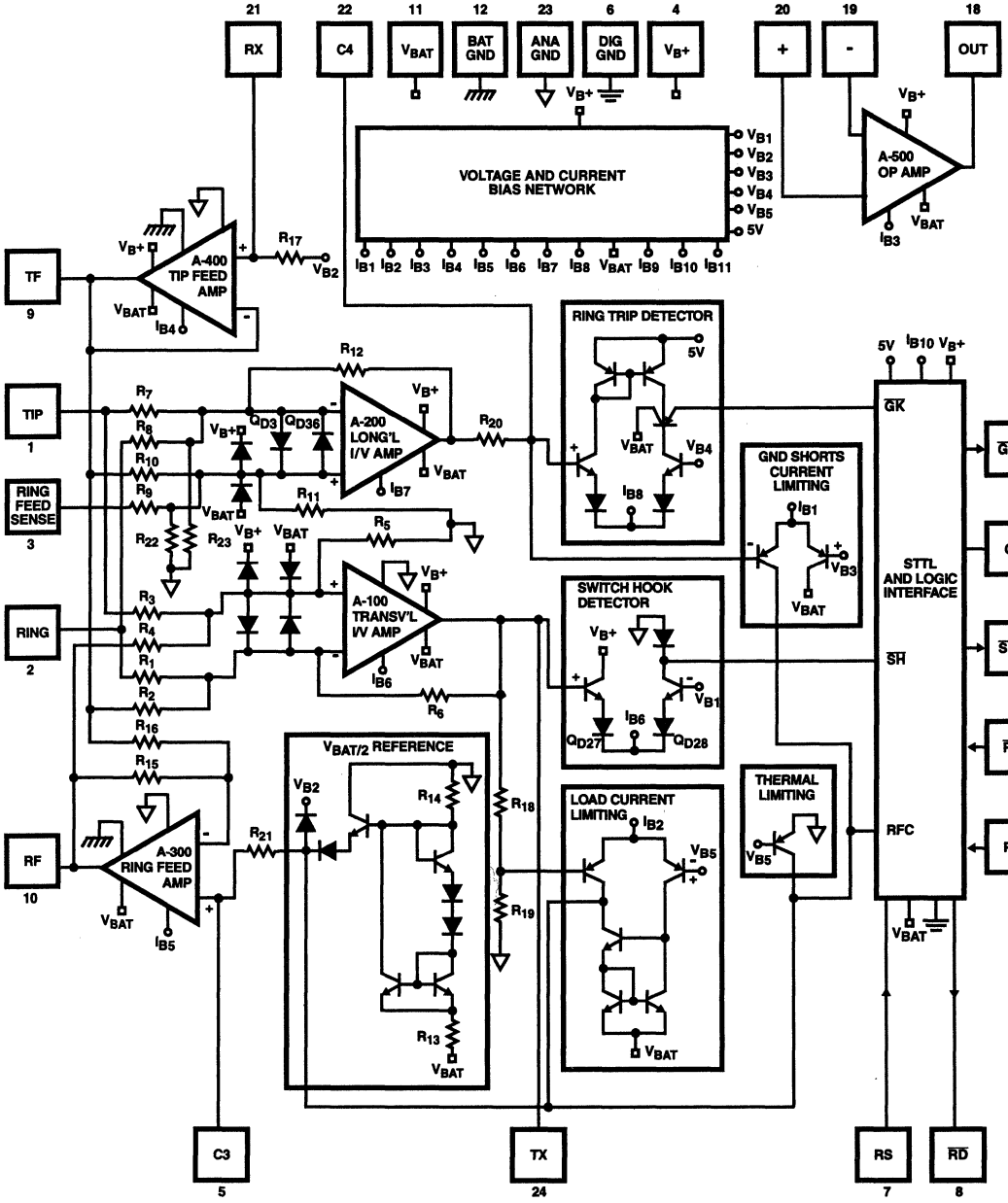
NOTE: All grounds (AG, BG, and DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Functional Diagram



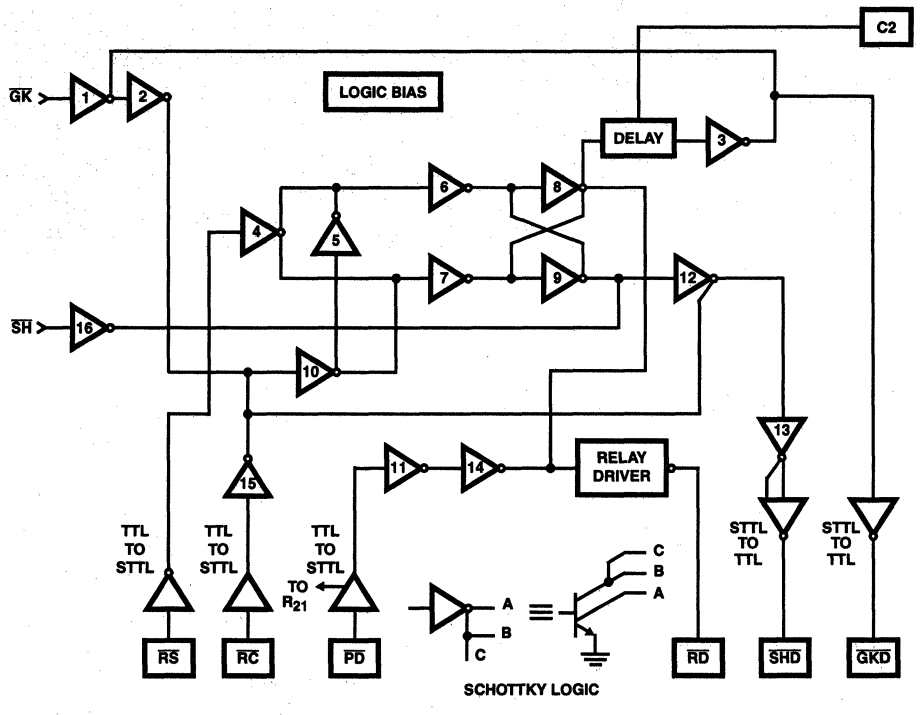
Schematic

SLIC FUNCTIONAL SCHEMATIC
DIP/SOIC Pin Numbers Shown



Schematic (Continued)

LOGIC GATE SCHEMATIC



Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or $30mA_{RMS}$, $15mA_{RMS}$ per leg, without any performance degradation.

TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
50/60Hz Current T/GND R/GND	11 Cycles Limited to $10A_{RMS}$	700 (Plastic)	V_{RMS}

Applications Diagram

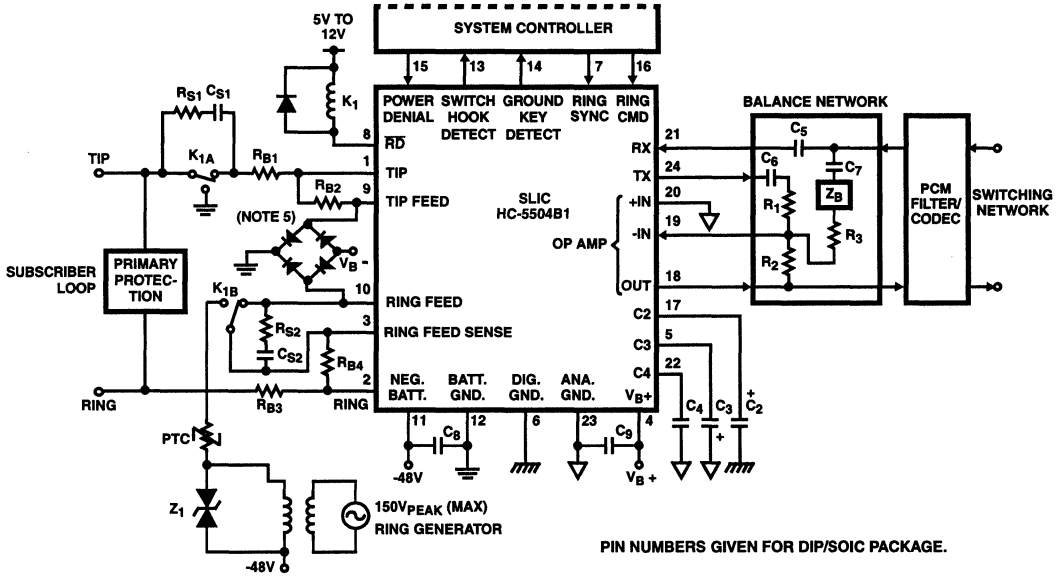


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values

C_2 = 0.15µF, 10V

C_3 = 0.3µF, 30V

C_4 = 0.5µF to 1.0µF, 10%, 20V (Should be nonpolarized)

C_5 = 0.5µF, 20V

C_6 = C_7 = 0.5µF (10% Match Required) (Note 6)

C_8 = 0.01µF, 100V

C_9 = 0.01µF, 20V, ±20%

R_1 = R_2 = R_3 = 100k (0.1% Match Required, 1% absolute value) Z_B = 0 for 600Ω Terminations (Note 6).

R_{B1} = R_{B2} = R_{B3} = R_{B4} = 150Ω (0.1% Match Required, 1% absolute value).

R_{S1} = R_{S2} =1kΩ, typically.

C_{S1} = C_{S2} = 0.1µF, 200V typically, depending on V_{RING} and line length.

Z_1 = 150V to 200V transient protection.

PTC used as ring generator ballast.

NOTES:

5. Secondary protection diode bridge recommended is a 2A, 200V type.
6. To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C_6-R_1 and R_2 and C_7-Z_B-R_3, to match in impedance to within 0.3%. Thus, if C_6 and C_7 are 1µF each, a 20% match is adequate. It should be noted that the transmit output to C_6 sees a -22V step when the loop is closed. Too large a value for C_6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

   A 0.5µF and 100kΩ gives a time constant of 50ms. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.
7. All grounds (AG, BG, and DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
8. Application shows Ring Injected Ringing, Balanced or Tip injected configuration may be used.

HARRIS SEMICONDUCTOR

HC-5502B1

SLIC
Subscriber Line Interface Circuit

January 1997

Features

- Low Cost Version of HC-5502B
- Capable of 12V or 5V (V_B+) Operation
- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (30mA)
- Internal Ring Relay Driver
- Low Power Consumption During Standby
- Switch Hook, Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBXs
- Related Literature
  - AN549, The HC-5502S/4X Telephone Subscriber Line Interface Circuits (SLIC)
  - AN571, Using Ring Sync with HC-5502A and HC-5504 SLICs

Description

The Harris SLIC incorporates many of the BORSHT function on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Harris dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

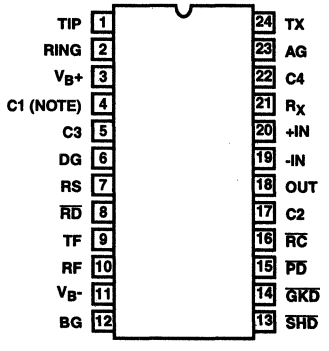
The Harris SLIC is ideally suited for the design of new digital PBX systems, by eliminating bulky hybrid transformers.

Ordering Information

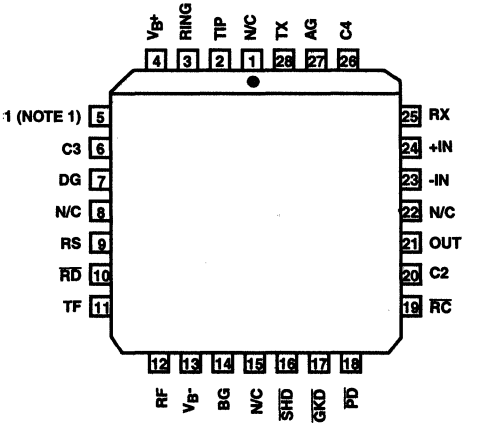
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC3-5502B1-5	0 to 75	24 Ld PDIP	E24.6
HC4P5502B1-5	0 to 75	28 Ld PLCC	N28.45
HC9P5502B1-5	0 to 75	24 Ld SOIC	M24.3

Pinouts

HC-5502B1 (PDIP, SOIC)
TOP VIEW



HC-5502B1 (PLCC)
TOP VIEW



NOTE: Optional.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4127.1**

Absolute Maximum Ratings (Note 1)

Supply Voltage
(V_{B-}) ..... -60 to 0.5V
(V_{B+}) ..... -0.5 to 15V
(V_{B+} - V_{B-}) 75V
Relay Drive Voltage (V_{RD}) ..... -0.5 to 15V

Operating Conditions

Relay Driver Voltage (V_{RD}) ..... 5V to 12V
Positive Supply Voltage (V_{B+}) ... 4.75V to 5.25V or 10.8V to 13.2V
Negative Supply Voltage (V_{B-}) ..... -42V to -58V
High Level Logic Input Voltage 2.4V
Low Level Logic Input Voltage 0.6V
Loop Resistance (R_L) ..... 200 to 1200Ω
Operating Temperature Range
HC-5502B1-5 ..... 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
24 Lead PDIP	65
24 Lead SOIC	75
28 Lead PLCC	65

Maximum Junction Temperature Plastic ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC and PLCC - Lead Tips Only)

Die Characteristics

Transistor Count 183
Diode Count 33
Die Dimensions ..... 137 x 102 mils
Substrate Potential ..... V_{B-}
Process ..... Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Unless Otherwise Specified, V_{B-} = -48V, V_{B+} = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I_{LONG} = 0 (Note 4), V_{B+} = 12V	-	135	235	mW
Off Hook Power Dissipation	R_L = 600Ω, I_{LONG} = 0 (Note 4), V_{B+} = 12V	-	450	690	mW
Off Hook I_{B+}	R_L = 600Ω, I_{LONG} = 0 (Note 4), T_A = -40°C	-	-	6.0	mA
Off Hook I_{B+x}	R_L = 600Ω, I_{LONG} = 0 (Note 4), T_A = 25°C	-	-	5.3	mA
Off Hook I_{B-}	R_L = 600Ω, I_{LONG} = 0 (Note 4)	-	-	39	mA
Off Hook Loop Current	R_L = 1200Ω, I_{LONG} = 0 (Note 4)	-	21	-	mA
Off Hook Loop Current	R_L = 1200Ω, V_{B-} = -42V, I_{LONG} = 0 (Note 4), T_A = 25°C	17.5	-	-	mA
Off Hook Loop Current	R_L = 200Ω, I_{LONG} = 0 (Note 4)	25.5	30	34.5	mA
Fault Currents					
TIP to Ground		-	14	-	mA
RING to Ground		-	47	-	mA
TIP to RING		-	30	-	mA
TIP and RING to Ground		-	47	-	mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	V_{RD} = 12V, $\overline{RC}$ = 1 = HIGH, T_A = 25°C	-	-	100	µA
Ring Trip Detection Period	R_L = 600Ω, T_A = 25°C	-	2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD}$ = V_{OL}	10	-	-	mA
	$\overline{SHD}$ = V_{OH}	-	-	5	mA
Ground Key Detection Threshold	$\overline{GKD}$ = V_{OL}	20	-	-	mA
	$\overline{GKD}$ = V_{OH}	-	-	10	mA

Electrical Specifications Unless Otherwise Specified, V_{B-} = -48V, V_{B+} = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Loop Current During Power Denial	R_L = 200Ω	-	±2	-	mA
Dial Pulse Distortion		0	-	5	ms
Receive Input Impedance	(Note 3)	-	110	-	kΩ
Transmit Output Impedance	(Note 3)	-	10	20	Ω
Two Wire Return Loss	Referenced to 600Ω +2.16µF (Note 3)				
SRL LO		-	15.5	-	dB
ERL		-	24	-	dB
SRL HI		-	31	-	dB
Longitudinal Balance	$1V_{RMS}$ 200Hz - 3400Hz, (Note 3)				
2-Wire Off Hook	IEEE Method $0°C \le T_A \le 75°C$	53	58	-	dB
2-Wire On Hook		53	58	-	dB
4-Wire Off Hook		50	58	-	dB
Low Frequency Longitudinal Balance	R.E.A. Method, (Note 3) R_L = 600Ω, $0°C \le T_A \le 75°C$	-	-	23	dBrnC
		-	-	-67	dBm0p
Insertion Loss 2-Wire to 4-Wire, 4-Wire to 2-Wire	at 1kHz, 0dBm Input Level, Referenced 600Ω	-	±0.05	±0.2	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 3)	-	±0.02	±0.05	dB
Idle Channel Noise 2-Wire to 4-Wire, 4-Wire to 2-Wire	(Note 3)	-	1	5	dBrnC
		-	-89	-85	dBm0p
Absolute Delay 2-Wire to 4-Wire, 4-Wire to 2-Wire	(Note 3)	-	-	2	µs
Trans Hybrid Loss	Balance Network Set Up for 600Ω Termination at 1kHz	30	40	-	dB
Overload Level 2-Wire to 4-Wire, 4-Wire to 2-Wire	V_{B+} = 5V	1.5			V_{PEAK}
	V_{B+} = 12V	1.75	-	-	V_{PEAK}
Level Linearity	at 1kHz, (Note 3) Referenced to 0dBm Level				
2-Wire to 4-Wire, 4-Wire to 2-Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB

Electrical Specifications Unless Otherwise Specified, V_{B^-} = -48V, V_{B^+} = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio	(Note 3)				
V_{B^+} to 2-Wire	30 - 60Hz, R_L = 600Ω	15	-	-	dB
V_{B^+} to Transmit		15	-	-	dB
V_{B^-} to 2-Wire		15	-	-	dB
V_{B^-} to Transmit		15	-	-	dB
V_{B^+} to 2-Wire	200 - 16kHz, R_L = 600Ω	30	-	-	dB
V_{B^+} to Transmit		30	-	-	dB
V_{B^-} to 2-Wire		30	-	-	dB
V_{B^-} to Transmit		30	-	-	dB
Logic Input Current (RS, $\overline{RC}$, $\overline{PD}$)	0V ≤ V_{IN} ≤ 5V	-	-	±100	µA
Logic Inputs					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} 800µA, V_{B^+} = 12V, 5V	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} 80µA, V_{B^+} = 12V	2.7	5.0	5.5	V
	I_{LOAD} 40µA, V_{B^+} = 5V	2.7	-	5.0	V

Uncommitted Op Amp Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Input Bias Current		-	20	-	nA
Differential Input Resistance	(Note 3)	-	1	-	MΩ
Output Voltage Swing	R_L = 10kΩ, V_{B^+} = 12V	-	±5	-	V_{PEAK}
	R_L = 10kΩ, V_{B^+} = 5V	-	±3	-	V_{PEAK}
Output Resistance	A_{VCL} = 1 (Note 3)	-	10	-	Ω
Small Signal GBW	(Note 3)	-	1	-	MHz

NOTES:

3. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterised upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.
4. I_{LONG} = Longitudinal Current.

Pin Descriptions

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
2	1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring process.
3	2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
4	3	$V_{B}+$	Positive Voltage Source - Most positive supply. $V_{B}+$ is typically 12V or 5V.
5	4	C_1	Capacitor #1 - Optional Capacitor used to improve power supply rejection. This pin should be left open if unused.
6	5	C_3	Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering $V_{B}-$ supply. Typical value is 0.3µF, 30V.
7	6	DG	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC.
9	7	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock should be arranged such that a positive transition occurs on the negative going zero crossing of the ring voltage source, ensuring that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If synchronization is not required, tie to 5V.
10	8	$\overline{RD}$	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
11	9	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
12	10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signal to the telephone set, and sink longitudinal current.
13	11	$V_{B}-$	Negative Voltage Source - Most negative supply. $V_{B}-$ is typically -48V with an operational range of -42V to -58V. Frequently referred to as "battery".
14	12	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
16	13	$\overline{SHD}$	Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
17	14	$\overline{GKD}$	Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.
18	15	$\overline{PD}$	Power Denial - A low active TTL - Compatible logic input. When enabled the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.
19	16	$\overline{RC}$	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next rising edge of the ring sync ($\overline{RS}$) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off- hook ($\overline{SHD}$ = 0).
20	17	C_2	Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15µF, 10V. This capacitor is not used if ground key function is not required.
21	18	OUT	The analog output of the spare operational amplifier.
23	19	-IN	The inverting analog input of the spare operational amplifier.

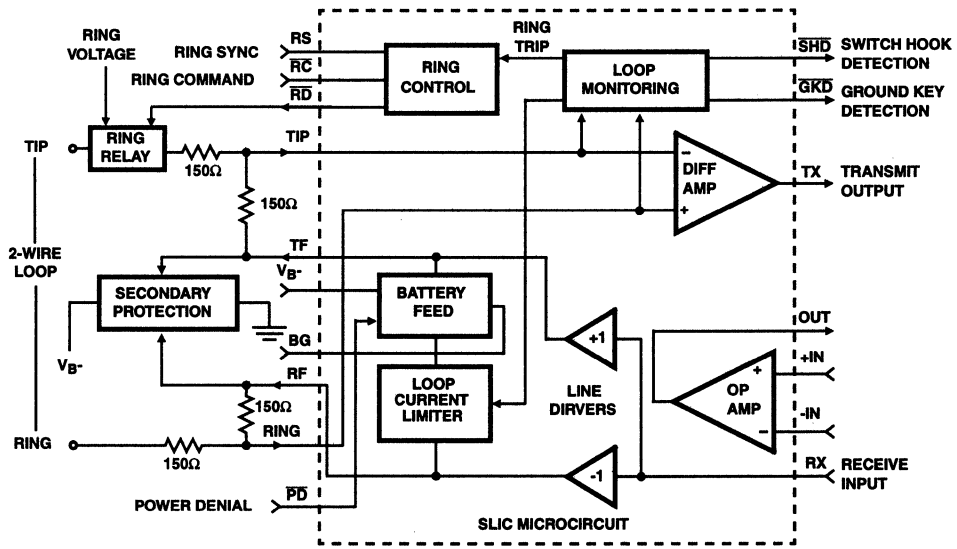
Pin Descriptions (Continued)

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
24	20	+IN	The non-inverting analog input of the spare operational amplifier.
25	21	RX	Receive Input, Four Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed amplifiers, which in turn drive tip and ring through 300Ω of feed resistance on each side of the line.
26	22	C_4	Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from nearby power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5µF to 1.0µF, 20V. This capacitor should be nonpolarized.
27	23	AG	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
28	24	TX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
1, 8, 5, 22		NC	No Internal Connection.

NOTE:

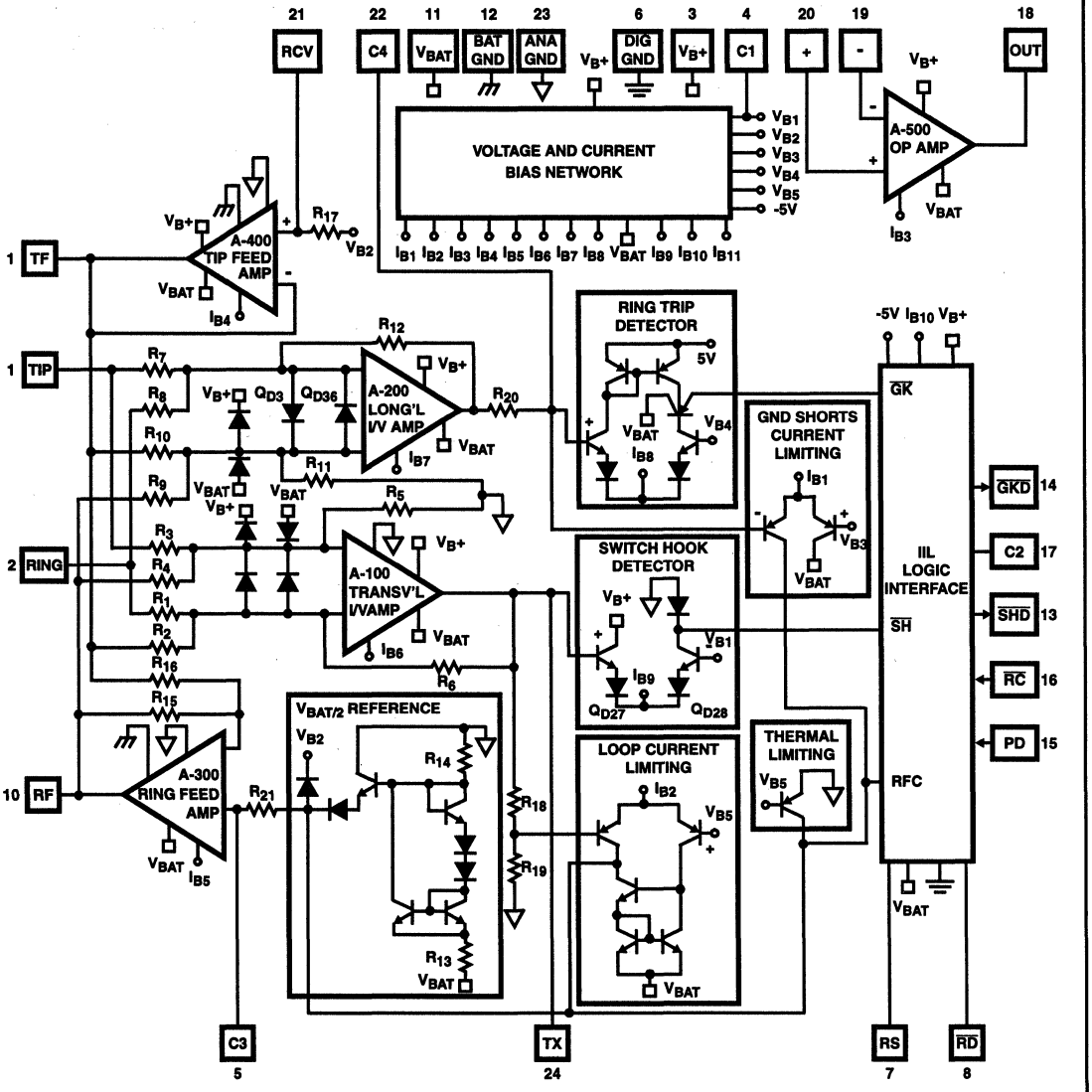
5. All grounds (AG, BG, and DG) must be applied before V_{B+} or V_{B-}. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Functional Diagram



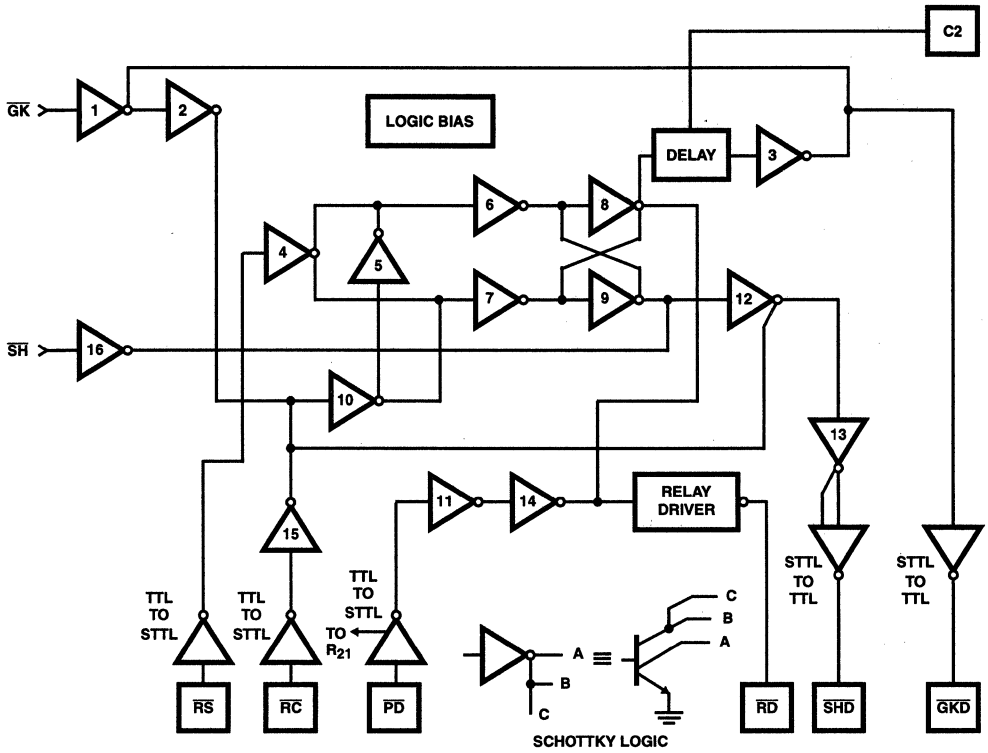
Schematic

SLIC FUNCTIONAL SCHEMATIC
Pin Numbers for DIP/SOIC Package



Logic Diagram

LOGIC GATE SCHEMATIC



Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or $30mA_{RMS}$, $15mA_{RMS}$ per leg, without any performance degradation.

TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
50/60Hz Current T/GND R/GND	11 Cycles Limited to $10A_{RMS}$	700 (Plastic)	V_{RMS}

Applications Diagram

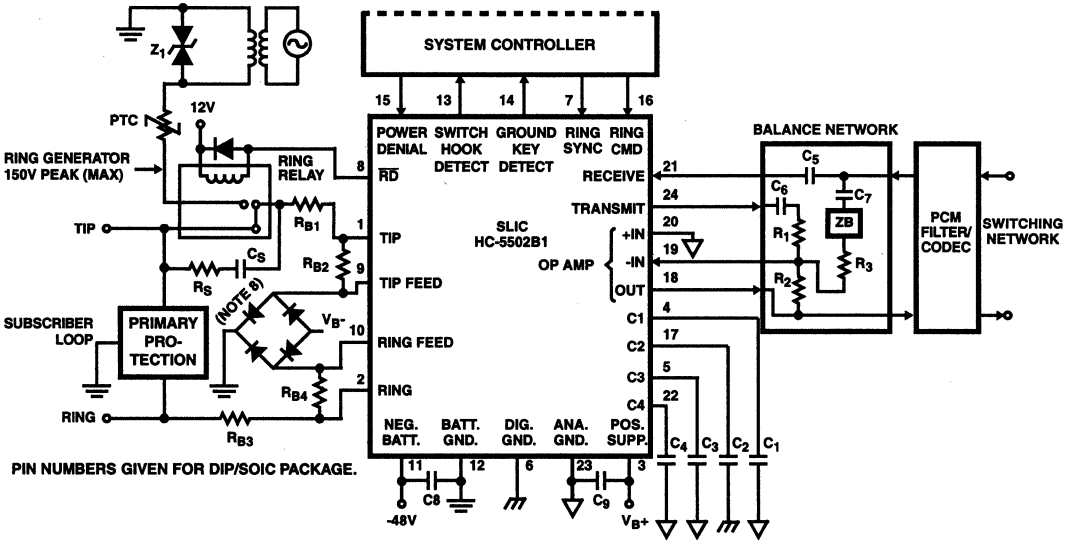


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values

C_1 = 0.5µF (Note 6)

C_2 = 0.15µF, 10V

C_3 = 0.3µF, 30V

C_4 = 0.5µF to 1.0µF, 10%, 20V (Should be nonpolarized)

C_5 = 0.5µF, 20V

$C_6 = C_7$ = 0.5µF (10% Match Required) (Note 7), 20V

C_8 = 0.01µF, 100V

C_9 = 0.01µF, 20V, ±20%

$R_1 = R_2 = R_3$ = 100kΩ (0.1% Match Required, 1% absolute value), Z_B = 0 for 600Ω Terminations (Note 7)

$R_{B1} = R_{B2} = R_{B3} = R_{B4}$ = 150Ω (0.1% Match Required, 1% absolute value)

R_S = 1kΩ, C_S = 0.1µF, 200V typically, depending on V_{RING} and line length.

Z_1 = 150V to 200V transient protection. PTC used as ring generator ballast.

NOTES:

6. C_1 is an optional capacitor used to improve V_{B+} supply rejection. This pin must be left open if unused.
7. To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C_6-R_1 and R_2 and C_7-Z_B-R_3, to match in impedance to within 0.3%. Thus, if C_6 and C_7 are 1µF each, a 20% match is adequate. It should be noted that the transmit output to C_6 sees a -22V step when the loop is closed. Too large a value for C_6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

   A 0.5µF and 100kΩ gives a time constant of 50ms. The uncommitted op amp output is internally clamped to stay within 5.5V and also has current limiting protection.
8. Secondary protection diode bridge recommended is a 2A, 200V type.
9. All grounds (AG, BG, and DG) must be applied before V_{B+} or V_{B-}. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first

HARRIS SEMICONDUCTOR

HC-5504B

SLIC
Subscriber Line Interface Circuit

January 1997

Features

- Pin for Pin Replacement for the HC-5504
- Capable of 5V or 12V (V_B+) Operation
- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (41mA)
- Internal Ring Relay Driver
- Allows Interfacing With Negative Superimposed Ringing Systems
- Low Power Consumption During Standby
- Switch Hook Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBXs
- Related Literature
  - AN549, The HC-5502S/4X Telephone Subscriber Line Interface Circuits (SLIC)
  - AN571, Using Ring Sync with HC-5502A and HC-5504 SLICs

Description

The Harris SLIC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Harris dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

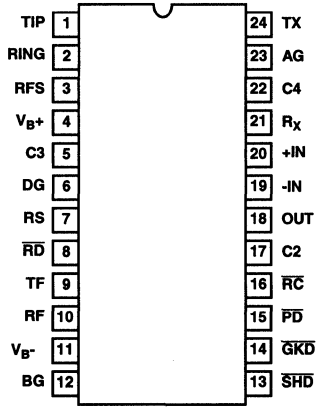
The Harris SLIC is ideally suited for the design of new digital PBX systems by eliminating bulky hybrid transformers.

Ordering Information

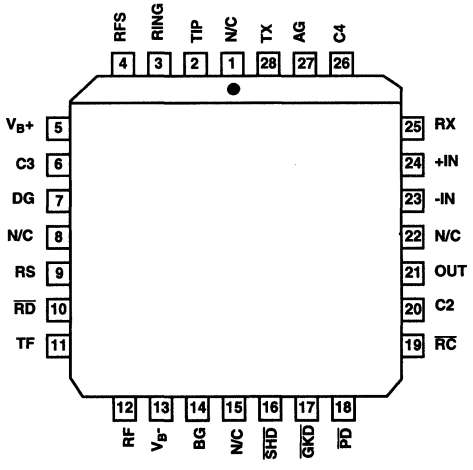
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC1-5504B-5	0 to 75	24 Ld CERDIP	F24.6
HC1-5504B-9	-40 to 85	24 Ld CERDIP	F24.6
HC3-5504B-5	0 to 75	24 Ld PDIP	E24.6
HC3-5504B-9	-40 to 85	24 Ld PDIP	E24.6
HC4P5504B-5	0 to 75	28 Ld PLCC	N28.45
HC4P5504B-9	-40 to 85	28 Ld PLCC	N28.45
HC9P5504B-5	0 to 75	24 Ld SOIC	M24.3
HC9P5504B-9	-40 to 85	24 Ld SOIC	M24.3

Pinouts

HC-5504B (PDIP, CERDIP, SOIC)
TOP VIEW



HC-5504B (PLCC)
TOP VIEW



4 WIRED COMMUNICATIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2886.3**

Absolute Maximum Ratings (Note 1)

Maximum Continuous Supply Voltages
- (V_B-) ..... -60V to 0.5V
- (V_B+) ..... -0.5V to 15V
- (V_B+ - V_B-) 75V

Relay Drive Voltage (V_{RD}) ..... -0.5V to 15V

Operating Conditions

Operating Temperature Range
- HC-5504B-5 ..... 0°C to 75°C
- HC-5504B-9 ..... -40°C to 85°C

Relay Driver Voltage (V_{RD}) ..... 5 to 12V
Positive Supply Voltage (V_B+) ..... 4.75 to 5.25 or 10.8 to 13.2V
Negative Supply Voltage (V_B-) ..... -36 to -58V
High Level Logic Input Voltage 2.4V
Low Level Logic Input Voltage 0.6V
Loop Resistance (R_L) ..... 200 to 1200Ω

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
CERDIP Package	52
PDIP Package	65
PLCC Package	65
SOIC Package	75

Maximum Junction Temperature (Hermetic Packages) ..... 175°C
Maximum Junction Temperature (Plastic Packages) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(PLCC and SOIC - Lead Tips Only)

Die Characteristics

Transistor Count 185
Diode Count 36
Die Dimensions ..... 137 x 102
Substrate Potential ..... Connected
Process ..... Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Unless Otherwise Specified, V_B- = -48V, V_B+ = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I_{LONG} = 0 (Note 3), V_B+ = 12V	-	170	235	mW
Off Hook Power Dissipation	R_L = 600Ω, I_{LONG} = 0 (Note 3), V_B+ = 12V	-	425	550	mW
Off Hook I_B+	R_L = 600Ω, I_{LONG} = 0 (Note 3), T_A = -40°C	-	-	6.0	mA
Off Hook I_B+	R_L = 600Ω, I_{LONG} = 0 (Note 3), T_A = 25°C	-	-	5.3	mA
Off Hook I_B-	R_L = 600Ω, I_{LONG} = 0 (Note 3)	-	35	41	mA
Off Hook Loop Current	R_L = 1200Ω, I_{LONG} = 0 (Note 3)	-	21	-	mA
Off Hook Loop Current	R_L = 1200Ω, V_B- = -42V, I_{LONG} = 0 (Note 3) T_A = 25°C	17.5	-	-	mA
Off Hook Loop Current	R_L = 200Ω, I_{LONG} = 0 (Note 3)	36	41	48	mA
Fault Currents					
TIP to Ground		-	14	-	mA
RING to Ground		-	55	-	mA
TIP to RING		-	41	-	mA
TIP and RING to Ground		-	55	-	mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	V_{RD} = 12V, $\overline{RC}$ = 1 = HIGH, T_A = 25°C	-	-	100	µA
Ring Trip Detection Period	R_L = 600Ω	-	2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD}$ = V_{OL}	10	-	-	mA
	$\overline{SHD}$ = V_{OH}	-	-	5	mA

Electrical Specifications Unless Otherwise Specified, V_B- = -48V, V_B+ = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Ground Key Detection Threshold	$\overline{GKD}$ = V_{OL}	20	-	-	mA
	$\overline{GKD}$ = V_{OH}	-	-	10	mA
Loop Current During Power Denial	R_L = 200Ω	-	±2	-	mA
Dial Pulse Distortion		0	-	5	ms
Receive Input Impedance	(Note 3)	-	110	-	kΩ
Transmit Output Impedance	(Note 3)	-	10	20	Ω
2-Wire Return Loss	Referenced to 600Ω + 2.16µF, (Note 3)				
SR_L LO		-	15.5	-	dB
ER_L		-	24	-	dB
SR_L HI		-	31	-	dB
Longitudinal Balance	$1V_{RMS}$ 200Hz - 3400Hz, (Note 3) IEEE Method				
2-Wire Off Hook	0°C ≤ T_A ≤ 75°C	58	65	-	dB
2-Wire On Hook		60	63	-	dB
4-Wire Off Hook		50	58	-	dB
Low Frequency Longitudinal Balance	R.E.A. Method, (Note 3), R_L = 600Ω	-	-	23	dBrnC
	0°C ≤ T_A ≤ 75°C	-	-	-67	dBm0p
Insertion Loss	at 1kHz, 0dBm Input Level, Referenced 600Ω				
2-Wire to 4-Wire, 4 Wire to 2-Wire		-	±0.05	±0.2	dB
Frequency Response	200Hz - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 3)	-	±0.02	±0.05	dB
Idle Channel Noise	(Note 3)				
2-Wire to 4-Wire, 4 Wire to 2-Wire		-	1	5	dBrnC
		-	-89	-85	dBm0p
Absolute Delay	(Note 3)				
2-Wire to 4-Wire, 4 Wire to 2-Wire		-	-	2	ms
Trans Hybrid Loss	Balance Network Set Up for 600Ω Termination at 1kHz	36	40	-	dB
Overload Level	V_B+ = +5V	1.5	-	-	V_{PEAK}
2-Wire to 4-Wire, 4 Wire to 2-Wire	V_B+ = 12V	1.75	-	-	V_{PEAK}
Level Linearity	At 1kHz Referenced to 0dBm Level, (Note 3)				
2-Wire to 4-Wire, 4 Wire to 2-Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
Power Supply Rejection Ratio	(Note 3)				
V_B+ to 2-Wire	30 - 60Hz, R_L = 600Ω	15	-	-	dB
V_B+ to Transmit		15	-	-	dB
V_B- to 2-Wire		15	-	-	dB
V_B- to Transmit		15	-	-	dB

Electrical Specifications Unless Otherwise Specified, V_{B^-} = -48V, V_{B^+} = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{B^+} to 2-Wire	200 - 16kHz, R_L = 600Ω	30	-	-	dB
V_{B^+} to Transmit		30	-	-	dB
V_{B^-} to 2-Wire		30	-	-	dB
V_{B^-} to Transmit		30	-	-	dB
Logic Input Current (RS, $\overline{RC}$, $\overline{PD}$)	0V ≤ V_{IN} ≤ 5V	-	-	±100	µA
Logic Inputs					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} 800µA, V_{B^+} = 12V, 5V	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} 80µA, V_{B^+} = 12V	2.7	5.0	5.5	V
	I_{LOAD} 40µA, V_{B^+} = 5V	2.7	-	5.0	V

Uncommitted Op Amp Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Input Bias Current		-	20	-	nA
Differential Input Resistance	(Note 3)	-	1	-	MΩ
Output Voltage Swing	R_L = 10K, V_{B^+} = 12V	-	±5	-	V_{PEAK}
	R_L = 10K, V_{B^+} = 5V	-	±3	-	V_{PEAK}
Output Resistance	A_{VCL} = 1 (Note 3)	-	10	-	Ω
Small Signal GBW	(Note 3)	-	1	-	MHz

NOTES:

3. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

4. I_{LONG} = Longitudinal Current

Pin Descriptions

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
2	1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring purposes.
3	2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
4	3	RFS	Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.
5	4	V_B+	Positive Voltage Source - Most positive supply. V_B+ is typically 12V or 5V.
6	5	C_3	Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V_B-. Typical value is 0.3µF, 30V.
7	6	DG (Note 5)	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
9	7	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock should be arranged such that a positive pulse transition occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring relay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to 5V.
10	8	$\overline{RD}$	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
11	9	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
12	10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
13	11	V_B-	Negative Voltage Source - Most negative supply. V_B- is typically -48V with an operational range of -42V to -58V. Frequently referred to as "battery".
14	12	BG (Note 5)	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
16	13	$\overline{SHD}$	Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
17	14	$\overline{GKD}$	Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.
18	15	$\overline{PD}$	Power Denial - A low active TTL - Compatible logic input. When enabled, the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.
19	16	$\overline{RC}$	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off- hook ($\overline{SHD}$ = 0).
20	17	C_2	Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15µF, 10V. This capacitor is not used if ground key function is not required and (Pin 17) may be left open or connected to digital ground.
21	18	OUT	The analog output of the spare operational amplifier. The output voltage swing is typically ±5V.

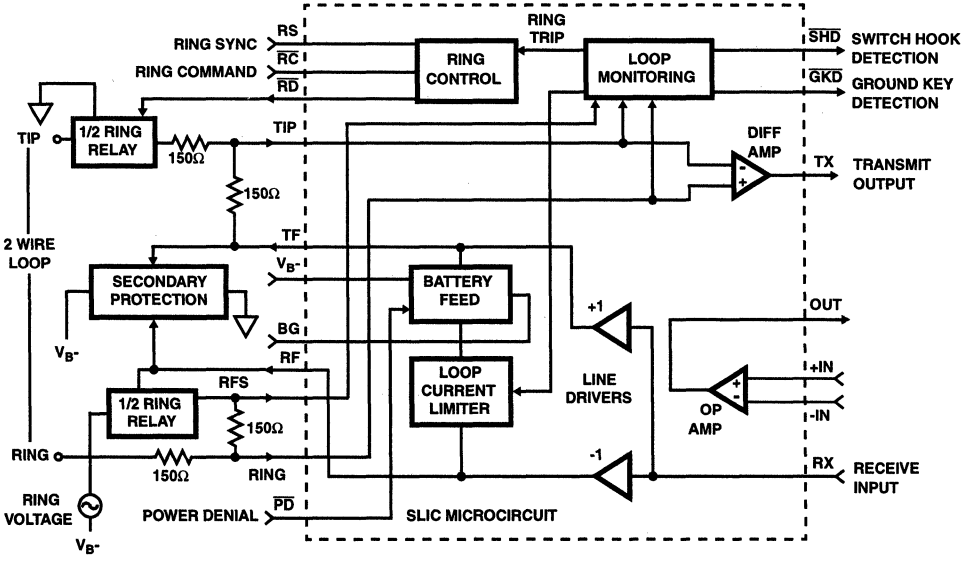
Pin Descriptions (Continued)

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
23	19	-IN	The inverting analog input of the spare operational amplifier.
24	20	+IN	The non-inverting analog input of the spare operational amplifier.
25	21	RX	Receive Input, 4-Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed terminals, which in turn drive tip and ring through 300Ω of feed resistance on each side of the line.
26	22	C_4	Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near by power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5µF, to 1.0µF, 20V. This capacitor should be nonpolarized.
27	23	AG (Note 5)	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
28	24	TX	Transmit Output, 4-Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
1, 8, 15, 22		NC	No internal connection.

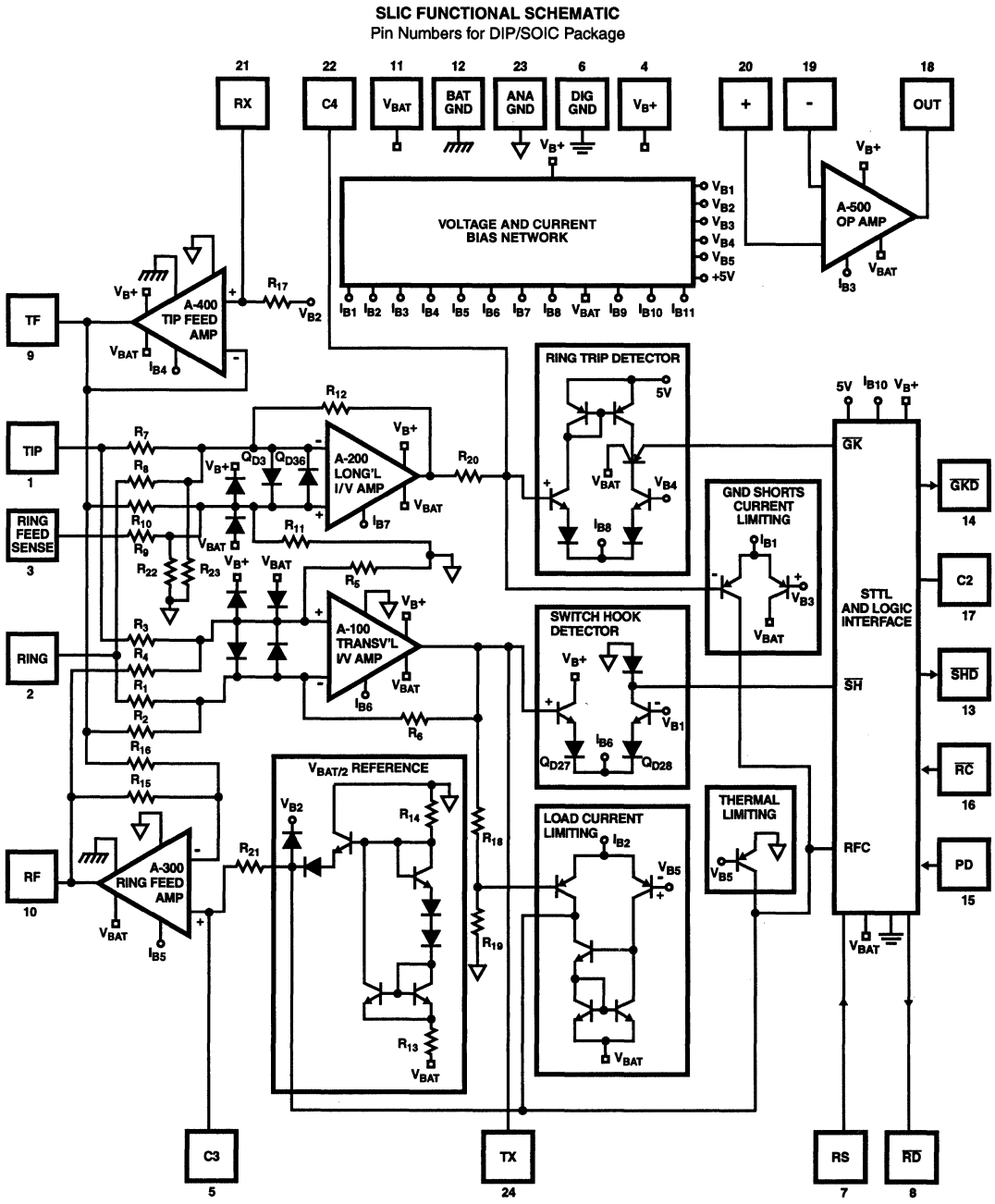
NOTE:

5. All grounds (AG, BG, and DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Functional Diagram

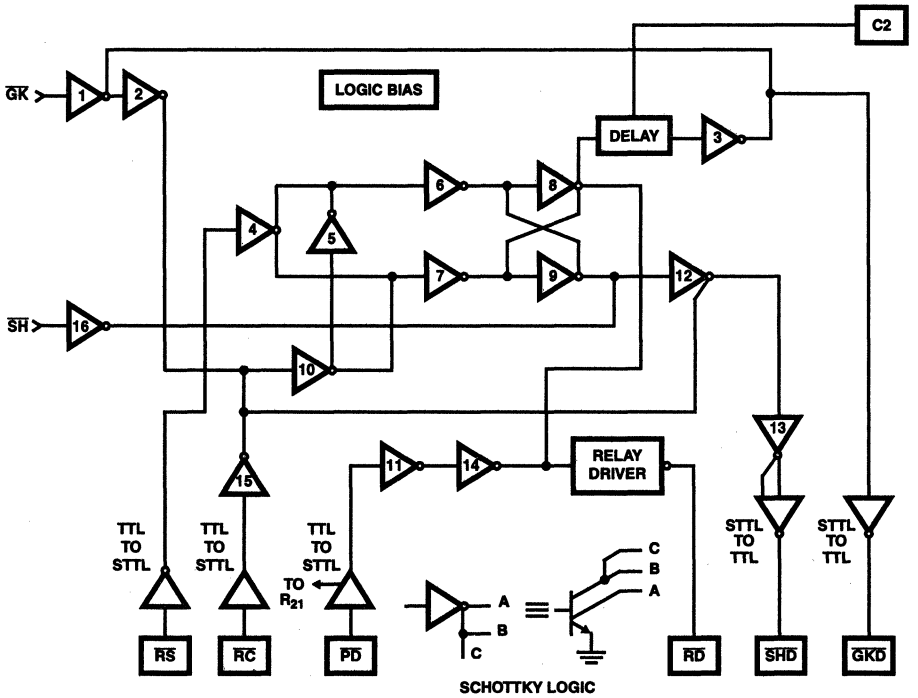


Schematic Diagram



Schematic Diagram (Continued)

LOGIC GATE SCHEMATIC



Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or $30mA_{RMS}$, $15mA_{RMS}$ per leg, without any performance degradation.

TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/	±1000 (Plastic)	V_{PEAK}
	1000µs Fall	±500 (Ceramic)	V_{PEAK}
Metallic Surge	10µs Rise/	±1000 (Plastic)	V_{PEAK}
	1000µs Fall	±500 (Ceramic)	V_{PEAK}
T/GND	10µs Rise/	±1000 (Plastic)	V_{PEAK}
R/GND	1000µs Fall	±500 (Ceramic)	V_{PEAK}
50/60Hz Current			
T/GND	11 Cycles	700 (Plastic)	V_{RMS}
R/GND	Limited to $10A_{RMS}$	350 (Ceramic)	V_{RMS}

Applications Diagram

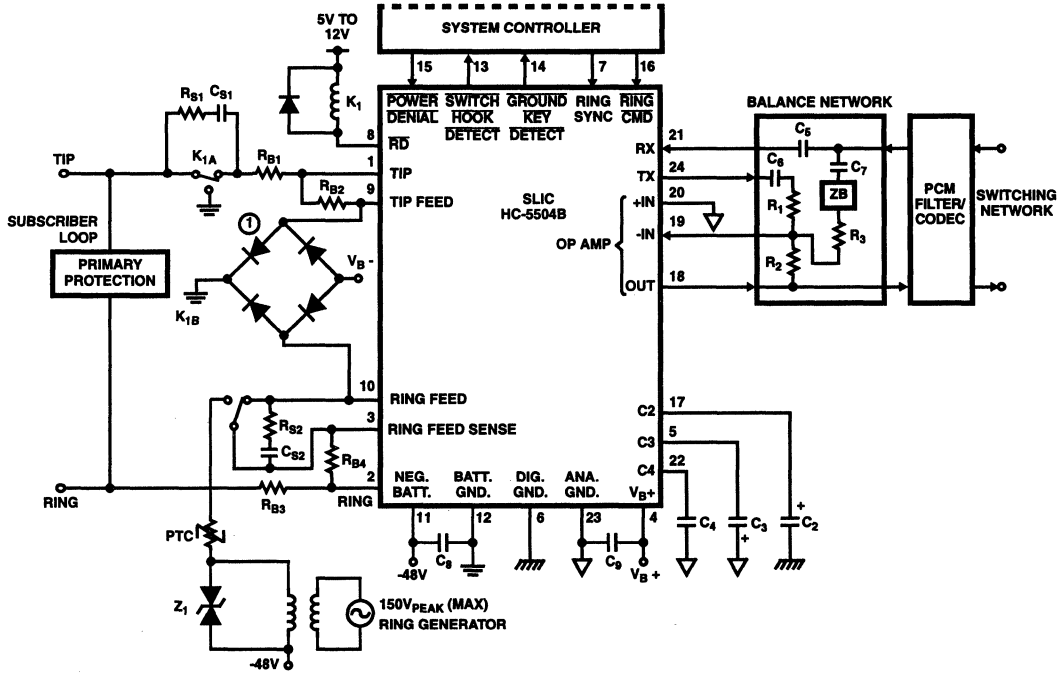


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values

C_2 = 0.15µF, 10V

C_3 = 0.3µF, 30V

C_4 = 0.5µF to 1.0µF, 10%, 20V (Should be nonpolarized)

C_5 = 0.5µF, 20V

$C_6 = C_7$ = 0.5µF (10% Match Required) (Note 7)

C_8 = 0.01µF, 100V

C_9 = 0.01µF, 20V, ±20%

$R_1 = R_2 = R_3$ = 100k (0.1% Match Required, 1% absolute value) ZB = 0 for 600Ω Terminations (Note 7).

$R_{B1} = R_{B2} = R_{B3} = R_{B4}$ = 150Ω (0.1% Match Required, 1% absolute value).

$R_{S1} = R_{S2}$ =1kΩ, typically.

$C_{S1} = C_{S2}$ = 0.1µF, 200V typically, depending on V_{RING} and line length.

Z_1 = 150V to 200V transient protection.

PTC used as ring generator ballast.

NOTES:

6. Secondary protection diode bridge recommended is a 2A, 200V type.
7. To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C_6-R_1 and R_2 and C_7-ZB-R_3, to match in impedance to within 0.3%. Thus, if C_6 and C_7 are 1µF each, a 20% match is adequate. It should be noted that the transmit output to C_6 sees a -22V step when the loop is closed. Too large a value for C_6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

   A 0.5µF and 100kΩ gives a time constant of 50ms. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.
8. All grounds (AG, BG, and DG) must be applied before V_{B+} or V_{B-}. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
9. Application shows Ring Injected Ringing, Balanced or Tip injected configuration may be used.
10. Pin numbers given for DIP/SOIC package.

HARRIS SEMICONDUCTOR

HC-5502B

SLIC
Subscriber Line Interface Circuit

January 1997

Features

- Pin For Pin Replacement For The HC-5502A
- Capable of 12V or 5V (V_B+) Operation
- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (30mA)
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- Selective Denial of Power to Subscriber Loops

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- Direct Inward Dial (DID) Trunks
- Voice Messaging PBXs
- Related Literature
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The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

The Harris SLIC is ideally suited for the design of new digital PBX systems, by eliminating bulky hybrid transformers.

Ordering Information

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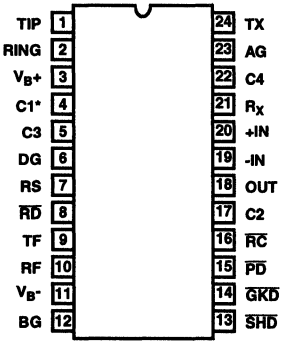
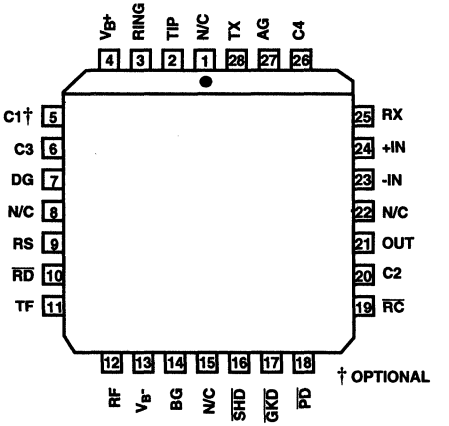
HC1-5502B-9	-40 to 85	24 Ld CERDIP	F24.6
HC3-5502B-5	0 to 75	24 Ld PDIP	E24.6
HC4P5502B-5	0 to 75	28 Ld PLCC	N28.45
HC9P5502B-5	0 to 75	24 Ld SOIC	M24.3
HC9P5502B-9	-40 to 85	24 Ld SOIC	M24.3

Pinouts

HC-5502B
(PDIP, CERDIP, SOIC)
TOP VIEW



HC-5502B
(PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2884.3**

Absolute Maximum Ratings (Note 1)

Supply Voltage
- (V_B-) ..... -60 to 0.5V
- (V_B+) ..... -0.5 to 15V
- (V_B+ - V_B-) 75V

Relay Drive Voltage (V_{RD}) ..... -0.5 to 15V

Operating Conditions

Relay Driver Voltage (V_{RD}) ..... 5V to 12V
Positive Supply Voltage (V_B+) ... 4.75V to 5.25V or 10.8V to 13.2V
Negative Supply Voltage (V_B-) ..... -42V to -58V
High Level Logic Input Voltage 2.4V
Low Level Logic Input Voltage 0.6V
Loop Resistance (R_L) ..... 200 to 1200Ω
Operating Temperature Range
- HC-5502B-5 ..... 0°C to 75°C
- HC-5502B-9 ..... -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
CERDIP Package	52
PDIP Package	65
SOIC Package	75
PLCC Package	65

Maximum Junction Temperature (Hermetic Package) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(PLCC and SOIC - Lead Tips Only)

Die Characteristics

Transistor Count 183
Diode Count 33
Die Dimensions ..... 137 mils x 102 mils
Substrate Potential ..... V_B-
Process ..... Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Unless Otherwise Specified, V_B- = -48V, V_B+ = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I_{LONG} = 0, V_B+ = 12V (Note 3)	-	135	235	mW
Off Hook Power Dissipation	R_L = 600Ω, I_{LONG} = 0, V_B+ = 12V (Note 3)	-	450	690	mW
Off Hook I_B+	R_L = 600Ω, I_{LONG} = 0, T_A = -40°C (Note 3)	-	-	6.0	mA
Off Hook I_B+	R_L = 600Ω, I_{LONG} = 0, T_A = 25°C (Note 3)	-	-	5.3	mA
Off Hook I_B-	R_L = 600Ω, I_{LONG} = 0 (Note 3)	-	-	39	mA
Off Hook Loop Current	R_L = 1200Ω, I_{LONG} = 0 (Note 3)	-	21	-	mA
Off Hook Loop Current	R_L = 1200Ω, V_B- = -42V, I_{LONG} = 0, T_A = 25°C (Note 3)	17.5	-	-	mA
Off Hook Loop Current	R_L = 200Ω, I_{LONG} = 0 (Note 3)	25.5	30	34.5	mA
Fault Currents					
TIP to Ground		-	14	-	mA
RING to Ground		-	47	-	mA
TIP to RING		-	30	-	mA
TIP and RING to Ground		-	47	-	mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	V_{RD} = 12V, $\overline{RC}$ = 1 = HIGH, T_A = 25°C	-	-	100	µA
Ring Trip Detection Period	R_L = 600Ω, T_A = 25°C	-	2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD}$ = V_{OL}	10	-	-	mA
	$\overline{SHD}$ = V_{OH}	-	-	5	mA

Electrical Specifications Unless Otherwise Specified, V_{B}- = -48V, V_{B}+ = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Ground Key Detection Threshold	$\overline{GKD}$ = V_{OL}	20	-	-	mA
	$\overline{GKD}$ = V_{OH}	-	-	10	mA
Loop Current During Power Denial	R_L = 200Ω	-	±2	-	mA
Dial Pulse Distortion		0	-	5	ms
Receive Input Impedance	(Note 4)	-	110	-	kΩ
Transmit Output Impedance	(Note 4)	-	10	20	Ω
2-Wire Return Loss SRL LO	Referenced to 600Ω +2.16µF (Note 4)	-	15.5	-	dB
ERL		-	24	-	dB
SRL HI		-	31	-	dB
Longitudinal Balance 2-Wire Off Hook	$1V_{RMS}$ 200Hz - 3400Hz, (Note 4) IEEE Method 0°C ≤ T_A ≤ 75°C	58	65	-	dB
2-Wire On Hook		60	63	-	dB
4-Wire Off Hook		50	58	-	dB
Low Frequency Longitudinal Balance	R.E.A. Method, (Note 4) R_L = 600Ω, 0°C ≤ T_A ≤ 75°C	-	-	23	dBrnC
		-	-	-67	dBm0p
Insertion Loss 2-Wire to 4-Wire, 4-Wire to 2-Wire	At 1kHz, 0dBm Input Level, Referenced 600Ω	-	±0.05	±0.2	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 4)	-	±0.02	±0.05	dB
Idle Channel Noise 2-Wire to 4-Wire, 4-Wire to 2-Wire	(Note 4)	-	1	5	dBrnC
		-	-89	-85	dBm0p
Absolute Delay 2-Wire to 4-Wire, 4-Wire to 2-Wire	(Note 4)	-	-	2	µs
Trans Hybrid Loss	Balance Network Set Up for 600Ω Termination at 1kHz	36	40	-	dB
Overload Level 2-Wire to 4-Wire, 4-Wire to 2-Wire	V_{B}+ = 5V	1.5			V_{PEAK}
	V_{B}+ = 12V	1.75	-	-	V_{PEAK}
Level Linearity 2-Wire to 4-Wire, 4-Wire to 2-Wire	At 1kHz, (Note 4) Referenced to 0dBm Level +3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB

Electrical Specifications Unless Otherwise Specified, V_{B^-} = -48V, V_{B^+} = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio V_{B^+} to 2-Wire	30 - 60Hz, R_L = 600Ω, (Note 4)	15	-	-	dB
V_{B^+} to Transmit		15	-	-	dB
V_{B^-} to 2-Wire		15	-	-	dB
V_{B^-} to Transmit		15	-	-	dB
V_{B^+} to 2-Wire	200 - 16kHz, R_L = 600Ω	30	-	-	dB
V_{B^+} to Transmit		30	-	-	dB
V_{B^-} to 2-Wire		30	-	-	dB
V_{B^-} to Transmit		30	-	-	dB
Logic Input Current (RS, $\overline{RC}$, $\overline{PD}$)	0V ≤ V_{IN} ≤ 5V	-	-	±100	µA
Logic Inputs Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Logic Outputs Logic '0' V_{OL}	I_{LOAD} 800µA, V_{B^+} = 12V, 5V	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} 80µA, V_{B^+} = 12V	2.7	5.0	5.5	V
	I_{LOAD} 40µA, V_{B^+} = 5V	2.7	-	5.0	V

Uncommitted Op Amp Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Input Bias Current		-	20	-	nA
Differential Input Resistance	(Note 4)	-	1	-	MΩ
Output Voltage Swing	R_L = 10kΩ, V_{B^+} = 12V	-	±5	-	V_{PEAK}
	R_L = 10kΩ, V_{B^+} = 5V	-	±3	-	V_{PEAK}
Output Resistance	A_{VCL} = 1, (Note 4)	-	10	-	Ω
Small Signal GBW	(Note 4)	-	1	-	MHz

NOTES:

3. I_{LONG} = Longitudinal Current
4. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterised upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Pin Descriptions

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
2	1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring process.
3	2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
4	3	V_B+	Positive Voltage Source - Most positive supply. V_B+ is typically 12V or 5V.
5	4	C_1	Capacitor #1 - Optional Capacitor used to improve power supply rejection. This pin should be left open if unused.
6	5	C_3	Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V_B- supply. Typical value is 0.3µF, 30V.
7	6	DG (Note 5)	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC.
9	7	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock should be arranged such that a positive transition occurs on the negative going zero crossing of the ring voltage source, ensuring that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If synchronization is not required, tie to 5V.
10	8	$\overline{RD}$	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
11	9	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
12	10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signal to the telephone set, and sink longitudinal current.
13	11	V_B-	Negative Voltage Source - Most negative supply. V_B- is typically -48V with an operational range of -42V to -58V. Frequently referred to as "battery".
14	12	BG (Note 1)	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
16	13	$\overline{SHD}$	Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
17	14	$\overline{GKD}$	Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.
18	15	$\overline{PD}$	Power Denial - A low active TTL - Compatible logic input. When enabled the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.
19	16	$\overline{RC}$	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next rising edge of the ring sync ($\overline{RS}$) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off- hook ($\overline{SHD}$ = 0).
20	17	C_2	Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15µF, 10V. This capacitor is not used if ground key function is not required.
21	18	OUT	The analog output of the spare operational amplifier.
23	19	-IN	The inverting analog input of the spare operational amplifier.

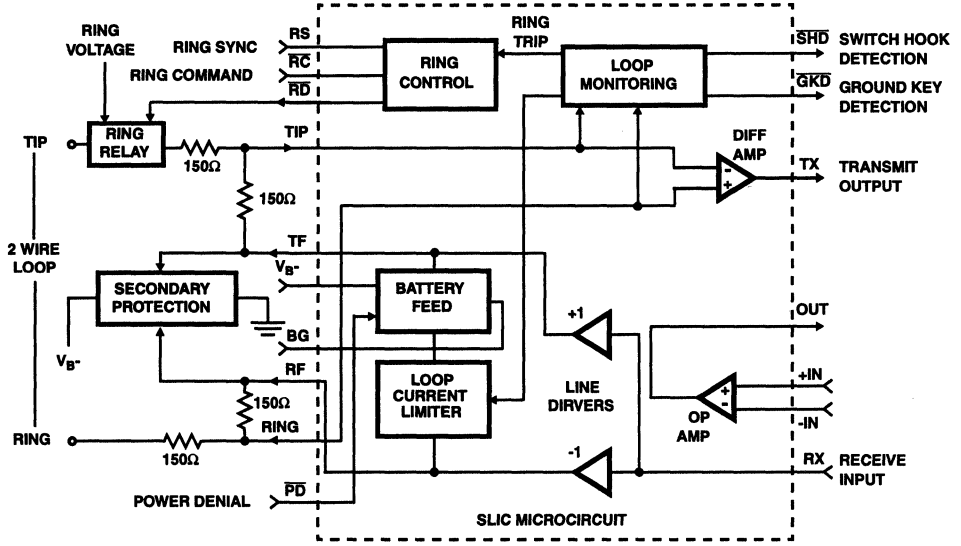
Pin Descriptions (Continued)

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
24	20	+IN	The non-inverting analog input of the spare operational amplifier.
25	21	RX	Receive Input, 4-Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed amplifiers, which in turn drive tip and ring through 300Ω of feed resistance on each side of the line.
26	22	C_4	Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from nearby power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5µF to 1.0µF, 20V. This capacitor should be nonpolarized.
27	23	AG (Note 5)	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
28	24	TX	Transmit Output, 4-Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
1, 8, 5, 22		NC	No internal connection.

NOTE:

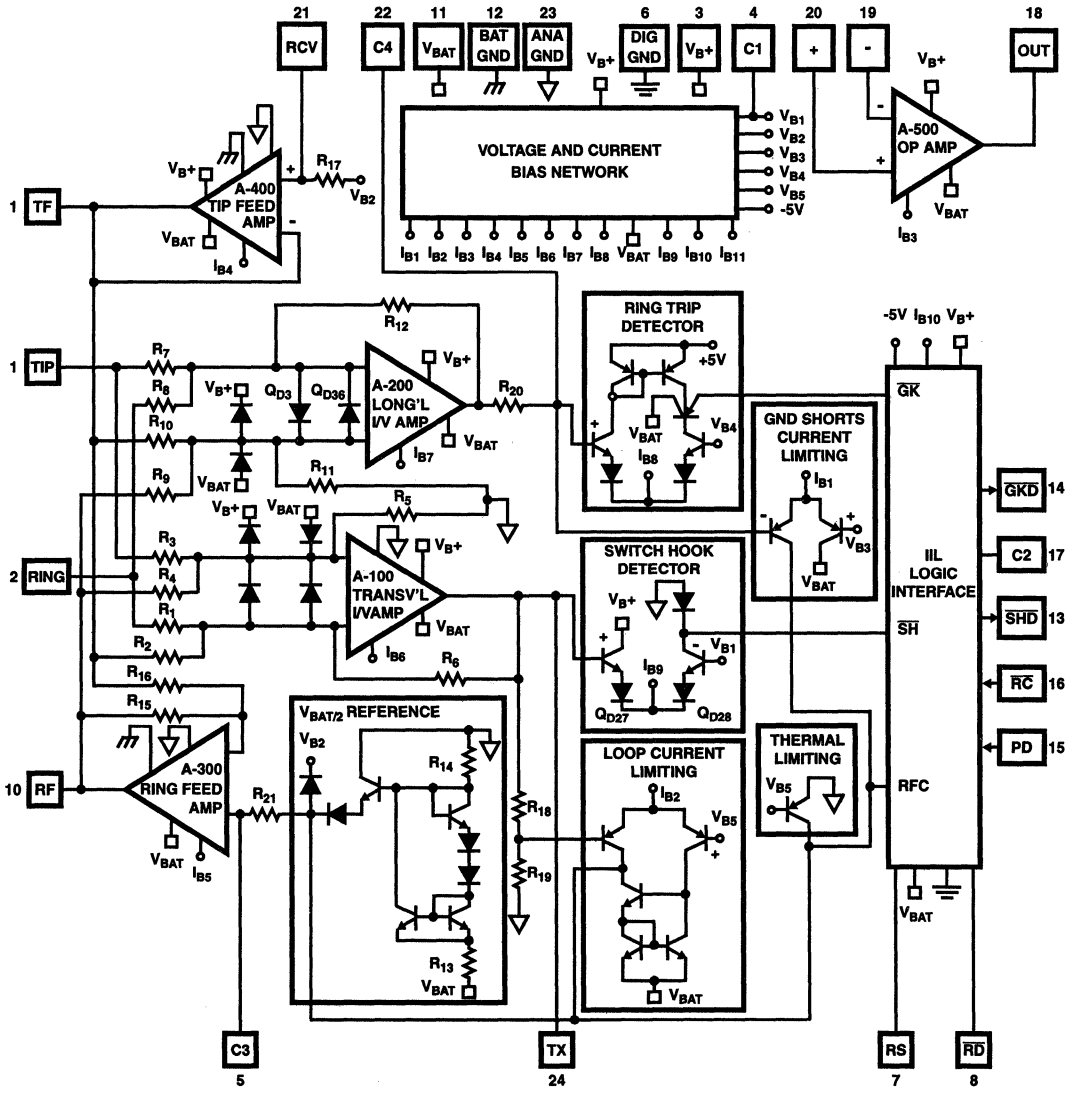
5. All grounds (AG, BG, and DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Functional Diagram



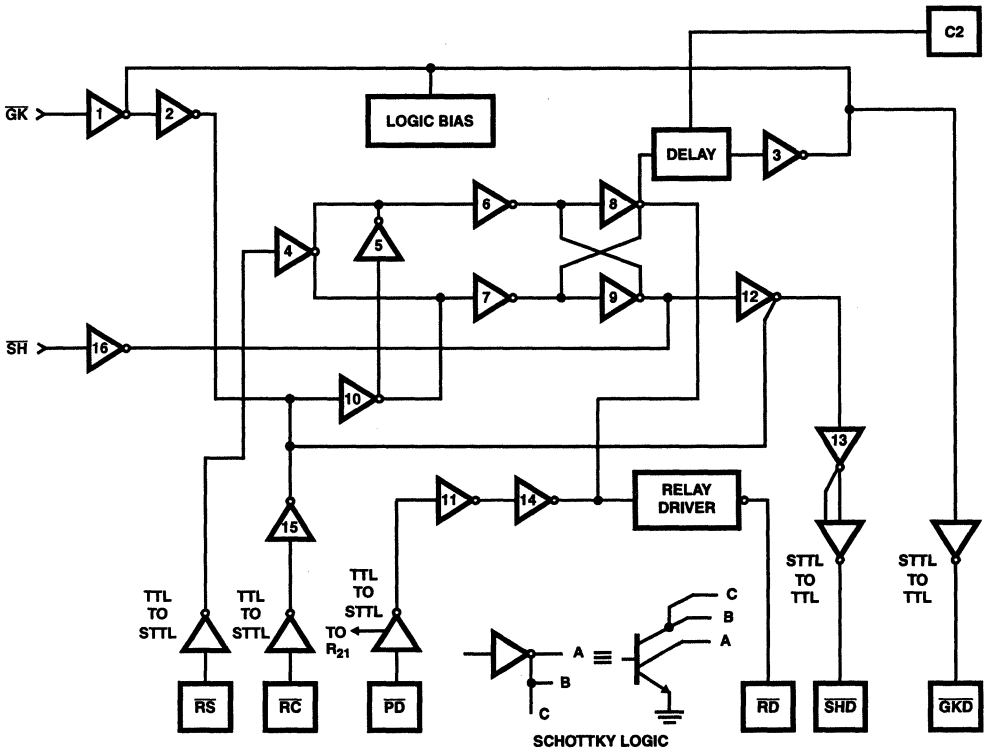
Schematic Diagram

HC-5502B
Pin Numbers for DIP/SOIC Package



Logic Diagram

HC-5502B LOGIC GATE SCHEMATIC



Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or 30mARMS, 15mARMS per leg, without any performance degradation

TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/	±1000 (Plastic)	V_{PEAK}
	1000µs Fall	±500 (Ceramic)	V_{PEAK}
Metallic Surge	10µs Rise/	±1000 (Plastic)	V_{PEAK}
	1000µs Fall	±500 (Ceramic)	V_{PEAK}
T/GND	10µs Rise/	±1000 (Plastic)	V_{PEAK}
R/GND	1000µs Fall	±500 (Ceramic)	V_{PEAK}
50/60Hz Current			
T/GND	11 Cycles	700 (Plastic)	V_{RMS}
R/GND	Limited to $10A_{RMS}$	350 (Ceramic)	V_{RMS}

Applications Diagram

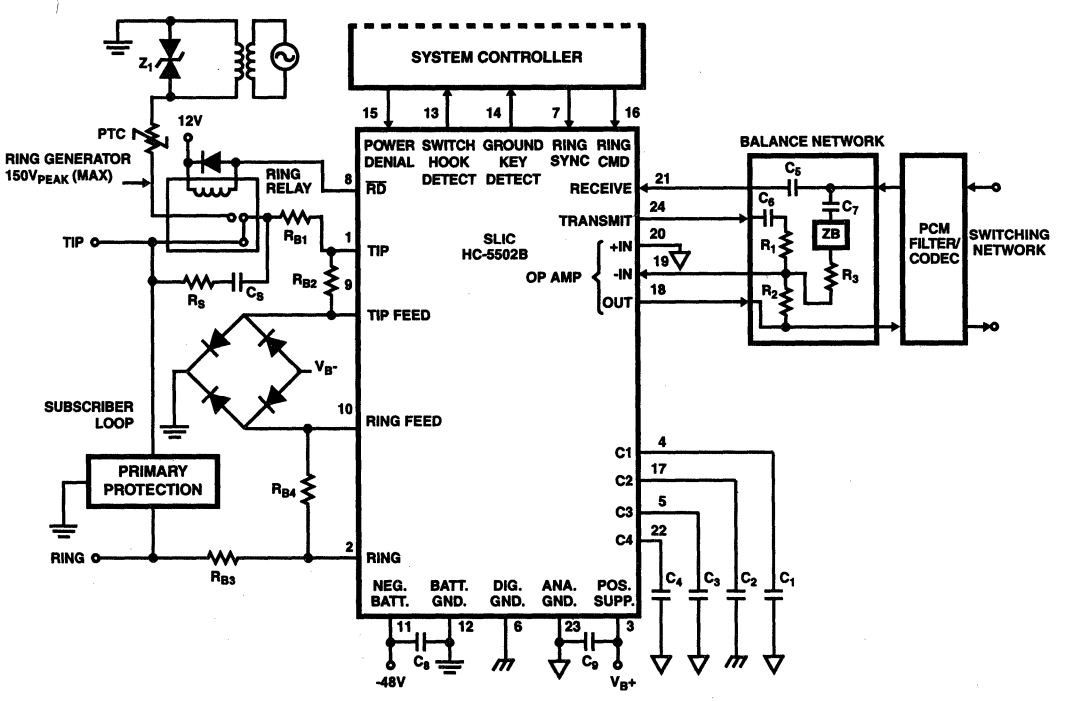


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values

C_1 = 0.5µF (Note 6)

C_2 = 0.15µF, 10V

C_3 = 0.3µF, 30V

C_4 = 0.5µF to 1.0µF, 10%, 20V (Should be nonpolarized)

C_5 = 0.5µF, 20V

$C_6 = C_7$ = 0.5µF (10% Match Required) (Note 7), 20V

C_8 = 0.01µF, 100V

C_9 = 0.01µF, 20V, ±20%

$R_1 = R_2 = R_3$ = 100kΩ (0.1% Match Required, 1% absolute value), ZB = 0 for 600Ω Terminations (Note 7)

$R_{B1} = R_{B2} = R_{B3} = R_{B4}$ = 150Ω (0.1% Match Required, 1% absolute value)

R_S = 1kΩ, C_S = 0.1µF, 200V typically, depending on V_{RING} and line length.

Z_1 = 150V to 200V transient protection. PTC used as ring generator ballast.

NOTES:

6. C_1 is an optional capacitor used to improve V_{B+} supply rejection. This pin must be left open if unused.
7. To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C_6-R_1 and R_2 and C_7-ZB-R_3, to match in impedance to within 0.3%. Thus, if C_6 and C_7 are 1µF each, a 20% match is adequate. It should be noted that the transmit output to C_6 sees a -22V step when the loop is closed. Too large a value for C_6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

   A 0.5µF and 100kΩ gives a time constant of 50ms. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.
8. Secondary protection diode bridge recommended is a 2A, 200V type.
9. All grounds (AG, BG, and DG) must be applied before V_{B+} or V_{B-}. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first
10. Pin numbers given for DIP/SOIC package.

HARRIS SEMICONDUCTOR

CD22354A, CD22357A

CMOS Single-Chip, Full-Feature PCM CODEC

January 1997

Features

- Meets or Exceeds All AT&T D3/D4 Specifications and CCITT Recommendations
- Complete CODEC and Filtering Systems: No External Components for Sample-and-Hold and Auto-Zero Functions. Receive Output Filter with (SIN X)/X Correction and Additional 8kHz Suppression
- Variable Data Clocks - From 64kHz 2.1MHz
- Receiver Includes Power-Up Click Filter
- TTL or CMOS-Compatible Logic
- ESD Protection on All Inputs and Outputs

Applications

- PABX
- Central Office Switching Systems
- Accurate A/D and D/A Conversions
- Digital Telephones
- Cellular Telephone Switching Systems
- Voice Scramblers - Descramblers
- T1 Conference Bridges
- Voice Storage and Retrieval Systems
- Sound Based Security Systems
- Computerized Voice Analysis
- Mobile Radio Telephone Systems
- Microwave Telephone Networks
- Fiber-Optic Telephone Networks

Description

The CD22354A and CD22357A are monolithic silicon-gate, double-poly CMOS integrated circuits containing the band-limiting filters and the companding A/D and D/A conversion circuits that conform to the AT&T D3/D4 specifications and CCITT recommendations. The CD22354A provides the AT&T μ-law and the CD22357A provides the CCITT A-law companding characteristic.

The primary applications for the CD22354A and CD22357A are in telephone systems. These circuits perform the analog and digital conversions between the subscriber loop and the PCM highway in a digital switching system. The functional block diagram is shown below.

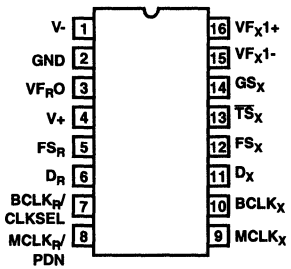
With flexible features, including synchronous and asynchronous operations and variable data rates, the CD22354A and CD22357A are ideally suited for PABX, central office switching system, digital telephones as well as other applications that require accurate A/D and D/A conversions and minimal conversion time.

Ordering Information

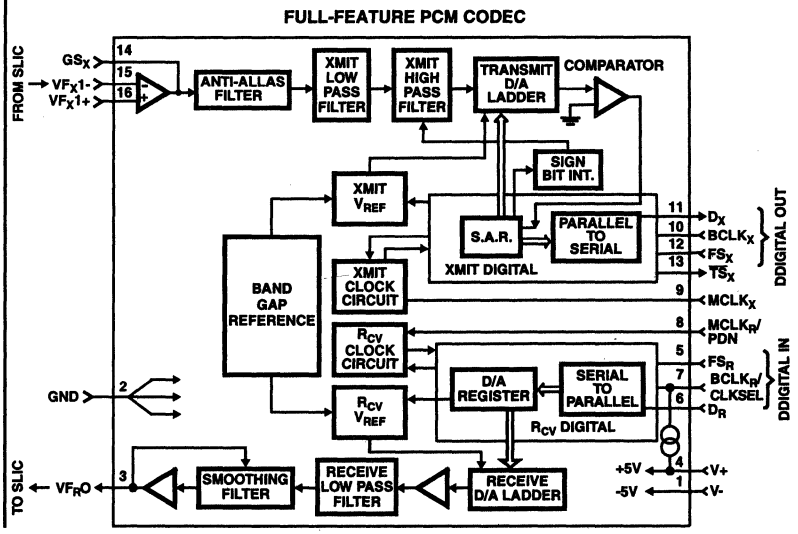
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22354AE	-40 to 80	16 Ld PDIP	E16.3
CD22357AE	-40 to 80	16 Ld PDIP	E16.3

Pinout

CD22354A, CD22357A
(PDIP)
TOP VIEW



Functional Block Diagram



4 WIRED COMMUNICATIONS

File Number 1682.3

Absolute Maximum Ratings

DC Supply-Voltage, (V+) ..... -0.5 to 7V
DC Supply-Voltage, (V-) ..... 0.5 to -7V
DC Input Diode Current,
I_{IK} (V_I < V- -0.5V or V_I > V+ 0.5V) ..... ±20mA
DC Output Diode Current,
I_{OK} (V_I < V- -0.5V or V_O > V+ 0.5V) ..... ±20mA
DC Drain Current, Per Output
I_O (V- -0.5V < V_O < V+ 0.5V) ..... ±25mA
DC Supply/Ground Current ..... ±50mA
Power Dissipation Per Package (P_D):
For T_A = -40°C to 60°C 500mW
For T_A = 60°C to 85°C ..... Derate Linearly at 8mW/°C to 300mW

Thermal Information

Maximum Junction Temperature ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range (T_{STG}) ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C

Operating Conditions

Operating-Temperature Range (T_A) ..... -40°C to 80°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
STATIC SPECIFICATIONS						
Positive Power Supply	V+		4.75	5	5.25	V
Negative Power Supply	V-		-4.75	-5	-5.25	V
Power Dissipation (Operating)	P_{OPR}	V+ = 5V	-	75	90	mW
Power Dissipation (Standby)	P_{STBY}	V- = -5V	-	9	15	mW

Electrical Specifications At T_A = 0°C to 70°C; V+ = 5V ±5%, V- = -5V ±5%

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
STATIC SPECIFICATIONS						
Analog Input Resistance	R_{INA}		10	-	-	MΩ
Input Capacitance	C_{IN}	All Logic and Analog Inputs	-	5	-	pF
Input Leakage Current, Digital	I_I	V_I = 0V or V+	-10	-	10	µA
Low Level Input Voltage	V_{IL}	I_{IL} = ±10µA (Max)	-	-	0.8	V
High Level Input Voltage	V_{IH}	I_{IH} = ±10µA (Max)	2	-	-	V
Low Level Output Voltage	V_{OL}	I_{OL} = 3.2mA	-	-	0.4	V
High Level Output Voltage	V_{OH}	I_{OH} = 1.0mA	2.4	-	-	V
Open State Output Current	I_{OZ}	GND < D_X < V+	-10	-	10	µA
Input Leakage Current, Analog	I_I	-2.5V ≤ VF_X < 2.5V	-200	-	200	nA

Electrical Specifications

$V+ = 5V \pm 5\%$, $V- = -5V \pm 5\%$, $BCLK_R = BCLK_X = MCLK_X = 1.544MHz$, $V_{IN} = 0dBm0$, $T_A = 0^oC$ to 70^oC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMIT AND RECEIVE FILTER TRANSFER CHARACTERISTICS						
Transmit Gain (Relative to Gain at 1020Hz) Input Amplifier Set to Unity Gain	G_{RX}	f = 16Hz	-	-	-40	dB
		f = 50Hz	-	-	-30	dB
		f = 60Hz	-	-	-26	dB
		f = 200Hz	-1.8	-	-0.1	dB
		f = 300Hz to 3000Hz	-0.15	-	0.15	dB
		f = 3300Hz	-0.35	-	0.05	dB
		f = 3400Hz	-0.7	-	0	dB
		f = 4000Hz	-	-	-14	dB
		f ≥ 4600Hz, Measure 0 - 4kHz Response	-	-	-32	dB
Receive Gain (Relative to Gain at 1020Hz) (Includes (SIN X)/X Compensation)	G_{RR}	f = 0Hz to 3000Hz	-0.15	-	0.15	dB
		f = 3300Hz	-0.35	-	0.05	dB
		f = 3400Hz	-0.9	-	0	dB
		f = 4000Hz	-	-	-14	dB

AC Specifications

Unless otherwise specified, the following conditions apply:

$V+ = 5V \pm 5\%$, $V- = -5V \pm 5\%$
GND_A, $GND_D = 0V$, $F_{FX} = 1020Hz$ at 0dBm0
Transmit input amplifier operating in a unity gain configuration
Temperature . . . . . 0^oC to 70^oC
Receive output is measured single-ended. All output levels are (SIN X)/X corrected.

Definition

AMPLITUDE RESPONSE
Absolute Levels Definition:
$V_{REF} = -2.5V$
Nominal 0dBm0 level . . . . . 4dBm into 600Ω
$1.2276V_{RMS}$
Maximum Overload Level:
Voltage reference (V_{REF}) of -2.5V . . . . . 2.5V μ-Law
2.49V A-Law

AC Specifications Encoding Format at D_X Output

	CD22354A μ-LAW								CD22357A A-LAW (INCLUDES EVEN BIT INVERSION)							
V_{IN} (at GS_X) = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} (at GS_X) = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} (at GS_X) = -Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC DISTORTION						
Signal to Total Distortion Xmit or R_{CV}	STD_X, STD_R	Level = +3dBm0	33	-	-	dBc
		Level = 0 to -30dBm0	36	-	-	dBc
		Level = -40dBm0	30	-	-	dBc
		Level = -55dBm0, XMT	14	-	-	dBc
		Level = -55dBm0, R_{CV}	15	-	-	dBc
Single Frequency Distortion Xmit or R_{CV}	SFD_X, SFD_R		-	-	-46	dBc
Intermodulation (End-to-End Measurement) 2-Tone	IMD	V_{FX} = -4dBm0 to -21dBm0 f1, f2 from 300 to 3400Hz	-	-	-41	dB
Transmit Delay, Absolute	t_{DAX}	f = 1600Hz	-	280	315	µs
Transmit Envelope Delay Relative to t_{DAX}	t_{DEX}	f = 500-600Hz	-	170	220	µs
		f = 600-1000Hz	-	70	145	µs
		f = 1000-2600Hz	-	40	75	µs
		f = 2600-2800Hz	-	90	105	µs
Receive Delay, Absolute	t_{DAR}	f = 1600Hz	-	180	200	µs
Receive Envelope Delay Relative to t_{DAR}	t_{DER}	f = 500-600Hz	-40	-25	-	µs
		f = 600-1000Hz	-40	-25	-	µs
		f = 1000-2600Hz	-	60	90	µs
		f = 2600-2800Hz	-	110	125	µs

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC GAIN TRACKING						
Transmit Gain Tracking Error	GTX	+3 to -40dBm0	-	-	±0.2	dB
		-40 to -50dBm0	-	-	±0.4	dB
		-50 to -55dBm0	-	-	±1.2	dB
Receive Gain Tracking Error	GTR	+3 to -40dBm0	-	-	±0.2	dB
		-40 to -50dBm0	-	-	±0.4	dB
		-50 to -55dBm0	-	-	±1.2	dB
Transmit Input Amplifier Gain, Open Loop	A_{OL}	$R_L \geq 1M\Omega$ at GS_X	68	-	-	dB

Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Transmit Input Amplifier Gain, Unity	A_{CL}	Unity Gain Configuration Inverting or Non-Inverting $R_L \geq 10K$, $C_L \leq 50pF$	-0.01	-	0.01	dB
Transmit Gain, Absolute	G_{XA}	$R_L \geq 10K$, $C_L \leq 50pF$	-0.15	-	0.15	dB
Receive Gain, Absolute	G_{RA}	$R_L \geq 600\Omega$, $C_L \leq 500pF$	-0.15	-	0.15	dB

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC NOISE						
Transmit Noise	N_X	VF_XI- = GND	-	12	15	dBrnc0
		VF_XI+ = GND	-	-74	-67	dBrn0p
Receive Noise	N_R	PCM Code Equivalent to 0V	-	7	11	dBrnc0
			-	-83	-79	dBrn0p
V+ Power Supply Rejection Transmit	PSRR	VF_XI+ = 0V V+ = 5V + ($100mV_{RMS}$) f = 0kHz to 50kHz	40	-	-	dBc
V- Power Supply Rejection Transmit	PSRR	VF_XI- = 0V V- = -5V + ($100mV_{RMS}$) f = 0kHz to 50kHz	40	-	-	dBc
V+ Power Supply Rejection Receive	PSRR	PCM Code = All 1 Code V+ = 5V + ($100mV_{RMS}$) f = 0kHz to 4kHz	40	-	-	dBc
		f = 4kHz to 25kHz	37	-	-	dB
		f = 25kHz to 50kHz	36	-	-	dB
V- Power Supply Rejection Receive	PSRR	PCM Code = All 1 Code V- = -5V + ($100mV_{RMS}$) f = 0kHz to 4kHz	40	-	-	dBc
		f = 4kHz to 25kHz	40	-	-	dB
		f = 25kHz to 50kHz	36	-	-	dB
Cross Talk Transmit to Receive	CT_{XR}	VF_XI- = 0dBm0 at 1020Hz	-	-80	-70	dB
Cross Talk Receive to Transmit	CT_{RX}	D_R = 0dBm0 at 1020Hz, VF_XI- = 0V	-	-76	-70	dB

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC TIMING						
Frequency of Master Clocks	$1/t_{PM}$	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin	-	1.536	-	MHz
			-	1.544	-	MHz
		$MCLK_X$ and $MCLK_R$	-	2.048	-	MHz
Width of Master Clock High	t_{WMH}	$MCLK_X$ and $MCLK_R$	160	-	-	ns
Width of Master Clock Low	t_{WML}	$MCLK_X$ and $MCLK_R$	160	-	-	ns
Rise Time of Master Clock	t_{RM}	$MCLK_X$ and $MCLK_R$	-	-	50	ns
Fall Time of Master Clock	t_{FM}	$MCLK_X$ and $MCLK_R$	-	-	50	ns
Set-up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	t_{SBFM}	First Bit Clock after the Leading Edge of FS_X	100	-	-	ns
Period of Bit Clock	t_{PB}		485	488	15,725	ns
Width of Bit Clock High	t_{WBH}	V_{IH} = 2.2V	160	-	-	ns
Width of Bit Clock Low	t_{WBL}	V_{IL} = 0.6V	160	-	-	ns
Rise Time of Bit Clock	t_{RB}	t_{PB} = 488ns	-	-	50	ns
Fall Time of Bit Clock	t_{FB}	t_{PB} = 488ns	-	-	50	ns
Hold Time from Bit Clock Low to Frame Sync	t_{HBF}	Long Frame Only	0	-	-	ns
Hold Time from Bit Clock High to Frame Sync	t_{HOLD}	Short Frame Only	0	-	-	ns
Set-up Time from Frame Sync to Bit Clock Low	t_{SFB}	Long Frame Only	80	-	-	ns
Delay Time from $BCLK_X$ High to Data Valid	t_{DBD}	Load = 150pF plus 2 LSTTL Loads	0	-	180	ns
Delay Time to $\overline{TS}_X$ Low	t_{XDP}	Load = 150pF plus 2 LSTTL Loads	-	-	140	ns
Delay Time from $BCLK_X$ Low or FS_X Low to Data Output Disabled	t_{DZC}		50	-	165	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	t_{DZF}	C_L = 0pF to 150pF	20	-	165	ns
Set-up Time from D_R Valid to $BCLK_{R/X}$ Low	t_{SDB}		50	-	-	ns
Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	t_{HBD}		50	-	-	ns
Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	t_{SF}	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	50	-	-	ns
Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	t_{HF}	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	100	-	-	ns

Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	t_{HBFI}	Long Frame Sync Pulse (from 3 to 8-Bit Clock Periods Long)	100	-	-	ns
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64K Bit/s Operating Mode	160	-	-	ns

NOTE:

1. For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

Pin Descriptions

PIN NO.	SYMBOL	DESCRIPTION
1	V-	Negative power supply, V- = -5V ±5%.
2	GND	Analog and digital ground. All signals referenced to this pin.
3	VF_RO	Analog output of RECEIVE FILTER.
4	V+	Positive power supply, V+ = 5V ±5%.
5	FS_R	Receive Frame Sync Pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8kHz PULSE TRAIN.
6	D_R	Receive Data Input. PCM data is shifted into D_R following the FS_R leading edge.
7	$BCLK_R$/CLK-SEL	The Receive Bit Clock, which shifts data into D_R after the frame sync leading edge, may vary from 64kHz to 2.048MHz. Alternatively, the leading edge may be a logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for Master Clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions.
8	$MCLK_R$/PDN	Receive Master Clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_X$, but best performance is realized from synchronous operation. When this pin is continuously connected low, $MCLK_X$ is selected for all internal timing. When this pin is continuously connected high, the device is powered down.
9	$MCLK_X$	Transmit Master Clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_R$, but best performance is realized from synchronous operation.
10	$BCLK_X$	The Bit Clock which shifts out the PCM Data on D_X. May vary from 64kHz to 2.048MHz, but must be synchronous with $MCLK_X$.
11	D_X	The THREE-STATE PCM Data Output which is enabled by FS_X.
12	FS_X	Transmit Frame Sync Pulse input which enables $BCLK_X$ to shift out the data on D_X. FS_X is an 8kHz PULSE TRAIN.
13	$\overline{TS}_X$	Open drain output which pulses low during the encoder time slot.
14	GS_X	Transmit gain adjust.
15	VF_XI-	Inverting input of the transmit input amplifier.
16	VF_XI+	Non-inverting input of the transmit input amplifier.

Functional Description

Power Supply Sequencing

Do not apply input signal or load on output before powering up V_{CC} supply. Care must be taken to ensure that D_X pin goes on common back plane (with other D_X pins from other chips). D_X pin cannot drive >50mA before Power-Up. This will cause the part to latch up.

Power-Up

When power is first applied, the Power-On reset circuitry initializes the CODEC and places it in a Power-Down mode. When the CODEC returns to an active state from the Power-Down mode, the receive output is muted briefly to minimize turn-on "click".

To power up the device, there are two methods available.

1. A logical zero at $MCLK_R$/PDN will power up the device, provided FS_X or FS_R pulses are present.
2. Alternatively, a clock ($MCLK_R$) must be applied to $MCLK_R$/PDN and FS_X or FS_R pulses must be present.

Power-Down

Two power-down modes are available.

1. A logical 1 at $MCLK_R$/PDN, after approximately 0.5ms, will power down the device.
2. Alternatively, hold both FS_X and FS_R continuously low, the device will power down approximately 0.5ms after the last FS_X or FS_R pulse.

Synchronous Operation (Transmit and Receive Sections use the Same Master Clock)

The same master clock and bit-clock should be used for the receive and transmit sections. $MCLK_X$ (pin 9) is used to provide the master clock for the transmit section; the receive section will use the same master clock if the $MCLK_R$/PDN (pin 8) is grounded (synchronous operation), or at V+ (power-down mode). $MCLK_R$/PDN may be clocked only if a clock is provided at $BCLK_R$/CLKSEL (pin 7) as in asynchronous operation.

The $BCLK_X$ (pin 10) is used to provide the bit clock to the transmit section. In synchronous operation, this bit clock is also used for the receive section if $MCLK_R$/PDN (pin 8) is grounded. $BCLK_R$/CLKSEL (pin 7) is then used to select the proper internal frequency division for 1.544MHz, 1.536MHz or 2.048MHz operation (see Table below). For 1.544MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the leading edge of $BCLK_X$. After 8 bit-clock periods, the tristate D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of the $BCLK_X$. FS_X and FS_R must be synchronous with $MCLK_X$.

CLOCKING OPTIONS

MODE	$BCLK_R$/CLKSEL (PIN 7)	MASTER CLOCK FREQUENCY SELECTED	
		CD22354A (μ)	CD22357A (A)
Asynchronous or Synchronous	Clocked	1.536MHz or 1.544MHz	2.048MHz
Synchronous	0	2.048MHz	1.536MHz or 1.544MHz
Synchronous	1(or open circuit)	1.536MHz or 1.544MHz	2.048MHz

Asynchronous Operation (Transmit and Receive Sections use Separate Master Clocks)

For the CD22357A, the $MCLK_X$ and $MCLK_R$ must be 2.048MHz and for the CD22354A must be 1.536MHz or 1.544MHz. These clocks need not be synchronous. However, for best transmission performance, it is recommended that $MCLK_X$ and $MCLK_R$ be synchronous.

For 1.544MHz operation the device automatically compensates for the 193rd clock pulse each frame. FS_X starts the encoding operation and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts the decoding operation and must be synchronous with $BCLK_R$. $BCLK_R$ must be clocked in asynchronous operation. $BCLK_X$ and $BCLK_R$ may be between 64kHz - 2.04MHz.

Short-Frame Sync Mode

When the power is first applied, the power initialization circuitry places the CODEC in a short-frame sync mode. In this mode both frame sync pulses must be 1 bit-clock period long, with the timing relationship shown in Figure 1.

With FS_X high during the falling edge of the $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X tristate output buffer, which will output the sign bit. The following rising seven edges clock out the remaining seven bits upon which the next falling edge will disable the D_X output.

With FS_R high during the falling edge of the $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven edges latch in the seven remaining bits.

Long-Frame Sync Mode

In this mode of operation, both of the frame sync pulses must be three or more bit-clock periods long with the timing relationship shown in Figure 2.

Based on the transmit frame sync FS_X, the CODEC will sense whether short or long-frame sync pulses are being used.

For 64kHz operation the frame sync pulse must be kept low for a minimum of 160ns.

The D_X tristate output buffer is enabled with the rising edge of FS_X or the rising edge of the $BCLK_X$, whichever comes later and the first bit clocked out is the sign bit. The following seven rising edges of the $BCLK_X$ clock out the remaining seven bits. The D_X output is disabled by the next falling edge of the $BCLK_X$ following the 8th rising edge or by FS_X going low whichever comes later.

A rising edge on the receive frame sync, FS_R, will cause the PCM data at D_R to be latched in on the next falling edge of the $BCLK_R$. The remaining seven bits are latched on the successive seven falling edges of the bit-clock ($BCLK_X$ in synchronous mode).

Transmit Section

The transmit section consists of a gain-adjustable input op-amp, an anti-aliasing filter, a low-pass filter, a high-pass filter and a compressing A/D converter. The input op-amp drives a RC active anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides 30dB attenuation (Min) at the sampling frequency. From this filter the signal enters a 5th order low-pass filter clocked at 128kHz, followed by a 3rd order high-pass filter clock at 32kHz. The output of the high-pass filter directly drives the encoder capacitor ladder at an 8kHz sampling rate. A precision voltage reference is trimmed in manufacturing to provide an input overload of nominally $2.5V_{PEAK}$. Transmit frame sync pulse FS_X controls the process. The 8-bit PCM data is clocked out at D_X by the $BCLK_X$. $BCLK_X$ can be varied from 64kHz to 2.048MHz.

Receive Section

The receive section consists of an expanding D/A converter and a low-pass filter which fulfills both the AT&T D3/D4 specifications and CCITT recommendations. PCM data enters the receive section at D_R upon the occurrence of FS_R, Receive Frame sync pulse. $BCLK_R$, Receive Data Clock, which can range from 64kHz to 2.048MHz, clocks the 8-bit PCM data into the receive data register. A D/A conversion is performed on the 8-bit PCM data and the corresponding analog signal is held on the D/A capacitor ladder. This signal is transferred to a switched capacitor low-pass filter clocked at 128kHz to smooth the sample-and-hold signal as well as to compensate for the (SIN X)/X distortion.

The filter is then followed by a second order Sallen and Key active filter capable of driving a 600Ω load to a level of 7.2dBm.

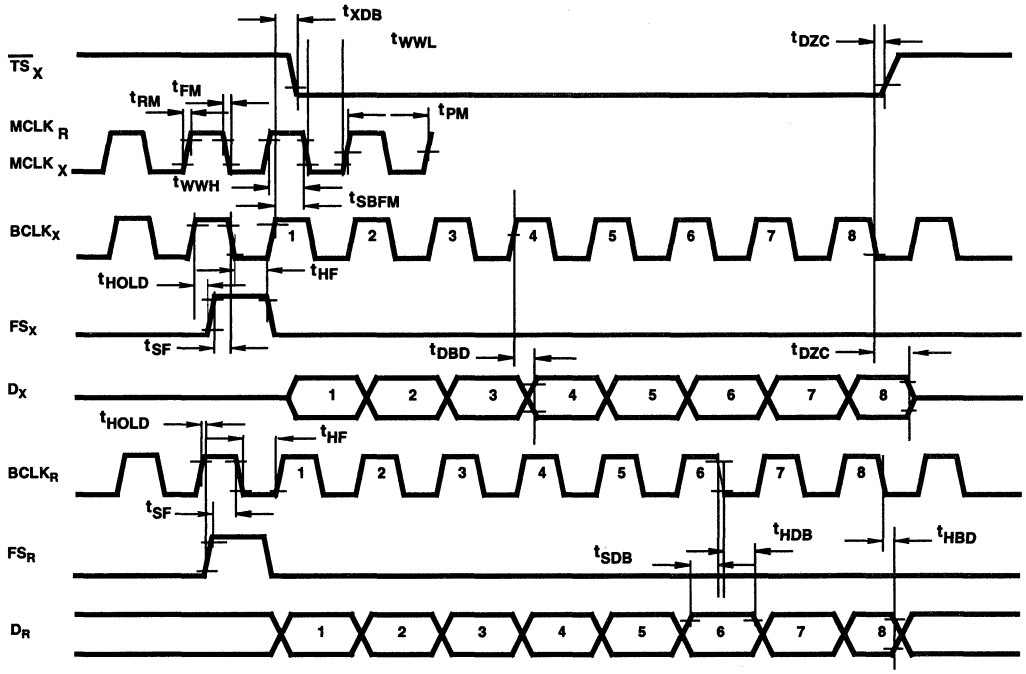


FIGURE 1. SHORT FRAME-SYNC TIMING

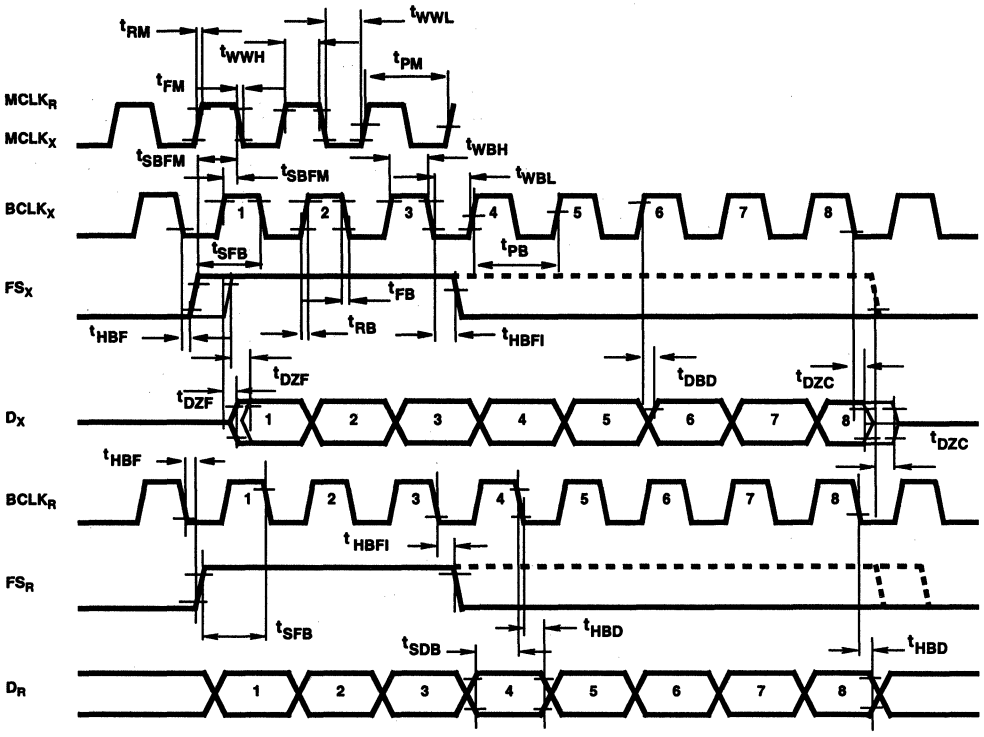


FIGURE 2. LONG FRAME-SYNC TIMING

HARRIS SEMICONDUCTOR

HC-5524

SLIC
Subscriber Line Interface Circuit

January 1997

Features

- DI Monolithic High Voltage Process
- Compatible with Worldwide PBX and DLC Performance Requirements
- Controlled Supply of Battery Feed Current with Programmable Current Limit
- Operates with 5V Positive Supply (V_B+)
- Internal Ring Relay Driver and a Utility Relay Driver
- High Impedance Mode for Subscriber Loop
- High Temperature Alarm Output
- Low Power Consumption During Standby Functions
- Switch Hook, Ground Key, and Ring Trip Detection
- Selective Power Denial to Subscriber
- Voice Path Active During Power Denial
- On-Chip Op Amp for 2-Wire Impedance Matching

Applications

- Solid State Line Interface Circuit for PBX or Digital Loop Carrier Systems
- Hotel/Motel Switching Systems
- Direct Inward Dialing (DID) Trunks
- Voice Messaging PBXs
- 2-Wire/4-Wire, 4-Wire/2-Wire Hybrid
- Related Literature
  - AN9607, Impedance Matching Design Equations
  - AN9628, AC Voltage Gain
  - AN9608, Implementing Pulse Metering
  - AN549, The HC-5502S/4X Telephone Subscriber Line Interface Circuits (SLIC)

Description

The HC-5524 telephone Subscriber Line Interface Circuit integrates most of the BORSCHT functions on a monolithic IC. The device is manufactured in a Dielectric Isolation (DI) process and is designed for use as a 24V interface between the traditional telephone subscriber pair (Tip and Ring) and the low voltage filtering and coding/decoding functions of the line card. Together with a secondary protection diode bridge, the device will withstand 500V induced surges, in plastic packages. The SLIC also maintains specified transmission performance in the presence of externally induced longitudinal currents. The BORSCHT functions that the SLIC provides are:

- Battery Feed with Subscriber Loop Current Limiting
- Overvoltage Protection
- Ring Relay Driver
- Supervisory Signaling Functions
- Hybrid Functions (with External Op-Amp)
- Test (or Battery Reversal) Relay Driver

In addition, the SLIC provides selective denial of power to subscriber loops, a programmable subscriber loop current limit from 20mA to 60mA, a thermal shutdown with an alarm output and line fault protection. Switch hook detection, ring trip detection and ground key detection functions are also incorporated in the SLIC device.

The HC-5524 SLIC is ideally suited for line card designs in PBX and DLC systems, replacing traditional transformer solutions.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC3-5524-5	0 to 75	28 Ld PDIP	E28.6
HC3-5524-9	-40 to 85	28 Ld PDIP	E28.6
HC4P5524-5	0 to 75	44 Ld PLCC	N44.65
HC4P5524-9	-40 to 85	44 Ld PLCC	N44.65
HC9P5524-5	0 to 75	28 Ld SOIC	M28.3
HC9P5524-9	-40 to 85	28 Ld SOIC	M28.3

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2798.4**

Absolute Maximum Ratings (Note 1)

Maximum Supply Voltages
- (V_B+) ..... -0.5V to 7V
- (V_B+) - (V_B-) 40V

Relay Drive Voltage ..... -0.5V to 15V

Operating Conditions

Operating Temperature Range
- HC-5524-5 ..... 0°C to T_A to 75°C
- HC-5524-9 ..... -40°C to T_A to 85°C

Relay Driver Voltage ..... 5V to 12V
Positive Power Supply (V_B+) ..... 5V ±5%
Negative Power Supply (V_B-) ..... -20V to -28V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	55
PLCC Package	47
SOIC Package	75

Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to T_A to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(PLCC and SOIC - Lead Tips Only)

Die Characteristics

Transistor Count 224
Diode Count 28
Die Dimensions ..... 174 mils x 120 mils
Substrate Potential ..... Connected
Process ..... Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Typical Parameters are at T_A = 25°C, V_B+ = 5V, V_B- = -24V, AG = DG = BG = 0V. Min-Max Parameters are Over Operating Positive and Negative Battery Voltages and Over the Operating Temperature Range. All Parameters are Specified at 600W 2-Wire Terminating Impedance, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC TRANSMISSION PARAMETERS					
RX Input Impedance	300Hz to 3.4kHz, (Note 3)	-	100	-	kΩ
TX Output Impedance		-	-	20	Ω
4-Wire Input Overload Level	300Hz to 3.4kHz, 600Ω Reference	+1.0	-	-	V_{PEAK}
2-Wire Return Loss	Matched for 600Ω, (Note 3)				
SRL LO		26	35	-	dB
ERL		30	40	-	dB
SRL HI		30	40	-	dB
2-Wire Longitudinal to Metallic Balance Off Hook	Per ANSI/IEEE STD 455-1976, 300Hz to 3400Hz, (Note 3)	58	63	-	dB
4-Wire Longitudinal Balance Off Hook	Per ANSI/IEEE STD 455-1976, 300Hz to 3400Hz, (Note 3)	50	55	-	dB
Low Frequency Longitudinal Balance	R.E.A. Test Circuit	-	-80	-67	dBmp
	I_{LINE} = 40mA, T_A = 25°C (Note 3)	-	10	23	dBrnC
Longitudinal Current Capability	I_{LINE} = 40mA, T_A = 25°C (Note 3)	-	-	40	mA_{RMS}
Insertion Loss					
2-Wire/4-Wire	-1.58dBm at 1kHz, Referenced 600Ω	-	±0.05	±0.2	dB
4-Wire/2-Wire	0dBm at 1kHz, Referenced 600Ω	-	±0.05	±0.2	dB
4-Wire/4-Wire	-1.58dBm at 1kHz, Referenced 600Ω	-	-	±0.2	dB
Frequency Response	300Hz to 3400Hz, Referenced to Absolute Level at 1kHz, 0dBm Referenced 600Ω (Note 3)	-	±0.02	±0.06	dB

Electrical Specifications Typical Parameters are at $T_A = 25^oC$, $V_B+ = 5V$, $V_B- = -24V$, AG = DG = BG = 0V. Min-Max Parameters are Over Operating Positive and Negative Battery Voltages and Over the Operating Temperature Range. All Parameters are Specified at 600W 2-Wire Terminating Impedance, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Level Linearity 2-Wire to 4-Wire and 4-Wire to 2-Wire	Referenced to -10dBm, (Note 3) +3 to -40dBm	-	-	±0.08	dB
	-40 to -50dBm	-	-	±0.12	dB
	-50 to -55dBm	-	-	±0.3	dB
Absolute Delay 2-Wire/4-Wire	(Note 2) 300Hz to 3400Hz	-	-	1	µs
4-Wire/2-Wire	300Hz to 3400Hz	-	-	1	µs
4-Wire/4-Wire	300Hz to 3400Hz	-	0.95	1.5	µs
Total Harmonic Distortion 2-Wire/4-Wire, 4-Wire/2-Wire, 4-Wire/4-Wire	Reference Level 0dBm at 600Ω, 300Hz to 3400Hz (Note 3)	-	-	-50	dB
Idle Channel Noise 2-Wire and 4-Wire	C-Message, (Note 3)	-	-	5	dBrnC
	Psophometric	-	-	-85	dBmp
	3kHz Flat	-	-	16	dBrn
Open Loop Voltage (V_{TIP} - V_{RING})	$V_B+ = 5V$, $V_B- = -24V$	-	15.8	-	V
Power Supply Rejection Ratio V_B+ to 2-Wire	30Hz to 200Hz, $R_L = 600\Omega$, (Note 3)	20	40	-	dB
V_B+ to 4-Wire		20	40	-	dB
V_B- to 2-Wire		20	40	-	dB
V_B- to 4-Wire		20	50	-	dB
V_B+ to 2-Wire	200Hz to 16kHz, $R_L = 600\Omega$	30	40	-	dB
V_B+ to 4-Wire		20	28	-	dB
V_B- to 2-Wire		20	50	-	dB
V_B- to 4-Wire		20	50	-	dB
Ring Sync Pulse Width		50	-	500	µs
DC PARAMETERS					
Loop Current Programming Limit Range		20	-	60	mA
Accuracy		10	-	-	%
Loop Current During Power Denial	$R_L = 200\Omega$	-	±4	±7	mA
Fault Currents TIP to Ground		-	30	-	mA
RING to Ground		-	120	-	mA
TIP and RING to Ground		-	150	-	mA
Switch Hook Detection Threshold		-	12	15	mA
Ground Key Detection Threshold		-	10	-	mA
Thermal $\overline{ALM}$ Output	Safe Operating Die Temperature Exceeded	140	-	160	°C
Ring Trip Detection Threshold	$V_{RING} = 105V_{RMS}$, $f_{RING} = 20Hz$	-	10	-	mA
Ring Trip Detection Period		-	100	150	ms
Dial Pulse Distortion		-	0.1	0.5	ms

Electrical Specifications Typical Parameters are at $T_A = 25^oC$, $V_B+ = 5V$, $V_B- = -24V$, AG = DG = BG = 0V. Min-Max Parameters are Over Operating Positive and Negative Battery Voltages and Over the Operating Temperature Range. All Parameters are Specified at 600W 2-Wire Terminating Impedance, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Relay Driver Outputs					
On Voltage V_{OL}	I_{OL} ($\overline{PR}$) = 60mA, I_{OL} ($\overline{RD}$) = 30mA	-	0.2	0.5	V
Off Leakage Current	V_{OH} = 13.2V	-	±10	±100	µA
TTL/CMOS Logic Inputs (F0, F1, RS, $\overline{TST}$, PRI)					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Input Current (F0, F1, RS, $\overline{TST}$, PRI)	$0V \le V_{IN} \le 5V$	-	-	±100	µA
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} = 800µA	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} = 40µA	2.7	-	-	V
Power Dissipation On Hook	Relay Drivers Off	-	60	-	mW
I_B+	$V_B+ = 5.25V$, $V_B- = -28V$, $R_{LOOP} = \infty$	-	-	4	mA
I_B-	$V_B+ = 5.25V$, $V_B- = -28V$, $R_{LOOP} = \infty$	-4	-	-	mA
I_B+	$V_B+ = 5V$, $V_B- = -24V$, $R_{LOOP} = 600\Omega$	-	3	6	mA
I_B-	$V_B+ = 5V$, $V_B- = -24V$, $R_{LOOP} = 600\Omega$	-28	-24	-	mA
UNCOMMITED OP AMP PARAMETERS					
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Differential Input Resistance	(Note 3)	-	1	-	MΩ
Output Voltage Swing	$R_L = 10k\Omega$	-	±3	-	V_{P-P}
Small Signal GBW	(Note 3)	-	1	-	MHz

NOTE:

3. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Pin Descriptions

DIP/ SOIC	PLCC	SYMBOL	DESCRIPTION
1	2	AG (Note 4)	Analog Ground - To be connected to zero potential. Serves as a reference for the transmit output and receive input terminals.
2	3	V_B+	Positive Voltage Source - Most Positive Supply.
3	4	C_1	Capacitor #C_1 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function.
4	8	F1	Function Address #1 - A TTL and CMOS compatible input used with F0 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on front page. F1 should be toggled high after power is applied.
5	9	F0	Function Address #0 - A TTL and CMOS compatible input used with F1 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on front page.

Pin Descriptions (Continued)

DIP/ SOIC	PLCC	SYMBOL	DESCRIPTION
6	10	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive pulse (50µs - 500µs) occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring delay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5V.
7	11	$\overline{SHD}$	Switch Hook Detection - An active low LS TTL compatible logic output. A line supervisory output.
8	12	$\overline{GKD}$	Ground Key Detection - An active low LS TTL compatible logic output. A line supervisory output.
9	13	$\overline{TST}$	A TTL logic input. A low on this pin will set a latch and keep the SLIC in a power down mode until the proper F1, F0 state is set and will keep $\overline{ALM}$ low. See Truth Table on front page.
10	17	$\overline{ALM}$	A LS TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded. When $\overline{TST}$ is forced low by an external control signal, $\overline{ALM}$ is latched low until the proper F1, F0 state and $\overline{TST}$ input is brought high. The $\overline{ALM}$ can be tied directly to the $\overline{TST}$ pin to power down the part when a thermal fault is detected and then reset with F0, F1. See Truth Table on front page. It is possible to ignore transient thermal overload conditions in the SLIC by delaying the response to the $\overline{TST}$ pin from the $\overline{ALM}$. Care must be exercised in attempting this as continued thermal overstress may reduce component life.
11	18	I_{LIMIT}	Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions using a resistive voltage divider.
12	19	OUT1	The analog output of the spare operational amplifier.
13	20	-IN1	The inverting analog input of the spare operational amplifier.
14	22	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor and ring relay contact. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purposes.
15	24	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.
16	25	RFS	Ring Feed Sense - Senses RING side of the loop for Ground Key Detection. During Ring injected ringing the ring signal at this node is isolated from RF via the ring relay. For Tip injected ringing, the RF and RFS pins must be shorted.
17	27	V_{RX}	Receive Input, 4-Wire Side - A high impedance analog input. AC signals appearing at this input drive the Tip Feed and Ring Feed amplifiers differentially.
18	31	C_2	Capacitor #2 - An external capacitor to be connected between this terminal and ground. It prevents false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from power lines and other noise sources. This capacitor should be nonpolarized.
19	32	V_{TX}	Transmit Output, 4-Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Transhybrid balancing must be performed beyond this output to completely implement two to four wire conversion. This output is referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is necessary.
20	33	PRI	A TTL compatible input used to control $\overline{PR}$. PRI active High = $\overline{PR}$ active low.
21	34	$\overline{PR}$	An active low open collector output. Can be used to drive a Polarity Reversal Relay.
22	35	DG (Note 4)	Digital Ground - To be connected to zero potential. Serves as a reference for all digital inputs and outputs on the SLIC.
23	36	$\overline{RD}$	Ring Relay Driver - An active low open collector output. Used to drive a relay that switches ringing signals onto the 2-Wire line.

Pin Descriptions (Continued)

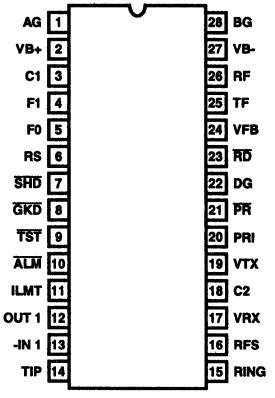
DIP/ SOIC	PLCC	SYMBOL	DESCRIPTION
24	37	V_{FB} (Note 5)	Feedback input to the tip feed amplifier; may be used in conjunction with transmit output signal and the spare op-amp to accommodate 2-Wire line impedance matching. (This is not used in the typical applications circuit).
25	38	TF_2	Tip Feed - A low impedance analog output connected to the TIP terminal through a feed resistor. Functions with the RF terminal to provide loop current, and to feed voice signals to the telephone set and to sink longitudinal currents. Must be tied to TF_1.
NA	39	TF_1	Tie directly to TF_2 in the PLCC application.
26	41	RF_1	Ring Feed - A low impedance analog output connected to the RING terminal through a feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and to sink longitudinal currents. Tie directly to RF2.
NA	42	RF_2	Tie directly to RF_1 in the PLCC application.
27	43	V_B-	The battery voltage source. The most negative supply.
28	44	BG (Note 4)	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
	1, 5, 6, 7, 14, 15, 16, 21, 23, 26, 28, 29, 30, 40	NC	No internal connection.

NOTES:

4. All grounds (AG, BG, and DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
5. Although not used in the typical applications circuit, V_{FB} may be used in matching complex 2-Wire impedances.

Pinouts

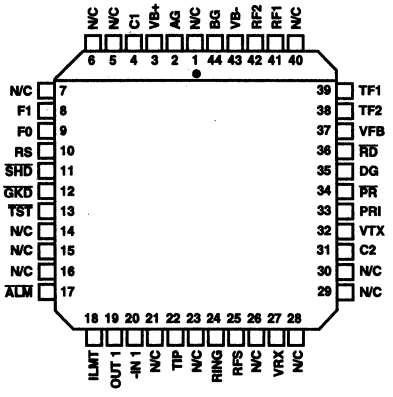
HC-5524 (PDIP, SOIC)
TOP VIEW



TRUTH TABLE

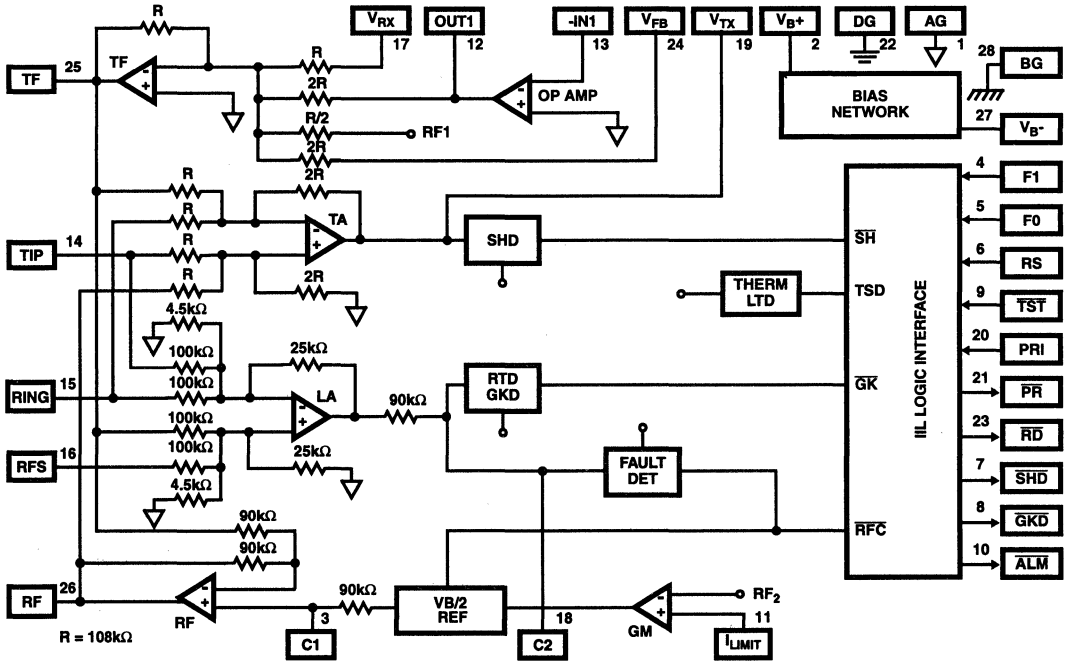
F1	F0	Action
0	0	Normal Loop Feed
0	1	$\overline{RD}$ Active
1	0	Power Down Latch RESET
1	0	Power on RESET
1	1	Loop Power Denial Active

HC-5524 (PLCC)
TOP VIEW

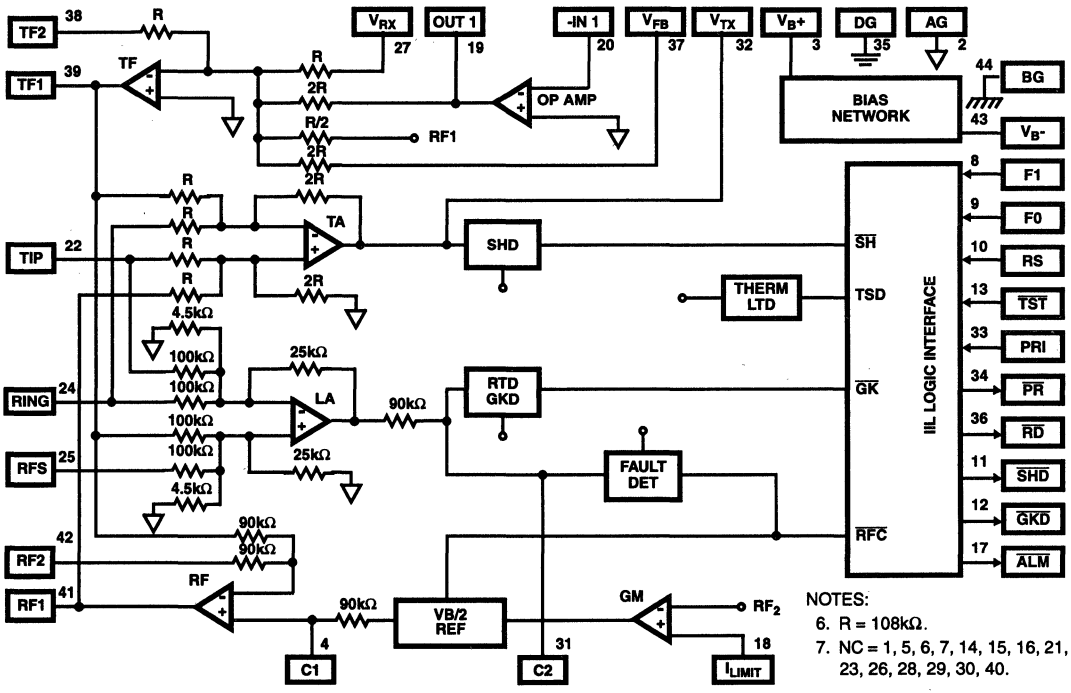


Functional Diagram

DIP OR SOIC



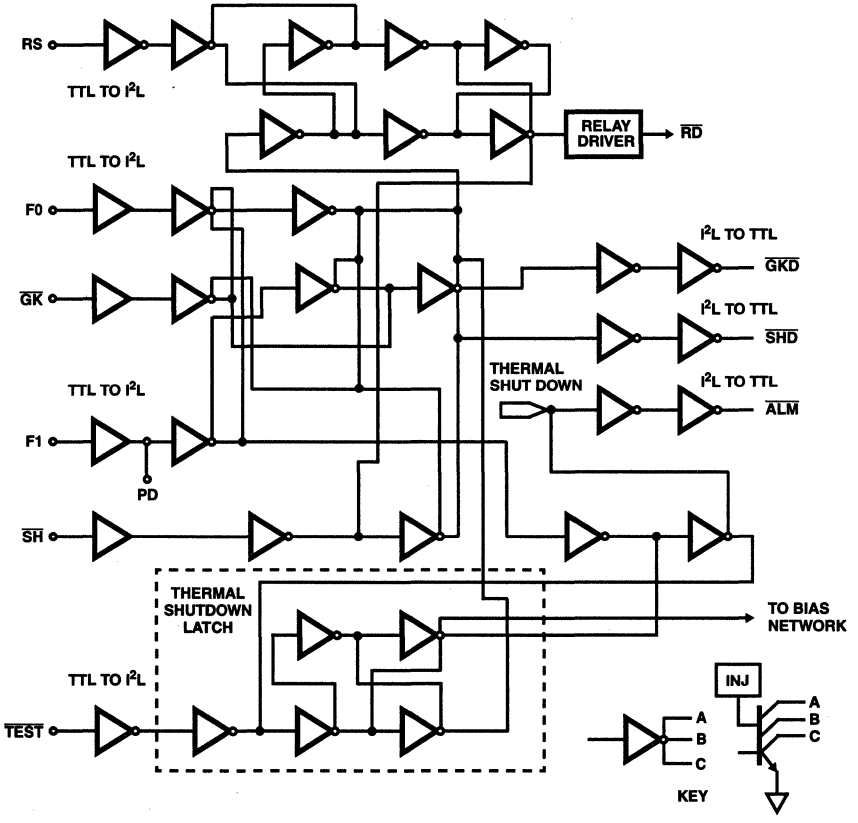
PLCC



NOTES:

6. R = 108kΩ.
7. NC = 1, 5, 6, 7, 14, 15, 16, 21, 23, 26, 28, 29, 30, 40.

Logic Diagram



Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or $40mA_{RMS}$, $20mA_{RMS}$ per leg, without any performance degradation.

TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
50/60Hz Current T/GND R/GND	11 Cycles Limited to $10A_{RMS}$	700 (Plastic)	V_{RMS}

Typical Applications

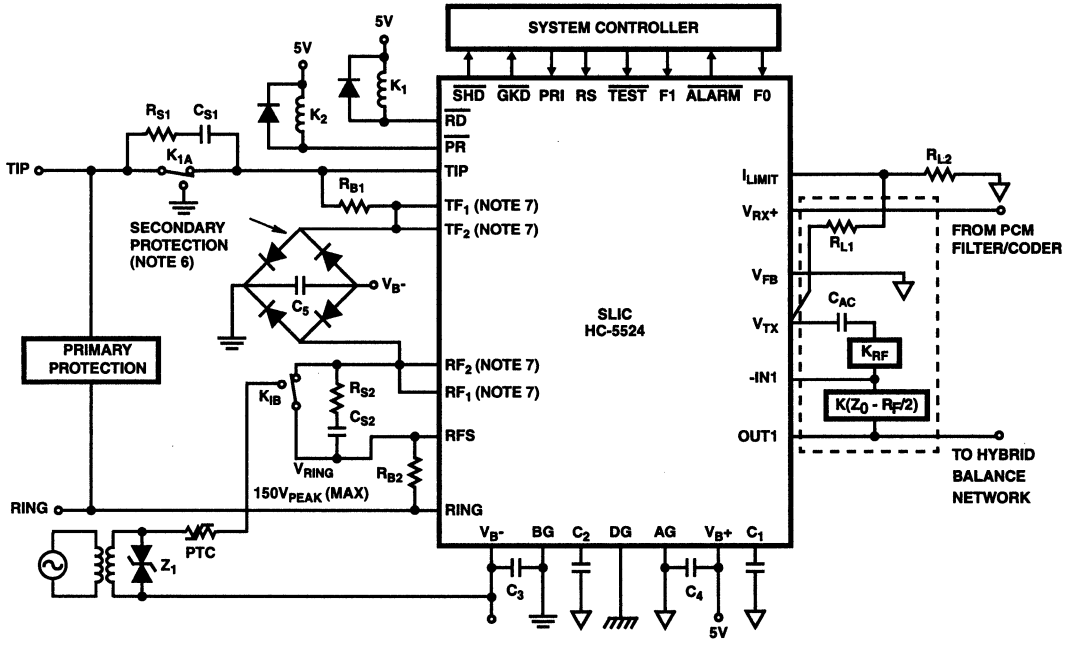


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values

C_1 = 0.5µF, 20V

C_2 = 1.0µF ±10%, 20V (for other values of C2, refer to AN9667)

C_3 = 0.01µF, 50V ±20%

C_4 = 0.01µF, 50V ±20%

C_5 = 0.01µF, 50V ±20%

C_{AC} = 0.5µF, 20V

$K(Z_0 - R_F/2)$ = 50kΩ, (Z_0 = 600Ω, K = Scaling Factor = 100)

R_{L1}, R_{L2}; Current Limit Setting Resistors
$R_{L1}+R_{L2} > 90k\Omega$

$I_{LIMIT} = (.6)\ (R_{L1} + R_{L2})/(200 \times R_{L2})$, R_{L1} typically 100kΩ

KR_F = 20kΩ, $R_F = 2(R_{B1}+R_{B2})$, K = Scaling Factor = 100)

$R_{B1} = R_{B2}$ = 50Ω (1% absolute, matching requirements covered in a Tech Brief)

$R_{S1} = R_{S2}$ = 1kΩ typically

$C_{S1} = C_{S2}$ = 0.1µF, 200V typically, depending on V_{Ring} and line length.

Z_1 = 150V to 200V transient protector. PTC used as ring generator ballast.

NOTES:

8. All grounds (AG, BG, and DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first
9. Application shows Ring Injected Ringing, Balanced or Tip injected configuration may be used.
10. Secondary protection diode bridge recommended is 3A, 200V type.
11. TF_1, TF_2 and RF_1, RF_2 are on PLCC only and should be connected together as shown.

HARRIS SEMICONDUCTOR

CD22100

CMOS 4 x 4 Crosspoint Switch with Control Memory High-Voltage Type (20V Rating)

January 1997

Features

- Low ON Resistance . . . . . 75Ω (Typ) at V_{DD} = 12V
- "Built-In" Control Latches
- Large Analog Signal Capability . . . . . $\pm V_{DD}/2$
- 10MHz Switch Bandwidth
- Matched Switch Characteristics ΔR_{ON} = 18Ω (Typ) at V_{DD} = 12V
- High Linearity - 0.5% Distortion (Typ) at f = 1kHz, $V_{IN} = 5V_{P-P}$, V_{DD} = 10V, and R_L = 1kΩ
- Standard CMOS Noise Immunity
- 100% Tested for Maximum Quiescent Current at 20V

Description

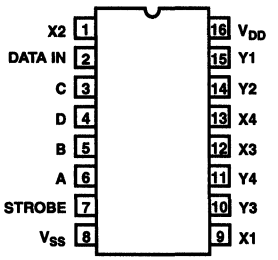
CD22100 combines a 4 x 4 array of crosspoints (transmission gates) with a 4-line to 16-line decoder and 16 latch circuits. Any one of the sixteen transmission gates (crosspoints) can be selected by applying the appropriate four line address. The selected transmission gate can be turned on or off by applying a logic one or zero, respectively, to the data input and strobing the strobe input to a logic one. Any number of the transmission gates can be ON simultaneously. When the required operating power is applied to the CD22100, the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high and data in low, and then addressing all switches in succession.

Ordering Information

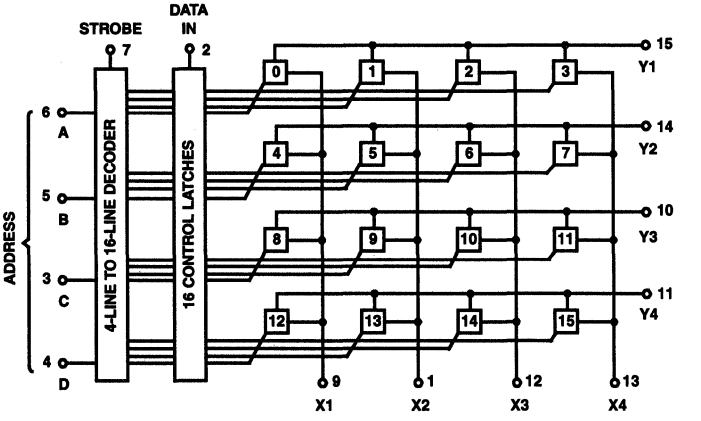
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22100E	-40 to 85	16 Ld PDIP	E16.3
CD22100F	-55 to 125	16 Ld CERDIP	F16.3

Pinout

CD22100
(PDIP, CERDIP)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1076.3**

Absolute Maximum Ratings

Supply Voltage (Referenced to VSS Terminal) . . . . . -0.5 to 20V
Input Voltage (All Inputs) . . . . . -0.5 to V_{DD} 0.5V
Input Current (Any one input (Note 1)) . . . . . ±10mA
Power Dissipation
For T_A = -40°C to 60°C (Package Type E) 500mW
For T_A = 60°C to 85°C
(Package Type E) . . . . . Derate Linearly 12mW/°C to 200mW
For T_A = -55°C to 100°C (Package Type F) 500mW
For T_A = 100°C to 125°C
(Package Type F) . . . . . Derate Linearly 12mW/°C to 200mW
Device Dissipation per Transmission Gate
For T_A = Full Package Temperature Range (All Types) 100mW

Thermal Information

Maximum Junction Temperature . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Storage Temperature Range . . . . . -65°C ≤ T_A ≤ 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Temperature Range
Package Type F . . . . . -55°C ≤ T_A ≤ 125°C
Package Type E . . . . . -40°C ≤ T_A ≤ 85°C
Supply Voltage Range
For T_A = Full Package Temperature Range . . . . . 3V to 18V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Values at -55°C, 25°C, 125°C Apply to F Package
Values at -40°C, 25°C, 85°C Apply to E Package

PARAMETER	SYMBOL	TEST CONDITIONS	FIG.	V_{DD} (V)	-55°C MAX	-40°C MAX	85°C MAX	125°C MAX	25°C MIN	25°C TYP	25°C MAX	UNITS
STATIC CROSSPOINTS												
Quiescent Device Current	I_{DD} (Max)		1	5	5	5	150	150	-	0.04	5	µA
			1	10	10	10	300	300	-	0.04	10	µA
			1	15	20	20	600	600	-	0.04	20	µA
			1	20	100	100	3000	3000	-	0.08	100	µA
On Resistance	R_{ON} (Max)	Any Switch V_{IS} = 0 to V_{DD}	11	5	475	500	725	800	-	225	600	Ω
			12	10	135	145	205	230	-	85	180	Ω
			-	12	100	110	155	175	-	75	135	Ω
			13	15	70	75	110	125	-	65	95	Ω
ΔR_{ON} Resistance	ΔR_{ON}	Between any two switches	-	5	-	-	-	-	-	25	-	Ω
			-	10	-	-	-	-	-	10	-	Ω
			-	12	-	-	-	-	-	8	-	Ω
			-	15	-	-	-	-	-	5	-	Ω
OFF Switch Leakage Current	I_L (Max)	All switches OFF, V_{IS} = 18V	3	18	±100		±1000		-	±1	±100 (Note 2)	nA
STATIC CONTROLS												
Input Low Voltage	V_{IL} (Max)	OFF switch I_L < 0.2µA	-	5	1.5				-	-	1.5	V
			-	10	3				-	-	3	V
			-	15	4				-	-	4	V
Input High Voltage	V_{IH} (Min)	ON switch see R_{ON} characteristic	-	5	3.5				3.5	-	-	V
			-	10	7				7	-	-	V
			-	15	11				11	-	-	V
Input Current	I_{IN} (Max)	Any control V_{IN} = 0, 18V	2	18	±0.1	±0.1	±1	±1	-	$±10^{-5}$	±0.1	µA

NOTES:

1. Maximum current through transmission gates (switches) = 25mA.
2. Determined by minimum feasible leakage measurement for automatic testing.

Electrical Specifications $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS FIGURE	f_{IS} (kHz)	R_L (kΩ)	V_{IS} (V) (Note 3)	V_{DD} (V)	MIN	TYP	MAX	UNITS
DYNAMIC CROSSPOINTS										
Propagation Delay Time, (Switch ON) Signal Input to Output	t_{PHL}, t_{PLH}	5	-	10	5	5	-	30	60	ns
					10	10	-	15	30	ns
					15	15	-	10	20	ns
			C_L = 50pF; t_R, t_F = 20ns							
Frequency Response (Any Switch ON)	f_{3dB}	16	1	1	5	10	-	40	-	MHz
			Sine Wave Input, $20 \log \frac{V_{OS}}{V_{IS}}$ = -3dB							
Sine Wave Response (Distortion)	THD		1	1	5	10	-	0.5	-	%
Feedthrough (All switches OFF)	F_{DT}		1.6	1	5	10	-	-80	-	dB
			Sine Wave Input							
Frequency for Signal Crosstalk	F_{CT}	7	-	1	10	10				
Attenuation of 40dB			Sine Wave Input				-	1.5	-	MHz
Attenuation of 110dB			-	-	-	-	-	0.1	-	kHz
Capacitance:	C_{IS}									
Xn to Ground			-	-	-	5 - 15	-	18	-	pF
Yn to Ground			-	-	-	5 - 15	-	30	-	pF
Feedthrough	C_{IOS}		-	-	-	-	-	0.4	-	pF
DYNAMIC CONTROLS										
Propagation Delay Time: Strobe to Output (Switch Turn-ON to High Level)	t_{PZH}	8	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	300	600	ns
						10	-	125	250	ns
						15	-	80	160	ns
Propagation Delay Time: Data-In to Output (Turn-ON to High Level)	t_{PZH}	9	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	110	220	ns
						10	-	40	80	ns
						15	-	25	50	ns
Propagation Delay Time: Address to Output (Turn-ON to High Level)	t_{PZH}	10	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	350	700	ns
						10	-	135	270	ns
						15	-	90	180	ns
Propagation Delay Time: Strobe to Output (Switch Turn-OFF)	t_{PHZ}	8	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	165	330	ns
						10	-	85	170	ns
						15	-	70	140	ns
Propagation Delay Time: Data-In to Output (Turn-ON to Low Level)	t_{PZL}	9	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	210	420	ns
						10	-	110	220	ns
						15	-	100	200	ns
Propagation Delay Time: Address to Output (Turn-OFF)	t_{PHZ}	10	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	435	870	ns
						10	-	210	420	ns
						15	-	160	320	ns

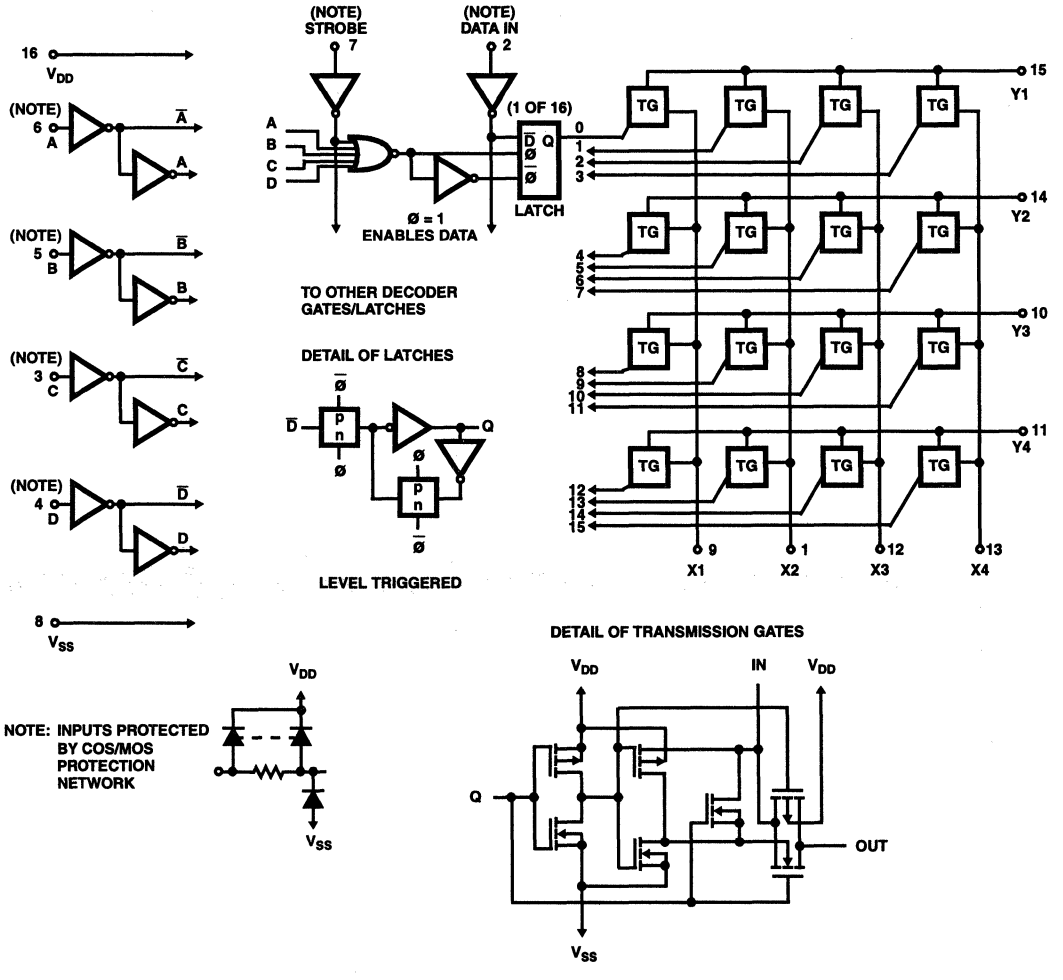
Electrical Specifications $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS					MIN	TYP	MAX	UNITS
		FIGURE	f_{IS} (kHz)	R_L (kΩ)	V_{IS} (V) (Note 3)	V_{DD} (V)				
Minimum Setup Time Data-In to Strobe, Address	t_S	8, 10	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	95	190	ns
						10	-	25	50	ns
						15	-	15	30	ns
Minimum Hold Time Data-In to Strobe, Address	t_H	8, 10	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	180	360	ns
						10	-	110	220	ns
						15	-	35	70	ns
Maximum Switching Frequency	$f_Ø$		R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	0.6	1.2	-	MHz
						10	1.6	3.2	-	MHz
						15	2.5	5	-	MHz
Minimum Strobe Pulse Width	t_W	8				5	-	300	600	ns
						10	-	120	240	ns
						15	-	90	180	ns
Control Crosstalk, Data-In, Address or Strobe to Output		6	Square Wave Input; t_R, t_F = 20ns			10	-	75	-	mV_{PEAK}
			-	10	10					
Input Capacitance	C_{IN}		Any Control Input			-	-	5	7.5	pF

NOTE:

3. Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$.

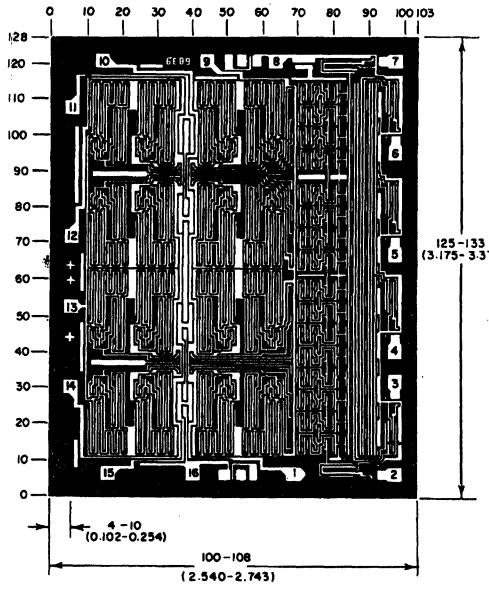
Schematic Diagram



TRUTH TABLE

ADDRESS					ADDRESS				
A	B	C	D	SELECT	A	B	C	D	SELECT
0	0	0	0	X1Y1	0	0	0	1	X1Y3
1	0	0	0	X2Y1	1	0	0	1	X2Y3
0	1	0	0	X3Y1	0	1	0	1	X3Y3
1	1	0	0	X4Y1	1	1	0	1	X4Y3
0	0	1	0	X1Y2	0	0	1	1	X1Y4
1	0	1	0	X2Y2	1	0	1	1	X2Y4
0	1	1	0	X3Y2	0	1	1	1	X3Y4
1	1	1	0	X4Y2	1	1	1	1	X4Y4

Metallization Mask Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Test Circuits and Waveforms

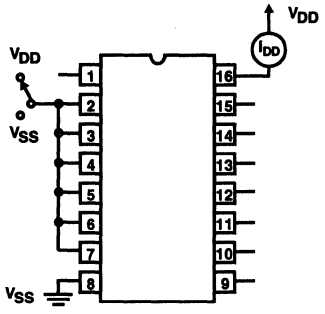


FIGURE 1. QUIESCENT CURRENT TEST CIRCUIT

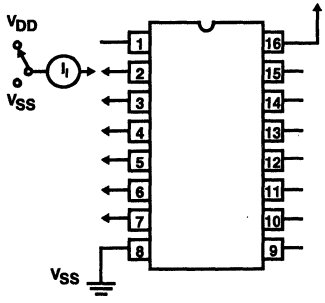


FIGURE 2. INPUT CURRENT TEST CIRCUIT

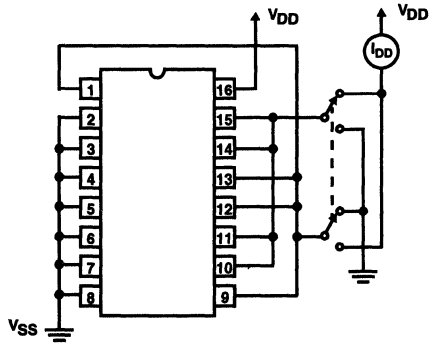
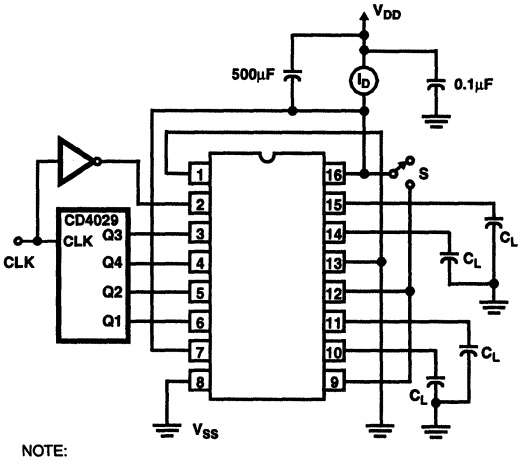


FIGURE 3. OFF SWITCH INPUT OR OUTPUT LEAKAGE CURRENT TEST CIRCUIT

Test Circuits and Waveforms (Continued)



NOTE:
CLOSE SWITCH S AFTER APPLYING V_{DD}

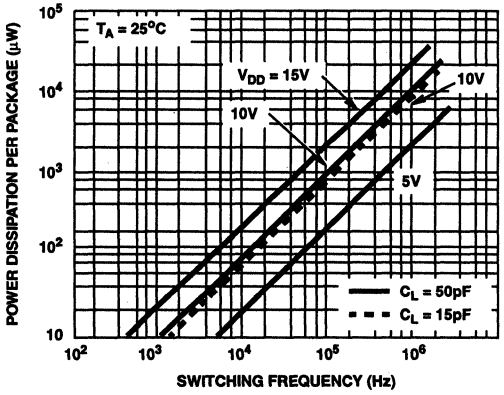


FIGURE 4. DYNAMIC POWER DISSIPATION TEST CIRCUIT AND TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF SWITCHING FREQUENCY

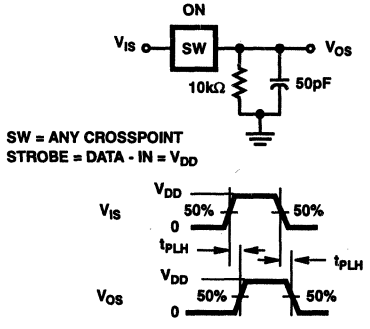


FIGURE 5. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (SIGNAL INPUT TO SIGNAL OUTPUT, SWITCH ON)

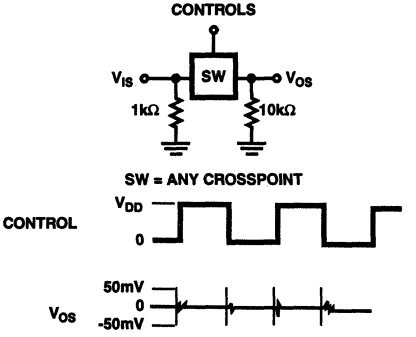
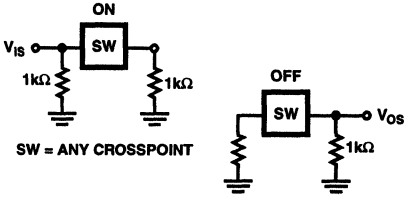


FIGURE 6. TEST CIRCUIT AND WAVEFORMS FOR CROSSTALK (CONTROL INPUT TO SIGNAL OUTPUT)



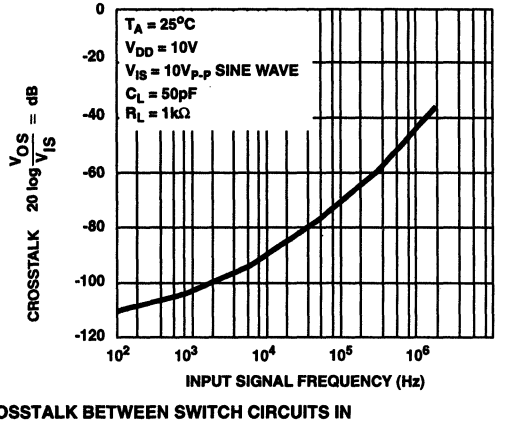


FIGURE 7. TEST CIRCUIT AND TYPICAL CROSSTALK BETWEEN SWITCH CIRCUITS IN THE SAME PACKAGE AS A FUNCTON OF SIGNAL FREQUENCY

Test Circuits and Waveforms (Continued)

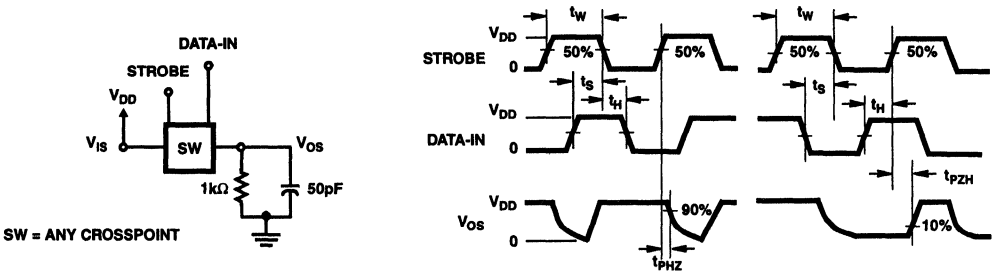


FIGURE 8. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS
(STROBE TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

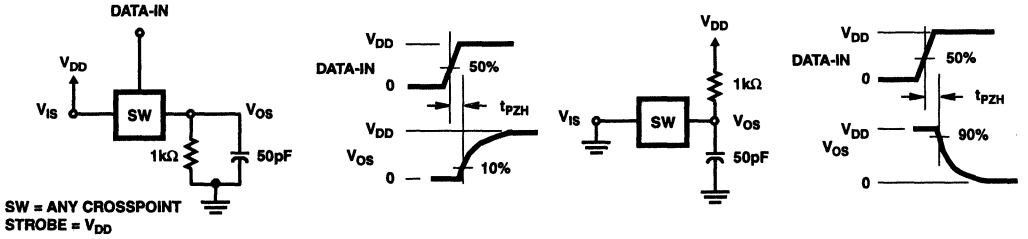


FIGURE 9. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS
(DATA-IN TO SIGNAL OUTPUT, SWITCH TURN-ON TO HIGH OR LOW LEVEL)

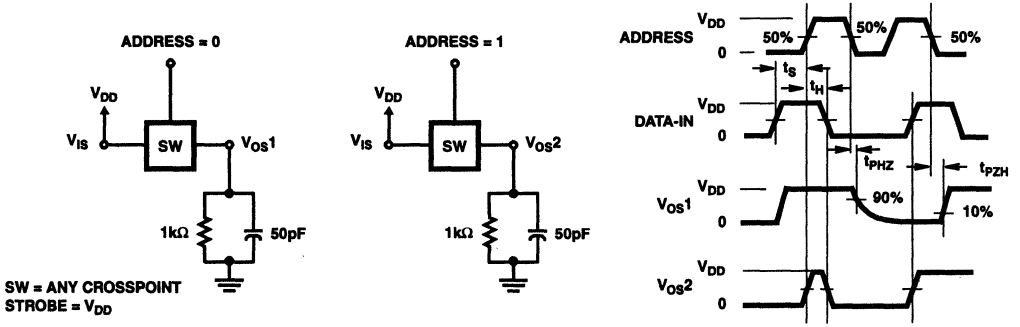


FIGURE 10. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS
(ADDRESS TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

Typical Performance Curves

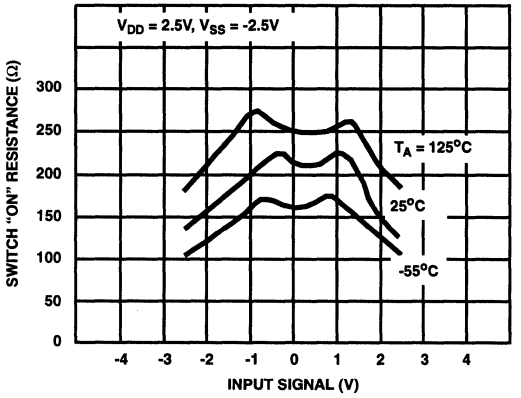


FIGURE 11. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT $V_{DD} = -V_{SS} = 2.5V$

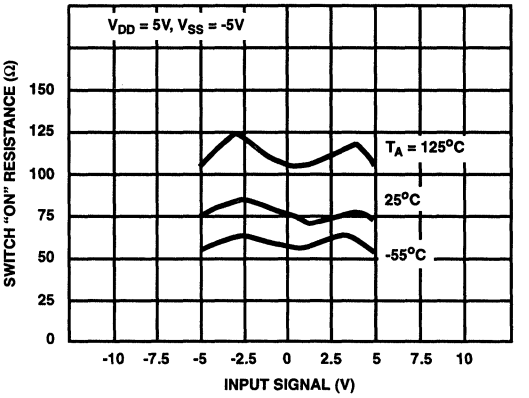


FIGURE 12. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT $V_{DD} = -V_{SS} = 5V$

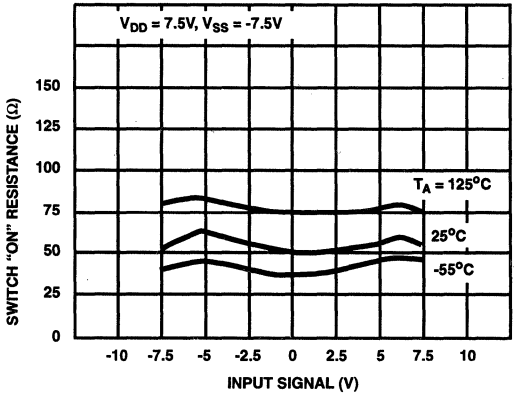


FIGURE 13. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT $V_{DD} = -V_{SS} = 7.5V$

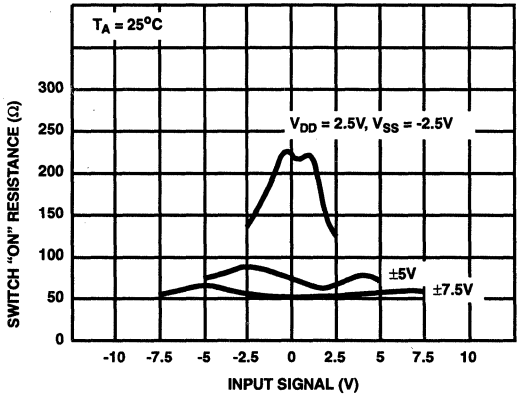


FIGURE 14. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT $T_A = 25°C$

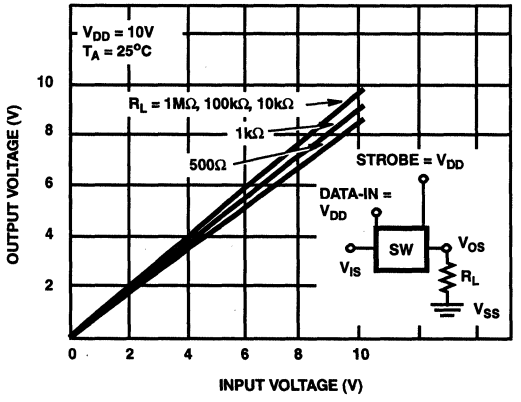


FIGURE 15. TYPICAL SWITCH ON TRANSFER CHARACTERISTICS (1 OF 16 SWITCHES)

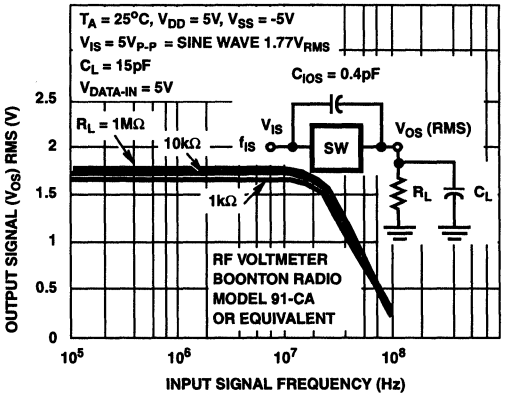


FIGURE 16. TYPICAL SWITCH ON FREQUENCY RESPONSE CHARACTERISTICS

HARRIS SEMICONDUCTOR CD22101, CD22102

CMOS 4 x 4 x 2 Crosspoint Switch with Control Memory

January 1997

Features

- Low ON Resistance ..... 75Ω (Typ) at V_{DD} = 12V
- "Built - In" Latched Inputs
- Large Analog Signal Capability ..... $\pm V_{DD}/2$
- Switch Bandwidth 10MHz
- Matched Switch Characteristics ΔR_{ON} = 8Ω (Typ) at V_{DD} = 12V
- High Linearity - 0.25% Distortion (Typ) at f = 1kHz, $V_{IN} = 5V_{P-P}$, $V_{DD} - V_{SS}$ = 10V, and R_L = 1kΩ
- Standard CMOS Noise Immunity

Applications

- Telephone Systems
- PBX
- Studio Audio Switching
- Multisystem Bus Interconnect

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22101E	-40 to 85	24 Ld PDIP	E24.6
CD22101F	-55 to 125	24 Ld CERDIP	F24.6
CD22102E	-40 to 85	24 Ld PDIP	E24.6

Description

CD22101 and CD22102 crosspoint switches consist of 4 x 4 x 2 arrays of crosspoints (transmission gates) with a 4-line to 16-line decoder and 16 latch circuits. Any one of the sixteen crosspoint pairs can be selected by applying the appropriate four-line address, corresponding crosspoints in each array are turned on and off simultaneously. Any number of crosspoints can be turned on simultaneously.

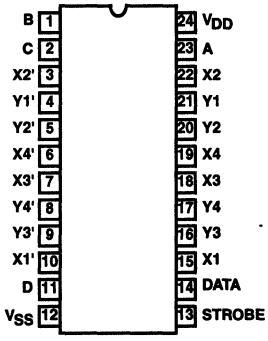
In the CD22101, the selected crosspoint pair can be turned on or off by applying a logic ONE or ZERO, respectively, to the data input, and applying a ONE to the strobe input. When the device is "powered up", the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high, data-in low, and then addressing all switches in succession.

The selected pair of crosspoints in the CD22102 is turned on by applying a logic ONE to the K_A (set) input while a logic ZERO is on the K_B input, and turned off by applying a logic ONE to the K_B (reset) input while a logic ZERO is on the K_A input. In this respect, the control latches of the CD22102 are similar to SET/RESET flip-flops. They differ, however, in that the simultaneous application of ONEs to the K_A and K_B inputs turns off (resets) all crosspoints. All crosspoints in both devices must be turned off as V_{DD} is applied.

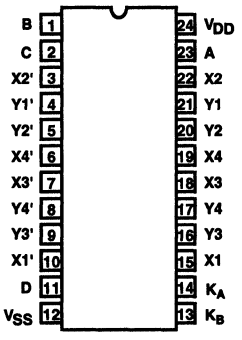
4 WIRED COMMUNICATIONS

Pinouts

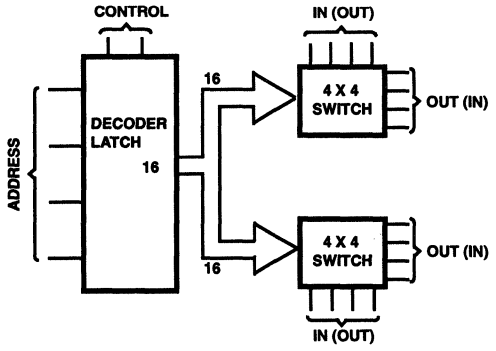
CD22101 (PDIP, SBDIP) TOP VIEW



CD22102 (PDIP) TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 2871.2

Absolute Maximum Ratings

Supply Voltage (V_{DD}) (Referenced to V_{SS} Terminal) . . . . -0.5 to 20V
Input Voltage (All Inputs) . . . . . -0.5 to V_{DD} +0.5V
Supply Voltage Range
For T_A = Full Package Temperature Range . . . . . 3V to 18V
Input Current (Any One Input) (Note 1) . . . . . ±10mA
Power Dissipation
For T_A = -40°C to 60°C (Package Type E) 500mW
For T_A = 60°C to 85°C
Package Type E) . . . . . Derate Linearly 12mW/°C to 200mW
For T_A = -55°C to 100°C (Package Type D, F) 500mW
For T_A = 100°C to 125°C
(Package Type D, F) . . . . . Derate Linearly 12mW/°C to 200mW
Device Dissipation per Output Transistor
For T_A = Full Package Temperature Range (All Types) 100mW

Thermal Information

Maximum Junction Temperature . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . $-65°C \le T_A \le 150°C$
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Temperature Range
Package Type D, F . . . . . $-55°C \le T_A \le 125°C$
Package Type E . . . . . $-40°C \le T_A \le 85°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Values at -55°C, 25°C, 125°C Apply to D, F, H Packages
Values at -40°C, 25°C, 85°C Apply to E Package

PARAMETER	SYMBOL	TEST CONDITIONS	FIGURE	V_{DD} (V)	-55°C MAX	-40°C MAX	85°C MAX	125°C MAX	25°C MIN	25°C TYP	25°C MAX	UNITS
STATIC CROSSPOINTS												
Quiescent Device Current	I_{DD} (Max)		1	5	5	5	150	150	-	0.04	5	µA
			1	10	10	10	300	300	-	0.04	10	µA
			1	15	20	20	600	600	-	0.04	20	µA
			1	20	100	100	3000	3000	-	0.08	100	µA
On Resistance	R_{ON} (Max)	Any Switch V_{IS} = 0 to V_{DD}	14	5	475	500	725	800	-	225	600	Ω
			15	10	135	145	205	230	-	85	180	Ω
			-	12	100	110	155	175	-	75	135	Ω
			16	15	70	75	110	125	-	65	95	Ω
Δ_{ON} Resistance	ΔR_{ON}	Between Any Two Switches		5	-	-	-	-	-	25	-	Ω
				10	-	-	-	-	-	10	-	Ω
				12	-	-	-	-	-	8	-	Ω
				15	-	-	-	-	-	5	-	Ω
OFF Leakage Current	I_L (Max)	All Switches OFF, V_{IS} = 18V	4	18	±1000				-	±1	±100 (Note 2)	nA
STATIC CONTROLS												
Input Low Voltage	V_{IL} (Max)	OFF Switch I_L < 0.2µA		5	1.5				-	-	1.5	V
				10	3				-	-	3	V
				15	4				-	-	4	V
Input High Voltage	V_{IH} (Min)	ON Switch See R_{ON} Characteristic		5	3.5				3.5	-	-	V
				10	7				7	-	-	V
				15	11				11	-	-	V
Input Current	I_{IN} (Max)	Any Control V_{IN} = 0, 18V	2	18	±0.1	±0.1	±1	±1	-	$\pm 10^{-5}$	±0.1	µA

NOTES:

1. Maximum current through transmission gates (switches) = 25mA.
2. Determined by minimum feasible leakage measurement for automatic testing.

Electrical Specifications $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS					MIN	TYP	MAX	UNITS
		FIGURE	f_{IS} (kHz)	R_L (kΩ)	V_{IS} (V) (Note 3)	V_{DD} (V)				
DYNAMIC CROSSPOINTS										
Propagation Delay Time, (Switch ON) Signal Input to Output	t_{PHL}, t_{PLH}	5	-	-	5	5	-	30	60	ns
			-	10	10	10	-	15	30	ns
					15	15	-	10	20	ns
			C_L = 50pF; t_R , t_F = 20ns							
Frequency Response (Any Switch ON)	f_{3dB}	19	1	1	5	10	-	40	-	MHz
			Sine Wave Input, $20\log\frac{V_{OS}}{V_{IS}}$ = -3dB							
Sine Wave Response (Distortion)	THD	-	1	1	2.5	5	-	1	-	%
			1	1	5	10	-	0.25	-	%
			1	1	7.5	15	-	0.15	-	%
Feedthrough (All Switches OFF)	F_{DT}	13	1.6	0.6	2 (Note 4)	10	-	-96	-	dB
			Sine Wave Input							
Frequency for Signal Crosstalk	F_{CT}	12	-	0.6	1 (Note 4)	10				
Attenuation of 40dB			Sine Wave Input				-	2.5	-	MHz
Attenuation of 95dB								0.1		kHz
Capacitance:										
X_N to Ground	C_{IS}			-	-	-	-	25	-	pF
Y_N to Ground				-	-	-	-	60	-	pF
Feedthrough	C_{IOS}			-	-	-	-	0.6	-	pF
DYNAMIC CONTROLS										
Propagation Delay Time: High Impedance to High Level or Low Level	t_{PZH}, t_{PZL}	6	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	500	1000	ns
Strobe to Output, CD22101						10	-	230	460	ns
						15	-	170	340	ns
Data-In to Output, CD22101	t_{PZH}, t_{PZL}	7	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	515	1000	ns
						10	-	220	440	ns
						15	-	170	340	ns
K_A to Output, CD22102	t_{PZH}, t_{PZL}	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	500	1000	ns
						10	-	215	430	ns
						15	-	160	320	ns
Address to Output CD22101, CD22102	t_{PZH}, t_{PZL}	8	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	480	960	ns
						10	-	225	450	ns
						15	-	155	300	ns

Electrical Specifications $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS					MIN	TYP	MAX	UNITS
		FIGURE	f_{IS} (kHz)	R_L (kΩ)	V_{IS} (V) (Note 3)	V_{DD} (V)				
Propagation Delay Time: High Level or Low Level to High Impedance	t_{PHZ}, t_{PLZ}	6	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	450	900	ns
Strobe to Output, CD22101						10	-	200	400	ns
						15	-	135	270	ns
K_B to Output, CD22102	t_{PHZ}, t_{PLZ}	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	450	900	ns
						10	-	200	400	ns
						15	-	130	260	ns
Data-In to Output, CD22101	t_{PHZ}, t_{PLZ}	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	450	900	ns
						10	-	165	330	ns
						15	-	110	220	ns
$K_A \bullet K_B$ to Output, CD22102	t_{PHZ}, t_{PLZ}	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	280	560	ns
						10	-	130	260	ns
						15	-	90	180	ns
Address to Output CD22101, CD22102	t_{PHZ}, t_{PLZ}	8	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	425	850	ns
						10	-	190	380	ns
						15	-	130	260	ns
Minimum Strobe Pulse Width, CD22101	t_W	6	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	260	500	ns
						10	-	120	240	ns
						15	-	80	160	ns
Address to Strobe Setup or Hold Times, CD22101	t_{SU}, t_H	9	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	-160	0	ns
						10	-	-70	0	ns
						15	-	-50	0	ns
Strobe to Data-In Hold Time, CD22101	t_{HHL}, t_{HLH}	10	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	200	400	ns
						10	-	80	160	ns
						15	-	60	120	ns
Address to K_A and K_B Setup or Hold Times, CD22102	t_{SU}, t_H	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	-160	0	ns
						10	-	-70	0	ns
						15	-	-50	0	ns
Minimum $K_A \bullet K_B$ Pulse Width, CD22102	t_W	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	375	750	ns
						10	-	160	320	ns
						15	-	110	220	ns
Minimum K_A Pulse Width, CD22102	t_W	-	R_L = 1kΩ, C_L = 50pF, t_R, t_F = 20ns			5	-	425	850	ns
						10	-	175	350	ns
						15	-	120	240	ns

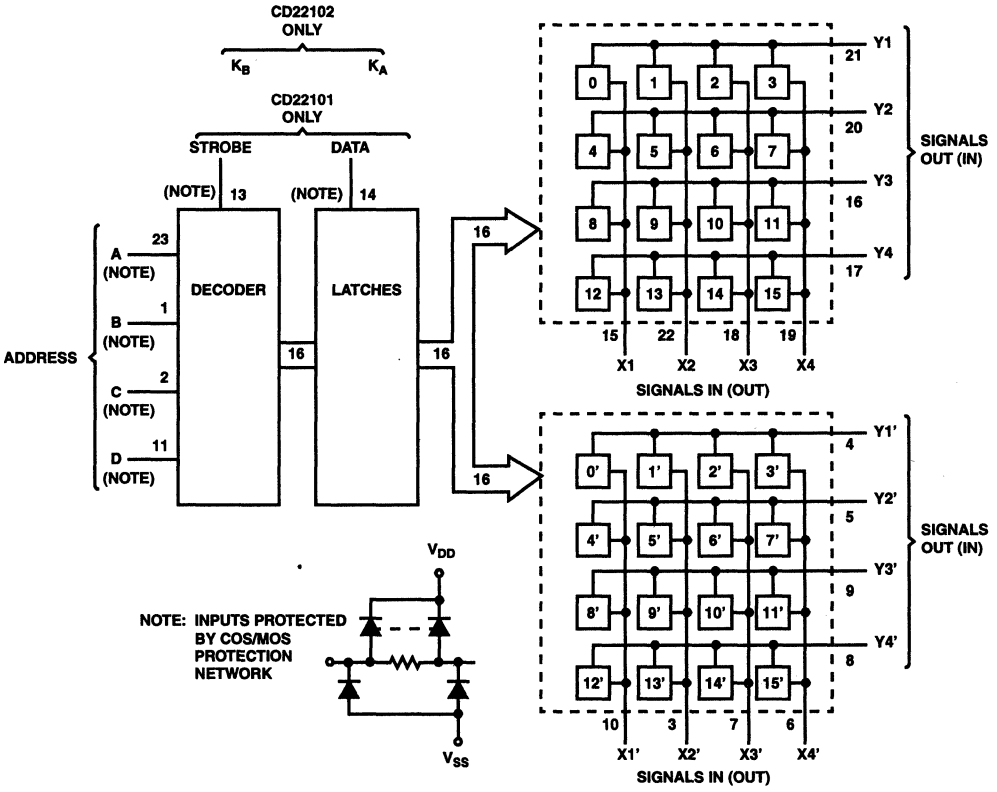
Electrical Specifications $T_A = 25^oC$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS FIGURE	f_{IS} (kHz)	R_L (kΩ)	V_{IS} (V) (Note 3)	V_{DD} (V)	MIN	TYP	MAX	UNITS
Minimum K_B Pulse Width, CD22102	t_W	-	$R_L = 1k\Omega$, $C_L = 50pF$, t_R, $t_F = 20ns$			5	-	200	400	ns
						10	-	90	180	ns
						15	-	70	140	ns
Control Crosstalk, Data-In, Address or Strobe to Output		11	100	10		5	-	75	-	mV_{PEAK}
			Square Wave Input = 5V, t_R, $t_F = 20ns$, $R_S = 1k\Omega$							
Input Capacitance	C_{IN}		Any Control Input			-	-	5	7.5	pF

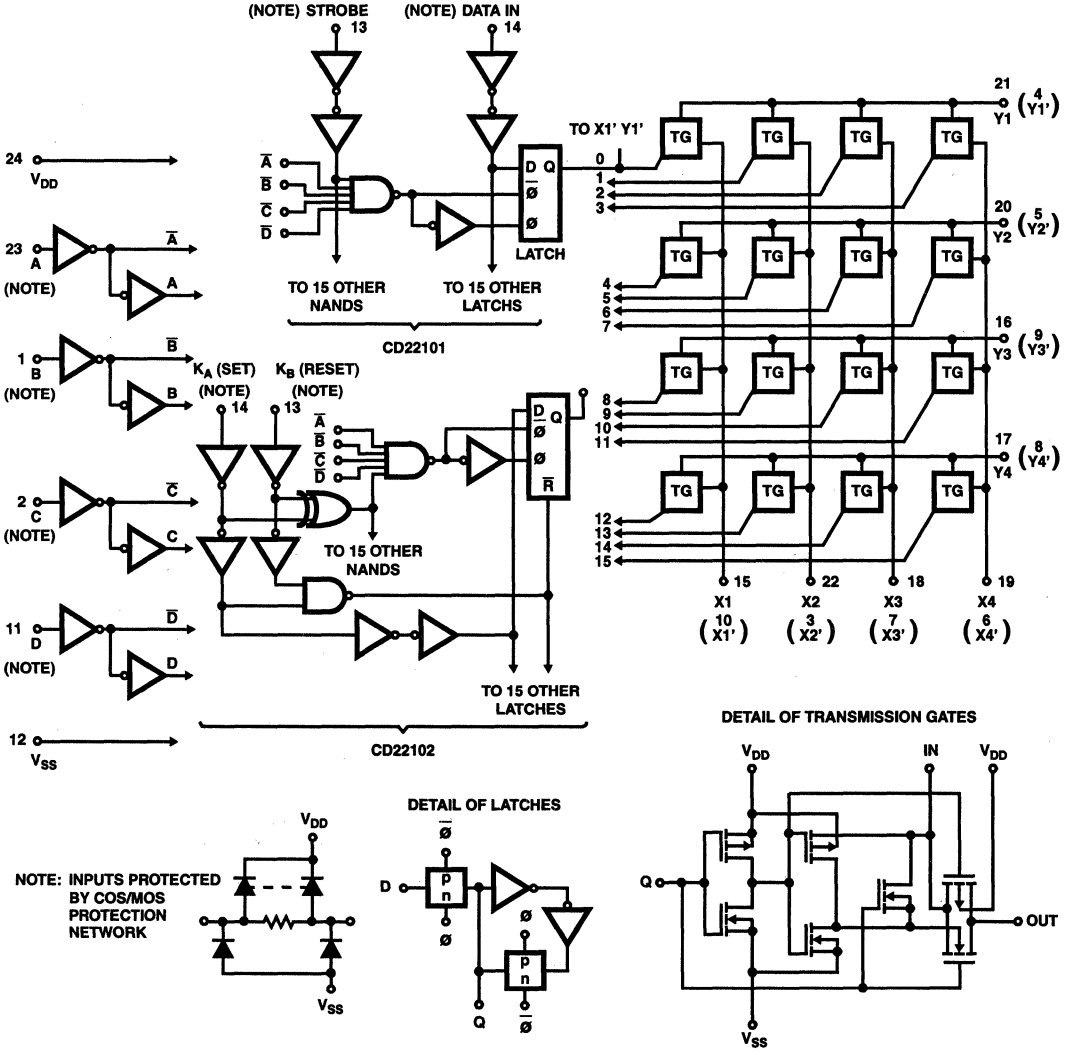
NOTES:

3. Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$, unless otherwise specified.
4. RMS.

Functional Block Diagram



Schematic Diagram



NOTE: INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

DETAIL OF LATCHES

DETAIL OF TRANSMISSION GATES

DECODER TRUTH TABLE

ADDRESS					ADDRESS				
A	B	C	D	SELECT	A	B	C	D	SELECT
0	0	0	0	X1Y1 and X1'Y1'	0	0	0	1	X1Y3 and X1'Y3'
1	0	0	0	X2Y1 and X2'Y1'	1	0	0	1	X2Y3 and X2'Y3'
0	1	0	0	X3Y1 and X3'Y1'	0	1	0	1	X3Y3 and X3'Y3'
1	1	0	0	X4Y1 and X4'Y1'	1	1	0	1	X4Y3 and X4'Y3'
0	0	1	0	X1Y2 and X1'Y2'	0	0	1	1	X1Y4 and X1'Y4'
1	0	1	0	X2Y2 and X2'Y2'	1	0	1	1	X2Y4 and X2'Y4'
0	1	1	0	X3Y2 and X3'Y2'	0	1	1	1	X3Y4 and X3'Y4'
1	1	1	0	X4Y2 and X4'Y2'	1	1	1	1	X4Y4 and X4'Y4'

CONTROL TRUTH TABLE FOR CD22101

FUNCTION	ADDRESS A	B	C	D	STROBE	DATA	SELECT
Switch ON	1	1	1	1	1	1	15 (X4Y4) and 15' (X4'Y4')
Switch OFF	1	1	1	1	1	0	15 (X4Y4) and 15' (X4'Y4')
No Change	X	X	X	X	0	X	X X X X

1 = High Level 0 = Low Level X = Don't Care

CONTROL TRUTH TABLE FOR CD22102

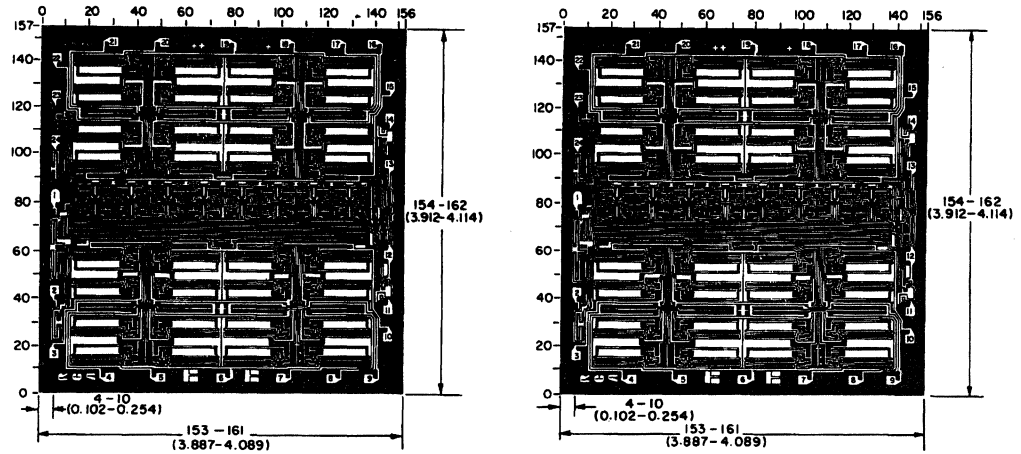
FUNCTION	ADDRESS A	B	C	D	K_A	K_B	SELECT
Switch ON	1	1	1	1	1	0	15 (X4Y4) and 15' (X4'Y4')
Switch OFF	1	1	1	1	0	1	15 (X4Y4) and 15' (X4'Y4')
All Switches OFF (Note 5)	X	X	X	X	1	1	All
No Change	X	X	X	X	0	0	X X X X

1 = High Level 0 = Low Level X = Don't Care

NOTE:

5. In the event that K_A and K_B are changed from levels 1, 1 to 0, 0 K_B should not be allowed to go to 0 before K_A, otherwise a switch which was off will inadvertently be turned on.

Metallization Mask Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Test Circuits and Waveforms

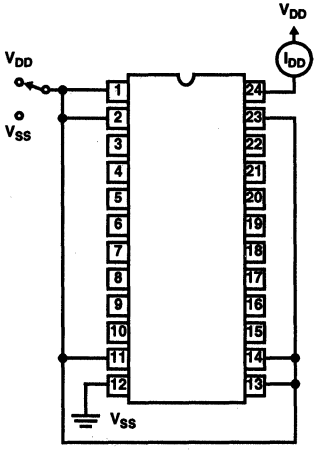
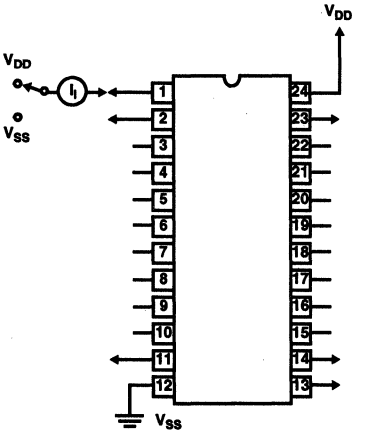
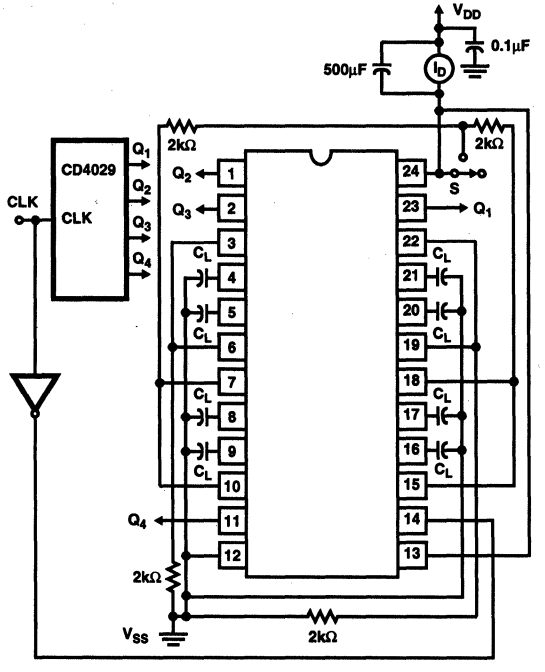


FIGURE 1. QUIESCENT CURRENT TEST CIRCUIT



MEASURE INPUTS SEQUENTIALLY TO BOTH V_{DD} AND V_{SS}
CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}

FIGURE 2. INPUT CURRENT TEST CIRCUIT



CLOSE SWITCH S AFTER APPLYING V_{DD}

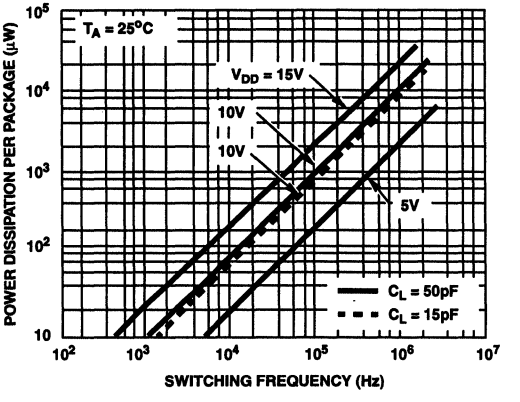


FIGURE 3. DYNAMIC POWER DISSIPATION TEST CIRCUIT FOR CD22101AND TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF SWITCHING FREQUENCY

Test Circuits and Waveforms (Continued)

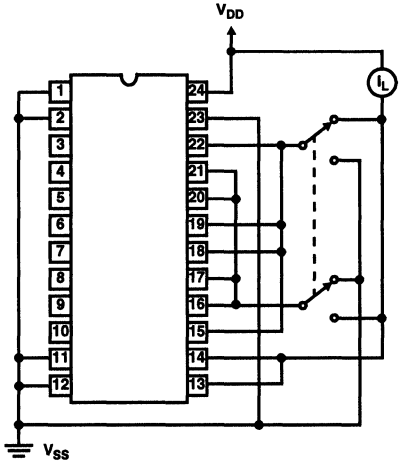


FIGURE 4. OFF SWITCH INPUT OR OUTPUT LEAKAGE CURRENT TEST CIRCUIT (16 OF 32 SWITCHES)

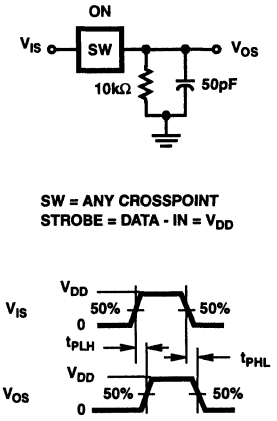


FIGURE 5. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (SIGNAL INPUT TO SIGNAL OUTPUT, SWITCH ON)

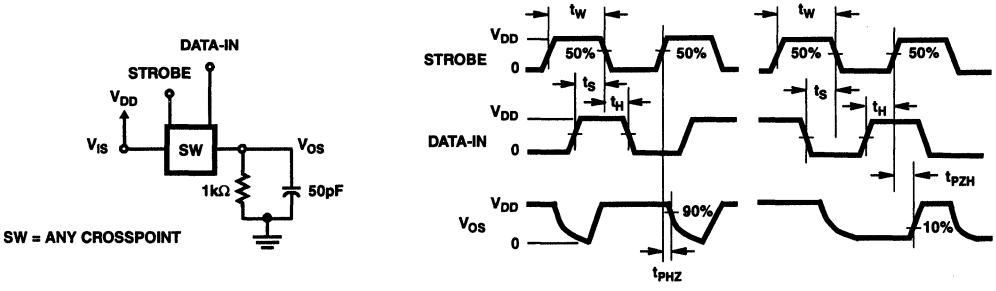


FIGURE 6. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (STROBE TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

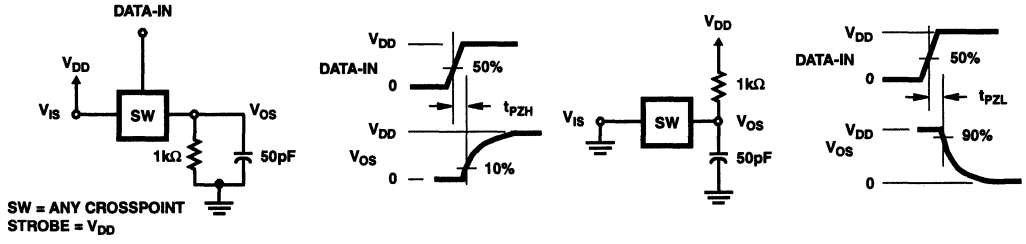


FIGURE 7. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (DATA-IN TO SIGNAL OUTPUT, SWITCH TURN-ON TO HIGH OR LOW LEVEL)

Test Circuits and Waveforms (Continued)

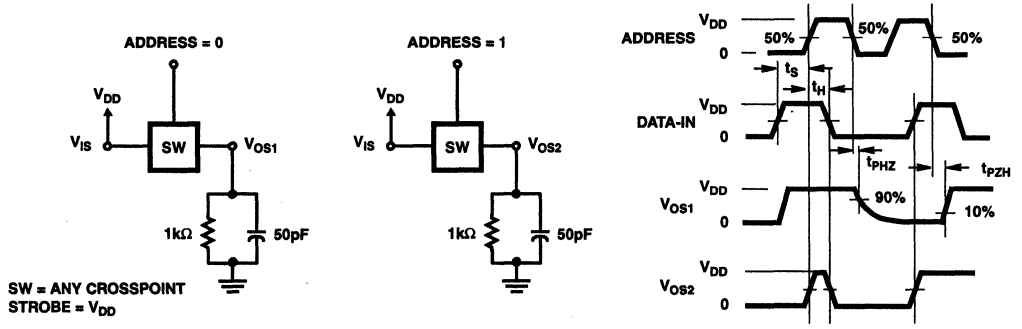
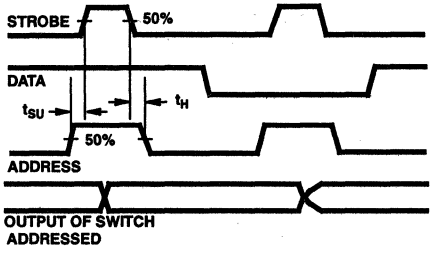
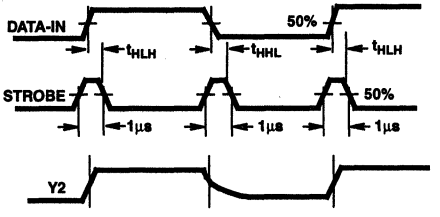


FIGURE 8. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (ADDRESS TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)



IF SETUP AND HOLD TIMES PROVIDED ARE TOO SHORT, AN UNADDRESSED SWITCH MAY BE TURNED ON OR OFF SIMULTANEOUSLY WITH THE ADDRESSED SWITCH

FIGURE 9. ADDRESS TO STROBE SETUP AND HOLD TIMES



SET ALL SWITCHES TO OFF INITIALLY APPLY VDD TO ALL X INPUTS AND RETURN ALL Y OUTPUTS TO VSS THROUGH 1kΩ. ADDRESS X1Y2 (ABCD) WITH f_{IN} = 10kHz

FIGURE 10. STROBE TO DATA-IN HOLD TIME t_H, FOR CD22101

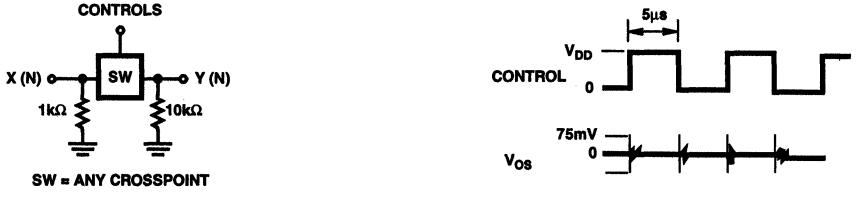


FIGURE 11. TEST CIRCUIT AND WAVEFORMS FOR CROSSTALK (CONTROL INPUT TO SIGNAL OUTPUT)

Test Circuits and Waveforms (Continued)

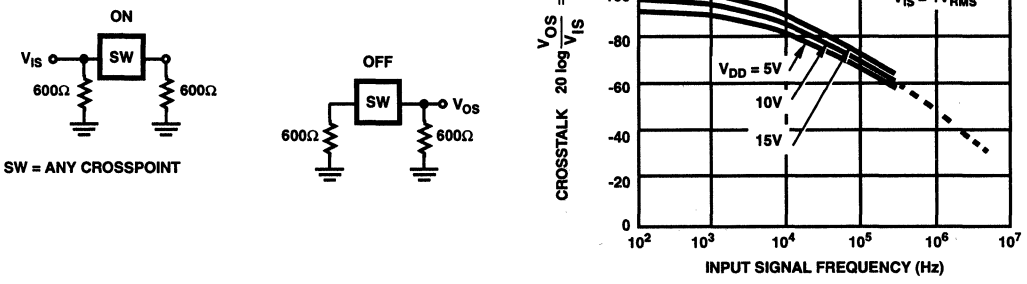


FIGURE 12. TEST CIRCUIT AND TYPICAL CROSSTALK AS A FUNCTION OF FREQUENCY BETWEEN SWITCH CIRCUITS IN THE SAME PACKAGE

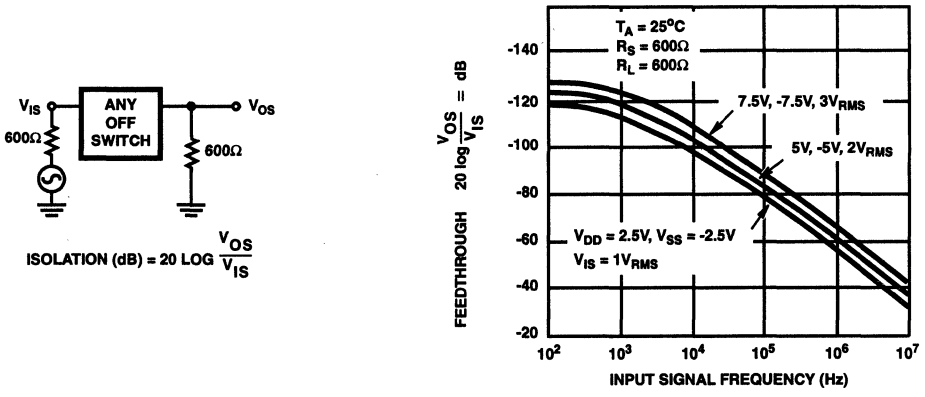


FIGURE 13. TEST CIRCUIT AND TYPICAL FEEDTHROUGH AS A FUNCTION OF FREQUENCY (ANY OFF SWITCH)

Typical Performance Curves

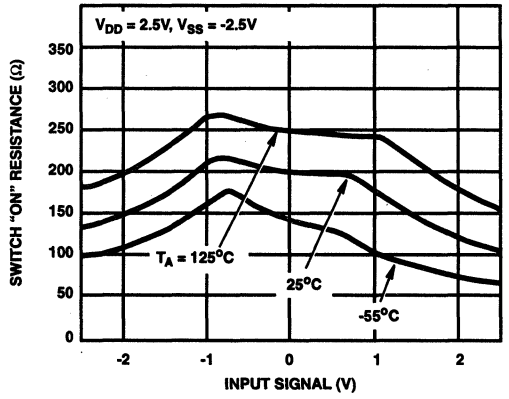


FIGURE 14. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT V_{DD} = -V_{SS} = 2.5V

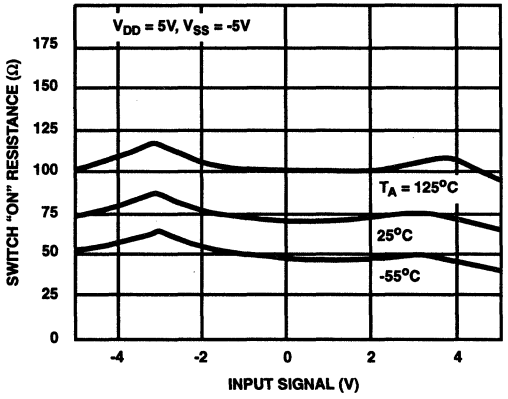


FIGURE 15. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT V_{DD} = -V_{SS} = 5V

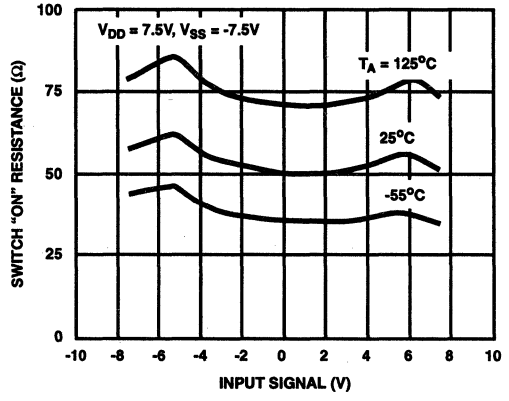


FIGURE 16. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT V_{DD} = -V_{SS} = 7.5V

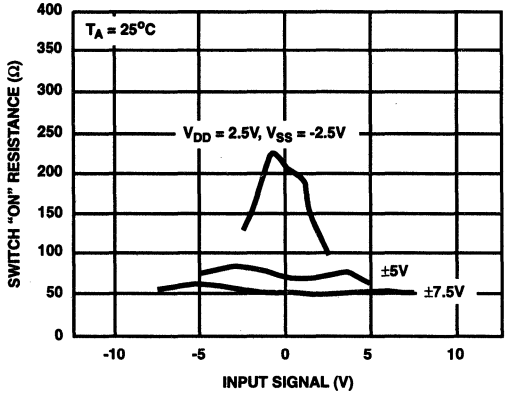


FIGURE 17. TYPICAL ON RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE AT T_A = 25°C

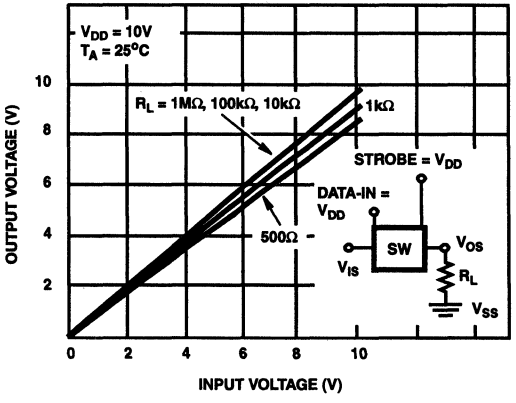


FIGURE 18. TYPICAL SWITCH ON TRANSFER CHARACTERISTICS (1 OF 16 SWITCHES)

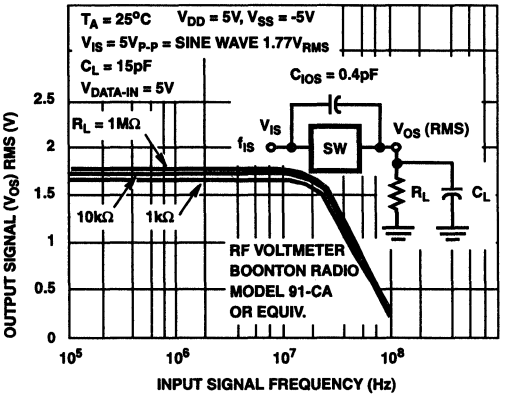


FIGURE 19. TYPICAL SWITCH ON FREQUENCY RESPONSE CHARACTERISTICS

HARRIS SEMICONDUCTOR

CD22M3493

12 x 8 x 1 BiMOS-E Crosspoint Switch

January 1997

Features

- 96 Analog Switches
- Low R_{ON}
- Guaranteed R_{ON} Matching
- Analog Signal Input Voltage Equal to the Supply Voltage
- Wide Operating Voltage. . . . . 4V to 16V
- Parallel Input Addressing
- High Latch Up Current. . . . . 50mA (Min)
- Very Low Crosstalk
- Pin and Functionally Compatible with the Following Types: SGS M3493, SGS M093, SSI 78A093A, and Mitel MT8812

Applications

- PBX Systems
- Instrumentation
- Analog and Digital Multiplexers
- Video Switching Networks

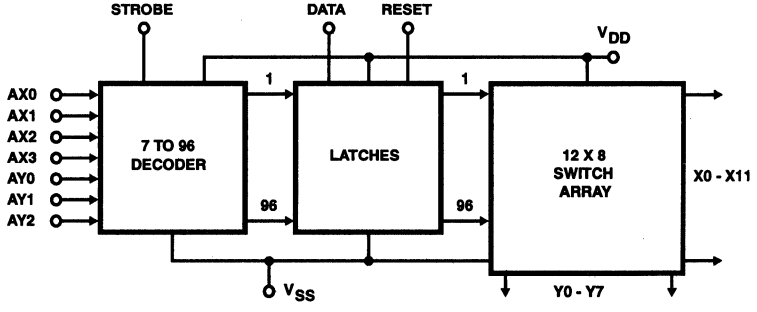
Description

The Harris CD22M3493 is an array of 96 analog switches capable of handling signals from DC to video. Because of the switch structure, input signals may swing through the total supply voltage range, V_{DD} to V_{SS}. Each of the 96 switches may be addressed via the ADDRESS input to the 7 to 96 line decoder. The state of the addressed switch is established by the signal to the DATA input. A low or logic zero input will open the switch, while a high logic level or a one will result in closure of the addressed switch when the STROBE input goes high from its normally low state. Any number or combination of connections may be active at one time. Each connection, however, must be made or broken individually in the manner previously described. All switches may be reset by taking the RESET input from a zero state to a one state and then returning it to its normal low state.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22M3493E	-40 to 85	40 Ld PDIP	E40.6
CD22M3493Q	-40 to 85	44 Ld PLCC	N44.65

Block Diagram



4 WIRED COMMUNICATIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 2491.4

Absolute Maximum Ratings

DC Supply Voltage (V_{DD}) (Referenced to VSS. . . . . -0.5V to 17V
Supply Voltage Range
For T_A = Full Package Temperature Range
V_{SS} = 0V, V_{DD} 4V to 16V
DC Input Diode Current, I_{IN}
For $V_I < V_{SS}$ -0.5V or $V_I > V_{DD}$ +0.5V. . . . . ±20mA
DC Output Diode Current, I_{OK}
For $V_O < V_{SS}$ -0.5V or $V_O > V_{DD}$ +0.5V . . . . . ±20mA
DC Transmission Gate Current. . . . . ±25mA
Power Dissipation Per Package (Po)
For T_A = -40°C to 85°C (PDIP) 500mW
For T_A = -40°C to 85°C (PLCC) 600mW

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
Plastic DIP Package 55
PLCC Package 43
Maximum Junction Temperature Plastic . . . . . 150°C
Maximum Storage Temperature Range (T_{STG}) . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A)
Package Type E and Q . . . . . -40°C to 85°C
DC Input or Output Voltage . . . . . Min = V_{SS} , Max = V_{DD}
Digital Input Voltage . . . . . Min = V_{SS} , Max = V_{DD}

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = -40°C to 85°C, V_{SS} = 0V, V_{DD} = 14V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{DD}	V_{DD} = 5V, Logic Inputs = V_{DD}	-	-	2	mA
		V_{DD} = 16V, Logic Inputs = V_{DD}	-	-	5	mA
High-Level Input Voltage	V_{IH}		2.4	-	-	V
Low-Level Input Voltage	V_{IL}		-	-	0.8	V
Input Leakage Current, Digital	I_{IN}	Reset = Low (Note 2)	-	-	±10 (Note 3)	µA

Electrical Specifications

T_A = -40°C to 85°C, V_{SS} = 0V, V_{DD} = 14V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
STATIC CROSSPOINTS							
ON Resistance	R_{ON}	T_A = 25°C, V_{IN} = V_{DD}/2, VX - VY = 0.25V	V_{DD} = 5V	-	40	70	Ω
			V_{DD} = 14V	-	22	45	Ω
ON Resistance	R_{ON}	T_A = -40°C to 85°C, V_{IN} = V_{DD}/2, VX - VY = 0.25V	V_{DD} = 5V	-	-	80	Ω
			V_{DD} = 14V	-	-	55	Ω
Difference in ON Resistance Between Any Two Switches	ΔR_{ON}	T_A = 25°C, V_{IN} = V_{DD}/2, VX - VY = 0.25V, V_{DD} = 14V		-	4	10	Ω
Difference in ON Resistance Between Any Two Switches	ΔR_{ON}	T_A = -40°C to 85°C, V_{IN} = V_{DD}/2, VX - VY = 0.25V, V_{DD} = 14V		-	-	10	Ω
OFF-State Leakage Current	I_L	|VX - VY| = 14V		-	-	±10 (Note 3)	µA

Electrical Specifications

T_A = 25°C, V_{SS} = 0V, V_{DD} = 14V, C_L = 50pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CROSSPOINTS					
Switch I/O Capacitance	V_{IN} = 7V, f = 1MHz	-	20	-	pF
Switch Feedthrough Capacitance	V_{IN} = 7V, f = 1MHz	-	0.2	-	pF
Propagation Delay Time (Switch ON) Signal Input to Output, t_{PHL} or t_{PLH}		-	30	100	ns

Electrical Specifications $T_A = 25^oC$, $V_{SS} = 0V$, $V_{DD} = 14V$, $C_L = 50pF$, Unless Otherwise Specified **(Continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Response Channel ON f = 20log (VX/VY) = -3dB		$C_L = 3pF$, $R_L = 75\Omega$, $V_{IN} = 2V_{P-P}$	-	50	-	MHz
Total Harmonic, THD		$V_{IN} = 2V_{P-P}$, f = 1kHz	-	0.01	-	%
Feedthrough Channel OFF Feedthrough = 20log (VX/VY) = F_{DT}		$V_{IN} = 2V_{P-P}$, f = 1kHz	-	-95	-	dB
Frequency for Signal Crosstalk, f_{CT} Attenuation of:	40dB	$V_{IN} = 2V_{P-P}$, $R_L = 75\Omega$	-	10	-	MHz
	110dB	$V_{IN} = 2V_{P-P}$, $R_L = 1k\Omega$ II 10pF	-	5	-	kHz
Control Crosstalk DATA-Input, ADDRESS, or STROBE to Output		Control Input = $3V_{P-P}$ Square Wave, $t_R = t_F = 10ns$ $R_{IN} = 1K$, $R_{OUT} = 10k\Omega$ II 10pF	-	75	-	mV_{PEAK}

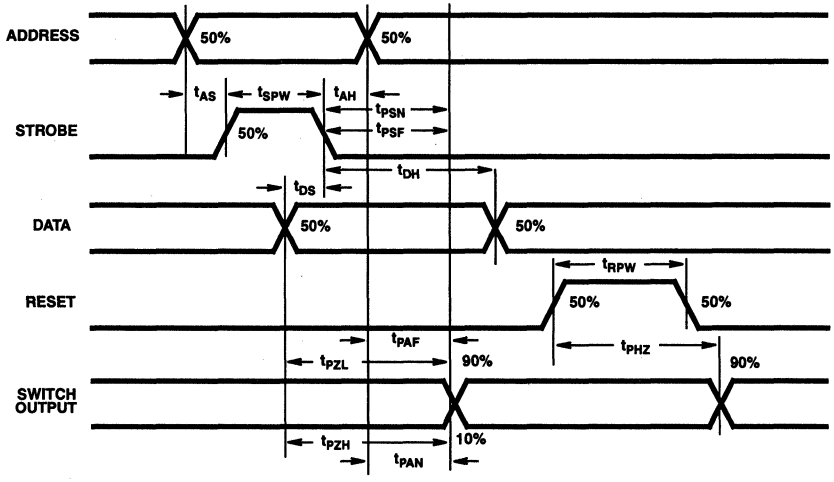
Electrical Specifications $T_A = 25^oC$, $V_{SS} = 0V$, $V_{DD} = 14V$, $R_L = 1k\Omega$ II 50pF, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CONTROLS						
Digital Input Capacitance	C_{IN}	$V_{IN} = 5V$, f = 1MHz	-	5	-	pF
Propagation Delay Time STROBE to Output						
Switch Turn-ON	t_{PSN}		-	30	100	ns
Switch Turn-OFF	t_{PSF}		-	40	100	ns
DATA-IN to Output						
Turn-ON to High Level	t_{PZH}		-	30	100	ns
Turn-ON to Low Level	t_{PZL}		-	30	100	ns
ADDRESS to Output						
Turn-ON to High Level	t_{PAN}		-	30	100	ns
Turn-OFF to Low Level	t_{PAF}		-	25	100	ns
Setup Time						
DATA-IN to STROBE	t_{DS}		20	-	-	ns
ADDRESS to STROBE	t_{AS}		20	-	-	ns
Hold Time						
STROBE to DATA-IN	t_{DH}		20	-	-	ns
STROBE to ADDRESS	t_{AH}		10	-	-	ns
Pulse Width						
STROBE	t_{SPW}		30	-	-	ns
RESET	t_{RPW}		50	-	-	ns
RESET Turn-OFF to Output Delay	t_{PHZ}		-	100	200	ns

NOTES:

2. Reset $I_{IH} < 2mA$, Reset = $V_{DD} = 16V$.
3. At 25^oC Limit is ±100nA.

Timing Diagram



TRUTH TABLE X AXIS

X ADDRESS					
AX3	AX2	AX1	AX0	NOTE	X SWITCH
0	0	0	0		X0
0	0	0	1		X1
0	0	1	0		X2
0	0	1	1		X3
0	1	0	0		X4
0	1	0	1		X5
0	1	1	0	4	No Connect
0	1	1	1	4	No Connect
1	0	0	0		X6
1	0	0	1		X7
1	0	1	0		X8
1	0	1	1		X9
1	1	0	0		X10
1	1	0	1		X11
1	1	1	0	4	No Connect
1	1	1	1	4	No Connect

NOTE: 4. When X switch addresses are in these states, no change in status will occur in switches between any X and Y points.

TRUTH TABLE Y AXIS

Y ADDRESS			
AY2	AY1	AY0	Y SWITCH
0	0	0	Y0
0	0	1	Y1
0	1	0	Y2
0	1	1	Y3
1	0	0	Y4
1	0	1	Y5
1	1	0	Y6
1	1	1	Y7

To make a connection (close switch) between any two points, specify an "X" address, a "Y" address, set "DATA" high, and switch "Strobe" from low to high. To break a connection, follow this same procedure with "DATA" low.:

Example:

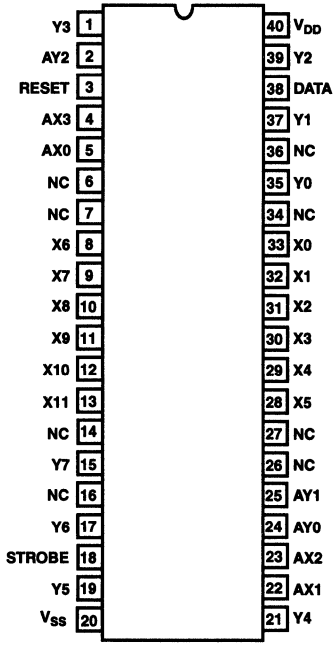
	DATA	X ADDRESS				Y ADDRESS		
		AX3	AX2	AX1	AX0	AY2	AY1	AY0
To connect switch X3 to switch Y4:	1	0	0	1	1	1	0	0
To connect switch X6 to switch Y7:	1	1	0	0	0	1	1	1
To break connection from X3 to Y4:	0	0	0	1	1	1	0	0

Pin Descriptions

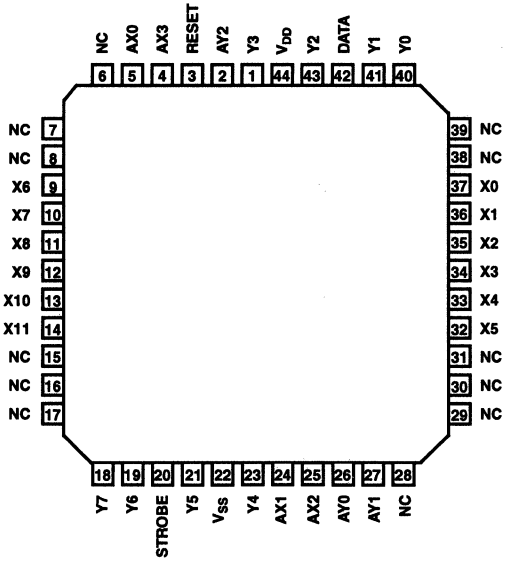
SYMBOL	40 LEAD PDIP PIN NO.	44 LEAD PLCC PIN NO.	DESCRIPTION
POWER SUPPLIES			
V_{DD}	40	44	Positive Supply
V_{SS}	20	22	Negative Supply
ADDRESS			
AX0 - AX3	5, 22, 23 and 4	5, 24, 25 and 4	X Address Lines. These pins select one of the 12 rows of switches. See the Truth Table for the valid addresses.
AY0 - AY2	24, 25 and 2	26, 27 and 2	Y Address Lines. These pins select one of the 8 columns of switches. See the Truth Table for the valid addresses.
CONTROL			
DATA	38	42	DATA Input determines the state of the addressed switch. A high or one will close the switch. A low or zero will open the switch.
STROBE	18	20	STROBE Input enables the action defined by the DATA and ADDRESS Inputs. A low or zero results in no action. The ADDRESS Input must be stable before the STROBE Input goes to the active high level. The DATA Input must be stable on the failing edge of the STROBE.
RESET	3	3	MASTER RESET. A high or one on this line opens all switches.
INPUTS/OUTPUTS			
X0 - X5 I/O X6 - X11	33 - 28 8 - 13	37 - 32 9 - 14	Analog or Digital Inputs/Outputs. These pins are the rows X0 - X11.
Y0 - Y7 I/O	35, 37, 39, 1, 21, 19, 17 and 15	40, 41, 43, 1, 23, 21, 19 and 18	Analog or Digital Inputs/Outputs. These pins are the columns Y0 - Y7.

Pinouts

CD22M3493 (PDIP)
TOP VIEW



CD22M3493 (PLCC)
TOP VIEW



HARRIS SEMICONDUCTOR

CD22M3494

16 x 8 x 1 BiMOS-E Crosspoint Switch

January 1997

Features

- 128 Analog Switches
- Low R_{ON}
- Guaranteed R_{ON} Matching
- Analog Signal Input Voltage Equal to the Supply Voltage
- Wide Operating Voltage..... 4V to 15V
- Parallel Input Addressing
- High Latch Up Current..... 50mA (Min)
- Very Low Crosstalk
- Pin and Functionally Compatible with the Following Types: SGS M3494 and Mitel MT8816

Applications

- PBX Systems
- Instrumentation
- Analog and Digital Multiplexers
- Video Switching Networks

Description

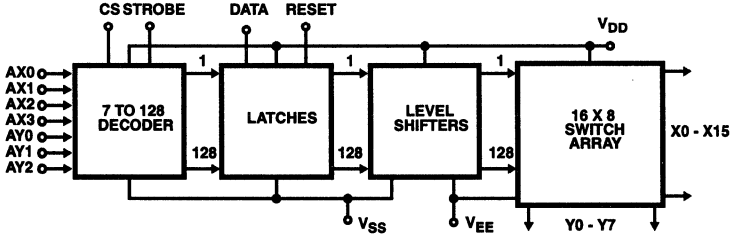
The Harris CD22M3494 is an array of 128 analog switches capable of handling signals from DC to video. Because of the switch structure, input signals may swing through the total supply voltage range, V_{DD} to V_{EE}. Each of the 128 switches may be addressed via the ADDRESS input to the 7 to 128 line decoder. The state of the addressed switch is established by the signal to the DATA input. A low or zero input will open the switch, while a high logic level or a one will result in closure of the addressed switch when the STROBE input goes high from its normally low state. Any number or combination of connections may be active at one time. Each connection, however, must be made or broken individually in the manner previously described. All switches may be reset by taking the RESET input from a zero state to a one state and then returning it to its normal low state.

CS allows crosspoint array to be cascaded for matrix expansion.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22M3494E	-40 to 85	40 Ld PDIP	E40.6
CD22M3494MQ	-40 to 85	44 Ld PLCC (Mitel Ld Compatible)	N44.65
CD22M3494SQ	-40 to 85	44 Ld PLCC (SGS Ld Compatible)	N44.65

Block Diagram



File Number 2793.5

Absolute Maximum Ratings

DC Supply Voltage (V_{DD})
Voltages Referenced to V_{EE} ..... -0.5 to 16V
DC Supply Voltage (V_{DD})
Voltages Referenced to V_{SS} ..... -0.5, 16V
DC Input Diode Current, I_{IN}
For V_I, Digital < V_{SS} -0.5V or V_I,
Analog < V_{EE} -0.5V or V_I > V_{DD} 0.5V ..... ±20mA
DC Output Diode Current, I_{OK}
For V_O, Digital < V_{SS} -0.5V or V_O,
Analog < V_{EE} -0.5V or V_O > V_{DD} 0.5V ..... ±20mA
DC Transmission Gate Current ..... ±25mA
Power Dissipation Per Package (Po)
For T_A = -40°C to 85°C (PDIP) 500mW
For T_A = 60°C to 85°C Derate Linearly ..... 12mW/°C to 200mW
For T_A = -40°C to 85°C (PLCC) 600mW

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	55
PLCC Package	43

Maximum Junction Temperature Plastic Package ..... 150°C
Maximum Storage Temperature Range (T_{STG}) ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(PLCC - Lead Tips Only)

Operating Conditions

Operating Temperature Range (T_A)
Package Type E and Q ..... -40°C to 85°C
Supply Voltage Range
For T_A = Full Package Temperature Range
V_{SS} = 0V, V_{EE} = 0V, V_{DD} ..... 4V to 15V
DC Input or Output Voltage V_I or V_O ..... V_{EE} to V_{DD}
Digital Input Voltage ..... V_{SS} to V_{DD}

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = -40°C to 85°C, V_{DD} = 5V, V_{SS} = 0V, V_{EE} = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
STATIC CONTROLS						
Supply Current	I_{DD}	V_{DD} = 5V, Logic Inputs = V_{DD}	-	-	2	mA
		V_{DD} = 15V, Logic Inputs = V_{DD}	-	-	5	mA
High-Level Input Voltage	V_{IH}	V_{DD} = 5V	2.4 (Note 2)	-	-	V
Low-Level Input Voltage	V_{IL}		-	-	0.8 (Note 2)	V
Input Leakage Current, Digital	I_{IN}	Reset = Low (Note 3)	-	-	±10 (Note 4)	µA

Electrical Specifications

T_A = -40°C to 85°C, V_{DD} = 12V, V_{SS} = 0V, V_{EE} = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
STATIC CROSSPOINTS						
ON Resistance	R_{ON}	V_{SS} = V_{EE} = 0V, T_A = 25°C, V_{IN} = V_{DD}/2, VX - VY = 0.2V, V_{DD} = 10V	-	40	75	Ω
		V_{DD} = 12V	-	36	65	Ω
ON Resistance	R_{ON}	T_A = -40°C to 85°C, V_{IN} = V_{DD}/2, VX -VY = 0.2V, V_{SS} = V_{EE} = 0V, V_{DD} = 10V	-	50	75	Ω
		V_{DD} = 12V	-	45	65	Ω
Difference in ON Resistance Between Any Two Switches	ΔR_{ON}	T_A = 25°C, V_{IN} = V_{DD}/2, VX - VY = 0.2V, V_{SS} = V_{EE} = 0V, V_{DD} = 12V	-	6	10	Ω

Electrical Specifications T_A = -40°C to 85°C, V_{DD} = 12V, V_{SS} = 0V, V_{EE} = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Difference in ON Resistance Between Any Two Switches	ΔR_{ON}	T_A = -40°C to 85°C, $V_{IN} = V_{DD}/2$, VX - VY = 0.2V, V_{DD} = 12V $V_{SS} = V_{EE}$ = 0V, VDD = 12V	-	-	10	Ω
OFF-State Leakage Current	I_L	|VX - VY| = 12V	-	-	±10 (Note 4)	µA

Electrical Specifications T_A = 25°C, V_{SS} = 0V, V_{EE} = 0V, V_{DD} = 14V, C_L = 50pF, Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CROSSPOINTS						
Switch I/O Capacitance		$V_{IN} = V_{DD}/2$, f = 1MHz	-	-	20	pF
Switch Feedthrough Capacitance		$V_{IN} = V_{DD}/2$, f = 1MHz	-	0.3	-	pF
Propagation Delay Time (Switch ON) Signal Input to Output, t_{PHL} or t_{PLH}			-	5	30	ns
Frequency Response Channel ON f = 20log (VX/VY) = -3dB		C_L = 3pF, R_L = 75Ω, $V_{IN} = 2V_{P-P}$	-	50	-	MHz
Total Harmonic, THD		$V_{IN} = 2V_{P-P}$, f = 1kHz	-	0.01	-	%
Feedthrough Channel OFF Feedthrough = 20log (VX/VY) = F_{DT}		$V_{IN} = 2V_{P-P}$, f = 1kHz	-	-95	-	dB
Frequency for Signal Crosstalk, f_{CT} Attenuation of:	40dB	$V_{IN} = 2V_{P-P}$, R_L = 75Ω	-	10	-	MHz
	110dB	$V_{IN} = 2V_{P-P}$, R_L = 1kΩ ll 10pF	-	5	-	kHz
Control Crosstalk DATA-Input, ADDRESS, or STROBE to Output		Control Input = $3V_{P-P}$ Square Wave, $t_R = t_F$ = 10ns R_{IN} = 1K, R_{OUT} = 10kΩ ll 10pF	-	75	-	mV_{PEAK}

Electrical Specifications T_A = 25°C, V_{SS} = 0V, V_{EE} = 0V, V_{DD} = 14V, R_L = 1kΩ ll 50pF, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CONTROLS						
Digital Input Capacitance	C_{IN}	V_{IN} = 5V, f = 1MHz	-	5	-	pF
Propagation Delay Time STROBE to Output						
Switch Turn-ON	t_{PSN}		-	50	100	ns
Switch Turn-OFF	t_{PSF}		-	50	100	ns
DATA-IN to Output						
Turn-ON to High Level	t_{PZH}		-	60	100	ns
Turn-ON to Low Level	t_{PZL}		-	70	100	ns
ADDRESS to Output						
Turn-ON to High Level	t_{PAN}		-	70	-	ns
Turn-OFF to Low Level	t_{PAF}		-	70	-	ns

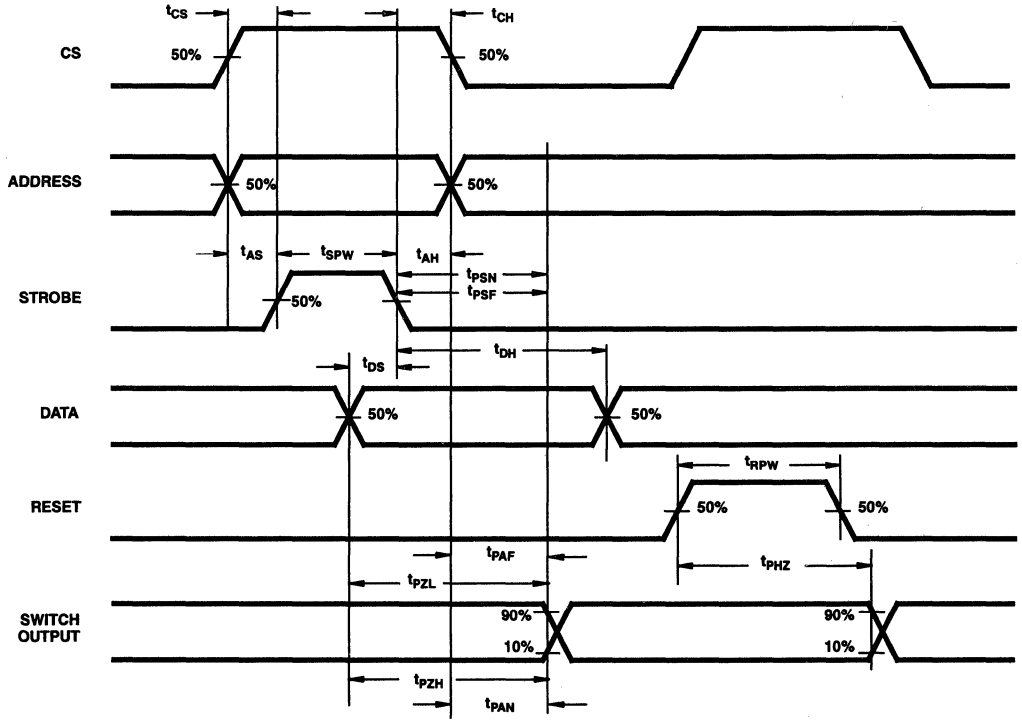
Electrical Specifications $T_A = 25^oC$, $V_{SS} = 0V$, $V_{EE} = 0V$, $V_{DD} = 14V$, $R_L = 1k\Omega$ II 50pF, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time						
CS to STROBE	t_{CS}		10	-	-	ns
DATA-IN to STROBE	t_{DS}		10	-	-	ns
ADDRESS to STROBE	t_{AS}		10	-	-	ns
Hold Time						
STROBE to CS	t_{CH}		10	-	-	ns
ADDRESS to CS			10	-	-	ns
STROBE to DATA-IN	t_{DH}		20	-	-	ns
STROBE to ADDRESS	t_{AH}		10	-	-	ns
DATA-IN to CS			20	-	-	ns
Pulse Width						
STROBE	t_{SPW}		20	-	-	ns
RESET	t_{RPW}		20	-	-	ns
RESET Turn-OFF to Output Delay	t_{PHZ}		-	70	100	ns

NOTES:

2. Operation of V_{IH} at 2.4V or V_{IL} at 0.8V will result in much higher supply current (I_{DD}) than for logic inputs equal to V_{DD} or V_{SS} respectively.
3. Reset $I_{IH} < 20\mu A$, Reset = V_{IH}.
4. At 25^oC Limit is $\pm 100nA$.

Timing Diagram



TRUTH TABLE X AXIS

X ADDRESS				
AX3	AX2	AX1	AX0	X SWITCH
0	0	0	0	X0
0	0	0	1	X1
0	0	1	0	X2
0	0	1	1	X3
0	1	0	0	X4
0	1	0	1	X5
0	1	1	0	X12
0	1	1	1	X13
1	0	0	0	X6
1	0	0	1	X7
1	0	1	0	X8
1	0	1	1	X9
1	1	0	0	X10
1	1	0	1	X11
1	1	1	0	X14
1	1	1	1	X15

TRUTH TABLE Y AXIS

Y ADDRESS			
AY2	AY1	AY0	Y SWITCH
0	0	0	Y0
0	0	1	Y1
0	1	0	Y2
0	1	1	Y3
1	0	0	Y4
1	0	1	Y5
1	1	0	Y6
1	1	1	Y7

To make a connection (close switch) between any two points, specify an "X" address, a "Y" address, set "DATA" high, and switch "STROBE" from low to high. To break a connection, follow this same procedure with "DATA" low.

Example:

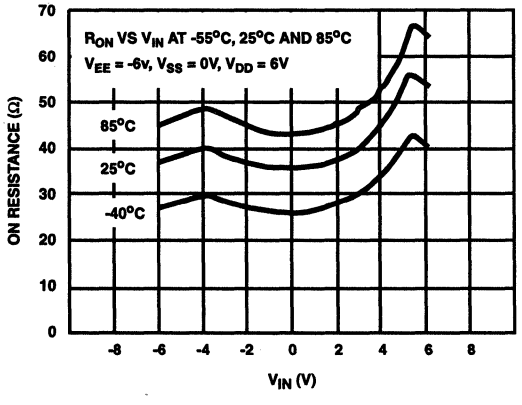
To connect switch X3 to switch Y4:

To connect switch X6 to switch Y7:

To break connection from X3 to Y4:

	X ADDRESS				Y ADDRESS		
DATA	AX3	AX2	AX1	AX0	AY2	AY1	AY0
1	0	0	1	1	1	0	0
1	1	0	0	0	1	1	1
0	0	0	1	1	1	0	0

Typical Performance Curve

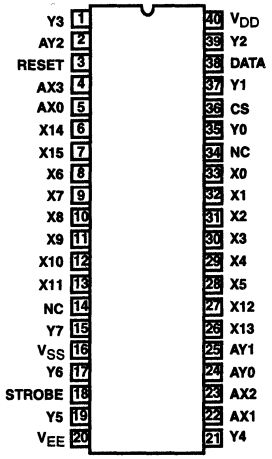


Pin Descriptions

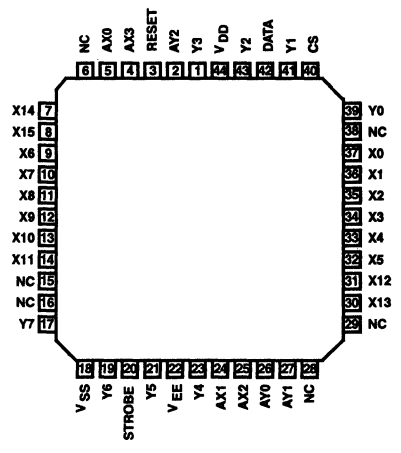
SYMBOL	40 LEAD PDIP PIN NO.	44 LEAD PLCC PIN NO. MQ	44 LEAD PLCC PIN NO. SQ	DESCRIPTION
POWER SUPPLIES				
V_{DD}	40	44	44	Positive Supply
V_{SS}	16	18	17	Negative Supply (Digital)
V_{EE}	20	22	22	Negative Supply (Analog)
ADDRESS				
AX0 - AX3	5, 22, 23 and 4	5, 24, 25 and 4		X Address Lines. These pins select one of the 16 rows of switches. See the Truth Table for the valid addresses.
AY0 - AY2	24, 25 and 2	26, 27 and 2		Y Address Lines. These pins select one of the 8 columns of switches. See the Truth Table for the valid addresses.
CONTROL				
DATA	38	42		DATA Input determines the state of the addressed switch. A high or one will close the switch. A low or zero will open the switch.
STROBE	18	20		STROBE Input enables the action defined by the DATA and ADDRESS Inputs. A low or zero results in no action. The ADDRESS Input must be stable before the STROBE Input goes to the active high level. The DATA Input must be stable on the failing edge of the STROBE.
RESET	3	3		MASTER RESET. A high or one on this line opens all switches.
CS	36	40	39	CHIP SELECT. Device is selected when CS is at a high level, allows the crosspoint array to be cascaded for matrix expansion.
INPUTS/OUTPUTS				
X0 - X5 X6 - X11 X12 - X15	33 - 28, 8 - 13, 27, 26, 6, 7	37 - 32 9 - 14, 31, 30, 7, 8		Analog or Digital Inputs/Outputs. These pins are the rows X0 - X15.
Y0 - Y7 I/O	35, 37, 39, 1, 21, 19, 17 and 15	40, 41, 43, 1, 23, 21, 19 and 18		Analog or Digital Inputs/Outputs. These pins are the columns Y0 - Y7.

Pinouts

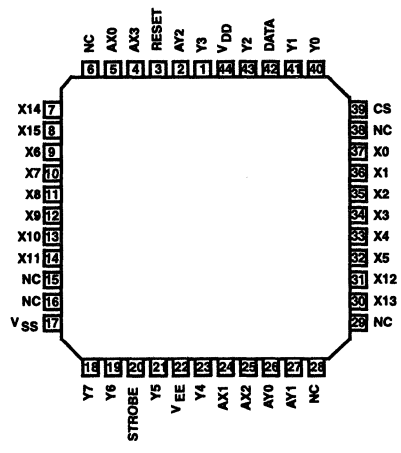
CD22M3494E
(PDIP)
TOP VIEW



CD22M3494MQ
(PLCC) (MITEL LEAD COMPATIBLE)
TOP VIEW



CD22M3494SQ
(PLCC) (SGS LEAD COMPATIBLE)
TOP VIEW



HARRIS SEMICONDUCTOR

CD74HC22106, CD74HCT22106

QMOS 8 x 8 x 1 Crosspoint Switches with Memory Control

January 1997

Features

- 64 Analog Switches in an 8 x 8 x 1 Array
- On-Chip Line Decoder and Control Latches
- Automatic Power-Up Reset by Using a 0.1μF Capacitor at the MR Pin
- R_{ON} Resistanced 95Ω at V_{CC} = 4.5V
- Analog Signal Capability: $V_{DD}/2$
- Wide Operating Temp. Range: -40°C to 85°C

Family Features

- CD74HC Types
  - 2V to 10V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{DD}; at V_{DD} = 5V and 10V
- CD74HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility: V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS Input Compatibility: $I_I < 1\mu A$ at V_{OL}, V_{OH}

Description

The CD74HC22106 and CD74HCT22106 are digitally controlled analog switches which utilize silicon-gate CMOS technology. The CD74HC22106 type features CMOS input-voltage-level compatibility and the CD74HCT22106 features LSTTL input-voltage-level compatibility.

The Master Reset has an internal pull-up resistor and is normally used with a 0.1μF capacitor. During power up all switches are automatically reset. The crosspoint switches will reset with MR = 0 even if CE is high. A 6-bit address through a 6 line to 64 line decoder selects the transmission gate which can be turned on by applying a logic ONE to the DATA input and logic ZERO to the STROBE. Similarly, any transmission gate can be turned OFF by applying a logic ZERO to the DATA input while strobing the STROBE with a logic ZERO.

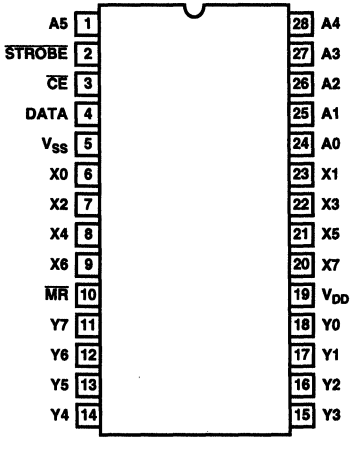
The CE pin allows the crosspoint array to be cascaded for matrix expansion in both the X and Y directions.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC22106E	-40 to 85	28 Ld PDIP	E28.6
CD74HCT22106E	-40 to 85	28 Ld PDIP	E28.6

Pinout

CD74HC22106, CD74HCT22106
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 1719.3

Absolute Maximum Ratings

DC Supply Voltage (V_{DD})
Voltage Reference to V_{SS} Terminal. . . . . -0.5V to 11V
DC Input Diode Current
I_{IK} (for V_I < -0.5 or V_I > V_{DD} 0.5V. . . . . ±20mA
DC Output Diode Current
I_{OK} (For V_O < -0.5 or V_O > V_{DD} 0.5V. . . . . ±20mA
DC Transmission Gate Current . . . . . ±25mA
Power Dissipation per Package (P_D)
For T_A = -40°C to 60°C (Package Type E) 500mW
For T_A = -60°C to 85°C (Package Type E) . . . . . Derate Linearily at 12mW/°C to 200mW

Thermal Information

Maximum Junction Temperature . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C ≤T_A ≤150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Temperature Range (T_A)
Package Type E . . . . . -40°C to 85°C
Supply Voltage Range (for T_A = Full Package Temp. Range) V_{DD}
CD74HC22106 . . . . . 2V to 10V
CD74HCT22106 . . . . . 4.5V to 5.5V
DC Input or Output Voltage V_I, V_O . . . . . 0V to V_{DD}

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{SS} = GND

PARAMETER	CD74HC22106 TEST CONDITIONS V_{IS} (V)	CD74HC22106 TEST CONDITIONS V_{DD} (V)	CD74HC22106 25°C MIN	CD74HC22106 25°C TYP	CD74HC22106 25°C MAX	CD74HC22106 -40°C to 85°C MIN	CD74HC22106 -40°C to 85°C MAX	CD74HCT22106 TEST CONDITIONS V_{IS} (V)	CD74HCT22106 TEST CONDITIONS V_{DD} (V)	CD74HCT22106 25°C MIN	CD74HCT22106 25°C TYP	CD74HCT22106 25°C MAX	CD74HCT22106 -40°C to 85°C MIN	CD74HCT22106 -40°C to 85°C MAX	UNITS
STATIC SPECIFICATIONS															
High-Level Input Voltage V_{IH}	-	2	1.5	-	-	1.5	-	-	4.5 to 5.5	2	-	-	2	-	V
	-	4.5	3.15	-	-	3.5	-	-							
	-	9	6.3	-	-	6.3	-	-							
Low-Level Input Voltage V_{IL}	-	2	-	-	0.5	-	0.5	-	4.5 to 5.5	-	-	0.8	-	0.8	V
	-	4.5	-	-	1.35	-	1.35	-							
	-	9	-	-	2.7	-	2.7	-							
Input Leakage Current (Any Control) I_L	V_{DD} or GND	10	-	-	±0.1	-	±1	Any Voltage Between V_{DD} and GND	5.5	-	-	±0.1	-	±1	µA
Quiescent Device Current, I_{CC} (with $\overline{MR}$ = 1)	V_{DD} or GND	10	-	-	5	-	50	V_{DD} or GND	5.5	-	-	2	-	20	µA
Off Leakage Current, I_L (with $\overline{MR}$ = 1)	All Switches OFF	10	-	-	0.1	-	1	-	5.5	-	-	0.1	-	1	µA
"On" Resistance R_{ON}	V_{DD} to GND Figures 8, 9	2	-	470	700	-	875	Figure 8	4.5	-	64	95	-	120	Ω
		4.5	-	64	95	-	120								
		9	-	45	70	-	90								
	V_{DD}/2	-	-	-	-	-	-	-	4.5	-	58	85	-	110	Ω
		4.5	-	58	85	-	110								
		9	-	40	60	-	80								
"On" Resistance Between Any Two Channels ΔR_{ON}	V_{DD} to GND	-	-	-	-	-	-	V_{DD} to GND	4.5	-	25	-	-	-	Ω
		4.5	-	25	-	-	-								
		9	-	23	-	-	-								

4 WIRED COMMUNICATIONS

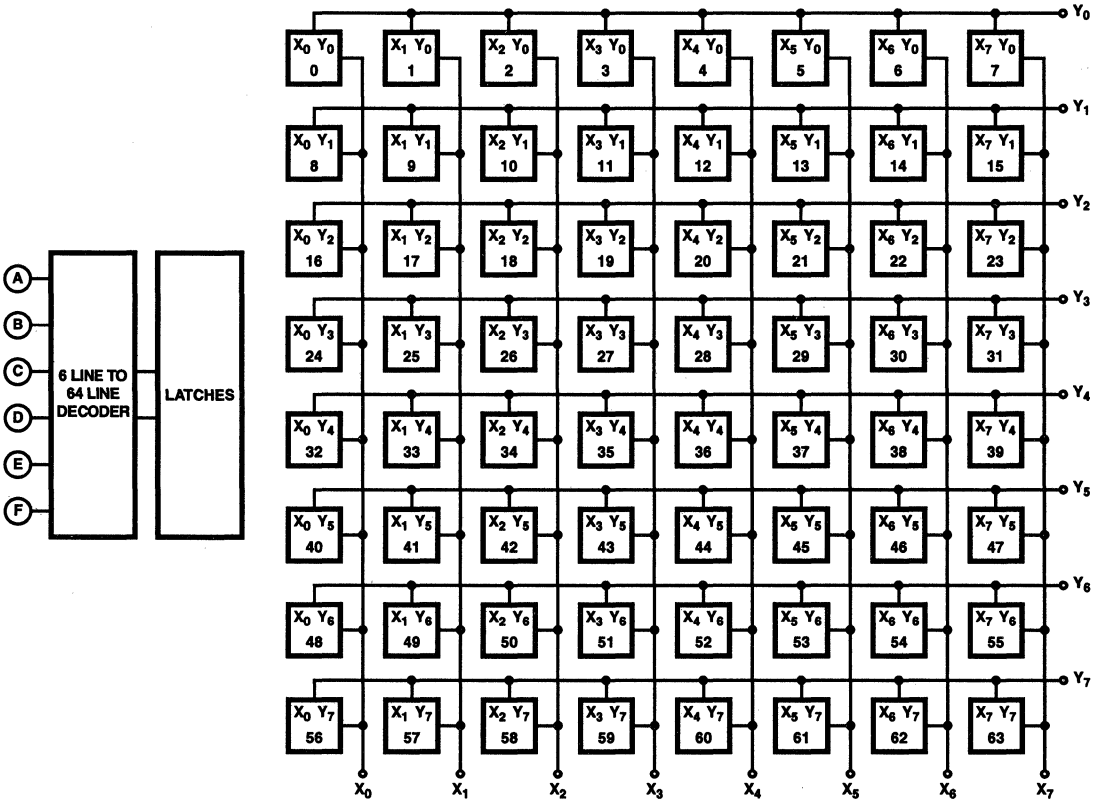
Electrical Specifications V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	FIG.	V_{DD} (V)	25°C HC MIN	25°C HC MAX	25°C HCT MIN	25°C HCT MAX	-40°C to 85°C HC MIN	-40°C to 85°C HC MAX	-40°C to 85°C HCT MIN	-40°C to 85°C HCT MAX	UNITS
DYNAMIC CONTROLS													
Propagation Delay Time: Strobe to Output (Switch Turn-On to High Level)	t_{PZH}	R_L = 10kΩ, C_L = 50pF, t_R, t_F = 6ns	1	2	-	370	-	-	-	385	-	-	ns
				4.5	-	110	-	120	-	125	-	135	ns
				9	-	65	-	-	-	70	-	-	ns
Data-In to Output (Turn-On to High Level)	t_{PZH}		2	2	-	240	-	-	-	255	-	-	ns
				4.5	-	75	-	85	-	85	-	95	ns
				9	-	50	-	-	-	55	-	-	ns
Address to Output (Turn-On to High Level)	t_{PZH}		3	2	-	380	-	-	-	400	-	-	ns
				4.5	-	110	-	120	-	125	-	135	ns
				9	-	65	-	-	-	75	-	-	ns
Propagation Delay Time: Strobe to Output Switch Turn-Off	t_{PHZ}		1	2	-	400	-	-	-	420	-	-	ns
				4.5	-	135	-	150	-	155	-	170	ns
				9	-	90	-	-	-	100	-	-	ns
Data-In to Output (Turn-On to Low Level)	t_{PZL}		2	2	-	240	-	-	-	255	-	-	ns
				4.5	-	75	-	85	-	85	-	95	ns
				9	-	50	-	-	-	55	-	-	ns
Address to Output (Turn-Off)	t_{PHZ}		3	2	-	420	-	-	-	440	-	-	ns
				4.5	-	140	-	150	-	155	-	170	ns
				9	-	95	-	-	-	100	-	-	ns
Minimum Setup Time (Data-In to Strobe, Address to Strobe)	t_{SU}		-	2	35	-	-	-	40	-	-	-	ns
				4.5	20	-	20	-	20	-	20	-	ns
				9	15	-	-	-	15	-	-	-	ns
Minimum Hold Time (Data-In to Strobe, Address to Strobe)	t_H		-	2	85	-	-	-	90	-	-	-	ns
				4.5	25	-	25	-	25	-	25	-	ns
				9	20	-	-	-	20	-	-	-	ns
Minimum Strobe Pulse Width	t_W		-	2	200	-	-	-	210	-	-	-	ns
				4.5	45	-	55	-	55	-	65	-	ns
				9	25	-	-	-	30	-	-	-	ns
Maximum Switching Frequency	F_O		-	2	0.7	-	-	-	0.6	-	-	-	MHz
				4.5	3.0	-	2.8	-	2.8	-	2.6	-	MHz
				9	7	-	-	-	6.5	-	-	-	MHz
Input (Control) Capacitance	C_I		-	-	-	10	-	10	-	10	-	10	pF

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	V_{IS} (V_{P-P})	V_{SS} (V)	V_{DD} (V)	25°C				-40°C to 85°C				UNITS
						HC		HCT		HC		HCT		
						MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
DYNAMIC SPECIFICATIONS														
Propagation Delay Time, Signal Input to Output	t_{PLH}, t_{PHL}	R_L = 10kΩ, C_L = 50pF, t_R, t_F = 6ns	-	0	2	-	30	-	-	-	33	-	-	ns
			-	0	4.5	-	20	-	20	-	22	-	22	ns
			-	-	9	-	15	-	-	-	17	-	-	ns
						HC Typical		HCT Typical						
Switch Frequency Response at -3dB	f_{3dB}	R_S = R_L = 600Ω	2	-2.25	2.25	5		5		-	-	-	-	MHz
			2	-4.5	4.5	6		6		-	-	-	-	MHz
Crosstalk Between Any Two Channels	F_{CT}	R_S = R_L = 600Ω, f = 1kHz	2	-2.25	2.25	-110		-110		-	-	-	-	dB
		R_S = R_L = 600Ω, f = 1MHz	2	-2.25	2.25	-53		-53		-	-	-	-	dB
			2	-4.5	4.5	-55		-55		-	-	-	-	dB
Switch "OFF" -40dB Feed Through Frequency	F_{DT}	R_S = R_L = 600Ω	2	-2.25	2.25	7		7		-	-	-	-	MHz
			2	-4.5	4.5	8		8		-	-	-	-	MHz
Total Harmonic Distortion	THD	R_L = 10kΩ, f = 1kHz sine-wave	4	-2.25	2.25	0.05		0.05		-	-	-	-	%
			8	-4.5	4.5	0.05		0.05		-	-	-	-	%
		R_L = 600Ω, f = 1kHz sinewave	4	-2.25	2.25	0.25		0.25		-	-	-	-	%
			7	-4.5	4.5	0.12		0.12		-	-	-	-	%
Control to Switch Feed-Through Noise (DATA IN, Strobe, Address)		R_L = 10kΩ, t_R, t_F = 6ns	V_{DD}	0	5	35		35		-	-	-	-	mV
			V_{DD}	0	10	65		65		-	-	-	-	mV
Capacitance, Xn to GND	C_{IS}	f = 1MHz	-	0	10	48		48		-	-	-	-	pF
Yn to GND			-	0	10	44		44		-	-	-	-	pF

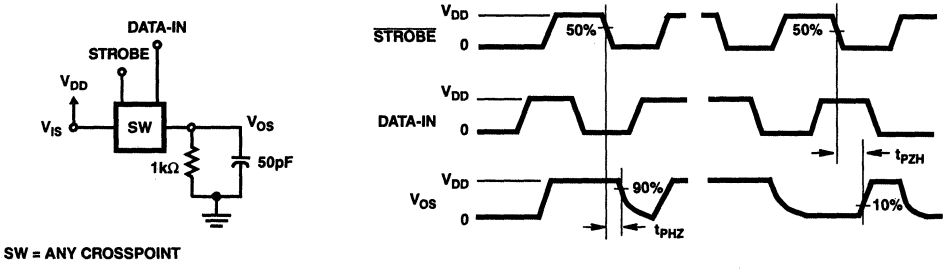
Functional Diagram



TRUTH TABLE

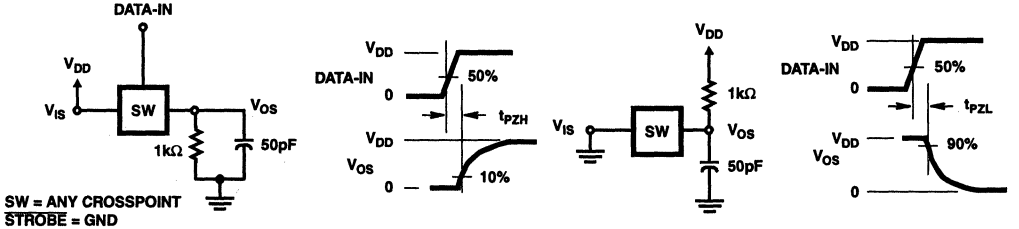
A_5	A_4	A_3	A_2	A_1	A_0	SWITCH SELECT	A_5	A_4	A_3	A_2	A_1	A_0	SWITCH SELECT
0	0	0	0	0	0	X_0 Y_0	1	0	0	0	0	0	X_0 Y_4
0	0	0	0	0	1	X_1 Y_0	1	0	0	0	0	1	X_1 Y_4
0	0	0	0	1	0	X_2 Y_0	1	0	0	0	1	0	X_2 Y_4
0	0	0	0	1	1	X_3 Y_0	1	0	0	0	1	1	X_3 Y_4
0	0	0	1	0	0	X_4 Y_0	1	0	0	1	0	0	X_4 Y_4
0	0	0	1	0	1	X_5 Y_0	1	0	0	1	0	1	X_5 Y_4
0	0	0	1	1	0	X_6 Y_0	1	0	0	1	1	0	X_6 Y_4
0	0	0	1	1	1	X_7 Y_0	1	0	0	1	1	1	X_7 Y_4
0	0	1	0	0	0	X_0 Y_1	1	0	1	0	0	0	X_0 Y_5
0	0	1	0	0	1	X_1 Y_1	1	0	1	0	0	1	X_1 Y_5
0	0	1	0	1	0	X_2 Y_1	1	0	1	0	1	0	X_2 Y_5
0	0	1	0	1	1	X_3 Y_1	1	0	1	0	1	1	X_3 Y_5
0	0	1	1	0	0	X_4 Y_1	1	0	1	1	0	0	X_4 Y_5
0	0	1	1	0	1	X_5 Y_1	1	0	1	1	0	1	X_5 Y_5
0	0	1	1	1	0	X_6 Y_1	1	0	1	1	1	0	X_6 Y_5
0	0	1	1	1	1	X_7 Y_1	1	0	1	1	1	1	X_7 Y_5
0	1	0	0	0	0	X_0 Y_2	1	1	0	0	0	0	X_0 Y_6
0	1	0	0	0	1	X_1 Y_2	1	1	0	0	0	1	X_1 Y_6
0	1	0	0	1	0	X_2 Y_2	1	1	0	0	1	0	X_2 Y_6
0	1	0	0	1	1	X_3 Y_2	1	1	0	0	1	1	X_3 Y_6
0	1	0	1	0	0	X_4 Y_2	1	1	0	1	0	0	X_4 Y_6
0	1	0	1	0	1	X_5 Y_2	1	1	0	1	0	1	X_5 Y_6
0	1	0	1	1	0	X_6 Y_2	1	1	0	1	1	0	X_6 Y_6
0	1	0	1	1	1	X_7 Y_2	1	1	0	1	1	1	X_7 Y_6
0	1	1	0	0	0	X_0 Y_3	1	1	1	0	0	0	X_0 Y_7
0	1	1	0	0	1	X_1 Y_3	1	1	1	0	0	1	X_1 Y_7
0	1	1	0	1	0	X_2 Y_3	1	1	1	0	1	0	X_2 Y_7
0	1	1	0	1	1	X_3 Y_3	1	1	1	0	1	1	X_3 Y_7
0	1	1	1	0	0	X_4 Y_3	1	1	1	1	0	0	X_4 Y_7
0	1	1	1	0	1	X_5 Y_3	1	1	1	1	0	1	X_5 Y_7
0	1	1	1	1	0	X_6 Y_3	1	1	1	1	1	0	X_6 Y_7
0	1	1	1	1	1	X_7 Y_3	1	1	1	1	1	1	X_7 Y_7

Test Circuits and Waveforms



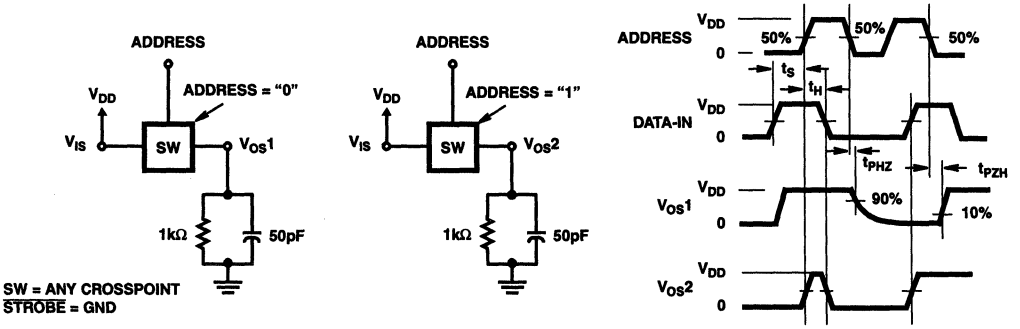
SW = ANY CROSSPOINT

FIGURE 1. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (STROBE TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-0FF)



SW = ANY CROSSPOINT
$\overline{STROBE}$ = GND

FIGURE 2. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (DATA-IN TO SIGNAL OUTPUT, SWITCH TURN-ON TO HIGH OR LOW LEVEL)



SW = ANY CROSSPOINT
$\overline{STROBE}$ = GND

FIGURE 3. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (ADDRESS TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-0FF)

Typical Application Information

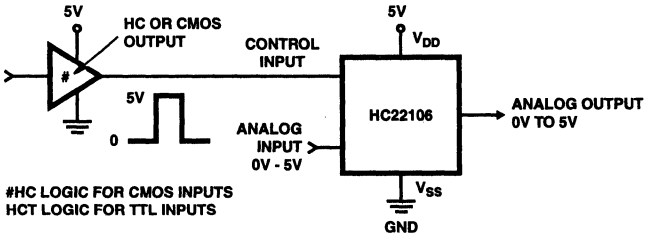


FIGURE 4. TYPICAL SINGLE SUPPLY CONNECTION FOR HC22106

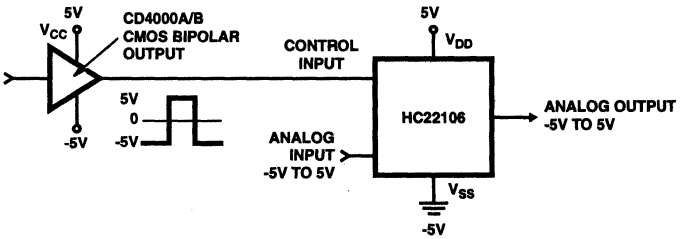
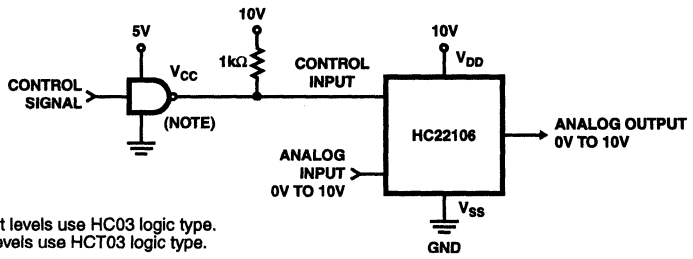


FIGURE 5. TYPICAL DUAL SUPPLY CONNECTION FOR HC22106



NOTE: For CMOS input levels use HC03 logic type.
For TTL input levels use HCT03 logic type.

FIGURE 6. USE OF HC/HCT03 WHEN CONTROL IS 0V TO 5V AND ANALOG SIGNAL IS 0V TO 10V

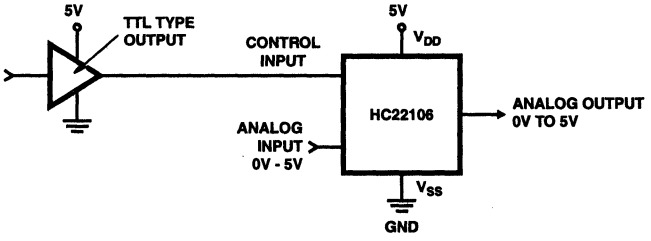


FIGURE 7. TYPICAL SINGLE SUPPLY CONNECTION FOR HCT22106 WITH TTL INPUT

Typical Performance Curves

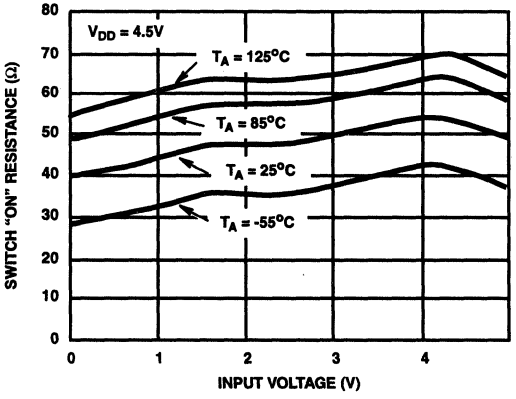


FIGURE 8. TYPICAL "ON" RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE vs TEMPERATURE

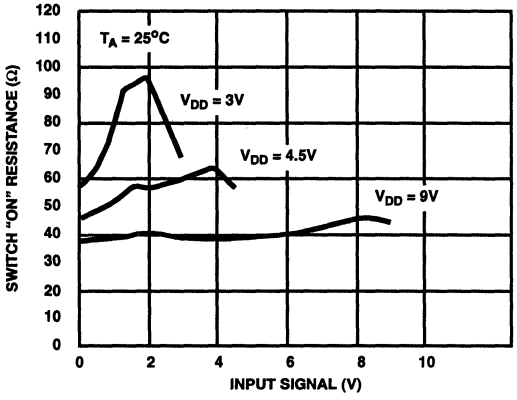


FIGURE 9. TYPICAL "ON" RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE vs V_{DD}

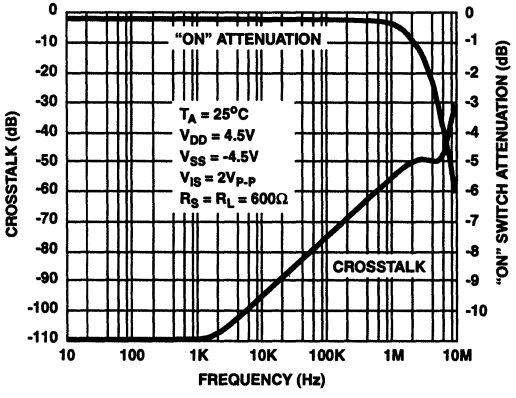


FIGURE 10. TYPICAL "ON" SWITCH ATTENUATION AND CROSSTALK AS A FUNCTION OF FREQUENCY

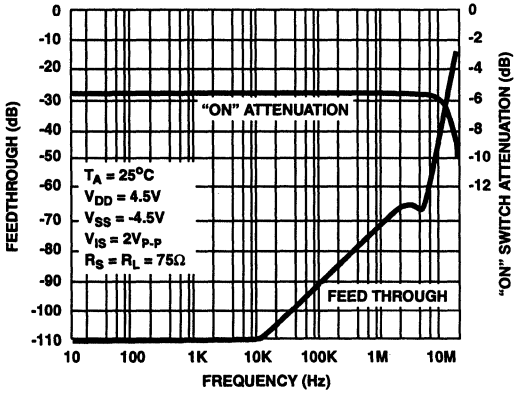


FIGURE 11. TYPICAL "ON" SWITCH ATTENUATION AND "OFF" SWITCH FEED THROUGH AS A FUNCTION OF FREQUENCY

HARRIS SEMICONDUCTOR

CD22103A

CMOS HDB3 (High Density Bipolar 3) Transcoder for 2.048/8.448Mb/s Transmission Applications

January 1997

Features

- **HDB3 Coding and Decoding for Data Rates from 50Kb/s to 10Mb/s in a Manner Consistent with CCITT G703 Recommendations**
- **HDB3/AMI Transmission Coding/Reception Decoding with Code Error Detection is Performed in Independent Coder and Decoder Sections**
- **All Transmitter and Receiver Inputs/Outputs are TTL Compatible**
- **Internal Loop Test Capability**
- **Pin and Functionally Compatible with Type MJ1471**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22103AD	-55 to 125	16 Ld SBDIP	D16.3
CD22103AE	-40 to 85	16 Ld PDIP	E16.3

Description

The CD22103A is an LSI SOS integrated circuit which performs the HDB3 transmission coding and reception decoding functions with error detection. It is used in 2.048Mb/s and 8.448Mb/s transmission applications. The CD22103A performs HDB3 coding and decoding for data rates from 50Kb/s to 10Mb/s in a manner consistent with CCITT G703 recommendations.

HDB3 transmission coding/reception decoding with code error detection is performed in independent coder and decoder sections. All transmitter and receiver inputs/outputs are TTL compatible.

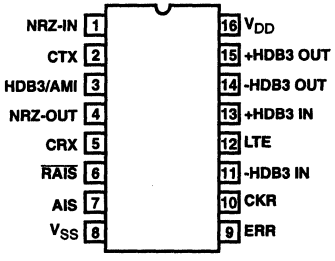
The HDB3 transmitter coder codes an NRZ binary unipolar input signal (NRZ-IN) and a synchronous transmission clock (CTX) into two HDB3 binary unipolar RZ output signals (+HDB3 OUT, -HDB3 OUT). The TTL compatible output signals +HDB3 OUT, -HDB3 OUT are externally mixed to generate ternary bipolar HDB3 signals for driving transmission lines.

The receiver decoder converts binary unipolar inputs (+HDB3 IN, -HDB3 IN), which were externally split from ternary bipolar HDB3 signals, and a synchronous clock signal (CRX) into binary unipolar NRZ signals (NRZ-OUT).

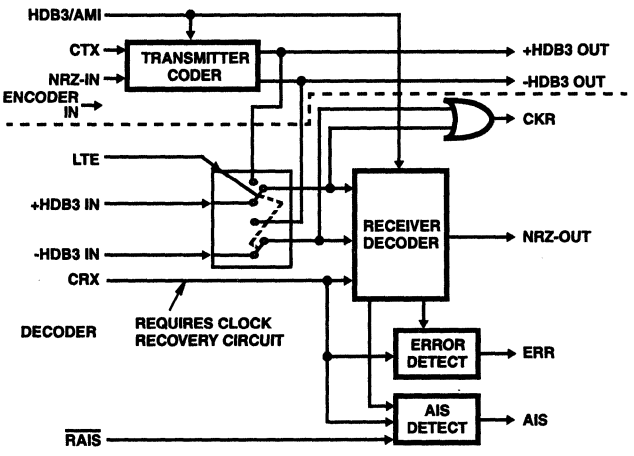
The CD22103A operates with a 5V ±10% power supply voltage over the full military temperature range at data rates from 50Kb/s up to 10Mb/s.

Pinout

CD22103A
(PDIP, SBDIP)
TOP VIEW



Block Diagram



4 WIRED COMMUNICATIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1310.3**

Absolute Maximum Ratings

Supply Voltage (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . -0.5 to 8V
Supply Voltage Range
For T_A = Full Package Temperature Range . . . . . 4.5V to 5.5V
Input Voltage (All Inputs) . . . . . -0.5 to V_{DD} +0.5V
Input Current (Any One Input) . . . . . ±10mA
Power Dissipation
For T_A = -40°C to 60°C (Package Type E) 500mW
For T_A = 60°C to 85°C
(Package Type E) . . . . . Derate Linearly 12mW/°C to 200mW
For T_A = -55°C to 100°C (Package Type D) 500mW
For T_A = 100°C to 125°C
(Package Type D) . . . . . Derate Linearly 12mW/°C to 200mW
Device Dissipation per Output Transistor
For T_A = Full Package Temperature Range (All Types) 100mW

Thermal Information

Maximum Junction Temperature . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C ≤ T_A ≤ 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Temperature Range
Package Type D . . . . . -55°C ≤ T_A ≤ 125°C
Package Type E . . . . . -40°C ≤ T_A ≤ 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} = 5V ±10%, T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
STATIC SPECIFICATIONS						
Quiescent Device Current	I_{DD}		-	-	100	µA
Operating Device Current		f_{CL} = 10MHz	-	-	8	mA
HDB3 Output Low (Sink) Current	I_{OL1}	V_{OL} = 0.5V	1.6	-	-	mA
HDB3 Output High (Source) Current	I_{OH1}	V_{OH} = 2.8V	-10	-	-	mA
All Other Outputs Low (Sink) Current	I_{OL2}	V_{OL} = 0.5V	1.6	-	-	mA
All Other Outputs High (Source) Current	I_{OH2}	V_{OH} = 2.8V	-1.6	-	-	mA
Input Low Current	I_{IL}		-	-	-1	µA
Input High Current	I_{IH}		-	-	1	µA
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2	-	-	V
Input Capacitance	I_{IN}		-	-	5	pF

Electrical Specifications

T_A = -40°C to 85°C for Plastic Package; -55°C to 125°C for Ceramic Package; V_{DD} = 4.5V to 5.5V; C_L = 15pF

PARAMETER	SYMBOL	FIGURE	MIN	TYP	MAX	UNITS
DYNAMIC INPUT						
CTX, CRX Input Frequency	f_{CTX}, f_{CRX}		0.05	-	10	MHz
CTX, CRX Input Rise Time	t_{RCL}	3	-	-	1	µs
Fall Time	t_{FCL}	3	-	-	1	µs
NRZ-IN to CTX						
Data Setup Time	t_S	3	15	-	-	ns
Data Hold Time	t_H	3	15	-	-	ns
HDB3 IN to CRX						
Data Setup Time	t_S	4	15	-	-	ns
Data Hold Time	t_H	3	0	-	-	ns
CRX to CKR (CRX = 8.448MHz)						
Pretrigger	t_P	5	-	-	20	ns
Delay	t_D	5	-	-	20	ns

Electrical Specifications T_A = -40°C to 85°C for Plastic Package; -55°C to 125°C for Ceramic Package; V_{DD} = 4.5V to 5.5V; C_L = 15pF **(Continued)**

PARAMETER	SYMBOL	FIGURE	MIN	TYP	MAX	UNITS
DYNAMIC OUTPUT						
Transmitter Coder, CTX to HDB3 OUT:						
Data Propagation Delay Time	t_{DD}	3	-	-	90	ns
Handling Delay Time	t_{HD}	1	-	4	-	Clock Period
HDB3 OUT Output Pulse Width (Clock duty cycle = 50%)						
f_{CL} = 2.048MHz	t_W	3	238	-	260	ns
f_{CL} = 8.448MHz	t_W	3	53	-	65	
Receiver Decoder CRX to NRZ OUT:						
Data Propagation Delay Times	t_{DD}	4	-	-	90	ns
Handling Delay Time	t_{HD}	2	-	4	-	Clock Period
HDB3 IN to CKR HDB3 Propagation Delay Time						
LTE = 0	$t_{IN\ CKR}$	4	-	-	65	ns
LTE = 1		4	-	-	30	ns

Functional Description

The CD22103A is designed to code and decode HDB3 signals which are coded as binary digital signals (NRZ-IN) and (+HDB3 IN, -HDB3 IN), accompanied by sampling clocks (CTX) and (CRX). The two binary coded HDB3 outputs, (+HDB3 OUT, -HDB3 OUT) may be externally mixed to create the ternary HDB3 signals (See Figure 1).

The two binary HDB3 input signals have been split from the input ternary HDB3 in an external line receiver.

The receiver decoder converts binary unipolar inputs (+HDB3 IN, -HDB3 IN), which were externally split from ternary bipolar HDB3 signals, and a synchronous clock signal (CRX) into binary unipolar NRZ signals (NRZ-OUT).

Received signals not consistent with HDB3 coding rules are detected as errors. The receiver error output (ERR) is active high during one CRX period of each bit of received data that is inconsistent with HDB3 coding rules.

An input string consisting of all ones (or marks) is detected and signaled by a high level at the Alarm Signal (AIS) output. The AIS output is set to a high level when less than three zeros are received during two consecutive periods of the Reset Alarm Inhibit Signal (RAIS). The AIS output is subsequently reset to a low level when three or more zeros are received during two periods of the reset signal ($\overline{RAIS}$).

A diagnostic Loop-Test Mode may be entered by driving the Loop Test Enable Input (LTE) high. In this mode the HDB3 transmitter outputs (+HDB3 OUT, -HDB3 OUT) are internally connected to the HDB3 receiver inputs, and the external HDB3 receiver inputs, and the external HDB3 receiver inputs (+HDB3 IN, -HDB3 IN) are disabled. The NRZ binary output signal (NRZ - OUT) corresponds to the NRZ binary input signal (NRZ - IN) delayed by approximately 8 clock periods.

The Clock Receiver Output (CKR) is the product of the two HDB3 input signals or-ed together. The CRX clock signal may be derived from the CKR signal with external clock extraction circuitry. In the Loop Test Mode (LTE = 1) CKR is the product of the +HDB3 OUT and -HDB3 OUT signals or-ed together.

The CD22103A may also be used to perform the AMI to NRZ coding/decoding function. To use the CD22103A in this mode, the HDB3/AMI control input is driven low.

Error Detection

Received HDB3/AMI binary input signals are checked for coding violations, and an error signal (ERR) is generated as described below.

- **HDB3 Signals HDB3/AMI = High**

The error signal (ERR) is flagged high for one CTX period if a violation pulse (±V) is received of the same polarity as the last received violation pulse.

A violation pulse (±V) is considered a reception error and does not cause replacement of the last string of 4 bits to zeros, if:

The received 4 data bits previous to reception of the violation pulse have not been the sequence BX00 (where X = don't care). The error signal (ERR) remains low.

NOTES:

1. The data sequences B000V and BB00V are valid HDB3 codings of the NRZ binary sequence 10000.
2. The error signal (ERR) count, is the accurate number of all single bit errors.

- **AMI Signals HDB3/AMI = Low**
  - A coding error (ERR) is signaled when a violation pulse (+V) is received.
- **In Either the HDB3 or AMI Mode**
  - When high levels appear simultaneously on both HDB3 inputs (+ HDB3 IN, -HDB3 IN) a logical one is assumed in the HDB3/AMI input stream and the error signal (ERR) goes high for the duration of the violation.

Alarm Inhibit Signal

- The alarm output (AIS) is set high if, in two successive periods of the external Reset Alarm Signal ($\overline{RAIS}$), less than three zeros are received.
- The alarm output (AIS) is reset low when three or more zeros are received during two Reset Alarm Signal periods.

Transcoder Operation

Transmitter Coder (See Figure 1)

The HDB3/AMI transmitter coder operates on 4-bit serial strings of NRZ binary data and a synchronous transmitter clock (CTX). NRZ binary data is serially clocked into the transmitter on the negative transition of the (CTX) clock. HDB3/AMI coding is performed on the 4-bit string, and HDB3/AMI binary output data is clocked out to the (+HDB3 OUT, -HDB3 OUT) outputs on the positive transition of the transmitter clock (CTX) 3 1/2 clock pulses after the data appeared at the (NRZ-IN) input.

Receiver Decoder (See Figure 2)

The HDB3/AMI receiver decoder operates on 4-bit serial strings of binary coded HDB3/AMI signals, and a synchronous receiver clock (CRX), HDB3/AMI binary data is serially clocked into the receiver on the positive transition of the (CRX) clock. HDB3/AMI decoding is performed on the 4-bit string, and NRZ binary output data is clocked out to the (NRZ-OUT) output on the positive transition of the receiver clock (CRX) 4 clock pulses after the data appeared at the (+HDB3 IN, -HDB3 IN) inputs.

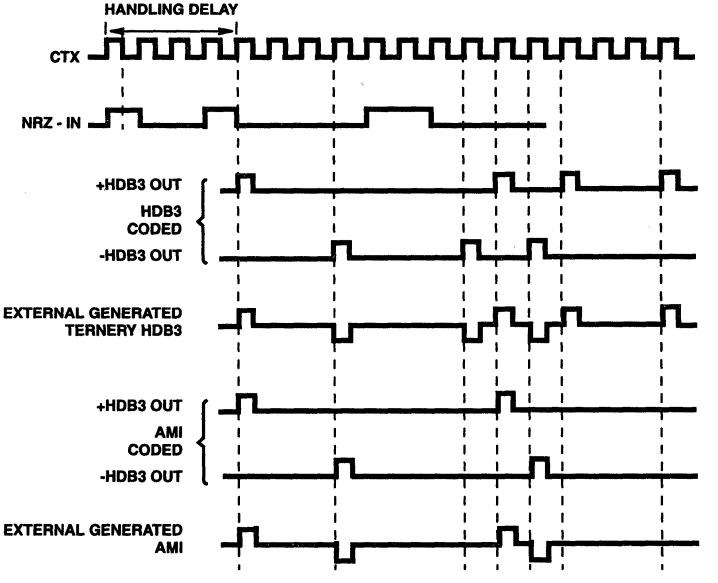


FIGURE 1. TRANSMITTER CODER OPERATION TIMING WAVEFORMS - NRZ TO HDB3/AMI CODING

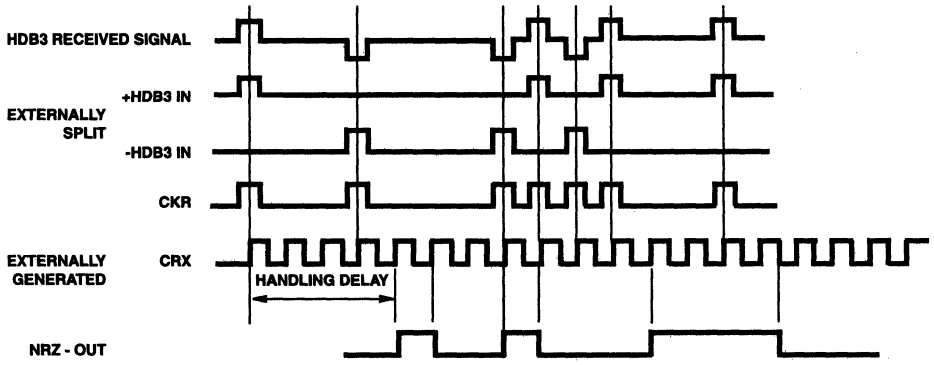


FIGURE 2. RECEIVER DECODER OPERATION TIMING WAVEFORMS - HDB3 TO NRZ DECODING

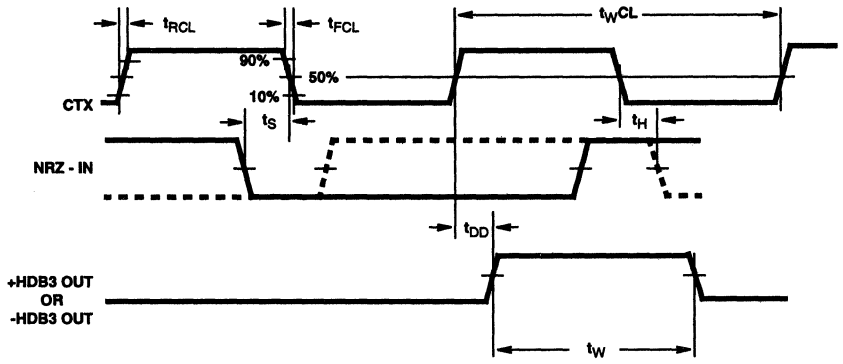


FIGURE 3. TRANSMITTER CODER TIMING WAVEFORMS

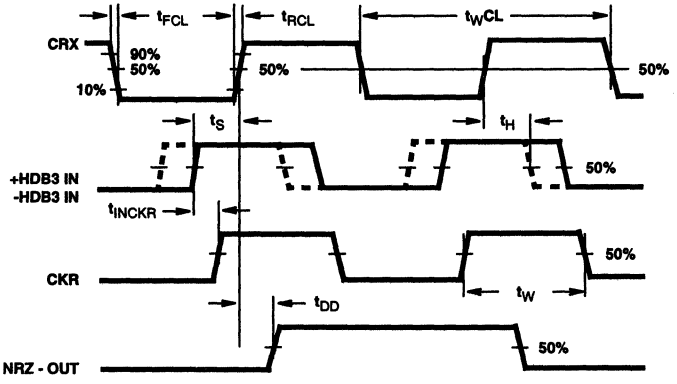


FIGURE 4. INPUT REQUIREMENTS AND OUTPUT CHARACTERISTICS

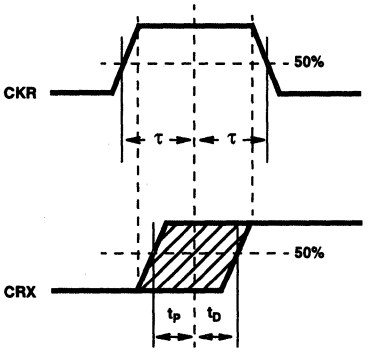


FIGURE 5. CRX RECONSTRUCTION REQUIREMENTS

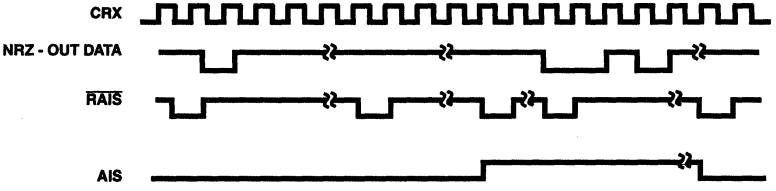


FIGURE 6. RECEIVER ALARM-INHIBIT-SIGNALS TIMING WAVEFORMS

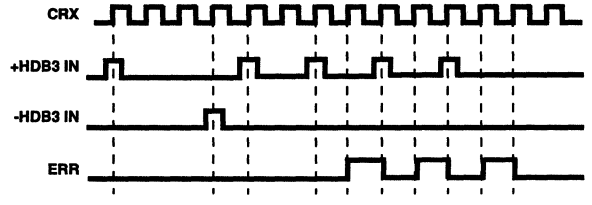


FIGURE 7. RECEIVER ERROR-SIGNALS TIMING WAVEFORMS

Definition of HDB3 Code Used in CD22103A HDB3 Transcoder (As Per CCITRT G703 Annex Recommendations) and Error Detection

Coding Of A Binary Signal Into An HDB3 Signal Is Done According To The Following Rules:

1. HDB3 signal is pseudoternary; the three states are denoted B+, B-, and 0.
2. Spaces (zeros) in the binary NRZ signal are coded as spaces in the HDB3 signal. For strings of four spaces, however, special rules apply (See Item 4 below).
3. Marks (ones) in the binary signal are coded alternately as B+ and B- in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (See Item 4 below).
4. Strings of four spaces in the binary signal are coded according to the followinq rules:

A. The first space of a string is coded as a space if the polarity of the preceding mark of the HDB3 signal has a polarity opposite to the preceding violation and is not a violation by itself; it is coded as a mark, i.e., not a violation (i.e., B+ or B-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.

This rule ensures that successive violations are of alternate polarity so that no DC component is introduced.

B. The second and third spaces of a string are always coded as spaces.

C. The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V+ or V- according to their polarity.

HARRIS SEMICONDUCTOR

CD22301

January 1997

Monolithic PCM Repeater

Features

- **Automatic Line Buildout**
- **Supply Voltage 5.1V**
- **Buffered Output**

Applications

- **Bipolar Carrier System T1 1.544Mbits/s**
- **Ternary Carrier System T148 2.37Mbits/s**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22301E	-40 to 85	18 Ld PDIP	E18.3

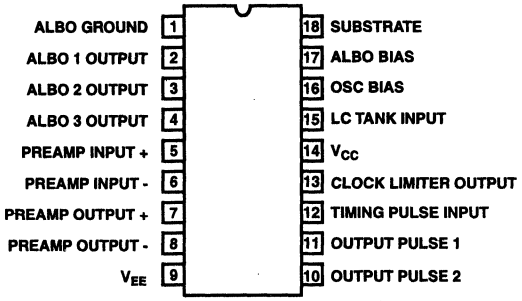
Description

The CD22301 monolithic PCM repeater circuit is designed for T1 carrier systems operating with a bipolar pulse train of 1.544Mbits/s. It can also be used in the T148 carrier system operating with a ternary pulse train of 2.37Mbits/s. The circuit operates from a 5.1V ±5% externally regulated supply.

The CD22301 provides active circuitry to perform all functions of signal equalization and amplification, automatic line buildout (ALBO), threshold detection, clock extraction, pulse timing and buffered output formation.

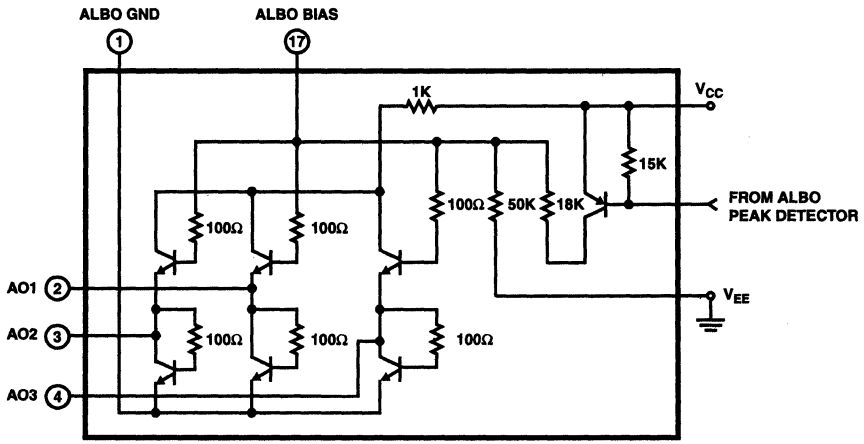
Pinout

CD22301 (PDIP)
TOP VIEW



Functional Diagram

ALBO OUTPUT CIRCUIT



4 WIRED COMMUNICATIONS

File Number **1368.3**

Absolute Maximum Ratings

Supply Voltage 10V
Input Current (Into Pin 9 or 10) 25mA
Peak Current (Into Pin 9 or 10) 100mA
Input Surge Voltage (Between Pins 5 and 6, t = 10ms) 50V
Output Surge Voltage (Between Pins 10 and 11, t = 1ms) 50V
Power Dissipation
For T_A = -40°C to 60°C 500mW
For T_A = 60°C to 85°C .... Derate Linearly 12mW/°C to 200mW
Device Dissipation per Output Transistor
For T_A = Full Package Temperature Range (All Types) 100mW

Thermal Information

Maximum Junction Temperature ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C ≤ T_A ≤ 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C

Operating Conditions

Temperature Range ..... -40°C ≤ T_A ≤ 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = 25°C, V_{CC} = 5.1V ±5% (See Figure 4)

PARAMETER	MIN	TYP	MAX	UNITS
STATIC DC VOLTAGES				
ALBO Pins (Pins 2, 3, 4 and 17)	-	0	0.1	V
Pre Amp Inputs and Outputs (Pins 5, 6, 7 and 8)	2.4	2.9	3.4	V
Output Pulse 1, 2 (Pins 10 and 11)	-	5.1	-	V
Oscillator/Clock (Pins 12, 13, 15 and 16)	3.1	3.6	4.1	V
STATIC DC CURRENTS				
I_{CC}	-	22	30	mA
Output Pulse 1, 2 (Pins 10 and 11)	-	0	100	µA

Electrical Specifications T_A = 25°C, V_{CC} = 5.1V ±5%

PARAMETER	SYMBOL	FIGURE	NOTE	MIN	TYP	MAX	UNITS
DYNAMIC SPECIFICATIONS							
Preamplifier Input Impedance	Z_{IN}	7		20	-	-	kΩ
Preamplifier Output Impedance	Z_{OUT}	7		-	-	2	kΩ
Preamplifier Gain at 2.37MHz	A_O	7		47	50	-	dB
Preamplifier Output Offset Voltage	ΔV_{OUT}	7	1	-50	0	50	mV
Clock Limiter Input Impedance	$Z_{IN}(CL)$	5	2	10	-	-	kΩ
ALBO Off Impedance	$Z_{ALBO}(off)$	5	3	20	-	-	kΩ
ALBO On Impedance	$Z_{ALBO}(on)$	5	4	-	-	10	Ω
DATA Threshold Voltage	$V_{TH}(D)$	6	5, 8	0.62	0.7	0.78	V
CLOCK Threshold Voltage	$V_{TH}(CL)$	6	6, 8	0.92	1.1	1.28	V
ALBO Threshold	$V_{TH}(AL)$	6	7, 8	1.4	1.5	1.6	V
$V_{TH}(D)$ as % of $V_{TH}(AL)$				44	47	49	%
$V_{TH}(CL)$ as % of $V_{TH}(AL)$				66	73	80	%
Buffer Gate Voltage (low)	V_{OL}	4	9	0.65	0.8	0.95	V
Differential Buffer Gate Voltage	ΔV_{OL}	4	9	-0.15	0	0.15	V
Output Pulse Rise Time	t_R	4, 8	9, 10	-	-	40	ns

Electrical Specifications $T_A = 25^oC$, $V_{CC} = 5.1V \pm 5\%$ (Continued)

PARAMETER	SYMBOL	FIGURE	NOTE	MIN	TYP	MAX	UNITS
Output Pulse Fall Time	t_F	4, 8	9, 10	-	-	40	ns
Output Pulse Width	t_W	4, 8	9, 10	290	324	340	ns
Pulse Width Differential	Δt_W	4, 8	9, 10	-10	0	10	ns
Clock Drive Current	I_{CL}			-	2	-	mA

NOTES:

1. No signal input. Measure voltage between pins 7 and 8.
2. Measure clock limiter input impedance at pin 15. See Figure 5.
3. Adjust potentiometer for 0V (See Figure 5). Measure ALBO off impedances from pins 2, 3 and 4 to pin 1.
4. Increase potentiometer until voltage at pin 17 = 2V (See Figure 5). Measure ALBO on impedances from pins 2, 3 and 4 to pin 1.
5. Adjust potentiometer for $\Delta V = 0V$ (See Figure 6). Then slowly increase ΔV in the positive direction until pulses are observed at the DATA terminal.
6. Continue increasing ΔV until the DC level at the clock terminal drops to 4V (See Figure 6).
7. Continue increasing ΔV until the ALBO terminal rises to 1V (See Figure 6).
8. Turn potentiometer in the opposite direction and measure negative threshold voltages by repeating tests outlined in notes 5, 6 and 7.
9. Set $e_{IN} = 2.75mV_{RMS}$ at $f \approx 1.185MHz$. Adjust frequency until maximum amplitude is obtained at pin 15. Observe output pulses at pins 10 and 11.
10. Adjust input signal amplitude until pulses just appear in outputs. Increase input amplitude by 3dB.

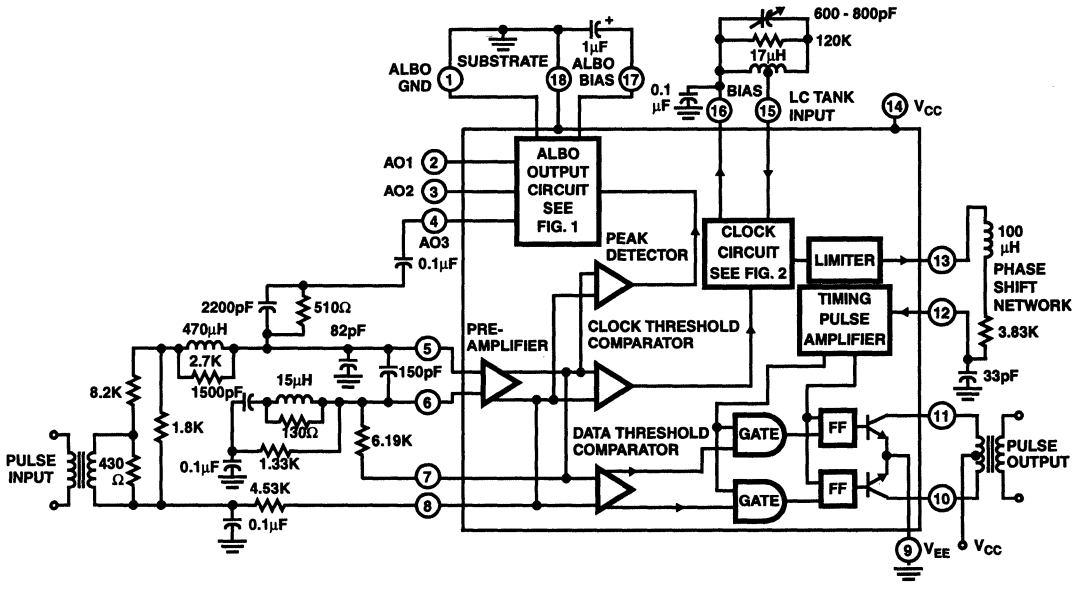


FIGURE 1. TYPICAL 1.544MHz T1 REPEATER SYSTEM

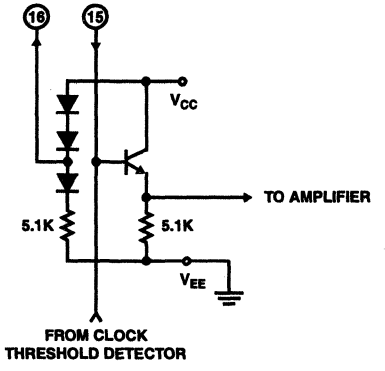


FIGURE 2. CLOCK INTERFACE CIRCUIT

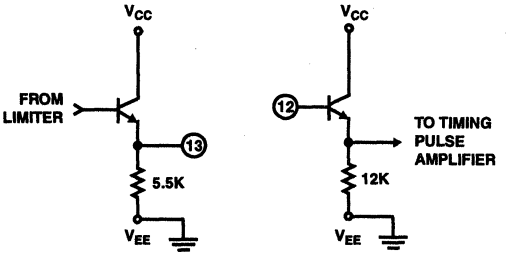


FIGURE 3. PHASE-SHIFT INTERFACE CIRCUITS

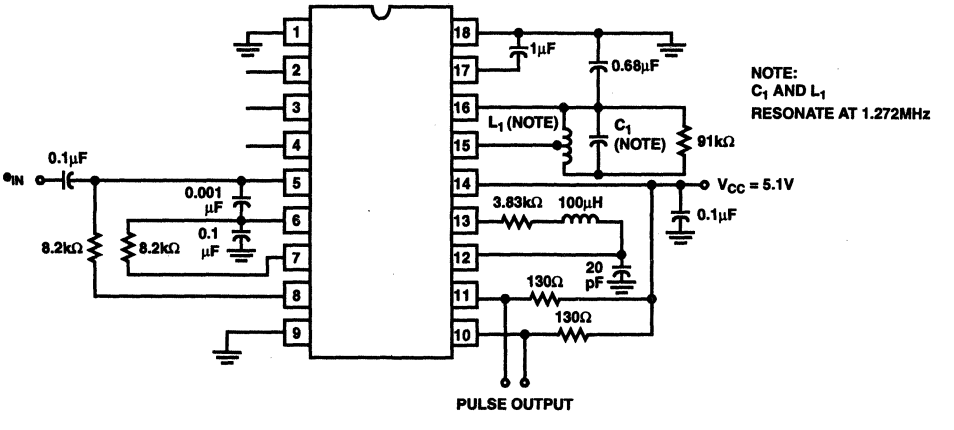


FIGURE 4. DC AND OUTPUT PULSE TEST CIRCUIT

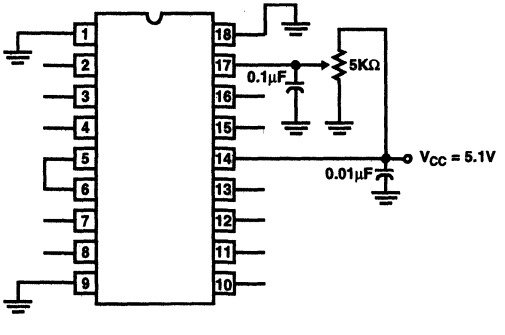


FIGURE 5. TEST CIRCUIT FOR IMPEDANCE MEASUREMENT

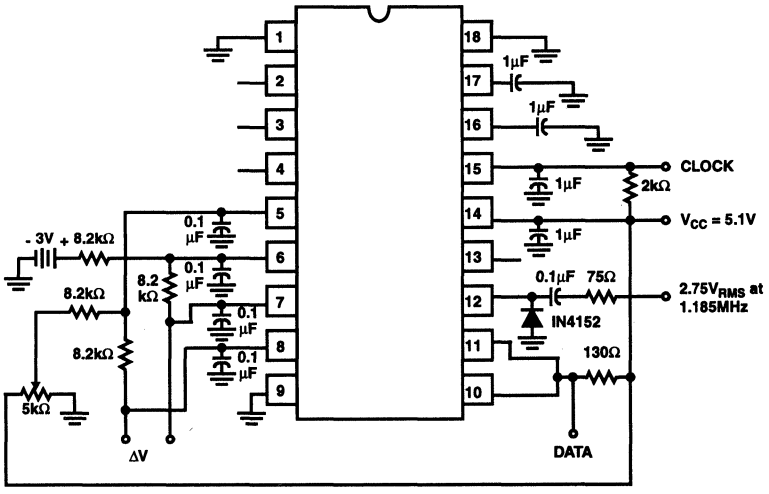


FIGURE 6. TEST CIRCUIT FOR THRESHOLD VOLTAGE MEASUREMENT

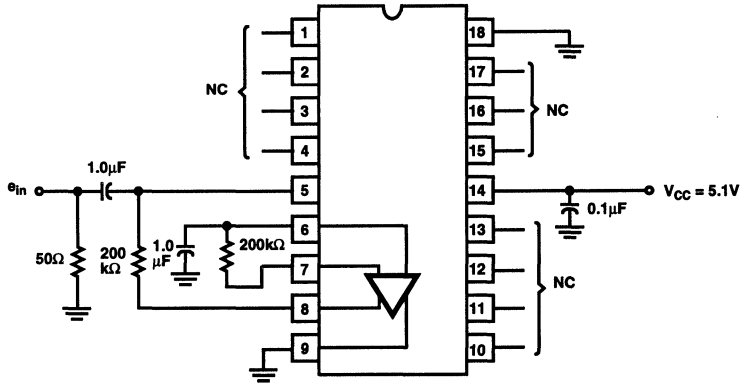


FIGURE 7. PREAMPLIFIER GAIN AND IMPEDANCE MEASUREMENT CIRCUIT

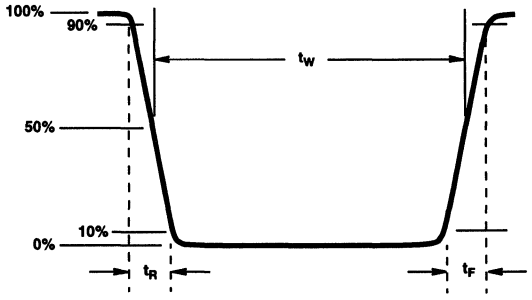


FIGURE 8. OUTPUT PULSE WAVEFORM

HARRIS SEMICONDUCTOR

HC-5560

January 1997

PCM Transcoder

Features

- Single 5V Supply ..... 10mA (Typ)
- Mode Selectable Coding Including:
  - AMI (T1, T1C)
  - B8ZS (T1)
  - HDB3 (PCM30)
- North American and European Compatibility
- Simultaneous Encoding and Decoding
- Asynchronous Operation
- Loop Back Control
- Transmission Error Detection
- Alarm Indication Signal
- Replaces MJ1440, MJ1471 and TCM2201 Transcoders

Applications

- North American and European PCM Transmission Lines where Pseudo Ternary Line Code Substitution Schemes are Desired
- Any Equipment that Interfaces T1, T1C, T2 or PCM30 Lines Including Multiplexers, Channel Service Units, (CSUs) Echo Cancellors, Digital Cross-Connects (DSXs), T1 Compressors, etc.
- Related Literature
  - AN573, The HC-5560 Digital Line Transcoder

Description

The HC-5560 digital line transcoder provides encoding and decoding of pseudo ternary line code substitution schemes. Unlike other industry standard transcoders, the HC-5560 provides four worldwide compatible mode selectable code substitution schemes, including HDB3 (High Density Bipolar 3), B6ZS, B8ZS (Bipolar with 6 or 8 Zero Substitution) and AMI (Alternate Mark Inversion).

The HC-5560 is fabricated in CMOS and operates from a single 5V supply. All inputs and outputs are TTL compatible.

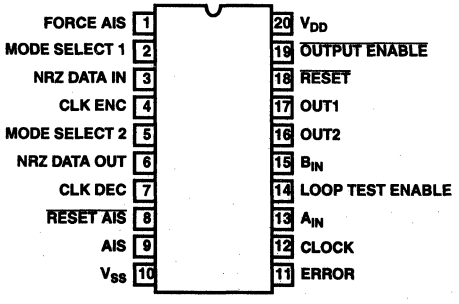
Application Note #573, "The HC-5560 Digital Line Transcoder," by D.J. Donovan is available.

Ordering Information

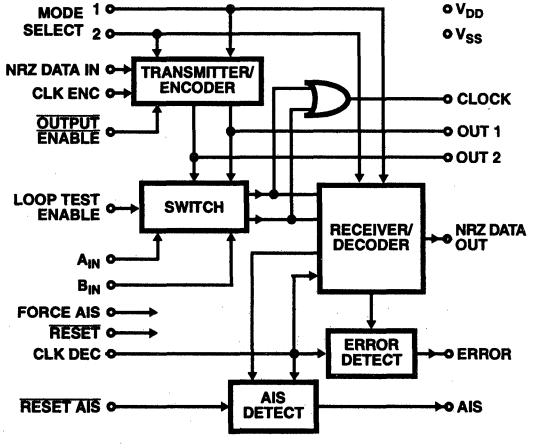
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC3-5560-5	0 to 70	20 Ld PDIP	E20.3

Pinout

HC-5560
(PDIP)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2887.2**

Absolute Maximum Ratings

Voltage at Any Pin ..... GND -0.3V to V_{DD} 0.3V
Maximum V_{DD} Voltage 7.0V

Operating Conditions

Operating Temperature Range ..... 0°C to 70°C
Operating V_{DD} ..... 5V ±5%

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
PDIP Package 67
Maximum Junction Temperature ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°

Die Characteristics

Transistor Count 4322
Die Dimensions ..... 119 mils x 133 mils
Substrate Potential ..... +V
Process ..... SAJI CMOS

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Unless Otherwise Specified, Typical parameters at 25°C, Min-Max parameters are over operating temperature range. V_{DD} = 5V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
STATIC SPECIFICATIONS					
Quiescent Device Current	I_{DD}			100	µA
Operating Device Current			10		mA
OUT1, OUT2 Low (Sink) Current (V_{OL} = 0.4V)	I_{OL1}	3.2			mA
All Other Outputs Low (Sink) Current (V_{OL} = 0.8V)	I_{OL2}	2			mA
All Outputs High (Source) Current (V_{OH} = 4V)	I_{OH}	2			mA
Input Low Current	I_{IL}			10	µA
Input High Current	I_{IH}			10	µA
Input Low Voltage	V_{IL}			0.8	V
Input High Voltage	V_{IH}	2.4			V
Input Capacitance	C_{IN}			8	pF

Electrical Specifications Unless Otherwise Specified, Typical parameters at 25°C, Min-Max parameters are over operating temperature range. V_{DD} = 5V

PARAMETER	SYMBOL	FIGURE	MIN	TYP	MAX	UNITS
DYNAMIC SPECIFICATIONS						
CLK ENC, CLK DEC Input Frequency	f_{CL}				8.5	MHz
CLK ENC,CLK DEC Rise Time (1.544MHz)	t_{RCL}	1, 2		10	60	ns
Fall Time	t_{FCL}	1, 2		10	60	ns
Rise Time (2.048MHz)	t_{RCL}	1, 2		10	40	ns
Fall Time	t_{FCL}	1, 2		10	40	ns
Rise Time (6.3212MHz)	t_{RCL}	1, 2		10	30	ns
Fall Time	t_{FCL}	1, 2		10	30	ns
Rise Time (8.448MHz)	t_{RCL}	1, 2		5	10	ns
Fall Time	t_{FCL}	1, 2		5	10	ns

Electrical Specifications Unless Otherwise Specified, Typical parameters at 25°C, Min-Max parameters are over operating temperature range. V_{DD} = 5V **(Continued)**

PARAMETER	SYMBOL	FIGURE	MIN	TYP	MAX	UNITS
NRZ-Data In to CLK ENC Data Setup Time	t_S	1	20	-	-	ns
Data Hold Time	t_H	1	20	-	-	ns
A_{IN}, B_{IN} to CLK DEC Data Setup Time	t_S	2	15	-	-	ns
Data Hold Time	t_H	2	5	-	-	ns
CLK ENC to OUT1, OUT2	t_{DD}	1	-	23	80	ns
OUT1, OUT2 Pulse Width (CLK ENC Duty Cycle = 50%)						
f_{CL} = 1.544MHz	t_W	1	-	324	-	ns
f_{CL} = 2.048MHz	t_W	1	-	224	-	ns
f_{CL} = 6.3212MHz	t_W	1	-	79	-	ns
f_{CL} = 8.448MHz	t_W	1	-	58	-	ns
CLK DEC to NRZ-Data Out	t_{DD}	2	-	25	54	ns
Setup Time CLK DEC to $\overline{\text{Reset AIS}}$	t_{S2}	3	35	-	-	ns
Hold Time of $\overline{\text{Reset AIS}}$ = '0'	t_{H2}	3	20	-	-	ns
Setup Time $\overline{\text{Reset AIS}}$ = '1' to CLK DEC	t_{S2}	3	0	-	-	ns
$\overline{\text{Reset AIS}}$ to AIS output	t_{PD5}	3	-	-	42	ns
CLK DEC to Error output	t_{PD4}	3	-	-	62	ns

Pin Descriptions

PIN NUMBER	FUNCTION	DESCRIPTION
1	Force AIS	Pin 19 must be at logic '0' to enable this pin. A logic '1' on this pin forces OUT1 and OUT2 to all '1's. A logic '0' on this pin allows normal operation.
2, 5	Mode Select 1, Mode Select 2	MS1 / MS2 / Functions As 0 / 0 / AMI 0 / 1 / B8ZS 1 / 0 / B6ZS 1 / 1 / HDB3
3	NRZ Data In	Input data to be encoded into ternary form. The data is clocked by the negative going edge of CLK ENC.
4	CLK ENC	Clock encoder, clock for encoding data at NRZ Data In.
6	NRZ Data Out	Decoded data from ternary inputs A_{IN} and B_{IN}.
7	CLK DEC	Clock decoder, clock for decoding ternary data on inputs A_{IN} and B_{IN}.
8, 9	$\overline{\text{Reset AIS}}$, AIS	Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS output to zero provided 3 or more zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ period or sets AIS to '1' if less than 3 zeros have been decoded in the preceding two $\overline{\text{Reset AIS}}$ periods. A period of $\overline{\text{Reset AIS}}$ is defined from the bit following the bit during which $\overline{\text{Reset AIS}}$ makes a high to low transition to the bit during which $\overline{\text{Reset AIS}}$ makes the next high to low transition.
10	V_{SS}	Ground reference.
11	Error	A logic '1' indicates that a violation of the line coding scheme has been decoded.
12	Clock	"OR" function of A_{IN} and B_{IN} for clock regeneration when pin 14 is at logic '0', "OR" function of OUT1 and OUT2 when pin 14 is at logic '1'.

Pin Descriptions (Continued)

PIN NUMBER	FUNCTION	DESCRIPTION
13, 15	A_{IN}, B_{IN}	Inputs representing the received PCM signal. A_{IN} = '1' represents a positive going '1' and B_{IN} = '1' represents a negative going '1'. A_{IN} and B_{IN} are sampled by the positive going edge of CLK DEC. A_{IN} and B_{IN} may be interchanged.
14	LTE	Loop Test Enable, this pin selects between normal and loop back operation. A logic '0' selects normal operation where encode and decode are independent and asynchronous. A logic '1' selects a loop back condition where OUT1 is internally connected to A_{IN} and OUT2 is internally connected to B_{IN}. A decode clock must be supplied.
16, 17	OUT1, OUT2	Outputs representing the ternary encoded NRZ Data In signal for line transmission. OUT1 and OUT2 are in return to zero form and are clocked out on the positive going edge of CLK ENC. The length of OUT1 and OUT2 is set by the length of the positive clock pulse.
18	$\overline{\text{Reset}}$	A logic '0' on this pin resets all internal registers to zero. A logic '1' allows normal operation of all internal registers.
19	$\overline{\text{Output Enable}}$	A logic '1' on this pin forces outputs OUT1 and OUT2 to zero. A logic '0' allows normal operation.
20	V_{DD}	Power to chip.

Functional Description

The HC-5560 TRANSCODER can be divided into six sections: transmission (coding), reception (decoding), error detection, all ones detection, testing functions, and output controls.

The transmitter codes a non-return to zero (NRZ) binary unipolar input signal (NRZ Data In) into two binary unipolar return to zero (RZ) output signals (OUT1, OUT2). These output signals represent the NRZ data stream modified according to the selected encoding scheme (i.e., AMI, B8ZS, B6ZS, HDB3) and are externally mixed together (usually via a transistor or transformer network) to create a ternary bipolar signal for driving transmission lines.

The receiver accepts as its input the ternary data from the transmission line that has been externally split into two binary unipolar return to zero signals (A_{IN} and B_{IN}). These signals are decoded, according to the rules of the selected line code into one binary unipolar NRZ output signal (NRz Data Out).

The encoder and decoder sections of the chip perform independently (excluding loopback condition) and may operate simultaneously.

The Error output signal is active high for one cycle of CLK DEC upon the detection of any bipolar violation in the received A_{IN} and B_{IN} signals that is not part of the selected line coding scheme. The bipolar violation is not removed, however, and shows up as a pulse in the NRZ Data Out signal. In addition, the Error output signal monitors the received A_{IN} and B_{IN} signals for a string of zeros that violates the maximum consecutive zeros allowed for the selected line coding scheme (i.e., 15 for AMI, 8 for B8ZS, 6 for B6ZS, and 4 for HDB3). In the event that an excessive amount of zeros is detected, the Error output signal will be active high for one cycle of CLK DEC during the zero that exceeds the maximum number. In the case that a high level should simultaneously appear on both received input signals A_{IN} and B_{IN} a logical one is assumed and appears on the NRZ Data Out stream with the Error output active.

An input signal received at inputs A_{IN} and B_{IN} that consists of all ones (or marks) is detected and signaled by a high level at the Alarm Indication Signal (AIS) output. This is also known as Blue Code. The AIS output is set to a high level when less than three zeros are received during one period of $\overline{\text{Reset AIS}}$ immediately followed by another period of $\overline{\text{Reset AIS}}$ containing less than three zeros. The AIS output is reset to a low level upon the first period of $\overline{\text{Reset AIS}}$ containing 3 or more zeros.

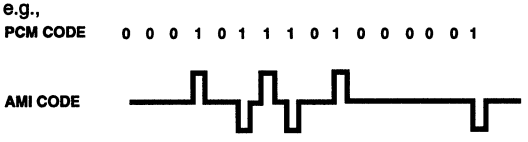
A logic high level on LTE enables a loopback condition where OUT1 is internally connected to A_{IN} and OUT2 is internally connected to B_{IN} (this disables inputs A_{IN} and B_{IN} to external signals). In this condition, NRZ Data In appears at NRZ Data Out (delayed by the amount of clock cycles it takes to encode and decode the selected line code). A decode clock must be supplied for this operation.

The output controls are $\overline{\text{Output Enable}}$ and Force AIS. These pins allow normal operation, force OUT1 and OUT2 to zero, or force OUT1 and OUT2 to output all ones (AIS condition).

Line Code Descriptions

AMI, Alternate Mark Inversion, is used primarily in North American T1 (1.544MHz) and T1C (3.152MHz) carriers. Zeros are coded as the absence of a pulse and ones are coded alternately as positive or negative pulses. This type of coding reduces the average voltage level to zero to eliminate DC spectral components, thereby eliminating DC wander. To simplify timing recovery, logic 1's are encoded with 50% duty cycle pulses.

e.g.,



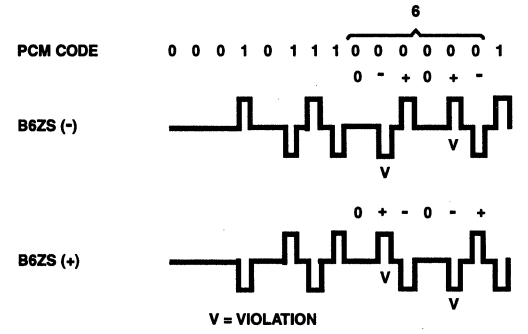
To facilitate timing maintenance at regenerative repeaters along a transmission path, a minimum pulse density of logic 1s is required. Using AMI, there is a possibility of long strings of zeros and the required density may not always exist, leading to timing jitter and therefore higher error rates.

A method for insuring minimum logic 1 density by substituting bipolar code in place of strings of 0s is called BNZS or Bipolar with N Zero Substitution. B6ZS is used commonly in North American T2 (6.3212MHz) carriers. For every string of 6 zeros, bipolar code is substituted according to the following rule:

If the immediate preceding pulse is of (-) polarity, then code each group of 6 zeros as 0+- 0+-, and if the immediate preceding pulse is of (+) polarity, code each group of 6 zeros as 0+- 0-+.

One can see the consecutive logic 1 pulses of the same polarity violate the AMI coding scheme.

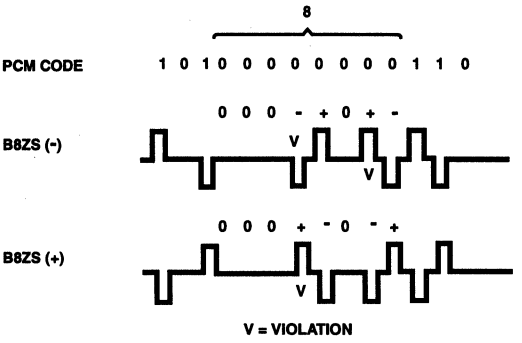
e.g.,



B8ZS is used commonly in North American T1 (1.544MHz) and T1C (3.152MHz) carriers. For every string of 8 zeros, bipolar code is substituted according to the following rules:

1. If the immediate preceding pulse is of (-) polarity, then code each group of 8 zeros as 000-+ 0+-.
2. If the immediate preceding pulse is of (+) polarity then code each group of 8 zeros as 000+-0-+.

e.g.,

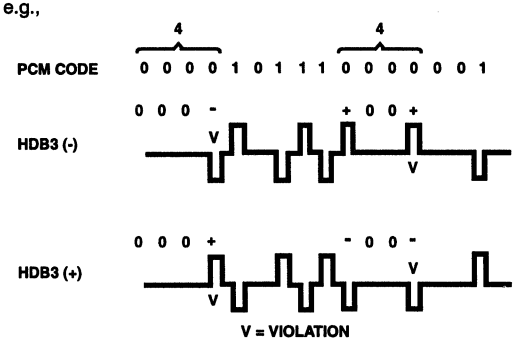


The BNZS coding schemes, in addition to eliminating DC wander, minimize timing jitter and allow a line error monitoring capability.

Another coding scheme is HDB3, high density bipolar 3, used primarily in Europe for 2.048MHz and 8.448MHz carriers. This code is similar to BNZS in that it substitutes bipolar code for 4 consecutive zeros according to the following rule:

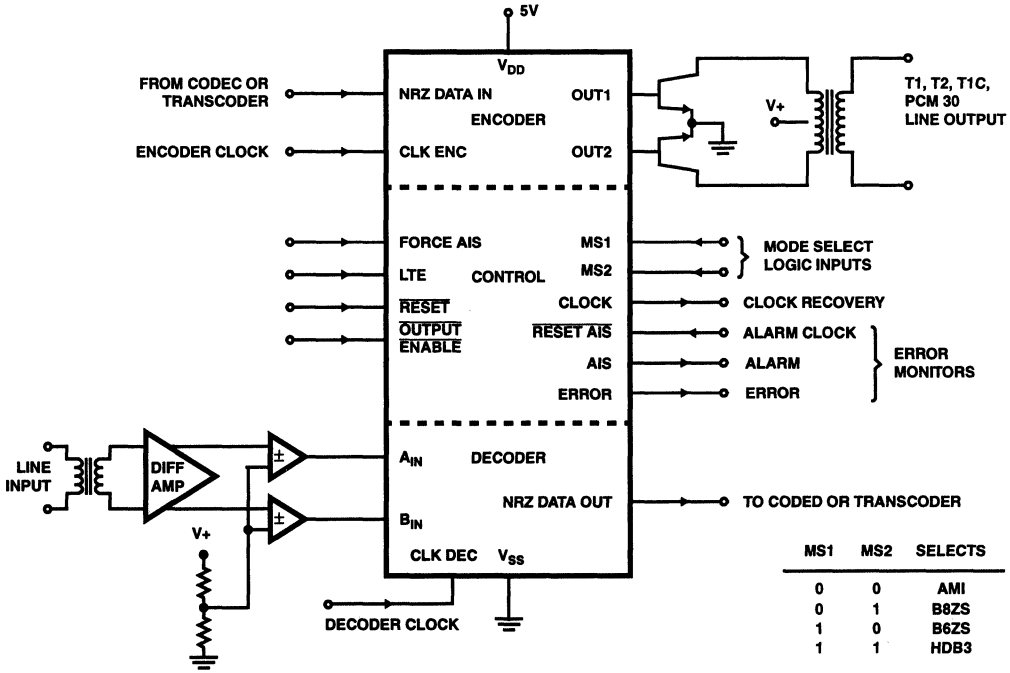
1. If the polarity of the immediate preceding pulse is (-) and there have been an odd (even) number of logic 1 pulses since the last substitution, each group of 4 consecutive zeros is coded as 000-(+00+).
2. If the polarity of the immediate preceding pulse is (+) then the substitution is 000+(-00-) for odd (even) number of logic 1 pulses since the last substitution.

e.g.,



The 3 in HDB3 refers to the coding format that precludes strings of zeros greater than 3. Note that violations are produced only in the fourth bit location of the substitution code and that successive substitutions produce alternate polarity violations.

Application Diagram



MS1	MS2	SELECTS
0	0	AMI
0	1	B8ZS
1	0	B6ZS
1	1	HDB3

Timing Waveforms

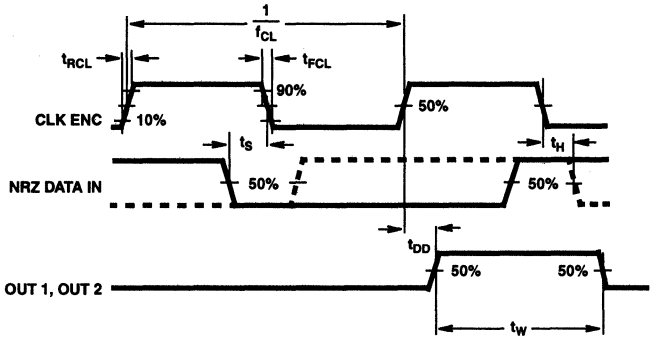


FIGURE 1. TRANSMITTER (CODER) TIMING WAVEFORMS

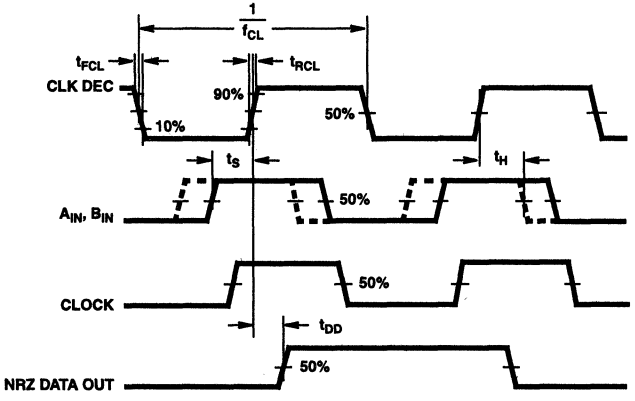


FIGURE 2. RECEIVER (DECODER) TIMING WAVEFORMS

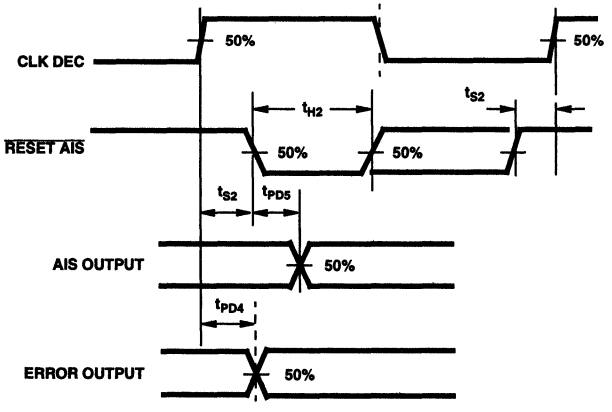


FIGURE 3. $\overline{\text{RESET AIS}}$ INPUT, AIS OUTPUT, ERROR OUTPUT

Timing Waveforms (Continued)

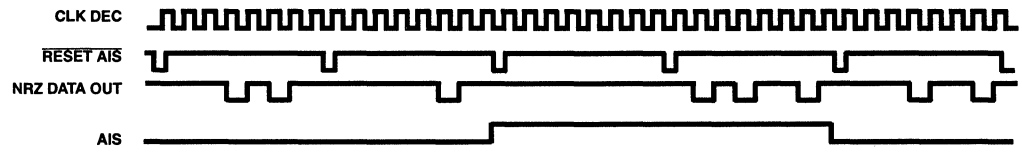


FIGURE 4.

Two consecutive periods of $\overline{\text{Reset AIS}}$, each containing less than three zeros, sets AIS to a logic '1' and remains in a logic '1' state until a period of $\overline{\text{Reset AIS}}$ contains three or more zeros.

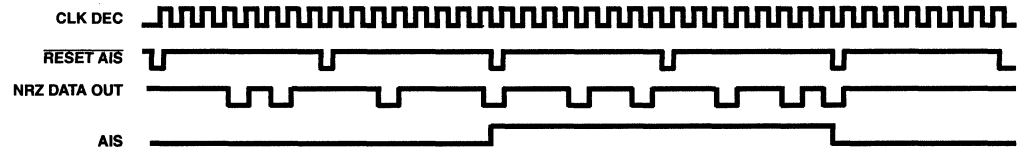


FIGURE 5.

Zeros which occur during a high to low transition of Reset AIS are counted with the zeros that occurred before the high to low transition.

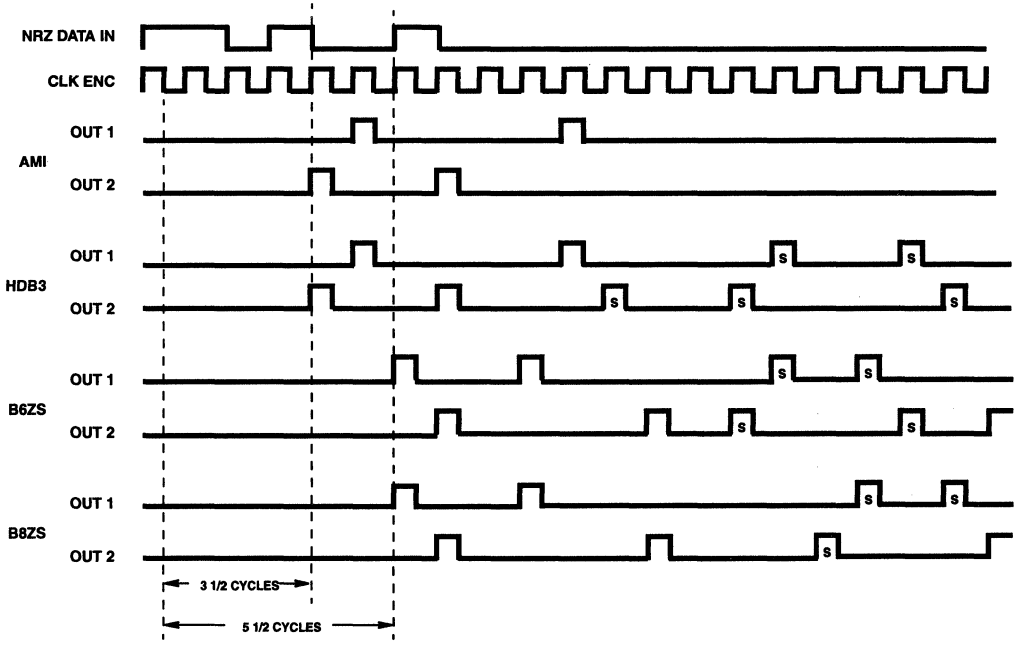


FIGURE 6. ENCODE TIMING AND DELAY

Data is clocked on the negative edge of CLK ENC and appears on OUT1 and OUT2. OUT1 and OUT2 are interchangeable. Bipolar violations and all other pulses inserted by the line coding scheme to encode strings of zeros are labeled with an "S".

Timing Waveforms (Continued)

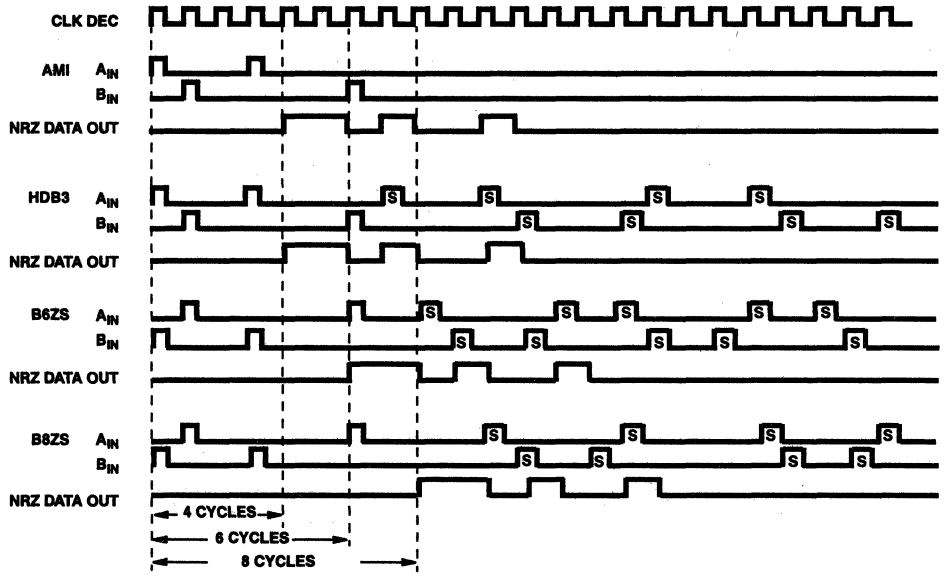


FIGURE 7. DECODE TIMING AND DELAY

Data that appears on A_{IN} and B_{IN} is clocked by the positive edge of CLK DEC, decoded, and zeros are inserted for all valid line code substitutions. The data then appears in non-return to zero to zero form at output NRZ Data Out. A_{IN} and B_{IN} are interchangeable.

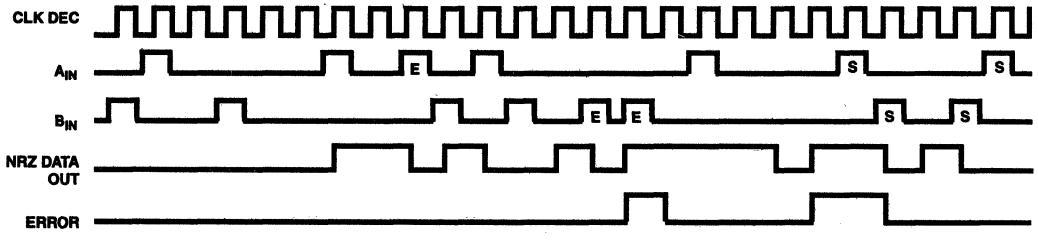


FIGURE 8.

The ERROR signal indicates bipolar violations that are not part of a valid substitution.

CD22202, CD22203

January 1997

5V Low Power DTMF Receiver

Features

- Central Office Quality
- No Front End Band Splitting Filters Required
- Single, Low Tolerance, 5V Supply
- Detects Either 12 or 16 Standard DTMF Digits
- Uses Inexpensive 3.579545MHz Crystal for Reference
- Excellent Speech Immunity
- Output in Either 4-Bit Hexadecimal Code or Binary Coded 2-of-8
- Synchronous or Handshake Interface
- Three-State Outputs
- Excellent Latch-Up Immunity

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22202E	0 to 70	18 Ld PDIP	E18.3
CD22203E	0 to 70	18 Ld PDIP	E18.3

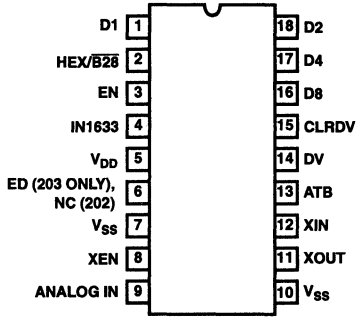
Description

The CD22202 and CD22203 complete dual-tone multiple frequency (DTMF) receivers detect a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.579545MHz TV "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is possible through the use of the clock output of a crystal connected CD22202/CD22203 receiver to drive the time bases of additional receivers. This is a monolithic integrated circuit fabricated with low-power, complementary symmetry CMOS processing. It only requires a single low tolerance power supply.

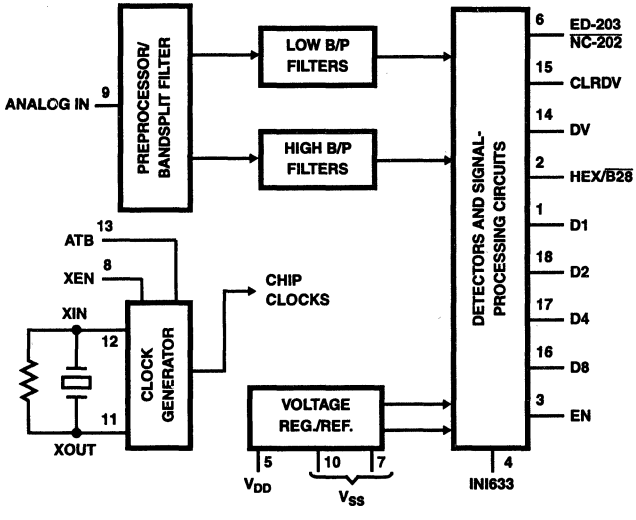
The CD22202 and CD22203 employ state-of-the-art circuit technology to combine the digital and analog functions on the same CMOS chip using a standard digital semiconductor process. The analog input is preprocessed by 60Hz reject and band splitting filters and then hard limited to provide AGC. Eight Bandpass filters detect the individual tones. The digital post processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry and are three-state enabled to facilitate bus oriented architectures.

Pinout

CD22202, CD22203
(PDIP)
TOP VIEW



Functional Diagram



File Number 1695.3

Absolute Maximum Ratings

DC Supply Voltage (V_{DD})(Referenced to V_{SS} Terminal)..... 7V
Power Dissipation
T_A = 25°C (Derate above T_A = 25°C at 6.25mW/°C..... 65mW
Input Voltage Range
All Inputs Except Analog In..... (V_{DD} +0.5V) to -0.5V
Analog in Voltage Range ..... (V_{DD} +0.5V) to (V_{DD} -10V)
DC Current into any Input or Output .....±20mA

NOTE: Unused inputs must be connected to V_{DD} or V_{SS} as appropriate.

Thermal Information

Maximum Junction Temperature..... 175°C
Maximum Junction Temperature (Plastic)..... 150°C
Maximum Storage Temperature Range .....-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)..... 300°C

Operating Conditions

Temperature Range ..... 0°C to 70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

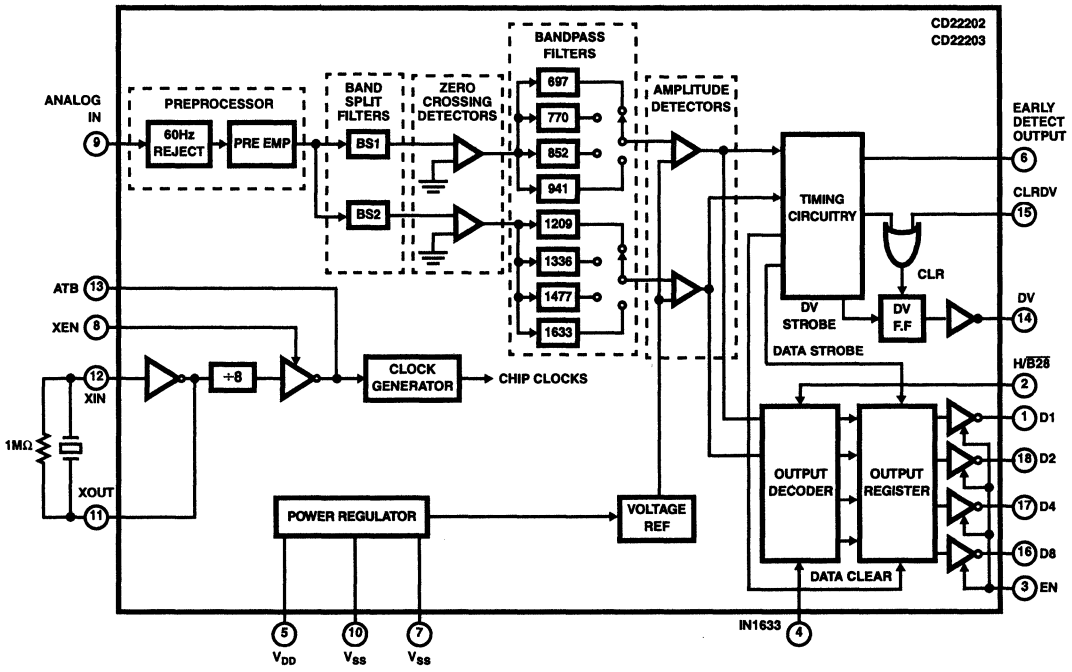
Electrical Specifications

$0°C \le T_A \le +70°C$, V_{DD} = 5V ±10%

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		±(1.5 + 2Hz)	±2.3	±3.5	% of f_O
Amplitude for Detection	Each Tone	-32	-	-2	dBm Referenced to 600Ω
Minimum Acceptable Twist	$Twist = \frac{High\ Tone}{Low\ Tone}$	-10	-	+10	dB
60Hz Tolerance		-	-	0.8	V_{RMS}
Dial Tone Tolerance	"Precise" Dial Tone	-	-	0	dB Referenced to Lower Amplitude Tone
Talk Off	MITEL Tape #CM7291	-	2	-	Hits
Digital Outputs (except XOUT)	"0" Level, 400µA Load	0	-	0.5	V
	"1" Level, 200µA Load	V_{DD} -0.5	-	V_{DD}	V
Digital Inputs	"0" Level	0	-	$0.3V_{DD}$	V
	"1" Level	$0.7V_{DD}$	-	V_{DD}	V
Supply Current	T_A = +25°C	-	10	16	mA
Noise Tolerance	MITEL Tape #CM7291 (Note 1)	-	-	-12	dB Referenced to Lowest Amplitude Tone
Input Impedance	$V_{DD} \ge V_{IN} \ge (V_{DD}$ -10)	100kΩ//15pF	300kΩ	-	

NOTE:
1. Bandwidth limited (3kHz) Gaussian noise.

Functional Block Diagram



NOTE: Pin 6: Early detect output on CD22203 only.

System Functions

Analog In

The Analog In pin accepts the analog input. It is internally biased so that the input signal may be either AC or DC coupled, as long as it does not exceed the positive supply voltage. Proper input coupling is illustrated below.

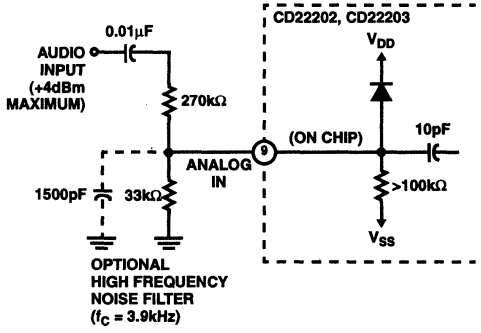


FIGURE 1. ANALOG IN

The CD22202 and CD22203 are designed to accept sinusoidal input waveforms, but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics that are at least 20dB below the fundamental.

Crystal Oscillator

The CD22202 and CD22203 contain an on-board inverter with sufficient gain to provide oscillation when connected to a low cost television "color-burst" (3.579545MHz) crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1MΩ resistor is also connected between these pins in this mode. ATB is a clock frequency output. Other CD22202 and CD22203 devices may use the same frequency reference by tying their ATB pins to the ATB output of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low, respectively. Up to ten devices may be run from a single crystal connected CD22202 and CD22203 as shown in Figure 2.

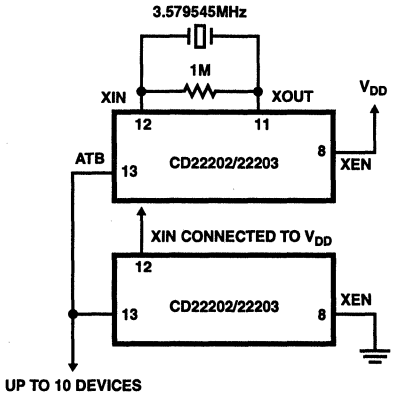


FIGURE 2. CRYSTAL OSCILLATOR

HEX/$\overline{B28}$

This pin selects the format of the digital output code. When HEX/$\overline{B28}$ is tied high, the output is hexadecimal. When tied low, the output is binary coded 2-of-8. The following table describes the two output codes.

TABLE 1. OUTPUT CODES

	HEXADECIMAL				BINARY CODED 2-OF-8			
DIGIT	D8	D4	D2	D1	D8	D4	D2	D1
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0
0	1	0	1	0	1	1	0	1
*	1	0	1	1	1	1	0	0
#	1	1	0	0	1	1	1	0
A	1	1	0	1	0	0	1	1
B	1	1	1	0	0	1	1	1
C	1	1	1	1	1	0	1	1
D	0	0	0	0	1	1	1	1

ED

This pin, on the CD22203 only, indicates the presence of frequencies which are likely to be DTMF digits, but have not yet been verified by a DV signal. It is comparable to a "button-down" output, and it is useful as an EARLY DETECT signal to interrupt a microprocessor for digit storage and validation.

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs or CLRDV is raised high, whichever is sooner. This handshake can save microprocessor time.

DTMF Dialing Matrix

	COL 0 1209Hz	COL 1 1336Hz	COL 2 1477Hz	COL 3 1633Hz
ROW 0 697Hz	1	2	3	A
ROW 1 770Hz	4	5	6	B
ROW 2 852Hz	7	8	9	C
ROW 3 941Hz	*	0	#	D

NOTE: Column 3 is for special applications and is not normally used in telephone dialing.

IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

N/C Pin

This pin has no internal connection and should be left floating.

Digital Inputs and Outputs

All digital inputs and outputs of the DTMF receivers are represented by the schematic below. Only the "analog in" pin is different, and is described above. Care must be exercised not to exceed the voltage or current ratings on these pins as listed in the "maximum ratings" section.

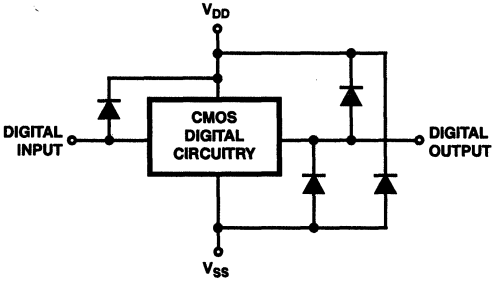


FIGURE 3. DIGITAL INPUTS AND OUTPUTS

Input Filter

The CD22202 and CD22203 will tolerate total input noise of a maximum of 12dB below the lowest amplitude tone. For most telephone applications, the combination of the high frequency attenuation of the telephone line and internal band limiting make special circuitry at the input to these receivers unnecessary. However, noise near the 56kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present

above 28kHz, the simple RC filter shown below may be used to band limit the incoming signal. The cut off frequency is 3.9kHz.

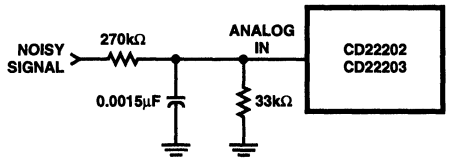
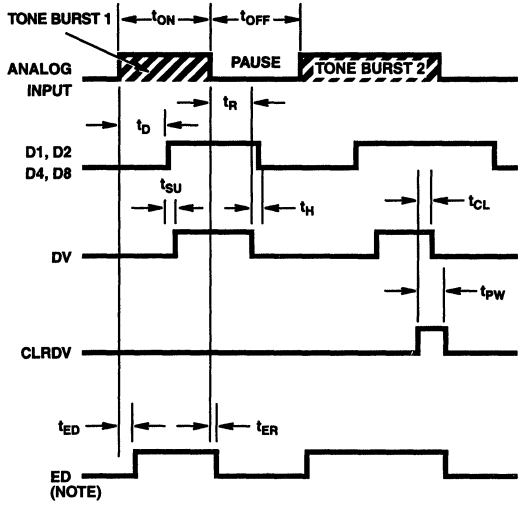


FIGURE 4. FILTER FOR USE IN EXTREME HIGH FREQUENCY INPUT NOISE ENVIRONMENT

Noise will also be reduced by placing a grounded trace around XIN and XOUT pins on the circuit board layout when using a crystal. It is important to note that XOUT is not intended to drive an additional device. XIN may be driven externally; in this case, leave XOUT floating.

Timing Waveforms



NOTE: Early Detect output is available only on the CD22203.

FIGURE 5.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Tone Time					
For Detection	t_{ON}	40	-	-	ms
For Rejection	t_{ON}	-	-	20	ms
Pause Time					
For Detection	t_{OFF}	40	-	-	ms
For Rejection	t_{OFF}	-	-	20	ms
Detect Time	t_D	25	-	46	ms
Release Time	t_R	35		50	ms
Data Setup Time	t_{SU}	7	-	-	µs
Data Hold Time	t_H	4.2	-	5	ms
DV Clear Time	t_{CL}	-	160	250	ns
CLRDV Pulse Width	t_{PW}	200	-	-	ns
ED Detect Time	t_{ED}	7	-	22	ms
ED Release Time	t_{ER}	2	-	18	ms
Output Enable Time C_L = 50pF, R_L = 1kΩ	-	-	200	300	ns
Output Disable Time C_L = 35pF, R_L = 500Ω	-	-	150	200	ns
Output Rise Time C_L = 50pF	-	-	200	300	ns
Output Fall Time C_L = 50pF	-	-	160	250	ns

Guard Time

Whenever the DTMF receiver is continually monitoring a voice channel containing distorted or musical voices or tones, additional guard time may be added in order to prevent false decoding. This may be done in software by verifying that both ED and DV are present simultaneously for about 55ms. An appropriate guard time should be selected to balance the fastest expected dialing speed against the rejection of distorted or musical voices or tones (most autodialers operate in the 65ms to 75ms range although a few generate 50ms tones). A hardware guard time circuit is shown in Figure 6. R_3 and R_4 should keep the voice amplitude as low as practical, while R_2 and R_5 adjust detection speed.

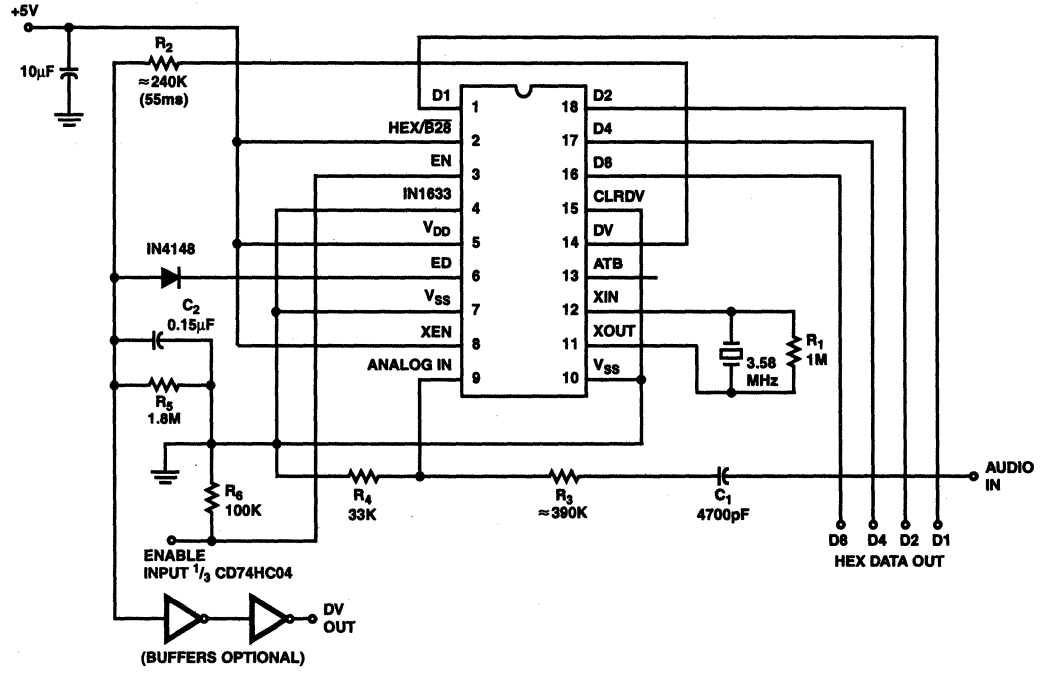


FIGURE 6. CD22203 DTMF RECEIVER WITH GUARD TIME CIRCUIT TO PROVIDE EXCEPTIONAL TALK-OFF PERFORMANCE

Operating and Handling Considerations

Handling

All inputs and outputs of CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits".

Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turnoff transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} - V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 20mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

HARRIS SEMICONDUCTOR

CD22204

5V Low Power Subscriber DTMF Receiver

January 1997

Features

- No Front End Band Splitting Filters Required
- Single Low Tolerance 5V Supply
- Three-State Outputs for Microprocessor Based Systems
- Detects all 16 Standard DTMF Digits
- Uses Inexpensive 3.579545MHz Crystal
- Excellent Speech Immunity
- Output in 4-Bit Hexadecimal Code
- Excellent Latch-Up Immunity

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22204E	0 to 70	14 Ld PDIP	E14.3
CD22204M	0 to 70	24 Ld Plastic SOIC	M24.3

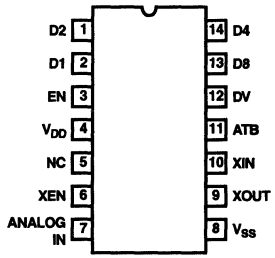
Description

The CD22204 complete dual tone multiple frequency (DTMF) receiver detects a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.579545MHz TV "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is possible through the use of the Alternate Time Base (ATB) output of a crystal connected CD22204 receiver to drive the time bases of up to 10 additional receivers. This is a monolithic integrated circuit fabricated with low power, complementary symmetry CMOS processing. It only requires a single power supply.

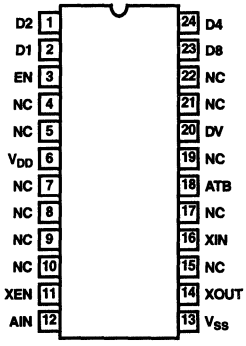
The CD22204 employs state-of-the-art "switched-capacitor" filter technology, resulting in approximately 40 poles of filtering and digital circuitry on the same CMOS chip. The analog input is preprocessed by 60Hz reject and bandsplitting filters and then zero-cross detected to provide AGC. Eight bandpass filters detect the individual tones. Digital processing is used to measure the tone and pause durations and provides the correctly coded and timed digital outputs. The outputs interface directly to standard CMOS circuitry and are three-state enabled to facilitate bus oriented architectures.

Pinouts

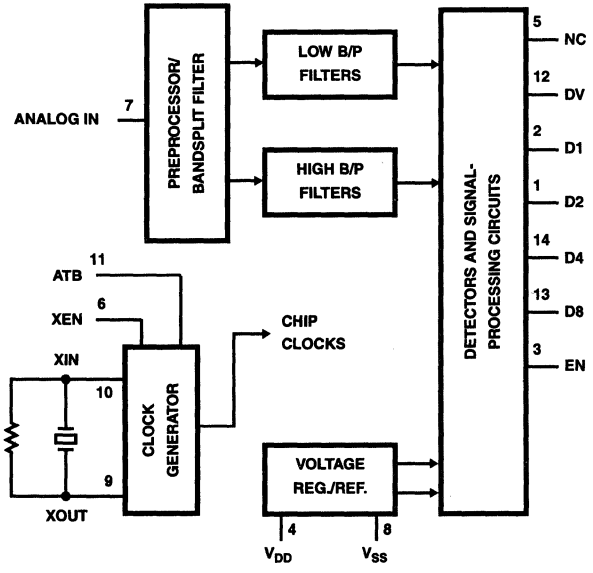
CD22204 (PDIP)
TOP VIEW



CD22204 (SOIC)
TOP VIEW



Functional Diagram



NOTE: Pin numbers are for PDIP.

4 WIRED COMMUNICATIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 1696.3

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{DD}) (Referenced to V_{SS} Terminal) 7V
Power Dissipation
$T_A = 25^oC$ (Derate above $T_A = 25^oC$ at 6.25mW/^oC..... 65mW
Input Voltage Range
All Inputs Except Analog In..... (V_{DD} 0.5V) to -0.5V
Analog in Voltage Range ..... (V_{DD} 0.5V) to (V_{DD} -10V)
DC Current into any Input or Output.....±20mA

Thermal Information

Maximum Junction Temperature..... 175^{o}C
Maximum Junction Temperature (Plastic)..... 150^{o}C
Maximum Storage Temperature Range .....-65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s)..... 300^{o}C

Operating Conditions

Temperature Range ..... 0^{o}C to 70^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

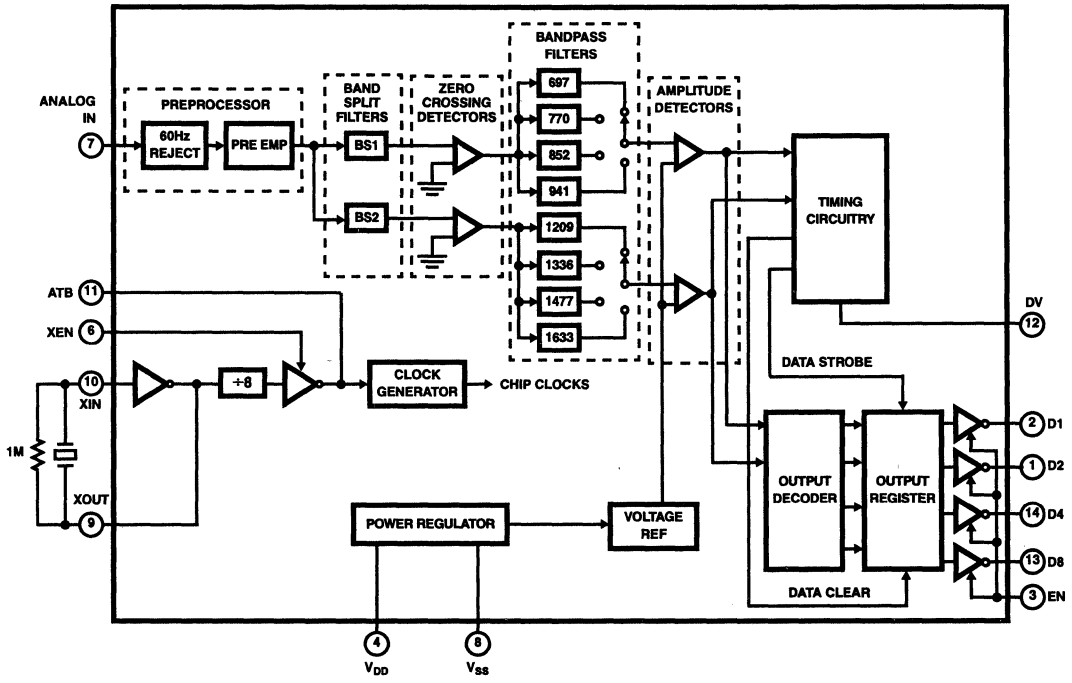
Electrical Specifications $0^oC \le T_A \le 70^oC$, $V_{DD} = 5V \pm 10\%$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		±(1.5 + 2Hz)	±2.3	±3.5	% of f_O
Amplitude for Detection	Each Tone	-32 (Note 3)	-	-2	dBm Referenced to 600Ω
Minimum Acceptable Twist	$Twist = \frac{High\ Tone}{Low\ Tone}$	-8	-	+4	dB
60Hz Tolerance		-	-	0.8	V_{RMS}
Dial Tone Tolerance	"Precise" Dial Tone	-	-	0	dB Referenced to Lower Amplitude Tone
Talk Off	MITEL Tape #CM7291	-	2	-	Hits
Digital Outputs (except XOUT)	"0" Level, 400µA Load	0	-	0.5	V
	"1" Level, 200µA Load	V_{DD} -0.5	-	V_{DD}	V
Digital Inputs	"0" Level	0	-	$0.3V_{DD}$	V
	"1" Level	$0.7V_{DD}$	-	V_{DD}	V
Supply Current	$T_A = 25^oC$	-	10	20	mA
Noise Tolerance	MITEL Tape #CM7291 (Note 2)	-	-	-12	dB Referenced to Lowest Amplitude Tone
Input Impedance	$V_{DD} \ge V_{IN} \ge (V_{DD}$ -10)	100kΩ//15pF	300kΩ	-	

NOTES:

1. Unused inputs must be connected to V_{DD} or V_{SS} as appropriate.
2. Bandwidth limited (3kHz) Gaussian noise.
3. Lower minimum available, please contact sales office.
(-32dBm = 19.45mV_{RMS}, -2dBm = 0.615mV_{RMS})

Functional Block Diagram



NOTE: Pin numbers are for plastic DIP.

System Functions

Analog In

The Analog In pin accepts the analog input. It is internally biased so that the input signal may be either AC or DC coupled, as long as it does not exceed the positive supply voltage. Proper input coupling is illustrated below.

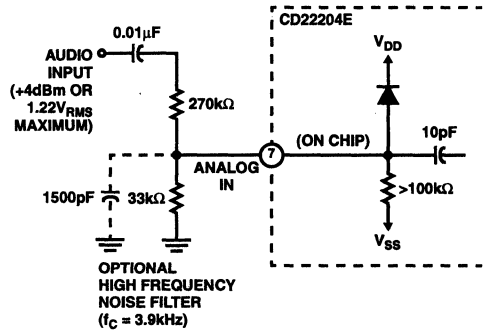


FIGURE 1. ANALOG IN

The CD22204 is designed to accept sinusoidal input waveforms, but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics that are at least 20dB below the fundamental.

Crystal Oscillator

The CD22204 contains an on-board inverter with sufficient gain to provide oscillation when connected to a low cost television "color-burst" (3.579545MHz) crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1MΩ resistor is also connected between these pins in this mode. ATB is a clock frequency output. Other CD22204 devices may use the same frequency reference by tying their ATB pins to the ATB output of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low, respectively. Up to ten devices may be run from a single crystal connected CD22204 as shown in Figure 2.

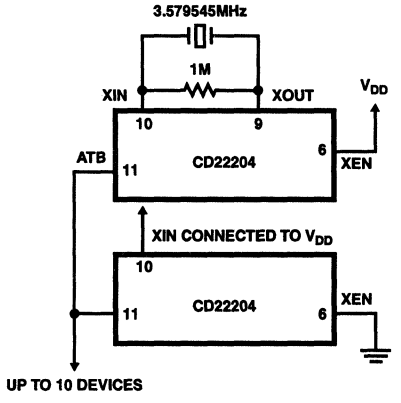


FIGURE 2. CRYSTAL OSCILLATOR

Outputs D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the hexadecimal code corresponding to the detected digit. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed. The table below describes the hexadecimal codes.

TABLE 1. OUTPUT CODES

DIGIT	D8	D4	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

DV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs.

N/C Pin

This pin has no internal connection and should be left floating.

DTMF Dialing Matrix

	COL 0 1209Hz	COL 1 1336Hz	COL 2 1477Hz	COL 3 1633Hz
ROW 0 697Hz	1	2	3	A
ROW 1 770Hz	4	5	6	B
ROW 2 852Hz	7	8	9	C
ROW 3 941Hz	*	0	#	D

NOTE: Column 3 is for special applications and is not normally used in telephone dialing.

Digital Inputs and Outputs

All digital inputs and outputs of the DTMF receivers are represented by the schematic below. Only the "analog in" pin is different, and is described above. Care must be exercised not to exceed the voltage or current ratings on these pins as listed in the "maximum ratings" section.

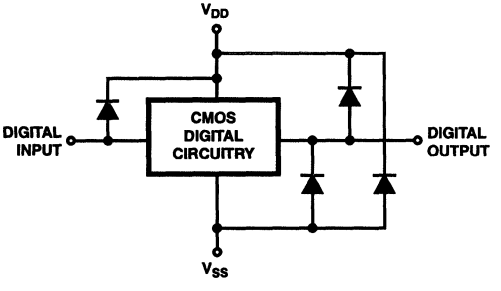


FIGURE 3. DIGITAL INPUTS AND OUTPUTS

Input Filter

The CD22204 will tolerate total input noise of a maximum of 12dB below the lowest amplitude tone. For most telephone applications, the combination of the high frequency attenuation of the telephone line and internal band limiting make special circuitry at the input to these receivers unnecessary. However, noise near the 56kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present above 28kHz, the simple RC filter shown below may be used to band limit the incoming signal. The cut off frequency is 3.9kHz.

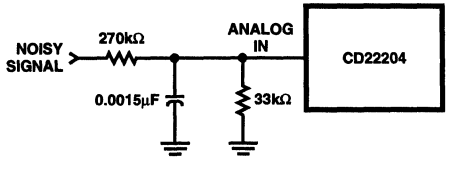


FIGURE 4. FILTER FOR USE IN EXTREME HIGH FREQUENCY INPUT NOISE ENVIRONMENT

Noise will also be reduced by placing a grounded trace around XIN and XOUT pins on the circuit board layout when using a crystal. It is important to note that XOUT is not intended to drive an additional device. XIN may be driven externally; in this case, leave XOUT floating.

Timing Waveforms

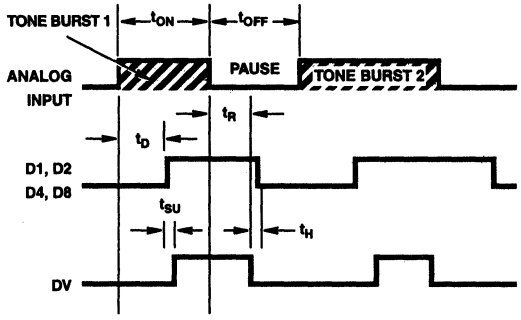


FIGURE 5.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Tone Time					
For Detection	t_{ON}	40	-	-	ms
For Rejection	t_{ON}	-	-	20	ms
Pause Time					
For Detection	t_{OFF}	40	-	-	ms
For Rejection	t_{OFF}	-	-	20	ms
Detect Time	t_D	25	-	46	ms
Release Time	t_R	35		50	ms
Data Setup Time	t_{SU}	7	-	-	µs
Data Hold Time	t_H	4.2	-	5	ms
Output Enable Time C_L = 50pF, R_L = 1kΩ	-	-	200	300	ns
Output Disable Time C_L = 35pF, R_L = 500Ω	-	-	150	200	ns
Output Rise Time C_L = 50pF	-	-	200	300	ns
Output Fall Time C_L = 50pF	-	-	160	250	ns

HARRIS SEMICONDUCTOR

CD22859

Monolithic Silicon COS/MOS Dual-Tone Multifrequency Tone Generator

January 1997

Features

- **Mute Drivers On-Chip**
- **Device Power can Either be Regulated DC or Telephone Loop Current**
- **Use of an Inexpensive 3.579545MHz TV Crystal Provides High Accuracy and Stability for all Frequencies**

Applications

- **For Use In Dual-tone Telephone Dialing Systems**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22859E	-40 to 85	16 Ld PDIP	E16.3

Description

The CD22859 is a CMOS dual-tone multifrequency (DTMF) tone generator for use in dual-tone telephone dialing systems. The device can easily be interfaced to a standard push-button telephone keyboard to provide enabling operation directly with the telephone lines.

The CD22859 generates standard DTMF sinusoidal dialing tones from an on-chip reference crystal oscillator. The reference oscillator uses an inexpensive 3.579545MHz color TV crystal to create highly stable and accurate tones. The sinusoidal tones are digitally synthesized by a stair-step approximation.

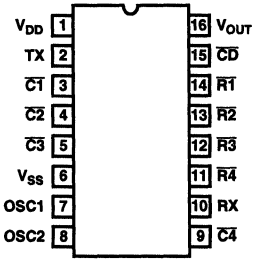
One of four low-frequency band row tones and one of four high-frequency band column tones are selected by driving one of the four row inputs and one of the four column inputs low. Simultaneous selection of more than one row input and/or more than one column input will inhibit tone generation, or generate a single-tone sinusoid. These operating modes are described in the functional truth table.

Control logic is included to allow easy interface to standard K500-type telephones. Two CMOS outputs (T_X, R_X) capable of driving external pnp receiver and transmitter muting transistors are provided. A low input to the $\overline{CD}$ pin inhibits tone generation, turns off the reference oscillator and causes T_X and R_X outputs to go to logic '0'. During tone generation mode, $\overline{CD}$ = 1 and T_X, R_X = logic 1.

The row, column and $\overline{CD}$ inputs are provided with pull-up resistors to allow the use of SPST switch matrixes.

Pinout

CD22859
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1257.3**

Absolute Maximum Ratings

Supply Voltage (V_{DD} - V_{SS}) . . . . . -0.5 to 12V
Input Voltage. . . . . -0.5V to V_{DD} 0.5V
Power Dissipation, P_D
T_A = -40°C to 60°C 500mW
T_A = 60°C to 85°C. . . . . Derate Linearly at 1.2mW/°C to 200mW

Thermal Information

Maximum Junction Temperature . . . . . 175°C
Maximum Junction Temperature (Plastic) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Power Dissipation Per Output 100mW
Temperature Range . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = -25°C to 60°C, All Voltages Referenced to V_{SS} = 0V

PARAMETER	V_{DD} (V)	MIN	MAX	UNITS
DYNAMIC DC SUPPLY VOLTAGE				
Tone Generation Mode with Valid Input (Note 1)		2.5	10	V
Non-Tone Generation (Note 2)		1.7	10	V
DYNAMIC OPERATING CURRENT				
Tone Generation Mode (Outputs Unloaded)	3.7	-	2.7	mA
	9.3	-	13	mA
No Keydown Mode	3.7	-	100	µA
	9.3	-	200	µA
Input Pull-Up Current	3 - 10	-	400	µA
Input Low Voltage (V_{IL}) Maximum	3 - 10	-	$0.2V_{DD}$	V
Input Low Voltage (V_{IH}) Minimum	3 - 10	-	$0.8V_{DD}$	V

Electrical Specifications T_A = -25°C to 60°C

PARAMETER	V_{DD} (V)	V_O (V)	MIN	MAX	UNITS
STATIC TONE OUTPUTS (R_L = 82Ω)					
V_O; Dual-Tone Output	3.7 - 9.3	-	350	700	mV_{RMS}
V_O (C_L); Single-Tone Output, Column (Note 3)	3.7 - 9.3	-	300	-	mV_{RMS}
V_O (R_L); Single-Tone Output, Row (Note 4)	3.7 - 9.3	-	260	-	mV_{RMS}
Distortion (Note 5)	3.9 - 9.3	-	-	10	%
Rise and Fall Time (Dual-Tone Out) (Note 6)	3.9 - 9.3	-	-	5	ms
Pre-Emphasis (Note 7)	3.9 - 9.3	-	1	3	dB
Output Frequency (Note 8)	3.9 - 9.3	-	(Nom. -1%)	(Nom. +1%)	Hz

Electrical Specifications T_A = -25°C to 60°C **(Continued)**

PARAMETER	V_{DD} (V)	V_O (V)	MIN	MAX	UNITS
STATIC MUTE OUTPUT CURRENT					
Transmitter	1.7	1.2	-0.5	-	mA
I_{OH} (Source)	10	9.5	-3.4	-	mA
I_{OL} (Sink)	10	2.5	-	10	µA
Receiver	1.7	1.2	-0.5	-	mA
I_{OH} (Source)	10	9.5	-3.4	-	mA
I_{OL} (Sink)	10	2.5	-	10	µA

NOTES:

1. All logic and counters functional.
2. Mute switches remain open.
3. Two or more row inputs low and one column input low.
4. Two or more column inputs low and one row input low.
5. Distortion is defined as: The ratio of all extraneous frequency components generated in the voiceband 0.5kHz to 3kHz, to the power of the dual-tone signal, measure across R_L.

$$\text{Distortion} = \frac{\sqrt{(V_1^2 + V_2^2 + \ldots + V_n^2)}}{\sqrt{V_L^2 + V_H^2}},$$

where V_1, V_2 . . . . V_n are extraneous frequency components in the voiceband 0.5kHz to 3kHz, V_L is the low-band frequency tone, and V_H is the high-band frequency tone.

6. Tone rise time is defined as the time for each of the 2 DTMF frequencies to attain 90% of full amplitude, measured from the time when a row and column signal are driven low.
7. Pre-emphasis is the ratio of the high-group level to the low-group level.
8. Refer to Figure 1 for standard DTMF frequencies.
9. Corresponds to normal dual-tone operation.
10. Corresponds to single-tone generation mode.

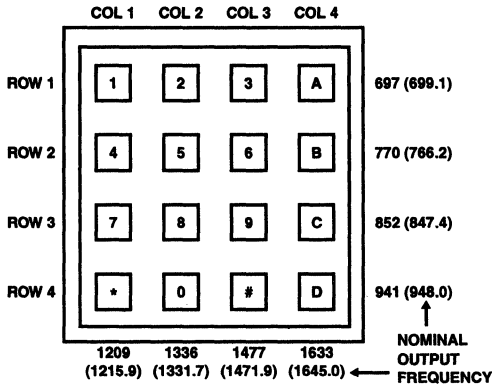


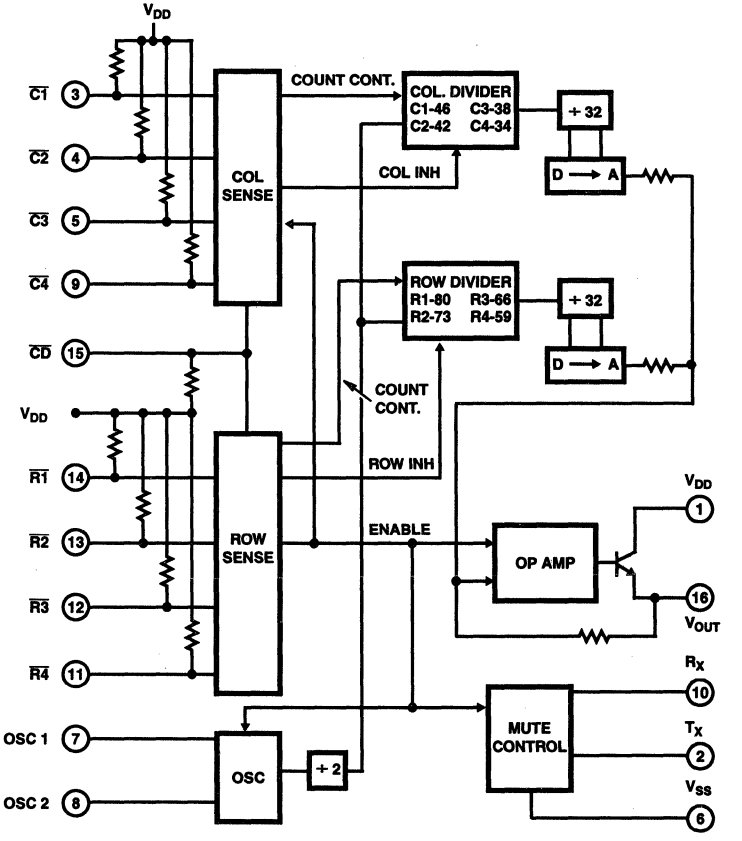
FIGURE 1. BELL AND NOMINAL OUTPUT FREQUENCIES (IN PARENTHESIS) FOR 3.579545MHz CRYSTAL

DTMF GENERATOR FUNCTIONAL TRUTH TABLE

	INPUTS			OUTPUTS			
KEYBOARD MODE	NUMBER OF COLUMN INPUTS ACTIVATED "LOW"	NUMBER OF ROW INPUTS ACTIVATED "LOW"	$\overline{CD}$	TONE	OSC RUNNING	R_X	T_X
X	X	X	"0"	None	No	"0"	"0"
No Key Depressed	0	0	"1"	None	No	"0"	"0"
	0	1	"1"	Dual Tone R_A, C_1	Yes	"1"	"1"
	1, 2, 3, or 4	0	"1"	None	No	"0"	"0"
Normal Dialing One Key Depressed (Note 9)	1	1	"1"	Dual Tone R_A, C_B	Yes	"1"	"1"
Two or More Keys In Same Row (Note 10)	2, 3, or 4	1	"1"	Single Row Tone R_A	Yes	"1"	"1"
Two or More Keys In Same Column	1	2, 3, or 4	"1"	Single Column Tone C_B	Yes	"1"	"1"
Two or More Keys In Different Rows and Columns	2, 3, or 4	2, 3, or 4	"1"	None	Yes	"1"	"1"

Where:
X = Don't Care
R_A refers to Tone Output frequencies corresponding to Row 1, Row 2, Row 3, Row 4; C_B refers to Tone Output frequencies corresponding to Column 1, Column 2, Column 3, Column 4.
A = 1, 2, 3, 4 B = 1, 2, 3, 4 A = B, or A ≠ B

Functional Diagram



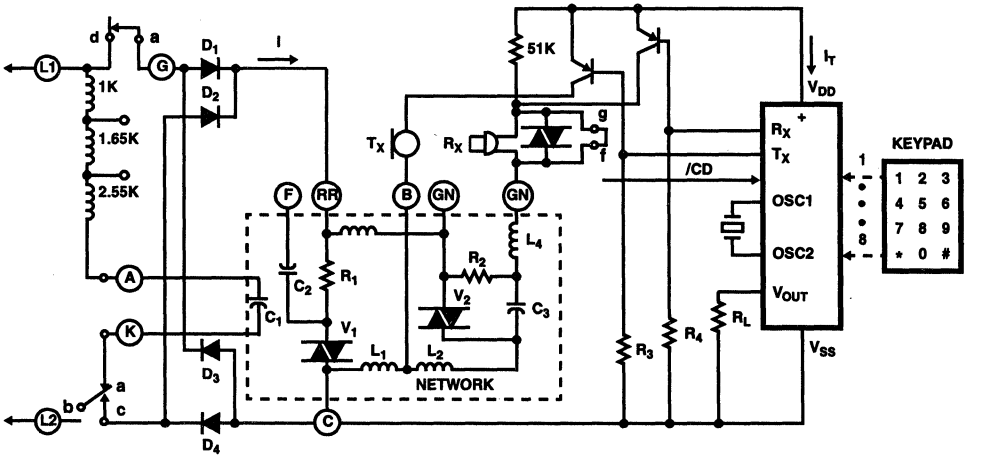


FIGURE 2. INTERFACE WITH STANDARD K500 TELEPHONE NETWORK

HARRIS SEMICONDUCTOR

HC-55564

Continuously Variable Slope Delta-Modulator (CVSD)

January 1997

Features

- All Digital
- Requires Few External Parts
- Low Power Drain: 1.5mW Typical From Single 3V To 6V Supply
- Time Constants Determined by Clock Frequency; No Calibration or Drift Problems: Automatic Offset Adjustment
- Half Duplex Operation Under Digital Control
- Filter Reset Under Digital Control
- Automatic Overload Recovery
- Automatic "Quiet" Pattern Generation
- AGC Control Signal Available

Applications

- Voice Transmission Over Data Channels (Modems)
- Voice/Data Multiplexing (Pair Gain)
- Voice Encryption/Scrambling
- Voicemail
- Audio Manipulations: Delay Lines, Time Compression, Echo Generation/Suppression, Special Effects, etc.
- Pagers/Satellites
- Data Acquisition Systems
- Voice I/O for Digital Systems and Speech Synthesis Requiring Small Size, Low Weight, and Ease of Reprogrammability
- Related Literature
  - AN607, Delta Modulation for Voice Transmission

Description

The HC-55564 is a half duplex modulator/demodulator CMOS intergrated circuit used to convert voice signals into serial NRZ digital data and to reconvert that data into voice. The conversion is by delta-modulation, using the Continuously Variable Slope (CVSD) method of modulation/demodulation.

While the signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by very low power digital filters which require no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

The fundamental advantages of delta-modulation, along with its simplicity and serial data format, provide an efficient (low data rate/low memory requirements) method for voice digitization.

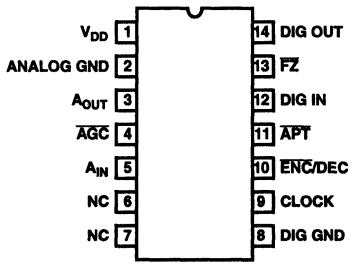
The HC-55564 is usable from 9kbits/s to above 64kbps. See the Harris Military databook for a MIL-STD-883C compliant CVSD. Application Note 607.

Ordering Information

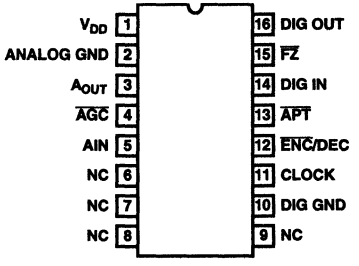
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC1-55564-2	-55 to 125	14 Ld CERDIP	F14.3
HC1-55564-5	0 to 75	14 Ld CERDIP	F14.3
HC1-55564-9	-40 to 85	14 Ld CERDIP	F14.3
HC3-55564-5	0 to 75	14 Ld PDIP	E14.3
HC3-55564-9	-40 to 85	14 Ld PDIP	E14.3
HC9P55564-5	0 to 75	16 Ld Plastic SOIC (W)	M16.15
HC9P55564-9	-40 to 85	16 Ld Plastic SOIC (W)	M16.15

Pinouts

HC-55564
(PDIP, CERDIP)
TOP VIEW



HC-55564
(SOIC)
TOP VIEW



4 WIRED COMMUNICATIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2889.2**

Absolute Maximum Ratings

Voltage at Any Pin ..... GND -0.3V to V_{DD} 0.3V
Maximum V_{DD} Voltage 7.0V
Junction Temperature ..... 175°C

Operating Conditions

Temperature Range
HC-55564-5, -7 ..... 0°C to 75°C
HC-55564-9 ..... -40°C to 85°C
HC-55564-2 ..... -55°C to 125°C
Operating V_{DD} ..... 3.0V to 6.0V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
CERDIP Package	70
PDIP Package	85
SOIC Package	98

Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C

Die Characteristics

Transistor Count 1897
Die Dimensions ..... 147 x 82
Substrate Potential ..... $+V_{DD}$
Process ..... BiMOSE

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Unless Otherwise Specified, typical parameters are at 25°C, Min-Max are over operating temperature ranges. V_{DD} = 5.0V, Sampling Rate = 16Kbps, AG = DG = 0V, A_{IN} = 1.2V_{RMS}

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sampling Rate	CLK	Note 1	9	16	64	kbps
Supply Current	I_{DD}		-	0.3	1.5	mA
Logic '1' Input	V_{IH}	Note 2	3.5	-	-	V
Logic '0' Input	V_{IL}	Note 2	-	-	1.5	V
Logic '1' Output	V_{OH}	Note 3	4.0	-	-	V
Logic '0' Output	V_{OL}	Note 3	-	-	0.4	V
Clock Duty Cycle			30	-	70	%
Audio Input Voltage	A_{IN}	AC Coupled (Note 4)	-	0.5	1.2	V_{RMS}
Audio Output Voltage	A_{OUT}	AC Coupled (Note 5)	-	0.5	1.2	V_{RMS}
Audio Input Impedance	Z_{IN}	Note 6	-	280	-	kΩ
Audio Output Impedance	Z_{OUT}	Note 6	-	150	-	kΩ
Transfer Gain	A_{E-D}	No Load, Audio In to Audio Out.	-2.0	-	+2.0	dB
Syllabic Filter Time Constant	t_{SF}	Note 7	-	4.0	-	ms
Signal Estimate Filter Time Constant	t_{SE}	Note 7	1.0	-	-	ms
Enc Threshold		AIN at 100Hz (Note 8), (Typ) 0.3% = 15mV_{RMS}	-	6	-	mV_{PEAK}
Minimum Step Size	MSS	Note 9	-	0.1	-	$\%V_{DD}$
Quieting Pattern Amplitude	V_{QP}	$\overline{FZ}$ = 0V or $\overline{APT}$ = 0V (Note 10)	-	10	-	mV_{P-P}
AGC Threshold	V_{ATH}	Note 11	-	0.1	-	F.S.
Clamping Threshold	V_{CTH}	Note 12	-	0.75	-	F.S.

NOTES:

2. There is one NRZ (Non-Return Zero) data bit per clock period. Data is clocked out on the negative clock edge. Data is clocked into the CVSD on the positive going edge (see Figure 2). Clock may be run at less than 9kbps and greater than 64kbps.
3. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.
4. Logic outputs are CMOS compatible at supply voltage and will withstand short-circuits to V_{DD} or ground. Digital data output is NRZ and changes with negative clock transitions. Each output will drive one LS TTL load.
5. Recommended voice input range for best voice performance. Should be externally AC coupled.
6. May be used for side-tone in encode mode. Should be externally AC coupled. Varies with audio input level by ±2dB.
7. Presents series impedance with audio signal. Zero signal reference is approximately $V_{DD}/2$.
8. Note that filter time constants are inversely proportional to clock rate. Both filters approximate single pole responses.
9. The minimum audio input voltage above which encoding takes place.
10. The minimum audio output voltage change that can be produced by the internal DAC.
11. Settled value, the "quieting" pattern or idle-channel audio output steps at one-half the bit rate, changing state on negative clock transitions.
12. A logic "0" will appear at the AGC output pin when the recovered signal reaches one-half of full-scale value (positive or negative), i.e., at $V_{DD}/2$ ±25% of V_{DD}.
13. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

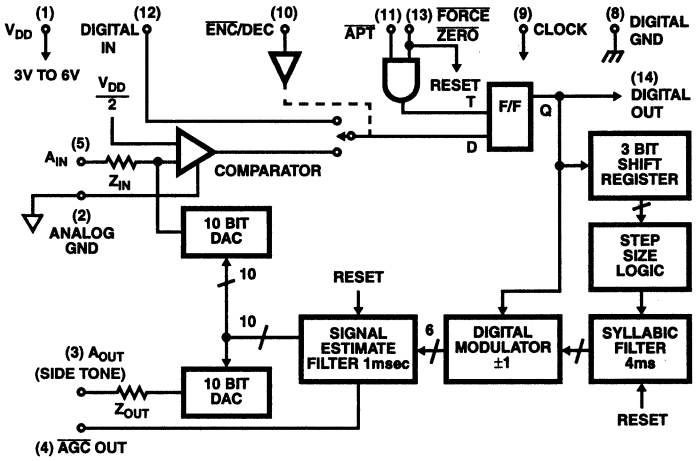
Pin Descriptions

PIN NUMBER 14 LEAD DIP	SYMBOL	DESCRIPTION
1	V_{DD}	Positive Supply Voltage. Voltage range is 3.0V to 6.0V.
2	Analog GND	Analog Ground connection to D/A ladders and comparator.
3	A_{OUT}	Audio Out recovered from 10-bit DAC. May be used as side tone at the transmitter. Presents approximately 150kΩ source with DC offset of $V_{DD}/2$. Within ±2dB of Audio Input. Should be externally AC coupled.
4	$\overline{AGC}$	Automatic Gain Control output. A logic low level will appear at this output when the recovered signal excursion reaches one-half of full scale value. In each half cycle full scale is $V_{DD}/2$. The mark-space ratio is proportional to the average signal level.
5	A_{IN}	Audio Input to comparator. Should be externally AC coupled. Presents approximately 280kΩ in series with $V_{DD}/2$.
6, 7	NC	No internal connection is made to these pins.
8	Digital GND	Logic ground. 0V reference for all logic inputs and outputs.
9	Clock	Sampling rate clock. In the decode mode, must be synchronized with the digital input data such that the data is valid at the positive clock transition. In the encode mode, the digital data is clocked out on the negative going clock transition. The clock rate equals the data rate.
10	$\overline{Encode}$/ Decode	A single CVSD can provide half-duplex operation. The encode or decode function is selected by the logic level applied to this input. A low level selects the encode mode, a high level the decode mode.
11	$\overline{APT}$	Alternate Plain Text input. Activating this input caused a digital quieting pattern to be transmitted, however; internally the CVSD is still functional and a signal is still available at the A_{OUT} port. Active low.
12	Digital In	Input for the received digital NRZ data.
13	$\overline{FZ}$	Force Zero input. Activating this input resets the internal logic and forces the digital output and the recovered audio output into the "quieting" condition. An alternating 1-0 pattern appears at the digital output at 1/2 the clock rate. When this is decoded by a receive CVSD, a $10mV_{P-P}$ inaudible signal appears at audio output. Active low.
14	Digital Out	Output for transmitted digital NRZ data.

NOTE:

14. No active input should be left in a "floating condition."

Functional Diagram (DIP Pin Numbers Shown)



Timing Waveforms

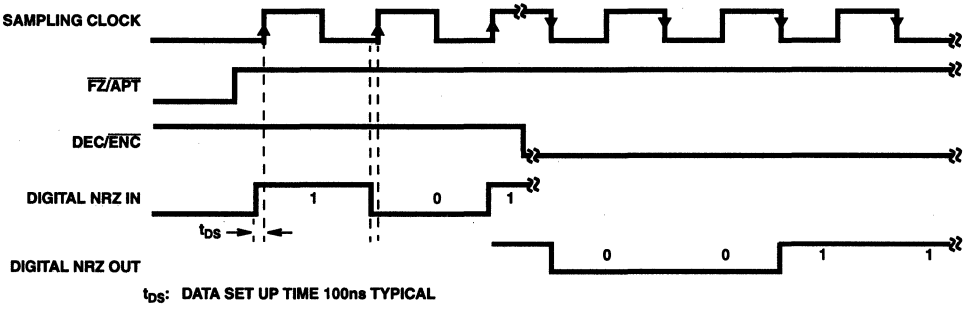


FIGURE 2. CVSD TIMING DIAGRAM

Interface Circuit for HC-55564 CVSD (DIP Pin Numbers Shown)

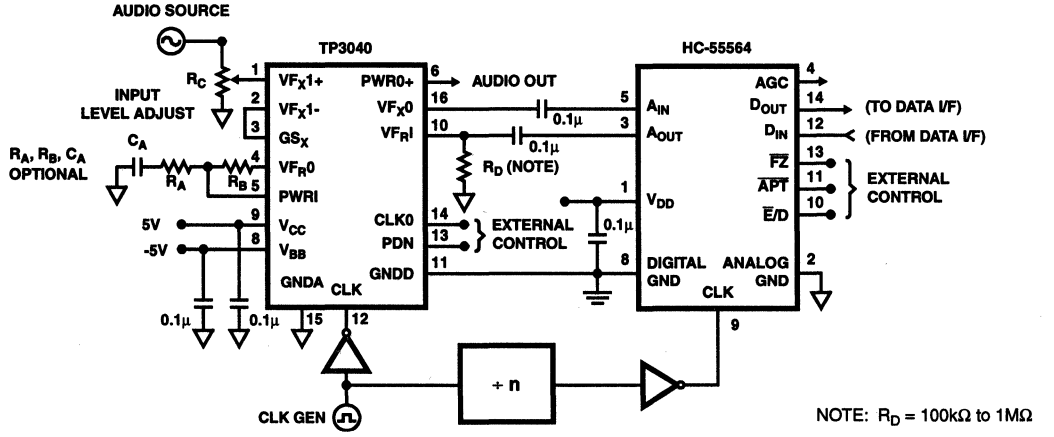


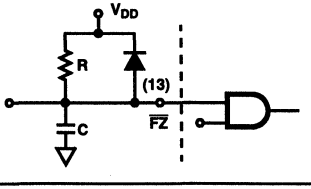
FIGURE 3.

CVSD Hookup for Evaluation

The circuit in Figure 3 is sufficient to evaluate the voice quality of the CVSD, since when encoding, the feedback signal at the audio output pin is the reconstructed audio input signal.

CVSD design considerations are as follows:

1. Care should be taken in layout to maintain isolation between analog and digital signal paths for proper noise consideration.
2. Power supply decoupling is necessary as close to the device as possible. A 0.1µF should be sufficient.
3. Ground, then power, must be present before any input signals are applied to the CVSD. Failure to observe this may cause a latchup condition which may be destructive. Latchup may be removed by cycling the power off/on. A power-up reset circuit may be used that strobes Force Zero (Pin 13) during power-up as follows:
4. Analog (signal) ground (Pin 2) should be externally tied to Digital GND (Pin 8) and power supply ground. It is recommended that the A_{IN} and A_{OUT} ground returns connect only to Pin 2.
5. Digital inputs and outputs are compatible with standard CMOS logic using the same supply voltage. All unused logic inputs must be tied to the appropriate logic level for desired operation. It is recommended that unused inputs tied high be done so through a pull-up resistor (1kΩ to 10kΩ). TTL outputs will require 1kΩ pull-up resistors. Pins 4 and 14 will each drive CMOS logic or one low power TTL input.
6. Since the Audio Out pins are internally DC biased to $V_{DD}/2$, AC coupling is required. In general, a value of 0.1µF is sufficient for AC coupling of the CVSD audio pins to a filter circuit.
7. The AGC output may be externally integrated to drive an AGC pre-amp, or it could drive an LED indicator through a buffer to indicate proper speaking volume.



Figures 4, 5, and 6 illustrate the typical frequency response of the HC-55564 for varying input levels and for varying sampling rates. To prevent slope overload (slew limiting), the 0dB boundary should not be exceeded. The frequency response is directly proportional to the sampling clock rate. The flat bandwidth at 0dB doubles for every doubling in sampling rate. The output levels were measured in the encode mode, without filtering, from A_{IN} to A_{OUT}, at V_{DD} = 5V. 0dB = $1.2V_{RMS}$.

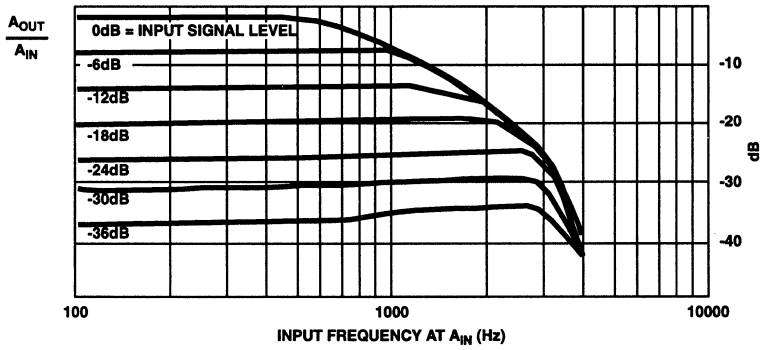


FIGURE 4. 16kbps

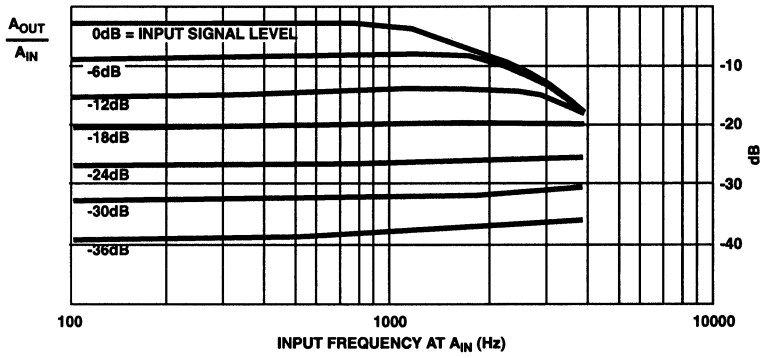


FIGURE 5. 32kbps

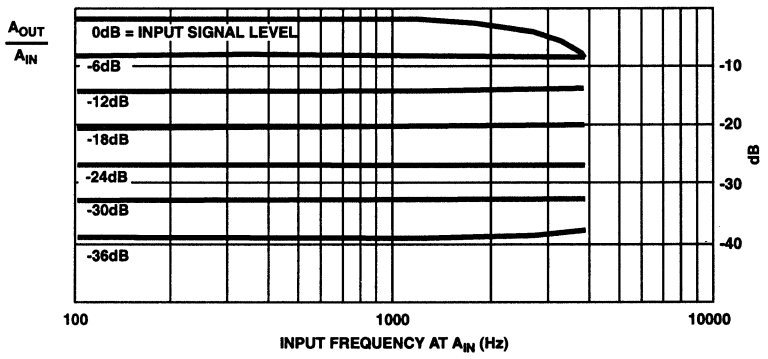


FIGURE 6. 64kbps

The following typical performance distortion graphs were realized with the test configuration of Figure 7. The measurement vehicle for Total Harmonic Distortion (THD) was an HP-339A distortion measurement set, and for 2nd and 3rd harmonic distortion, an HP-3582A spectrum analyzer. All measurement conditions were at V_{DD} = 5V, and 2nd and 3rd harmonic distortion measurements were C-message filtered. 0dB = 1.2V_{RMS}.

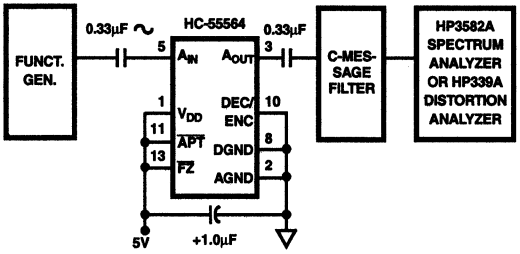


FIGURE 7. TEST AND MEASUREMENT CIRCUIT

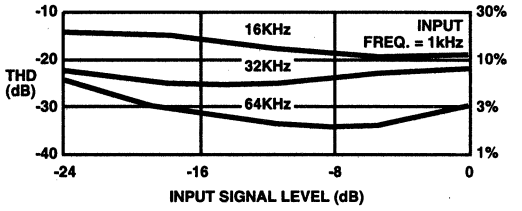


FIGURE 8. CVSD SIGNAL LEVEL vs TOTAL HARMONIC DISTORTION

CVSD INPUT LEVEL vs 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED

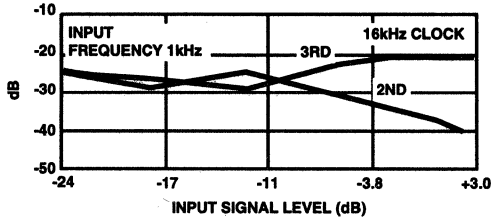


FIGURE 9A.

CVSD SIGNAL TO 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED

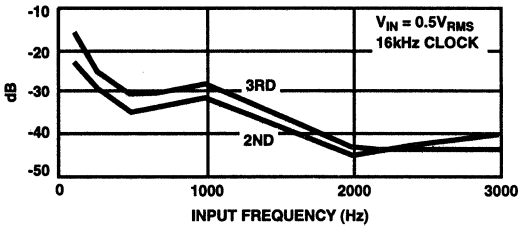


FIGURE 10A.

CVSD INPUT LEVEL vs 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED

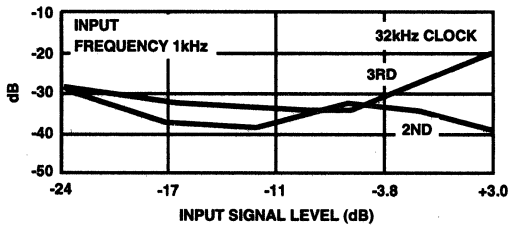


FIGURE 9B.

CVSD SIGNAL TO 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED

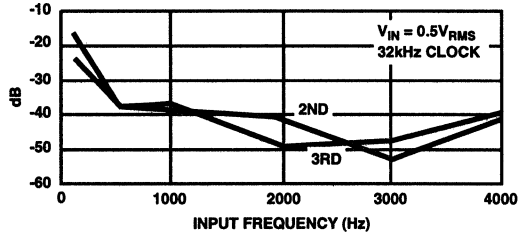


FIGURE 10B.

CVSD INPUT LEVEL vs 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED

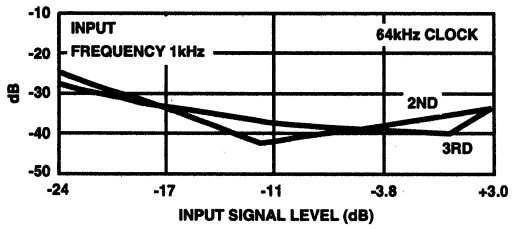


FIGURE 9C.

CVSD SIGNAL TO 2ND AND 3RD HARMONIC DISTORTION
C-MESSAGE WEIGHTED

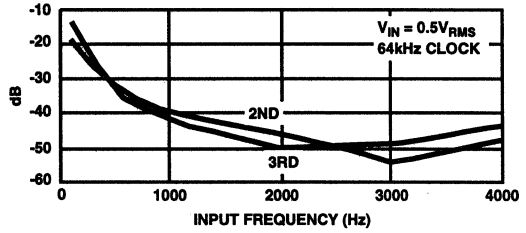


FIGURE 10C.

FIGURE 9. CVSD INPUT LEVEL vs 2ND AND 3RD HARMONIC DISTORTION

FIGURE 10. CVSD INPUT FREQUENCY vs 2ND AND 3RD HARMONIC DISTORTION

COMMUNICATIONS 5

STANDARD PRODUCTS

Standard Products (Continued)

Standard Products (Continued)

Power MOSFET Data Sheets

AN9640 "Glossary of Communication Terms" (32 pages) is not included in this data book, but is available on the net at *http://www.semi.harris.com/appnotes/an9640/* and Harris AnswerFAX (407-724-7800) document # 99640.

A/D CONVERTERS

PART NO.	DESCRIPTION	RESOLUTION (BITS)	CONVERSION RATE (MIN) (MSPS)	BANDWIDTH (MHz)	SINAD AT f_{IN} (dB)	DIFF. GAIN (%)	DIFF. PHASE (DEG.)	POWER DISSIPATION (mW)	LOGIC TYPE	SUPPLY VOLTAGE (V)	PACKAGE OPTIONS	TEMP. RANGE	(NOTE 1) AnswerFAX^{SM} DOC #	(NOTE 2) EVAL BOARD
HI5710A	Low Power, Power Down	10	20	100	54 at 3MHz	1	0.3	140	CMOS/ TTL	5/3.3	PQFP	C	3921	Yes
HI5746	Low Power, High Speed	10	40	100	56.0 at 10MHz	0.5	0.1	225	TTL/ CMOS	5/3	SOIC	C	4129	Yes
HI5703	Low Power, High Accuracy	10	40	250	55.3 at 10MHz	0.5	0.1	400	TTL	5/3.3	SOIC	C	3950	Yes
HI5766	Low Power, High Speed	10	60	100	52.0 at 10MHz	0.5	0.1	315	TTL/ CMOS	5/3	SOIC	C	4130	Yes
HI5800	12-Bit A/D Conversion System, V-Ref	12	3	20	68 at 1MHz	0.9	0.05	1800	CMOS/ TTL	5/-5	CDIP, PLCC	C, I	2938	Yes
HI5804	Low Power	12	5	100	64 at 1MHz	n/a	n/a	300	TTL/ CMOS	5/3	SOIC	C	4026	Yes
HI5805	Low Power, High Performance	12	5	100	68 at 1MHz	n/a	n/a	300	TTL/ CMOS	5/3	SOIC	I	3984	Yes
HI5808	Low Power, High Performance, V-Ref	12	10	100	67 at 1MHz	n/a	n/a	300	TTL/ CMOS	5/3	SOIC	I	4233	Yes

D/A CONVERTERS

P/N	DESCRIPTION	RESOLUTION (BITS)	UPDATE RATE (MHz)	GLITCH AREA (pV-s)	INL (LSB MAX)	DNL (LSB MAX)	SETTLING TIME (ns)	POWER DISSIPATION (mW)	LOGIC TYPE	SUPPLY VOLTAGE (V)	PACKAGE OPTIONS	TEMP. RANGE	(NOTE 1) AnswerFAX^{SM} DOC #	(NOTE 2) EVAL BOARD
HI5780	10-Bit Low Power DAC	10	80	40	2.0	0.5	6	100	CMOS/ TTL	5	MQFP	C	4024	Yes
HI5721	10-Bit Communications DAC	10	125	1.5	1.5	1.0	4.5	700	CMOS/ TTL	5/-5.2	PDIP, SOIC	I	3949	Yes
HI20201	Voltage Output, 75Ω Drive Capability	10	160	15	1	0.5	5.2	420	ECL	-5.2	PDIP, SOIC	C	3581	Yes
HI5731	12-Bit Communications DAC	12	100	3.0	1.5	1.0	20	650	CMOS/ TTL	5/-5.2	PDIP, SOIC	I	4070	Yes
HI5741	14-Bit Communications DAC	14	100	7.5	1.5	1.0	25	650	CMOS/ TTL	5/-5.2	PDIP, SOIC	I	4071	Yes

NOTES:

1. For complete data sheets by fax, call Harris AnswerFAX^{SM} at (407) 724-7800 and enter this document number.
2. Evaluation board part number is base part number plus -EV suffix. (Example: HI5703-EV)

HIGH PERFORMANCE OP AMPS AND BUFFERS

P/N	(NOTE 3) ARCHI-TECTURE	DESCRIPTION	-3dB BANDWIDTH AT MIN. A_{CL} (MHz)	SLEW RATE (V/µs)	SET-TLING TIME (ns TO 0.1%)	MIN. A_{CL} (V/V)	DIFF. GAIN (%)	DIFF. PHASE (DEG.)	OFFSET VOLT. (mV)	BIAS CURRENT (µA)	OUTPUT CURRENT (mA)	SUPPLY RANGE ($\pm V_{DC}$)	SUPPLY CURRENT (mA/A)	(NOTE 5) AnswerFAX℠ DOC #	(NOTE 6) EVAL BOARD
SINGLE															
HFA1100	CFB	850MHz Op Amp	850	2300	11	1	0.03	0.05	2	12	60	4.5 to 5.5	21	2945	A
HFA1120	CFB	850MHz Op Amp with Balance Adjust	850	2300	11	1	0.03	0.05	2	12	60	4.5 to 5.5	21	2945	A
HFA1130	CFB	850MHz Op Amp with Output Limiting	850	2300	11	1	0.03	0.05	2	12	60	4.5 to 5.5	21	3369	A
HFA1112	BUF	850MHz Prog. Gain (+2, ±1) Buffer	850	2400	11	±1, +2	0.02	0.04	8	25	60	4.5 to 5.5	21	2992	A
HFA1113	BUF	850MHz Prog. Gain and Output Limiting	850	2400	13	±1, +2	0.02	0.04	8	25	60	4.5 to 5.5	21	1342	A
HFA1114	BUF	850MHz Prog. Gain Cable Driver	850	2400	11	±1, +2	0.02	0.04	8	25	60	4.5 to 5.5	21	3151	A
HFA1110	BUF	750MHz Unity Gain Buffer	750	1300	11	1	0.04	0.025	8	10	60	4.5 to 5.5	21	2944	B
HFA1102	CFB	600MHz Op Amp with Compensation	600	2000	11	1	0.03	0.03	2	12	60	4.5 to 5.5	21	3597	A

NOTES:

3. Architecture: CFB = Current Feedback, BUF = Buffer.
4. Typical values at 25°C unless otherwise specified.
5. For complete data sheets by fax, call Harris AnswerFAX℠ at (407) 724-7800 and enter this document number.
6. Order evaluation board P/N (PDIP only): A = HFA11XXEval, B = HFA1110Eval.

TRANSISTOR ARRAYS

PART NUMBER	CONFIGURATION	F_T	NOISE F (dB)	h_{FE}	I_C	PACKAGE	(NOTE 7) AnswerFAX^{SM} DOC #
CA3046	NPN - 5	120MHz	3.25	110	10mA	14, SOIC, PDIP, CDIP, T&R	341
CA3081	NPN - 7, Common emitter	120MHz	3.25	85	20mA	16, SOIC, PDIP, CDIP, T&R	480
CA3082	NPN - 7, Common collector	120MHz	3.25	85	20mA	16, SOIC, PDIP, CDIP, T&R	480
CA3083	NPN - 5	450MHz	3.25	75	100mA	16, SOIC, PDIP, CDIP, T&R	481
CA3086	NPN - 5, Diff Amp + 3	550MHz	3.25	100	3mA	14, SOIC, PDIP, CDIP, T&R	483
CA3096	NPN - 3, PNP - 2	335MHz	2.2	300	1mA	16, PDIP, SOIC, T&R	595
CA3127	NPN - 5	1.15GHz	3.5	90	10mA	16, PDIP, CDIP, SOIC, T&R	662
CA3146	NPN - 5, Diff Pair + 3	500MHz	3.2	100	1mA	14, PDIP, SOIC, T&R	532
CA3183	NPN - 5	500MHz	3.2	40	50mA	16, PDIP, SOIC, T&R	532
CA3227	NPN - 5	3GHz	3.2	110	10mA	16, PDIP, SOIC, T&R	1345
CA3246	NPN - 5, Diff Amp + 3	3GHz	3.2	110	10mA	14, PDIP, SOIC, T&R	1345
HFA3046	NPN - 5, Diff Amp +3	8GHz	2.5	70	10mA	14, SOIC, T&R	3076
HFA3096	NPN - 3, PNP - 2	8GHz, 5.5GHz	2.5	70/40	10mA	16, CDIP, SOIC, T&R	3076
HFA3127	NPN - 5	8GHz	2.5	70	10mA	16, CDIP, SOIC, T&R	3076
HFA3128	PNP - 5	5.5GHz	2.5	40	10mA	16, SOIC, T&R	3076

WIRELESS BUILDING BLOCKS

PART NUMBER	FUNCTION	FEATURES	PACKAGE	(NOTE 7) AnswerFAX^{SM} DOC #
HFA3101	Gilbert Cell Mixer	GBP = 10GHz, h_{FE} = 70, 3, 5dB Noise Figure	8, SOIC, T&R	3663
HFA3102	Dual Long Tailed Pair	GBP = 10GHz, h_{FE} = 70, 3, 5dB Noise Figure	14, SOIC, T&R	3635
HFA3600	LNA/Mixer	Noise Figure 3.97dB at 900MHz, 19.8dB Power Gain, -16.7dBm Intercept	14, SOIC, T&R	3655

NOTE:

7. For complete data sheets by fax, call Harris AnswerFAX^{SM} at (407) 724-7800 and enter this document number.

DIGITAL FILTERS

PART NUMBER	DESCRIPTION	MAX ATTENUATION (dB)	CLOCK (MHz)	FILTER TAPS	DATA (BITS)	COEFFICIENT (BITS)	DECIMATION FILTER LENGTH	µP INTERFACE	PACKAGE TYPE	(NOTE 8) AnswerFAX^{SM} DOC #
HSP43168	Dual FIR	60	45	16	10	10 or 20	1 to 16	Standard	PLCC, MQFP, PGA	2808
HSP43220	Digital Decimating	96	33	512	16	20	Up to 16,384	Standard	MQFP, PGA	2486
HSP43216	Halfband	90	52	67	16	20		Standard	PLCC, MQFP, PGA	3365
HSP43124	Serial I/O	140	45	Up to 256	24	32	1 to 256	Standard	PDIP, SOIC	3555

SIGNAL SYNTHESIS

PART NUMBER	DESCRIPTION	CLOCK (MHz)	SIZE	RANGE	RESOLUTION	OUTPUT	MODULATION TECHNIQUES	µP INTERFACE	PACKAGE TYPE	(NOTE 8) AnswerFAX^{SM} DOC #
HSP45102	Oscillator (NCO)	40	12	69	0.009	12 sin	QPSK, FSK	Standard	PDIP, SOIC	2810
HSP45106	Oscillator (NCO)	33	16	90	<0.008	16 sin/cos	FM, PSK, FSK	Standard	PLCC, PGA	2809
HSP45116	Oscillator/Modulator (NCOM)	25	16	90	<0.008	20 sin/cos	AM, FM, PSK, FSK, QAM	Standard	MQFP, PGA	2485
HSP45116A	Oscillator/Modulator (NCOM)	52	16	90	<0.013	20 sin/cos	AM, FM, PSK, FSK, QAM	Standard	MQFP	4156

NOTE:

8. For complete data sheets by fax, call Harris AnswerFAX^{SM} at (407) 724-7800 and enter this document number.

DOWN CONVERSION AND DEMODULATION

PART NUMBER	DESCRIPTION	CLOCK (MHz)	DATA (BITS)	DECIMATION FACTORS	FREQUENCY SELECTIVITY (Hz)	STOPBAND ATTENUATION (dB)	PASSBAND RIPPLE (dB)	PACKAGE TYPE	(NOTE 9) AnswerFAX^{SM} DOC #
HSP50016	Digital Down Converter	75	16	64 - 131,072	<0.009	104	<0.04	PLCC, PGA	3288
HSP50214	Programmable Down Converter	52	14	4 - 16,384	0.013	100dB		MQFP	4266

PART NUMBER	DESCRIPTION	INPUT SAMPLE RATES (MSPS)	DATA (BITS)	DECIMATION FACTORS	FREQUENCY SELECTIVITY (Hz)	AUTOMATIC GAIN CONTROL	OUTPUT FORMAT	FILTERING	CARRIER TRACKING	SYMBOL TRACKING	(NOTE 9) AnswerFAX^{SM} DOC #
HSP50110 and HSP50210	SATCOM Modem Chip Set	52	10 (Real or Complex)	1 - 4096	<.013	Yes	I, Q, ISoft, QSoft	RRC ($\alpha \approx 0.4$) or Integrate and Dump	Yes	Yes	3651 and 3652
HSP50110	Digital Quadrature Tuner	52	10 (Real or Complex)	1 - 4096	<.013	Yes	I, Q	Third Order CIC	Yes	N/A	3651

PART NUMBER	DESCRIPTION	CLOCK (MSPS)	DATA (BITS)	MODULATION TECHNIQUES	CARRIER TRACKING IF FREQUENCY	4-TAP ADAPTIVE EQUALIZER	CARRIER RECOVERY LOOP	SYMBOL TRACKING	PACKAGE TYPE	(NOTE 9) AnswerFAX^{SM} DOC #
HSP50306	Digital QPSK Demodulator	2.048	6	QPSK	10.7MHz	Yes	Yes	Yes	SOIC	4162

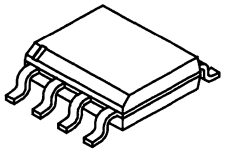
PART NUMBER	DESCRIPTION	DATA RATE	MODULATION TECHNIQUES	PROGRAMMABLE CARRIER FREQUENCY	FILTER	SYNTHESIZER	OUTPUT POWER	PACKAGE TYPE	(NOTE 9) AnswerFAX^{SM} DOC #
HSP50307	QPSK Burst	256 KBPS	QPSK	8 - 15MHz	RRC ($\alpha = 0.5$)	Yes	22 - 62dBmV	SOIC	4219

NOTE:

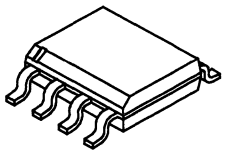
9. For complete data sheets by fax, call Harris AnswerFAX^{SM} at (407) 724-7800 and enter this document number.

Power MOSFET Selection Guide

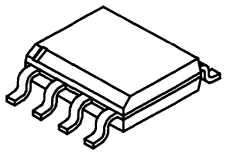
N-CHANNEL MOSFETs

MAXIMUM RATINGS			
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	 MS-012AA
30	3.5	2 x 0.06	RF1K49086
30	6.3	0.03	RF1K49157
60	2.0	2 x 0.13	RF1K49154

N-CHANNEL LOGIC LEVEL DEVICES

MAXIMUM RATINGS			
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	 MS-012AA
12	2.5/3.5	0.05/0.13 (COMP N&P)	RF1K49092
12	3.5	2 x 0.05	RF1K49090
30	3.5	2 x 0.06	RF1K49088
30	6.3	0.030	RF1K49156

P-CHANNEL LOGIC LEVEL DEVICES

MAXIMUM RATINGS			
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	 MS-012AA
12	2.5/3.5	0.05/0.13 (COMP N&P)	RF1K49092
12	3.5	2 x 0.13	RF1K49093

HI5721

January 1997

10-Bit, 125 MSPS High Speed D/A Converter

Features

- 125 MSPS Throughput Rate
- Low Power - 700mW
- 1.5 LSB Integral Linearity Error
- Low Glitch Energy - 1.5pV-s
- TTL/CMOS Compatible Inputs
- Improved Hold Time - 0.5ns
- Excellent Spurious Free Dynamic Range
- Improved Second Source for the AD9721

Applications

- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- HDTV
- Test Equipment
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

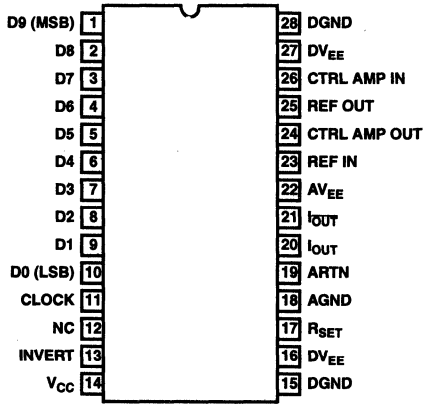
The HI5721 is a 10-bit 125 MSPS high speed D/A converter. The converter incorporates a 10-bit input data register with quadrature data logic capability, and current outputs. The HI5721 features low glitch energy and excellent frequency domain specifications.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5721BIP	-40 to 85	28 Ld PDIP (600 mil)	E28.6
HI5721BIB	-40 to 85	28 Ld SOIC (W)	M28.3
HI5721-EVP	25	Evaluation Board (PDIP)	
HI5721-EVS	25	Evaluation Board (SOIC)	

Pinout

HI5721
(PDIP, SOIC)
TOP VIEW



HARRIS SEMICONDUCTOR

HI5731

January 1997

12-Bit, 100 MSPS High Speed D/A Converter

Features

- 100 MSPS Throughput Rate
- Low Power 650mW
- 0.75 LSB Integral Linearity Error
- Low Glitch Energy 3.0pV-s
- TTL/CMOS Compatible Inputs
- Improved Hold Time 0.25ns
- Excellent Spurious Free Dynamic Range

Applications

- Cellular Base Stations
- GSM Base Stations
- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- Test Equipment
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

Description

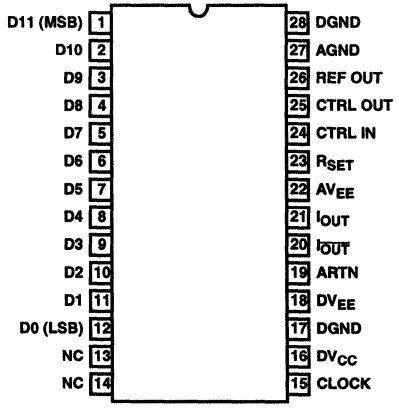
The HI5731 is a 12-bit, 100 MSPS D/A converter which is implemented in the Harris BiCMOS 10V (HBC-10) process. Operating from +5V and -5.2V, the converter provides -20.48mA of full scale output current and includes an input data register and bandgap voltage reference. Low glitch energy and excellent frequency domain performance are achieved using a segmented architecture. The digital inputs are TTL/CMOS compatible and translated internally to ECL. All internal logic is implemented in ECL to achieve high switching speed with low noise. The addition of laser trimming assures 12-bit linearity is maintained along the entire transfer curve.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5731BIP	-40 to 85	28 Ld PDIP	E28.6
HI5731BIB	-40 to 85	28 Ld SOIC	M28.3
HI5731-EVP	25	Evaluation Board (PDIP)	
HI5731-EVS	25	Evaluation Board (SOIC)	

Pinout

HI5731
(PDIP, SOIC)
TOP VIEW



File Number 4070.2

HARRIS SEMICONDUCTOR

HI5741

January 1997

14-Bit, 100 MSPS High Speed D/A Converter

Features

- 100 MSPS Throughput Rate
- Low Power - 650mW
- 1.0 LSB Integral Linearity Error
- Low Glitch Energy - 1.0pV-s
- TTL/CMOS Compatible Inputs
- Improved Hold Time - 0.25ns
- Excellent Spurious Free Dynamic Range

Applications

- Cellular Base Stations
- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- Test Equipment
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

Description

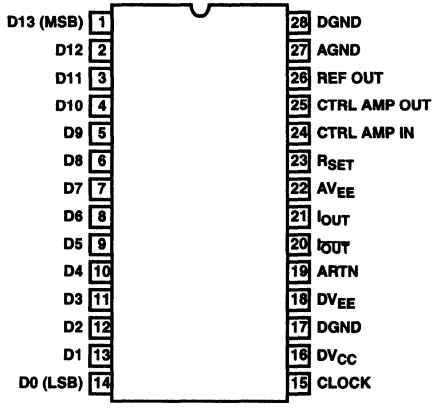
The HI5741 is a 14-bit, 100 MSPS D/A converter which is implemented in the Harris BiCMOS 10V (HBC-10) process. Operating from +5V and -5.2V, the converter provides 20.48mA of full scale output current and includes an input data register and bandgap voltage reference. Low glitch energy and excellent frequency domain performance are achieved using a segmented architecture. The digital inputs are TTL/CMOS compatible and translated internally to ECL. All internal logic is implemented in ECL to achieve high switching speed with low noise. The addition of laser trimming assures 14-bit linearity is maintained along the entire transfer curve.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5741BIP	-40 to 85	28 Ld PDIP	E28.6
HI5741BIB	-40 to 85	28 Ld SOIC	M28.3
HI5741-EVS	25	Evaluation Board (SOIC)	

Pinout

HI5741
(PDIP, SOIC)
TOP VIEW



5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 4071.2

HARRIS SEMICONDUCTOR

HI5780, CXD2306

10-Bit, 80 MSPS High Speed, Low Power D/A Converter

January 1997

Features

- 80 MSPS Throughput Rate
- Low Power - 150mW
- ±0.5 LSB Differential Linearity Error
- TTL/CMOS Compatible Inputs
- Built in Bandgap Voltage Reference
- Power Down and Blanking Control Pins

Applications

- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- Test Equipment
- High Resolution Imaging and Graphics Systems
- Arbitrary Waveform Generators

Description

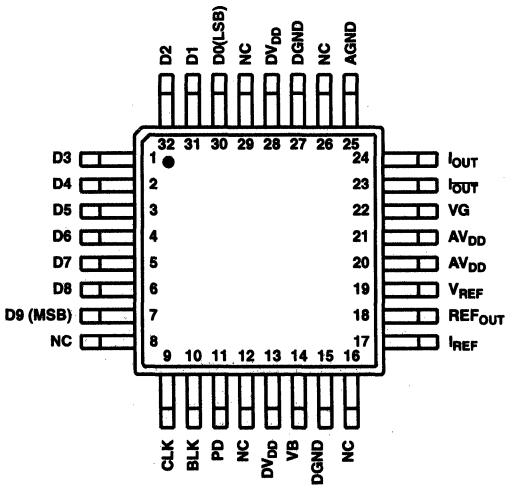
The HI5780, CXD2306 is a 10-bit 80MHz high speed, low power D/A converter. The converter incorporates a 10-bit input data register with current outputs. The HI5780, CXD2306 includes a power down feature that reduces power consumption and a blanking control. The on-chip bandgap reference can be used to set the output current range of the D/A.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5780JCQ, CXD2306Q	-20 to 75	32 Ld MQFP	Q32.7x7-S
HI5780-EV	25	Evaluation Kit	

Pinout

HI5780, CXD2306
(MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4024.3**

HARRIS SEMICONDUCTOR

HI20201, CX20201-1, CX20202-1

10-Bit, 160 MSPS Ultra High-Speed D/A Converter

January 1997

Features

- 160 MSPS Throughput Rate
- 10-Bit (HI20201, CX20201-1, CX20202-1) Resolution
- 0.5 LSB Differential Linearity Error
- Low Glitch Noise
- Analog Multiplying Function
- Low Power Consumption 420mW
- Evaluation Board Available

Applications

- Wireless Communications
- Signal Reconstruction
- Direct Digital Synthesis
- High Definition Video Systems
- Digital Measurement Systems
- Radar

Description

The HI20201, CX20201-1, CX20202-1 is a 160MHz ultra high speed D/A converter. The converter is based on an R/2R switched current source architecture that includes an input data register with a complement feature and is Emitter Coupled Logic (ECL) compatible.

The HI20201, CX20201-1, CX20202-1 is a 10-bit accurate D/A with a linearity error of 1 LSB.

The HI20201, CX20201-1, CX20202-1 is available in a commercial temperature range and are offered in a 28 lead plastic SOIC (300 mil) and a 28 lead plastic DIP package.

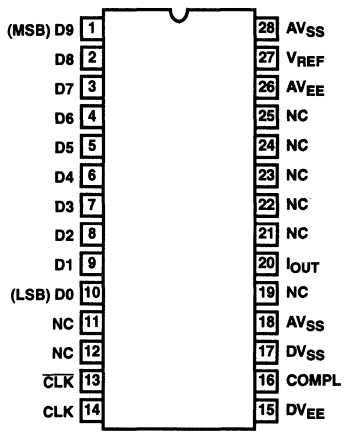
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI20201JCB, CX20201A-1	-20 to 75	28 Ld SOIC	M28.3A-S
HI20201JCP, CX20202A-1	-20 to 75	28 Ld PDIP	E28.6A-S
HI20201-EV	25	Evaluation Kit	

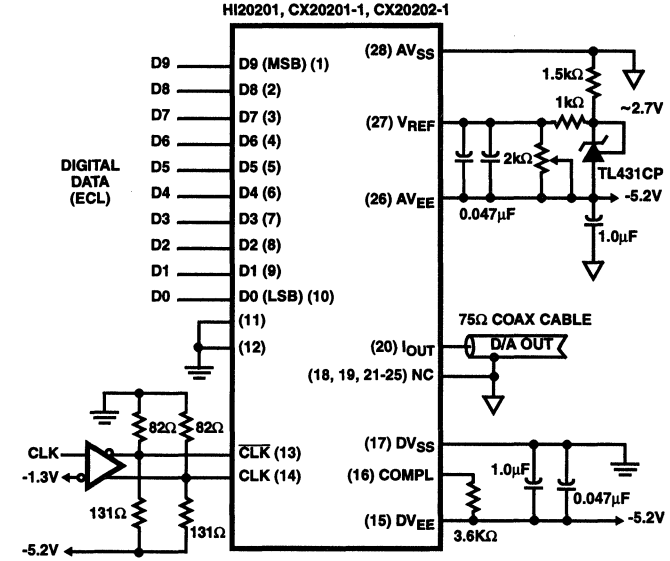
5 STANDARD PRODUCTS

Pinout

HI20201, CX20201-1, CX20202-1
(PDIP, SOIC)
TOP VIEW



Typical Applications Circuit



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3581.4

HARRIS SEMICONDUCTOR

HI5703

January 1997

10-Bit, 40 MSPS A/D Converter

Features

- 40 MSPS Sampling Rate
- 8.55 Bits Guaranteed at f_{IN} = 10MHz
- Low Power
- Wide 250MHz Full Power Input Bandwidth
- On Chip Sample and Hold
- Fully Differential or Single-Ended Analog Input
- Single +5V Supply Voltage
- TTL Compatible Interface
- 3.3V Digital Outputs Available
- Evaluation Board Available (HI5703EVAL)

Applications

- Professional Video Digitizing
- Medical Imaging
- Digital Communication Systems
- High Speed Data Acquisition
- Additional Reference Documents
  - AN9534 Using the HI5703 Evaluation Board
  - AN9413 Driving the Analog Input of the HI5702
  - AN9214 Using Harris High Speed A/D Converters

Description

The HI5703 is a monolithic, 10-bit, analog-to-digital converter fabricated in Harris's BiCMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 40 MSPS speed is made possible by a fully differential pipeline architecture with an internal sample and hold.

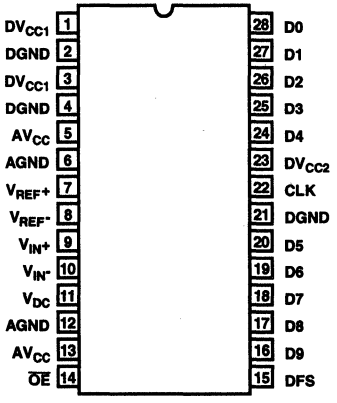
The HI5703 has excellent dynamic performance while consuming only 400mW power at 40 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles. It is pin-to-pin compatible with the HI5702.

Ordering Information

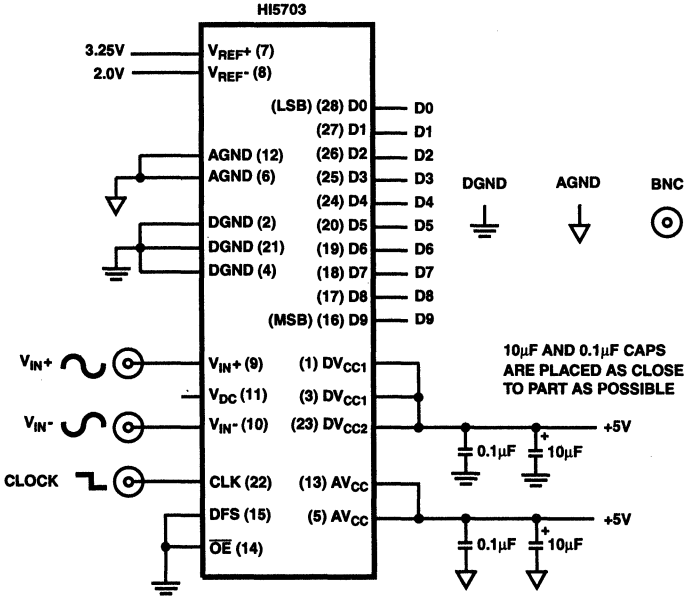
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5703KCB	0 to 70	28 Ld SOIC (W)	M28.3
HI5703EVAL	25	Evaluation Board	

Pinout

HI5703 (SOIC)
TOP VIEW



Typical Application Schematic



File Number 3950.5

HI5710A, CXD2310A

January 1997

10-Bit, 20 MSPS A/D Converter

Features

- Resolution 10-Bit ±0.5 LSB (DNL)
- Maximum Sampling Frequency 20 MSPS
- Low Power Consumption 150mW (Reference Current Excluded)
- Standby Mode Power 5mW
- No Sample and Hold Required
- TTL Compatible Inputs
- Three-State TTL Compatible Outputs
- Single +5V Analog Power Supply
- Single +3.3V or +5V Digital Power Supply

Applications

- Video Digitizing - Multimedia
- Data Communications
- Image Scanners
- Medical Imaging
- Video Recording Equipment
- Camcorders
- QAM Demodulation

Description

The HI5710A, CXD2310A is a low power, 10-bit, CMOS analog-to-digital converter. The use of a 2-step architecture realizes low power consumption, 150mW, and a maximum conversion speed of 20MHz with only a 3 clock cycle data latency. The HI5710A, CXD2310A can be powered down, disabling the chip and the digital outputs, reducing power to less than 5mW. A built-in, user controllable, calibration circuit is used to provide low linearity error, 1 LSB. The low power, high speed and small package outline make the HI5710A, CXD2310A an ideal choice for CCD, battery, and high channel count applications.

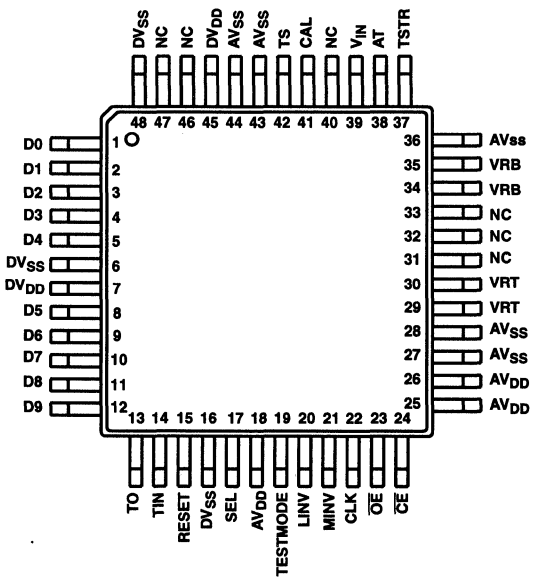
The HI5710A, CXD2310A does not require an external sample and hold but requires an external reference and includes force and sense reference pins for increased accuracy. The digital outputs can be inverted, with the MSB controlled separately, allowing for various digital output formats. The HI5710A, CXD2310A includes a test mode where the digital outputs can be set to a fixed state to ease in-circuit testing.

Ordering Information

PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5710AJCQ, CXD2310AR	0 to 75	48 Ld MQFP	Q48.7x7-S

Pinout

HI5710A, CXD2310A (MQFP)
TOP VIEW



HARRIS SEMICONDUCTOR

HI5746

January 1997

10-Bit, 40 MSPS A/D Converter

Features

- 40 MSPS Sampling Rate
- 8.8 Bits at f_{IN} = 10MHz
- Low Power 225mW at 40 MSPS
- Wide 250MHz Full Power Input Bandwidth
- On Chip Sample and Hold
- Fully Differential or Single-Ended Analog Input
- Single +5V Supply Voltage
- TTL/CMOS Compatible Digital Inputs
- 3.0/5.0V CMOS Compatible Digital Outputs
- Offset Binary or Two's Complement Output Format

Applications

- Professional Video Digitizing
- Medical Imaging
- Digital Communication Systems
- High Speed Data Acquisition

Description

The HI5746 is a monolithic, 10-bit, analog-to-digital converter fabricated in a CMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 40 MSPS speed is made possible by a fully differential pipelined architecture with an internal sample and hold.

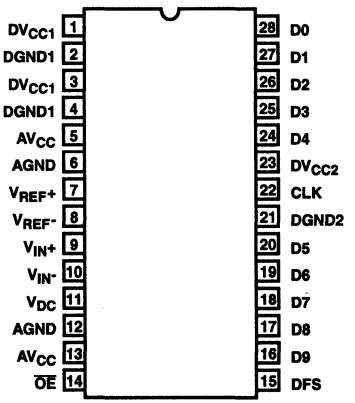
The HI5746 has excellent dynamic performance while consuming only 225mW power at 40 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles. It is pin-for-pin functionally compatible with the HI5702 and the HI5703.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5746KCB	0 to 70	28 Ld SOIC (W)	M28.3
HI5746EVAL1	25	Evaluation Board	

Pinout

HI5746 (SOIC)
TOP VIEW



File Number 4129.2

HARRIS SEMICONDUCTOR

HI5766

January 1997

10-Bit, 60 MSPS A/D Converter

Features

- 60 MSPS Sampling Rate
- 8.3 Bits at f_{IN} = 10MHz
- Low Power 260mW at 60 MSPS
- Wide 250MHz Full Power Input Bandwidth
- On Chip Sample and Hold
- Fully Differential or Single-Ended Analog Input
- Single +5V Supply Voltage
- TTL/CMOS Compatible Digital Inputs
- 3.0/5.0V CMOS Compatible Digital Outputs
- Offset Binary or Two's Complement Output Format

Applications

- Professional Video Digitizing
- Medical Imaging
- Digital Communication Systems
- High Speed Data Acquisition

Description

The HI5766 is a monolithic, 10-bit, analog-to-digital converter fabricated in a CMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 60 MSPS speed is made possible by a fully differential pipelined architecture with an internal sample and hold.

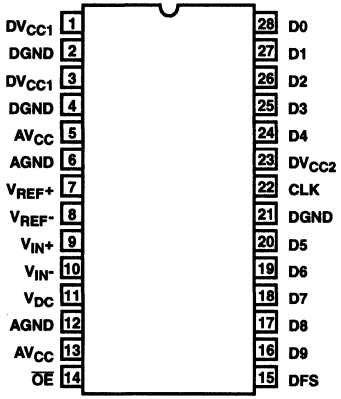
The HI5766 has excellent dynamic performance while consuming only 260mW power at 60 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles. It is pin-for-pin functionally compatible with the HI5702, HI5703 and the HI5746.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5766KCB	0 to 70	28 Ld SOIC (W)	M28.3
HI5766EVAL1	25	Evaluation Board	

Pinout

HI5766 (SOIC)
TOP VIEW



5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 4130.2

HARRIS SEMICONDUCTOR

HI5800

January 1997

12-Bit, 3 MSPS Sampling A/D Converter

Features

- 3 MSPS Throughput Rate
- 12-Bit, No Missing Codes Over Temperature
- 1.0 LSB Integral Linearity Error
- Buffered Sample and Hold Amplifier
- Precision Voltage Reference
- ±2.5V Input Signal Range
- 20MHz Input BW Allows Sampling Beyond Nyquist
- Zero Latency/No Pipeline Delay
- Evaluation Board Available

Applications

- High Speed Data Acquisition Systems
- Medical Imaging
- Radar Signal Analysis
- Document and Film Scanners
- Vibration/Waveform Spectrum Analysis
- Digital Servo Control

Description

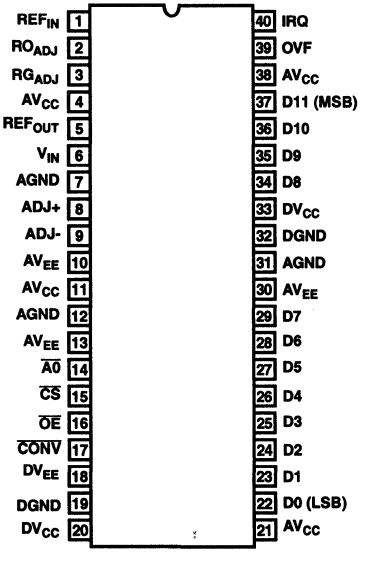
The HI5800 is a monolithic, 12-bit, sampling Analog-to-Digital Converter fabricated in the HBC10 BiCMOS process. It is a complete subsystem containing a sample and hold amplifier, voltage reference, two-step subranging A/D, error correction, control logic, and timing generator. The HI5800 is designed for high speed applications where wide bandwidth, accuracy and low distortion are essential.

Ordering Information

PART NUMBER	LINEARITY	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5800BID	±1 LSB	-40 to 85	40 Ld SBDIP	D40.6
HI5800JCD HI5800KCD	±2 LSB ±1 LSB	0 to 70	40 Ld SBDIP	D40.6
HI5800-EV		25	Evaluation Board	

Pinout

HI5800
(SBDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2938.9**

HARRIS SEMICONDUCTOR

HI5804

January 1997

12-Bit, 5 MSPS A/D Converter

Features

- 5 MSPS Sampling Rate
- Low Power
- Internal Sample and Hold
- Fully Differential Architecture
- 100MHz Full Power Input Bandwidth
- Low Distortion
- Internal Reference
- TTL/CMOS Compatible Digital I/O
- 3V to 5V Digital Outputs

Applications

- High Speed Data Acquisition Systems
- Digital IF Communication Systems
- Document and Film Scanners
- Medical Imaging
- Radar Signal Analysis
- Vibration/Waveform Spectrum Analysis
- Digital Servo Loop Control
- Reference Literature
  - AN9214 Using Harris High Speed Converters

Description

The HI5804 is a monolithic, 12-bit, Analog-to-Digital Converter fabricated in Harris' HBC10 BiCMOS process. It is designed for high speed, high resolution applications where wide bandwidth and low power consumption are essential.

The HI5804 is designed in a fully differential pipelined architecture with a front end differential-in-differential-out sample-and-hold (S/H). The HI5804 has excellent dynamic performance while consuming 300mW power at 5 MSPS.

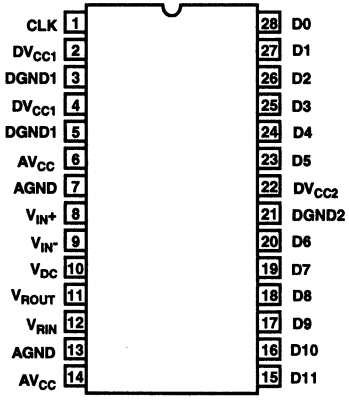
The 100MHz full power input bandwidth is ideal for communication systems and document scanner applications. Data output latches are provided which present valid data to the output bus with a latency of 3 clock cycles. The digital outputs have a separate supply pin which can be powered from a 3.0V to 5.0V supply.

Ordering Information

PART NUMBER	SAMPLE RATE	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5804KCB	5 MSPS	0 to 70	28 Ld SOIC	M28.3

Pinout

HI5804
(SOIC)
TOP VIEW



5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 4026.2

HARRIS SEMICONDUCTOR

HI5805

January 1997

12-Bit, 5 MSPS A/D Converter

Features

- 5 MSPS Sampling Rate
- Low Power
- Internal Sample and Hold
- Fully Differential Architecture
- 100MHz Full Power Input Bandwidth
- Low Distortion
- Internal Voltage Reference
- TTL/CMOS Compatible Digital I/O
- 5V to 3.0V Digital Outputs

Applications

- Digital Communication Systems
- Undersampling Digital IF
- Document Scanners
- Additional Reference Documents
  - AN9214 Using Harris High Speed A/D Converters

Description

The HI5805 is a monolithic, 12-bit, Analog-to-Digital Converter fabricated in Harris' HBC10 BiCMOS process. It is designed for high speed, high resolution applications where wide bandwidth and low power consumption are essential.

The HI5805 is designed in a fully differential pipelined architecture with a front end differential-in-differential-out sample-and-hold (S/H). The HI5805 has excellent dynamic performance while consuming 300mW power at 5 MSPS.

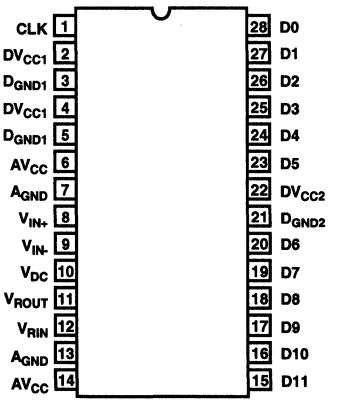
The 100MHz full power input bandwidth is ideal for communication systems and document scanner applications. Data output latches are provided which present valid data to the output bus with a latency of 3 clock cycles. The digital outputs have a separate supply pin which can be powered from a 3.0V to 5.0V supply.

Ordering Information

PART NUMBER	SAMPLE RATE	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5805BIB	5 MSPS	-40 to 85	28 Ld SOIC (W)	M28.3
HI5805EVAL1		25	Evaluation Board	

Pinout

HI5805 (SOIC)
TOP VIEW



HI5808

October 1996

12-Bit, 10 MSPS A/D Converter

Features

- 10 MSPS Sampling Rate
- Low Power
- Internal Sample and Hold
- Fully Differential Architecture
- 100MHz Full Power Input Bandwidth
- Low Distortion
- Internal Voltage Reference
- TTL/CMOS Compatible Digital I/O
- 5V to 3.0V Digital Outputs

Applications

- Digital Communication Systems
- Undersampling Digital IF
- Document Scanners
- Additional Reference Documents
  - AN9214 Using Harris High Speed A/D Converters

Description

The HI5808 is a monolithic, 12-bit, Analog-to-Digital Converter fabricated in Harris' HBC10 BiCMOS process. It is designed for high speed, high resolution applications where wide bandwidth and low power consumption are essential.

The HI5808 is designed in a fully differential pipelined architecture with a front end differential-in-differential-out sample-and-hold (S/H). The HI5808 has excellent dynamic performance while consuming 325mW power at 10 MSPS.

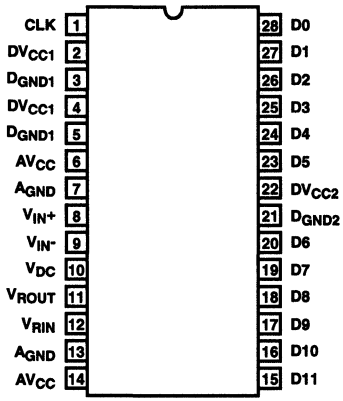
The 100MHz full power input bandwidth is ideal for communication systems and document scanner applications. Data output latches are provided which present valid data to the output bus with a latency of 3 clock cycles. The digital outputs have a separate supply pin which can be powered from a 3.0V to 5.0V supply.

Ordering Information

PART NUMBER	SAMPLE RATE	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5808BIB	10 MSPS	-40 to 85	28 Ld SOIC	M28.3

Pinout

HI5808
(SOIC)
TOP VIEW



5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 4233.1

HARRIS SEMICONDUCTOR

CA3045, CA3046

General Purpose NPN Transistor Arrays

November 1996

Features

- Two Matched Transistors
  - V_{BE} Match ..... ±5mV
  - I_{IO} Match ..... 2μA (Max)
- Low Noise Figure ..... 3.2dB (Typ) at 1kHz
- 5 General Purpose Monolithic Transistors
- Operation From DC to 120MHz
- Wide Operating Current Range
- Full Military Temperature Range

Applications

- Three Isolated Transistors and One Differentially Connected Transistor Pair for Low Power Applications at Frequencies from DC Through the VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- See Application Note, AN5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for Suggested Applications

Description

The CA3045 and CA3046 each consist of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

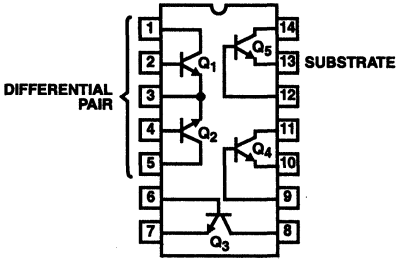
The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3045	-55 to 125	14 Ld SBDIP	D14.3
CA3045F	-55 to 125	14 Ld CERDIP	F14.3
CA3046	-55 to 125	14 Ld PDIP	E14.3
CA3046M (3046)	-55 to 125	14 Ld SOIC	M14.15
CA3046M96 (3046)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15

Pinout

CA3045, (CERDIP, SBDIP)
CA3046 (PDIP, SOIC)
TOP VIEW



HARRIS SEMICONDUCTOR

CA3081, CA3082

General Purpose High Current NPN Transistor Arrays

November 1996

Features

- CA3081 - Common Emitter Array
- CA3082 - Common Collector Array
- Directly Drive Seven Segment Incandescent Displays and Light Emitting Diode (LED) Display
- 7 Transistors Permit a Wide Range of Applications in Either a Common Emitter (CA3081) or Common Collector (CA3082) Configuration
- High I_C ..... 100mA (Max)
- Low V_{CESAT} (at 50mA) ..... 0.4V (Typ)

Applications

- Drivers for
  - Incandescent Display Devices
  - LED Displays
  - Relay Control
- Thyristor Firing

Description

CA3081 and CA3082 consist of seven high current (to 100mA) silicon NPN transistors on a common monolithic substrate. The CA3081 is connected in a common emitter configuration and the CA3082 is connected in a common collector configuration.

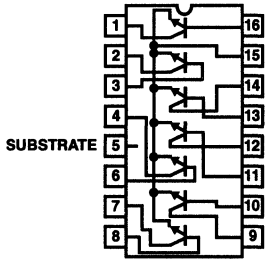
The CA3081 and CA3082 are capable of directly driving seven segment displays, and light emitting diode (LED) displays. These types are also well suited for a variety of other drive applications, including relay control and thyristor firing.

Ordering Information

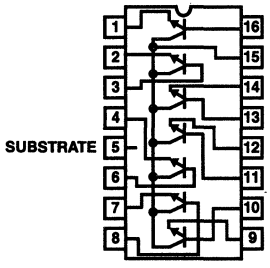
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3081	-55 to 125	16 Ld PDIP	E16.3
CA3081F	-55 to 125	16 Ld CERDIP	F16.3
CA3081M (3081)	-55 to 125	16 Ld SOIC	M16.15
CA3081M96 (3081)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15
CA3082	-55 to 125	16 Ld PDIP	E16.3
CA3082F	-55 to 125	16 Ld CERDIP	F16.3
CA3082M (3082)	-55 to 125	16 Ld SOIC	M16.15
CA3082M96 (3082)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15

Pinouts

CA3081
COMMON EMITTER CONFIGURATION
(PDIP, CERDIP, SOIC)
TOP VIEW



CA3082
COMMON COLLECTOR CONFIGURATION
(PDIP, CERDIP, SOIC)
TOP VIEW



5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **480.3**

CA3083

General Purpose High Current NPN Transistor Array

September 1996

Features

- High I_C ..... 100mA (Max)
- Low $V_{CE\ sat}$ (at 50mA) ..... 0.7V (Max)
- Matched Pair (Q_1 and Q_2)
  - V_{IO} (V_{BE} Match) ..... ±5mV (Max)
  - I_{IO} (at 1mA) ..... 2.5µA (Max)
- 5 Independent Transistors Plus Separate Substrate Connection

Applications

- Signal Processing and Switching Systems Operating from DC to VHF
- Lamp and Relay Driver
- Differential Amplifier
- Temperature Compensated Amplifier
- Thyristor Firing
- See Application Note AN5296 "Applications of the CA3018 Circuit Transistor Array" for Suggested Applications

Description

The CA3083 is a versatile array of five high current (to 100mA) NPN transistors on a common monolithic substrate. In addition, two of these transistors (Q_1 and Q_2) are matched at low current (i.e., 1mA) for applications in which offset parameters are of special importance.

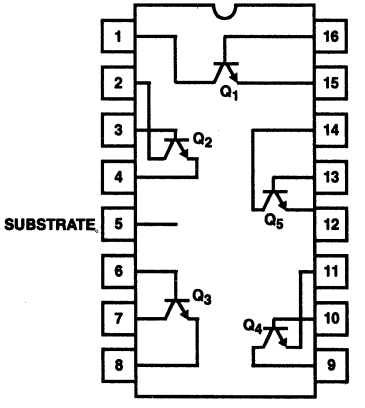
Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3083	-55 to 125	16 Ld PDIP	E16.3
CA3083F	-55 to 125	16 Ld CERDIP	F16.3
CA3083M (3083)	-55 to 125	16 Ld SOIC	M16.15
CA3083M96 (3083)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15

Pinout

CA3083
(PDIP, CERDIP, SOIC)
TOP VIEW



File Number 481.3

CA3086

General Purpose NPN Transistor Array

November 1996

Applications

- **Three Isolated Transistors and One Differentially Connected Transistor Pair For Low-Power Applications from DC to 120MHz**
- **General-Purpose Use in Signal Processing Systems Operating in the DC to 190MHz Range**
- **Temperature Compensated Amplifiers**
- **See Application Note, AN5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for Suggested Applications**

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3086	-55 to 125	14 Ld PDIP	E14.3
CA3086M (3086)	-55 to 125	14 Ld SOIC	M14.15
CA3086M96 (3086)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15
CA3086F	-55 to 125	14 Ld CERDIP	F14.3

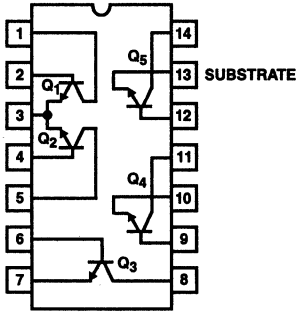
Description

The CA3086 consists of five general-purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching

Pinout

CA3086
(PDIP, CERDIP, SOIC)
TOP VIEW



5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **483.3**

CA3096, CA3096A, CA3096C

NPN/PNP Transistor Arrays

August 1996

Applications

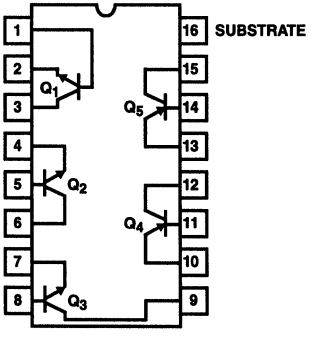
- **Five-Independent Transistors**
  - **Three NPN and**
  - **Two PNP**
- **Differential Amplifiers**
- **DC Amplifiers**
- **Sense Amplifiers**
- **Level Shifters**
- **Timers**
- **Lamp and Relay Drivers**
- **Thyristor Firing Circuits**
- **Temperature Compensated Amplifiers**
- **Operational Amplifiers**

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3096AE	-55 to 125	16 Ld PDIP	E16.3
CA3096AM (3096A)	-55 to 125	16 Ld SOIC	M16.15
CA3096AM96 (3096A)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15
CA3096CE	-55 to 125	16 Ld PDIP	E16.3
CA3096E	-55 to 125	16 Ld PDIP	E16.3
CA3096M (3096)	-55 to 125	16 Ld SOIC	M16.15
CA3096M96 (3096)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15

Pinout

CA3096, CA3096A, CA3096C
(PDIP, SOIC)
TOP VIEW



Description

The CA3096C, CA3096, and CA3096A are general purpose high voltage silicon transistor arrays. Each array consists of five independent transistors (two PNP and three NPN types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096A, CA3096, and CA3096C are identical, except that the CA3096A specifications include parameter matching and greater stringency in I_{CBO}, I_{CEO}, and $V_{CE}(SAT)$. The CA3096C is a relaxed version of the CA3096.To type this body text, simply triple click this paragraph and begin typing. The paragraph tag for this area is called body.

CA3096, CA3096A, CA3096C Essential Differences

CHARACTERISTIC		CA3096A	CA3096	CA3096C
$V_{(BR)CEO}$ (V) (Min)				
	NPN	35	35	24
	PNP	-40	-40	-24
$V_{(BR)CBO}$ (V) (Min)				
	NPN	45	45	30
	PNP	-40	-40	-24
h_{FE} at 1mA				
	NPN	150-500	150-500	100-670
	PNP	20-200	20-200	15-200
h_{FE} at 100µA				
	PNP	40-250	40-250	30-300
I_{CBO} (nA) (Max)				
	NPN	40	100	100
	PNP	-40	-100	-100
I_{CEO} (nA) (Max)				
	NPN	100	1000	1000
	PNP	-100	-1000	-1000
$V_{CE\ SAT}$ (V) (Max)				
	NPN	0.5	0.7	0.7
$\|V_{IO}\|$ (mV) (Max)				
	NPN	5	-	-
	PNP	5	-	-
$\|I_{IO}\|$ (µA) (Max)				
	NPN	0.6	-	-
	PNP	0.25	-	-

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **595.3**

CA3127

August 1996

High Frequency NPN Transistor Array

Features

- Gain Bandwidth Product (f_T) . . . . . >1GHz
- Power Gain . . . . . 30dB (Typ) at 100MHz
- Noise Figure . . . . . 3.5dB (Typ) at 100MHz
- Five Independent Transistors on a Common Substrate

Applications

- VHF Amplifiers
- Multifunction Combinations - RF/Mixer/Oscillator
- Sense Amplifiers
- Synchronous Detectors
- VHF Mixers
- IF Converter
- IF Amplifiers
- Synthesizers
- Cascade Amplifiers

Description

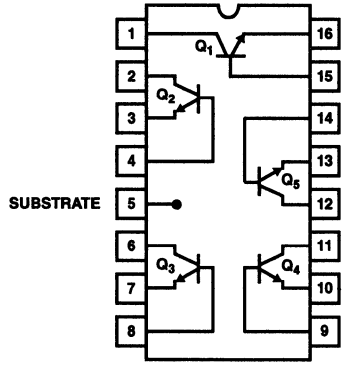
The CA3127 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1GHz, making the CA3127 useful from DC to 500MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127 provides close electrical and thermal matching of the five transistors.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3127E	-55 to 125	16 Ld PDIP	E16.3
CA3127M (3127)	-55 to 125	16 Ld SOIC	M16.15
CA3127M96 (3127)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15

Pinout

CA3127
(PDIP, SOIC)
TOP VIEW



5 STANDARD PRODUCTS

File Number 662.3

CA3146, CA3146A, CA3183, CA3183A

August 1996

High-Voltage Transistor Arrays

Features

- Matched General Purpose Transistors
  - V_{BE} Match ..... ±5mV (Max)
- Operation from DC to 120MHz (CA3146, CA3146A)
- Low Noise Figure 3.2dB (CA3146, CA3146A)
- High I_C ..... 75mA (Max) (CA3183, CA3183A)

Applications

- General Use in Signal Processing Systems in DC through VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- Lamp and Relay Drivers (CA3183, CA3183A)
- Thyristor Firing (CA3183, CA3183A)

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3146AE	-40 to 85	14 Ld PDIP	E14.3
CA3146AM (3146A)	-40 to 85	14 Ld SOIC	M14.15
CA3146AM96 (3146A)	-40 to 85	14 Ld SOIC Tape and Reel	M14.15
CA3146E	-40 to 85	14 Ld PDIP	E14.3
CA3146M (3146)	-40 to 85	14 Ld SOIC	M14.15
CA3146M96 (3146)	-40 to 85	14 Ld SOIC Tape and Reel	M14.15
CA3183AE	-40 to 85	16 Ld PDIP	E16.3
CA3183AM (3183A)	-40 to 85	16 Ld SOIC	M16.15
CA3183AM96 (3183A)	-40 to 85	16 Ld SOIC Tape and Reel	M16.15
CA3183E	-40 to 85	16 Ld PDIP	E16.3
CA3183M (3183)	-40 to 85	16 Ld SOIC	M16.15
CA3183M96 (3183)	-40 to 85	16 Ld SOIC Tape and Reel	M16.15

Description

The CA3146A, CA3146, CA3183A, and CA3183 are general purpose high voltage silicon NPN transistor arrays on a common monolithic substrate.

Types CA3146A and CA3146 consist of five transistors with two of the transistors connected to form a differentially connected pair. These types are recommended for low power applications in the DC through VHF range. (CA3146A and CA3146 are high voltage versions of the popular predecessor type CA3046.)

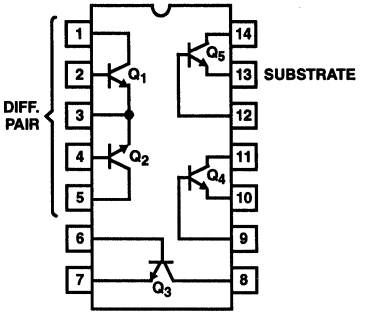
Types CA3183A and CA3183 consist of five high current transistors with independent connections for each transistor. In addition two of these transistors (Q_1 and Q_2) are matched at low current (i.e., 1mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design. (CA3183A and CA3183 are high voltage versions of the popular predecessor type CA3083.)

The types with an "A" suffix are premium versions of their non-"A" counterparts and feature tighter control of breakdown voltages making them more suitable for higher voltage applications.

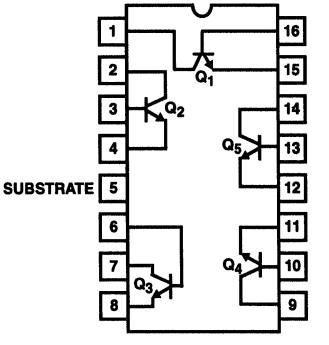
For detailed application information, see companion Application Note AN5296 "Application of the CA3018 Integrated Circuit Transistor Array."

Pinouts

CA3146, CA3146A (PDIP, SOIC)
TOP VIEW



CA3183, CA3183A (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **532.3**

CA3227, CA3246

August 1996

High-Frequency NPN Transistor Arrays For Low-Power Applications at Frequencies Up to 1.5GHz

Features

- Gain-Bandwidth Product (f_T) . . . . . >3GHz
- Five Transistors on a Common Substrate

Applications

- VHF Amplifiers
- VHF Mixers
- Multifunction Combinations - RF/Mixer/Oscillator
- IF Converter
- IF Amplifiers
- Sense Amplifiers
- Synthesizers
- Synchronous Detectors
- Cascade Amplifiers

Description

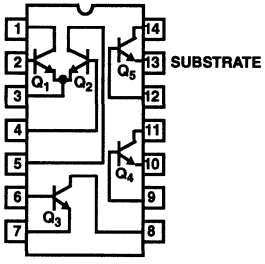
The CA3227 and CA3246 consist of five general purpose silicon NPN transistors on a common monolithic substrate. Each of the transistors exhibits a value of f_T in excess of 3GHz, making them useful from DC to 1.5GHz. The monolithic construction of these devices provides close electrical and thermal matching of the five transistors.

Ordering Information

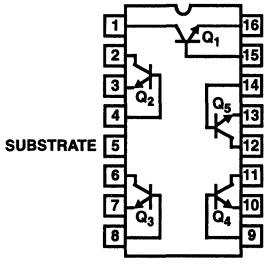
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3227E	-55 to 125	16 Ld PDIP	E16.3
CA3227M (3227)	-55 to 125	16 Ld SOIC	M16.15
CA3227M96 (3227)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15
CA3246E	-55 to 125	14 Ld PDIP	E14.3
CA3246M (3246)	-55 to 125	14 Ld SOIC	M14.15
CA3246M96 (3246)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15

Pinouts

CA3246
(PDIP, SOIC)
TOP VIEW



CA3227
(PDIP, SOIC)
TOP VIEW



5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1345.3**

HARRIS SEMICONDUCTOR

HFA1100, HFA1120

November 1996

850MHz, Low Distortion Current Feedback Operational Amplifiers

Features

- Low Distortion (30MHz, HD2) ..... -56dBc
- -3dB Bandwidth 850MHz
- Very Fast Slew Rate 2300V/µs
- Fast Settling Time (0.1%) 11ns
- Excellent Gain Flatness
  - (100MHz) ..... ±0.14dB
  - (50MHz) ..... ±0.04dB
  - (30MHz) ..... ±0.01dB
- High Output Current 60mA
- Overdrive Recovery ..... <10ns

Applications

- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems
- Related Literature
  - AN9420, Current Feedback Theory
  - AN9202, HFA11XX Evaluation Fixture

Description

The HFA1100, 1120 are a family of high-speed, wideband, fast settling current feedback amplifiers. Built with Harris' proprietary complementary bipolar UHF-1 process, these devices are the fastest monolithic amplifiers available from any semiconductor manufacturer.

The HFA1100 is a basic op amp with uncommitted pins 1, 5, and 8. The HFA1120 includes inverting input bias current adjust pins (pins 1 and 5) for adjusting the output offset voltage.

These devices offer a significant performance improvement over the AD811, AD9617/18, the CLC400-409, and the EL2070, EL2073, EL2030.

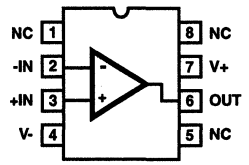
For Military grade product refer to the HFA1100/883, HFA1120/883 data sheet.

Ordering Information

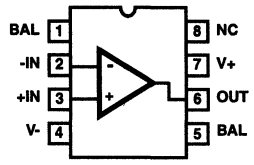
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1100MJ/883, HFA1120MJ/883	-55 to 125	8 Ld CERDIP	F8.3A
HFA1100IJ, HFA1120IJ	-40 to 85	8 Ld CERDIP	F8.3A
HFA1100IP, HFA1120IP	-40 to 85	8 Ld PDIP	E8.3
HFA1100IB, HFA1120IB (H1100I, H1120I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High-Speed Op Amps		

Pinouts

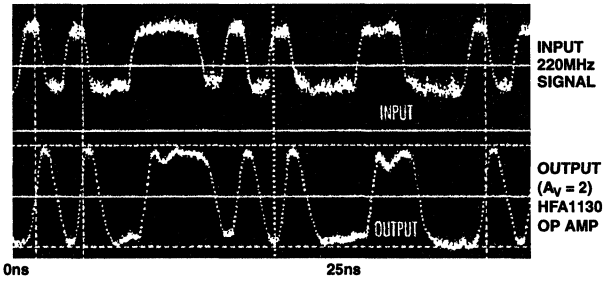
HFA1100
(PDIP, CERDIP, SOIC)
TOP VIEW



HFA1120
(PDIP, CERDIP, SOIC)
TOP VIEW



The Op Amps With Fastest Edges



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2945.5**

HARRIS SEMICONDUCTOR

HFA1102

600MHz Current Feedback Amplifier with Compensation Pin

November 1996

Features

- Compensation Pin for Bandwidth Limiting
- Low Distortion (HD2 at 30MHz) ..... -56dBc
- -3dB Bandwidth 600MHz
- Very Fast Slew Rate 2000V/µs
- Fast Settling Time (0.1%) 11ns
- Excellent Gain Flatness
  - (100MHz) ..... ±0.05dB
  - (50MHz) ..... ±0.02dB
  - (30MHz) ..... ±0.01dB
- High Output Current 60mA
- Overdrive Recovery ..... <10ns

Applications

- Low Noise Amplifiers
- Video Switching and Routing
- Pulse and Video Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems

Description

The HFA1102 is a high speed wideband current feedback amplifier featuring a compensation pin for bandwidth limiting. Built with Harris' proprietary complementary bipolar UHF-1 process, it has excellent AC performance and low distortion.

Because the HFA1102 is already unity gain stable, the primary purpose for limiting the bandwidth is to reduce the total noise (broadband) of the circuit. The bandwidth of the HFA1102 may be limited by connecting a capacitor and series damping resistor from pin 8 to ground. Typical bandwidths for various values of compensation capacitors are shown in the Electrical Specifications section of this datasheet.

A variety of packages and temperature grades are available. See the ordering information below for details.

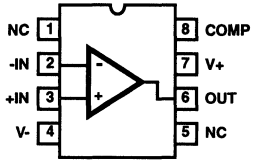
Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1102IJ	-40 to 85	8 Ld CERDIP	F8.3A
HFA1102IP	-40 to 85	8 Ld PDIP	E8.3
HFA1102IB (HI102I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps		

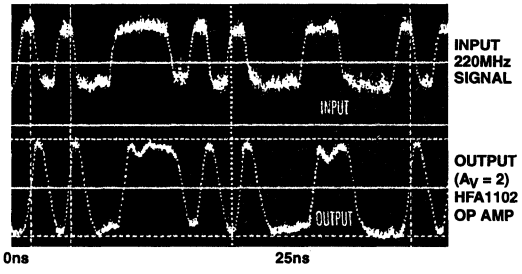
5 STANDARD PRODUCTS

Pinout

HFA1102
(PDIP, CERDIP, SOIC)
TOP VIEW



The Op Amps with Fastest Edges



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3597.2

HARRIS SEMICONDUCTOR

HFA1110

750MHz, Low Distortion Unity Gain, Closed Loop Buffer

November 1996

Features

- Wide -3dB Bandwidth 750MHz
- Very Fast Slew Rate..... 1300V/µs
- Fast Settling Time (0.2%) 7ns
- High Output Current 60mA
- Fixed Gain of +1
- Gain Flatness (100MHz)..... 0.03dB
- Differential Phase..... 0.025 Degrees
- Differential Gain..... 0.04%
- 3rd Harmonic Distortion (50MHz)..... -80dBc
- 3rd Order Intercept (100MHz) 30dBm

Applications

- Video Switching and Routing
- RF/IF Processors
- Driving Flash A/D Converters
- High-Speed Communications
- Impedance Transformation
- Line Driving
- Radar Systems

Description

The HFA1110 is a unity gain closed loop buffer that achieves -3dB bandwidth of 750MHz, while offering excellent video performance and low distortion. Manufactured on Harris' proprietary complementary bipolar UHF-1 process, the HFA1110 also offers very fast slew rate, and high output current. It is one more example of Harris' intent to enhance its leadership position in products for high speed signal processing applications.

The HFA1110's settling time of 11ns to 0.1%, low distortion and ability to drive capacitive loads make it an ideal flash A/D driver.

The HFA1110 is an enhanced, pin compatible upgrade for the AD9620, AD9630, CLC110, EL2072, BUF600 and BUF601.

For buffer applications requiring a standard op amp pinout, or selectable gain (-1, +1, +2), see the HFA1112 data sheet. For output limiting see the HFA1113 datasheet.

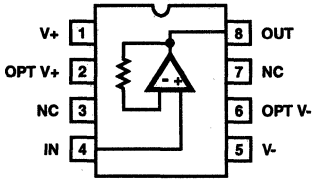
For military grade product please refer to the HFA1110/883 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HFA1110IJ	-40 to 85	8 Ld CERDIP	F8.3A
HFA1110IP	-40 to 85	8 Ld PDIP	E8.3
HFA1110IB (H1110I)	-40 to 85	8 Ld SOIC	M8.15
HFA1110EVAL	High Speed Buffer DIP Evaluation Board		

Pinout

HFA1110
(PDIP, CERDIP, SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
V+	1	Positive Supply
Opt V+	2	Optional Positive Supply
NC	3	No Connection
IN	4	Input
V-	5	Negative Supply
Opt V-	6	Optional Negative Supply
NC	7	No Connection
OUT	8	Output

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2944.5**

HFA1112

850MHz, Low Distortion Programmable Gain Buffer Amplifier

November 1996

Features

- User Programmable for Closed-Loop Gains of +1, -1 or +2 without Use of External Resistors
- Wide -3dB Bandwidth 850MHz
- Very Fast Slew Rate..... 2400V/μs
- Fast Settling Time (0.1%) 11ns
- High Output Current 60mA
- Excellent Gain Accuracy..... 0.99V/V
- Overdrive Recovery..... <10ns
- Standard Operational Amplifier Pinout

Applications

- RF/IF Processors
- Driving Flash A/D Converters
- High-Speed Communications
- Impedance Transformation
- Line Driving
- Video Switching and Routing
- Radar Systems
- Medical Imaging Systems
- Related Literature
  - AN9507, Video Cable Drivers Save Board Space

Description

The HFA1112 is a closed loop Buffer featuring user programmable gain and ultra high speed performance. Manufactured on Harris' proprietary complementary bipolar UHF-1 process, the HFA1112 offers a wide -3dB bandwidth of 850MHz, very fast slew rate, excellent gain flatness, low distortion and high output current.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components. Gain selection is accomplished via connections to the inputs, as described in the "Application Information" section. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

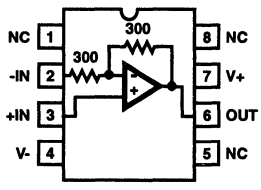
This amplifier is available with programmable output limiting as the HFA1113. For applications requiring a standard buffer pinout, please refer to the HFA1110 datasheet. For Military product, refer to the HFA1112/883 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1112IJ	-40 to 85	8 Ld CERDIP	F8.3A
HFA1112IP	-40 to 85	8 Ld PDIP	E8.3
HFA1112IB (H1112I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	High Speed Op Amp DIP Evaluation Board		

Pinout

HFA1112
(PDIP, CERDIP, SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1, 5, 8	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
OUT	6	Output
V+	7	Positive Supply

5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 2992.4

HFA1113

850MHz, Low Distortion, Output Limiting, Programmable Gain, Buffer Amplifier

November 1996

Features

- User Programmable Output Voltage Limiting
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Wide -3dB Bandwidth 850MHz
- Excellent Gain Flatness (to 100MHz) ..... ±0.07dB
- Low Differential Gain and Phase.... 0.02%/0.04 Degrees
- Low Distortion (HD3, 30MHz) ..... -73dBc
- Very Fast Slew Rate 2400V/µs
- Fast Settling Time (0.1%) 13ns
- High Output Current 60mA
- Excellent Gain Accuracy..... 0.99V/V
- Overdrive Recovery..... <1ns
- Standard Operational Amplifier Pinout

Applications

- RF/IF Processors
- Driving Flash A/D Converters
- High-Speed Communications
- Impedance Transformation
- Line Driving
- Video Switching and Routing
- Radar Systems
- Medical Imaging Systems

Description

The HFA1113 is a high speed Buffer featuring user programmable gain and output limiting coupled with ultra high speed performance. This buffer is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overload recovery times. The output limiting function allows the designer to set the maximum positive and negative output levels, thereby protecting later stages from damage or input saturation. The sub-nanosecond overdrive recovery time quickly returns the amplifier to linear operation following an overdrive condition.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components, as described in the "Application Information" section. Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

Component and composite video systems will also benefit from this buffer's performance, as indicated by the excellent gain flatness, and 0.02%/0.04 Degree Differential Gain/Phase specifications (R_L = 150Ω).

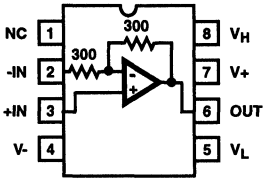
For Military product, refer to the HFA1113/883 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1113MJ/883	-55 to 125	8 Ld CERDIP	F8.3A
HFA1113IJ	-40 to 85	8 Ld CERDIP	F8.3A
HFA1113IP	-40 to 85	8 Ld PDIP	E8.3
HFA1113IB (H1113I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board For High Speed Op Amps		

Pinout

HFA1113
(PDIP, CERDIP, SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
V_L	5	Lower Output Limit
OUT	6	Output
V+	7	Positive Supply
V_H	8	Upper Output Limit

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1342.3**

HFA1114

November 1996

850MHz Video Cable Driving Buffer

Features

- Access to Summing Node Allows Circuit Customization
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Wide -3dB Bandwidth 850MHz
- Very Fast Slew Rate 2400V/µs
- Fast Settling Time (0.1%) 11ns
- High Output Current 60mA
- Excellent Gain Accuracy..... 0.99V/V
- Overdrive Recovery..... <10ns
- Standard Operational Amplifier Pinout

Applications

- RF/IF Processors
- Driving Flash A/D Converters
- High Speed Communications
- Impedance Transformation
- Line Driving
- Video Switching and Routing
- Radar Systems
- Medical Imaging Systems

Description

The HFA1114 is a closed loop Buffer featuring user programmable gain and ultra high speed performance. Manufactured on Harris' proprietary complementary bipolar UHF-1 process, the HFA1114 offers a wide -3dB bandwidth of 850MHz, very fast slew rate, excellent gain flatness, low distortion and high output current.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components. Gain selection is accomplished via connections to the inputs, as described in the "Application Information" section. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

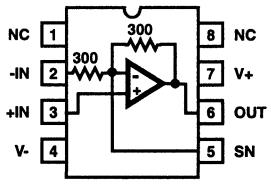
For applications requiring a standard buffer pinout, please refer to the HFA1110 datasheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1114IP	-40 to 85	8 Ld PDIP	E8.3
HFA1114IB (H1114I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps		

Pinout

HFA1114
(PDIP, SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1, 8	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
SN	5	Summing Node
OUT	6	Output
V+	7	Positive Supply

5 STANDARD PRODUCTS

File Number 3151.3

HARRIS SEMICONDUCTOR

HFA1130

850MHz, Output Limiting, Low Distortion Current Feedback Operational Amplifier

November 1996

Features

- User Programmable Output Voltage Limits
- Low Distortion (30MHz, HD2) ..... -56dBc
- -3dB Bandwidth 850MHz
- Very Fast Slew Rate 2300V/μs
- Fast Settling Time (0.1%) 11ns
- Excellent Gain Flatness
  - (100MHz) 0.14dB
  - (50MHz) 0.04dB
  - (30MHz) 0.01dB
- High Output Current 60mA
- Overdrive Recovery ..... <1ns

Applications

- Residue Amplifier
- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems
- Related Literature
  - AN9420, Current Feedback Theory
  - AN9202, HFA11XX Evaluation Fixture

Description

The HFA1130 is a high speed wideband current feedback amplifier featuring programmable output limits. Built with Harris' proprietary complementary bipolar UHF-1 process, it is the fastest monolithic amplifier available from any semiconductor manufacturer.

This amplifier is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overdrive recovery times. The output limiting function allows the designer to set the maximum positive and negative output levels, thereby protecting later stages from damage or input saturation. The sub-nanosecond overdrive recovery time quickly returns the amplifier to linear operation, following an overdrive condition.

The HFA1130 offers significant performance improvements over the CLC500/501/502.

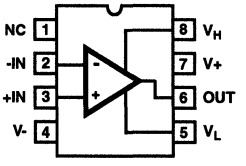
A variety of packages and temperature grades are available. See the ordering information below for details. For /883 product refer to the HFA1130/883 datasheet.

Ordering Information

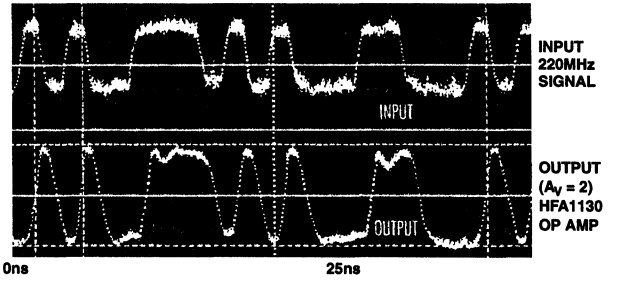
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1130MJ/883	-55 to 125	8 Ld CERDIP	F8.3A
HFA1130IJ	-40 to 85	8 Ld CERDIP	F8.3A
HFA1130IP	-40 to 85	8 Ld PDIP	E8.3
HFA1130IB (H1130I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High-Speed Op Amps		

Pinout

HFA1130
(PDIP, CERDIP, SOIC)
TOP VIEW



The Op Amps With Fastest Edges



File Number 3369.1

HFA3046, HFA3096, HFA3127, HFA3128

August 1996

Ultra High Frequency Transistor Arrays

Features

- NPN Transistor (f_T) 8GHz
- NPN Current Gain (h_{FE})..... 70
- NPN Early Voltage (V_A) 50V
- PNP Transistor (f_T)..... 5.5GHz
- PNP Current Gain (h_{FE})..... 40
- PNP Early Voltage (V_A) 25V
- Noise Figure (50Ω) at 1.0GHz 3.5dB
- Collector-to-Collector Leakage..... <1pA
- Complete Isolation Between Transistors
- Pin Compatible with Industry Standard 3XXX Series Arrays

Applications

- VHF/UHF Amplifiers
- VHF/UHF Mixers
- IF Converters
- Synchronous Detectors

Description

The HFA3046, HFA3096, HFA3127 and the HFA3128 are Ultra High Frequency Transistor Arrays that are fabricated from Harris Semiconductor's complementary bipolar UHF-1 process. Each array consists of five dielectrically isolated transistors on a common monolithic substrate. The NPN transistors exhibit a f_T of 8GHz while the PNP transistors provide a f_T of 5.5GHz. Both types exhibit low noise (3.5dB), making them ideal for high frequency amplifier and mixer applications.

The HFA3046 and HFA3127 are all NPN arrays while the HFA3128 has all PNP transistors. The HFA3096 is an NPN-PNP combination. Access is provided to each of the terminals for the individual transistors for maximum application flexibility. Monolithic construction of these transistor arrays provides close electrical and thermal matching of the five transistors.

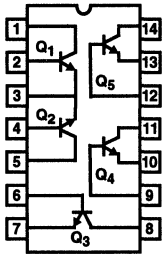
For PSPICE models, please request AnswerFAX document number 663046. Harris also provides an Application Note illustrating the use of these devices as RF amplifiers (request AnswerFAX document 99315).

Ordering Information

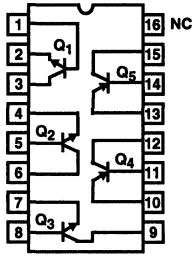
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA3046B	-55 to 125	14 Ld SOIC	M14.15
HFA3096B	-55 to 125	16 Ld SOIC	M16.15
HFA3127B	-55 to 125	16 Ld SOIC	M16.15
HFA3128B	-55 to 125	16 Ld SOIC	M16.15

Pinouts

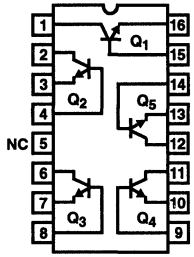
HFA3046
TOP VIEW



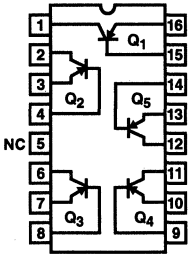
HFA3096
TOP VIEW



HFA3127
TOP VIEW



HFA3128
TOP VIEW



5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3076.8**

HARRIS SEMICONDUCTOR

HFA3101

November 1996

Gilbert Cell UHF Transistor Array

Features

- High Gain Bandwidth Product (f_T) 10GHz
- High Power Gain Bandwidth Product 5GHz
- Current Gain (h_{FE}) 70
- Low Noise Figure (Transistor) 3.5dB
- Excellent h_{FE} and V_{BE} Matching
- Low Collector Leakage Current ..... <0.01nA
- Pin-to-Pin Compatible to UPA101

Applications

- Balanced Mixers
- Multipliers
- Demodulators/Modulators
- Automatic Gain Control Circuits
- Phase Detectors
- Fiber Optic Signal Processing
- Wireless Communication Systems
- Wide Band Amplification Stages
- Radio and Satellite Communications
- High Performance Instrumentation

Description

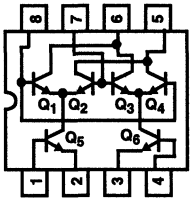
The HFA3101 is an all NPN transistor array configured as a Multiplier Cell. Based on Harris bonded wafer UHF-1 SOI process, this array achieves very high f_T (10GHz) while maintaining excellent h_{FE} and V_{BE} matching characteristics that have been maximized through careful attention to circuit design and layout, making this product ideal for communication circuits. For use in mixer applications, the cell provides high gain and good cancellation of 2nd order distortion terms.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA3101B (H3101B)	-40 to 85	8 Ld SOIC	M8.15
HFA3101B96 (H3101B)	-40 to 85	8 Ld SOIC Tape and Reel	M8.15

Pinout

HFA3101
(SOIC)
TOP VIEW



NOTE: Q_5 and Q_6 - 2 Paralleled 3µm x 50µm Transistors
Q_1, Q_2, Q_3, Q_4 - Single 3µm x 50µm Transistors

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3663.3**

HFA3102

August 1996

Dual Long-Tailed Pair Transistor Array

Features

- High Gain-Bandwidth Product (f_T) 10GHz
- High Power Gain-Bandwidth Product 5GHz
- High Current Gain (h_{FE}) 70
- Noise Figure (Transistor) 3.5dB
- Low Collector Leakage Current . . . . . <0.01nA
- Excellent h_{FE} and V_{BE} Matching
- Pin-to-Pin to UPA102G

Applications

- Single Balanced Mixers
- Wide Band Amplification Stages
- Differential Amplifiers
- Multipliers
- Automatic Gain Control Circuits
- Frequency Doublers, Tripplers
- Oscillators
- Constant Current Sources
- Wireless Communication Systems
- Radio and Satellite Communications
- Fiber Optic Signal Processing
- High Performance Instrumentation

Description

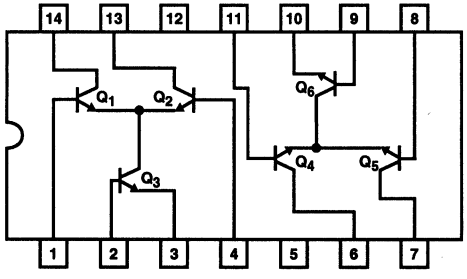
The HFA3102 is an all NPN transistor array configured as dual differential amplifiers with tail transistors. Based on Harris bonded wafer UHF-1 SOI process, this array achieves very high f_T (10GHz) while maintaining excellent h_{FE} and V_{BE} matching characteristics over temperature. Collector leakage currents are maintained to under 0.01nA.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA3102B	-40 to 85	14 Ld SOIC	M14.15
HFA3102B96	-40 to 85	14 Ld SOIC Tape and Reel	M14.15

Pinout/Functional Diagram

HFA3102
(SOIC)
TOP VIEW



5 STANDARD PRODUCTS

File Number **3635.2**

HARRIS SEMICONDUCTOR

HFA3600

December 1996

Low-Noise Amplifier/Mixer

Features

- LNA
  - Low Noise Figure . . . . . 2.3dB at 900MHz
  - High Power Gain . . . . . 12.8dB at 900MHz
  - High Intercept . . . . . +12.8dBm at Output
- MIXER
  - Low Noise Figure . . . . . 12.1dB at 900MHz
  - High Power Gain . . . . . 7.0dB at 900MHz
  - High Intercept . . . . . +3.2dBm at Output
  - Low LO Drive . . . . . - 3dBm
- LNA + MIXER
  - Low Noise Figure . . . . . 3.97dB at 900MHz
  - High Power Gain . . . . . 19.8dB at 900MHz
  - High Intercept . . . . . -16.7dBm at Input
  - Low Operating Power 5V/11.3mA
  - Low Shutdown Power 5V/250µA
  - Small Package: 14 Lead SOIC (Plastic, Small Outline Package, 150 Mil Width, 50 Mil Lead Spacing)

Applications

- Portable Cellular Telephone (AMPS, IS-54, GSM, JDC)
- Wireless Data Com. (ISM, Narrowband PCS)
- UHF and Mobile Radio Receiver
- 900MHz Digital Cordless Telephone (CT-2, ISM)
- Wireless Telemetry

Description

The HFA3600 is a silicon Low-Noise Amplifier with high performance characteristics allowing the design of very sensitive, wide dynamic-range 900MHz receivers with minimal external components.

The LNA, Mixer RF, and LO inputs are internally matched to 50Ω. The Mixer IF output is open collector allowing flexibility in choosing the IF output impedance, with 1000Ω operation fully characterized. The mixer performance is optimized for low LO drive (-3dBm) applications.

Power consumption is kept to a minimum, making the device ideal for battery-powered hand-held communication equipment. An integrated power-down feature maximizes battery life and eliminates the need for external shut down circuitry. Although fully characterized under 5V single supply, the HFA3600 is operable down to 4V with slight performance differences.

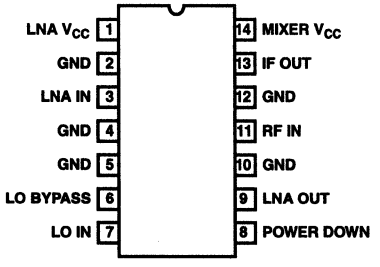
The HFA3600 is part of a complete solution including application circuit schematics, S-parameters, noise figure, third-order intercept characterization data and PC board artwork. Evaluation boards are also available through local Harris Sales offices.

Ordering Information

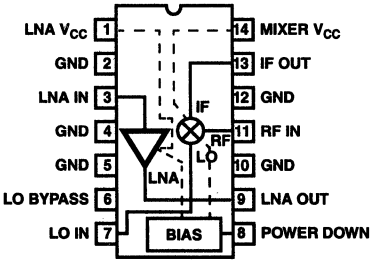
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA3600IB	-40 to 85	14 Ld SOIC	M14.15
HFA3600IB96	-40 to 85	14 Ld SOIC in Tape and Reel	

Pinout

HFA3600 (SOIC)
TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC handling procedures.

File Number 3655.3

HSP43124

January 1997

Serial I/O Filter

Features

- 45MHz Clock Rate
- 256 Tap Programmable FIR Filter
- 24-Bit Data, 32-Bit Coefficients
- Cascade of up to 5 Half Band Filters
- Decimation from 1 to 256
- Two Pin Interface for Down Conversion by $F_S/4$
- Multiplier for Mixing or Scaling Input with an External Source
- Serial I/O Compatible with Most DSP Microprocessors

Applications

- Low Cost FIR Filter
- Filter Co-Processor
- Digital Tuner

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP43124PC-45	0 to 70	28 Ld PDIP	E28.6
HSP43124PC-33	0 to 70	28 Ld PDIP	E28.6
HSP43124SC-45	0 to 70	28 Ld SOIC	M28.3
HSP43124SC-33	0 to 70	28 Ld SOIC	M28.3
HSP43124SI-40	-40 to 85	28 Ld SOIC	M28.3

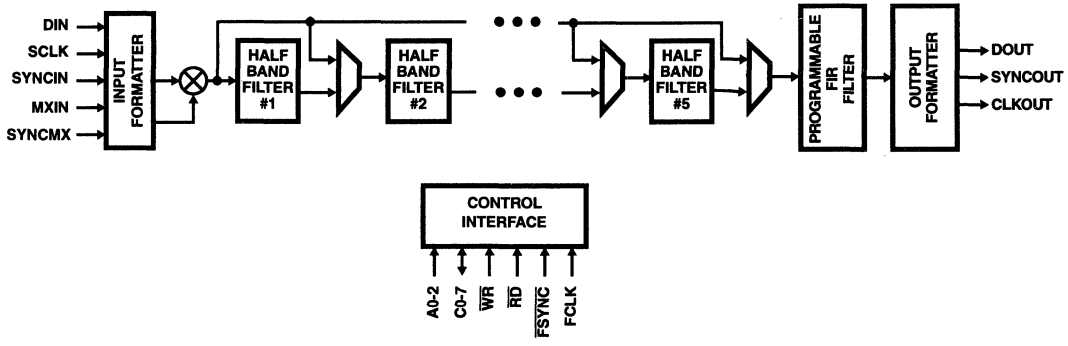
Description

The Serial I/O Filter is a high performance filter engine that is ideal for off loading the burden of filter processing from a DSP microprocessor. It supports a variety of multistage filter configurations based on a user programmable filter and fixed coefficient halfband filters. These configurations include a programmable FIR filter of up to 256 taps, a cascade of from one to five halfband filters, or a cascade of halfband filters followed by a programmable FIR. The half band filters each decimate by a factor of two, and the FIR filter decimates from one to eight. When all six filters are selected, a maximum decimation of 256 is provided.

For digital tuning applications, a separate multiplier is provided which allows the incoming data stream to be multiplied, or mixed, by a user supplied mix factor. A two pin interface is provided for serially loading the mix factor from an external source or selecting the mix factor from an on-board ROM. The on-board ROM contains samples of a sinusoid capable of spectrally shifting the input data by one quarter of the sample rate, $F_S/4$. This allows the chip to function as a digital down converter when the filter stages are configured as a low-pass filter.

The serial interface for input and output data is compatible with the serial ports of common DSP microprocessors. Coefficients and configuration data are loaded over a bidirectional eight bit interface.

Block Diagram



5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3555.5

HSP43168

December 1996

Dual FIR Filter

Features

- **Two Independent 8-Tap FIR Filters Configurable as a Single 16-Tap FIR**
- **10-Bit Data and Coefficients**
- **On-Board Storage for 32 Programmable Coefficient Sets**
- **Up To: 256 FIR Taps, 16 x 16 2-D Kernels, or 10 x 19-Bit Data and Coefficients**
- **Programmable Decimation to 16**
- **Programmable Rounding on Output**
- **Standard Microprocessor Interface**

Applications

- **Quadrature, Complex Filtering**
- **Image Processing**
- **Polyphase Filtering**
- **Adaptive Filtering**

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP43168VC-33	0 to 70	100 Ld MQFP	Q100.14x20
HSP43168VC-40	0 to 70	100 Ld MQFP	Q100.14x20
HSP43168VC-45	0 to 70	100 Ld MQFP	Q100.14x20
HSP43168JC-33	0 to 70	84 Ld PLCC	N84.1.15
HSP43168JC-40	0 to 70	84 Ld PLCC	N84.1.15
HSP43168JC-45	0 to 70	84 Ld PLCC	N84.1.15
HSP43168JI-40	-40 to 85	84 Ld PLCC	N84.1.15
HSP43168GC-33	0 to 70	84 Ld CPGA	G84.A
HSP43168GC-45	0 to 70	84 Ld CPGA	G84.A

Description

The HSP43168 Dual FIR Filter consists of two independent 8-tap FIR filters. Each filter supports decimation from 1 to 16 and provides on-board storage for 32 sets of coefficients. The Block Diagram shows two FIR cells each fed by a separate coefficient bank and one of two separate inputs. The outputs of the FIR cells are either summed or multiplexed by the MUX/Adder. The compute power in the FIR Cells can be configured to provide quadrature filtering, complex filtering, 2-D convolution, 1-D/2-D correlations, and interpolating/decimating filters.

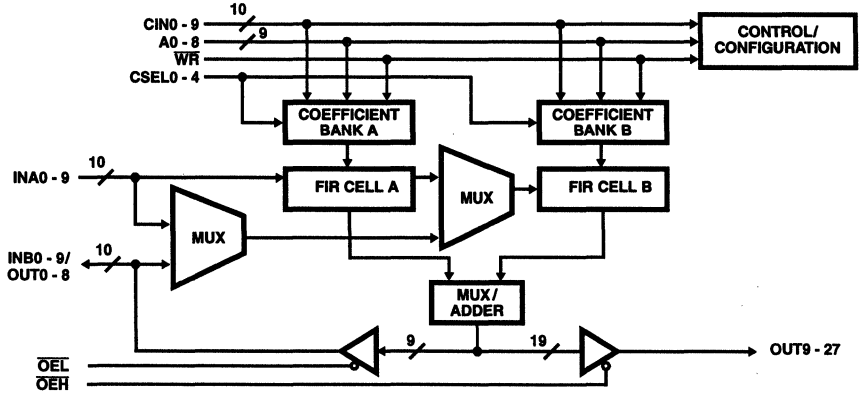
The FIR cells take advantage of symmetry in FIR coefficients by pre-adding data samples prior to multiplication. This allows an 8-tap FIR to be implemented using only 4 multipliers per filter cell. These cells can be configured as either a single 16-tap FIR filter or dual 8-tap FIR filters. Asymmetric filtering is also supported.

Decimation of up to 16 is provided to boost the effective number of filter taps from 2 to 16 times. Further, the decimation registers provide the delay necessary for fractional data conversion and 2-D filtering with kernels to 16x16.

The flexibility of the Dual is further enhanced by 32 sets of user programmable coefficients. Coefficient selection may be changed asynchronously from clock to clock. The ability to toggle between coefficient sets further simplifies applications such as polyphase or adaptive filtering.

The HSP43168 is a low power fully static design implemented in an advanced CMOS process. The configuration of the device is controlled through a standard microprocessor interface.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2808.6**

HSP43216

January 1997

Halfband Filter

Features

- Sample Rates to 52 MSPS
- Architected to Support Sample Rates to 104 MSPS Using External Multiplexer
- Four Modes of Operation:
  - Interpolate by 2 Filtering
  - Decimate by 2 Filtering
  - Quadrature to Real Signal Conversion
  - $F_S/4$ Quadrature Down Conversion Followed by Decimate by 2 Filtering
- 16-Bit Inputs and Outputs
- 67-Tap Halfband FIR Filter with 20-Bit Coefficients
- Two's Complement or Offset Binary Outputs
- Programmable Rounding on Outputs
- 1.24:1 Filter Shape Factor
- >90dB Stopband Attenuation
- <0.0003dB Passband Ripple
- Saturation Logic on Output

Applications

- Digital Down Conversion
- D/A and A/D pre/post Filtering
- Tuning Bandwidth Expansion for HSP45116 and HSP45106

Description

The HSP43216 Halfband Filter addresses a wide variety of applications by combining $F_S/4$ (F_S = sample frequency) quadrature up/down convert circuitry with a fixed coefficient halfband filter processor as shown in the block diagram. These elements may be configured to operate in one of the four following modes: decimate by 2 filtering of a real input signal; interpolate by 2 filtering of a real input signal; $F_S/4$ quadrature down conversion of a real input signal followed by decimate-by-2 filtering to produce a complex analytic signal; interpolate-by-2 filtering of a complex analytic signal followed by $F_S/4$ quadrature up conversion to produce a real valued output.

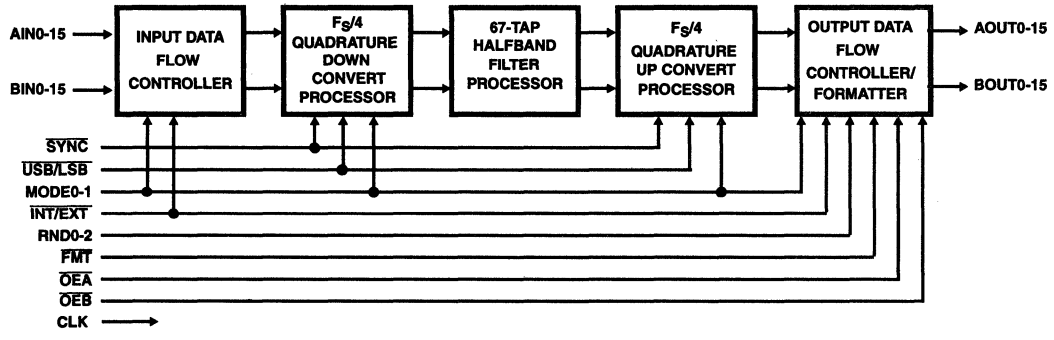
The frequency response of the HSP43216's halfband filter has a shape factor, (passband+transition band)/passband, of 1.24:1 with 90dB of stopband attenuation. The passband has less than 0.0003dB of ripple from $0F_S$ to $0.2F_S$ with stopband attenuation of greater than 90dB from $0.3F_S$ to Nyquist. At $0.25F_S$ the filter provides 6dB of attenuation.

The HSP43216 processes data streams with word widths up to 16 bits and data rates up to 52 MSPS. The processing throughput of the part is easily doubled to rates of up to 104 MSPS by using the part together with an external multiplexer or demultiplexer. Programmable rounding is provided to support output precisions from 8 bits to 16 bits.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE TYPE	PKG. NO.
HSP43216GC-52	0 to 70	85 Ld CPGA	G85.A
HSP43216JC-52	0 to 70	84 Ld PLCC	N84.1.15
HSP43216VC-52	0 to 70	100 Ld MQFP	Q100.14x20
HSP43216JI-52	-40 to 85	84 Ld PLCC	N84.1.15

Block Diagram



5 STANDARD PRODUCTS

File Number 3365.6

HARRIS SEMICONDUCTOR

HSP43220

December 1996

Decimating Digital Filter

Features

- **Single Chip Narrow Band Filter with up to 96dB Attenuation**
- **DC to 33MHz Clock Rate**
- **16-Bit 2's Complement Input**
- **20-Bit Coefficients in FIR**
- **24-Bit Extended Precision Output**
- **Programmable Decimation up to a Maximum of 16,384**
- **Standard 16-Bit Microprocessor Interface**
- **Filter Design Software Available DECI•MATE™**
- **Up to 512 Taps**

Applications

- **Very Narrow Band Filters**
- **Zoom Spectral Analysis**
- **Channelized Receivers**
- **Large Sample Rate Converter**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP43220VC-15	0 to 70	100 Ld MQFP	Q100.14x20
HSP43220VC-25	0 to 70	100 Ld MQFP	Q100.14x20
HSP43220VC-33	0 to 70	100 Ld MQFP	Q100.14x20
HSP43220JC-15	0 to 70	84 Ld PLCC	N84.1.15
HSP43220JC-25	0 to 0	84 Ld PLCC	N84.1.15
HSP43220JC-33	0 to 70	84 Ld PLCC	N84.1.15
HSP43220GC-15	0 to 70	84 Ld CPGA	G84.A
HSP43220GC-25	0 to 70	84 Ld CPGA	G84.A
HSP43220GC-33	0 to 70	84 Ld CPGA	G84.A
HSP43220GI-15	-40 to 85	84 Ld CPGA	G84.A
HSP43220GI-25	-40 to 85	84 Ld CPGA	G84.A
HSP43220GI-33	-40 to 85	84 Ld CPGA	G84.A
Deci•Mate™ Software Development Tool (This software tool may be downloaded from our Internet site: http://www.semi.harris.com)			

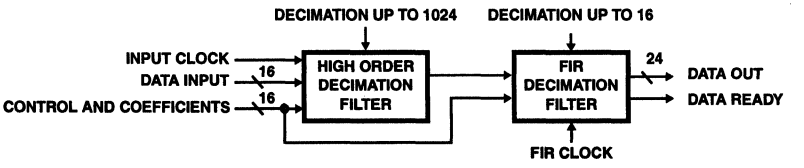
Description

The HSP43220 Decimating Digital Filter is a linear phase low pass decimation filter which is optimized for filtering narrow band signals in a broad spectrum of a signal processing applications. The HSP43220 offers a single chip solution to signal processing applications which have historically required several boards of ICs. This reduction in component count results in faster development times as well as reduction of hardware costs.

The HSP43220 is implemented as a two stage filter structure. As seen in the block diagram, the first stage is a high order decimation filter (HDF) which utilizes an efficient sample rate reduction technique to obtain decimation up to 1024 through a coarse low-pass filtering process. The HDF provides up to 96dB aliasing rejection in the signal pass band. The second stage consists of a finite impulse response (FIR) decimation filter structured as a transversal FIR filter with up to 512 symmetric taps which can implement filters with sharp transition regions. The FIR can perform further decimation by up to 16 if required while preserving the 96dB aliasing attenuation obtained by the HDF. The combined total decimation capability is 16,384.

The HSP43220 accepts 16-bit parallel data in 2's complement format at sampling rates up to 33 MSPS. It provides a 16-bit microprocessor compatible interface to simplify the task of programming and three-state outputs to allow the connection of several ICs to a common bus. The HSP43220 also provides the capability to bypass either the HDF or the FIR for additional flexibility.

Block Diagram



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CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2486.6**

HSP45102

December 1996

12-Bit Numerically Controlled Oscillator

Features

- 33MHz, 40MHz Versions
- 32-Bit Frequency Control
- BFSK, QPSK Modulation
- Serial Frequency Load
- 12-Bit Sine Output
- Offset Binary Output Format
- 0.009Hz Tuning Resolution at 40MHz
- Spurious Frequency Components <-69dBc
- Fully Static CMOS
- Low Cost

Applications

- Direct Digital Synthesis
- Modulation
- PSK Communications
- Related Products
  - HI5731 12-Bit, 100MHz D/A Converter

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP45102PC-33	0 to 70	28 Ld PDIP	E28.6
HSP45102PC-40	0 to 70	28 Ld PDIP	E28.6
HSP45102PI-33	-40 to 85	28 Ld PDIP	E28.6
HSP45102PI-40	-40 to 85	28 Ld PDIP	E28.6
HSP45102SC-33	0 to 70	28 Ld SOIC	M28.3
HSP45102SC-40	0 to 70	28 Ld SOIC	M28.3
HSP45102SI-33	-40 to 85	28 Ld SOIC	M28.3
HSP45102SI-40	-40 to 85	28 Ld SOIC	M28.3

Description

The Harris HSP45102 is Numerically Controlled Oscillator (NCO12) with 32-bit frequency resolution and 12-bit output. With over 69dB of spurious free dynamic range and worst case frequency resolution of 0.009Hz, the NCO12 provides significant accuracy for frequency synthesis solutions at a competitive price.

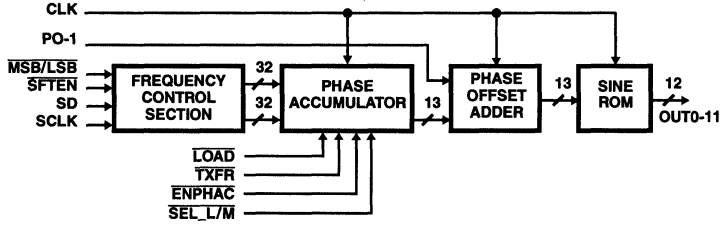
The frequency to be generated is selected from two frequency control words. A single control pin selects which word is used to determine the output frequency. Switching from one frequency to another occurs in one clock cycle, with a 6 clock pipeline delay from the time that the new control word is loaded until the new frequency appears on the output.

Two pins, P0-1, are provided for phase modulation. They are encoded and added to the top two bits of the phase accumulator to offset the phase in 90^{o} increments.

The 13-bit output of the Phase Offset Adder is mapped to the sine wave amplitude via the Sine ROM. The output data format is offset binary to simplify interfacing to D/A converters. Spurious frequency components in the output sinusoid are less than -69dBc.

The NCO12 has applications as a Direct Digital Synthesizer and modulator in low cost digital radios, satellite terminals, and function generators.

Block Diagram



5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2810.5**

HARRIS SEMICONDUCTOR

HSP45106

December 1996

16-Bit Numerically Controlled Oscillator

Features

- 25.6MHz, 33MHz Versions
- 32-Bit Center and Offset Frequency Control
- 16-Bit Phase Control
- 8 Level PSK Supported Through Three Pin Interface
- Simultaneous 16-Bit Sine and Cosine Outputs
- Output in Two's Complement or Offset Binary
- <0.008Hz Tuning Resolution at 33MHz
- Serial or Parallel Outputs
- Spurious Frequency Components <-90dBc
- 16-Bit Microprocessor Compatible Control Interface

Applications

- Direct Digital Synthesis
- Quadrature Signal Generation
- Spread Spectrum Communications
- PSK Modems
- Modulation - FM, FSK, PSK (BPSK, QPSK, 8PSK)
- Frequency Hopping Communications
- Precision Signal Generation
- Related Products
  - Use with Data Acquisition Parts HI5731 or HI5741

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP45106JC-25	0 to 70	84 Ld PLCC	N84.1.15
HSP45106JC-33	0 to 70	84 Ld PLCC	N84.1.15
HSP45106GC-25	0 to 70	85 Ld CPGA	G85.A
HSP45106GC-33	0 to 70	85 Ld CPGA	G85.A

Description

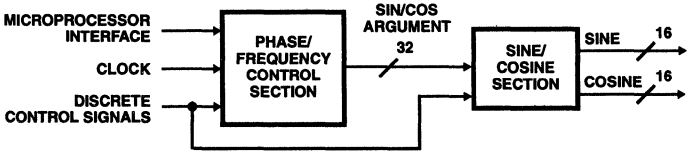
The Harris HSP45106 is a high performance 16-bit quadrature numerically controlled oscillator (NCO16). The NCO16 simplifies applications requiring frequency and phase agility such as frequency-hopped modems, PSK modems, spread spectrum communications, and precision signal generators. As shown in the block diagram, the HSP45106 is divided into a Phase/Frequency Control Section (PFCS) and a Sine/Cosine Section.

The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The frequency resolution is 32 bits, which provides for resolution of better than 0.008Hz at 33MHz. User programmable center frequency and offset frequency registers give the user the capability to perform phase coherent switching between two sinusoids of different frequencies. Further, a programmable phase control register allows for phase control of better than 0.006^{o}. In applications requiring up to 8-level PSK, three discrete inputs are provided to simplify implementation.

The output of the PFCS is a 28-bit phase which is input to the Sine/Cosine Section for conversion into sinusoidal amplitude. The outputs of the sine/cosine section are two 16-bit quadrature signals. The spurious free dynamic range of this complex vector is greater than 90dBc.

For added flexibility when using the NCO16 in conjunction with DAC's, a choice of either parallel of serial outputs with either two's complement or offset binary encoding is provided. In addition, a synchronization signal is available which indicates serial word boundaries.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2809.3**

HSP45116

May 1996

Numerically Controlled Oscillator/Modulator

Features

- NCO and CMAC on One Chip
- 15MHz, 25.6MHz, 33MHz Versions
- 32-Bit Frequency Control
- 16-Bit Phase Modulation
- 16-Bit CMAC
- 0.008Hz Tuning Resolution at 33MHz
- Spurious Frequency Components < -90dBc
- Fully Static CMOS

Applications

- Frequency Synthesis
- Modulation - AM, FM, PSK, FSK, QAM
- Demodulation, PLL
- Phase Shifter
- Polar to Cartesian Conversions

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP45116VC-15	0 to 70	160 Ld MQFP	Q160.28x28
HSP45116VC-25	0 to 70	160 Ld MQFP	Q160.28x28
HSP45116GC-15	0 to 70	145 Ld CPGA	G145.A
HSP45116GC-25	0 to 70	145 Ld CPGA	G145.A
HSP45116GC-33	0 to 70	145 Ld CPGA	G145.A
HSP45116GI-15	-40 to 85	145 Ld CPGA	G145.A
HSP45116GI-25	-40 to 85	145 Ld CPGA	G145.A
HSP45116GI-33	-40 to 85	145 Ld CPGA	G145.A
HSP45116GM-15/883	-55 to 125	145 Ld CPGA	G145.A
HSP45116GM-25/883	-55 to 125	145 Ld CPGA	G145.A
HSP45116AVC-52 †	0 to 70	160 Ld MQFP	Q160.28x28

†This part has its own data sheet under HSP45116A, AnswerFAX document no. 4156.

Description

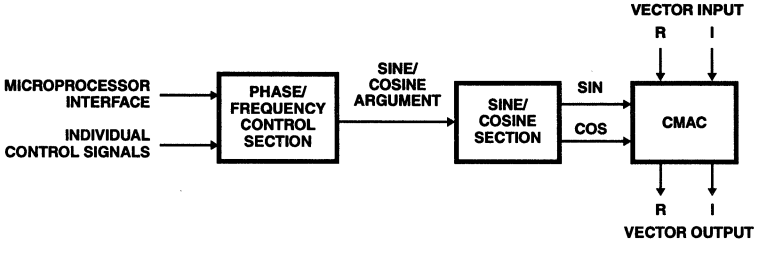
The Harris HSP45116 combines a high performance quadrature numerically controlled oscillator (NCO) and a high speed 16-bit Complex Multiplier/Accumulator (CMAC) on a single IC. This combination of functions allows a complex vector to be multiplied by the internally generated (cos, sin) vector for quadrature modulation and demodulation. As shown in the block diagram, the HSP45116 is divided into three main sections. The Phase/Frequency Control Section (PFCS) and the Sine/Cosine Section together form a complex NCO. The CMAC multiplies the output of the Sine/Cosine Section with an external complex vector.

The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The phase resolution of the PFCS is 32 bits, which results in frequency resolution better than 0.008Hz at 33MHz. The output of the PFCS is the argument of the sine and cosine. The spurious free dynamic range of the complex sinusoid is greater than 90dBc.

The output vector from the Sine/Cosine Section is one of the inputs to the Complex Multiplier/Accumulator. The CMAC multiplies this (cos, sin) vector by an external complex vector and can accumulate the result. The resulting complex vectors are available through two 20-bit output ports which maintain the 90dB spectral purity. This result can be accumulated internally to implement an accumulate and dump filter.

A quadrature down converter can be implemented by loading a center frequency into the Phase/Frequency Control Section. The signal to be down converted is the Vector Input of the CMAC, which multiplies the data by the rotating vector from the Sine/Cosine Section. The resulting complex output is the down converted signal.

Block Diagram



5 STANDARD PRODUCTS

File Number 2485.6

HARRIS SEMICONDUCTOR

HSP45116A

December 1996

Numerically Controlled Oscillator/Modulator

Features

- NCO and CMAC on One Chip
- 52MHz Version
- 32-Bit Frequency Control
- 16-Bit Phase Modulation
- 16-Bit CMAC
- 0.013Hz Tuning Resolution at 52MHz
- Programmable Rounding Option
- Spurious Frequency Components < -90dBc
- Fully Static CMOS

Applications

- Frequency Synthesis
- Modulation - AM, FM, PSK, FSK, QAM
- Demodulation, PLL
- Phase Shifter
- Polar to Cartesian Conversions

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP45116AVC-52	0 to 70	160 Ld MQFP	Q160.28x28

Description

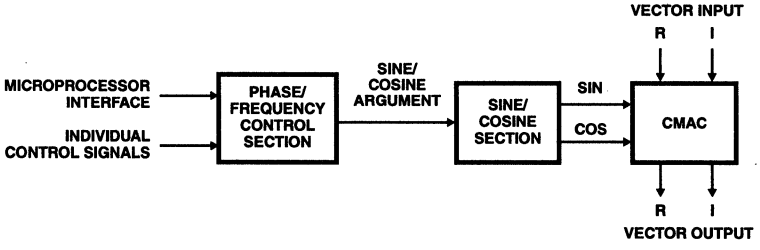
The Harris HSP45116A combines a high performance quadrature numerically controlled oscillator (NCO) and a high speed 16-bit Complex Multiplier/Accumulator (CMAC) on a single IC. This combination of functions allows a complex vector to be multiplied by the internally generated (cos, sin) vector for quadrature modulation and demodulation. As shown in the block diagram, the HSP45116A is divided into three main sections. The Phase/Frequency Control Section (PFCS) and the Sine/Cosine Section together form a complex NCO. The CMAC multiplies the output of the Sine/Cosine Section with an external complex vector.

The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The phase resolution of the PFCS is 32 bits, which results in frequency resolution better than 0.013Hz at 52MHz. The output of the PFCS is the argument of the sine and cosine. The spurious free dynamic range of the complex sinusoid is greater than 90dBc.

The output vector from the Sine/Cosine Section is one of the inputs to the Complex Multiplier/Accumulator. The CMAC multiplies this (cos, sin) vector by an external complex vector and can accumulate the result. The resulting complex vectors are available through two 20-bit output ports which maintain the 90dB spectral purity. This result can be accumulated internally to implement an accumulate and dump filter.

A quadrature down converter can be implemented by loading a center frequency into the Phase/Frequency Control Section. The signal to be down converted is the Vector Input of the CMAC, which multiplies the data by the rotating vector from the Sine/Cosine Section. The resulting complex output is the down converted signal. The bit position and widths for the outputs of CMAC and Complex Accumulator (ACC) are programmable.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4156.1**

HARRIS SEMICONDUCTOR

HSP50016

December 1996

Digital Down Converter

Features

- 75 MSPS Input Data Rate
- 16-Bit Data Input; Offset Binary or 2's Compliment Format
- Spurious Free Dynamic Range Through Modulator >102dB
- Frequency Selectivity: <0.006Hz
- Identical Lowpass Filters for I and Q
- Passband Ripple: <0.04dB
- Stopband Attenuation: >104dB
- Filter -3dB to -102dB Shape Factor: <1.5
- Decimation from 64 to 131,072
- IEEE 1149.1 Test Access Port
- HSP50016-EV Evaluation Board Available

Applications

- Cellular Base Stations
- Smart Antennas
- Channelized Receivers
- Spectrum Analysis
- Related Products: HI5703, HI5746, HI5766 A/Ds

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP50016JC-52	0 to 70	44 Ld PLCC	N44.65
HSP50016JC-75	0 to 70	44 Ld PLCC	N44.65
HSP50016GC-52	0 to 70	48 Ld CPGA	G48.A

Description

The Digital Down Converter (DDC) is a single chip synthesizer, quadrature mixer and lowpass filter. Its input data is a sampled data stream of up to 16 bits in width and up to a 75 MSPS data rate. The DDC performs down conversion, narrowband low pass filtering and decimation to produce a baseband signal.

The internal synthesizer can produce a variety of signal formats. They are: CW, frequency hopped, linear FM up chirp, and linear FM down chirp. The complex result of the modulation process is lowpass filtered and decimated with identical real filters in the in-phase (I) and quadrature (Q) processing chains.

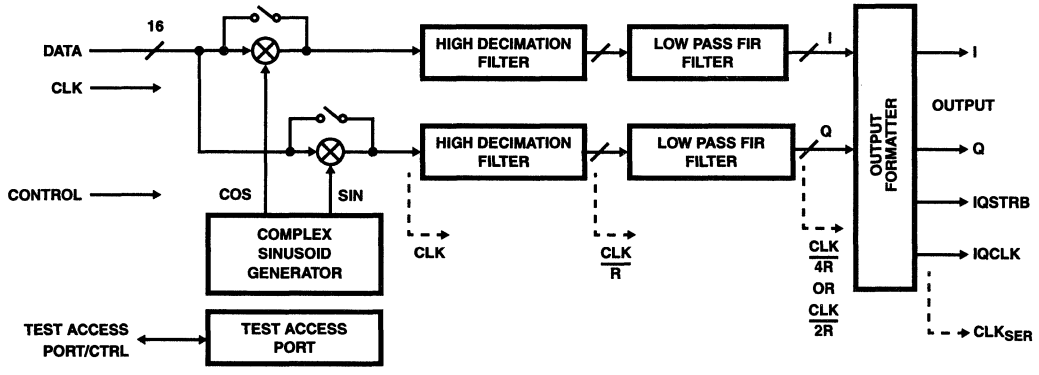
Lowpass filtering is accomplished via a high decimation filter (HDF) followed by a fixed finite impulse response (FIR) filter. The combined response of the two stage filter results in a -3dB to -102dB shape factor of better than 1.5. The stopband attenuation is greater than 106dB. The composite passband ripple is less than 0.04dB. The synthesizer and mixer can be bypassed so that the chip operates as a single narrow band low pass filter.

The chip receives forty bit serial commands as a control input. This interface is compatible with the serial I/O port available on most microprocessors.

The output data can be configured in fixed point or single precision floating point. The fixed point formats are 16, 24, 32, or 38-bit, two's complement, signed magnitude, or offset binary.

The circuit provides an IEEE 1149.1 Test Access Port.

Block Diagram



5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3288.4**

HARRIS SEMICONDUCTOR

HSP50110

January 1997

Digital Quadrature Tuner

Features

- Input Sample Rates to 52 MSPS
- Internal AGC Loop for Output Level Stability
- Parallel or Serial Output Data Formats
- 10-Bit Real or Complex Inputs
- Bidirectional 8-Bit Microprocessor Interface
- Frequency Selectivity <0.013Hz
- Low Pass Filter Configurable as Three Stage Cascaded-Integrator-Comb (CIC), Integrate and Dump, or Bypass
- Fixed Decimation from 1-4096, or Adjusted by NCO Synchronization with Baseband Waveforms
- Input Level Detection for External IF AGC Loop
- Designed to Operate with HSP50210 Digital Costas Loop
- 84 Lead PLCC

Applications

- Satellite Receivers and Modems
- Complex Upconversion/Modulation
- Tuner for Digital Demodulators
- Digital PLL's
- Related Products: HSP50210 Digital Costas Loop ; A/D Products HI5703, HI5746, HI5766
- HSP50110/210EVAL Digital Demod Evaluation Board

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP50110JC-52	0 to 70	84 Ld PLCC	N84.1.15
HSP50110JI-52	-40 to 85	84 Ld PLCC	N84.1.15

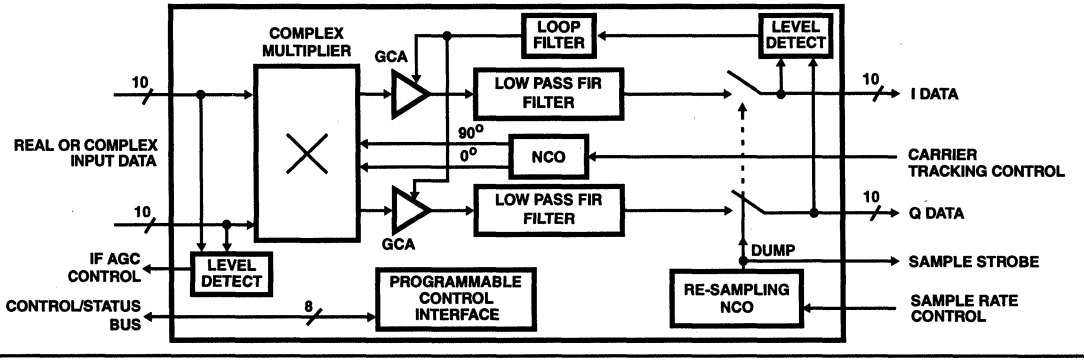
Description

The Digital Quadrature Tuner (DQT) provides many of the functions required for digital demodulation. These functions include carrier LO generation and mixing, baseband sampling, programmable bandwidth filtering, baseband AGC, and IF AGC error detection. Serial control inputs are provided which can be used to interface with external symbol and carrier tracking loops. These elements make the DQT ideal for demodulator applications with multiple operational modes or data rates. The DQT may be used with HSP50210 Digital Costas Loop to function as a demodulator for BPSK, QPSK, 8-PSK OQPSK, FSK, FM, and AM signals.

The DQT processes a real or complex input digitized at rates up to 52 MSPS. The channel of interest is shifted to DC by a complex multiplication with the internal LO The quadrature LO is generated by a numerically controlled oscillator (NCO) with a tuning resolution of 0.012Hz at a 52MHz sample rate. The output of the complex multiplier is gain corrected and fed into identical low pass FIR filters. Each filter is comprised of a decimating low pass filter followed by an optional compensation filter. The decimating low pass filter is a 3 stage cascaded-integrator-comb (CIC) filter. The CIC filter can be configured as an integrate and dump filter or a third order CIC filter with a $(\sin(X)/X)^3$ response. Compensation filters are provided to flatten the $(\sin(X)/X)^N$ response of the CIC. If none of the filtering options are desired, they may be bypassed. The filter bandwidth is set by the decimation rate of the CIC filter. The decimation rate may be fixed or adjusted dynamically by a symbol tracking loop to synchronize the output samples to symbol boundaries. The decimation rate may range from 1-4096. An internal AGC loop is provided to maintain the output magnitude at a desired level. Also, an input level detector can be used to supply error signal for an external IF AGC loop closed around the A/D.

The DQT output is provided in either serial or parallel formats to support interfacing with a variety DSP processors or digital filter components. This device is configurable over a general purpose 8-bit parallel bidirectional microprocessor control bus.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3651.3**

HARRIS SEMICONDUCTOR

HSP50210

January 1997

Digital Costas Loop

Features

- Clock Rates Up to 52MHz
- Selectable Matched Filtering with Root Raised Cosine or Integrate and Dump Filter
- Second Order Carrier and Symbol Tracking Loop Filters
- Automatic Gain Control (AGC)
- Discriminator for FM/FSK Detection and Discriminator Aided Acquisition
- Swept Acquisition with Programmable Limits
- Lock Detector
- Data Quality and Signal Level Measurements
- Cartesian to Polar Converter
- 8-Bit Microprocessor Control - Status Interface
- Designed to work with the HSP50110 Digital Quadrature Tuner
- 84 Lead PLCC

Applications

- Satellite Receivers and Modems
- BPSK, QPSK, 8-PSK, OQPSK, FSK, AM and FM Demodulators
- Digital Carrier Tracking
- Related Products: HSP50110 Digital Quadrature Tuner, D/A Converters HI5721, HI5731, HI5741
- HSP50110/210EVAL Digital Demod Evaluation Board

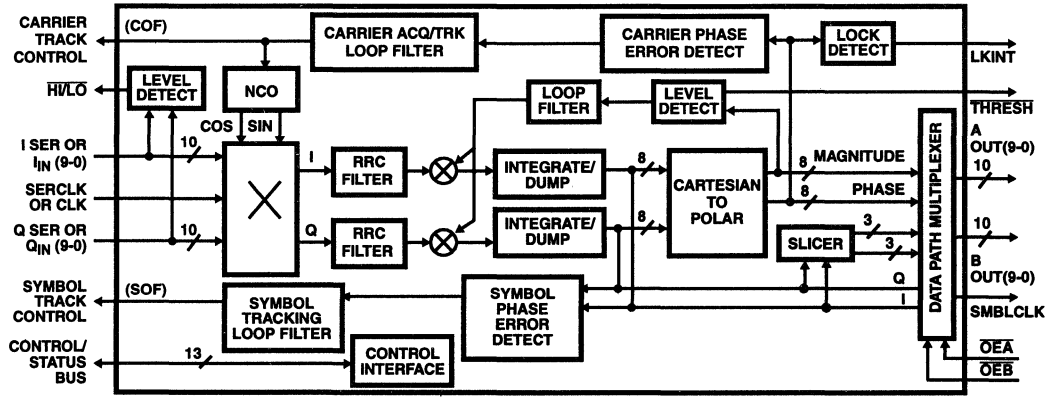
Description

The Digital Costas Loop (DCL) performs many of the baseband processing tasks required for the demodulation of BPSK, QPSK, 8-PSK, OQPSK, FSK, AM and FM waveforms. These tasks include matched filtering, carrier tracking, symbol synchronization, AGC, and soft decision slicing. The DCL is designed for use with the HSP50110 Digital Quadrature Tuner to provide a two chip solution for digital down conversion and demodulation.

The DCL processes the In-phase (I) and quadrature (Q) components of a baseband signal which have been digitized to 10 bits. As shown in the block diagram, the main signal path consists of a complex multiplier, selectable matched filters, gain multipliers, cartesian-to-polar converter, and soft decision slicer. The complex multiplier mixes the I and Q inputs with the output of a quadrature NCO. Following the mix function, selectable matched filters are provided which perform integrate and dump or root raised cosine filtering ($\alpha \sim 0.40$). The matched filter output is routed to the slicer, which generates 3-bit soft decisions, and to the cartesian-to-polar converter, which generates the magnitude and phase terms required by the AGC and Carrier Tracking Loops.

The PLL system solution is completed by the HSP50210 error detectors and second order Loop Filters that provide carrier tracking and symbol synchronization signals. In applications where the DCL is used with the HSP50110, these control loops are closed through a serial interface between the two parts. To maintain the demodulator performance with varying signal power and SNR, an internal AGC loop is provided to establish an optimal signal level at the input to the slicer and to the cartesian-to-polar converter.

Block Diagram



5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3652.3

HARRIS SEMICONDUCTOR

HSP50214

ADVANCE INFORMATION

November 1996

Programmable Downconverter

Features

- Up to 52 MSPS Input
- 32-Bit Programmable NCO for Channel Selection and Carrier Tracking
- Digital Resampling Filter for Symbol Tracking Loops and Incommensurate Sample-to-Output Clock Ratios
- Digital AGC with Programmable Limits and Slew Rate to Optimize Output Signal Resolution
- Processing Capable of >100dB SFDR
- Up to 255 Tap Programmable FIR
- Overall Decimation Factor Ranging from 4 to 16384.
- Output Samples Rates to ≅ 6.5 MSPS with Output Bandwidths to ≅500kHz Low Pass
- Serial, Parallel, and FIFO 16-Bit Output Modes
- Cartesian-to-Polar Converter and Discriminator for AFC Loops and to Support Demodulation of AM, FM, FSK, DPSK
- Input Level Detector for External I.F. AGC Support

Applications

- Single Channel Digital Software Radio Receivers (Wide Band or Narrow Band)
- Base Station Receivers
- Operate with HSP50210 Digital Costas Loop for Loop Filter
- Used with HI5805 and HI5703 A/D Converters

Description

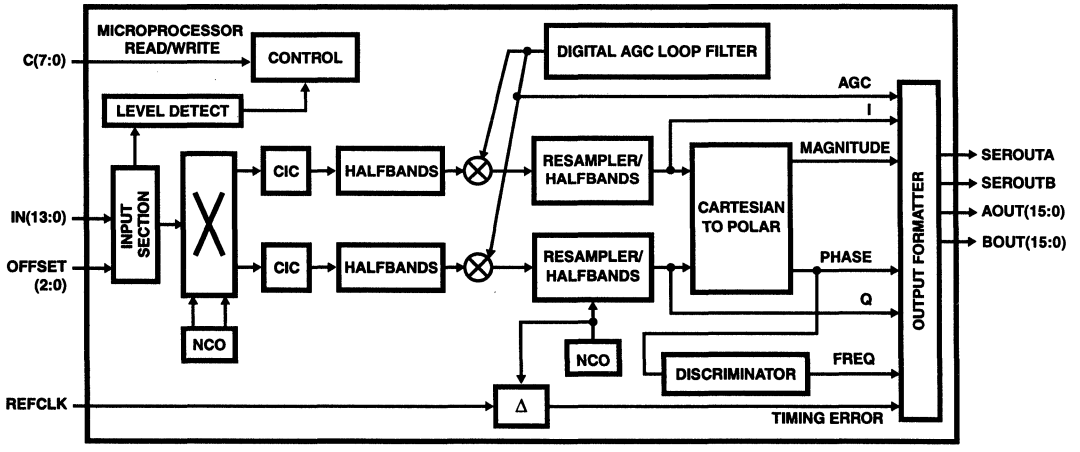
The HSP50214 Programmable Downconverter converts digitized IF data into data which can be processed by the standard DSP microprocessor. At least 14 bits of dynamic range is maintained through the mathematical processing within the part. The Programmable Downconverter frees the DSP microprocessor from the burden of down conversion, decimation, narrowband low pass filtering, gain control, resampling, and converting the data from Cartesian to polar.

The 14-bit input data is down converted by digital mixers and a 32-bit programmable NCO for channel selection and carrier tracking as shown in the Block Diagram. A decimating (4 to 32) fifth order CIC filter can be applied to the data before being processed by up to 5 decimate-by-2 halfband filters. The halfband filter stage is followed by a 255 tap programmable FIR filter. The data from the 255 tap programmable filter is scaled by a digital AGC before entering a polyphase resampling filter. The output section can provide data in Cartesian (I,Q), polar (R,θ), or frequency filtered (dθ/dt).

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP50214VC	0 to 70	120 Ld MQFP	Q120.28x28
HSP50214VI	-40 to 85	120 Ld MQFP	Q120.28x28

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4266**

HSP50306

January 1997

Digital QPSK Demodulator

Features

- 25.6MHz or 26.97MHz Clock Rates
- Single Chip QPSK Demodulator with 10kHz Tracking Loop
- Square Root of Raised Cosine ($\alpha = 0.4$) Matched Filtering
- 2.048 MBPS Reconstructed Output Data Stream
- Bit Synchronization with 3kHz Loop Bandwidth
- Internal Equalization for Multipath Distortion
- 6-Bit Real Input: Digitized 10.7MHz or 2.1MHz IF
- Level Detection for External IF AGC Loop
- 0.1s Acquisition Time
- 10^{-9} BER
- <116mA on +5.0V Supply

Applications

- Cable Data Link Receivers
- Cable Control Channel Receivers

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP50306SC-27	0 to 70	16 Ld SOIC	M16.3
HSP50306SC-2796	0 to 70	Tape and Reel	
HSP50306SC-25	0 to 70	16 Ld SOIC	M16.3
HSP50306SC-2596	0 to 70	Tape and Reel	

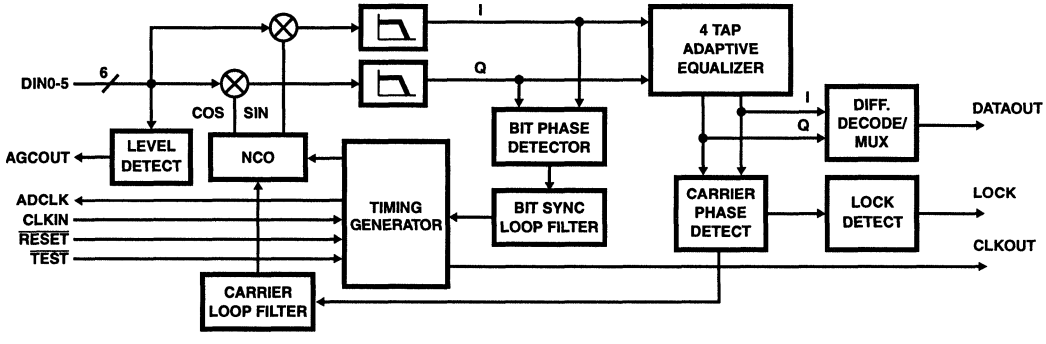
Description

The HSP50306 is a 6-bit QPSK demodulator chip designed for use in high signal to noise environments which have some multipath distortion. The part recovers 2.048 MBPS data from samples of a QPSK modulated 10.7MHz or 2.1MHz carrier. The chip coherently demodulates the waveform, recovers symbol timing, adaptively equalizes the signal to remove multipath distortion, differentially decodes and multiplexes the data decisions. A lock signal is provided to indicate when the tracking loops are locked and the data decisions are valid. To optimize performance, a gain error feedback signal is provided which can be filtered and used to close an I.F. AGC loop around the A/D converter.

The QPSK demodulator derives all timing from CLKIN. The chip divides this clock by 2 to provide the sample clock for the external A/D converter. The -27 version operates at a clock input of 26.97MHz and demodulates a 10.7MHz QPSK signal to recover the 2048 KSPS data. The -25 version operates at a clock input of 25.6MHz and demodulates a 2.1MHz QPSK signal to recover the 2048 KSPS data. Variation from these CLKIN frequencies will progressively degrade the receive data rate, the receive IF, acquisition sweep rate, acquisition sweep range and loop bandwidths as the deviation increases from normal CLKIN. Details on the maximum allowable deviation are found in the Input Characteristics section. The HSP50306 processes 6-bit offset binary data. 4-bit data provides adequate performance for many applications.

The block diagram of the QPSK Demodulator is shown below. To demodulate the data, the I.F. samples are multiplied by sine and cosine samples from a numerically controlled oscillator. The digital mixer outputs are then low pass filtered to remove mixer products. The filtered data is then equalized by a 4 tap equalizer (1 precursor, one reference tap, and a 2 tap Decision Feedback Equalizer (DFE)) to remove distortion caused by multipath. The output of the equalizer is differential decoded and multiplexed into the output data

Block Diagram



5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4162.1**

HARRIS SEMICONDUCTOR

HSP50307

December 1996

Burst QPSK Modulator

Features

- 256 KBPS Data Rate and 128 KBPS Baud Rate
- Burst QPSK Modulation
- Programmable Carrier Frequency from 8MHz to 15MHz With a Frequency Step Size of 32kHz
- α = 0.5 Root Raised Cosine (RRC) Filtering For Spectrum Shaping
- On-Board Synthesizer
- Programmable Output Level From 22 to 62dBmV in 1dB Steps
- Programmable Charge Pump Current Control
- 62dBmV Differential Output Driver for 75Ω Cable

Applications

- Burst QPSK Modulator
- HSP50307EVAL1 Evaluation Board Is Available

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP50307SC	0 to 70	28 Ld SOIC	M28.3

Description

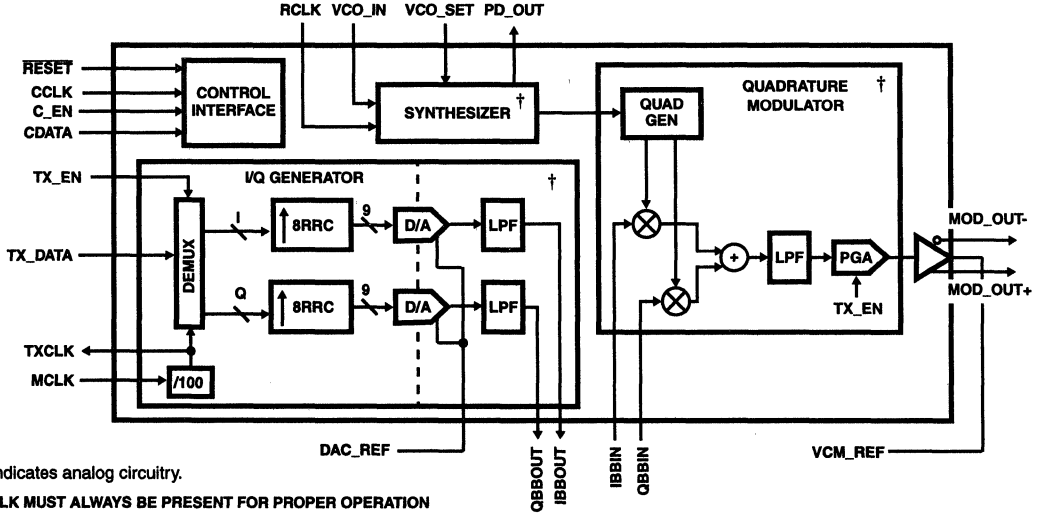
The HSP50307 is a mixed signal burst QPSK Modulator for upstream CATV Applications. The HSP50307 demultiplexes and modulates a serial data stream onto an RF Carrier centered between 8 and 15MHz. The signal spectrum is shaped with α = 0.5 root raised cosine (RRC) digital filters. On-chip filtering limits spurs and harmonics to levels below -35dBc during transmissions. The output power level is adjustable over a 40dB range in 1dB steps. The maximum differential output level is +62dBmV into 75Ω. A transmitter inhibit function disables the RF output outside the burst interval. The differential output amplifier interfaces to the cable via a transformer.

The block diagram of the HSP50307 QPSK Modulator is shown below. The HSP50307 consists of a digital control interface, an I/Q generator, a synthesizer, and a quadrature modulator.

The data clock is derived from the master clock. The HSP50307 demultiplexes the input data bits into in-phase (I) and quadrature (Q) data streams. The first bit and subsequent alternating bits of the burst are in-phase data. The two data streams are filtered, converted from digital to analog, and low pass filtered to produce the baseband I and Q analog signals.

The baseband signals are up-converted to RF in the quadrature modulation section The synthesizer provides the local oscillator (LO) for the quadrature modulator. The frequency is programmable via the control interface with a resolution of 32kHz. The output of the quadrature modulator is low pass filtered to remove harmonic distortion.

Block Diagram



† Indicates analog circuitry.

MCLK MUST ALWAYS BE PRESENT FOR PROPER OPERATION

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4219**

RF1K49086

January 1997

3.5A, 30V, Avalanche Rated, Dual N-Channel LittleFET™ Enhancement Mode Power MOSFET

Features

- 3.5A, 30V
- $r_{DS(ON)}$ = 0.060Ω
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
RF1K49086	MS-012AA	RF1K49086

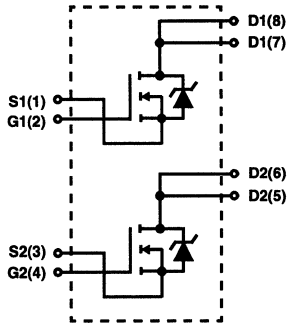
NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4908696.

Description

The RF1K49086 Dual N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low voltage bus switches. This device can be operated directly from integrated circuits.

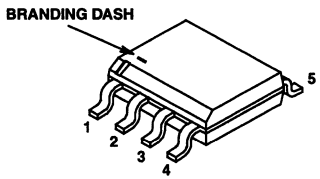
Formerly developmental type TA49086.

Symbol



Packaging

JEDEC MS-012AA



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HARRIS SEMICONDUCTOR

RF1K49088

3.5A, 30V, Avalanche Rated, Logic Level, Dual N-Channel LittleFET™ Enhancement Mode Power MOSFET

January 1997

Features

- 3.5A, 30V
- $r_{DS(ON)} = 0.060\Omega$
- *Temperature Compensating* PSPICE Model
- On-Resistance vs Gate Drive Voltage Curves
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
RF1K49088	MS-012AA	RF1K49088

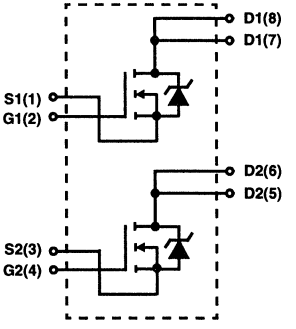
NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4908896.

Description

The RF1K49088 Dual N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low voltage bus switches. This product achieves full rated conduction at a gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

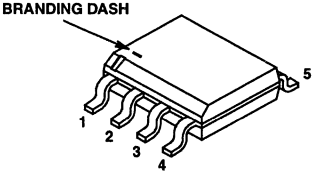
Formerly developmental type TA49088.

Symbol



Packaging

JEDEC MS-012AA



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CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3952.4**

HARRIS SEMICONDUCTOR

RF1K49090

January 1997

3.5A, 12V, Avalanche Rated, Logic Level, Dual N-Channel LittleFET™ Enhancement Mode Power MOSFET

Features

- 3.5A, 12V
- $r_{DS(ON)} = 0.050\Omega$
- *Temperature Compensating* PSPICE Model
- On-Resistance vs Gate Drive Voltage Curves
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
RF1K49090	MS-012AA	RF1K49090

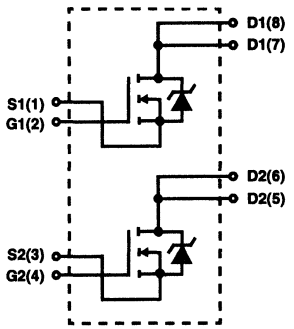
NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4909096.

Description

The RF1K49090 Dual N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low voltage bus switches. This product achieves full rated conduction at a gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

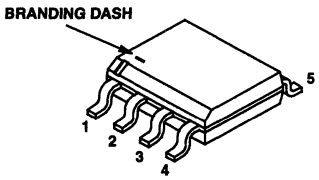
Formerly developmental type TA49090.

Symbol



Packaging

JEDEC MS-012AA



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5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3985.5**

HARRIS SEMICONDUCTOR

RF1K49092

3.5A/2.5A, 12V, Avalanche Rated, Logic Level, Complementary LittleFET™ Enhancement Mode Power MOSFET

January 1997

Features

- 3.5A, 12V (N-Channel)
  2.5A, 12V (P-Channel)
- $r_{DS(ON)}$ = 0.050Ω (N-Channel)
  $r_{DS(ON)}$ = 0.130Ω (P-Channel)
- *Temperature Compensating* PSPICE Model
- On-Resistance vs Gate Drive Voltage Curves
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
RF1K49092	MS-012AA	RF1K49092

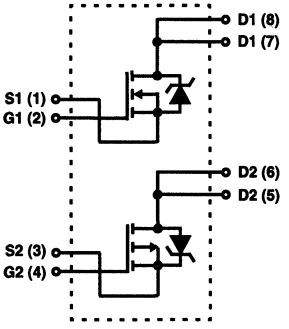
NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4909296.

Description

The RF1K49092 complementary power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low voltage bus switches. This product achieves full rated conduction at a gate bias in the 3V to 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

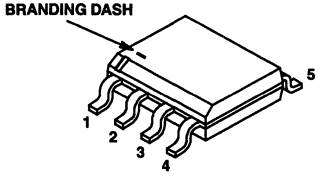
Formerly developmental type TA49092.

Symbol



Packaging

JEDEC MS-012AA



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CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3968.4**

RF1K49093

January 1997

2.5A, 12V, Avalanche Rated, Logic Level, Dual P-Channel LittleFET™ Enhancement Mode Power MOSFET

Features

- 2.5A, 12V
- $r_{DS(ON)}$ = 0.130Ω
- *Temperature Compensating* PSPICE Model
- On-Resistance vs Gate Drive Voltage Curves
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
RF1K49093	MS-012AA	RF1K49093

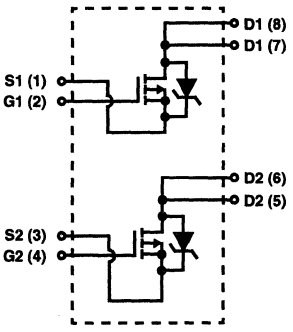
NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4909396.

Description

The RF1K49093 Dual P-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low voltage bus switches. This product achieves full rated conduction at a gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

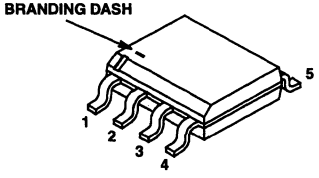
Formerly developmental type TA49093.

Symbol



Packaging

JEDEC MS-012AA



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RF1K49154

2A, 60V, ESD Rated, Avalanche Rated, Dual N-Channel LittleFET™ Enhancement Mode Power MOSFET

January 1997

Features

- 2A, 60V
- $r_{DS(ON)} = 0.130\Omega$
- 2kV ESD Protected
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
RF1K49154	MS-012AA	RF1K49154

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4915496.

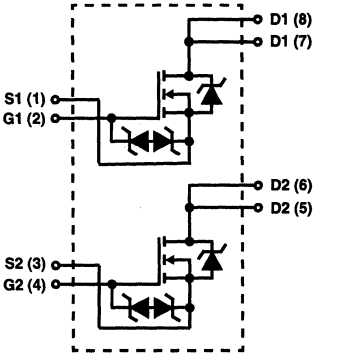
Formerly developmental type TA49154.

Description

The RF1K49154 Dual N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low voltage bus switches. These devices can be operated directly from integrated circuits.

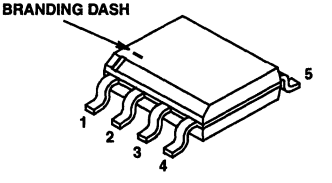
The RF1K49154 incorporates ESD protection and is designed to withstand 2kV (Human Body Model) of ESD.

Symbol



Packaging

JEDEC MS-012AA



LittleFET™ is a trademerk of Harris Corporation

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4143.1**

HARRIS SEMICONDUCTOR

RF1K49156

January 1997

6.3A, 30V, Avalanche Rated, Logic Level, Single N-Channel LittleFET™ Enhancement Mode Power MOSFET

Features

- 6.3A, 30V
- $r_{DS(ON)}$ = 0.030Ω
- *Temperature Compensating* PSPICE Model
- On-Resistance vs Gate Drive Voltage Curves
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
RF1K49156	MS-012AA	RF1K49156

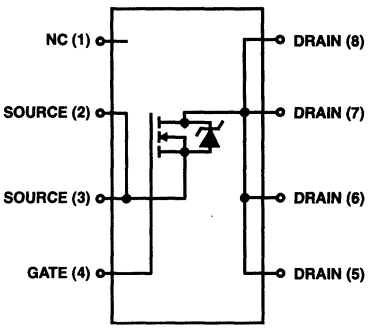
NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e., RF1K4915696.

Description

The RF1K49156 Single N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It was designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low voltage bus switches. This product achieves full rated conduction at a gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

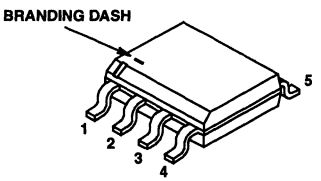
Formerly developmental type TA49156.

Symbol



Packaging

JEDEC MS-012AA



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5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4011.2**

HARRIS SEMICONDUCTOR

RF1K49157

6.3A, 30V, Avalanche Rated, Single N-Channel LittleFET™ Enhancement Mode Power MOSFET

January 1997

Features

- 6.3A, 30V
- $r_{DS(ON)} = 0.030\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
RF1K49157	MS-012AA	RF1K49157

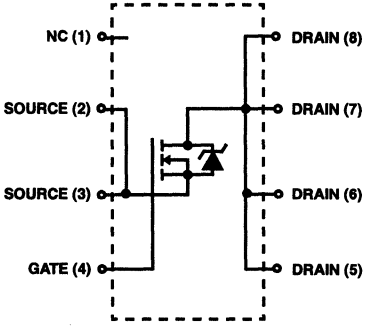
NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e., RF1K4915796.

Description

The RF1K49157 Single N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It was designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low voltage bus switches. This device can be operated directly from integrated circuits.

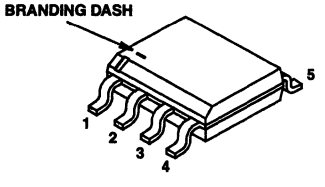
Formerly developmental type TA49157.

Symbol



Packaging

JEDEC MS-012AA



LittleFET™ is a trademerk of Harris Corporation

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4012.4**

COMMUNICATIONS 6

DEVELOPMENT TOOLS

PART NUMBER	DEVELOPMENT TOOL
WIRELESS COMMUNICATIONS	
PRISM™ 2.4GHz Chip Set	PRISM1KIT-EVAL
	WLANKITPR1-EVAL
HFA3424	HFA3424EVAL
HFA3524	HFA3524EVAL
HFA3624	HFA3624EVAL
HFA3724	HFA3724EVAL
HSP3824	HSP3824EVAL
HFA3925	HFA3925EVAL
WIRED COMMUNICATIONS	
HC5517	HC5517EVAL
HC-5509B	SPICE Model Available
HC-5513	HC5513EVAL
STANDARD PRODUCTS	
Data Acquisition - D/A Converters	
HI5721	HI5721-EVP/-EVS
HI5731	HI5731-EVP/-EVS
HI5741	HI5741-EVS
HI5780	HI5780-EV
HI20201	HI20201-EV
Data Acquisition - A/D Converters	
HI5703	HI5703EVAL
HI5710A	HI5710EVAL
HI5746	HI5746EVAL1
HI5800	HI5800EVAL
HI5804	HI5804EVAL
HI5805	HI5805EVAL1
HI5808	HI5808EVAL1

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Development Tools (Continued)

PART NUMBER	DEVELOPMENT TOOL
Linear	
HFA1100, HFA1120	HFA11XXEVAL, SPICE Model Available
HFA1110	HFA1110EVAL
HFA3046, HFA3096, HFA3127, HFA3128	SPICE Model Available
HFA3600	HFA3600EVAL
Digital Signal Processing	
DSP Evaluation Platform	HSP-EVAL
HSP43124	SERINADE™ Development Software
HSP43220	DECI•MATE™ Development Software
HSP45116	HSP45116-DB
HSP50016	HSP50016-EV
HSP50110	HSP50110/210EVAL
HSP50210	HSP50110/210EVAL

COMMUNICATIONS 7

APPLICATION NOTES

AN9640 "Glossary of Communication Terms" (32 pages) is not included in this data book, but is available on the net at *http://www.semi.harris.com/appnotes/an9640/* and Harris AnswerFAX (407-724-7800) document # 99640.

No. AN549.1 January 1997

Harris Linear

The HC-5502X/4X Telephone Subscriber Line Interface Circuits (SLIC)

Author: Geoff Phillips

Introduction

The HC-5502X/4X family of telephone subscriber line interface circuits (SLIC) integrate most of the BORSCHT functions of the traditional hybrid transformer interface circuits onto one chip. The circuits are manufactured in a 200V dielectric isolation (DI) process and together with a secondary protection diode bridge give 1kV of isolation from lightning induced faults between the subscriber loop and the telephone office.

The BORSCHT functions provided are:

- Battery Feed With Loop Current Limiting
- Overvoltage Protection
- Ringing
- Supervision/Signalling
- Hybrid

The HC-5502X is intended for use in systems utilizing single ended tip (positive side) injected ringing and limits the short loop current to 30mA; the HC-5504X is intended for use in ring side (negative side) injected ringing systems and will limit the short loop current to 40mA. It should be noted that the HC-5504X can also be configured to operate in switches employing either of the two single ended ringing methods and in balanced ringing systems.

This note will describe each subfunction of the SLIC and will discuss several system design features, including balance networks and complex impedance matching.

An Overview of the Basic Phone Loop And Its Environment

Figure 1 illustrates a simplified telephone network. Each subscriber is connected via a 2-wire (2W) loop to a switch office which provides intersubsciber loop switching and signal processing (analog and/or digital).

The SLIC is the primary interface between the 4 wire (4W) (ground referenced) low voltage switch environment and the 2W ("floating") high voltage loop environment.

The loop consists of a wire A (the Tip wire), the telephone set or its equivalent, and wire B (the ring wire). A DC voltage is applied across the Tip and Ring wires at the line card which is housed in the telephone office: The battery is usually a nominal -48V, and is often called the quiet or talking battery. When the telephone is off-hook, a DC path is established around the loop. DC loop current will flow around the loop from tip feed to ring feed. This is called Battery Feed.

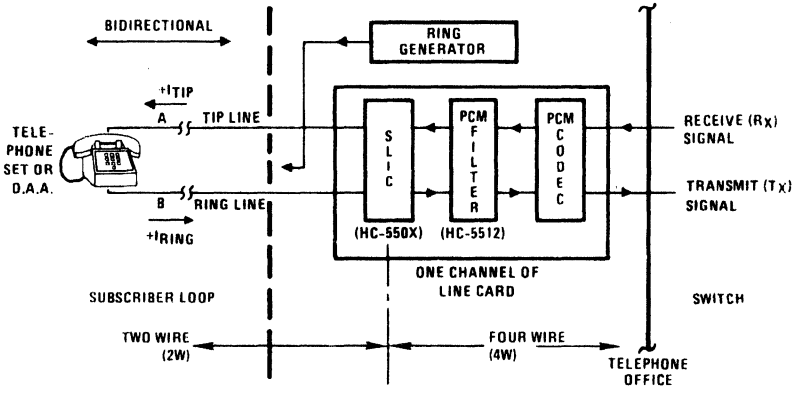


FIGURE 1. SIMPLIFIED TELEPHONE NETWORK

The SLIC must be able to sense this DC current and flag the switch controller: This is referred to as Switch Hook Detection (SHD). It tells the switch controller that the line is busy, and is a supervisory function.

The subscriber set is often located very close to the switch office. Thus, the loop resistance will be very low and the SLIC should incorporate a feedback network that will limit the loop current to a specified maximum to prevent battery power drain and minimize power dissipation at the board level. The HC-5502X/4X SLICs sense the loop current and adjust the voltage on the ring side of the line to cause line current saturation.

The telephone can be rung by switching a ring relay to connect a ring generator to the loop. The on-off switching of the relay (cadencing) is controlled by the Ring Command (RC) input which gates the relay driver output. When the user answers the telephone, the ring relay is automatically tripped, the ring command signal is inhibited and the 2W loop is made ready for voice transmission. Voice signals are transmitted onto the loop by directly modulating the DC feed. This AC voice signal is coupled to the users earpiece via a transformer in the telephone set. Voice transmission for the 2W to the 4W system is called the hybrid function. For 2W to 4W transmission, the subscriber talking into his set modulates the resistance of the telephone microphone. This causes AC current in the loop which is sensed by the SLIC and transmitted as a ground referenced voltage signal to the signal processing electronics within the switch.

Subscriber loops are usually measured in terms of loop resistance. The nominal loop length is 1200Ω. Owing to the length of the lines and their location near power lines, common mode or longitudinal currents are often induced. The SLIC has to distinguish between these noise signals (longitudinal) and the transversal signals, and reject the unwanted longitudinal components: this is a measure of the SLIC's longitudinal balance. The primary noise sources are 60/50Hz power lines, cable cross talk, and R_F transmissions. The Harris SLICs will accommodate $15mA_{RMS}$ of noise currents on each side of the loop.

The line is also subjected to lightning strikes. Together with primary and secondary protection networks, the SLIC must withstand 1kV peak of lightning induced energy. In fact, the plastic encapsulated Harris SLIC can withstand a 1kV peak strike with a small signal diode bridge providing voltage clamping and current steering.

The Harris HC-5502X/4X

The HC-5502X/4X family of SLICs are primary intended for use within Private Branch Exchanges (PBX) although they can be used in the larger switch networks found in Central Offices (CO).

Figure 2 shows the functional schematic of the SLIC. The subfunctions to be described are:

- Line Feed Amplifiers
- Transversal Amplifiers
- Loop Current Limiting: Metallic, Fault and Thermal Limiting
- Ring Trip and Ground Key Detection
- Spare or Uncommitted Operational Amplifier
- Logic Network

Line Feed Amplifiers

The line feed amplifiers are high power op amps, and are connected to the subscriber loop through 300Ω of feed resistance; the configuration is shown in Figure 3. The feed resistors provide a 600Ω balanced load for the 2W to 4W transmission, and limit longitudinal currents; the two resistors immediately adjacent to the feed amplifiers function as sense resistors for 2W to 4W transmission and signalling purposes.

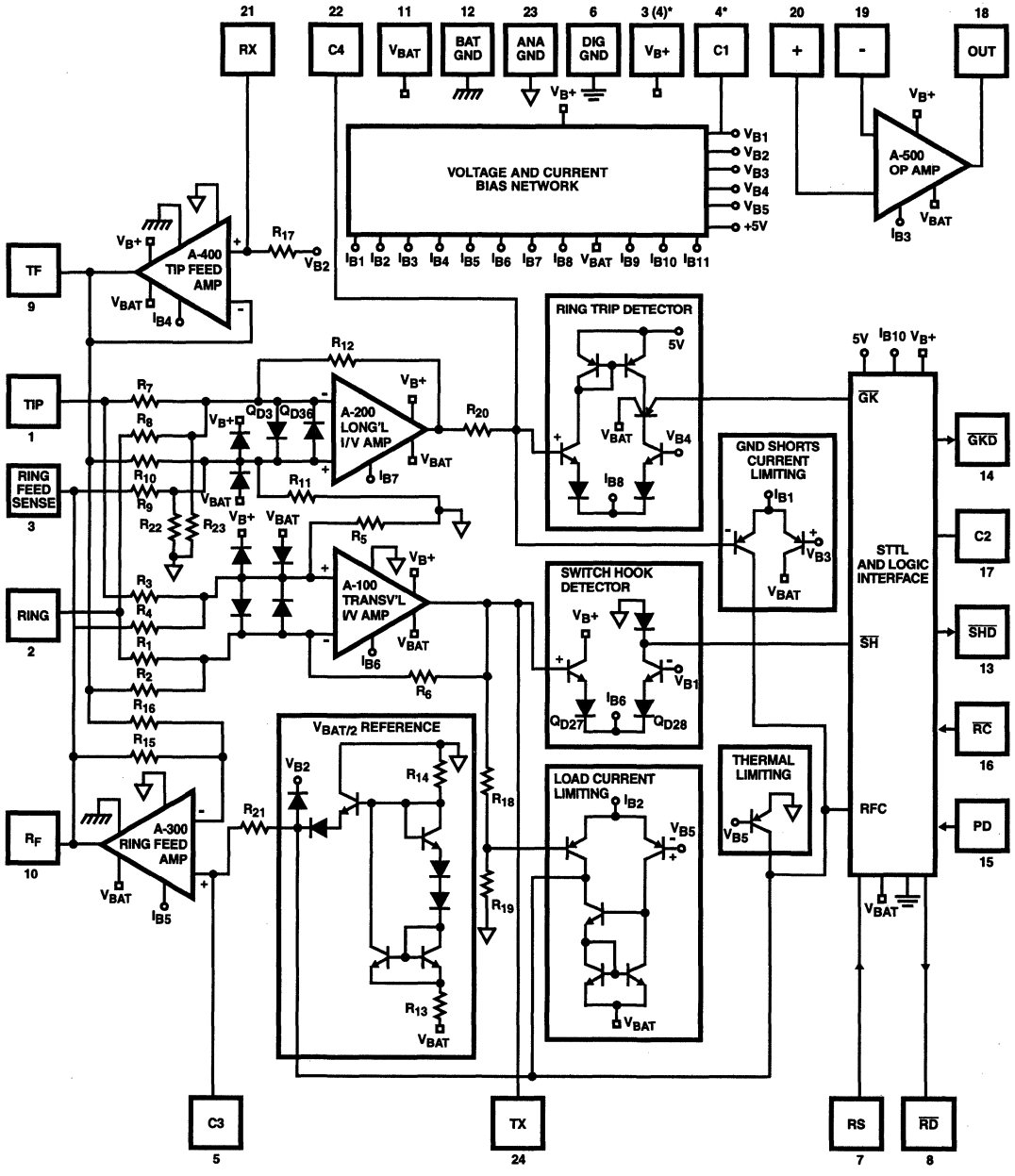
The tip feed amplifier is configured as a unity gain noninverting buffer. A -4V bias (derived from the negative battery (V_{B-}) in the bias network) is applied to the input of the amplifier. Hence, the tip feed DC level is at -4V. The principal reason for this offset is to accommodate sourcing and sinking of longitudinal noise currents up to $15mA_{RMS}$ without saturating the amplifier output. The tip feed amplifier also feeds the ring feed amplifier, which is configured as a unity gain inverting amplifier as seen from the TF amplifier. The noninverting input to the R_F amp is biased at a VB-/2. Looking into this terminal the amplifier has a noninverting gain of 2. Thus, the DC output at ring feed is:

$V_{RF}(DC) = (4 + V_{B-})$ Volts

For a -48V battery, V_{RF} = -44V. Hence, the nominal battery feed across the loop provided by the SLIC is 40V. When the subscriber goes off-hook this DC feed causes current (metallic current) to flow around the loop.

The received audio signal V_{RX} from the switch is fed into the tip feed amplifier and appears at the TF terminal. It is also fed through the ring feed amplifier and is inverted. Thus, a differential signal of $2V_{RX}$ appears across the line: for a 600Ω line this compensates the 6dB loss due to the 600Ω of line feed resistance. The V_{RX} signal causes AC audio currents to flow around the loop which are then AC coupled to the earpiece of the telephone set. Figure 4 shows the single ended AC equivalent circuit of the subscriber loop for voice transmission. In the general case the signal design equation for 4W to 2W transmission is given by:

$$V_{LINE} = \left(\frac{Z_{LINE}}{600 + Z_{LINE}}\right) \times 2V_{RX}$$



* PIN DESIGNATION DIFFERS BETWEEN HC5502X AND HC5504X

FIGURE 2. SLIC FUNCTIONAL SCHEMATIC

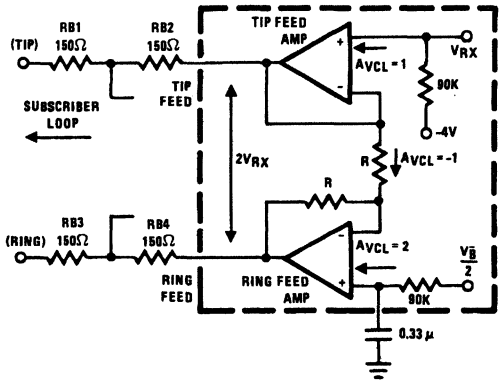


FIGURE 3. LINE FEED AMPLIFIERS

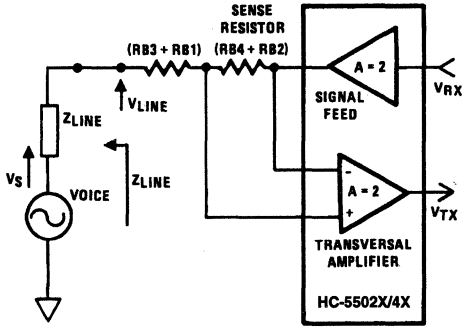


FIGURE 4. SINGLE ENDED AC SIGNAL EQUIVALENT CIRCUIT

The Transversal Amplifier (TA)

Whereas the feed amplifiers perform the 4W to 2W transmission function, the transversal amplifier acts as the 2W to 4W hybrid. The TA is a summing amplifier configured to reject common mode signals. It will thus reject 2W common mode signals. Figure 4 shows the single ended signal transmission path. Given below is the design equation of the 2W to 4W signal transmission path. Given below is the design equation of the 2W to 4W signal transmission. It can be seen that RB2 and RB4 act as loop current sense resistors, and that the voice signal output of the amplifier is a function of the differential voltages appearing across RB2 and RB4.

Thus, the transversal amplifier also has a DC output proportional to the metallic current in the loop. The output voltage is given by:

$$V_{TX} = 2(I_{TIP} + I_{RING})(R_{B2} + R_{B4})$$

where I_{TIP} and I_{RING} are assumed positive as indicated in Figure 1. This DC level is used as an input to a comparator whose output feeds into the logic circuitry as SH. This signal is used to gate SHD.

Voice signals on the loop are transformed by the TA into ground referenced signals as shown by the above equations. Since the TA output has a DC offset it is necessary to AC couple the output to any external circuitry. Note, that during 4W to 2W transmission, the transversal amplifier will have an audio signal at its output proportional to the 4W audio receive signal and the loop's equivalent AC impedance. This is called the transhybrid return, and must be cancelled (or balanced) out to prevent an echo effect. This is discussed more fully in Transhybrid Balancing.

Loop Current Limiting

The nominal loop length is equivalent to an 1800Ω load across the feed amplifiers. However, on a short loop the line resistance often approaches zero. Thus, a need exists to control the maximum DC loop current that can flow around the loop to prevent an excessive current drain from the system battery. This limit is typically specified between 30mA and 40mA for general PBX applications. Figure 5 depicts the feedback network that modifies the R_F voltage as a function of metallic current. Figure 6 illustrates the loop current characteristics as a function of line resistance.

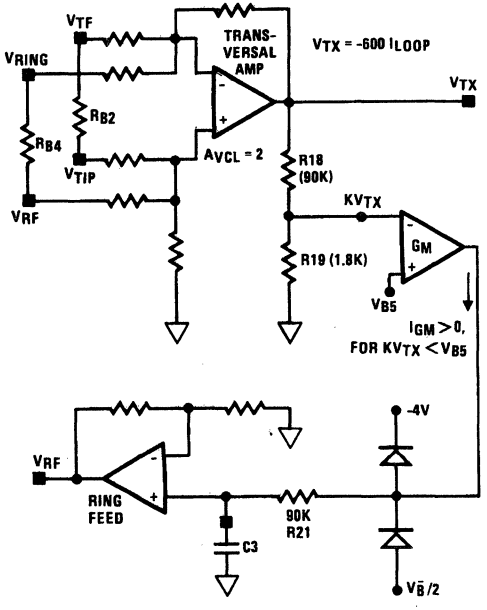


FIGURE 5. LOOP CURRENT LIMIT CONTROL

As indicated above, the TA has a DC voltage output directly proportional to the loop current. This voltage level is scaled by R19 and R18. The scaled level forms the 'Metallic' input to one side of a Transconductance Amplifier. The reference input to this amplifier is generated in the bias network, and is equivalent to 30mA or 40mA loop current, typically, for the HC-5502X and HC-5504X, respectively. When the metallic input exceeds the set reference level, the transconductance amplifier sources current. This current will charge

C3 in positive direction causing the R_F (Ring Feed) voltage to approach the TF (Tip Feed), effectively reducing the battery feed across the loop which will limit the DC loop current. C3 will continue to charge until an equilibrium level is attained at $I_{LOOP} = I_{LOOP}$ MAXmA. The time constant of this feedback loop is set by R21 (90kΩ) and C3 which is nominally 0.33μF.

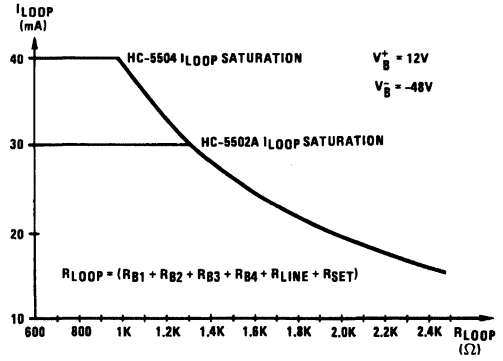


FIGURE 6. DC LOOP CURRENT CHARACTERISTICS

The R_F voltage level is also modified to reduce or control loop current during ring line faults (e.g. ground or power line crosses), and thermal overload. Figure 2 illustrates this. It can be seen that the thermal and fault current circuitry works in parallel with the transconductance amplifier.

Longitudinal Amplifier

The longitudinal amplifier is an op amp configured as a closed loop differential amplifier with a nominal gain of 0.1 (HC-5504X) or 0.581 (HC-5502X). The output is a measured of any imbalance between ITIP and IRING as described in Figure 1. The transfer function of this amplifier is given by:

$$V_{LONG} = K(I_{TIP} - I_{RING})\ 150$$

Where K is the gain factor of the amplifier. The gain factor is much less than one since ring voltage (up to $150V_{PEAK}$) can appear at the Ring or Ring Feed Sense terminals and are attenuated to protect the amplifier.

The longitudinal amplifier's principal functions are Ring Tip Detection (RTD) and Ground Key Detection (GKD). GKD provides a means for the subscriber to flag a PBX attendant and is used extensively in Europe. The ring line is grounded at the telephone set via a push switch incorporated within the telephone. This causes a DC current imbalances between the tip and ring sides of the loop which gives rise to a negative voltage at the output of the longitudinal amplifier. The output of the amplifier after being filtered by R20 and C4 to attenuate AC signals is fed into a detector whose output GK gates the necessary logic to drive GKD or inhibit the ring relay driver to remove ringing signals from the line in an off-hook condition. In order to prevent false ground key owing to line noise or during ring trip, the internal GKD logic is delayed via C2. An internal current source of 5μA has to change C2 up to a 5V level before allowing the ground key signal to propagate. Thus, for C2 = 0.15μF, a delay of 150ms is established.

Ringing the line and Ring Trip Detection are discussed more fully in the following section, Designing with the Harris SLIC.

Uncommitted Op Amp

An uncommitted op amp is provided on the chip. This is a standard op amp with an output swing of ±5V. It is primarily intended to be used to balance the transhybrid return signal discussed in The Transversal Amplifier (TA) section. The amplifier has an offset voltage of 10mV; an open loop gain of 66dB; a GBW product of 2MHz; slews at 1V/μs typically, and has a ±2mA output current drive capability.

The Logic Network

The logic network utilizes I^2L logic. All external inputs and outputs are LS TTL compatible: the relay driver is an open collector output that can sink 60mA with a V_{CE} of 1V.

Figure 7 is a schematic of the combination logic within the network. The external inputs RC (Relay Control) and PD (Power Denial) allow the switch controller to ring the line or deny power to the loop, respectively. The Ring Synchronization input (RS) facilitates switching of the ring relay near a ring current zero crossing in order to minimize inductive kickback from the telephone ringer.

The internal inputs SH and GK control ring trip and provide supervisory flags to the system controller via the Switch Hook Detect (SHD) and Ground Key Detect (GKD) outputs.

Designing with the Harris SLIC

General application circuits for the HC-5502X and HC-5504X SLICs are given in Figures 8 and 9. In this section, several specific design and application areas will be discussed:

- Ringing the Line
- Power Denial
- Transhybrid and Longitudinal Balance
- Complex Impedance Matching
- Surge Protection

Ringing The Line

The HC-5502X is used for tip injected ringing (also called single ended ground referenced ringing), and the HC-5504X is used for ring injected or single ended battery referenced ringing. Figures 10 and 11 show the two different ringing schemes. Note, that the HC-5504X can be used for either of the single ended ringing schemes: to use the HC-5504 for tip injected ringing the Ring Feed Sense (RFS) and R_F pins are permanently connected externally, and the scheme shown in Figure 10 adopted.

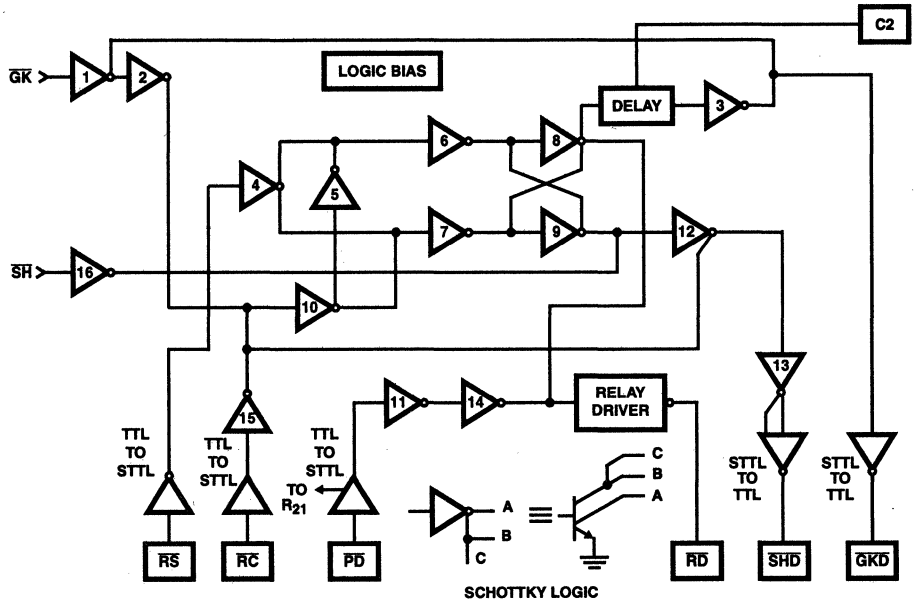
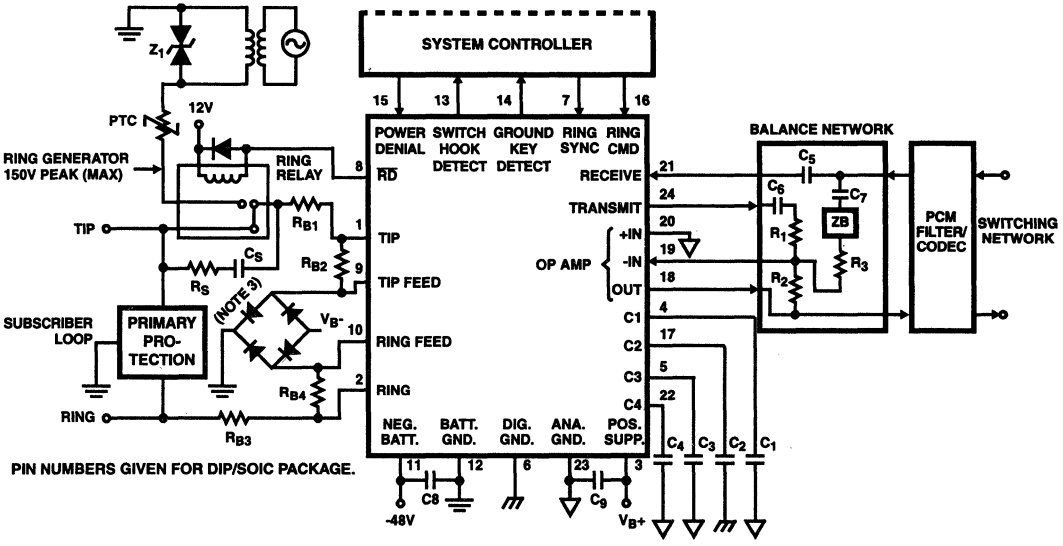


FIGURE 7. HC-5502X/04 LOGIC GATE SCHEMATIC



Typical Component Values

C_1 = 0.5µF (Note 1)

C_2 = 0.15µF, 10V

C_3 = 0.3µF, 30V

C_4 = 0.5µF to 1.0µF, 10%, 20V (Should be nonpolarized)

C_5 = 0.5µF, 20V

$C_6 = C_7$ = 0.5µF (10% Match Required) (Note 2), 20V

C_8 = 0.01µF, 100V

C_9 = 0.01µF, 20V, 20%

$R_1 = R_2 = R_3$ = 100kΩ (0.1% Match Required, 1% absolute value), ZB = 0 for 600Ω Terminations (Note 2)

RB1 = RB2 = RB3 = RB4 = 150Ω (0.1% Match Required, 1% absolute value)

R_S = 1kΩ, C_S = 0.1µF, 200V typically, depending on V_{RING} and line length.

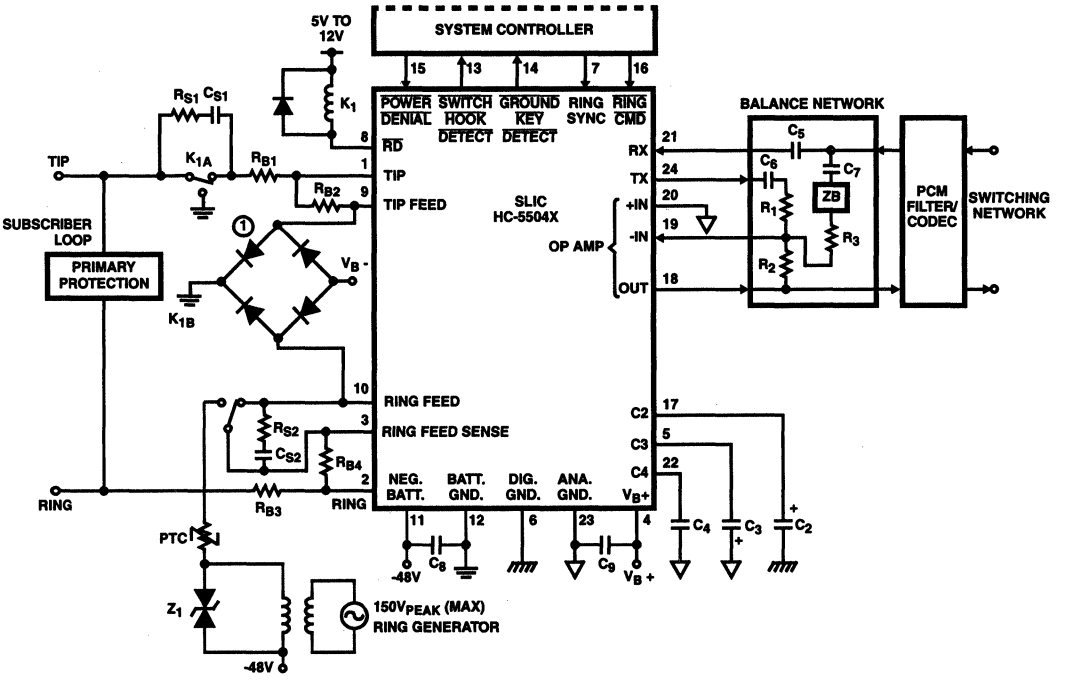
Z_1 = 150V to 200V transient protection. PTC used as ring generator ballast.

NOTES:

1. C_1 is an optional capacitor used to improve V_B+ supply rejection. This pin must be left open if unused.
2. To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C_6-R_1 and R_2 and C_7-Z_B-R_3, to match in impedance to within 0.3%. Thus, if C_6 and C_7 are 1µF each, a 20% match is adequate. It should be noted that the transmit output to C_6 sees a -22V step when the loop is closed. Too large a value for C_6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

   A 0.5µF and 100kΩ gives a time constant of 50ms. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.
3. Secondary protection diode bridge recommended is a 2A, 200V type.
4. All grounds (AG, BG, and DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first

FIGURE 8. HC-5502X LINE APPLICATION CIRCUIT



Typical Component Values

C_2 = 0.15µF, 10V

C_3 = 0.3µF, 30V

C_4 = 0.5µF to 1.0µF, 10%, 20V (Should be nonpolarized)

C_5 = 0.5µF, 20V

C_6 = C_7 = 0.5µF (10% Match Required) (Note 6)

C_8 = 0.01µF, 100V

C_9 = 0.01µF, 20V, 20%

R_1 = R_2 = R_3 = 100k (0.1% Match Required, 1% absolute value) ZB = 0 for 600Ω Terminations (Note 6).

R_{B1} = R_{B2} = R_{B3} = R_{B4} = 150Ω (0.1% Match Required, 1% absolute value).

R_{S1} = R_{S2} =1kΩ, typically.

C_{S1} = C_{S2} = 0.1µF, 200V typically, depending on V_{RING} and line length.

Z_1 = 150V to 200V transient protection.

PTC used as ring generator ballast.

NOTES:

5. Secondary protection diode bridge recommended is a 2A, 200V type.
6. To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C_6-R_1 and R_2 and C_7-ZB-R_3, to match in impedance to within 0.3%. Thus, if C_6 and C_7 are 1mF each, a 20% match is adequate. It should be noted that the transmit output to C_6 sees a -22V step when the loop is closed. Too large a value for C_6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

   A 0.5µF and 100kΩ gives a time constant of 50ms. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.
7. All grounds (AG, BG, and DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
8. Application shows Ring Injected Ringing, Balanced or Tip injected configuration may be used.
9. Pin numbers given for DIP/SOIC package.

FIGURE 9. HC-5504X LINE APPLICATION CIRCUIT

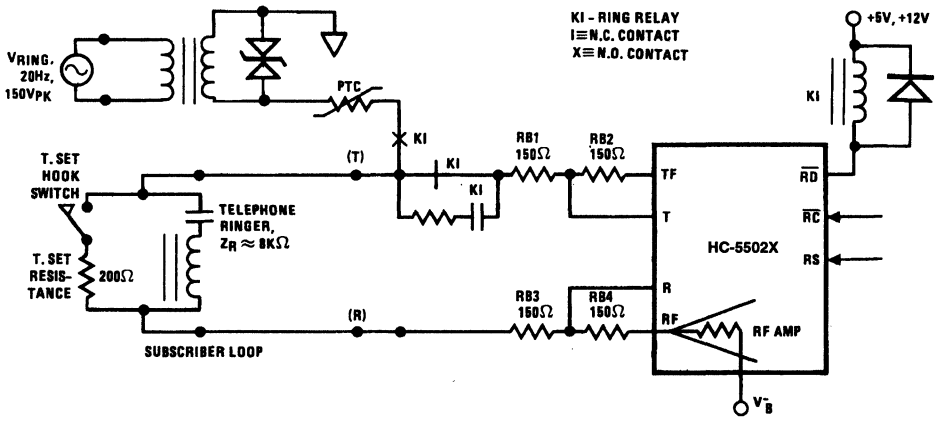


FIGURE 10. HC-5502X TIP INJECTED SINGLE ENDED RINGING

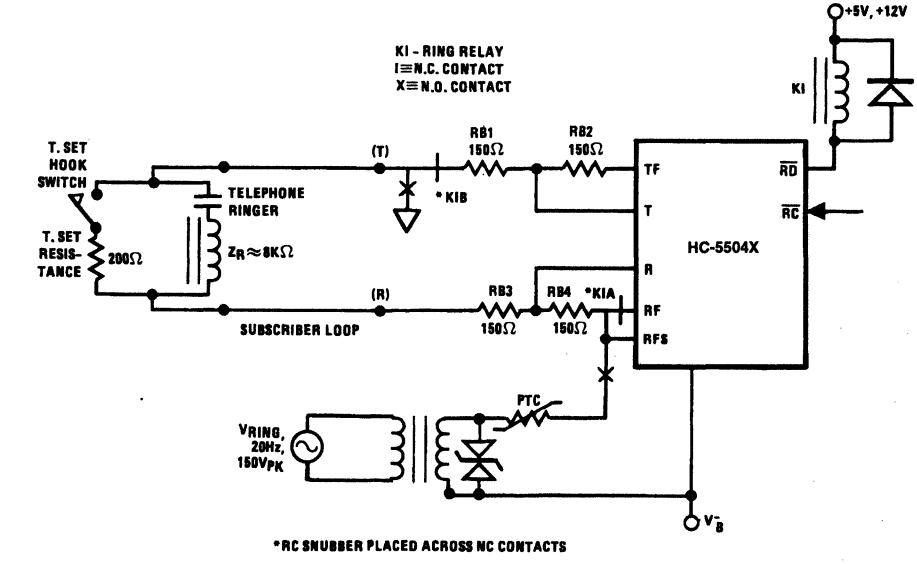


FIGURE 11. HC-5504X RING INJECTED SINGLE ENDED RINGING

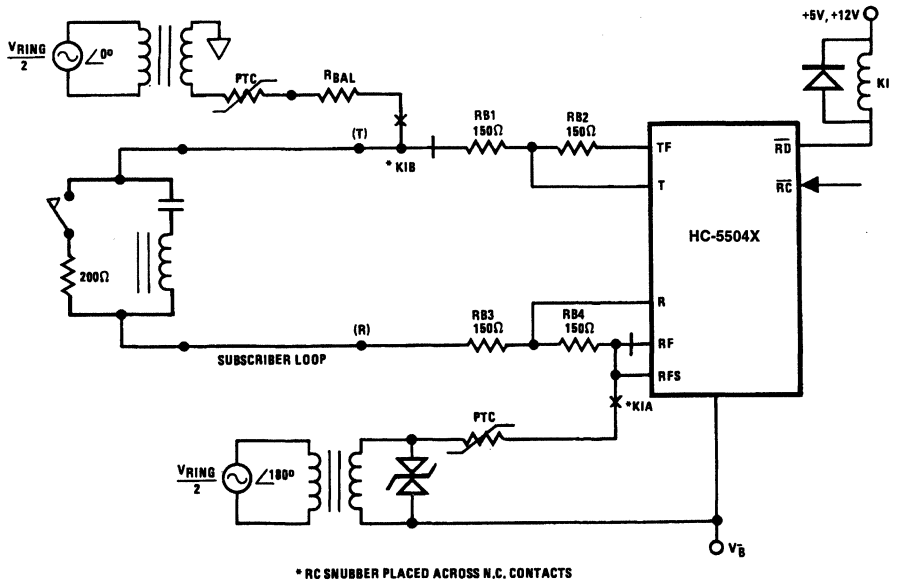


FIGURE 12. HC-5504X BALANCED RINGING CONFIGURATION

The Ring Command (RC) input is taken low during ringing. This activates the ring relay driver (RR) output providing the telephone is not off-hook or the line is not in a power denial state. The ring relay connects the ring generator to the subscriber loop. The ring generator output is usually an $80V_{RMS}$, 20Hz signal. For use with the Harris SLIC, the ring signal should not exceed 150V peak. Since the telephone ringer is AC coupled only ring current will flow. For the HC-5502X SLIC, the ring current is sunk by the ring feed amplifier output stage whereas for the HC-5504X the ring path flows directly into V_{B-} via a set of relay contacts. The high impedance terminal RFS exists on the HC-5504X so that the low impedance R_F node can be isolated from the hot end of the ring path in the battery referenced ring scheme.

The AC ring current flowing in the subscriber circuit will be sensed across RB4, and will give rise to an AC voltage at the output of the longitudinal amplifier. R20 and C4 attenuate this signal before it reaches the ring trip detector to prevent false ring trip. C4 is nominally set at 0.47µF but can be increased towards 1µF for short lines or if several telephones are connected in parallel across the line in order to prevent false or intermittent ring trip.

When the subscriber goes off-hook, a DC path is established between the output winding of the ring generator and the battery ground or V_{B-} terminal. A DC longitudinal imbalance is established since no tip feed current is flowing through the tip feed resistors. The longitudinal amplifier output is driven negative. Once it exceeds the ring trip threshold of the ring trip detector, the logic circuitry is driven by GK to trip the ring relay establishing an off-hook condition such that SHD will become active as loop metallic current starts to flow.

In addition to its ability to be used for tip or ring injected systems, the HC-5504 can also be configured for systems utilizing balanced ringing. Figure 12 shows such an application. The main advantage of balanced ringing is that it tends to minimize cross coupling effects owing to the differential nature of the ring tone across the line.

Figure 13 illustrates the sequence of events during ring trip with ring synchronization for a tip injected ring system. Note, that owing to the 90° phase shift introduced by the low pass filter (R20, C4) the RS pulse will occur at the most negative point of the attenuated ring signal that is fed into the ring trip detector. Hence, when DC conditions are established for RTD, the AC component actually assists ring trip taking place. For a ring side injected ring system, the RS pulse should occur at the positive zero crossing of the ring signal as it appears at RFS. If ring synchronization is not used, then the RS pin should be held permanently to a logic high of 5V nominally: ring trip will occur asynchronously with respect to the ring voltage. Ring trip is guaranteed to take place within three ring cycles after the telephone going off-hook.

It is recommended that an RC snubber network is placed across the ring relay contacts to minimize inductive kickback effects from the telephone ringer. Typical values for such a network are shown in Figure 9.

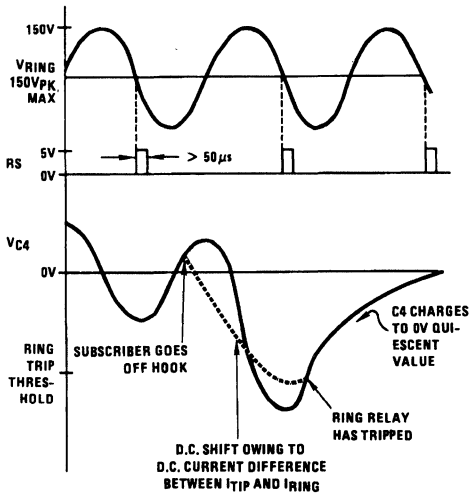


FIGURE 13. RING TIP SEQUENCE

Power Denial (PD)

Power denial limits power to the subscriber loop: it does not power down the SLIC, i.e. the SLIC will still consume its normal on-hook quiescent power during a power denial period. This function is intended to "isolate" from the battery, under processor control, selected subscriber loops during an overload or similar fault status.

If PD is selected, the logic circuitry inhabits RC and switches in a current source to C3. The capacitor charges up to a nominal -3.5V at which point it is clamped. Since TF is always biases at -4V, the battery feed across the loop is essentially zero, and minimum loop power will be dissipated if the circuit goes off-hook. No signalling functions are available during this mode.

After power denial is released (PD = 1), it will be several hundred milliseconds (300ms) before the R_F output reaches its nominal battery setting. This is due to the RC time constant of R21 and C3.

Transhybrid Loss and Longitudinal Balance

During 4W to 2W transmission, the 4W signal is returned to the transmit output: this is called transhybrid return: it is not a reflection from the line as it will only occur if the loop is closed. In order to prevent echo and instability in the switch, this returned signal must be balanced out before it reaches the filter/CODEC. The level of the returned signal is given below, and a balancing network utilizing the on-chip spare op amp is indicated in Figure 14. Since the returned received signal's amplitude and phase are a function of the line's AC impedance, the balance network is a function of the same.

For a resistive line, the two arms of the balance network (Figure 14) are also resistive. In the simplest case, for a 600Ω system, the two parts of the summing network have equi-resistance values. For a transhybrid balance greater than 36dB, component tolerances of ±0.5% are recommended. Both arms of the summing network are capacitively coupled since the TA and TF amplifiers have output and input D.C. biases, respectively. The values of the capacitors are chosen to prevent degradation of the audio frequency response. For capacitive values of 0.5µF, components with tolerances of 10% can be used since at voice band frequencies the reactance of the capacitor has minimal effect on the impedance of the balance network.

The transhybrid returned signal is given by:

$$V_{TX} = -V_{RX} \frac{(4R)}{(2R + Z_L)}$$

where $R = (R_{B1} + R_{B2}) = (R_{B3} + R_{B4})$, and Z_L = Line Impedance.

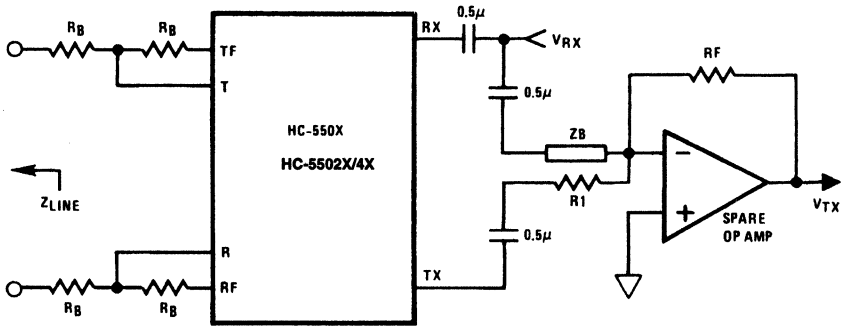
For the balance network, the general equation is given by:

$Z_B = 2R + Z_L$ with R1 = 4R in Figure 14.

A full derivation of the balance equation is given in Appendix 1. A measure off this balance is known as transhybrid loss. For a 600Ω resistive line, a balance of 40dB at 1kHz is attainable. In practice owing to variations in lines and telephone sets the balance is usually lower than in the ideal case: A balance in the order of 25dB will often be measured and accepted.

By switching out the balance network, it is possible for the controller to conduct loop back tests providing the loop can be closed via a test relay in the line card.

Longitudinal balance is equivalent to common mode rejection ratio. Looking into the line card tip and ring terminals towards the SLIC, the 2W balance is a function of the impedance match between tip and ring to ground. The 4W balance is a function of the 2W balance, and the matching of the feedback resistor ratios around the transversal amplifier. (The TA itself must also exhibit a CMRR in excess of the required longitudinal balance.) The SLIC user can only control the matching of the feed resistors. For a nominal 60dB of rejection, these must match within 0.1%. The on-chip resistors are thin film SiCr resistors and are matched within 0.1%. The amplifier has a CMRR of 70dB giving a typical 4W balance of 60dB.



$Z_B = R1\left(\frac{4R_B + Z_L}{8R_B}\right)$ WHERE $R_B = 150$

$\therefore$ IF $Z_L = 4R_B$ (i.e. 600Ω LINE)

THEN $Z_B = R1$

IN GENERAL CASE IF R1 IS SCALED TO $R1 = 8KR_B$

$Z_B = K(4R_B + Z_L)$ WHERE $K = 10, \rightarrow 100$

FIGURE 14. SLIC TRANSHYBRID BALANCE EQUATIONS

Complex Impedance Matching

The SLIC is usually used in systems that have a line characteristic impedance of 600Ω resistive. Thus, the 4 x 150Ω feed resistors present a balanced 600Ω load to the line. If the characteristic impedance of the line varies from 600Ω but remains resistive, then this can be compensated for by increasing or decreasing the value of R_{B1} and R_{B3}. For example, if the line is defined as 900Ω resistive, then R_{B1} and R_{B3} could be increased to 300Ω each and the line will be matched. The increase in feed resistance could impact the DC performance on long lines.

In cases of lines having a complex characteristic impedance, the SLIC circuit can be configured to adequately match the line. Figure 15 shows a typical equivalent line impedance as defined in many European countries. Figure 16 illustrates the circuitry required to match and balance such a line. The component design equations are given in Appendix A along with a qualitative description of the circuit to explain its operation.

For the equivalent impedance shown in Figure 15, it can be seen that at low frequencies, the impedance will increase and become more resistive. As the voice frequency increases, the reactance of C_L decreases, thus the line impedance will also decrease. In order to match the line impedance, a feedback network is required that provides low frequency positive feedback and high frequency negative feedback. The scheme of Appendix A does this.

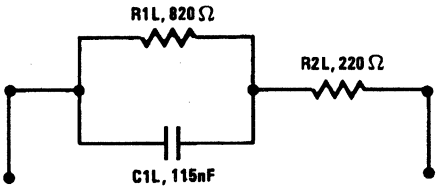


FIGURE 15. RING TIP SEQUENCE

The degree of match over the voice band is a function of the R and C component tolerances and the degree of approximation to their theoretical values. The curves in Figure 16 show typical matching characteristics. The objective is to maximize the 2W return loss. Some values are indicated in Figure 16.

For complex impedance applications a certain amount of circuit optimization will be required by the user in order to obtain an adequate 2W return loss performance and a satisfactory transmit frequency response.

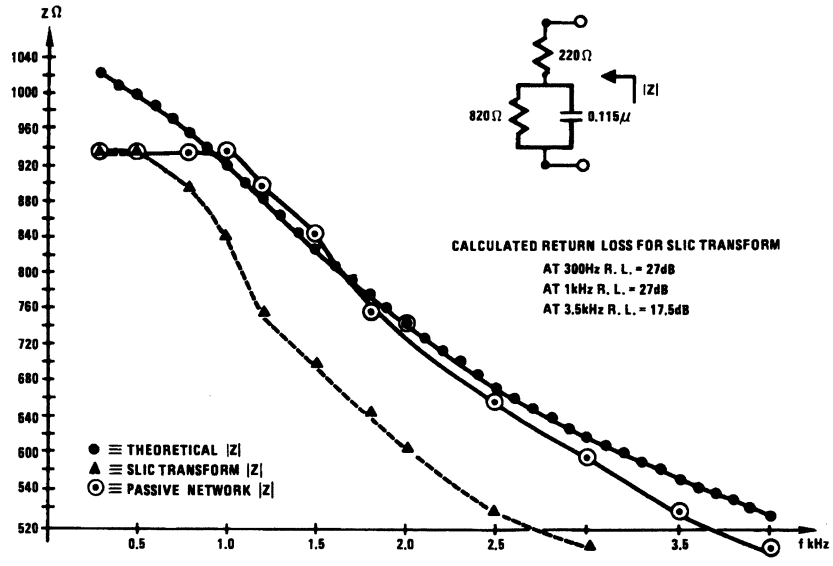


FIGURE 16. |Z| vs FREQUENCY

Line Fault Protection

The subscriber loop can exist in a very hostile electrical environment. It is often in close proximity to very high voltage power lines, and can be subjected to lightning induced voltage surges. The SLIC has to provide isolation between the subscriber loop and the telephone office. Methods for dealing with longitudinally induced power frequency currents and excessive DC line current have been discussed.

The most stringent line fault condition that the SLIC has to withstand is that of the lightning surge.

The Harris monolithic SLIC in conjunction with a simple low cost diode bridge can achieve up to 1kV of isolation between the loop and switch office. The level of isolation is a function of the packaging technology and geometry together with the chip layout geometries. One of the principal reasons for using DI technology for fabricating the SLIC is that it lends itself most readily to manufacturing monolithic circuits for high voltage applications.

Figures 8 and 9 show general application circuits for the HC-5502X and HC-5504X SLICs. A secondary protection diode bridge is indicated which protects the feed amplifiers during a fault. Figure 18 illustrates more clearly the fault current paths during a lightning or transient high voltage strike. Most line systems will have primary protection networks. They often take the form of a carbon block or arc discharge device. These limit the fault voltage to 500V - 1000V peak before it reaches the switch line cards. Thus when a transient high voltage fault has occurred, it will be transmitted as a wave front down the line. The primary protection network limits the voltage to 500V to 1000V. The attenuated wave front will continue down the line towards the SLIC. The feed amplifier outputs appear to the surge as very low impedance paths to the system battery. Once the surge reaches the feed resistors, fault current will flow into or out of the feed amplifier output stages until the relevant protection diodes switch on. Bench measurements have indicated peak fault currents of up to 150mA into and out of the SLIC during the finite turn on time of the diode bridge. Once the necessary diodes have started to conduct all the fault current will be handled by them. The geometry of the SLIC and its package has been designed to withstand the full rated peak fault voltage at its tip (T) and ring (R) terminals: for ceramic packages this is 500V peak, and for plastic (or epoxy) packaged SLICs this is 1000V peak. The circuits are rated against standard lightning characteristics defined by Figure 19. The ceramic package contains an air gap whereas the plastic packages contain no void. The dielectric constant of air is lower than that of the epoxy and it is this which breaks down at lower voltages than the plastic compound.

If the user wishes to characterize SLIC devices under simulated high voltage fault conditions on the bench, he should ensure that the negative battery power supply has sufficient current capability to source the negative peak fault current and low series inductance. If this is not the case, then the battery supply could be pulled more negative and destroy the SLIC if the total (V_B+ + V_B-) voltage across it exceeds 75V.

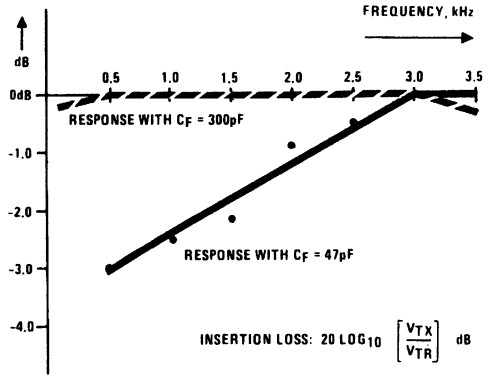


FIGURE 17. TWO WIRE - FOUR WIRE TRANSMISSION

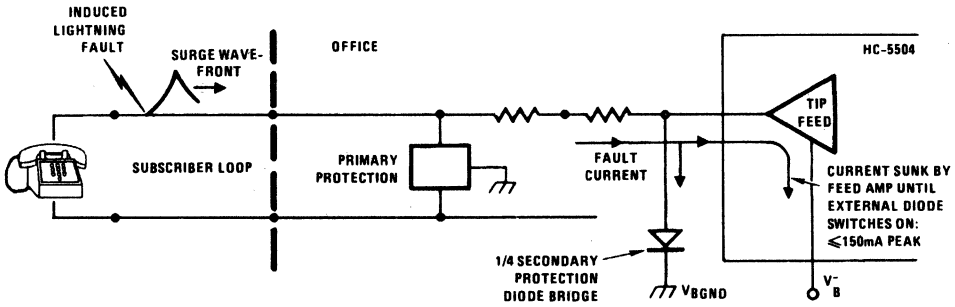


FIGURE 18. FAULT PROTECTION

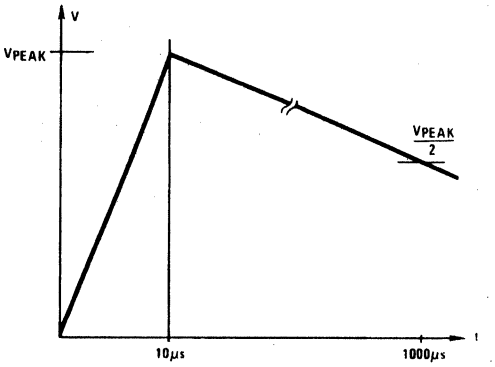


FIGURE 19. SIMULATED LIGHTNING STRIKE WAVEFORM

Appendix A

COMPLEX LINE IMPEDANCE MATCHING WITH SLIC

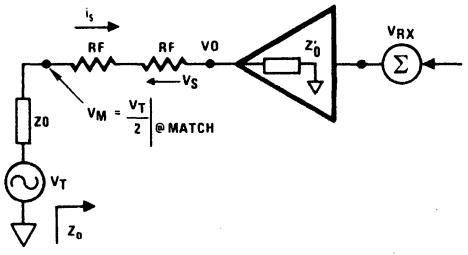


FIGURE A1. TWO TO FOUR WIRE TRANSMISSION. SINGLE ENDED AC EQUIVALENT CIRCUIT OF SUBSCRIBER LOOP.

Consider Figure A1. Assume $V_{RX} = 0$.
(2W to 4W transmission). At match:

$$i_s = \frac{V_T}{2Zo} = \frac{Vm}{Zo}$$

$$Zo = 2R_F + Zo'$$

$$Zo' = \frac{Vo}{i_s}$$

$$Vo = Zo' \cdot i_s = i_s Zo - 2i_s R_F$$

but $Vm = i_s Zo$; $\therefore Vo = Vm - 2i_s R_F$ (EQ. 1)

$$Vs = i_s R_F, \quad \therefore Vs = \frac{R_F}{(2R_F + Zo')} \times Vm$$

$$\therefore Vm = (i_s R_F)\frac{(2R_F + Zo')}{R_F} \quad \text{(EQ. 2)}$$

(2) in (1) for Vm, and $Zo = 2R_F + Zo'$

$$Vo = 2Vs\left(\left(\frac{Zo}{2R_F}\right) - 1\right)$$

This matching equation can be realized as shown in Figure A2.

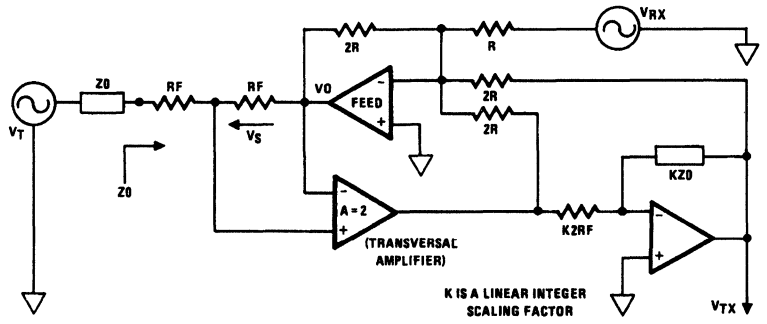


FIGURE A2. FOUR WIRE TO TWO WIRE TRANSMISSION

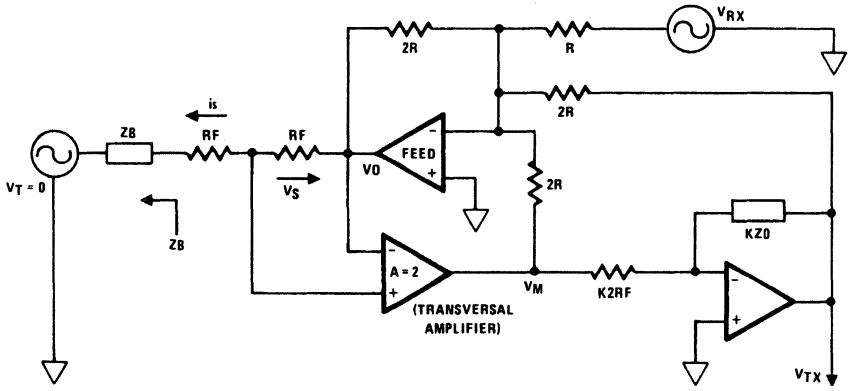


FIGURE A3.

Transhybrid Balance

Consider Figure A3. Evaluate V_{TX} in terms of V_{RX}, in order to establish transhybrid balance equation.

For general case, let line transhybrid impedance be Z_B.

$$Vo = -2\left[V_{RX} + \frac{Vm}{2} + \frac{V_{TX}}{2}\right] \quad \text{(EQ. 3)}$$

$$Vm = -2Vs = \frac{-2R_F}{2R_F + Z_B} \times Vo$$

$$V_{TX} = \frac{(Zo)}{(2R_F + Z_B)} \times Vo \quad \text{(EQ. 4)}$$

From Equation 3:

$$V_{RX} = -\left[\frac{Vo}{2} + \frac{Vm}{2} + \frac{V_{TX}}{2}\right]$$

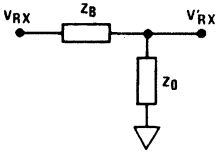
$$2V_{RX} = -\left[\frac{Z_B + Zo}{2R_F + Z_B}\right] \times Vo$$

$$V_{RX} = \frac{-(Z_B + Zo)}{2(2R_F + Z_B)} \times Vo \quad \text{(EQ. 5)}$$

Compare Equations 4 and 5: we need to scale Equation 5 by:

$$Zo\left(\frac{2}{Z_B + Zo}\right)$$

in order to equate to Equation 4.



V_{RX} = EQUATION 5.

$$V'_{RX} = \frac{Zo}{2(2R_F + Z_B)} \times Vo$$

$$\therefore V'_{RX} = \frac{-V_{TX}}{2}$$

Transhybrid balance can be achieved using simple summing amplifier network.

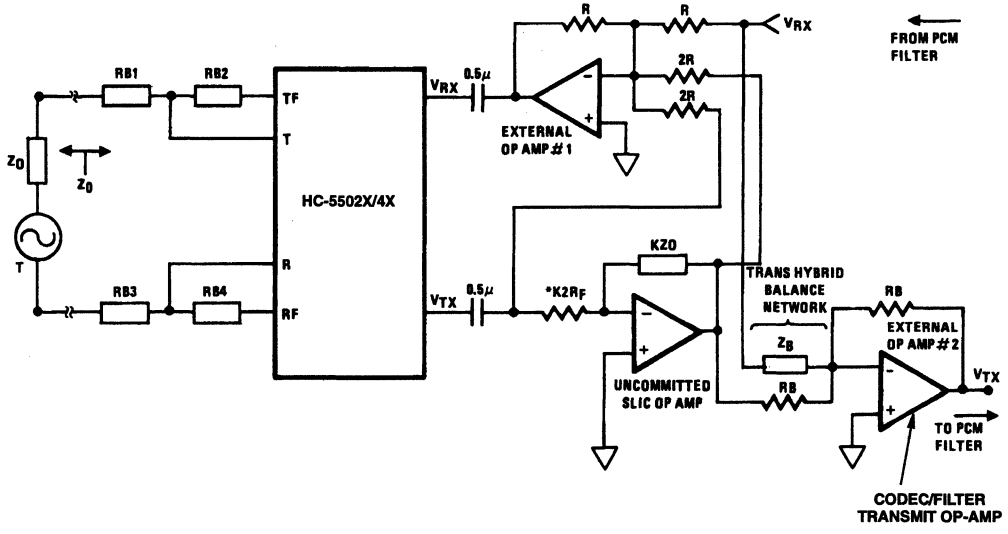
If Z_B - Zo then Equation 5 becomes:

$$V_{RX} = \frac{-(Zo)}{(2R_F + Zo)} \times Vo \quad \text{(EQ. 6)}$$

and Equation 4 becomes:

$$V_{TX} = \frac{Zo}{2R_F + Zo} \times Vo \quad \text{(EQ. 7)}$$

$\therefore V_{TX} = -V_{RX}$ and TH balance is achieved using a resistive summing amp network. The complete application circuit is shown in Figure A4.



* $R_F = R_{B2} + R_{B4}$

FIGURE A4. APPLICATION OF SECOND LINE IMPEDANCE MATCHING ALGORITHIM

Harris Semiconductor

APPNOTE

No. AN571.1 January 1997

Harris Linear

Using Ring Sync with HC-5502A and HC-5504 SLICs

Author: Dave Donovan

Introduction

The ring synchronization (sync) input pin is a TTL compatible clock input in both the HC-5502A and HC-5504 SLICs. It's purpose is to insure that the ring relay is activated or deactivated only when the instantaneous AC ring voltage, which may be as high as 150V peak, is at or near AC zero crossing.

If ring sync is not used, it must be tied high to insure proper ring trip. When used, it is important to consider at which zero crossing of the AC ring voltage, positive or negative, the ring sync signal must be synchronized with. Subsequent illustrations and equations highlight this consideration.

For detailed description of the ring trip sequence of events, refer to Application Note 549 by P. G. Phillips. Excerpts from the pertinent section are included below.

Ring Trip Sequence

The Ring Command ($\overline{RC}$) input is taken low during ringing. This activates the ring relay driver ($\overline{RD}$) output providing the telephone is not off-hook or the line is not in a power denial state. The ring relay connects the ring generator to the subscriber loop. The ring generator output is usually an $80V_{RMS}$, 20Hz signal. For use with the Harris SLIC, the ring signal should not exceed 150V peak. Since the telephone ringer is AC coupled, only ring current will flow. For the HC-5502A SLIC, the ring current is sunk by the ring feed amplifier output stage whereas for the HC-5504 the ring path flows directly into V_B- via a set of relay contacts. The high impedance terminal RFS exists on the HC-5504 so that the low impedance RF node can be isolated from the hot end of the ring path in the battery referenced ring scheme.

The AC ring current flowing in the subscriber circuit will be sensed across RB4, and will give rise to an AC voltage at the output of the longitudinal amplifier. R19 and C4 attenuate this signal before it reaches the ring trip detector to prevent false ring trip. C4 is nominally set at 0.47µF but can be increased towards 1µF for short lines or if several telephones are connected in parallel across the line in order to prevent false or intermittent ring trip.

When the subscriber goes off-hook, a DC path is established between the output winding of the ring generator and the battery ground or V_B- terminal. A DC longitudinal imbalance is established since no tip feed current is flowing through the tip feed resistors. The longitudinal amplifier output is driven negative. Once it exceeds the ring trip threshold of the ring trip detector, the logic circuitry is driven by GK to trip the ring relay establishing an off-hook condition such that SHD will become active as loop metallic current starts to flow.

Figure 1 illustrates the sequence of events during ring trip with ring synchronization. Note, that owing to the 90° phase shift introduced by the low pass filter (R19, C4) the RS pulse will occur at the most negative point of the attenuated ring signal that is fed into the ring trip detector. Hence, when DC conditions are established for RTD, the AC component actually assists ring trip taking place. If ring synchronization is not used, then the RS pin should be held permanently to a logic high of 5V nominally: ring trip will occur asynchronously with respect to the ring voltage. Ring trip is guaranteed to take place within three ring cycles after the telephone going off-hook.

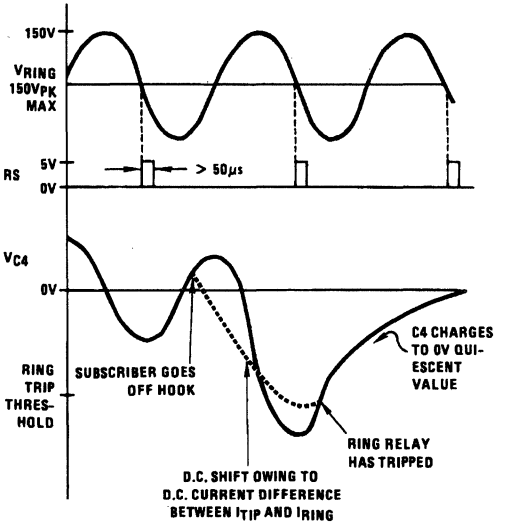


FIGURE 1. RING TRIP SEQUENCE

Case 1: HC-5502A Tip Injected Ringing

$V_{LA} = (I_{RING} - I_{TIP})$ (RB4) (K)
(During Ringing $I_{TIP} = 0$)
$V_{LA} = (I_{RING})$ (RB4) (K)
$I_{RING} = (V_{RF} - V_{RING})/RB4$
$V_{LA} = (V_{RF} - V_{RING})$ K

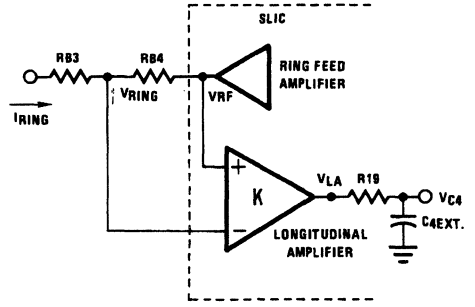


FIGURE 2.

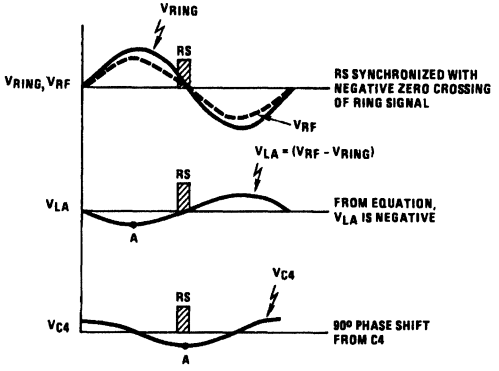


FIGURE 3.

For Case 1, refer to Figures 2 and 3. In this situation the desired result is obtained, namely, that ring sync occurs during the negative peak of V_{C4}. This helps achieve ring trip faster because, once a subscriber goes off-hook, a negative DC shift is observed at V_{C4}. This shift approaches a comparator threshold in the ring trip detection circuit. If the negative peak of V_{C4}(AC) precedes the negative going DC shift at V_{C4}, one can achieve ring trip in a shorter time frame. Also this configuration allows ring trip to occur for long lines, in the order of 3000Ω. At these line lengths, the DC negative shift will never reach the threshold because there is not enough DC current through the sense resistor, RB4. However, the negative peak of V_{C4} (AC) will cross the ring trip detector comparator threshold and ring trip will occur.

Conclusion 1: For this case make sure ring sync is synchronized with the negative zero crossing of V_{RING} as it appears on the line.

Case 2: HC-5504 Ring Injected Ringing

$V_{LA} = (I_{RING} - I_{TIP})$ (RB4) (K)
(During Ringing $I_{TIP} = 0$)
$V_{LA} = (I_{RING})(RB4)$ (K)
$I_{RING} = (V_{RFS} - V_{RING})/RB4$
$V_{LA} = (V_{RFS} - V_{RING})$ K

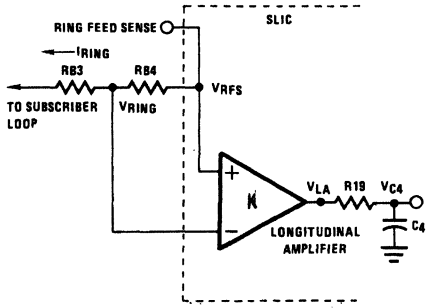


FIGURE 4.

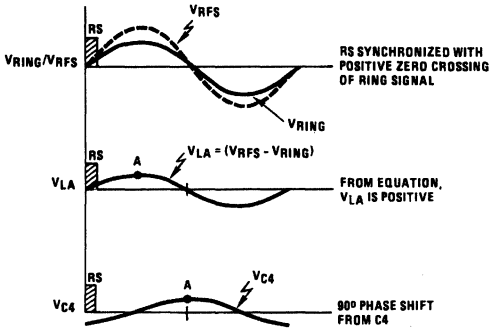


FIGURE 5.

For Case 2 refer to Figures 4 and 5. Here ring sync must be synchronized with the positive zero crossing of V_{RING} (AC) as it appears on the line so as to coincide with the negative peak of V_{C4} (AC), as in the previous case. One can see from Figure 5 that ring sync on the negative zero crossing would coincide with the positive peak of V_{C4}, inhibiting ring trip for loops greater than approximately 800Ω.

Conclusion 2: For this case make sure ring sync is synchronized with the positive zero crossing of V_{RING} (AC.).

For all other ring configurations, namely, tip injected and balanced ringing for the HC-5504, if ring sync is used, it must be synchronized with the negative zero crossing of V_{RING}(AC).

Acknowledgment

The author wishes to thank Geoff Phillips for his contribution to this paper.

Harris Semiconductor

APPNOTE

No. AN573.1 January 1997

Harris Linear

The HC-5560 Digital Line Transcoder

Author: David J. Donovan

Introduction

The Harris HC-5560 digital line transcoder provides mode selectable, pseudo ternary line coding and decoding schemes for North American and European transmission lines. Coding schemes include Alternate Mark Inversion (AMI), Bipolar with N Zero Substitution (BNZS), and High Density Bipolar 3 (HDB3), used for transmission lines as follows:

AMI: North American T1 (1.544MHz) and T1C (3.152MHz) lines

B6ZS: North American T2 (6.3212MHz) lines

B8ZS: North American T1 (1.544MHz) lines

HDB3: European PCM30 (2.048 and 8.448MHz) CEPT lines. Recommended by CCITT

The transcoder is a single chip, single supply device fabricated with standard cell CMOS. Features include simultaneous coding and decoding, asynchronous operation, loop back mode, transmission error detection, an alarm indication signal, and a full chip reset.

This application note will describe why coding for digital transmission is necessary, the types of coding, which is best, and why, and the functionality and applications of the HC-5560 digital line transcoder.

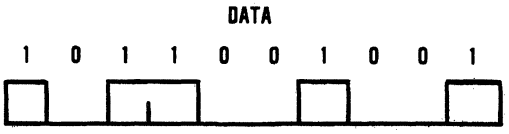
Why Line Coding?

Transmission of serial data over any distance, be it a twisted pair, fiber optic link, coaxial cable, etc., requires "maintenance" of the data as it is transmitted (through repeaters, echo cancellors etc.). The data integrity must be maintained through data reconstruction, with proper timing, and retransmitted. Line codes were created to facilitate this "maintenance".

In selecting a particular line coding scheme some considerations must be made, as not all line codes adequately provide the all important synchronization between transmitter and receiver. Other considerations for line code selection are noise and interference levels, error detection/checking, implementation requirements, and the available bandwidth.

Unipolar Coding

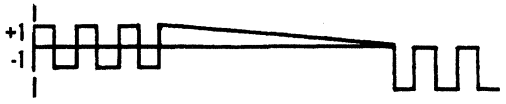
The most basic transmission code is unipolar or unbalanced coding whereby each discrete variable to be transmitted is assigned a different level, 0V and +3V, for example:



UNIPOLAR (UNBALANCED) SIGNAL

There are, however, a number of disadvantages:

- The average power (Ao/2) is two times other codes
- The coded signal contains DC and low frequency components. When long strings of zeros are present, a DC or baseline wander occurs. This results in loss of timing and data because a receiver/repeater cannot optimally discriminate ones and zeros.



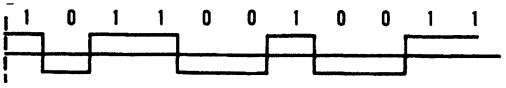
DC WANDER

- Repeaters/receivers require a minimum pulse density for proper timing extraction. Long strings of ones or zeros contain no timing information and lead to timing jitter and possible loss of synchronization.
- There is no provision for line error rate monitoring.

Bipolar Coding is Better

With bipolar, or balanced, coding, the same data may be transmitted more efficiently achieving the same error distance with half the power (Ao/4). This coding is often referred to as Non-Return to Zero (NRZ) coding as the signal level is maintained for the duration of the signal interval.

Although bipolar coding is more efficient than unipolar, it still lacks provisions for line error monitoring, and is susceptible to DC wander and timing jitter.



BIPOLAR (BALANCED) SIGNAL

The HC-5560 digital line transcoder provides a number of augmented bipolar coding schemes which:

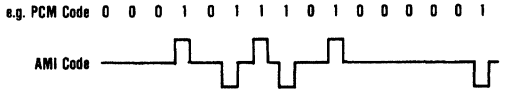
- Eliminate DC Wander
- Minimize Timing Jitter
- Provide for Line Error Monitoring

This is accomplished by introducing controlled redundancy in the code through extra coding levels.

Line Code Descriptions

The HC-5560 transcoder allows a user to implement any of the four line coding schemes described below.

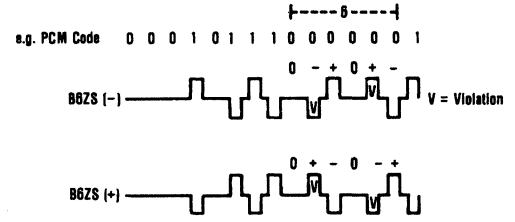
AMI, Alternate Mark Inversion, is used primarily in North American T1 (1.544MHz) and T1C (3.152MHz) carriers. Zeros are coded as the absence of a pulse and one's are coded alternately as positive or negative pulses. This type of coding reduces the average voltage level to zero to eliminate DC spectral components, thereby eliminating DC wander.



To facilitate timing maintenance at regenerative repeaters along a transmission path, a minimum pulse density of logic 1's is required. Using AMI, there is a possibility of long strings of zeros and the required density may not always exist, leading to timing jitter and therefore higher error rates.

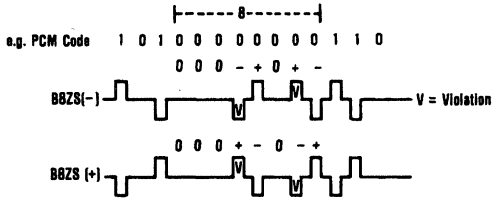
A method for insuring a minimum logic 1 density by substituting bipolar code in place of strings of 0's is called BNZS or Bipolar with N Zero Substitution. B6ZS is used commonly in North American T2 (6.3212MHz) carriers. For every string of 6 zeros, bipolar code is substituted according to the following rule:

If the immediate preceding pulse is of (-) polarity, then code each group of 6 zeros as 0-+0+-, and if the immediate preceding pulse is of (+) polarity, code each group of 6 zeros as 0+-0+. One can see the consecutive logic 1 pulses of the same polarity violate the AMI coding scheme.



B8ZS is used commonly in North American T1(1.544MHz) and T1C(3.152MHz) carriers. For every string of 8 zeros, bipolar code is substituted according to the following rules:

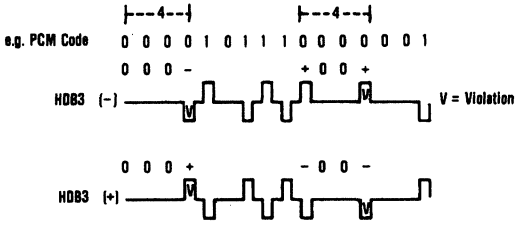
1) If the immediate preceding pulse is of (-) polarity, then code each group of 8 zeros as 000-+0+-.
2) If the immediate preceding pulse is of (z) polarity, then code each group of 8 zeros as 000+-0-+.



The BNZS coding schemes, in addition to eliminating DC wander, minimize timing jitter and allow a line error monitoring capability.

Another coding scheme is HDB3, high density bipolar 3, used primarily in Europe for 2.048MHz carriers. This code is similar to BNZS in that it substitutes bipolar code for 4 consecutive zeros according to the following rules:

1) If the polarity of the immediate preceding pulse is (-) and there have been an odd (even) number of logic 1 pulses since the last substitution, each group of 4 consecutive zeros is coded as 000-(+00+).
2) If the polarity of the immediate preceding pulse is (+) then the substitution is 000+(-00-) for odd (even) number of logic 1 pulses since the last substitution.



The 3 in HDB3 refers to the coding format that precludes strings of zeros greater than 3. Note that violations are produced only in the fourth bit location of the substitution code and that successive substitutions produce alternate polarity violations.

A summary graph of all four substitution coding schemes is illustrated in Figure 1. To simplify timing recovery, logic 1's are encoded with 50% duty cycle pulses.

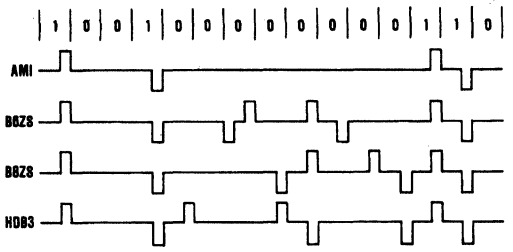


FIGURE 1. SUMMARY OF CODING SCHEMES PROVIDED BY THE HC-5560 TRANSCODER

Functional Description

The HC-5560 transcoder can be divided into six sections: transmitter (coder), receiver (decoder), error detector, all ones detector, testing functions, and output controls. A block diagram is shown in Figure 2.

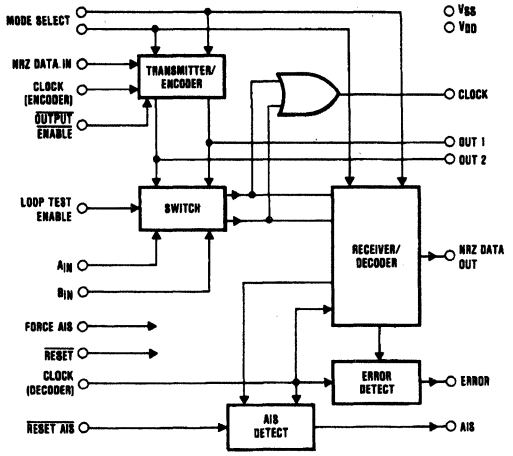


FIGURE 2. HC-5560 TRANSCODER FUNCTIONAL BLOCK DIAGRAM

Transmitter (Coder)

The transmitter codes a non-return to zero (NRZ) binary unipolar input signal (NRZ IN) into two binary unipolar return to zero (RZ) output signals (OUT1, OUT2). These output signals represent the NRZ data stream modified according to the selected encoding scheme (i.e., AMI, B8ZS, B6ZS, HDB3) and are externally mixed together (usually via a transistor or transformer network) to create a ternary bipolar signal for driving transmission lines.

Receiver (Decoder)

The receiver accepts as its input the ternary data from the transmission line that has been externally split into two binary unipolar return to zero signals (A_{IN} and B_{IN}). These signals are decoded, according to the rules of the selected line code into one binary unipolar NRZ output signal (NRZ OUT).

The encoder and decoder sections of the chip perform independently (excluding loopback condition) and may operate simultaneously.

Error Detector

The Error output signal is active high for one cycle of CLK DEC upon the detection of any bipolar violation in the received A_{IN} and B_{IN} signals that is not part of the selected line coding scheme. The bipolar violation is not removed, however, and shows up as a pulse in the NRZ DATA OUT signal. In addition, the Error output signal monitors the received A_{IN} and B_{IN} signals for a string of zeros that violates the maximum consecutive zeros allowed for the selected line coding scheme (i.e., 8 for B8ZS, 6 for B6ZS, and 4 for HDB3). In the event that an excessive amount of zeros is detected, the Error output signal will be active high for one cycle of CLK DEC during the zero that exceeds the maximum number. In the case that a high level should simultaneously appear on both received input signals A_{IN} and B_{IN} a logical one is assumed and appears on the NRZ data out stream with the error signal active.

All Ones Detector

An input signal received at inputs A_{IN} and B_{IN} that consists of all ones (or marks) is detected and signalled by a high level at the alarm indication signal (AIS) output is set to a high level when less than three zeros are received during one period of Reset AIS immediately followed by another period of Reset AIS containing less than three zeros. The AIS output is reset to a low level upon the first period of Reset AIS containing 3 or more zeros.

Testing Functions

A logic high level on LTE enables a loopback condition where OUT1 is internally connected to input A_{IN} and OUT2 is internally connected to B_{IN} (this disables inputs A_{IN} and B_{IN} to external signals). In this condition, the input signal NRZ DATA IN appears at output NRZ DATA OUT (delayed by the amount of clock cycles it takes to encode and decode the selected line code). A decode clock must be supplied for this operation. The Reset input can be used to initialize this process.

Output Controls

The output controls are Output Enable and Force AIS. These pins allow normal operation, force OUT1 and OUT2 to zero, or force OUT1 and OUT2 to output all ones (AIS condition).

Applications

The HC-5560 transcoder is designed for use in North American and European PCM transmission lines where pseudo ternary line code substitution schemes are desired. Any equipment that interfaces to T1, T1C, T2 or PCM30 transmission lines may incorporate transcoders. Such equipment includes multiplexers, channel service units, echo cancellors, repeaters, etc. This section will illustrate and describe a basic circuit application, and various system level applications examples.

Basic Applications Circuit

The basic applications circuit is shown in Figure 3. The encoder accepts serially clocked unipolar non-return to zero (NRZ/PCM) data at the NRZ IN pin and codes it into two unipolar return to zero (RZ) signals at pins OUT1 and OUT2. A coding scheme is chosen via mode select pins MS1 and MS2. Data is clocked in on the negative edge of ECLK and clocked out on the positive edge of ECLK. The outputs must be mixed externally, via a transistor/transformer network, to produce the ternary 'bipolar' code selected and to drive the transmission line. The length of OUT1 and OUT2 are set by the length of the positive ECLK pulse.

To decode ternary coded data, the signal must first be split into two unipolar signals and presented to the A_{IN} and B_{IN} pins. This may be accomplished by an amplifier with a differential output, and two comparators. Both inputs are sampled by the positive edge of DCLK. Decoded data is clocked out in NRZ form to the NRZ OUT pin on the positive edge of DCLK.

All the logic inputs and outputs are TTL compatible.

System Level Examples

Examples of system level transcoder applications are illustrated in Figure 4 through 8.

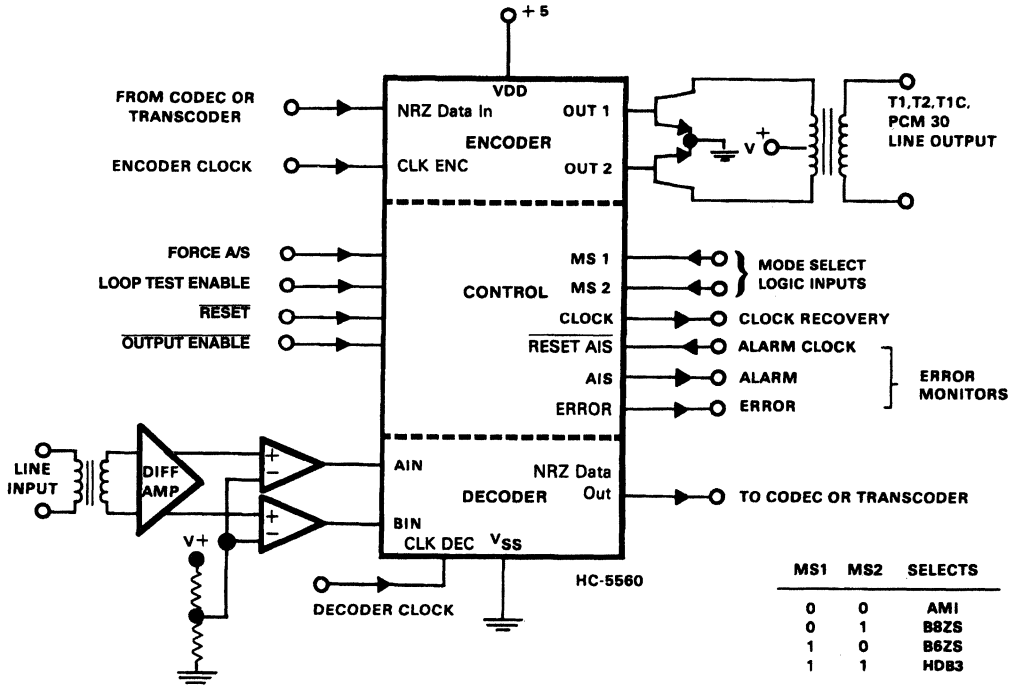


FIGURE 3. BASIC TRNASCODER APPLICATIONS CIRCUIT

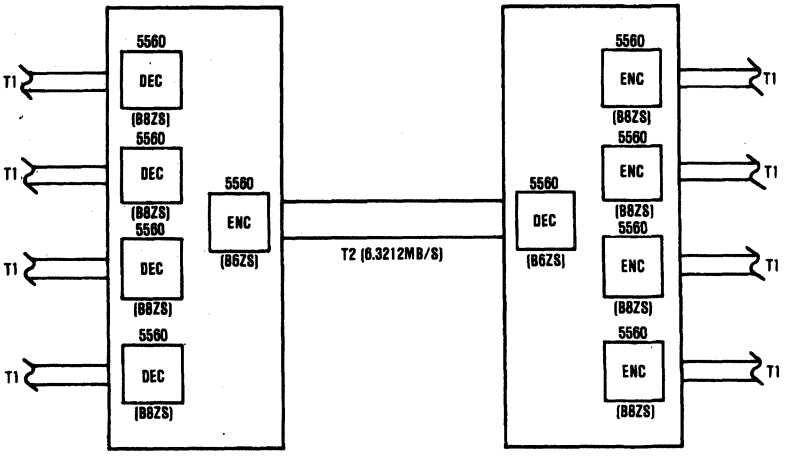


FIGURE 4. M12 MULTIPLIER

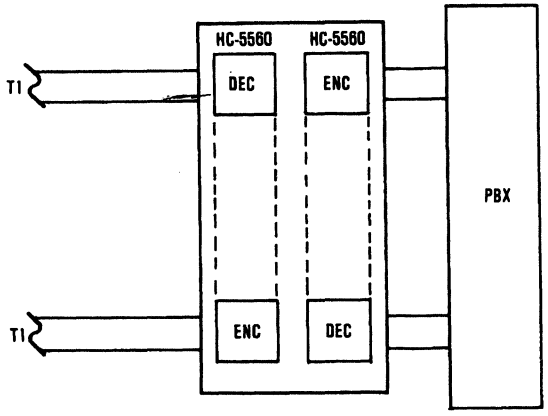


FIGURE 5. CHANNEL SERVICE UNIT (CSU)

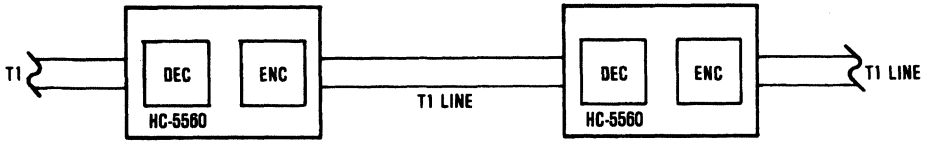


FIGURE 6. ECHO CANCELLOR

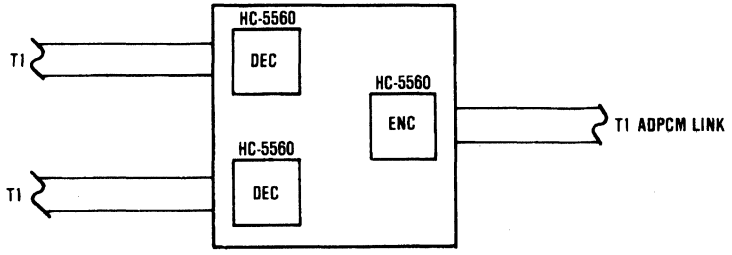


FIGURE 7. T1 COMPRESSION BY ADPCM

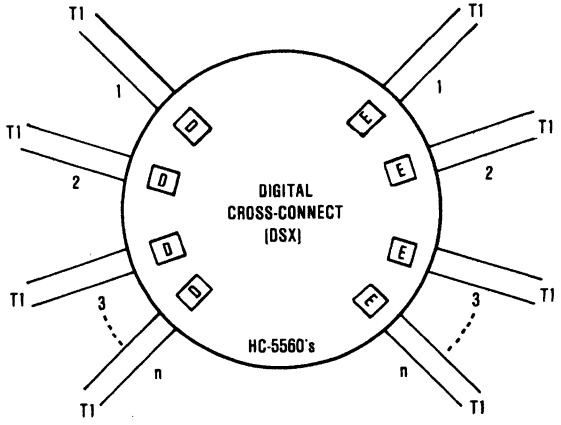


FIGURE 8. DIGITAL CROSS CONNECT (DCS)

Harris Semiconductor

APP NOTE

No. AN574.1 January 1997

Harris Linear

Understanding PCM Coding

Author: David J. Donovan

Introduction

The process of converting analog voice signals into Time Division Multiplexed (TDM) Pulse Code Modulated (PCM) format is described and illustrated herein. Application Note No. 570, "Understanding CODEC Timing", by D.J. Donovan is recommended reading as accompaniment to this application note.

Analog time varying voice input information is transmitted over two-wire (2W) pairs (channels) from subscribers. The PCM filter band-limits voice signals to 4kHz, one per channel, and removes power line and ringing frequencies. Research has shown that voice transmission band-limited to 4kHz has enough fidelity for telephony purposes.

Sampling

The process of converting filtered voice information into a digitized pulse train format begins with sampling the voice signal at uniform intervals. These intervals are determined by the Nyquist Sampling Theorem, which simply states that any signal may be completely re-constructed from its representative sampling if it is sampled at least twice the maximum frequency of interest. The telephone system, being a worldwide standard 8kHz sampling system, satisfies Nyquist, as all voice signals are band-limited to 4kHz. When the voice waveform is sampled, a train of short pulses is produced, each representing the amplitude of the waveform at the specific instant of sampling. This process is called Pulse Amplitude Modulation (PAM). The envelope of the PAM samples replicate the original waveform. Figures 1A thru 1D illustrate representative PAM samples for up to 24(30) individual voice channels in a μ-Law (A-Law) telephone system.

There are relatively large intervals between each PAM sample that may be used for transmitting PAM samples from other voice channels. Interleaving several voice channels on a common bus is the fundamental principle of Time Division Multiplexing (TDM). As the number of voice channels on the TDM bus increases, the time allotted to each sample is reduced, and bandwidth requirements increase (See Figure 1E).

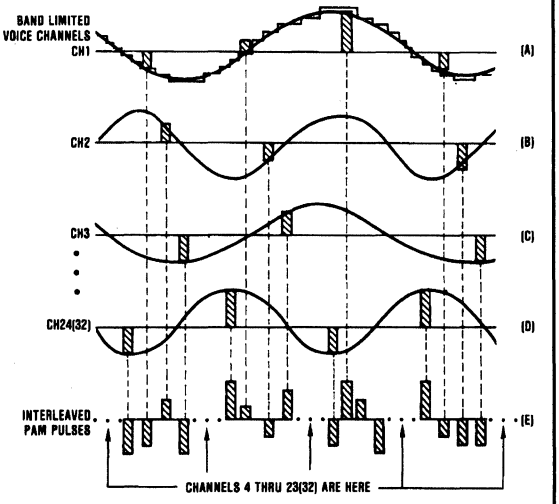


FIGURE 1. (A THROUGH E)

Quantizing

The PAM samples still represent the voice signal in analog form. For digital transmission, further processing is required. Pulse Code Modulation (PCM) is a technique used to convert the PAM samples to a binary weighted code for digital transmission. PCM coding is a two step process performed by the CODEC. The first step is quantization, where each sample is assigned a specific quantizing interval. The second step is PCM coding of the quantizing interval into an 8-bit PCM code word. Each is discussed in the text that follows.

Converting PAM samples to a digital signal involves assigning the amplitude of a PAM sample one of a whole range of possible amplitude values, which are divided into quantizing intervals. There are 256 possible quantizing intervals, 128 positive and 128 negative. The boundaries between adjacent quantizing intervals are called decision values.

If PAM samples are uniformly quantized, there will be situations where several different amplitude values will be assigned the same quantizing interval during encoding. Then, during decoding, one signal amplitude value is recovered for each quantizing interval which corresponds to the midpoint of the quantizing interval. This results in small discrepancies that occur between the original waveform and the quantized approximation; i.e., infinite analog levels in the original waveform being assigned finite quantizing intervals. These discrepancies result in a quantizing noise or quantizing distortion, the magnitude of which is inversely proportional to the number of discrete quantizing intervals. These noise signals may be of the same order of magnitude as the input signal, thereby reducing the signal to quantizing noise ratio to an intolerable level. For this reason non-uniform quantization is used. Large signals need a smaller number of quantizing intervals, while small signals require a larger number of quantizing intervals. Such a non-uniform quantization process is defined as companding characteristics by both Bell and CCITT.

The PCM CODEC performs this non-uniform or non-linear quantization through μ-Law or A-law companding characteristics shown in Figure 2. This process enhances lower amplitude signals, to allow them to compete with system noise, and attenuates higher amplitude signals, preventing them from saturating the system. This form of signal compression results in a relatively uniform signal to quantization noise ratio, approaching 40dB for a wide range of input amplitudes. Also, the dynamic range approaches that of a 13(11) bit A/D or 80(66)dB for μ-Law (A-Law) companding. The digital realization of this companding process is obtained by a segment and chord piecewise linear approximation to a semi-logarithmic function.

Both the μ-Law and A-law companding characteristics are composed of 8 linear segments or chords in each quadrant. Within each chord are 16 uniform quantization intervals, or steps. With μ-Law, moving away from the origin, each chord is twice the width of the preceding chord, and each group of 16 uniform steps is twice the width of the preceding group. It is also referred to as the 15 segment characteristic. The first chord about the origin in the positive and the negative quadrant are of the same slope and are therefore considered one chord (chord 0). With A-law, the first two chords and step groups in each quadrant are uniform. Successive chords and steps follow the same pattern as μ-Law. A-Law is referred to as the 13 segment characteristic. The first two chords about the origin in the positive quadrant, and the first two chords about the origin in the negative quadrant are all of the same slope and therefore are considered one chord (chord 1). There are 64 uniform steps in chord 1, 32 positive and 32 negative. However, for purposes of encoding and decoding samples that fall into the quantization intervals in chord 1, a different 3 bit chord code (refer to Figure 3) is assigned for the first segment of 16 uniform steps closest to the origin and the next segment moving away from the origin. Chord 1 in A-Law is twice that of chord 0 in μ-Law.

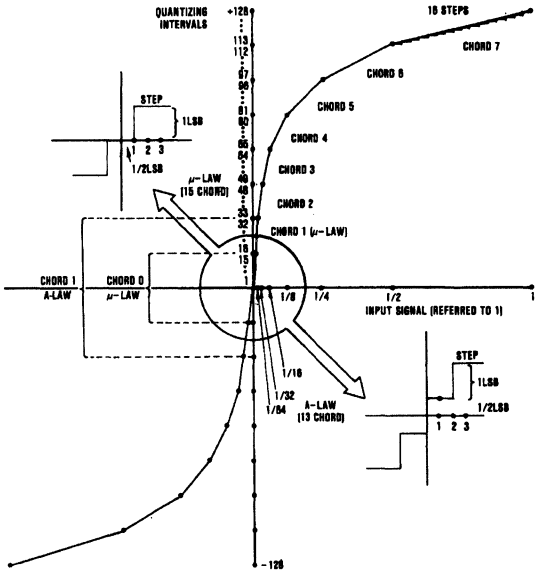


FIGURE 2.

The μ-Law companding characteristic is used primarily in North America and Japan, while A-Law is used primarily in Europe. The differences are minimal and are summarized below:

μ-Law

- Step sizes double for each successive chord
- Virtual edge = ±8159 units
- Input level = 3.172dBm0
- 2 codes for 0 input

A-Law

- Step sizes double for each successive chord after the second chord
- Virtual edge = ±4096 units
- Input level = 3.14dbm0
- No code for 0 input

The input level is determined with reference to the power level at the central office or 'switch'. That point is referred to as the zero transmission level point (0TLP). All CODEC measurements must be translated to the 0TLP. The unit of translated level is the dBm0 (dB relative to 1mW referred to a transmission level of 0TLP).

There is no absolute voltage standard for the CODEC, however, a standard exists relative to full scale. The point at which the CODEC begins to clip is called the virtual edge. It is measured in normalized voltage units or steps, ±8159 steps for μ-Law and ±4096 steps for A-Law. If a PAM sample representing the peak of a voice input signal hits the virtual edge of a μ-Law system, it has a relative power of +3.172dBm0. The corresponding A-Law relative power is +3.14dBm0. These numbers are chosen to minimize intrinsic gain error at 0dBm0 and 1000Hz.

Encoding

The second stage of conversion to binary PCM data for transmission involves the coding of the 256 quantizing intervals assigned to the individual PAM samples into 8-bit binary words (7 data bits plus 1 sign bit). The MSB in each word is a polarity bit indicating a 1 for positive quadrant quantizing intervals, and a 0 for negative quadrant quantizing intervals. The next three bits represent the chord, and the last four bits identify the step within the chord. The 8-bit PCM word partitioning is illustrated in Figure 3.

BIT NUMBER	1	2	3	4	5	6	7	8	
BIT WEIGHT -MSB	±	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LSB
	SIGN	CHORD			STEP				

A-Law and μ-Law coding about the origin differ. μ-Law defines two codes for 0V input while A-Law defines no code for 0V input (see Table 1). The two μ-Law zero codes represent a normal quantization step that is divided into halves by the y-axis of the companding curve (refer to Figure 2). These half steps represent the lowest resolvable signal of the μ-Law characteristic.

TABLE 1.

INPUT	BINARY EQUIVALENT	μ-LAW	A-LAW
+FULL SCALE	1111 1111	1000 0000	1010 1010
+CENTER	1000 0000	1111 1111	1101 0101
-CENTER	0000 0000	0111 1111	0101 0101
-FULL SCALE	0111 1111	0000 0000	0010 1010

Multiplexing and Transmission

Each 8-bit PCM word is transmitted in its respective time slot, which is assigned to each CODEC by the system controller (See Application Note 570). A number of PCM words may be transmitted consecutively from different channels, creating a PCM TDM signal for transmission. Each CODEC channel has an average data rate of 8K samples/sec x 8-bits = 64kbits/s. This means that within a 1/8kHz = 125μs period, 24(30) PCM words of 8 bits each are transmitted consecutively in a μ-Law (A-Law) system.

μ-Law Systems

For μ-Law systems, the bus format allows 24 groups, or timeslots, of 8-bit PCM words, plus one synchronization (sync) bit for a total of 193 bits per frame (see Figure 4). This sync bit partitions the boundary between timeslots 24 and 1, and allows the time slot counter at the receive end to maintain sync with the transmit end. All signalling information is contained in bit 8 (LSB) of the PCM word. These multiplexed frames of 24, 193-bit channels constitute the 1.544MHz T1 transmission channel.

A-Law Systems

For A-Law systems, the bus format groups data into 32 timeslots of 8-bit PCM words each, giving 30 voice channels plus one 8-bit sync and alarm channel, and one 8-bit signalling channel. The sync and alarm, and signalling in formation are contained in channels 0 and 16, respectively (see Figure 4). Bits 2, 4, 6, and 8 are inverted for transmission per CCITT recommendation. These multiplexed frames of 32, 256-bit channels constitute the 2.048MHz PCM30-CEPT (Committee of European Postal and Telegraph) transmission channel.

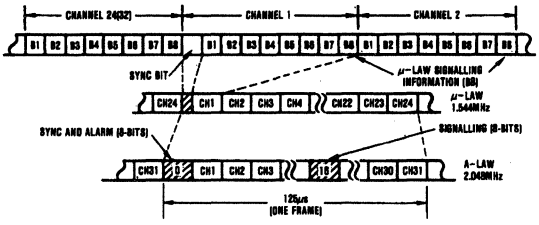


FIGURE 3.

Line Coding

PCM code generated by the CODEC function is in Non-Return to Zero (NRZ) format. It cannot effectively be transmitted directly on a transmission line because the signal contains a DC component and lacks timing information.

An additional coding step is necessary which converts NRZ code to a pseudo ternary code suitable for transmission. Practical coding schemes include Alternate Mark Inversion (AMI), Bipolar with N Zero Substitution (BNZS), and High Density Bipolar 3 (HDB3) coding. These schemes eliminate the DC component of NRZ code, thereby eliminating the troublesome DC wander phenomenon. They also provide a means for detecting line coding errors, and enhance synchronization between transmitter and receiver through reduction of timing jitter. For additional information, refer to Application Note 573, "The HC-5560 Transcoder", by D. J. Donovan.

Demultiplexing

After transmission, the CODEC must recover the 8-bit PCM words from the TDM signal, sort out, decode, and distribute the PCM information appropriately. The demultiplexing process is fully controlled electronically.

Decoding

The CODEC receive function allocates a signal amplitude to each 8-bit PCM word which corresponds to the midpoint of the particular quantizing interval. The expanding characteristic is the same as that for non-linear companding on the transmit side. If the LSB of a μ-Law PCM word contains signalling information, it is extracted by the CODEC, latched into a flip-flop, and distributed to the CODEC signalling output (Sig_R). This means that there is a lost bit (LSB) in the incoming PCM data stream during a signalling frame. The decoder interprets the missing LSB as a 1/2 (i.e. halfway between a 0 and a 1) to minimize noise and distortion. The PCM words are decoded in the order in which they are received and then converted to PAM pulses. The PAM pulses are summed, then low pass filtered, which smooths the PAM envelope and reproduces the original voice signal.

Harris Semiconductor

APPNOTE

No. AN607.1 January 1997

Harris Linear

Delta Modulation For Voice Transmission

Author: Don Jones

Introduction

Delta modulation has evolved into a simple, efficient method of digitizing voice for secure, reliable communications and for voice I/O in data processing.

To illustrate basic principles, a very simple delta modulator and demodulator are illustrated in Figure 1. The modulator is a sampled data system employing a negative feedback loop. A comparator senses whether or not the instantaneous level of the analog voice input is greater or less than the feedback signal. The comparator output is clocked by a flip-flop to form a continuous NRZ digital data stream. This digital data is also integrated and fed back to the comparator. The feedback system is such that the integrator ramps up and down to produce a rough approximation of the input waveform. An identical integrator in the demodulator produces the same waveform, which when filtered, reproduces the voice.

One can see that the digital data 0's and 1's are commands to the integrators to "go up" or "go down" respectively. Another way of looking at it is that the digital data stream also has analog significance; it approximates the differential of the voice, since analog integration of the data reproduces the voice.

Note that the integrator output never stands still; it always travels either up or down by a fixed amount in any clock period. Because of its fixed integrator output slope, the simple delta modulator is less than ideal for encoding human voice which may have a wide dynamic amplitude range.

The integrator cannot track large, high frequency signals with its fixed slope. Fortunately, human speech has statistically smaller amplitudes at higher frequencies, therefore an integrator time constant of about 1ms will satisfactorily reproduce voice in a 3kHz bandwidth.

A more serious limitation is that voice amplitude changes which are less than the height of the integrator ramp during one clock period cannot be resolved. So dynamic range is proportional to clock frequency, and satisfactory range cannot be obtained at desirable low clock rates.

A means of effectively increasing dynamic range is called "companding" (compressing-expanding); where at the modulator, small signals are given higher relative gain, and an inverse characteristic is produced at the demodulator.

The CVSD: A popular effective scheme for companded delta modulation is known as CVSD (continuously variable slop deltamod) shown in Figure 2. Additional digital logic, a second integrator, and an analog multiplier are added to the simple modulator.

Under small input signal conditions, the second integrator (known as the syllabic filter) has no input, and circuit function is identical to the simple modulator, except that the multiplier is biased to output quite small ramp amplitudes giving good resolution to the small signals.

A larger signal input is characterized by consecutive strings of 1's or 0's in the data as the integrator attempts to track the input. The logic input to the syllabic filter actuates whenever 3 or more consecutive 0's or 1's are present in the data. When this happens, the syllabic filter output starts to build up increasing the multiplier gain, passing larger amplitude ramps to the comparator, enabling the system to track the larger signal. Up to a limit, the more consecutive 1's or 0's generated, the larger the ramp amplitude. Since the larger signals increase the negative feedback of the modulator and the forward gain of the demodulator, companding takes place. By listening tests, the syllabic filter time constant of 4 to 10ms is generally considered optimum.

An outstanding characteristic of CVSD is its ability, with fairly simple circuitry, to transmit intelligible voice at relatively low data rates. Companded PCM, for telephone quality transmission, requires about 64K bits/sec data rate per channel. CVSD produces equal quality at 32K bits/sec. (However, at this rate it does not handle tone signals or phase encoded modern transmissions as well.)

CVSD is useful at even lower data rates. At 16K bits/sec the reconstructed voice is remarkably natural, but has a slightly "Fuzzy Edge". At 9.6K bits/sec intelligibility is still excellent, although the sound is reminiscent of a damaged loudspeaker. Of course, very sophisticated speech compression techniques have been used to transmit speech at even lower data rates; but CVSD is an excellent compromise between circuit simplicity and bandwidth economy.

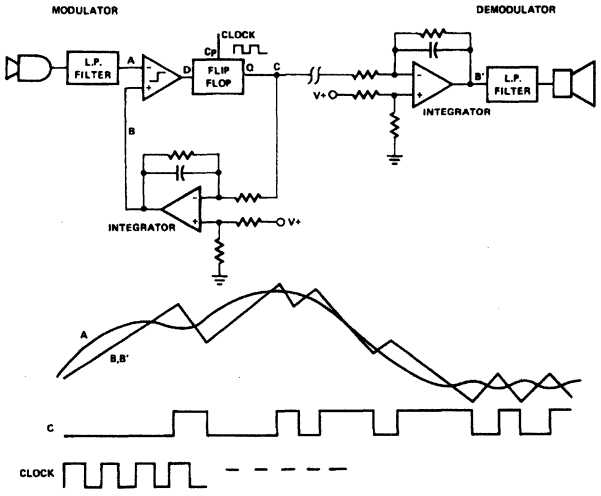


FIGURE 1.

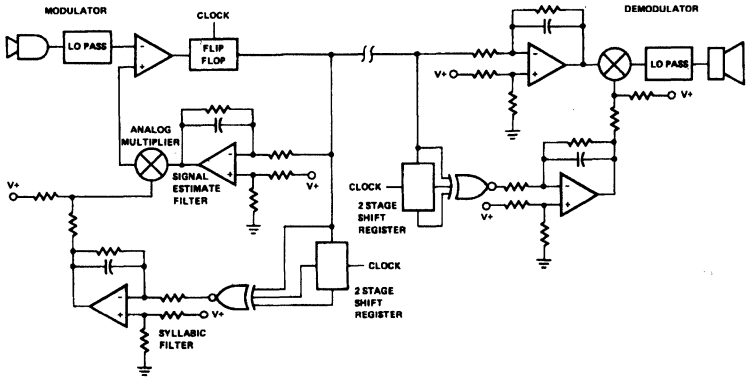


FIGURE 2.

The Digital CVSD

Delta modulated data is in a form which can be digitally filtered with fairly simple circuitry. A compatible CVSD can be made using digital integrators and multipliers driving a digital-to-analog converter. The block diagram of the HC-55564 monolithic CVSD is shown in Figure 3.

The CMOS digital circuit functions of Figure 3 closely parallel the equivalent analog function in Figure 2. The filters are single pole recursive types using shift registers with feedback. A digital multiplier feeds a 10-bit R-2R DAC which reconstructs the voice waveform. The DAC output is in steps, rather than ramps.

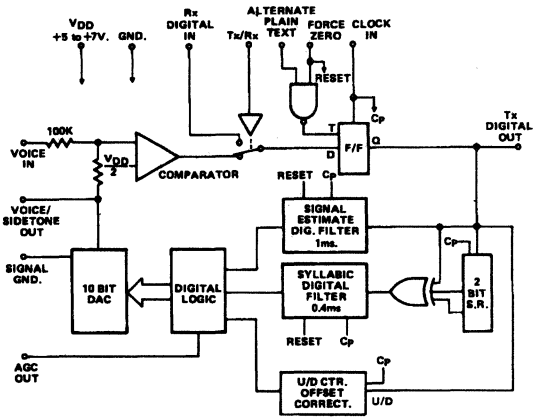


FIGURE 3. HC-55564 CVSD FUNCTIONAL DIAGRAM

The digital CVSD has a number of advantages over its analog counterpart, and has desirable features which would otherwise require additional circuitry:

1) The all CMOS device requires only 1mA current from a single +4.5V to +7V supply.

2) No bulky external precision resistors or capacitors are required for the integrators; time constants of the digital filters are set by the clock frequency and do not drift with time or temperature.

3) For best intelligibility and freedom from listener fatigue, it is important that the recovered audio is quiet during the pauses between spoken words. During quiet periods, an alternate "1", "0" pattern should be encoded, which when decoded and filtered will be inaudible. Achieving this in the analog CVSD requires that up and down ramp slopes are precisely equal and that offsets in the comparator and amplifiers are adjusted to zero. Improper adjustment or excessive component drift can result in noisy oscillations. In the digital design, comparator offset and drift are adjusted by a long up-down counter summed to the DAC to insure that over a period of time equal numbers of 1's and 0's are generated.

   An added feature is automatic quieting, where if the DAC input would be less than 2 LSB's the quieting pattern is generated instead. This has proven to aid intelligibility.

4) To prevent momentary overload when beginning to encode or decode, it is desirable to initialize the integrators. In the analog CVSD, external analog switches would be required to discharge the capacitors.

   In the digital CVSD, the filters are reset by momentarily putting the "Force Zero" pin low. At the same time, a quieting pattern is generated without affecting internal encoding by putting the "Alternate Plain Text" pin low.

5) In some analog CVSD designs, transient noise will be generated during recovery from a low frequency overdriven input condition. The digital CVSD has a clipped output with instant recovery, when overdriven.

6) Half-duplex operation (using the same device, switching between the encode and decode functions) requires external circuits with the analog CVSD, while the digital type is switched internally by a logic input.

Applications of Delta Modulation

1) **Telecommunications**: Digitized signals are easily routed and multiplexed with low cost digital gates. Voice channels may be easily added to existing multiplexed digital data transmission systems. The digital signals are much more immune to crosstalk and noise when transmitted over long distances by wire, R.F., or optical paths. CVSD has better intelligibility than PCM when random bit errors are introduced during transmission.

2) **Secure Communications**: Digital data can be quite securely encrypted using fairly simple standard hardware (Figure 4A). Scrambled speech for audio channels may also be accomplished by encoding into a shift register, then selecting different segments of the shifted data in pseudo-random fashion and decoding it (Figure 4B).

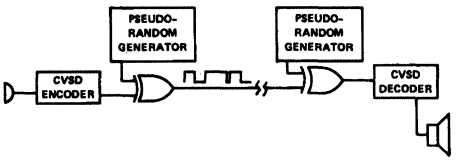


FIGURE 4A. DIGITAL TRANSMISSION ENCRIPTION

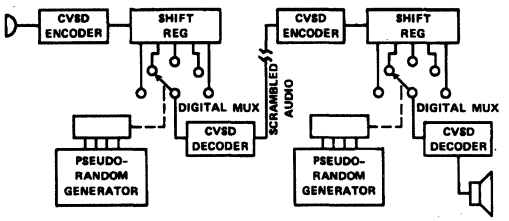


FIGURE 4B. VOICE TRANSMISSION SCRAMBLING

3) **Audio Delay Lines**: Although charge-coupled deviced (CCD) will perform this function, they are still expensive and choice of configurations is quite limited. Also, there is a practical limit to the number of CCD stages, since each introduces a slight degradation to the signal.

   As shown in Figure 5, the delay line consists of a CVSD modulator, a shift register and a demodulator. Delay is proportional to the number of register stages divided by the clock frequency. This can be used in speech scrambling, as explained above, echo suppression in PA systems; special echo effects; music enhancement or synthesis; and recursive or nonrecursive filtering.

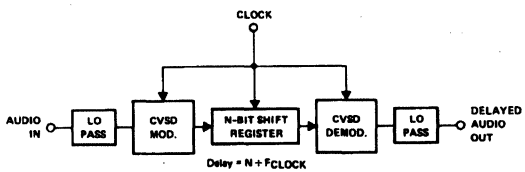


FIGURE 5. AUDIO DELAY LINE

4) **Voice I/O**: Digitized speech can be entered into a computer for storage, voice identification, or word recognition. Words stored in ROM's, disc memory, etc. can be used for voice output. CVSD, since it can operate at low data rates, is more efficient in storage requirements than PCM or other A to D conversions. Also, the data is in a useful form for filtering or other processing.

Figure 6 illustrates a simple evaluation breadboard circuit for the HC-55564. A single device is sufficient to evaluate sound quality, etc. since, when encoding, the feedback signal at pin 3 is identical to the decoded signal from a receiver. The following are some pointers for using the devices:

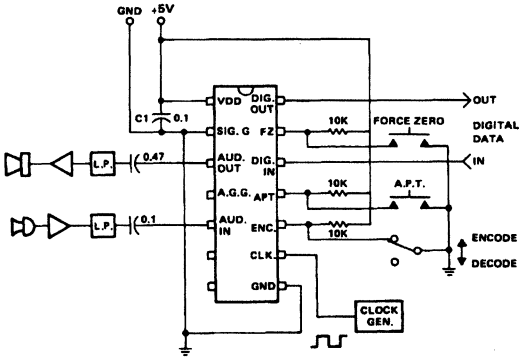


FIGURE 6. CVSD HOOKUP FOR EVALUATION

1) Power supply decoupling is essential with the capacitor (C1 in Figure 6) located close to the I.C.

2) Power to the I.C. must be present before the audio input, the clock, or other digital inputs are applied. Failure to observe this may result in a latchup condition, which is usually not destructive and may be removed by cycling the supply off, then on.

3) Signal ground (pin 2) should be externally connected to pin 8 and power ground. It is recommended for noise-free operation that the audio input and output ground returns connect directly to pin 2 and to no other grounds in the system. Pins 6 and 7 must be open circuited.

4) Digital inputs and outputs are similar to and compatible with standard CMOS logic circuits using the same supply voltage. The illustrated 10K pullup resistors are necessary only with mechanical switches, and are not necessary when driving these pins with CMOS. Unused digital inputs should be tied to the appropriate supply rail for the desired operation. TTL output, however, will require CMOS input levels. Pins 4 and 14 will drive CMOS logic, or each can drive one low power TTL input.

5) Capacitor coupling is recommended for the audio in and out (pins 3 and 5) as each pin is internally biased to about 1/2 the supply voltage.

6) The AGC output (pin 4) is a digital output, whose duty cycle is dependently on the average audio level. This may be externally integrated to drive an AGC preamplifier; or it could be used (through a buffer gate) to drive an LED indicator to indicate proper speaking volume.

7) To prevent generation of alias frequencies, the input filter should reduce the audio amplitude at frequencies greater than half the clock rate to less than $12mV_{P-P}$.

8) The PCM Filter shown in the data sheet lends itself well as a cost-effective input/output filter to the CVSD.

9) A suggested receiver clock circuit is a free running multivibrator, synchronized at each transition of the incoming data. Any synch errors occurring during reception of long strings of zeros or ones will have negligible effect on the decoded voice.

Figures 7 through 11 illustrate some typical audio output (before filtering) and digital output waveforms. To make the scope picture stationary, the audio input generator was synchronized with a submultiple of the clock frequency.

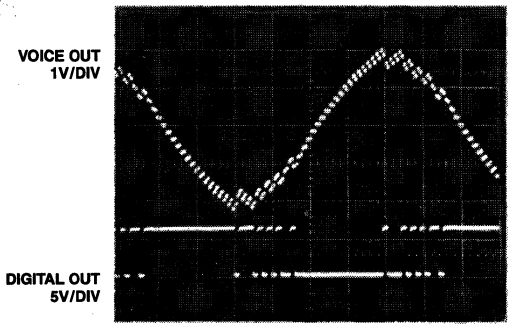
Figure 7 shows the results of a large low frequency sine wave. The somewhat jagged peaks are typical of all CVSD systems. Note that the digital output is continuous "ones" while the waveform is slewing down and continuous "zeros" while slewing up.

Figure 8 shows the excellent recovery from overdriven conditions at low frequency. Some analog type CVSD's have trouble recovering from this condition.

As mentioned previously, CVSD's cannot handle large signals at high frequencies (but these are not generally present in the human voice). Figure 9 shows this limitation where the voice output is slewing at its maximum rate, but cannot catch up with the input. At reduced amplitudes, however, the same signal can be reproduced, as shown in Figure 10.

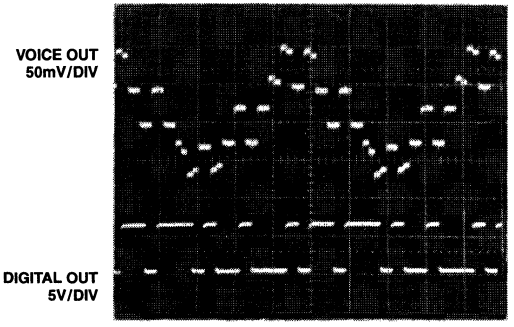
The transfer function curve on the data sheet shows that at 16kHz clock rate, a $1.2V_{RMS}$ signal can be tracked up to 500Hz. With a 32kHz clock, the same curves may be used, but with each of the indicated frequencies doubled. Likewise, each of the SNR figures shown on the data sheet will be 6dB better than a 32kHz clock.

Figure 11 shows the 10mV voice output waveform at 1/2 the clock rate, when there is no audio input. After filtering, this signal is inaudible.



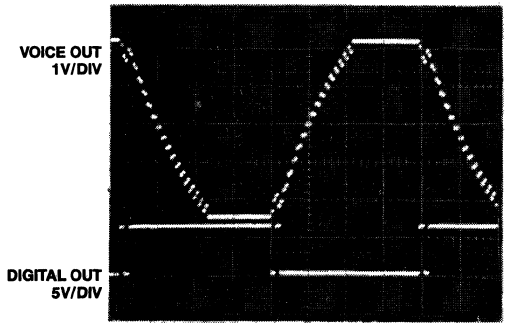
0.5ms/DIV
VOICE IN = 250Hz, $4V_{P-P}$ SINE WAVE
CLOCK = 16kHz

FIGURE 7. CVSD LARGE SIGNAL SINE WAVE RECONSTRUCTION



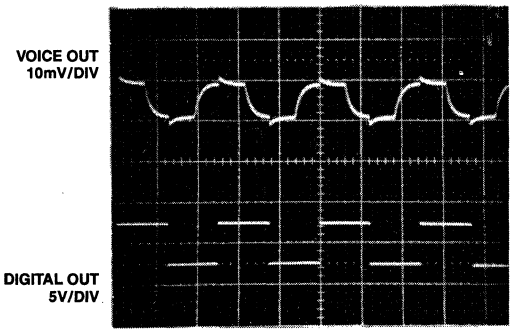
0.2ms/DIV
VOICE IN = 1kHz, $0.15V_{P-P}$ SINE WAVE
CLOCK = 16kHz

FIGURE 8. CVSD SMALL SIGNAL SINE WAVE RECONSTRUCTION



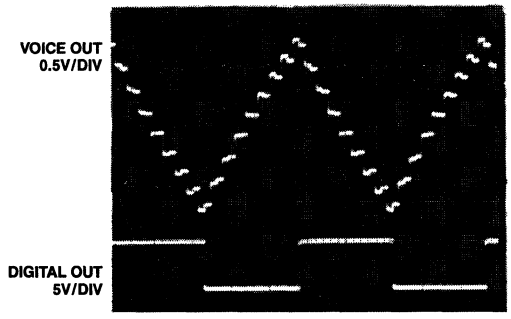
0.5ms/DIV
VOICE IN = 250Hz, $6V_{P-P}$ SINE WAVE
CLOCK = 16kHz

FIGURE 9. CVSD LARGE SIGNAL, LOW FREQUENCY CLIPPED WAVEFORM



50ms/DIV
VOICE IN = 0
CLOCK = 16kHz

FIGURE 10. CVSD ZERO SIGNAL IDLE PATTERN



0.2ms/DIV
VOICE IN = 1kHz, $6V_{P-P}$ SINE WAVE
CLOCK = 16kHz

FIGURE 11. CVSD LARGE SIGNAL, HIGH FREQUENCY SLEW LIMITING

Impedance Matching Design Equations for the HC5509 Series of SLICs

Authors: Don LaFontaine and Ed Berrios

Introduction

The HC5509 Series of SLICs use feedback to synthesize the impedance at the 2-wire tip and ring terminals. The network is capable of synthesizing both resistive and complex impedances. Matching the SLIC's 2-wire impedance to the load is important to maximize power transfer and 2-wire return loss. The 2-wire return loss is a measure of the similarity of the impedance of a transmission line (tip and ring) and the impedance at it's termination. It is a ratio, expressed in decibels, of the power of the outgoing signal to the power of the signal reflected back from an impedance discontinuity.

This application note will discuss the basic DC operation of the tip and ring amplifiers for an understanding of the reaction between the tip and ring amplifiers, the requirements for impedance matching and the derivation of the design equations for calculating the required feedback components for both resistive and complex impedances. The analysis will use the HC5509B as the basis for the discussion. Design solutions for the HC5509A1R3060, HC5524 and HC5517 are provided in Table 1.

Tip and Ring Amplifiers

The tip and ring amplifiers are voltage feedback op amps that are connected to generate a differential output (e.g. if tip sources 20mA then ring sinks 20mA). Figure 1 shows the connection of the tip and ring amplifiers. The tip DC voltage is set by an internal +2V reference, resulting in -4V at the output. The ring DC voltage is set by the tip DC output voltage and an internal $V_{BAT}/2$ reference, resulting in V_{BAT} +4V at the output (see Equations 1, 2 and 3).

$$V_{TIP\ FEED} = V_C = -2V\left(\frac{R}{R/2}\right) = -4V \quad \text{(EQ. 1)}$$

$$V_{RING\ FEED} = V_D = \frac{V_{BAT}}{2}\left(1+\frac{R}{R}\right) - V_{TIP\ FEED}\left(\frac{R}{R}\right) \quad \text{(EQ. 2)}$$

$$V_D = V_{BAT} + 4 \quad \text{(EQ. 3)}$$

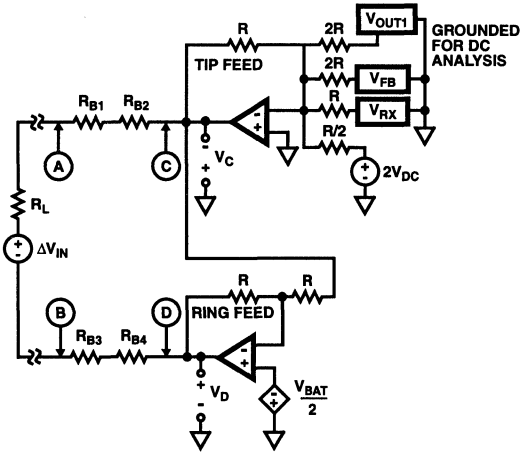


FIGURE 1. OPERATION OF THE TIP AND RING AMPLIFIERS

Requirements for Impedance matching

Impedance matching of the HC5509B application circuit to the transmission line requires that the impedance be matched to points "A" and "B" in Figure 2. To do this, the sense resistors R_{B1}, R_{B2}, R_{B3} and R_{B4} must be accounted for by the feedback network to make it appear as if the output of the tip and ring amplifiers are at points "A" and "B". The feedback network takes a voltage that is equal to the voltage drop across the sense resistors and feeds it into the summing node of the tip amplifier. The effect of this is to cause the tip feed voltages to become more negative by a value that is proportional to the voltage drop across the sense resistors R_{B1} and R_{B2}. At the same time the ring amplifier becomes more positive by the same amount to account for resistors R_{B3} and R_{B4}.

The net effect cancels out the voltage drop across the feed resistors. By nullifying the effects of the feed resistors the feedback circuitry becomes relatively easy to match the impedance at points "A" and "B".

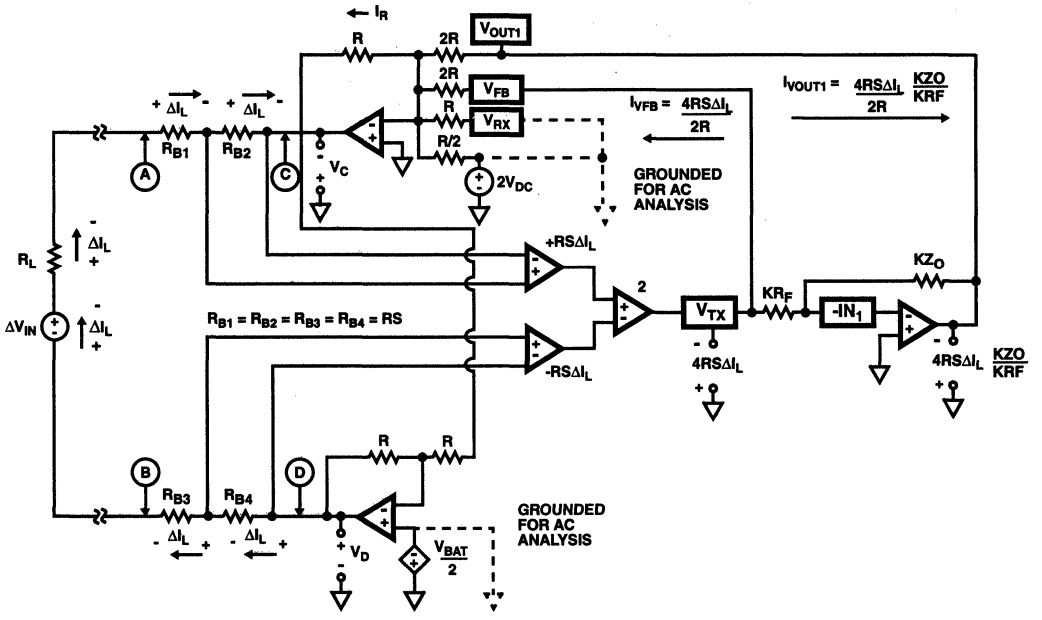


FIGURE 2. FEEDBACK NETWORK FOR IMPEDANCE MATCHING

Impedance Matching Design Equations

Before writing the loop equation to solve for the proper feedback to match the SLICs 2-wire impedance to the load, the AC voltage at V_C and V_D (Figure 2) must first be determined.

The feedback loop senses the loop current through resistors R_{B2} and R_{B4}. For the current direction shown in Figure 2 the VTX output is equal to $+4RS\Delta I_L$. The VTX outputs feedback into the tip current summing node via the VFB pin. The current into VFB is equal to:

$$I_{VFB} = \frac{4RS\Delta I_L}{2R} \quad \text{(EQ. 5)}$$

The VTX voltage is also feed into the -IN input of the SLIC's internal op amp. This signal is amplified by the ratio KZ0/KRF then feed into the tip current summing node via the VOUT1 pin. (Note: the VRX pin and the internal +2V reference are grounded for the AC analysis.) The current into the VOUT1 pin is equal to:

(EQ. 6)

Equation 7 is the node equation for the tip amplifier summing node. The current in the tip feedback resistor (I_R) is given in Equation 8.

$$-I_R + \frac{4RS\Delta I_L}{2R} - \frac{4RS\Delta I_L}{2R}\left(\frac{Z0}{RF}\right) = 0 \quad \text{(EQ. 7)}$$

$$I_R = \frac{4RS\Delta I_L}{2R} - \frac{4RS\Delta I_L}{2R}\left(\frac{Z0}{RF}\right) \quad \text{(EQ. 8)}$$

The voltage V_C is then equal to:

$$V_C = (I_R)(R) \quad \text{(EQ. 9)}$$

$$V_C = -2RS\Delta I_L\left(1 - \frac{Z0}{RF}\right) \quad \text{(EQ. 10)}$$

and the AC voltage at V_D is:

$$V_D = 2RS\Delta I_L\left(1 - \frac{Z0}{RF}\right) \quad \text{(EQ. 11)}$$

(Note $V_{BAT}/2$ is grounded for AC analysis)

Having the voltages at V_C and V_D, as a function of the feedback network, the loop equation to match the impedance of any load is as follows:

$$-2RS\Delta I_L\left(1 - \frac{Z0}{RF}\right) + 2RS\Delta I_L - \Delta V_{IN} +$$

(EQ. 12)

$$\Delta V_{IN} = -4RS\Delta I_L\left(1 - \frac{Z0}{RF}\right) + 4RS\Delta I_L + RL\Delta I_L \quad \text{(EQ. 13)}$$

$$\Delta V_{IN} = \Delta I_L\left[-4RS\left(1 - \frac{Z0}{RF}\right) + 4RS + R_L\right] \quad \text{(EQ. 14)}$$

$$\frac{\Delta V_{IN}}{\Delta I_L} = 4RS\left(\frac{Z0}{RF}\right) + R_L \qquad \frac{\Delta V_{IN}}{\Delta I_L} = 4RS\frac{Z0}{RF} + R_L \quad \text{(EQ. 15)}$$

Equation 14 can be separated into two terms, the feedback term (-4RS(1 - ZO/RF) and the loop impedance term (+4RS + R_L). The +4RS term of the loop impedance is can-

celled by the -4RS term of the feedback. The result is shown in Equation 15. Figure 3 is a schematic representation of Equation 15.

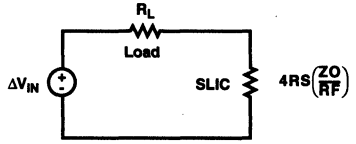


FIGURE 3. SCHEMATIC REPRESENTATION OF EQUATION 15

To match the impedance of the SLIC to the impedance of the load set

$$R_L = 4RS\left(\frac{ZO}{RF}\right) \quad \text{(EQ. 16)}$$

If RF is made to equal 4RS then:

$$R_L = ZO \quad \text{(EQ. 17)}$$

Therefore to match the HC5509B, with RS equal to 50Ω, to a 600 Ω load:

$$RF = 4RS = 4(50\Omega) = 200\Omega \quad \text{(EQ. 18)}$$

and

$$R_L = ZO = 600\Omega \quad \text{(EQ. 19)}$$

To prevent loading down the VTX output, the value of RF and ZO are typically scaled by a factor of K = 100, therefore:

$$KRF = 20k\Omega \qquad KZO = 60K\Omega \quad \text{(EQ. 20)}$$

Since the impedance matching is a function of the voltage gain, scaling of the resistors to achieve a standard value is recommended.

For complex impedances the above analysis is the same.

$$KRF = 20k\Omega \qquad KZO = 100(\text{Resistive}) + \frac{\text{Reactive}}{100} \quad \text{(EQ. 21)}$$

Table 1 list the values of KRF, KZO for several worldwide Typical line impedances. The analysis for the HC5509A1R3060, HC5524 and the HC5517 are similar to that of the HC5509B. The only exception is the HC5517 in that the VFB feedback path is not connected. Other than that the analysis are identical.

NOTE: When matching a complex impedance some impedance models (900 + 2.15µF, K = 100) will cause the op amp feedback to be open at DC currents, bring the op amp to an output rail. A resistor with a value of about 10 times the reactance of the capacitor (21.6nF) at the low frequency of interest (200Hz for example) can be placed in parallel with the capacitor in order to solve the problem (368kΩ for a 21.6nF capacitor).

TABLE 1.

LOAD IMPEDANCE	KRF	KZO	OPTIONAL PARALLEL RESISTOR
HC5509B1: VFB CONNECTED			
600Ω	20kΩ	60kΩ	NA
900Ω	20kΩ	90kΩ	NA
600Ω + 2.2µF	20kΩ	60kΩ + 22nF	360kΩ
725Ω + 2.2µF	20kΩ	72.5kΩ + 22nF	360kΩ
900Ω + 2.2µF	20kΩ	90kΩ + 22nF	360kΩ

TABLE 1. (Continued)

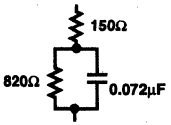
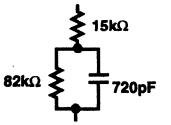
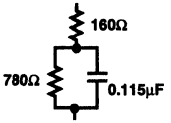
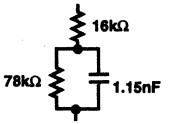
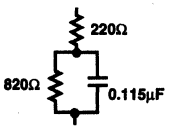
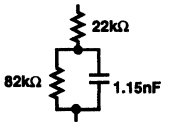
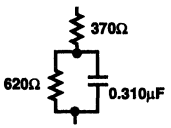
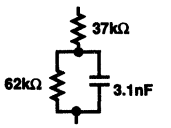
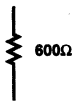
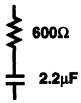
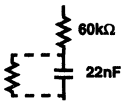
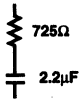
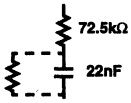
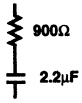
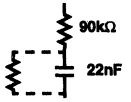
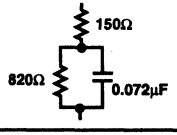
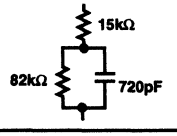
LOAD IMPEDANCE	KRF	KZO	OPTIONAL PARALLEL RESISTOR
			NA
			NA
			NA
			NA
HC55509A1R3060: VFB CONNECTED			
			NA
			NA
			360kΩ
			360kΩ
			360kΩ
			NA

TABLE 1. (Continued)

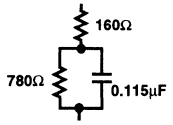
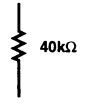
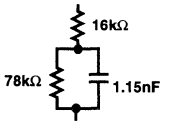
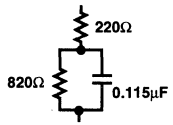
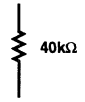
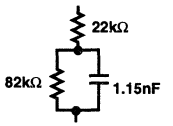
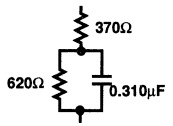
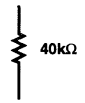
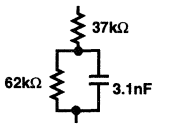
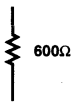
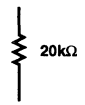
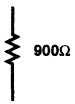
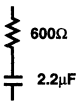
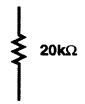
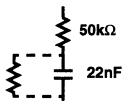
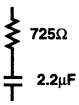
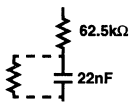
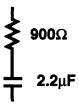
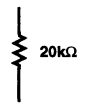
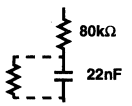
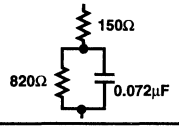
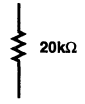
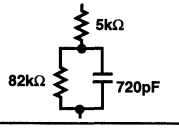
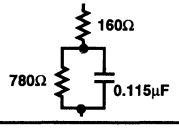
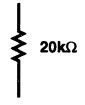
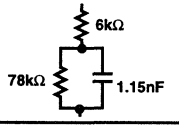
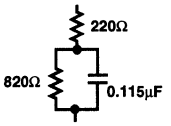
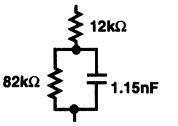
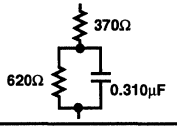
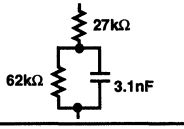
LOAD IMPEDANCE	KRF	KZO	OPTIONAL PARALLEL RESISTOR
			NA
			NA
			NA
HC5524: VFB CONNECTED. Single feed resistor for tip and one for ring.			
			NA
			NA
			360kΩ
			360kΩ
			360kΩ
			NA
			NA

TABLE 1. (Continued)

LOAD IMPEDANCE	KRF	KZO	OPTIONAL PARALLEL RESISTOR
			NA
			NA
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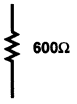
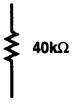
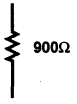
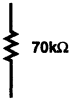
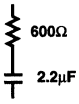
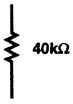
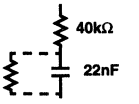
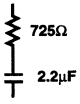
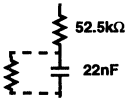
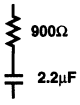
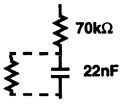
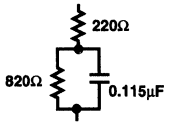
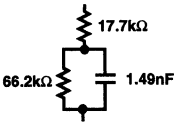
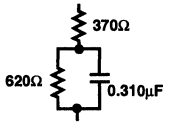
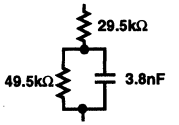
			NA
			NA
			360kΩ
			360kΩ
			360kΩ
			NA
			NA

Harris Semiconductor

APPNOTE

No. AN9608 July 1996

Harris Telecom

Implementing Pulse Metering for the HC5509 Series of SLICs

Authors: Ed Berrios and Don LaFontaine

Introduction

Pulse metering or Teletax is used outside the United States for billing purposes at pay phones. A 12kHz or 16kHz burst (see Figure 1) is injected into the 4-wire side of the SLIC and transmitted across the tip and ring lines from the central office to the pay phone. The burst updates a counter that indicates the cost of the call to the user. The repetition rate of the burst is dependent upon the billing rates for the specific time of the day and the distance of the call.

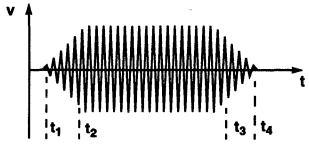


FIGURE 1. PULSE METERING SIGNAL ENVELOPE

The waveform in Figure 1 represents the pulse metering signal burst. The rise and fall times of the waveform are specified to minimize emissions of the burst. Table 1 lists the electrical specifications of the waveform.

TABLE 1. PULSE METERING ELECTRICAL PARAMETERS

PARAMETER	VALUE	NOTE	LIMITS
Frequency	12kHz or 16kHz	Selectable	±50Hz
Level	$1V_{RMS}$	200Ω load	±10%
2nd, 3rd Harmonics	<200mV	200Ω load	-
2-Wire Impedance	200Ω	12kHz or 16kHz	±40Ω
Rise (t_r) and fall (t_f) times	10ms or 20ms	$t_r = t_2 - t_1$ $t_f = t_4 - t_3$	±10%

This Application Note discusses the technique for injecting a pulse metering signal into the 4-wire side of the SLIC for transmission on the 2-wire side. The complete implementation includes a circuit for injecting the AC pulse metering signal, a circuit for offsetting the tip and ring DC voltages and a circuit for the transhybrid balance of the pulse metering return signal. The tip and ring DC voltages must be offset by the peak value of the pulse metering signal to allow simultaneous transmission of voice and pulse metering. A brief discussion of impedance matching will lead into the detailed pulse metering discussion. For a detailed discussion, refer to AN9607, "Impedance Matching Design Evaluation for the HC5509 Series of SLIC", AnswerFAX Document No. 99607.

SLIC Impedance Matching

Impedance matching is used to set the 4-wire to 2-wire gain of the SLIC for a specified termination impedance across tip and ring. The termination may vary from purely resistive (typ 600Ω) to complex (resistive plus capacitive).

The impedance matching is synthesized by feeding back a voltage that is proportional to the 2-wire loop current. This voltage is then scaled and injected into the summing node of the tip feed amplifier. The feedback compensates for the voltage drop across the tip and ring sense resistors (R_S), which results in the impedance of the SLIC matching the load (R_L).

Figure 2 shows the network used to derive the impedance matching equations. The loop equation from tip to ring is written as follows:

$$V_C + 2R_S\Delta I_L - \Delta V_{IN} + R_L\Delta I_L + 2R_S\Delta I_L - V_D = 0 \quad \text{(EQ. 1)}$$

where

$$V_C = -V_D = -2R_S\Delta I_L\left(1 - \frac{Z_O}{R_F}\right) \quad \text{(EQ. 2)}$$

Solving for $\Delta V_{IN}/\Delta I_L$ results in Equation 3.

$$\frac{\Delta V_{IN}}{\Delta I_L} = 4R_S\left(\frac{Z_O}{R_F}\right) + R_L \quad \text{(EQ. 3)}$$

By setting R_F equal to $4R_S$ then:

$$R_L = Z_O \quad \text{(EQ. 4)}$$

Therefore, to match the impedance of the SLIC, with R_S equal to 50Ω, to a 600Ω load:

$$R_F = 4R_S = 4(50\Omega) = 200\Omega \quad \text{(EQ. 5)}$$

and

$$R_L = Z_O = 600\Omega \quad \text{(EQ. 6)}$$

To prevent loading of the V_{TX} output, the value of R_F and Z_O are typically scaled up by a factor of 100:

$$KR_F = 20k\Omega \qquad KZ_O = 60k\Omega \quad \text{(EQ. 7)}$$

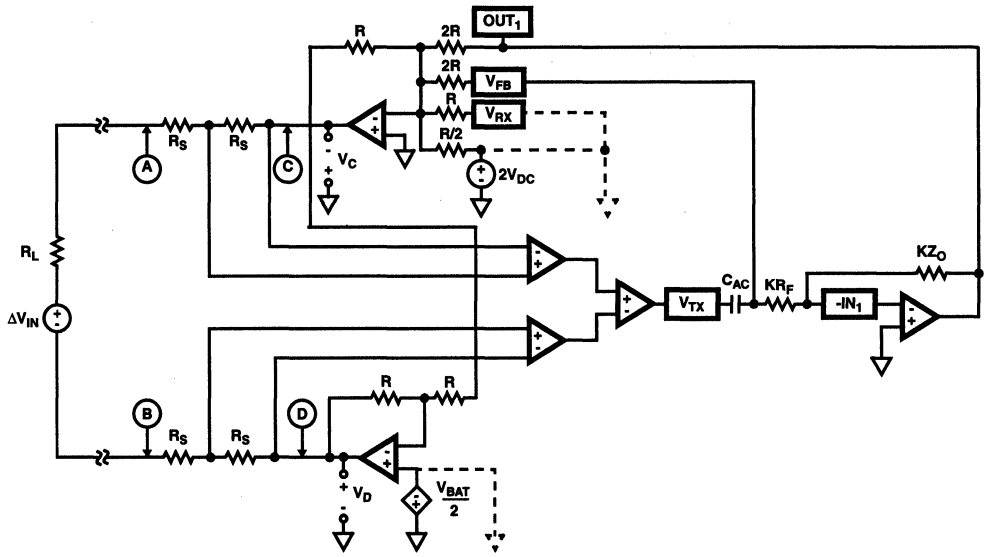


FIGURE 2. FEEDBACK NETWORK FOR IMPEDANCE MATCHING

Injecting The Pulse Metering Signal

Two circuits must be designed for injection of the pulse metering signal. One circuit is used to sum the pulse metering signal and the incoming voice signal on the 4-wire side and the other is used to offset both tip and ring by the peak amplitude of the pulse metering signal.

Summing Amplifier Design

The pulse metering signal is injected in the $-IN_1$ pin of the SLIC. This pin is the inverting input of the internal amplifier (A1) that is used to implement impedance matching.

The components required for pulse metering are C_{PM} and R_{PM}, are shown in Figure 3. The pulse metering signal is AC coupled to prevent a DC offset on the input of the internal amplifier. The value of C_{PM} should be 10μF. The value of R_{PM} is calculated from Equations 9 and 10.

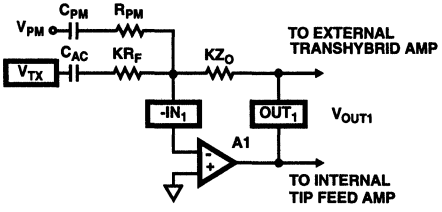


FIGURE 3. PULSE METERING SUMMING AMPLIFIER DESIGN

$$V_{OUT1} = -V_{TX} \bullet \frac{KZ_O}{K_{RF}} - V_{PM} \bullet \frac{KZ_O}{R_{PM}} \quad \text{(EQ. 8)}$$

The first term of Equation 8 is the gain of the feedback voltage from the 2-wire side and the second term is the gain of the injected pulse metering signal. The effects of C_{AC} and C_{PM} are negligible and therefore omitted from the analysis.

The injected pulse metering output term of Figure 3 is shown below in Equation 9 and rearranged to solve for R_{PM} in Equation 10.

$$V_{OUT1}(\text{injected}) = V_{PM} \bullet \frac{KZ_O}{R_{PM}} = 2 \quad \text{(EQ. 9)}$$

$$R_{PM} = \frac{KZ_O}{2} \quad \text{(EQ. 10)}$$

The ratio of KZ_O to R_{PM} is set to 2 to compensate for the gain of 0.5 at the tip feed amplifier. This results in unity gain of the pulse metering signal from 4-wire side to 2-wire side. The value of KZ_O is considered to be a constant since it is selected based on impedance matching requirements.

When complex impedance matching is implemented, match the R_{PM} circuit to the KZ_O circuit, keeping in mind the required gain of 2.

Additional Tip and Ring Offset Voltage

A DC offset is required to level shift tip and ring from ground and V_{BAT} respectively. By design, the tip amplifier is offset 4V below ground and the ring amplifier is offset 4V above V_{BAT}. The 4V offset was designed so that the peak voice signal could pass through the SLIC without distortion. Therefore, to maintain distortion free transmission of pulse metering and voice, an additional offset equal to the peak of the pulse metering signal is required.

The tip and ring voltages are offset by a voltage divider network on the V_{RX} pin. The V_{RX} pin is a unity gain input designed as the 4-wire side voice input for the SLIC. Figure 4 details the circuit used to generate the additional offset voltage.

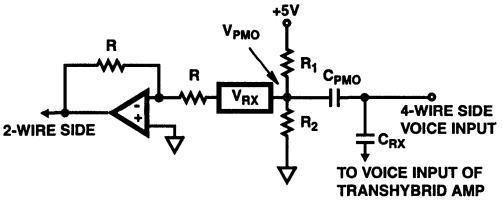


FIGURE 4. PULSE METERING OFFSET GENERATION

The amplifier shown is the tip amplifier. Other signals are connected to the summing node of the amplifier but only those components used for the offset generation are shown. The offset generated at the output of the tip amplifier is summed at the ring amplifier inverting input to provide a positive offset from the battery voltage. The connection to the ring amplifier was omitted from Figure 4 for clarity, refer to Figure 2 for details. The typical component values for Figure 4 are listed in Table 2.

TABLE 2. TYPICAL COMPONENT VALUES FOR FIGURE 4

REF DES	VALUE	REF DES	VALUE
C_{RX}	10µF	R	108kΩ
C_{PMO}	10µF	R_1	23.2kΩ
		R_2	10kΩ

The term V_{PMO} is defined to be the offset required for the pulse metering signal. The value of the offset voltage is calculated as the peak value of the pulse metering signal. Equation 11 assumes the amplitude of the pulse metering signal is expressed as an rms voltage.

$$V_{PMO} = \sqrt{2} \bullet V_{PM} \qquad \text{(EQ. 11)}$$

The value of R_1 can be calculated from the following equation:

$$R_1 = \left(\frac{R_2 R}{R_2 + R}\right)\left(\frac{5 - V_{PMO}}{V_{PMO}}\right) \qquad \text{(EQ. 12)}$$

The component labeled R is the internal summing resistor of the tip amplifier and has a typical value of 108kΩ. The value of R_2 should be selected in the range of 4.99kΩ and 10kΩ. Staying within these limits will minimize the parallel loading effects of the internal resistor R on R_2 as well as minimize the constant power dissipation introduced by the divider.

Solving equation 11 for $1V_{RMS}$ results in a 1.414V requirement for V_{PMO}. Setting R_2 of Equation 12 to 10kΩ and substituting the values for V_{PMO} and R yields 23.2kΩ for R_1. The value of R_1 can be rounded to the nearest standard value without significantly changing the offset voltage.

Voice Path Considerations

The presence of the offset circuitry in the voice path alters the input impedance seen by the voice signal. The input impedance for the standard application is equal to the value of R (108kΩ) in Figure 4. The additional offset circuitry lowers the impedance to approximately 5kΩ which maintains a relatively high impedance for the voice driver.

The configuration used also results in a high pass RC network as shown in Figure 5.

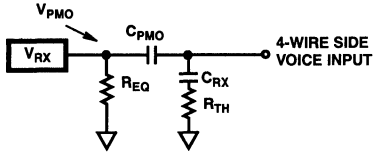


FIGURE 5. HIGH PASS NETWORK FORMED AT V_{RX} NODE

The impact of the resultant high pass network is negligible in the voice band, 200Hz to 3400Hz. The value of the input impedance varies slightly over the voice band, 5.3kΩ at 200Hz versus 5.2kΩ at 3400Hz. Replacing both capacitors with a short circuit (f = ∞), the steady state value obtained is 5.19kΩ. The relatively constant input impedance implies the high pass corner frequency is well below the band of interest.

Loop Length Considerations

The additional offset required for pulse metering reduces the maximum loop resistance driven by the SLIC. For a loop current (I_L) of 25mA and battery voltage of -48V, the maximum loop resistance is equal to:

$$R_{L_{MAX}} = \frac{V_{TR}}{I_L} = \frac{(-4 + 48)}{0.025} = 1.6k\Omega \qquad \text{(EQ. 13)}$$

For a pulse metering level (V_{PM}) of $1V_{RMS}$ and the same conditions as above the maximum loop resistance is:

$$R_{L_{MAX}} = \frac{V_{TR} - 2V_{PMO}}{I_L} = \frac{(-4 + 48 - 2(1.414))}{0.025} = 1.48k\Omega \qquad \text{(EQ. 14)}$$

The loop resistance terms in Equations 13 and 14 include the 200Ω contribution of the SLIC's sense resistors. Therefore, actual loop resistance is 200Ω less than the calculated values in the above example.

Cancellation of the Pulse Metering Signal

There are many techniques available for cancelling the return pulse metering signal. The techniques range from filtering of the return signal to transhybrid cancellation. The selected approach varies from application to application and is dependent on the impedance characteristics of the line. The discussion to follow will address the transhybrid technique of cancellation shown in Figure 6.

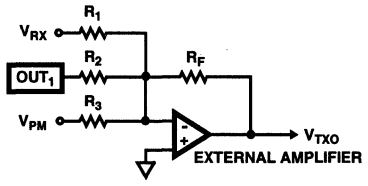


FIGURE 6. CANCELLATION OF THE PULSE METERING SIGNAL

The transhybrid cancellation technique that is used for the voice signal is also implemented for pulse metering. The technique is to drive the transhybrid amplifier with the signal that is injected on the 4-wire side, then adjust its level to match the amplitude of the feedback signal, and cancel the signals at the summing node of an amplifier.

NOTE: The external operational amplifier is used in the application as a "stand in" for the operational amplifier that is traditionally located in the CODEC, where transhybrid cancellation is performed.

Referring to Figure 2, V_{TX} is the feedback signal used to drive the internal amplifier (A1) that drives the OUT_1 pin of the SLIC. The voltage measured at V_{TX} is related to the loop impedance as follows:

$$V_{TX} = \frac{-200}{R_L} \bullet V_{PM} \bullet G_{PM} \qquad \text{(EQ. 15)}$$

For a 600Ω termination and a pulse metering gain (G_{PM}) of 1, the feedback voltage (V_{TX}) is equal to one third the pulse metering signal on the 4-wire side. Note, depending upon the line impedance characteristics and the degree of impedance matching, the pulse metering gain may differ from the voice gain. The pulse metering gain (G_{PM}) must be accounted for in the transhybrid balance circuit.

The following equation is used to calculate the output voltage of the internal amplifier (A1) at OUT_1:

$$OUT_1 = -\left(\frac{K_{ZO}}{KR_F}\right) \bullet V_{TX} + \left(-\frac{K_{ZO}}{R_{PM}}\right) \bullet V_{PM} \qquad \text{(EQ. 16)}$$

The first term of the equation is the gain of the feedback signal through the internal amplifier. The second term is the gain of the injected pulse metering signal discussed in the Summing Amplifier Design section of this Application Note. The polarity of the signal at OUT_1 is opposite of V_{PM} allowing the circuit of Figure 6 to perform the final stage of transhybrid cancellation.

The following equations do not require much discussion. They are based on inverting amplifier design theory. The voice path V_{RX} signal has been omitted for clarity. All reference designators refer to components of Figures 3 and 6.

$$V_{TXO} = -KZ_O \bullet \left(-\frac{V_{TX}}{KR_F} - \frac{V_{PM}}{R_{PM}}\right) \bullet \frac{R_F}{R_2} - \left(V_{PM} \bullet \frac{R_F}{R_3}\right) \qquad \text{(EQ. 17)}$$

The first term refers to the signal at OUT_1 and the second term refers to the 4-wire side pulse metering signal used to complete the transhybrid cancellation. Since ideal transhybrid cancellation implies V_{TXO} equals zero when a signal is injected on the 4-wire side, V_{TXO} is set to zero and the resulting equation is shown below.

$$0 = KZ_O \bullet \left(\frac{V_{TX}}{KR_F} + \frac{V_{PM}}{R_{PM}}\right) \bullet \frac{R_F}{R_2} - \left(V_{PM} \bullet \frac{R_F}{R_3}\right) \qquad \text{(EQ. 18)}$$

Rearranging terms of Equation 18 and solving for R_3 results in Equation 19. This is the only value to be calculated for the transhybrid cancellation. All other values either exist in the application circuit or have been calculated in previous sections of this Application Note.

$$R_3 = \left(\frac{KZ_O}{R_2} \bullet \left(\frac{-200 \bullet G_{PM}}{R_L \bullet KR_F} + \frac{1}{R_{PM}}\right)\right)^{-1} \qquad \text{(EQ. 19)}$$

The value of R_3 (Figure 6) is 8.25kΩ given the following set of values:

KZ_O = 60kΩ, KR_F = 20kΩ, R_L = 600Ω, R_2 = 8.25kΩ, R_{PM} = 30kΩ, G_{PM} = 1

Substituting the same values into Equations 15 and 16, it can be shown that the signal at OUT_1 is equal to $-V_{PM}$. This result, along with Equation 18 where R_2 equals to R_3, indicates the signal levels into the transhybrid amplifier are equal in magnitude but opposite in phase, thereby achieving transhybrid balance at V_{TXO}.

Harris Semiconductor

APPNOTE

No. AN9628 July 1996

Harris Telecom

AC Voltage Gain for the HC5509 Series of SLICs

Authors: Don LaFontaine Ed Berrios

Introduction

The HC5509 Series of SLICs use feedback to synthesize the impedance at the 2-wire tip and ring terminals. This feed back network determines the AC voltage gains for the SLIC.

This application note will discuss the basic AC operation of SLIC. The DC operation and the requirements for impedance matching are discussed in application note AN9607 "Impedance Matching Design Equations for the HC5509 Series of SLICs" and is recommended reading as accompaniment to this application note.

The analysis will use the HC5509B as the basis for the discussion. The same analysis is applicable to the HC5509A1R3060, HC5524 and the HC5517.

AC Voltage Gain Design Equations

The 4-wire to 2-wire voltage gain (V_{RX} to V_{TR}) is set by the feedback loop shown in Figure 1. The First Feedback Loop senses the loop current through resistors R_{13} and R_{14}, sums their voltage drop and gains it up by 2 to produce an output voltage at the V_{TX} pin equal to $+4R_S\Delta IL$. This voltage is then fed back into the tip current summing node via the V_{FB} pin. The current into V_{FB} is equal to:

$$I_{VFB} = \frac{4R_S\Delta I_L}{2R} \quad \text{(EQ. 1)}$$

The V_{TX} voltage is also fed into the -IN input of the SLIC's internal op-amp (Feedback). This signal is gained up by KZ_0/KR_F then fed into the tip current summing node via the OUT1 pin. (Note: the V_{RX} pin and the internal +2V reference are grounded for the AC analysis.) The current into the OUT1 pin is equal to:

$$I_{OUT1} = -\frac{4R_S\Delta I_L}{2R}\left(\frac{Z_0}{R_F}\right) \quad \text{(EQ. 2)}$$

Equation 3 is the node equation for the tip amplifier summing node. The current in the tip feedback resistor (I_R) is given in Equation 4.

$$-I_R + \frac{4R_S\Delta I_L}{2R} - \frac{4R_S\Delta I_L}{2R}\left(\frac{Z_0}{R_F}\right) + \frac{V_{RX}}{R} = 0 \quad \text{(EQ. 3)}$$

$$I_R = \frac{4R_S\Delta I_L}{2R} - \frac{4R_S\Delta I_L}{2R}\left(\frac{Z_0}{R_F}\right) + \frac{V_{RX}}{R} \quad \text{(EQ. 4)}$$

The voltage V_C is then equal to:

$$V_C = (I_R)(R) \quad \text{(EQ. 5)}$$

$$V_C = 2R_S\Delta I_L\left(1 - \frac{Z_0}{R_F}\right) + V_{RX} \quad \text{(EQ. 6)}$$

and the AC voltage at V_D is:

$$V_D = -2R_S\Delta I_L\left(1 - \frac{Z_0}{R_F}\right) + V_{RX} \quad \text{(EQ. 7)}$$

NOTE: $V_{BAT}/2$ is grounded for AC analysis.

The values for Z_0 and R_F are selected to match the impedance requirements on tip and ring, for more information reference AN9607. The following loop current calculations will assume the proper Z_0 and R_F values for matching a 600Ω load (reference Table 1).

TABLE 1. FEEDBACK RESISTORS FOR MATCHING A 600Ω LOAD

PART	R_F	Z_0
HC5509B	20kΩ	60kΩ
HC5509A1R3060	20kΩ	30kΩ
HC5524	20kΩ	50kΩ
HC5517	40kΩ	40kΩ

The loop current (ΔI_L, Figure 1) with respect to the feedback network, is calculated in equations 8 through 11. Where Z_0 = 60kΩ, R_F = 20kΩ, R_L = 600Ω, $R_{11} = R_{12} = R_{13} = R_{14}$ = 50Ω.

$$\Delta I_L = \frac{V_C - V_D}{R_L + R_{11} + R_{12} + R_{13} + R_{14}} \quad \text{(EQ. 8)}$$

$$\Delta I_L = \frac{2 \times \left(2R_S\Delta I_L\left(1 - \frac{Z_0}{R_F}\right) + V_{RX}\right)}{R_L + R_{11} + R_{12} + R_{13} + R_{14}} \quad \text{(EQ. 9)}$$

$$\Delta I_L = \frac{2V_{RX} - 400\Delta I_L}{800} \quad \text{(EQ. 10)}$$

$$\Delta I_L = \frac{V_{RX}}{600} \quad \text{(EQ. 11)}$$

Equation 11 is the loop current with respect to the feedback network. From this, the 4-wire to 2-wire and the 2-wire to 4-wire AC voltage gains can be calculated. Equation 12 shows the 4-wire to 2-wire AC voltage gain is equal to one. Equation 13 shows the 2-wire to 4-wire AC voltage gain is also equal to one.

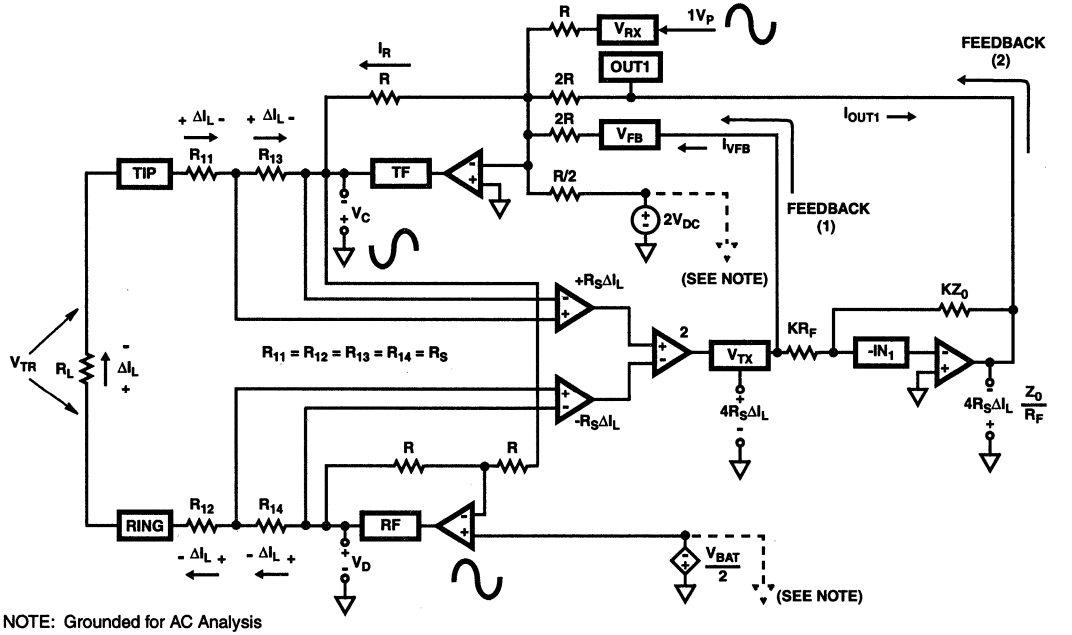
$$A_{4w-2w} = \frac{V_{TR}}{V_{RX}} = \frac{\Delta I_L(R_L)}{V_{RX}} = \frac{\frac{V_{RX}}{600}(600)}{V_{RX}} = 1 \quad \text{(EQ. 12)}$$

$$A_{2w-4w} = \frac{V_{OUT1}}{V_{TR}} = \frac{4R_S\Delta I_L\left(\frac{Z_0}{R_F}\right)}{\Delta I_L(R_L)} = \frac{200\frac{V_{RX}}{600}(3)}{\frac{V_{RX}}{600}(600)} = 1 \quad \text{(EQ. 13)}$$

Table 2 lists the AC voltage gains for the HC5509 family of SLICs:

TABLE 2. AC VOLTAGE GAINS

PART	AC GAIN 4-WIRE TO 2-WIRE	AC GAIN 2-WIRE TO 4-WIRE
HC5509B	1	1
HC5509A1R3060	1	1/3
HC5524	1	1
HC5517	1	1/3



NOTE: Grounded for AC Analysis

FIGURE 1. AC VOLTAGE GAIN AND IMPEDANCE MATCHING

Harris Semiconductor

APPNOTE

No. AN9636.1 January 1997

Harris Telecom

Implementing an Analog Port for ISDN Using the HC5517

Authors: Dave Feller, Don LaFontaine

Introduction

With the need for faster and faster data communications for the home and office, more and more people are turning to the ISDN (Integrated Services Digital Network) line as a solution. The standard data modem that operates over a twisted pair telephone line has been traditionally limited to 28,800 B/s. Compression algorithms and special modulation techniques have pushed the data rate to the extremes. The limited bandwidth of the twisted pair and standard central office SLICs and CODEC's puts an upper limit on the possible data rates. The industry has just about reached that limit. There are quite a few options available to increase the data rates to the outside world including ADSL/VDSL modems, bringing a T1 connection straight to the computer (1.544 Mb/s - typical for video teleconferencing setups), and even fiber optic cabling. However, most of these options are very expensive or are not yet available in all areas of the country. ISDN provides an affordable, available, supported solution to the need for higher data rates.

This application note includes a brief discussion of ISDN and ISDN signaling, the use of the HC5517 as an interface between the analog subscriber side and the digital ISDN line, and provides a detailed description of the hardware interface. A good understanding of the hardware is necessary to understand ISDN protocol so that software can be written to properly control the SLIC and translate analog queues into ISDN signal commands. The discussion of the hardware will include the SLIC, the power supply, all appropriate signaling circuitry, glue circuitry to a standard analog interface, and battery backup recommendations.

Implementing ISDN in the Home or Office

ISDN is an entirely digital system, it is not backwards compatible with any of the analog equipment on the market today (telephones, fax machines, modems, answering machines, etc.). To allow backwards compatibility, a method is needed to allow an analog device to be plugged into the ISDN line. That need has pushed the creation of the HC5517 ringing SLIC. The concept is actually simple: move the standard SLIC (Subscriber Line Interface Circuit) and CODEC that normally controls a telephone from the central office to the home.

Having the SLIC/CODEC local presents a new set of challenges for the designer. The standard telephone commands and signaling techniques must now be taken care of locally, and perhaps more importantly the ring signal must be generated locally. The HC5517 SLIC allows the ring signal to be routed and driven through the SLIC instead of using relays and high power high voltage generators to ring the phone. The functions of an At The Home SLIC (ATH SLIC) will be discussed shortly, but suffice it to say that the HC5517 will make the ringing function easier and cheaper than conventional methods.

ISDN Basics

Data Rates and Services

It is important to note that an ISDN line in any form is a true digital interface to the service provider, and all the data rates discussed below are true digital rates and not analog modulated digital information.

ISDN service comes in two forms: Basic Rate Interface (BRI), and Primary Rate Interface (PRI). BRI is the typical ISDN line purchased by individuals and most small businesses. It consists of a total possible data rate of 128KB/s with a 16KB/s data channel added for signaling and control. The 128K total throughput can be broken down into two distinct digital channels of 64KB/s each called Bearer (B) channels. The 16KB signaling and control channel is referred to as the D channel. Therefore, the BRI is commonly referred to as 2B + D indicating two 64K channels for data and one 16KB data channel for signaling. Each B channel is independent and two separate calls can be made at the same time by making use of both B channels, or they can be synchronously combined in software with the proper protocol to provide a total of 128K to a single destination. The PRI is simply a large grouping of B channels that can be purchased at great expense for very high speed communications. This interface is usually only purchased by larger corporations or service providers but is included here for completeness. The total bandwidth of the PRI is based on the predominant carrier trunk in the area, so in the US the total bandwidth is 1.544MB/s (T1) and in Europe it is 2.048MB/s (E1). The 1.544MB/s is broken down into 24 individual 64KB lines one of which is reserved for signaling much like the 2B + D line. Therefore the PRI in the USA is commonly referred to as a 23B + D connection.

The basic 64KB/s data rate is derived from the present analog system. The typical bandwidth of standard analog tele-

phone connection is very nearly 3,500Hz or 4,000Hz if rounded up to the nearest thousand. Nyquist tells us that we must over sample by two to get an accurate reproduction of the digitized waveform; that brings us to 8K. If we take 8 bits of data for each sample that indicates that the primary bandwidth needed for a standard analog connection is 64KB/s. It is therefore logical that the standards should use this rate since the equipment already in place must be utilized. So each B channel assigned is treated like any other digitized analog connection once it reaches the switch (more or less).

Interface Breakdown

With a 2B + D entering the home, the next major goal is to connect an analog device to it via some interface box. The interface solution can vary depending on what kind of device is being plugged in as well as where it is located (see Figure 1). The two wire connection that the service provider installs is generally referred to as the U interface. It is transformer coupled and generally converted to a four wire S interface that can be distributed within a reasonable distance within an office. The U interface is a standard RJ11 jack and the S interface is usually an RJ45 jack like a standard Ethernet connection. Unlike an analog telephone, only one device can be plugged into a U interface at a time. This is the primary reason for converting to an S interface; up to 8 devices can be plugged into an S interface and each can have its own unique address. An obvious conflict arises if three different S interface devices each request a B channel and the U interface is a standard 2B + D connection; one of them simply has to wait. The S interface is extremely useful if the number of users is small and the individual usage times are short, or if there are a number of different devices that are to be plugged in. The device that converts from U to S is called a Network Termination (NT-1) and can either be a stand alone device or it can be built into a LAN card. The final interface is generally a high speed serial port like RS232. A device can be purchased to convert from U or S to RS232 and is referred to as a Terminal Adapter (TA). TAs can also be purchased as stand alone or integrated units. These are primarily useful if all IRQs or ISA/PCI slots are used up, or if the desired device needs to be backwards compatible with standard Hayes modem commands and normal communications software.

The NT-1

This primary conversion point is an ideal spot for an analog port for a standard telephone connection. This provides a main port access to standard communications systems for system check and ease of initial setup. If any part of the system is working it is likely to be the U interface since it is the direct line to the service provider. An analog port here with a simple battery backup is also necessary for emergency communications in the event of a power failure. The closer to the U interface the more likely a connection can be established. The HC5517 ringing SLIC described below makes the analog port interface a simple task.

The ISDN Modem Card (NT-1 Included)

Since the U interface is the primary connection to the home, most ISDN modems available on the commercial market will most likely include an NT-1 on board so that there is no accessible S interface. This is primarily because the vast majority of users will only need one connection per site. A card that plugs directly into the U interface and provides conversion to ISA or PCI is the most likely place to have an analog port or two. An analog port provides the user with the ability to utilize standard telephones as well as fax machines, answering machines, modems, and even caller ID services.

The S-BUS ISDN Modem Card

The S interface LAN card while functionally similar to the standard ISDN modem card does not include an on board NT-1. The typical S interface card plugs into an external NT-1 via an RJ45 connector and is typically located within a few hundred feet of that NT-1. These modems are primarily used in small businesses and multiple computer sites that all require periodic ISDN access. The inclusion of analog ports in these cards is identical to that of the standard ISDN modem.

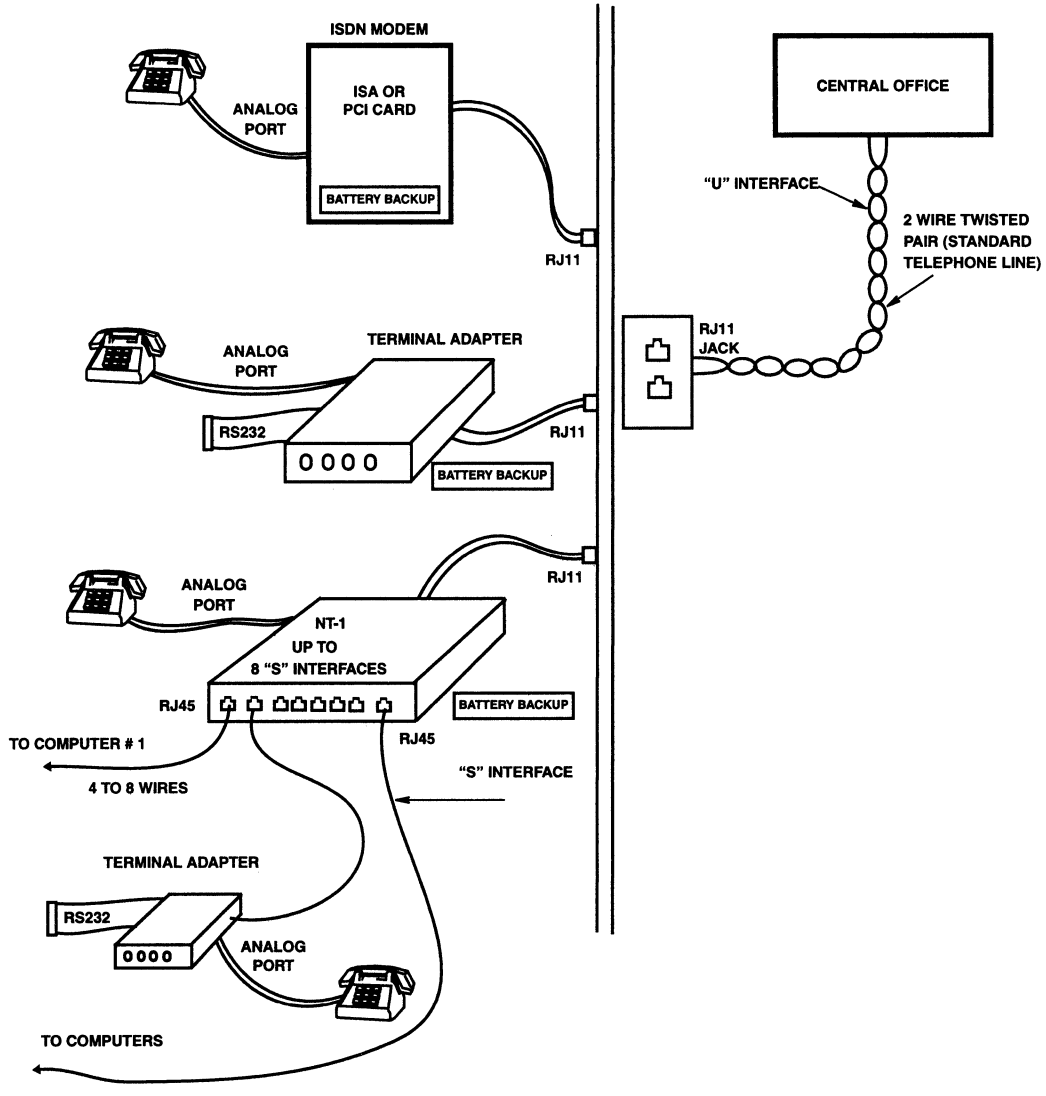
Basic Signaling

For purposes of this discussion, it will be assumed from here on that we are talking about an analog port that is to be installed into a standard ISDN modem that plugs directly into a PCI or ISA slot. A separate IC vendor will provide the necessary devices to get from a U interface to a four wire analog interface.

If we make the basic assumption that the hardware is in place, then we can focus on analog port control software. The software driving the modem that runs on the host PC must convert the ISDN commands into the proper signals needed by the HC5517 SLIC. The basic interface signals include audio in, audio out, ring generation, switch hook detection, ring trip detection and power supply control. With the exception of the audio signals, these can be any set of I/O pins controllable and readable by the host processor. These hardware connections are shown in detail in the hardware section, but first the steps needed for connection will be discussed.

Call Setup Protocol

The process of making a call on ISDN is roughly similar to the progression of a standard telephone call. For the purposes of this discussion, an ISDN call will refer to the process of establishing a link to another computer over an ISDN line and is not necessarily analog port to analog port. The actual service desired (voice, 3.1KB analog, or pure data) that is to be transmitted on the B channel can either be established during call setup or after call connection as a function of normal B channel communications. This setup of the channel is referred to as out-of-band if done during setup and in-band if done after the B channel is connected. Out-of-band is most common for telephony connections via the analog port, and In-band setup is most common for data and 3.1kHz analog (analog modem use). Since a telephone connection normally takes place during call setup, that is the most logical situation to discuss. The following connection process would also take place in the same basic order for the in-band condition.



NOTES:

1. Only one device can be plugged into the "U" interface at a time!
2. Local battery backup is necessary only if ISDN is the only communication line into a home or residence since it is not provided by the telephone company. A power outage would make communication on ISDN impossible without local battery backup.

FIGURE 1. INTERFACE BREAKDOWN

For the sake of brevity, the call setup process will be discussed on the level seen by the host software. It is not necessary at this point to get into the actual bit stream commands at the two wire level. To properly envision the process we will consider that only three distinct computers are involved: the originator, the network (the computer controlling the network switch), and the Receiving computer (see Figure 2).

The basic steps are Setup, Call Proceeding, Alerting, Connect, and Connect Acknowledge. These five steps, if identified correctly in software, can be used as the breaking points for proper SLIC control. It should be noted that the D channel of the U interface is normally active and communicating with the central office. A connection usually refers to the connection of the B channels only.

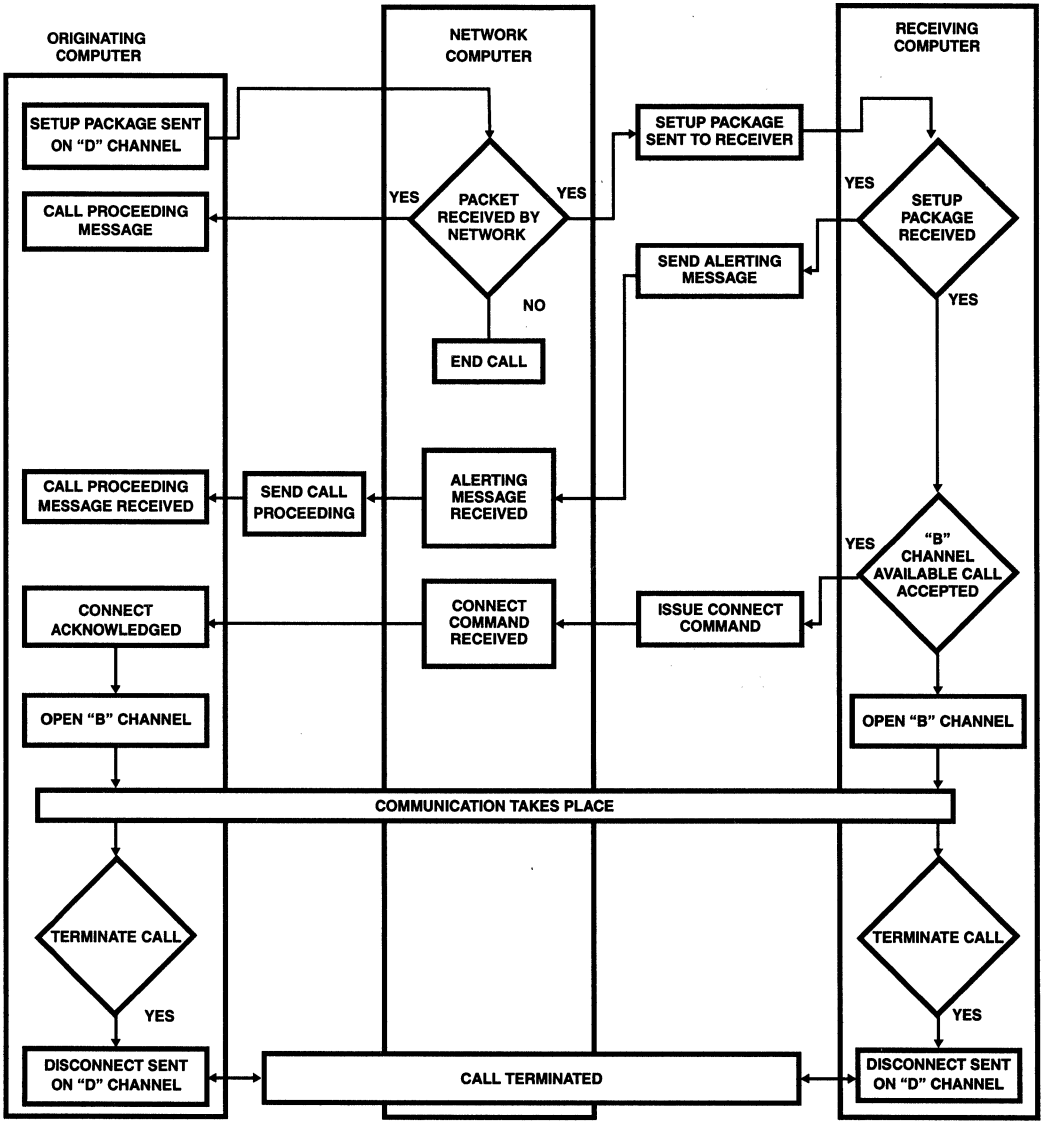


FIGURE 2. CALL SETUP PROTOCOL AN CALL RELEASE

Setup

The "setup" step is analogous to dialing an analog telephone. During this process a number of packets are sent over the D channel specifying the originating telephone number, the destination phone number, the quality of line required, the type of transmission to follow including the compounding method if telephony is selected (μ law or A law).

This packet is received by the network and passed on to the receiving station. Just after the network passes this packet on (sometimes with slight modification), the network returns a "call proceeding" message back to the originator. There is no direct equivalent in the analog world with the possible exception that a series of clicks or varying static can be heard after completing a DTMF sequence and before ring back begins. The next step is totally dependent on the receiving station. It has to acknowledge the receipt of the

setup packet and return an "alerting" message to the network. The network passes this "altering" message on to the originating station as a "call proceeding" message. This "call proceeding" message is equivalent to ring back in an analog system. At the receiving end, the NT-1 passes the "setup" message on to the end user that may be connected directly, via an S interface, or via a terminal adapter. If a B channel is available and if the intended receiving station accepts the call, it issues a "connect" command to the network. The network passes this command back to the originating station as a "connect acknowledge" message and opens a B channel for both the receiving station and the originating station. The originator processes the "connect" message received and begins to communicate on the B channel with the type of service requested by the original "setup" message. At this point synchronization on the B channels takes place and communication begins.

Call Release

The process of call release (hang-up) is quite straightforward. It can be initiated by either end of the call in progress at any time since the D channel does not have to wait for any particular pause in the B channel(s) in use. A disconnect signal is sent to the network on the D channel, passed on to the opposite station, and both sides then disconnect their respective B channels as does the network. It should be noted that timers similar to those in an analog interface are used by the network to make sure that no phase of setup or call release hangs up and a line holds open.

Services Provided and Handshaking

Simply stated, a service is a method of communication over a B line. This can take the form of a pure data connection using one of the more common protocols such as Point to point Protocol, Multilink Point to Point Protocol or the service can be specified as a telephone voice connection or as a 3.1kHz analog connection for analog modem use. Of course, there are a number of other services such as teleconferencing over a B line, but the three just mentioned are the most common. The two that are of particular interest here are the two analog services. They may seem arbitrary, but specifying one or the other actually optimizes the total bandwidth and the bit error rate of the line in use. Some of the original specs governing ISDN separated these into two categories defining mostly the quality of the line assigned. A voice connection can stand to lose a little data here and there, where a modem connection cannot.

Interface Functions

In every telephone system there has to be some way to transform the analog voice signals to a digitally coded bit stream. In a standard telecommunications application, that part is called a CODEC. It provides the Analog to Digital (A/D) and Digital to Analog (D/A) function between the four wire transmit/receive interface to the two wire analog world. It also performs a function called companding that reduces the overall bandwidth of the signal. A part is needed in the ISDN world that provides a similar function as well as telephone control, ring signaling, status detection, and power control. One family of parts that provides these functions is the ARCOFI® by Siemens. Although initially designed to power a separate microphone and loudspeaker for implementing a crude speaker phone, the ARCOFI makes a good starting platform for the analog interface by providing the following functions:

a) Analog to Digital Interface.

b) Digital to Analog Interface.

c) Switch Hook Detection Interface.

d) Ring Trip Detection Interface.

e) Power Supply Control.

f) Ring Signaling Including Ring Cadence Generation.

g) Two Wire Power Denial for rEfusing Access to the ISDN Line Through the Analog Port.

h) Companding (μ-Law or A-law Selectable).

SLIC Functions

The HC5517 SLIC provides the two wire to four wire interface, as well as most of the standard Borscht functions needed to completely control the telephone. The basic goal is to make the RJ11 analog port on the ISDN modem card as close as possible to a standard telephone line. The HC5517 accomplishes this by providing the following functions:

Loop Current Generation

The loop current provides a medium for incoming and outgoing calls to take place, as well as providing power to any DTMF generation circuitry in the phone. Programming of the maximum loop current is performed by resistors R_{10} and R_{28} (see Figure 3). Since an ISDN modem application is typically very short loop, the total two wire voltage as well as the loop current are both limited to prevent overheating of the SLIC and wasted power in the modem.

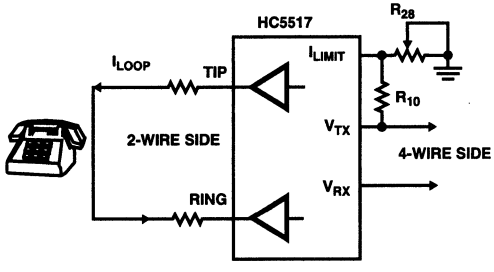


FIGURE 3. LOOP CURRENT GENERATION

Switch Hook Detection

The SHD pin on the HC5517 goes low whenever the telephone goes off hook. This provides an indication of the status of the telephone set as well as providing a signal to the ISDN interface to begin an ISDN connection upon call initiation.

Ring Trip Detection

The RTD pin on the HC5517 goes low whenever the telephone goes off hook during a ring period. This provides signaling to the ISDN interface to stop ringing and answer the incoming call on the ISDN line by sending a CONNECT command to the network.

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Ring Generation

This function of the HC5517 is the primary advantage of using this type of SLIC over a standard Central Office SLIC. The standard topology to ring a telephone is shown in Figure 4.

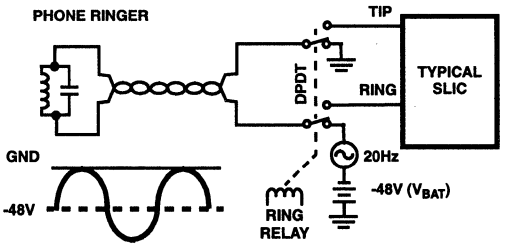


FIGURE 4. BATTERY BACKED RINGING

Typically the SLIC is removed from the two wire side by a DPDT relay which then inserts a high current 20Hz AC signal biased on top of V_{BAT} which is typically -48V_{DC}. The resulting waveform is also shown in Figure 4. This is called battery backed ringing since the 20Hz AC signal is backed or biased up by the battery voltage. Obviously this method requires a separate high power AC signal generator precisely tuned to 20Hz; that can get expensive and bulky. This is the type of ringing approved by TR57 and required for all central office applications. However, since the ISDN modem is not connected to the standard analog telephone system, and is therefore not directly governed by that part of the TR57 spec, some liberties can be taken to allow a much simpler design that is much more cost effective.

The HC5517 topology to ring a telephone is shown in Figure 5. Instead of removing the SLIC from the two wire lines as in the standard central office topology, the SLIC is left connected and the ring signal is supplied by the large amplifiers feeding the tip and ring lines internal to the SLIC. If the control line (RC) goes high, the SLIC is put into ring mode. In this mode the tip and ring terminals both slew to $V_{BAT}/2$ (40V if the V_{BAT} power supply is at 80V). Any signal on the V_{RING} pin is multiplied by a gain of 40 and appears across the tip and ring amplifiers. The rest of the hardware involved in this process will be described in the "Glue Circuitry" section.

The circuit in Figure 5 provides balanced non battery backed ringing at power levels adequate to ring 3 REN. A REN (Ringing Equivalency Number) is defined in the FCC specs as a standard impedance by which telephone systems can be measured and tested. A single REN is generally equivalent to an old desktop telephone with mechanical bell ringers. Therefore, the HC5517 would be capable of ringing up to three of these old phones. The vast majority of newer phones use piezo or other electronic ringers that make use of only a fraction of a REN. In that type of situation many phones could be rung simultaneously. The ring signal is also not battery backed; this brings the peak voltages down to a much lower level that is simpler and cheaper to generate and creates less of a safety issue inside the computer (see Figure 5). Telephones and other equipment only respond to the AC RMS signal, so the lack of a DC bias is not a requirement for ring. The primary requirement to ring all telephones reliably is for the ringing voltage to be at least 40V_{RMS} at 20Hz. Some other papers indicate that all phones will ring with a peak of 56V_{RMS} and a crest factor of only 1.2, however that is not the case. A full 1.41 crest factor is needed to ring many newer phones such as those produced by Northern Telecom.

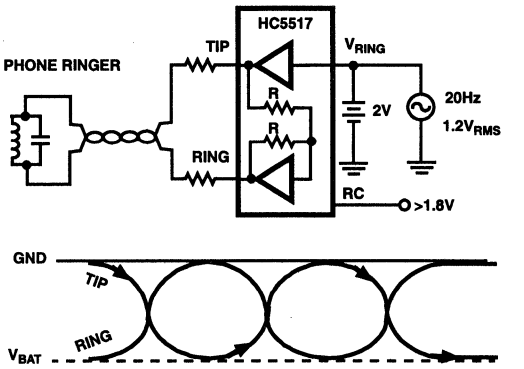


FIGURE 5. BALANCED RINGING

It should be noted that 20Hz is critical since most phones are tuned to respond to a very narrow frequency band around 20Hz. The HC5517 will easily generate the ring signal at this frequency with any desired wave shape. There are three main options for wave shape in the present industry: square wave, trapezoidal wave, and sine wave. TR57 requires a sine wave to reduce channel to channel interference and provide the highest possible energy to the telephone. A square wave is composed of the primary and an infinite number of harmonics that cause interference in adjacent channels and become merely unused energy as the telephone ringer filters out everything but the primary 20Hz. A trapezoidal wave is a compromise of the two. It also wastes some energy in the harmonics and creates a noisy ring signal. Therefore, the sine wave is preferred whenever possible. The HC5517 SLIC will drive any of the above ring signals and provides the most options for ringing of any SLIC on the market.

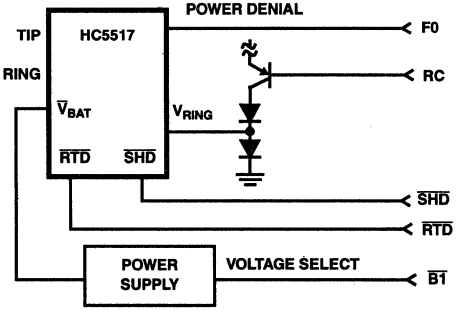


FIGURE 6. SLIC CONTROL AND INTERFACE

SLIC Control and Interface

For the most robust control of the analog port, 5 digital I/O lines are needed for communication with the ISDN interface (see Figure 6). These 5 lines can come directly from a device like the Siemens ARCOFI, any controller connected to the S or U interfaces, or directly from the host processor by way of the Peripheral Component Interconnect (PCI) or Industry Standard Architecture (ISA) bus. The 5 signals needed are Switch Hook Detect (SHD), Ring Trip Detect (RTD), Ring Cadence (RC), F1 (power denial pin), and Battery Switch (B1). SHD and RTD are described above in the SLIC functions section. RC is the Ring Cadence input to the SLIC circuitry that gates the sine generator connection to the V_{RING} pin and switches the transistor to create the proper DC bias on the V_{RING} pin for optimum balanced ringing. RC is normally provided by timing generators that produce a variety of pattern as shown in Table 1. F1 is an input to the SLIC that will put the system in a low power mode. This limits loop current to the two wire side which disables voice and Dual Tone Multi Frequency (DTMF) signals from an external handset. It can be used to password protect the analog port for cost savings since the use of a standard telephone line (if available) is generally cheaper. Finally the B1 is used to switch from the ringing voltage of -80V to the active voltage of -27V.

TABLE 1. DISTINCTIVE ALERTING PATTERNS

	INTERVAL DURATION IN SECONDS					
PATTERN	RINGING	SILENT	RINGING	SILENT	RINGING	SILENT
A	0.4	0.2	0.4	0.2	0.8	4.0
B	0.2	0.1	0.2	0.1	0.6	4.0
C	0.8	0.4	0.8	0.4	-	-
D	0.4	0.2	0.6	4.0	-	-
E	1.2	4.0	-	-	-	-
F	1 ±0.2	3 ±0.3	-	-	-	-
G	0.3	0.2	1.0	0.2	0.3	4.0

TABLE 2. LOGIC STATES FOR APPLICATIONS REQUIRING FAX AND ANSWERING MACHINE OPERATION

STATE	RC	F1	B1	BATTERY (V)
Standby (On-hook)	0	1	0	-80
Ringing (On-hook)	1 (Pulsed)	1	0	-80
Active (Off-hook)	0	1	1	-27
Power Denial	x	0	x	x

Power Needs

For standby and ringing modes, the SLIC requires $-80V_{DC}$ and for the off hook active mode the SLIC can be operated at $-27V_{DC}$ for power conservation (see Table 2). The -80V provides the high energy needed to ring a telephone during the ring period and provides a high enough voltage to create a -48V potential across the two wire interface during standby operation. In the standby state the application circuit limits the tip to ring voltage to within the Maintenance Termination Unit (MTU) voltage of -42.25 to -56V. The MTU voltage is generated by using the breakover voltage of the external zener diode (D11) to set the internal reference voltage. The MTU potential across the tip and ring wires is not necessary for normal telephone operation, but some fax machines, answering machines, and test equipment look for an MTU voltage to signal on hook active lines. If a system does not need to support fax or answering machines, the -27V supply can be used during all modes except for ringing, see Table 3.

TABLE 3. LOGIC STATES FOR APPLICATIONS NOT REQUIRING FAX AND ANSWERING MACHINE OPERATION

STATE	RC	F1	B1	BATTERY (V)
Standby (On-hook)	0	1	1	-27
Ringing (On-hook)	1 (Pulsed)	1	0	-80
Active (Off-hook)	0	1	1	-27
Power Denial	x	0	x	x

Supply currents are minimal since an ISDN modem is truly a short loop application. During the on hook mode, the 80V source only needs to supply a maximum of a few milliamps to the SLIC and its supporting circuitry. During the active mode, the current around the two wire loop is set by external resistors usually somewhere in the range of 25 to 40mA. Therefore the total supply current will be the loop current plus about 5mA for SLIC internal use. During the ring mode the largest amount of power is needed. If we assume that a single REN is roughly equivalent to 8000Ω resistive (a rough approximation strictly for power consumption calculations) then it can be shown that for each REN connected to a $40V_{RMS}/56.6V_{PEAK}$ two wire interface about 7mA of current will be drawn. The maximum power will be drawn at the highest load of 3 REN supported by the HC5517. This creates about 21mA around the two wire loop. The SLIC itself draws about 10mA of internal current during the ring mode so the total is about 31mA at 80V for a fully loaded ringing SLIC.

Hardware

The Two Wire Side

The two wire interface is the user interface of the analog port. It consists of a pair of wires that closely emulates a standard telephone jack. The polarity of these wires for normal operation is irrelevant. This interface is shown to the left of the SLIC in Figure 11 and the supporting components include the diode bridge (D1-D4) and the four feed/sense resistors (R11-R14). The diode bridge provides a small amount of surge protection for the circuit. Any voltage higher than V_{BAT} or lower than ground is chopped off and prevented from reaching the SLIC.

The "Glue Circuitry"

A number of intermediate functions can be controlled by external discrete components around the SLIC such as loop current, two wire impedance, transhybrid balance, DC ring

bias, short circuit protection, MTU voltage, and ring trip detection. The application note for the HC5517 evaluation board includes parts for pulse metering, but since ISDN does not perform that function those components will not be discussed here.

The loop current can be set by adjusting resistors R10 and R28. The ratio of R10 to the set resistance on R28 determines the current limit for the two wire loop. The current limit is determined by the following equation:

$$I_{Limit} = 0.6\frac{(R_{10} + R_{28})}{200 \times R_{28}} \quad \text{(EQ. 1)}$$

Resistors R8 and R9 should be set to provide a gain of one for the internal transmit op amp. This sets the two wire impedance, as well as the transhybrid balance circuit input. More information on impedance setting can be obtained in Application Note AN9607. A good choice would be 40K resistors as shown in the schematic. C8 provides AC coupling to block the bias generated by the loop current limit pot R28.

Transhybrid balance refers to the electrical canceling of the input signal in the SLIC output. This is necessary because of the full duplex nature of the two wire interface. Both received signals (from the ISDN interface) and transmitted signals (from the handset microphone) are simultaneously present on the two wire interface. Both then appear on the transmit line on the output of the SLIC. If not canceled, the signal originally received from the network would be retransmitted to the network causing an intolerable echo on the line, making communication almost impossible. The simple solution is to remove the original input signal from the signal transmitted to the network. Simply (In + Out)-In = Out. This is accomplished by creating a resistive network around an op amp that sums the currents into a node. The original input signal goes into the node as +In, the summed signal comes out of the SLIC as (-In) + (-Out) and the result is (+In) + (-In) + (-Out) =-Out. The result is inverted by the external op amp and simply becomes +Out. Transhybrid balance therefore, measures the ability of this circuit to cancel the input signal. A number of elements factor in to the value of transhybrid balance, but the better the impedance matching, the better the transhybrid balance and the less echo present. The only other thing to note is the gain of three in the external op amp circuit. This is necessary because of the HC5517's internal gain of one third. Reference Application Note AN9628 "AC Voltage Gain for the 5509 Series of SIIC's".

As previously mentioned, when the RC input goes high the external application circuitry puts the tip and ring voltages at $V_{BAT}/2$ to provide the most headroom for differential ringing. The circuit used to generate the centering voltage is shown in Figure 7.

The circuitry within the dotted lines is internal to the HC5517. The value of the resistor designated as R is 108kΩ and the resistor R/20 is 5.4kΩ. The tip amplifier gain of 20V/V amplifies the $+1.8V_{DC}$ at VC to $+36V_{DC}$ and adds it to the internal $4V_{DC}$ offset, generating $-40V_{DC}$ at the tip amplifier output. The -40V dc offset also sums into the ring amplifier, adding to the battery voltage, achieving -40V at the ring amplifier output.

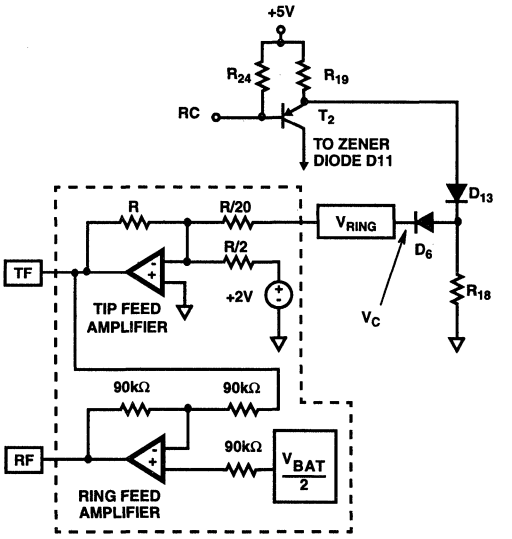


FIGURE 7. BALANCED RINGING

The 1.8V is applied to the V_{RING} pin when the pnp transistor is turned off by the high on RC. This causes the resistors R18 and R19 to create a simple divider from $5V_{DC}$ along with a couple of forward diode drops. Putting the V_{RING} input between the diodes has the effect of isolating the V_{RING} pin from the resistor to ground seen in R18. That resistor would affect the longitudinal balance, 2-wire return loss and Idle Channel noise.

A simple sine wave generator is needed to provide the proper voltage to the V_{RING} pin. The proper voltage is one that utilizes the entire headroom so as to provide the greatest ring energy to the telephone, while not being so large as to clip against the rails. The maximum tip to ring voltage is equal to V_{BAT} minus the output transistor overhead of 6V (3V for tip and 3V for ring). The maximum tip to ring voltage with an 80V supply is 80 -6 = 74V. Therefore, the maximum input voltage to prevent clipping is approximately $1.3V_{RMS}$. (1.3*1.414*40 = $74V_{PEAK}$ or $52.33V_{RMS}$). Recall that $40V_{RMS}$ is the minimum voltage required to ring all telephones so there is considerable headroom in this design. Any input voltage from $1V_{RMS}$ to $1.3V_{RMS}$ will normally be acceptable.

When the transistor (T2) is on (RC low) and $V_{BAT}/2$ is greater than the zener diode (D11) breakdown voltage, D11 clamps the maximum voltage on the V_{REF} pin and thereby the ring feed amplifier voltage. The maximum DC output voltage of the ring feed amplifier (V_{RDC}) is given in Equation 2.

$$V_{RDC} = 2(-V_Z + (V_{BE} - V_{CE})) + 4 \quad \text{(EQ. 2)}$$

The V_{RDC}, with a 28V zener, is -52.6V (2(-28+0.3) +4). The MTU voltage is the ring voltage minus the tip voltage and is equal to -48.6V.

Short circuit protection is simply provided by the capacitor C16, Figure 11. When the metallic loop current exceeds the set reference level, the SLIC's transconductance amplifier

sources current. This current charges up C16 in the positive direction, causing the ring feed voltage to approach the tip feed voltage, effectively reducing the battery feed across the loop which will limit the DC loop current. The value of the capacitor determines the speed of this reduction.

The Ring Trip Detect circuit uses R15-R17, D5, and C10 to detect the negative high voltage peak when a handset is lifted off hook during a ring interval. Under normal conditions during a ring mode, a high voltage differential sine wave is applied across a relatively high impedance (up to 8KΩ for 1 REN). This creates a relatively low current and is sensed by the SLIC and output on the V_{TX} pin. When the handset is lifted off hook, the metallic contacts provide a much lower impedance to the same applied ring voltage creating a significantly higher AC loop current. This difference in AC current is used for ring trip detection, by putting a trip point between the high and low level output voltages. All that has to be done is rectify that AC voltage, divide down the output voltages, and set a trip point in-between them. The trip point should be high enough to guarantee that noise does not cause an artificial ring trip detection yet low enough to guarantee that even with modest loop lengths and a variety of phones that removing the receiver from the hook crosses the trip point. The resistor divider simply sets this trip point to match the internal 0.24V reference. The capacitor provides a bit of a filter to damp out fast transients that might cause a false ring trip detect. The RTI pin on the SLIC is essentially an input to an internal comparator that trips at 0.24V. To activate the RTD pin, at least 0.24V must appear on the RTI pin. The resistors can be changed to create different trip points for different operating voltages and conditions.

Test bar and RS pins should be pulled high by a 10K resistor.

Sine Wave Generator

There are literally hundreds of circuits that would provide a cost effective sine wave oscillator for use in the ring circuit, but one of the easiest to understand and implement is a simple Wein bridge oscillator. This straightforward circuit can be found in a majority of college texts and is simple to derive. The basic assumption is that a circuit will oscillate according to the Barkhausen criterion. That is, a circuit will oscillate where the overall loop gain is one and the phase shift is zero. (see Figure 9) The loop equations for the frequency response of the circuit are:

$$V_{in+j\omega} = \frac{\frac{R}{1+j(RC)}}{\frac{R}{1+j(RC)}+R+\frac{1}{jC}} \qquad \text{(EQ. 3)}$$

Since we add R_6 and R_5 around the negative feedback path, the total loop equation reduces to:

$$T_{(j\omega)} = \left(1+\frac{R_6}{R_5}\right)\times\left[\frac{1}{3+J\omega\left(RC-\frac{1}{RC}\right)}\right] \qquad \text{(EQ. 4)}$$

Therefore, the frequency at which the circuit will oscillate is where the phase is zero or:

$$\omega = \frac{1}{RC} \qquad \text{(EQ. 5)}$$

And the gain to sustain oscillation needs to be a total of 1 around the loop so:

$$\left(1+\frac{R_6}{R_5}\right)\left(\frac{1}{3}\right) = 1 \qquad \text{(EQ. 6)}$$

or $R_6/R_5 = 2$

The amplitude of the oscillation can be controlled with a non-linear limiter around the entire loop. In this case the oscillation needs to be set at $1.3V_{RMS}$ and the frequency needs to be kept as close to 20Hz as possible; in fact TR57 says it needs to be within 3Hz. The values shown on the schematic should do just that. The CA124 op amp can also be used in place of the CA324 if more precision is necessary. The resistor values should have a tolerance of 1% and the capacitors should be 5% ceramics.

ARCOFI Interface

Whether the ARCOFI is used or one of the many other brands of interface chips, the basic interface idea is the same. These types of chips generally include a microphone input, a speaker output (amplified), a CODEC, a number of programmable timers, multiple programmable gain stages, and analog filters. The internal CODEC needs to be programmed to the appropriate companding type for the area, and the gain stages should be set to transmit and receive a maximum of $2.5V_{PEAK}$ without clipping. The microphone input is used in a balanced configuration to receive the outgoing transmission from the transhybrid balance circuit. The input is centered about 2.5V by using the internal V_{REF} of the ARCOFI tied to the non inverting input of the external op amp. There is also a diode clamp that limits the output of the amp to between +5V and ground. This is necessary to protect the input of the ARCOFI and may or may not be needed, depending on the interface chip used. The HOP pin is used for the receive signal from the network to the SLIC. It is generally meant for a handset output, but the specs for its impedance and voltage capabilities more closely match the SLIC than any other output. The simplest implementation of the digital I/O interface uses the four programmable pins on the ARCOFI for control and monitoring of the SLIC.

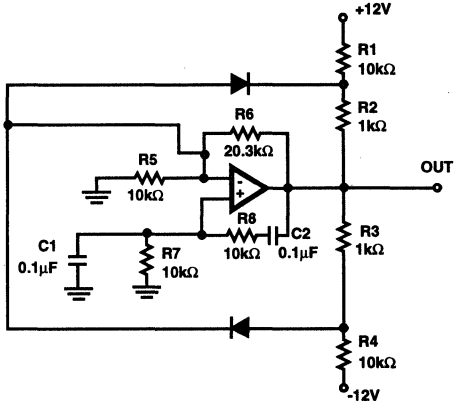


FIGURE 8. TYPICAL WEINBRIDGE OSCILLATOR

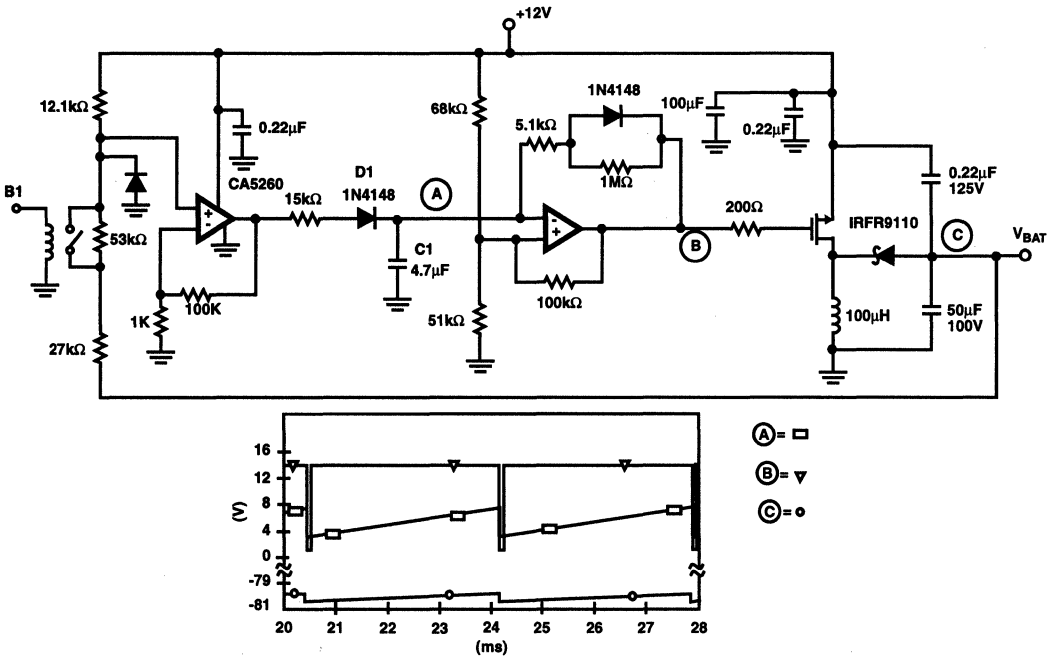


FIGURE 9. SIMPLE BOOST CONVERTER

Simple Boost Converter

The power needs for this type of circuit are new to computer cards. There will be no -80VDC supply available on the PCI or ISA bus so it needs to be generated locally. The first issue is safety - does the supply need to be isolated? Probably not, since the primary supply from which it draws its power is undoubtedly already isolated. Does it need overcurrent protection? Again, probably not since the SLIC itself provides short circuit protection. However, since requirements vary from system to system, two different power supplies will be shown that would adequately support the analog interface. The simple boost converter is shown in the schematic and has the advantages of being the smallest and cheapest. The object will be to derive -27 and -80VDC from the +12V supply with a reasonably high efficiency and with a minimum parts count.

The circuit basically consists of a dual op amp, a FET, an inductor, a rectifying diode, and some output capacitance (see Figure 9). The first amp on the left acts merely as an error amplifier. The resistors on its input form a voltage divider. The error amp tries to maintain a virtual ground on that pin so zero appears on that pin when the output voltage is correct. A 48K resistor would give -48V, an 80K resistor gives -80V, and a 27K resistor gives -27V. Obviously it will be quite simple to change the output voltage by simply switching in different resistances to the bottom of the divider. The only precaution is that the switch needs to withstand a full 80V of potential. A simple relay is the most straightforward method of switching. Note that a SPST relay can be used if it is put across the 53K resistor. When open the total resistance is 53 + 27 = 80KW and when closed the total resistance is 27+(contact resistance) = ~27KW. This is cheaper than using a SPDT relay with a 27K and an 80K resistor attached. The gain around the error amp is about 100 to set the sensitivity and accuracy of the supply.

In any other application the next section to the right would be termed a peak detector, but upon further investigation the diode and cap interact with the following op amp to form a simple multivibrator. The basic circuit can be found in most college textbooks, but the basic function is fairly straightforward. The resistors on the non inverting input of the second amp form a resistor divider that sets the trip points of the "comparator". The trip points are skewed by the positive feedback to create some hysteresis. The basic triangle wave that the amp compares the trip points to is generated by the resistors in the negative feedback loop acting on C1. If the output is high, diode D1 is reverse biased and the total resistance between the 12V output and the cap C1 is a little more than 1MW. The cap will charge to the high trip point and cause the output of the amp to go low. This forward biases D1 and causes the total resistance between C1 and ground to be about 5.1K. This discharges the capacitor rather quickly. This alternating charge and discharge sets up the basic triangle wave that translates to a square wave at the output of the amp, that in turn drives the gate of a P channel FET. A low output corresponds to the 5.1K time constant and sets the on time of the FET. If the voltage detected by the error amplifier is too low, the off time is simply reduced by pre-charging C1 with the error amplifier. Waveforms for the circuit are also shown in Figure 9.

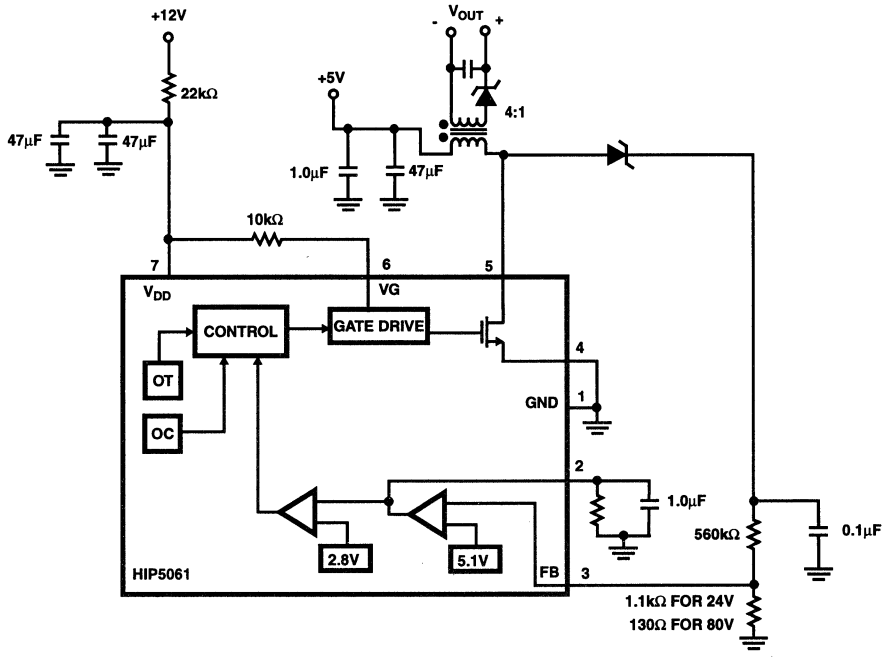


FIGURE 10. ALTERNATE ISOLATED CONVERTER

The rest of the circuit follows the well understood equations of an inverting boost converter. When the FET is on, the rectifying diode is reverse biased. The current in the inductor ramps up linearly at a rate di/dt = Vin/L. After the on time (governed by the time constant of 5.1K and 4.7nF) a total energy has been stored in the inductor of:

$$E = \frac{1}{2}(LI_P^2) \quad \text{(EQ. 7)}$$

where the peak current is given by:

$$I_P = \frac{V_{in}t_{on}}{L} \quad \text{(EQ. 8)}$$

When the FET turns off, the inductor tries to maintain constant current so the voltage across it changes polarity and the peak current begins to flow through the rectifying diode and the output capacitor. This charges the cap up to a negative voltage. If all of the energy stored in the inductor is transferred to the output capacitor before the next turn on period, then the circuit is said to operate in discontinuous mode. This in fact is necessary for stability of the control loop. The total power delivered to the load is

$$P = \frac{1}{2}\frac{L(I_P^2)}{T} \quad \text{(EQ. 9)}$$

$$V_o = V_{in}\left[T_{on} \times \sqrt{\frac{R_o}{2T \times L}}\right] \quad \text{(EQ. 10)}$$

T = total period

and of course $P = V^2/R$ so the output voltage can be found from Equation 10:

Note that in this particular case the on time is held constant and the period is varied unlike a standard pulse width modulator where the opposite is true.

The output capacitor must be capable of sustaining the output current during an entire cycle of the FET without allowing excessive droop. Since the cap must support the entire output current for a majority of the time, a fairly large value is required.

Alternate Isolated Boost Converter

Since system requirements periodically dictate more stringently designed power supplies, an alternate power solution is also available. If isolation, overcurrent protection, or overtemperature protection are needed, a simple boost regulator with an output transformer can be used. The simplest and most cost effective solution that provides all these features can be found in the HIP5061 family of controllers. The HIP5061 (see Figure 10) contains all the necessary components on a monolithic die to perform all the necessary functions involved in controlling a boost regulator (oscillator, PWM, OT, OC, precision reference, and integrated FET). The only limitation of using the HIP5061 to implement the telecom supply is that the HIP5061 has a maximum voltage rating of 60V. The output transformer needs to be a step up so that the primary can run at a lower voltage that is within

the range the HIP5061 can handle. A 4:1 transformer provides a reasonable primary voltage.

In order to keep the cost down, primary side control will be used (otherwise another isolation boundary must be crossed by either another transformer or an optocoupler). The same basic method of setting the output voltage applies to this circuit except that the internal reference is 5.1V. So a 1.1K resistor on the bottom gives 24V and a 130Ω resistor gives 80V.

A small rectifier and output cap on the secondary side is all that is needed to provide sustained DC voltage. All protection functions are taken care of internal to the HIP5061 so only those parts shown are necessary. This implementation is slightly more expensive than the simple boost converter but if the extra features are needed it provides a simple topology.

Battery Backup

The local telephone operator provides a large battery bank at each central office to give emergency power to telephones during the event of a power loss Even if electric power to the home is lost, the telephone line keeps working (although cordless and powered phones will obviously die). This is necessary since 911 and emergency services often need to be accessed during power outages. The ISDN line, however, has no battery backup provided by the telephone company to power the ISDN modem. That power has to come from the computer slot. It might not be necessary to provide battery backup for ISDN unless it is the only communication line into the home. Most homes will have ISDN and a standard analog telephone to provide emergency access. If ISDN is the only line, there are two methods for battery backup. If the NT-1 is an independent unit and it has an analog port with an HC5517 SLIC installed, only the NT-1 needs battery backup. The rest of the devices on the S interface can go down, and the analog port on the NT-1 can still dial out. If the NT-1 is part of another card like a modem card, the entire computer with that card needs battery backup. These devices are very reasonably priced and will also prevent data loss in the event of a power failure. An uninterruptable power supply can be constructed fairly simply using Application Note 9611 "A DC-AC Isolated Inverter Using the HIP4082" with a few minor modifications. A gel cell battery provides a reliable long life energy source that can be continuously trickle charged.

Options

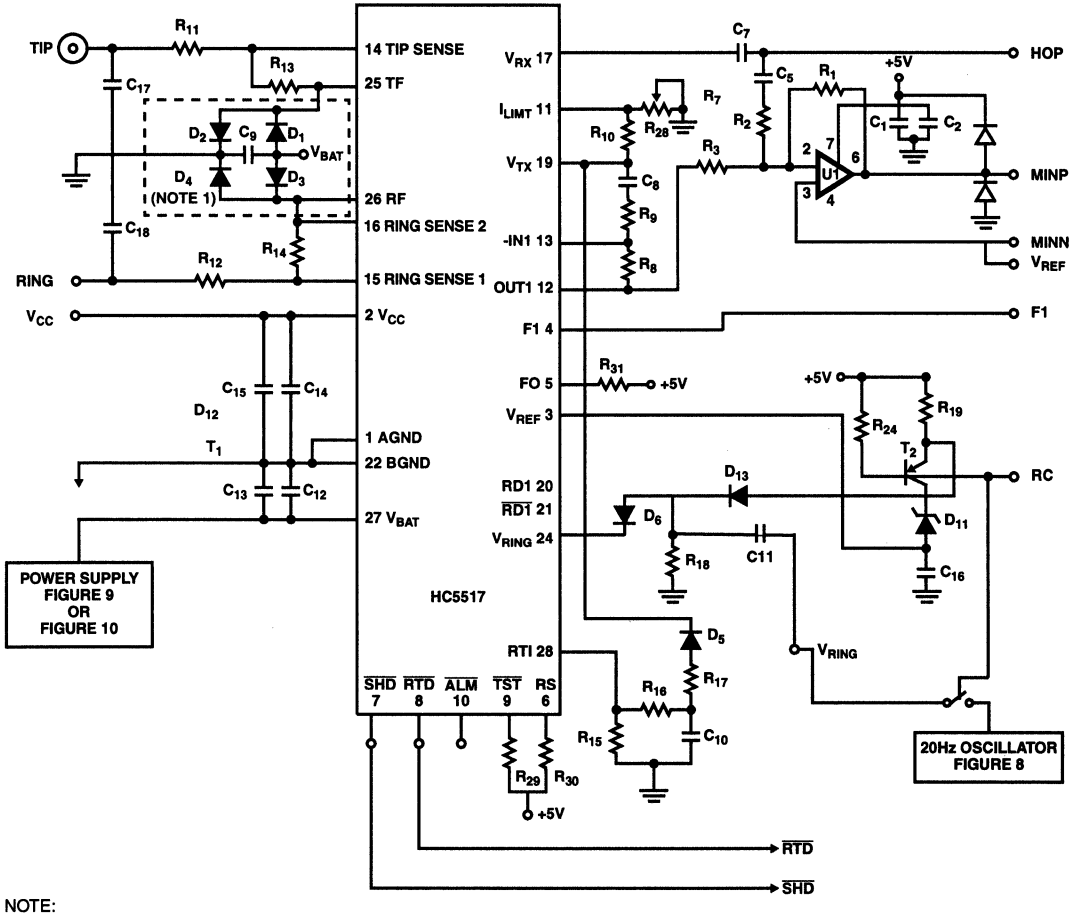
To simplify the design a number of things can be done.

For instance, it is not necessary to distinguish between switch hook detect and ring trip detect. These signals could be or'd together to create a detect output to the ISDN interface. All that needs to be known is whether the phone is off hook or on hook.

Depending on what voltage choices have been made, that off hook condition could be used to also control the power supply (for instance if we choose to have 80V supplied to the SLIC in both ringing and standby modes and 27V supplied only during active or off hook periods).

The F1 (Power denial pin) could be controlled by an unused state of RC and B1 such as RC high and B1 indicating 27V. There would never be an instance when a ring is commanded with only 27V applied to the SLIC. This could signal a power denial state with simple logic and shut the SLIC down.

Using shortcuts like these could allow control of the SLIC with one digital input for switch hook detection and two outputs for RC and F1 (or RC and PS). This is only necessary if the number of I/O lines are limited since the most versatility can be obtained by having all five control lines active.



NOTE:

1. Diode bridge optional for in-house use.

FIGURE 11. APPLICATION CIRCUIT

COMPONENT	VALUE	TOLERANCE	RATING	COMPONENT	VALUE	TOLERANCE	RATING
SLIC	HC5517	n/a	N/A	C_2, C_{15}	0.1µF	20%	50V
R_1, R_2	24.9kΩ	1%	1/4 Watt	C_5, C_7	10µF	20%	20V
R_3	8.25kΩ	1%	1/4 Watt	C_8	0.47µF	20%	20V
R_8, R_9	40kΩ	1%	1/4 Watt	C_9, C_{12}	0.01µF	20%	100V
R_{10}	100kΩ	5%	1/4 Watt	C_{10}	1.0µF	20%	50 V
$R_{11\text{-}14}$	50Ω	1%	1/4 Watt	C_{11}	100µF	20%	5V
R_{R15}	47kΩ	1%	1/4 Watt	C_{13}	0.1µF	20%	100V
R_{16}	1.5MΩ	1%	1/4 Watt	C_{16}	0.5µF	20%	50V
R_{17}	56.2kΩ	1%	1/4 Watt	C_{17}, C_{18}	3300pF	20%	100V
R_{18}	1.1kΩ	1%	1/4 Watt	$D_{1\text{-}4}$	1N4007	-	100V, 1A
R_{19}	825Ω	1%	1/4 Watt	D_5, D_6, D_{13}	1N914	-	100V, 1A
R_{29}, R_{30}, R_{31}	10kΩ	5%	1/4 Watt	D_{11}	1N5255	-	28V, 1/2W
R_{24}	47kΩ	5%	1/4 Watt	T_2	2N2907	-	60V,150mA
$R_{25\text{-}27}$	560Ω	5%	1/4 Watt	F1, RC, Battery	SPDT Toggle switches, center off.		
R_{28}	20kΩ Potentiometer		1/4 Watt	U1	CA741C Op Amp		
C_1, C_{14}	0.01µF	20%	50V	Textool Socket	228-5523		

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Using the PRISM™ Chip Set for Low Data Rate Applications

Authors: Carl Andren and John Fakatselis

Introduction

The PRISM™ chip set has been optimized to address high data rate applications with up to 4 MBPS data rates. The PRISM™ can also be utilized for low data rate applications. To implement low data rate applications (below 250 KBPS) the designer needs to address design considerations in the following areas:

A. Selection of external filtering supporting the PRISM™ components.

B. Limitations on filter cut off frequencies of the HFA3724 internal Low Pass Filters.

C. Selection of appropriate carrier and clock oscillators to achieve the desired performance, given the HSP3824 internal Acquisition and Tracking loop integration constraints.

The system designer should also evaluate the option where the radio maintains its high data rate configuration but transmits the data using infrequent high data rate burst packets.

Where the system requires that the radio operate at low rates (<250 KBPS), the designer must address the areas highlighted on the PRISM™ block diagram shown in Figure 1.

Description

A. External IF Filtering

The band pass filters shown between the HFA3624 and the HFA3724 labeled as BPF1a and BPF1b on Figure 1 are centered at IF and filter the spread wideband waveform before demodulation on the receive side and before the final upconversion on the transmit side.

One might think that the TX filter can be avoided but it is required to meet the sidelobe suppression specifications according to FCC requirements.

PRISM™ PCMCIA Reference Radio Block Diagram

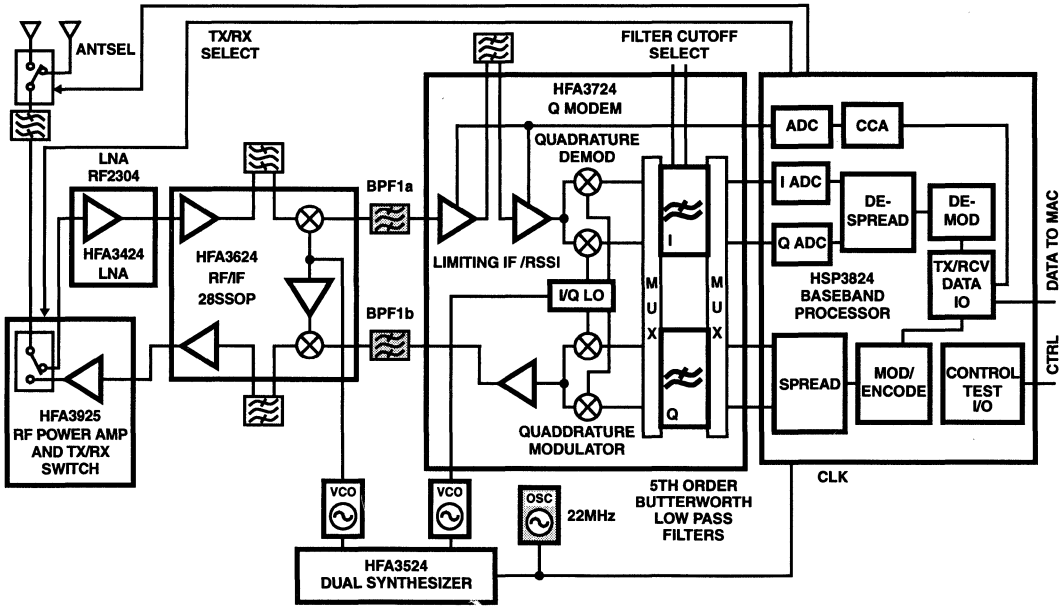

FIGURE 1. PRISM™ CHIP SET BLOCK DIAGRAM

For the high rate configuration of the PRISM™, a recommended implementation is to use SAW BPFs centered at 280MHz with a BW of about 17MHz. This is assuming an 11MHz chip rate (thus 22MHz spread null to null bandwidth). A recommended device that meets these requirements is the ToyoCom TQS-432.

If a low data rate configuration is implemented then substitute IF filters need to be identified that will filter to the channel bandwidth of the spread waveform at the lower chip rate. The designer can use any IF center frequency within the HFA3724 range. The designer must be sure, though, that the identified filter meets the transmission spectral mask requirements for FCC for the 2.4MHz ISM band. SAW filters for PCMCIA applications are not widely available at these specifications and a custom design may be required.

B. Limitations of HFA3724 LPFs

The HFA3724 includes a set of baseband low pass filters as the final filtering stage of the complex spread waveform. These are placed before the In phase (I) and Quadrature (Q) A/D converters for baseband processing. These filters are shown on Figure 1, as LPFs (Rx) and LPFs(TX). There are four cut off frequencies that can be selected for these LPFs. The cut off can be selected to be 17.6MHz (for a chip rate of 22 MCPS), 8.8MHz (for a 11 MCPS rate), 4.4MHz (for a 5.5 MCPS rate) or 2.2MHz (for a 2.75 MCPS rate). In addition these cut off frequencies are tunable through an external resistor by ±20%. The user can select one of the four discrete cut off frequencies. The lowest cut off is set for a spread rate of 2.5MHz chip rate and any chip rates lower than this will require the design of external filtering between the HFA3724 outputs and the HSP3824 A/D inputs. The HFA3724 I and Q LPFs are fifth order Butterworth filters and equivalent external filters need to be designed at the lower cut off specifications.

C. Selection of Carrier Frequency and Clock Oscillators

The HSP3824 performs the baseband demodulation function. The design includes digital signal acquisition and tracking loops for both the symbol timing clock and the carrier frequency.

The primary concern when the radio needs to be operated with a low instantaneous data rate is that it requires a wide bandwidth to accommodate oscillator frequency tolerances.

As an example at 2400MHz and ±25 PPM, the radio frequencies at each end of the link can be off by as much as 120kHz from each other. This offset must be well within the basic data bandwidth of the radio in order for it to be tolerated without degrading the performance of the link. If it is not, a frequency sweep would be needed to find the signals and this is not built into the radio design. Operating the radio with wide data bandwidth and low data rate is inefficient and would cause unacceptable loss in performance.

If the PRISM™ is used as a spread spectrum system with 11 chips per bit spreading ratio, this then gives it an IF bandwidth of nominally 22MHz null to null at 1 MSPS. We filter to 17MHz to allow closer packing of the channels. While this seems wide compared to the frequency offset, remember that this is a direct spread system. The first stage of processing the signal despreads it and collapses it to the data bandwidth. In PRISM™ this is done in a time invariant matched filter correlator. This correlator has an FIR filter structure where the PN sequence is substituted for the tap weights. The filter is operated at baseband, so the I and Q quadrature components are separately correlated with the same sequence. The outputs of the I and Q correlators are the vector components of the correlation. These will show a distinct peak in magnitude (compressed pulse) when correlation occurs. Correlation performance falls off when the signal is not stationary (i.e. has offset). The correlator convolves a stationary signal, (the PN sequence) with the input signal. The vector correlation is being rotated throughout the correlation by the offset frequency. This means that the signal correlates at one angle at the start of a symbol and at a different angle at the end. If this angular difference is small, no great loss occurs. The net correlation goes as the vector sum of all the correlation angles between the start and the end of the symbol as shown below. Thus the magnitude falls off to zero if the offset causes a baseband phase rotation of one cycle per symbol. The magnitude is obviously maximum at no offset and falls off about 0.22dB at 45 degrees rotation. This corresponds to the 120kHz offset (~1/8th of 1 MBPS).

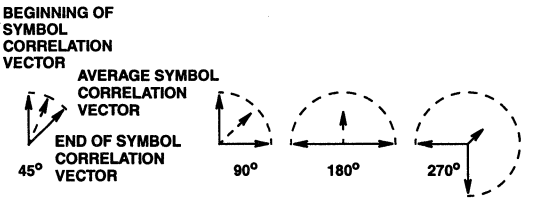

FIGURE 2. PRISM™ CORRELATION PERFORMANCE vs FREQUENCY OFFSET

Crystal oscillators of better than ±25 PPM accuracy can be purchased, but their cost goes up significantly as the tolerances are tightened. Given this offset, we must be sure that the receiver can accept the offset. At a data rate of 250 KBPS, the same offset loss occurs with a frequency offset 1/4th as large. This means that to get the same performance, we need oscillators specified to ±6 PPM. To go lower in data rate means tightening up the specification even further.

Similar consideration needs to be taken for the clocks that are used to run the baseband processor itself. The symbol timing clock tracking algorithm operates over 128 symbol integration intervals. To maintain acceptable BER performance the symbol timing phase drift must be less than 1/8th chip over the 128 symbol integration interval. Remember that we are tracking the peak of the compressed pulse which is 2 chips wide and must keep the straddling loss low by sampling close to the peak. For a 0.25 MBPS data rate, the chip rate is 2.75 MCPS. With this rate, the integration interval is 512ms which translates to an oscillator within ±89 PPM to keep the drift less than 1/8th chip (0.045ms). Since the spread rate to data rate ratio is not changed at the lower data rates, this tolerance is not effected by lower data rates.

High Rate Burst Transmissions With Low Average Rate

Generally, the incentive to use lower data rates is to achieve a given range with the minimum amount of power. We can show that this is also achievable by using the radio in its high data rate design configuration. The PRISM™ is a packet radio communications device and, as such, can send the data in a short burst with open environment ranges up to 5 miles. This has significant potential for power savings and reduction in interference. In the high data rate configuration the design considerations mentioned above are no longer of concern.

The system approach is to accept the 1 MBPS data rate of the radio as long as the achievable range is acceptable, and use it in a short burst mode which is consistent with its' packet nature. With a low power watch crystal, the controller can keep adequate time to operate either a polled or a time allocated scheme. In these modes, the radio is powered off most of the time and only awakens when communications is expected. This station would be awakened periodically to listen for a beacon transmission. The beacon serves to reset the timing and to alert the radio to traffic. If traffic is waiting, the radio is instructed when to listen and for how long. In a polled scheme, the remote radio can respond to the poll with its traffic if it has any. With these techniques, the average power consumption of the radio can be reduced by more than an order of magnitude while meeting all data transfer objectives.

Even using the 802.11 network protocols, the low data rate can allow low average power operation. The Media Access Controller (MAC) or network processor can operate the radio in the sleep mode except for the times it needs to receive the beacon signals.

The short, fast transmission is good for several reasons. First, if the signal is corrupted for any reason, a retransmission will occur without noticeable delay. Secondly, interference to other spectrum users is of brief duration. Third, and most important, the burst can be sent into small time gaps in the medium, which makes it more effective against certain type of interference in the ISM band. For example, if an 802.11 FH network is operating in the vicinity, it could cause interference with this network. The FH network has, however, a brief guard time when it is hopping and none of its stations are on the air. This time can be used to transmit the burst communications packets. Additionally, the microwave oven has been identified as an interference source of concern within the 2.4GHz ISM band. The oven is a pulsed source with about a 50% duty cycle. The gaps allow messages of about 1000 bytes through at the 1 MBPS rate.

In addition, the system can be set at its sleep mode most of the time to achieve low power consumption. It only needs to operate at full power consumption during the transmission of a packet or during the expected window for received packets.

The communications range achievable depends on the nature of the environment. A line of sight (LOS) path allows the best range. With 1W and 6dB gain in the antennas, you can readily achieve a 5 mile LOS range. The propagation loss at S-band is less than 0.5dB per mile in heavy rain, so weather is not usually of great concern. Antennas with 6dB gain are for fixed installations with one on one links. Mobile and network installations use omnidirectional antennas with around 0dB gain. Indoors, the range is much reduced by extra losses due to walls and other obstructions. The power is also usually reduced to 100mW for interference and safety concerns. These reduce the available range, but most applications will achieve sufficient range (300 ft.).

Antenna diversity is also used in the PRISM™ design to combat multipath interference. Since the PRISM™ waveform is wideband by being spread at the chip rate, the 1 MBPS data rate is not a contributor to multipath problems and a lower data rate is of no benefit.

So, in general, unless it is required to use low instantaneous data rates to achieve some other purpose, the packet capabilities of PRISM™ will serve well for these applications in its normal high data rate design configuration.

Harris Semiconductor

APPNOTE

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Harris Wireless Products

Programming the HSP3824

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Introduction

This application note serves as a firmware designers manual for the PRISM™ HSP3824 baseband processor. The note groups the programmable registers and their bit content by function. This note can serve as a quick reference for code development and system test and modification by function.

SW Overview

The HSP3824 offers flexibility for various system configurations through its programmable features. Among other the user has many options to control synchronization time, link protocol formats, data rates, performance thresholds, and visibility to internal modem parameters and status.

Preamble/Header

These configuration registers include preamble generation, transmit header modes and receive header modes. Preamble and header can be either generated internally from the HSP3824 or can be received from an external source i.e. a network processor.

Modem Configuration

These configuration registers include configuration for transmitter and receiver modem. The transmit and receive symbol rates, scrambler configuration, PN code configuration and antenna selection are also programmed through these registers.

I/O Configuration

These configuration registers include configuration of active signal levels (polarity) of HSP3824 I/O signals and set up of other miscellaneous I/O signal parameters. This is to provide flexibility and minimize glue logic to external circuits if there is a signal polarity issue.

Test Port Configuration

These configuration registers include configuration for selection of internal HSP3824 signals and/or data to become available at the Test Port pins. These signals can be useful during debugging, regulatory compliance testing as well as to design enhanced external algorithms to improve overall radio performance.

Threshold Settings

These configuration registers include a number of configurable threshold settings. They cover, Received Signal Strength Indication and Clear Channel Assessment threshold parameters, as well as, received signal quality thresholds used during acquisition and data tracking. By setting these acquisition and tracking thresholds, the user can define the desired modem performance i.e. set the probability of detection vs. the probability of false alarm ratio.

A/D Calibration

These configuration registers include configuration data to activate the A/D level adjustment circuit of the HSP3824. This circuit is designed to maximize utilization of the A/D dynamic range. This programmable circuit tries to keep the A/Ds close to saturation.

Modem Status

These configuration registers include information that represent both control and status registers (read-only). The status components indicate the real time state of the modem operation.

Signal Status

These configuration registers include information that represent modem parameter (read-only) registers. These modem status components are updated real time. They can be used to design external SW or HW algorithms to improve overall modem performance. In addition this set of registers provide information on the link protocol (header) that is presently in use.

Description of Configuration Register Assignments by Function.

The following paragraphs describe the configuration register (CR) content of the programmable HSP3824 registers. The bits within the CR that define the particular function or data are also indicated. The CR description and references below are broken by the primary HSP3824 programmable functional groups which are:

- Preamble/ header.
- Modem configuration
- I/O configuration
- Test Port configuration
- Threshold settings
- A/D calibration
- Modem status
- Signal status

This can serve as a quick reference to program or to modify registers by function. Refer also to the HSP3824 data sheet for description of the hardware algorithms at its appropriate sections. An example of a default set up is also attached to this note.

Preamble/Header

Preamble Generation CR3<2:2>

This control bit is used to select the origination of the Preamble/Header information. The preamble and header can be either generated internally by the HSP3824 or from an external source.

Transmit Mode CR0<4:3>

These control bits are used to select one of the four Preamble Header modes for transmitting data. The four modes contain different combinations of fields.

CR0<4:3> Header Contents

00 SFD, field
01 SFD and CRC16, fields
10 SFD, Length and CRC16, fields
11 SFD, Signal, Length and CRC16, fields

Receive Mode CR2<1:0>

These control bits are used to select one of four Preamble Header modes for receiving data.

CR2<1:0> Header Contents

00 SFD
01 SFD and CRC16
10 SFD, Length and CRC16
11 SFD, Signal, Length and CRC16

Transmit Preamble Length CR56<7:0>

This control register defines the Preamble length field value.

Start Frame Delimiter Definition CR49<7:0> CR50<7:0>

These control registers contain the Start Frame Delimiter used for both the Transmit and Receive header. This field is the address field for each individual receiver within the network.

Start Frame Delimiter Timer Enable CR0<2:2>

This control bit is used to enable the Start Frame Delimiter timer. If the timer expires before the SFD has been detected, the HSP3824 returns to acquisition mode. The search time is defined by the start frame delimiter value registers.

Start Frame Delimiter Value CR41<7:0>

This control register contains the number of symbol periods for the demodulator to search for a SFD in a receive header before returning to acquisition mode.

Data Field Counter Enable CR0<1:1>

This control bit is used to enable/disable counting the number of data bits in the length field embedded in the header. The HSP3824 returns to acquisition mode at the end of the count as defined by the "Length" field of the header. This can only be used in header modes 2 and 3.

CRC Check Enable CR2<5:5>

This control bit is used to enable/disable the CRC16 check on the received Header.

Modem Configuration

TRANSMIT CONFIGURATION

Chips per Symbol CR3<6:5>

These control bits are used to select the number of chips per symbol used in the I and Q transmit paths.

CR3<6:5>	00	01	10	11
Chips/Symbol	11	13	15	16

Rate Divisor CR3<4:3>

These control bits are used to select the divide ratio required to achieve the required data rate (refer to the HSP3824 data sheet).

CR3<4:3>	00	01	10	11
Divisor	2	4	8	16

Antenna Select CR0<7:7>

This control bit is used to select the transmit antenna (half-duplex mode only).

Modulation CR3<1:1>

This control bit is used to select the signal modulation type for the transmit packet.

Spread Sequence CR13<7:0> CR14<7:0>

These control registers contain the spreading code for the I and Q transmit paths.

RECEIVE CONFIGURATION

Chips per Symbol CR2<7:6>

These control bits are used to select the number of chips per symbol used in the I and Q receive paths.

CR2<7:6>	00	01	10	11
Chips/Symbol	11	13	15	16

Rate Divisor CR2<4:3>

These control bits are used to select the divide ratio required for the desired receive data rate.

CR2<4:3>	00	01	10	11
Divisor	2	4	8	16

Antenna Select CR0<6:6>

This control bit is used to select the receive antenna (single antenna mode only).

Modulation CR3<0:0>

This control bit is used to select the signal modulation type for the receive packet.

Spread Sequence CR20<7:0> CR21<7:0>

These control registers contain the despreading code for the I and Q receive paths.

Scrambler Taps CR16<6:0>

This control register contains the tap configuration for the transmit scrambler / receive descrambler.

Scrambler Seed CR15<6:0>

This control register contains the seed value for the transmit scrambler / receive descrambler.

Antenna Operation CR0<5:5>

This control bit is used to select between full duplex and half duplex operation.

Antenna Mode CR2<2:2>

This control bit is used to select single or dual antenna mode.

I/O Configuration

Allow Microprocessor Rate Change CR1<7:7>

This control bit is used to enable/disable constant data rates to the external processor that receives the demodulated data from the HSP3824. Rate changes from DBPSK to DQPSK within the same packet can be programmed to be transparent to the external processor.

Invert Transmit Clock Phase CR9<0:0>

This control bit is used to select the phase of the transmit output clock.

Assert TX_RDY Clock Count CR1<6:2>

These control bits are used to define the number of clocks before the first data bit that TX_RDY will be asserted.

ACTIVE SIGNAL LEVELS

These components allow the user to invert the sense of certain signals available as pins on the HSP3824.

MAC Data Ready (MD_RDY) CR9<6:6>

This control bit is used to select the active level of the MD_RDY signal.

Clear Channel Assessment (CCA) CR9<5:5>

This control bit is used to select the active level of the CCA signal.

Energy Detect (ED) CR9<4:4>

This control bit is used to select the active level of the ED signal.

Carrier Sense (CRS) CR9<3:3>

This control bit is used to select the active level of the CRS signal.

Transmit Data Ready (TX_RDY) CR9<2:2>

This control bit is used to select the active level of the TX_RDY signal.

Transmit Power Enable (TX_PE) CR9<1:1>

This control bit is used to select the active level of the TX_PE signal.

Test Port Configuration

Test Mode CR4<7:0>

The HSP3824 provides the capability to access a number of internal signals and/or data through the test port pins TEST 0-7 and TEST_CLK. The TEST_CLK is selected given the data that is clocked out from TEST 0-7 port. TX_CLK is intended to be used to clock the TEST 0-7 data from the HSP3824.

(0) Normal Operation Mode

<7:7> Carrier Sense (CRS)

<6:6> Energy Detect (ED)

<5:3> Reserved

<2:2> Initial Detect

<1:0> Reserved

TEST_CLK Internal TX Clock (TX chip rate)

(1) Correlator Test Mode

<7:0> Correlator Magnitude (PN correlator)

TEST_CLK Internal TX Clock (TX chip rate)

(2) Frequency Test Mode

<7:0> Frequency offset Register

TEST_CLK Subsample Clock (Rx symbol rate)

(3) Phase Test Mode

<7:0> Phase (instantenous I,Q)

TEST_CLK Subsample Clock (Rx symbol rate)

(4) NCO Test Mode

<7:0> Phase Accum Register (8 most significant bits)

TEST_CLK Subsample Clock (Rx symbol rate)

(5) SQ Test Mode

<7:0> Signal Quality (SQ) Phase Variance (8 most significant bits)

TEST_CLK Load Signal Quality Signal

(6) Bit Sync Test Mode 1

<7:0> Bit Sync Accum

TEST_CLK Internal RX Clock

(7) Bit Sync Test Mode 2

<7:0> SQ Bit Sync Reference Data (8 most significant bits)

TEST_CLK Load SQ Signal

(8) A/D Cal Test Mode

<7:7> Carrier Sense (CRS)

<6:6> Energy Detect (ED)

<5:5> Reserved

<4:0> A/D Calibrate

TEST_CLK (Internal RX Clock)

Threshold Settings

Received Signal Strength Indication (RSSI) CR19<5:0>

These control bits are used to specify the RSSI threshold for measuring and generating the energy detect (ED) signal. When RSSI exceeds this threshold, ED is declared.

Clear Channel Assessment Timer CR17<7:0>

This control register is used to configure the period of the time-out threshold of the CCA watchdog timer.

Clear Channel Assessment Cycle CR18<7:0>

This control register is used to configure how many times the CCA timer is allowed to reach its maximum count before it declares that the channel is clear (independent of the actual energy measured in the channel).

Enable 1/4 Chip Adjust During Acquisition/Data CR5<6:6>

This control bit is used to enable/disable 1/4 chip timing adjustments during acquisition or data. The default is 1/2 chip adjustments.

Receive Bit Synch Amplitude (Acquisition/Data) CR22<7:0> CR23<7:0>

These control registers are used to specify the bit synch amplitude quality threshold used for acquisition and for data. See typical values in the HSP3824 data sheet.The received signal must be above this programmable value to be declared valid.

Receive Phase Variance (Acquisition/Data) CR30<7:0> CR31<7:0>

These control registers are used to specify the phase variance quality threshold used for acquisition and for data. See typical values in the HSP3824 data sheet. The received signals phase variance has to be less than this programmable value to be declared as valid signal.

A/D Calibration

Reference Value CR1<1:1>

This control bit is used to select whether internal A/D calibration circuit is active or not and if not, sets the reference to mid-scale.

Last Value CR1<0:0>

This control bit is used to select whether internal A/D calibration circuit is held at its most recent value.

Positive Increment Adjust CR11<7:0>

This control register contains the value used for positive increments of the level adjusting circuit of the A/D reference. These positive increment steps define how fast the A/D will be driven to saturation.

Negative Increment Adjust CR12<7:0>

This control register contains the value used for negative increments of the level-adjusting circuit of the A/D reference. These negative increments define the back off step size from when the A/D reaches saturation.

Modem Status

Transmit Ready (TX_RDY) CR7<7:7>

This status bit indicates the status of the TX_RDY output pin. It is only used when the Preamble/Header is generated internally within the HSP3824.

Antenna CR7<6:6>

This status bit indicates the antenna selected by the device (status of the ANTSEL pin) during antenna diversity.

Clear Channel Assessment (CCA) CR7<5:5>

This status bit indicates the status of the Clear Channel Assessment output pin.

Carrier Sense (CRS) CR7<4:4>

This status bit indicates the status of Carrier Sense (or PN lock).

RSSI vs. Threshold CR7<3:3>

This status bit indicates whether the RSSI signal is above or below threshold (or energy detect (ED)).

MAC Data Ready (MD_RDY) CR7<2:2>

This status bit indicates the status of the MD_RDY output pin. It signals that a valid Preamble/Header has been received and that the next available bit on the RXD bus will be the first data packet bit.

Transmit Power Enable (TX_PE) CR7<1:1>

This status bit indicates whether the external device has acknowledged that the channel is clear for transmission (or status of the TX_PE pin).

Valid CRC16 CR7<0:0>

This status bit indicates whether a valid CRC16 has been calculated for the Header information. The CRC16 does not cover the preamble bits or the data packet.

Packet Status CR8<7:7>

This status bit indicates whether a valid packet has been received. This is meaningful only when the device operates under the full protocol (mode 3).

Start Frame Delimiter Search Timer CR8<6:6>

This status bit indicates the status of the SFD search timer.

Modulation Type CR8<5:5>

This status bit indicates the modulation type for the data packet. Preamble and Header data are always at 1MBPS.

Signal Status

TRANSMIT PREAMBLE INFORMATION

Service Field CR51<7:0>

This control register contains the value of the service field to be transmitted in a Header.

Length Field CR52<7:0> CR53<7:0>

These control registers contain the value of the length field to be transmitted. It indicates the number of bits transmitted in the data packet.

CRC16 Field CR54<7:0> CR55<7:0>

These status registers indicate the calculated CRC16 for the transmitted header.

RECEIVE PREAMBLE INFORMATION

Service Field CR44<7:0>

This status register contains the value of the service field received in a Header.

Length Field CR45<7:0> CR46<7:0>

These status registers contain the value of the length field of the received packet. It indicates the number of bits transmitted in the data packet.

CRC16 Field CR47<7:0> CR48<7:0>

These status registers indicate the received CRC16 for the received header.

SIGNAL FIELD

BPSK CR42<7:0>

This control register contains the 8-bit value indicating that the data packet modulation is DBPSK.

QPSK CR43<7:0>

This control register contains the 8-bit value indicating that the data packet modulation is DQPSK.

RECEIVE SIGNAL QUALITY INDICATORS

Bit Synch Amplitude Acquisition CR24<6:0> CR25<7:0>

These status registers contain the measured bit synch amplitude signal quality during acquisition.

Bit Synch Amplitude Data CR28<6:0> CR29<7:0>

These status registers contain the measured bit synch amplitude signal quality during data tracking.

Phase Variance Acquisition CR32<7:0> CR33<7:0>

These status registers contain the measured phase variance signal quality during acquisition.

Phase Variance Data CR36<7:0> CR37<7:0>

These status registers contain the measured phase variance signal quality during data tracking.

RSSI Value CR10<5:0>

These status bits contain the value of the RSSI analog input signal from the on-chip ADC. This register is updated at the chip rate divided by 11.

Receive Signal Quality for Best Antenna Dwell CR38<7:0>

This status register contains the bit synch amplitude signal quality measurement derived from the Bit Synch signal quality stored in the CR28-29 registers of the HSP3824. This value is the result of the signal quality measurement for the best antenna dwell in the antenna diversity mode.

DEFAULT CONFIGURATION

Table 1 contains a set of default configuration values that can be used for QPSK and BPJK modulation. These values can be initially used for systems test and then modified as appropriate, per each application. The default configuration table is followed by the detail description of all the available registers of the HSP3824.

TABLE 1. CONTROL REGISTER VALUES FOR SINGLE ANTENNA ACQUISITION

REGISTER	NAME	TYPE	REG ADDR IN HEX	QPSK	BPSK
CR0	MODEM CONFIG. REG A	R/W	00	3C	64
CR1	MODEM CONFIG. REG B	R/W	04	00	00
CR2	MODEM CONFIG. REG C	R/W	08	07	24
CR3	MODEM CONFIG. REG D	R/W	0C	04	07
CR4	INTERNAL TEST REGISTER A	R/W	10	00	00
CR5	INTERNAL TEST REGISTER B	R/W	14	00	00
CR6	INTERNAL TEST REGISTER C	R	18	X	X
CR7	MODEM STATUS REGISTER A	R	1C	X	X
CR8	MODEM STATUS REGISTER B	R	20	X	X
CR9	I/O DEFINITION REGISTER	R/W	24	00	00
CR10	RSSI VALUESTATUS REGISTER	R	28	X	X
CR11	ADC_CAL_POS REGISTER	R/W	2C	01	01
CR12	ADC_CAL_NEG REGISTER	R/W	30	FD	FD
CR13	TX_SPREAD SEQUENCE(HIGH)	R/W	34	05	05
CR14	TX_SPREAD SEQUENCE (LOW)	R/W	38	B8	B8
CR15	SCRAMBLE_SEED	R/W	3C	7F	7F
CR16	SCRAMBLE_TAP (RX AND TX)	R/W	40	48	48
CR17	CCA_TIMER_TH	R/W	44	2C	2C
CR18	CCA_CYCLE_TH	R/W	48	03	03
CR19	RSSI_TH	R/W	4C	1E	1E
CR20	RX_SPREAD SEQUENCE (HIGH)	R/W	50	05	05
CR21	RX_SREAD SEQUENCE (LOW)	R/W	54	B8	B8
CR22	RX_SQ1_ IN_ACQ (HIGH) THRESHOLD	R/W	58	01	01
CR23	RX-SQ1_ IN_ACQ (LOW) THRESHOLD	R/W	5C	E8	E8
CR24	RX-SQ1_ OUT_ACQ (HIGH) READ	R	60	X	X
CR25	RX-SQ1_ OUT_ACQ (LOW) READ	R	64	X	X
CR26	RX-SQ1_ IN_DATA (HIGH) THRESHOLD	R/W	68	0F	0F
CR27	RX-SQ1-SQ1_ IN_DATA (LOW) THRESHOLD	R/W	6C	FF	FF
CR28	RX-SQ1_ OUT_DATA (HIGH)READ	R	70	X	X
CR29	RX-SQ1_ OUT_DATA (LOW) READ	R	74	X	X
CR30	RX-SQ2_ IN_ACQ (HIGH) THRESHOLD	R/W	78	00	00

TABLE 1. CONTROL REGISTER VALUES FOR SINGLE ANTENNA ACQUISITION (Continued)

REGISTER	NAME	TYPE	REG ADDR IN HEX	QPSK	BPSK
CR31	RX-SQ2- IN-ACQ (LOW) THRESHOLD	R/W	7C	CA	CA
CR32	RX-SQ2_ OUT_ACQ (HIGH) READ	R	80	X	X
CR33	RX-SQ2_ OUT_ACQ (LOW) READ	R	84	X	X
CR34	RX-SQ2_IN_DATA (HIGH)THRESHOLD	R/W	88	09	09
CR35	RX-SQ2_ IN_DATA (LOW) THRESHOLD	R/W	8C	80	80
CR36	RX-SQ2_ OUT_DATA (HIGH) READ	R	90	X	X
CR37	RX-SQ2_ OUT_DATA (LOW) READ	R	94	X	X
CR38	RX_SQ_READ; FULL PROTOCOL	R	98	X	X
CR39	RESERVED	W	9C	00	00
CR40	RESERVED	W	A0	00	00
CR41	UW_Time Out_LENGTH	R/W	A4	90	90
CR42	SIG_DBPSK Field	R/W	A8	0A	0A
CR43	SIG_DQPSK Field	R/W	AC	14	14
CR44	RX_SER_Field	R	B0	X	X
CR45	RX_LEN Field (HIGH)	R	B4	X	X
CR46	RX_LEN Field (LOW)	R	B8	X	X
CR47	RX_CRC16 (HIGH)	R	BC	X	X
CR48	RX_CRC16 (LOW)	R	C0	X	X
CR49	UW -(HIGH)	R/W	C4	F3	F3
CR50	UW _(LOW)	R/W	C8	A0	A0
CR51	TX_SER_F	R/W	CC	00	00
CR52	TX_LEN (HIGH)	R/W	D0	FF	FF
CR53	TX_LEN(LOW)	R/W	D4	FF	FF
CR54	TX_CRC16 (HIGH)	R	D8	X	X
CR55	TX_CRC16 (LOW)	R	DC	X	X
CR56	TX_PREM_LEN	R/W	E0	80	80

Control Registers, Address and Bit Location Specification

The following tables describe the function of each control register along with the associated bits in each control register.

CONFIGURATION REGISTER 0 ADDRESS (0h) MODEM CONFIGURATION REGISTER A

Bit 7	This bit selects the transmit antenna, controlling the output ANT_SEL pin. It is only used in half duplex mode. (Bit 5 = 0) Logic 1 = Antenna A. Logic 0 = Antenna B.
Bit 6	In single antenna operation this bit is used as the output of the ANT_SEL pin. In dual antenna mode this bit is ignored. Logic 1 = Antenna A. Logic 0 = Antenna B.
Bit 5	This control bit is used to select between full duplex and half duplex operation. If set for full duplex operation, the ANT_SEL pin reflects the setting of CR0 bit 7 when TX_PE is active and reflects the receiver's choice when TX_PE is inactive. In full duplex operation, the ANT_SEL pin always reflects the receiver's choice antenna. Logic 1 = full duplex. Logic 0 = half duplex.
Bit 4, 3	These control bits are used to select one of the four input Preamble Header modes for transmitting data. The preamble and header are DBPSK for all modes of operation. Mode 0 is followed by DBPSK data. For modes 1-3, the data can be configured as either DBPSK or DQPSK. This is a "don't care" if the header is generated externally.

MODE	BIT 4	BIT 3	MODE DESCRIPTION
0	0	0	Preamble with SFD Field.
1	0	1	Preamble with SFD, and CRC16.
2	1	0	Preamble with SFD, Length, and CRC16.
3	1	1	Full preamble and header.

Bit 2	This control bit is used to enable the SFD (Start Frame Delimiter) timer. If the time is set and expires before the SFD has been detected, the HSP3824 will return to its acquisition mode. Logic 1: Enables the SFD timer to start counting once the PN acquisition has been achieved. Logic 0: Disables the SFD Timer.
Bit 1	This control bit enables counting the number of data bits per the length field embedded in the header. Only used in header modes 2 and 3. Then according to the count it returns the processor into its acquisition mode at the end of the count. If length field is 0000h, modem will reset at end of SFD regardless of this bit setting. Logic 1 = Enable Length Time Out. Logic 0 = Disabled.
Bit 0	Unused don't care.

CONFIGURATION REGISTER 1 ADDRESS (04h) MODEM CONFIGURATION REGISTER B

Bit 7	When active this bit maintains the RXCLK and TXLK rates constant for preamble and data transfers even if the data is modulated in DQPSK. This bit is used if the external processor can not accommodate rate changes. This is an active high signal. The rate used is the QPSK rate and the BPSK header bits are double clocked.
Bit 6, 5, 4, 3, 2	These control bits are used to define a binary count (N) from 0 - 31. This count is used to assert TX_RDY N - clocks (TXCLK) before the beginning of the first data bit. If this is set to zero, then the TX_RDY will be asserted immediately after the last bit of the Preamble Header.
Bit 1	When active the internal A/D calibration circuit sets the reference to mid-scale. When inactive then the calibration circuit adjusts the reference voltage in real time to optimize I, Q levels. Logic 1 = Reference set at mid-scale (fixed). Logic 0 = Real time reference adjustment.
Bit 0	When active the A/D calibration circuit is held at its last value. Logic 1 = Reference held at the most recent value. Logic 0 = Real time reference level adjustment.

CONFIGURATION REGISTER 2 ADDRESS (08h) MODEM CONFIGURATION REGISTER C

Bit 7, 6

These control bits are used to select the number of chips per symbol used in the I and Q paths of the receiver matched filter correlators (see table below).

CHIPS PER SYMBOL	BIT 7	BIT 6
11	0	0
13	0	1
15	1	0
16	1	1

Bit 5

This control bit is used to disable the CRC16 check. When this bit is set, the processor will accept the received packet and any packet error checks have to be detected externally. The HSP3824 will remain in the receive mode until either the carrier is lost or the network processor resets the device to the acquisition mode, or if, in modes 2 or 3, the length times out.
Logic 1 = Disable receiver error checks.
Logic 0 = Enable receiver checks.

Bit 4, 3

These control bits are used to select the divide ratio for the demodulators receive chip clock timing.The value of N is determined by the following equation:
Symbol Rate = MCLK/(N x Chips per symbol).

MASTER CLOCK/N	BIT 4	BIT 3
N = 2	0	0
N = 4	0	1
N = 8	1	0
N = 16	1	1

Bit 2

This control bit sets the receiver into single or dual antenna mode. The Preamble acquisition processing length and whether the modem scans antennas is controlled by this bit. If in single antenna mode, the ANT_SEL pin reflects CR0 bit 6 otherwise it reflects the receiver's choice of antenna.
Logic 0 = Acquisition processing is for dual antenna acquisition.
Logic 1 = Acquisition processing is for single antenna acquisition.

Bit 1, 0

These control bits are used to indicate one of the four Preamble Header modes for receiving data. Each of the modes includes different combinations of Header fields. Users can choose the mode with the fields that are more appropriate for their networking requirements. The Header fields that are combined to form the various modes are:

- SFD field
- CRC16 field
- Data length field (indicates the number of data bits that follow the Header information)
- Full protocol Header

INPUT MODE	BIT 1	BIT 0	RECEIVE PREAMBLE - HEADER FIELDS
0	0	0	Preamble, with SFD Field
1	0	1	Preamble, with SFD, CRC16
2	1	0	Preamble, with SFD Length, CRC16
3	1	1	Preamble, with Full Protocol Header

CONFIGURATION REGISTER 3 ADDRESS (0Ch) MODEM CONFIGURATION REGISTER D

Bit 7	Reserved (must set to "0").
Bit 6, 5	These control bits combined are used to select the number of chips per symbol used in the I and Q transmit paths (see table below).

CHIPS PER	BIT 6	BIT 5
11	0	0
13	0	1
15	1	0
16	1	1

Bit 4, 3	These control bits are used to select the divide ratio for the transmit chip clock timing. NOTE: The value of N is determined by the following equation: Symbol Rate = MCLK/(N x Chips per symbol)

MASTER	BIT 4	BIT 3
N = 2	0	0
N = 4	0	1
N = 8	1	0
N = 16	1	1

Bit 2	This control bit is used to select the origination of Preamble/Header information. Logic 1: The HSP3824 generates the Preamble and Header internally by formatting the programmed header information and generating a TX_RDY to indicate the beginning of the data packet. Logic 0: Accepts the Preamble/Header information from an externally generated source.
Bit 1	This control bit is used to indicate the signal modulation type for the transmitted data packet. When configured for mode 0 header, or mode 3 and external header, this bit is ignored. See Register 0 bits 4 and 3. Logic 1 = DBPSK modulation for data packet. Logic 0 = DQPSK modulation for data packet.
Bit 0	This control bit is used to indicate the signal modulation type for the received data packet Used only with header modes 1 and 2. See register 2-bits 1 and 0. Logic 1 = DBPSK. Logic 0 = DQPSK.

CONFIGURATION REGISTER 4 ADDRESS (10h) INTERNAL TEST REGISTER A

Bit 7 - 0	These control bits are used to direct various internal signals to test port output pins. These internal signals are monitored to fault isolate the device at manufacturing testing. During normal operation, the value 0h is recommended. This will result to the following signals becoming available at the output test pins of the device: Pin 46 (TEST7): Carrier Sense (CRS), a Logic 1 indicates PN lock. Pin 45 (TEST6): Energy Detect (ED), a Logic 1 indicates that there is energy detected in the channel. The ED goes active when the RSSI exceeds the threshold level programmed by the user. Pin 1 (TEST_CK): PN clock.

CONFIGURATION REGISTER 5 ADDRESS (14h,18h) INTERNAL TEST REGISTER B

Bits 7 - 0	These bits need to be programmed to 0h. They are used for manufacturing test only.

CONFIGURATION REGISTER 7 ADDRESS (1Ch) MODEM STATUS REGISTER A

Bit 7	This bit indicates the status of the TX_RDY output pin. TX_RDY is used only when the HSP3824 generates the Preamble/Header data internally. Logic 1: Indicates that the HSP3824 has completed transmitting Preamble header information and is ready to accept data from the external source (i.e. MAC) to transmit. Logic 0: Indicates that the HSP3824 is in the process of transmitting Preamble Header information.
Bit 6	This status bit indicates the antenna selected by the device. Logic 0: Antenna A is selected. Logic 1: Antenna B is selected.

CONFIGURATION REGISTER 7 ADDRESS (1Ch) MODEM STATUS REGISTER A (Continued)

Bit 5	This status bit indicates the present state of clear channel assessment (CCA) which is output pin 32. The CCA is being asserted as a result of a channel energy monitoring algorithm that is a function of RSSI, carrier sense, and time out counters that monitor the channel activity.
Bit 4	This status bit, when active indicates Carrier Sense, or PN lock. Logic 1: Carrier present. Logic 0: No Carrier Sense.
Bit 3	This status bit indicates whether the RSSI signal is above or below the programmed RSSI 6-bit threshold setting. This signal is referred as Energy Detect (ED). Logic 1: RSSI is above the programmed threshold setting. Logic 0: RSSI is below the programmed threshold setting.
Bit 2	This bit indicates the status of the output control pin MD_RDY (pin 34). It signals that a valid Preamble/Header has been received and that the next available bit on the TXD bus will be the first data packet bit. Logic 1: Envelopes the data packet as it becomes available on pin 3 (TXD). Logic 0: No data packet on TXD serial bus.
Bit 1	This status bit indicates whether the external device has acknowledged that the channel is clear for transmission. This is the same as the input signal TX_PE on pin 2. Logic 1 = Acknowledgment that channel is clear to transmit. Logic 0 = Channel is NOT clear to transmit.
Bit 0	This status bit indicates that a valid CRC16 has been calculated. The CRC16 is calculated on the Header information. The CRC16 does not cover the preamble bits. Logic 1 = Valid CRC16 check. Logic 0 = Invalid CRC16 check.

CONFIGURATION REGISTER 8 ADDRESS (20h) MODEM STATUS REGISTER B

Bit 7	This status bit is meaningful only when the device operates under the full protocol mode. Errors imply CRC errors of the header fields. Logic 0 = Valid packet received. Logic 1 = Errors in received packet.
Bit 6	This bit is used to indicate the status of the SFD search timer. The device monitors the incoming Header for the SFD. If the timer, times out the HSP3824 returns to its signal acquisition mode looking to detect the next Preamble and Header. Logic 1 = SFD not found, return to signal acquisition mode. Logic 0 = No time out during SFD search.
Bit 5	This status bit is used to indicate the modulation type for the data packet. This signal is generated by the header detection circuitry in the receive interface. Logic 0 = DBPSK. Logic 1 = DQPSK.
Bit 4	Unused, don't care.
Bit 3	Unused, don't care.
Bit 2	Unused, don't care.
Bit 1	Unused, don't care.
Bit 0	Unused, don't care.

CONFIGURATION REGISTER 9 ADDRESS (24h) I/O DEFINITION REGISTER

	This register is used to define the phase of clocks and other interface signals.
Bit 7	This bit needs to always be set to logic 0.
Bit 6	This control bit selects the active level of the MD_RDY output pin 34. Logic 1 = MD_RDY is active 0. Logic 0 = MD_RDY is active 1.

CONFIGURATION REGISTER 9 ADDRESS (24h) I/O DEFINITION REGISTER

Bit 5	This control bit selects the active level of the Clear Channel Assessment (CCA) output pin 32. Logic 1 = CCA active 1. Logic 0 = CCA active 0.
Bit 4	This control bit selects the active level of the Energy Detect (ED) output which is an output pin at the test port, pin 45. Logic 1 = ED active 0. Logic 0 = ED active 1.
Bit 3	This control bit selects the active level of the Carrier Sense (CRS) output pin which is an output pin at the test port, pin 46. Logic 1 = CRS active 0. Logic 0 = CRS active 1.
Bit 2	This control bit selects the active level of the transmit ready (TX_RDY) output pin 5. Logic 1 = TX_RDY active 0. Logic 0 = TX_RDY active 1.
Bit 1	This control bit selects the active level of the transmit enable (TX_PE) input pin 2. Logic 1 = TX_PE active 0. Logic 0 = TX_PE active 1.
Bit 0	This control bit selects the phase of the transmit output clock (TXCLK) pin 4. Logic 1 = Inverted TXCLK. Logic 0 = NON-Inverted TXCLK

CONFIGURATION REGISTER 10 ADDRESS (28h) RSSI VALUE REGISTER

Bits 0 - 7

This is a read only register reporting the value of the RSSI analog input signal from the on chip 6-bit ADC. This register is updated at (chip rate/11). Bits 7 and 6 are not used and set to Logic 0.
Example:

	BITS (0:7)	RANGE
RSSI_STAT	7 6 5 4 3 2 1 0	
	0 0 0 0 0 0 0 0	00h (Min)
	0 0 1 1 1 1 1 1	3Fh (Max)

CONFIGURATION REGISTER 11 ADDRESS (2ch) A/D CAL POS REGISTER

Bits 0 - 7	This 8-bit control register contains a binary value used for positive increment for the level adjusting circuit of the A/D reference. The larger the step the faster the level reaches saturation.

CONFIGURATION REGISTER 12 ADDRESS (30h) A/D CAL NEG REGISTER

Bits 0 - 7	This 8-bit control register contains a binary value used for the negative increment for the level adjusting reference of the A/D. The number is programmed as 256 - the value wanted since it is a negative number.

CONFIGURATION REGISTER 13 ADDRESS (34h) TX SPREAD SEQUENCE (HIGH)

Bits 0 - 7	This 8-bit register is programmed with the upper byte of the transmit spreading code. This code is used for both the I and Q signalling paths of the transmitter. This register combined with the lower byte TX_SPREAD(LOW) generates a transmit spreading code programmable up to 16-bits. Code lengths permitted are 11, 13, 15, and 16. Right justified MSB first.

CONFIGURATION REGISTER 14 ADDRESS (38h) TX SPREAD SEQUENCE (LOW)

Bits 0 - 7	This 8-bit register is programmed with the lower byte of the transmit spreading code. This code is used for the I and Q signalling paths of the transmitter. This register combined with the higher byte TX_SPREAD(HIGH) generates the transmit spreading code programmable up to 16-bits. The example below illustrates the bit positioning for one of the 11-bit Barker PN codes. Example: Transmit Spreading Code 11-Bit Barker Word Right Justified MSB First.

	MSB	LSB
TX_SPREAD(HIGH)	15 14 13 12 11 10 9 8	
TX_SPREAD(LOW)		7 6 5 4 3 2 1 0
11-bit Barker code	X X X X X 1 0 1	1 0 1 1 1 0 0 0

CONFIGURATION REGISTER 15 ADDRESS (3Ch) SCRAMBLER SEED

Bits 0 - 7	This register contains the 7-bit (seed) value for the transmit scrambler which is used to preset the transmit scrambler to a known starting state. The MSB bit position (7) is unused and must be programmed to a Logic 0. The example below illustrates the bit positioning of seed.

CONFIGURATION REGISTER 16 ADDRESS (40h) SCRAMBLER TAP

Bits 0 - 7	This register is used to configure the transmit scrambler with a 7-bit polynomial tap configuration. The transmit scrambler is a 7-bit shift register, with 7 configurable taps. A logic 1 is the respective bit position enables that particular tap. The MSB bit 7 is not used and it is set to a Logic 0. The example below illustrates the register configuration for the polynomial $F(x) = 1 + X^{-4}+X^{-7}$. Each clock is a shift left

		LSB
Bits (0:7)		7 6 5 4 3 2 1 0
		$XZ^{-7}Z^{-6}Z^{-5}Z^{-4}Z^{-3}Z^{-2}Z^{-1}$
Scrambler Taps	$F(x) = 1 + X^{-4}+X^{-7}$	0 1 0 0 1 0 0 0

CONFIGURATION REGISTER 17 ADDRESS (44h)CCA TIMER THRESHOLD

Bits 0 - 7	This 8-bit register is used to configure the period of the time-out threshold of the CCA watchdog timer. If the channel is busy the timer counts until it reaches the programmed value and at that point it declares that the channel is clear independent of the actual energy measured within the channel. This register is programmable up to 8-bits. $\text{Time (ms)} = 1000 \bullet \frac{N \bullet 5632}{\text{Chip Rate}}$, where N is the programmable value of CR17. For example, for a chip rate of 11 MCPS and a desired timeout of ~11ms, N = 2ch.

	LSB	
Bits (0:7)	7 6 5 4 3 2 1 0	
	0 0 0 0 0 0 1 0	02h (Min)
CCA_TIMER_TH	1 1 1 1 1 1 1 1	FFh (Max)

CONFIGURATION REGISTER 18 ADDRESS (48h) CCA CYCLE THRESHOLD

Bits 0 - 7	This 8-bit register is used to configure how many times the CCA timer is allowed to reach its maximum count before the channel is declared clear for transmission independent of the actual energy in the channel. This is an outer counter loop of the CCA timer. Each increment represents a time out of the CCA timer. Use a value of 03h for a time out of 2 CCA timer counts.

	MSB LSB	
Bits (0:7)	7 6 5 4 3 2 1 0	
	0 0 0 0 0 0 1 0	2h; 1 CCA timer (Min)
CCA_TIMER_TH	1 1 1 1 1 1 1 1	FFh; 256 CCA timer (Max)

CONFIGURATION REGISTER 19 ADDRESS (4Ch) RSSI THRESHOLD, ENERGY DETECT

Bits 0 - 7	This register contains the value for the RSSI threshold for measuring and generating energy detect (ED). When the RSSI exceeds the threshold ED is declared. ED indicates the presence of energy in the channel. The threshold that activates ED is programmable. Bits 7 an 6 of this register are not used and set to Logic 0.

	MSB LSB	
Bits (0:7)	7 6 5 4 3 2 1 0	
	0 0 0 0 0 0 0 0	00h (Min)
RSSI_STAT	0 0 1 1 1 1 1 1	3Fh (Max)

CONFIGURATION REGISTER 20 ADDRESS (50h) RX SPREAD SEQUENCE (HIGH)

Bits 0 - 7	This 8-bit register is programmed with the upper byte of the receive despreading code. This code is used for both the I and Q signalling paths of the receiver. This register combined with the lower byte RX_SPRED(LOW) generates a receive despreading code programmable up to 16-bits. Right justified MSB first. See address 13 and 14 for example.

CONFIGURATION REGISTER 21 ADDRESS (54h) RX SPREAD SEQUENCE (LOW)

Bits 0 - 7	This 8-bit register is programmed with the lower byte of the receiver despreading code. This code is used for both the I and Q signalling paths of the receiver. This register combined with the upper byte RX_SPRED(HIGH) generates a receive despreading code programmable up to 16-bits.

CONFIGURATION REGISTER 22 ADDRESS (58h) RX SIGNAL QUALITY 1 ACQ (HIGH) THRESHOLD

Bits 0 - 7	This control register contains the upper byte bits (8 - 14) of the bit sync amplitude signal quality threshold used for acquisition. This register combined with the lower byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements made during acquisition at each antenna dwell. This threshold comparison is added with the SQ2 threshold in registers 30 and 31 for acquisition. A lower value on this threshold will increase the probability of detection and the probability of false alarm. Set the threshold according to instructions in the text.

CONFIGURATION REGISTER 23 ADDRESS (5Ch) RX SIGNAL QUALITY 1 ACQ THRESHOLD (LOW)

Bits 0 - 7	This control register contains the lower byte bits (0 - 7) of the bit sync amplitude signal quality threshold used for acquisition. This register combined with the upper byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurement made during acquisition at each antenna dwell.

CONFIGURATION REGISTER 24 ADDRESS (60h) RX SIGNAL QUALITY 1 ACQ READ (HIGH)

Bits 0 - 7	This status register contains the upper byte bits (8 - 14) of the measured signal quality threshold for the bit sync amplitude used for acquisition. This register combined with the lower byte represents a 15-bit value, representing the measured bit sync amplitude. This measurement is made at each antenna dwell and is the result of the best antenna.

CONFIGURATION REGISTER 25 ADDRESS (64h) RX SIGNAL QUALITY 1 ACQ READ (LOW)

Bits 0 - 7	This register contains the lower byte bits (0 - 7) of the measured signal quality threshold for the bit sync amplitude used for acquisition. This register combined with the higher byte represents a 15-bit value, of the measured bit sync amplitude. This measurement is made at each antenna dwell and is the result of the best antenna.

CONFIGURATION REGISTER 26 ADDRESS (68h) RX SIGNAL QUALITY 1 DATA THRESHOLD (HIGH)

Bits 0 - 7	This control register contains the upper byte bits (8-14) of the bit sync amplitude signal quality threshold used for drop lock decisions. This register combined with the lower byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements, made every 128 symbols. These thresholds set the drop lock probability. A higher value will increase the probability of dropping lock.

CONFIGURATION REGISTER ADDRESS 27 (6Ch) RX SIGNAL QUALITY 1 DATA THRESHOLD (LOW)

Bits 0 - 7	This control register contains the lower byte bits (0 - 7) of the bit sync amplitude signal quality threshold used for drop lock decisions. This register combined with the upper byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements, made every 128 symbols.

CONFIGURATION REGISTER 28 ADDRESS (70h) RX SIGNAL QUALITY 1 DATA (high) THRESHOLD READ (HIGH)

Bits 0 - 7	This status register contains the upper byte bits (8-14) of the measured signal quality of bit sync amplitude used for drop lock decisions. This register combined with the lower byte represents a 15-bit value, representing the measured signal quality for the bit sync amplitude. This measurement is made every 128 symbols.

CONFIGURATION REGISTER 29 ADDRESS (74h) RX SIGNAL QUALITY 1 DATA THRESHOLD READ (LOW)

Bits 0 - 7	This register contains the lower byte bits (0-7) of the measured signal quality of bit sync amplitude used for drop lock decisions. This register combined with the lower byte represents a 16-bit value, representing the measured signal quality for the bit sync amplitude. This measurement is made every 128 symbols.

CONFIGURATION REGISTER 30 ADDRESS (78h) RX SIGNAL QUALITY 2 ACQ THRESHOLD (HIGH)

Bits 0 - 7	This control register contains the upper byte bits (8-15) of the carrier phase variance threshold used for acquisition. This register combined with the lower byte represents a 16-bit threshold value for carrier phase variance measurement made during acquisition at each antenna dwell and is based on the choice of the best antenna. This threshold is used with the bit sync threshold in registers 22 and 23 to declare acquisition. A higher value in this threshold will increase the probability of acquisition and false alarm.

CONFIGURATION REGISTER 31 ADDRESS (7Ch) RX SIGNAL QUALITY 2 ACQ THRESHOLD (LOW)

Bits 0 - 7	This control register contains the lower byte bits (0-7) of the carrier phase variance threshold used for acquisition.

CONFIGURATION REGISTER 33 ADDRESS (84h) RX SIGNAL QUALITY 2 ACQ READ (LOW)

Bits 0 - 7	This status register contains the lower byte bits (0-7) of the measured signal quality of the carrier phase variance used for acquisition. This register combined with the lower byte generates a 16-bit value, representing the measured signal quality of the carrier phase variance. This measurement is made during acquisition at each antenna dwell and is based on the selected best antenna

CONFIGURATION REGISTER 34 ADDRESS (88h) RX SIGNAL QUALITY 2 DATA THRESHOLD (HIGH)

Bits 0-7	This control register contains the upper byte bits (8-15) of the carrier phase variance threshold. This register combined with the lower byte represents a 16-bit threshold value for the carrier phase variance signal quality measurements made every 128 symbols.

CONFIGURATION REGISTER 35 ADDRESS (8Ch) RX SIGNAL QUALITY 2 DATA THRESHOLD (LOW)

Bits 0-7	This control register contains the lower byte bits (0-7) of the carrier phase variance threshold. This register combined with the upper byte) represents a 16-bit threshold value for the carrier phase variance signal quality measurements made every 128 symbols.

CONFIGURATION REGISTER 36 ADDRESS (90h) RX SIGNAL QUALITY 2 DATA READ (HIGH)

Bits 0-7	This status register contains the upper byte bits (8-15) of the measured signal quality of the carrier phase variance. This register combined with the lower byte represents a 16-bit value, of the measured carrier phase variance. This measurement is made every 128 symbols.

CONFIGURATION REGISTER 37 ADDRESS (94h) RX SIGNAL QUALITY 2 DATA READ (LOW)

Bits 0-7	This register contains the lower byte bits (0-7) of the measured signal quality of the carrier phase variance. This register combined with the represents a 16-bit value, of the measured carrier phase variance. This measurement is made every 128 symbols.

CONFIGURATION REGISTER ADDRESS 38 (98h) RX SIGNAL QUALITY 8-BIT READ

Bits 0 - 7	This 8-bit register contains the bit sync amplitude signal quality measurement derived from the 16-bit Bit Sync signal quality value stored in the CR28-29 registers. This value is the result of the signal quality measurement for the best antenna dwell. The signal quality measurement provides 256 levels of signal to noise measurement.

CONFIGURATION REGISTER 39 ADDRESS RESERVED

	Reserved

CONFIGURATION REGISTER 40 ADDRESS RESERVED

	Reserved

CONFIGURATION REGISTER 41 ADDRESS (A4h) SFD SEARCH TIME

Bits 0 - 7	This register is programmed with an 8-bit value which represents the length of time for the demodulator to search for a SFD in a receive Header. Each bit increment represents 1 symbol period.

CONFIGURATION REGISTER 42 ADDRESS (A8h) DSBPSK SIGNAL

Bits 0 - 7	This register contains an 8-bit value indicating the data packet modulation is DBPSK. This value will be a OAH for full protocol operation at a data rate of 1 MBPS, and is used in the transmitted Signalling Field of the header. This value will also be used for detecting the modulation type on the received Header.

CONFIGURATION REGISTER 43 ADDRESS (ACh) DQPSK SIGNAL

Bits 0 - 7	This register contains the 8-bit value indicating the data packet modulation is DQPSK. This value will be a 14h for full protocol operation at a data rate of 2 MBPS and is used in the transmitted Signalling Field of the header. This value will also be used for detecting the modulation type on the received header.

CONFIGURATION REGISTER 44 ADDRESS (B0h) RX SERVICE FIELD (RESERVED)

Bits 0 - 7	This register contains the detected received 8-bit value of the Service Field for the Header. This field is reserved for the full protocol mode for future use and should be always a 00h.

CONFIGURATION REGISTER 45 ADDRESS (B4h) RX DATA LENGTH (HIGH)

Bits 0 - 7	This register contains the detected higher byte (bits 8-15) of the received Length Field contained in the Header. This byte combined with the lower byte indicates the number of transmitted bits in the data packet.

CONFIGURATION REGISTER 46 ADDRESS (B8h) RX DATA LENGTH (LOW)

Bits 0 - 7	This register contains the detected lower byte of the received Length Field contained in the Header. This byte combined with the upper byte indicates the number of transmitted bits in the data packet.

CONFIGURATION REGISTER 47 ADDRESS (BCh) RX CRC16 (HIGH)

Bits 0 - 7	This register contains the upper byte bits (8 -15) of the received CRC16 field Header. This register combined with the lower byte represents a 16-bit CRC16 value protecting transmitted header. The fields protected are selected by configuring the header control bits at configuration register 2.

CONFIGURATION REGISTER 48 ADDRESS (C0h) RX CRC16 (LOW)

Bits 0 - 7

This register contains the lower byte bits (0-7) of the received CRC16 field Header. This register combined with the upper byte represents a 16-bit CRC16 value protecting transmitted header. The fields protected are selected by configuring the header control bits at configuration register 2.

	MSB LSB
RX_CRC16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RX_CRC16(HIGH)	7 6 5 4 3 2 1 0
RX_CRC16(LOW)	7 6 5 4 3 2 1 0

NOTE: The receive CRC16 Field protects the following fields depending upon the mode selection, as defined in configuration register 2.

Mode 0 CRC16 not used
Mode 1 CRC16 protects SFD
Mode 2 CRC16 protects SFD, and Length Field
Mode 3 CRC16 protects Signalling Field, Service Field, and Length Field

CONFIGURATION REGISTER 49 ADDRESS (C4h) SFD (HIGH)

Bits 0 - 7	This 8-bit register contains the upper byte bits (8-15) of the SFD used for both the Transmit and Receive header. This register combined with the lower byte represents the 16-bit value for the SFD field.

CONFIGURATION REGISTER 50 ADDRESS (C8h) SFD (LOW)

Bits 0 - 7	This 8-bit register contains the upper byte bits (0-7) of the SFD used for both the Transmit and Receive header. This register combined with the lower byte represents the 16-bit value for the SFD field.

CONFIGURATION REGISTER 51 ADDRESS (CCh) TX SERVICE FIELD

Bits 0 - 7	This 8-bit register is programmed with the 8-bit value of the Service Field to be transmitted in a Header. This field is reserved for future use and should be always a 00h.

CONFIGURATION REGISTER 52 ADDRESS (D0h) TX DATA LENGTH FIELD (HIGH)

Bits 0 - 7	This 8-bit register contains the higher byte (bits 8-15) of the transmit Length Field described in the Header. This byte combined with the lower byte indicates the number of bits to be transmitted in the data packet. CR 52/53 should not be set to 0000h. This value would cause the modem to reset after SFD.

CONFIGURATION REGISTER 53 ADDRESS (D4h) TX DATA LENGTH FIELD (LOW)

Bits 0 - 7	This 8-bit register contains the lower byte bits (0-7) of the transmit Length Field described in the Header. This byte combined with the higher byte indicates the number of bits to be transmitted in the data packet, including the MAC payload header. CR 52/53 should not be set to 0000h. This value would cause the modem to reset after SFD.

CONFIGURATION REGISTER 54 ADDRESS (D8h) TX CRC16 (HIGH)

Bits 0 - 7	This 8-bit register contains the upper byte (bits 8-15) of the transmitted CRC16 Field for the Header. This register combined with the lower byte represents a 16-bit CRC16 value calculated by the HSP3824 to protect the transmitted header. The fields protected are selected by configuring the header mode control bits at register address 02.

CONFIGURATION REGISTER 55 ADDRESS (DCh) TX CRC16 (LOW)

Bits 0 - 7	This 8-bit register contains the lower byte (bits 0-7) of the transmitted CRC16 Field for the Header. This register combined with the higher byte represents a 16-bit CRC16 value calculated by the HSP3824 to protect the transmitted header. The fields protected are selected by configuring the header mode control bits at register address 02.

configuration register 2

	MSB LSB
RX_CRC16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RX_CRC16(HIGH)	7 6 5 4 3 2 1 0
RX_CRC16(LOW)	7 6 5 4 3 2 1 0

NOTE: The receive CRC16 Field protects the following fields depending upon the mode selection. as defined in register address 02.

Mode 0 CRC16 not used
Mode 1 CRC16 protects SFD
Mode 2 CRC16 protects SFD, and Length Field
Mode 3 CRC16 protects Signalling Field, Service Field, and Length Field

CONFIGURATION REGISTER 56 ADDRESS (E0h) TX PREAMBLE LENGTH

Bits 0 - 7	This register contains the count for the Preamble length counter. This counter is programmable up to 8-bits and represents the number of preamble bits. This should be set at 50h for 1 antenna and 80h for dual antennas.

APPNOTE

No. AN9617.1 January 1997

Harris Wireless Products

Hardware/Software Interface Description for PRISM™ Radio Design with an Example Using the AM79C930 Media Access Controller

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Introduction

This document includes a description of the HW/SW interface for the IEEE802.11 target radio architecture based on the Harris PRISM™ chip set and the AMD Media Access Controller (MAC) AM79C930 processor. The information includes all the necessary interface requirements that can be used to control the PRISM radio with any other controller or processor that does not necessarily target IEEE802.11. The design example, though, addresses special design issues interfacing with the AM79C930.

Hardware Configuration

The block diagram in Figure 1 is intended to show a top level view of the basic hardware devices comprising the radio design. The detailed list of all signal interfaces required between MAC and the Physical Layer (PHY) or the PRISM radio are listed in Table 1 of this document.

List of Signals

Table 1 summarizes the signals that are required to control the PHY radio operations. The first column lists the PHY signal name, the second column indicates whether the signal is an output or an input to the MAC, the next column contains a brief description of each listed signal and the last two columns indicate the HW component part number and the pin connection for each of the listed signals at both the PHY and the MAC ends.

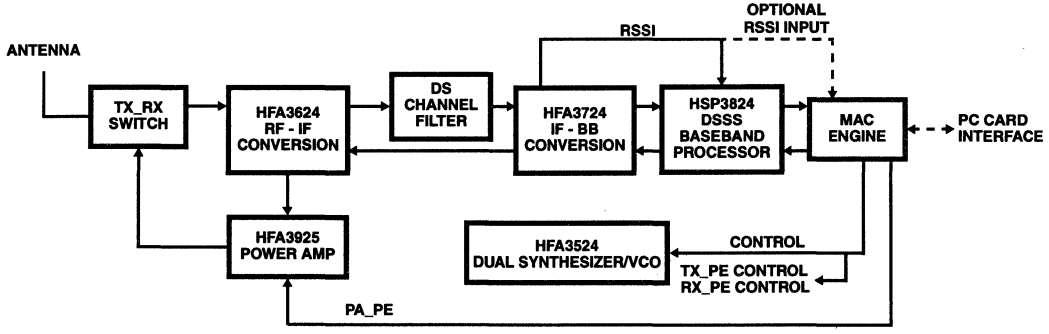

FIGURE 1. PRISM™ CHIPSET SYSTEM BLOCK DIAGRAM

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Summary List of MAC-PHY Interface Signals

TABLE 1. MAC-PHY INTERFACE SIGNALS

PHY SIGNAL NAME	I/O FROM/ TO MAC	DESCRIPTION	PHY PART/PIN NUMBER	MAC PIN NUMBER AM79C930
SYNTH_DATA	O	Serial Data Bus (Synthesizer)	HFA3524 (12)	MAC (102)
SYNTH_CLK	O	Serial Control Clock (Synthesizer)	HFA3524 (11)	MAC (101)
SYNTH_LE	O	Load Enable (Synthesizer)	HFA3524 (13)	MAC (3)
RX_PE	O	Receive Power Enable (RF/IF Converter)	HFA3624 (28)	MAC (126)
TX_PE	O	Transmit Power Enable (RF/IF Convt.)	HFA3624 (15)	MAC (142)
RX_PE	O	Receive Power Enable (Qmodem)	HFA3724 (21, 43, 54, 74)	MAC (126)
TX_PE	O	Transmit Power Enable (Qmodem)	HFA3724 (22, 41)	MAC (142)
SEL0	O	Low Pass Filter Control (Qmodem)	HFA3724 (17)	MAC (132)
SEL1	O	Low Pass Filter Control (Qmodem)	HFA3724 (16)	MAC (141)
TX_PE_BB	O	Transmit Power Enable (transmit port)	HSP3824 (2)	MAC (131)
TXD	O	Transmit Data (Transmit Port)	HSP3824 (3)	MAC (121)
TXCLK	I	Transmit Clock (Transmit Port)	HSP3824 (4)	MAC (115)
TX_RDY	I	Transmit Data Ready (Transmit Port)	HSP3824 (5)	MAC (91)
RX_PE_BB	O	Receiver Power Enable (Receive Port)	HSP3824 (33)	MAC (122)
MD_RDY	I	MAC Data Ready (Receive Port)	HSP3824 (34)	MAC (95)
RXD	I	Receive Data (Receive Port)	HSP3824 (35)	MAC (123)
RXCLK	I	Receive Clock (Receive Port)	HSP3824 (36)	MAC (124)
CS	O	Chip Select (Control Port)	HSP3824 (9)	MAC (107)
AS	O	Address Strobe (Control Port)	HSP3824 (23)	MAC (105)
R/W	O	Read/write Strobe (Control Port)	HSP3824 (8)	MAC (103)
SCLK	O	Serial Control Clock (Control Port)	HSP3824 (24)	MAC (101)
SDATA	I/O	Bi-directional Serial Data Bus (Cnt. Port)	HSP3824 (25)	MAC (102)
CCA	I	Clear Channel Assessment	HSP3824 (32)	MAC (96)
RESET	O	Master Reset	HSP3824 (28)	MAC (118)
PA_PE	O	Transmit Amplifier Power Enable (RFPA)	HFA3925 (11,18, 23)	MAC (131)
OSC_START	O	VCO Enable Circuit	VCO Startup Circuit	MAC(92)
RADIO_PE	O	Radio Power Enable.	RADIO	MAC (2)

Interface Signal Description

Table 2 Consists of a functional description for each of the PHY signals that are part of the HW/SW interface.

TABLE 2. MAC-PHY INTERFACE SIGNALS

SIGNAL NAME	SIGNAL DESCRIPTION
SYNTH_DATA	Binary serial data input used to configure the PHY RF frequency synthesizer (HFA3524). Data is entered MSB first. A single data transfer is 22-bits wide. This is a high impedance CMOS input to the PHY.
SYNTH_CLK	This is the clock for the SYNTH_DATA. The data is clocked in the appropriate synthesizer register on the rising edge of SYNTH_CLK. This is a high impedance CMOS input to the PHY.
SYNTH_LE	Load enable for the PHY RF frequency synthesizer (HFA3524). When signal goes active (High), data stored in the shift register is loaded in one of the 4 synthesizer operational registers as defined by the control bits which are the two LSBs of the SYNTH_DATA.
SEL0, SEL1	Digital control input to the PHY. Selects four programmed cut off frequencies for both receive and transmit channels of the analog baseband LPF. Tuning speed from one cutoff to another is less than 1ms. For IEEE802.11 the 8.8MHz cutoff frequency is used. SEL1 SEL0 Cutoff Frequency — SEL1 SEL0 Cutoff Frequency LO LO 2.2MHz — HI LO 8.8MHz LO HI 4.4MHz — HI HI 17.6MHz
TX_PE	Transmit Channel Power Enable Control Input. TTL compatible input. Enable logic level is High. This signal controls several IF/RF components of the PHY transmit chain. It is driving a total of 3 PHY inputs of the PHY components HFA3634 and HFA3724.
RX_PE	Receive Channel Power Control Input. TTL compatible input. Enable logic level is High.This signal controls several IF/RF componets of the PHY. It is driving a total of 5 PHY inputs of the PHY components HFA3624 and HFA3724.
TX_PE_BB	TX_PE_BB is an input from the Media Access Controller (MAC). The rising edge of TX_PE_BB will start the internal transmit state machine of the PHY digital modem and the falling edge will inhibit the state machine. TX_PE _BB en velopes the transmit data.
TXD	TXD is an input, used to transfer serial Data or Preamble/Header information bits from the MAC to the PHY digital modem (HSP3824). The data is received serially with the LSB first. The data is clocked in the HSP3824 at the falling edge of TXCLK.
TXCLK	TXCLK is a clock output used to receive the data on the TXD from the MAC to the PHY digital modem (HSP3824), synchronously. Transmit data on the TXD bus is clocked into the PHY on the falling edge.
TX_RDY	When the HSP3824 is configured to generate the Preamble and Header information internally, TX_RDY is an output to the external network processor indicating that Preamble and Header information has been generated and that the HSP3824 is ready to receive the data packet from the network processor over the TXD serial bus. TX_RDY returns to the inactive state when TX_PE goes inactive indicating the end of the data transmission. TX_RDY is an active high signal. This signal is meaningful only when the HSP3824 generates its own Preamble.
CCA	Clear Channel Assessment (CCA) is an output used to signal that the channel is clear to transmit. The CCA algorithm is user programmable and makes its decision as a function of RSSI, Energy detect (ED), Carrier Sense (CRS) and the CCA watch dog timer. The CCA algorithm and its programmable features are described in the data sheet of the HSP3824 PHY component. Logic 0 = Channel is clear to transmit. Logic 1 = Channel is NOT clear to transmit (busy). NOTE: This polarity is programmable and can be inverted.
RXD	RXD is an output to the MAC transferring demodulated Header information and data in a serial format. The data is sent serially with the LSB first. The data is frame aligned with MD-RDY.
RXCLK	RXCLK is the output bit clock to the MAC. This clock is used to transfer Header information and data through the RXD serial bus to the MAC. This clock reflects the bit rate in use. RXCLK will be held to a logic "0" state during the acquisition process of the PHY. RXCLK becomes active when the PHY enters in the data demodulation mode, im mediately following signal acquisition. This occurs once bit sync is declared and a valid signal quality estimate is made, when comparing the programmed signal quality thresholds.
MD_RDY	MD_RDY is an output signal to the MAC, indicating a data packet is ready to be transferred to the MAC. MD_RDY is an active high signal and it envelopes the data transfer to the MAC over the RXD serial bus. MD_RDY returns to its inactive state when there is no more receiver data, when the programmable data length counter reaches its value or when the link has been interrupted. MD_RDY remains inactive during preamble synchronization. MD_RDY can be programmed to become active after the SFD detection in the protocol or after the CRC check field in the Header.

TABLE 2. MAC-PHY INTERFACE SIGNALS (Continued)

SIGNAL NAME	SIGNAL DESCRIPTION
RX_PE_BB	When active, digital modem receiver of the PHY is configured to be operational, otherwise the digital modem receiver (HSP3824) is in standby mode. This is an active high input signal.
SD	SD is a serial bi-directional data bus which is used to transfer address and data to/from the internal registers of the PHY digital modem. The bit ordering of an 8-bit word is MSB first. The first 8-bits during transfers indicate the register address immediately followed by 8 more bits representing the data that needs to be written or read from that register.
SCLK	SCLK is the clock for the SD serial bus of the PHY digital modem. The data on SD is clocked at the rising edge. SCLK is an input clock to the PHY digital modem (HSP3824). The maximum rate of this clock is 10MHz.
AS	AS is an address strobe used to envelope the Address or the data on SD of the PHY digital modem. This is an input signal to the PHY digital modem (HSP3824) Logic 1 = envelopes the address bits. Logic 0 = envelopes the data bits.
R/W	R/W is an input to the PHY digital modem (HSP3824) used to change the direction of the SD bus when reading or writing data on the SD bus. R/W must be set up prior to the rising edge of SCLK. A high level indicates read while a low level is a write.
CS	CS is a chip select for the PHY digital modem to activate the serial control port. This is an input signal to the PHY. The CS doesn't impact any of the other interface ports and signals, i.e., the TX or RX ports and interface signals. This is an active low signal. When inactive SD, SCLK, AS and R/W become "don't care" signals.
RESET	Master reset for the PHY digital modem (HSP3824). When active, TX and RX functions are disabled. If RESET is kept low the HSP3824 goes into the power standby mode. RESET does not alter any of the configuration register values nor does it preset any of the registers into default values. The device requires programming upon power-up. RESET can be either active or inactive during programming of the device.
PA_PE	Enable for the PHY RF power amplifier (HFA3925) to start transmission. This is a digital interface. A Logic "1" enables the transmission.
OSC_START	Enable for the VCO Startup Circuit. A low going pulse of 200 ±10µs is required to activate the VCO after programming the synthesizer.
RADIO_PE	Enable for power regulators and clocks driving the PHY. A logic "1" enables operation, a logic "0" puts the complete PHY in a power down mode.

HW/SW Interfaces

There are four primary HW/SW interfaces that are used for configuration and during normal operation of the device. The interfaces are power on initialization, transmit mode operation, receive mode operation and power shut down mode. These interfaces are summarized as follows

- The **Initialization & Control Interface,** which is used to configure, write and/or read the status of the physical layer digital modem and the RF synthesizer. This interface is required to configure the programmable portions of the PHY during power up and coming out of certain power down modes. This interface is also used during operations for real time reconfiguration of PHY parameters and / or for reading PHY status.
- The **TX Interface**, which is used to control the transmit data transfers between the MAC and the physical layer. It is also used to control all PHY devices for the transmit chain of the radio.
- The **RX Interface**, which is used to control the receive data transfers between the MAC and the physical layer. It is also used to control all PHY devices for the receive chain of the radio.
- The **Power Down Interface,** which is used to set the physical layer into one of three power savings modes.

INITIALIZATION & CONTROL INTERFACE

This HW/SW interface is used to configure and monitor the programmable registers of the PHY. There are two PHY devices that contain programmable registers:

- The digital modem
- The RF frequency synthesizer. This interface is required to configure the PHY radio upon power up initialization and to monitor status during normal operation. This interface is also used to select or switch the frequency channel as required for the transmit and receive operations.

Digital Modem Interface

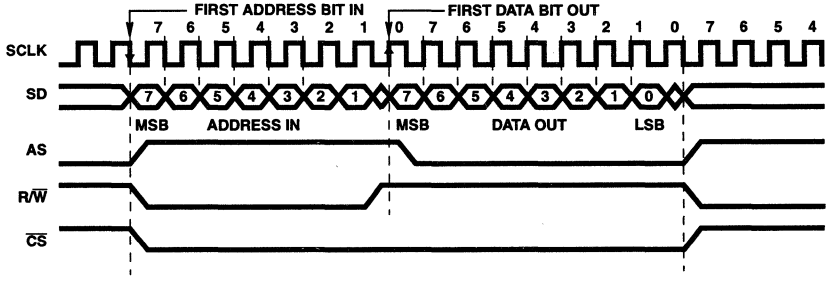
The signals necessary to accomplish the functions of this interface are:

CS: Chip select
AS: Address strobe
R/W: Read / Write strobe
SD: Serial Data.
SCLK: Serial Data Clock.

This HW/SW interface is required to configure the digital modem registers and performs all read and write operations to and from the digital modem. The serial control interface is used to serially write and read data to/from the digital

modem. This serial interface can operate up to a 10MHz rate or the maximum sampling clock rate of the PHY (whichever is lower). The sampling or master clock of the physical layer is designated as MCLK and must be running during programming. This interface is used to program and to read all internal registers. The first 8-bits always represent the address followed immediately by the 8 data bits for that register. The serial transfers are accomplished through the serial data signal (SD). SD is a bi-directional serial data bus. An Address Strobe (AS), Chip Select (CS), and Read/Write (R/W) are also required as handshake signals for this interface. The clock used in conjunction with the address and data on SD is SCLK. This clock is provided to the PHY. The timing relationships of these signals are illustrated in Figure 2. AS is active high during the clocking of the address bits. R/W is high when data is to be read, and low when it is to be written. CS must be active (low) during the entire data transfer cycle. CS selects the device. The serial control interface operates asynchronously from the TX and RX interfaces and can accomplish data transfers independent of the activity at the other digital or analog interfaces. CS does not effect the TX or RX operation of the device; impacting only the operation of the Control interface.

CONTROL PORT READ TIMING



CONTROL PORT WRITE TIMING

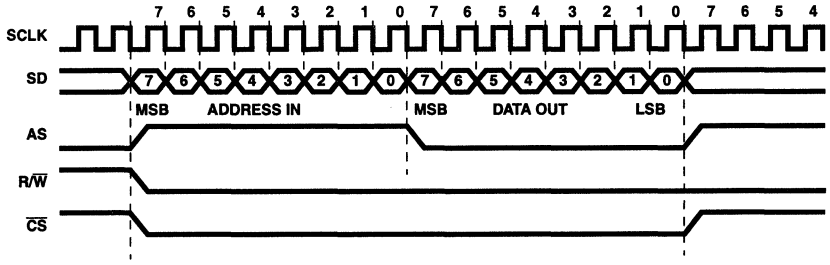


FIGURE 2. DIGITAL MODEM CONTROL INTERFACE

PHY Modem Configuration

The PHY modem has 57 internal registers that can be configured through the control interface. These registers are listed in Table 3 below. The table lists the configuration register number, a brief name describing the register, and the HEX address to access each of the registers. The type indicates whether the corresponding register is Read only (R) or Read/Write (R/W). Some registers are two bytes wide as indicated on the table (high & low bytes). Table 3 indicates the proper modem register configuration to implement the IEEE802.11 requirements as of the JULY 95 proposed draft.

TABLE 3. CONFIGURATION AND CONTROL PHY REGISTER LIST

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX	REGISTER DATA HEX
CR0	MODEM CONFIG. REG #1	R/W	00	1E
CR1	MODEM CONFIG. REG #2	R/W	04	82
CR2	MODEM CONFIG. REG #3 ytd	R/W	08	23
CR3	MODEM CONFIG. REG #4	R/W	0C	03
CR4	INTERNAL TEST REGISTER #1	R/W	10	00
CR5	INTERNAL TEST REGISTER #2	R/W	14	00

TABLE 3. CONFIGURATION AND CONTROL PHY REGISTER LIST (Continued)

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX	REGISTER DATA HEX
CR6	INTERNAL TEST REGISTER #3	R	18	-
CR7	MODEM STATUS REGISTER #1	R	1C	-
CR8	MODEM STATUS REGISTER #2	R	20	-
CR9	I/O DEFINITION REGISTER	R/W	24	00
CR10	RSSI VALUE REGISTER	R	28	-
CR11	ADC_CAL_POS REGISTER	R/W	2C	01
CR12	ADC_CAL_NEG REGISTER	R/W	30	FD
CR13	TX_SPREAD SEQUENCE (HIGH)	R/W	34	05
CR14	TX_SPREAD SEQUENCE (LOW)	R/W	38	B8
CR15	SCRAMBLE_SEED	R/W	3C	7F
CR16	SCRAMBLE_TAP (RX & TX)	R/W	40	48
CR17	CCA_TIMER_TH	R/W	44	2C
CR18	CCA_CYCLE_TH	R/W	48	03
CR19	RSSI_TH	R/W	4C	1E
CR20	RX_SPREAD SEQUENCE (HIGH)	R/W	50	05
CR21	RX_SPREAD SEQUENCE (LOW)	R/W	54	B8
CR22	RX_SQ1_ACQ (HIGH) THRESHOLD	R/W	58	01
CR23	RX_SQ1_ACQ (LOW) THRESHOLD	R/W	5C	E8
CR24	RX_SQ1_ACQ (HIGH) READ	R	60	-
CR25	RX_SQ1_ACQ (LOW) READ	R	64	-
CR26	RX_SQ1_DATA (HIGH) THRESHOLD	R/W	68	00
CR27	RX_SQ1_DATA (LOW) THRESHOLD	R/W 6C	00	
CR28	RX_SQ1_DATA (HIGH) READ	R	70	-
CR29	RX_SQ1_DATA (LOW) READ	R	74	-
CR30	RX_SQ2_ACQ (HIGH) THRESHOLD	R/W	78	00
CR31	RX_SQ2_ACQ (LOW) THRESHOLD	R/W	7C	CA
CR32	RX_SQ2_ACQ (HIGH) READ	R	80	-
CR33	RX_SQ2_ACQ (LOW) READ	R	84	-
CR34	RX_SQ2_DATA (HIGH) THRESHOLD	R/W	88	FF
CR35	RX_SQ2_DATA (LOW) THRESHOLD	R/W	8C	FF
CR36	RX_SQ2_DATA (HIGH) READ	R	90	-
CR37	RX_SQ2_DATA (LOW) READ	R	94	-
CR38	RX_SQ_READ FULL PROTOCOL	R	98	-
CR39	RESERVED	W	9C	00
CR40	RESERVED	W	A0	00
CR41	UW_TIME_OUT_LENGTH	R/W	A4	90
CR42	SIG_DBPSK FIELD	R/W	A8	0A
CR43	SIG_DQPSK FIELD	R/W	AC	14

TABLE 3. CONFIGURATION AND CONTROL PHY REGISTER LIST (Continued)

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX	REGISTER DATA HEX
CR44	RX_SER_FIELD	R	B0	-
CR45	RX_LEN FIELD (HIGH)	R	B4	-
CR46	RX_LEN FIELD (LOW)	R	B8	-
CR47	RX_CRC16 (HIGH)	R	BC	-
CR48	RX_CRC16 (LOW)	R	C0	-
CR49	UW (HIGH)	R/W	C4	F3
CR50	UW (LOW)	R/W	C8	A0
CR51	TX_SER_F	R/W	CC	00
CR52	TX_LEN (HIGH)	R	D0	-
CR53	TX_LEN (LOW)	R	D4	-
CR54	TX_CRC16 (HIGH)	R	D8	-
CR55	TX_CRC16 (LOW)	R	DC	-
CR56	TX_PREM_LEN	R/W	E0	80

Synthesizer Interface

The following signals are required to accomplish the functions of this interface:

Synth_Data: Serial Synthesizer Data
Synth_Clk: Synthesizer Data Clock
Synth_LE: Synthesizer Load Enable

These signals are utilized to configure the RF frequency synthesizer. The synthesizer tunes the radio to the appropriate receive and transmit channels. Figure 3 illustrates the required timing to write the appropriate frequency to the PHY synthesizer.

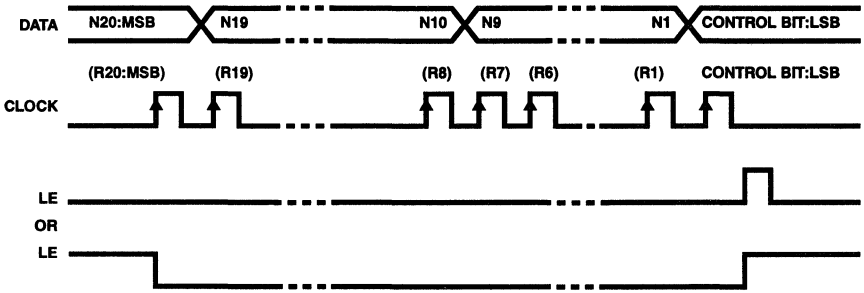


FIGURE 3. SYNTHESIZER SERIAL DATA INTERFACE

The following Data patterns are required to initialize the PHY synthesizer for IEEE802.11 operation. It should be noted that the register order is important with IF R first followed by IF N, RF R, and RF N. Also note that when powering up or coming out of Power Down Mode #2 (see page 10). The 4 registers should be written to twice. This is because the device RF and IF sections should be enabled before configuring the R and N pairs; and this effectively occurs if the values below are written twice in the IF R, IF N, RF R, RF N order. Also note that the OSC_START signal must follow any synthesizer programming cycle.

```
SYNTH_DATA  16,1801h    ;IF R Counter register
SYNTH_DATA  6, 60h       initialization.
SYNTH_DATA  16,4118h    ;IF N Counter register
SYNTH_DATA  6,04h        initialization.
SYNTH_DATA  16,1801h    ;RF R Counter register
SYNTH_DATA  6,68h        initialization.
```

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The Harris_Freq_Table holds the 22-bit values for the synthesizer RF N Counter control register. Each entry is comprised of three bytes. Eight bits of the first byte is serially shifted out to the synthesizer (MSBit first), followed by 8-bits of the second byte (MSBit first), followed finally by the 6 MSBits of the third byte (MSBit first). The two LSBits of the third byte in each entry are ignored. The synthesizer configuration for each of the 12 IEEE802.11 channels is shown below.

```
Harris_Freq_Table   label byte
        db          02h, 011h, 04Ch     ;Channel 1
        db          02h, 011h, 09Ch     ;Channel 2
        db          02h, 011h, 0ECh     ;Channel 3
        db          02h, 018h, 03Ch     ;Channel 4
        db          02h, 018h, 08Ch     ;Channel 5
        db          02h, 018h, 0DCh     ;Channel 6
        db          02h, 019h, 02Ch     ;Channel 7
        db          02h, 019h, 07Ch     ;Channel 8
        db          02h, 019h, 0CCh     ;Channel 9
        db          02h, 020h, 01Ch     ;Channel 10
        db          02h, 020h, 06Ch     ;Channel 11
        db          02h, 021h, 0CCh     ;Channel 12
```

TX INTERFACE

The signals required for the control of the transmit functions of the radio are:

- TX_PE_BB: Transmit power enable for digital modem
- TXD: Transmit digital data
- TXCLK: Transmit data clock
- TX_RDY: Transmit data ready
- TX_PE: Transmit power enable for RF and IF sections
- PA_PE: Power amplifier transmit enable
- SEL 0,1: Selection of appropriate baseband LPF
- CCA: Clear channel assessment indicator from PHY

To initiate the transmit operation the MAC generates TX_PE. The Preamble and Header are then generated by the PHY. Finally, when cued, the MAC delivers the data packet to the PHY for transmission. The transmit data digital interface transfers the data that needs to be transmitted serially to the PHY. The data is modulated and transmitted as soon as it is received from the MAC. The serial digital data is input to the PHY through TXD using the falling edge of TXCLK to clock it in the PHY. TXCLK is an output from the PHY. A timing diagram of the transmit signal sequence is shown on Figure 4.

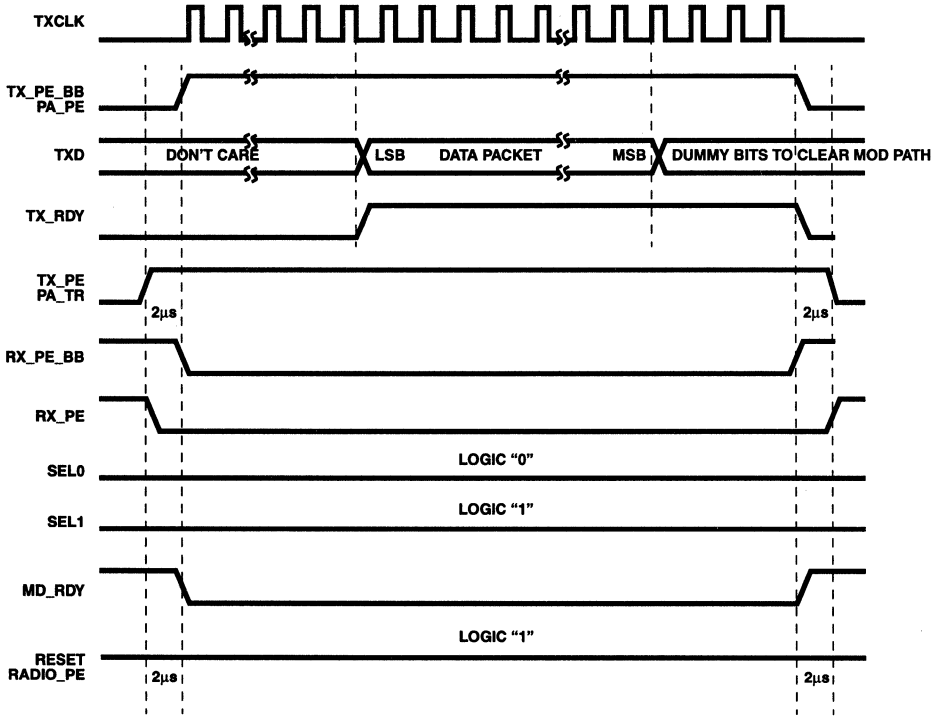


FIGURE 4. TRANSMIT TIMING DIAGRAM

The preamble and PHY header transmission is always at a 1Mbps (BPSK) data rate. The MAC header and data that follows can be either at 1Mbps (BPSK) or at 2Mbps (QPSK). To avoid rate switching within any single transmission between the MAC-PHY interface, the TXCLK will always be at the higher rate of 2Mbps. This implies that each of the BPSK symbols needs to be coming into the PHY twice. The MAC needs to send the same BPSK symbol twice at a rate of 2Mbps and this action will make it equivalent to the required BPSK symbol rate of 1Mbps. If QPSK data bits follow the PHY header, they will be sent from the MAC to the PHY only once at the 2Mbps rate.

The MAC initiates the transmit sequence by asserting TX_PE. Then TX_PE_BB envelopes the transmit data packet on TXD. The PHY responds by generating TXCLK to input the serial data on TXD. TXCLK will run until TX_PE_BB goes back to its inactive state indicating the end of the data packet. In addition Figure 4 illustrates the state of the PHY receive signals while transmitting as well as, the power enable, reset, and filter select proper signal states.

The PHY supports two possible data transfer scenarios, one where the preamble and header fields are generated within the PHY and one where the MAC generates the preamble and header fields. The scenario described herein assumes that the PHY generates the preamble and PHY header.

During this mode the PHY will immediately start transmitting the preamble and header as internally generated. Data available on TXD upon assertion of TX_PE_BB would be ignored. When the internally generated preamble and header are finished the PHY asserts TX_RDY. This signals the MAC to begin sending the data packet. TX_RDY assertion timing is programmable via Configuration Register (CR) 1. The timing diagram of this TX scenario, where the preamble and header are generated internal to the PHY, is illustrated on Figure 4.

One other signal that can be used to assist MAC transmit decisions as part of the TX interface is the Clear Channel Assessment (CCA) signal which is an output from the PHY. The CCA provides the indication that the channel is clear of energy and the transmission will not be subject to collisions. CCA can be monitored by the MAC to assist in deciding when to initiate transmissions. The CCA indication can be bypassed or ignored by the MAC without impacting any of the physical layer operations. The state of the CCA does not effect the transmit operation of the PHY. TX_PE and TX_PE_BB will always initiate the transmit state independent of the state of CCA. The CCA timing is not shown in the timing diagram of Figure 4 since it is an optional signal and does not influence the PHY transmit operations.

Signals TX_RDY, TX_PE_BB and TXCLK can be set individually, by programming CR9, as either active high or active low signals.

To avoid increasing throughput delays it is critical that the timing of TX_PE and RX_PE are as close to complementary of each other as possible.

When first attempting to transmit upon power-up, PA_PE must stay low for at least 10ms after RADIO_PE goes high.

RX INTERFACE

The signals that control the receive functions of the radio are:

- RX_PE_BB: Receive power enable for digital PHY modem
- MD_RDY: MAC data ready, enveloping the MAC data packet from the PHY
- RXD: Receive serial baseband data to the MAC
- RXCLK: Receive data clock to the MAC
- RX_PE: Receive power enable for the RF and IF section of the PHY radio
- SEL 0,1: Receive LPF frequency select

Timing diagram, Figure 5 illustrates the relationships between the various signals required to control the PHY during the receive operations.

The receive data interface of the PHY digital modem (RXD) serially outputs the demodulated data to the MAC. The data is output as soon as it is demodulated by the PHY. RX_PE and RX_PE_BB must be at their active state throughout the receive operation. When RX_PE, RX_PE_BB are inactive the PHY receive functions, including acquisition,. will be in a stand by mode. The timing relationships between RX_PE and RX_PE_BB, as well as, the state of the transmit signals, power enable signals, reset and filter select signal states are illustrated on Figure 5 for the receive operation during the reception of a single packet.

RXCLK is an output from the PHY and is the clock for the serial demodulated data on RXD. MD_RDY is an output from the PHY and it envelopes the valid data on RXD. MD_RDY is programmable and is asserted either after the Start Frame Delimiter field has been detected or immediately after the CRC field of the header has been checked. MD_RDY is programmed through CR3, bit-7 to select when it will be asserted. The PHY may also be programmed to ignore error detection during the CRC check of the header fields. If programmed to ignore errors the device continues to output the demodulated data in its entirety regardless of the CRC check result. This option is programmed through CR2, bit-5.

The preamble and PHY header are always received at a 1Mbps (BPSK) data rate. The MAC header and data that follows can be either at 1 Mbps (BPSK) or at 2 Mbps (QPSK). To avoid rate switching within any single packet reception between the MAC-PHY interface, the RXCLK will always be at the higher rate of 2 Mbps. This implies that each of the BPSK symbols is coming out of the PHY twice. The PHY sends to the MAC the same BPSK symbol twice at a rate of 2 Mbps and this action will make it equivalent to the required BPSK symbol rate of 1Mbps. If QPSK data bits follow the PHY header, they will be sent to the MAC from the PHY only once at the 2 Mbps rate.

If rate switching is not an issue for the controller (MAC) then the HSP3824 can be configured to rate switch within the packet. The HSP3824 can automatically switch from BPSK to the QPSK rate at the appropriate time.

Note that RXCLK and RXD become active after acquisition, well before MD_RDY is asserted. MD_RDY returns to its inactive state under the following conditions:

- The number of data symbols, as defined by the length field in the protocol, has been received and output through RXD in its entirety (normal condition).
- PN tracking is lost during demodulation.
- RX_PE_BB is deactivated by the MAC.

MD_RDY can be configured through CR9, bit-6 to be active low, or active high.

To avoid increasing throughput delays it is critical that the timing of TX_PE and RX_PE are as close to complementary of each other as possible.

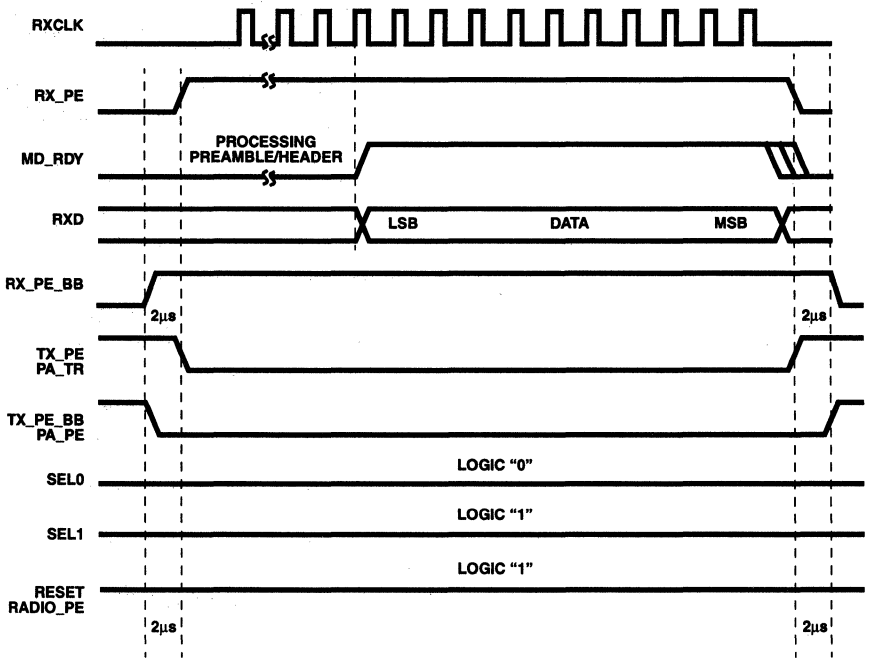


FIGURE 5. RECEIVE TIMING DIAGRAM

POWER DOWN MODES

The power consumption modes of the PHY are controlled by the following control signals:

- Receiver Power Enable (RX_PE & RX_PE_BB), which disable the radio receiver when inactive.
- Transmitter Power Enable (TX_PE & TX_PE_BB & PA_PE), which disable the radio transmitter when inactive.
- Reset (RESET), which puts the digital receiver in a sleep mode when it is asserted at least 2 MCLK's after RX_PE is set at its inactive state.
- RADIO_PE, which disables power regulators and all digital clocks to the PHY.
- In addition the radio RF synthesizer is programmable and can be set at a maximum power savings mode.

Utilizing the availability of the signals above there are three power savings modes defined:

- Power Down mode #1: During this mode the current consumption of the radio is estimated at 38mA. The radio can not receive or transmit when configured for this mode. When in this mode, it takes 25µs. to return the radio in its operational mode. when set in this mode, the PHY maintains its configuration data. There is no need to reprogram any of the radio register values. To activate Power Down mode #1 the following signals need to be set at the states shown below:

RX_PE: LOW
RX_PE_BB: LOW
TX_PE: LOW
TX_PE_BB: LOW
PA_PE: LOW
RESET: LOW
RADIO_PE: HIGH

- Power Down mode #2: During this mode the current consumption of the radio is estimated at 23mA. The radio cannot receive or transmit when configured for this mode. When in this mode, it takes 2ms. to return the radio in its operational mode. During this mode the synthesizer is programmed into its power savings mode. When set at this mode, the PHY maintains its configuration data. There is no need to reprogram any of the radio register values. However, the Synthesizer needs to be reprogrammed according to Synthesizer Interface Section on page 7.

To activate Power Down mode #2 the following signals need to be set as shown below:

RX_PE: LOW
RX_PE_BB: LOW
TX_PE: LOW
TX_PE_BB: LOW
PA_PE: LOW
RESET: LOW
RADIO_PE: HIGH

In addition the Synthesizer needs to be programmed via the synthesizer configuration interface as shown below:

```
SYNTH_DATA  16,1801h    ;IF R Counter register
SYNTH_DATA  6,0h          initialization.

SYNTH_DATA  16,0C118h   ;IF N Counter register
SYNTH_DATA  6,04h         initialization.

SYNTH_DATA  16,1801h    ;RF N Counter register
SYNTH_DATA  6,68h         initialization.

SYNTH_DATA  16,8211h    ;RF N Counter register
SYNTH_DATA  6,4Ch         initialization.
```

- Power Down mode #3: During this mode the current consumption of the radio is estimated at 1ma. The radio can not receive or transmit when configured for this mode. When set in this mode, it takes 15ms. to return the radio to its operational mode. When set in this mode, the PHY does not maintain its register configuration. All radio register values need to be reprogrammed to resume operation. This holds for both the PHY digital modem (HSP3824) and the PHY frequency synthesizer (HFA3925). To activate Power Down mode #3 the following signals need to be set as shown below:

RX_PE: Don't Care
RX_PE_BB: LOW
TX_PE: Don't Care
TX_PE_BB: LOW
PA_PE: LOW
RESET: LOW
RADIO_PE: LOW

When first attempting to transmit upon power-up, PA_PE must stay low for at least 10ms after RADIO_PE goes high.

Appendix A

Control Register Values for Single Antenna Acquisition

REGISTER	NAME	TYPE	REGISTER ADDRESS IN HEX	QPSK	BPSK
CR0	MODEM CONFIG. REG #1	R/W	00	3C	64
CR1	MODEM CONFIG. REG#2	R/W	04	00	00
CR2	MODEM CONFIG. REG#3	R/W	08	07	24
CR3	MODEM CONFIG. REG#4	R/W	0C	04	87
CR4	INTERNAL TEST REGISTER#1	R/W	10	00	00
CR5	INTERNAL TEST REGISTER #2	R/W	14	00	00
CR6	INTERNAL TEST REGISTER#3	R/W	18	00	00
CR7	MODEM STATUS REGISTER #1	R	1C	X	X
CR8	MODEM STATUS REGISTER #2	R	20	X	X
CR9	I/O DEFINITION REGISTER	R/W	24	00	00
CR10	RSSI VALUESTATUS REGISTER #2	R	28	X	X
CR11	ADC_CAL_POS REGISTER	R/W	2C	01	01
CR12	ADC_CAL_NEG REGISTER	R/W	30	FD	FD

Appendix A

Control Register Values for Single Antenna Acquisition (Continued)

REGISTER	NAME	TYPE	REGISTER ADDRESS IN HEX	QPSK	BPSK
CR13	TX_SPREAD SEQUENCE (HIGH)	R/W	34	05	05
CR14	TX_SPREAD SEQUENCE (LOW)	R/W	38	B8	B8
CR15	SCRAMBLE_SEED	R/W	3C	7F	7F
CR16	SCRAMBLE_TAP (RX & TX)	R/W	40	48	48
CR17	CCA_TIMER_TH	R/W	44	2C	2C
CR18	CCA_CYCLE_TH	R/W	48	03	03
CR19	RSSI_TH	R/W	4C	1E	1E
CR20	RX_SPREAD SEQUENCE (HIGH)	R/W	50	05	05
CR21	RX_SREAD SEQUENCE (LOW)	R/W	54	B8	B8
CR22	RX_SQ1_ IN_ACQ(HIGH) THRESHOLD	R/W	58	01	01
CR23	RX-SQ1_ IN_ACQ(LOW) THRESHOLD	R/W	5C	E8	E8
CR24	RX-SQ1_ OUT_ACQ(HIGH) READ	R	60	X	X
CR25	RX-SQ1_ OUT_ACQ (LOW) READ	R	64	X	X
CR26	RX-SQ1_ IN_DATA (HIGH) THRESHOLD	R/W	68	0F	0F
CR27	RX-SQ1-SQ1_ IN_DATA (LOW) THRESHOLD	R/W	6C	FF	FF
CR28	RX-SQ1_ OUT_DATA (HIGH) READ	R	70	X	X
CR29	RX-SQ1_ OUT_DATA (LOW) READ	R	74	X	X
CR30	RX-SQ2_ IN_ACQ (HIGH) THRESHOLD	R/W	78	00	00
CR31	RX-SQ2- IN-ACQ (LOW) THRESHOLD	R/W	7C	CA	CA
CR32	RX-SQ2_ OUT_ACQ (HIGH) READ	R	80	X	X
CR33	RX-SQ2_ OUT_ACQ (LOW) READ	R	84	X	X
CR34	RX-SQ2_IN_DATA (HIGH) THRESHOLD	R/W	88	09	09
CR35	RX-SQ2_ IN_DATA (LOW) THRESHOLD	R/W	8C	80	80
CR36	RX-SQ2_ OUT_DATA (HIGH) READ	R	90	X	X
CR37	RX-SQ2_ OUT_DATA (LOW) READ	R	94	X	X
CR38	RX_SQ_READ; FULL PROTOCOL80211	R	98	X	X
CR39	RESERVED	W	9C	X	X
CR40	RESERVED	W	A0	X	X
CR41	UW_TIME_OUT_LENGTH	R/W	A4	90	90

Appendix A

Control Register Values for Single Antenna Acquisition (Continued)

REGISTER	NAME	TYPE	REGISTER ADDRESS IN HEX	QPSK	BPSK
CR42	SIG_DBPSK Field	R/W	A8	0A	0A
CR43	SIG_DQPSK Field	R/W	AC	14	14
CR44	RX_SER_Field	R	B0	X	X
CR45	RX_LEN Field (HIGH)	R	B4	X	X
CR46	RX_LEN Field (LOW)	R	B8	X	X
CR47	RX_CRC16 (HIGH)	R	BC	X	X
CR48	RX_CRC16 (LOW)	R	C0	X	X
CR49	UW -(HIGH)	R/W	C4	F3	F3
CR50	UW _(LOW)	R/W	C8	A0	A0
CR51	TX_SER_F	R/W	CC	00	00
CR52	TX_LEN (HIGH)	R	D0	X	X
CR53	TX_LEN(LOW)	R	D4	X	X
CR54	TX_CRC16 (HIGH)	R	D8	X	X
CR55	TX_CRC16 (LOW)	R	DC	X	X
CR56	TX_PREM_LEN	R/W	E0	80	80

Harris Semiconductor

APPNOTE

No. AN9623 July 1996

Harris Wireless Products

Packet Error Rate Measurements Using the PRISM™ Chip Set

Author: John Fakatselis

Introduction

The Harris PRISM chip set has been designed to be used for both continuous and packetized data transmission applications. System designers need the capability to evaluate and test the radio performance under their operating environments and by using their own transmission method and protocols. In the case of continuous transmission testing, there are commercially available Bit Error Rate (BER) testers that can be utilized to perform the required evaluation tests.

In contrast when it comes to packetized data evaluation, the availability of Packet Error Rate (PER) testers, to test a packetized radio, are not as readily available. In most cases the system evaluators are designing custom test beds to accomplish these performance measurements. This application note is an attempt to provide some guidance of how to design a PER test environment for the PRISM radio.

Test Bed Description

The Test bed required is comprised of a TX and an RX set of PRISM radios, a PER Tester (PERT) and any other noise and interference equipment as required for the emulation of the channel environment. Figure 1, illustrates this top level test bed configuration. The focus of this note is to explore some possibilities for a custom designed PER tester.

The function of the tester is to generate the desired data packets at baseband (digital Data) and feed them to the PRISM radio for transmission through an interface with the PRISM HSP3824 Baseband Processor. The TX PRISM radio will transmit the packet through the channel. The RX radio will demodulate the baseband packet, which will be transferred to the PER tester via the HSP3824 interface. The PER tester will detect any errors within the received packets. In addition the PERT should be able to report any dropped transmitted packets that were not acknowledged at the receiver. These dropped packets will also be accounted as part of the PER measurement.

The test bed includes an interference source to add noise and interference at RF to accomplish the PER measurement as a function of SNR.

Test Packets

The format of the test packets to be transmitted must always have one of the formats as described in the HSP3824 data sheet. All of the packet formats include a preamble field, header fields, and data.

The preamble is programmable and can be up to 256 symbols long. The preamble is used for initial PN synchronization of the receiver.

The header can consists of various fields depended on the desired protocol mode. The header always includes the Start Frame Delimiter (SFD) field. This is true under any mode of

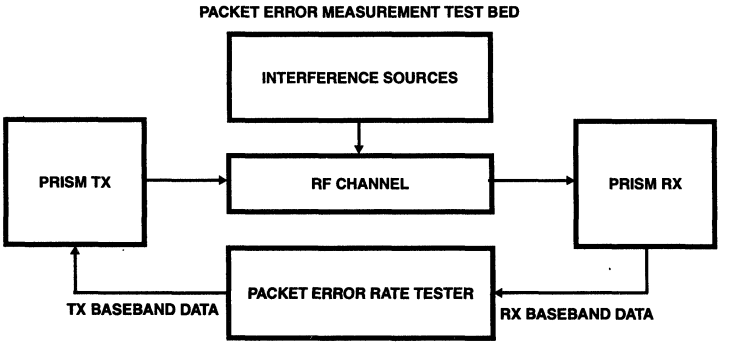


FIGURE 1. PRISM PER MEASUREMENTS TOP LEVEL TEST BED CONFIGURATION

operation. Other fields are optional per the mode in use. There is also a choice to either protect the header fields with CRC or not.

The PERT will be responsible for generating and appending the data portion of the packet to the preamble and header fields.

The example of this note will expand on the simplest possible header format that the HSP3824 is capable of self-generating. This format is shown on Figure 2, and it consists of the preamble bits and the SFD header field immediately followed by the externally provided data.

The transmit side of the PER tester generates the data, controls the data length and the packet transmission rate.

The receive side of the PER tester adds the number of errorless messages received for comparison with the number of actual packets transmitted to derive a PER performance figure.

PER Tester Description

The PERT functional block diagram is illustrated in Figure 3. The PER functions are grouped into the TX, RX and modem interface functions.

The test philosophy requires that the data sent by the PER tester includes a CRC check field. The CRC is checked at the RX and it either declares a successful packet reception or a packet in error. If for some reason the packet is never seen at the receiver then the PER tester should be able to account for the missed packet. The PER tester should also be able to control the packet length and the frequency (rate) of the transmissions. The PER tester maintains a count of the transmitted vs. the successfully received packets. These counts will be used to calculate the PER performance of the experiment.

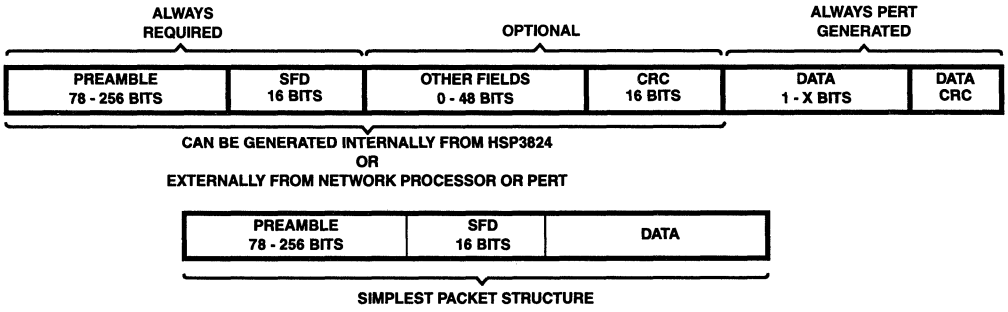


FIGURE 2. PACKET FORMAT DESCRIPTION

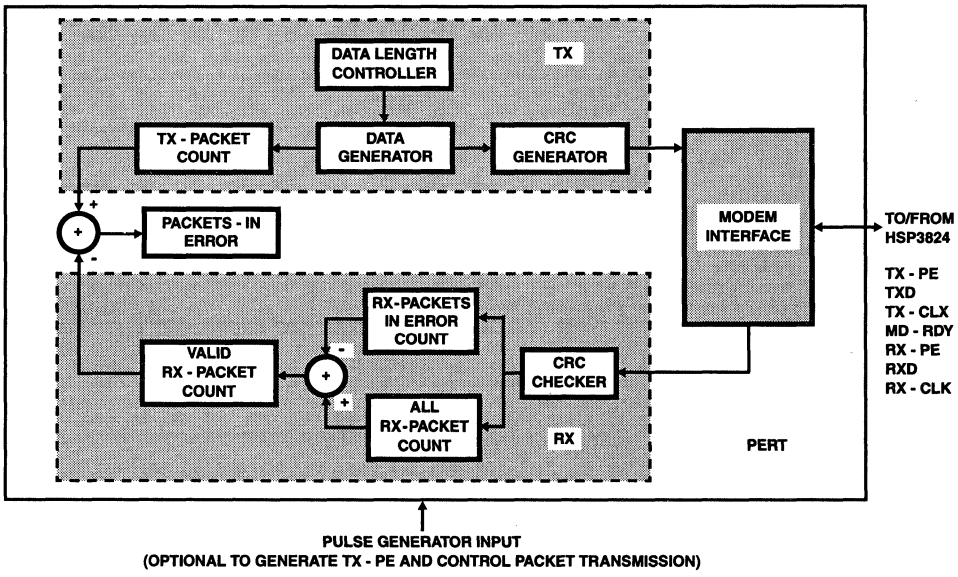


FIGURE 3. PERT TOP LEVEL BLOCK DIAGRAM

Modem Interface

The PERT is required to send the transmit packet to the PRISM radio and also to receive the demodulated received packet from the radio. The PERT will interface directly with the HSP3824 PRISM Baseband Processor. Details of the HSP3824 interface requirements are described in the HSP3824 data sheet. A timing diagram of the TX and RX interfaces are shown on subsequent figures of this note. The TX_PE signal initiates the transmit operation of the radio. The actual rate and duty cycle of this signal will define the rate of packet transmission, as well as the length of the transmitted packet size. As shown on Figure 4, TX_PE envelops the preamble, header and the packet data. The TX_PE line can be driven directly from an external, off the shelf, pulse generator with a programmable duty cycle. The programmable pulse generator will provide a variety of packet lengths and transmission rates to adequately evaluate the radio performance.

TX Function

The PERT TX functions include the data generator, the data length controller, the CRC generator and the TX packet counter.

The data generator outputs the test data that needs to be appended to the header. The interface signal TX_RDY indicates to the PER tester when it should start sending the data through the HSP3824 interface. The timing is shown on Figure 5. More details of this interface are described in the HSP3824 data sheet.

The data generator uses the data length defined by the data length controller. The data length controller can be simply a register that is programed to indicate the desired size of the data packet or it can be controlled directly from the signal of the external pulse generator that drives the TX_PE line as described above.

The CRC generator appends a CRC check at the end of the data. The CRC will be checked at the RX portion of the PER tester after it has been transmitted and received through the channel. The RX will check the data for CRC errors and if in error then the packet will be declared as such. The PER tester TX function maintains a count of all transmitted packets through the TX packet counter.

RX Function

The PERT RX functions include a CRC Check and the RX packet counter. The timing of the RX interface between the PRISM (HSP3824) and the PERT receiver is shown on Figure 6.

The PERT checks the data for the CRC calculation starting when MD_RDY is asserted by the HSP3824. MD_RDY envelopes the first data bit after the preamble and it is deasserted at the end of the data CRC.

The PERT receiver counts all packets received and then subtracts from that count any packets that have been detected with a CRC error. This count, that is maintained by the PERTs receiver, in conjunction with the count that is maintained by the PERTs transmitter (which keeps track of the number of all transmitted packets) are used to derive the PER performance of the system under test.

This PERT design is capable to account for all packets in error.

- If a packet is never received, the transmitter will report it to its TX packet count and the error will be accounted for.
- If an error occurs within the PRISM (HSP3824) header, which has not been processed by the PERTs CRC circuit, the packet in error will not be received by the PERT. The HSP3824 will drop the packet (will not assert MD_RDY), upon detecting a corrupt header.
- If an error occurs within the PERT generated data, it will be detected by the CRC check function of the PERT receiver. This packet will be subtracted from the received packet count.

By utilizing the PERTs CRC checks in combination with the HSP3824 programmable features, the design can be simplifed since no actual data comparisons need to be implemented. This design can lead to effective PER performance measurements for a PRISM based packetized system.

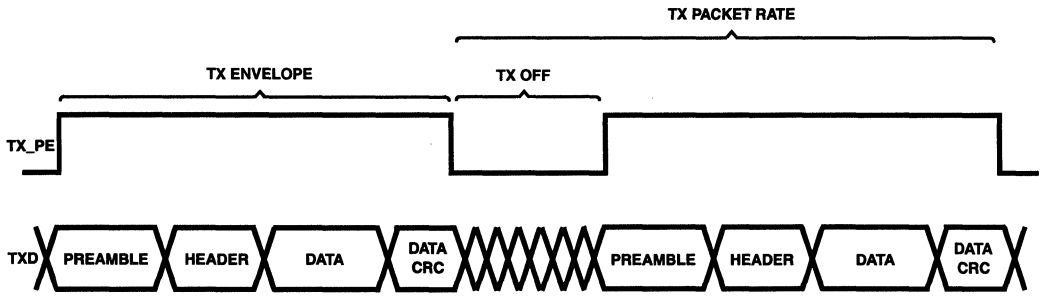
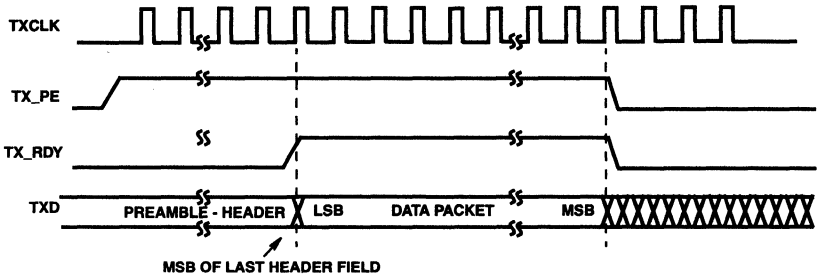
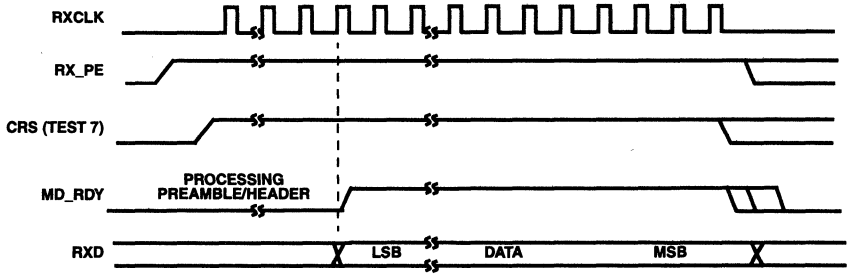


FIGURE 4. PACKET TRANSMISSION TIMING DIAGRAM



NOTE: Preamble/Header and Data is transmitted LSB first TX_RDY is inactive Logic 0 when generated externally. TXD shown generated from rising edge TXCLK.

FIGURE 5. PRISM (HSP3824) DIGITAL TX INTERFACE



NOTE: MD_RDY active after CRC16.

FIGURE 6. PRISM (HSP3824) DIGITAL RX INTERFACE

Harris Semiconductor

APPNOTE

No. AN9624.2 January 1997

Harris Wireless Products

PRISM™ DSSS PC Card Wireless LAN Description

Author: Carl Andren, Mike Paljug, Doug Schultz

Introduction

The PRISM™ PC Card Wireless LAN Kit is provided with two reference wireless LAN PC Cards. This note will detail the RF and analog design of these cards. The physical layer (PHY) sections of these PC Cards are described in detail in the following sections. The medium access control (MAC) section of the PC Cards is described in detail in the pending AMD application note titled "Wireless LAN DSSS PC Card Reference Design" [1].

Figure 1 shows a block diagram of the reference radio design. This radio has been designed to conform to the draft IEEE 802.11 specification but does not include the antenna diversity selection.

The specifications of the PC Card wireless LAN are as follows:

General Specifications

- Targeted Standard ..... IEEE 802.11 (Draft)
- Data Rate ..... 1MBPS DBPSK
  2MBPS DQPSK
- Range ..... 400ft Indoor Typ (Note 1)
  3700ft Outdoor Typ (Note 1)
- Frequency Range .....2412 - 2484MHz
- Step Size 1MHz
- IF Frequency 280MHz
- IF Bandwidth 17MHz
- RX/TX Switching Speed.....2µs Typ
- Operating Voltage ..... 4.5 - 5.5V_{DC}
- Standby Current..... 100mA at 25µs Recovery (Note 4)
  65mA at 2ms Recovery (Note 4)
  18mA at 15ms Recovery (Note 4)
- Operating Temperature Range ...-30°C to 70°C (Note 2)
- Storage Temperature Range .....-55°C to 125°C
- Mechanical.... Type II PC Card, with Antenna Extension
- Antenna Interface.....SMA, 50Ω

Receive Specifications

- Sensitivity .....-93dBm Typ, 1MBPS, 8E-2 FER (Note 3)
  -90dBm Typ, 2MBPS, 8E-2 FER (Note 3)
- Input Third Order Intercept Point.....-17dBm Typ
- Image Rejection ..... 80dB Typ
- IF Rejection..... 80dB Typ
- Adjacent Channel Rejection ..... 35dB Min
- Supply Current ..... 320mA Typ, 2MBPS

Transmit Specifications

- Output Power ..... +18dBm Typ
- Transmit Spectral Mask....-32dBc Typ at First Side-Lobe
- Supply Current ...560mA Typ, 2MBPS, 100% Duty Cycle

NOTES:

1. Using omnidirectional antenna.
2. Oscillator and AM79C930, limited to 0°C to 70°C currently.
3. FER = Frame Error Rate or Packet Error Rate.
4. Recovery times do not include MAC recovery.

Receive Processing

Referring to the block diagram in Figure 1, a single antenna is used. Up to two antennas are supported in the HSP3824[2] Baseband Processor to implement diversity, countering the adverse effects of multi-path fading. From the antenna, the received input is applied to FL1, a Toko TDF2A-2450T-10 two pole dielectric bandpass filter, which is used to provide image rejection for the receiver. The IF frequency is 280MHz, and low-side injection is used, thereby placing the received image 560MHz below the tuned channel. FL1 also provides protection for the RF front-end from out of band interfering signals.

The T/R switch is integrated in the HFA3925[3] RF Power Amplifier (RFPA). The HFA3925 RFPA operates from the unregulated 5V PC Card supply. Following the T/R switch, the HFA3424[4] Low Noise Amplifier (LNA) is used to set the receiver noise figure. The HFA3424 LNA operates from a regulated 3.5V supply.

A trade-off between noise figure and input intercept point exists in any receiver, to balance these conflicting requirements in the PRISM™ radio, an attenuator follows the HFA3424 LNA. The attenuation chosen is 5dB. To improve

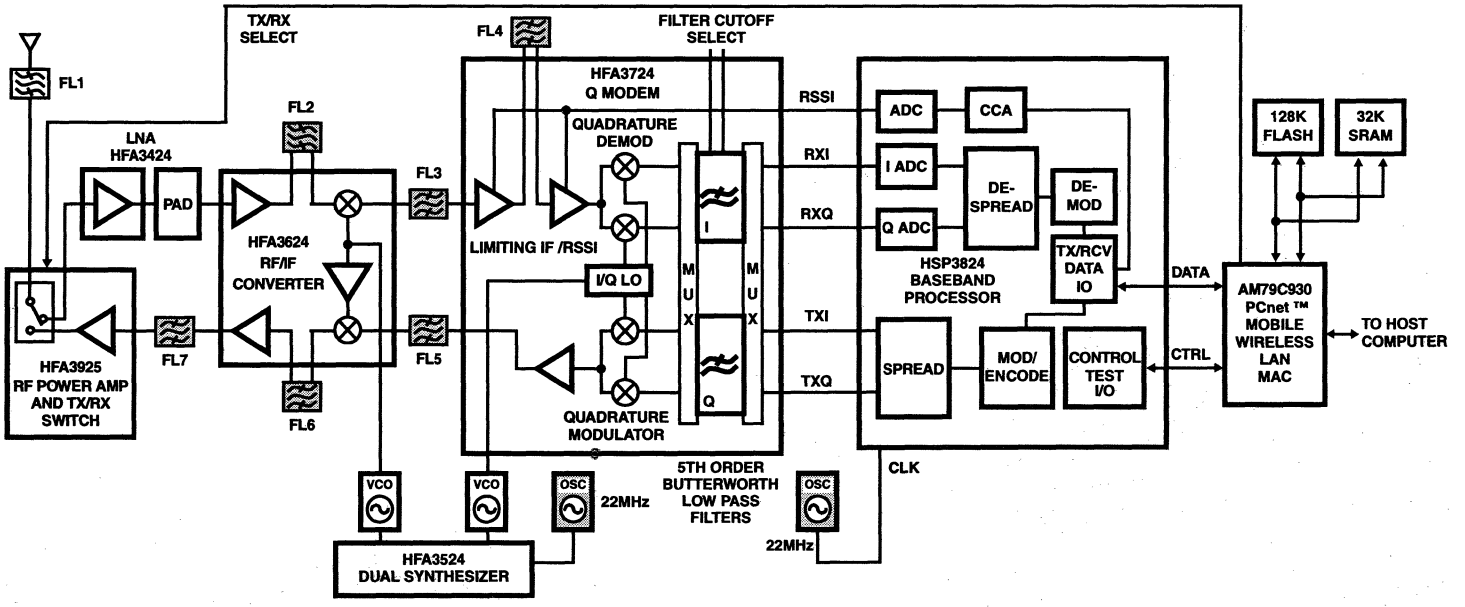


FIGURE 1. PRISM™ PC CARD BLOCK DIAGRAM

Cnet™ is a trademark of AMD, Inc.

TABLE 1. PRISM™ CASCADED FRONT-END ANALYSIS

STAGE	G	GC	F	FC	IP3O	IP3OC	IP3IC
FL1 RF FILTER	- 2.0	- 2.0	2.0	2.0	100.0	100.0	102.0
HFA3925 T/R SWITCH	- 1.2	- 3.2	1.2	3.2	34.0	34.0	37.2
HFA3424 LNA	13.0	9.8	2.0	5.2	11.1	11.0	1.2
ATTENUATOR	- 5.0	4.8	5.0	5.5	100.0	6.0	1.2
HFA3624 LNA	15.6	20.4	3.8	6.0	15.0	14.1	- 6.3
FL2 RF FILTER	- 3.0	17.4	3.0	6.0	100.0	11.1	- 6.3
HFA3624 MIXER	3.0	20.4	12.0	6.3	4.0	3.6	- 16.8
FL3 IF FILTER	- 10.0	10.4	10.0	6.4	100.0	- 6.4	- 16.8
HFA3724[6] IF STRIP	0.0	10.4	7.0	6.8	100.0	- 6.4	- 16.8

Cascaded Gain = 10.4 dB
Cascaded NF = 6.8 dB
Cascaded Input IP3 = -16.8 dBm

NOTE: G (individual stage gain, dB), GC (cumulative gain, dB), F (NF, dB), FC (cumulative NF, dB), IP3O (individual stage output IP3, dBm), IP3OC (cumulative output IP3, dBm), IP3IC (cumulative input IP3, dBm)

noise figure, this attenuation may be reduced; alternatively, to improve input intercept point, this attenuation may be increased. The cascaded front-end noise figure and input intercept point analysis is shown in Table 1.

Next, the signal enters the HFA3624[5] RF/IF Converter LNA section, which aids in setting receiver NF. FL2 is used to suppress image noise generated in both the HFA3424 LNA and the HFA3624 LNA, and is a Murata LFJ30-03B2442B084 two pole monolithic LC bandpass filter. Only modest attenuation at the image frequency is required. The insertion loss is not critical, since at this point in the receiver, component loss or NF is offset by the preceding gain stages. All sections of the HFA3624 RF/IF Converter operate from a regulated 3.5V supply.

Down-conversion from the 2.4GHz - 2.5GHz band is performed in the HFA3624 RF/IF Converter mixer section. As previously mentioned, the IF center frequency is 280MHz, and low-side local oscillator (LO) injection is used. A discrete LC matching network is used at the mixer output to differentially combine the IF outputs, as well as impedance match to a 50Ω environment. A trimmer capacitor is used as part of the narrow-band matching network. An alternative, broadband matching network is described in the HFA3624 RF/IF Converter application note, and does not require any tunable elements. A direct impedance match to the IF filter, FL3 could be implemented if desired. The 50Ω environment was chosen to allow ease in measurement of portions of the radio with external test equipment.

The IF receive filter, FL3, is a Toyocom TQS-432 SAW bandpass filter. The center frequency is 280MHz, the 3dB bandwidth is 17MHz, and the differential group delay is less than 100ns. Insertion loss is typically 6dB, making it ideal for single-conversion systems. The impedance of the SAW is 270Ω, and a series 33nH inductor is used to match the filter input to 50Ω. The SAW output is matched directly to the IF input of the HFA3724 Quadrature IF Modulator/Demodulator, using a shunt 56nH inductor. This presents a 250Ω source impedance to the limiter input, thereby optimizing the limiter's NF.

In the receive mode, the HFA3724 Quadrature IF Modulator/Demodulator provides two limiting amplifiers, a quadrature baseband demodulator, and two baseband low pass filters. All sections of the HFA3724 operate from a regulated 3.5V supply. The first limiting amplifier establishes the NF of the IF strip at approximately 7dB. A discrete one pole LC differential filter, FL4, is placed between the two limiters to restrict the noise bandwidth of the first limiter. As both limiters exhibit a broadband response, with over 400MHz bandwidth, a noise bandwidth reduction filter is appropriate to ensure that the second limiter is fully limiting on the front-end noise within the signal bandwidth, as opposed to the broadband noise generated by the first limiter. This filter has a center frequency of 280MHz, and a 3dB bandwidth of 50MHz. It consists of a fixed 10nH inductor and a fixed 20pF capacitor, as described in the HFA3724 data sheet.

At the output of the limiters, a $200mV_{P-P}$ differential signal level is maintained under all input conditions. This limited signal is then mixed in quadrature to baseband in the HFA3724 Quadrature IF Modulator/Demodulator. The LO needed for the quadrature mixing is applied at twice the IF frequency, or 560MHz. A divide by two circuit then provides an accurate quadrature LO for the mixers. The baseband outputs of the quadrature mixers are AC coupled off-chip to the integrated fifth order Butterworth filters. The output levels of the low pass filters are nominally $500mV_{P-P}$ single-ended, and are intended to be AC coupled to the HSP3824 Baseband Processor. The AC coupling time constant is approximately 25 times longer than the symbol period, and is implemented with 0.01µF series capacitors. These coupling capacitors must be taken into account, however, when estimating the time it takes to power up or awaken from sleep mode.

At the input to the HSP3824 Baseband Processor, the quadrature signals are analog to digital converted in wideband 3 bit converters. The signals are spread spectrum with no DC term, so it is feasible to AC couple the signals to the ADCs and avoid DC bias offsets. The signal at this point has been limited to a constant IF amplitude and then passed through two separate mixer and low pass filter paths. The component variations in these two paths can introduce offsets in amplitude and phase and can also use up some of the headroom in the ADCs. The maximum amplitude variation is 2dB and the maximum phase balance variation is 4 degrees. Since the signal is limited, the IF signals will have low peak to average ratios even with noise as an input. The I and Q signals will have sinusoidal properties with PSK modulation imposed. It is their combined vector magnitude that is limited, not their individual amplitudes. To optimize the demodulator's performance, the ADCs are operated at the point where they are at full scale on either I or Q one third of the time. To maintain this operating point in the face of component variations, there is an active adjustment of the ADC reference voltage by feedback. This avoids the necessity of allowing extra headroom for the variation. The adjustment circuit is very slow and averages the energy from the two channels over both packet and noise conditions.

The HSP3824 Baseband Processor correlates the PN spreading to remove it and to uncover the differential BPSK or QPSK data. The processor initially uses differential detection to identify and lock onto the signal. It then makes measurements of the carrier and symbol timing phase and frequency and uses these to initialize tracking loops for fast acquisition. Once demodulating and tracking, the processor uses coherent demodulation for best performance. Since this radio uses a spread spectrum signal, the signal to noise ratio (SNR) in the chip rate bandwidth is about 0dB when the demodulator is at the desired bit error rate in BPSK. The radio operates with about 2.5dB of implementation loss relative to theoretical performance and achieves a sensitivity of -93dBm with BPSK.

The HSP3824 Baseband Processor provides differential decoding and descrambling of the data to prepare it for the Media Access Controller (MAC). The MAC is an AMD AM79C930 PCnet™-Mobile controller. All packet signals have a preamble followed by a header containing a start frame delimiter (SFD), other signal related data and a cyclic redundancy check (CRC). The MAC processes the header data to locate the SFD, determine the mode and length of the incoming message and to check the CRC. The MAC then processes the packet data and sends it on through the PC Card interface to the host computer. The MAC checks the packet data CRC to determine the data purity. If corrupted data is received, a retransmission is requested by the MAC which handles the physical layer link protocols.

Transmit Processing

Data from the host computer is sent to the MAC via the PC Card interface. Prior to any communications, however, the MAC sends a Request to Send packet to the other end of the link and receives a Clear to Send packet. The MAC then formats the data by appending it to a preamble and header and sends it on to the HSP3824 Baseband Processor which clocks it in. The HSP3824 Baseband Processor scrambles the packet and differentially encodes it before applying the spread spectrum modulation. The data can be either DBPSK or DQPSK modulated at 1 MSPS and is a baseband quadrature signal with I and Q components. The spreading is an 11 chip Barker sequence that is clocked at 11MHz and is modulated with the I and Q data components. These are then output to the HFA3724 as CMOS logic signals.

Transmit quadrature single-bit digital inputs are applied to the HFA3724 Quadrature IF Modulator/Demodulator from the HSP3824 Baseband Processor. These inputs are attenuated by 1/7 and DC coupled to the fifth order Butterworth low pass filters, which are used to provide shaping of the phase shift keyed (PSK) signal. The required transmit spectral mask, at the antenna, is -30dBc at the first side-lobe relative to the main-lobe. An unfiltered PSK waveform would have the first side-lobe suppressed only -13dBc. The fifth-order filters are tuned to an approximate 7.7MHz cutoff, using a 909Ω resistor external to the HFA3724.

In the PC Card wireless LAN, the goal is to control the regrowth of the side-lobes, with the HFA3925 RFPA dominating the regrowth. This will result in maximum transmitted power available. To achieve this goal, once the PSK waveform is filtered at baseband, all remaining transmit elements are operated at a 6dB back-off from compression, except for the HFA3925 RFPA, which is operated at less back-off.

The low pass filters provide initial shaping of the PSK waveform. Final shaping is provided by a transmit IF filter, FL5, a Toyocom TQS-432 SAW bandpass filter. The low pass filter outputs are off-chip AC coupled to the quadrature up-converter in the HFA3724. As in the receive mode, the baseband AC coupling time constant is approximately 25 times longer than the symbol period, and is implemented with 0.01µF series capacitors. The same twice IF frequency LO used previously is also used in this up-conversion. The IF output of the HFA3724 is reactively matched to FL5, with a 250Ω resistive load presented to the HFA3724. A shunt 47nH inductor, in parallel with a 316Ω resistor, is used to provide this match, negate the effects of board and component capacitance, and provide a DC return to V_{CC} to prevent saturation in the IF output stage of the HFA3724.

The output of FL5 is terminated in a 200Ω potentiometer that is used for transmit gain control. A shunt 47nH inductor is used to negate the effects of parasitic board and component shunt capacitance, as well as match the SAW output to the potentiometer. This potentiometer has it's center wiper connected to the HFA3624 RF/IF Converter transmit IF input, which has an input resistance of approximately 3kΩ. By varying the potentiometer, the gain of the transmit chain is controlled, allowing for precise control of the signal back-off at the HFA3925 RFPA. Therefore, this potentiometer is adjusted to achieve the desired compromise between transmit output power and the main-lobe to side-lobe ratio of the output PSK waveform, typically -32dBc to -35dBc.

Upconversion to the 2.4GHz - 2.5GHz band is performed in the HFA3624 RF/IF Converter transmit mixer. The mixer output is filtered with FL6, a Murata LFJ30-03B2442B084 two pole monolithic LC bandpass filter. This filter suppresses the

LO feedthrough from the mixer, and selects the upper sideband. The transmit buffer in the HFA3624 RF/IF Converter preamplifies the selected sideband, easing the requirement for HFA3925 RFPA gain.

FL7, a Toko TDF2A-2450T-10 two pole dielectric bandpass filter, is used to further suppress both the transmit LO leakage and the undesired sideband.

The HFA3925 RFPA amplifies the transmit signal to a level of approximately +20dBm, as measured at the T/R switch output. This represents a back-off from 1dB compression of approximately 4.5dB. Transmit side-lobe performance is approximately -32dBc to -35dBc with this level of back-off.

The HFA3925 RFPA is the only physical layer component that operates directly from the 5V PC Card supply. To supply the needed negative gate bias to the HFA3925 RFPA, a ICL7660SIBA[7] charge pump is used. A second potentiometer is used to adjust the drain current on the third stage of the HFA3925 to a quiescent operating current of 90mA, as measured through a one ohm sense resistor.

A logic-level PMOS switch, RF1K49093[8], is used to control the drain supply voltage to the HFA3925 RFPA, and implement a power down mode when receiving. As the RF1K49093 is a dual device, the other PMOS switch is used to control the supply voltage to the HFA3424 LNA and implement a power down mode when transmitting. A 2N2222 NPN transistor is used to level shift the 3.5V logic level from the AM79C30 MAC to drive the 5V PMOS switch gates, as well as the 5V HFA3925 RFPA T/R control gate.

Following the T/R switch, FL1 is reused in the transmit mode to attenuate harmonics generated in the HFA3925 RFPA, as well as providing additional suppression of the LO. As the loss of FL1 is approximately 2dB, the amount of transmit power available at the antenna is approximately +18dBm.

Synthesizer Section

The dual frequency synthesizer section uses the HFA3524[9] Synthesizer and two voltage controlled oscillators to provide a tunable 2132MHz - 2204MHz first LO, and a fixed 560MHz second LO. Both feedback loops use a 1MHz reference frequency that is derived from a 22MHz MF Electronics T3391-22.0M crystal oscillator. This crystal oscillator currently limits the operating temperature range of the radio to 0°C to 70°C. Both passive loop filters were designed to have loop bandwidths of 10kHz, and phase margins of 50 degrees. The feedback loop analysis is described in the HFA3524 Synthesizer evaluation board documentation. All components in the synthesizer section operate from a regulated 3.5V supply.

The tunable 2132MHz to 2204MHz first LO oscillator is a Z~Communications SMV2100L VCO. To ensure operation at low tuning voltages, a start-up circuit was added to force the tuning voltage from the HFA3524 Synthesizer RF charge pump to a high state for a short period (~1ms) following HFA3524 programming. A 2N2907 PNP transistor was used to implement this function, and the AM79C930 MAC device provides the control signal. The output level of the first LO to the HFA3624 RF/IF Converter is attenuated to approximately -3dBm.

The fixed 560MHz second LO oscillator is a discrete design, using a Phillips BFR505 transistor and a Siemens BBY51 varactor, as described in the HFA3524 Synthesizer evaluation board documentation. The output level of the second LO to the HFA3724 Quadrature IF Modulator/Demodulator is attenuated to approximately -6dBm and a three pole low pass filter is included to preserve the duty cycle of the output. High even order components in the second LO can result in offsets from a 50% duty cycle, and will degrade the quadrature phase accuracy of the HFA3724. A transconductance network is used at the HFA3724 LO input to convert the second LO voltage into a current, as recommended in the HFA3724 data sheet. As the HFA3524 Synthesizer auxiliary IF input covers the 560MHz range, the internal divide-by-two LO buffer output of the HFA3724 is disabled, as recommended in the HFA3724 data sheet.

Regulator Section

Linear voltage regulators are used to provide filtering and isolation from the 5V PC Card input supply. An additional advantage of using voltage regulators is a savings in overall supply current, as all of the components that are regulated consume less current at a 3.5V operating point, as opposed to a 5V operating point. The only components operating directly from the 5V supply are the HFA3925 RFPA, in order to maximize RF output power, and the PC Card interface. Sections of the AM79C930 MAC controller, as well as the host computer may use 5V logic levels.

A total of three regulators, 3.5V Toko TK11235MTL, are used in the PC Card wireless LAN. One regulator is devoted to the HSP3824 Baseband Processor and AM79C930 MAC devices. The remaining two regulate the RF and IF sections of the radio. One regulator supplies voltage to the synthesizer section, the HFA3424 LNA, and the HFA3624 RF/IF Converter. The second regulator supplies voltage to the HFA3724 Quadrature IF Modulator/Demodulator.

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[3] HFA3925 AnswerFAX document #4132, 407-724-7800. Available on Internet, Harris' home page is http://www.semi.harris.com

[4] HFA3424 AnswerFAX document #4131, 407-724-7800. Available on Internet, Harris' home page is http://www.semi.harris.com

[5] HFA3624 AnswerFAX document #4066, 407-724-7800. Available on Internet, Harris' home page is http://www.semi.harris.com

[6] HFA3724 AnswerFAX document #4067, 407-724-7800. Available on Internet, Harris' home page is http://www.semi.harris.com

[7] ICL7660S AnswerFAX document #3179, 407-724-7800. Available on Internet, Harris' home page is http://www.semi.harris.com

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APPNOTE

No. AN9633 August 1996

Harris Wireless Products

Processing Gain for Direct Sequence Spread Spectrum Communication Systems and PRISM™

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Introduction

This application note addresses the concept of processing gain (PG) of Direct Sequence Spread Spectrum (DSSS) systems. The PRISM chipset is used to implement DSSS radio designs. The processing gain provides the unique properties to the DSSS waveform primarily in terms of interference tolerance. The PG of a DSSS system is centered around the utilization of random codes which are used in conjunction with the data. These random codes are referred as Pseudo Noise (PN) codes. The HSP3824 provides this coding capability for the PRISM.

Description

In a DSSS system random binary data with a bit rate of r_b bits per sec (bps) is multiplied (Exclusive Ored) by a pseudorandom binary waveform, which is at much higher rate and it provides the frequency spreading operation. This pseudorandom (PN) binary source outputs symbols called chips at a constant chip rate r_C chips per sec (cps).This is a random, noise like signal and hence the name PN signal. The chip rate is always higher than the bit rate, and the ratio of the chip rate to the bit rate is defined as the processing gain (PG) [2]. The PG is a true signal to jammer (interference) ratio at the receiver after the despreading operation (removal of PN).

The rate of the PN code is the one that defines the bandwidth of the transmitted spread waveform.

The receiver of a DSSS system must remove the spreading as the first step in the demodulation process.

During the despreading operation the receiver must generate a phase locked exact replica of the pseudorandom spreading waveform to match the transmitted signal. This is achieved by the code acquisition, and code tracking loops embedded in the HSP3824. The receiver PN sequence must be exactly in phase with the transmitted PN sequence, and this is achieved by correlation techniques.

DSSS Transceiver

A DSSS transmitter is shown in Figure 1. The data is denoted by d(t), the spreading signal is denoted by c(t), and the spread waveform q(t) is fed to the BPSK modulator operating at a carrier frequency f_C, and the transmitted signal is denoted by x(t).

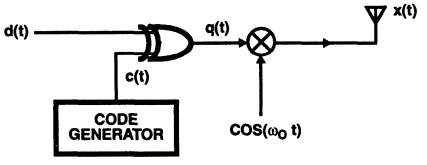

FIGURE 1. DSSS TRANSMITTER

A text book conceptual block diagram of a DSSS receiver is depicted in Figure 2. Note that PRISM is architected to perform the despreading function at baseband (HSP3824) rather than at RF as shown on Figure 2. This example is used for illustration of the concept and not to reflect the actual PRISM implementation.

The received signal for this text book example is the combination of the transmitted spread spectrum signal and a narrow band jammer $x_J(t)$. The locally generated despreading sequence is denoted by c'(t), and should be equal to c(t). The despread signal is then band pass filtered before data demodulation and d'(t) should be equal to d(t).

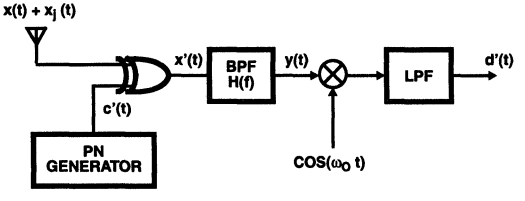

FIGURE 2. DSSS RECEIVER

PG Benefits

The primary benefit of processing gain is its contribution towards jamming resistance to the DSSS signal. The PN code spreads the transmitted signal in bandwidth and it makes it less susceptible to narrowband interference within the spread BW. The receiver of a DSSS system can be viewed as unspreading the intended signal and at the same time spreading the interfering waveform. This operation is best illustrated on Figure 3.

Figure 3 depicts the power spectral density (psd) functions of the signals at the receiver input, the despread signal, the bandpass filter power transfer function, and the band pass filter output. Figure 3 graphically describes the effect of the processing gain on a jammer. The jammer is narrow, and has a highly peaked psd, while the psd of the DSSS is wide and low. The despreading operation spreads the jammer power psd and lowers its peak, and the BPF output shows the effect on the signal to jammer ratio.

If for example, BPSK modulation is used and an Eb/No of lets say 14dB is required to achieve a certain BER performance, when this waveform is spread with a processing gain of 10dB then the receiver can still achieve its required performance with the signal having a 4dB power advantage over the interference. This is derived from the 14dB required minus the 10dB of PG.

The higher the processing gain of the DSSS waveform the more the resistance to interference of the DSSS signal.

The classical definition of processing gain is the 10 Log number $[r_C/r_B]$ in dB. By this definition a system that has a data rate of 1MBPS and a chip rate (rate of PN code) of 1MCPS will have a PG of 10.41dB. Using the PRISM chip set each data bit is x-ored with an 11 bit sequence for this particular example. The processing gain can be then viewed as the 10Log[11]dB where 11 is the length of the PN code. If a code with a length of 16 bits is to be used then the processing gain is equivalent to 10 Log[16] dB or 12.04dB.

To this end these PN signals must posses certain mathematical properties to be useful as part of a DSSS system. Primarily the PN codes that are useful must have very good autocorrelation and crosscorrelation properties as well as maintaining some randomness properties.

The DSSS receiver is utilizing a reference PN sequence which is a replica to the transmitted sequence and when it detects correlation between the reference and the incoming sequences it declares initial acquisition and it establishes initial symbol timing. Any partial correlations can result to false acquisitions and degradation to the receiver performance. This is why the PN code must have good correlation properties. Some of the PN code classes with such properties are described next.

This paper highlights the Barker codes, Willard codes and m-sequences with 7 and 15 chips per period which are implementable using the HSP3824.

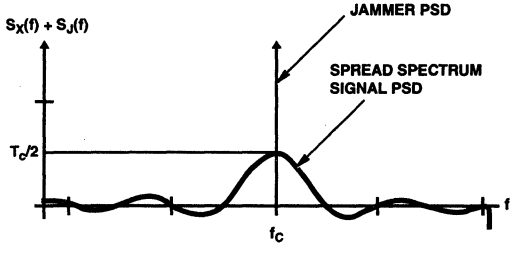

FIGURE 3A. PSD OF SPREAD SPECTRUM SIGNAL AND NARROWBAND JAMMER

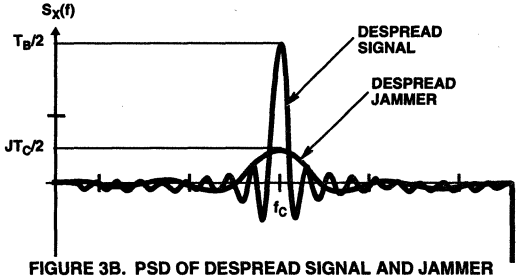

FIGURE 3B. PSD OF DESPREAD SIGNAL AND JAMMER

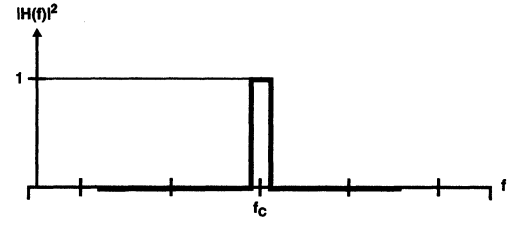

FIGURE 3C. POWER TRANSFER FUNCTION OF BPF

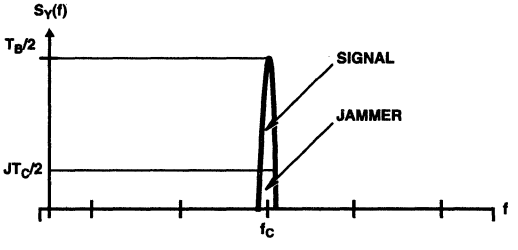

FIGURE 3D. PSD OF BPF OUTPUT

FIGURE 3. PROCESSING GAIN EFFECT ON NARROW BAND JAMMING

PN Codes

PN codes with the mathematical properties required for implementation of a DSSS radio are:

Maximum Length Sequences

Maximum length sequences (m-sequences), are PN sequences that repeat every 2^n-1, where n is an integer, they are implemented by shift registers and Exclusive Or gates, they are governed by primitive polynomials, and possess good randomness properties including a two-valued autocorrelation function [3].

For example the 7 chip PN sequence is governed by the primitive polynomial generator

$$c_7(x) = 1 + x^2 + x^3$$

and the output chips are given by:
0 0 1 0 1 1 1 0 0 1 0 1 1 1 **0 0 1 0 1 1 1** 0 0 1 0 1 1 1 0...

Figure 4 depicts the d(t), c(t) with the above m-sequence, and with q(t) the x-or of d(t) and (ct).

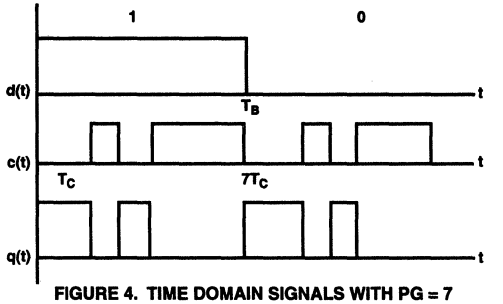

FIGURE 4. TIME DOMAIN SIGNALS WITH PG = 7

Figure 5 depicts the 7 chip sequence and its autocorrelation function. Note that the autocorrelation also repeats every 7 chips, or once per bit of the actual data if each of the data bits is spread by the entire sequence.

As another example, the 15 chip PN sequence is governed by the primitive polynomial generator

$$c_{15}(x) = 1 + x^3 + x^4$$

and the output chips are given by:
0 0 0 1 0 0 1 1 0 1 0 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0 1 1 1 1
0 0 0 1 0 0 1 1 0 1 0 1 1 1 1...

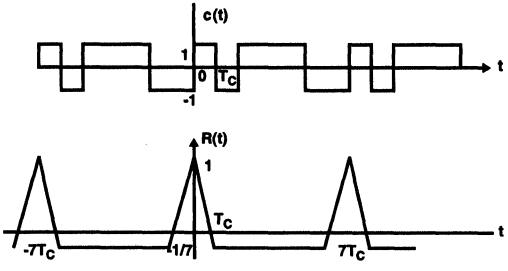

FIGURE 5. SEVEN CHIP M-SEQUENCE AND ITS AUTOCORRELATION FUNCTION

Barker Codes

Barker Codes are short unique codes that exhibit very good correlation properties. These short codes with N bits, with N=3 to 13, are very well suited for DSSS applications and can all be generated by the HSP3824. A list of Barker Codes is tabulated in Table 1.

Willard Codes

Willard Codes, found by computer simulation and optimization, and under certain conditions, offer better performance than Barker Codes. They can all be generated by the HSP3824, as was done for the Barker Codes. A list of Willard Codes is provided in Table 1.

The inverted or bit reversed versions of the codes listed on Table 1 can be used since they still maintain the desired autocorrelation properties.

TABLE 1. BARKER AND WILLARD CODES

N	BARKER SEQUENCES	WILLARD SEQUENCES
3	110	110
4	1110 or 1101	1100
5	11101	11010
7	1110010	1110100
11	11100010010	11101101000
13	1111100110101	1111100101000

Configuring the HSP3824 to Implement Various PN Codes

The HSP3824 is the baseband processor of the PRISM chipset and it generates the PN sequence. The device is programmable to any desirable sequence of up to 16 bits.

PN Generator Description

The spread function for the radio is the same sequence and is applied to every symbol as BPSK modulation. PN generation is performed by parallel loading the sequence from a configuration register (CR) within the HSP3824 and serially shifting it out to the modulator.

PN Generator Programmable Registers

A maximum of 16 bits can be programmed into the configuration register. Registers CR13 and CR14 contain the high and low bytes of the sequence for the transmitter. The corresponding registers for the receiver are CR20 & CR21. Bits 5 & 6 of CR3 set the sequence length in chips per bit. The sequence is transmitted MSB first. When fewer than 16 bits are in the sequence, the MSBs are truncated.

PN Correlator Description

The PN correlator is designed to handle BPSK spreading. Since the spreading is BPSK, the correlator is implemented with two real correlators, one for the I and one for the Q channel. It has programmable registers to hold the spreading sequence and the sequence length for both the receiver and the transmitter. This allows a full duplex link with different spreading parameters for each direction.

The correlators are time invariant matched filters otherwise known as parallel correlators.

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TechBrief

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Harris Wireless Products

A Brief Tutorial on Spread Spectrum and Packet Radio

Author: Carl Andren

Introduction

The new communications standard for wireless local networks, IEEE 802.11, uses spread spectrum and packet radio techniques and these are features which are not common knowledge. The first term, spread spectrum, indicates a radio frequency modulation technique where the radio energy is spread over a much wider bandwidth than needed for the data rate. We do this to get some benefits that are not readily apparent. The easiest spread spectrum technique to explain is frequency hop (FH). In this technique, the channel being used is rapidly changed in a pseudo random pattern so that the communications appears to occupy a wide bandwidth over time. See Figure 1. This spreads the energy out so that the average power in any narrow part of the band is minimized. Of course, the transmitting and receiving radios need to synchronize their hopping patterns so that they hop together.

As an example, 802.11 specifies that we use the ISM band at 2.4GHz. The ISM band is 83MHz wide and has been subdivided into 1MHz channels for the FH specification. The FCC insists that any spread spectrum FH radio operating in this band must visit at least 79 of the channels at least once every 30 seconds. This works out to a minimum hop rate of 2.5 hops per second.

The next form of spread spectrum is called Direct Spread (DS) and this is the other form of spread spectrum allowed by the FCC in this band. With DS, the data is mixed (XOR) with a high rate pseudo random sequence before being PSK modulated onto the RF carrier. This high rate sequence can be many orders of magnitude higher in rate than the data. In the ISM band, it is limited to not less than a 10:1 spreading ratio. This high rate phase modulation spreads the spectrum out while dropping the power spectral density. This means that this kind of signal will interfere less with narrow band users. It also has some interference immunity to those narrow band emitters. The receiver processing of DS signals begins with despreading the signals. This is done by mixing the spread signal with the same PN sequence that was used for spreading. See Figure 2A. This collapses the desired signal to its original bandwidth and form. It meanwhile spreads all other signals that don't correlate with the spreading signal. Thus a narrowband interference will get spread in this operation and will not fit through the narrow data filter. See Figure 2B. When the signal energy is collapsed to the data bandwidth, its power spectral density is increased by the amount of the processing gain which is proportional to the bandwidth reduction. Thus a signal that was received at or below the noise floor, is now above the noise and can be demodulated.

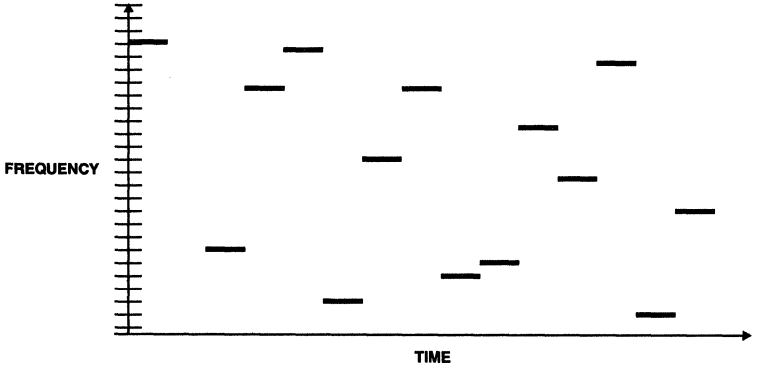


FIGURE 1. FH SPREAD SPECTRUM

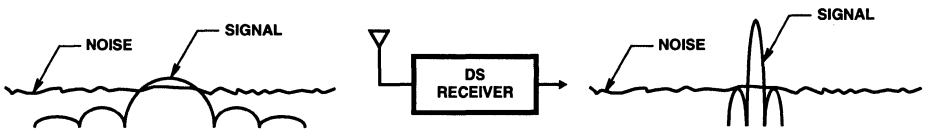


FIGURE 2A. LOW POWER DENSITY

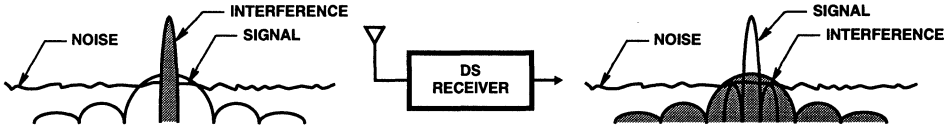


FIGURE 2B. INTERFERENCE REJECTION

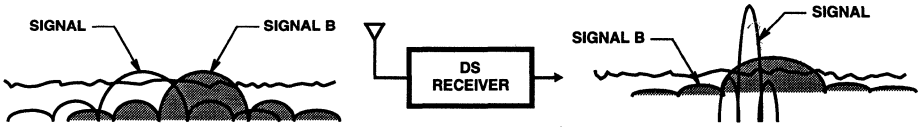


FIGURE 2C. MULTIPLE ACCESS

FIGURE 2. DIRECT SEQUENCE SPREAD SPECTRUM PROPERTIES

Finally, DS spread spectrum can allow more than one user to occupy the same channel through a feature called multiple access. Each DS receiver collapses only correlated signals to the data bandwidth. Other, non correlated signals will remain spread in this step. When the desired signal is filtered to the signal bandwidth, only a small fraction of the undesired signal remains. See Figure 2C.

The term packet radio or packet communications is common where the communications medium is not well controlled. There are numerous reasons why a radio communications link may be interrupted, such as the microwave oven. [1] The microwave oven radiates in the middle of the ISM band with a 50% duty cycle and a pulse rate locked to the power line. Thus it is off for 8ms every 16ms. These off periods allow the transmission of bursts (or packets) of 1000 bytes at a time. Frequency hopping also means that the radio communications is interrupted every 400ms while the sending and receiving radios are retuned. The breaking up of a large block of data into small "packets" is a common technique in communications to insure that error free communications can take place even with interruptions. [2] If the medium is corrupted intermittently, a large block of data will never make it through without errors. In the packet technique this block is broken into small packets that each have some error detection bits added. Then, if an error is detected, a retransmission of the small packet that was corrupted will not unduly burden the network. This packet communications technique has short control packets that check to see if the medium is clear, the other end is ready to receive and, to request a retransmission if a packet did not get through correctly. See Figure 3. All of this requires some overhead expense that reduces the net system throughput. Packet length can be optimized to minimize overhead while insuring the greatest throughput with data integrity.

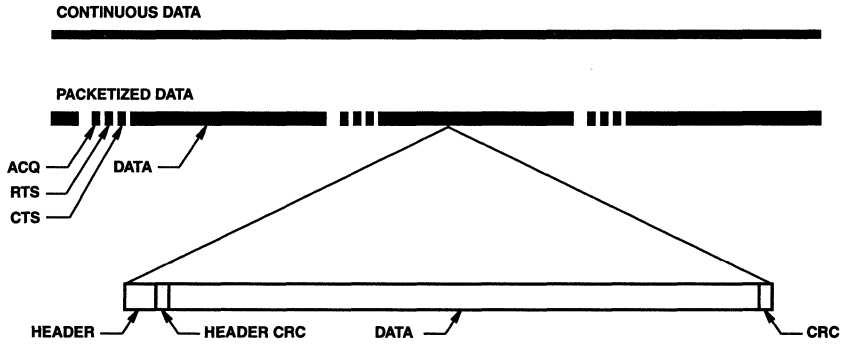


FIGURE 3. PACKET TRANSMISSION

When continuous data is packetized, the instantaneous rate must increase since the time allowed for data transmission is reduced. This allows time for the packet protocol interchange, packet headers and other overhead. Packet communications can be used with various access protocols such as carrier sense multiple access (CSMA) or time division multiple access (TDMA). CSMA allows asynchronous communications, but requires each communicator to first establish that the medium is not busy. It then establishes the link with an interchange consisting of a request to send (RTS), followed by a clear to send (CTS), the data packet and acknowledgment or not (ACK/NAK). TDMA allows synchronous communications where each user is allocated a time slot to communicate in. The network overhead in this scheme is in the wasted time when some users have nothing to send and in the packets from the controller necessary to allocate the time slots.

The combination of spread spectrum and packet communications for the 802.11 wireless local area networks allows robust communications in a crowded and noisy band.

References

[1] The 2.4GHz ISM band has been called the Junk band because it is already contaminated by oven emissions. Years ago, 2.43GHz was allocated to the microwave oven and it was felt that no one else would ever want to co-occupy this band. As pressure to allocate more spectrum to communications was felt, the FCC set up rules for unlicensed Instrumentation, Scientific and Medical (ISM) operation in this "worthless" band.

[2] Remember the days of typewriters where typing a whole page without error was a trying experience. The first word processor that allowed you to look over and correct each sentence before committing it to paper was a real breakthrough.

Harris Semiconductor

TechBrief

No. TB338 June 1996

Harris Wireless Products

Using the PRISM™ Chip Set for Timing Measurements (Ranging)

Authors: Carl Andren and Perry Frogge

PRISM™ Many applications use the properties of Direct Sequence Spread Spectrum to establish accurate timing which is useful for ranging and time dissemination. DS receivers use a wide bandwidth and correlation techniques to measure the time of arrival of signals to a high degree of accuracy. While the PRISM™ chip set was not designed specifically for this, it does, however, have all the required assets to do medium accuracy time of arrival measurements.

It is quite simple to use the PRISM™ radio for accurate timing measurements. All of the timing information is available from the HSP3824 Baseband Processor. At the sending end, the asynchronous rising edge of TX_PE will reset the counter of the internal transmit state machine which will output the header and data a fixed amount later. This is timed to within one MCLK (22MHz), so there is an ambiguity of 0.5 MCLK (45ns) in this time. Additionally, the setup to hold time of TX_PE to MCLK is not specified in the data sheet. This can, however, be included in the calibration measurements. Thus, all you have know is the offset between MCLK and the source timing to get even better resolution. This offset can be sent in the data portion of the message. The length of the preamble and header is fixed (128 + 64 = 192), so the start of data is at a fixed offset in bits.

On the receive side, MD_RDY is output after the CRC-16 check. Thus it indicates the precise time the first bit of the data part of the message is received. This is, of course, 192 bits after the arrival of the first bit of the packet. The MD_RDY offset from MCLK also needs to be taken into account to resolve the overall offset between the correlation and the signal timing to within a fraction of MCLK. On the data sheet, this is listed as t_{D3} which has a maximum value of 25ns.

The accuracy the receiver is going to get in capturing the asynchronous correlation peak in the header is ±0.25 MCLK or about 11ns. To improve on this, more heroic processing can be attempted. Over the length of the message, the timing can be refined further by averaging, as long as there is an offset between the RX and TX clocks. That is, the timing will slowly drift and be reset, allowing the external system to judge when in the process the timing was at the peak. Since this occurs half way between resets, it is not too hard to find. Thus, the ultimate receive time accuracy is probably about 0.1 MCLK or 5ns. This ultimate accuracy will take some extra computation to achieve.

To the time of arrival measurement you need to add the propagation delay of ~1ns per foot, delays in the RF and IF filters and in other devices in the path. The propagation delay could be longer if a multipath signal is the one chosen by the receiver due to the direct path being blocked.

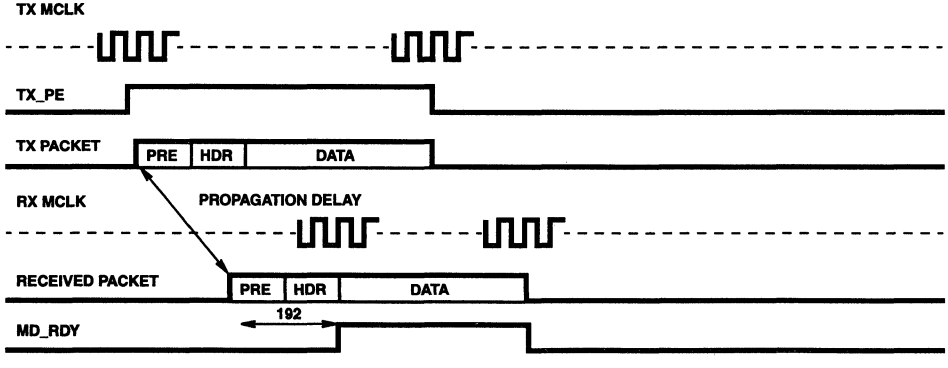


FIGURE 1.

In using this capability, the designer will need to take accurate measurements to calibrate the delays encountered in the PRISM™ hardware. Since the baseband processor is a state machine, its delays will be fixed offsets from the MCLK with minor variations over temperature and production tolerances.

Figure 1 shows some of the elements of the delay. The scale is not accurate; specifically, the clock rate is grossly under represented for clarity.

The total delay from initiation to response is as follows:

$T_D = t_{T\text{-}M} + t_{D2} + t_{Tx} + t_{IF} + t_{RF} + 192\mu s + t_{PROPAGATION} + t_{RF} + t_{IF} + t_{Rx} + t_{MCLK} + t_{D3}$

Where:

T_D = total delay (TX_PE to MD_RDY)

$t_{T\text{-}M}$ = delay from TX_PE to next rising edge of MCLK

t_{D2} = MCLK to TXCLK delay

t_{Tx} = delay through the transmit state machine to IF

t_{IF} = IF filter and amplifier delays

t_{RF} = RF filter and amplifier delays

192µs = length of preamble and header

$t_{PROPAGATION}$ = propagation loss due to speed of light (about 1ns per foot)

t_{RF} = RF filter and amplifier delays

t_{IF} = IF filter and amplifier delays

t_{Rx} = delay through the receive processing from IF

t_{MCLK} = accuracy of tracking the actual received timing to the local MCLK

t_{D3} = MCLK to MD_RDY delay

All processing operations are timed by the transmit and receive MCLKs (22MHz) which can be also slaved to or shared with the source's and sink's clocks. If 802.11 compliant operation is not needed the MCLK can be other than 22MHz to allow sharing with the application.

No. AN9658 January 1997

Implementation of a High Rate Radio Receiver (HSP43124, HSP43168, HSP43216, HSP50110, HSP50210)

Authors: John Henkelman and David Damerow

Features

- **Modulation Formats: BPSK, QPSK, SQPSK, 8-PSK, FM, FSK**
- **Symbol Rates: To 22.5 MSPS (4 Samples/Symbol)**
- **Programmable: Reconfigurable to Data Rate, Modulation Format, and Order/Type of Tracking Loop**
- **Digital: Repeatable Performance Over Temperature and Time**
- **High Performance Reception: Bit Error Rate Approaches Less Than 0.5dB From Theory**

TABLE 1. HARRIS DSP PRODUCTS FOR HIGH RATE DIGITAL RADIO RECEIVERS

FUNCTIONAL BLOCK	HARRIS PART
VCA	Analog Discrete
140MHz Quadrature Output 6-Bit A/D Converter (8-Bit A/D Converter)	HI3086JCQ, CXA3086Q (HI3026JCQ, HI3026AJCQ)
Decimating Filter	HSP43216 Halfband Filter
Digital DownConverter	HSP50110 Digital Quadrature Tuner
Matched Filter	HSP43168 Dual FIR Filter
Carrier & Symbol Tracking Loops	HSP50210 Digital Costas Loop
AGC Loop Filter	Analog Discrete

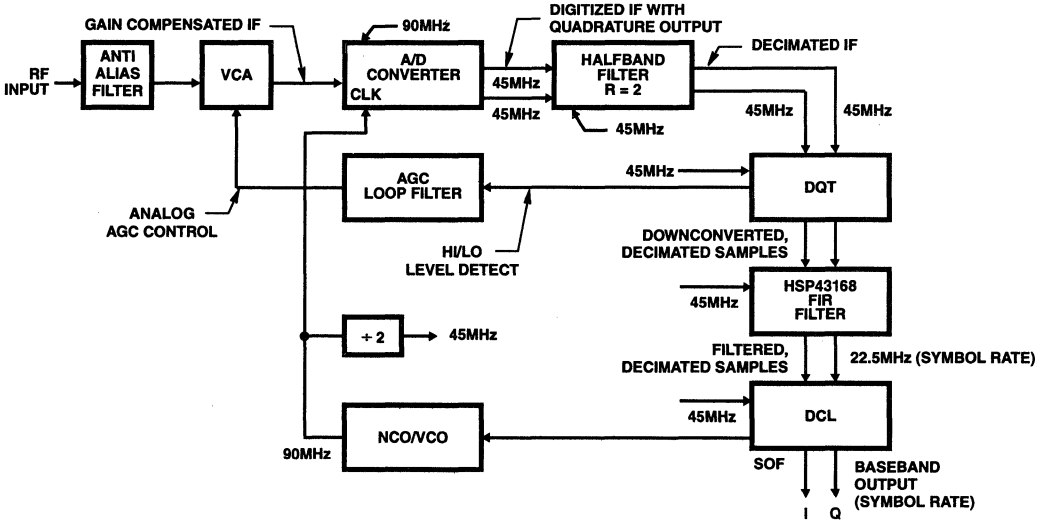


FIGURE 1. BLOCK DIAGRAM OF A HIGH RATE DIGITAL RADIO RECEIVER

Introduction

The present HSP50110/210EVAL board provides capabilities for evaluating received modulated signals with symbol rates up to 2.5 MSPS. This high end limit on symbol rate is based on 20 samples per symbol. Many applications do not require such a large number of samples per symbol, and can still use the HSP50110/210EVAL evaluation board to breadboard and test these applications. Two limitations come into play as higher rates are implemented with this evaluation board:

1. The Serial FIR Filter maximum clock rate is (45MHz/10 bits) = 4.5MHz.
2. The transport delay, or propagation delay in the loop causing loop instability for input rates above 4.5MHz.

It is these limitations that prompts the presentation of a high symbol rate receiver implementation using the HSP50110 Digital Quadrature Tuner (DQT) and HSP50210 Digital Costas Loop (DCL) chip set. Figure 1. illustrates a high rate receiver configuration using the DQT and DCL demod parts. This implementation will be offered as the design solution, after the design considerations and trades have been presented.

High Rate Design Concerns

The primary limitations on a high speed design are the maximum operating speed of the digital parts and the bandwidth and resolution on the A/D converter. These key parameters are listed for the parts that will be configured for our high rate receiver design.

Maximum Clock Speed of HSP43216: 52MHz
Maximum Clock Speed of HSP50110: 52MHz
Maximum Clock Speed of HSP43168: 45MHz
Maximum Quadrature A/D
Conversion Speed: ..... 140 MSPS with 6 Bits
120 MSPS with 8 Bits
Minimum Number Samples
per Symbol ..... 4 Samples/Symbol

Selecting An A/D Converter

The design begins with selecting a high speed, wide bandwidth, high resolution D/A converter. Devices exist that output dual demultiplexed data samples at half the sample rate. This relaxes the maximum clock rate of the following devices by 2. Such a device is the HI3086JCQ Harris A/D. It is a 6-bit 140 MSPS Flash A/D Converter with quadrature output samples. (The HI3026 A/D, an 8-bit 120 MSPS device with dual demultiplexed output is also a design candidate.) Subsequent DSP parts could operate up to a 70MHz maximum clock rate if the HI3086 is used.

Selecting The DSP Sample Rate

The Clock Rate Criterion

Selecting 4 samples per symbol yields the desired bandwidth. This sets the rate at which the HSP50110 Digital Quadrature Tuner will output symbol data. We can construct a DSP processing chain from this baseline symbol rate. The clock rate of the IF signal into the HSP50110 Digital Quadrature Tuner is set to be four times the symbol rate. By using an HSP43216 Halfband Filter in the Downconvert and Decimate mode (INT/EXT# = 0), the dual channel demultiplexed sampled data from the A/D can be input at four times the symbol rate. By noting that the A/D outputs 2 synchronous samples at half the A/D sample clock rate, the A/D sample rate is effectively four times the symbol rate.

The Re-Sampler in the DQT eliminates the need for the sample clock and the symbol rate to be exact integer related. (An even integer is used as an example for clarity and to yield a "ball park" solution for applications with non integer relationships.) Note that an external NCO is used to drive the A/D clock port. This minimizes the clocking jitter in the system. Use of the DQT Re-Sample NCO in addition to a separate clock generator for the A/D and halfband will inherently have more jitter than the configuration shown. The DQT is used in the complex input mode.

Determining the DSP System Limiting Rate

The next limiting clock DSP element is the Halfband Filter which has a maximum clock rate at 52MHz. The rate through this decimating filter part can be optimized by using it in the Downconvert and Decimate Mode (INT/EXT# = 0). This allows dual (demultiplexed) inputs at the maximum clock rate. This sets the maximum system sustainable clock rate at the output of the A/D converter at 52MHz per data stream. The maximum system sustainable A/D input sample clock becomes twice the A/D output clock, or 104MHz. The decimate by two HalfBand filter output becomes a quadrature data stream at 52MHz and the symbol rate is one half of this, or 26MHz (2 samples on I, 2 samples on Q = 4 samples per symbol).

System Design Considerations

Frequency Domain Considerations for the A/D Sample Rate

Determining the appropriate A/D sample rate, requires more than just consideration of the clocking criterion of the DSP parts. The frequency plan of the receive system must compliment the digitizing hardware and not produce alias components that will impede the ability to recover the signal of interest. Thus it is equally important that the sample rate be selected in a location relative to the IF signal, in a way that will not cause alias signals to fall in band. Many applications use undersampling techniques to recover signals from IF carriers by locating a harmonic of the sample frequency at a strategic distance from the IF signal. An alias of the high frequency IF carrier is then processed by the DSP hardware.

Figure 2A and 2B illustrate two examples of how a 90MHz A/D sample clock can be used to downconvert and process modulated IF signals. Figure 2A shows an oversampled 20MHz IF, while Figure 2B shows an undersampled 160MHz IF.

Figure 3 illustrates the spectral development at several points in the data path in the block diagram, from IF input to baseband output. The example has $F_S' = F_S/2$ (Decimate by 2) in the HBF and $F_S'' = F_S'/8$ (Decimate by 8) in the DCL.

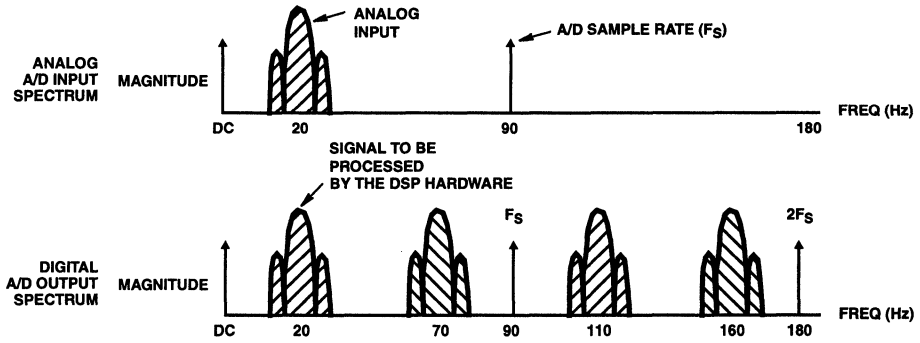


FIGURE 2A. OVERSAMPLED 20MHz IF INPUT SPECTRAL PLOTS

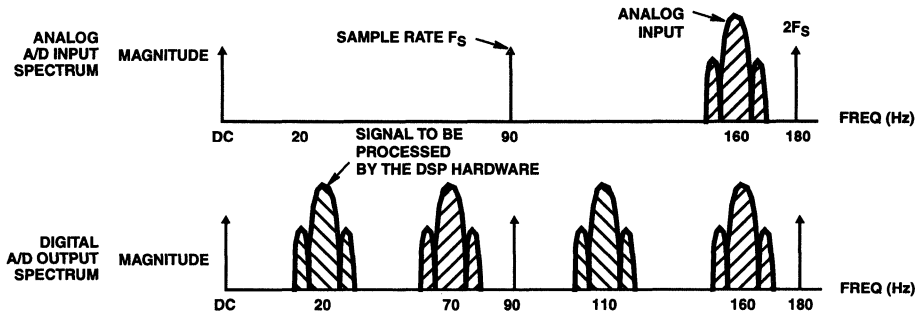
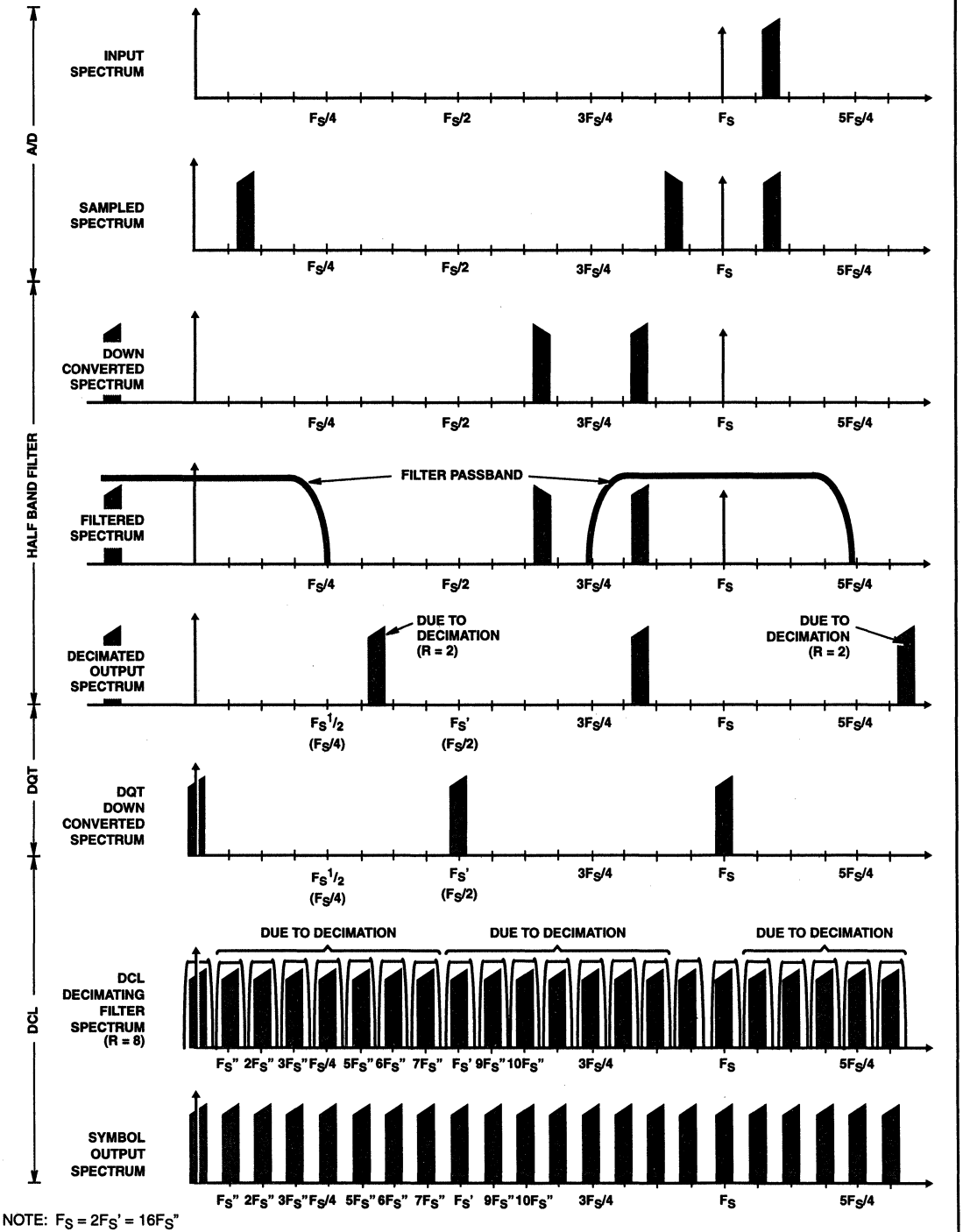


FIGURE 2B. UNDERSAMPLED 120MHz IF INPUT SPECTRAL PLOTS

Additionally it is insufficient to just consider the signals of interest. Those signals that fall in the band of the A/D converter, must be removed by any anti-aliasing filters ahead of the A/D converter. These in band signals; if not filtered out, will also alias around the clock frequency and may appear directly on top of the signal of interest. In example B of Figure 2, a 70MHz signal will interfere in such a way. The anti alias filter should be designed to attenuate the undesired signals to the point that it prevents such signal degradation. Note that an important system trade is the implementation of the anti-alias filter and the selection of the A/D clock frequency.



NOTE: $F_S = 2F_S' = 16F_S''$

FIGURE 3. HIGH RATE RECEIVER SPECTRAL DEVELOPMENT

Matched Baseband Filter Requirements

The final receiver design consideration is the construction of a matched baseband filter for the received signal. The DQT/DCL chipset offers two filters integral to the chip: 1) Integrate and Dump and 2) Square Root of Raised Cosine α = 0.4. If one of these filters meets your system performance requirements, then no further design is required.

If your application requires a different filter, the HSP43168 or the HSP43124 can be inserted between the DQT and the DCL. The serial I/O filter (HSP43124) is limited to CLK = (45MHz/bit width). The Dual FIR filter (HSP43168) is limited to CLK = 45MHz. These parts may become the limiting factor for the maximum clock speed. This translates to an A/D sample rate at 90MHz, an A/D dual demultiplexed data output rate of 45MHz, a Halfband Filter dual data Output Rate of 45MHz, and a symbol rate of 22.5MHz. In general, filtering requirements may demand that greater than eight taps be used in the filter, and two HSP43168 chips may be required (one for I, one for Q) for adequate shaping.

Summary

Figure 1 outlines the implementation of the high symbol rate receiver. The solution assumes the need for an application specific matched filter, limiting the symbol rate to 22.5MHz. Key elements of the design are: the anti-alias filter, the quadrature output A/D converter, the dual input decimating Halfband Filter, the Digital Quadrature Tuner and the Digital Costas loop. The design uses the level detection feature of the HSP50110 to drive a Voltage Controlled Attenuator to keep the level at the converter input at an optimum value.

For information relative to setting the internal PLL parameters in the DQT/DCL chipset, refer to the HSP50110/210 EVAL Users Manual.

Harris Semiconductor

APPNOTE

No. AN9659 January 1997

Digital Signal Processing

Using the HSP50110/210EVAL Example Configuration Files

Authors: John Henkelman and David Damerow

Introduction

Every HSP50110/210EVAL evaluation kit contains a floppy disk labeled DEMOD CHIPSET EVALUATION SOFTWARE. This disk contains the DEMODEVB.EXE file and other software necessary to configure and operate the evaluation card which is provided in the demod chipset kit. This kit provides all the software required for the configuration, operation and evaluation of the HSP50110 Digital Quadrature Tuner (DQT) and HSP50210 Digital Costas Loop (DCL).Additional software is provided to demonstrate the various filtering features of the evaluation board. The software provided in the kit ensures that a user can quickly set up the evaluation board, configure it, and output data for test evaluation. This Evaluation Kit will leave the user confident that these parts can be easily ported into an application specific design. Four directories (folders) are provided to assist in familiarizing the evaluator with key features of the chipset. These four directories are labeled "examples", "filters", "schemat" and "serinade" are provided for this purpose.

The "EXAMPLES" Folder

The first directory is filled with example configuration files which have been tested and proven to provide BER performance that is better than 1dB from theory. **It is the use of these example configuration files that is the focus of this application note.** This application note will detail the location, use and application of the example configuration files. The quickest way to configure the evaluation board for your application, is to find a configuration file that most closely matches your symbol rate, and load that file. The file can then be edited to change any of the parameters (such as IF frequency, Filtering, etc.) as needed.

Figures 1A and 1B detail the test Hardware configurations used to verify the BER performance of each configuration file. A study of these figures reveals that Figure 1A utilizes a 70MHz IF, while Figure 1B utilizes a 5MHz IF. These are the only two IF frequencies that will be found in the example files.

The "FILTERS" Folder

This folder contains example FIR filter configuration files. These files have been created with SERINADE, a software package developed for Harris Semiconductor to assist in the design of digital filters of the type found on the evaluation board. This application note will provide information on the description, and use of these filter files.

The "SCHEMAT" Folder

This folder contains the schematic of the evaluation board, as captured using the ORCAD application. The files are provided for design re-use and should help shorten the critical "Time to Market" development time. These schematics, which were used to generate the evaluation board, are offered for use in designs, it is the user's responsibility to secure the proper ORCAD revision and any ORCAD technical assistance in porting, opening and editing these schematics.

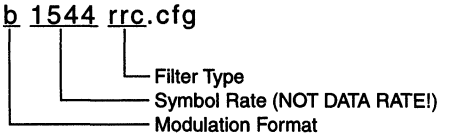
The "SERINADE" Folder

This folder contains the latest version of the SERINADE software. This software will assist in any application specific FIR filter design. The "filters" folder contains examples of filters already designed using this software, and should be used to verify results until the user is proficient with the application. All SERINADE generated filters are readily ported into a format that the HSP50110/210EVAL kit can import.

It is highly recommended that the distribution disk provided in the evaluation kit be backed up prior to use. Obtain a printout of the files in the "EXAMPLES" and "FILTERS" and use it to maintain a fully functional software package.

The "EXAMPLE" Configuration Files

The example configuration files included on the distribution disk are labeled according to the key shown below and in Appendix H of the User's Manual. The first field is an alphanumeric digit which indicates the modulation type. Options are: B for BPSK, Q for QPSK, and E for 8PSK. In the future F will be used to denote FSK, while M will denote MSK.



The second field is numeric and represents the symbol, or baud rate of the signal, expressed in KHz. The symbol rate numeric field utilizes a "p" to represent a decimal point. For example, a data rate of 1200bps is represented as 1p2. Similarly 9600bps is expressed as 9p6.

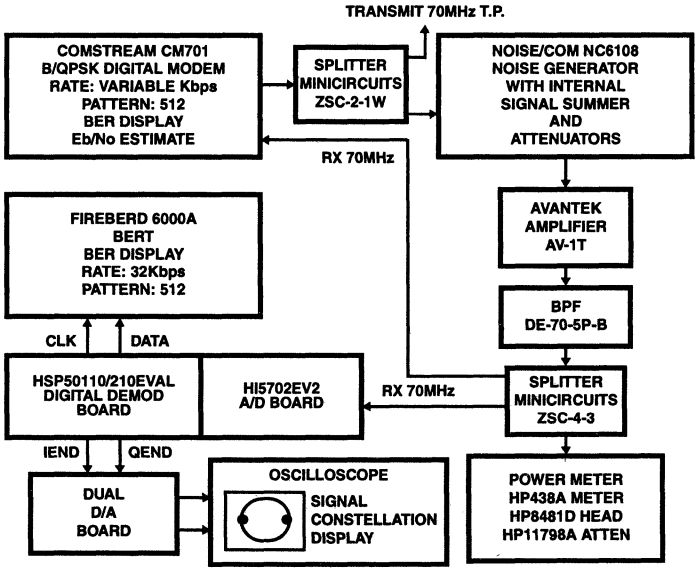


FIGURE 1A. 70MHz IF TEST CONFIGURATION

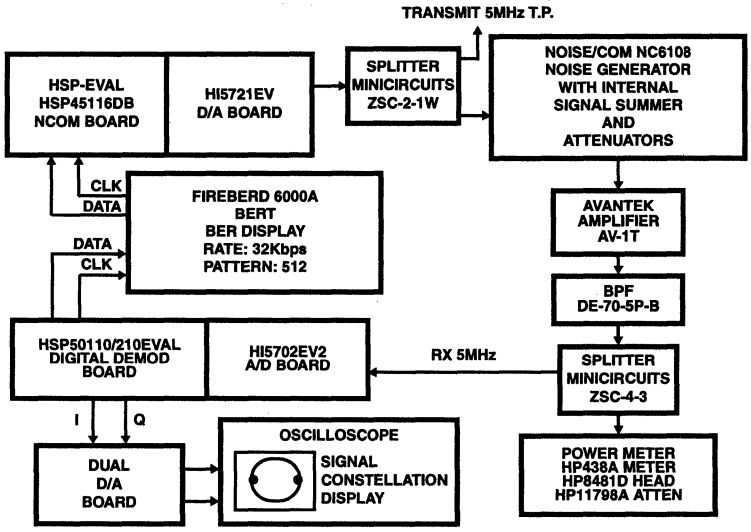


FIGURE 1B. 5MHz TEST CONFIGURATION

Care must be taken not to confuse symbol rate with data rate. Recall that for BPSK, data rate and symbol rate are identical. For QPSK, however, the symbol rate is 1/2 the data rate, because two bits of data are used to form a symbol. For 8PSK the symbol rate is 1/3 the data rate, because three bits of data are used to form a symbol. Figure 2 details how a typical QPSK modulator is implemented, while Figure 3 illustrates the data to quadrature symbol relationship for QPSK for both the in-phase and quadrature components. Two data bits will determine in which of four phase states the carrier will be placed: 0^o, 90^o, 180^o, or 270^o. This phase shift is accomplished using the I (in-phase) and (Q) quadrature orthogonal vectors as shown in Figure 4. Figure 5 illustrates the data and symbol relationship for 8PSK, while Figure 6 shows the possible carrier vectors created for a symbol.

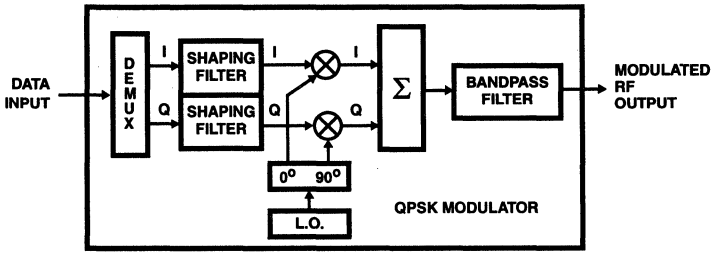


FIGURE 2. TYPICAL QPSK MODULATOR

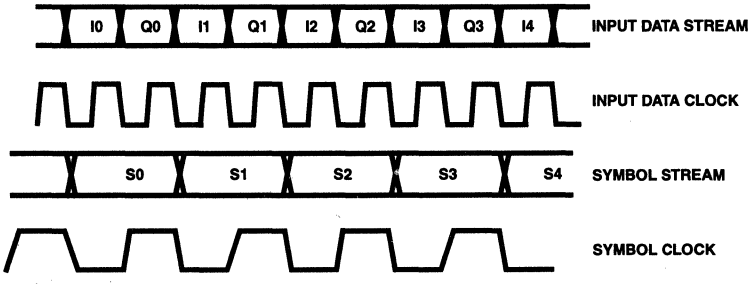


FIGURE 3. DATA TO SYMBOL RELATIONSHIP FOR QPSK

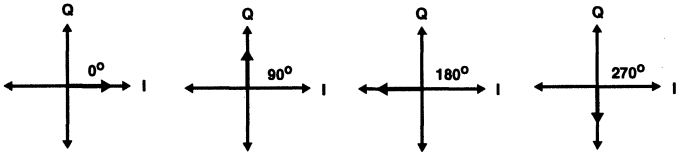


FIGURE 4. VECTOR REPRESENTATIONS OF THE QPSK SYMBOLS CREATED FROM TWO DATA BITS

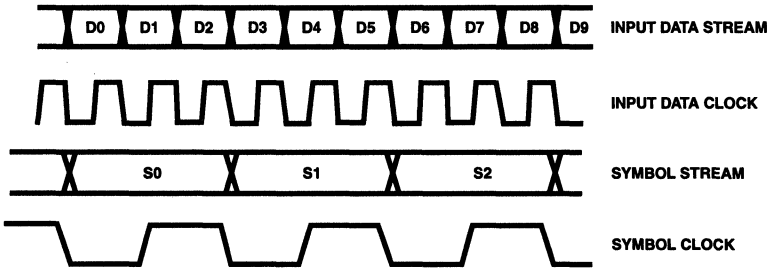


FIGURE 5. DATA TO SYMBOL RELATIONSHIPS FOR 8PSK MODULATION

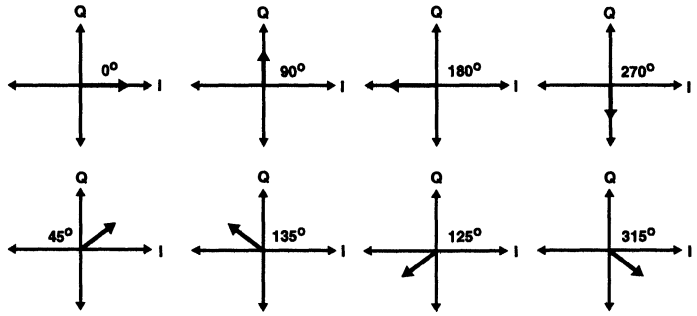


FIGURE 6. VECTOR REPRESENTATIONS OF THE 8PSK SYMBOLS CREATED FROM THREE DATA BITS

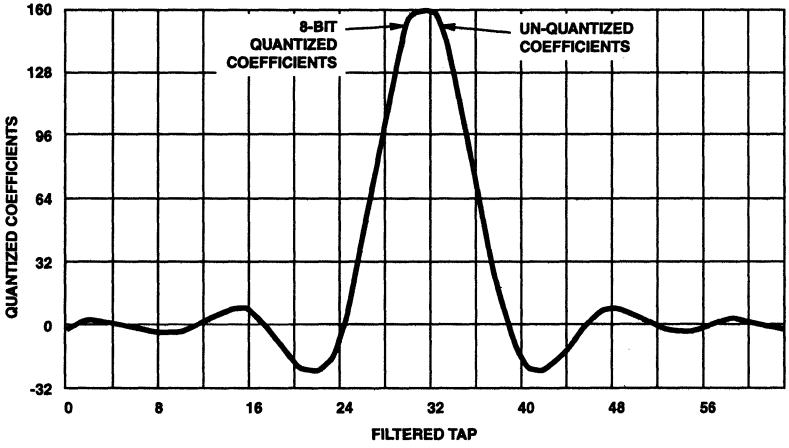


FIGURE 7. COEFICIENTS FOR THE SQUARE ROOT OF RAISED COSINE $\alpha = 0.4$ FILTER

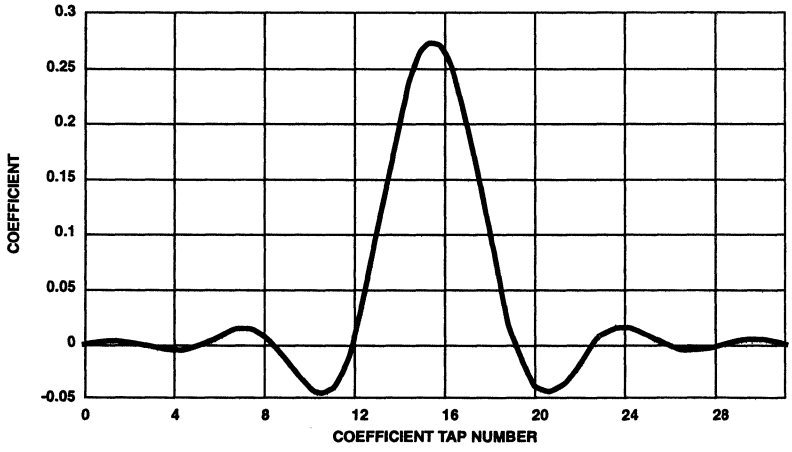


FIGURE 8. COEFFICIENTS FOR THE b128fir.cfg CONFIGURATION FILE FILTER: rrc4a4x.imp

The final field of the file name is the filter type. The options are RRC for Square Root of Raised Cosine α = 0.4 filtering (for bandlimited applications), I&D for Integrate and Dump filtering (for unfiltered data applications), and FIR filtering (for creating application specific onboard serial FIR filters). Figure 7 details the coefficients of the RRC Cosine α = 0.4 filter. The FIR selection implies that the DCL RCC and I&D filters are bypassed. In this case the file represents the coefficients for the FIR filter. Figure 8 details the coefficients for the FIR filter in example configuration file. Table 1 lists the configuration files provided as examples with the EVAL kit and details the modulation format, data rate and filtering associated with each file.

When using the "fir" filter configuration, the FIR filter coefficient file that is used can be changed. Figure 8 illustrates that the Data Path/Modulation Menu Item (14) must be selected and changed from "0" (Bypassed) to "1" (enabled). After selecting "1", the user is prompted for the file name of the filter. The software will automatically append a ".rpt" suffix to the file name, indicating a SERINADE generated file, so do not enter a suffix with your file name. A number of example FIR filter files have been included on the distribution disk in the kit under the ***FILTERS*** directory, for the evaluation of a variety of Square Root of Raised Cosine filters. The files with the ***".imp"*** suffix are files ready to import into ***SERINADE***. The ***SERINADE*** FIR filter design software is included on the evaluation kit distribution disk, allowing the user to create files for specific applications. The files with the ***".rpt"*** and ***".ser"*** suffixes are generated by ***SERINADE***. The HSP50110/210EVAL software uses the files with the ***".rpt"*** suffix. Table 2 defines the available FIR filter coefficient files.

HSP50110/210 Evaluation Board Software

DATA PATH/MODULATION MENU

Current File Name.\B128RRC
(1) Master Clock Freq. 40000000Hz
(2) Input Sample Rate 40000000Hz
(3) Input Mode . . . . . Gated
(4) DQT Input Samples . . . . . .Real
(5) DQT Input Format. . . . . Offset Bin
(6) L.O. Center Freq. . . . . .+5000000 Hz
(7) Data Modulation . . . . . .BPSK
(8) Baud Rate. 128000Hz
(9) DQT Output Rate . . . . . 256000Hz .
(10) I.F. NBW. . . . . 750000Hz .
(11) DQT Filter. . . . . CIC w/Comp
(12) DCL RRC Filter. . . . . .Enabled
(13) DCL I&D . . . . . Bypassed
(14) HSP43124 . . . . . .Bypassed
(15) Es/No (min). . . . . +0dB
(16) Es/No (max. . . . . +100dB
(17) Es/No (design) . . . . . +6dB
(18) A/D backoff (min.). 12dB
(19) A/D backoff (max.) 18dB
(20) DCL Output Vector. . . . . -6dBFS
(21) DQT Output Level. . . . . -12dBFS
(22) DCL Detect. Level . . . . . -12dBFS
(23) Slicer Threshold 0.25
(24) DQT AGC Slew Rate 30dB/sec
(25) DCL AGC Slew Rate 10dB/sec
(26) AGC Limits . . . . . FULL RANGE
(27) Output Mux Control 7
(0) MAIN MENU
ENTER SELECTION: (14) ←

FIGURE 9. DATA PATH/MODULATION MENU ITEM (14) IS USED TO SELECT THE ONBOARD SERIAL FIR FILTERS

TABLE 1. EXAMPLE CONFIGURATION FILE DEFINITIONS

NO.	FILE NAME	MODULATION FORMAT	SYMBOL RATE (KSps)	DATA RATE (KBps)	FILTER TYPE
1	b1024rrc.cfg	BPSK	1024	1024	Square Root of Raised Cosine
2	b128fir.cfg	BPSK	128	128	Serial FIR
3	b128i&d.cfg	BPSK	128	128	Integrate and Dump
4	b128rrc.cfg	BPSK	128	128	Square Root of Raised Cosine
5	b19p2i&d.cfg	BPSK	19.2	19.2	Integrate and Dump
6	b1p23i&d.cfg	BPSK	1.23	1.23	Integrate and Dump
7	b1p2i&d.cfg	BPSK	1.2	1.2	Integrate and Dump
8	b256rrc.cfg	BPSK	256	256	Square Root of Raised Cosine
9	b2.4i&d.cfg	BPSK	2.4	2.4	Integrate and Dump
10	b32i&d.cfg	BPSK	32	32	Integrate and Dump
11	b32rrc.cfg	BPSK	32	32	Square Root of Raised Cosine
12	b4p8i&d.cfg	BPSK	4.8	4.8	Integrate and Dump
13	b512rrc.cfg	BPSK	512	512	Square Root of Raised Cosine
14	b64i&d.cfg	BPSK	64	64	Integrate and Dump
15	b64rrc.cfg	BPSK	64	64	Square Root of Raised Cosine
16	b9p6i&d.cfg	BPSK	9.6	9.6	Integrate and Dump
17	q1024rrc.cfg	QPSK	1024	2048	Square Root of Raised Cosine
18	q128i&d.cfg	QPSK	128	256	Integrate and Dump
19	q128rrc.cfg	QPSK	128	256	Square Root of Raised Cosine
20	q1544rrc.cfg	QPSK	1544	3088	Square Root of Raised Cosine
21	q2048rrc.cfg	QPSK	2048	4096	Square Root of Raised Cosine
22	q256rrc.cfg	QPSK	256	512	Square Root of Raised Cosine
23	q32i&d.cfg	QPSK	32	64	Integrate and Dump
24	q32rrc.cfg	QPSK	32	64	Square Root of Raised Cosine
25	q512rrc.cfg	QPSK	512	1024	Square Root of Raised Cosine
26	q64i&d.cfg	QPSK	64	128	Integrate and Dump

TABLE 2. EXAMPLE FIR FILTER COEFFICIENT FILES

NO.	FILE NAME	SQUARE ROOT OF RAISED COSINE FILTER α	NUMBER OF TAPS	FILTER SPAN (SYMBOLS)	FILTER DECIMATION	REQUIRED DQT OUTPUT RATE
1	rrc2a2x	0.2	16	8	None	2 x Symbol Rate
2	rrc2a4x	0.2	32	8	2	4 x Symbol Rate
3	rrc2a8x	0.2	64	8	4	8 x Symbol Rate
4	rrc35a2x	0.35	16	8	None	2 x Symbol Rate
5	rrc35a4x	0.35	32	8	2	4 x Symbol Rate
6	rrc35a8x	0.35	64	8	4	8 x Symbol Rate
7	rrc4a2x	0.4	16	8	None	2 x Symbol Rate
8	rrc4a4x	0.4	32	8	2	4 x Symbol Rate
9	rrc4a8x	0.4	64	8	4	8 x Symbol Rate
10	rrc5a2x	0.5	16	8	None	2 x Symbol Rate
11	rrc5a4x	0.5	32	8	2	4 x Symbol Rate
12	rrc5a8x	0.5	64	8	4	8 x Symbol Rate

Summary

The HSP50110/210EVAL kit includes software that enables the user to configure the hardware for data processing. Example configuration files represent a variety of symbol rates, filtering and modulation formats. Additional files are provided for using the onboard serial FIR filters. The following recommendations will facilitate your use of the HSP50110/210EVAL kit:

1. It is recommended that users conform to the conventions used for naming both the configuration and FIR filter files, minimizing confusion when seeking application assistance.
2. It is critical that the user understand that the evaluation board outputs data at symbol rate, not the data rate. Setup problems masked when operating in the BPSK format, come to confuse the operator when higher level modulation formats are invoked. Review of the material on the first section of this application note can avoid the most common mistakes in modulator and demodulator test setups. QPSK and 8PSK modulators are likely to input data at the data rate, rather than the symbol rate, especially if the units have integral encoders. The HSP50110/210EVAL outputs I and Q data at the symbol rate, not the data rate. External generation of 2X or 3X clocks may be required to re-multiplex the data into a single data stream if decoding is not employed. Decoders generally require the I and Q symbols to properly perform decoding.
3. It is also recommended that users begin with one of the example configurations, rather than attempt an original configuration creation. The user needs to become familiar with the operation of the evaluation board before attempting the process of configuration design.
4. Users that wish to design application specific FIR filters should begin with the FIR configuration example. The second step should be to select a different FIR filter file for the example configuration. The third step is to use SERINADE to create an application specific FIR file. Following these steps will introduce the user to the operation of the evaluation board, the example configuration files, the example filter files and the SERINADE filter design software in a methodical order, minimizing confusion and reducing the likelihood of mistakes.
5. In standard Bit Error Rate Testers (BERT), maximal length sequences are used as the PseudoRandom test sequences. Common code lengths are 2^7-1, 2^{10}-1, 2^{15}-1, and 2^{23}-1. One of the properties of these codes is that if every other bit of the sequence is selected, the original sequence will be generated at the lower rate at a new phase of the code. This property can be useful when testing the card in the QPSK mode when regeneration of the composite data rate cannot be done. The receive BERT should be set to the same code length as the transmit BERT but the symbol rate is entered as the operating rate. Either I or Q is connected to the BERT. Bit Error Rate data can be taken at the symbol rate. Note that imperfections in implementing the modulator (I/Q imbalance, d.c. offset, orthogonality, etc.) may degrade the BER of the individual channels (I or Q) at one or more of the lock points. Ideally, the BER at each lock point (2 for BPSK, 4 for QPSK, and 8 for 8PSK) will be identical. By taking an average of the BER on the I and Q Channels at the various lock points, the composite I/Q BER can be calculated.

APPNOTE

No. AN9661 January 1997

Digital Signal Processing

Implementing Polyphase Filtering with the HSP50110 (DQT) HSP50210 (DCL) and the HSP43168 (DFF)

Authors: John Henkelman and David Damerow

Introduction

Polyphase resampling filters are often used for timing adjustments in bit synchronizer loops. They are most commonly used at high baud rates where the sample rate to baud rate ratio (F_S/R_{Baud}) is low. The HSP50110 Digital Quadrature Tuner (DQT) and HSP50210 Digital Costas Loop (DCL) chips support NCO driven polyphase resampling filtering when the HSP43168 Dual FIR Filter (DFF) is inserted between them. This application note will address use of the DQT, DFF and DCL in the polyphase filtering configuration.

Polyphase Filtering Overview

In polyphase resamplers, the process can be conceptually described as interpolation to a high rate, followed by a decimation to the desired lower rate. In practice, the process is done in a single step by changing the filter coefficients.

For example, in a 3/5 resampler, the input is interpolated by three using three sets of coefficient phases 0, 1, and 2. The interpolated signal is then decimated by 5, discarding 4/5 of the phases. The two steps are combined by computing three outputs for every five inputs. The resulting phases are:

$IOUT_0 = 0_A$;
$IOUT_1 = 2_B$;
$IOUT_1 = 1_D$;
$IOUT_2 = 0_F$;
$IOUT_3 = 0_F$;

as shown in Table 1. One can see by inspection, that the same result can be accomplished by providing unique sets of coefficients and applying the appropriate filter coefficient set to the input data at the desired output rate. A unique coefficient set is required for every interpolated phase of the data, in this example - 3.

DQT/DCL Resampling Capabilities

The DQT/DCL have four design elements which enable polyphase filtering to be accomplished:

1. A resampling NCO with carry output
2. A latched resampling NCO phase word: SPH(4:0)
3. A programmable clock counter with carry output
4. A strobe, SSTRB, latched synchronous to both the Resampler NCO carry and the programmable clock counter carry.

In the DQT/CDL implementation, the resampling ratio is controlled by the resampling NCO. The ratio can be both irrational and variable. The DQT is fixed (controlled by a counter) at an output sample rate faster than the desired rate. The resampling NCO and the DFF are used to choose when to compute the next output and which interpolation phase to use. The DFF can store up to 32 filter phases (coefficient sets). This gives a timing resolution of ~3% of a symbol time.

TABLE 1. INTERPOLATE BY 3 DECIMATE BY 5

INPUT DATA	INTERPOLATE BY 3 DATA	DECIMATE BY 5 DATA
I_A	0_A	$IOUT_0$
	1_A	
	2_A	
I_B	0_B	
	1_B	
	2_B	$IOUT_1$
I_C	0_C	
	1_C	
	2_C	
I_D	0_D	
	1_D	$IOUT_2$
	2_D	
I_E	0_E	
	1_E	
	2_E	
I_F	0_F	$IOUT_3$

The DQT resampling NCO is programmed for the desired output sample rate. When the NCO rolls over, it sets a flag internally so that the NCO's phase, SPH(4:0), is sampled and the SSTRB signal is asserted aligned with the next output sample. The SSTRB signal indicates that a FIR computation is required. The SPH(4:0) signals hold the NCO phase at the output sample time, indicating which filter interpolation coefficient set to use.

PolyPhase Filter Design

The coefficients for the interpolation phases are generated by designing the filter at the interpolated rate (32x the input sample rate since there are five bits of phase represented in SPH(4:0)) with desired passband at <1X in input sample rate. With the DFF (without alternating the FWD and RVRS data), the prototype filter would have (32 phases x 8 taps) 256 taps. These taps are divided into the 32 filter phases by taking every 32^{nd} sample and storing the result as coefficient sets 0 through 31. The first coefficient set would be C0, C32, C64, C96, C128, C160, C193, and C224. The last coefficient set would be C31, C63, C95, C127, C159, C192, C223, and C255. **Note: Preadders in the DFF cannot be used since interpolation phase coefficients are asymmetric.**

Decimation can be used if fewer interpolation phases are used - for example 16 coefficient phases can be realized by decimating by two. Because the resampling filter has only an 8 sample span (4 symbol), the short span yields relatively gradual transition band roll off, making it a poor shaping filter.

Implementing a Resampling Filter Using the DQT, DCL and the DFF

There are several configurations for implementing polyphase filtering using the HSP50110 (DQT) and HSP50210 (DCL) with external FIR filters. Three distinct operational cases which are related to the selected input mode of the input controller of the DQT are: Normal, Gated, and Interpolated. This application note addresses only the Normal Input Mode, which has the $\overline{ENI}$ input to the DQT tied low. Bit position 1 of Control Address = 4 should be set high (1), selecting the gated mode. Hardwiring $\overline{ENI}$ will continuously gate the input.

Consider the implementation shown in Figure 1. The $\overline{SSTRB}$ and the SPH0-4 are used to gate the output of the filter address the filter and the coefficients respectively. Note that the $\overline{SSTRB}$ must be delayed an amount equivalent to the filter, to properly gate the filter output into the HSP50210 via the $\overline{SYNC}$ input signal. Using the fine phase address bits in SPH0-4, 32 filter phases (coefficient sets) can be realized.

The clocking and control of the FIR using CLK, $\overline{SSTRB}$, $\overline{SYNC}$, DATARDY and SPH0-4 becomes critical. Figure 2 outlines the configuration required. It is very important to understand the relationship between the various DQT clock and control outputs.

CLK, the Programmable Divider, and the Re-Sampler NCO

The Programmable Divider must be configured to have CLK (the DQT input sample clock) as the clock source, rather than the Re-Sampler NCO carry out. To select CLK as the source, BIT 18 of DESTINATION ADDRESS 5 must be set to "1". The Programmable Divider (Destination Address 5 Bit 6 to 17) is set to a value of 2^n, where n = 0, 1, 2, or 3. This generates a CIC Filter Clock that is CLK, CLK/2, CLK/4 or CLK/8, respectively. This clock will be gated to become the $\overline{DATARDY}$ signal, and will be used to gate the data into the external FIR filter. This selection of the Programmable Divider determines the SPH_OUT_SEL settings for the shifter or the Re-Sampler Phase output bits. Table 2 details the required settings.

TABLE 2. DIVIDER AND PHASE SHIFT SETTINGS

PROGRAMMABLE DIVIDER	SHIFTER SETTINGS
0H	11
1H	10
3H	01
7H	00

Note that when the CIC Filter is clocked at CLK rate, no shifting occurs. Similarly, when the CIC Filter is clocked at CLK/8 rate, the shifter selects the phase bits fourth from the top as the MSB.

We desire finer phase resolution of a single decimated sample time. The Programmable Divider output, which is DQT CIC and DQT CIC compensation filter clock, is one positive (programmable positive or negative) pulse the width of one input sample clock period.

Note that the input sample clock (CLK) is the clock that should be used to clock the FIR filter input. The $\overline{DATARDY}$ signal will be used to enable the FIR filter input data sampling at the decimated rate.

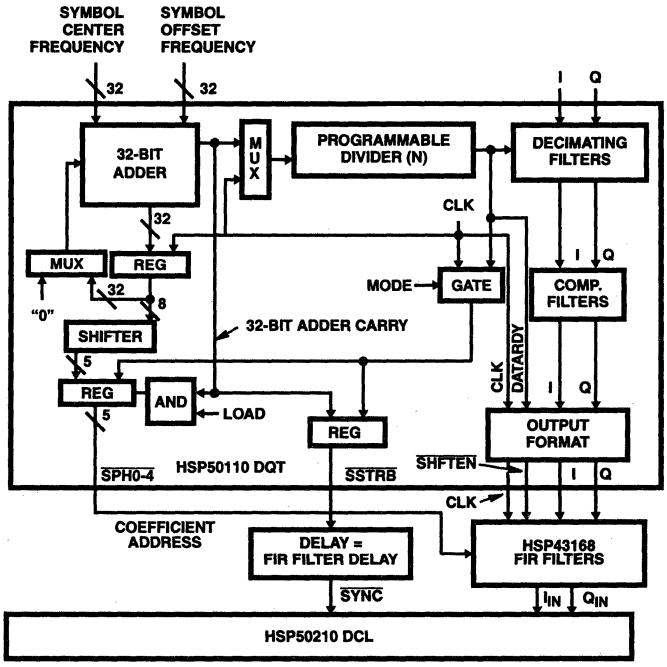


FIGURE 1. SIGNAL GENERATION FOR POLYPHASE FILTERING WITH HSP50110/HSP50210

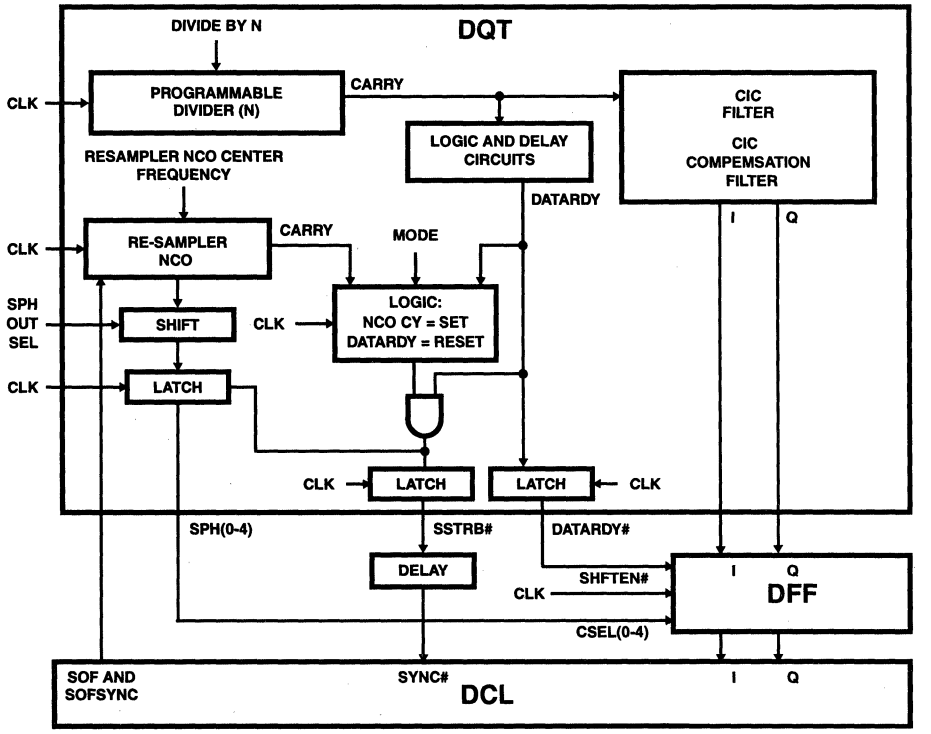


FIGURE 2. CLOCK AND CONTROL CONNECTIONS FOR POLYPHASE FILTERING

The $\overline{\text{SSTRB}}$ Signal and the Re-Sampler Phase Output

The Re-Sampler NCO is programmed to the desired sample frequency of the DCL input. It is not connected to clock any hardware in the DQT. This NCO provides a carry output, which identifies the zero phase location. Additionally, 5 bits of phase resolution are provided. The $\overline{\text{SSTRB}}$ signal is the gated version of the carry out of the Re-Sampler NCO.

There are two selectable modes of operation for the $\overline{\text{SSTRB}}$ signal. The first mode is an asynchronous continuous mode, where the carry out is passed directly out of the chip without concern for the timing of the programmable counter. The carry out is updated with every CLK rising edge. Do not use the asynchronous continuous mode for this application.

The second mode synchronizes the carry output pulse with the rising clock edge out of the programmable counter. Program BIT POSITION 13 of DESTINATION ADDRESS = 6 to be "0". This gating will "synchronize" the $\overline{\text{SSTRB}}$ and the 5 bits of sampler phase to the $\overline{\text{DATARDY}}$ signal. The synchronization occurs during gating and the gate will occasionally prevent the $\overline{\text{SSTRB}}$ and phase signals from their expected location, because they did not occur aligned with the $\overline{\text{DATARDY}}$ signal (during that output sample period).

The frequency of the Re-Sampler NCO carry out is equal to the programmed Re-Sampler NCO Center Frequency value multiplied by the frequency of CLK, scaled to 32 bits of resolution. If there is a Symbol Offset Frequency offset term, the sum of the offset and the center frequencies is multiplied by the frequency of CLK, and scaled to 32-bit resolution. This is detailed in Equation 1.

$$FCO = Fs \times (SCF + SOF)/2^{32} \qquad \text{(EQ. 1)}$$

where FCO = the frequency of the Re-Sampler NCO carry out; Fs = the DQT input sampling frequency (CLK); SCF = the Sampler Center Frequency; SOF = Sampler Offset Frequency.

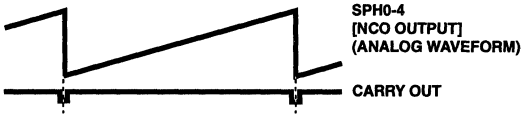


FIGURE 3. THE CARRY OUT SIGNAL RELATIONSHIP TO RE-SAMPLER PHASE BITS

NOTES:

1. Because the SCF and SOF are both 32-bit words, the maximum value for the parenthetical expression is (FFFFFFFF + FFFFFFFF)/ 2^{32}= 2, which yields an erroneous value of greater than one for the multiplier of the sampling frequency F_S. This will cause the NCO to "rollover". If the sum of these two values (SCF + SOF) are kept less than 2^{32}, rollover will not be an issue.
2. If the value of SCF is a multiple of 2, then there will be no jitter on the carry out of the NCO (and thus no jitter on the decimation filter clock or the $\overline{\text{DATARDY}}$ signal) so long as the SOF is zero. But as SOF adjusts the phase of the NCO, jitter on the order of one NCO clock will be introduced due to the non-integer value of the sampling frequency multiplier (SCF + SOF)/ 2^{32}.
3. If the value of SCF is not a multiple of 2, then there will be jitter on carry out of the NCO on the order of one NCO clock due to the non-integer value of the sampling frequency multiplier (SCF)/2^{32}. As the SOF signal adjusts the phase of the NCO, the jitter will remain, except on those rare moments when the sum of SOF and SCF is a multiple of 2.

Figure 3 shows the relationship to the NCO output values and the frequency of the NCO carry out signal. SPH (0-5) are 5 MSB's selected from the top 8 bits of the NCO output word. It is these bits that will be used to provide finer sampler phase resolution to address the coefficient sets in the FIR filter. A programmable shifter selects which 5 of the 8 MSB's are used as the sampler phase output. Up to thirty two symbol phase values can be achieved with these 5 bits. The shifter scaling retains the 32 state resolution for most NCO frequencies. These 5 bits should be connected to the FIR filter coefficient address lines.

The External FIR Filter

A FIR filter is used to provide for the resampling of the DQT output with timing associated with the Re-Sampler NCO frequency. Figure 4 shows a typical filter response for this FIR filter. The filter is designed as an Interpolate by 32/Decimate by n filter. The Interpolate by 32 is a "virtual" interpolation, since the part is being clocked at CLK rate, but enabled at the $\overline{\text{DATARDY}}$ rate. The FIR decimation rate is with respect to the $\overline{\text{DATARDY}}$ enable rate, which is the rate at which the FIR shifter is enabled. As shown in Figure 5, the filter must be designed to ensure that the RRC filter in the DCL chip is well within the flat passband of the FIR filter and not corrupted by aliasing. The DFF will aid in, but not be, the primary shaping filter in the receive path.

The HSP43168 dual FIR filter provides the capability to provide both the I and Q filters in a single chip if a 8 tap symmetric filter meets the customer requirements. Each of the 8 taps is used with 32 coefficient sets to yield a total filter of up to 8 x 32 = 256 taps. Another way to look at this is that this provides 8 filter taps per phase. Each of the 32 filter coefficient sets should be programmed with coefficients for different phases of the response. A typical single phase filter response is shown in Figure 6. This response becomes just one of 32 phase responses that as a composite will represent the filter. The main lobe response of composite filter, with 32 phases, is shown in Figure 7.

A Typical Single Phase Filter Response

The DCL will accept the output of the FIR Filter at the FIR decimated rate. These inputs will be enabled by the $\overline{\text{SYNC}}$ input, which is the $\overline{\text{SSTRB}}$ signal delayed by exact processing delay of the FIR Filter. Note that the $\overline{\text{SSTRB}}$ represents the "zero or start" phase sample of the 32 phases of the resampled rate clock. The designer must provide the input processing clock. This processing clock can be the CLK signal from the DQT, since the DCL inputs are enabled by $\overline{\text{SYNC}}$. Thus the effective sampling rate of the DCL is determined by the $\overline{\text{SSTRB}}$ ($\overline{\text{SYNC}}$) signal. The symbol loop filter output of the DCL, SOF and $\overline{\text{SOFSYNC}}$, should be routed to the DCL Re-sampler inputs of the same name.

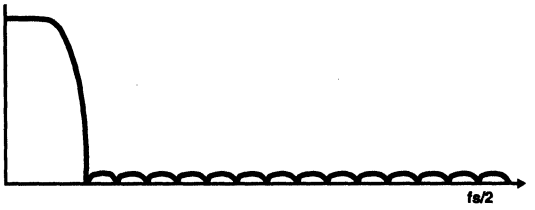


FIGURE 4. A TYPICAL DATA FILTER FOR THE FIR FILTER STRUCTURE

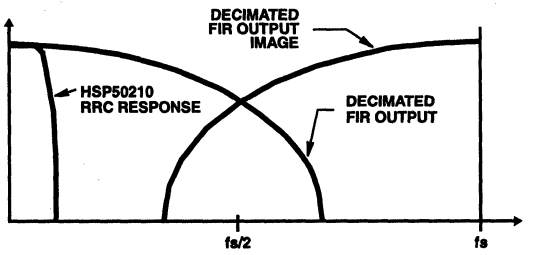


FIGURE 5. KEEPING THE DCL RRC FILTER WELL WITHIN THE FLAT PASSBAND

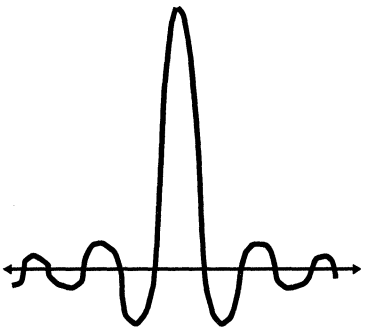


FIGURE 6. A TYPICAL SINGLE PHASE FILTER RESPONSE

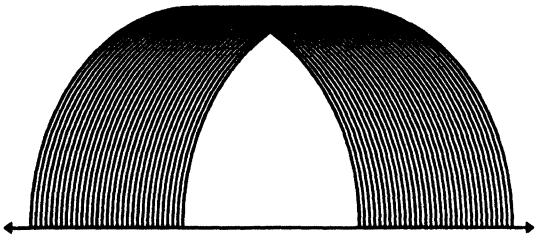


FIGURE 7. THE "MAIN LOBE" COMPOSITE COEFFICIENT FILTER RESPONSE FOR A 32 PHASE FILTER

COMMUNICATIONS 8

HARRIS QUALITY AND RELIABILTY

Harris Quality

Introduction

Success in the integrated circuit industry means more than simply meeting or exceeding the demands of today's market. It also includes anticipating and accepting the challenges of the future. It results from a process of continuing improvement and evolution, with perfection as the constant goal.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force – from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of the Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. In addition to facilitating the development of SPC and DOX, Quality professionals support other continuous improvement tools such as control charts, measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs – with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress.

The Improvement Process

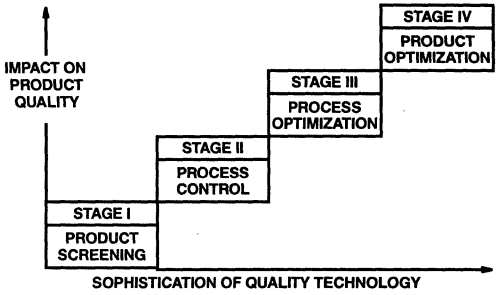


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage III to Stage IV, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

ISO 9000 Certification

The manufacturing operations of Harris Semiconductor have all received ISO certification. The ISO 9000 series of standards were very consistent with our goals to build an even stronger quality system foundation.

Qualified Manufacturing List (QML)

Harris Semiconductor has supplied military grade integrated circuits for over 20 years. The government's certifying body had audited and granted approval to ship JAN, 883 compliant, and Source Military Drawing parts used in ground and space applications. The discipline required to manufacture high reliability components has been beneficial to the commercial product lines. Harris has now taken the next evolutionary step by transitioning into QML as defined in MIL-PRF-38535. These guidelines incorporate the best commercial practices for semiconductor manufacturing.

Designing for Manufacturability

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

AREA	CONTROLS/MONITORS
Wafer Fab	• Internal Audits • Environmental - Room/Hood Particulates - Temperature/Humidity - Water Quality • Product - Junction Depth - Sheet Resistivities - Defect Density - Critical Dimensions - Visual Inspection - Lot Acceptance • Process - Film Thickness - Implant Dosages - Capacitance Voltage Changes - Conformance to Specification • Equipment - Repeatability - Profiles - Calibration - Preventive Maintenance
Assembly	• Internal Audits • Environmental - Room/Hood Particulates - Temperature/Humidity - Water Quality • Product - Documentation Check - Dice Inspection - Wire Bond Pull Strength/Controls - Ball Bond Shear/Controls - Die Shear Controls - Post-Bond/Pre-Seal Visual - Fine/Gross Leak - PIND Test - Lead Finish Visuals, Thickness - Solderability • Process - Operator Quality Performance - Saw Controls - Die Attach Temperatures - Seal Parameters - Seal Temperature Profile - Sta-Bake Profile - Temp Cycle Chamber Temperature - ESD Protection - Plating Bath Controls - Mold Parameters

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (Continued)

AREA	CONTROLS/MONITORS
Test	• Internal Audits • Temperature/Humidity • ESD Controls • Temperature Test Calibration • Test System Calibration • Test Procedures • Control Unit Compliance • Lot Acceptance Conformance • Group A Lot Acceptance
Probe	• Internal Audits • Wafer Repeat Correlation • Visual Requirements • Documentation • Process Performance
Burn-In	• Internal Audits • Functionality Board Check • Oven Temperature Controls • Procedural Conformance
Brand	• Internal Audits • ESD Controls • Brand Permanency • Temperature/Humidity • Procedural Conformance
QCI Inspection	• Internal Audits • Group B Conformance • Group C and D Conformance

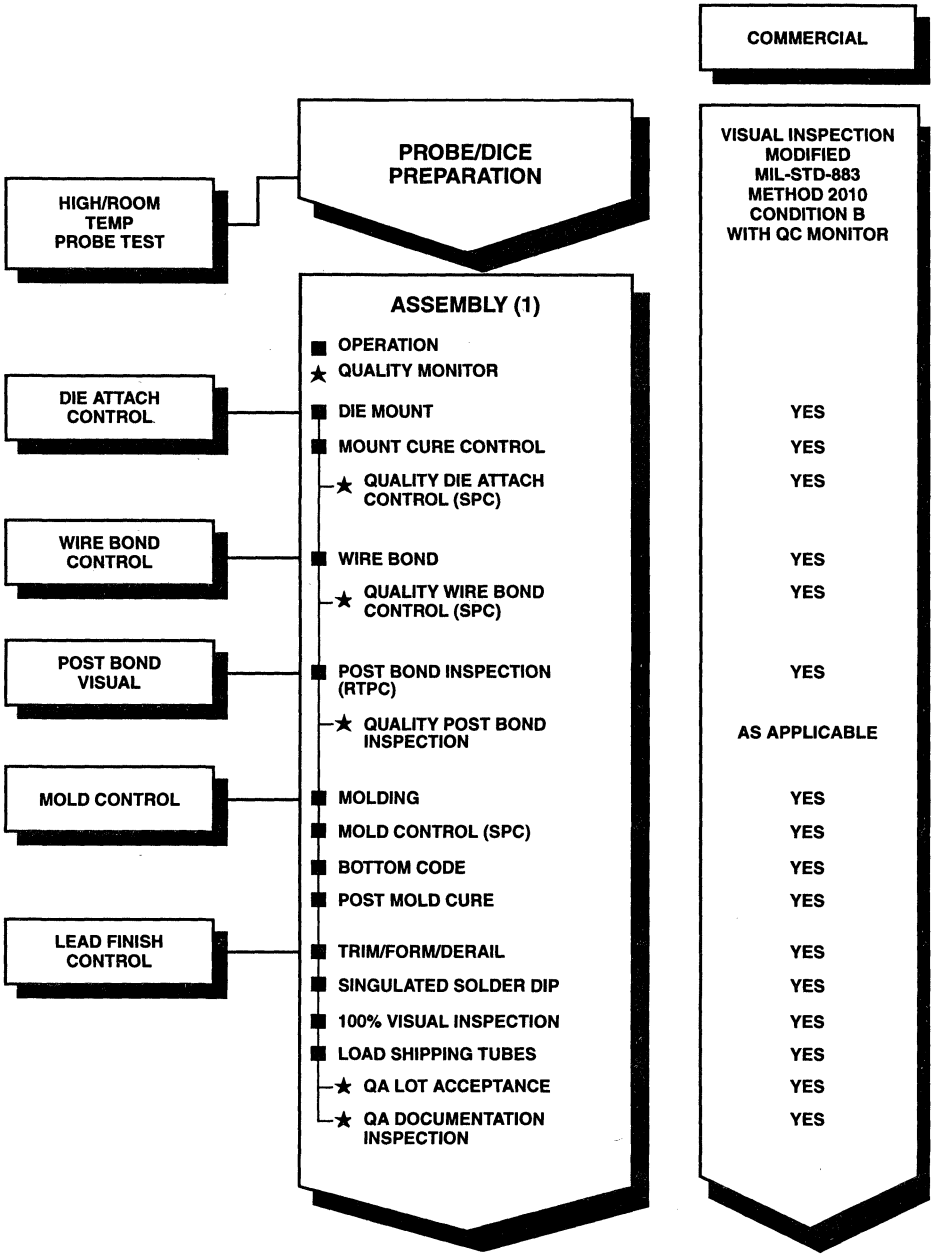
NOTE: QCI Inspection is applicable only to Hi-Rel products.

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 2).

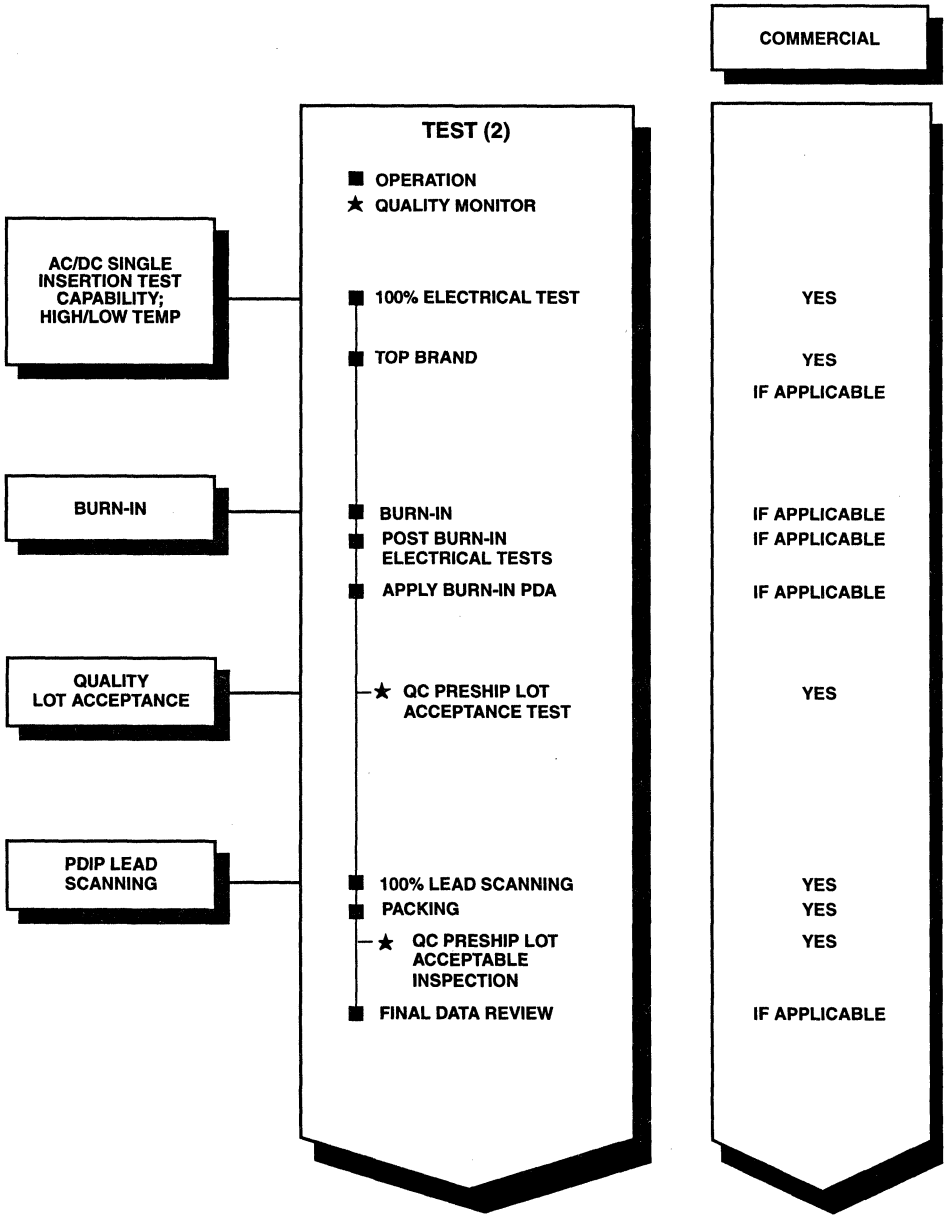


NOTE:

1. Example for a PDIP Package Part

FIGURE 2.

Harris Semiconductor Standard Processing Flow



NOTE:

2. Example for a Linear Part in PDIP Package

FIGURE 3.

TABLE 2. SUMMARIZING CONTROL APPLICATIONS

FAB			
• Diffusion - Junction Depth - Sheet Resistivities - Oxide Thickness - Implant Dose Calibration - Uniformity	• Thin Film - Film Thickness - Uniformity - Refractive Index - Film Composition - Particles Added	• Photo Resist - Critical Dimension - Resist Thickness - Etch Rates - Energy Monitor (E_O)	• Measurement Equipment - Critical Dimension - Film Thickness - Resistivity
ASSEMBLY			
• Pre-Seal - Die Prep Visuals - Yields - Die Attach Heater Block - Die Shear - Wire Pull - Ball Bond Shear - Saw Blade Wear - Pre-Cap Visuals	• Post-Seal - Internal Package Moisture - Tin Plate Thickness - PIND Defect Rate - Solder Thickness - Leak Tests - Module Rm. Solder Pot Temp. - Seal - Temperature Cycle	• Measurement - XRF - Radiation Counter - Thermocouples - GM-Force Measurement	
TEST			
	- Handlers/Test System - Defect Pareto Charts - Lot % Defective - ESD Failures per Month	- Monitor Failures - Lead Strengthening Quality - After Burn-In PDA	
OTHER			
• IQC - Vendor Performance - Material Criteria - Quality Levels	• Environment - Water Quality - Clean Room Control - Temperature - Humidity	• IQC Measurement/Analysis - XRF - ADE - 4 Point Probe - Chemical Analysis Equipment	

Special Testing

Harris Semiconductor offers several standard screen flows to support a customer's need for additional testing and reliability assurance. These flows include environmental stress testing, burn-in, and electrical testing at temperatures other than +25°C. The flow shown in Figure 2 and Figure 3 indicates the Harris standard processing flow for a commercial linear part in a PDIP package. In addition, Harris can supply products tested to customer specifications both for electrical requirements and for nonstandard environmental stress screening. Consult your field sales representative for details.

TABLE 3. HARRIS I.C. DESIGN TOOLS

DESIGN STEP	PRODUCTS	
	ANALOG	DIGITAL
Functional Simulation	Cds Spice	Cds Spice Verilog
Parametric Simulation	Cds Spice Monte Carlo	Cds Spice
Schematic Capture	Cadence	Cadence
Functional Checking	Cadence	Cadence
Rules Checking	Cadence	Cadence
Parasitic Extraction	Cadence	Cadence

Controlling and Improving the Manufacturing Process - SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use control charts to determine the normal variabilities in processes, materials, and products. Critical process variables and performance characteristics are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that an operation is outside the process control limits or indicates a nonrandom pattern inside the limits. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 3 lists some typical manufacturing applications of control charts at Harris Semiconductor.

SPC is important, but still considered only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost (see Table 4).

TABLE 4. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

STAGE		APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at upgrading process performance by studying the key variables controlling the process, and optimizing the procedures or design to yield the best result. This approach is a more time-consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in ANSI/ASQC Z1.4, MIL-STD-883 and MIL-PRF-38535 are used by our quality inspectors.

The focus on this quality parameter has resulted in a continuous improvement to less than 100 PPM, and the goal is to continue improvement toward 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of Harris statisticians, private consultants, and internally developed programs, training of engineers, facilitators, and operators/technicians has been an ongoing activity in Harris Semiconductor.

Over the past years, Harris has also deployed a comprehensive training program for hourly operators and facilitators in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

Incoming Materials

Improving the quality and reducing the variability of critical incoming materials is essential to product quality enhancement, yield improvement, and cost control. With the use of statistical techniques, the influence of silicon, chemicals, gases and other materials on manufacturing is highly measurable. Current measurements indicate that results are best achieved when materials feeding a statistically controlled manufacturing line have also been produced by statistically controlled vendor processes.

To assure optimum quality of all incoming materials, Harris has initiated an aggressive program, linking key suppliers with our manufacturing lines. This user-supplier network is the Harris Vendor Certification process by which strategic vendors, who have performance histories of the highest quality, participate with Harris in a lined network; the vendor's factory acts as if it were a beginning of the Harris production line.

SPC seminars, development of open working relationships, understanding of Harris's manufacturing needs and vendor capabilities, and continual improvement programs are all part of the certification process. The sole use of engineering limits no longer is the only quantitative requirement of incoming materials. Specified requirements include centered means, statistical control limits, and the requirement that vendors deliver their products from their own statistically evaluated, in-control manufacturing processes.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 5. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	TOPICS COVERED
SPC, Basic	Manufacturing Operators, Non-Manufacturing Personnel	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts
SPC, Intermediate	Manufacturing Supervisors, Technicians	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Introduction to Capability
SPC, Advanced	Manufacturing Engineers, Manufacturing Managers	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Advanced Control Charts, Variance Component Analysis, Capability Analysis
Design of Experiments (DOX)	Engineers, Managers	Factorial and Fractional Designs, Blocking Designs, Nested Models, Analysis of Variance, Normal Probability Plots, Statistical Intervals, Variance Component Analysis, Multiple Comparison Procedures, Hypothesis Testing, Model Assumptions/Diagnostics
Regression	Engineers, Managers	Simple Linear Regression, Multiple Regression, Coefficient Interval Estimation, Diagnostic Tools, Variable Selection Techniques
Response Surface Methods (RSM)	Engineers, Managers	Steepest Ascent Methods, Second Order Models, Central Composite Designs, Contour Plots, Box-Behnken Designs
Capability Studies	Techs, Facilitators, Engineers	Capability Indices (C_P and C_{PK}), Variance Components, Nested Models, Fixed and Random Effects

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Taper • Thickness • Total Thickness Variation • Backside Criteria • Oxygen • Carbon	• Equipment Capability Control Charts - Oxygen - Resistivity • Control Charts Related to - Enhanced Gettering - Total Thickness Variation - Total Indicated Reading - Particulates • Certificate of Analysis for all Critical Parameters • Control Charts from On-Line Processing • Certificate of Conformance
Chemicals/Photoresists/ Gases	• Chemicals - Assay - Major Contaminants • Molding Compounds - Spiral Flow - Thermal Characteristics • Gases - Impurities • Photoresists - Viscosity - Film Thickness - Solids - Pinholes	• Certificate of Analysis on all Critical Parameters • Certificate of Conformance • Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Water - Selected Parameters • Control Charts - Assay - Contaminants • Control Charts on - Photospeed - Thickness - UV Absorbency - Filterability - Water - Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Dimensional Characteristics • Certificate of Analysis for all Critical Parameters • Certificate of Conformance
Assembly Materials	• Visual Inspection • Physical Dimension Checks • Glass Composition • Bondability • Intermetallic Layer Adhesion • Ionic Contaminants • Thermal Characteristics • Lead Coplanarity • Plating Thickness • Hermeticity	• Certificate of Analysis • Certificate of Conformance • Process Control Charts on Outgoing Product Checks and In-Line Process Controls

Calibration Laboratory

Another important resource in the product assurance system is a calibration lab in each Harris Semiconductor operation site. These labs are responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both production and engineering areas. The accuracy of instruments used at Harris is traceable to a national standards. Each lab maintains a system which conforms to the current revision of ANSI/NCSL Z540-1.

Each instrument requiring calibration is assigned a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Manufacturing Science - CAM, JIT, TPM

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened - in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Just In Time (JIT)

The major focus of JIT is cycle time reduction and linear production. Significant improvements in these areas result in large benefits to the customer. JIT is a part of the Total Quality Management philosophy at Harris and includes Employee Involvement, Total Quality Control, and the total elimination of waste.

Some key JIT methods used for improvement are sequence of events analysis for the elimination of non-value added activities, demand/pull to improve production flow, TQC check points and Employee Involvement Teams using root cause analysis for problem solving.

JIT implementations at Harris Semiconductor have resulted in significant improvements in cycle time and linearity. The benefits from these improvements are better on time delivery, improved yield, and a more cost effective operation.

JIT, SPC, and TPM are complementary methodologies and used in conjunction with each other create a very powerful force for manufacturing improvement.

Total Productive Maintenance (TPM)

TPM or Total Productive Maintenance is a specific methodology which utilizes a definite set of principles and tools focusing on the improvement of equipment utilization. It focuses on the total elimination of the six major losses which are equipment failures, setup and adjustment, idling and minor stoppages, reduced speed, process defects, and reduced yield. A key measure of progress within TPM is the overall equipment effectiveness which indicates what percentage of the time is a particular equipment producing good parts. The basic TPM principles focus on maximum equipment utilization, autonomous maintenance, cross functional team involvement, and zero defects. There are some key tools within the TPM technical set which have proven to be very powerful to solve long standing problems. They are initial clean, P-M analysis, condition based maintenance, and quality maintenance.

Utilization of TPM has shown significant increases in utilization on many tools across the Sector and is rapidly becoming widespread and recognized as a very valuable tool to improve manufacturing competitiveness.

The major benefits of TPM are capital avoidance, reduced costs, increased capability, and increased quality. It is also very compatible with SPC techniques since SPC is a good stepping stone to TPM implementation and it is in turn a good stepping stone to JIT because a high overall equipment effectiveness guarantees the equipment to be available and operational at the right time as demanded by JIT.

Harris Reliability

Introduction

At Harris Semiconductor, reliability is built into every product by emphasizing quality throughout manufacturing. This starts by ensuring the excellence of the design, layout, and manufacturing processes. The quality of the raw materials and workmanship is monitored using statistical process control (SPC) to preserve the reliability of the product. The primary and ultimate goal of these efforts is to provide full performance to the product specification throughout its useful life.

Reliability Engineering

The Reliability Engineering department is responsible for all aspects of reliability assurance at Harris Semiconductor:

- Charter
  - To ensure that Harris is recognized by our customers and competitors as a company that consistently delivers products with high reliability.

- Mission
  - To develop systems for assessing, enhancing, and assuring that quality and reliability are integrated into all aspects of our business.

- Vision
  - To establish excellence and integrity through all design and manufacturing processes as it relates to quality and reliability.

Values

- To be considered responsive and service oriented by our customers.
- To be acknowledged by Harris as a highly qualified resource for reliability assurance, product analysis, and electronic materials characterization.
- To successfully utilize the organization's talents through trained, empowered employees/employee team participation.
- To maintain an attitude of integrity, dignity and respect for all.

Strategy

- To provide quantitative assessments of product reliability focusing on the identification and timely elimination of design and processing deficiencies that degrade product performance and operating life expectancy.
- To provide systems for continuous improvement of reliability and quality through the assessment of existing processes, products, and packages.
- To perform product analysis as a means of problem solving and feedback to our customers, both internal and external.
- To exercise full authority over the internal qualifications of new products, processes, and packages.

The reliability organization is comprised of a team that possesses a broad cross section of expertise in these areas:

- Custom Military (Radiation Hardened)
- Automotive ASICs
- Harsh Environment Plastic Packaging
- Advanced Methods for Design for Reliability (DFR)
- Strength in Power Semiconductor
- Chemical/Surface Analysis Capabilities
- Failure Analysis Capabilities

The reliability focus is customer satisfaction (external and internal) and is accomplished through the development of standards, performance metrics, and service systems. These major systems are summarized below:

- A process and product development system known as ACT PTM (Applying Concurrent Teams to Product-To-Market) has been established. The ACT PTM philosophy is one of new product development through a team that pursues customer involvement. The team has the authority, responsibility, and training necessary to successfully bring the product to market. This not only includes product definition and design, but also all manufacturing capabilities as well.
- Standard test vehicles (over 100) have been developed for process characterization of wear-out failure mechanisms. These vehicles are used for conventional stresses (for modeling failure rates) and for wafer level reliability characterization during development.
- Common qualification standards have been established for all sites.
- A reliability monitoring system (also known as the Matrix monitoring system) is utilized for products in production to ensure ongoing reliability and verification of continuous improvement.
- The field return system is designed to handle a variety of customer issues in a timely manner. Product issues are often handled by routing the product into the PFAST (Product Failure Analysis Solution Team) system. Return authorizations (RAs) are issued where an entire lot of product needs to be returned to Harris. The Customer Return Services (CRS) group is responsible for the administration of this system (see Customer Return Services.)
- The PFAST system has been established to expedite failure analysis, failure root cause determination, and corrective actions for field returns. PFAST is a team effort involving many functional areas at all Harris sites. The purpose of this system is to enable Harris's Field Sales and Quality operations to properly route, track, and respond to our customer's needs as they relate to product analysis.

Design for Reliability (Wear-Out Characterization)

The concept of "Design for Reliability" focuses on moving reliability assessment away from tests on sample product to a point much earlier in the design cycle. Effort is directed at building in and verifying the reliability of a new process well before manufacture of the first shippable product that uses that technology. This gives these first new products a higher probability of success and achieves reduced product-to-market cycle times.

In practice, a set of standardized test vehicles containing special test structures are transferred to the new process using the layout ground rules specified for that process. Each test structure is designed for a specific wear-out failure mechanism. Highly accelerated stress tests are performed on these structures and the results can be extrapolated to customer use conditions. Generally, log-normal statistics are used to define wear-out distributions for the life prediction models. The results are used to establish reliability design ground rules and critical node lists for each process. These ground rules and critical nodes ensure that wear-out failures do not occur during the customer's projected use of the product.

Process/Product/Package Qualifications

Once the new process has successfully completed wear-out characterization, the final qualification consists of more conventional testing (e.g. biased life, storage life, temp cycle etc.). These tests are performed on the first new product designs (sampled across multiple wafer production lots). Successful completion of the final qualification tests concurrently qualifies the new process and the new products that were used in the qualification. Subsequent products designed within the now-established ground rules are qualified individually prior to introduction. New package configurations are also qualified individually prior to being available for use with new products.

Harris's qualification procedures are specified via controlled documentation and the same standard is used at Harris's sites worldwide. Figure 4 gives more information on the new process/product development and life cycle.

Product/Package Reliability Monitors

Many of the accelerated stress-tests used during initial reliability qualification are also employed during the routine monitoring of standard product. Harris's continuing reliability monitoring program consists of three groups of stress tests, labeled Matrix I, II and III. Table 6 outlines the Matrix tests used to monitor plastic packaged ICs in Harris's off-shore assembly plants, where each wafer fab technology is sampled. Matrix I consists of highly accelerated, short duration (typically 48 hours) tests, sampled biweekly, which provide real-time feedback on product reliability. Matrix II consists of the more conventional, longer term stress-tests, sampled monthly, which are similar to those used for product qualification. Finally, Matrix III, performed monthly on each package style, monitors the mechanical reliability aspects of the package. Any failures occurring on the Matrix monitors are fully analyzed and the failure mechanisms identified, with containment and corrective actions obtained from Manufacturing and Engineering. This information along with all of the test results are routinely transmitted to a central data base in Reliability Engineering, where failure rate trends are analyzed and tracked on an ongoing basis. These data are used to drive product improvements, to ensure that failure rates are continuously being reduced over time.

Reliability data, including the Matrix Monitor results, can be obtained by contacting your local Harris sales office.

TABLE 7. PLASTIC PACKAGED IC MONITORING TESTS

MATRIX I

TEST	CONDITIONS	DURATION	SAMPLE/ LTPD
Autoclave	+121°C, 100%RH, 15PSIG	96 Hours	45/5
Biased Life	+175°C	48 Hours	45/5
Biased Life	+125°C	48 Hours	45/5
HAST	+135°C, 85% RH	48 Hours	45/5
Thermal Shock	-65°C to +150°C	200 Cycles	45/5

MATRIX II

TEST	CONDITIONS	DURATION	SAMPLE/ LTPD
Autoclave	+121°C, 100%RH, 15PSIG	192 Hours	45/5
Biased Humidity	+85°C, 85% RH	1000 Hours	45/5
Biased Life	+125°C	1000 Hours	45/5
Dynamic Life	+125°C	1000 Hours	45/5
Storage Life	+150°C	1000 Hours	45/5
Temp. Cycle	-65°C to +150°C	1000 Cycles	45/5

MATRIX III

TEST	CONDITIONS	SAMPLE/LTPD
Brand Adhesion	MIL-STD-883/2015	15/15
Flammability	(UL-94 Vertical Burn)	11/20
Lead Fatigue	MIL-STD-883/2004	15/15
Physical Dimensions	MIL-STD-883/2016	11/20
Solderability	MIL-STD-883/2003	45/15

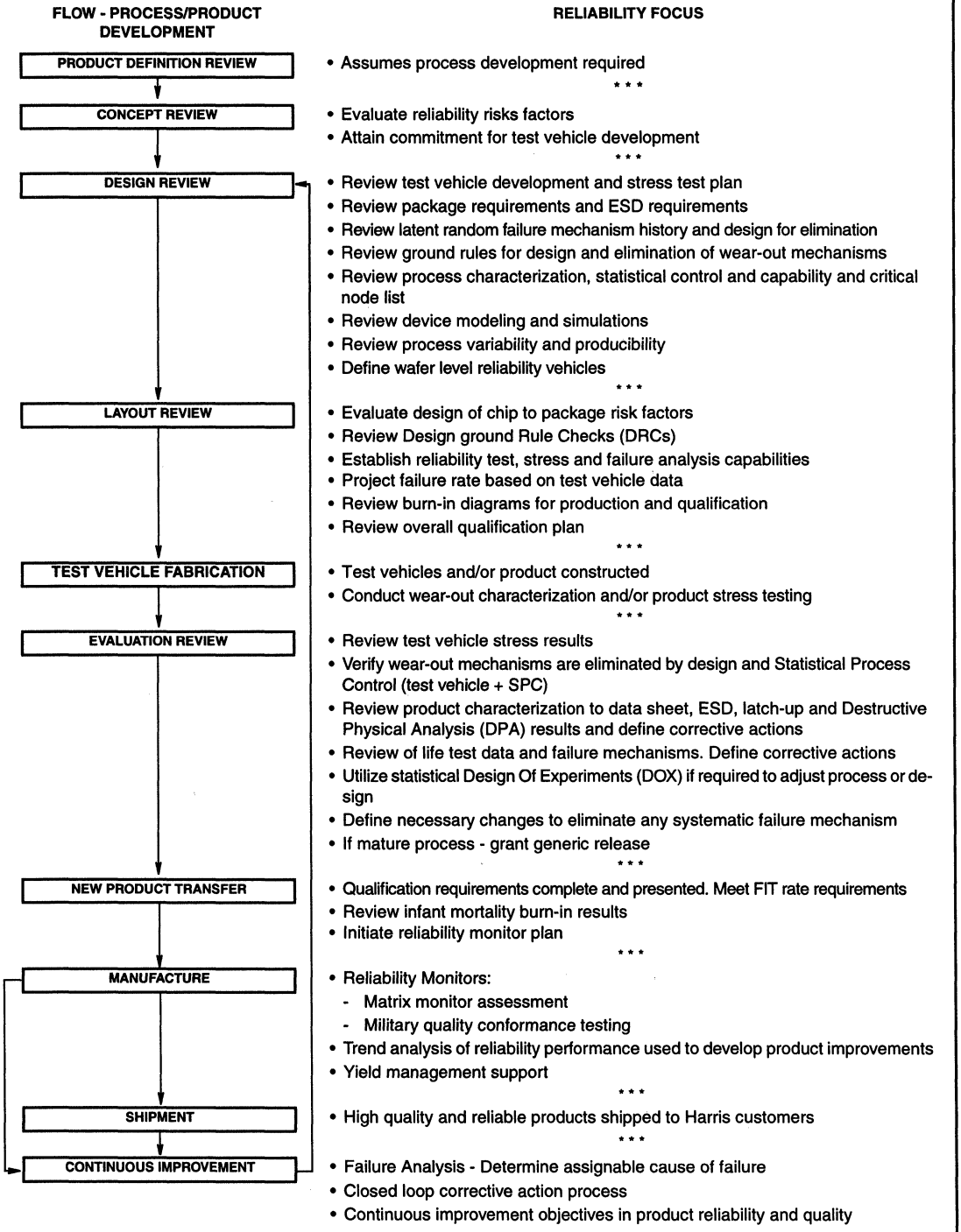


FIGURE 4. NEW PROCESS/PRODUCT DEVELOPMENT AND LIFE CYCLE

Customer Return Services

Harris places a high priority on resolving customer return issues. The Customer Return Services (CRS) department is responsible for determining the best manner to handle a return issue as illustrated in Figure 5.

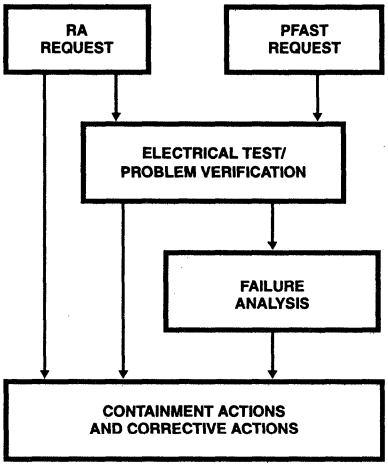


FIGURE 5. GENERAL RETURN FLOW

The diversity of return reasons requires that many different organizations be involved to test, analyze, and correct field return issues. The CRS group coordinates the responses from the supporting organizations to drive closure of issues within the customer response time requirements, see Table 7. The results from the work performed on customer returns are used to initiate corrective actions and continuous improvements within the factories.

The two methods used to return devices are by a RA (Return Authorization) request or by a PFAST (Product Failure Analysis Solution Team) request. The main difference between RA and PFAST is that the PFAST requests often require extensive analysis and a more formal response to the customer. All returns follow the same general procedure from the customer's perspective as seen in steps one to four of the customer return procedure.

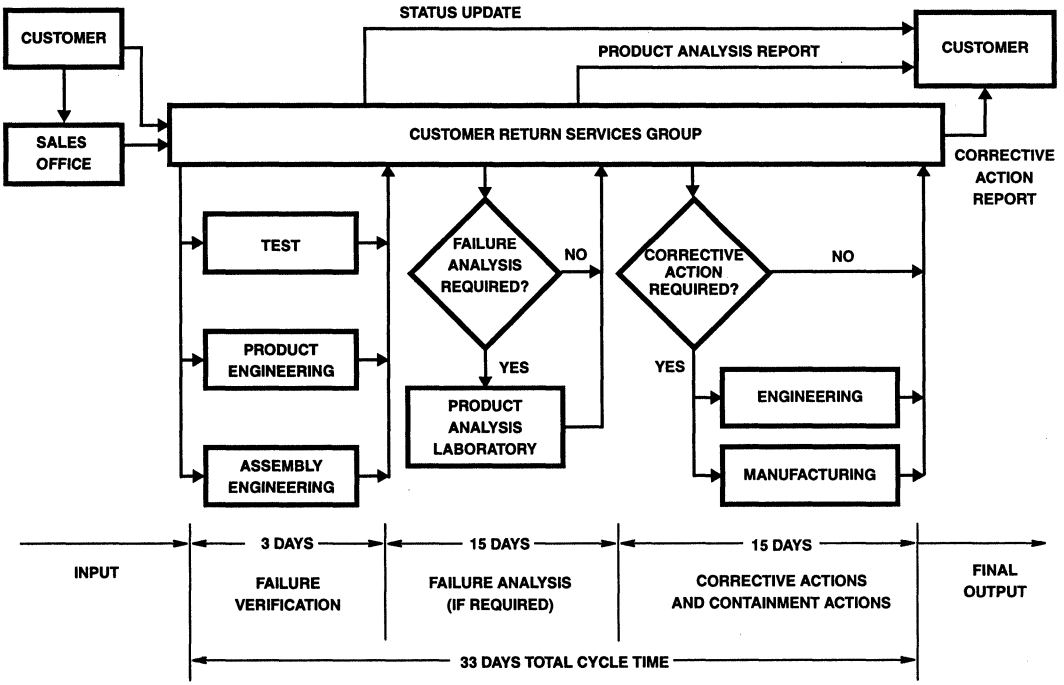
- **Step 1** - Customer or Sales office contacts the Customer Return Services department. If a return is to be routed into the PFAST system, then a PFAST Action Request (see the PFAST form in this section) needs to be completed to understand the customer's issue and direct the analysis efforts.
  - **Phone Number: (407)-724-7400**
  - **FAX Number: (407)-724-7658**
  - **Internet: creturn@harris.com**
  - **PROFS: CRETURN**
- **Step 2** - The Customer Return Services department notifies all affected sales, factory, and engineering organizations of the issue.
- **Step 3** - When product is received, the issue is verified and any required analysis is performed. Where applicable, a preliminary analysis report is sent to the customer.
- **Step 4** - A determination of the root cause of failure initiates the corrective actions to address the source of the problem. A final corrective action report is sent to the customer if requested.

The RA request is used to return and replace an entire lot of product. The lot is returned to Harris for replacement or credit. Once the product is received various tests and evaluations will be performed to determine the appropriate actions that should be taken to resolve any problems or issues.

A PFAST request is used to return a small sample for analysis of a problem. The ultimate outcome of both types of requests is to determine corrective actions that would preclude the same problem occurring in the future. Where appropriate, a containment plan is also implemented to prevent a re-occurrence of the problem in the field. The customer return flow diagram (Figure 6) provides the typical activities and cycle times for processing a PFAST request.

TABLE 8. CUSTOMER RETURN SERVICES

CHARTER	MISSION	RESPONSIBILITIES
To resolve product quality issues while providing feedback to both external and internal customers to facilitate corrective actions and continuous improvement of the product.	To provide a single point interface between the customer and the factory for resolving technical problems, issues, and field returns.	1. Maintain customer return history. 2. Track returns through the factory. 3. Establish a history library of problems and corrective actions. 4. Ensure closure with customers.



NOTE: The days indicated are the typical number of 'working days' not calendar days. Analysis difficulty and the nature of the corrective actions may either improve or degrade the total cycle time.

FIGURE 6. CUSTOMER RETURN FLOW DIAGRAM

HARRIS SEMICONDUCTOR

PFAST ACTION REQUEST

(Product Failure Analysis Solution Team)

Request # _____

Date: _____

Originator _____	Customer _____
Company/Phone No. _____	Location _____
Device Type/Part No. _____	Customer's Reference No. _____
No. Samples Returned _____	Quantity Received _____

Instructions and requirements are on the back of this form.

Has Field Applications been contacted for assistance? ☐ No ☐ Yes - Who was contacted _____

SOURCE OF PROBLEM

(Enter the sequence of events in the boxes provided)

1. Visual/Mechanical
   - ☐ Describe _____
2. Incoming Test ☐ Not Performed
   - ☐ 100% Tested ☐ Sample Tested
   - No. Tested _____ No. of Rejects _____
   - Are results representative of previous lots?
   - ☐ YES ☐ NO
3. In Process/Manufacturing Failure
   - ☐ Board Test ☐ System Test
   - How many units failed? _____
   - Failed after _____hours of testing
   - Was unit retested at incoming inspection?
   - ☐ YES ☐ NO
   - Are results representative of previous lots?
   - ☐ YES ☐ NO
4. Field Failure
   - Failed after _____hours operation
   - Estimated failure rate_____ % per _____
   - End User_____ Location _____
   - Min. _____°C Ave. _____°C Max. _____°C
5. Other

ACTION REQUESTED BY CUSTOMER

Specific Action Requested (Contact PFAST Coordinator for other options)

- ☐ Test Sample for Correlation Only
- ☐ Test Sample for Product Return >$5k
- ☐ Failure Analysis
- ☐ Other

Impact of Failed Units on Customer's Situation: _____

Customer Contact with Specific Knowledge of Rejects

Name _____

Position _____ Phone_____

REASON FOR ELECTRICAL REJECT

(Where appropriate serialize units and specify for each)

Test Conditions Relating to Failure

Tester Used (Mfgr/Model) _____

Test Temperature _____

Test Time ☐ Continuous (T = _____sec) ☐ One Shot (T = _____sec)

Describe any observed condition to which failure appears sensitive _____

1. ☐ DC Failure
   - ☐ Open ☐ Short ☐ Leakage
   - ☐ Power Drain ☐ Input Level ☐ Output Level
   - Pin Number_____
2. ☐ AC Failure
   - Power Supply Voltages = _____V
   - Input Voltages V_{IH} = _____V V_{IL} = _____V
   - Pin Number_____
   - Failing characteristics _____
3. ☐ RAM and ROM Failures (ROM failures must be returned with a good master unit if failure analysis is requested).
   - Address of Failing Location _____
   - Describe Pattern Used (If not standard patterns, give very complete description including address sequence). _____
   - Include timing diagrams and circuit schematic if available.
   - ROM Programmer Used (If purchased unprogrammed) _____

Conformal Coating (Mfgr/Model) _____

Additional Comments:

FIGURE 7. PFAST ACTION REQUEST

INSTRUCTIONS FOR COMPLETING PFAST ACTION REQUEST FORM

The purpose of this form is to help us provide you with a more accurate, complete, and timely response to failures which may occur. Accurate and complete information is essential to ensure that the appropriate corrective action can be implemented. Due to this need for accurate and complete information, requests without a completed PFAST Action Request form will be returned.

Source of Problem:

This section requests the product flow leading to the failure. Mark an 'X' in the appropriate boxes up to and including the step which detected the failure. Also mark an 'X' in the appropriate box under "ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?" to indicate whether this is a rare failure or a repeated problem.

Example 1. No incoming electrical test was performed; the units were installed onto boards; the boards functioned correctly for two hours and then 1 unit failed. The customer rarely has a failure due to the Harris device.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE _____
2. INCOMING TEST ☒ NOT PERFORMED
   ☐ 100% TESTED ☐ SAMPLE TESTED
   NO. TESTED _____ NO. OF REJECTS _____
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ☒ BOARD TEST ☐ SYSTEM TEST
   HOW MANY UNITS FAILED? 1
   FAILED AFTER 2 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ☒ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☒ NO
4. FIELD FAILURE
   FAILED AFTER _____ HOURS OPERATION
   ESTIMATED FAILURE RATE _____% PER _____
   END USER _____ LOCATION _____
   MIN. _____°C AVE. _____°C MAX._____°C
5. OTHER _____

Example 2. 100 out of the 500 units shipped were tested at incoming and all passed. The units were installed into boards and the boards passed. The boards were installed into the system and the system failed immediately when turned on. There were 3 system failures due to this part. The customer frequently has failures of this Harris device. The 3 units were not retested at incoming.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE _____
2. INCOMING TEST ☐ NOT PERFORMED
   ☐ 100% TESTED ☒ SAMPLE TESTED
   NO. TESTED 100 NO. OF REJECTS 0
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☒ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ☒ BOARD TEST ☒ SYSTEM TEST
   HOW MANY UNITS FAILED? 3
   FAILED AFTER 0 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ☒ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☒ YES ☐ NO
4. FIELD FAILURE
   FAILED AFTER _____ HOURS OPERATION
   ESTIMATED FAILURE RATE _____% PER _____
   END USER _____ LOCATION _____
   MIN. _____°C AVE. _____°C MAX._____°C
5. OTHER _____

Action Requested by Customer:

This section should be completed with the customer's expectations. This information is essential for an appropriate response.

Reason for Electrical Reject:

This section should be completed if the type of failure could be identified. If this information is contained in attached customer correspondence there is no need to transpose onto the PFAST Action Request form.

PFAST REQUIREMENTS

The value of returning failing products is in the corrective actions that are generated. Failure to meet the following requirements can cause erroneous conclusion and corrective action; therefore, failure to meet these requirements will result in the request being returned. Contact the local PFAST Coordinator if you have any questions.

Units with conformal coating should include the coating manufacturer and model. This is requested since the coating must be removed in order to perform electrical and hermeticity testing.

1. Units must be returned with proper ESD protection (ESD-safe shipping tubes within shielding box/bag or inserted into conductive foam within shielding box/bag). No tape, paper bags, or plastic bags should be used. This requirement ensures that the devices are not damaged during shipment back to Harris.
2. Units must be intact (lid not removed and at least part of each package lead present). This is a requirement since the parts must be intact in order to perform electrical test. Also, opening the package can remove evidence of the cause of failure and lead to an incorrect conclusion.
3. Programmable parts (ROMs, PROMs, UVEPROMs, and EEPROMs) must include a master unit with the same pattern. This requirement is to provide the pattern so all failing locations can be identified. A master unit is required if a failure analysis is requested.

FIGURE 7. PFAST ACTION REQUEST (Continued)

Product Analysis Lab

The Product Analysis Laboratory capabilities and charter encompass the isolation and identification of failure modes and mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. The primary activities of the Product Analysis Lab are electrical verification/characterization of the failure, package inspection/analysis, die inspection/analysis, and circuit isolation/probing. A variety of tools and techniques have been developed to ensure the accuracy and integrity of the product analysis. This section lists some of the tools and techniques that are employed during a typical analysis.

The electrical verification/characterization of devices failing electrical parameters is essential prior to performing an analysis. The information obtained from the electrical verification provides a direction for the analysis efforts. The following electrical verification/characterization equipment may be used to obtain electrical data on a device:

- HP82000M Mixed Signal Tester
- LV500 ASIC verification system
- LTS2020 Analog tester
- Curve Tracer
- Parametric Analyzer

Prior to die level analysis, package inspection and analysis are performed. These steps are performed routinely since valuable data may not be obtainable once the package is opened. The package inspection and analysis may require the use of some of the following lab equipment:

- X-Ray
- C-Mode Scanning Acoustic Microscope (C-SAM)
- Optical inspection microscopes
- Package opening tools and techniques

Once the device has been opened, die inspection and analysis can be performed. Depending on the type of failure, several tools and techniques may be used to identify the failure mechanism. Usually the faster and easier to use operations are performed first in an attempt to expedite the analysis. The list of equipment and techniques for performing die inspection and analysis is as follows:

- Optical microscopes
- Liquid crystal
- Emission microscope
- Scanning electron microscopes - SEM

The final step of circuit isolation is ready to be performed when an area of the circuit has been identified as the source of the problem through one of the previous analysis efforts. Circuit analysis is performed using the following probing and isolation tools:

- Mechanical probing
- Laser cutter and isolation
- E-Beam probing
- Cross sectioning and chemical deprocessing

A typical analysis flow is shown in the Figure 8 below. The exact analysis steps and sequence are determined as the situation dictates. For the analysis to be conclusive, it is essential that the failure mechanism correlates to the initial product failure conditions. Some failure mechanisms require elemental and chemical analysis to identify the root cause within the manufacturing process. Elemental and chemical analysis tasks are sent to the Analytical Services Lab for further evaluation.

The results of each analysis are entered into a computer data base. This data base is used to search for specific types of problems, to identify trends, and to verify that the corrective actions were effective.

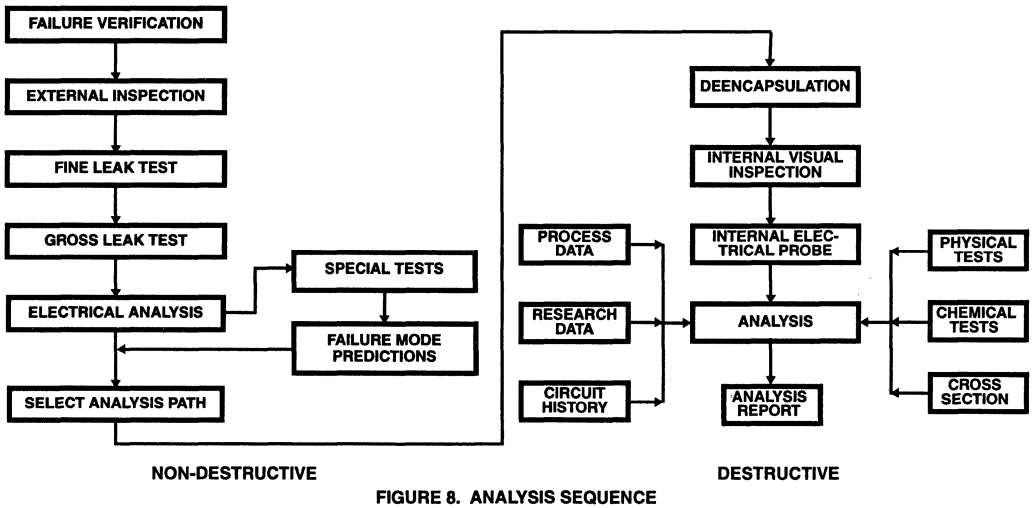


FIGURE 8. ANALYSIS SEQUENCE

Analytical Services Laboratory

Chemical and physical analysis of materials and processes is an integral part of Harris' Total Quality/Continuous Improvement efforts to build reliability into processes and products. Manufacturing operations are supported with real-time analyses to help maintain robust processes. Analyses are run in cooperation with raw material suppliers to help them provide controlled materials in dock-to-stock procurement programs.

Harris facilities, engineering, manufacturing, and product assurance are supported by the Analytical Services Laboratory. Organized into chemical or microbeam analysis methodology, staff and instrumentation from both labs cooperate in fully integrated approaches necessary to complete analytical studies.

The department also maintains ongoing working arrangements with commercial laboratories, universities, and equipment manufacturers to obtain any materials analysis in cases where instrumental capabilities are not available in our own facility. Figure 9 and Figure 10 show the capabilities of each area.

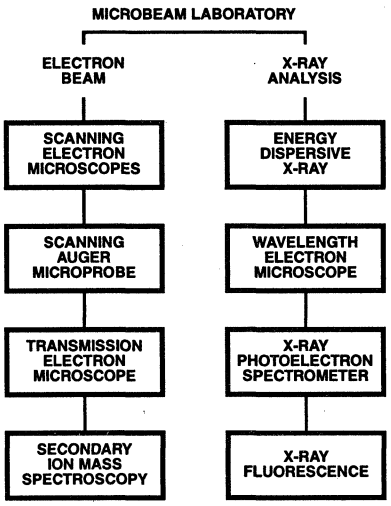


FIGURE 9. MICROBEAM LABORATORY

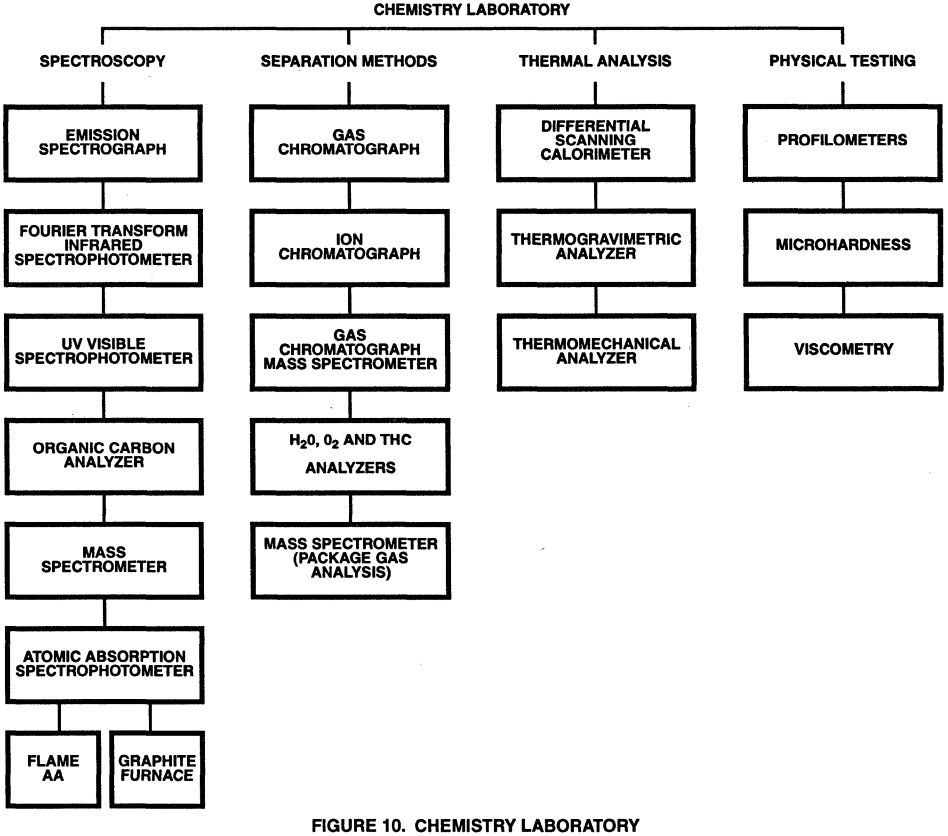


FIGURE 10. CHEMISTRY LABORATORY

Reliability Fundamentals and Calculation of Failure Rate

Table 9 defines some of the more important terminology used in describing the lifetime of integrated circuits. Of prime importance is the concept of "failure rate" and its calculation.

Failure Rate Calculations

Since reliability data can be accumulated from a number of different life tests with several different failure mechanisms, a comprehensive failure rate is desired. The failure rate calculation can be complicated if there are more than one failure mechanism in a life test, since the failure mechanisms are thermally activated at different rates The equation below accounts for these considerations along with a statistical factor to obtain the upper confidence level (UCL) for the resulting failure rate.

$$\lambda = \left[\sum_{i=1}^{\beta} \frac{x_i}{\sum_{j=1}^{k} TDH_j \, AF_{ij}} \right] \times \frac{M \times 10^9}{\sum_{i=1}^{\beta} x_i}$$

where,

λ = failure rate in FITs (Number fails in 10^9 device hours)

β = number of distinct possible failure mechanisms

k = number of life tests being combined

x_i = number of failures for a given failure mechanism $i = 1, 2, \ldots \beta$

TDH_j = Total device hours of test time (unaccelerated) for Life Test $j, j = 1, 2, 3, \ldots k$

AF_{ij} = Acceleration factor for appropriate failure mechanism $i = 1, 2, \ldots k$

$M = X^2_{(\alpha, 2r+2)}/2$
where,
X^2 = chi square factor for $2r + 2$ degrees of freedom
r = total number of failures (Σx_i)
α = risk associated with UCL;
i.e. α = (100-UCL(%))/100

In the failure rate calculation, Acceleration Factors (AF_{ij}) are used to derate the failure rate from the thermally accelerated life test conditions to a failure rate indicative of actual use temperature. Although no standard exists, a temperature of +55°C has been popular. Harris Semiconductor Reliability Reports will derate to +55°C and will express failure rates at 60% UCL. Other derating temperatures and UCLs are available upon request.

TABLE 9. FAILURE RATE PRIMER

TERMS	DEFINITIONS/DESCRIPTION
Failure Rate λ	Measure of failure per unit of time. The early life failure rate is typically higher, decreases slightly, and then becomes relatively constant over time. The onset of wear-out will show an increasing failure rate, which should occur well beyond useful life. The useful life failure rate is based on the exponential life distribution.
FIT (Failure In Time)	Measure of failure rate in 10^9 device hours; e.g., 1 FIT = 1 failure in 10^9 device hours, 100 FITS = 100 failure in 10^9 device hours, etc.
Device Hours	The summation of the number of units in operation multiplied by the time of operation.
MTTF (Mean Time To Failure)	Mean of the life distribution for the population of devices under operation or expected lifetime of an individual, MTTF = $1/\lambda$, which is the time where 63.2% of the population has failed. Example: For λ = 10 FITS (or 10 E-9/Hr.), MTTF = $1/\lambda$ = 100 million hours.
Confidence Level (or Limit)	Probability level at which population failure rate estimates are derived from sample life test: 10 FITs at 95% UCL means that the population failure rate is estimated to be no more that 10 FITs with 95% certainty. The upper limit of the confidence interval is used.
Acceleration Factor (AF)	A constant derived from experimental data which relates the times to failure at two different stresses. The AF allows extrapolation of failure rates from accelerated test conditions to use conditions.

Acceleration Factors

Acceleration factor is determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and has been found to be an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP\left[\frac{E_a}{k}\left(\frac{1}{T_{USE}} - \frac{1}{T_{STRESS}}\right)\right]$$

where,

AF = Acceleration Factor

E_a = Thermal Activation Energy (See Table 10)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

Both T_{use} and T_{stress} (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature.

Activation Energy

The Activation Energy (E_a) of a failure mechanism is determined by performing at least two tests at different levels of stress (temperature and/or voltage). The stresses will provide the time to failure (t_f) for the two (or more) populations thus allowing the simultaneous solution for the activation energy as follows:

$$\ln (t_{f1}) = C + \frac{E_a}{kT_1} \qquad \ln (t_{f2}) = C + \frac{E_a}{kT_2}$$

By subtracting the two equations and solving for the activation energy, the following equation is obtained:

$$E_a = \frac{k[\ln(t_{f1}) - \ln(t_{f2})]}{(1/T1 - 1/T2)}$$

where,

E_a = Thermal Activation Energy (See Table 10)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

T_1, T_2 = Life test temperatures in degrees Kelvin

TABLE 10. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3eV - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3eV - 0.5eV	HTOL and voltage stress screens.	Vendor statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress testing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5eV - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistical Process Control of assembly processes, proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation.
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles, Statistical Process Control of photoresist/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test and HTOL.	Statistical Process Control of C-V data, oxide/ interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL and oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

COMMUNICATIONS 9

PACKAGING INFORMATION

Communications Package Selection Guide

PART NUMBER	PDIP	SOIC	SSOP	TSSOP	PLCC	MQFP	TQFP	CERDIP	CPGA	SBDIP	TAB
CA3045								F14.3		D14.3	
CA3046	E14.3	M14.15									
CA3081	E16.3	M16.15						F16.3			
CA3082	E16.3	M16.15						F16.3			
CA3083	E16.3	M16.15						F16.3			
CA3086	E14.3	M14.15						F14.3			
CA3096	E16.3	M16.15									
CA3096A	E16.3	M16.15									
CA3096C	E16.3	M16.15									
CA3127	E16.3	M16.15									
CA3146	E14.3	M14.15									
CA3146A	E14.3	M14.15									
CA3183	E16.3	M16.15									
CA3183A	E16.3	M16.15									
CA3227	E16.3	M16.15									
CA3246	E14.3	M14.15									
CD22100	E16.3							F16.3			
CD22101	E24.6							F24.6			
CD22102	E24.6										
CD22103A	E16.3									D16.3	
CD22202	E18.3										
CD22203	E18.3										
CD22204	E14.3	M24.3									
CD22301	E18.3										
CD22354A	E16.3										
CD22357A	E16.3										
CD22859	E16.3										
CD22M3493	E40.6				N44.65						
CD22M3494	E40.6				N44.65						
CD74HC22106	E28.6										
CD74HCT22106	E28.6										
CXD2306						Q32.7x7-S					
CXD2310A						Q48.7x7-S					
CX20201-1		M28.3A-S									
CX20202-1	E28.6A-S										
HC-5502B	E24.6	M24.3			N28.45			F24.6			
HC-5502B1	E24.6	M24.3			N28.45						

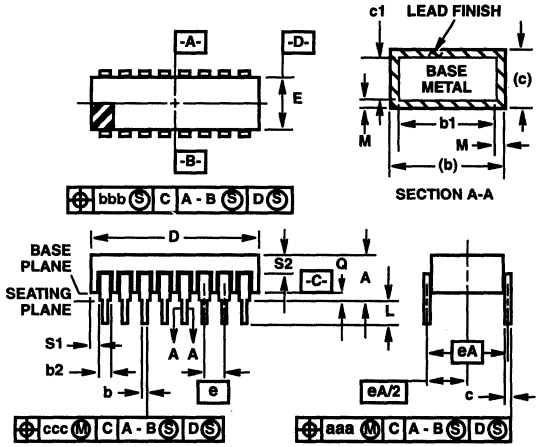
Communications Package Selection Guide

PART NUMBER	PDIP	SOIC	SSOP	TSSOP	PLCC	MQFP	TQFP	CERDIP	CPGA	SBDIP	TAB
HC-5504B	E24.6	M24.3			N28.45			F24.6			
HC5504B1	E24.6	M24.3			N28.45						
HC5509A1R3060					N28.45						
HC-5509B	E28.6	M28.3			N44.65						
HC5513	E22.4				N28.45						
HC5515	E22.4				N28.45						
HC5517		M28.3			N28.45						
HC5519						Q80.14x20					
HC5520					N44.65	Q44.10x10					
HC5521					N44.65	Q44.10x10					
HC5523	E22.4				N28.45						
HC-5524	E28.6	M28.3			N44.65			F28.6			
HC5526	E22.4				N28.45						
HC-5560	E20.3										
HC6094						Q44.10x10					
HC-55564	E14.3							F14.3			
HFA1100	E8.3	M8.15						F8.3A			
HFA1102	E8.3	M8.15						F8.3A			
HFA1110	E8.3	M8.15						F8.3A			
HFA1112	E8.3	M8.15						F8.3A			
HFA1113	E8.3	M8.15						F8.3A			
HFA1114	E8.3	M8.15									
HFA1120	E8.3	M8.15						F8.3A			
HFA1130	E8.3	M8.15						F8.3A			
HFA3046		M14.15									
HFA3096		M16.15									
HFA3101		M8.15									
HFA3102		M8.15									
HFA3127		M16.15									
HFA3128		M16.15									
HFA3424		M8.15									
HFA3524				M20.173							
HFA3600		M14.15									
HFA3624			M28.15								
HFA3724							Q80.14x14				
HFA3925			M28.15								
HI5703		M28.3									

Communications Package Selection Guide

PART NUMBER	PDIP	SOIC	SSOP	TSSOP	PLCC	MQFP	TQFP	CERDIP	CPGA	SBDIP	TAB
HI5710A						Q48.7x7-S					
HI5721	E28.6	M28.3									
HI5731	E28.6	M28.3									
HI5741	E28.6	M28.3									
HI5746		M28.3									
HI5766		M28.3									
HI5780						Q32.7x7-S					
HI5800										D40.6	
HI5804		M28.3									
HI5805		M28.3									
HI5808		M28.3									
HI5905						Q44.10x10					
HI20201	E28.6A-S										
HSP3824							Q48.7x7				
HSP43124	E28.6	M28.3									
HSP43168					N84.1.15	Q100.14x20			G84.A		
HSP43216					N84.1.15	Q100.14x20			G85.A		
HSP43220					N84.1.15	Q100.14x20			G84.A		S84.A
HSP45102	E28.6	M28.3									
HSP45106					N84.1.15				G85.A		
HSP45116						Q160.28x28			G145.A		S156.A
HSP45116A						Q160.28x28					
HSP50016					N44.65				G48.A		
HSP50110					N84.1.15						
HSP50210					N84.1.15						
HSP50214						Q120.28x28					
HSP50306		M16.3									
HSP50307		M28.3									
RF1K49086		MS-012AA									
RF1K49088		MS-012AA									
RF1K49090		MS-012AA									
RF1K49092		MS-012AA									
RF1K49093		MS-012AA									
RF1K49154		MS-012AA									
RF1K49156		MS-012AA									
RF1K49157		MS-012AA									

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D14.3 MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C)
14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

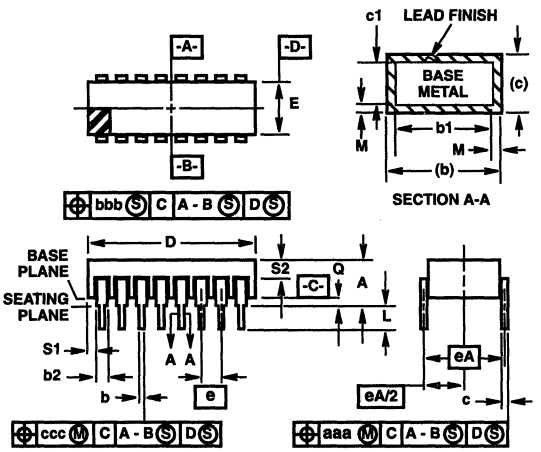
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

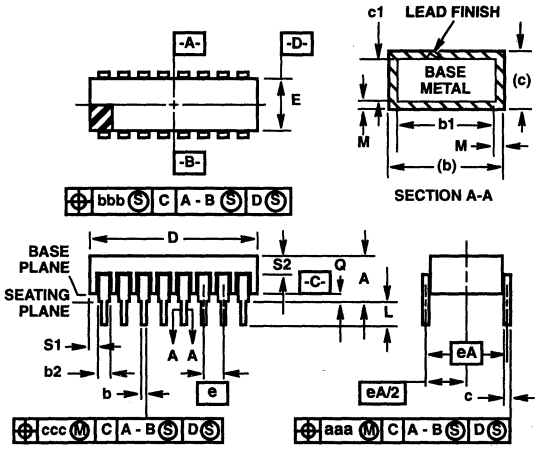
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D40.6 MIL-STD-1835 CDIP2-T40 (D-5, CONFIGURATION C)
40 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

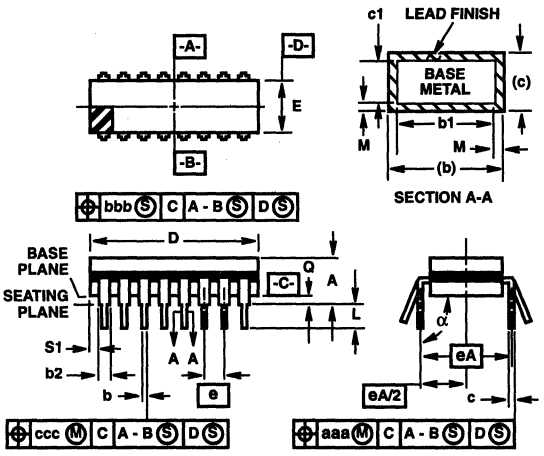
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	2.096	-	53.24	4
E	0.510	0.620	12.95	15.75	4
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	40		40		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

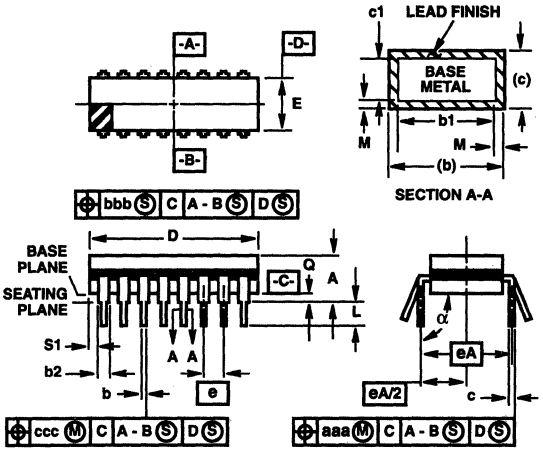
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

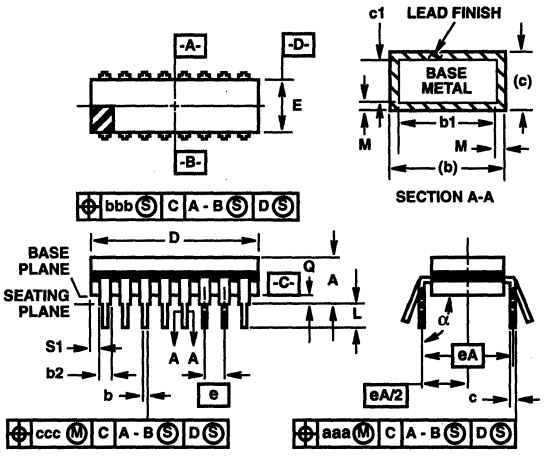
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

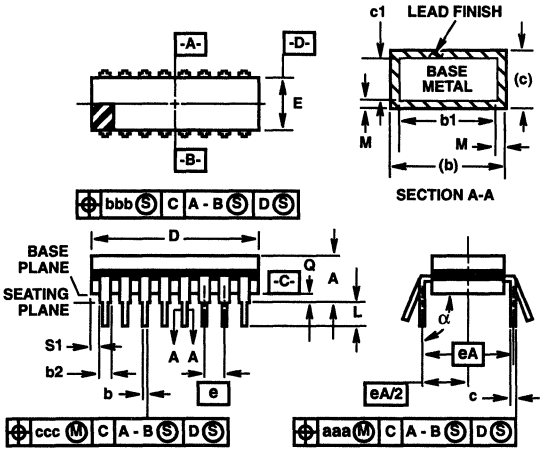
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F24.6 MIL-STD-1835 GDIP1-T24 (D-3, CONFIGURATION A)
24 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

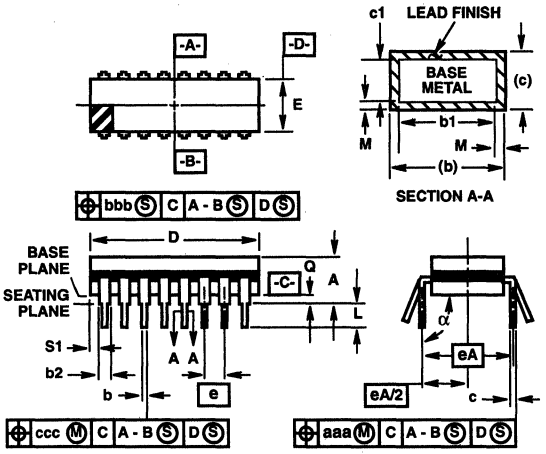
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.120	0.200	3.05	5.08	-
Q	0.015	0.075	0.38	1.91	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	24		24		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F28.6 MIL-STD-1835 GDIP1-T28 (D-10, CONFIGURATION A)
28 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

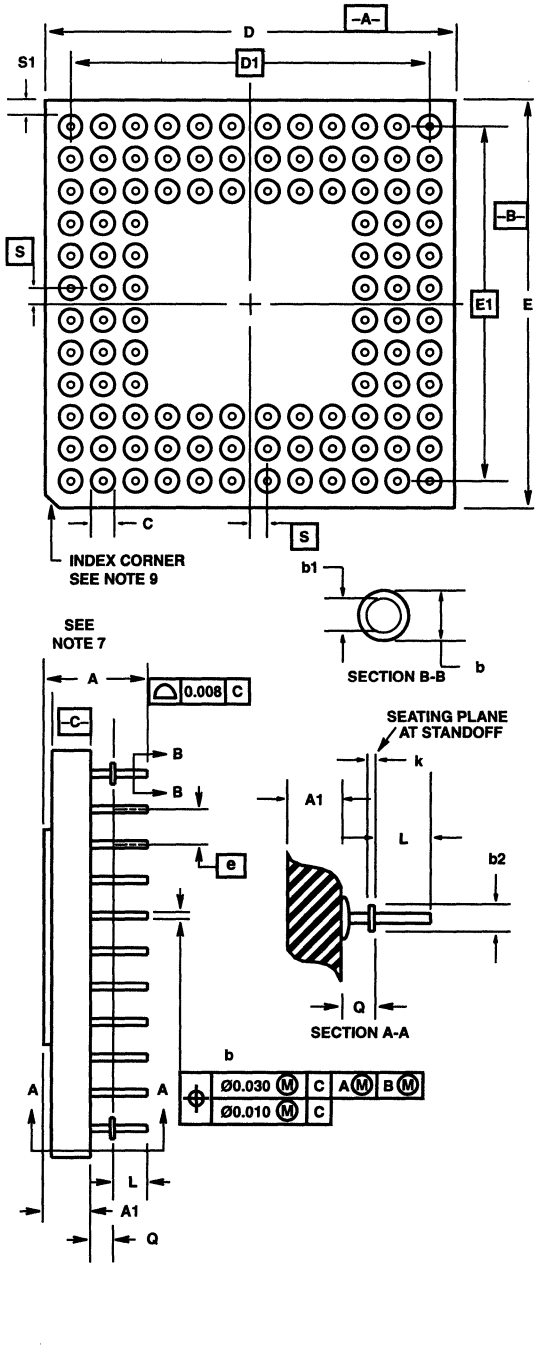
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	28		28		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Pin Grid Array Packages (CPGA)



G48.A

48 LEAD CERAMIC PIN GRID ARRAY PACKAGE

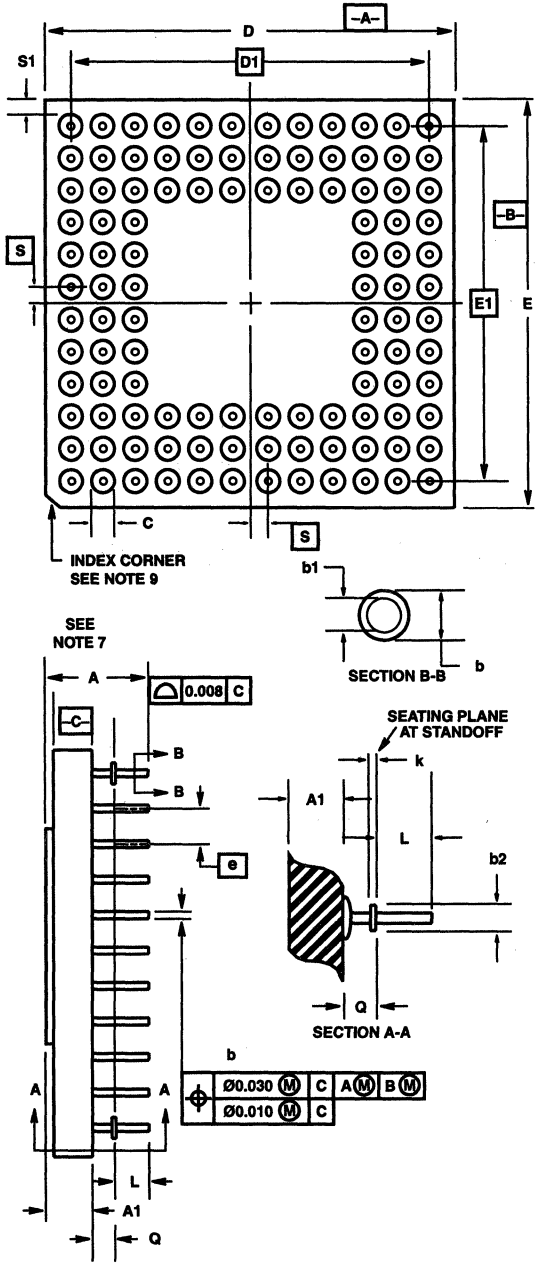
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	-	-	-	-
A1	0.080	0.120	2.03	3.05	3
b	0.016	0.0215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.040	0.060	1.02	1.52	4
C	-	0.80	-	2.03	-
D	0.790	0.810	20.07	20.57	-
D1	0.700 BSC		17.78 BSC		-
E	0.790	0.810	20.07	20.57	-
E1	0.700 BSC		17.78 BSC		-
e	0.100 BSC		2.54 BSC		6
k	-	-	-	-	-
L	0.090	0.110	2.29	2.79	-
Q	0.40	0.060	1.02	1.52	5
S	0.050 BSC		1.27 BSC		10
S1	-	-	-	-	
M	8		8		1
N	-	64	-	64	2

Rev. 1 6/28/95

NOTES:

1. "M" represents the maximum pin matrix size.
2. "N" represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension "A1" includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity up. Dimension "A1" does not include heatsinks or other attached features.
4. Standoffs are intrinsic and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimensions Q.
5. Dimension "Q" applies to cavity-up configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension "S" is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling dimension: INCH.

Ceramic Pin Grid Array Packages (CPGA)



G84.A MIL-STD-1835 CMGA3-P84C (P-AC)
84 LEAD CERAMIC PIN GRID ARRAY PACKAGE

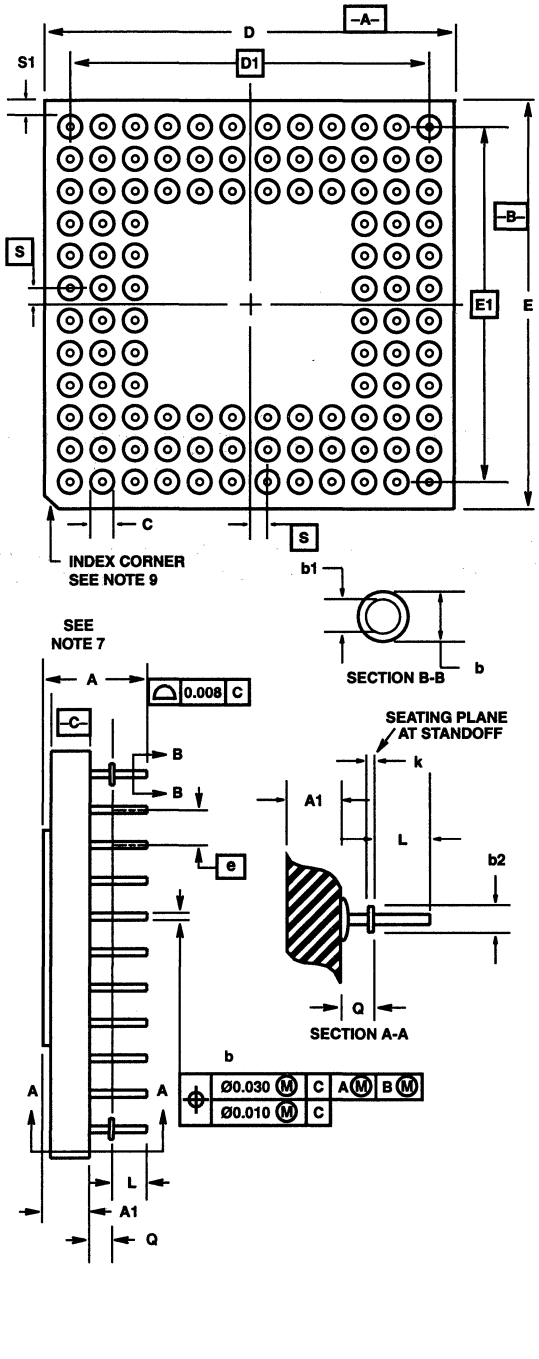
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.215	0.345	5.46	8.76	-
A1	0.070	0.145	1.78	3.68	3
b	0.016	0.0215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.042	0.058	1.07	1.47	4
C	-	0.080	-	2.03	-
D	1.140	1.180	28.96	29.97	-
D1	1.000 BSC		25.4 BSC		-
E	1.140	1.180	28.96	29.97	-
E1	1.000 BSC		25.4 BSC		-
e	0.100 BSC		2.54 BSC		6
k	0.008 REF		0.20 REF		-
L	0.120	0.140	3.05	3.56	-
Q	0.040	0.060	1.02	1.52	5
S	0.000 BSC		0.00 BSC		10
S1	0.003	-	0.08	-	-
M	11		11		1
N	-	121	-	121	2

Rev. 1 6/28/95

NOTES:

1. "M" represents the maximum pin matrix size.
2. "N" represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension "A1" includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity up. Dimension "A1" does not include heatsinks or other attached features.
4. Standoffs are intrinsic and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimensions Q.
5. Dimension "Q" applies to cavity-up configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension "S" is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling dimension: INCH.

Ceramic Pin Grid Array Packages (CPGA)



G85.A MIL-STD-1835 CMGA3-P85C (P-AC)
85 LEAD CERAMIC PIN GRID ARRAY PACKAGE

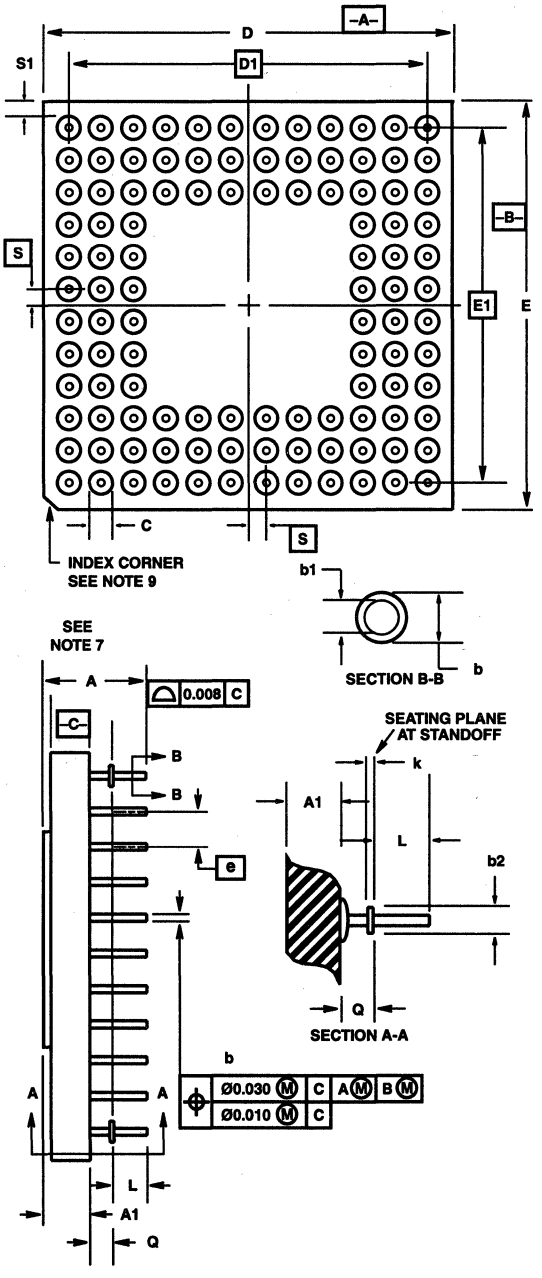
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.215	0.345	5.46	8.76	-
A1	0.070	0.145	1.78	3.68	3
b	0.016	0.0215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.042	0.058	1.07	1.47	4
C	-	0.080	-	2.03	-
D	1.140	1.180	28.96	29.97	-
D1	1.000 BSC		25.4 BSC		-
E	1.140	1.180	28.96	29.97	-
E1	1.000 BSC		25.4 BSC		-
e	0.100 BSC		2.54 BSC		6
k	0.008 REF		0.20 REF		-
L	0.120	0.140	3.05	3.56	-
Q	0.040	0.060	1.02	1.52	5
S	0.000 BSC		0.00 BSC		10
S1	0.003	-	0.08	-	-
M	11		11		1
N	-	121	-	121	2

Rev. 1 6/21/95

NOTES:

1. "M" represents the maximum pin matrix size.
2. "N" represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension "A1" includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity up. Dimension "A1" does not include heatsinks or other attached features.
4. Standoffs are intrinsic and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimensions Q.
5. Dimension "Q" applies to cavity-up configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension "S" is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling dimension: INCH.

Ceramic Pin Grid Array Packages (CPGA)



G145.A MIL-STD-1835 CMGA7-P145C (P-AG)
145 LEAD CERAMIC PIN GRID ARRAY PACKAGE

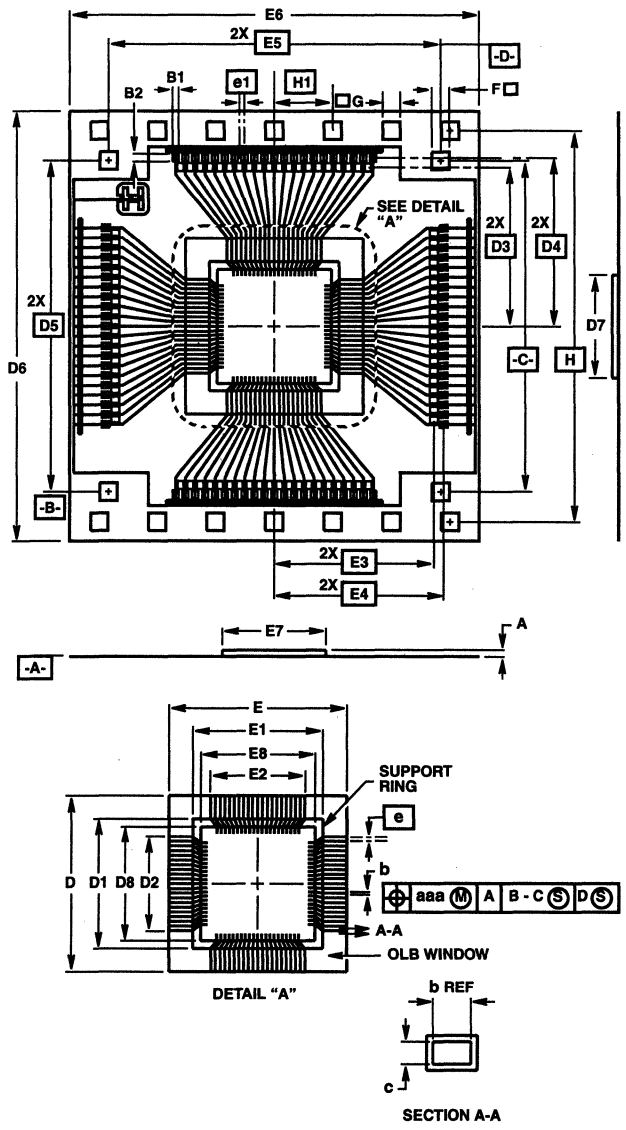
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.215	0.345	5.46	8.76	-
A1	0.070	0.145	1.78	3.68	3
b	0.016	0.0215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.042	0.058	1.07	1.47	4
C	-	0.080	-	2.03	-
D	1.540	1.590	39.12	40.38	-
D1	1.400 BSC		35.56 BSC		-
E	1.540	1.590	39.12	40.38	-
E1	1.400 BSC		35.56 BSC		-
e	0.100 BSC		2.54 BSC		6
k	0.008 REF		0.20 REF		-
L	0.120	0.140	3.05	3.56	-
Q	0.040	0.060	1.02	1.52	5
S	0.000 BSC		0.00 BSC		10
S1	0.003	-	0.08	-	-
M	15		15		1
N	-	225	-	225	2

Rev. 1 6/28/95

NOTES:

1. "M" represents the maximum pin matrix size.
2. "N" represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension "A1" includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity up. Dimension "A1" does not include heatsinks or other attached features.
4. Standoffs are intrinsic and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimensions Q.
5. Dimension "Q" applies to cavity-up configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension "S" is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling dimension: INCH.

Tape Automated Bonding Packages (TAB)



S84.A

84 LEAD TAPE AUTOMATED BONDING PACKAGE

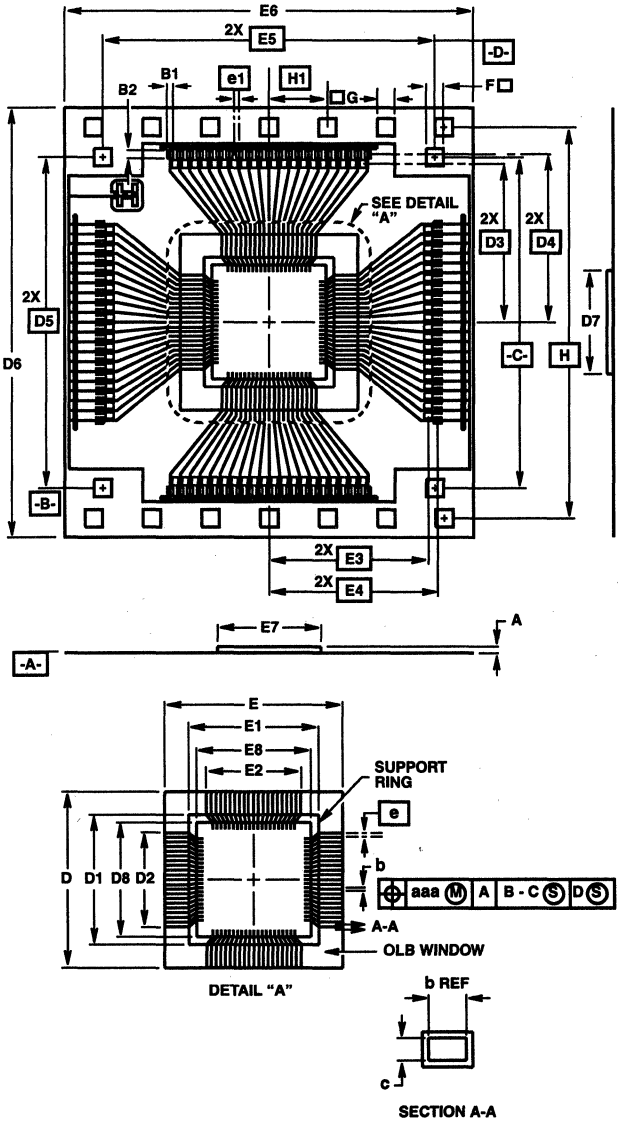
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.034	-	0.86	-
b	0.002	0.004	0.05	0.10	2, 7
c	0.0010	0.0018	0.025	0.046	2, 7
B1	0.019	0.021	0.47	0.53	5
B2	0.023	0.028	0.60	0.70	5
D	0.559	0.569	14.20	14.45	-
E	0.562	0.572	14.27	14.53	-
D1	0.410	0.420	10.41	10.67	3
E1	0.409	0.419	10.39	10.64	3
D2	0.300	0.310	7.62	7.87	4
E2	0.300	0.310	7.62	7.87	4
D3/E3	0.500 BSC		12.70 BSC		-
D4/E4	0.531 BSC		13.475 BSC		-
D5/E5	1.061 BSC		26.95 BSC		-
D6	1.372	1.382	34.85	35.10	-
E6	1.244	1.314	31.62	33.37	-
D7	0.345	0.351	8.77	8.92	-
E7	0.344	0.350	8.74	8.89	-
D8	0.360	0.370	9.14	9.40	-
E8	0.358	0.368	9.09	9.35	-
e	0.015 BSC		0.38 BSC		2
e1	0.016 BSC		0.40 BSC		5
F	0.054	0.057	1.39	1.45	-
G	0.055	0.057	1.40	1.45	-
H	1.253 BSC		31.83 BSC		-
H1	0.187 BSC		4.75 BSC		-
aaa	0.003		0.08		-

Rev. 0 4/94

NOTES:

1. All dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Controlling dimension is MILLIMETERS except for dimensions b, c and e which are in INCHES.
3. Dimensions D1/E1 define the package "body size".
4. Dimensions D2/E2 define the maximum allowable dimension between the outside edges of the outermost leads. This dimension provides necessary clearance from the OLB window corners for excise operations.
5. This dimension applies to all test pads.
6. All lead and test pad arrays shall be arranged in a symmetric configuration with respect to datums D or B-C.
7. Dimensions b and c apply to base material only.
8. Lead Material: Copper
   Lead Finish: Gold over nickel underplate
9. Film format and test pads per JEDEC US-001, Ax - 2x.
10. TAB packages shipped in slide carriers per JEDEC CS-006 with the leads unformed (flat).

Tape Automated Bonding Packages (TAB)



S156.A

156 LEAD TAPE AUTOMATED BONDING PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.034	-	0.86	-
b	0.002	0.004	0.05	0.10	2
c	0.0010	0.0018	0.025	0.046	2, 7
B1	0.019	0.021	0.47	0.53	5
B2	0.023	0.028	0.60	0.70	5
D	0.559	0.569	14.20	14.45	-
E	0.562	0.572	14.27	14.53	-
D1	0.429	0.439	10.90	11.15	3
E1	0.431	0.441	10.95	11.20	3
D2	0.380	0.390	9.65	9.90	4
E2	0.380	0.390	9.65	9.90	4
D3/E3	0.500 BSC		12.70 BSC		-
D4/E4	0.531 BSC		13.475 BSC		-
D5/E5	1.061 BSC		26.95 BSC		-
D6	1.372	1.382	34.85	35.10	-
E6	1.244	1.314	31.62	33.37	-
D7	0.349	0.355	8.87	9.02	-
E7	0.346	0.352	8.79	8.94	-
D8	0.360	0.370	9.14	9.40	-
E8	0.367	0.377	9.32	9.57	-
e	0.010 BSC		0.254 BSC		2
e1	0.016 BSC		0.40 BSC		5
F	0.054	0.057	1.39	1.45	-
G	0.055	0.057	1.40	1.45	-
H	1.253 BSC		31.83 BSC		-
H1	0.187 BSC		4.75 BSC		-
aaa	0.002		0.05		-

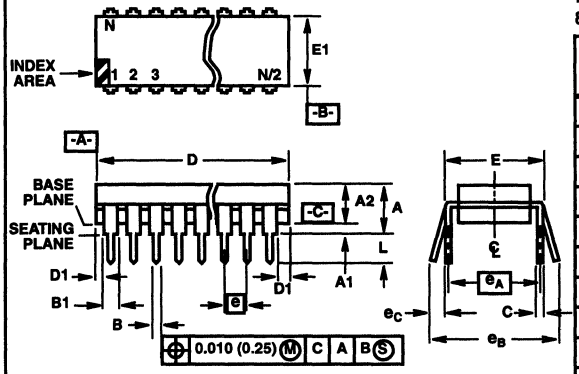
Rev. 0 4/94

NOTES:

1. All dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Controlling dimension is MILLIMETERS except for dimensions b, c and e which are in INCHES.
3. Dimensions D1/E1 define the package "body size".
4. Dimensions D2/E2 define the maximum allowable dimension between the outside edges of the outermost leads. This dimension provides necessary clearance from the OLB window corners for excise operations.
5. This dimension applies to all test pads.
6. All lead and test pad arrays shall be arranged in a symmetric configuration with respect to datums D or B-C.
7. Dimensions b and c apply to base material only.
8. Lead Material: Copper
   Lead Finish: Gold over nickel underplate
9. Film format and test pads per JEDEC US-001, Ax - 2x.
10. TAB packages shipped in slide carriers per JEDEC CS-006 with the leads unformed (flat).

Plastic Packages for Integrated Circuits

Dual-In-Line Plastic Packages (PDIP)



E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

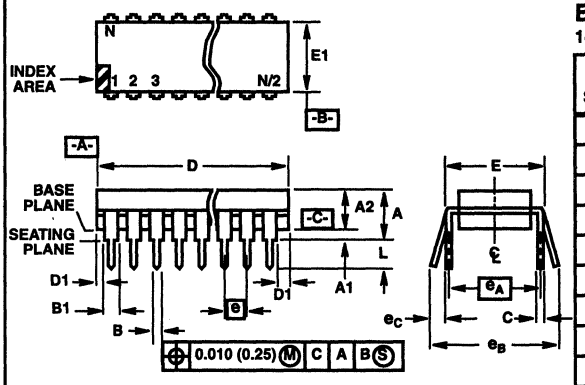
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

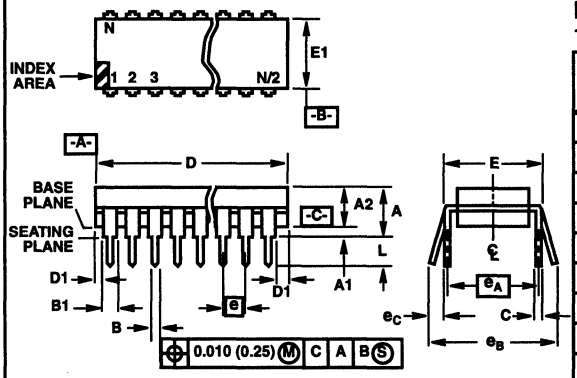
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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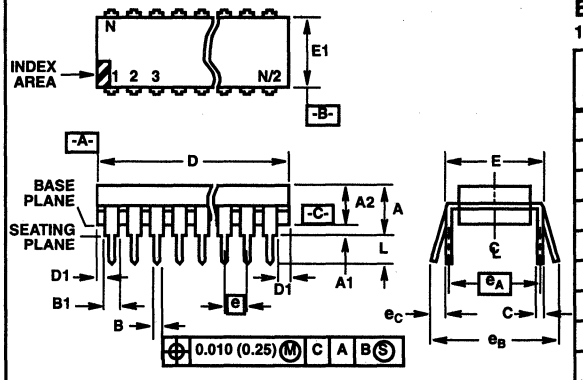
Dual-In-Line Plastic Packages (PDIP)



E18.3 (JEDEC MS-001-BC ISSUE D)
18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

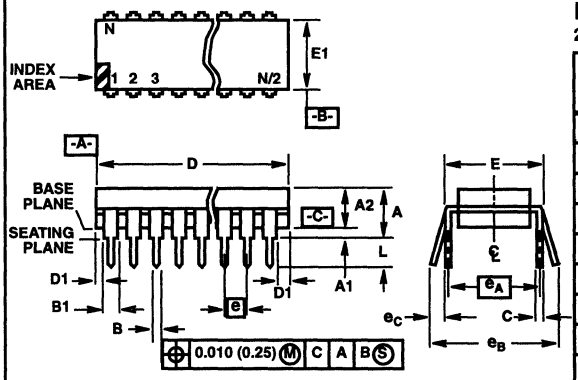
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.845	0.880	21.47	22.35	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	18		18		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

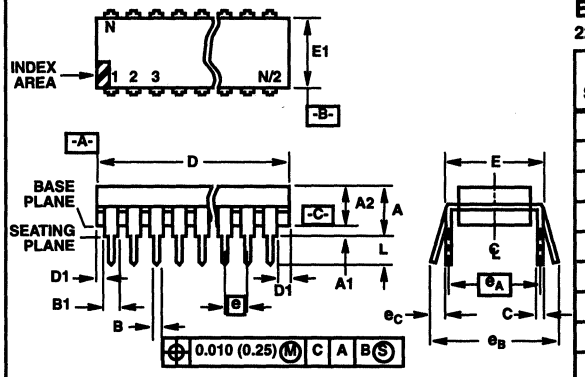
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E22.4 (JEDEC MS-010-AA ISSUE C)
22 LEAD DUAL-IN-LINE PLASTIC PACKAGE

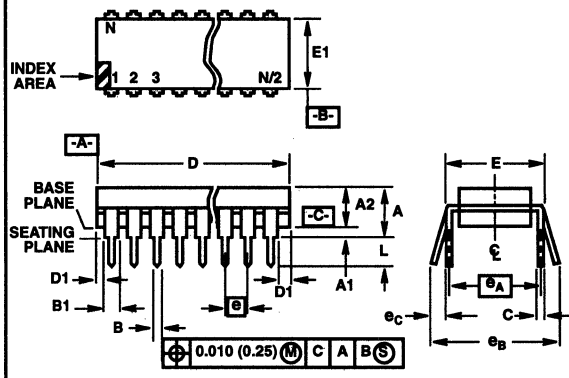
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.065	1.15	1.65	8
C	0.009	0.015	0.229	0.381	-
D	1.065	1.120	27.06	28.44	5
D1	0.005	-	0.13	-	5
E	0.390	0.425	9.91	10.79	6
E1	0.330	0.390	8.39	9.90	5
e	0.100 BSC		2.54 BSC		-
e_A	0.400 BSC		10.16 BSC		6
e_B	-	0.500	-	12.70	7
L	0.115	0.160	2.93	4.06	4
N	22		22		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E24.6 (JEDEC MS-011-AA ISSUE B)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

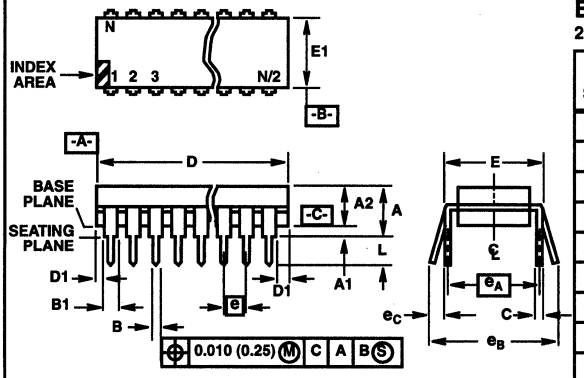
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.150	1.290	29.3	32.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	24		24		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E28.6 (JEDEC MS-011-AB ISSUE B)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

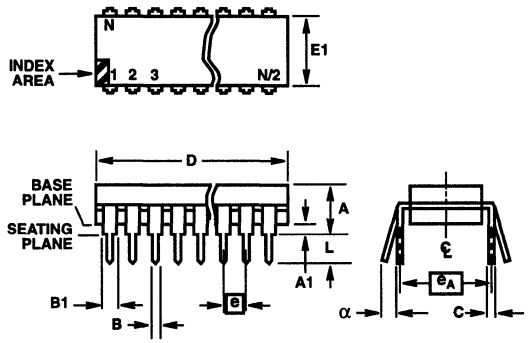
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E28.6A-S

28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

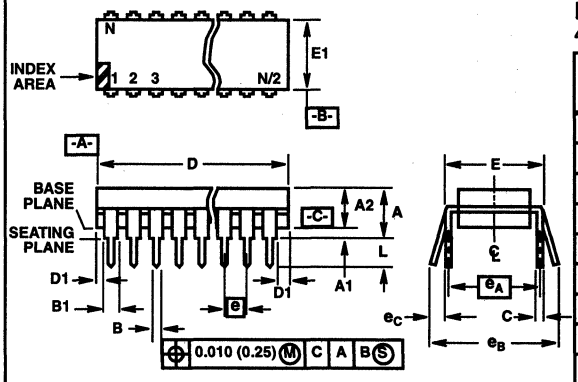
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.178	0.196	4.5	5.0	2
A1	0.020	-	0.50	-	2
B	0.016	0.023	0.40	0.60	-
B1	0.042	0.053	1.05	1.35	-
C	0.008	0.13	0.20	0.35	-
D	1.485	1.503	37.7	38.2	3
E1	0.508	0.523	12.9	13.3	3
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		4
L	0.119	-	3.0	-	2
N	28		28		5
α	0°	15°	0°	15°	-

Rev. 1 4/95

NOTES:

1. Controlling Dimensions: MILLIMETER. In case of conflict between English and Metric dimensions, the metric dimensions control.
2. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
3. D and E1 dimensions do not include mold flash or protrusions.
4. e_A is measured with the leads constrained to be perpendicular to base plane.
5. N is the maximum number of terminal positions.

Dual-In-Line Plastic Packages (PDIP)



E40.6 (JEDEC MS-011-AC ISSUE B)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

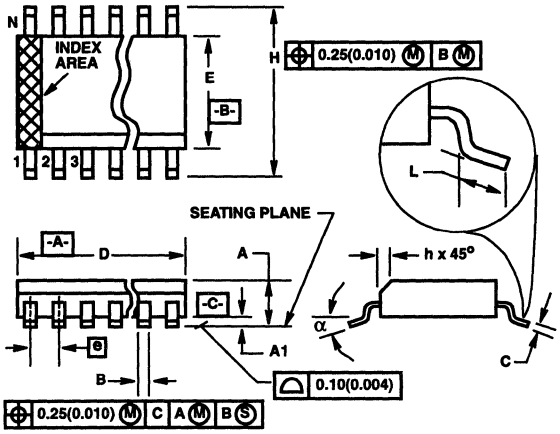
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

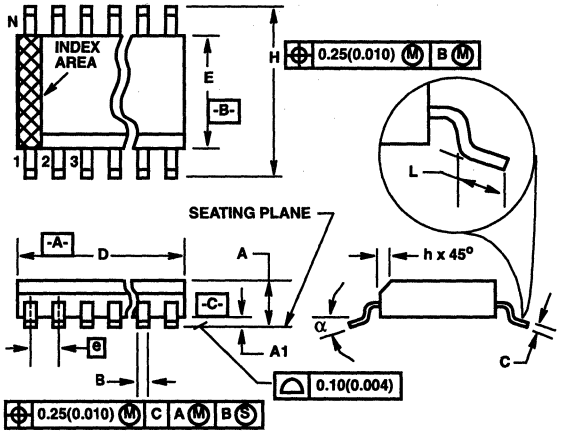
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

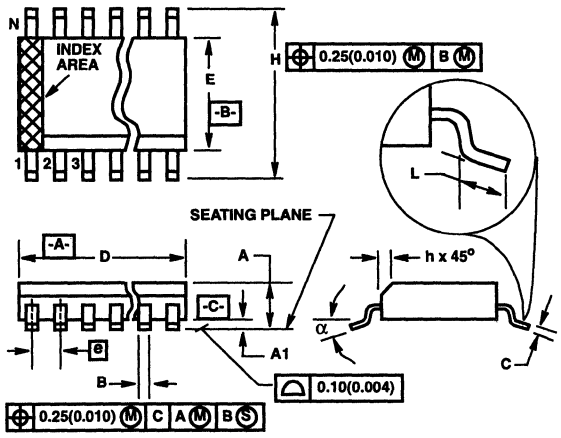
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

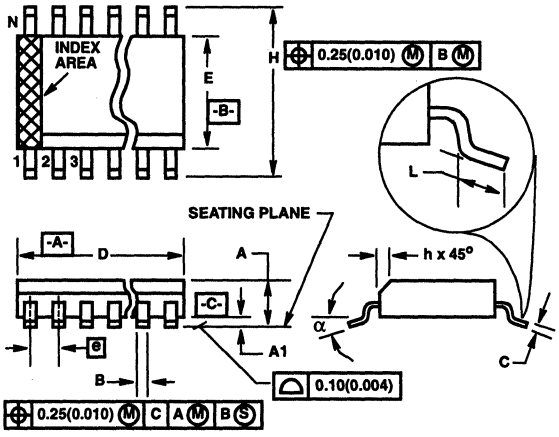
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

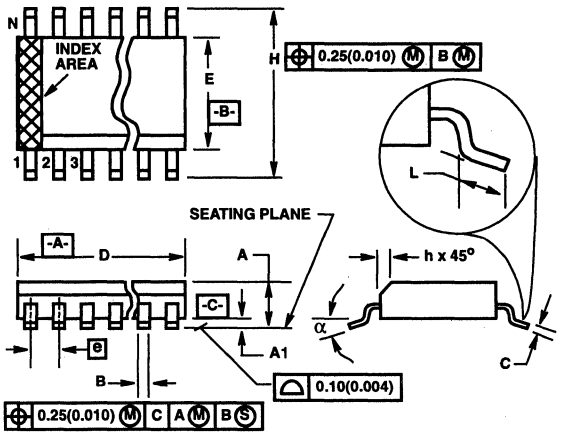
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

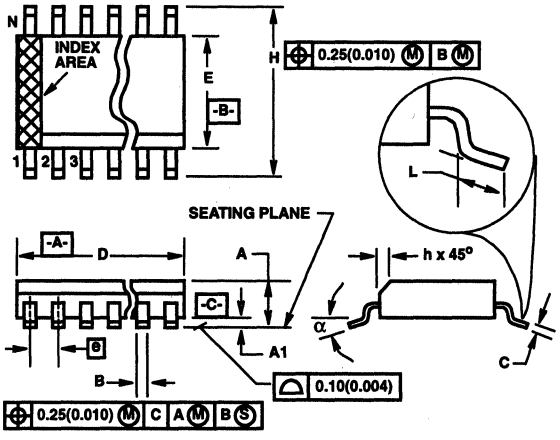
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

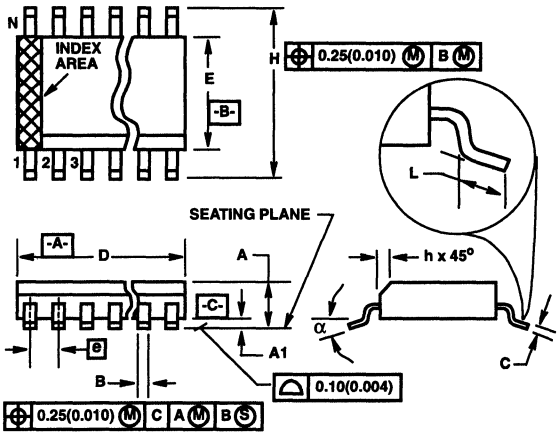
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

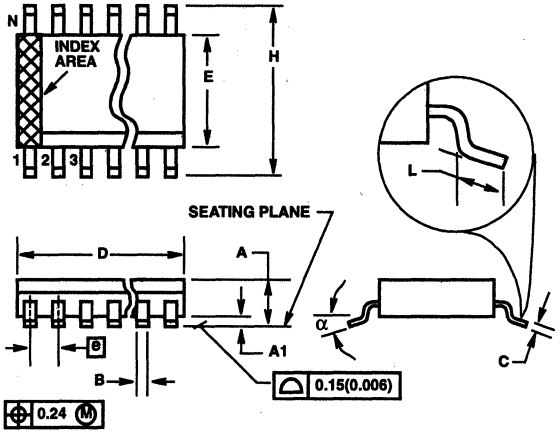
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M28.3A-S

28 LEAD SMALL OUTLINE PLASTIC PACKAGE (300 MIL)

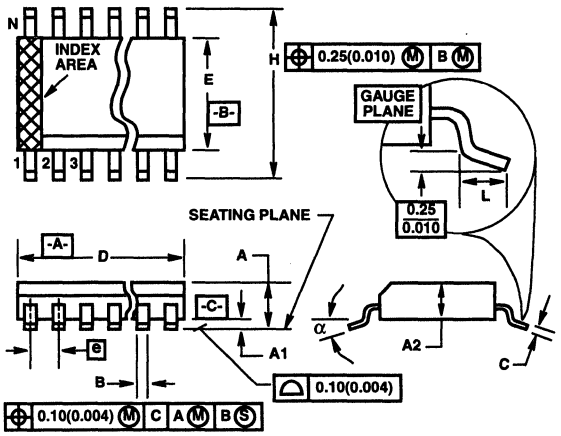
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.085	0.106	2.15	2.7	-
A1	0.002	0.011	0.05	0.30	-
B	0.014	0.021	0.35	0.55	-
C	0.004	0.009	0.10	0.25	-
D	0.737	0.755	18.7	19.2	1
E	0.296	0.311	7.50	7.90	2
e	0.05 BSC		1.27 BSC		-
H	0.390	0.421	9.90	10.70	-
L	0.012	0.027	0.30	0.70	3
N	28		28		4
α	0^o	10^o	0^o	10^o	-

Rev. 1 4/95

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Thin Shrink Small Outline Plastic Packages (TSSOP)



M20.173

20 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

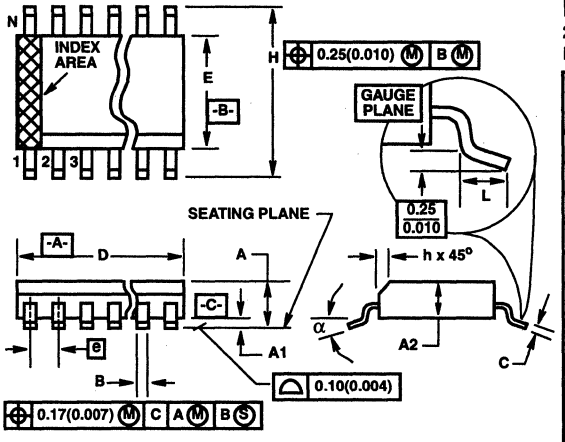
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.043	-	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.0335	0.0374	0.85	0.95	-
B	0.0075	0.0118	0.19	0.30	9
C	0.0035	0.0079	0.09	0.20	-
D	0.252	0.260	6.40	6.60	3
E	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
H	0.246	0.256	6.25	6.50	-
L	0.020	0.028	0.50	0.70	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 0 10/95

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue B.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP)



M28.15

28 LEAD SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

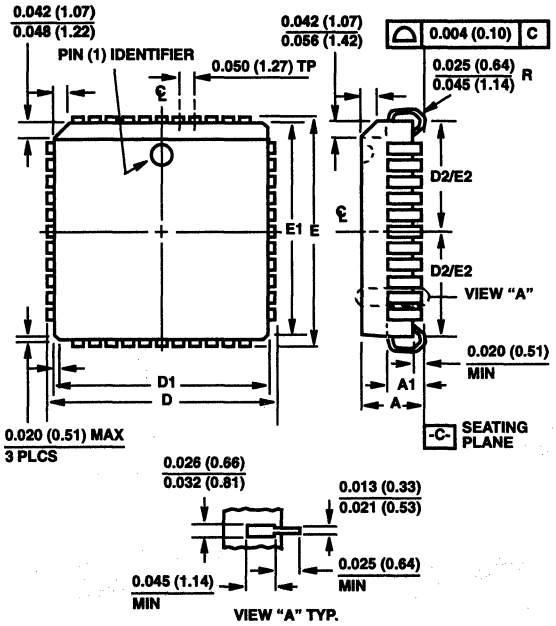
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 0 2/95

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

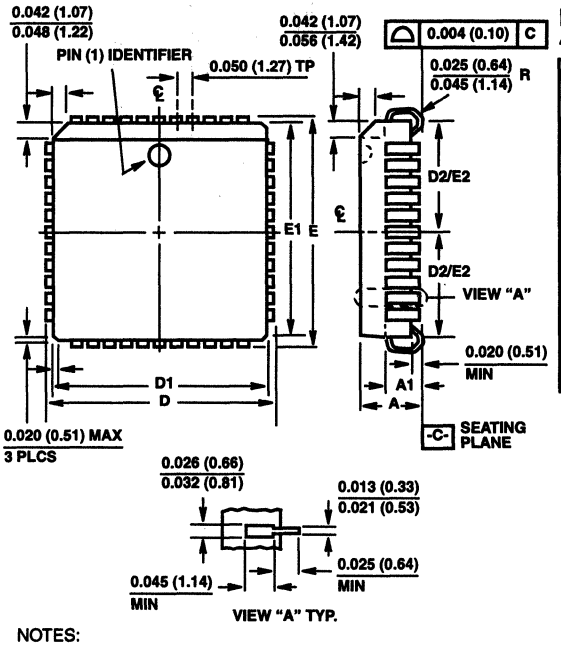
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Plastic Leaded Chip Carrier Packages (PLCC)



N44.65 (JEDEC MS-018AC ISSUE A)
44 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

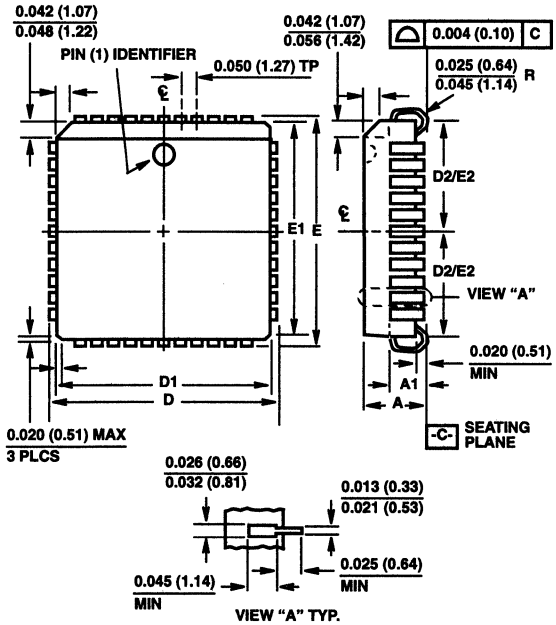
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.685	0.695	17.40	17.65	-
D1	0.650	0.656	16.51	16.66	3
D2	0.291	0.319	7.40	8.10	4, 5
E	0.685	0.695	17.40	17.65	-
E1	0.650	0.656	16.51	16.66	3
E2	0.291	0.319	7.40	8.10	4, 5
N	44		44		6

Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Plastic Leaded Chip Carrier Packages (PLCC)



N84.1.15 (JEDEC MS-018AF ISSUE A)
84 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

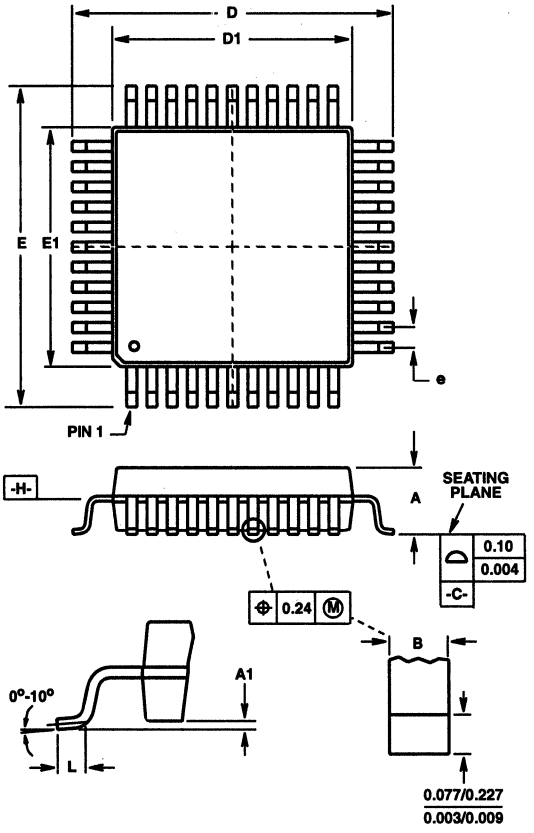
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	1.185	1.195	30.10	30.35	-
D1	1.150	1.158	29.21	29.41	3
D2	0.541	0.569	13.75	14.45	4, 5
E	1.185	1.195	30.10	30.35	-
E1	1.150	1.158	29.21	29.41	3
E2	0.541	0.569	13.75	14.45	4, 5
N	84		84		6

Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP)



Q32.7x7-S

32 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

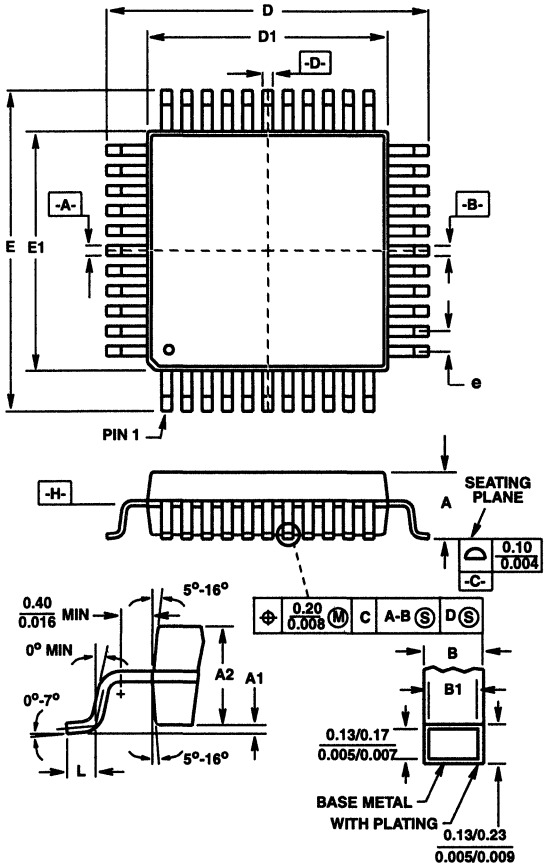
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.054	0.072	1.35	1.85	-
A1	0.000	0.011	0.00	0.30	-
B	0.008	0.017	0.20	0.45	5
D	0.347	0.362	8.80	9.20	2
D1	0.272	0.287	6.90	7.30	3, 4
E	0.347	0.362	8.80	9.20	2
E1	0.272	0.287	6.90	7.30	3, 4
L	0.012	0.027	0.30	0.70	-
N	32		32		6
e	0.032 BSC		0.80 BSC		-

Rev. 2 4/95

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP)



Q44.10x10 (JEDEC MO-108AA-2 ISSUE A)
44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

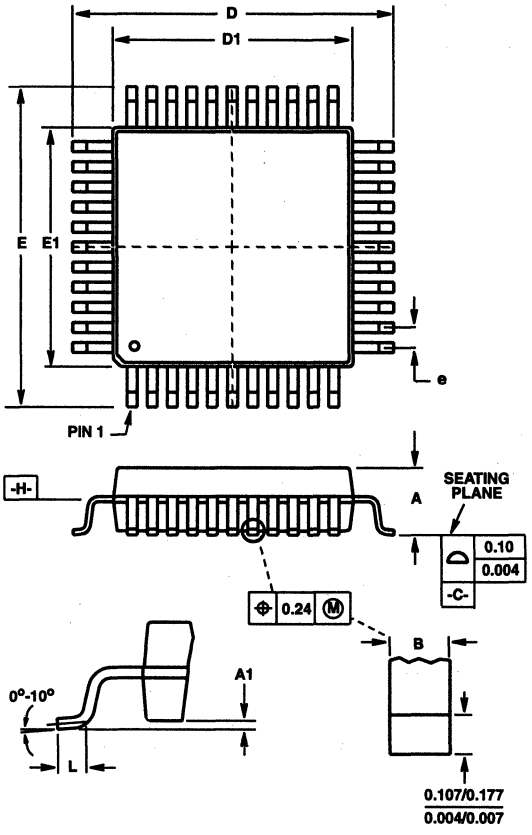
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.093	-	2.35	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.510	0.530	12.95	13.45	3
D1	0.390	0.398	9.90	10.10	4, 5
E	0.510	0.530	12.95	13.45	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

Rev. 1 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP)



Q48.7x7-S

48 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

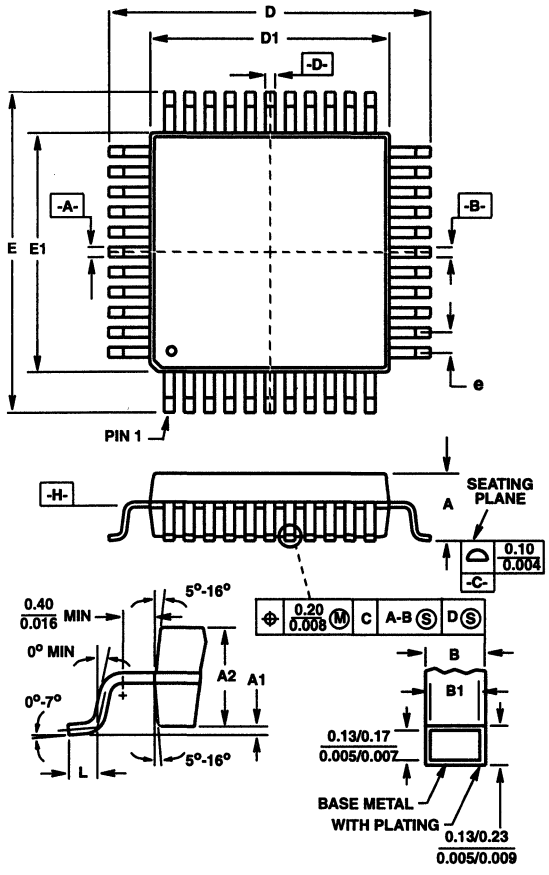
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.056	0.066	1.40	1.70	-
A1	0.000	0.007	0.00	0.20	-
B	0.006	0.010	0.15	0.26	5
D	0.347	0.362	8.80	9.20	2
D1	0.272	0.279	6.90	7.10	3, 4
E	0.347	0.362	8.80	9.20	2
E1	0.272	0.279	6.90	7.10	3, 4
L	0.012	0.027	0.30	0.70	-
N	48		48		6
e	0.020 BSC		0.500 BSC		-

Rev. 1 4/95

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP)



Q80.14x20 (JEDEC MO-108CB-1 ISSUE A)
80 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

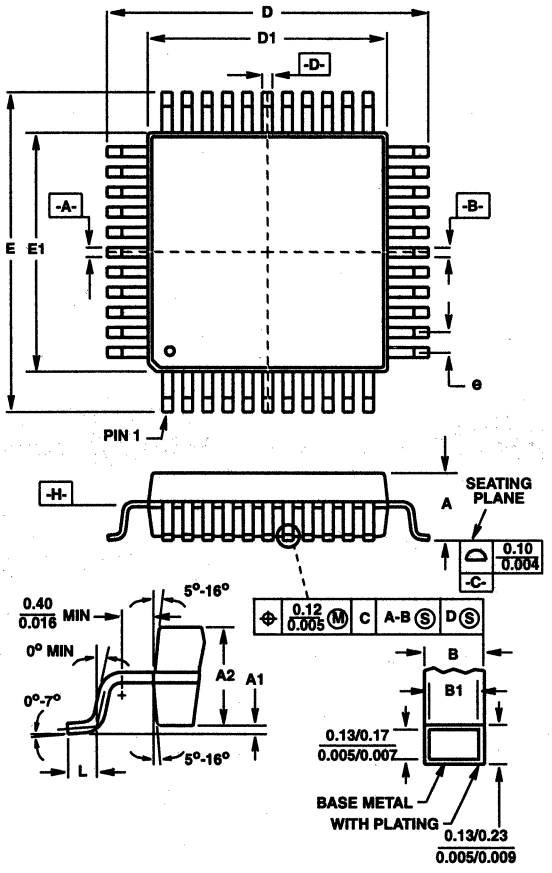
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.134	-	3.40	-
A1	0.010	-	0.25	-	-
A2	0.100	0.120	2.55	3.05	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.904	0.923	22.95	23.45	3
D1	0.783	0.791	19.90	20.10	4, 5
E	0.667	0.687	16.95	17.45	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	80		80		7
e	0.032 BSC		0.80 BSC		-
ND	24		24		-
NE	16		16		-

Rev. 0 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP)



Q100.14x20 (JEDEC MO-108CC-1 ISSUE A)
100 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

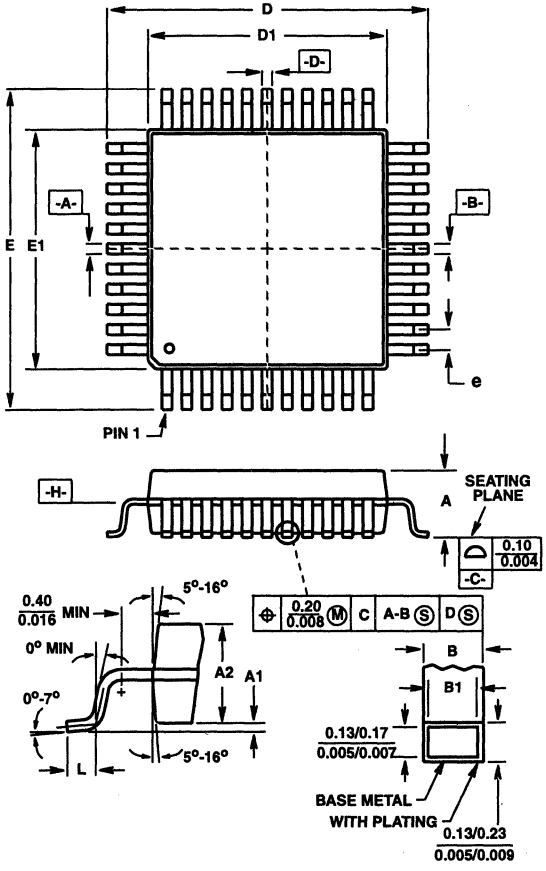
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.134	-	3.40	-
A1	0.010	-	0.25	-	-
A2	0.100	0.120	2.55	3.05	-
B	0.009	0.015	0.22	0.38	6
B1	0.009	0.013	0.22	0.33	-
D	0.904	0.923	22.95	23.45	3
D1	0.783	0.791	19.90	20.10	4, 5
E	0.667	0.687	16.95	17.45	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	100		100		7
e	0.026 BSC		0.65 BSC		-
ND	30		30		-
NE	20		20		-

Rev. 0 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP)



Q120.28x28 (JEDEC MO-108DA-1 ISSUE A)
120 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

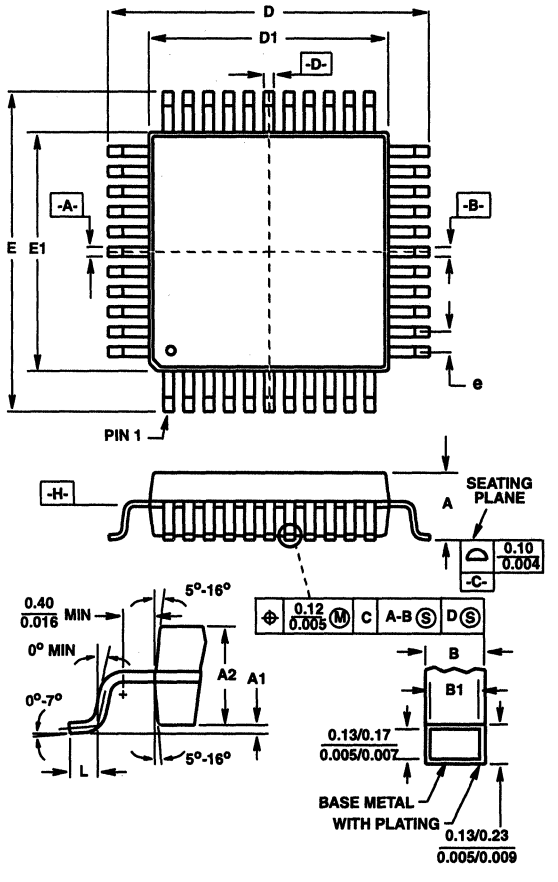
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.160	-	4.07	-
A1	0.010	-	0.25	-	-
A2	0.125	0.144	3.17	3.67	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	1.219	1.238	30.95	31.45	3
D1	1.098	1.106	27.90	28.10	4, 5
E	1.219	1.238	30.95	31.45	3
E1	1.098	1.106	27.90	28.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	120		120		7
e	0.032 BSC		0.80 BSC		-

Rev. 0 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP)



Q160.28x28 (JEDEC MO-108DD-1 ISSUE A)
160 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

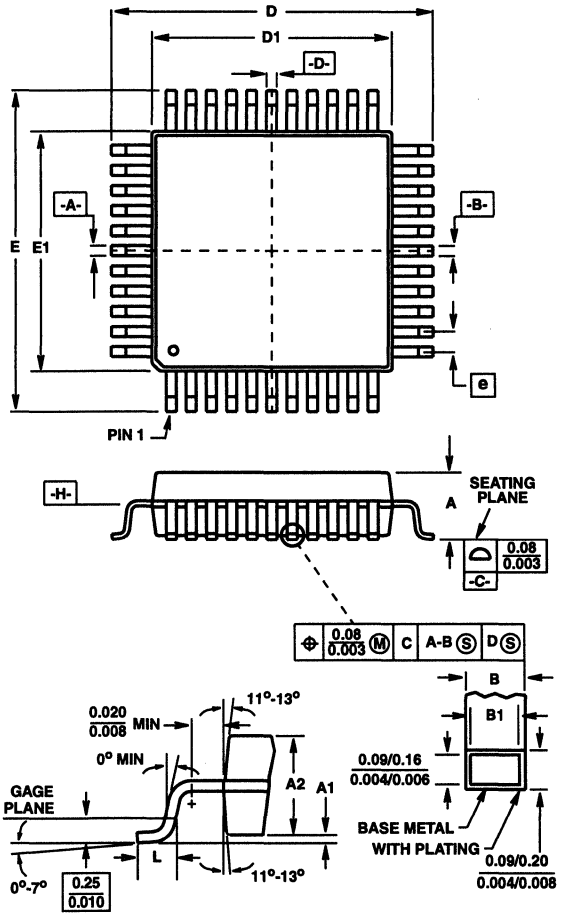
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.160	-	4.07	-
A1	0.010	-	0.25	-	-
A2	0.125	0.144	3.17	3.67	-
B	0.009	0.015	0.22	0.38	6
B1	0.009	0.013	0.22	0.33	-
D	1.219	1.238	30.95	31.45	3
D1	1.098	1.106	27.90	28.10	4, 5
E	1.219	1.238	30.95	31.45	3
E1	1.098	1.106	27.90	28.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	160		160		7
e	0.026 BSC		0.65 BSC		-

Rev. 0 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

Thin Plastic Quad Flatpack Packages (TQFP)



Q48.7x7 (JEDEC MO-136AE ISSUE C)
48 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

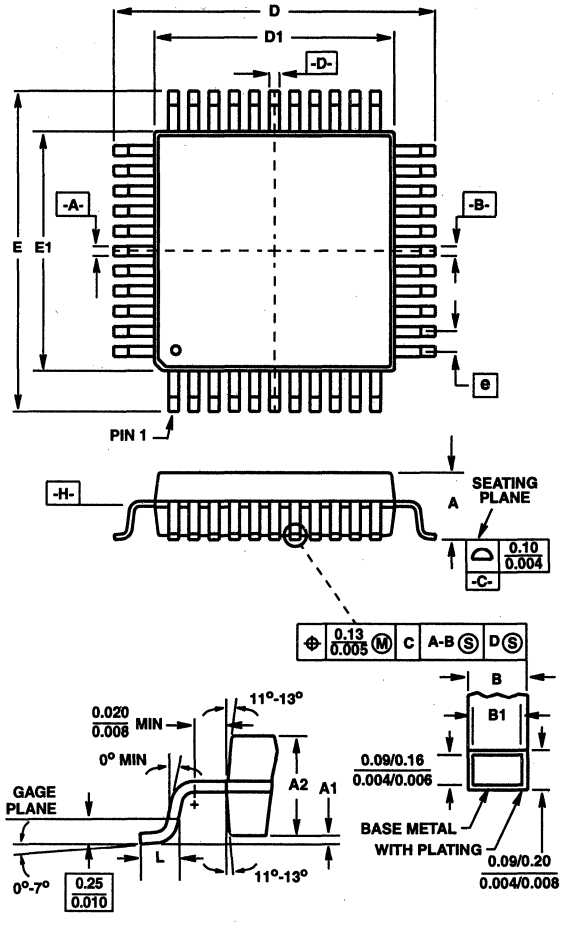
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.005	0.05	0.15	-
A2	0.038	0.041	0.95	1.05	-
B	0.007	0.010	0.17	0.27	6
B1	0.007	0.009	0.17	0.23	-
D	0.347	0.362	8.80	9.20	3
D1	0.268	0.283	6.80	7.20	4, 5
E	0.347	0.362	8.80	9.20	3
E1	0.268	0.283	6.80	7.20	4, 5
L	0.018	0.029	0.45	0.75	-
N	48		48		7
e	0.020 BSC		0.50 BSC		-

Rev. 0 4/95

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum B dimension by more than 0.08mm (0.003 inch).
7. "N" is the number of terminal positions.

Thin Plastic Quad Flatpack Packages (TQFP)



Q80.14x14 (JEDEC MO-136BQ ISSUE C)
80 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.062	-	1.60	-
A1	0.002	0.005	0.05	0.15	-
A2	0.054	0.057	1.35	1.45	-
B	0.009	0.014	0.22	0.38	6
B1	0.009	0.012	0.22	0.33	-
D	0.623	0.637	15.80	16.20	3
D1	0.544	0.559	13.80	14.20	4, 5
E	0.623	0.637	15.80	16.20	3
E1	0.544	0.559	13.80	14.20	4, 5
L	0.018	0.029	0.45	0.75	-
N	80		80		7
e	0.026 BSC		0.65 BSC		-

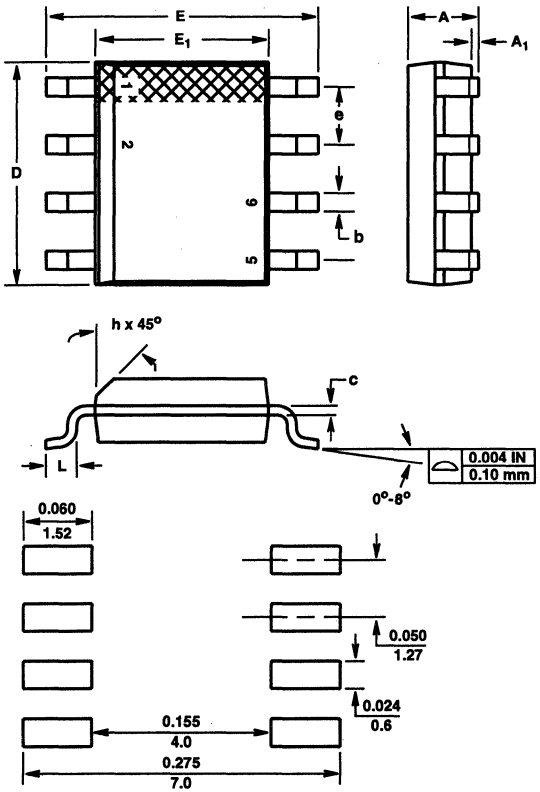
Rev. 1 4/95

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum B dimension by more than 0.08mm (0.003 inch).
7. "N" is the number of terminal positions.

MS-012AA

8 LEAD JEDEC MS-012AA SMALL OUTLINE PLASTIC PACKAGE



MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE-MOUNTED APPLICATIONS

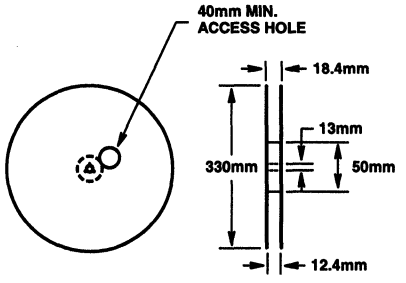
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A_1	0.004	0.0098	0.10	0.25	-
b	0.013	0.020	0.33	0.51	-
c	0.0075	0.0098	0.19	0.25	-
D	0.189	0.1968	4.80	5.00	2
E	0.2284	0.244	5.80	6.20	-
E_1	0.1497	0.1574	3.80	4.00	3
e	0.050 BSC		1.27 BSC		-
H	0.0099	0.0196	0.25	0.50	-
L	0.016	0.050	0.40	1.27	4

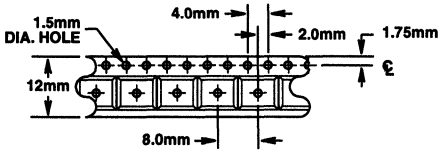
NOTES:

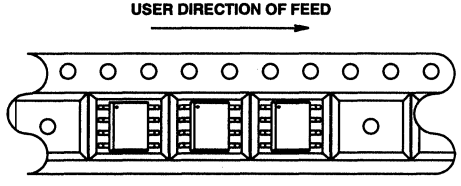
1. All dimensions are within allowable dimensions of Rev. C of JEDEC MS-012AA outline dated 5-90.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006 inches (0.15mm) per side.
3. Dimension "E_1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 inches (0.25mm) per side.
4. "L" is the length of terminal for soldering.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. Controlling dimension: Millimeter.
7. Revision 5 dated 2-23-96.

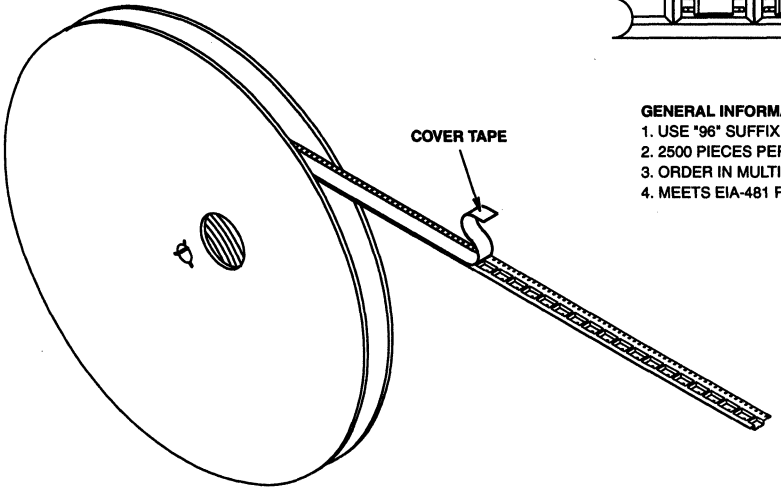
MS-012AA

12mm TAPE AND REEL









GENERAL INFORMATION

1. USE "96" SUFFIX ON PART NUMBER.
2. 2500 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 5 dated 2-96

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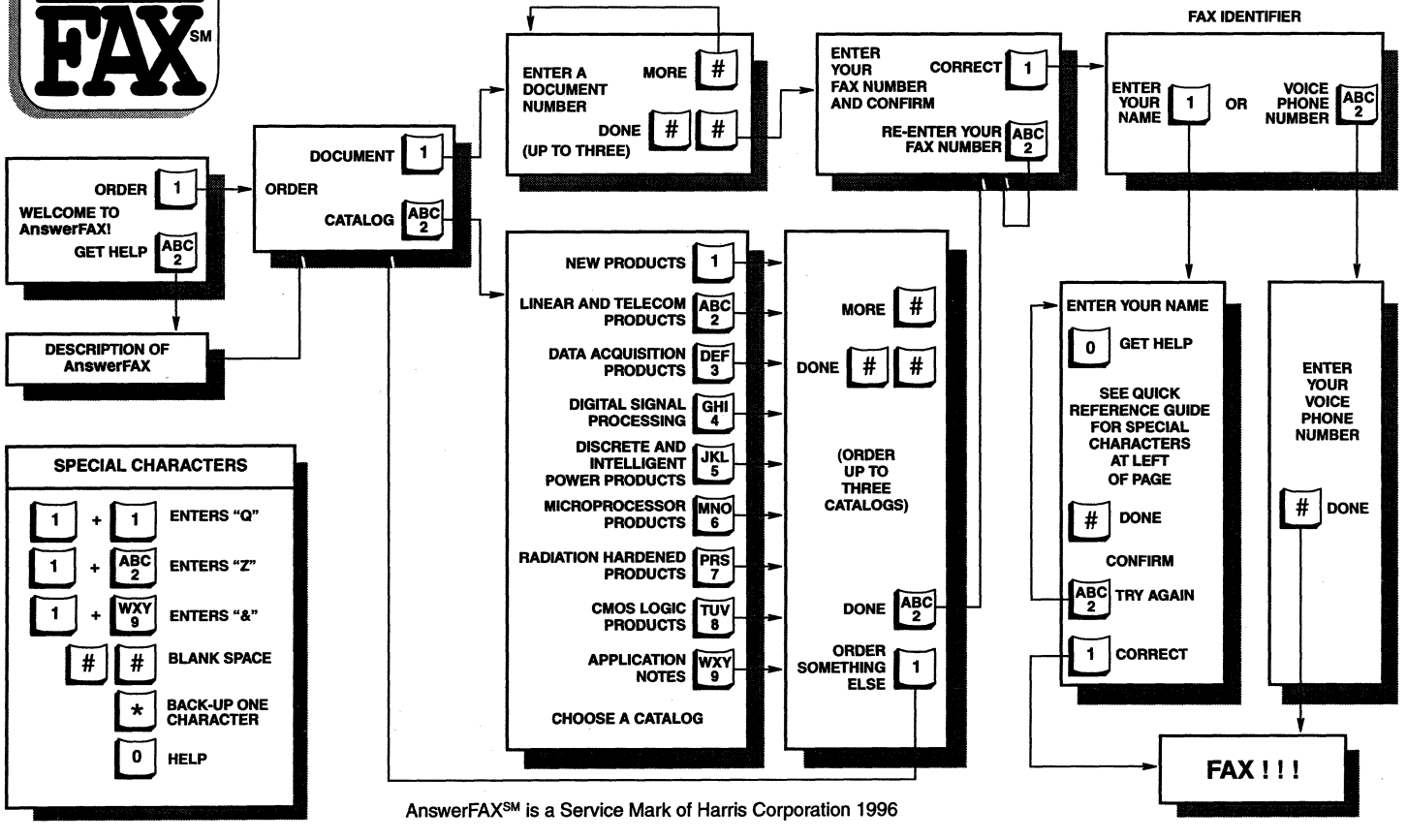

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	DB316	**POWER MOSFET DATA BOOK SUPPLEMENT** (1996: 380pp) This data book contains the data sheets of recently introduced products and also updates some of the data sheets in the Power MOSFET Data Book DB223B. These data sheets contain the detailed specification for these products.
	DB235B	**RADIATION HARDENED** (1993: 2,232pp) The Harris radiation-hardened products include the CD4000, HCS/HCTS and ACS/ACTS logic families, SRAMs, PROMs, op amps, analog multiplexers, the 80C85/80C86 microprocessor family, analog switches, gate arrays, standard cells and custom devices.
	DB260.2	**CDP6805 CMOS MICROCONTROLLERS & PERIPHERALS** (1995: 436pp) This data book represents the full line of Harris Semiconductor CDP6805 products for commercial applications and supersedes previously published CDP6805 data books under the Harris, GE, RCA or Intersil names.
	DB301B	**DATA ACQUISITION** (1994: 1,104pp) Product specifications on A/D converters (display, integrating, successive approximation, flash); D/A converters, switches, multiplexers, and other products.
	DB302B	**DIGITAL SIGNAL PROCESSING** (1994: 528pp) Product specifications on one-dimensional and two-dimensional filters, signal synthesizers, multipliers, special function devices (such as address sequencers, binary correlators, histogrammer).
	DB303	**MICROPROCESSOR PRODUCTS** (1992: 1,156pp) For commercial and military applications. Product specifications on CMOS microprocessors, peripherals, data communications, and memory ICs.
	DB304.1	**INTELLIGENT POWER ICs** (1994: 946pp) This data book includes a complete set of data sheets for product specifications, application notes with design details for specific applications of Harris products, and a description of the Harris quality and high reliability program.
	DB309.1	**MCT/IGBT/DIODES** (1995: 706pp) This MCT/IGBT/Diodes Data book represents the full line of these products made by Harris Semiconductor Discrete Power Products for commercial applications.
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	DB317	**COMMUNICATIONS DATA BOOK** (1997: 708pp) This data book contains technical information including data sheets and application notes for a variety of Harris Integrated Circuits targeted for the communications industry. These products include the PRISM 2.4GHz DSSS Wireless Transceiver Chip Set, the new HC5517 Ringing SLIC as well as Standard Linear, Data Acquisition, DSP and Power products.
	DB450.4	**TRANSIENT VOLTAGE SUPPRESSION DEVICES** (1995: 400pp) Product specifications of Harris varistors and surgectors. Also, general informational chapters such as: "Voltage Transients - An Overview," "Transient Suppression - Devices and Principles," "Suppression - Automotive Transients."
	DB500.3	**LINEAR ICs** (1996/97: 1446pp) Harris offers an extensive line of Linear components including: High Speed and General Purpose Op Amps, Comparators, Sample/Hold Amps, Video Crosspoint Switches, Special Analog Circuits and Transistor Arrays.
	Analog Military	**ANALOG MILITARY** (1989: 1,264pp) This data book describes Harris' military line of Linear, Data Acquisition, and Telecommunications circuits.
	DB312	**ANALOG MILITARY DATA BOOK SUPPLEMENT** (1994: 432pp) The 1994 Military Data Book Supplement, combined with the 1989 Analog Military Product Data Book, contain detailed technical information on the extensive line of Harris Semiconductor Linear and Data Acquisition products for Military (MIL-STD-883, DESC SMD and JAN) applications and supersedes all previously published Linear and Data Acquisition Military data books. For applications requiring Radiation Hardened products, please refer to the 1993 Harris Radiation Hardened Product Data Book (document #DB235B)
	PSG201.23	**PRODUCT SELECTION GUIDE** (1996: 834pp) Key product information on all Harris Semiconductor devices. Sectioned (Linear, Data Acquisition, Digital Signal Processing, Telecom, Intelligent Power, Discrete Power, Digital Microprocessors and Hi-Rel/Military and Rad Hard) for easy use and includes cross references and alphanumeric part number index.
	SG103	**CMOS LOGIC SELECTION GUIDE** (1994: 288pp) This product selection guide contains technical information on Harris Semiconductor High Speed 54/74 CMOS Logic Integrated Circuits for commercial, industrial and military applications. It covers Harris' High Speed CMOS Logic HC/HCT Series, AC/ACT Series, BiCMOS Interface Logic FCT Series and CMOS Logic CD4000B Series.
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FAX: 407 724 7240

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FAX: 407 723 3845

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TEL: (813) 536-5771
FAX: 813 536 6933

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FAX: 317 844 5861

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Stafford, TX 77477
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Burbank, CA 91504-1052
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FAX: (818) 767-7038

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Austin, TX 78754
TEL: (512) 834-2022
FAX: (512) 837-6285

Puerto Rican Authorized Distributor

Hamilton Hallmark
Suite 318
S1 Mariolga Luis Munoz-Marin
Caguas, Puerto Rico 00725
TEL: (800) 327-8950

South American Authorized Distributor

Graftec Electronic Sales Inc.
One Boca Place, Suite 305 East
2255 Glades Road
Boca Raton, Florida 33431
TEL: (561) 994-0933
FAX: 561 994-5518

BRASIL

Graftec Brasil Ltda.
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336 cj. 51/52 Sao Paulo - SP
CEP: 01231-000
TEL: 55-11-826-1666
FAX: 55-11-826-6526

North American Authorized Distributors and Corporate Offices

Hamilton Hallmark and Zeus are the only authorized North American distributors for stocking and sale of Harris Rad Hard Space products.

Alliance Electronics
(SAB Status)
7550 E. Redfield Rd.
Scottsdale, AZ 85260
TEL: (602) 483-9400
(800) 608-9494
FAX: (602) 443 3898

Allied Electronics
7410 Pebble Dr.
Ft. Worth, TX 76118
TEL: (800) 433-5700

Anthem Canada
300 North Rivermede Rd.
Concord, Ontario
Canada L4K 3N6
TEL: (416) 798-4884
FAX: 416 798 4889

Arrow/Schweber Electronics
25 Hub Dr.
Melville, NY 11747
TEL: (800) 777-2776

Bell Microproducts
1941 Ringwood Avenue
San Jose, CA 95131
TEL: (408)451-9400
FAX: (408)451-1600

EMC/Kent Electronics
1150 West Third Avenue
Columbus, OH 43212
TEL: (614) 299-4161
FAX: 614 299 4121

Gerber Electronics
128 Carnegie Row
Norwood, MA 02062
TEL: (617) 769-6000, x156
FAX: 617 762 8931

Hamilton Hallmark
10950 W. Washington Blvd.
Culver City, CA 90230
TEL: (800) 332-8638

Newark Electronics
4801 N. Ravenswood
Chicago, IL 60640
TEL: (312) 784-5100
(800) 367-3673
FAX: 312 275-9596

Wyle Electronics
(Commercial Products)
3000 Bowers Avenue
Santa Clara, CA 95051
TEL: (800) 414-4144
FAX: 801 226-0210

Zeus Electronics, An Arrow Company
2900 Westchester Avenue
Purchase, NY 10577
TEL: (800) 524-4735

Obsolete/Discontinued Products:

Rochester Electronics
10 Malcom Hoyt Drive
Newburyport, MA 01950
TEL: (508) 462-9332
FAX: 508 462 9512

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EBV Elektronik
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A - 1150 Vienna
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Spoerle Electronic
Heiligenstädterasse 50-52
A - 1190 Vienna
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ACAL
Lozenberg 4
B - 1932 Zaventem
TEL: 32 2 720 59 83
FAX: 32 2 725 10 14

EBV Spoerle Electronic
* Keiberg II
Minervastraat, 14/B2
B-1930 Zaventem
TEL: 32 2 725 46 60
FAX: 32 2 725 45 11

EBV Elektronik
* Excelsiorlaan 35B
B - 1930 Zaventem
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Avnet Nortec A/S
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DK - 2730 Herlev
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EBV Elektronik
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DK - 8230 Abyhoj
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Independent Electronic Components
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DK-2000 Frederiksberg
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Arrow Field OY
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Avnet Nortec OY
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EBV Electronics
Pihatorma 1A
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Via A. Simoni 5
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FAX: 39 2 661 01385

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Spoerle Electronic
* Coltbaan 17
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FAX: 31 30 603 5924

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EBV Elektronik
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13 Burn Bridge Oval
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Harris Semiconductor Chip Distributors

Die Technology
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Rood Technology
Test House Mill Lane, Alton
Hampshire GU34 2QG
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Harris Semiconductor China Ltd.
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Edal Electronics Co., Ltd.
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FAX: (852) 2759-8225

Golden Way Electronics (HK) Ltd.
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Lucas Trading
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Kowloon, Hong Kong
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Means Come Ltd.
Room 1007, Harbour Centre
8 Hok Cheung Street
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Sunnice Electronics Co., Ltd.
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Array Electronics Limited
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S M Creative Electronics Ltd
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Micron, Inc.
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