1989

DIGITAL

PRODUCT DATA BOOK

MILITARY

HARRIS

DIGITAL
PRODUCT DATA BOOK
MILITARY

HARRIS

Harris Semiconductor Military & Aerospace Products

This databook contains detailed technical information on the extensive line of military and aerospace digital products currently available from Harris Semiconductor. A sister publication describing analog military and aerospace ICs — "Analog Military Databook" — published in January 1989 is also available. Other high reliability products available under the brand names of **GE, RCA** and **Intersil** — now a part of the **New Harris Semiconductor** — can be found in the two-volume GE Solid State High-Reliability databook. Volume I contains information on CMOS ICs and Volume II covers Analog ICs and Discrete Devices.

Harris CMOS Digital Products

Harris Semiconductor is the eighth largest U.S. merchant semiconductor supplier and is a sector of Harris Corporation. Harris acquired the solid state division of General Electric (including RCA and Intersil semiconductor products) in December 1988. Harris is a pioneer in developing and producing digital CMOS products including: CMOS RAMs, CMOS PROMs, CMOS microprocessors, CMOS peripherals, CMOS data communications products and a full line of 80C286 and 80C86/88 microprocessors and peripherals.

This data book describes Harris Semiconductor's military line of CMOS digital products. It includes a complete set of data sheets for product specifications, application notes with design details for specific applications of Harris products, and a description of the Harris quality and high reliability program.

If you need more information on these and other Harris products, please contact the nearest Harris sales office listed in the back of this data book, or the Harris Semiconductor literature department.

DIGITAL

1989 Military Data Book

ALPHA NUMERIC PRODUCT INDEX

CMOS Devices by Families

Ordering Information

Harris Semiconductor products are represented by an extensive network of factory sales personnel, sales representative, and authorized distributors throughout the world. Please contact your nearest sales office, representative, or distributor for product information, pricing, ordering, or delivery details. A complete list of sales offices is available by contacting the Harris Semiconductor literature department at (407) 724-3739. Headquarters are also listed at the end of this book.

Product Code

Harris products are designated by a "Product Code". This code includes designators for the product family, device type, performance grade, temperature grade and package style. Examples of the product codes are shown below:

PRODUCT CODE EXAMPLE

H M - 1 65162 B /883

PREFIX:
H: Harris

FAMILY:
D: Digital
M: Memory

PACKAGE:
1: Ceramic DIP
1B: Ceramic Sidebrazed DIP
4: Leadless Chip Carrier (LCC)
5: Ceramic Substrate
6: Slimline DIP

PART NUMBER

PERFORMANCE GRADE:
B: High Performance
C: Relaxed Specification
S: High Speed
Blank: Standard Performance

TEMPERATURE GRADE:
-8: -55°C to +125°C Harris Class B Equivalent Devices For Use In Military and Flight Systems
-Q: -55°C to +125°C Harris Class S Equivalent Devices For Use In Spacecraft or High-Rel Applications
/883: Fully Compliant to MIL-STD-883
-BXXX: Altered to Customer Specifications. B Number is Uniquely Assigned to Specific Customer Requirements

MICROPROCESSOR/PERIPHERAL PRODUCT CODE

M D 80C86 - 2 /883

TEMPERATURE RANGE:
M: -55°C to +125°C

PACKAGE:
D: Ceramic DIP
R: Leadless Chip Carrier (LCC)
G: Pin Grid Array

PART NUMBER
80CXXX: CMOS Microprocessor
82CXXX: CMOS Peripherals

SPEED DESIGNATION:

PERIPHERALS	MICROPROCESSORS
5: 5MHz	Blank: 5MHz
Blank: 8MHz	2: 8MHz

TEMPERATURE/GRADE
/883: Fully Compliant to MIL-STD-883

Harris Semiconductor offers Leadless Chip Carriers (LCC) as a packaging option on various Digital integrated circuits. An LCC is a square or rectangular package for an Integrated Circuit (IC) that is manufactured in the same manner as a conventional side-braze dual-in-line package (DIP). The LCC is comprised of the cavity and seal ring section of a standard DIP and offers the user a means of achieving high density system configurations while retaining the reliability benefits of hermetic IC Packaging. Figure 1 provides a comparison of the construction of an LCC and a conventional side-braze DIP.

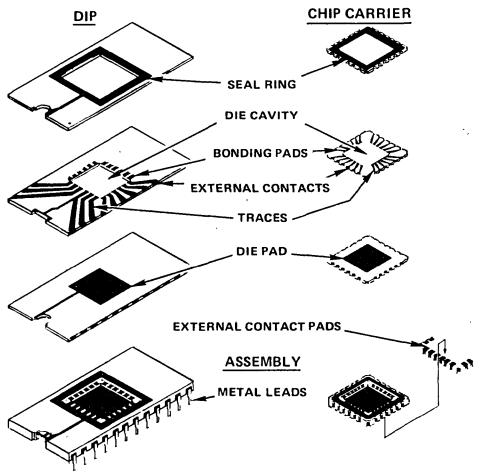


FIGURE 1. EXPLODED VIEW OF CHIP CARRIER AND DIP

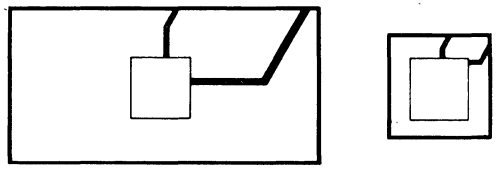
The LCC's two principle advantages over conventional side-braze DIPs are packaging density and electrical performance. Packaging density is the number one advantage to an LCC over a side-braze DIP. The size of a DIP is governed primarily by the number of leads required and not by the size of the IC. As pin count increases, more and more of the DIP package is used only to provide an electrical trace path to the external leads. The size of an LCC is dependent on the size of the die not on the number of leads. As pin count increases, overall size increases but at a much slower rate. Table 1 provides a comparison between the areas of 18, 28 and 48 lead LCCs to 18, 28 and 48 lead side-braze DIPs.

TABLE 1.

LEAD COUNT	LCC AREA	DIP AREA	DIP AREA vs. LCC AREA
18	0.10	0.22	220%
28	0.20	0.84	420%
48	0.31	1.68	542%

(All Units in Square Inches)

The chart indicates a 220% improvement in packaging area for the 18 lead LCC, and 542% improvement for the 48 lead LCC. Obviously, sizeable savings in circuit board area can be achieved with this packaging option. The second major advantage of the LCC is in electrical performance. The package size and geometry also dictates trace length and uniformity. Figure 2 provides a comparison between the trace lengths for various LCCs and side-braze DIPs. As pin count goes up, trace lengths get longer, adding resistance and capacitance unequally around the package. As ICs get faster and more complex these factors start to become a limiting factor on performance. LCCs minimize this effect by maintaining, as close as possible, uniform trace length so that the package is a significantly smaller determinant of system performance.



LEAD COUNT	LONGEST TRACE DIP LONGEST TRACE LCC	LONGEST TRACE SHORTEST TRACE	
		LCC	DIP
18	2:1	1.5:1	6:1
24	4:1	1.5:1	3:1
40	5:1	1.5:1	6:1
54	6:1	1.5:1	7:1

FIGURE 2. ELECTRICAL PERFORMANCE (RESISTANCE AND SPEED)

The LCC also offers environmental advantages over "chip-and-wire" manufacturing techniques used in high density hybrid circuits. An IC can be fully tested, burned-in and processed in an LCC, thereby guaranteeing its performance.

The IC is further protected by a small hermetic package in which internal vapor content can be carefully controlled during production.

Harris Semiconductor Leadless Chip Carriers in both Ceramic and Epoxy provide reliable, high density, high performance packaging options for today's systems.

Consult the factory or your Harris sales representative for pricing and availability.

Self Aligned Junction Isolation (SAJI)

The most prevalent CMOS Technology was patented by Harris (#4,135,955) and has been in production at Harris since 1980. It incorporates self-aligned guard ring techniques and more recently planarization prior to first metal into the traditional complementary transistor structures.

The process begins on 1-0-0 N- type silicon, although a process option is available with N epi over N++ starting material to eliminate circuit latch-up due to parasitic SCR action. A sequence of oxidation, photo resist delineation, Boron implant and diffusion create the P well for the N channel devices. A critical feature of the diffusion causes all of the silicon crystal defects to be annihilated, resulting in a defect free zone for the transistors to be fabricated.

Next, silicon nitride is deposited and etched to define the active NMOS and PMOS areas followed by implants which create the self aligned guard rings around the active devices. These guard rings provide electrical isolation between transistors and also raise the field thresholds of the parasitic MOS devices to allow leakage-free circuit operation. The self aligning of these guard rings allows a substantial reduction in circuit area.

Following is the local oxidation and the conventional formation of the poly gate MOS transistors. The electrical channel length of these all implanted devices is 1.5 micron.

The field oxide and metalization structure are based on a time proved reflowed glass process with one important improvement. Prior to metal deposition the surface is planarized and the walls of the contacts are sloped which creates a final topography with excellent interconnect step coverage. The aluminum interconnect is silicon doped to prevent contact spiking and improved reliability. The passivation, metalization and layout rules guarantee electromigration free operation at +125°C for over ten years.

The principal advantages of the process can be summarized as:

- Low leakage operation
- Latch-up free option
- Good packing density
- Excellent step coverage
- Electromigration free designs

This process has been successfully applied to numerous designs including static RAMs, microprocessors, peripherals, and custom ROM circuits.

L7

A newer, higher performance process, named L7, builds on and enhances the basic CMOS technology. This 1.5 micron process has several advantages over the older 2.5 micron version. The epi over N++ starting material is standard with the epi thickness being scaled down in concert with the P well and device junctions. This brings even more latch-up immunity to all circuits on this technology.

Transistors achieve electrical channel lengths of 1.0μ typical with the N channel incorporating a double diffused LDD structure which eliminates susceptibility to hot electron damage. Of greatest impact is the use of a planarized double layer metal structure allowing greater layout freedom without introducing step coverage or electromigration concerns. The low stress oxinitride passivation provides moisture protection in plastic packages.

The L7 process with its added features has been successfully employed on numerous semicustom and standard cell designs as well as supplying production quantities of the 80C286 microprocessor.

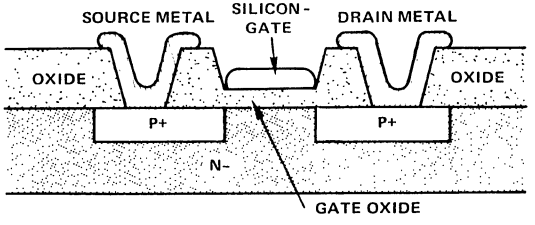


FIGURE 3. SILICON-GATE PFET STRUCTURE

CROSS-SECTION SHOWS THE HEAVILY DOPED SOURCE AND DRAIN REGION. THEY ARE SEPARATED BY THE NARROW GAP OVER WHICH LIES A THIN-GATE OXIDE AND GATE MATERIAL.

IC Handling Procedures

Harris Digital IC processes are designed to produce the most rugged products on the market. However, no semiconductor is immune from damage resulting from the sudden application of many thousands of volts of static electricity. While the phenomenon of catastrophic failure of devices containing MOS transistors or capacitors is well known, even bipolar circuits can be damaged by static discharge, with altered electrical properties and diminished reliability. None of the common IC internal protection networks operate quickly enough to positively prevent damage.

It is suggested that all semiconductors be handled, tested, and installed using standard "MOS handling techniques" of proper grounding of personnel and equipment. Parts and subassemblies should not be in contact with untreated plastic bags or wrapping material. High impedance IC inputs wired to a P.C. connector should have a path to ground on the card.

Handling Rules

Since the introduction of integrated circuits with MOS structures and high quality junctions, a safe and effective means of handling these devices has been of primary importance. One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existence in the industry. In addition, most compensation networks in linear circuits are located at high impedance nodes, where protection networks would disturb normal circuit operation. If static discharge occurs at sufficient magnitude (2kV or more), some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10kV in a low humidity environment. Thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. It is evident, therefore, that proper handling procedures or rules should be adopted.

Elimination or reduction of static charge can be accomplished as follows:

- Use static-free work stations. Static-dissipative mats on work benches and floor, connected to common point ground through a 1MΩ resistor, help eliminate static build-up and discharge. Do not use metallic surfaces.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1MΩ to ground (the 1MΩ resistor will prevent electroshock injury to personnel). Transient product personnel should wear grounding heel straps when conductive flooring is present.
- Smocks and clothing of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold, or aid in the generation of a static charge. Where they cannot be eliminated, natural materials such as cotton should be used to minimize charge generation capacity. Conductive smocks are also available as an alternative.
- Control relative humidity to as high a level as practical. 50% is generally considered sufficient. (Operations should cease if R.H. falls below 25%).
- Ionized air blowers reduce charge build-up in areas where grounding is not possible or practical.
- Devices should be in conductive static-shielded containers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam, or foil.
- In automated handling equipment, the belts, chutes, or other surfaces should be of conducting non-metal material. If this is not possible, ionized air blowers or ionizing bars may be a good alternative.

ESD Handling Procedures

Harris has developed a static control program that enables employees to detect problems generated by static electricity whether on site, in transit, or in the field. Controlling the requirements, methods, materials, and training for static protection of our products is ongoing and updated with new developments in electrostatic prevention. Harris has responded with controls and procedures as part of daily operations to be followed in all areas.

The challenge is to insure all electrostatic control procedures are followed throughout the system — from manufacturing through end use. Unprotected integrated circuits can be destroyed or functionally altered by merely passing them through the electrostatic field of something as simple as styrofoam™ or human contact.

Measures of Protection and Prevention

When handling static sensitive devices, three standard procedures must be followed:

1. Prior to any handling of static-sensitive components, the individual must be properly grounded.
2. All static-sensitive components must be handled at static safeguarded work stations.
3. Containers and packing materials that are static-protective must be used when transporting all static-sensitive components.

Special handling equipment (static-safeguarded work stations, conductive wrist straps, static-protected packaging, ionized air blowers) should be used to reduce damaging effects of electrostatic fields and charges.

Static-safeguarded work station is an area that is free from all damaging electricity, including people. To accomplish this, static on conductors and nonconductors must be controlled.

Controlling electrically conductive items can be accomplished by bonding and grounding techniques. The human body is considered a conductor of electricity and is by far the greatest generator of static electricity. Personnel handling ICs must use conductive wrist straps to ground themselves. Simple body moves act like a variable capacitor, and can create static charges. In addition, conductive clothing is recommended for minimizing electrostatic build up.

Static protective packaging prevents electric field from influencing or damaging ICs. An effective static-protective package exhibits three types of features:

1. Antistatic protection that prevents triboelectric or frictional charging,
2. Dielectric protection that insulates discharging, and
3. Shielding or Faraday cage protection that prevents transient field penetration.

Harris uses only packaging that exhibits all three features. Employees are required to adhere to the same static-protective packaging techiques during handling and shipment to assure device integrity is maintained.

Ionized air blowers aid in neutralizing charges on nonconductors such as synthetic clothing, plastics, and Styrofoam™. The blowers are placed at the work site and in close proximity to the IC handling area, since nonconductors do not lose or drain charges using normal grounding techniques.

By using wrist straps, static-protected work stations and static-protected containers, Harris product quality is maintained throughout the product cycle.

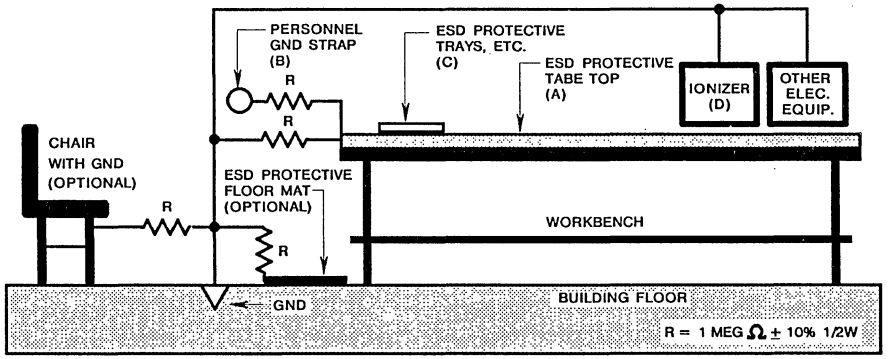


FIGURE 4. STATIC-SAFEGUARDED WORK STATION

NOTE 1. All electrical equipment on the conductive table top must be hard grounded and isolated from the table top.
2. Earth ground is not computer ground or RF ground or any other limited ground.

Styrofoam™ is a trademark of Dow Chemical Corporation

Harris Product Specification Highlights

Harris Semiconductor is a leading supplier of high reliability integrated circuits to the military and aerospace community and takes pride in offering products tailored to the most demanding applications requirements. Our Manufacturing facilities are JAN-Certified to MIL-M-38510 and provide JAN-qualified and MIL-STD-883 compliant products as standard data book items. This Digital Military Products Data Book contains detailed information on high-reliability integrated circuits presently available from Harris Semiconductor.

The intent of the /883 data sheet is to provide to our customers a clear understanding of the testing being performed in conformance with MIL-STD-883 requirements. Additionally, it is our intent to provide the most effective and comprehensive testing feasible.

This data book is organized in 8 different sections, each being identified by the darkened tab index which is provided as a visual guide to the reader. Each section covers a specific topic or product line, such as CMOS Memories, CMOS Microprocessors and General Information. Section 7 emphasizes the Harris commitment to Quality and Reliability in all levels of production, test and documentation, and may be of special interest to military customers.

Document Control

Harris has established each of the /883 data sheets as an internally revision controlled document. Any product revision or modification must be approved and signed-off throughout the manufacturing and engineering sections. Harris has made every effort to ensure accuracy of the information in this data book through quality control methods. Harris reserves the right to make changes to the products contained in this data book to improve performance, reliability and producibility. Each data sheet will use the printed date as the revision control identification. Harris has also established a Data Sheet Registration Program to inform users of data sheet updates. Registration is done through the sign-up card attached to the back of this data book. Otherwise, contact Harris for the latest available specifications and performance data.

/883 Data Sheet Highlights

Each specific /883 data sheet documents the features, description, pinouts, tested electrical parameters, test circuits, burn-in circuits, die characteristics, packaging and design information. The following are notes and clarifications that will help in applying the information provided in the data sheet.

Absolute Maximum Ratings: These ratings are provided as maximum stress ratings and should be taken into consideration during system design to prevent conditions which may cause permanent damage to the device. Operation of the device at or above the "Absolute Maximum Ratings" is not intended, and extended exposure may affect the device reliability.

Reliability Information: Each /883 data sheet contains thermal information relating to the package and die. This information is intended to be used in system design for determining the expected device junction temperatures for overall system reliability calculations.

Packaging: Harris utilizes MIL-M-38510, Appendix C for packages used for /883 products. The mechanical dimensions and materials used are shown for each individual product to complete each data sheet as a self contained document.

D.C. and A.C. Electrical Parameters: Tables 1 and 2 define the D.C. and A.C. Electrical Parameters that are 100% tested in production to guarantee compliance to MIL-STD-883. The subgroups used are defined in MIL-STD-883, Method 5005 and designated under the provisions of Paragraph 1.2.1a. Test Conditions and Test Circuits are provided for specific parameter testing.

Table 3 provides additional device limits that are guaranteed by characterization of the device and are not directly tested in production. Characterization takes place at initial device design and after any major process or design changes. The characterization data is on file and available demonstrating the test limits established.

Table 4 provides a summary of the test requirements and the applicable MIL-STD-883 subgroups.

Burn-in Circuits: The Burn-in circuits defined in the individual data sheets are those used in the actual production process. Burn-in is conducted per MIL-STD-883, Method 1015.

Design Information Sections: Harris provides an additional Design Information Section in many of the data sheets to assist in system application and design. This information may be in the form of applications circuits, typical device parameters, or additional device related user information such as programming information. While this information cannot be guaranteed, it is based on actual characterization of the product and is representative of the data sheet device.

High Reliability Products Information

Harris' High Reliability Products are all produced in accordance with military specifications and standards, primarily MIL-M-38510 (General Specifications for Microcircuits) and MIL-STD-883 (Test Methods and Procedures for Microelectronics).

MIL-M-38510 provides the ground rules for standardization in the manufacturing, testing and qualification of Integrated Circuits which are applicable to all qualified suppliers. MIL-M-38510 delineates two product assurance levels of screening, sampling, and documentation control requirements (Class S and Class B).

Class S is intended for use in manned space flight or extreme high reliability aerospace applications where replacement is extremely difficult or impossible.

Class B is intended for use in unmanned space flight, high reliability ground systems or commercial "hi-reliability use". These devices are the most frequently procured military ICs.

MIL-STD-883 contains test methods and procedures for various electrical, mechanical and environmental tests as well as requirements for screening, qualification and quality conformance inspection. Method 5004 of MIL-STD-883 lists the 100% screening tests which are required for each of the product assurance classes defined above.

Following the device screening, samples are removed from the production lot(s) for Quality Conformance Inspection testing. This testing is divided into four inspection groups: A, B, C and D, which are performed at prescribed intervals per MIL-M-38510 to assure the processes are in control and to ensure the continued quality level of the product being produced.

Group A electrical inspection involves dynamic, static, functional and switching tests at maximum, minimum and ambient operating temperatures. Sample sizes and specific tests performed depend upon the particular product assurance class chosen. Electrical test sampling is performed on all subgroups as defined in MIL-STD-883, Method 5005.

Group B inspection includes tests for marking permanency, internal visual and mechanical correctness, bond strength, and solderability. It is intended to provide assurance of the absence of lot-to-lot fabrication and manufacturing variances. Group B tests are again defined in test Method 5005.

Group C is oriented toward die integrity and consists of operating life testing as defined in MIL-STD-883, Method 5005.

Group D environmental testing is provided to verify die and package reliability. Among the Group D tests are lead integrity, hermeticity, temperature cycling, thermal and mechanical shock, and constant acceleration.

MIL-M-38510 requires that Group A and Group B inspection be performed on each lot, while Group C inspection must be done every 3 months and Group D every 6 months to be in compliance with MIL-M-38510 JAN requirements. To limit the amount of testing, MIL-M-38510 allows the multitude of microcircuits to be grouped by technology, commonly known as "generic families". Thus, one group C performed will cover all parts included in that generic family for three months. For Group D, which is package related, although there are some restrictions, one Group D performed on a 24-pin ceramic dual-in-line packaged part will cover all devices in the same package regardless of the technology group.

For MIL-STD-883 products, Groups A and B are required on each lot, Groups C and D are required every 52 weeks by generic die family and package fabricated and manufactured from the same plant as the die and package represented.

General Test Philosophy

The general philosophy for test set development is to supply test software that guarantees the high performance and quality of the products being designed and manufactured by Harris. The general final test set includes a guardbanded initial test program and a QA test program for the quality test step. Characterization software is an additional test program that parametrically measures and records the performance of the device under test. This test set is used to evaluate the performance of a product and to determine the acceptability of non-standard Source Control Drawings. BSPEC test programs are custom final test programs written to conform to customer specifications.

The general test development strategy is to develop software using a "shell" programming technique which creates standard test program flows, and reduces test development and execution times. Statistically derived guardbands are utilized in the "shell" programs to null out test system variability. High performance hardware interface designs are incorporated for maximized test effectiveness, and efficient fault graded vector sets are utilized for functional and AC testing.

The initial step in generating the test set is the test vector generation. The test vectors are the binary stimulus applied to the device under test to functionally test the operation of the product. The vectors are developed against a behavioral model that is a software representation of the device functionality. The output of the behavioral model can be translated directly to ATE test vectors or prepared for CAD simulation.

The philosophy in the generation of test vectors is to develop efficient fault graded patterns with a goal of greater than 90% fault coverage. There is no intent to generate a worst case or best case noise vector set. The intent is to maximize fault coverage through efficient vector use. Generally only one vector set will be required to enable complete test coverage within a given test program. Exceptions to this would be vector generation to test certain identified critical AC speed paths or DC vectors for testing VIH/VIL parameters. These vector sets typically will not increase fault coverage and can not be substituted for fault graded vector sets.

The ultimate goal for testing all military /883, SMD and JAN products is data sheet compliancy, thoroughness, and quality of testing. By taking this approach to test set generation, Harris is capable of supplying high performance semiconductors of the highest quality to the marketplace.

TechBrief

No. 52 February 1989

Harris Digital

ELECTROSTATIC DISCHARGE CONTROL A GUIDE TO HANDLING INTEGRATED CIRCUITS

This paper discusses methods and materials recommended for protection of ICs against ESD damage or degradation during manufacturing operations vulnerable to ESD exposure. Areas of concern include dice prep and handling, dice and package inspection, packing, shipping, receiving, testing, assembly and all operations where ICs are involved.

All integrated circuits are sensitive to electrostatic discharge (ESD) to some degree. Since the introduction of integrated circuits with MOS structures and high quality junctions, safe and effective means of handling these devices have been of primary importance.

If static discharge occurs at a sufficient magnitude, 2kV or greater, some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10kV in a low humidity environment; thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. Avoiding any damage or degradation by ESD when handling devices during the manufacturing flow is therefore essential.

ESD Protection and Prevention Measures

One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existence in the industry.

In areas where ICs are being handled, certain equipment should be utilized to reduce the damaging effects of ESD. Typically, equipment such as grounded work stations, conductive wrist straps, conductive floor mats, ionized air blowers and conductive packaging materials are included in the IC handling environment. Any time an individual intends to handle an IC, in any way, they must insure they have been grounded to eliminate circuit damage.

Grounding personnel can, practically, be performed by two methods. First, grounded wrist straps which are usually made of a conductive material, such as Velostat or metal. A resistor value of 1 megohm (1/2 watt) in series with the strap to ground completes a discharge path for ESD when the operator wears the strap in contact with the skin. Another method is to insure direct physical contact with a grounded, conductive work surface.

This consists of a conductive surface like Velostat, covering the work area. The surface is connected to a 1 megohm (1/2 watt) resistor in series with ground.

In addition to personnel grounding, areas where work is being performed with ICs, should be equipped with an ionized air blower. Ionized air blowers force positive and negative ions simultaneously over the work area so that any nonconductors that are near the work surface would have their static charge neutralized before it would cause device damage or degradation.

Relative humidity in the work area should be maintained as high as practical. When the work environment is less than 40% RH, a static build-up condition can exist on nonconductors allowing stored charges to remain near the ICs causing possible static electricity discharge to ICs.

Integrated circuits that are being shipped or transported require special handling and packaging materials to eliminate ESD damage. Dice or packaged devices should be in conductive carriers during all phases of transport and handling. Leads of packaged devices can be shorted by tubular metalic carriers, conductive foam or foil.

Do's and Don'ts for Integrated Circuit Handling

Do's

Do keep paper, nonconductive plastic, plastic foams and films or cardboard off the static controlled conductive bench top. Placing devices, loaded sticks or loaded burn-in boards on top of any of these materials effectively insulates them from ground and defeats the purpose of the static controlled conductive surface.

Do keep hand creams and food away from static controlled conductive work surfaces. If spilled on the bench top, these materials will contaminate and increase the resistivity of the work area.

Do be especially careful when using soldering guns around conductive work surfaces. Solder spills and heat from the gun may melt and damage the conductive mat.

Do check the grounded wrist strap connections daily. Make certain they are snugly fitted before starting work with the product.

Do put on grounded wrist strap before touching any devices. This drains off any static build-up from the operator.

Do know the ESD caution symbols.

Do remove devices or loaded sticks from shielding bags only when grounded via wrist strap at grounded work station. This also applies when loading or removing devices from the antistatic sticks or the loading on or removing from the burn-in boards.

Do wear grounded wrist straps in direct contact with the bare skin - never over clothing.

Do use the same ESD control with empty burn-in boards as with loaded boards if boards contain permanently mounted ICs as part of driver circuits.

Do insure electrical test equipment and solder irons at an ESD control station are grounded and only uninsulated metal hand tools be used. Ordinary plastic solder suckers and other plastic assembly aids shall not be used.

Do use ionizing air blowers in static controlled areas when the use of plastic (nonconductive) materials cannot be avoided.

Don'ts

Don't allow anyone not grounded to touch devices, loaded sticks or loaded burn-in boards. To be grounded they must be standing on a conductive floor mat with conductive heel straps attached to footwear or must wear a grounded wrist strap.

Don't touch the devices by the pins or leads unless grounded since most ESD damage is done at these points.

Don't handle devices or loaded sticks during transport from work station to work station unless protected by shielding bags. These items must never be directly handled by anyone not grounded.

Don't use freon or chlorinated cleaners at a grounded work area.

Don't wax grounded static controlled conductive floor and bench top mats. This would allow build-up of an insulating layer and thus defeating the purpose of a conductive work surface.

Don't touch devices or loaded sticks or loaded burn-in boards with clothing or textiles even though grounded wrist strap is worn. This does not apply if conductive coats are worn.

Don't allow personnel to be attached to hard ground. There must always be 1 megohm series resistance (1/2 watt between the person and the ground).

Don't touch edge connectors of loaded burn-in boards or empty burn-in boards containing permanently mounted driver circuits when not grounded. This also applies to burn-in programming cards containing ICs.

Don't unload stick on a metal bench top allowing rapid discharge of charged devices.

Don't touch leads. Handle devices by their package even though grounded.

Don't allow plastic "snow or peanut" polystyrene foam or other high dielectric materials to come in contact with devices or loaded sticks or loaded burn-in boards.

Don't allow rubber/plastic floor mats in front of static controlled work benches.

Don't solvent-clean devices when loaded in antistatic sticks since this will remove antistatic inner coating from sticks.

Don't use antistatic sticks for more than one throughput process. Used sticks should not be reused unless recoated.

Recommended Maintenance Procedures

Daily:

Perform visual inspection of ground wires and terminals on floor mats, bench tops, and grounding receptacles to ensure that proper electrical connections via 1 megohm resistor (1/2 watt) exist.

Clean bench top mats with a soft cloth or paper towel dampened with a mild solution of detergent and water.

Weekly:

Damp mop conductive floor mats to remove any accumulated dirt layer which causes high resistivity.

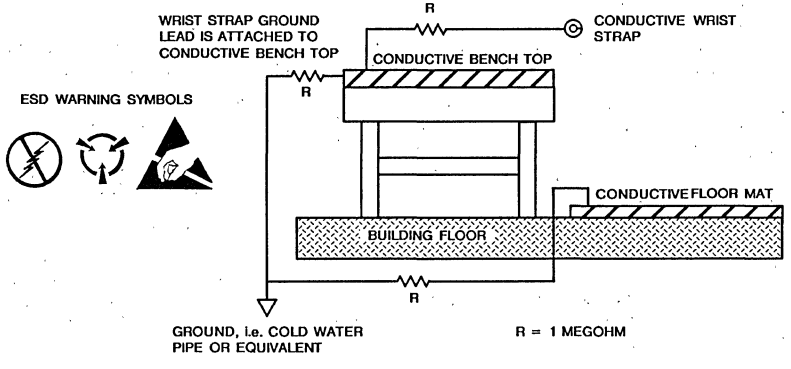
Annually:

Replace nuclear elements for ionized air blowers.

Review ESD protection procedures and equipment for updating and adequacy.

Static Controlled Work Station

The figure below shows an example of a work bench properly equipped to control electro-static discharge. Note that the wrist strap is connected to a 1 megohm resistor. This resistor can be omitted in the setup if the wrist strap has a 1 megohm assembled on the cable attached.



DIGITAL

Military Programs

2

Military Grade Product Offerings

Harris High Reliability Products are offered in the following Military grades:

- **JAN (Joint Army Navy)**

  Registered trademark of the U.S. Government indicating that a device is fully compliant to MIL-M-38510. The Defense Electronics Supply Center (DESC) maintains a continuing audit of manufacturing compliance. There are two product assurance classes available for M38510 products (Class S and B). Devices are defined and identified by their particular detail specification or "slash sheet" number issued by DESC (eg. M38510/29104BJX). The IC manufacturers who are qualified to supply products to a particular M38510 slash sheet are identified in the Qualified Products List (QPL) issued by DESC.

- **SMD (Standard Military Drawing)**

  The SMD evolved from the DESC drawing program which was viewed as a preliminary specification prior to JAN approval. SMDs were created to control the proliferation of non-standard Source Control Drawings. The Standard Military Drawing provides standardized MIL-STD-883 processing in conjunction with non-JAN devices as specified in paragraph 1.2.1 of MIL-STD-883. These devices are defined and identified by their Standard Military Drawing number issued by DESC (eg. 5962-8757701RA). The manufacturers qualified to supply a particular SMD device are listed in the back of the individual Standard Military Drawing.

- **Harris Class B Compliant**

  These devices are fully compliant to MIL-STD-883, Class B and are identified by the /883 suffix on the Harris part number. The parametric limits for an /883 data sheet are controlled by the manufacturer rather than a governmental agency, and therefore, there may be differences in the test methodology and actual limits for "similar" devices made by different manufacturers.

  This manufacturer control of the /883 specifications allows the offering of 883-level products long before they might become available as MIL-M-38510 or SMD devices. In many cases, Harris actually specifies /883 devices with more stringent conditions than those appearing on the MIL-M-38510 slash sheet or SMD describing the same generic device. Harris recommends using our /883 data sheets as the baseline for new military or aerospace source control drawings.

- **Harris Class B "Equivalent"**

  These devices are processed and tested in a manner equivalent to the MIL-STD-883 compliant devices. They may not be classified as compliant since government standards have not been established for processing these types of components (eg. Ram Modules). The Class B "Equivalent" products can be identified by the -8 suffix on the Harris part number.

- **Non-Standard Product Offerings**

  Harris understands the need for customer generated Source Control Drawings with non-standard parameter and/or screening requirements. A Customer Engineering Department is responsible for efficiently expediting the SCDs through a comprehensive review process. Our Customer Engineering Group compares the SCD to its closest equivalent product grade and works closely with the Product Engineer, Manufacturing Engineer, Design Engineer, or applicable individual to compare Harris' screening ability against the customer's non-standard requirement(s). For products processed to non-standard requirements, a unique part number suffix is assigned.

  Harris shares the military's objective to utilize standards wherever possible. We recommend using our /883 data sheets as guidelines for generating new Source Control Drawings. In instances where an available military specification or Harris /883 data sheet is inappropriate, it is Harris' sincerest wish to work closely with the customer in establishing an acceptable procurement document. For this reason, the customer is requested to contact the nearest Harris Sales Office or Representative before finalizing the Source Control Drawing. Harris looks forward to working with the customer prior to implementation of the formal drawing so that both parties may create a mutually acceptable procurement document.

Harris/883/JAN/DESC Part Number Listing

HARRIS PART #	JAN PART #	SMD/DESC PART #	/883 PART #
MICROPROCESSOR PRODUCTS			
MG80C286-12			MG80C286-12/883
MG80C286-10			MG80C286-10/883
MD82C284-12			MD82C284-12/883
MD82C284-10			MD82C284-10/883
MD82C288-12			MD82C288-12/883
MD82C288-10			MD82C288-10/883
MD80C86		8405201QA	MD80C86/883
MR80C86		8405201XA	MR80C86/883
MD80C86-2			MD80C86-2/883
MR80C86-2			MR80C86-2/883
MD80C88			MD80C88/883
MR80C88			MR80C88/883
MD80C88-2			MD80C88-2/883
MR80C88-2			MR80C88-2/883
MD82C37A			MD82C37A/883
MR82C37A			MR82C37A/883
MD82C37A-5			MD82C37A-5/883
MR82C37A-5			MR82C37A-5/883
MD82C52		8501501XA	MD82C52/883
MR82C52		85015013A	MR82C52/883
MD82C54		8406501JA	MD82C54/883
MR82C54		84065013A	MR82C54/883
MD82C55A		8406602QA	MD82C55A/883
MR82C55A		8406602XA	MR82C55A/883
MD82C55A-5		8406601QA	MD82C55A-5/883
MR82C55A-5		8406601XA	MR82C55A-5/883
MD82C59A		5962-8501602YA	MD82C59A/883
MR82C59A		5962-85016023A	MR82C59A/883
MD82C59A-5		5962-8501601YA	MD82C59A-5/883
MR82C59A-5		5962-85016013A	MR82C59A-5/883
MD82C82		8406701RA	MD82C82/883
MR82C82		84067012A	MR82C82/883
MD82C83H		8406702RA	MD82C83H/883
MR82C83H		84067022A	MR82C83H/883
MD82C84A		8406801VA	MD82C84A/883
MR82C84A		84068012A	MR82C84A/883
MD82C85			MD82C85/883
MR82C85			MR82C85/883
MD82C86H-5		5962-8757701RA	MD82C86H-5/883
MR82C86H-5		5962-87577012A	MR82C86H-5/883
MD82C87H-5		5962-8757702RA	MD82C87H-5/883
MR82C87H-5		5962-87577022A	MR82C87H-5/883
MD82C88		8406901RA	MD82C88/883
MR82C88		84069012A	MR82C88/883
MD82C89		5962-8552801RA	MD82C89/883
MR82C89		5962-85528012A	MR82C89/883

Harris/883/JAN/DESC Part Number Listing

HARRIS PART #	JAN PART #	SMD/DESC PART #	/883 PART #
DATA COMMUNICATION PRODUCTS			
HD1-6409			HD1-6409/883
HD1-15530		7802901JA	HD1-15530/883
HD4-15530		78029013A	HD4-15530/883
HD1-15531			HD1-15531/883
HD1-15531B			HD1-15531B/883
HD1-4702			HD1-4702/883
HD1-6402			HD1-6402/883
CMOS MEMORY PRODUCTS			
1K CMOS STATIC RAMs			
HM1-6508			HM1-6508/883
HM1-6508B			HM1-6508B/883
HM1-6518			HM1-6518/883
HM1-6518B			HM1-6518B/883
HM1-6551			HM1-6551/883
HM1-6551B			HM1-6551B/883
HM1-6561			HM1-6561/883
HM1-6561B			HM1-6561B/883
4K CMOS STATIC RAMs			
HM1-6504		8102405VA	HM1-6504/883
HM1-6504B		8102403VA	HM1-6504B/883
HM1-6504S	M38510/24501BVA		HM1-6504S/883
HM1-6514		8102406VA	HM1-6514/883
HM1-6514B		8102404VA	HM1-6514B/883
HM1-6514S	M38510/24502BVA		HM1-6514S/883
16K CMOS SYNCHRONOUS STATIC RAMs			
HM1-6516	M38510/29102BJA		HM1-6516/883
HM4-6516	M38510/29102BXA		HM4-6516/883
HM1-6516B		8403607JA	HM1-6516B/883
HM4-6516B		8403607ZA	HM4-6516B/883
16K CMOS ASYNCHRONOUS STATIC RAMs			
HM1-65162	M38510/29104BJA		HM1-65162/883
HM4-65162	M38510/29104BXA		HM4-65162/883
HM1-65162B	M38510/29110BJA		HM1-65162B/883
HM4-65162B	M38510/29110BXA		HM4-65162B/883
HM1-65162C		8403603JA	HM1-65162C/883
HM4-65162C		8403603ZA	HM4-65162C/883
HM1-65262	M38510/29103BRA		HM1-65262/883
HM4-65262	M38510/29103BYA		HM4-65262/883
HM1-65262B	M38510/29109BRA		HM1-65262B/883
HM4-65262B	M38510/29109BYA		HM4-65262B/883

Harris/883/JAN/DESC Part Number Listing

HARRIS PART #	JAN PART #	SMD/DESC PART #	/883 PART #
CMOS MEMORY PRODUCTS (CONTINUED)			
64K CMOS STATIC RAMs			
HM1-65642			HM1-65642/883
HM4-65642			HM4-65642/883
HM1-65642B	M38510/29205BXA		HM1-65642B/883
HM4-65642B	M38510/29205BYA		HM4-65642B/883
HM1-65642C			HM1-65642C/883
HM4-65642C			HM4-65642C/883
CMOS FUSE LINK PROMs			
HM1-6617			HM1-6617/883
HM4-6617			HM4-6617/883
HM6-6617			HM6-6617/883
HM1-6617B			HM1-6617B/883
HM4-6617B			HM4-6617B/883
HM6-6617B			HM6-6617B/883
HM1-6642			HM1-6642/883
HM4-6642			HM4-6642/883
HM6-6642			HM6-6642/883
HM1-6642B			HM1-6642B/883
HM4-6642B			HM4-6642/883
HM6-6642B			HM6-6642B/883
CMOS STATIC RAM MODULES			
HM5-6564			
HM5-8808			
HM5-8808B	Harris CMOS Static RAM Modules are available for military and high reliability applications processed to our high-rel DASH 8 program flow. This includes burn-in and value added processing (temperature cycling, SEM inspection, etc.) Please contact your local Harris sales office or representative for details.		
HM5-8808S			
HM5-8808A			
HM5-8808AB			
HM5-8808AS			
HM5-8816H			
HM5-8832			
HM5-8832B			
HM5-92560			
HM5-92570			

Military Product Program Controls

	REQUIREMENT	883 REFERENCE	JAN	DESC/SMD	/883	-8
SYSTEM CONTROLS	Product Assurance Plan	1.2.1.B.21	Per Appendix A of MIL M38510			Per Harris R&QA Manual
	Facility Certification	1.2.1.B.28	RADC/DESC	Harris QC	Harris QC	Harris QC
	Product Certification	1.2.1.B.26	RADC/DESC	RADC/DESC	Harris QA	Not Required
	Detail Specifications	1.2.1.A	Slash Sheet	DESC DWG/ SMD	Harris /883 Data Sheet	Harris Catalog
	Qualifying Activity	1.2.1.B.1	RADC/DESC	Harris	Harris	Harris
	Qualification Test GPC	1.2.1.B.17	Required	Per Governing Military Spec	Per Governing Military Spec	Per Harris Spec
	Qualification Test GPD	1.2.1.B.17	Required	Per Governing Military Spec	Per Governing Military Spec	Per Harris Spec
	QPL Listing		MIL M38510	None	None	None
	Change Controls	1.2.1.B.25	MIL M38510 para 3.4.2	DoD 480	DoD 480	Harris Internal ECN Controls
	Change Notification	1.2.1.B.25	DESC	DESC	Data Sheet Registration	Catalog
	Traceability	1.2.1.B.27	Wafer Lot	6 Week Seal	6 Week Seal	6 Week Seal
	Deviations to 883	1.2.1	Per Slash Sheet	Per DESC DWG/SMD	None	Per Harris Spec
	Product Construction	1.2.1.B.2-12	Compliant	Compliant	Compliant	May Be Non-Compliant
LOCATIONS	Fab		USA Only	USA	USA	USA
	Assembly		USA Only	USA/Malaysia	USA/Malaysia	Malaysia
	Screening		USA Only	USA/Malaysia	USA/Malaysia	Malaysia
	Quality Conformance		USA Only	USA	USA	Malaysia

† -8 is available in support of programs with part requirements dated prior to Dec. 31, 1984 in accordance with paragraph 1.2. of MIL-STD-883 or where 883 is not currently available.

Programs Served By Harris

Tube-Launched, Optically Tracked, Wire-Guided Missile
Angle Rate Bombing Set
Advanced Medium Range Air-To-Air Missile
Advanced Capability (MK-48 Torpedo)
Position Location and Reporting System
Joint Tactical Information Distribution System
Target Acquisition System (MK-23)
Miniature Vehicle Sensors
Driver's Thermal Viewer
Detecting and Ranging Set
Fighting Vehicle System (Bradley)
Helicopter (or Hughes) Night Vision System
Advanced Optic Adjunct
Advanced Light Weight Torpedo
Ground Launched Cruise Missile
Air Launched Cruise Missile
Medium Range Air-To-Surface Missile
Modular Universal Laser Equipment
Low Altitude Navigation and Targeting Infrared
Anti-Submarine Warfare
Multiple Launch Rocket System
Advanced Self Protection Jammer
Global Positioning System
Distant Early Warning
High Speed Anti-Radar Missile
Rolling Airframe Missile
Medium Depth Mine
Terminal Guidance Small Missile
Time Division Multiple Access
Distributed Time Division Multiple Access
Long Range Search and Track
Glide Bomb Unit
Divisional Air Defense

Field Support Tracked Vehicle
Integrated Solar Sensor Assembly
Continuous Motion Gyro for ISSA
Advanced Warning and Control System
Forward Looking Infrared
Ring Laser Gyro Programs
Tail Warning System
Space Telescope
Mariner Series
MK 46 NEARTIP
AV8B HARRIER
F14/A6E SMS
Bearclaw
CAINS II
TAI/MK6
B1
F-16
Phalanx
Stinger
Locust
Sidearm
Rattler
Pavetack
Viking
Skylab
Shuttle
Intelsat
Spacelab
Voyager
Mark 50
Captor
Maverick
Phoenix

DIGITAL

CMOS Memory

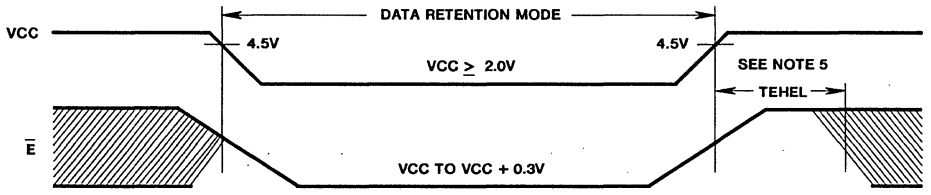
3

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retendtion:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC to VCC +0.3V
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC +0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL (for synchronous RAMs) and > 5ns (for asynchronous RAMs) after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



HARRIS CMOS RAMs

Industry CMOS RAM Cross Reference

DESCRIPTION	HARRIS	AMD	EDI	FUJI-ITSU	HIT-ACHI	IDT	MITSU-BISHI	MOT-OROLA	NAT-IONAL	NEC	OKI	HARRIS/RCA	SMOS	TOSH-IBA	NMOS, OTHER
1K CMOS RAMs															
1k x 1, 16 Pin Synchronous	HM-6508			8401				6508	6508 74C929	443		6508 1821		5508	2125, 4015
1K x 1, 18 Pin Synchronous	HM-6518							6518	6518 74C930						
256 x 4, 22 Pin Synchronous	HM-6551								6551 74C920			1822 5101		5101	2101
256 x 4, 18 Pin Synchronous	HM-6561														2111
4K CMOS RAMs															
4K x 1, 18 Pin Synchronous	HM-6504	92L44		8404	4315 6147			6504	6504		5104		6504	5504	2141, 2147 315D, 4104 4404
1K x 4, 18 Pin Synchronous	HM-6514	91L14 91L24		8414	4334 6148		58981	6514	6514	444	5114 5115	5114	6514	5514	2114, 2148 2149, 4045 314A
16K CMOS RAMs															
2K x 8, 24 Pin Synchronous	HM-6516								6516						
2K x 8, 24 Pin Asynchronous	HM-65162			8416	6116	6116	5117	65116	6116	446	5128	6116	2016	5517	4802, 2116 2016, 4016
16K x 1, 20 Pin Asynchronous	HM-65262			8167	6167	6167							2267 2367		2167, 8167 1400
64K CMOS RAMs															
8K x 8, 28 Pin Asynchronous	HM-65642 HM-8808A* HM-8808*	99C88	8808A 8808	8464	6264	7164 7M864 8M864	5164	6164	6164	4464		6264	2064 2264	5564 5565	
128K CMOS RAM MODULE															
16K x 8, 28 Pin Asynchronous	HM-8816H		8816H												
256K CMOS RAM MODULE															
32K x 8/16K x 16 48 Pin Module Asynchronous	HM-92560 HM-92570														
32K x 8 28 Pin Module Asynchronous	HM-8832		8832												
1M CMOS MODULE															
128 x 8/64K x 16	HM-91M2														

*CMOS RAM Module

HARRIS

HM-6508/883

June 1989

1024 x 1 CMOS RAM

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby ..... 50µW Max.
- Low Power Operation ..... 20mW/MHz Max.
- Fast Access Time..... 180ns Max.
- Data Retention ..... 2.0V Min.
- TTL Compatible Input/Output
- High Output Drive - 2 TTL Loads
- On-Chip Address Register

Description

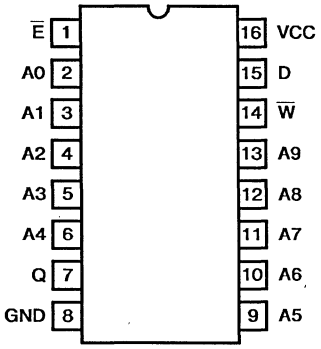
The HM-6508/883 is a 1024 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6508/883 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

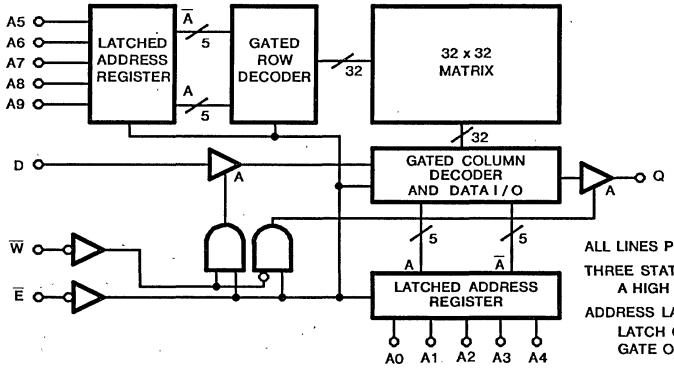
Pinout

HM1-6508/883 (CERAMIC DIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

Functional Diagram



ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON FALLING EDGE OF $\overline{E}$
GATE ON FALLING EDGE OF $\overline{E}$

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Typical Derating Factor ..... 1.5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	75°C/W	15°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.67 Watt
Gate Count ..... 1925 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VCC-2.0V to VCC
Input Rise and Fall Time ..... 40ns Max.

TABLE 1. HM-6508B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 3.2mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -0.4mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5 V, VO = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC IO = 0mA, VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	5	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 3) $\overline{E}$ = 1MHz, IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.0V, IO = 0mA VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 3.2mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6508B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	(1)TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	180	ns
Address Access Time	(2)TAVQV	VCC = 4.5 and 5.5V Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	180	ns
Chip Enable Output Enable Time	(3)TELQX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Write Enable Output Disable Time	(4)TWLQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	120	ns
Chip Enable Output Disable Time	(5)TEHQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	120	ns
Chip Enable Pulse Negative Width	(6)TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	180	-	ns
Chip Enable Pulse Positive Width	(7)TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Address Setup Time	(8)TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Address Hold Time	(9)TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Data Setup Time	(10)TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	80	-	ns
Data Hold Time	(11)TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Enable Write Pulse Setup Time	(12)TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Chip Enable Write Pulse Hold Time	(13)TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Write Enable Pulse Width	(14)TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Read or Write Cycle Time	(15)TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	280	-	ns

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6508B/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	6	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	10	pF

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Typical Derating Factor ..... 1.5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	75°C/W	15°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.67 Watt
Gate Count ..... 1925 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VCC-2.0V to VCC
Input Rise and Fall Time ..... 40ns Max.

TABLE 1. HM-6508/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 3.2mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -0.4mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5 V, VO = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC IO = 0mA, VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 3) $\overline{E}$ = 1MHz, IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 3.2mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6508/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	(1)TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	250	ns
Address Access Time	(2)TAVQV	VCC = 4.5 and 5.5V Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	250	ns
Chip Enable Output Enable Time	(3)TELQX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Write Enable Output Disable Time	(4)TWLQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	160	ns
Chip Enable Output Disable Time	(5)TEHQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	160	ns
Chip Enable Pulse Negative Width	(6)TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	250	-	ns
Chip Enable Pulse Positive Width	(7)TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Address Setup Time	(8)TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Address Hold Time	(9)TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Data Setup Time	(10)TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	110	-	ns
Data Hold Time	(11)TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Enable Write Pulse Setup Time	(12)TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	130	-	ns
Chip Enable Write Pulse Hold Time	(13)TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	130	-	ns
Write Enable Pulse Width	(14)TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	130	-	ns
Read or Write Cycle Time	(15)TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	350	-	ns

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6508/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	6	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	10	pF

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

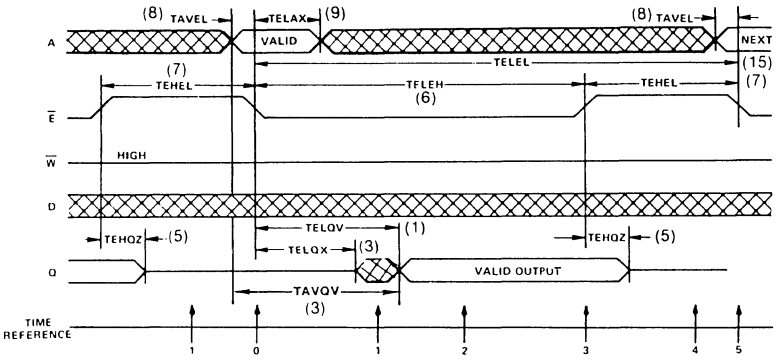
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Timing Waveforms

READ CYCLE



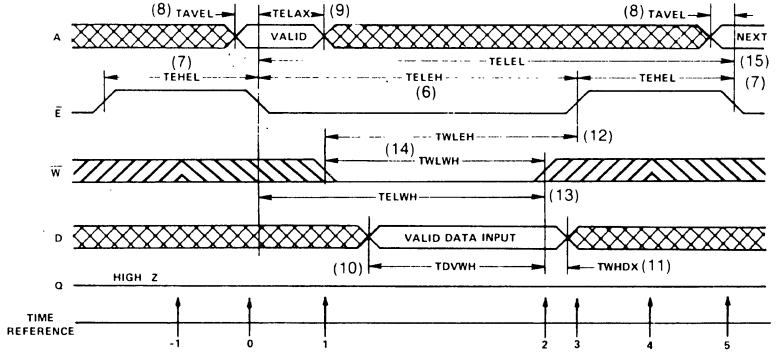
TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	X	Output Enabled
2	L	H	X	X	V	Output Valid
3	↑	H	X	X	V	Read Accomplished
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the HM-6508/883 Read Cycle, the address information is latched into the on chip registers on the falling edge of Ē (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the data output becomes enabled; however, the data is not valid until during time (T = 2). W̄ must remain high for the read cycle. After the output data has been read, Ē may return high (T = 3). This will disable the chip and force the output buffer to a high impedance state. After the required Ē high time (TEHEL) the RAM is ready for the next memory cycle (T = 4).

Timing Waveforms (Continued)

WRITE CYCLE



TRUTH TABLE

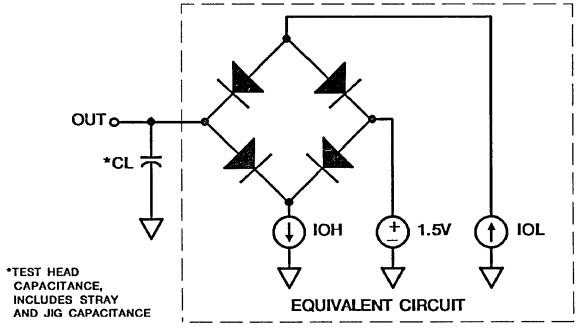
TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	X	V	X	Z	Cycle Begins, Addresses are Latched
1	L	↓	X	X	Z	Write Period Begins
2	L	↑	X	V	Z	Data is Written
3	↑	H	X	X	Z	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as both $\overline{E}$ and $\overline{W}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$ or $\overline{W}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

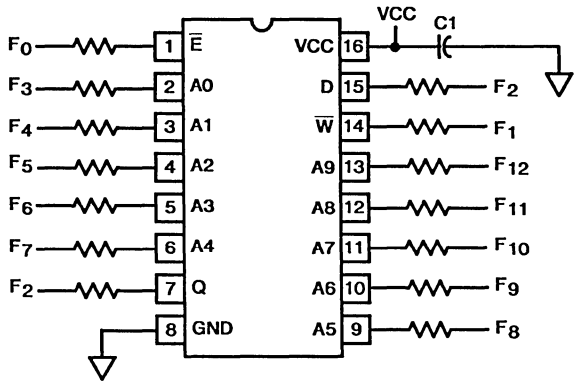
If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TELQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH). The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

Test Load Circuit



Burn-In Circuit

HM-6508/883 CERAMIC DIP



NOTES:
All Resistors 47kΩ ± 5%
F_0 = 100kHz ± 10%
$F_1 = F_0 \div 2$, $F_2 = F_1 \div 2$, $F_3 = F_2 \div 2 \cdots F_{12} = F_{11} \div 2$
VCC = 5.5V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to +0.4V
C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
130 x 150 x 19 ± 1 mils

METALLIZATION:
Type: Si-Al
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

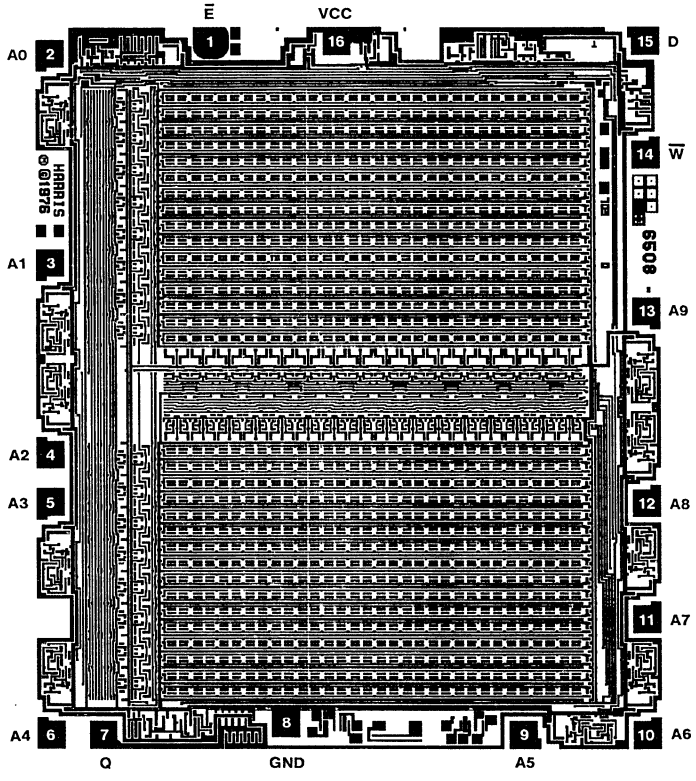
DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$1.342 \times 10^5 A/cm^2$

LEAD TEMPERATURE (10 seconds soldering):
≤300°C

Metallization Mask Layout

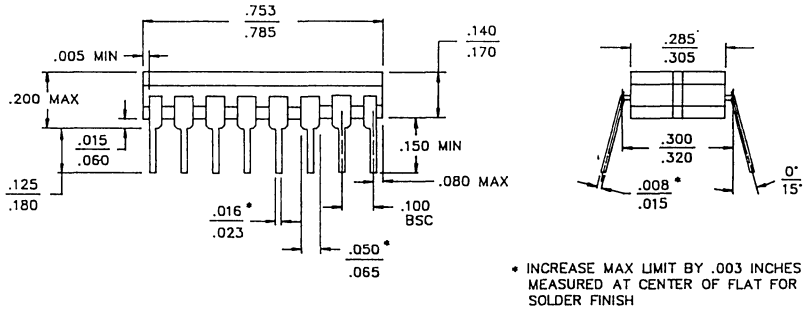
HM-6508/883



NOTE: Pin Numbers Correspond to DIP Package Only.

Packaging†

16 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HM-6518/883

June 1989

1024 x 1 CMOS RAM

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby ..... 50μW Max.
- Low Power Operation ..... 20mW/MHz Max.
- Fast Access Time..... 180ns Max.
- Data Retention ..... @ 2.0V Min.
- TTL Compatible Input/Output
- High Output Drive - 2 TTL Loads
- High Noise Immunity
- On-Chip Address Register
- Two-Chip Selects for Easy Array Expansion
- Three-State Output

Description

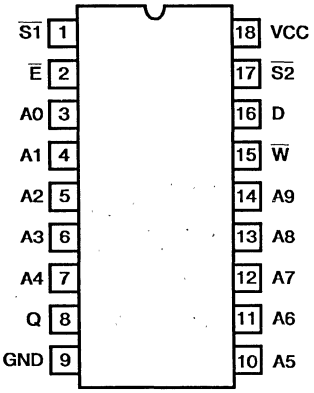
The HM-6518/883 is a 1024 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6518/883 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

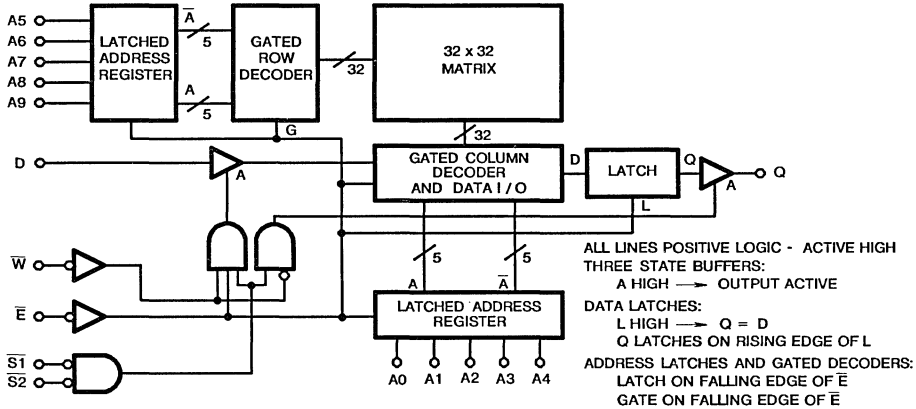
Pinout

HM1-6518/883 (CERAMIC DIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
S	Chip Select
D	Data Input
Q	Data Output

Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

	θ_{ja}	θ_{jc}
Thermal Resistance		
Ceramic DIP Package	75°C/W	18°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.67 Watt
Gate Count ..... 1936 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VCC-2.0V to VCC
Input Rise and Fall Time ..... 40ns Max.

TABLE 1. HM-6518/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 3.2mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -0.4mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5 V, VO = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC IO = 0mA, VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 3) $\overline{E}$ = 1MHz, IO =0mA VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 3.2mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6518/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	(1)TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	250	ns
Address Access Time	(2)TAVQV	VCC = 4.5 and 5.5V Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	250	ns
Chip Select Output Enable Time	(3)TSLQX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Write Enable Output Disable Time	(4)TWLQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	160	ns
Chip Select Output Disable Time	(5)TSHQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	160	ns
Chip Enable Pulse Negative Width	(6)TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	250	-	ns
Chip Enable Pulse Positive Width	(7)TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Address Setup Time	(8)TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Address Hold Time	(9)TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Data Setup Time	(10)TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	110	-	ns
Data Hold Time	(11)TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Select Write Pulse Setup Time	(12)TWLSH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	130	-	ns
Chip Enable Write Pulse Setup Time	(13)TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	130	-	ns
Chip Select Write Pulse Hold Time	(14)TSLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	130	-	ns
Chip Enable Write Pulse Hold Time	(15)TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	130	-	ns
Write Enable Pulse Width	(16)TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	130	-	ns
Read or Write Cycle Time	(17)TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	350	-	ns

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 3.2mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6518/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, T_A = +25°C, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	6	pF
Output Capacitance	CO	VCC = Open, T_A = +25°C, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	10	pF

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 3.2mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
Ceramic DIP Package ..... 75°C/W 18°C/W
Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.67 Watt
Gate Count ..... 1936 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VCC-2.0V to VCC
Input Rise and Fall Time ..... 40ns Max.

TABLE 1. HM-6518B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 3.2mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -0.4mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5 V, VO = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC IO = 0mA, VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	5	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 3) $\overline{E}$ = 1MHz, IO =0mA VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 3.2mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6518B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	(1)TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	180	ns
Address Access Time	(2)TAVQV	VCC = 4.5 and 5.5V Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	180	ns
Chip Select Output Enable Time	(3)TSLQX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Write Enable Output Disable Time	(4)TWLQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	120	ns
Chip Select Output Disable Time	(5)TSHQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	120	ns
Chip Enable Pulse Negative Width	(6)TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	180	-	ns
Chip Enable Pulse Positive Width	(7)TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Address Setup Time	(8)TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Address Hold Time	(9)TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Data Setup Time	(10)TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	80	-	ns
Data Hold Time	(11)TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Select Write Pulse Setup Time	(12)TWLSH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Chip Enable Write Pulse Setup Time	(13)TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Chip Select Write Pulse Hold Time	(14)TSLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Chip Enable Write Pulse Hold Time	(15)TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Write Enable Pulse Width	(16)TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Read or Write Cycle Time	(17)TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	280	-	ns

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 3.2mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6518B/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, T_A = +25°C, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	6	pF
Output Capacitance	CO	VCC = Open, T_A = +25°C, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	10	pF

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

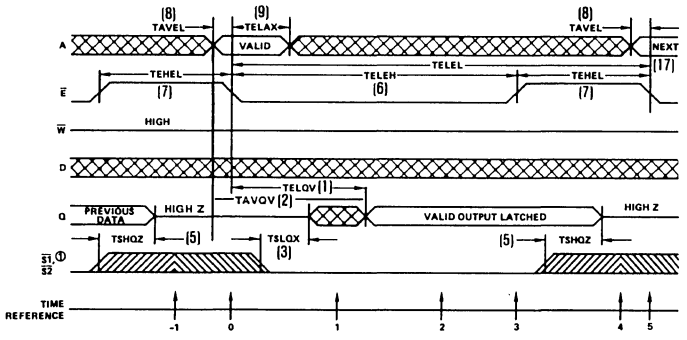
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Timing Waveforms

READ CYCLE



TRUTH TABLE

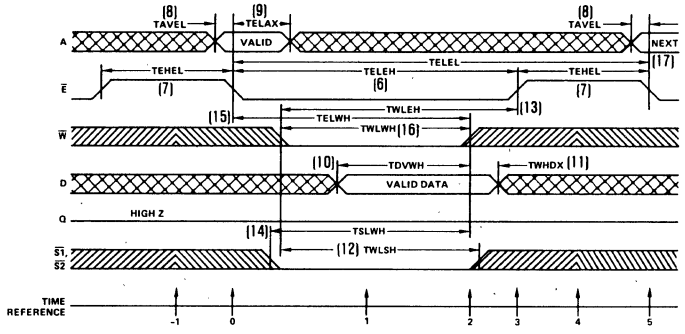
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	H	X	X	X	Z	Memory Disabled
0	↓	X	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	X	Output Enabled
2	L	L	H	X	X	V	Output Valid
3	↑	L	H	X	X	V	Output Latched
4	H	H	X	X	X	Z	Device Disabled, Prepare for Next Cycle (Same as -1)
5	↓	X	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high

In the HM-6518/883 read cycle the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. In order for the output to be read $\overline{S1}$, $\overline{S2}$ and $\overline{E}$ must be low, $\overline{W}$ must be high. When $\overline{E}$ goes high the output data is latched into an on chip register. Taking either or both $\overline{S1}$ or $\overline{S2}$ high forces the output buffer to a high impedance state. The output data may be re-enabled at any time by taking $\overline{S1}$ and $\overline{S2}$ low. On the falling edge of $\overline{E}$ the data will be unlatched.

Timing Waveforms (Continued)

WRITE CYCLE



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	S1	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	X	Z	Memory Disabled
0	↓	X	X	V	X	Z	Cycle Begins, Addresses are Latched
1	L	L	L	X	V	Z	Write Mode has Begun
2	L	↓	L	X	V	Z	Data is Written
3	↑	X	X	X	X	Z	Write Completed
4	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

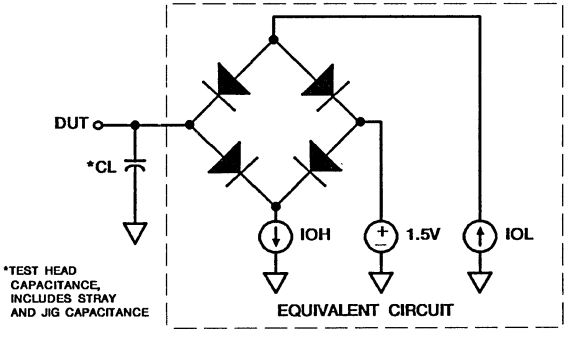
NOTE: 1. Device selected only if both S1 and S2 are low, and deselected if either S1 or S2 are high.

The write cycle is initiated by the falling edge of Ē which latches the address information into the on chip registers. The write portion of the cycle is defined as Ē, W̄, S1 and S2 being low simultaneously. W̄ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either Ē, W̄, S1 or S2. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the W̄ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of Ē. By positioning the W̄ pulse at different times within the Ē low time (TELEH), various types of write cycles may be performed. If the Ē low time (TELEH) is greater than the W̄ pulse (TWLWH) plus an output enable time (TSLQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

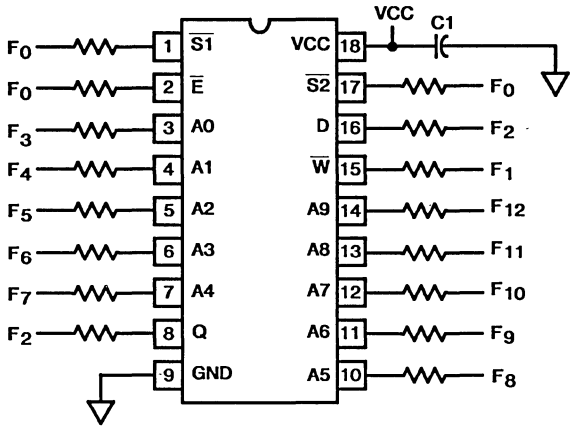
The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after W̄ goes low before applying input data to the bus. This will insure that the output buffers are not active.

Test Load Circuit



Burn-In Circuit

HM1-6518/883 CERAMIC DIP



NOTES:

All Resistors 47kΩ ± 5%

F_0 = 100kHz ± 10%

$F_1 = F_0 \div 2$, $F_2 = F_1 \div 2$, $F_3 = F_2 \div 2 \cdots F_{12} = F_{11} \div 2$

VCC = 5.5V ± 0.5V

VIH = 4.5V ± 10%

VIL = -0.2V to +0.4V

C1 = 0.01μF Min.

Die Characteristics

DIE DIMENSIONS:
130 x 150 x 19 ± 1 mils

METALLIZATION:
Type: Si-Al
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

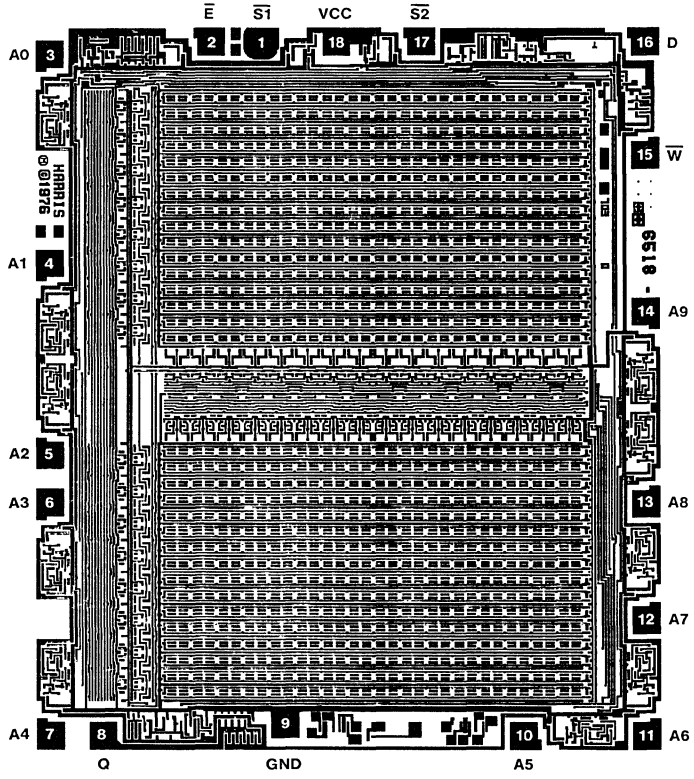
DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$1.342 \times 10^5 A/cm^2$

LEAD TEMPERATURE (10 seconds soldering):
≤300°C

Metallization Mask Layout

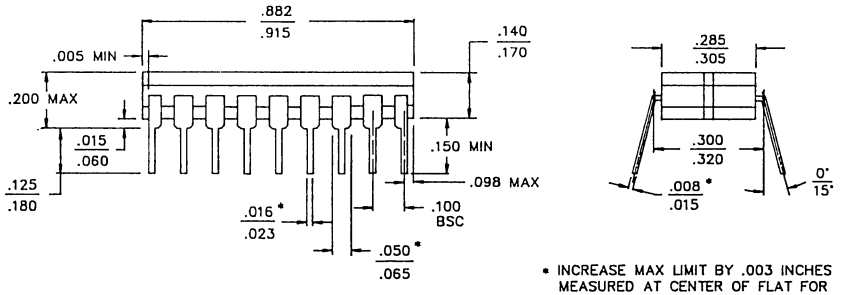
HM-6518/883



NOTE: Pin Numbers Correspond to DIP Package Only.

Packaging†

18 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-6

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HM-6551/883

June 1989

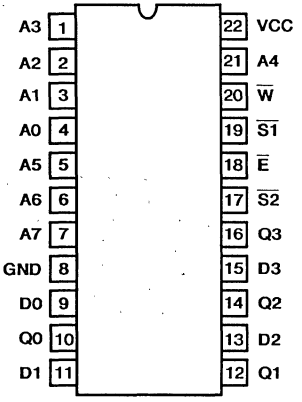
256 x 4 CMOS RAM

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby ..... 50µW Max.
- Low Power Operation ..... 20mW/MHz Max.
- Fast Access Time..... 220ns Max.
- Data Retention ..... @ 2.0V Min.
- TTL Compatible Input/Output
- High Output Drive - 1 TTL Load
- Internal Latched Chip Select
- High Noise Immunity
- On-Chip Address Register
- Latched Outputs
- Three-State Output

Pinout

HM1-6551/883 (CERAMIC DIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
D	Data Input
Q	Data Output

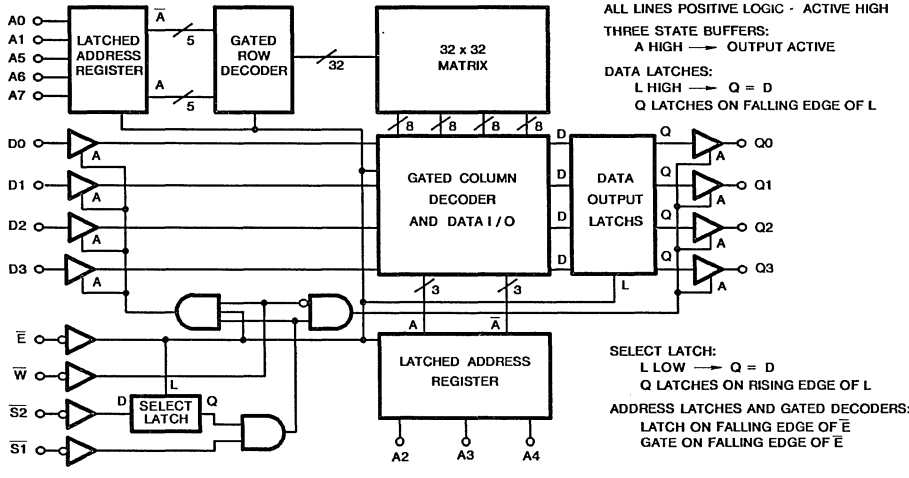
Description

The HM-6551/883 is a 256 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6551/883 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	60°C/W	15°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.83 Watt
Gate Count ..... 1930 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VCC-2.0V to VCC
Input Rise and Fall Time ..... 40ns Max.

TABLE 1. HM-6551B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 1.6mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -0.4mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5 V, VO = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC IO = 0mA, VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 3) $\overline{E}$ = 1MHz, IO =0mA VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6551B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	(1)TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	220	ns
Address Access Time	(2)TAVQV	VCC = 4.5 and 5.5V Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	220	ns
Chip Select 1 Output Enable Time	(3)TS1LQX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Write Enable Output Disable Time	(4)TWLQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	130	ns
Chip Select 1 Output Disable Time	(5)TS1HQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	130	ns
Chip Enable Pulse Negative Width	(6)TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	220	-	ns
Chip Enable Pulse Positive Width	(7)TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Address Setup Time	(8)TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Select 2 Setup Time	(9)TS2LEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Address Hold Time	(10)TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Chip Select 2 Hold Time	(11)TELS2X	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Data Setup Time	(12)TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Data Hold Time	(13)TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Select 1 Write Pulse Setup Time	(14)TWLS1H	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Chip Enable Write Pulse Setup Time	(15)TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Chip Select 1 Write Pulse Hold Time	(16)TS1LWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Chip Enable Write Pulse Hold Time	(17)TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Write Enable Pulse Width	(18)TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Read or Write Cycle Time	(19)TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	320	-	ns

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6551B/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	10	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	12	pF

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
Ceramic DIP Package ..... 60°C/W 15°C/W
Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.83 Watt
Gate Count ..... 1930 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VCC-2.0V to VCC
Input Rise and Fall Time ..... 40ns Max.

TABLE 1. HM-6551/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 1.6mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -0.4mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5 V, VO = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC IO = 0mA, VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 3) $\overline{E}$ = 1MHz, IO =0mA VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6551/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	(1)TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	300	ns
Address Access Time	(2)TAVQV	VCC = 4.5 and 5.5V Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	300	ns
Chip Select 1 Output Enable Time	(3)TS1LQX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Write Enable Output Disable Time	(4)TWLQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	150	ns
Chip Select 1 Output Disable Time	(5)TS1HQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	150	ns
Chip Enable Pulse Negative Width	(6)TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	300	-	ns
Chip Enable Pulse Positive Width	(7)TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Address Setup Time	(8)TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Select 2 Setup Time	(9)TS2LEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Address Hold Time	(10)TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Chip Select 2 Hold Time	(11)TELS2X	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Data Setup Time	(12)TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Data Hold Time	(13)TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Select 1 Write Pulse Setup Time	(14)TWLS1H	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	180	-	ns
Chip Enable Write Pulse Setup Time	(15)TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	180	-	ns
Chip Select 1 Write Pulse Hold Time	(16)TS1LWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	180	-	ns
Chip Enable Write Pulse Hold Time	(17)TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	180	-	ns
Write Enable Pulse Width	(18)TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	180	-	ns
Read or Write Cycle Time	(19)TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	400	-	ns

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6551/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	$T_A = +25^oC$	-	10	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	$T_A = +25^oC$	-	12	pF

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

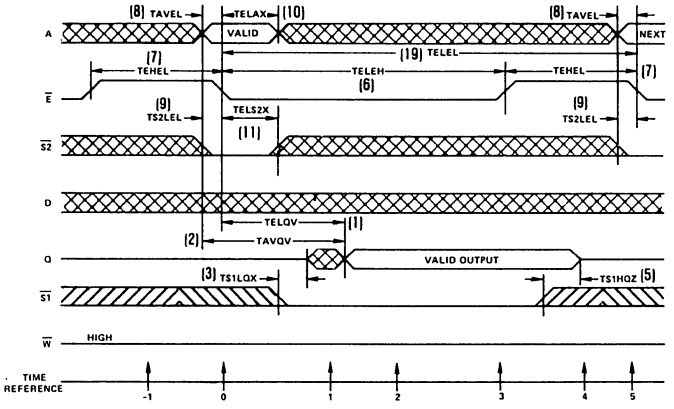
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Timing Waveforms

READ CYCLE



TRUTH TABLE

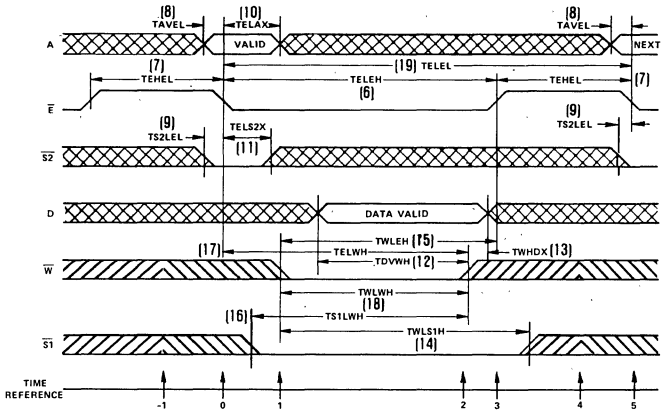
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↓	X	L	H	V	X	Z	Addresses and $\overline{S2}$ are Latched, Cycle Begins
1	L	L	X	H	X	X	X	Output Enabled But Undefined
2	L	L	X	H	X	X	V	Data Output Valid
3	↑	L	X	H	X	X	V	Outputs Latched, Valid Data, $\overline{S2}$ Unlatches
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	L	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The HM-6551/883 Read Cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word and $\overline{S2}$ into on chip registers providing the minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. $\overline{S2}$ acts as a high order address and simplifies decoding. For the output to be read, $\overline{E}$, $\overline{S1}$ must be low and $\overline{W}$ must be high. $\overline{S2}$ must have been latched low on the falling edge of $\overline{E}$. The output data will be valid at access time (TELQV).

The HM-6551/883 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains in that state until $\overline{E}$ falls. Also on the rising edge of $\overline{E}$, $\overline{S2}$ unlatches and controls the outputs along with $\overline{S1}$. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Timing Waveforms (Continued)

WRITE CYCLE



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	S1	S2	W	A	D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↘	X	L	X	V	X	Z	Cycle Begins, Addresses and S2 are Latched
1	L	L	X	↘	X	X	Z	Write Period Begins
2	L	L	X	↗	X	V	Z	Data in is Written
3	↗	X	X	H	X	X	Z	Write is Completed
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	L	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

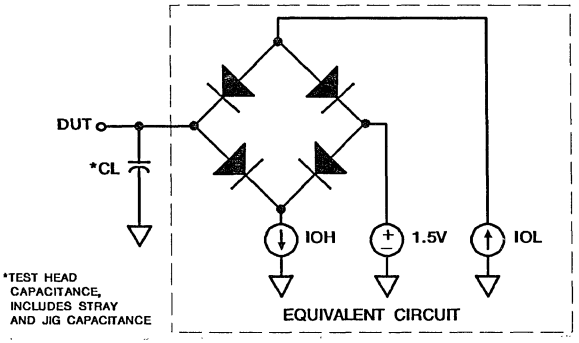
In the Write Cycle the falling edge of Ē latches the addresses and S2 into on chip registers. S2 must be latched in the low state to enable the device. The write portion of the cycle is defined as Ē, W, S1 being low and S2 being latched simultaneously. The W line may go low at any time during the cycle providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either Ē, W, or S1.

If a series of consecutive write cycles are to be executed, the W line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of Ē or S1.

By positioning the write pulse at different times within the Ē and S1 low time (TELEH), various types of write cycles may be performed. If the S1 low time (TS1LS1H) is greater than the W pulse plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

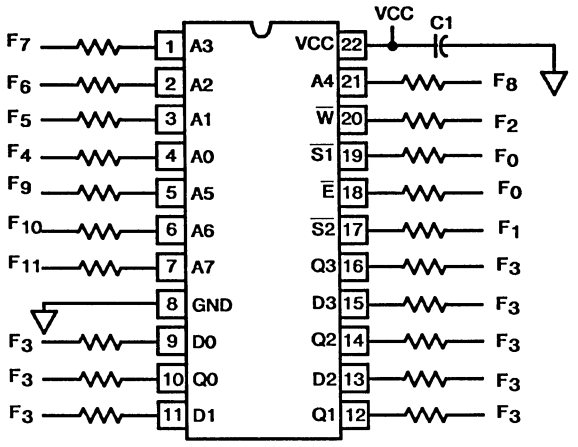
The HM-6551/883 be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the W line. In the write cycle, when W goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.

Test Load Circuit



Burn-In Circuit

HM1-6551/883 CERAMIC DIP



NOTES:

All Resistors 47kΩ ± 5%

F_0 = 100kHz ± 10%

$F_1 = F_0 + 2$, $F_2 = F_1 + 2$, $F_3 = F_2 + 2 \cdots F_{12} = F_{11} + 2$

VCC = 5.5V ± 0.5V

VIH = 4.5V ± 10%

VIL = -0.2V to +0.4V

C1 = 0.01μF Min.

Die Characteristics

DIE DIMENSIONS:
132 x 160 x 19 ± 1 mils

METALLIZATION:
Type: Si-Al
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

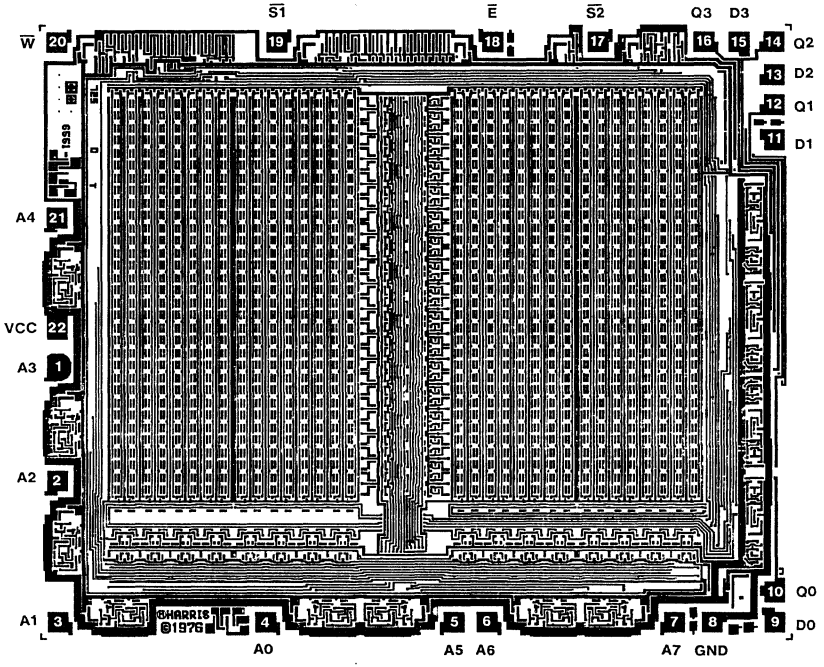
DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$1.337 \times 10^5 A/cm^2$

LEAD TEMPERATURE (10 seconds soldering):
≤300°C

Metallization Mask Layout

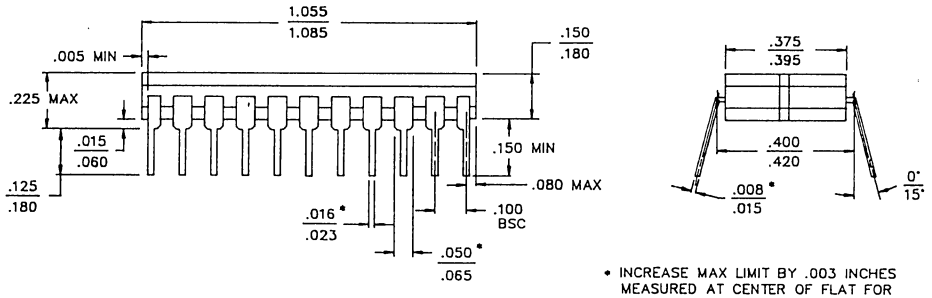
HM-6551/883



NOTE: Pin Numbers Correspond to DIP Package Only.

Packaging†

22 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-7

3
CMOS MEMORY

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS HM-6561/883

June 1989

256 x 4 CMOS RAM

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby ..... 50µW Max.
- Low Power Operation ..... 20mW/MHz Max.
- Fast Access Time..... 200ns Max.
- Data Retention ..... @ 2.0V Min.
- TTL Compatible Input/Output
- High Output Drive - 1 TTL Load
- On-Chip Address Registers
- Common Data In/Out
- Three-State Output
- Easy Microprocessor Interfacing

Description

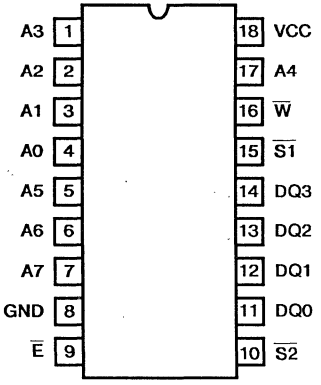
The HM-6561/883 is a 256 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM-6561/883 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

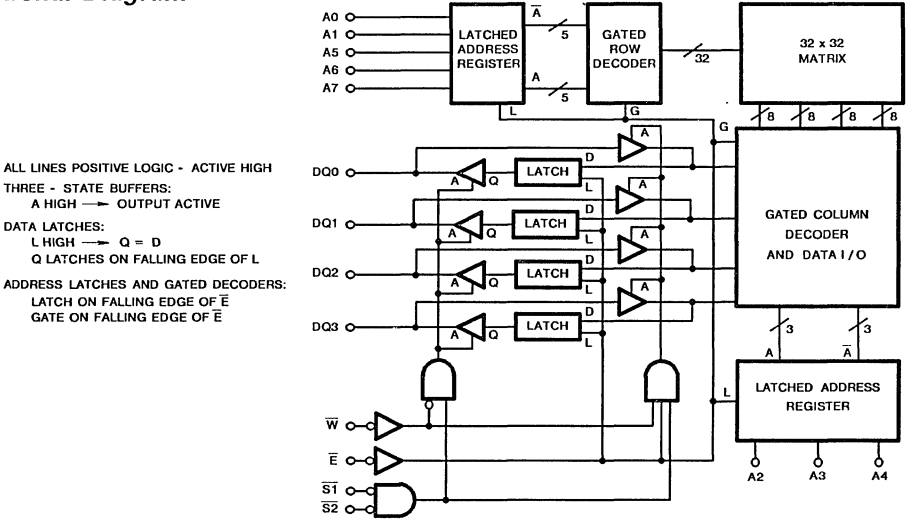
Pinout

HM1-6561/883 (CERAMIC DIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
DQ	Data In/Out

Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	74°C/W	18°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.68 Watt
Gate Count ..... 1944 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0.0V to 0.8V
Input High Voltage ..... VCC-2.0V to VCC
Input Rise and Fall Time ..... 40ns Max.

TABLE 1. HM-6561B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 1.6mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -0.4mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Input/Output Leakage Current	IIOZ	VCC = 5.5 V, VIO = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC IO = 0mA,	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 3) $\overline{E}$ = 1MHz, $\overline{W}$ =GND VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6561B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	(1)TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	220	ns
Address Access Time	(2)TAVQV	VCC = 4.5 and 5.5V Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	220	ns
Chip Select Output Enable Time	(3)TSLQX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Select Output Disable Time	(4)TSHQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	120	ns
Chip Enable Pulse Negative Width	(5)TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	220	-	ns
Chip Enable Pulse Positive Width	(6)TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Address Setup Time	(7)TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Address Hold Time	(8)TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Data Setup Time	(9)TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Data Hold Time	(10)TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Write Data Delay Time	(11)TWLDV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
Chip Select Write Pulse Setup Time	(12)TWLSH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Chip Enable Write Pulse Setup Time	(13)TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Chip Select Write Pulse Hold Time	(14)TSLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Chip Enable Write Pulse Hold Time	(15)TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Write Enable Pulse Width	(16)TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Read or Write Cycle Time	(17)TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	320	-	ns

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6561B/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	8	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	10	pF

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied ..... GND-0.3V to VCC+0.03V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	74°C/W	18°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.68 Watt
Gate Count ..... 1944 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... -0.3V to +0.8V
Input High Voltage ..... VCC-2.0V to VCC+0.3V
Input Rise and Fall Time ..... 40ns Max.

TABLE 1. HM-6561/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 1.6mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -0.4mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Input/Output Leakage Current	IIOZ	VCC = 5.5 V, VIO = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC IO = 0mA,	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 3) $\overline{E}$ = 1MHz, $\overline{W}$ =GND VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA VI = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6561/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	(1)TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	300	ns
Address Access Time	(2)TAVQV	VCC = 4.5 and 5.5V Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	300	ns
Chip Select Output Enable Time	(3)TSLQX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Select Output Disable Time	(4)TSHQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	150	ns
Chip Enable Pulse Negative Width	(5)TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	300	-	ns
Chip Enable Pulse Positive Width	(6)TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Address Setup Time	(7)TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Address Hold Time	(8)TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Data Setup Time	(9)TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Data Hold Time	(10)TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Write Data Delay Time	(11)TWLDV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	ns
Chip Select Write Pulse Setup Time	(12)TWLSH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	180	-	ns
Chip Enable Write Pulse Setup Time	(13)TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	180	-	ns
Chip Select Write Pulse Hold Time	(14)TSLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	180	-	ns
Chip Enable Write Pulse Hold Time	(15)TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	180	-	ns
Write Enable Pulse Width	(16)TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	180	-	ns
Read or Write Cycle Time	(17)TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	400	-	ns

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6561/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	8	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	10	pF

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

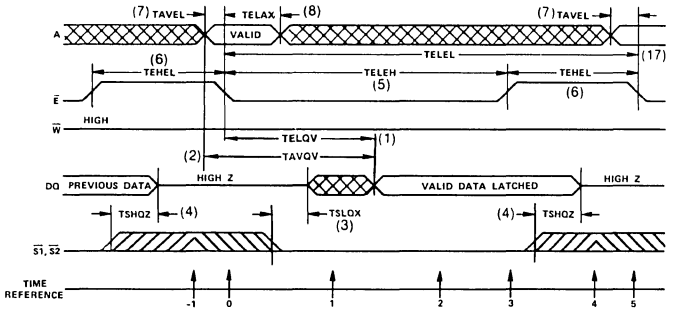
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Timing Waveforms

READ CYCLE



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	S1	W	A	OUTPUT DQ	FUNCTION
-1	H	H	X	X	Z	Memory Disabled
0	↓	X	H	V	Z	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	Output Enabled
2	L	L	H	X	V	Output Valid
3	↑	L	H	X	V	Output Latched
4	H	H	X	X	Z	Device Disabled, Prepare for Next Cycle (Same as -1)
5	↓	X	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

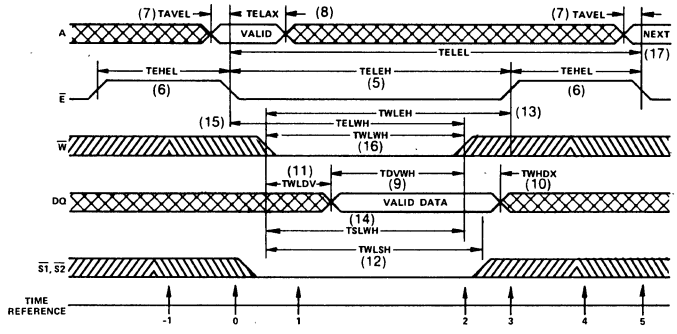
NOTES: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The HM-6561/883 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data $\overline{E}$, $\overline{S1}$ and $\overline{S2}$ must be low and $\overline{W}$ must be high. The output data will be valid at access time (TELQV).

The HM-6561/883 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains latched until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Timing Waveforms (Continued)

WRITE CYCLE



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{W}$	A	DQ	FUNCTION
-1	H	H	X	X	X	Memory Disabled
0	↓	X	X	V	X	Cycle Begins, Addresses are Latched
1	L	L	L	X	X	Write Period Begins
2	L	L	↑	X	V	Data In is Written
3	↑	X	H	X	X	Write is Completed
4	H	H	X	X	X	Prepare for Next Cycle (Same as -1)
5	↓	X	X	V	X	Cycle Ends, Next Cycle Begins (Same as 0)

NOTES: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle begins with the $\overline{E}$ falling edge latching the address. The write portion of the cycle is defined by $\overline{E}$, $\overline{S1}$, $\overline{S2}$ and $\overline{W}$ all being low simultaneously. The write portion of the cycle is terminated by the first rising edge of any control line, $\overline{E}$, $\overline{S1}$, $\overline{S2}$ or $\overline{W}$. The data setup and data hold times (TDVWH and TWHDX) must be referenced to the terminating signal. For example, if $\overline{S2}$ rises first, data setup and hold times become TDVS2H and TS2HDX; and are numerically equal to TDVWH and TWHDX.

Data input/output multiplexing is controlled by $\overline{W}$. Care must be taken to avoid data bus conflicts, where the RAM outputs become enabled when another device is driving the data inputs. The following two examples illustrate the timing required to avoid bus conflicts.

Case 1: Both $\overline{S1}$ and $\overline{S2}$ Fall Before $\overline{W}$ Falls.

If both selects fall before $\overline{W}$ falls, the RAM outputs will become enabled. $\overline{W}$ is used to disable the outputs, so a disable time (TWLQZ = TWLDV) must pass before any other device can begin to drive the data inputs. This method of operation requires a wider write pulse, because TWLDV + TDVWH is greater than TWLWH. In this case TWLSL and TSHWH are meaningless and can be ignored.

Case 2: $\overline{W}$ Falls Before Both $\overline{S1}$ and $\overline{S2}$ Fall.

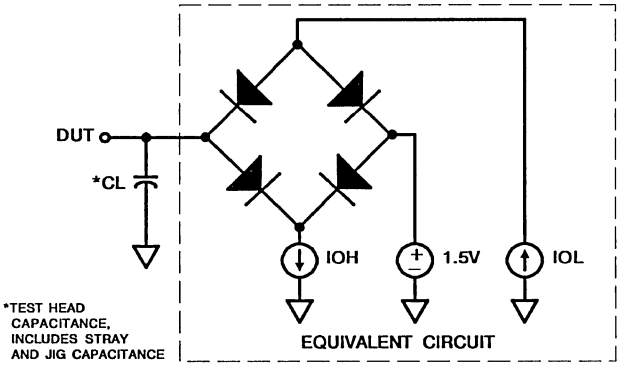
If one or both selects are high until $\overline{W}$ falls, the outputs are guaranteed not to enable at the beginning of the cycle. This eliminates the concern for data bus conflicts and simplifies data input timing. Data input may be applied as early as convenient, and TWLDV is ignored. Since $\overline{W}$ is not used to disable the outputs it can be shorter than in Case 1; TWLWH is the minimum write pulse. At the end of the write period, if $\overline{W}$ rises before either select the outputs will enable, reading the data just written. They will not disable until either select goes high (TSHQZ).

	IF	OBSERVE	IGNORE
CASE 1	Both $\overline{S1}$ and $\overline{S2}$ = Low Before $\overline{W}$ = Low	TWLQZ TWLDV TDVWH	TWLWH
CASE 2	$\overline{W}$ = Low Before Both $\overline{S1}$ and $\overline{S2}$ = Low	TWLWH TDVWH	TWLQZ TWLDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may remain low until all desired locations are written. This is an extension of Case 2.

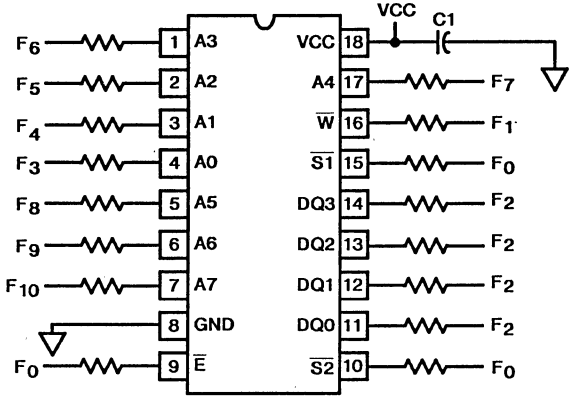
Read-Modify-Write cycles and Read-Write-Read cycles can be performed (extension of Case 1). In fact, data may be modified as many times as desired with $\overline{E}$ remaining low.

Test Load Circuit



Burn-In Circuit

HM1-6561/883 CERAMIC DIP



NOTES:
All Resistors 47kΩ ± 5%
F_0 = 100kHz ± 10%
$F_1 = F_0 + 2$, $F_2 = F_1 + 2$, $F_3 = F_2 + 2 \cdots F_{12} = F_{11} + 2$
VCC = 5.5V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to +0.4V
C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
132 x 160 x 19 ± 1 mils

METALLIZATION:
Type: Si-Al
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

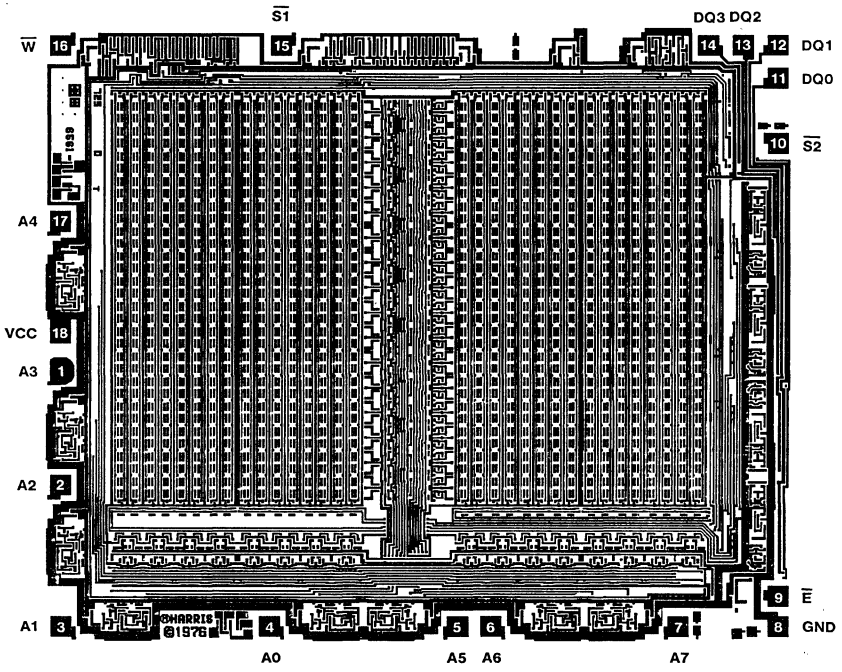
DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$1.337 \times 10^5 A/cm^2$

LEAD TEMPERATURE (10 seconds soldering):
≤300°C

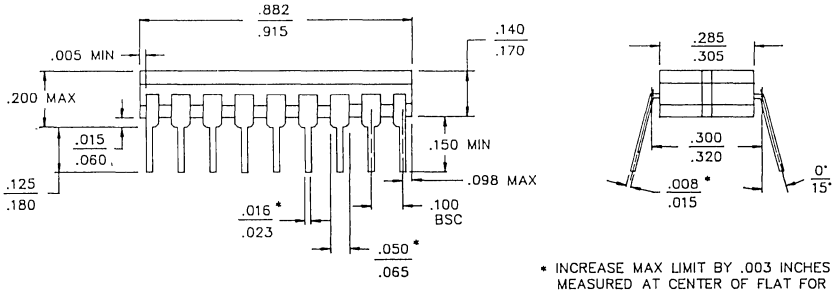
Metallization Mask Layout

HM-6561/883



Packaging†

18 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-6

3
CMOS MEMORY

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HM-6504/883

June 1989

4096 x 1 CMOS RAM

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby ..... 125μW Max.
- Low Power Operation ..... 35mW/MHz Max.
- Data Retention ..... @ 2.0V Min.
- TTL Compatible Input/Output
- Three-State Output
- Standard JEDEC Pinout
- Fast Access Time..... 120/200ns Max.
- 18 Pin Package for High Density
- On-Chip Address Register
- Gated Inputs - No Pull Up or Pull Down Resistors Required

Description

The HM-6504/883 is a 4096 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

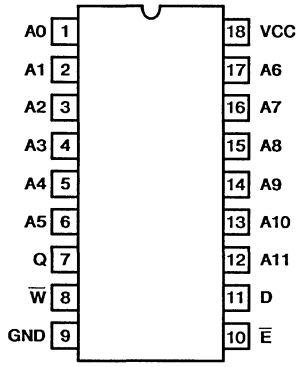
On chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

Gated inputs allow lower operating current and also eliminates the need for pull-up or pull-down resistors. The HM-6504/883 is a fully static RAM and may be maintained in any state for an indefinite period of time.

Data retention supply voltage and supply current are guaranteed over temperature.

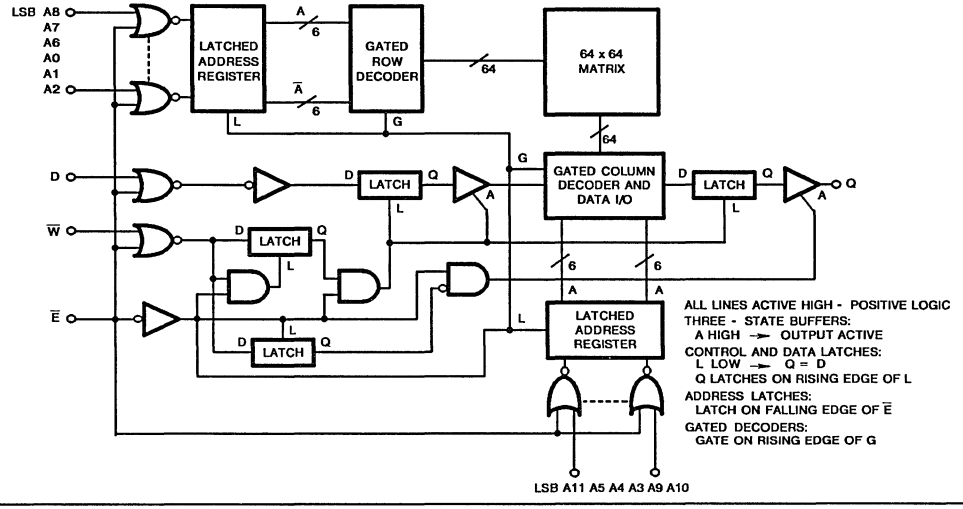
Pinout

HM1-6504/883 (CERAMIC DIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... 300°C
ESD Classification ..... Class 1

Reliability Information

	θ_{ja}	θ_{jc}
Thermal Resistance		
Ceramic DIP Package	66°C/W	12°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.75 Watt
Gate Count ..... 6910 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... -0.3V to +0.8V
Input High Voltage ..... VCC-2.0V to VCC+0.3V

TABLE 1. HM-6504S/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 2mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -1.0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5 V, VO = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	25	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 3) $\overline{E}$ = 1MHz , IO =0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	7	mA
Standby Supply Current	ICCSB	VCC = 5.5V, $\overline{E}$ = VCC-0.3V, IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	50	µA

NOTES:
1. All voltages referenced to VSS.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6504S/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	120	ns
Address Access Time	TAVQV	VCC = 4.5 and 5.5V Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	120	ns
Chip Enable Pulse Negative Width	TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Chip Enable Pulse Positive Width	TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Address Setup Time	TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Address Hold Time	TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Write Enable Pulse Width	TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
Write Enable Pulse Setup Time	TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	70	-	ns
Early Write Pulse Setup Time	TWLEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Early Write Pulse Hold Time	TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Data Setup Time	TDVWL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Early Write Data Setup Time	TDVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Data Hold Time	TWLDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	25	-	ns
Early Write Data Hold Time	TELDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	25	-	ns
Read or Write Cycle Time	TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	170	-	ns

NOTES:
1. All voltages referenced to VSS.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6504S/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	8	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	T_A = +25°C	-	10	pF
Chip Enable Output Enable Time	TELQX	VCC = 4.5V and 5.5V	4	-55°C ≤ T_A ≤ +125°C	5	-	ns
Chip Enable Output Disable Time	TEHQZ	VCC = 4.5V and 5.5V	4	-55°C ≤ T_A ≤ +125°C	-	50	ns
Write Enable Read Mode Setup Time	TWHEL	VCC = 4.5V and 5.5V	4	-55°C ≤ T_A ≤ +125°C	0	-	ns
High Level Output Voltage	VOHL	VCC = 4.5V, IO = -100µA	4	-55°C ≤ T_A ≤ +125°C	VCC -0.4	-	V

NOTES:
1. All voltages referenced to VSS.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	66°C/W	12°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.75 Watt
Gate Count ..... 6910 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... -0.3V to +0.8V
Input High Voltage ..... VCC-2.0V to VCC+0.3V

TABLE 1. HM-6504B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 2mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -1.0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5 V, VO = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC, IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	25	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 3), $\overline{E}$ = 1MHz, IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	7	mA
Standby Supply Current	ICCSB	VCC = 5.5V, $\overline{E}$ = VCC-0.3V, IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	50	µA

NOTES:
1. All voltages referenced to VSS.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6504B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	200	ns
Address Access Time	TAVQV	VCC = 4.5 and 5.5V Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	200	ns
Chip Enable Pulse Negative Width	TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	200	-	ns
Chip Enable Pulse Positive Width	TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	90	-	ns
Address Setup Time	TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
Address Hold Time	TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Write Enable Pulse Width	TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	60	-	ns
Write Enable Pulse Setup Time	TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Early Write Pulse Setup Time	TWLEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Early Write Pulse Hold Time	TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	60	-	ns
Data Setup Time	TDVWL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Early Write Data Setup Time	TDVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Data Hold Time	TWLDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	60	-	ns
Early Write Data Hold Time	TELDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	60	-	ns
Read or Write Cycle Time	TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	290	-	ns

NOTES:
1. All voltages referenced to VSS.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6504B/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	$T_A = +25^oC$	-	8	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	$T_A = +25^oC$	-	10	pF
Chip Enable Output Enable Time	TELQX	VCC = 4.5V and 5.5V	4	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Enable Output Disable Time	TEHQZ	VCC = 4.5V and 5.5V	4	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Write Enable Read Mode Setup Time	TWHEL	VCC = 4.5V and 5.5V	4	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
High Level Output Voltage	VOH2	VCC = 4.5V, IOH = -100µA	4	$-55^oC \leq T_A \leq +125^oC$	VCC -0.4	-	V

NOTES:
1. All voltages referenced to VSS.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	66°C/W	12°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.75 Watt
Gate Count ..... 6910 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... -0.3V to +0.8V
Input High Voltage ..... VCC-2.0V to VCC+0.3V

TABLE 1. HM-6504/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IO = 2mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IO = -1.0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC V, IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	25	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 3), $\overline{E}$ = 1MHz, IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	7	mA
Standby Supply Current	ICCSB	VCC = 5.5V, $\overline{E}$ = VCC-0.3V, IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	50	µA

NOTES:
1. All voltages referenced to VSS.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6504/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	-	300	ns
Address Access Time	TAVQV	VCC = 4.5 and 5.5V Note 5	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	-	320	ns
Chip Enable Pulse Negative Width	TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	300	-	ns
Chip Enable Pulse Positive Width	TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	120	-	ns
Address Setup Time	TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	20	-	ns
Address Hold Time	TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	50	-	ns
Write Enable Pulse Width	TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	80	-	ns
Write Enable Pulse Setup Time	TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	200	-	ns
Early Write Pulse Setup Time	TWLEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	0	-	ns
Early Write Pulse Hold Time	TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	80	-	ns
Data Setup Time	TDVWL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	0	-	ns
Early Write Data Setup Time	TDVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	0	-	ns
Data Hold Time	TWLDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	80	-	ns
Early Write Data Hold Time	TELDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	80	-	ns
Read or Write Cycle Time	TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	420	-	ns

NOTES:
1. All voltages referenced to VSS.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6504/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	$-55^oC \leq T_A \leq +125^oC$	-	8	pF
Output Capacitance	CO	VCC = 4.5V, f = 1MHz, All Measurements Referenced to Device Ground	4	$-55^oC \leq T_A \leq +125^oC$	-	10	pF
Chip Enable Output Enable Time	TELQX	VCC = 4.5V and 5.5V	4	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Enable Output Disable Time	TEHQZ	VCC = 4.5V and 5.5V	4	$-55^oC \leq T_A \leq +125^oC$	-	100	ns
Write Enable Read Mode Setup Time	TWHEL	VCC = 4.5V and 5.5V	4	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
High Level Output Voltage	VOH2	VCC = 4.5, IOH = -100µA	4	$-55^oC \leq T_A \leq +125^oC$	VCC -0.4	-	V

NOTES:
1. All voltages referenced to VSS.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL

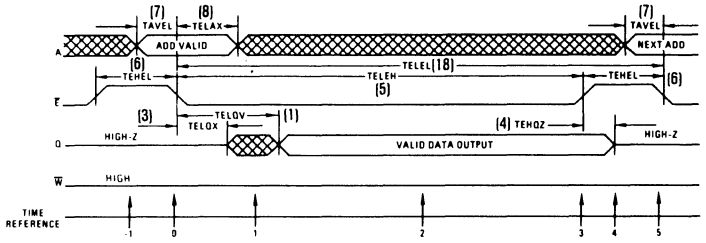
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Timing Waveforms

READ CYCLE

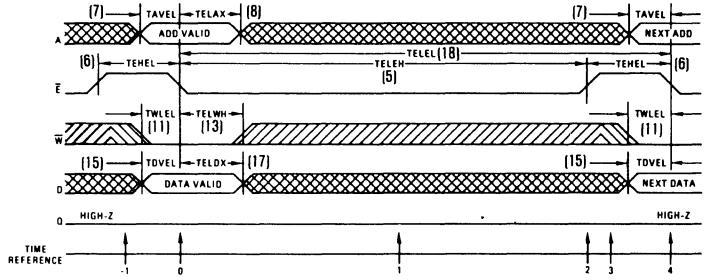


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↓	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↑	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as - 1)
5	↓	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all inputs and ready the RAM for the next memory cycle (T = 4).

EARLY WRITE CYCLE



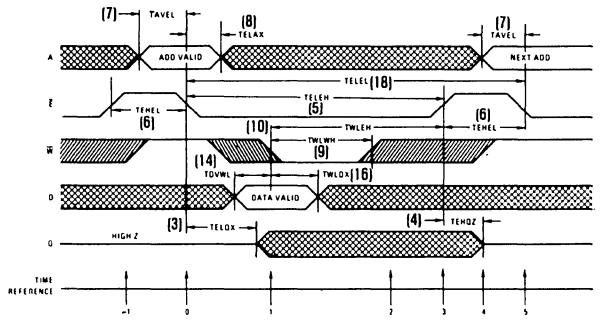
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	L	V	V	Z	Cycle Begins, Addresses are Latched
1	L	X	X	X	Z	Write in Progress Internally
2	↑	X	X	X	Z	Write Completed
3	H	X	X	X	Z	Prepare for Next Cycle (Same as - 1)
4	↓	L	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer and all inputs are disabled and all signals are unlatched. The device is now ready for the next cycle.

Timing Waveforms (Continued)

LATE WRITE CYCLE



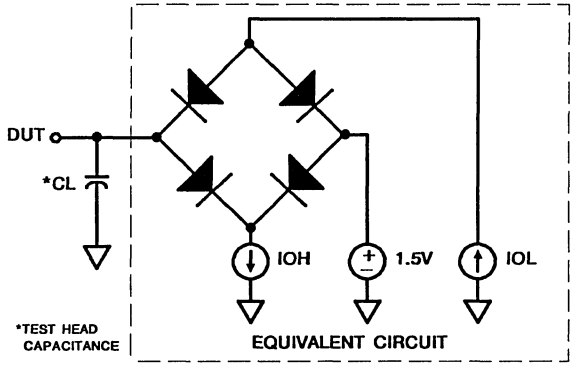
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↘	H	V	X	Z	Cycle Begins Addresses are Latched
1	L	↘	X	V	X	Write Begins, Data is Latched
2	L	H	X	X	X	Write in Progress Internally
3	↗	H	X	X	X	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

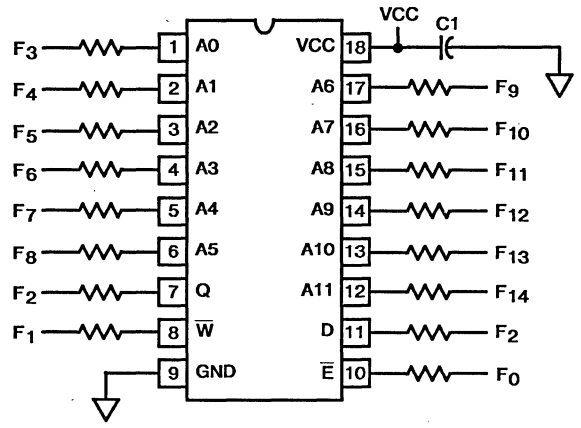
Recall that in the early write the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data setup, data hold, write setup and write pulse widths are observed.

Test Load Circuit



Burn-In Circuit

HM-6504/883 CERAMIC DIP



NOTES:

All Resistors 47k ± 5%

F_0 = 100kHz ± 10%

$F_1 = F_0 \div 2$, $F_2 = F_1 \div 2$, $F_3 = F_2 \div 2 \cdots F_{12} = F_{11} \div 2$

VCC = 5.5V ± 0.5V

VIH = 4.5V ± 10%

VIL = -0.2V to +0.4V

C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
136 x 169 x 19 ± 1 mils

METALLIZATION:
Type: Si-Al
Thickness: 11kÅ ± 2kÅ

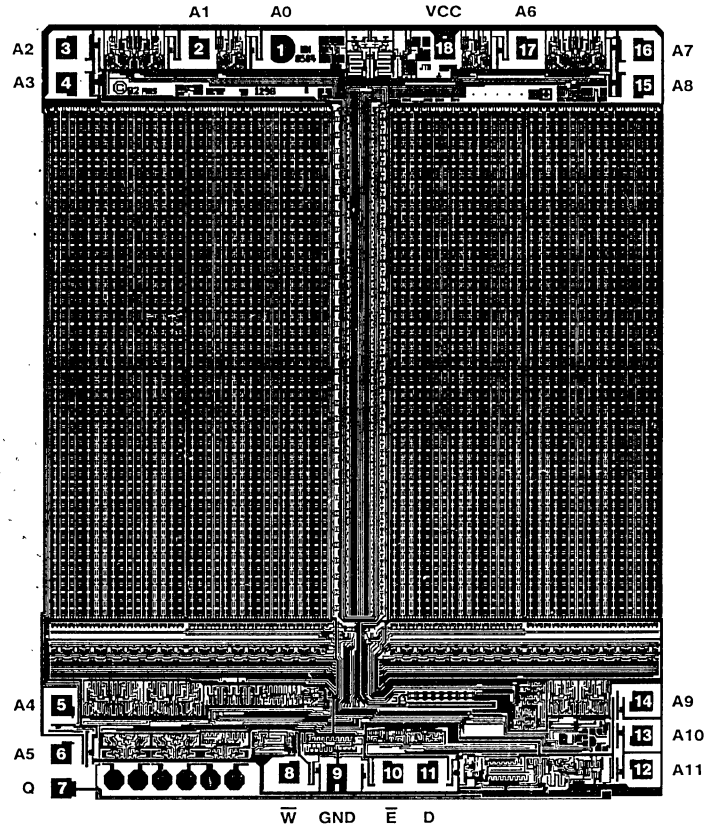
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
1.79 x 10^5A/cm^2

Metallization Mask Layout

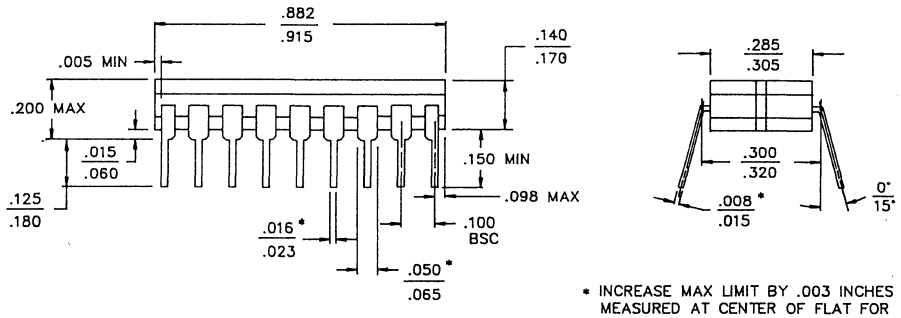
HM-6504/883



NOTE: Pin Numbers Correspond to DIP Package Only.

Packaging†

18 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-6

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HM-6514/883

June 1989

1024 x 4 CMOS RAM

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby ..... 125µW Max.
- Low Power Operation ..... 35mW/MHz Max.
- Data Retention ..... @ 2.0V Min.
- TTL Compatible Input/Output
- Common Data Input/Output
- Three-State Output
- Standard JEDEC Pinout
- Fast Access Time..... 120/200ns Max.
- 18 Pin Package for High Density
- On-Chip Address Register
- Gated Inputs - No Pull Up or Pull Down Resistors Required

Description

The HM-6514/883 is a 1024 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

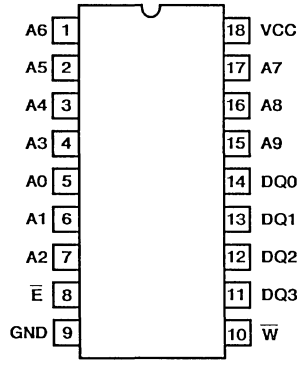
On chip latches are provided for addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

Gated inputs allow lower operating current and also eliminates the need for pull-up or pull-down resistors. The HM-6514/883 is a fully static RAM and may be maintained in any state for an indefinite period of time.

Data retention supply voltage and supply current are guaranteed over temperature.

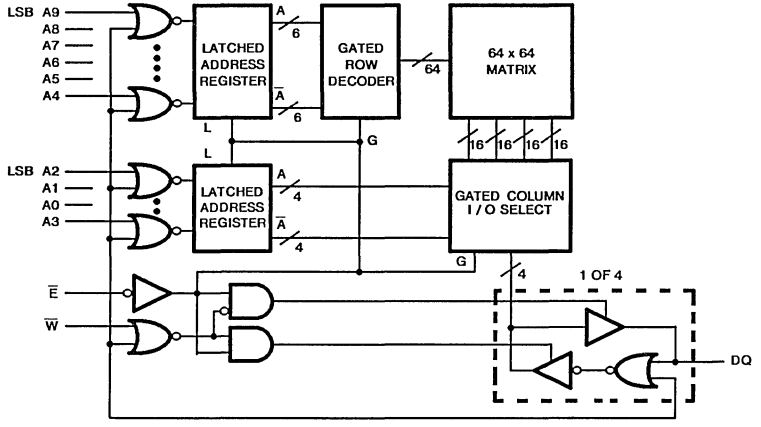
Pinout

HM1-6514/883 (CERAMIC DIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec)..... 300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	66°C/W	12°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.75 Watt
Gate Count ..... 6910 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage..... 0V to +0.8V
Input High Voltage ..... VCC-2.0V to VCC
Input Rise and Fall Time ..... 40ns max

TABLE 1. HM-6514S/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 3.2mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -1.0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Input/Output Leakage Current	IIOZ	VCC = 5.5 V, VIO= GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC-0.3V IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	25	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 3) $\overline{E}$ = 1MHz	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	7	mA
Standby Supply Current	ICCSB	VCC = 5.5V, $\overline{E}$ = VCC-0.3V, IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	50	µA

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6514S/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	120	ns
Address Access Time	TAVQV	VCC = 4.5 and 5.5V Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	120	ns
Chip Enable Pulse Negative Width	TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Chip Enable Pulse Positive Width	TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Address Setup Time	TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Address Hold Time	TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Write Enable Pulse Width	TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Write Enable Pulse Setup Time	TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Write Enable Pulse Hold Time	TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Data Setup Time	TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Data Hold Time	TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Write Data Delay Time	TWLDV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	70	-	ns
Early Output High-Z Time	TWLEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Late Output High-Z Time	TEHWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Read or Write Cycle Time	TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	170	-	ns

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6514S/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	$T_A = +25^oC$	-	8	pF
Input/Output Capacitance	CIO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	$T_A = +25^oC$	-	10	pF
Chip Enable Output Enable Time	TELQX	VCC = 4.5V and 5.5V	4	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Enable Output Disable Time	TEHQZ	VCC = 4.5V and 5.5V	4	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
High Level Output Voltage	VOH2	VCC = 4.5V, IO = -100μA	4	$-55^oC \leq T_A \leq +125^oC$	VCC -0.4	-	V

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec)..... +300°C

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	66°C/W	12°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.75 Watt
Gate Count ..... 6910 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage..... 0V to +0.8V
Input High Voltage ..... VCC-2.0V to VCC

TABLE 1. HM-6514B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 3.2mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -1.0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Input/Output Leakage Current	IIOZ	VCC = 5.5 V, VIO = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC, IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	25	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 3) f = 1 MHz	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	7	mA
Standby Supply Current	ICCSB	VCC = 5.5V, $\overline{E}$ = VCC-0.3V, IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	50	µA

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6514B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	200	ns
Address Access Time	TAVQV	VCC = 4.5 and 5.5V Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	220	ns
Chip Enable Pulse Negative Width	TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	200	-	ns
Chip Enable Pulse Positive Width	TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	90	-	ns
Address Setup Time	TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
Address Hold Time	TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Write Enable Pulse Width	TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	200	-	ns
Write Enable Pulse Setup Time	TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	200	-	ns
Write Enable Pulse Hold Time	TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	200	-	ns
Data Setup Time	TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Data Hold Time	TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Write Data Delay Time	TWLDV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	80	-	ns
Early Output High-Z Time	TWLEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Late Output High-Z Time	TEHWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Read or Write Cycle Time	TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	290	-	ns

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6514B/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	$T_A = +25^oC$	-	8	pF
Input/Output Capacitance	CIO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	$T_A = +25^oC$	-	10	pF
Chip Enable Output Enable Time	TELQX	VCC = 4.5V and 5.5V	4	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Enable Output Disable Time	TEHQZ	VCC = 4.5V and 5.5V	4	$-55^oC \leq T_A \leq +125^oC$	-	80	ns
High Level Output Voltage	VOHZ	VCC = 4.5V, IO = -100µA	4	$-55^oC \leq T_A \leq +125^oC$	VCC -0.4	-	V

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied .... GND-0.3V to VCC+0.03V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	66°C/W	12°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ..... 0.75 Watt
Gate Count ..... 6910 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VCC-2.0V to VCC

TABLE 1. HM-6514/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IO = 3.2mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IO = -1.0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Input/Output Leakage Current	IIOZ	VCC = 5.5V, VIO = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC-0.3V, IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	25	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 2), f = 1MHz	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	7	mA
Standby Supply Current	ICCSB	VCC = 5.5V, $\overline{E}$ = VCC-0.3V, IO = 0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	50	µA

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6514/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	300	ns
Address Access Time	TAVQV	VCC = 4.5 and 5.5V Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	320	ns
Chip Enable Pulse Negative Width	TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	300	-	ns
Chip Enable Pulse Positive Width	TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Address Setup Time	TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
Address Hold Time	TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Write Enable Pulse Width	TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	300	-	ns
Write Enable Pulse Setup Time	TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	300	-	ns
Write Enable Pulse Hold Time	TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	300	-	ns
Data Setup Time	TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	200	-	ns
Data Hold Time	TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Write Data Delay Time	TWLDV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Early Output High-Z Time	TWLEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Late Output High-Z Time	TEHWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Read or Write Cycle Time	TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	420	-	ns

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
5. TAVQV = TELQV + TAVEL

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6514/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	4	$T_A = +25^oC$	-	8	pF
Input/Output Capacitance	CIO	VCC = 4.5V, f = 1MHz, All Measurements Referenced to Device Ground	4	$T_A = +25^oC$	-	10	pF
Chip Enable Output Enable Time	TELQX	VCC = 4.5V and 5.5V	4	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Enable Output Disable Time	TEHQZ	VCC = 4.5V and 5.5V	4	$-55^oC \leq T_A \leq +125^oC$	-	100	ns
High Level Output Voltage	VOHZ	VCC = 4.5, IO = -100µA	4	$-55^oC \leq T_A \leq +125^oC$	VCC -0.4	-	V

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. Typical derating 5mA/MHz increase in ICCOP.
4. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

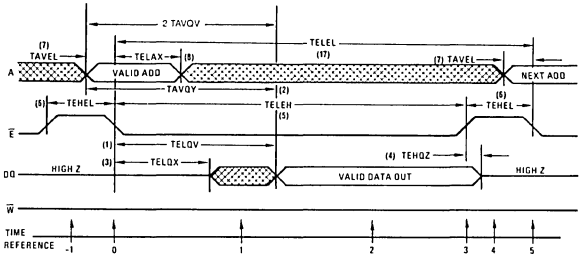
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Timing Waveforms

READ CYCLE



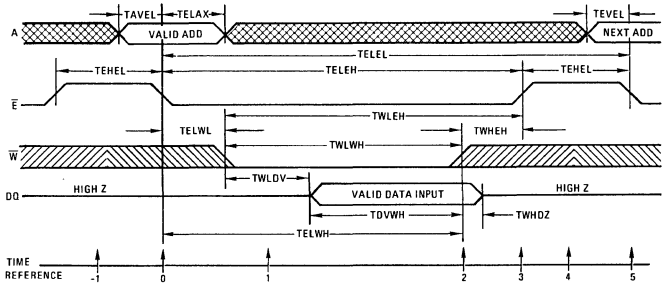
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↓	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↑	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as - 1)
5	↓	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all inputs and ready the RAM for the next memory cycle (T = 4).

Timing Waveforms (Continued)

WRITE CYCLE



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DQ	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↓	X	V	Z	Cycle Begins, Addresses are Latched
1	L	L	X	Z	Write Period Begins
2	L	↑	X	V	Data In is Written
3	↑	H	X	Z	Write Completed
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on-chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before $\overline{E}$. The RAM outputs and all inputs will three-state after $\overline{E}$ rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

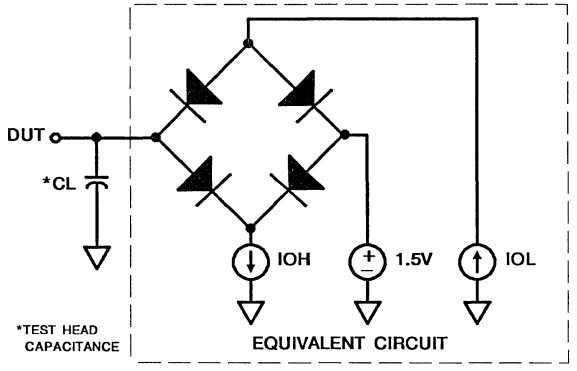
Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rising

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met, but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDX become TDVEH and TEHDX. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ and $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDX

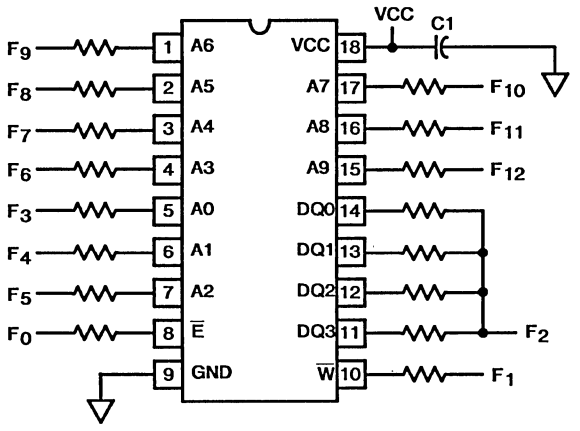
If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

Test Load Circuit



Burn-In Circuit

HM-6514/883 CERAMIC DIP



NOTES:

All Resistors 47kΩ ± 5%

F_0 = 100kHz ± 10%

$F_1 = F_0 \div 2$, $F_2 = F_1 \div 2$, $F_3 = F_2 \div 2 \cdots F_{12} = F_{11} \div 2$

VCC = 5.5V ± 0.5V

VIH = 4.5V ± 10%

VIL = -0.2V to +0.4V

C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
136 x 167 x 19 ± 1 mils

METALLIZATION:
Type: Si-Al
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

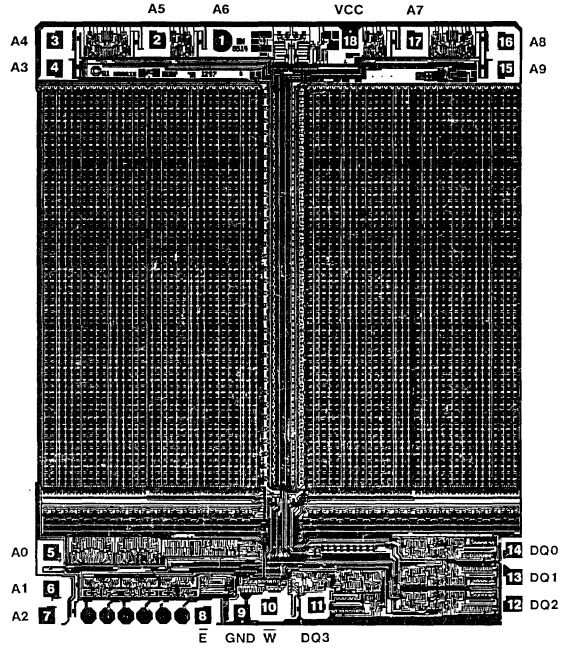
DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$1.79 \times 10^5 A/cm^2$

LEAD TEMPERATURE (10 seconds soldering):
300°C

Metallization Mask Layout

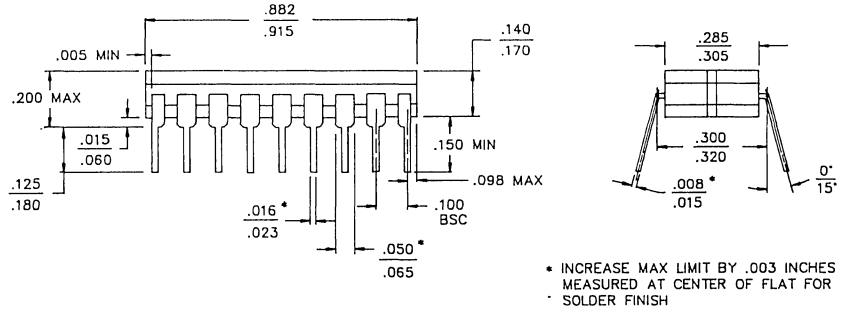
HM-6514/883



NOTE: Pin Numbers Correspond to DIP Package Only.

Packaging†

18 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-6

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HM-6516/883

June 1989

2K x 8 CMOS RAM

Features

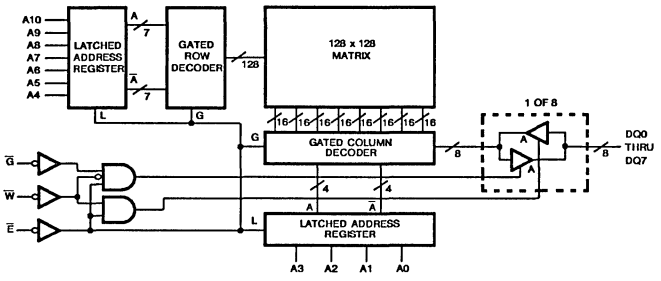
- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby ..... 275µW Max.
- Low Power Operation ..... 55mW/MHz Max.
- Fast Access ..... 120/200ns Max.
- Industry Standard Pinout
- Single Supply ..... 5.0 Volt VCC
- TTL Compatible
- Static Memory Cells
- High Output Drive
- On-Chip Address Latches
- Easy Microprocessor Interfacing

Description

The HM-6516/883 is a CMOS 2048 x 8 Static Random Access Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, which also gives fast access times. The pinout of the HM-6516/883 is the popular 24 pin, 8-bit wide JEDEC standard which allows easy memory board layouts, flexible enough to accomodate a variety of PROMs, RAMS, EPROMs, and ROMs.

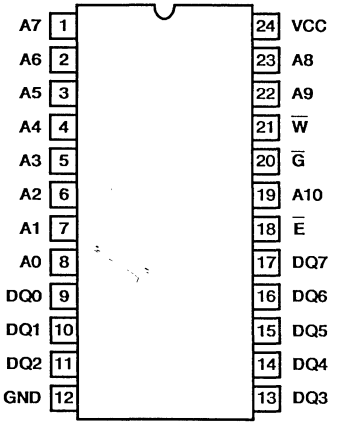
The HM-6516/883 is ideally suited for use in microprocessor based systems. The byte wide organization simplifies the memory array design, and keeps operating power down to a minimum because only one device is enabled at a time. The address latches allow very simple interfacing to recent generation microprocessors which employ a multiplexed address/data bus. The convenient output enable control also simplifies multiplexed bus interfacing by allowing the data outputs to be controlled independent of the chip enable.

Functional Diagram

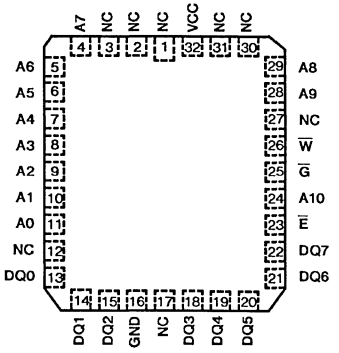


Pinouts

HM1-6516/883 (CERAMIC DIP)
TOP VIEW



HM4-6516/883 (CERAMIC LCC)
TOP VIEW



PIN	DESCRIPTION
NC	No Connect
$A_0 - A_{10}$	Address Inputs
$\overline{E}$	Chip Enable/Power Down
V_{SS}/GND	Ground
$DQ_0 - DQ_7$	Data In/Data Out
VCC	Power (+5V)
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	48°C/W	8°C/W
Ceramic LCC Package	66°C/W	12°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1W
Ceramic LCC Package 0.75W
Gate Count ..... 25953 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... 4.5V to 5.5V
Input Low Voltage ..... 0 to +0.8V
Input High Voltage ..... +2.4V to VCC
Data Retention Supply Voltage ..... 2.0V to 4.5V
Input Rise and Fall Time ..... 40ns Max

TABLE 1. HM-6516/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. VCC = 5.0V ± 10% Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH	VCC = 4.5V, IO = -1.0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 3.2mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = $\overline{G}$ = 5.5V, VIO = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	1.0	µA
Operating Supply Current	ICCOP	VCC = $\overline{G}$ = 5.5V, (Note 2), f = 1MHz, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	mA
Standby Supply Current	ICCSB1	VCC = 5.5V, HM-6516/883 $\overline{E}$ = VCC -0.3V, IO = 0mA VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	100	µA
		VCC = 5.5V, HM-6516B/883 $\overline{E}$ = VCC -0.3V, IO = 0mA VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	50	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, HM-6516/883 $\overline{E}$ = VCC -0.3V, IO = 0mA VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	50	µA
		VCC = 2.0V, HM-6516B/883 $\overline{E}$ = VCC -0.3V, IO = 0mA VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	25	µA
Functional Test	FT	VCC = 4.5V (Note 4)	7, 8A, 8B	$-55°C \leq T_A \leq +125°C$	-	-	

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-6516/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Guaranteed and 100% Tested. VCC = 5.0V ± 10% Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	(NOTES 1, 5) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/ Cycle Time	TELEL	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	280	-	ns
		VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	170	-	ns
Address Access Time	TAVQV (Note 6)	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	200	ns
		VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	120	ns
Chip Enable Access Time	TELQV	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	200	ns
		VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	120	ns
Chip Selection to End of Write	TELWH	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	200	-	ns
		VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Write Enable Pulse Width	TWLWH	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	200	-	ns
		VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Data Set-Up Time	TDVWH	VCC = 4.5V and 5.5V HM-6516/883 VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	80 50	-	ns
Data Hold Time	TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Write Enable Pulse Set-up Time	TWLEH	VCC = 4.5V and 5.5V HM-6516/883 VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	200 120	-	ns
Address Set-Up Time	TAVEL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Address Hold Time	TELAX	VCC = 4.5V and 5.5V HM-6516/883 VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50 30	-	ns
Chip Enable Pulse Positive Width	TEHEL	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	80	-	ns
		VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Chip Enable Pulse Negative Width	TELEH	VCC = 4.5V and 5.5V HM-6516/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	200	-	ns
		VCC = 4.5V and 5.5V HM-6516B/883	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns

NOTES:
1. All voltages referenced to Device Ground.
2. Typical derating = 5mA/MHz increase in ICCOP.
3. Shall be tested initially, and after any design changes.
4. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
5. AC measurements assume transistion time $\leq$ 5ns; input levels = 0V to 3V; timing reference levels = 1.5V; output load = CL $\geq$ 50pF and 1 TTL equivalent load; and for CL > 50pF, CL < 300pF, access time are derated by 0.15ns/pF.
6. TAVQV = TELQV + TAVEL.

TABLE 3. HM-6516/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open $T_A = +25^oC$, f = 1MHz, All Measurements Referenced to Device GND	1, 2	$T_A = +25^oC$	-	8	pF
		VCC = Open $T_A = +25^oC$, f = 1MHz, All Measurements Referenced to Device GND	1, 3	$T_A = +25^oC$	-	12	pF
Input/Output Capacitance	CI/O	VCC = Open $T_A = +25^oC$, f = 1MHz, All Measurements Referenced to Device GND	1, 2	$T_A = +25^oC$	-	10	pF
		VCC = Open $T_A = +25^oC$, f = 1MHz All Measurements Referenced to Device GND	1, 3	$T_A = +25^oC$	-	14	pF
Output Enable To Output Valid Time	TGLQX	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Chip Enable To Output Valid Time	TELQX	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Chip Enable Output Disable Time	TEHQZ	VCC = 4.5V and 5.5V HM-6516/883	1	$-55^oC \leq T_A \leq +125^oC$	-	80	ns
		VCC = 4.5V and 5.5V HM-6516B/883	1	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Output Disable Time	TGHQZ	VCC = 4.5V and 5.5V HM-6516/883	1	$-55^oC \leq T_A \leq +125^oC$	-	80	ns
		VCC = 4.5V and 5.5V HM-6516B/883	1	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Write Enable Output Disable Time	TWLQZ	VCC = 4.5V and 5.5V HM-6516/883	1	$-55^oC \leq T_A \leq +125^oC$	-	80	ns
		VCC = 4.5V and 5.5V HM-6516B/883	1	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	80	ns

NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

2. Applies to LCC device types only.

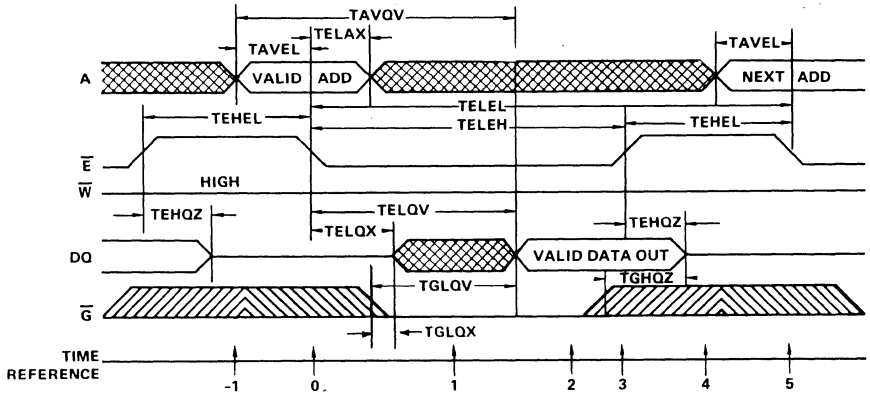
3. Applies to DIP device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Intial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

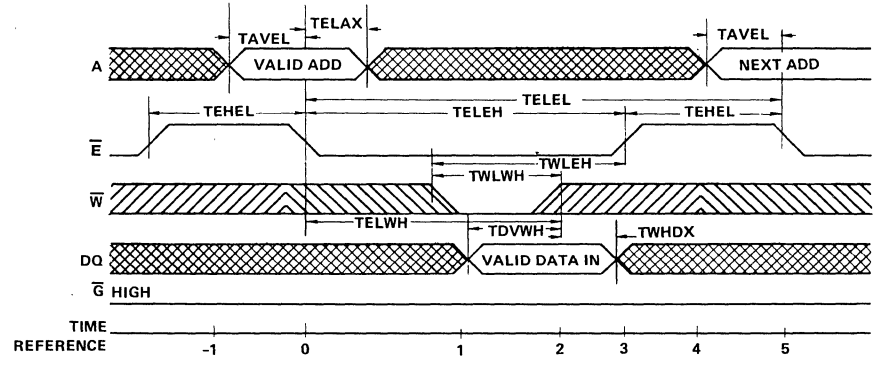
Timing Waveforms

READ CYCLE HM-6516/883 and HM-6516B/883



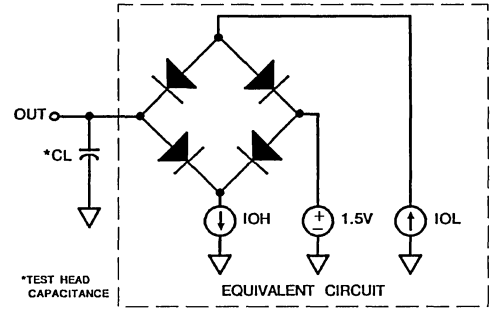
The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2), $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After (T = 4) time, the memory is ready for the next cycle.

WRITE CYCLE HM-6516/883 and HM-6516B/883



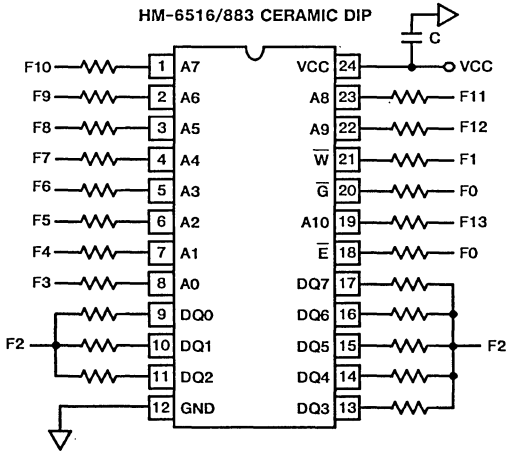
The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$ (T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising of $\overline{E}$.

Test Load Circuit

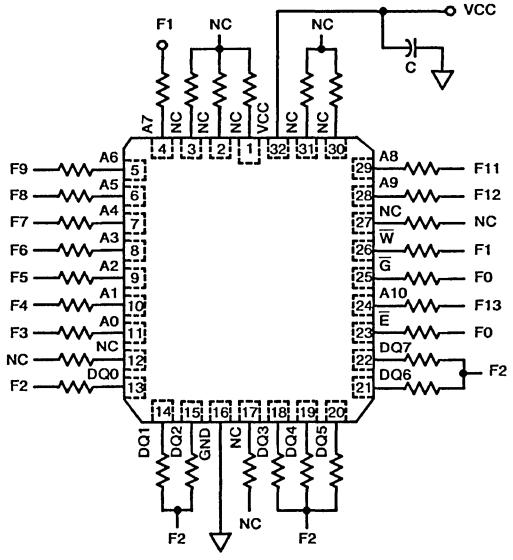


Burn-In Circuits

HM-6516/883 CERAMIC DIP



HM-6516/883 CERAMIC LCC



NOTES:
All resistors 47kΩ 5%
F0 = 100kHz ± 10%
VCC = 5.5V ± .5V
VIH = 4.5V ± 10%
VIL = -0.2V - +0.4V
C = 0.01µF min

Metallization Topology

DIE DIMENSIONS:
186.6 x 199.6 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 9kÅ - 13kÅ

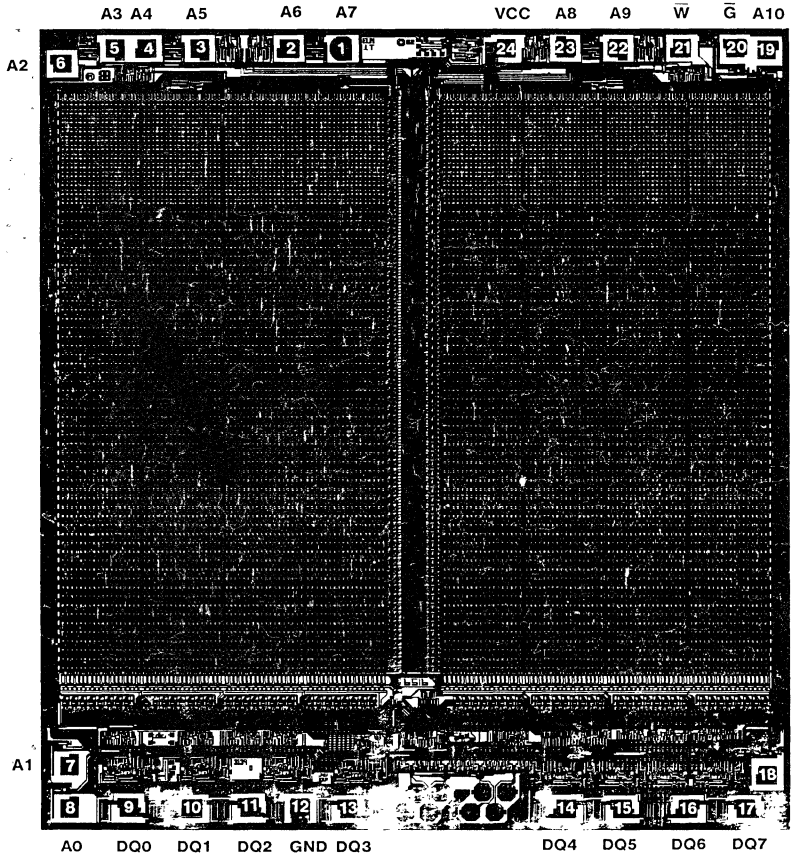
GLASSIVATION:
Type: SiO_2
Thickness: 7kÅ - 9kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
0.5 x 10^5 A/cm^2

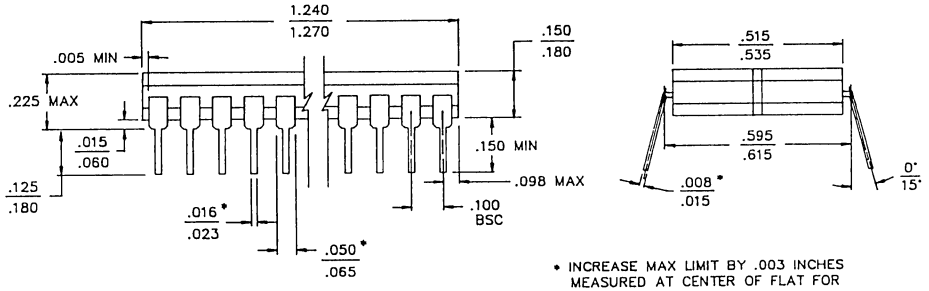
Metallization Mask Layout

HM-6516/883



Packaging†

24 PIN CERAMIC DIP

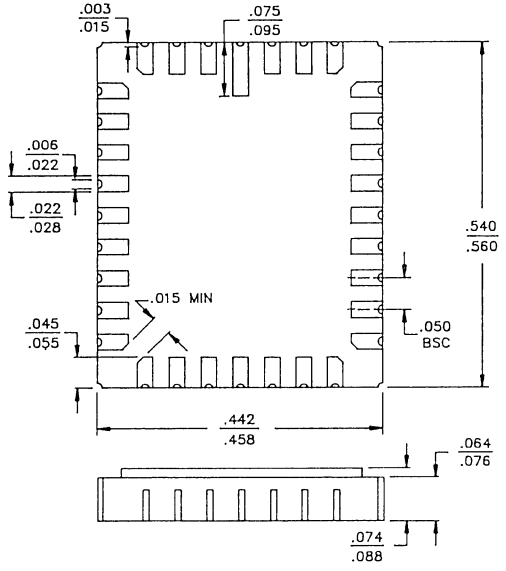


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-3

32 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80%/20%)
Temperature: 320°C ± 10°C
Method: Furnace Braze

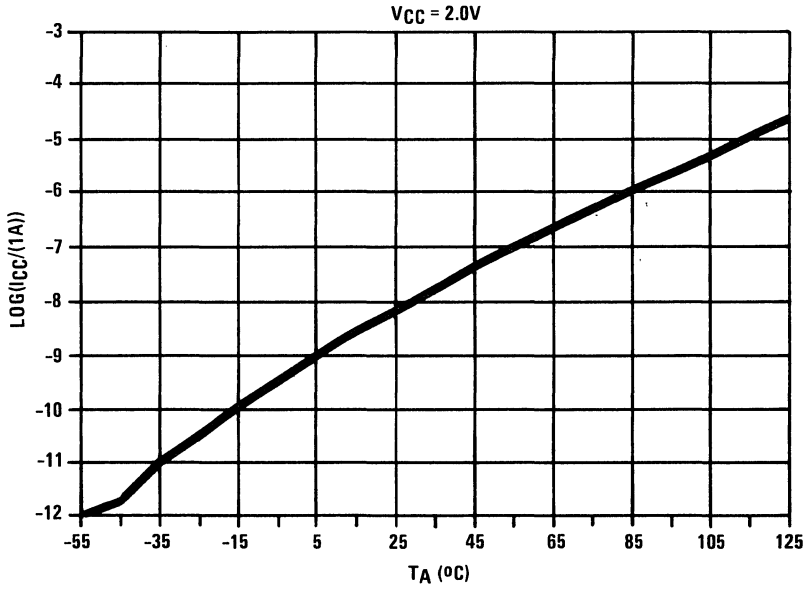
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-12

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL ICCDR vs T_A



HARRIS

HM-65162/883

2K x 8 Asynchronous CMOS Static RAM

June 1989

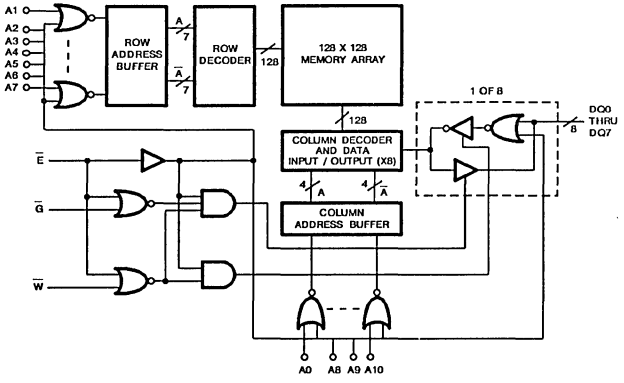
Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Fast Access Time..... 70/90ns Max
- Low Standby Current..... 50µA Max
- Low Operating Current .....70mA Max
- Data Retention at 2.0 Volts..... 20µA Max
- TTL Compatible Inputs and Outputs
- JEDEC Approved Pinout (2716, 6116 Type)
- No Clocks or Strobes Required
- Wide Temperature Range.....-55°C to +125°C
- Equal Cycle and Access Time
- Single 5 Volt Supply
- Gated Inputs—No Pull-Up or Pull-Down Resistors Required

Description

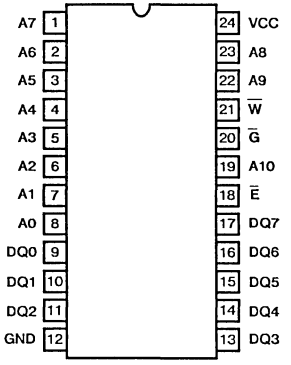
The HM-65162/883 is a CMOS 2048 x 8 Static Random Access Memory manufactured using the Harris Advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle time and ease of use. The pinout is the JEDEC 24 pin DIP, and 32 pad 8-bit wide standard which allows easy memory board layouts flexible to accommodate a variety of industry standard PROMs, RAMs, ROMs and EPROMs. The HM-65162/883 is ideally suited for use in microprocessor based systems with its 8-bit word length organization. The convenient output enable also simplifies the bus interface by allowing the data outputs to be controlled independent of the chip enable. Gated inputs lower operating current and also eliminate the need for pull-up or pull-down resistors.

Functional Diagram

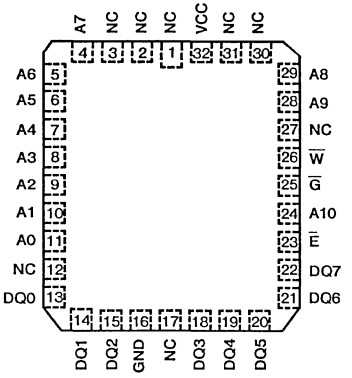


Pinouts

HM1-65162/883 (CERAMIC DIP)
TOP VIEW



HM4-65162/883 (CERAMIC LCC)
TOP VIEW



PIN NAMES

PIN	DESCRIPTION
NC	No Connect
A0 - A10	Address Input
$\overline{E}$	Chip Enable/Power Down
VSS/GND	Ground
DQ0 - DQ7	Data In/Data Out
VCC	Power (+5V)
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable

3 CMOS MEMORY

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	48°C/W	8°C/W
Ceramic LCC Package	85°C/W	40°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 0.58W
Gate Count ..... 26000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (VCC) ..... 4.5V to 5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0V to +0.8V
Input High Voltage (VIH) ..... +2.2V to VCC
Data Retention Supply Voltage ..... 2.0V to 4.5V
Input Rise and Fall Times ..... 40ns Max

TABLE 1. HM-65162/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VCC = 4.5V, IO = -1.0mA	1, 2, 3	-55°C≤T_A≤+125°C	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 4.0mA	1, 2, 3	-55°C≤T_A≤+125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 2.2V, or $\overline{E}$ = 2.2V VI/O = GND or VCC	1, 2, 3	-55°C≤T_A≤+125°C	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	-55°C≤T_A≤+125°C	-1.0	1.0	µA
Standby Supply Current	ICCSB1	VCC = 5.5V, IO = mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	-55°C≤T_A≤+125°C	-	100	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 2.2V	1, 2, 3	-55°C≤T_A≤+125°C	-	8	mA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = 5.5V, (Note 4), f = 1MHz, $\overline{E}$ = 0.8V	1, 2, 3	-55°C≤T_A≤+125°C	-	70	mA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V	1, 2, 3	-55°C≤T_A≤+125°C	-	70	mA
Data Retention Supply Current	ICCDR	VCC = 2.0V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	-55°C≤T_A≤+125°C	-	40	µA
Functional Test	FT	VCC = 4.5V (Note 5)	7, 8A, 8B	-55°C≤T_A≤+125°C	-	-	-

TABLE 2. HM-65162/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	90	-	ns
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	-	90	ns
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C		65	ns
Chip Enable Access Time	TELQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	-	90	ns
Write Enable Read Setup Time	TWHAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	10	-	ns
Address Setup Time	TAVWL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	10	-	ns
Chip Selection to End of Write	TELWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	55	-	ns
Write Enable Pulse Setup Time	TWLEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	55	-	ns
Chip Enable Data Setup Time	TDVEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	30	-	ns
Address Valid to End of Write	TAVWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	65	-	ns
Write Enable Pulse Write	TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	55	-	ns
Data Setup Time	TDVWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	30	-	ns
Data Hold Time	TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	15	-	ns

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-65162/883 ELECTRICAL PERFORMANCE CHARACTERISTICS, A.C. AND D.C. (NOTE 6)

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, F = 1MHz, All Measurements Referenced To Device Grounds	6, 8	+25°C	-	10	pF
		VCC = Open, F = 1MHz, All Measurements Referenced To Device Grounds	6, 9	+25°C	-	8	pF
I/O Capacitance	CI/O	VCC = Open, F = 1MHz, All Measurements Referenced To Device Grounds	6, 8	+25°C	-	12	pF
		VCC = Open, F = 1MHz, All Measurements Referenced To Device Grounds	6, 9	+25°C	-	10	pF
Write Enable to Output in High Z	TWLQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	50	ns
Write Enable High to Output ON	TWHQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	0	-	ns
Chip Enable to Output ON	TELQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	0	-	ns
Output Enable to Output ON	TGLQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Chip Enable High to Output ON	TEHQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	50	ns
Output Disable to Output in High Z	TGHQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	40	ns
Output Hold from Address Change	TAVQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Output High Voltage	VOH2	VCC = 4.5V, IO = -100μA	6	$-55^{o}C \leq T_A \leq +125^{o}C$	VCC -0.4V	-	V

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL $\geq$ 50pF; for CL > 50pF < 300pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.
4. Typical derating = 5mA/MHz increase in ICCOP.
5. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
6. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
7. This is a "typical" value and not a "maximum" value.
8. Applies to DIP device types only.
9. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... GND -0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	48°C/W	8°C/W
Ceramic LCC Package	85°C/W	40°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 0.58W
Gate Count ..... 26000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range (T_A) ..... -55°C to +125°C
Operating Supply Voltage (VCC) ..... 4.5V to 5.5V
Input Low Voltage (VIL) ..... 0V to +0.8V
Input High Voltage (VIH) ..... +2.2V to VCC
Data Retention Supply Voltage ..... 2.0V to 4.5V
Input Rise and Fall Times ..... 40ns (Max)

TABLE 1. HM65162B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VCC = 4.5V, IO = -1.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 4.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 2.2V, or $\overline{E}$ = 2.2V VI/O = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	1.0	µA
Standby Supply Current	ICCSB1	VCC = 5.5V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	50	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 2.2V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	8	mA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = 5.5V, (Note 4), f = 1MHz, $\overline{E}$ = 0.8V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	70	mA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V	1, 2, 3,	$-55°C \le T_A \le +125°C$	-	70	mA
Data Retention Supply Current	ICCDR	VCC = 2.0V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	20	µA
Functional Test	FT	VCC = 4.5V (Note 5)	7, 8A, 8B	$-55°C \le T_A \le +125°C$	-	-	-

TABLE 2. HM-65162B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	70	-	ns
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	70	ns
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	50	ns
Chip Enable Access Time	TELQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	70	ns
Write Enable Read Setup Time	TWHAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns
Address Setup Time	TAVWL	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns
Chip Selection to End of Write	TELWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	45	-	ns
Write Enable Pulse Setup Time	TWLEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	40	-	ns
Chip Enable Data Setup Time	TDVEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	30	-	ns
Address Valid to End of Write	TAVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	50	-	ns
Write Enable Pulse Write	TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	40	-	ns
Data Setup Time	TDVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	30	-	ns
Data Hold Time	TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. HM-65162B/883 ELECTRICAL PERFORMANCE CHARACTERISTICS, A.C. AND D.C. (NOTE 6)

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, f = 1MHz All Measurements Referenced to Device Ground	6, 8	+25°C	-	10	pF
		VCC = Open, f = 1MHz, All Measurements Refernced to Device Ground	6, 9	+25°C	-	8	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	6, 8	+25°C	-	12	pF
		VCC = Open, f = 1MHz All Measurements Referenced to Device Ground	6, 9	+25°C	-	10	pF
Write Enable to Output in High Z	TWLQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	40	ns
Write Enable High to Output ON	TWHQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	0	-	ns
Chip Enable to Output ON	TELQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Output Enable to Output ON	TGLQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Chip Enable High to Output ON	TEHQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	35	ns
Output Disable to Output in High Z	TGHQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	35	ns
Output Hold from Address Change	TAVQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Output High Voltage	VOH2	VCC = 4.5V, IO = -100µA	6	$-55^{o}C \leq T_A \leq +125^{o}C$	VCC -0.4V	-	V

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL $\geq$ 50pF; for CL > 50pF < 300pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.
4. Typical derating = 5mA/MHz increase in ICCOP.
5. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$1.5V, and VOL $\leq$ 1.5V.
6. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
7. This is a "typical" value and not a "maximum" value.
8. Applies to DIP device types only.
9. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 7, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C &D	Samples/5005	1, 7, 9

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... GND -0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	48°C/W	8°C/W
Ceramic LCC Package	85°C/W	40°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 0.58W
Gate Count ..... 26000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range (T_A) ..... -55°C to +125°C
Operating Supply Voltage (VCC) ..... 4.5V to 5.5V
Input Low Voltage (VIL) ..... 0V to +0.8V
Input High Voltage (VIH) ..... +2.2V to VCC
Data Retention Supply Voltage ..... 2.0V to 4.5V
Input Rise and Fall Times ..... 40ns (Max)

TABLE 1. HM-65162C/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VCC = 4.5V, IO = -1.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 4.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 2.2V, or $\overline{E}$ = 2.2V VI/O = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-5.0	5.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-5.0	5.0	µA
Standby Supply Current	ICCSB1	VCC = 5.5V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	900	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 2.2V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	8	mA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = 5.5V, (Note 4), f = 1MHz, $\overline{E}$ = 0.8V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	70	mA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V	1, 2, 3,	$-55°C \le T_A \le +125°C$	-	70	mA
Data Retention Supply Current	ICCDR	VCC = 2.0V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	300	µA
Functional Test	FT	VCC = 4.5V (Note 5)	7, 8A, 8B	$-55°C \le T_A \le +125°C$	-	-	-

TABLE 2. HM-65162C/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	90	-	ns
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	90	ns
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	65	ns
Chip Enable Access Time	TELQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	90	ns
Write Enable Read Setup Time	TWHAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns
Address Setup Time	TAVWL	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns
Chip Selection to End of Write	TELWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	55	-	ns
Write Enable Pulse Setup Time	TWLEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	55	-	ns
Chip Enable Data Setup Time	TDVEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	30	-	ns
Address Valid to End of Write	TAVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	65	-	ns
Write Enable Pulse Write	TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	55	-	ns
Data Setup Time	TDVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	30	-	ns
Data Hold Time	TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	15	-	ns

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. HM-65162C/883 ELECTRICAL PERFORMANCE CHARACTERISTICS, A.C. AND D.C. (NOTE 6)

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, f = 1MHz All Measurements Referenced to Device Ground	6, 8	+25°C	-	10	pF
		VCC = Open, f = 1MHz, All Measurements Refernced to Device Ground	6, 9	+25°C	-	8	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	6, 8	+25°C	-	12	pF
		VCC = Open, f = 1MHz All Measurements Referenced to Device Ground	6, 9	+25°C	-	10	pF
Write Enable to Output in High Z	TWLQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	50	ns
Write Enable High to Output ON	TWHQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	0	-	ns
Chip Enable to Output ON	TELQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Output Enable to Output ON	TGLQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Chip Enable High to Output ON	TEHQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	50	ns
Output Disable to Output in High Z	TGHQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	40	ns
Output Hold from Address Change	TAVQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Output High Voltage	VOH2	VCC = 4.5V, IO = -100µA	6	$-55^{o}C \leq T_A \leq +125^{o}C$	VCC -0.4V	-	V

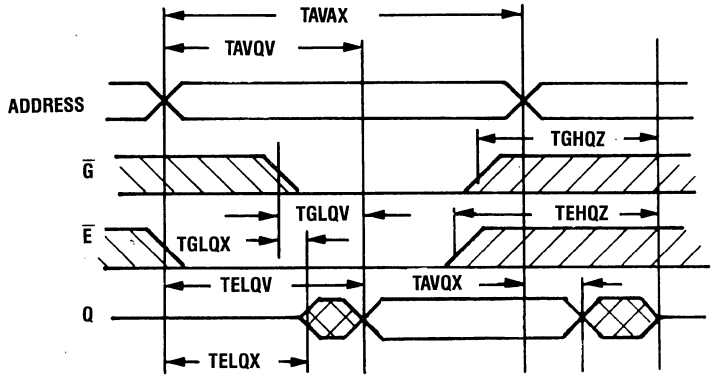
NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL $\geq$ 50pF; for CL > 50pF < 300pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.
4. Typical derating = 5mA/MHz increase in ICCOP.
5. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
6. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
7. This is a "typical" value and not a "maximum" value.
8. Applies to DIP device types only.
9. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 7, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C &D	Samples/5005	1, 7, 9

Timing Waveforms

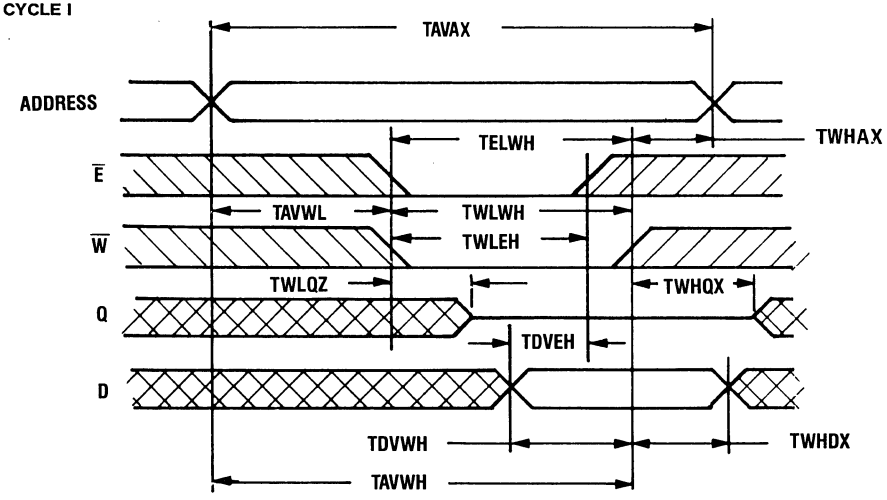
READ CYCLE



NOTE: $\overline{W}$ is High for a Read Cycle

Addresses must remain stable for the duration of the read cycle. To read, $\overline{G}$ and $\overline{E}$ must be $\leq$ VIL and $\overline{W} \geq$ VIH. The output buffers can be controlled independently by $\overline{G}$ while $\overline{E}$ is low. To execute consecutive read cycles, $\overline{E}$ may be tied low continuously until all desired locations are accessed. When $\overline{E}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.

WRITE CYCLE I

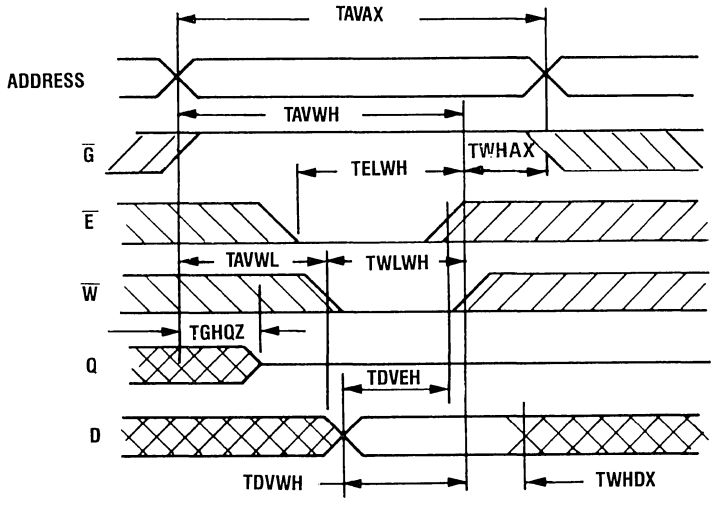


NOTE: $\overline{G}$ is Low Throughout Write Cycle

To write, addresses must be stable, $\overline{E}$ low and $\overline{W}$ falling low for a period no shorter than TWLWH. Data in is referenced with the raising edge of $\overline{W}$, (TDVWH and TWHDX). While addresses are changing, $\overline{W}$ must be high. When $\overline{W}$ falls low, the I/O pins are still in the output state for a period of TWLQZ and input data of the opposite phase to the outputs must not be applied, (Bus contention). If $\overline{E}$ transitions low simultaneously with the $\overline{W}$ line transitioning low or after the $\overline{W}$ transition, the output will remain in a high impedance state. $\overline{G}$ is held continuously low.

Timing Waveforms (Continued)

WRITE CYCLE II



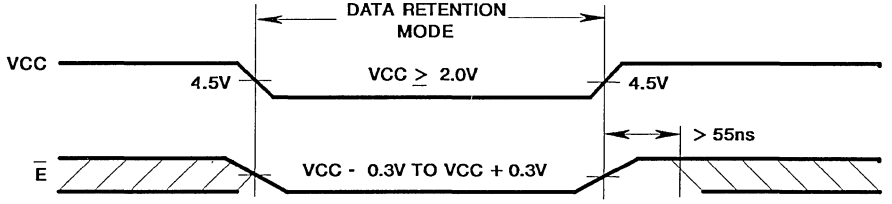
In this write cycle $\overline{G}$ has control of the output after a period, TGHQZ. $\overline{G}$ switching the output to a high impedance state allows data in to be applied without bus contention after TGHQZ. When $\overline{W}$ transitions high, the data in can change after TWHDX to complete the write cycle.

Low Voltage Data Retention

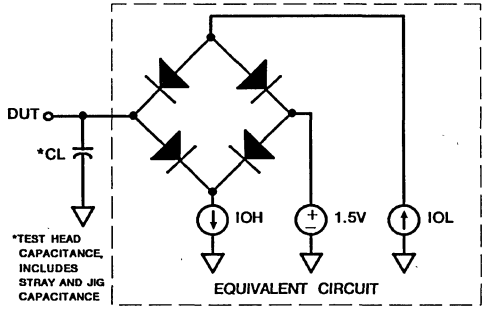
Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC - 0.3V to VCC + 0.3V.
2. On RAMs which have selects or output enables (e.g., S, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. Inputs which are to be held high (e.g., $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and down transitions.
4. The RAM can begin operation > 55ns after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING

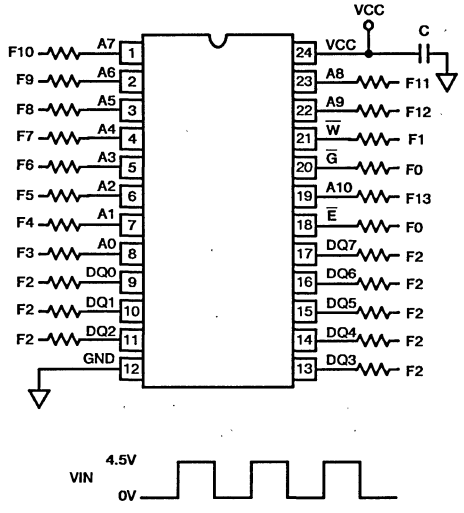


Test Circuit

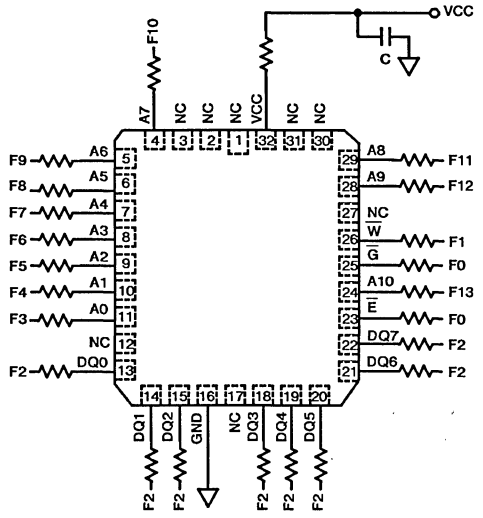


Burn-In Circuits

HM-65162/883 CERAMIC DIP



HM-65162/883 CERAMIC LCC



NOTES:
All Resistors 47kΩ, 5%
F0 = 100kHz ±10%
F1 = F0 ÷ 2, F2 = F1 ÷ 2,
F3 = F2 ÷ 2, . . . F13 = F12 ÷ 2
VCC = 5.5V, ±0.5V
C = 0.01μF (Min)
VIH = 4.5V ±10%
VIL = -0.2V to +0.4V

NOTES:
VCC = 5.5V ±0.5V
VIH = 4.5V ±10%
VIL = -0.2V to +0.4V
F1 = F0 ÷ 2, F2 = F1 ÷ 2,
F3 = F2 ÷ 2, . . . F13 = F12 ÷ 2
F0 = 100kHz ±10%
All Resistors 47kΩ, 5%
C = 0.01μF (Min)

Metal Topology

DIE DIMENSIONS:
186.2 x 200.1 x 19 ±1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 2kÅ

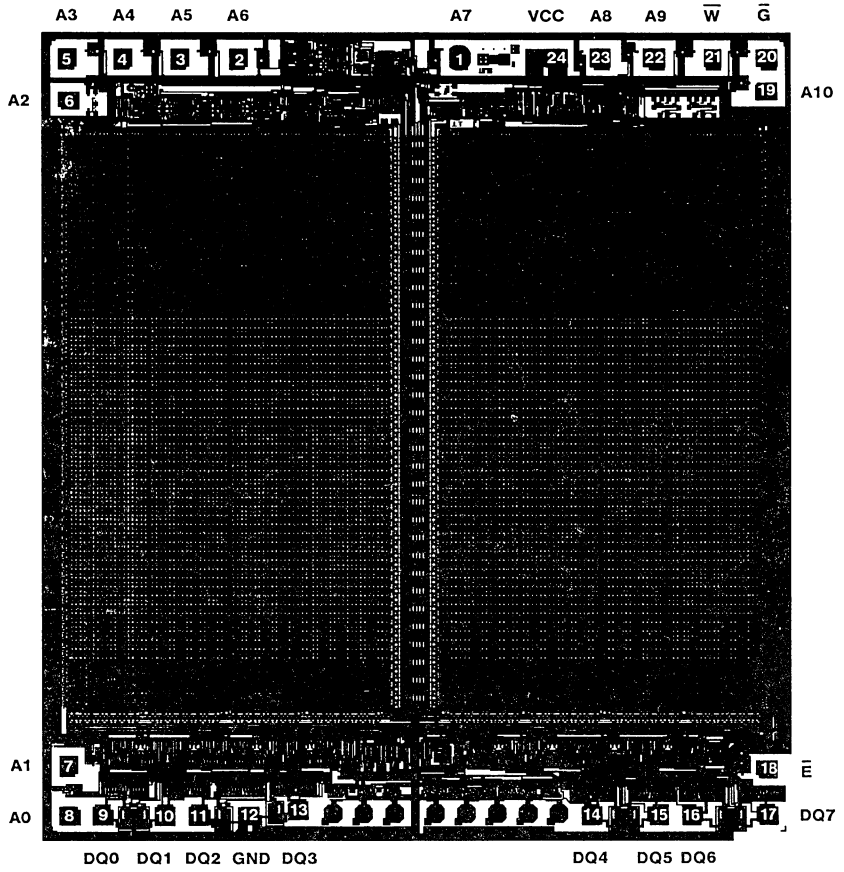
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.7×10^5 A/cm^2

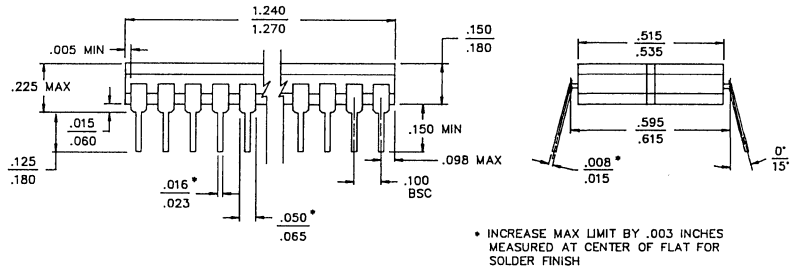
Metallization Mask Layout

HM-65162/883



Packaging†

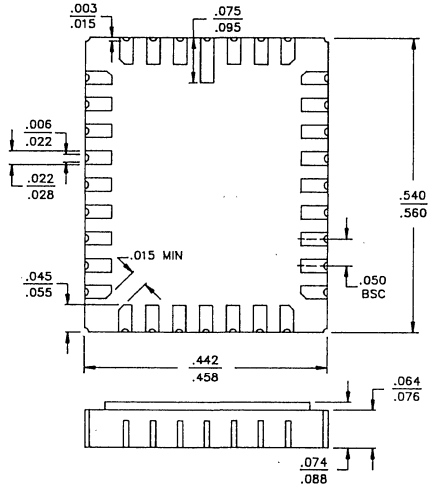
24 PIN CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-3

32 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

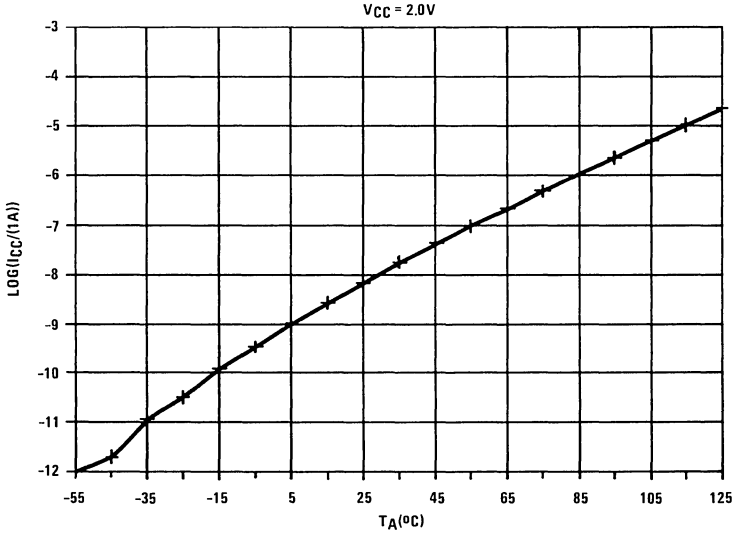
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-12

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

TYPICAL ICCDR vs. T_A



HARRIS

HM-65262/883

16K x 1 Asynchronous CMOS Static RAM

June 1989

Features

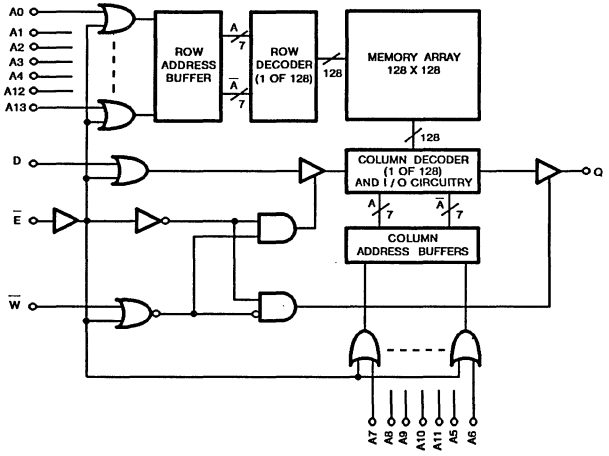
- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Fast Access Time..... 70/85ns Max
- Low Standby Current..... 50µA Max
- Low Operating Current ..... 50mA Max
- Data Retention at 2.0 Volts..... 20µA Max
- TTL Compatible Inputs and Outputs
- JEDEC Approved Pinout
- No Clocks or Strobes Required
- Temperature Range .....-55°C to +125°C
- Equal Cycle and Access Time
- Single 5 Volt Supply
- Gated Inputs-No Pull-Up or Pull-Down Resistors Required

Description

The HM-65262/883 is a CMOS 16384 x 1 bit Static Random Access Memory manufactured using the Harris Advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle times and ease of use. The HM-65262/883 is available in both JEDEC standard 20 pin, 0.300 inch wide DIP and 20 pad LCC packages, providing high board-level packing density. Gated inputs lower standby current, and also elminate the need for pull-up or pull-down resistors.

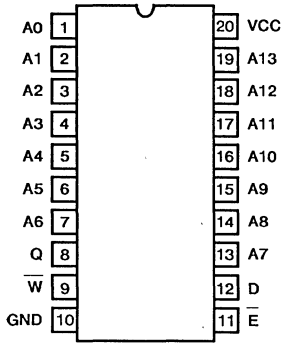
The HM-65262/883, a full CMOS RAM, utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T RAM cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor (4T) devices.

Functional Diagram

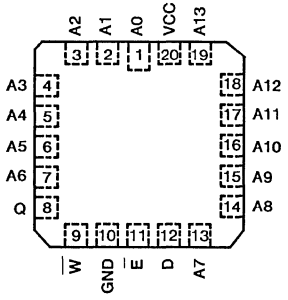


Pinouts

HM1-65262/883 (CERAMIC DIP)
TOP VIEW



HM4-65262/883 (CERAMIC LCC)
TOP VIEW



PIN	DESCRIPTION
A0 - A13	Address Input
$\overline{E}$	Chip Enable/Power Down
Q	Data Out
D	Data In
VSS/GND	Ground
VCC	Power (+5V)
$\overline{W}$	Write Enable

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	66°C/W	13°C/W
Ceramic LCC Package	85°C/W	40°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 0.75W
Ceramic LCC Package 0.58W
Gate Count ..... 26256 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (VCC) ..... 4.5V to 5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0V to +0.8V
Input High Voltage (VIH) ..... +2.2V to VCC
Data Retention Supply Voltage ..... 2.0V to 4.5V
Input Rise and Fall Time ..... 40ns Max

TABLE 1. HM-65262/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

D.C. PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VCC = 4.5V, IO = -4.0mA	1, 2, 3	-55°C≤T_A≤+125°C	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 8.0mA	1, 2, 3	-55°C≤T_A≤+125°C	-	0.4	V
High Impedance Output Leakage Current	IOZ	VCC = 5.5V, $\overline{E}$ = 5.5V, VO = GND or VCC	1, 2, 3	-55°C≤T_A≤+125°C	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	-55°C≤T_A≤+125°C	-1.0	1.0	µA
Standby Supply Current	ICCSB1	VCC = 5.5V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	-55°C≤T_A≤+125°C	-	50	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 2.2V	1, 2, 3	-55°C≤T_A≤+125°C	-	5	mA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 4), f = 1MHz, $\overline{E}$ = 0.8V	1, 2, 3	-55°C≤T_A≤+125°C	-	50	mA
Data Retention Supply Current	ICCDR	VCC = 2.0V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	-55°C≤T_A≤+125°C	-	20	µA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V	1, 2, 3	-55°C≤T_A≤+125°C	-	50	mA
Functional Test	FT	VCC = 4.5V (Note 5)	7, 8A, 8B	-55°C≤T_A≤+125°C	-	-	-

TABLE 2. HM-65262/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	(1) TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	85	-	ns
Address Access Time	(2) TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	-	85	ns
Chip Enable to End of Write	(3) TELWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	65	-	ns
Chip Enable Access Time	(4) TELQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	-	85	ns
Address Hold Time	(5) TWHAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Setup Time	(6) TAVWL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Valid to End of Write	(7) TAVWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	65	-	ns
Address Setup Time	(8) TAVEL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Hold Time	(9) TEHAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Valid to End of Write	(10) TAVEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	65	-	ns
Write Enable Pulse Write	(11) TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	45	-	ns
Data Setup Time	(12) TDVWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	35	-	ns
Data Hold Time	(13) TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ms
Enable Pulse Width	(14) TELEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	65	-	ns
Write to End of Write	(15) TWLEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	45	-	ns
Data Setup Time	(16) TDVEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	35	-	ns
Data Hold Time	(17) TEHDX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-65262/883 ELECTRICAL PERFORMANCE CHARACTERISTICS, A.C. AND D.C. (NOTE 6)

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6,7	$T_A = +25^oC$	-	10	pF
		VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6,8	$T_A = +25^oC$	-	6	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6,7	$T_A = +25^oC$	-	12	pF
		VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6,8	$T_A = +25^oC$	-	8	pF
Write Enable to Output in High Z	(18) TWLQZ	VCC = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
Write Enable High to Output ON	(19) TWHQX	VCC = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Enable to Output ON	(20) TELQX	VCC = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Output Enable High to Output in High Z	(21) TEHQZ	VCC = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
Chip Disable to Output Hold Time	(22) TEHQX	VCC = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Address Invalid Output Hold Time	(23) TAXQX	VCC = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
High Level Output Voltage	VOH2	VCC = 4.5V, IO = -100µA	6	$-55^oC \leq T_A \leq +125^oC$	VCC -0.4V	-	V

NOTES:
1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. AC measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL $\geq$ 50pF; for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.
4. Typical derating = 5mA/MHz increase in ICCOP.
5. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
6. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
7. Applies to DIP device types only.
8. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... -0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	66°C/W	13°C/W
Ceramic LCC Package	85°C/W	40°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 0.75W
Ceramic LCC Package 0.58W
Gate Count ..... 26256 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (VCC) ..... 4.5V to 5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0V to +0.8V
Input High Voltage (VIH) ..... +2.2V to VCC
Data Retention Supply Voltage ..... 2.0V to 4.5V
Input Rise and Fall Time ..... 40ns Max

TABLE 1. HM-65262B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

D.C. PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VCC = 4.5V, IO = -4.0mA	1, 2, 3	-55°C≤T_A≤+125°C	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 8.0mA	1, 2, 3	-55°C≤T_A≤+125°C	-	0.4	V
High Impedance Output Leakage Current	IOZ	VCC = 5.5V, $\overline{E}$ = 5.5V, VO = GND or VCC	1, 2, 3	-55°C≤T_A≤+125°C	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	-55°C≤T_A≤+125°C	-1.0	1.0	µA
Standby Supply Current	ICCSB1	VCC = 5.5V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	-55°C≤T_A≤+125°C	-	50	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 2.2V	1, 2, 3	-55°C≤T_A≤+125°C	-	5	mA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 4), f = 1MHz, $\overline{E}$ = 0.8V	1, 2, 3	-55°C≤T_A≤+125°C	-	50	mA
Data Retention Supply Current	ICCDR	VCC = 2.0V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	-55°C≤T_A≤+125°C	-	20	µA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V	1, 2, 3	-55°C≤T_A≤+125°C	-	50	mA
Functional Test	FT	VCC = 4.5V (Note 5)	7, 8A, 8B	-55°C≤T_A≤+125°C	-	-	-

TABLE 2. HM-65262B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	(1) TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	70	-	ns
Address Access Time	(2) TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	-	70	ns
Chip Enable to End of Write	(3) TELWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	55	-	ns
Chip Enable Access Time	(4) TELQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	-	70	ns
Address Hold Time	(5) TWHAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Setup Time	(6) TAVWL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Valid to End of Write	(7) TAVWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	55	-	ns
Address Setup Time	(8) TAVEL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Hold Time	(9) TEHAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Valid to End of Write	(10) TAVEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	55	-	ns
Write Enable Pulse Write	(11) TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	40	-	ns
Data Setup Time	(12) TDVWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	30	-	ns
Data Hold Time	(13) TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ms
Enable Pulse Width	(14) TELEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	55	-	ns
Write to End of Write	(15) TWLEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	40	-	ns
Data Setup Time	(16) TDVEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	30	-	ns
Data Hold Time	(17) TEHDX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-65262B/883 ELECTRICAL PERFORMANCE CHARACTERISTICS, A.C. AND D.C. (NOTE 6)

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 7	$T_A = +25^oC$	-	8	pF
		VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 8	$T_A = +25^oC$	-	6	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 7	$T_A = +25^oC$	-	10	pF
		VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 8	$T_A = +25^oC$	-	8	pF
Write Enable to Output in High Z	(18) TWLQZ	VCC = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
Write Enable High to Output ON	(19) TWHQX	VCC = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Enable to Output ON	(20) TELQX	VCC = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Output Enable High to Output in High Z	(21) TEHQZ	VCC = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
Chip Disable to Output Hold Time	(22) TEHQX	VCC = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Address Invalid Output Hold Time	(23) TAXQX	VCC = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
High Level Output Voltage	VOH2	VCC = 4.5V, IO = -100µA	6	$-55^oC \leq T_A \leq +125^oC$	VCC -0.4V	-	V

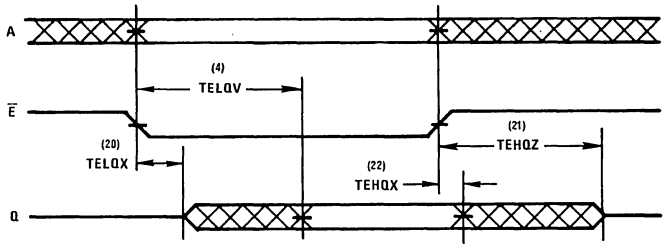
NOTES:
1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. AC measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL $\geq$ 50pF; for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.
4. Typical derating = 5mA/MHz increase in ICCOP.
5. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
6. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
7. Applies to DIP device types only.
8. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

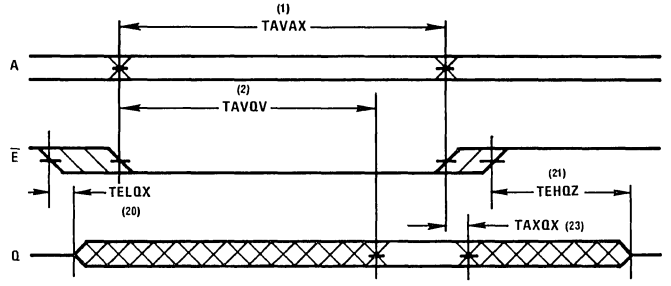
Timing Waveforms

READ CYCLE 1: CONTROLLED BY $\overline{E}$



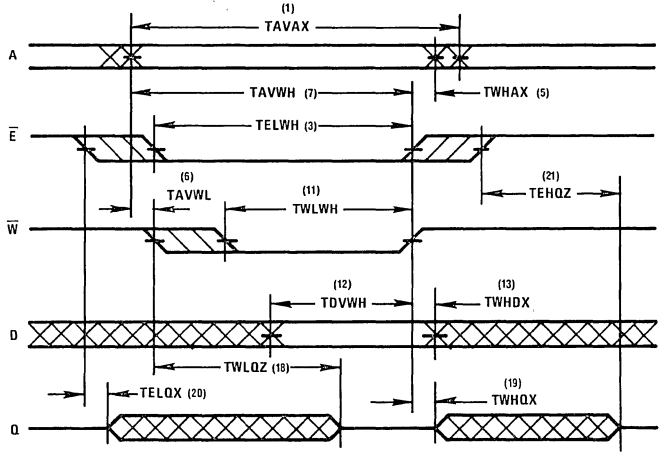
NOTE: $\overline{W}$ is high for entire cycle and D is ignored. Address is stable by the time $\overline{E}$ goes low and remains valid until $\overline{E}$ goes high.

READ CYCLE 2: CONTROLLED BY ADDRESS



NOTE: $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

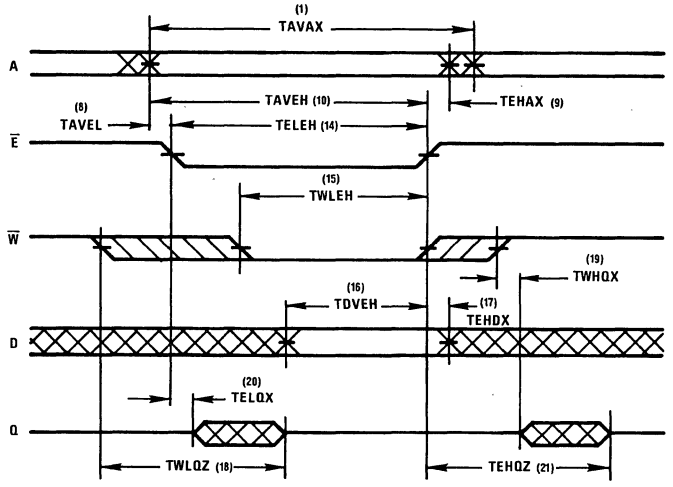
WRITE CYCLE 1: CONTROLLED BY $\overline{W}$ (LATE WRITE)



NOTE: In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

Timing Waveforms (Continued)

WRITE CYCLE 2: CONTROLLED BY $\overline{E}$ (EARLY WRITE)



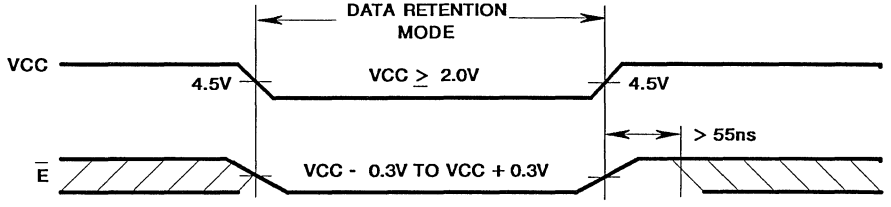
NOTE: In this mode, $\overline{W}$ rises after $\overline{E}$. If W falls before $\overline{E}$ by a time exceeding TWLQZ (Max) TELQX (Min), and rises after $\overline{E}$ by a time exceeding TEHQZ (Max)-TWHQZ (Min), then Q will remain in the high impedance state throughout the cycle.

Low Voltage Data Retention

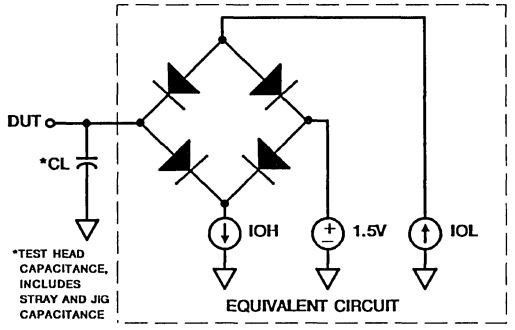
Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC to VCC + 0.3V.
2. On RAMs which have selects or output enables (e.g., S, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. Inputs which are to be held high (e.g., $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and down transitions.
4. The RAM can begin operation > 55ns after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING

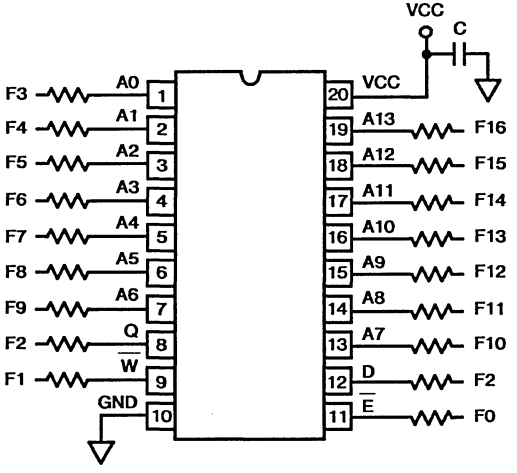


Test Circuit



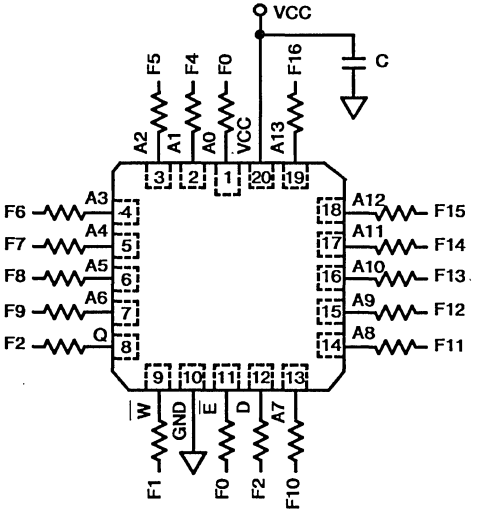
Burn-In Circuits

HM-65262/883 CERAMIC DIP



NOTES:
All Resistors 47kΩ, 5%
F0 = 100kHz ±10%
F1 = F0 ÷ 2,
F2 = F1 ÷ 2, . . . F16 = F15 ÷ 2
VCC = 5.5V, ±0.5V
VIH = 4.5V ±10%
VIL = -0.2V to +0.4V
C = 0.01μF (Min)

HM-65262/883 CERAMIC LCC



NOTES:
VCC = 5.5V ±0.5V
VIH = 4.5V ±10%
VIL = -0.2V to +0.4V
F1 = F0 ÷ 2, F2 = F1 ÷ 2,
F3 = F2 ÷ 2, . . . F13 = F12 ÷ 2
F0 = 100kHz ±10%
All Resistors 47kΩ,
C = 0.01μF (Min)

Metal Topology

DIE DIMENSIONS:
186.2 x 200.1 x 19 ±1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 2kÅ

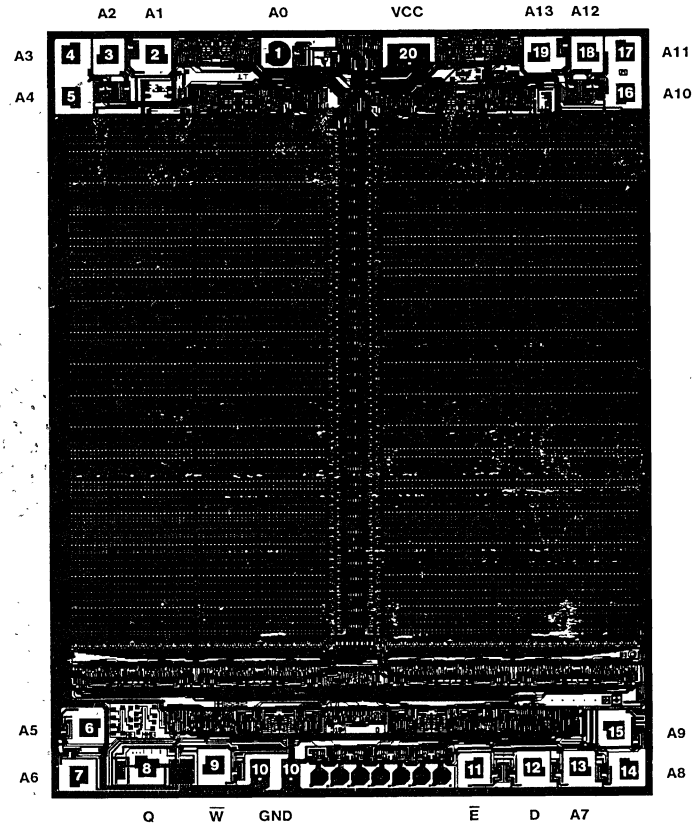
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.2 x 10^5 A/cm^2

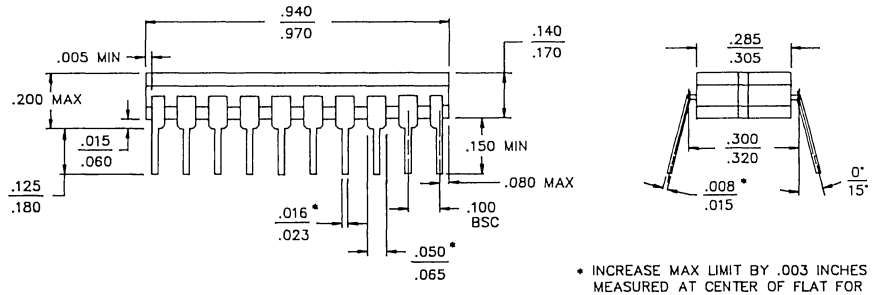
Metallization Mask Layout

HM-65262/883



Packaging†

20 PIN CERAMIC DIP

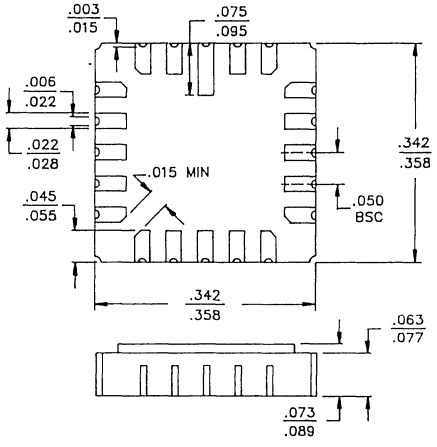


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-8

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

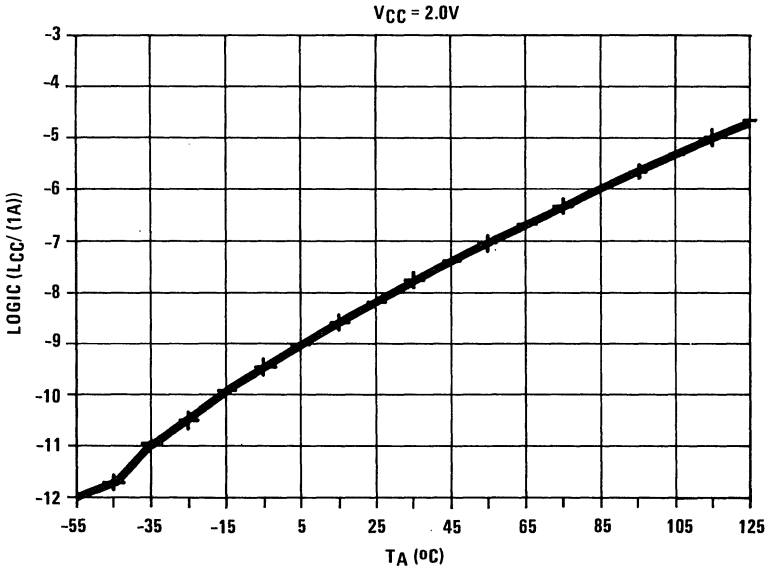
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

TYPICAL ICCDR vs. T_A



HARRIS

HM-65642/883

8K x 8 Asynchronous CMOS Static RAM

June 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Full CMOS Design
- Six Transistor Memory Cell
- Low Standby Supply Current 100µA
- Low Operating Supply Current 20mA
- Fast Address Access Time 150ns
- Low Data Retention Supply Voltage 2.0V
- CMOS/TTL Compatible Inputs/Outputs
- JEDEC Approved Pinout
- Equal Cycle and Access Times
- No Clocks or Strobes Required
- Gated Inputs — No Pull-Up or Pull-Down Resistors Required
- Temperature Range ..... -55°C to +125°C
- Easy Microprocessor Interfacing
- Dual Chip Enable Control

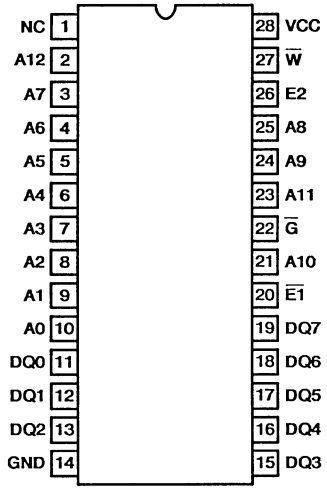
Description

The HM-65642/883 is a CMOS 8192 x 8-bit Static Random Access Memory. The pinout is the JEDEC 28 pin, 8-bit wide standard, which allows easy memory board layouts which accommodate a variety of industry standard ROM, PROM, EPROM, EEPROM and RAMs. The HM-65642/883 is ideally suited for use in microprocessor based systems. In particular, interfacing with the Harris 80C86 and 80C88 microprocessors is simplified by the convenient output enable ($\overline{G}$) input.

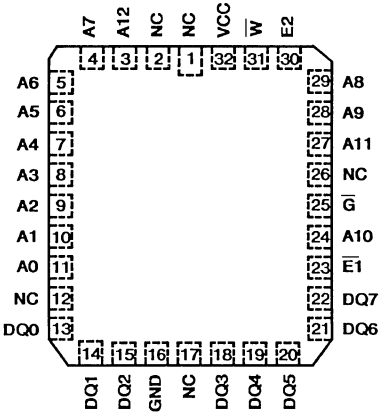
The HM-65642/883 is a full CMOS RAM which utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T RAM cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor or MIX-MOS (4T) devices.

Pinouts

HM1-65642/883 (CERAMIC DIP)
TOP VIEW



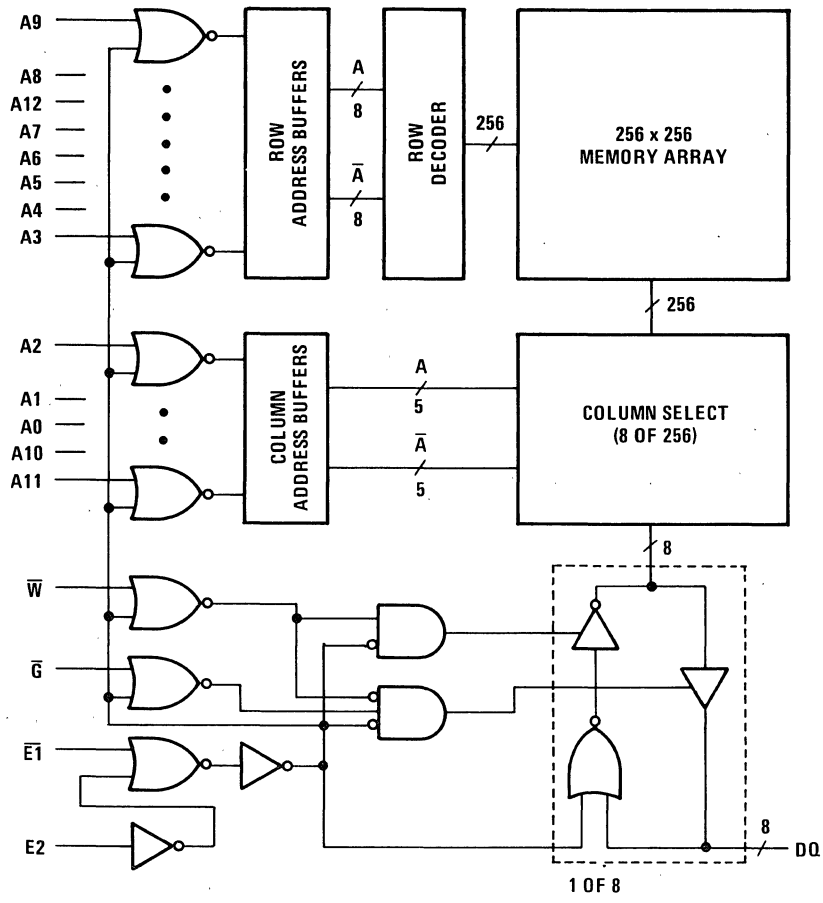
HM4-65642/883 (CERAMIC LCC)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
DQ	Data Input/Output
$\overline{E1}$	Chip Enable
E2	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
NC	No Connections
GND	Ground
VCC	Power

3 CMOS MEMORY

Functional Diagram



TRUTH TABLE

MODE	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$
Standby (CMOS)	X	GND	X	X
Standby (TTL)	VIH	X	X	X
	X	VIL	X	X
Enable (High Z)	VIL	VIH	VIH	VIH
Write	VIL	VIH	VIL	X
Read	VIL	VIH	VIH	VIL

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering Ten Seconds) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance Junction-to-Case (θ_{jc})
Ceramic DIP ..... 8°C/W
Ceramic LCC ..... 45°C/W
Thermal Impedance Junction-to-Ambient (θ_{ja})
Ceramic DIP ..... 45°C/W
Ceramic LCC ..... 55°C/W
Maximum Package Power Dissipation at +125°C
Ceramic DIP ..... 1.1 Watts
Ceramic LCC ..... 0.90 Watts
Gate Count ..... 101,000 Gates

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operationl sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (VCC) ..... 4.5V to 5.5V
Operating Temperature (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... -0.3V to +0.8V
Input High Voltage (VIH) ..... +2.2V to VCC +0.3V
Data Retention Supply Voltage 2.0V
Input Rise and Fall Time ..... 40ns Max

TABLE 1. HM-65642/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

D.C. PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH 1	VCC = 4.5V, IO = -1.0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	—	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 4.0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 2.2V VI/O = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	1.0	µA
Standby Supply Current	ICCSB1	VCC = 5.5V, IO = 0mA, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	250	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E1}$ = 2.2V or E2 = 0.8V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	5	mA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E1}$ = 0.8V, E2 = 2.2V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	5	mA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = 5.5V, (Note 5), f = 1MHz, $\overline{E1}$ = 0.8V, E2 = 2.2V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	20	mA
Data Retention Supply Current	ICCDR	VCC = 2.0V, IO = 0mA, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	150	µA
Functional Test	FT	VCC = 4.5V (Note 4)	7, 8A, 8B	$-55°C \leq T_A \leq +125°C$	-	-	-

NOTES: 1. All voltages referenced to device GND.

2. A.C. measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL $\geq$ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.

3. For timing waveforms see Low Voltage Data Retention and Read/Write Cycles.

4. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.

5. Typical derating = 5mA/MHz increase in ICCOP.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-65642/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	150	ns
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	70	ns
Chip Enable Access Time	TE1LQV TE2HQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	150	ns
Write Recovery Time	TWHAX TE1HAX TE2LAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Chip Enable to End-of-Write	TE1LE1H TE2HE2L	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	90	-	ns
Address Setup Time	TAVWL TAVE1L TAVE2H	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Write Enable Pulse Width	TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	90	-	ns
Data Setup Time	TDVWH TDVE1H TDVE2L	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	60	-	ns
Data Hold Time	TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
	TE1HDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
	TE2LDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns

NOTES: 1. All voltages referenced to device GND.

2. A.C. measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL $\geq$ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.

3. For timing waveforms see Low Voltage Data Retention and Read/Write Cycles.

4. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.

5. Typical derating = 5mA/MHz increase in ICCOP.

TABLE 3. HM-65642/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output High Voltage	VOH2	VCC = 4.5V, IO = -100µA	1	$-55^oC \leq T_A \leq +125^oC$	VCC-0.4	-	V
Input Capacitance	CIN	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	12	pF
		VCC = Open, f = 1MHz All Measurements Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	10	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz All Measurements Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	14	pF
		VCC = 4.5V, VI/O = GND or VCC, All Measurements Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	12	pF
Write Enable to Output in High Z	TWLQZ	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Write Enable High to Output ON	TWHQX	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Enable to Output ON	TE1LQX TE2HQX	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Output Enable to Output ON	TGLQX	VCC = 4.5 and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Enable to Output in High Z	TE1HQZ	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
	TE2LQZ		1	$-55^oC \leq T_A \leq +125^oC$	-	60	ns
Output Disable to Output in High Z	TGHQZ	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Output Hold from Address Change	TAXQX	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	10	-	ns

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

2. Applies to DIP device types only. For design purposes CIN = 6pF typical and CI/O = 7pF typical.

3. Applies to LCC device types only. For design purposes CIN = 4pF typical and CI/O = 5pF typical.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	GROUPS METHOD	SUBGROUPS
Interim Test 1	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test 1	100%/5004	2, 3, 8A, 8B, 10,11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering Ten Seconds) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance Junction-to-Case (θ_{jc})
Ceramic DIP ..... 8°C/W
Ceramic LCC ..... 45°C/W
Thermal Impedance Junction-to-Ambient (θ_{ja})
Ceramic DIP ..... 45°C/W
Ceramic LCC ..... 55°C/W
Maximum Package Power Dissipation
Ceramic DIP ..... 1.1 Watts
Ceramic LCC ..... 0.90 Watts
Gate Count ..... 101,000 Gates

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (VCC) ..... 4.5V to 5.5V
Operating Temperature (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... -0.3V to +0.8V
Input High Voltage (VIH) ..... +2.2V to VCC +0.3V
Data Retention Supply Voltage 2.0V
Input Rise and Fall Time ..... 40ns Max

TABLE 1. HM-65642B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

D.C. PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH 1	VCC = 4.5V, IO = -1.0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	—	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 4.0mA	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 2.2V VI/O = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	1.0	µA
Standby Supply Current	ICCSB1	VCC = 5.5V, IO = 0mA, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	100	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E1}$ = 2.2V or E2 = 0.8V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	5	mA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E1}$ = 0.8V, E2 = 2.2V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	5	mA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = 5.5V, (Note 5), f = 1MHz, $\overline{E1}$ = 0.8V, E2 = 2.2V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	20	mA
Data Retention Supply Current	ICCDR	VCC = 2.0V, IO = 0mA, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	75	µA
Functional Test	FT	VCC = 4.5V (Note 4)	7, 8A, 8B	$-55°C \leq T_A \leq +125°C$	-	-	-

NOTES: 1. All voltages referenced to device GND.

2. A.C. measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL $\geq$ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.

3. For timing waveforms see Low Voltage Data Retention and Read/Write Cycles.

4. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.

5. Typical derating = 5mA/MHz increase in ICCOP.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-65642B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	150	ns
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	70	ns
Chip Enable Access Time	TE1LQV TE2HQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	150	ns
Write Recovery Time	TWHAX TE1HAX TE2LAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Chip Enable to End-of-Write	TE1LE1H TE2HE2L	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	90	-	ns
Address Setup Time	TAVWL TAVE1L TAVE2H	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Write Enable Pulse Width	TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	90	-	ns
Data Setup Time	TDVWH TDVE1H TDVE2L	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	60	-	ns
Data Hold Time	TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
	TE1HDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
	TE2LDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns

NOTES: 1. All voltages referenced to device GND.

2. A.C. measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL $\geq$ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.

3. For timing waveforms see Low Voltage Data Retention and Read/Write Cycles.

4. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.

5. Typical derating = 5mA/MHz increase in ICCOP.

TABLE 3. HM-65642B/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output High Voltage	VOH2	VCC = 4.5V, IO = -100µA	1	$-55^oC \leq T_A \leq +125^oC$	VCC-0.4	-	V
Input Capacitance	CIN	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	12	pF
		VCC = Open, f = 1MHz All Measurements Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	10	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz All Measurements Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	14	pF
		VCC = 4.5V, VI/O = GND or VCC, All Measurements Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	12	pF
Write Enable to Output in High Z	TWLQZ	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Write Enable High to Output ON	TWHQX	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Enable to Output ON	TE1LQX TE2HQX	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Output Enable to Output ON	TGLQX	VCC = 4.5 and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Enable to Output in High Z	TE1HQZ	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
	TE2LQZ		1	$-55^oC \leq T_A \leq +125^oC$	-	60	ns
Output Disable to Output in High Z	TGHQZ	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Output Hold from Address Change	TAXQX	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	10	-	ns

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

2. Applies to DIP device types only. For design purposes CIN = 6pF typical and CI/O = 7pF typical.

3. Applies to LCC device types only. For design purposes CIN = 4pF typical and CI/O = 5pF typical.

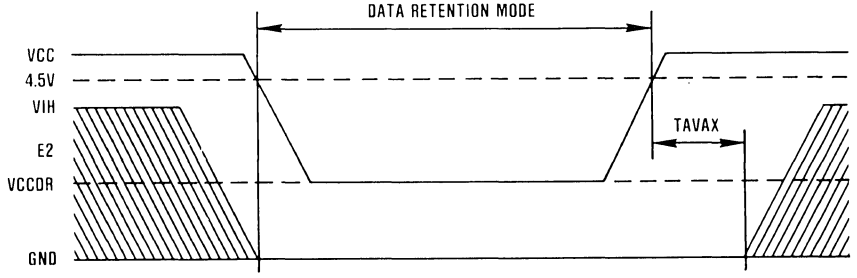
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	GROUPS METHOD	SUBGROUPS
Interim Test 1	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test 1	100%/5004	2, 3, 8A, 8B, 10,11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

Low Voltage Data Retention

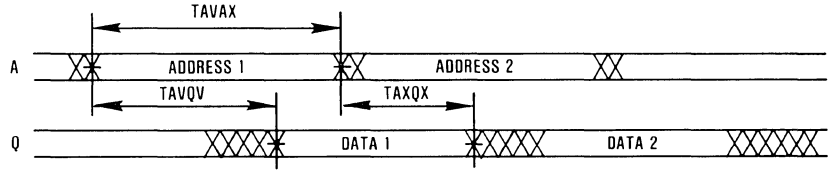
Harris CMOS RAMs are designed with battery backup in mind. Data Retention voltage and supply current are guaranteed over the operating temperature range. The following rules ensure data retention:

1. The RAM must be kept disabled during data retention. This is accomplished by holding the E2 pin between -0.3V and GND.
2. During power-up and power-down transitions, E2 must be held between -0.3V and 10% of VCC.
3. The RAM can begin operating one TAVAX after VCC reaches the minimum operating voltage of 4.5V.

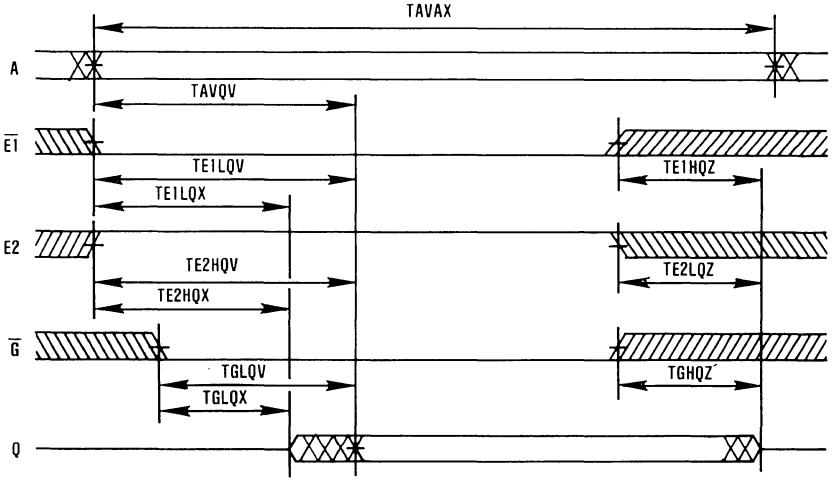


Read Cycles

READ CYCLE I: $\overline{W}$, E2 HIGH; $\overline{G}$, $\overline{E1}$ LOW

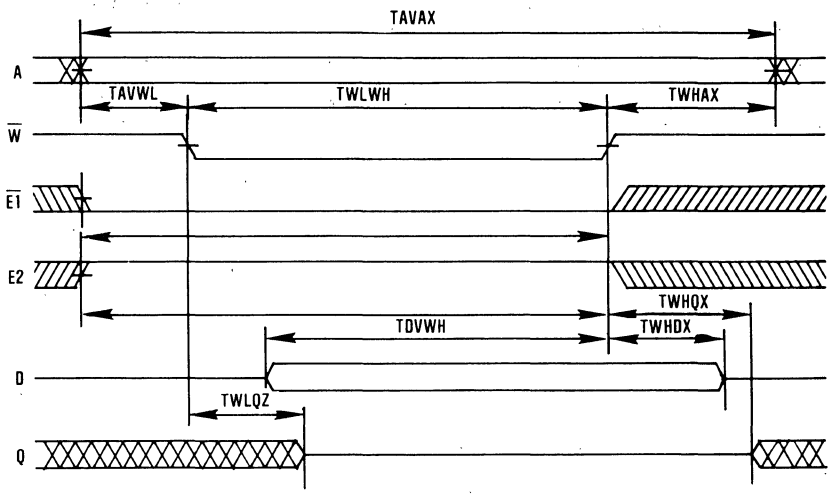


READ CYCLE II: $\overline{W}$ HIGH

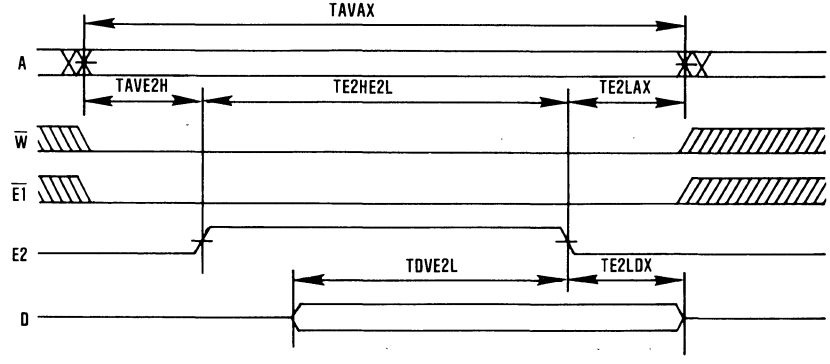


Write Cycles

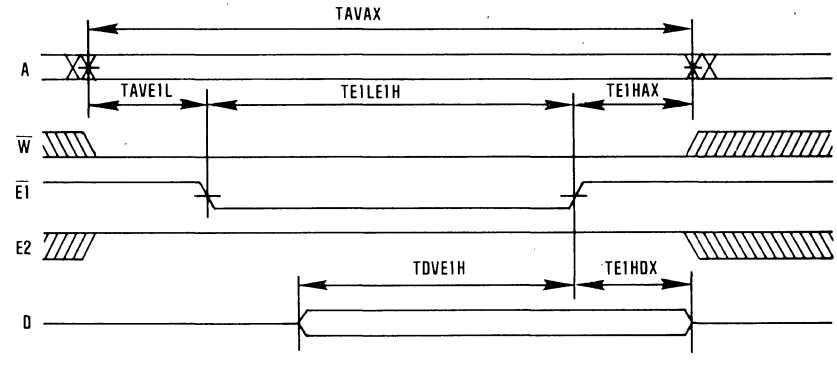
WRITE CYCLE I: LATE WRITE



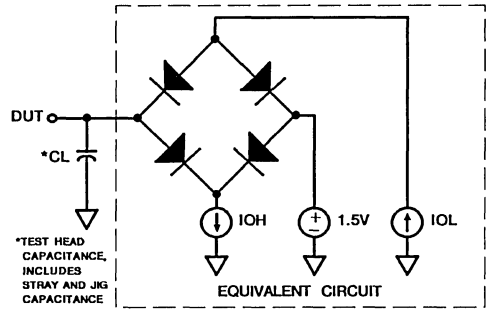
WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E1}$



WRITE CYCLE III: EARLY WRITE - CONTROLLED BY E2

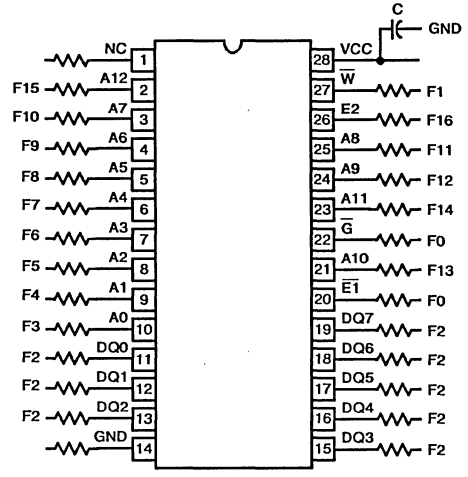


Test Circuit



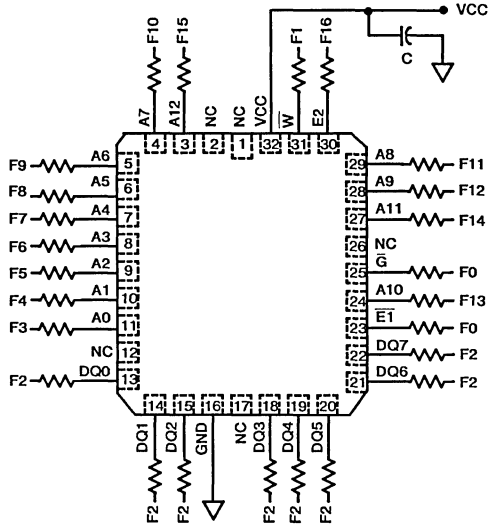
Burn-In Circuits

HM-65642/883 CERAMIC DIP



NOTES:
F0 = 100kHz ±10%
All Resistors 47kΩ, 5%
C = 0.01µF (Min)
VCC = 5.5V, ±0.5V
VIH = 4.5V, ±10%
VIL = -0.2V to +0.4V

HM-65642/883 CERAMIC LCC



NOTES:
F0 = 100kHz ±10%
C = 0.01µF (Min)
VCC = 5.5V, ±0.5V
VIH = 4.5V, ±10%
VIL = -0.2V to +0.4V

Die Characteristics

DIE DIMENSIONS:
276.8 x 305.5 x 19 ± 1 mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 2kÅ

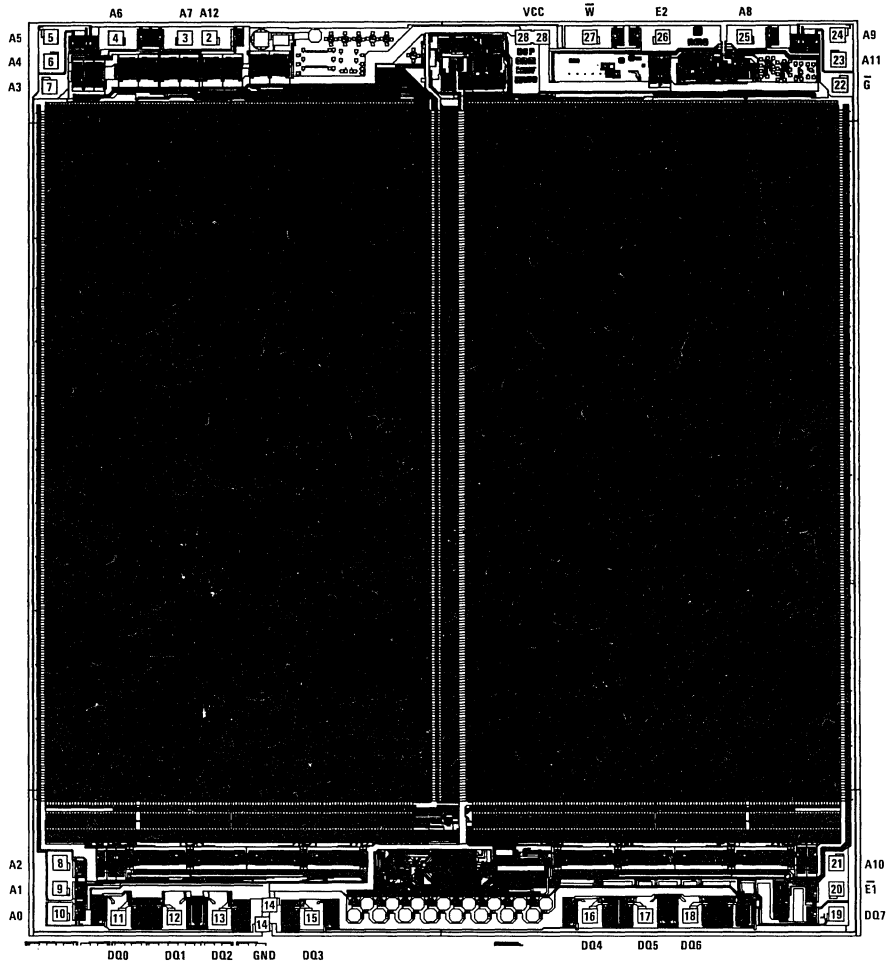
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ to ± 1kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY: 0.9 x 10^5 Amps/cm^2

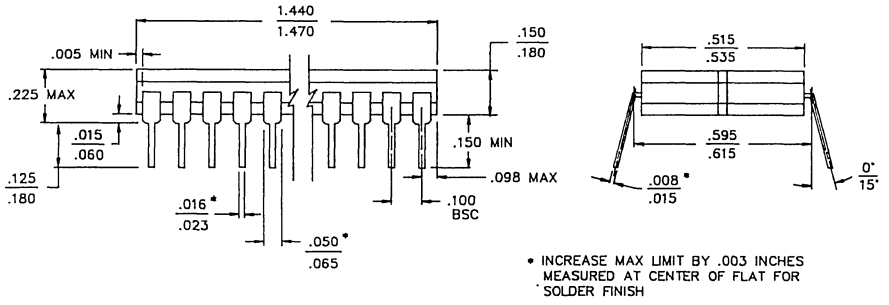
Metallization Mask Layout

HM-65642/883



Packaging†

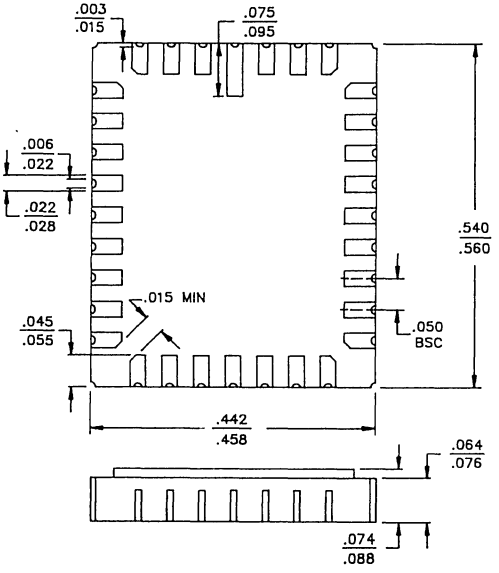
28 PIN CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Aluminum
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C to ±10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

32 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic 90% Aluminum
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ±10°C
Method: Furnace Braze

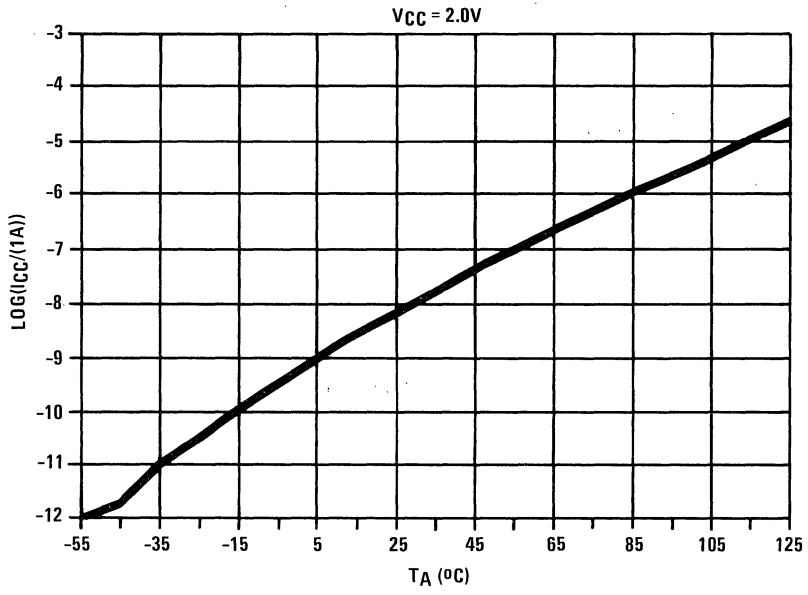
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-12

NOTE: All Dimensions are Min/Max, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

TYPICAL ICCDR vs. T_A



HARRIS

HM-65642C/883

8K x 8 Asynchronous CMOS Static RAM

June 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Full CMOS Design
- Six Transistor Memory Cell
- Low Standby Supply Current 400µA
- Low Operating Supply Current 20mA
- Fast Address Access Time 200ns
- Low Data Retention Supply Voltage 2.0V
- CMOS/TTL Compatible Inputs/Outputs
- JEDEC Approved Pinout
- Equal Cycle and Access Times
- No Clocks or Strobes Required
- Gated Inputs —
  No Pull-Up or Pull-Down Resistors Required
- Temperature Range ..... -55°C to +125°C
- Easy Microprocessor Interfacing
- Dual Chip Enable Control

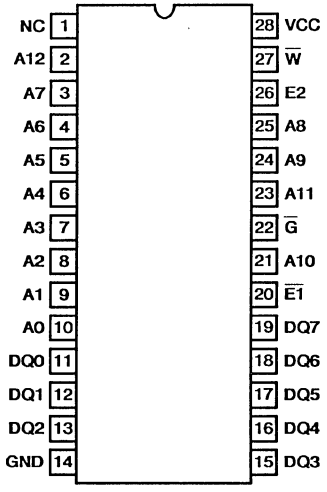
Description

The HM-65642C/883 is a CMOS 8192 x 8-bit Static Random Access Memory. The pinout is the JEDEC 28 pin, 8-bit wide standard, which allows easy memory board layouts which accommodate a variety of industry standard ROM, PROM, EPROM, EEPROM and RAMs. The HM-65642C/883 is ideally suited for use in microprocessor based systems. In particular, interfacing with the Harris 80C86 and 80C88 microprocessors is simplified by the convenient output enable ($\overline{G}$) input.

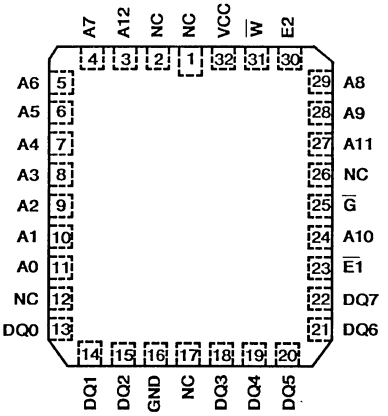
The HM-65642C/883 is a full CMOS RAM which utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T RAM cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor or MIX-MOS (4T) devices.

Pinouts

HM1-65642C/883 (CERAMIC DIP)
TOP VIEW



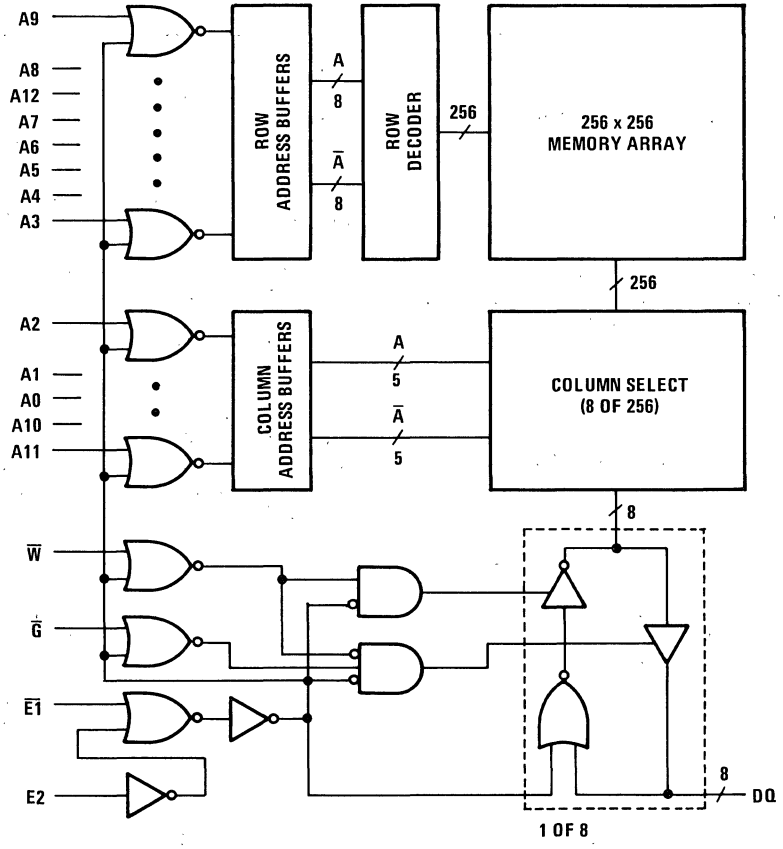
HM4-65642C/883 (CERAMIC LCC)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
DQ	Data Input/Output
$\overline{E1}$	Chip Enable
E2	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
NC	No Connections
GND	Ground
VCC	Power

3 CMOS MEMORY

Functional Diagram



TRUTH TABLE

MODE	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$
Standby (CMOS)	X	GND	X	X
Standby (TTL)	VIH	X	X	X
	X	VIL	X	X
Enable (High Z)	VIL	VIH	VIH	VIH
Write	VIL	VIH	VIL	X
Read	VIL	VIH	VIH	VIL

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering Ten Seconds) ..... 300°C
Junction Temperature ..... +175°C
ESD Classification ..... Class 1
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP

Reliability Information

Thermal Impedance Junction-to-Case (θ_{jc})
Ceramic DIP ..... 8°C/W
Ceramic LCC ..... 45°C/W
Thermal Impedance Junction-to-Ambient (θ_{ja})
Ceramic DIP ..... 45°C/W
Ceramic LCC ..... 55°C/W
Maximum Package Power Dissipation at +125°C
Ceramic DIP ..... 1.1 Watt
Ceramic LCC ..... 0.90 Watt
Gate Count ..... 101,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (VCC) ..... 4.5V to 5.5V
Operating Temperature (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... -0.3V to +0.8V
Input High Voltage (VIH) ..... +2.2V to VCC
Data Retention Supply Voltage 2.0V
Input Rise and Fall Time ..... 40ns Max

TABLE 1. HM-65642C/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

D.C. PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH 1	VCC = 4.5V, IO = -1.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	—	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 4.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 2.2V VI/O = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-2.0	2.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-2.0	2.0	µA
Standby Supply Current	ICCSB1	VCC = 5.5V, IO = 0mA, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	400	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E1}$ = 2.2V or E2 = 0.8V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	5	mA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E1}$ = 8.0V, E2 = 2.2V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	5	mA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = 5.5V, (Note 5), f = 1MHz, $\overline{E1}$ = 0.8V, E2 = 2.2V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	20	mA
Data Retention Supply Current	ICCDR	VCC = 2.0V, IO = 0mA, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	250	µA
Functional Test	FT	VCC = 4.5V (Note 4)	7, 8A, 8B	$-55°C \le T_A \le +125°C$	-	-	-

NOTES: 1. All voltages referenced to V_{SS}.

2. A.C. measurements assume transition time $\le$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL $\ge$ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.

3. For timing waveforms see Low Voltage Data Retention and Read/Write Cycles.

4. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\ge$ 1.5V, and VOL $\le$ 1.5V.

5. Typical derating = 5mA/MHz increase in ICCOP.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. HM-65642C/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	200	-	ns
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	200	ns
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	70	ns
Chip Enable Access Time	TE1LQV TE2HQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	200	ns
Write Recovery Time	TWHAX TE1HAX TE2LAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Chip Enable to End-of-Write	TE1LE1H TE2HE2L	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Address Setup Time	TAVWL TAVE1L TAVE2H	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Write Enable Pulse Width	TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Data Setup Time	TDVWH TDVE1H TDVE2L	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	80	-	ns
Data Hold Time	TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
	TE1HDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
	TE2LDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns

NOTES:
1. All voltages referenced to V_{SS}.
2. A.C. measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL $\geq$ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms see Low Voltage Data Retention and Read/Write Cycles.
4. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
5. Typical derating = 5mA/MHz increase in ICCOP.

TABLE 3. HM-65642C/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, All Measurements f = 1MHz, Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	12	pF
		VCC = Open, All Measurements f = 1MHz, Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	10	pF
I/O Capacitance	CI/O	VCC = Open, All Measurements f = 1MHz, Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	14	pF
		VCC = Open, All Measurements f = 1MHz, Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	12	pF
Write Enable to Output in High Z	TWLQZ	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	70	ns
Write Enable High to Output ON	TWHQX	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Enable to Output ON	TE1LQX TE2HQX	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Output Enable to Output ON	TGLQX	VCC = 4.5 and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Enable to Output in High Z	TE1HQZ	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	70	ns
	TE2LQZ				-	70	ns
Output Disable to Output in High Z	TGHQZ	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	60	ns
Output Hold from Address Change	TAXQX	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Output High Voltage	VOH2	VCC = 4.5V, IO = -100µA	1	$-55^oC \leq T_A \leq +125^oC$	VCC -0.4	-	V

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

2. Applies to DIP device types only. For design purposes CIN = 6pF typical and CI/O = 7pF.

3. Applies to LCC device types only. For design purposes CIN = 4pF typical and CI/O = 5pF typical.

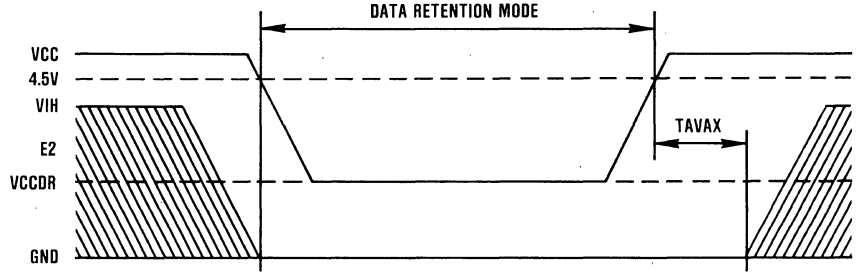
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	GROUPS METHOD	SUBGROUPS
Interim Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10,11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

Low Voltage Data Retention

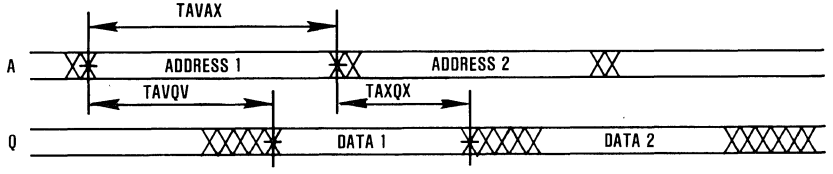
Harris CMOS RAMs are designed with battery backup in mind. Data Retention voltage and supply current are guaranteed over the operating temperature range. The following rules ensure data retention:

1. The RAM must be kept disabled during data retention. This is accomplished by holding the E2 pin between -0.3V and GND.
2. During power-up and power-down transitions, E2 must be held between -0.3V and 10% of VCC.
3. The RAM can begin operating one TAVAX after VCC reaches the minimum operating voltage of 4.5V.

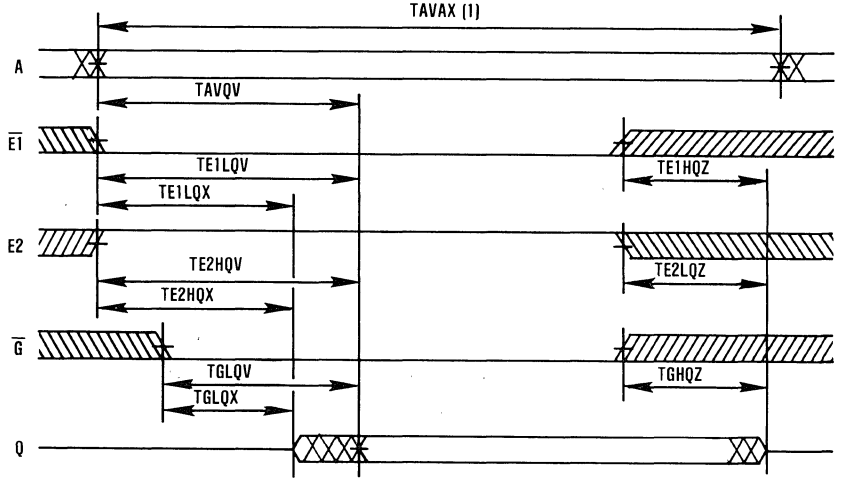


Read Cycles

READ CYCLE I: $\overline{W}$, E2 HIGH; $\overline{G}$, $\overline{E1}$ LOW

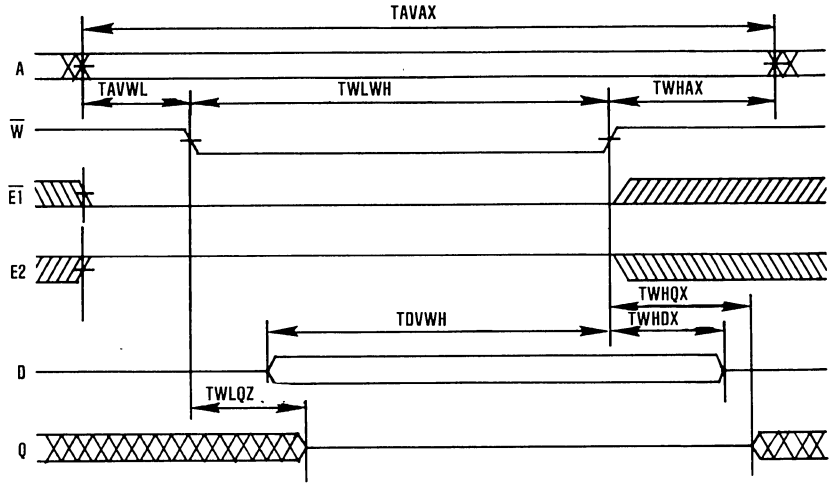


READ CYCLE II: $\overline{W}$ HIGH

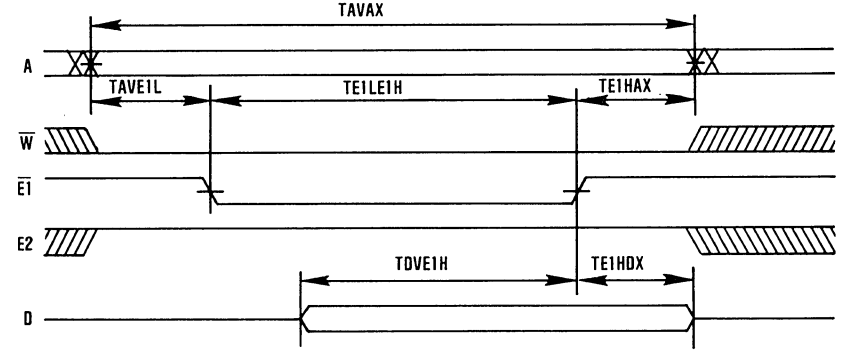


Write Cycles

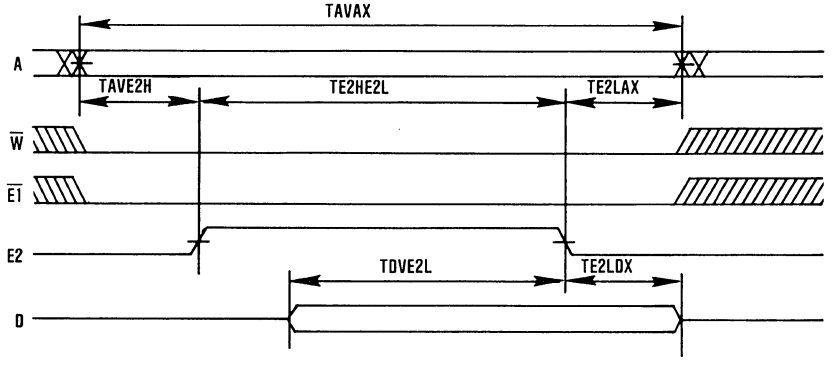
WRITE CYCLE I: LATE WRITE



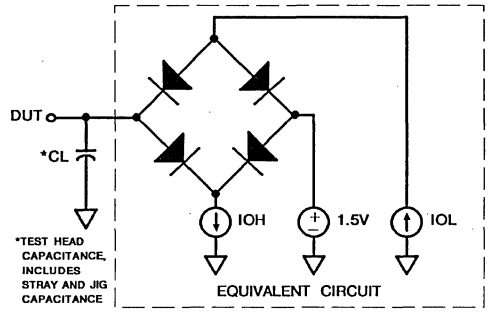
WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E1}$



WRITE CYCLE III: EARLY WRITE - CONTROLLED BY E2

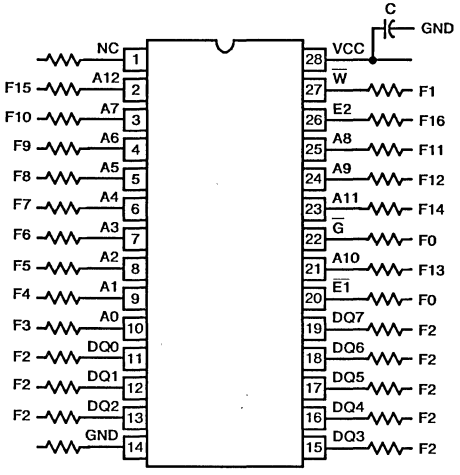


Test Circuit



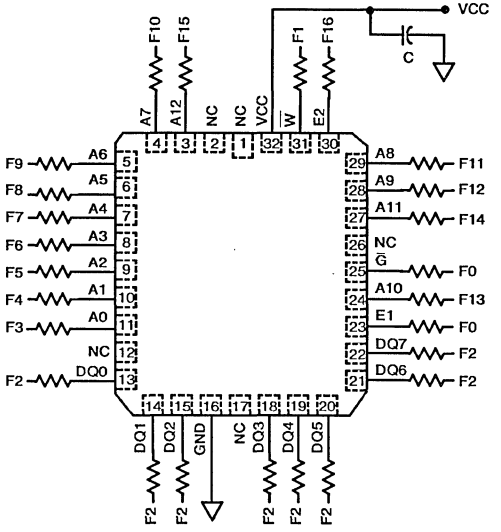
Burn-In Circuits

HM-65642C/883 CERAMIC DIP



NOTES:
F0 = 100kHz ±10%
All Resistors 47kΩ, 5%
C = 0.01μF (Min)
VCC = 5.5V, ±0.5V
VIN = 4.5V, ±10%
VIL = -0.2V to +0.4V

HM-65642C/883 CERAMIC LCC



NOTES:
F0 = 100kHz ±10%
All Resistors 47kΩ, 5%
C = 0.01μF (Min)
VCC = 5.5V ±0.5V
VIN = 4.5V ±10%
VIL = -0.2V to +0.4V

Die Characteristics

DIE DIMENSIONS:
276.8 x 305.5 x 19 ± 1 mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 2kÅ

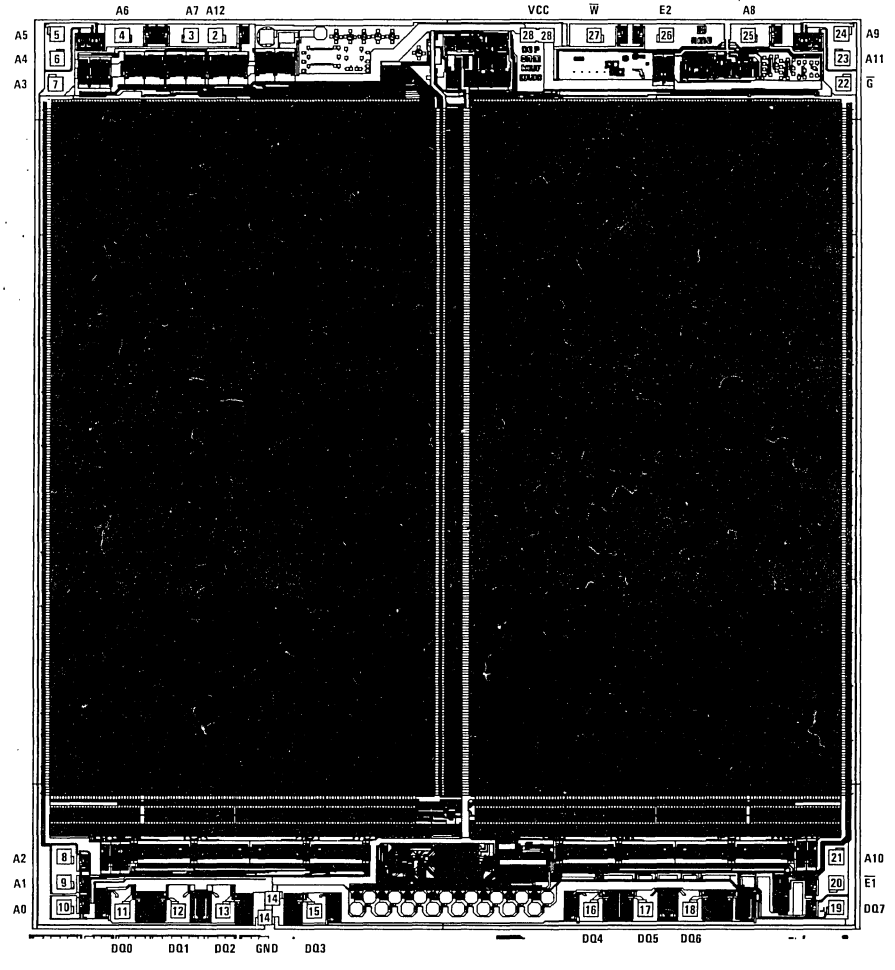
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ to ± 1kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY: 0.9 x 10^5 Amps/cm^2

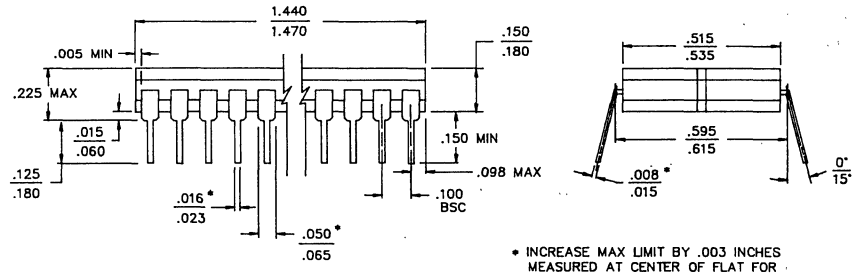
Metallization Mask Layout

HM-65642C/883



Packaging†

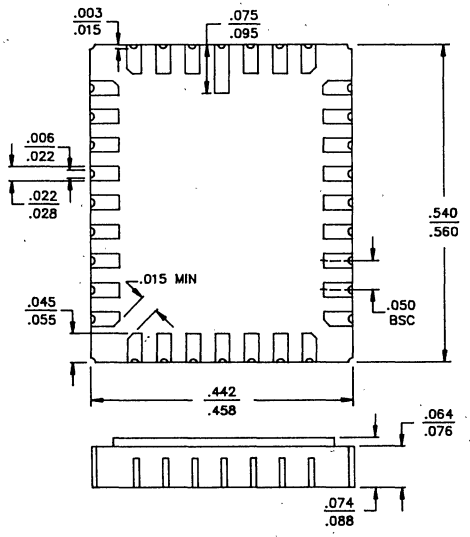
28 PIN CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Aluminum
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C to ±10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

32 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic 90% Aluminum
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ±10°C
Method: Furnace Braze

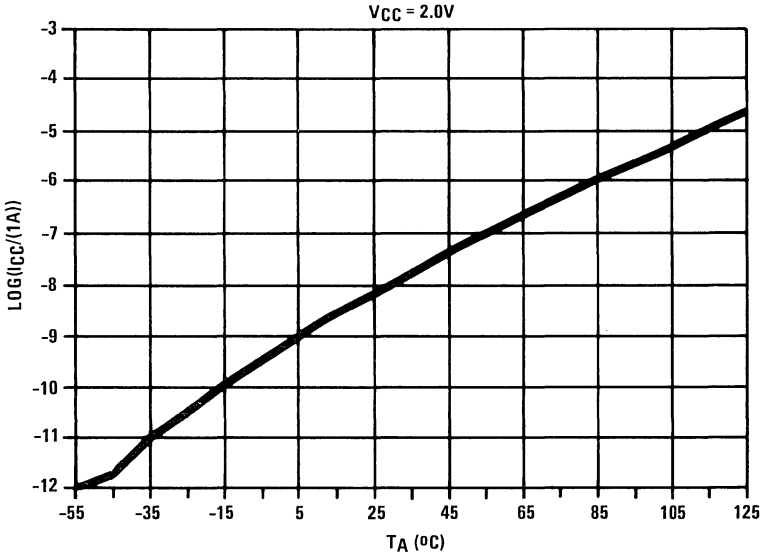
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-12

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

TYPICAL ICCDR vs. T_A



HARRIS

HM-6564-8

June 1989

8K x 8, 16K x 4 CMOS RAM

Features

- Low Power Standby ..... 4mW Maximum
- Low Power Operation ..... 280mW/MHz Maximum
- Data Retention ..... 2.0V Minimum
- TTL Compatible In/Out
- Three State Outputs
- Fast Access Time ..... 350ns Maximum
- Operating Temperature Range ..... -55°C to +125°C
- On Chip Address Registers
- Organizable 8K x 8 or 16K x 4
- 40 Pin DIP Pinout — 2.000" x 0.900"

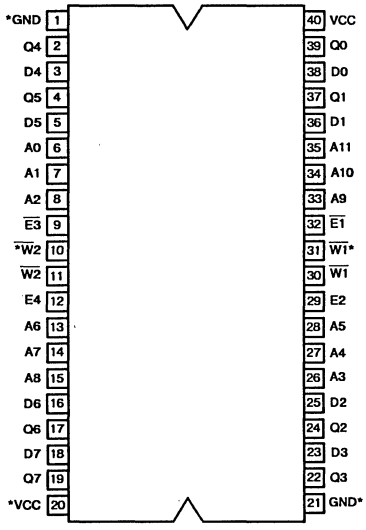
Description

The HM-6564-8 is a 64K bit CMOS RAM. It consists of 16 HM-6504 4K x 1 CMOS RAMs, in leadless carriers, mounted on a ceramic substrate. The HM-6564-8 is configured as an extra wide, standard length 40 pin DIP. The memory appears to the system as an array of 16 4K x 1 static RAMs. The array is organized as two 8K by 4 blocks of RAM sharing only the address bus. The data inputs, data outputs, chip enables and write enables are separate for each block of RAM. This allows the user to organize the HM-6564-8 RAM as either an 8K by 8 or a 16K by 4 array.

This 64K memory provides a unique blend of low power CMOS semiconductor technology and advanced packaging techniques. The HM-6564-8 is intended for use in any application where a large amount of RAM is needed, and where power consumption and board space are prime concerns. The guaranteed low voltage data retention characteristics allow easy implementation of non-volatile read/write memory by using very small batteries mounted directly on the memory circuit board. Example applications include digital avionic instrumentation, remote data acquisition, and portable or hand held digital communications devices.

Pinout

TOP VIEW

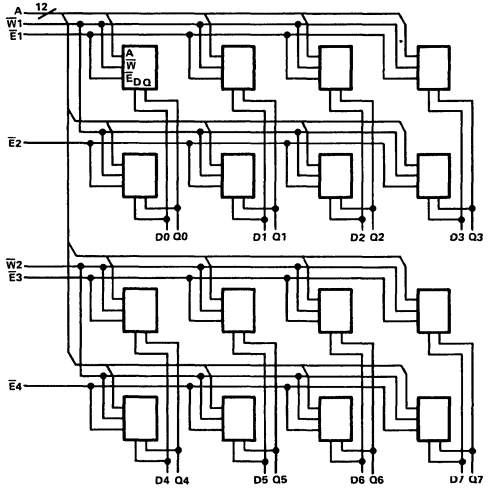


* NOTES:

Pins 20 and 40 (VCC) are internally connected. Similarly pins 1 and 21 (Ground) are connected. The user is advised to connect all four VCC pins and Ground pins to his board busses. This will improve power distribution across the array and will enhance decoupling.

Pin 10 is internally connected to pin 11, and pin 30 is connected to pin 31.

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature ..... -65°C to +150°C
Gate Count 112000
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten Seconds) ..... +300°C

CAUTION: Stresses above those listed in the Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Rise and Fall Time ..... 40ns Maximum
Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6564-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	800	µA	IO = 0, VI = VCC or GND
ICCOP1	Operating Supply Current (8K x 8) (Note 3)	-	56	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND
ICCOP2	Operating Supply Current (16K x 4) (Notes 2, 3)	-	28	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND
ICCDR	Data Retention Supply Current	-	400	µA	IO = 0, VCC = 2.0, VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0	-	V	
IIA	Address Input Leakage	-20	+20	µA	VI = VCC or GND
IID1	Data Input Leakage (8K x 8)	-3	+3	µA	VI = VCC or GND
IID2	Data Input Leakage (16K x 4) (Note 2)	-5	+5	µA	VI = VCC or GND
IIE1	Enable Input Leakage (8K x 8)	-10	+10	µA	VI = VCC or GND
IIE2	Enable Input Leakage (16K x 4) (Note 2)	-5	+5	µA	VI = VCC or GND
IIW	Write Enable Input Leakage (Each)	-10	+10	µA	VI = VCC or GND
IOZ1	Output Leakage (8K x 8)	-5	+5	µA	VO = VCC or GND
IOZ2	Output Leakage (16K x 4) (Note 2)	-10	+10	µA	VO = VCC or GND
VIL	Input Low Voltage	0	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC	V	
VOL	Output Low Voltage	-	0.4	V	IO = 2.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA
CIA	Address Input Capacitance (Note 2)	-	200	pF	f = 1MHz, VI = VCC or GND
CID1	Data Input Capacitance (8K x 8) (Note 2)	-	50	pF	f = 1MHz, VI = VCC or GND
CID2	Data Input Capacitance (16K x 4) (Note 2)	-	100	pF	f = 1MHz, VI = VCC or GND
CIE1	Enable Input Capacitance (8K x 8) (Note 2)	-	160	pF	f = 1MHz, VI = VCC or GND
CIE2	Enable Input Capacitance (16K x 4) (Note 2)	-	80	pF	f = 1MHz, VI = VCC or GND
CIW	Write Enable Input Capacitance (Each) (Note 2)	-	100	pF	f = 1MHz, VI = VCC or GND
CO1	Output Capacitance (8K x 8) (Note 2)	-	50	pF	f = 1MHz, VO = VCC or GND
CO2	Output Capacitance (16K x 4) (Note 2)	-	100	pF	f = 1MHz, VO = VCC or GND

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns max; Input and output timing reference level: 1.5V; Output load: 1TTL gate equivalent and CL = 50pF (Min) for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. ICCOP is proportional to operating frequency.
4. VCC = 4.5V and 5.5V

A.C. Electrical Specifications (Note 1) VCC = 5V ± 10%, TA = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access	-	350	ns	(Notes 1, 4)
(2)TAVQV	Address Access (TAVQV = TELQV + TAVEL)	-	400	ns	(Notes 1, 4)
(3)TELQX	Output Enable	5	-	ns	(Notes 2, 4)
(4)TEHQZ	Output Disable	-	120	ns	(Notes 2, 4)
(5)TELEL	Read or Write Cycle	480	-	ns	(Notes 1, 4)
(6)TELEH	Chip Enable Low	350	-	ns	(Notes 1, 4)
(7)TEHEL	Chip Enable High	130	-	ns	(Notes 1, 4)
(8)TAVEL	Address Setup	50	-	ns	(Notes 1, 4)
(9)TELAX	Address Hold	50	-	ns	(Notes 1, 4)
(10)TWLWH	Write Enable Low	150	-	ns	(Notes 1, 4)
(11)TWLEH	Write Enable Setup	250	-	ns	(Notes 1, 4)
(12)TWLEL	Early Write Setup (Write Mode)	10	-	ns	(Notes 1, 4)
(13)TELWH	Early Write Hold (Write Mode)	100	-	ns	(Notes 1, 4)
(14)TDVWL	Data Setup	10	-	ns	(Notes 1, 4)
(15)TDVEL	Early Write Data Setup	10	-	ns	(Notes 1, 4)
(16)TWLDX	Data Hold	100	-	ns	(Notes 1, 4)
(17)TELDX	Early Write Data Hold	100	-	ns	(Notes 1, 4)

NOTES: 1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns max; Input and output timing reference level: 1.5V; Output load: 1TTL gate equivalent and CL = 50pF (Min) for CL greater than 50pF, access time is derated by 0.15ns per pF.

2. Tested at initial design and after major design changes.

3. ICCOP is proportional to frequency.

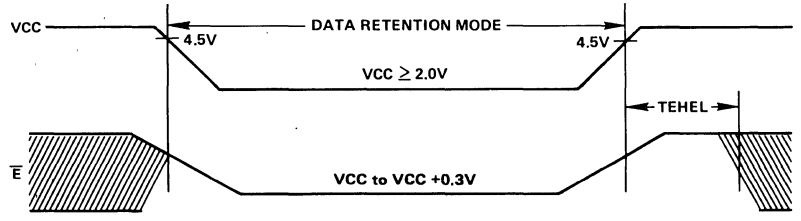
4. VCC = 4.5V and 5.5V

Low Voltage Data Retention

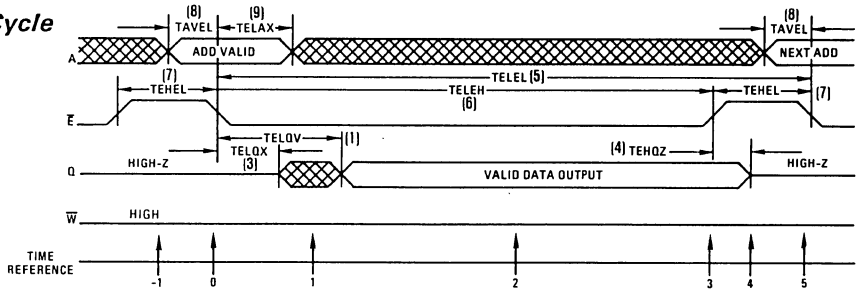
HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC +0.3V to VCC.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are held high (e.g. $\overline{E}$) must be kept between VCC +0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



Read Cycle

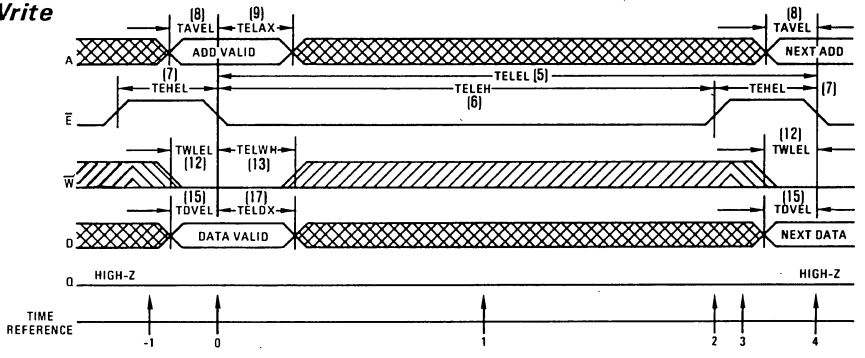


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↓	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↑	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

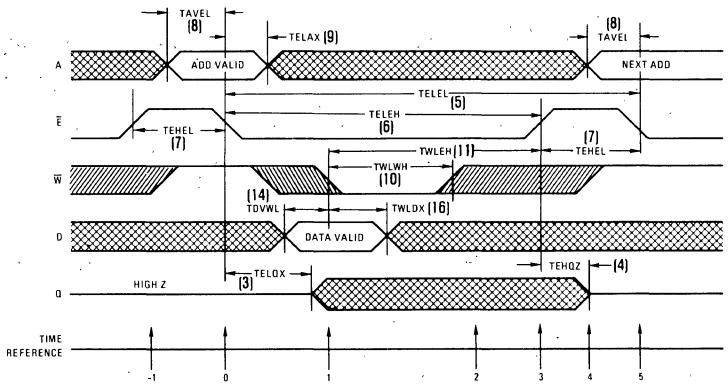


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	L	V	V	Z	Cycle Begins, Addresses are Latched
1	L	X	X	X	Z	Write in Progress Internally
2	↑	X	X	X	Z	Write Complete
3	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
4	↓	L	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for the cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Late Write Cycle



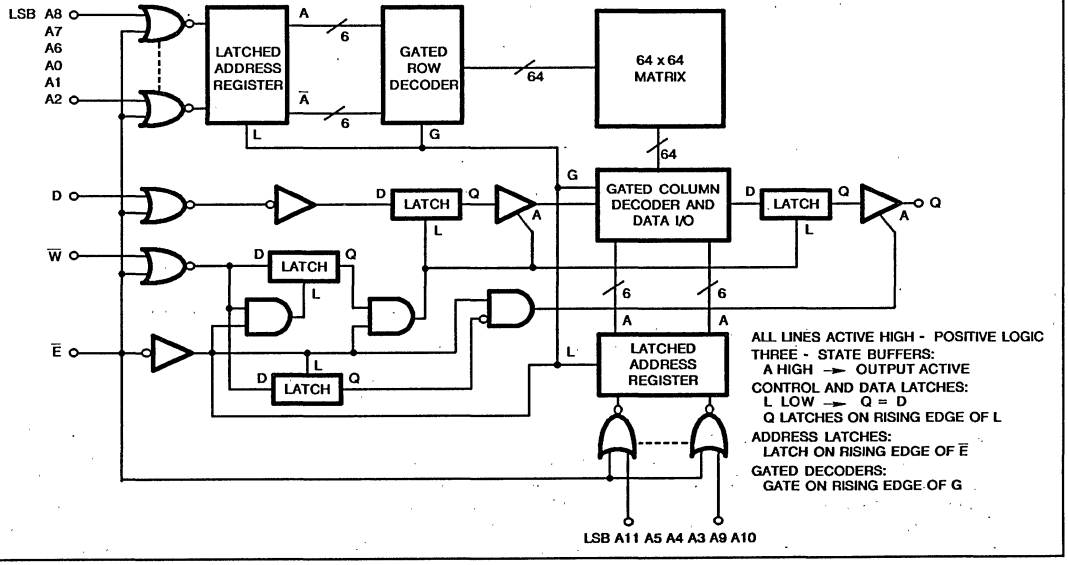
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	↓	X	V	X	Write Begins, Data is Latched
2	L	H	X	X	X	Write in Progress Internally
3	↑	H	X	X	X	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle. Recall that in the early write the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data set up, data hold, write setup and write pulse widths are observed.

NOTES: In the above descriptions the numbers in parenthesis (T = n) refers to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

HM-6504 (One of Sixteen)



Organization Guide

To Organize 8K x 8:

Connect:	$\overline{E1}$ with $\overline{E3}$	(Pins 9 + 32)
	$\overline{E2}$ with $\overline{E4}$	(Pins 12 + 29)
	$\overline{W1}$ with $\overline{W2}$	(Pins 11 + 31)

To Organize 16K x 4:

Connect:	Q0 with Q4	(Pins 2 + 39)
	D0 with D4	(Pins 3 + 38)
	Q1 with Q5	(Pins 4 + 37)
	D1 with D5	(Pins 5 + 36)
	D2 with D6	(Pins 16 + 25)
	Q2 with Q6	(Pins 17 + 24)
	D3 with D7	(Pins 18 + 23)
	$\overline{Q3}$ with Q7	(Pins 19 + 22)
Optional	$\overline{W1}$ may be common with $\overline{W2}$	(Pins 11 + 31)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 8K x 8 mode, use the chip enables as if there were only two, $\overline{E1}$ and $\overline{E2}$. In the 16K x 4 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoid.

Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HM-6564 have conductive lids. These lids are electrically floating, not connected to VCC or GND. The designer should be aware of the possiblity that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Board Size Tradeoffs

Printed circuit board real estate is a costly commodity. Actual board costs depend on layout tolerances, density, complexity, number of layers, choice of board material, and other factors.

The following table compares board space for 16 standard DIP 4K RAMs to the HM-6564 RAM array. Both fine line, close tolerance layout and standard "easy" layout board sizes are shown in the comparison.

64K ARRAY OR 16 4K RAMs ON A PC BOARD vs. THE HM-6564

PACKAGE	CIRCUIT SUBSTRATE	SIZE
18 Pin DIP	Standard Two Sided PCB	12 to 15 square inches
18 Pin DIP	Fine Line or Multilayer PCB	9 to 11 square inches
18 Pin Leadless Carrier	Multilayer Alumina Substrate	3 to 5 square inches
HM-6564	Two Sided Mounting Multilayer Alumina Substrate	2 square inches

The cost of semiconductor circuits decline with time. If actual costs were included, they would be out of date in a very short time. We urge you to contact your local Harris office of sales representative for accurate pricing allowing cost tradeoff analysis. In your cost analysis, also consider the advantages of a lighter, smaller overall package for your system. Consider how much more valuable your system will be when the memory array size is decreased to about 1/6 of normal size.

HARRIS

HM-8808-8
HM-8808A-8

8K x 8 Asynchronous CMOS Static RAM Module

June 1989

Features

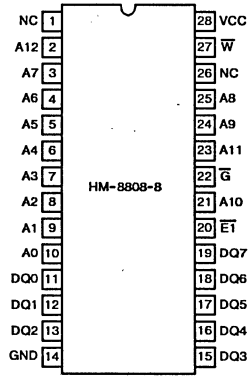
- Full CMOS Design
- 6 Transistor Memory Cell
- Low Standby Current 250/900µA
- Low Operating Current 70mA
- Fast Address Access Time 100/120/150ns
- CMOS/TTL Compatible Inputs/Outputs
- JEDEC Approved Pinout
- Equal Cycle and Access Time
- No Clocks or Strobes Required
- Single 5 Volt Supply
- Gated Inputs - No Pull-Up or Pull-Down Resistors Required
- Temperature Range ..... -55°C to +125°C
- Easy Microprocessor Interfacing
- Dual Chip Enable Control (HM-8808A)

Description

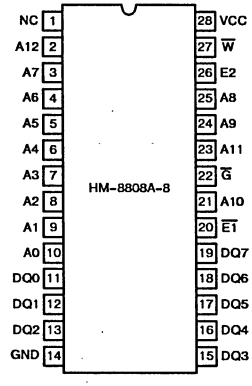
The HM-8808-8 and HM-8808A-8 are 8K x 8 Asynchronous CMOS Static RAM Modules, based on multi-layered, co-fired, dual-in-line substrates. Mounted on each substrate are four HM-65162 2K x 8 CMOS SRAMs, a high speed CMOS decoder, and a ceramic decoupling capacitor, all packaged in leadless chip carriers. The capacitor is added to reduce noise and the need for external decoupling. The HM-65162 RAMs used in these modules are full CMOS devices, utilizing arrays of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor devices. The HM-8808-8 and HM-8808A-8 have gated inputs to simplify system design for optimum standby supply current. The pinouts of these modules conform to the JEDEC 28 pin 8 bit wide standard, which is compatible with a variety of industry standard memories. The HM-8808A-8 is pin-compatible with many standard 8K x 8 RAMs, adding the advantage of high performance over the full military temperature range. Also, because of the second chip enable (E2), the HM-8808A-8 simplifies the design of low-power battery back-up memory systems.

Pinouts

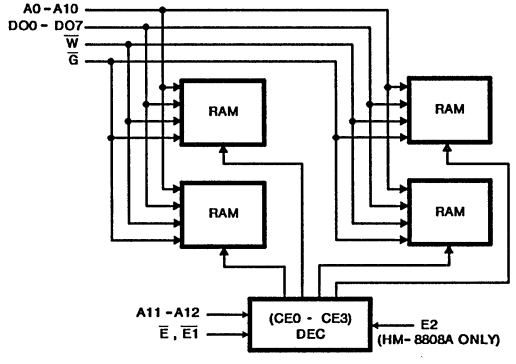
TOP VIEW



TOP VIEW



Functional Diagram



PIN DESCRIPTION

PIN	DESCRIPTION
A	Address Input
DQ	Data Input/Output
$\overline{E}$	Chip Enable (HM-8808-8)
$\overline{E1}$	Chip Enable (HM-8808A-8)
E2	Chip Enable (HM-8808A-8)
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable

SELECTION GUIDE

PART NUMBER	TELQV	ICCSB
HM-8808S-8/HM-8808AS-8	100ns	250µA
HM-8808B-8/HM-8808AB-8	120ns	250µA
HM-8808-8/HM-8808A-8	150ns	900µA

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage 7.0V
Input or Output Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Gate Count 105000
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten seconds) ..... +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Input Rise and Fall Time ..... 40ns Max
Operating Supply Voltage ..... 4.5V to 5.5V
Operating Temperature ..... -55°C to +125°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	-	250	µA	IO = 0, $\overline{E}$ = VCC-0.3V (Note 7), E2 = 0.3V (Note 8)
ICCSB	Standby Supply Current (TTL)	-	35	mA	IO = 0, $\overline{E}$ = VIH (Note 7), E2 = VIL (Note 8)
ICCEN	Enabled Supply Current	-	60	mA	IO = 0, $\overline{E}$ = VIL (Note 7), E2 = VIH (Note 8)
ICCOP	Operating Supply Current	-	70	mA	IO = 0, f = 1MHz, $\overline{E}$ = VIL (Note 7), E2 = VIH (Notes 8, 2)
ICCDR	Data Retention Supply Current	-	125	µA	VCC = 2.0V, $\overline{E}$ = VCC-0.3V (Note 7), E2 = 0.3V (Note 8)
II	Input Leakage Current	-1.0	+1.0	µA	VI = GND or VCC
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = GND or VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	VCC = 2.0V, $\overline{E}$ = VCC (Note 7), E2 = GND (Note 8)
VOL	Output Low Voltage	-	0.4	V	IO = 4.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage	VCC-0.4	-	V	IO = -100µA (Note 3)
VIL	Input Low Voltage	0	0.8	V	
VIH	Input High Voltage	2.4	VCC	V	

Capacitance (Note 3)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
CE	Enable Input Capacitance	-	15	pF	VE = VCC or GND, f = 1MHz (Note 3)
CW	Write Enable Capacitance	-	48	pF	VW = VCC or GND, f = 1MHz (Note 3)
CI	Input Capacitance: $\overline{G}$, A	-	35	pF	VI = VCC or GND, f = 1MHz (Note 3)
CIO	Input/Output Capacitance	-	43	pF	VIO = VCC or GND, f = 1MHz (Note 3)

NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Guaranteed but not tested.
4. Input pulse levels: VIL = 0.0V, VIH = 3.0V
   Input rise and fall times: 5ns (max.) VCC = 4.5V and 5.5V.
   Input and output timing reference levels: 1.5V
   Output load: 1 TTL gate equivalent and 50pF (min, including scope and jig).
5. "EL" (enable input valid) equivalent to:
   EL on the HM-8808-8. EIL and E2H on the HM-8808A-8.
6. "EH" (enable input invalid) equivalent to:
   EH on the HM-8808-8. EIH or E2L on the HM-8808A-8.
7. Relevant to the HM-8808-8 only.
8. Relevant to the HM-8808A-8 only.

A.C. Electrical Specifications $V_{CC} = 5V \pm 10\%$; $T_A = -55^oC$ to $+125^oC$

NO.	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE						
(1)	TAVAX	Read Cycle Time	100	-	ns	
(2)	TAVQV	Address Access Time	-	100	ns	
(3)	TELQV	Chip Enable Access Time	-	100	ns	(Note 5)
(4)	TGLQV	Output Enable Access Time	-	50	ns	
(5)	TELQX	Chip Enable Output Enable Time	20	-	ns	(Notes 3, 5)
(6)	TGLQX	Output Enable Output Enable Time	5	-	ns	(Note 3)
(7)	TAXQX	Address Output Hold Time	5	-	ns	
(8)	TEHQZ	Chip Disable Output Disable Time	0	60	ns	(Notes 3, 6)
(9)	TGHQZ	Output Disable Time	0	40	ns	(Note 3)
WRITE CYCLE						
(10)	TAVAX	Write Cycle Time	100	-	ns	
(11)	TELWH	Chip Enable to End of Write	70	-	ns	(Note 5)
(12)	TWLWH	Write Enable Pulse Width	40	-	ns	
(13)	TELEH	Enable Pulse Width (Early Write)	40	-	ns	(Notes 3, 5, 6)
(14)	TAVWL	Address Setup Time (Late Write)	15	-	ns	
(15)	TAVEL	Address Setup Time (Early Write)	0	-	ns	(Notes 3, 5)
(16)	TWHAX	Address Hold Time (Late Write)	10	-	ns	
(17)	TEHAX	Address Hold Time (Early Write)	30	-	ns	(Note 3)
(18)	TDVWH	Data Setup Time (Late Write)	30	-	ns	
(19)	TDVEH	Data Setup Time (Early Write)	30	-	ns	(Note 6)
(20)	TWHDX	Data Hold Time (Late Write)	10	-	ns	
(21)	TEHDX	Data Hold Time (Early Write)	30	-	ns	(Notes 3, 6)
(22)	TWLEH	Write Enable Pulse Setup Time	40	-	ns	(Note 6)
(23)	TWLQZ	Write Enable Output Disable Time	-	40	ns	(Note 3)
(24)	TWHQX	Write Disable Output Enable Time	0	-	ns	(Note 3)

NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Guaranteed but not tested.
4. Input pulse levels: VIL = 0.0V, VIH = 3.0V
   Input rise and fall times: 5ns (max.) VCC = 4.5V and 5.5V.
   Input and output timing reference levels: 1.5V
   Output load: 1 TTL gate equivalent and 50pF (min, including scope and jig).
5. "EL" (enable input valid) equivalent to:
   EL on the HM-8808-8. EIL and E2H on the HM-8808A-8.
6. "EH" (enable input invalid) equivalent to:
   EH on the HM-8808-8. EIH or E2L on the HM-8808A-8.
7. Relevant to the HM-8808-8 only.
8. Relevant to the HM-8808A-8 only.

Absolute Maximum Ratings

Supply Voltage 7.0V
Input or Output Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Gate Count 105000
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten seconds) ..... +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Input Rise and Fall Time ..... 40ns Max
Operating Supply Voltage ..... 4.5V to 5.5V
Operating Temperature ..... -55°C to +125°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	-	250	µA	IO = 0, $\overline{E}$ = VCC-0.3V (Note 7), E2 = 0.3V (Note 8)
ICCSB	Standby Supply Current (TTL)	-	35	mA	IO = 0, $\overline{E}$ = VIH (Note 7), E2 = VIL (Note 8)
ICCEN	Enabled Supply Current	-	60	mA	IO = 0, $\overline{E}$ = VIL (Note 7), E2 = VIH (Note 8)
ICCOP	Operating Supply Current	-	70	mA	IO = 0, f = 1MHz, $\overline{E}$ = VIL (Note 7), E2 = VIH (Notes 8, 2)
ICCDR	Data Retention Supply Current	-	125	µA	VCC = 2.0V, $\overline{E}$ = VCC-0.3V (Note 7), E2 = 0.3V (Note 8)
II	Input Leakage Current	-1.0	+1.0	µA	VI = GND or VCC
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = GND or VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	VCC = 2.0V, $\overline{E}$ = VCC (Note 7), E2 = GND (Note 8)
VOL	Output Low Voltage	-	0.4	V	IO = 4.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage	VCC-0.4	-	V	IO = -100µA (Note 3)
VIL	Input Low Voltage	0	0.8	V	
VIH	Input High Voltage	2.4	VCC	V	

Capacitance (Note 3)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
CE	Enable Input Capacitance	-	15	pF	VE = VCC or GND, f = 1MHz (Note 3)
CW	Write Enable Capacitance	-	48	pF	VW = VCC or GND, f = 1MHz (Note 3)
CI	Input Capacitance: $\overline{G}$, A	-	35	pF	VI = VCC or GND, f = 1MHz (Note 3)
CIO	Input/Output Capacitance	-	43	pF	VIO = VCC or GND, f = 1MHz (Note 3)

NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Guaranteed but not tested.
4. Input pulse levels: VIL = 0.0V, VIH = 3.0V
   Input rise and fall times: 5ns (max.) VCC = 4.5V and 5.5V.
   Input and output timing reference levels: 1.5V
   Output load: 1 TTL gate equivalent and 50pF (min, including scope and jig).
5. "EL" (enable input valid) equivalent to:
   EL on the HM-8808-8. EIL and E2H on the HM-8808A-8.
6. "EH" (enable input invalid) equivalent to:
   EH on the HM-8808-8. EIH or E2L on the HM-8808A-8.
7. Relevant to the HM-8808-8 only.
8. Relevant to the HM-8808A-8 only.

A.C. Electrical Specifications V_{CC} = 5V ± 10%; T_A = -55°C to +125°C

NO.	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE						
(1)	TAVAX	Read Cycle Time	120	-	ns	
(2)	TAVQV	Address Access Time	-	120	ns	
(3)	TELQV	Chip Enable Access Time	-	120	ns	(Note 5)
(4)	TGLQV	Output Enable Access Time	-	65	ns	
(5)	TELQX	Chip Enable Output Enable Time	20	-	ns	(Notes 3, 5)
(6)	TGLQX	Output Enable Output Enable Time	5	-	ns	(Note 3)
(7)	TAXQX	Address Output Hold Time	5	-	ns	
(8)	TEHQZ	Chip Disable Output Disable Time	0	70	ns	(Notes 3, 6)
(9)	TGHQZ	Output Disable Time	0	40	ns	(Note 3)
WRITE CYCLE						
(10)	TAVAX	Write Cycle Time	120	-	ns	
(11)	TELWH	Chip Enable to End of Write	80	-	ns	(Note 5)
(12)	TWLWH	Write Enable Pulse Width	55	-	ns	
(13)	TELEH	Enable Pulse Width (Early Write)	60	-	ns	(Notes 3, 5, 6)
(14)	TAVWL	Address Setup Time (Late Write)	15	-	ns	
(15)	TAVEL	Address Setup Time (Early Write)	0	-	ns	(Notes 3, 5)
(16)	TWHAX	Address Hold Time (Late Write)	10	-	ns	
(17)	TEHAX	Address Hold Time (Early Write)	30	-	ns	(Note 3)
(18)	TDVWH	Data Setup Time (Late Write)	30	-	ns	
(19)	TDVEH	Data Setup Time (Early Write)	30	-	ns	(Note 6)
(20)	TWHDX	Data Hold Time (Late Write)	15	-	ns	
(21)	TEHDX	Data Hold Time (Early Write)	30	-	ns	(Notes 3, 6)
(22)	TWLEH	Write Enable Pulse Setup Time	55	-	ns	(Note 6)
(23)	TWLQZ	Write Enable Output Disable Time	-	40	ns	(Note 3)
(24)	TWHQX	Write Disable Output Enable Time	0	-	ns	(Note 3)

NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Guaranteed but not tested.
4. Input pulse levels: VIL = 0.0V, VIH = 3.0V
   Input rise and fall times: 5ns (max.) VCC = 4.5V and 5.5V.
   Input and output timing reference levels: 1.5V
   Output load: 1 TTL gate equivalent and 50pF (min, including scope and jig).
5. "EL" (enable input valid) equivalent to:
   EL on the HM-8808-8. EIL and E2H on the HM-8808A-8.
6. "EH" (enable input invalid) equivalent to:
   EH on the HM-8808-8. EIH or E2L on the HM-8808A-8.
7. Relevant to the HM-8808-8 only.
8. Relevant to the HM-8808A-8 only.

Absolute Maximum Ratings

Supply Voltage 7.0V
Input or Output Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Gate Count 105000
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten seconds) ..... +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Input Rise and Fall Time ..... 40ns Max
Operating Supply Voltage ..... 4.5V to 5.5V
Operating Temperature ..... -55°C to +125°C

D.C. Electrical Specifications $V_{CC} = 5V \pm 10\%$; $T_A = -55°C$ to $+125°C$

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	-	900	µA	IO = 0, $\overline{E}$ = VCC-0.3V (Note 7), E2 = 0.3V (Note 8)
ICCSB	Standby Supply Current (TTL)	-	35	mA	IO = 0, $\overline{E}$ = VIH (Note 7), E2 = VIL (Note 8)
ICCEN	Enabled Supply Current	-	70	mA	IO = 0, $\overline{E}$ = VIL (Note 7), E2 = VIH (Note 8)
ICCOP	Operating Supply Current	-	70	mA	IO = 0, f = 1MHz, $\overline{E}$ = VIL (Note 7), E2 = VIH (Notes 8, 2)
ICCDR	Data Retention Supply Current	-	400	µA	VCC = 2.0V, $\overline{E}$ = VCC-0.3V (Note 7), E2 = 0.3V (Note 8)
II	Input Leakage Current	-5.0	+5.0	µA	VI = GND or VCC
IIOZ	Input/Output Leakage Current	-5.0	+5.0	µA	VIO = GND or VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	VCC = 2.0V, $\overline{E}$ = VCC (Note 7), E2 = GND (Note 8)
VOL	Output Low Voltage	-	0.4	V	IO = 4.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage	VCC-0.4	-	V	IO = -100µA (Note 3)
VIL	Input Low Voltage	0	0.8	V	
VIH	Input High Voltage	2.4	VCC	V	

Capacitance (Note 3)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
CE	Enable Input Capacitance	-	15	pF	VE = VCC or GND, f = 1MHz (Note 3)
CW	Write Enable Capacitance	-	48	pF	VW = VCC or GND, f = 1MHz (Note 3)
CI	Input Capacitance: $\overline{G}$, A	-	35	pF	VI = VCC or GND, f = 1MHz (Note 3)
CIO	Input/Output Capacitance	-	43	pF	VIO = VCC or GND, f = 1MHz (Note 3)

NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Guaranteed but not tested.
4. Input pulse levels: VIL = 0.0V, VIH = 3.0V
   Input rise and fall times: 5ns (max.) VCC = 4.5V and 5.5V.
   Input and output timing reference levels: 1.5V
   Output load: 1 TTL gate equivalent and 50pF (min, including scope and jig).
5. "EL" (enable input valid) equivalent to:
   EL on the HM-8808-8. EIL and E2H on the HM-8808A-8.
6. "EH" (enable input invalid) equivalent to:
   EH on the HM-8808-8. EIH or E2L on the HM-8808A-8.
7. Relevant to the HM-8808-8 only.
8. Relevant to the HM-8808A-8 only.

A.C. Electrical Specifications V_{CC} = 5V ± 10%; T_A = -55°C to +125°C

NO.	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE						
(1)	TAVAX	Read Cycle Time	150	-	ns	
(2)	TAVQV	Address Access Time	-	150	ns	
(3)	TELQV	Chip Enable Access Time	-	150	ns	(Note 5)
(4)	TGLQV	Output Enable Access Time	-	65	ns	
(5)	TELQX	Chip Enable Output Enable Time	25	-	ns	(Notes 3, 5)
(6)	TGLQX	Output Enable Output Enable Time	5	-	ns	(Note 3)
(7)	TAXQX	Address Output Hold Time	5	-	ns	
(8)	TEHQZ	Chip Disable Output Disable Time	0	80	ns	(Notes 3, 6)
(9)	TGHQZ	Output Disable Time	0	50	ns	(Note 3)
WRITE CYCLE						
(10)	TAVAX	Write Cycle Time	150	-	ns	
(11)	TELWH	Chip Enable to End of Write	90	-	ns	(Note 5)
(12)	TWLWH	Write Enable Pulse Width	65	-	ns	
(13)	TELEH	Enable Pulse Width (Early Write)	65	-	ns	(Notes 3, 5, 6)
(14)	TAVWL	Address Setup Time (Late Write)	20	-	ns	
(15)	TAVEL	Address Setup Time (Early Write)	5	-	ns	(Notes 3, 5)
(16)	TWHAX	Address Hold Time (Late Write)	20	-	ns	
(17)	TEHAX	Address Hold Time (Early Write)	45	-	ns	(Note 3)
(18)	TDVWH	Data Setup Time (Late Write)	35	-	ns	
(19)	TDVEH	Data Setup Time (Early Write)	35	-	ns	(Note 6)
(20)	TWHDX	Data Hold Time (Late Write)	20	-	ns	
(21)	TEHDX	Data Hold Time (Early Write)	45	-	ns	(Notes 3, 6)
(22)	TWLEH	Write Enable Pulse Setup Time	65	-	ns	(Note 6)
(23)	TWLQZ	Write Enable Output Disable Time	-	50	ns	(Note 3)
(24)	TWHQX	Write Disable Output Enable Time	0	-	ns	(Note 3)

NOTES: 1. All devices tested at worst case temperature and supply voltage limits.

2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.

3. Guaranteed but not tested.

4. Input pulse levels: VIL = 0.0V, VIH = 3.0V
Input rise and fall times: 5ns (max.) VCC = 4.5V and 5.5V.
Input and output timing reference levels: 1.5V
Output load: 1 TTL gate equivalent and 50pF (min, including scope and jig).

5. "EL" (enable input valid) equivalent to:
EL on the HM-8808-8. EIL and E2H on the HM-8808A-8.

6. "EH" (enable input invalid) equivalent to:
EH on the HM-8808-8. EIH or E2L on the HM-8808A-8.

7. Relevant to the HM-8808-8 only.

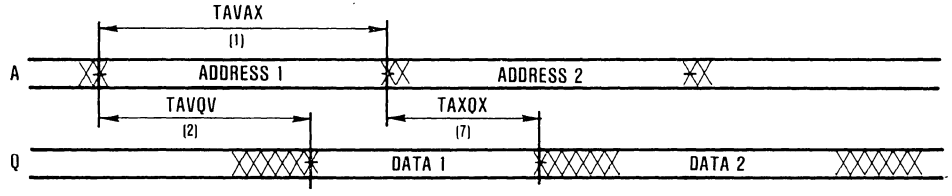
8. Relevant to the HM-8808A-8 only.

Truth Table

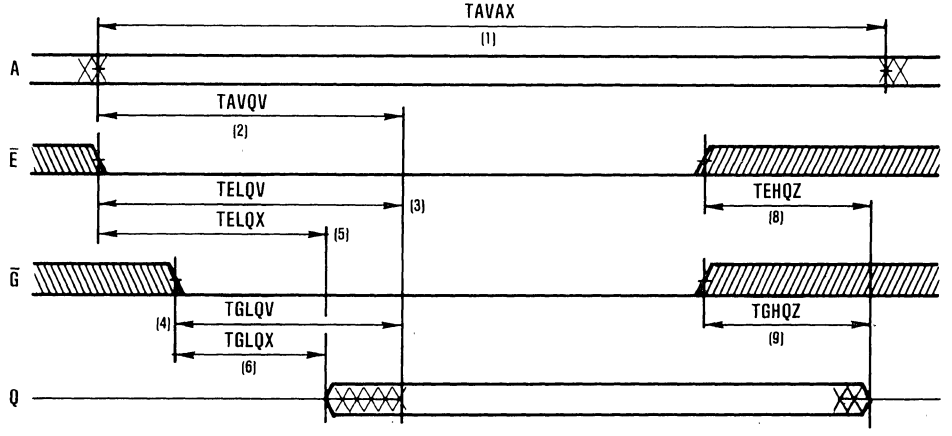
MODE	HM-8808	HM-8808A		HM-8808/8808A	
	$\overline{E}$	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$
Standby (CMOS)	VCC	X	GND	X	X
Standby (TTL)	VIH	VIH	VIL	X	X
Enabled (High Z)	VIL	VIL	VIH	VIH	VIH
Write	VIL	VIL	VIH	VIL	X
Read	VIL	VIL	VIH	VIH	VIL

HM-8808 Timing Diagram

READ CYCLE 1 (Notes 1, 2)



READ CYCLE 2 (Note 1)

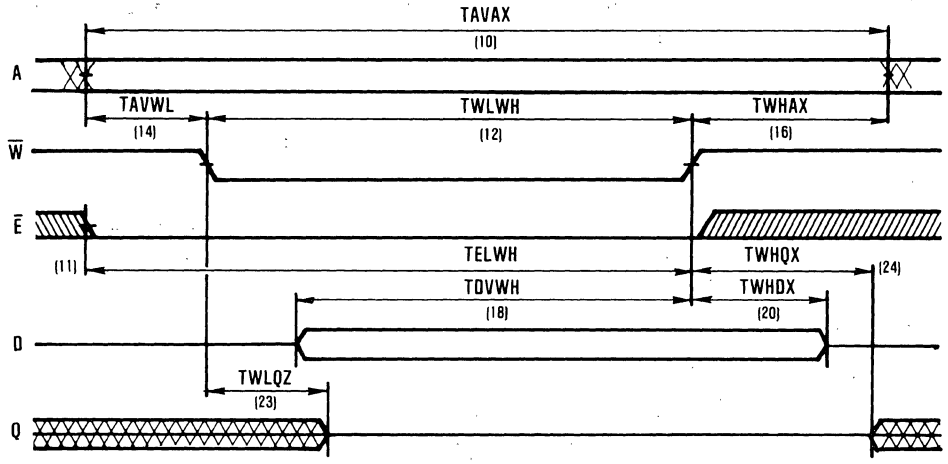


NOTES: 1. In a read cycle, $\overline{W}$ is held high.

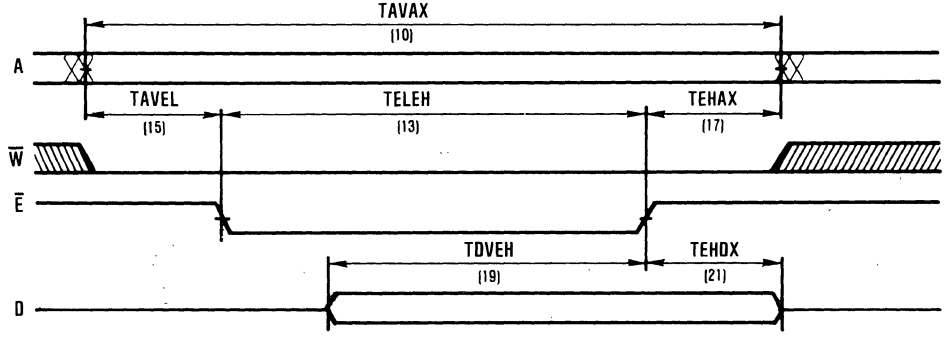
2. In read cycle 1, the module is kept continuously enabled. $\overline{G}$, and $\overline{E}$ are held at VIL.

HM-8808 Timing Diagrams (Continued)

WRITE CYCLE 1 (Notes 1, 3, 4)



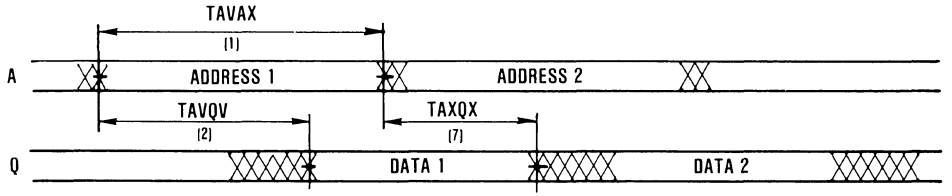
WRITE CYCLE 2 (Notes 2, 4)



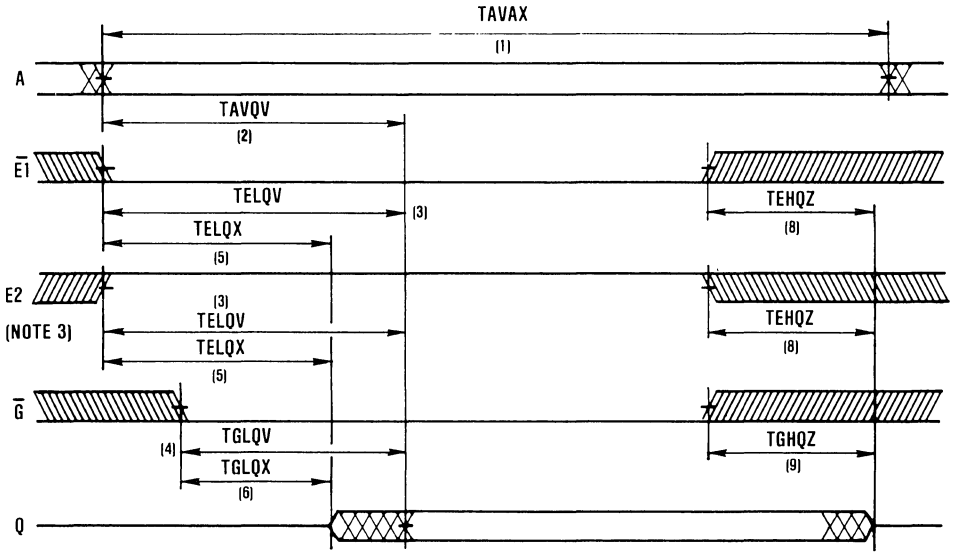
NOTES:
1. In Write Cycle 1, the module is first enabled and then data is strobed into the RAM with a pulse on Write Enable ($\overline{W}$). Because $\overline{W}$ becomes valid after the part is enabled, this is sometimes referred to as a "Late Write" cycle.
2. In Write Cycle 2 , Address (A) and Write Enable ($\overline{W}$) are first set up, and then data is strobed into the RAM with a pulse on $\overline{E}$. Because $\overline{W}$ is valid before the module is enabled, this is sometimes referred to as an "Early Write" cycle.
3. Output Enable ($\overline{G}$) is normally held stable throughout the entire cycle. If $\overline{G}$ is held high, then the outputs (Q) remain in the high impedance state. If $\overline{G}$ is held low, then it may be necessary to lengthen the cycle to prevent bus contention. This would occur if TWLQZ and TDVWH overlapped.
4. Data Inputs (D) and Data Outputs (Q) are connected internally at the DQ pins.

HM-8808A Timing Diagrams

READ CYCLE 1 (Note 1, 2)



READ CYCLE 2 (Note 1)



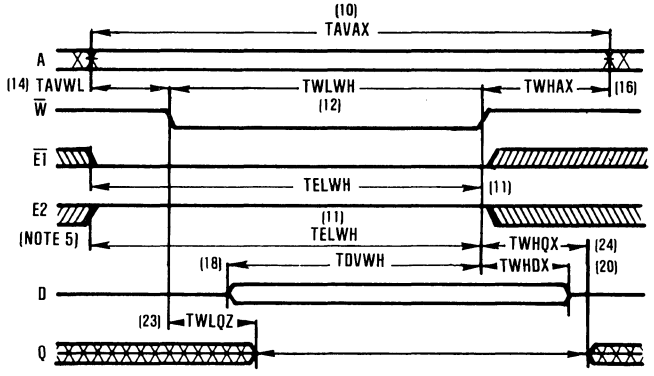
NOTES: 1. In a read cycle, $\overline{W}$ is held high.

2. In read cycle 2, the module is kept continuously enabled: $\overline{G}$ and $\overline{E1}$ are held at VIL. E2 is held at VIH.

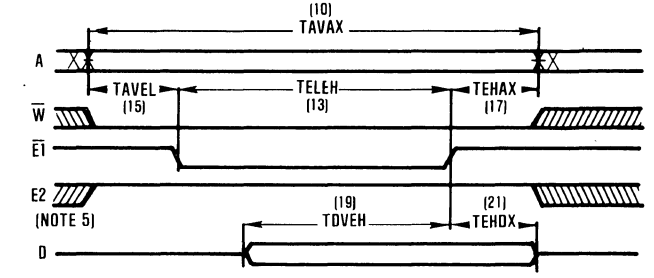
3. The AC timing of E2 is the same as that of $\overline{E1}$. Only the polarity is reversed. While $\overline{E1}$ is active low, E2 is active high. Therefore AC parameters that refer to the falling edge of enable, such as TELQV, can be applied to the rising edge of E2, and parameters that refer to the rising edge of enable, such as TEHQZ, can be applied to the falling edge of E2.

HM-8808A Timing Diagrams (Continued)

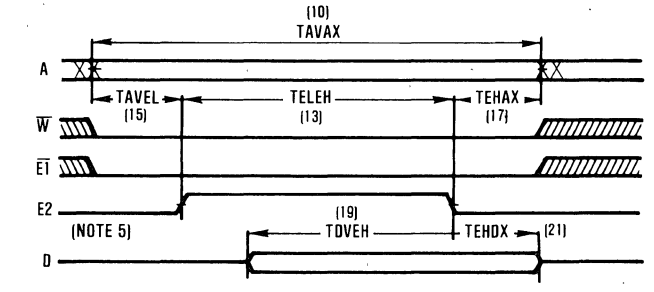
WRITE CYCLE 1: Controlled by $\overline{W}$ (Notes 1, 3, 4)



WRITE CYCLE 2: Controlled by $\overline{E1}$ (Notes 2, 4)



WRITE CYCLE 3: Controlled by E2 (Notes 2, 4)



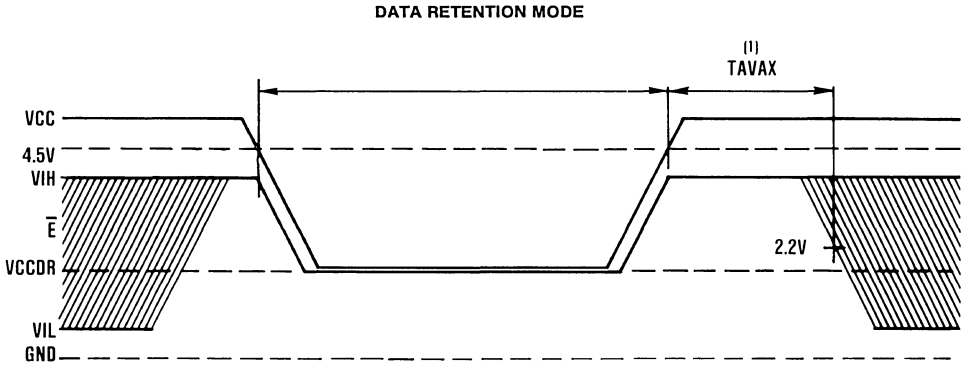
NOTES:
1. In Write Cycle 1, the module is first enabled and then data is strobed into the RAM with a pulse on Write Enable ($\overline{W}$). Because $\overline{W}$ becomes valid after the part is enabled, this is sometimes referred to as a "Late Write" cycle.
2. In Write Cycle 2 and 3, Address (A) and Write Enable ($\overline{W}$) are first set up, and then data is strobed into the RAM with a pulse on $\overline{E1}$ or E2. Because $\overline{W}$ is valid before the module is enabled, this is sometimes referred to as an "Early Write" cycle.
3. Output Enable ($\overline{G}$) is normally held stable throughout the entire cycle. If $\overline{G}$ is held high, then the outputs (Q) remain in the high impedance state. If $\overline{G}$ is held low, then it may be necessary to lengthen the cycle to prevent bus contention. This would occur if TWLQZ and TDVWH overlapped.
4. Data Inputs (D) and Data Outputs (Q) are connected internally at the DQ pins.
5. The AC timing of E2 is the same as that of $\overline{E1}$. Only the polarity is reversed. While $\overline{E1}$ is active low, E2 is active high. Therefore AC parameters that refer to the falling edge of enable, such as TELQV, can be applied to the rising edge of E2, and parameters that refer to the rising edge of enable, such as TEHQZ, can be applied to the falling edge of E2.

Low Voltage Data Retention

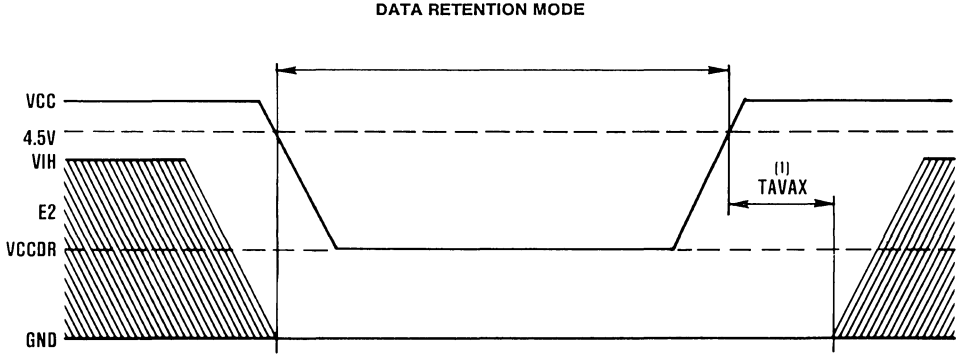
Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. The module must be kept disabled during data retention. The Chip Enable ($\overline{E}$) on the HM-8808 must be held between VCC-0.3V and VCC+0.3V. Chip Enable 2 (E2) on the HM-8808A must be held between -0.3V and GND +0.3V.
2. During power-up and power-down transitions, $\overline{E}$ (HM-8808) must be held between 90% of VCC and VCC +0.3V; E2 (HM-8808A) must be held above -0.3V and below 10% of VCC.
3. The RAM module can begin operation one TAVAX after VCC reaches the minimum operating voltage (4.5V).

HM-8808 Data Retention Timing

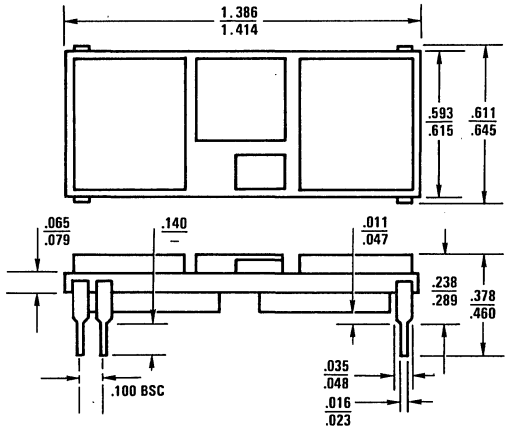


HM-8808A Data Retention Timing



Packaging

28 PIN MODULE



NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

HARRIS

HM-8816H-8

16K x 8 High Speed Asynchronous CMOS Static RAM Module

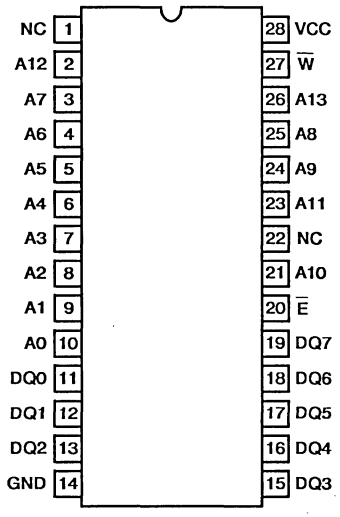
June 1989

Features

- Low Standby Supply Current 800µA
- Low Operating Supply Current 400mA
- Fast Access Time 70ns
- Low Data Retention Supply Voltage 2.0V
- Wide Operating Temperature Range ..... -55°C to +125°C
- CMOS/TTL Compatible Inputs/Outputs
- JEDEC Approved Pinout
- Full CMOS — Six Transistor RAM Cells
- No Clocks or Strobes Required
- Single 5V Power Supply
- Standard DIP Size ..... 0.6" x 1.5"
- Easy Microprocessor Interfacing
- Gated Inputs

Pinout

TOP VIEW

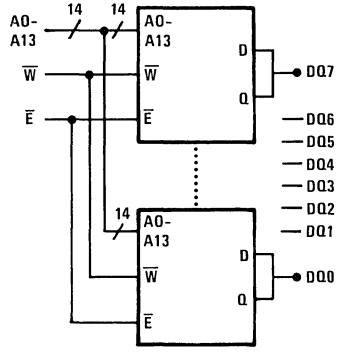


Description

The HM-8816H-8 is a high speed, asynchronous CMOS static RAM module, based on a multi-layer, co-fired, dual-in-line ceramic substrate and eight HM-65262 16K x 1 asynchronous CMOS static RAMs packaged in leadless chip carriers. The HM-8816H-8 uses on-substrate decoupling capacitors packaged in leadless chip carriers to reduce electrical noise and improve reliability. The pinout of the HM-8816H-8 conforms to the JEDEC 8-bit wide, 28 pin RAM standard, which allows the system designer to design sockets that will accomodate a variety of industry standard RAMs and EPROMs. The HM-8816H-8 also has gated inputs to simplify system design for optimum standby supply current.

The HM-65262 RAMs used in this module are full CMOS devices, utilizing arrays of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T cell provides excellent protection against soft errors due to electrical noise and alpha particles. This stability also improves the radiation tolerance of the RAMs over that of four transistor devices.

Functional Diagram



TRUTH TABLE

MODE	$\overline{E}$	$\overline{W}$
Standby (CMOS)	VCC	X
Standby (TTL)	VIH	X
Read	VIL	VIH
Write	VIL	VIL

PIN DESCRIPTIONS

PIN	FUNCTION
A0-A13	Address Inputs
DQ0-DQ7	Data Input/Outputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
VCC	Power (+5V)
GND	Ground

3 CMOS MEMORY

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings*

Supply Voltage ..... +7.0V
Input or Output Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Gate Count 210000
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten Seconds) ..... +300°C

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage ..... 4.5V to 5.5V
Operating Temperature Range ..... -55°C to +125°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSBI	Standby Supply Current (CMOS)	-	800	µA	IO = 0, $\overline{E}$ = VCC - 0.3V
ICCSB	Standby Supply Current (TTL)	-	40	mA	IO = 0, $\overline{E}$ = VIH
ICCEN	Enabled Supply Current	-	400	mA	IO = 0, $\overline{E}$ = VIL, VIN = VIH or VIL
ICCOP	Operating Supply Current (Note 3)	-	400	mA	IO = 0, f = 1MHz, $\overline{E}$ = VIL, VIN = VCC or GND
ICCDR	Data Retention Supply Current	-	320	µA	VCC = 2.0V, $\overline{E}$ = VCC - 0.3V, IO = 0
II	Input Leakage Current	-1	+1	µA	VIN = VCC or GND
IIOZ	IsO Leakage Current	-1	+1	µA	VIO = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0	-	V	$\overline{E}$ = VCC
VOL	Output Voltage Low	-	0.4	V	IOL = 8.0mA
VOH1	Output Voltage High	2.4	-	V	IOH = -4.0mA
VOH2	Output Voltage High (Note 2)	VCC-0.4	-	V	IOH = 100µA
VIL	Input Voltage Low	0	0.8	V	
VIH	Input Voltage High	2.4	VCC	V	

Capacitance (Note 2)

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance	70	pF	f = 1MHz, VIN = VCC or GND
CIO	Input/Output Capacitance	25	pF	f = 1MHz, VIO = VCC or GND

NOTES: 1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns max.; Input and output timing reference level: 1.5V; Output Load: 1TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.

2. Tested at initial design and after major design changes.

3. Typical derating: 40mA/MHz increase in ICCOP.

4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications V_{CC} = 5V ± 10%; T_A = -55°C to +125°C

NO.	SYMBOL		PARAMETER		HM-8816HB MIN	HM-8816HB MAX	HM-8816H MIN	HM-8816H MAX	UNITS	NOTES
READ CYCLE										
(1)	TAVAX	tRC	Read Cycle Time		70	-	85	-	ns	1,4
(2)	TAVQV	tAA	Address Access Time		-	70	-	85	ns	1,4
(3)	TELQV	tCE	Chip Enable Access Time		-	70	-	85	ns	1,4
(4)	TELQX	tLZ	Chip Enable Output Enable Time		5	-	5	-	ns	2,4
(5)	TEHQX		Chip Enable Output Hold Time		5	-	5	-	ns	2,4
(6)	TAXQX	tOH	Address Ouptut Hold Time		5	-	5	-	ns	2,4
(7)	TEHQZ	tHZ	Chip Disable Output Disable Time		0	40	0	40	ns	2,4
WRITE CYCLE										
(8)	TAVAX	tWC	Write Cycle Time		70	-	85	-	ns	1,4
(9)	TELWH	tCW	Chip Enable to End of Write	$\overline{W}$ Controlled	65	-	75	-	ns	1,4
(10)	TELEH	tCW	Chip Enable to End of Write	$\overline{E}$ Controlled	65	-	75	-	ns	2,4
(11)	TWLWH	tWP	Write Pulse Width		55	-	60	-	ns	1,4
(12)	TAVWL	tAS	Address Setup Time	$\overline{W}$ Controlled	0	-	0	-	ns	1,4
(13)	TAVEL	tAS	Address Setup Time	$\overline{E}$ Controlled	0	-	0	-	ns	2,4
(14)	TWHAX	tWR	Write Recovery Time	$\overline{W}$ Controlled	10	-	10	-	ns	1,4
(15)	TEHAX	tWR	Write Recovery Time	$\overline{E}$ Controlled	10	-	10	-	ns	2,4
(16)	TDVWH	tDW	Data Setup Time	$\overline{W}$ Controlled	30	-	35	-	ns	1,4
(17)	TDVEH	tDW	Data Setup Time	$\overline{E}$ Controlled	30	-	35	-	ns	2,4
(18)	TWHDX	tDH	Data Hold Time	$\overline{W}$ Controlled	5	-	5	-	ns	1,4
(19)	TEHDX	tDH	Data Hold Time	$\overline{E}$ Controlled	10	-	10	-	ns	1,4
(20)	TWLQZ	tWZ	Write Enable Low to Output Off		-	40	-	40	ns	2,4
(21)	TWHQX	tOW	Write Enable High to Output On		0	-	0	-	ns	2,4

NOTES: 1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns max.; Input and output timing reference level: 1.5V; Output Load: 1TTL gate equivalent and CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.

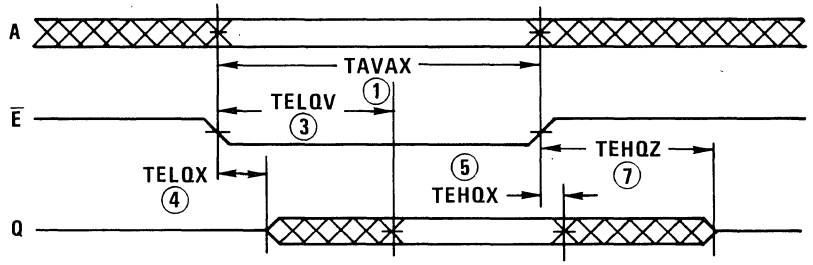
2. Tested at initial design and after major design changes.

3. Typical derating: 40mA/MHz increase in ICCOP.

4. VCC = 4.5V and 5.5V.

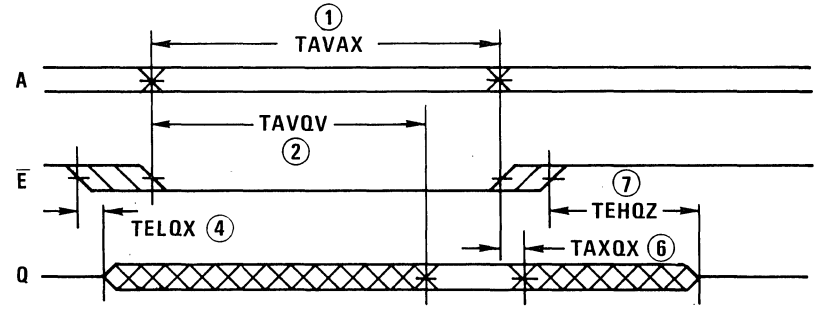
Timing Diagrams

READ CYCLE 1: CONTROLLED BY $\overline{E}$



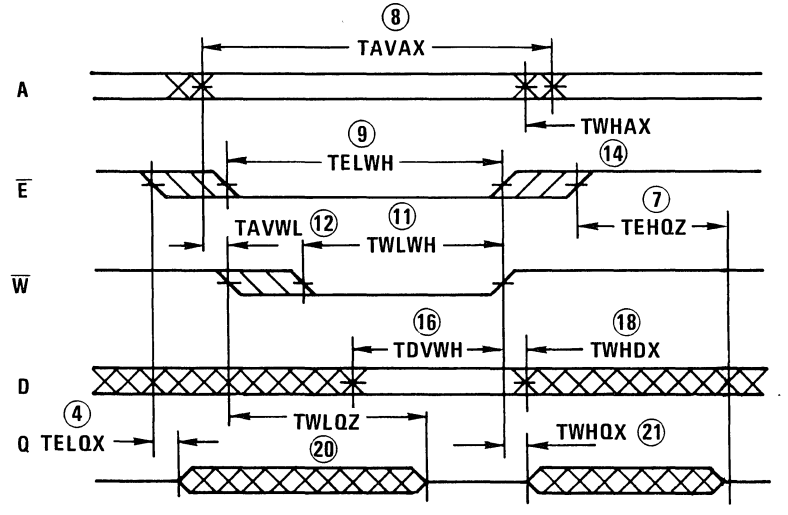
NOTE: $\overline{W}$ is held high for entire cycle and D is ignored. Address is stable by the time $\overline{E}$ goes low and remains valid until $\overline{E}$ goes high.

READ CYCLE 2: CONTROLLED BY ADDRESS



NOTE: $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

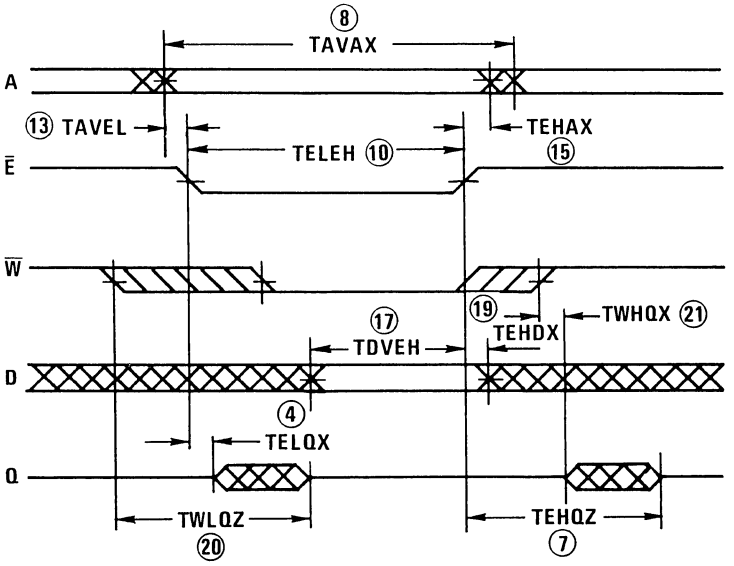
WRITE CYCLE 1: CONTROLLED BY $\overline{W}$ (LATE WRITE)



NOTE: In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are Low.

Timing Diagrams

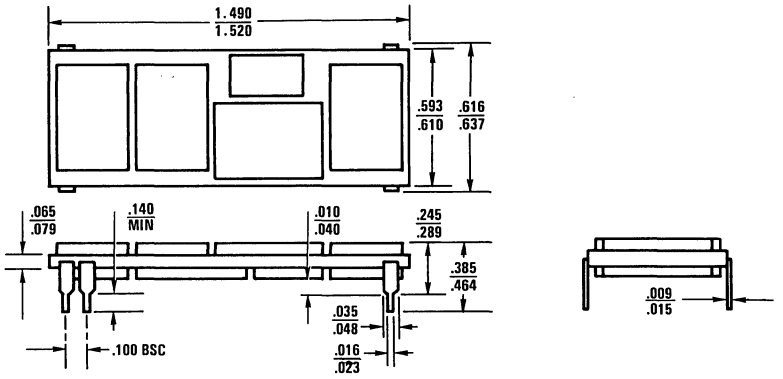
WRITE CYCLE 2: CONTROLLED BY $\overline{E}$ (EARLY WRITE)



NOTE: In this mode, $\overline{W}$ rises after $\overline{E}$. If $\overline{W}$ falls before $\overline{E}$ by a time exceeding TWLQZ (Max) - TELQX (Min), and rises after $\overline{E}$ by a time exceeding TEHQZ (Max) - TWHQZ (Min), then Q will remain in the high impedance state throughout the cycle. The address must remain stable whenever $\overline{E}$ and $\overline{W}$ are both low.

Packaging

28 PIN MODULE



NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

HARRIS

HM-8832-8

32K x 8 Asynchronous CMOS Static RAM Module

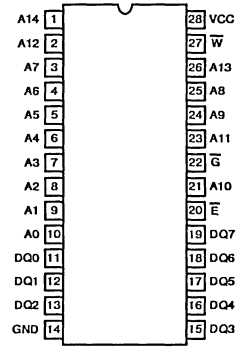
June 1989

Features

- Full CMOS Six Transistor Memory Cell
- Low Standby Supply Current 250µA
- Low Operating Supply Current 15mA
- Fast Address Access Time..... 180ns
- Low Data Retention Supply Voltage 2.0V
- CMOS/TTL Compatible Inputs/Outputs
- JEDEC Approved Pinout
- Equal Cycle and Access Times
- No Clocks or Strobes Required
- Single 5V Power Supply
- Easy Microprocessor Interfacing
- Operating Temperature Range ... -55°C to +125°C
- Standard DIP Size - 0.6" x 1.4"

Pinout

TOP VIEW

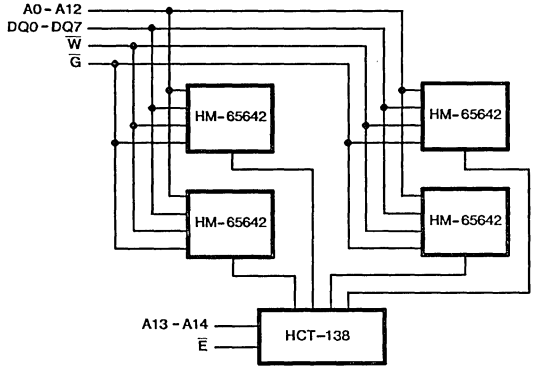


Description

The HM-8832-8 is a 32K x 8 Bit Asynchronous CMOS Static RAM Module based on a multi-layered, co-fired, dual-in-line ceramic substrate, four HM-65642 CMOS Asynchronous Static RAMs, and an HCT-138 high-speed CMOS decoder, all mounted in ceramic leadless chip carriers. In addition to this, each module is equipped with a ceramic capacitor to minimize power supply noise and reduce the need for external decoupling. Furthermore, this capacitor is sealed in a ceramic leadless carrier for maximum reliability, even in extreme environments. All inputs on the HM-8832-8 are gated by the $\overline{E}$ input to simplify system design requirements to obtain the minimum standby and data retention supply current. The pinout of the HM-8832-8 conforms with the JEDEC standard for eight-bit wide, 28 pin RAMs, which allows the module to be pin compatible with future generations of high density RAMs and EPROMs.

The HM-65642 RAMs used on the HM-8832-8 module are full CMOS devices, utilizing arrays of six-transistor (6T) memory cells for the most stable and lowest possible standby and data retention supply current over the full military operating temperature range. In addition to this, the high stability of the 6T cell provides excellent protection against soft errors due to power supply noise and alpha particles. This stability also improves the radiation tolerance of the module over that of RAMs utilizing four transistor (4T) Mix-MOS memory cells.

Functional Diagram



TRUTH TABLE

MODE	$\overline{E}$	$\overline{W}$	$\overline{G}$
Standby (CMOS)	VCC	X	X
Standby (TTL)	VIH	X	X
Enabled (High Z)	VIL	VIH	VIH
Read	VIL	VIH	VIL
Write	VIL	VIL	X

PIN DESCRIPTION

PIN	FUNCTION
A0-A14	Address Inputs
DQ0-DQ7	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
VCC	Power (+5V)
GND	Ground

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Gate Count ..... 405,230 Gates
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten Seconds) ..... +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

D.C. Electrical Specifications (Note 4) VCC = 5V ± 10%; T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSBI	Standby Supply Current (CMOS)	-	900	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCSB	Standby Supply Current (TTL)	-	10	mA	IO = 0, $\overline{E}$ = VIH
ICCEN	Enable Supply Current	-	10	mA	IO = 0, $\overline{E}$ = VIL
ICCOP	Operating Supply Current (Note 3)	-	15	mA	IO = 0, f = 1MHz, $\overline{E}$ = VIL, VI = VCC or GND
ICCDR	Data Retention Supply Current	-	750	µA	VCC = 2.0V, $\overline{E}$ = VCC -0.3V
VCCDR	Data Retention Supply Voltage	2.0	-	V	$\overline{E}$ = VCC
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	0	0.8	V	
VIH	Input High Voltage	2.4	VCC	V	
VOL	Output Low Voltage	-	0.4	V	IOL = 4.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance (Note 2)

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CA	Address Input Capacitance	40	pF	VA = VCC or GND, f = 1MHz
CDQ, CG	Data, Output Enable Capacitance	45	pF	VDQ, VG = VCC or GND, f = 1MHz
CEN	Chip Enable Capacitance	15	pF	VEN = VCC or GND, f = 1MHz
CW	Write Enable Capacitance	60	pF	VW = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 100pF (min) including scope and jig - for CL greater than 100pF, access time is derated by 0.15ns per pF.
2. Guaranteed but not tested.
3. Typical derating 5mA/MHz increase in ICCOP.
4. All devices tested at worst case temperature and supply voltage limits.

A. C. Electrical Specifications (Notes 1, 4) VCC = 5V ± 10%; T_A = -55°C to +125°C

PIN NO.	SYMBOL		PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE								
(1)	TAVAX	tRC	Read Cycle Time		180	-	ns	
(2)	TAVQV	tAA	Address Access Time		-	180	ns	
(3)	TELQV	tCE	Chip Enable Access Time		-	180	ns	
(4)	TGLQV	tOE	Output Enable Access Time		-	75	ns	
(5)	TELQX	tLZ	Chip Enable Output Enable Time		10	-	ns	(Note 2)
(6)	TGLQX	tOLZ	Output Enable Time		5	-	ns	(Note 2)
(7)	TAXQX	tOH	Address Output Hold Time		10	-	ns	(Note 2)
(8)	TEHQZ	tHZ	Chip Disable Output Disable Time		0	80	ns	(Note 2)
(9)	TGHQZ	tOZ	Output Disable Time		0	55	ns	(Note 2)
WRITE CYCLE								
(10)	TAVAX	tWC	Write Cycle Time		180	-	ns	
(11)	TWLWH	tWP	Write Pulse Width		95	-	ns	
(12)	TELWH	tCW	Chip Enable to End of Write	$\overline{W}$ Controlled	95	-	ns	
(13)	TELEH	tCW	Chip Enable to End of Write	$\overline{E}$ Controlled	90	-	ns	(Note 2)
(14)	TAVWL	tAS	Address Setup Time	$\overline{W}$ Controlled	30	-	ns	
(15)	TAVEL	tAS	Address Setup Time	$\overline{E}$ Controlled	30	-	ns	(Note 2)
(16)	TWHAX	tWR	Write Recovery Time	$\overline{W}$ Controlled	10	-	ns	
(17)	TEHAX	tWR	Write Recovery Time	$\overline{E}$ Controlled	40	-	ns	(Note 2)
(18)	TDVWH	tDW	Data Setup Time	$\overline{W}$ Controlled	65	-	ns	
(19)	TDVEH	tDW	Data Setup Time	$\overline{E}$ Controlled	65	-	ns	(Note 2)
(20)	TWHDX	tDH	Data Hold Time	$\overline{W}$ Controlled	10	-	ns	
(21)	TEHDX	tDH	Data Hold Time	$\overline{E}$ Controlled	40	-	ns	(Note 2)
(22)	TWLQZ	tWZ	Write Enable Output Disable Time		-	55	ns	(Note 2)
(23)	TWHQX	tOW	Write Disable Output Enable Time		5	-	ns	(Note 2)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 100pF (min) including scope and jig - for CL greater than 100pF, access time is derated by 0.15ns per pF.
2. Guaranteed but not tested.
3. Typical derating 5mA/MHz increase in ICCOP.
4. All devices tested at worst case temperature and supply voltage limits.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Gate Count ..... 405,230 Gates
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten Seconds) ..... +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

D.C. Electrical Specifications (Note 4) VCC = 5V ± 10%; T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSBI	Standby Supply Current (CMOS)	-	250	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCSB	Standby Supply Current (TTL)	-	2	mA	IO = 0, $\overline{E}$ = VIH
ICCEN	Enable Supply Current	-	10	mA	IO = 0, $\overline{E}$ = VIL
ICCOP	Operating Supply Current (Note 3)	-	15	mA	IO = 0, f = 1MHz, $\overline{E}$ = VIL, VI = VCC or GND
ICCDR	Data Retention Supply Current	-	200	µA	VCC = 2.0V, $\overline{E}$ = VCC -0.3V
VCCDR	Data Retention Supply Voltage	2.0	-	V	$\overline{E}$ = VCC
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	0	0.8	V	
VIH	Input High Voltage	2.4	VCC	V	
VOL	Output Low Voltage	-	0.4	V	IOL = 4.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance (Note 2)

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CA	Address Input Capacitance	40	pF	VA = VCC or GND, f = 1MHz
CDQ, CG	Data, Output Enable Capacitance	45	pF	VDQ, VG = VCC or GND, f = 1MHz
CEN	Chip Enable Capacitance	15	pF	VEN = VCC or GND, f = 1MHz
CW	Write Enable Capacitance	60	pF	VW = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 100pF (min) including scope and jig - for CL greater than 100pF, access time is derated by 0.15ns per pF.
2. Guaranteed but not tested.
3. Typical derating 5mA/MHz increase in ICCOP.
4. All devices tested at worst case temperature and supply voltage limits.

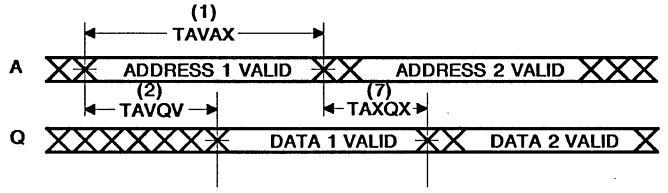
A. C. Electrical Specifications (Notes 1, 4) VCC = 5V ± 10%; T_A = -55°C to +125°C

PIN NO.	SYMBOL		PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE								
(1)	TAVAX	tRC	Read Cycle Time		180	-	ns	
(2)	TAVQV	tAA	Address Access Time		-	180	ns	
(3)	TELQV	tCE	Chip Enable Access Time		-	180	ns	
(4)	TGLQV	tOE	Output Enable Access Time		-	75	ns	
(5)	TELQX	tLZ	Chip Enable Output Enable Time		10	-	ns	(Note 2)
(6)	TGLQX	tOLZ	Output Enable Time		5	-	ns	(Note 2)
(7)	TAXQX	tOH	Address Output Hold Time		10	-	ns	(Note 2)
(8)	TEHQZ	tHZ	Chip Disable Output Disable Time		0	80	ns	(Note 2)
(9)	TGHQZ	tOZ	Output Disable Time		0	55	ns	(Note 2)
WRITE CYCLE								
(10)	TAVAX	tWC	Write Cycle Time		180	-	ns	
(11)	TWLWH	tWP	Write Pulse Width		95	-	ns	
(12)	TELWH	tCW	Chip Enable to End of Write	$\overline{W}$ Controlled	95	-	ns	
(13)	TELEH	tCW	Chip Enable to End of Write	$\overline{E}$ Controlled	90	-	ns	(Note 2)
(14)	TAVWL	tAS	Address Setup Time	$\overline{W}$ Controlled	30	-	ns	
(15)	TAVEL	tAS	Address Setup Time	$\overline{E}$ Controlled	30	-	ns	(Note 2)
(16)	TWHAX	tWR	Write Recovery Time	$\overline{W}$ Controlled	10	-	ns	
(17)	TEHAX	tWR	Write Recovery Time	$\overline{E}$ Controlled	40	-	ns	(Note 2)
(18)	TDVWH	tDW	Data Setup Time	$\overline{W}$ Controlled	65	-	ns	
(19)	TDVEH	tDW	Data Setup Time	$\overline{E}$ Controlled	65	-	ns	(Note 2)
(20)	TWHDX	tDH	Data Hold Time	$\overline{W}$ Controlled	10	-	ns	
(21)	TEHDX	tDH	Data Hold Time	$\overline{E}$ Controlled	40	-	ns	(Note 2)
(22)	TWLQZ	tWZ	Write Enable Output Disable Time		-	55	ns	(Note 2)
(23)	TWHQX	tOW	Write Disable Output Enable Time		5	-	ns	(Note 2)

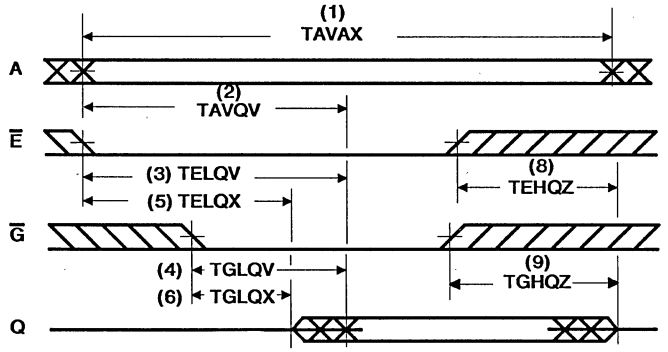
NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 100pF (min) including scope and jig - for CL greater than 100pF, access time is derated by 0.15ns per pF.
2. Guaranteed but not tested.
3. Typical derating 5mA/MHz increase in ICCOP.
4. All devices tested at worst case temperature and supply voltage limits.

Timing Diagrams

READ CYCLE I: ADDRESS CONTROLLED (Notes 1, 2)



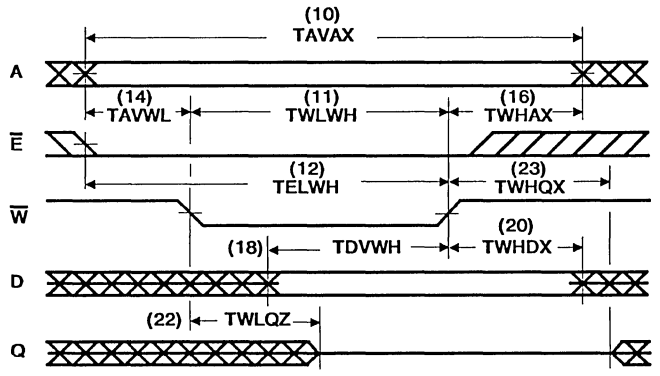
READ CYCLE II: $\overline{E}$ OR $\overline{G}$ CONTROLLED (Note 1)



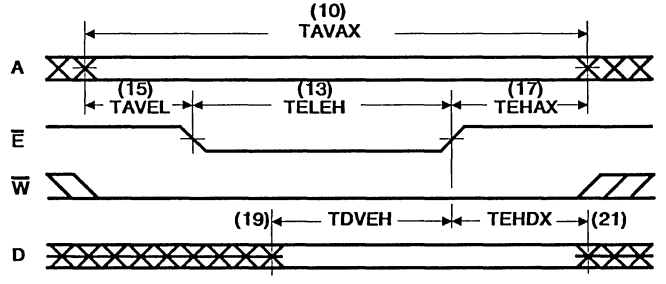
READ CYCLE NOTES:
1 In a read cycle, $\overline{W}$ is held high.
2. In read cycle 1, the module is kept continuously enabled: $\overline{E}$ and $\overline{G}$ are held low.

Timing Diagrams

WRITE CYCLE I: $\overline{W}$ CONTROLLED (Note 1)



WRITE CYCLE II: $\overline{E}$ CONTROLLED (Note 2)



WRITE CYCLE NOTES:

1. In Write Cycle I, the module is first enabled, and then data is strobed into the RAM with a pulse on $\overline{W}$. If $\overline{G}$ is held high for the entire cycle, the outputs will remain in the high impedance state. If $\overline{G}$ is held low, it may be necessary to lengthen the cycle to prevent bus contention. This would occur if TWLQZ and TDVWH overlapped.
2. In Write Cycle II, Address (A) and Write Enable ($\overline{W}$) are first set up and then data is strobed into the RAM with a pulse on $\overline{E}$.

HARRIS

HM-92560-8

256K Synchronous CMOS RAM Module

June 1989

Features

- Low Standby Current 500µA
- Fast Address Access Time 170ns
- Data Retention ..... 2.0V Min VCC
- Three-State Outputs
- Organizable as 32K x 8 or 16K x 16 Array
- On Chip Address Registers
- 48 Pin DIP Pinout - 2.66" x 1.30" x 0.29"
- Synchronous Operation Yields Low Operating Power ..30mA/MHz
- Operating Temperature Range ..... -55°C to +125°C

Description

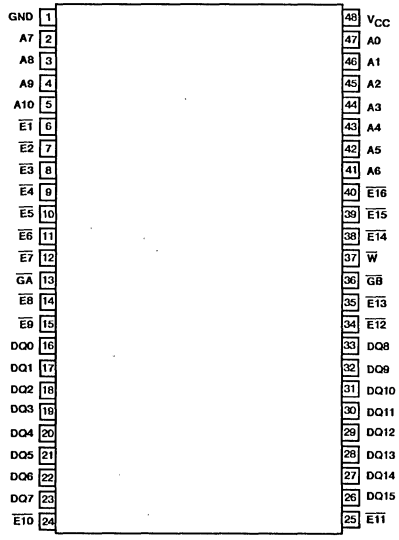
The HM-92560-8 is a high density 256K bit CMOS RAM module. Sixteen synchronous HM-6516 2K x 8 CMOS RAMs in Leadless Chip Carriers are mounted on a multilayer ceramic substrate. The HM-92560-8 RAM module is organized as two 16K x 8 CMOS RAM arrays sharing a common address bus. Separate data input/output buses and chip enables allow the user to format the HM-92560-8 as either a 16K x 16 or 32K x 8 array. Ceramic capacitors are included on the substrate to reduce noise and to minimize the need for additional external decoupling.

The synchronous design of the HM-92560-8 provides low operating power along with address latches for ease of interface to multiplexed address/data bus microprocessors.

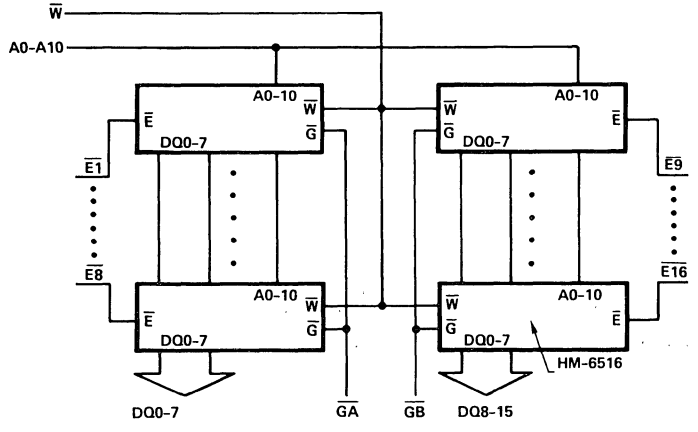
The HM-92560-8 is physically constructed as an extra wide 48 pin dual-in-line package with standard 0.1" centers between pins. This package technique combines the high packing density of CMOS and Leadless Chip Carriers with the ease of use of DIP packaging.

Pinout

TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard I.C. Handling Procedures.

Organizational Guide

FOR 32K x 8 CONFIGURATION

CONNECT: PIN 16 (DQ0) to PIN 33 (DQ8)
PIN 17 (DQ1) to PIN 32 (DQ9)
PIN 18 (DQ2) to PIN 31 (DQ10)
PIN 19 (DQ3) to PIN 30 (DQ11)
PIN 20 (DQ4) to PIN 29 (DQ12)
PIN 21 (DQ5) to PIN 28 (DQ13)
PIN 22 (DQ6) to PIN 27 (DQ14)
PIN 23 (DQ7) to PIN 26 (DQ15)

FOR 16K x 16 CONFIGURATION

CONNECT: PIN 6 ($\overline{E1}$) to PIN 15 ($\overline{E9}$)
PIN 7 ($\overline{E2}$) to PIN 24 ($\overline{E10}$)
PIN 8 ($\overline{E3}$) to PIN 25 ($\overline{E11}$)
PIN 9 ($\overline{E4}$) to PIN 34 ($\overline{E12}$)
PIN 10 ($\overline{E5}$) to PIN 35 ($\overline{E13}$)
PIN 11 ($\overline{E6}$) to PIN 38 ($\overline{E14}$)
PIN 12 ($\overline{E7}$) to PIN 39 ($\overline{E15}$)
PIN 14 ($\overline{E8}$) to PIN 40 ($\overline{E16}$)
PIN 13 ($\overline{GA}$) to PIN 36 ($\overline{GB}$)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 16K x 16 mode use the chip enables as if there were only eight, $\overline{E1}$ thru $\overline{E8}$. In the 32K x 8 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. As the HM-92560-8 is a synchronous memory every address transition must be accompanied by a chip enable transition (see timing diagrams). More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided.

Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HM-92560-8 have conductive lids. These lids are electrically connected to GND. The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Gate Count ..... 415250 Gates
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten Seconds) ..... +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	500	µA	IO = 0, VI = VCC or GND
ICCOP	Operating Supply Current 16K x 16 (Note 3)	-	30	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND $\overline{G}$ = VCC
ICCOP	Operating Supply Current 32K x 8 (Note 3)	-	15	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND $\overline{G}$ = VCC
ICCDR	Data Retention Supply Current	-	350	µA	IO = 0, VCC = 2.0, VI = VCC or GND, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-5	+5	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-5	+5	µA	VIO = VCC or GND
VIL	Input Low Voltage	0	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC	V	
VOL	Output Low Voltage	-	0.4	V	IO = 3.2mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
CIA	Address Input Capacitance (Note 2)	-	200	pF	VI = VCC or GND, f = 1MHz
CIE1	Enable Input Capacitance 16K x 16 (Note 2)	-	100	pF	VI = VCC or GND, f = 1MHz
CIE2	Enable Input Capacitance 32K x 8 (Note 2)	-	50	pF	VI = VCC or GND, f = 1MHz
CIG1	Output Enable Input Capacitance 16K x 16 (Note 2)	-	150	pF	VI = VCC or GND, f = 1MHz
CIG2	Output Enable Input Capacitance 32K x 8 (Note 2)	-	100	pF	VI = VCC or GND, f = 1MHz
CIO1	Input/Output Capacitance 16K x 16 (Note 2)	-	150	pF	VI/O = VCC or GND, f = 1MHz
CIO2	Input/Output Capacitance 32K x 8 (Note 2)	-	250	pF	VI/O = VCC or GND, f = 1MHz
CIW	Write Input Capacitance (Note 2)	-	200	pF	VI = VCC or GND, f = 1MHz
C_{VCC}	Decoupling Capacitance	0.5	-	µF	f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 10ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

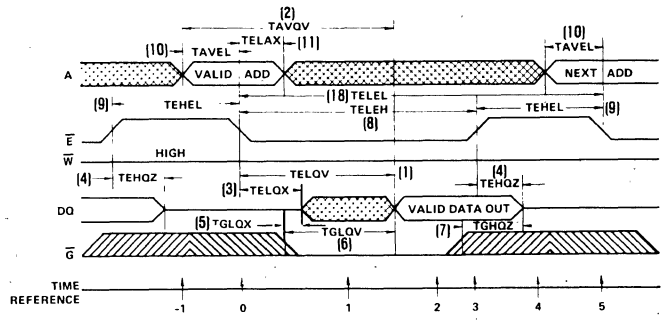
A.C. Electrical Specifications V_{CC} = 5V ± 10%; T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	150	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	170	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	10	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	70	ns	(Notes 2, 4)
(5) TGLQX	Output Enable Output Enable Time	10	-	ns	(Notes 2, 4)
(6) TGLQV	Output Enable Output Valid Time	-	70	ns	(Notes 1, 4)
(7) TGHQZ	Output Enable Output Disable Time	-	70	ns	(Notes 2,4)
(8) TELEH	Chip Enable Pulse Negative Width	150	-	ns	(Notes 1, 4)
(9) TEHEL	Chip Enable Pulse Positive Width	80	-	ns	(Notes 1, 4)
(10) TAVEL	Address Setup Time	20	-	ns	(Notes 1, 4)
(11) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(12) TWLWH	Write Enable Pulse Width	150	-	ns	(Notes 1, 4)
(13) TWLEH	Write Enable Pulse Setup Time	150	-	ns	(Notes 1, 4)
(14) TELWH	Write Enable Pulse Hold Time	150	-	ns	(Notes 1, 4)
(15) TDVWH	Data Setup Time	80	-	ns	(Notes 1, 4)
(16) TWHDX	Data Hold Time	20	-	ns	(Notes 1, 4)
(17) TWLDV	Write Data Delay Time	70	-	ns	(Notes 1, 4)
(18) TELEL	Read or Write Cycle Time	230	-	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 10ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Read Cycle

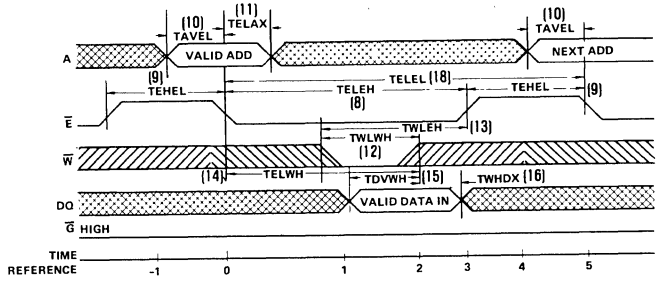


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0		H	X	V	Z	Cycle Begins, Addresses are Latched
1	L	H	L	X	X	Output Enabled
2	L	H	L	X	V	Output Valid
3		H	X	X	V	Read Accomplished
4	H	X	X	X	Z	Prepare for Next Cycle (Same as - 1)
5		H	X	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4).

Write Cycle



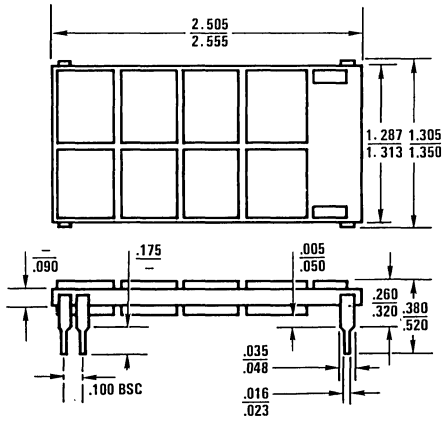
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
-1	H	X	H	X	X	Memory Disabled
0	↓	X	H	V	X	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	Write Period Begins
2	L	↑	H	X	V	Data In Is Written
3	↑	H	H	X	X	Write Completed
4	H	X	H	X	X	Prepare For Next Cycle (Same As -1)
5	↓	X	H	V	X	Cycle Ends. Next Cycle Begins (Same As 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TWHDX and TDVWH must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$ (T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

Packaging

48 PIN MODULE



NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

HARRIS

HM-92570-8

256K Buffered Synchronous CMOS RAM Module

June 1989

Features

- Low Standby Current 600µA/3.5mA
- Fast Access Time 250ns
- Data Retention 2.0V
- Three-State Outputs
- Organizable As 32K x 8 or 16K x 16 Array
- Buffered Address And Control Lines
- On Chip Address Registers
- 48 Pin DIP Pinout - 2.66" x 1.30" x0.29"
- Operating Temperature Range..... -55°C to +125°C

Description

The HM-92570-8 is a fully buffered 256K bit CMOS RAM Module consisting of sixteen HM-6516 2K x 8 CMOS RAMs, two 82C82 CMOS octal latching bus drivers, and two HCT-138 CMOS 3:8 decoders in leadless chip carriers mounted on a multilayer ceramic substrate. The HM-92570-8 RAM Module is organized as two 16K x 8 CMOS RAM arrays sharing a common address bus. Separate data input/output buses allow the user to format the HM-92570-8 as either a 16K x 16 or 32K x 8 array.

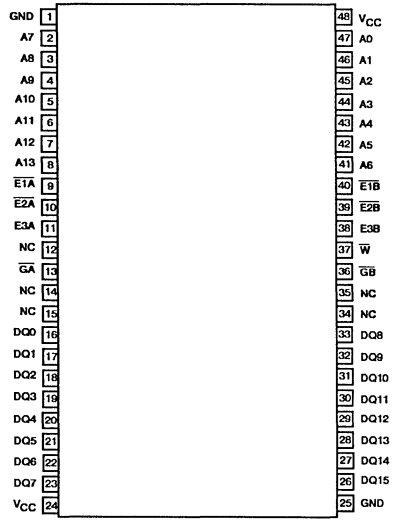
On-board buffers and decoders reduce external package count requirements. Write enable, output enable and chip enable control signals are buffered along with address inputs. Ceramic capacitors sealed in leadless carriers are included on the substrate to reduce power supply noise and to reduce the need for external decoupling.

The synchronous design of the HM-92570-8 provides low operating power along with address latches for ease of interface to multiplexed address/data bus microprocessors.

The HM-92570-8 is physically constructed as an extra wide 48 pin dual-in-line package with standard 0.1" centers between pins. This package technique combines the high packing density of CMOS and leadless chip carriers with the ease of use of DIP packaging.

Pinout

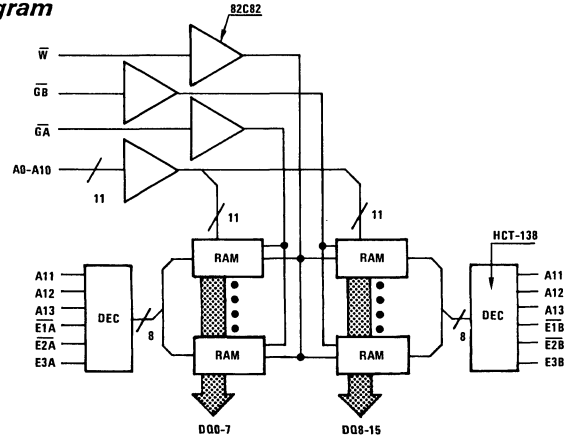
TOP VIEW



PIN NAMES

PIN	DESCRIPTION
A	Address Input
DQ	Data Input/ Output
GX	Output Enable
EXX	Chip Enable
$\overline{W}$	Write Enable
NC	No Connection

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Organizational Guide

FOR 32K X 8 CONFIGURATION

CONNECT: PIN 16 (DQ0) to PIN 33 (DQ8)
PIN 17 (DQ1) to PIN 32 (DQ9)
PIN 18 (DQ2) to PIN 31 (DQ10)
PIN 19 (DQ3) to PIN 30 (DQ11)
PIN 20 (DQ4) to PIN 29 (DQ12)
PIN 21 (DQ5) to PIN 28 (DQ13)
PIN 22 (DQ6) to PIN 27 (DQ14)
PIN 23 (DQ7) to PIN 26 (DQ15)

FOR 16K X 16 CONFIGURATION

CONNECT: Pin 9 ($\overline{E1A}$) to PIN 40 ($\overline{E1B}$)
PIN 10 ($\overline{E2A}$) to PIN 39 ($\overline{E2B}$)
PIN 11 (E3A) to PIN 38 (E3B)
PIN 13 ($\overline{GA}$) to PIN 36 ($\overline{GB}$)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 16K x 16 mode, use the chip enables as if there were only three, E1 thru E3. In the 32K x 8 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. As the HM-92570-8 is a synchronous memory, every address transition must be accompanied by a chip enable transition (see timing diagrams). More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided. To properly decode the chip enables, addresses A11, A12, and A13 must be valid for the duration of TAVAV.

Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HM-92570-8 have conductive lids. These lids are electrically connected to GND.The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Gate Count ..... 417200 Gates
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten Seconds) ..... +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

D.C. Electrical Specifications $VCC = 5V \pm 10\%$; $T_A = -55°C$ to $+125°C$

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	600	µA	IO = 0, VI = VCC or GND
ICCOP	Operating Supply Current (Note 3) 16K x 16	-	30	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND, $\overline{G}$ = VCC
ICCOP	Operating Supply Current (Note 3) 32K x 8	-	15	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND, $\overline{G}$ = VCC
ICCDR	Data Retention Supply Voltage	-	450	µA	VCC = 2.0V, IO = 0, VI = VCC or GND $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-5.0	+5.0	µA	VO = VCC or GND
VIL	Input Low Voltage	0	0.8	V	
VIH	Input High Voltage	3.5	VCC	V	
VOL	Output Low Voltage	-	0.4	V	IO = 3.2mA
VOH1	Output High Voltage	2.4	-	V	IO = -0.4mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
CIA	Address Input Capacitance (Note 2)	-	50	pF	VI = VCC or GND, f = 1MHz
CIE1	Decoder Enable Input Capacitance 16K x 16 (Note 2)	-	50	pF	VI = VCC or GND, f = 1MHz
CIE2	Decoder Enable Input Capacitance 32K x 8 (Note 2)	-	25	pF	VI = VCC or GND, f = 1MHz
CIG1	Output Enable Input Capacitance 16K x 16 (Note 2)	-	50	pF	VI = VCC or GND, f = 1MHz
CIG 2	Output Enable Input Capacitance 32K x 8 (Note 2)	-	25	pF	VI = VCC or GND, f = 1MHz
CIO1	Input/Output Capacitance 16K x 16 (Note 2)	-	150	pF	VI/O = VCC or GND, f = 1MHz
CIO2	Input/Output Capacitance 32K x 8 (Note 2)	-	250	pF	VI/O = VCC or GND, f = 1MHz
CIW	Write Input Capacitance (Note 2)	-	25	pF	VI = VCC or GND, f = 1MHz
CV_{CC}	Decoupling Capacitance	0.5	-	µF	f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 10ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. ICCOP is proportional to operating frequency.
4. VCC = 4.5V and 5.5V.

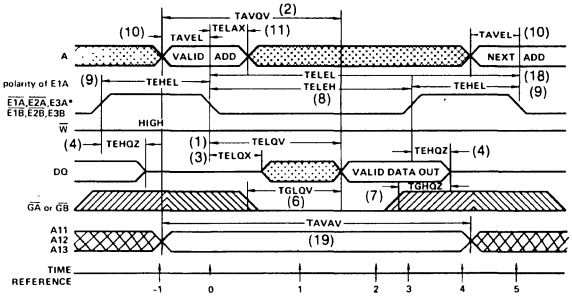
A.C. Electrical Specifications $V_{CC} = 5V \pm 10\%$; $T_A = -55^oC$ to $+125^oC$

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	250	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	270	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	150	ns	(Notes 2, 4)
(5) TGLQX	Output Enable Output Enable Time	10	-	ns	(Notes 2, 4)
(6) TGLQV	Output Enable Output Valid Time	-	120	ns	(Notes 1, 4)
(7) TGHQZ	Output Enable Output Disable Time	-	150	ns	(Notes 2, 4)
(8) TELEH	Chip Enable Pulse Negative Width	250	-	ns	(Notes 1, 4)
(9) TEHEL	Chip Enable Pulse Positive Width	100	-	ns	(Notes 1, 4)
(10) TAVEL	Address Setup Time	20	-	ns	(Notes 1, 4, 5)
(11) TELAX	Address Hold Time	120	-	ns	(Notes 1, 4)
(12) TWLWH	Write Enable Pulse Width	140	-	ns	(Notes 1, 4)
(13) TWLEH	Write Enable Pulse Setup Time	140	-	ns	(Notes 1, 4)
(14) TELWH	Write Enable Pulse Hold Time	250	-	ns	(Notes 1, 4)
(15) TDVWH	Data Setup Time	20	-	ns	(Notes 1, 4)
(16) TWHDX	Data Hold Time	70	-	ns	(Notes 1, 4)
(17) TWLDV	Write Data Delay Time	120	-	ns	(Notes 1, 4)
(18) TELEL	Read or Write Cycle Time	350	-	ns	(Notes 1, 4)
(19) TAVAV	Enable Decoder Address Valid Time	270	-	ns	(Applies Only to A11, A12, A13)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 10ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. ICCOP is proportional to operating frequency.
4. VCC = 4.5V and 5.5V.
5. Includes A11, A12, A13.

Read Cycle

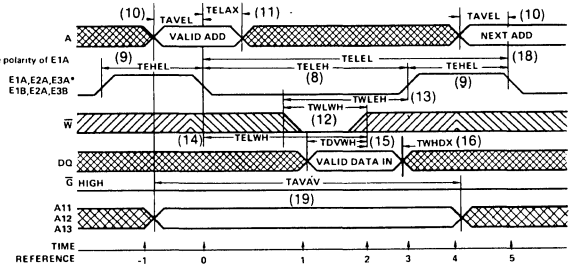


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	Ḡ	A	A11 A12 A13	DATA I/O DQ	FUNCTION
-1	H	X	X	X	X	Z	Memory Disabled
0		H	X	V	V	Z	Cycle Begins, Addresses are Latched
1	L	H	L	X	V	X	Output Enabled
2	L	H	L	X	V	V	Output Valid
3		H	X	X	V	V	Read Accomplished
4	H	X	X	X	X	Z	Prepare for next cycle (Same as -1)
5		H	X	V	V	Z	Cycle ends, next cycle begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2), $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After (T = 4) time, the memory is ready for the next cycle.

Write Cycle



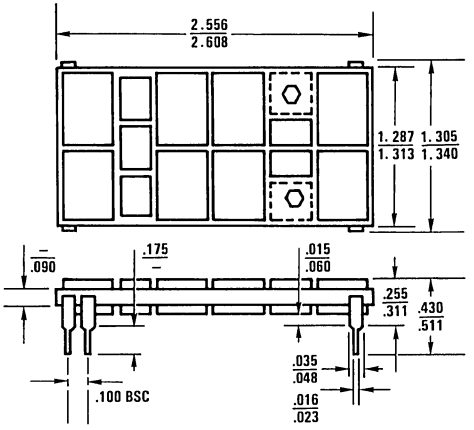
TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	Ḡ	A	A11 A12 A13	DATA I/O DQ	FUNCTION
-1	H	X	H	X	X	X	Memory Disabled
0		X	H	V	V	X	Cycle Begins, Addresses are Latched
1	L	L	H	X	V	X	Write Period Begins
2	L		H	X	V	V	Data In Is Written
3		H	H	X	V	X	Write Completed
4	H	X	H	X	X	X	Prepare For Next Cycle (Same As -1)
5		X	H	V	V	X	Cycle Ends, Next Cycle Begins (Same As 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (in-active). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$ (T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

Packaging

48 PIN MODULE



NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

HARRIS

HM-91M2-8

1M Bit Asynchronous CMOS Static RAM Module

June 1989

Features

- Low Standby Current 900µA
- Low Operating Supply Current 10/20mA
- Fast Address Access Time 180ns
- Low Data Retention Supply Voltage 2.0V
- CMOS/TTL Compatible Inputs/Outputs
- Buffered Address and Control Lines
- 48 Pin DIP Pinout ..... 2.66 x 1.3 x 0.3"
- Operating Temperature Range ..... -55°C to +125°C

Description

The HM-91M2-8 is a fully buffered 1,048,572 bit CMOS RAM module consisting of sixteen HM-65642 8K x 8 CMOS RAMs, two 82C82 CMOS octal buffers, and two HCT-138 CMOS 3:8 decoders in leadless chip carriers mounted on a multi-layer, co-fired, ceramic substrate. The HM-91M2-8 CMOS RAM module is organized as two 64K x 8 RAM arrays sharing a common address bus and write enable input. Separate data input/output buses allow the user to format the HM-91M2-8 as either a 64K x 16 or 128K x 8 bit array.

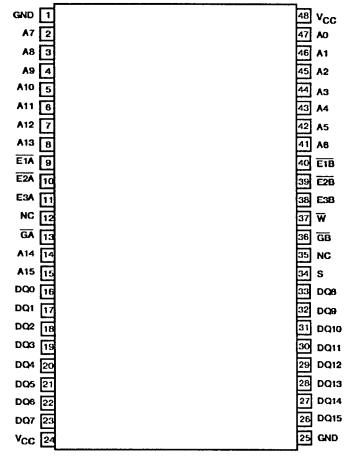
The on-substrate CMOS buffers and decoders on the HM-91M2-8 reduce the system package count and minimize the capacitive load on the system address and control buses. In addition to this, the HM-91M2-8 has on-substrate decoupling capacitors mounted in leadless chip carriers to reduce power supply noise and minimize the need for external decoupling while ensuring high reliability, even in harsh environments.

The HM-91M2-8 is physically constructed as an extra wide 48 pin dual-in-line package with standard 0.1" centers between pins to combine the high density of CMOS and leadless chip carriers with the ease of use of DIP packaging.

The HM-65642 RAMs used on the HM-91M2-8 module are full CMOS devices, utilizing arrays of six-transistor (6T) memory cells for the most stable and lowest possible standby and data retention supply current over full military operating temperature range. In addition to this, the high stability of the 6T cell provides excellent protection against soft errors due to power supply noise and alpha particles. This stability also improves the radiation tolerance of the module over that of RAMs utilizing four transistor (4T) Mix-MOS memory cells.

Pinout

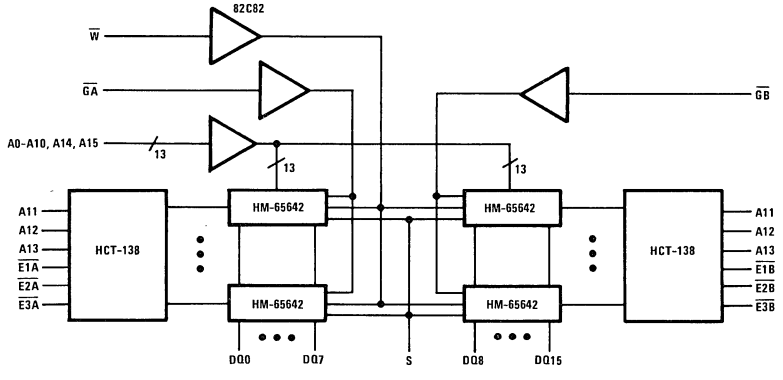
TOP VIEW



PIN NAMES

PIN	DESCRIPTION
A	Address Input
DQ	Data Input/Output
GX	Output Enable
EXX	Chip Enable
W	Write Enable
NC	No Connection
S	Module Select

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND-0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Gate Count ..... 1619000 Gates
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten Seconds) ..... +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	-	900	µA	IO = 0, E3 = S = 0.3V, VCC = 5.5V, VIN = VCC or GND
ICCSB	Standby Supply Current (TTL)	-	2.0	mA	IO = 0, $\overline{E1}$ = $\overline{E2}$ = VIH, E3 = S = VIL, VCC = 5.5V, VIN = VCC or GND
ICCEN	Enabled Supply Current 128K x 8 64K x 16	-	5.0 10	mA mA	IO = 0, $\overline{E1}$ = $\overline{E2}$ = VIL, E3 = VIH, S = VCC -0.3V, VCC = 5.5V, VIN = VCC or GND
ICCOP	Operating Supply Current 128K x 8 (Note 2) 64K x 16	-	10 20	mA mA	IO = 0, f = 1MHz, $\overline{E1}$ = $\overline{E2}$ = VIL, S = VCC E3 = VIH, VCC = 5.5V, VIN = VCC or GND
ICCDR	Data Retention Supply Current	-	750	µA	E3 = S = 0.3V, VCC = 2.0V, VIN = VCC or GND
II	Input Leakage Current (Except S)	-1.0	+1.0	µA	VIN = VCC or GND, VCC = 5.5V
IIS	Module Select Input Current	-5	+5	µA	VIN = VCC or GND, VCC = 5.5V
IIOZ	I/O Leakage Current	-5	+5	µA	VIO = VCC or GND, VCC = 5.5V
VCCDR	Data Retention Supply Voltage	2.0	-	V	
VOL	Output Voltage Low	-	0.4	V	IOL = 4.0mA, VCC = 4.5V
VOH1	Output Voltage High	2.4	-	V	IOH = -1.0mA, VCC = 4.5V
VOH2	Output Voltage High (Note 3)	VCC-0.4		V	IOH = -100µA, VCC = 4.5V
VIL	Input Voltage Low	-0.3	0.8	V	
VIH	Input Voltage High	2.4	VCC+0.3	V	

Capacitance (Note 3)

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Except S)	25	pF	f = 1MHz, VA = VCC or GND
CDQ	Data I/O Capacitance	150	pF	f = 1MHz, VDQ and VG = VCC or GND
CIS	Module Select Input Capacitance	150	pF	f =1MHz, VEN = VCC or GND

NOTES:

1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating: 128K x 8: 5mA/MHz increase in ICCOP; 64K x 16: 10mA/MHz.
3. Guaranteed but not tested.
4. Input pulse levels: 0 to 3.0V; Input rise and fall times: 10ns max; Input and output timing reference level: 1.5V; Output load: 1TTL gate equivalent and CL = 100pF min including scope and jig - for CL greater than 100pF, access time is derated by 0.15ns/pF.
5. Enable valid (EV) in a parameter is determined the last transition that results in the combination of $\overline{E1}$ low, $\overline{E2}$ low and E3 high. Enable invalid (EX) in a parameter is determined by the first transition that results in any other combination than $\overline{E1}$ low, $\overline{E2}$ low and E3 high.

A.C. Electrical Specifications (Notes 1, 4) VCC = 5V ±10%; T_A = -55°C to +125°C

PIN NO.	SYMBOL		PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE								
(1)	TAVAX	tRC	Read Cycle Time		200	-	ns	
(2)	TAVQV	tAA	Address Access Time		-	200	ns	
(3)	TEVQV	tCE1	Chip Enable Access Time		-	200	ns	(Note 5)
(4)	TSHQV	tCE2	Module Select Access Time		-	180	ns	
(5)	TGLQV	tOE	Output Enable Access Time		-	120	ns	
(6)	TEVQX	tLZ1	Chip Enable Output Enable Time		30	-	ns	(Notes 3, 5)
(7)	TSHQX	tLZ2	Module Select Output Enable Time		5	-	ns	(Note 3)
(8)	TGLQX	tOLZ	Output Enable Time		5	-	ns	(Note 3)
(9)	TAXQX	tOH	Address Output Hold Time		30	-	ns	(Note 3)
(10)	TEXQZ	tHZ1	Chip Disable Output Disable Time		0	85	ns	(Notes 3, 5)
(11)	TSLQZ	tHZ2	Module Select Output Disable Time		0	60	ns	(Note 3)
(12)	TGHQZ	tOZ	Output Disable Time		0	70	ns	(Note 3)
WRITE CYCLE								
(13)	TAVAX	tWC	Write Cycle Time		200	-	ns	
(14)	TWLWH	tWP	Write Pulse Width		100	-	ns	
(15)	TEVWH	tCW	Chip Enable to End of Write	$\overline{W}$ Controlled	145	-	ns	(Note 5)
(16)	TEVEX	tCW	Chip Enable to End of Write	E Controlled	120	-	ns	(Notes 3, 5)
(17)	TSHSL	tCW	Chip Enable to End of Write	S Controlled	120	-	ns	(Note 3)
(18)	TAVWL	tAS	Address Setup Time	$\overline{W}$ Controlled	50	-	ns	
(19)	TAVEV	tAS	Address Setup Time	E Controlled	20	-	ns	(Notes 3, 5)
(20)	TAVSH	tAS	Address Setup Time	S Controlled	40	-	ns	(Note 3)
(21)	TWHAX	tWR	Write Recovery Time	$\overline{W}$ Controlled	10	-	ns	
(22)	TEXAX	tWR	Write Recovery Time	E Controlled	10	-	ns	(Notes 3, 5)
(23)	TSLAX	tWR	Write Recovery Time	S Controlled	10	-	ns	(Note 3)
(24)	TDVWH	tDW	Data Setup Time	$\overline{W}$ Controlled	60	-	ns	
(25)	TDVEX	tDW	Data Setup Time	E Controlled	55	-	ns	(Note 3, 5)
(26)	TDVSL	tDW	Data Setup Time	S Controlled	55	-	ns	(Note 3)
(27)	TWHDX	tDH	Data Hold Time	$\overline{W}$ Controlled	35	-	ns	
(28)	TEXDX	tDH	Data Hold Time	E Controlled	35	-	ns	(Notes 3, 5)
(29)	TSLDX	tDH	Data Hold Time	S Controlled	35	-	ns	(Note 3)
(30)	TWLQZ	tWZ	Write Enable Output Disable Time		-	95	ns	(Note 3)
(31)	TWHQX	tOW	Write Disable Output Enable Time		10	-	ns	(Note 3)

NOTES:

1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating: 128K x 8: 5mA/MHz increase in ICCOP; 64K x 16: 10mA/MHz.
3. Guaranteed but not tested.
4. Input pulse levels: 0 to 3.0V; Input rise and fall times: 10ns max; Input and output timing reference level: 1.5V; Output load: 1TTL gate equivalent and CL = 100pF min including scope and jig - for CL greater than 100pF, access time is derated by 0.15ns/pF.
5. Enable valid (EV) in a parameter is determined the last transition that results in the combination of $\overline{E1}$ low, $\overline{E2}$ low and E3 high. Enable invalid (EX) in a parameter is determined by the first transition that results in any other combination than $\overline{E1}$ low, $\overline{E2}$ low and E3 high.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND-0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Gate Count ..... 1619000 Gates
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten Seconds) ..... +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	-	900	µA	IO = 0, E3 = S = 0.3V, VCC = 5.5V,
ICCSB	Standby Supply Current (TTL)	-	2.0	mA	IO = 0, $\overline{E1}$ = $\overline{E2}$ = VIH, E3 = S = VIL, VCC = 5.5V, VIN = VCC or GND
ICCEN	Enabled Supply Current 128K x 8 64K x 16	-	5.0 10	mA mA	IO = 0, $\overline{E1}$ = $\overline{E2}$ = VIL, E3 = VIH, S = VCC -0.3V, VCC = 5.5V, VIN = VCC or GND
ICCOP	Operating Supply Current 128K x 8 (Note 2) 64K x 16	-	10 20	mA mA	IO = 0, f = 1MHz, $\overline{E1}$ = $\overline{E2}$ = VIL, S = VCC E3 = VIH, VCC = 5.5V, VIN = VCC or GND
ICCDR	Data Retention Supply Current	-	750	µA	E3 = S = 0.3V, VCC = 2.0V
II	Input Leakage Current (Except S)	-1.0	+1.0	µA	VIN = VCC or GND, VCC = 5.5V
IIS	Module Select Input Current	-5	+5	µA	VIN = VCC or GND, VCC = 5.5V
IIOZ	I/O Leakage Current	-5	+5	µA	VIO = VCC or GND, VCC = 5.5V
VCCDR	Data Retention Supply Voltage	2.0	-	V	
VOL	Output Voltage Low	-	0.4	V	IOL = 4.0mA, VCC = 4.5V
VOH1	Output Voltage High	2.4	-	V	IOH = -1.0mA, VCC = 4.5V
VOH2	Output Voltage High (Note 3)	VCC-0.4	-	V	IOH = -100µA, VCC = 4.5V
VIL	Input Voltage Low	-0.3	0.8	V	
VIH	Input Voltage High	2.4	VCC+0.3	V	

Capacitance (Note 3)

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Except S)	25	pF	f = 1MHz, VA = VCC or GND
CDQ	Data I/O Capacitance	150	pF	f = 1MHz, VDQ and VG = VCC or GND
CIS	Module Select Input Capacitance	150	pF	f = 1MHz, VEN = VCC or GND

NOTES:

1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating: 128K x 8: 5mA/MHz increase in ICCOP; 64K x 16: 10mA/MHz.
3. Guaranteed but not tested.
4. Input pulse levels: 0 to 3.0V; Input rise and fall times: 10ns max; Input and output timing reference level: 1.5V; Output load: 1TTL gate equivalent and CL = 100pF min including scope and jig - for CL greater than 100pF, access time is derated by 0.15ns/pF.
5. Enable valid (EV) in a parameter is determined the last transition that results in the combination of $\overline{E1}$ low, $\overline{E2}$ low and E3 high. Enable invalid (EX) in a parameter is determined by the first transition that results in any other combination than $\overline{E1}$ low, $\overline{E2}$ low and E3 high.

D.C. Electrical Specifications (Notes 1, 4) VCC = 5V ±10%; T_A = -55°C to +125°C

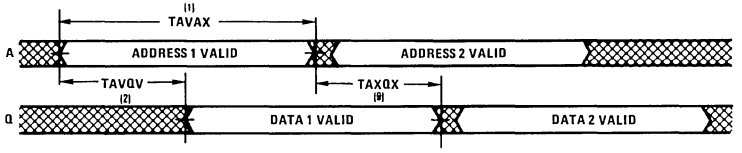
PIN NO.	SYMBOL		PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE								
(1)	TAVAX	tRC	Read Cycle Time		180	-	ns	
(2)	TAVQV	tAA	Address Access Time		-	180	ns	
(3)	TEVQV	tCE1	Chip Enable Access Time		-	180	ns	(Note 5)
(4)	TSHQV	tCE2	Module Select Access Time		-	160	ns	
(5)	TGLQV	tOE	Output Enable Access Time		-	120	ns	
(6)	TEVQX	tLZ1	Chip Enable Output Enable Time		25	-	ns	(Notes 3, 5)
(7)	TSHQX	tLZ2	Module Select Output Enable Time		5	-	ns	(Note 3)
(8)	TGLQX	tOLZ	Output Enable Time		5	-	ns	(Note 3)
(9)	TAXQX	tOH	Address Output Hold Time		30	-	ns	(Note 3)
(10)	TEXQZ	tHZ1	Chip Disable Output Disable Time		0	75	ns	(Notes 3, 5)
(11)	TSLQZ	tHZ2	Module Select Output Disable Time		0	50	ns	(Note 3)
(12)	TGHQZ	tOZ	Output Disable Time		0	60	ns	(Note 3)
WRITE CYCLE								
(13)	TAVAX	tWC	Write Cycle Time		180	-	ns	
(14)	TWLWH	tWP	Write Pulse Width		100	-	ns	
(15)	TEVWH	tCW	Chip Enable to End of Write	$\overline{W}$ Controlled	140	-	ns	(Note 5)
(16)	TEVEX	tCW	Chip Enable to End of Write	E Controlled	120	-	ns	(Notes 3, 5)
(17)	TSHSL	tCW	Chip Enable to End of Write	S Controlled	120	-	ns	(Note 3)
(18)	TAVWL	tAS	Address Setup Time	$\overline{W}$ Controlled	40	-	ns	
(19)	TAVEV	tAS	Address Setup Time	E Controlled	0	-	ns	(Notes 3, 5)
(20)	TAVSH	tAS	Address Setup Time	S Controlled	40	-	ns	(Note 3)
(21)	TWHAX	tWR	Write Recovery Time	$\overline{W}$ Controlled	10	-	ns	
(22)	TEXAX	tWR	Write Recovery Time	E Controlled	10	-	ns	(Notes 3, 5)
(23)	TSLAX	tWR	Write Recovery Time	S Controlled	10	-	ns	(Note 3)
(24)	TDVWH	tDW	Data Setup Time	$\overline{W}$ Controlled	60	-	ns	
(25)	TDVEX	tDW	Data Setup Time	E Controlled	55	-	ns	(Note 3,5)
(26)	TDVSL	tDW	Data Setup Time	S Controlled	55	-	ns	(Note 3)
(27)	TWHDX	tDH	Data Hold Time	$\overline{W}$ Controlled	35	-	ns	
(28)	TEXDX	tDH	Data Hold Time	E Controlled	35	-	ns	(Notes 3, 5)
(29)	TSLDX	tDH	Data Hold Time	S Controlled	35	-	ns	(Note 3)
(30)	TWLQZ	tWZ	Write Enable Output Disable Time		-	95	ns	(Note 3)
(31)	TWHQX	tOW	Write Disable Output Enable Time		10	-	ns	(Note 3)

NOTES:

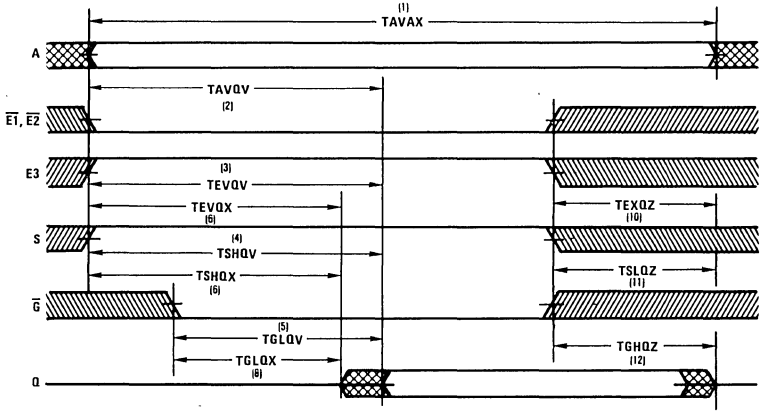
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating: 128K x 8: 5mA/MHz increase in ICCOP; 64K x 16: 10mA/MHz.
3. Guaranteed but not tested.
4. Input pulse levels: 0 to 3.0V; Input rise and fall times: 10ns max; Input and output timing reference level: 1.5V; Output load: 1TTL gate equivalent and CL = 100pF min including scope and jig - for CL greater than 100pF, access time is derated by 0.15ns/pF.
5. Enable valid (EV) in a parameter is determined the last transition that results in the combination of $\overline{E1}$ low, $\overline{E2}$ low and E3 high. Enable invalid (EX) in a parameter is determined by the first transition that results in any other combination than $\overline{E1}$ low, $\overline{E2}$ low and E3 high.

Timing Diagrams

READ CYCLE 1: ADDRESS CONTROLLED (NOTES 1, 2)



READ CYCLE 2: E, S, or $\overline{G}$ CONTROLLED (NOTE 1)

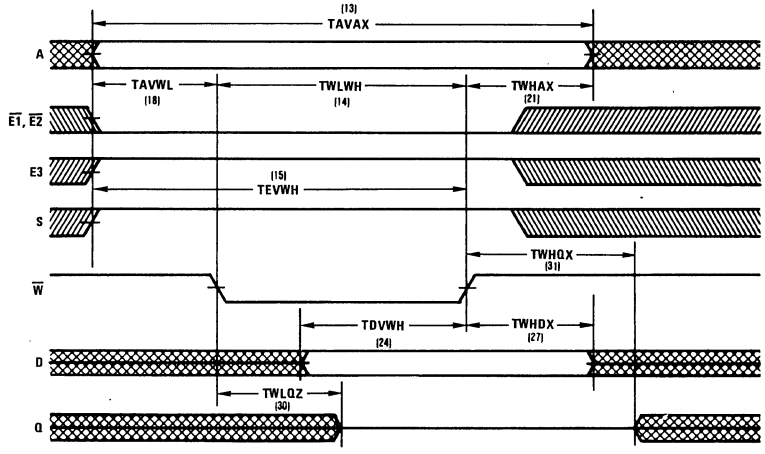


READ CYCLE NOTES: 1. In a read cycle, $\overline{W}$ is held high.

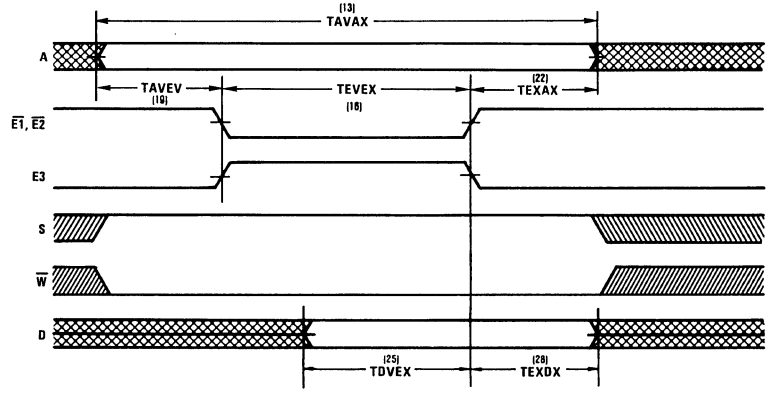
2. In read cycle 1, the module is kept continuously enabled: $\overline{E1}$, $\overline{E2}$ and $\overline{G}$ are held low; E3 and S are held high.

Timing Diagrams

WRITE CYCLE 1: $\overline{W}$ CONTROLLED (NOTE 1)

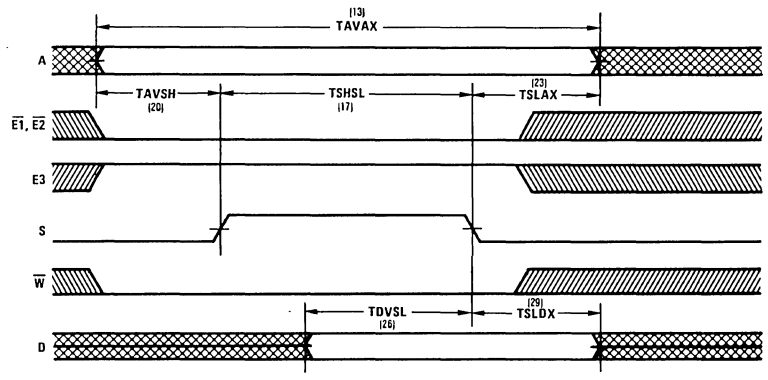


WRITE CYCLE 2: $\overline{E1}$, $\overline{E2}$, or E3 CONTROLLED (NOTE 2)



Timing Diagrams

WRITE CYCLE 3: S CONTROLLED (NOTE 3)



WRITE CYCLE NOTES:

1. In Write Cycle 1, the module is first enabled, and then data is strobed into the RAM with a pulse on $\overline{W}$. If $\overline{G}$ is held high for the entire cycle, the outputs will remain in the high impedance state. If $\overline{G}$ is held low, it may be necessary to lengthen the cycle to prevent bus contention. This would occur if TWLQZ and TDVWH overlapped.
2. In Write Cycle 2, Address (A) and Write Enable ($\overline{W}$) are first set up and then data is strobed into the RAM with a pulse on E.
3. In Write Cycle 3, Addresses (A), Write Enable ($\overline{W}$) and the Chip Enable inputs ($\overline{E1}$, $\overline{E2}$ and E3) are first set up and data is then strobed into the RAM with the Module Select (S) input.

TRUTH TABLE

INPUTS										MODE
S	$\overline{E1A}$	$\overline{E2A}$	E3A	$\overline{E1B}$	$\overline{E2B}$	E3B	$\overline{GA}$	$\overline{GB}$	$\overline{W}$	
GND	X	X	GND	X	X	GND	X	X	X	Standby (CMOS) Sides A and B
VIL	X	X	X	X	X	X	X	X	X	Standby (TTL) Sides A and B
X	VIH	X	X	X	X	X	X	X	X	Standby (TTL) Side A
X	X	VIH	X	X	X	X	X	X	X	Standby (TTL) Side A
X	X	X	VIL	X	X	X	X	X	X	Standby (TTL) Side A
X	X	X	X	VIH	X	X	X	X	X	Standby (TTL) Side B
X	X	X	X	X	VIH	X	X	X	X	Standby (TTL) Side B
X	X	X	X	X	X	VIL	X	X	X	Standby (TTL) Side B
VIH	VIL	VIL	VIH	X	X	X	VIH	X	VIH	Side A Enabled, Outputs High Impedance
VIH	X	X	X	VIL	VIL	VIH	X	VIH	VIH	Side B Enabled, Outputs High Impedance
VIH	VIL	VIL	VIH	X	X	X	VIL	X	VIH	Read Side A
VIH	X	X	X	VIL	VIL	VIH	X	VIL	VIH	Read Side B
VIH	VIL	VIL	VIH	X	X	X	X	X	VIL	Write Side A
VIH	X	X	X	VIL	VIL	VIH	X	X	VIL	Write Side B

NOTE:
Side A refers to the half of the module that connects to DQ0 through DQ7 and side B refers to the half of the module that connects to DQ8 through DQ15. When the module is configured as a 64K x 16 array, side A and side B may be enabled either simultaneously or separately. When the array is configured as a 128K x 8 array, side A and B should not be enabled simultaneously, as bus contention could result.

Organizational Guide

FOR 128K X 8 CONFIGURATION

CONNECT: PIN 16 (DQ0) to PIN 33 (DQ8)
PIN 17 (DQ1) to PIN 32 (DQ9)
PIN 18 (DQ2) to PIN 31 (DQ10)
PIN 19 (DQ3) to PIN 30 (DQ11)
PIN 20 (DQ4) to PIN 29 (DQ12)
PIN 21 (DQ5) to PIN 28 (DQ13)
PIN 22 (DQ6) to PIN 27 (DQ14)
PIN 23 (DQ7) to PIN 26 (DQ15)

FOR 64K X 16 CONFIGURATION

CONNECT: PIN 9 ($\overline{E1A}$) to PIN 40 ($\overline{E1B}$)
PIN 10 ($\overline{E2A}$) to PIN 39 ($\overline{E2B}$)
PIN 11 (E3A) to PIN 38 (E3B)
PIN 13 ($\overline{GA}$) to PIN 36 ($\overline{GB}$)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 64K x 16 mode use the chip enables as if there were only three, E1 thru E3. In the 128K x 8 mode all chip enables must be treated separately. Transitions between chip enables must be treated with the same constraints that apply to any one chip enable. More than one (internal) chip enable low simultaneously, for devices whose outputs are tied together either internally or externally, is an illegal input condition and must be avoided.

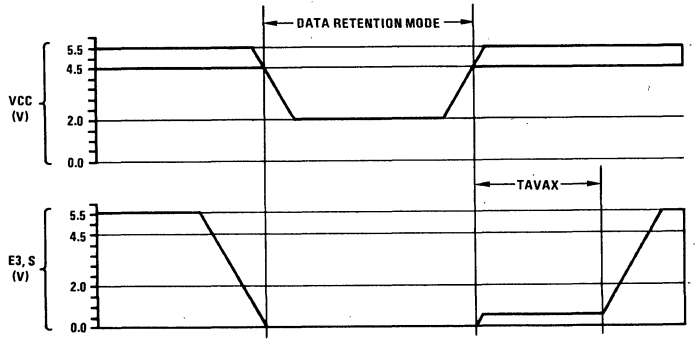
Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HM-91M2 have conductive lids. These lids are electrically connected to GND. The system designer should be aware that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Low Voltage Data Retention

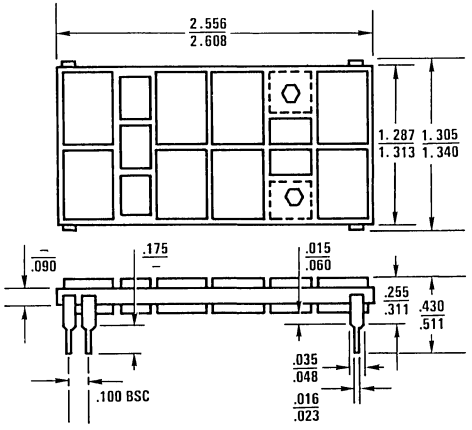
Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. The module must be kept disabled during data retention. The Chip Enable (E3A and E3B) and module select (S) must be between -0.3V and +0.3V.
2. During power-up and power-down transitions. S must be held between -0.3V and 10% of VCC.
3. The RAM module can begin operation one TAVAX after VCC reaches the minimum operating voltage (4.5V).



Packaging

HM-91M2-8 48 PIN MODULE



NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

HARRIS

HM-6642/883

June 1989

512 x 8 CMOS PROM

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby and Operating Power
  - ICCSB 100µA
  - ICCOP ..... 20mA at 1MHz
- Fast Access Time..... 120/200ns
- Wide Operating Temperature Range ..... -55°C to +125°C
- Industry Standard Pinout
- Single 5.0 Volt Supply
- CMOS/TTL Compatible Inputs
- Field Programmable
- Synchronous Operation
- On-Chip Address Latches
- Separate Output Enable

Description

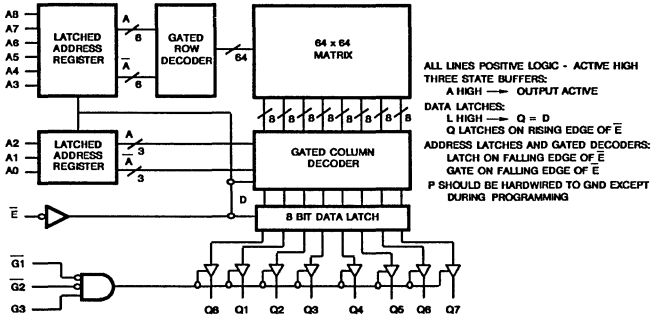
The HM-6642/883 is a 512 x 8 CMOS NiCr fusible link Programmable Read Only Memory in the popular 24 pin, byte wide pinout. Synchronous circuit design techniques combine with CMOS processing to give this device high speed performance with very low power dissipation.

On-chip address latches are provided, allowing easy interfacing with recent generation microprocessors that use multiplexed addresss/data bus structures, such as the 8085. The output enable controls, both active low and active high, further simplify microprocessor system interfacing by allowing output data bus control independent of the chip enable control. The data output latches allow the use of the HM-6642/883 in high speed pipelined architecture systems, and also in synchronous logic replacement functions.

Applications for the HM-6642/883 CMOS PROM include low power handheld microprocessor based instrumentation and comunications systems, remote data acquisition and processing systems, processor control store, and synchronous logic replacement.

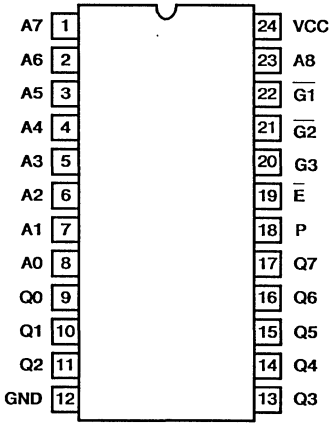
All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

Functional Diagram

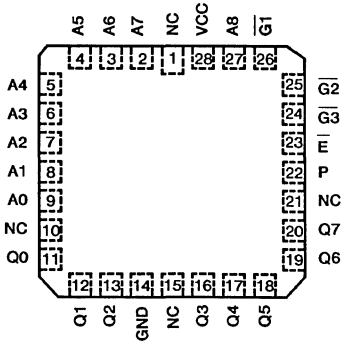


Pinouts

HM1-6642/883 (CERAMIC DIP)
TOP VIEW



HM4-6642/883 (CERAMIC LCC)
TOP VIEW



PIN	DESCRIPTION
NC	No Connect
A0-A8	Address Inputs
$\overline{E}$	Chip Enable
Q	Data Output
V_{CC}	Power (+5V)
$\overline{G}$	Output Enable
P*	Program Enable

* P Should be Hardwired to GND Except During Programming.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	52°C/W	20°C/W
Ceramic LCC Package	58°C/W	19°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 0.96W
Ceramic LCC Package 0.86W
Gate Count ..... 1680 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... ±4.5V
Input Low Voltage VIL ..... -0.3V to +0.8V
Input High Voltage VIH ..... +2.4 to VCC +0.3V

TABLE 1. HM-6642/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

D.C. PARAMETERS	SYMBOL	(NOTES 1, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH	VCC = 4.5V, IO = -1.0mA	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = +3.2mA	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 5.5V, VI/O = GND or VCC	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC, P Not Tested	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-1.0	1.0	µA
Standby Supply Current	ICCSB	VI = VCC or GND VCC = 5.5V, IO = 0mA	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	100	µA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = GND, G = VCC, (Note 3), f = 1MHz, IO = 0mA, VI = VCC or GND	1, 2, 3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	20	mA
Functional Test	FT	VCC = 4.5V (Note 10)	7, 8A, 8B	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	-	

TABLE 2. HM-6642/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	220	ns
Output Enable Access Time	TGVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	150	ns
Chip Enable Access Time	TELQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	200	ns
Address Setup Time	TAVEL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	20	-	ns
Address Hold Time	TELAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	60	-	ns
Chip Enable Low Width	TELEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	200	-	ns
Chip Enable High Width	TEHEL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	150	-	ns
Read Cycle Time	TELEL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	350	-	ns

NOTES:

1. All voltages referenced to VSS.
2. A.C. measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL $\cong$ 50pF.
3. Typical derating = 5mA/MHz increase in ICCOP.
4. All tests performed with P hardwired to GND.

CAUTION:These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6642/883 A.C. AND D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 4) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, f = 1MHz All Measurements Reference Device Ground	5, 7	$T_A = +25^oC$	-	10	pF
		VCC = Open, f = 1MHz All Measurements Reference Device Ground	5, 8	$T_A = +25^oC$	-	12	pF
			5, 9	$T_A = +25^oC$	-	5	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz All Measurements Reference Device Ground	5, 7	$T_A = +25^oC$	-	12	pF
		VCC = Open, f = 1MHz All Measurements Reference Device Ground	5, 8	$T_A = +25^oC$	-	14	pF
			5, 9	$T_A = +25^oC$	-	8	pF
Output Enable Time	TGVQX	VCC = 4.5V and 5.5V	5	$-55^oC \leq T_A \leq +125^oC$	5	150	ns
Output Disable Time	TGXQZ	VCC = 4.5V and 5.5V	5	$-55^oC \leq T_A \leq +125^oC$	-	150	ns

NOTES:

5. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design changes which would affect these characteristics.
6. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
7. Applies to .600 inch Ceramic Dual-In-Line (DIP) device types only.
8. Applies to .300 inch Ceramic Dual-In-Line (DIP) device types only.
9. Applies to Ceramic Leadless Chip Carrier (LCC) device types only.
10. Tested as follows: f = 1MHz, VIH = 2.4V, VIL = 0.8V, IOH = -1mA, IOL = +1mA, VOH $\geq$ 1.5V, VOL $\leq$ 1.5V.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 7, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
ESD Classification ..... Class 1
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	52°C/W	20°C/W
Ceramic LCC Package	58°C/W	19°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 0.96W
Ceramic LCC Package 0.86W
Gate Count ..... 1680 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... ±4.5V
Input Low Voltage VIL ..... -0.3V to +0.8V
Input High Voltage VIH ..... +2.4 to VCC +0.3V

TABLE 1. HM-6642B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

D.C. PARAMETERS	SYMBOL	(NOTES 1, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH	VCC = 4.5V, IO = -1.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = +3.2mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 5.5V, VI/O = GND or VCC	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC, P Not Tested	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	ICCSB	VI = VCC or GND VCC = 5.5V, IO = 0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	µA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = GND, G = VCC, (Note 3), f = 1MHz, IO = 0mA, VI = VCC or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	20	mA
Functional Test	FT	VCC = 4.5V (Note 10)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	

TABLE 2. HM-6642B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	140	ns
Output Enable Access Time	TGVQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	50	ns
Chip Enable Access Time	TELQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	120	ns
Address Setup Time	TAVEL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	20	-	ns
Address Hold Time	TELAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	25	-	ns
Chip Enable Low Width	TELEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	120	-	ns
Chip Enable High Width	TEHEL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	40	-	ns
Read Cycle Time	TELEL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	160	-	ns

NOTES:

1. All voltages referenced to VSS.
2. A.C. measurements assume transition time ≤ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL ≅ 50pF.
3. Typical derating = 5mA/MHz increase in ICCOP.
4. All tests performed with P hardwired to GND.

CAUTION:These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-6642B/883 A.C. AND D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 4) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, f = 1MHz All Measurements Reference Device Ground	5, 7	$T_A = +25^oC$	-	10	pF
		VCC = Open, f = 1MHz All Measurements Reference Device Ground	5, 8	$T_A = +25^oC$	-	12	pF
			5, 9	$T_A = +25^oC$	-	5	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz All Measurements Reference Device Ground	5, 7	$T_A = +25^oC$	-	12	pF
		VCC = Open, f = 1MHz All Measurements Reference Device Ground	5, 8	$T_A = +25^oC$	-	14	pF
			5, 9	$T_A = +25^oC$	-	8	pF
Output Enable Time	TGVQX	VCC = 4.5V and 5.5V	5	$-55^oC \leq T_A \leq +125^oC$	5	50	ns
Output Disable Time	TGXQZ	VCC = 4.5V and 5.5V	5	$-55^oC \leq T_A \leq +125^oC$	-	50	ns

NOTES:

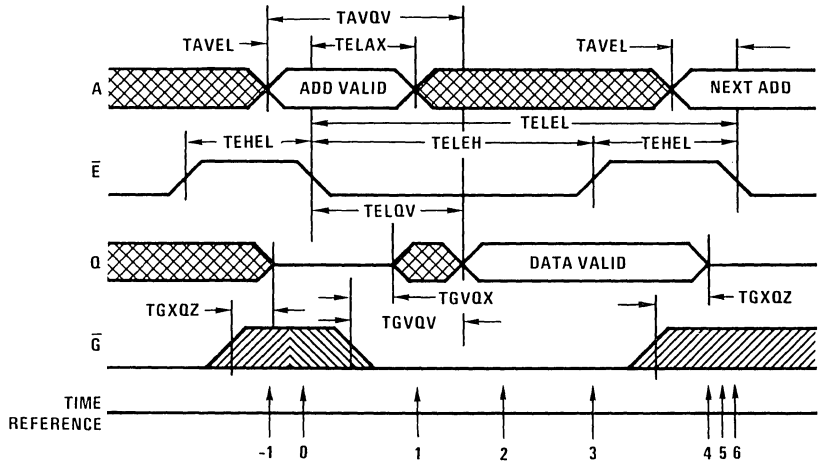
5. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design changes which would affect these characteristics.
6. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
7. Applies to .600 inch Ceramic Dual-In-Line (DIP) device types only.
8. Applies to .300 inch Ceramic Dual-In-Line (DIP) device types only.
9. Applies to Ceramic Leadless Chip Carrier (LCC) device types only.
10. Tested as follows: f = 1MHz, VIH = 2.4V, VIL = 0.8V, IOH = -1mA, IOL = +1mA, VOH $\geq$ 1.5V, VOL $\leq$ 1.5V.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 7, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

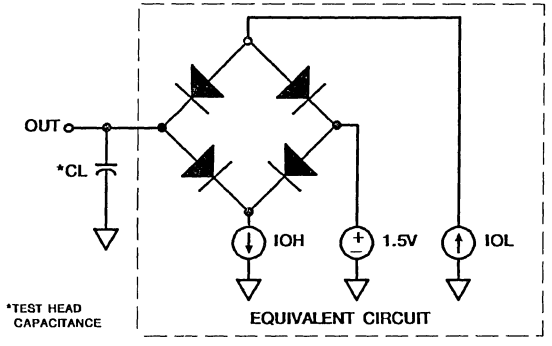
Switching Waveform

READ CYCLE



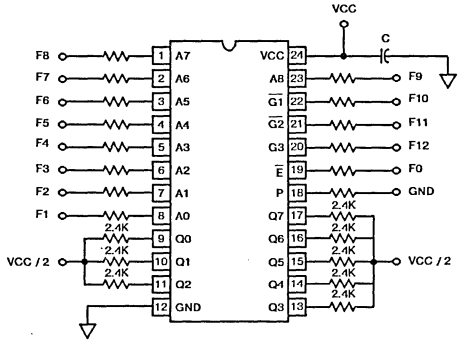
* G Has the same timing as $\overline{G}$ except signal is inverted.

Test Load Circuit

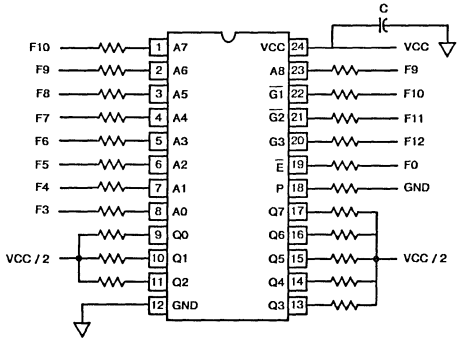


Burn-In Circuits

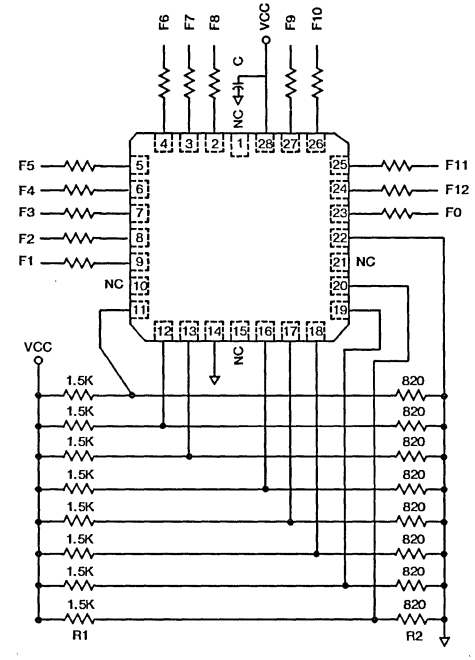
HM-6642/883 (.300 INCH) CERAMIC DIP



HM-6642/883 (.600 INCH) CERAMIC DIP



HM-6642/883 CERAMIC LCC



NOTES:

F_O = 100kHz ±10%

All Resistors = 47kΩ Unless Otherwise Noted

VCC = 5.5V ± 0.5V

VIH = -4.5V ± 10%

VIL = -0.2V to 0.4V

C = 0.01µF Min

Metallization Topology

DIE DIMENSIONS:
136 x 168 x 19 ±1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ to 15kÅ

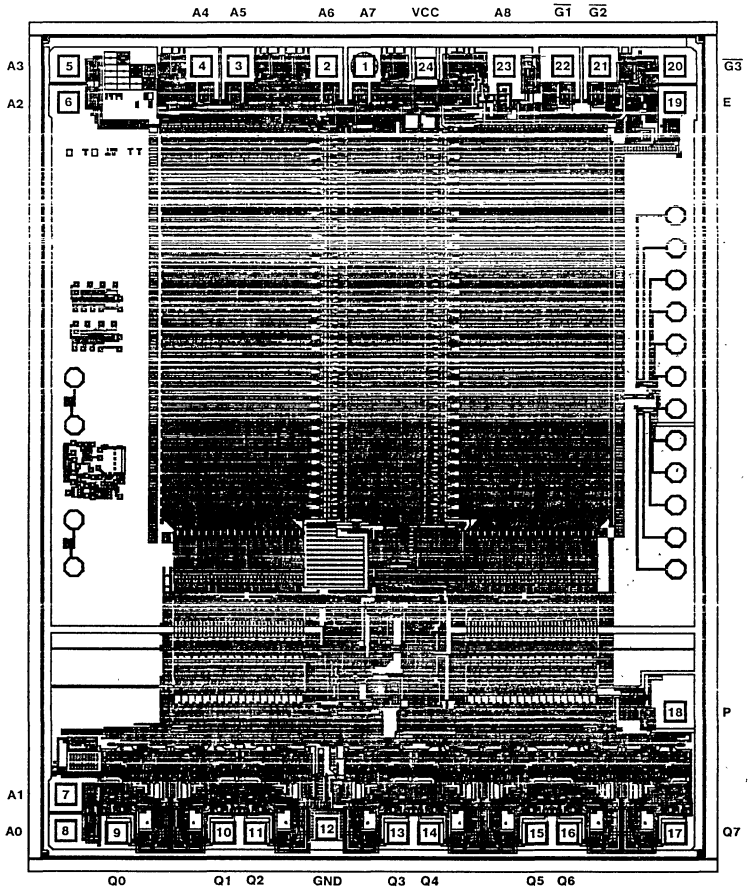
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.7×10^5 A/cm^2

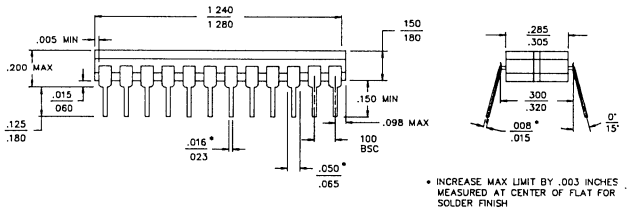
Metallization Mask Layout

HM-6642/883



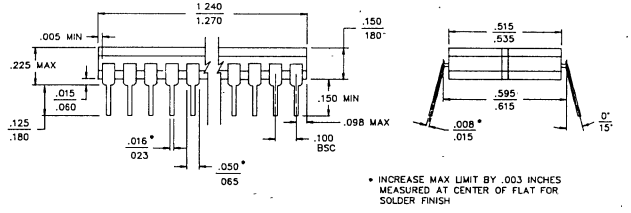
Packaging †

24 PIN (.300) CERAMIC DIP



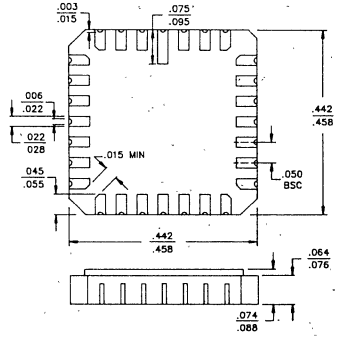
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-9

24 PIN (.600) CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-3

28 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
PAD DIMINISION: Type A
PACKAGE MATERIAL: Ceramic Al_2O_3 90%
PACKAGE SEAL:
Material: Gold/Tin
Temperature: 320°C ±10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Wedge
COMPLIANT OUTLINE: 38510 C-4

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Programming

Introduction

The HM-6642 is a 512 word by 8-bit field Programmable Read Only Memory utilizing nicrome fusible links as programmable memory elements. Selected memory locations are permanently changed from their manufactured state, of all low (VOL) to a logical high (VOH), by the controlled application of programming potentials and pulses. Careful adherence to the following programming specifications will result in high programming yield. Both high VCC (6.0V) and low VCC (4.0V) verify cycles are specified to assure the integrity of the programmed fuse. This programming specification, although complete, does not preclude rapid programming. The worst case programming time required is 37.4 seconds, and typical programming time can be approximately 4 seconds per device.

The chip ($\overline{E}$) and output enable (G) are used during the programming procedure. On PROMs which have more than one output enable control G3 is to be used. The other output enables must be held in the active, or enabled, state throughout the entire programming sequence. The programmer designer is advised that all pins of the programmer's socket should be at ground potential when the PROM is inserted into the socket. VCC must be applied to the PROM before any input or output pin is allowed to rise*.

Overall Programming Procedure

1. The address of the first bit to be programmed is presented, and latched by the chip enable ($\overline{E}$) falling edge. The output is disabled by taking the output enable G Low: The programming pin is enabled by taking (P) high.
2. VCC is raised to the programming voltage level, 12.5V.
3. All data output pins are pulled up to VCC program. Then the data output pin corresponding to the bit to be programmed is pulled low for 100μs. Only one bit should be programmed at a time.
4. The data output pin is returned to VCC, and the VCC pin is returned to 6.0V.
5. The address of the bit is again presented, and latched by a second chip enable falling edge.
6. The data outputs are enabled, and read, to verify that the bit was successfully programmed.
   a). If verified, the next bit to be programmed is addressed and programmed.
   b). If not verified, the programs verify sequence is repeated up to 8 times total.
7. After all bits to be programmed have been verified at 6.0V, the VCC is lowered to 4.0V and all bits are verified.
   a). If all bits verify, the device is properly programmed.
   b). If any bit fails to verify, the device is rejected.

Programming System Requirements

1. The power supply for the device to be programmed must be able to be set to three voltages: 4.0V, 6.0V, 12.5V. This supply must be able to supply 500mA average, and 1A dynamic, currents to the PROM during programming. The power supply rise fall times when switching between voltages must be no quicker than 1μs.
2. The address drivers must be able to supply a VIH of 4.0V and 6.0V and VIL when the system is at programming voltages.*
3. The control input buffers must be able to maintain input voltage levels of $\geq$ 70% and $\leq$ 20% VCC for VIH and VIL levels, respectively. Notice that chip enable ($\overline{E}$) and G does not require a pull up to programming voltage levels. The program control (P) must switch from ground to VIH and from VIH to the VCC PGM level.*
4. The data input buffers must be able to sink up to 3mA from the PROM's output pins without rising more than 0.7V above ground, be able to hold the other outputs high with a current source capability of 0.5mA to 2.0mA, and not interfere with the reading and verifying of the data output of the PROM. Notice that a bit to be programmed is changed from a low state (VOL) to high (VOH) by pulling low on the output pin. A suggested implementation is open collector TTL buffers (or inverters) with 4.7kΩ pull up resistors to VCC.*

* Never allow any input or output pin to rise more than 0.3V above VCC, or fall more than 0.3V below ground.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Background Information HM-6642 Programming

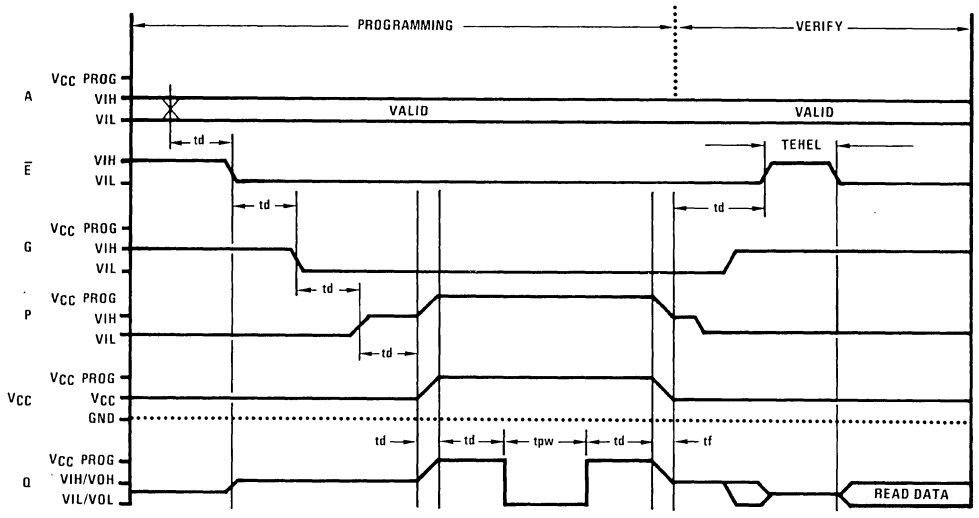
PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
VCC PROG	Programming VCC	12.0	12.0	12.5	V
VCCN	Operating VCC	4.5	5.5	5.5	V
VCC LV	Special Verify VCC	4.0	-	6.0	V
ICC	System ICC Capability	500	-	-	mA
ICC Peak	Transient ICC Capability	1.0	-	-	A
PROM INPUT PINS					
VOL	Output Low Voltage (To PROM)	-0.3	GND	20% VCC	V
VOH	Output High Voltage (To PROM)	70% VCC	VCC	VCC +0.3	V
IOL	Output Sink Current (At VOL)	0.01	-	-	mA
IOH	Output Source Current (At VOH)	0.01			mA
PROM DATA OUTPUT PINS					
VOL	Output Low Voltage (To PROM)	-0.3	GND	0.7	V
VOH	Output High Voltage (To PROM)	70% VCC	VCC	VCC +0.3	V
IOL	Output Sink Current (At VOL)	3.0			mA
IOH	Output Source Current (At VOH)	0.5	1.0	2.0	mA
td	Delay Time	1.0	1.0	-	µs
tr	Rise Time	1.0	10.0	10.0	µs
tf	Fall Time	1.0	10.0	10.0	µs
TEHEL	Chip Enable Pulse Width	500	-	-	ns
TAVEL	Address Valid to Chip Enable Low Time	500	-	-	ns
TELQV	Chip Enable Low to Output Valid Time	-	-	500	ns
tpw	Programming Pulse Width	90	100	110	µs
tIP	Input Leakage at VCC = VCC PROG	-10	+1.0	10	µA
TA	Ambient Temperature	-	25	-	°C

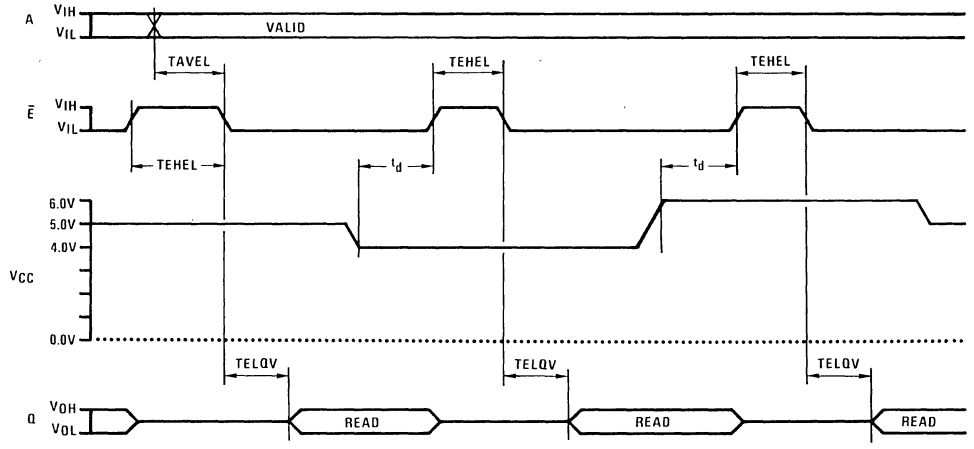
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

HM-6642 PROGRAMMING CYCLE



HM-6642 POST PROGRAMMING VERIFY CYCLE



HARRIS

HM-6617/883

June 1989

2K x 8 CMOS PROM

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby and Operating Power
  - ICCSB 100µA
  - ICCOP ..... 20mA at 1MHz
- Fast Access Time..... 90/120ns
- Industry Standard Pinout
- Single 5.0 Volt Supply
- CMOS/TTL Compatible Inputs
- High Output Drive ..... 12 LSTTL Loads
- Synchronous Operation
- On-Chip Address Latches
- Separate Output Enable
- Operating Temperature Range ..... -55°C to +125°C

Description

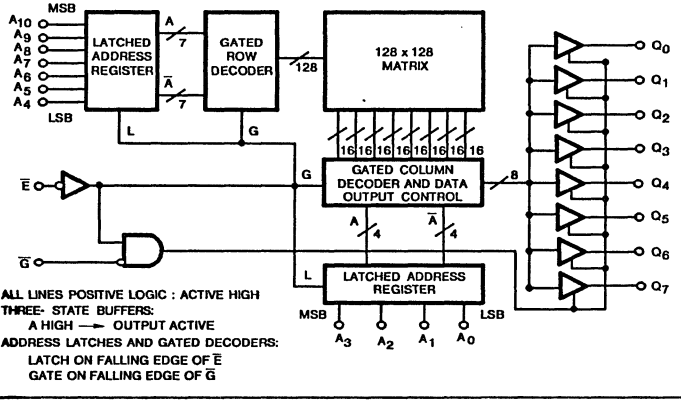
The HM-6617/883 is a 16,384 bit fuse link CMOS PROM in a 2K word by 8 bit/word format with "Three-State" outputs. This PROM is available in the standard 0.600 inch wide 24 pin Ceramic DIP, the 0.300 inch wide slimline Ceramic DIP, and the JEDEC standard 32 pad Ceramic LCC.

The HM-6617/883 utilizes a synchronous design technique. This includes on-chip address latches and a separate output enable control which makes this device ideal for applications utilizing recent generation microprocessors. This design technique, combined with the Harris advanced self-aligned silicon gate CMOS process technology offers ultra-low standby current. Low ICCSB is ideal for battery applications or other systems with low power requirements.

The Harris NiCr fuse link technology is utilized on this and other Harris CMOS PROMs. This gives the user a PROM with permanent, stable storage characteristics over the full industrial and military temperature voltage ranges. NiCr fuse technology combined with the low power characteristics of CMOS provides an excellent alternative to standard bipolar PROMs or NMOS EPROMs.

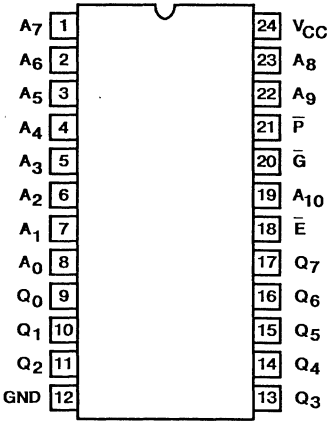
All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

Functional Diagram

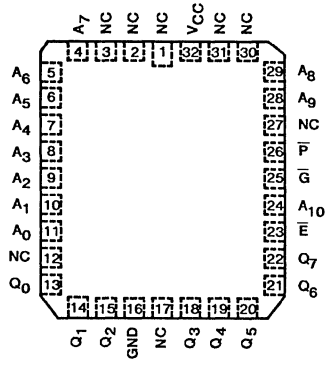


Pinouts

HM1-6617/883 (CERAMIC DIP)
TOP VIEW



HM4-6617/883 (CERAMIC LCC)
TOP VIEW



PIN	DESCRIPTION
NC	No Connect
A_0 - A_{10}	Address Inputs
$\overline{E}$	Chip Enable
Q	Data Input
VCC	Power (+5V)
$\overline{G}$	Output Enable
$\overline{P}$*	Program Enable

* $\overline{P}$ Should be Hardwired to V_{CC} Except During Programming

Absolute Maximum Ratings

Supply Voltage (All Voltages Reference to Device GND)..... +7.0V
Input or Output Voltage Applied for all Grades ..... GND-0.3V to V_{CC}+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec)..... +300°C
Junction Temperature ..... +175°C
ESD Classification ..... Class 1
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	48°C/W	9°C/W
Ceramic LCC Package	58°C/W	19°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 0.86W
Gate Count ..... 5473 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (V_{CC})..... 4.5V to 5.5V
Operating Temperature (T_A)..... -55°C to +125°C
Input Low Voltage (V_{IL}) ..... -0.3V to +0.8V
Input High Voltage (V_{IH}) ..... +2.4V to V_{CC} +0.3V

TABLE 1. HM-6617/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

D.C. PARAMETERS	SYMBOL	(NOTES 1, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	V_{OH1}	V_{CC} = 4.5V, IO = -2.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{CC} = 4.5V, IO = +4.8mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	V_{CC} = 5.5V, $\overline{G}$ = 5.5V, VI/O = GND or V_{CC}	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Input Leakage Current	II	V_{CC} = 5.5V, VI = GND or V_{CC}, $\overline{P}$ Not Tested	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	ICCSB	VI = V_{CC} or GND, V_{CC} = 5.5V, IO = 0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	µA
Operating Supply Current	ICCOP	V_{CC} = 5.5V, $\overline{G}$ = GND, (Note 3), f = 1MHz, IO = 0mA, VI = V_{CC} or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	20	mA
Functional Test	FT	V_{CC} = 4.5V (Note 12)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	

TABLE 2. HM-6617/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	TAVQV	V_{CC} = 4.5V and 5.5V (Note 5)	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	140	ns
Output Enable Access Time	TGLQV	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	50	ns
Chip Enable Access Time	TELQV	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	120	ns
Address Setup Time	TAVEL	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	20	-	ns
Address Hold Time	TELAX	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	25	-	ns
Chip Enable Low Width	TELEH	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	120	-	ns
Chip Enable High Width	TEHEL	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	40	-	ns
Read Cycle Time	TELEL	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	160	-	ns

NOTES: 1. All voltages referenced to Device GND.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL ≈ 50pF.
3. Typical derating = 5mA/MHz increase in ICCOP.
4. All tests performed with $\overline{P}$ hardwired to V_{CC}.
5. TAVQV = TELQV + TAVEL

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. HM-6617/883 A.C. AND D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 4) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 9	+25°C	-	10	pF
		V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 10	+25°C	-	12	pF
			6, 11	+25°C	-	10	pF
I/O Capacitance	$C_{I/O}$	V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 9	+25°C	-	12	pF
		V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 10	+25°C	-	14	pF
			6, 11	+25°C	-	12	pF
Chip Enable Time	TELQX	V_{CC} = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	5	-	ns
Output Enable Time	TGLQX	V_{CC} = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	5	-	ns
Chip Disable Time	TEHQZ	V_{CC} = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	-	50	ns
Output Disable Time	TGHQZ	V_{CC} = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	-	50	ns
Output High Voltage	V_{OH2}	V_{CC} = 4.5V, IO = 100µA	6	$-55°C \leq T_A \leq +125°C$	V_{CC}-1V	-	V

NOTES:
6. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after design or process changes which would affect these characteristics.
7. Tested as follows: f = 2MHz, V_{IH} = 2.4V, V_{IL} = 0.4V, I_{OH} = -4.0mA, $V_{OH} \geq$ 1.5V, and $V_{OL} \leq$ 1.5V.
8. This is a "typical" value and not a "maximum" value.
9. Applies to .600 inch Ceramic Dual-In-Line (DIP) device types only.
10. Applies to .300 inch Ceramic Dual-In-Line (DIP) device types only.
11. Applies to Ceramic Leadless Chip Carrier (LCC) device types only.
12. Tested as follows: f = 1MHz, V_{IH} = 2.4V, V_{IL} = 0.8V, I_{OH} = -1mA, I_{OL} = +1mA, $V_{OH} \geq$ 1.5V, $V_{OL} \leq$ 1.5V.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Absolute Maximum Ratings

Supply Voltage (All Voltages Reference to Device GND) ..... +7.0V
Input or Output Voltage Applied for all Grades ..... GND-0.3V to V_{CC}+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
ESD Classification ..... Class 1
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	48°C/W	9°C/W
Ceramic LCC Package	58°C/W	19°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 0.86W
Gate Count ..... 5473 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (V_{CC}) ..... 4.5V to 5.5V
Operating Temperature (T_A) ..... -55°C to +125°C
Input Low Voltage (V_{IL}) ..... -0.3V to +0.8V
Input High Voltage (V_{IH}) ..... +2.4V to V_{CC} +0.3V

TABLE 1. HM-6617B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

D.C. PARAMETERS	SYMBOL	(NOTES 1, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	V_{OH1}	V_{CC} = 4.5V, IO = -2.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{CC} = 4.5V, IO = +4.8mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	V_{CC} = 5.5V, $\overline{G}$ = 5.5V, VI/O = GND or V_{CC}	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Input Leakage Current	II	V_{CC} = 5.5V, VI = GND or V_{CC}, $\overline{P}$ Not Tested	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	ICCSB	VI = V_{CC} or GND, V_{CC} = 5.5V, IO = 0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	µA
Operating Supply Current	ICCOP	V_{CC} = 5.5V, $\overline{G}$ = GND, (Note 3), f = 1MHz, IO = 0mA, VI = V_{CC} or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	20	mA
Functional Test	FT	V_{CC} = 4.5V (Note 12)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	

TABLE 2. HM-6617B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	TAVQV	V_{CC} = 4.5V and 5.5V (Note 5)	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	105	ns
Output Enable Access Time	TGLQV	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	40	ns
Chip Enable Access Time	TELQV	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	90	ns
Address Setup Time	TAVEL	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	15	-	ns
Address Hold Time	TELAX	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	20	-	ns
Chip Enable Low Width	TELEH	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	95	-	ns
Chip Enable High Width	TEHEL	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	40	-	ns
Read Cycle Time	TELEL	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	136	-	ns

NOTES: 1. All voltages referenced to Device GND.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL ≈ 50pF.
3. Typical derating = 5mA/MHz increase in ICCOP.
4. All tests performed with $\overline{P}$ hardwired to V_{CC}.
5. TAVQV = TELQV + TAVEL

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. HM-6617B/883 A.C. AND D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 4) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 9	+25°C	-	10	pF
		V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 10	+25°C	-	12	pF
			6, 11	+25°C	-	10	pF
I/O Capacitance	$C_{I/O}$	V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 9	+25°C	-	12	pF
		V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 10	+25°C	-	14	pF
			6, 11	+25°C	-	12	pF
Chip Enable Time	TELQX	V_{CC} = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	5	-	ns
Output Enable Time	TGLQX	V_{CC} = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	5	-	ns
Chip Disable Time	TEHQZ	V_{CC} = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	-	45	ns
Output Disable Time	TGHQZ	V_{CC} = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	-	40	ns
Output High Voltage	V_{OH2}	V_{CC} = 4.5V, IO = 100µA	6	$-55°C \leq T_A \leq +125°C$	V_{CC}-1V	-	V

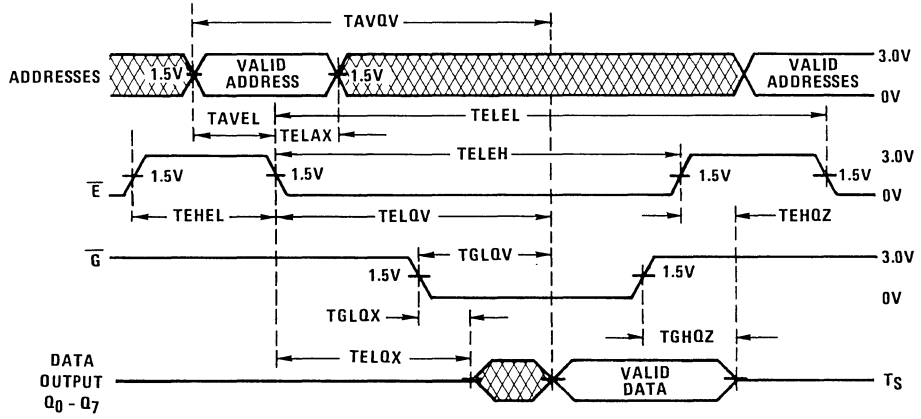
NOTES:
6. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design changes which would affect these characteristics.
7. Tested as follows: f = 2MHz, V_{IH} = 2.4V, V_{IL} = 0.4V, I_{OH} = -4.0mA, $V_{OH} \geq$ 1.5V, and $V_{OL} \leq$ 1.5V.
8. This is a typical" value and not a maximum" value.
9. Applies to .600 inch Ceramic Dual-In-Line (DIP) device types only.
10. Applies to .300 inch Ceramic Dual-In-Line (DIP) device types only.
11. Applies to Ceramic Leadless Chip Carrier (LCC) device types only.
12. Tested as follows: f = 1MHz, V_{IH} = 2.4V, V_{IL} = 0.8V, I_{OH} = -1mA, I_{OL} = +1mA, $V_{OH} \geq$ 1.5V, $V_{OL} \leq$ 1.5V.

TABLE 4. APPLICABLE SUBGROUPS

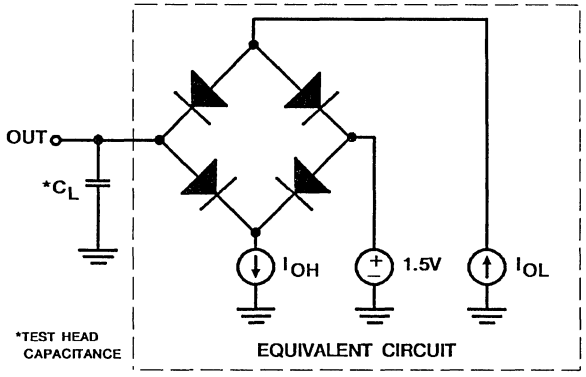
CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Switching Waveforms

READ CYCLE

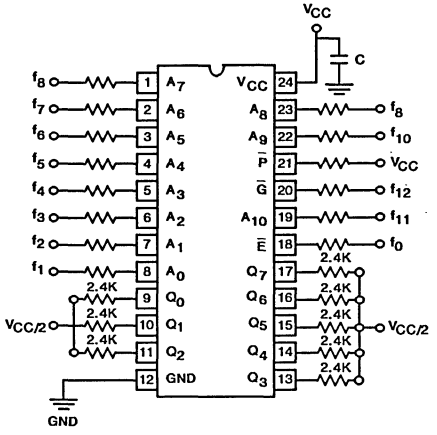


Test Circuit

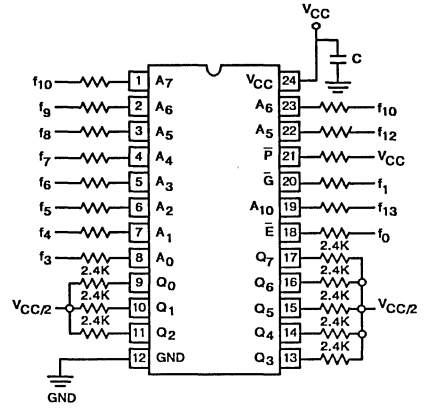


Burn-In Circuits

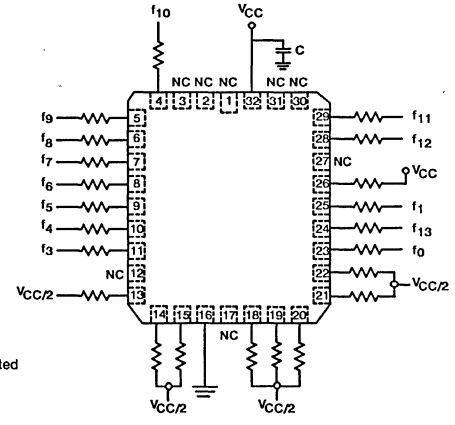
HM-6617/883 (.300 INCH) CERAMIC DIP



HM-6617/883 (.600) CERAMIC DIP



HM-6617/883 CERAMIC LCC



NOTES:

f_O = 100kHz ± 10%
All resistors = 47kΩ Unless Otherwise Noted
V_{CC} = 5.5V ± 0.05V
C = 0.01μF min

Metallization Topology

DIE DIMENSIONS:
140 x 232 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ - 15kÅ

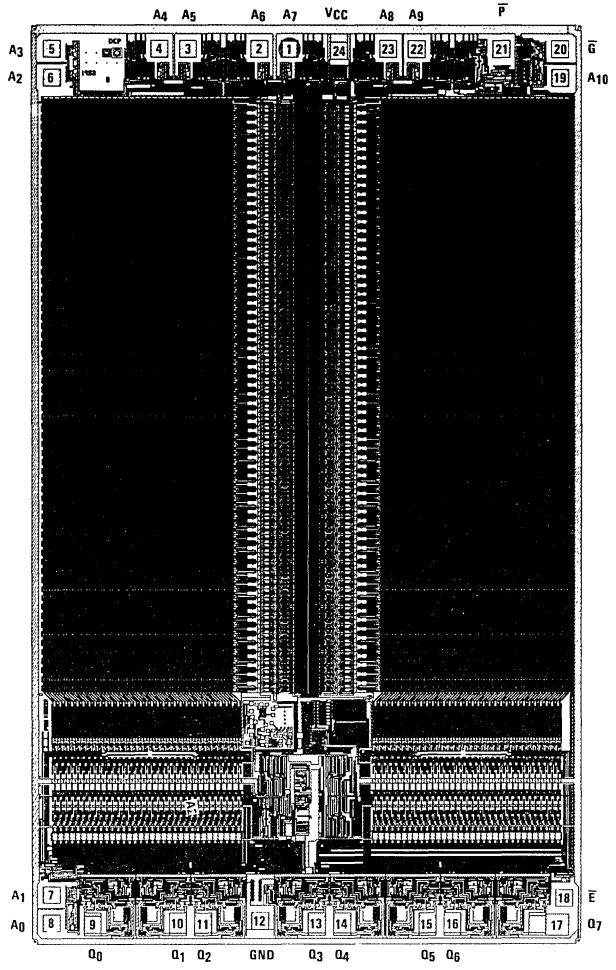
GLASSIVATION:
Type: SiO_2
Thickness: 7kÅ - 9kÅ

DIE ATTACH:
Material: Si - Au Eutectic
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.7×10^5 A/cm^2

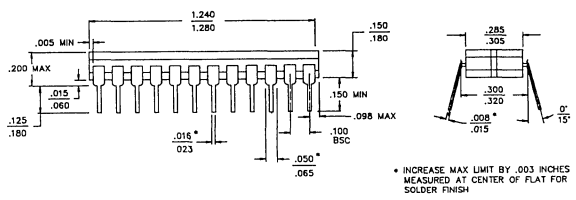
Metallization Mask Layout

HM-6617/883



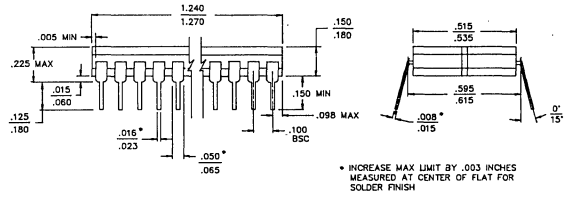
Packaging †

24 PIN (.300) CERAMIC DIP



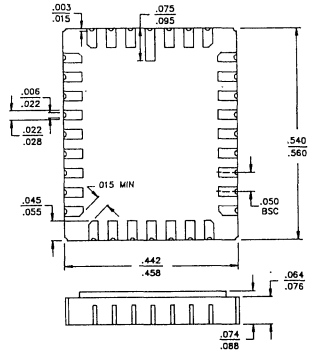
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-9

24 PIN (.600) CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-3

32 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic Al_2O_3 90%
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-12

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

DESIGN INFORMATION

2K x 8 CMOS PROM

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Background Information HM-6617 Programming

PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{IL}	Input "0"	0.0	0.2	0.8	V	
V_{IH}	Voltage "1"	V_{CC}-2	V_{CC}	V_{CC}+0.3	V	6
V_{CCPROG}	Programming V_{CC}	12.0	12.0	12.5	V	2
V_{CC1}	Operating V_{CC}	4.5	5.5	5.5	V	
V_{CC2}	Special Verify V_{CC}	4.0	-	6.0	V	3
t_d	Delay Time	1.0	1.0	-	µs	
t_r	Rise Time	1.0	10.0	10.0	µs	
t_f	Fall Time	1.0	10.0	10.0	µs	
TEHEL	Chip Enable Pulse Width	50	-	-	ns	
TAVEL	Address Valid to Chip Enable Low Time	20	-	-	ns	
TELQV	Chip Enable Low to Output Valid Time	-	-	120	ns	
t_{pw}	Programming Pulse Width	90	100	110	µs	4
I_{IP}	Input Leakage at $V_{CC} = V_{CCPROG}$	-10	+1.0	10	µA	
I_{OP}	Data Output Current at $V_{CC} = V_{CCPROG}$	-	-5.0	-10	mA	
R_n	Output Pull-Up Resistor	5	10	15	kΩ	5
T_A	Ambient Temperature	-	25	-	°C	

NOTES:

1. All inputs must track V_{CC} (pin 24) within these limits.
2. V_{CCPROG} must be capable of supplying 500mA.
3. See Steps 22 through 29 of the Programming Algorithm.
4. See Step 11 of the Programming Algorithm.
5. All outputs should be pulled up to V_{CC} through a resistor of value R_n.
6. Except during programming (See Programming Cycle Waveforms).

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Background Information Programming Algorithm

The HM-6617 CMOS PROM is manufactured with all bits containing a logical zero (output low). Any bit can be programmed selectively to a logical one (output high) state by following the procedure shown below. To accomplish this, a programmer can be built that meets the specifications shown, or any of the approved commercial programmers can be used.

PROGRAMMING SEQUENCE OF EVENTS

1) Apply a voltage of V_{CC1} to V_{CC} of the PROM.
2) Read all fuse locations to verify that the PROM is blank (output low).
3) Place the PROM in the initial state for programming: $\overline{E} = V_{IH}$, $\overline{P} = V_{IH}$, $\overline{G} = V_{IL}$.
4) Apply the correct binary address for the word to be programmed. No inputs should be left open circuit.
5) After a delay of t_d, apply voltage of V_{IL} to $\overline{E}$ (pin 18) to access the addressed word.
6) The address may be held through the cycle, but must be held valid at least for a time equal to t_d after the falling edge of $\overline{E}$. None of the inputs should be allowed to float to an invalid logic level.
7) After a delay of t_d, disable the outputs by applying a voltage of V_{IH} to $\overline{G}$ (pin 20).
8) After a delay of t_d, apply voltage of V_{IL} to $\overline{P}$ (pin 21).
9) After delay of t_d, raise V_{CC} (pin 24) to V_{CCPROG} with a rise time of t_r. All outputs at V_{IH} should track V_{CC} with V_{CC}-2.0V to V_{CC}+0.3V. This could be accomplished by pulling outputs at V_{IH} to V_{CC} through pull-up resistors of value R_n.
10) After a delay of t_d, pull the output which corresponds to the bit to be programmed to V_{IL}. Only one bit should be programmed at a time.
11) After a delay of t_{pw}, allow the output to be pulled to V_{IH} through pull-up resistor R_n.
12) After a delay of t_d, reduce V_{CC} (pin 24) to V_{CC1} with a fall time of t_f. All outputs at V_{IH} should track V_{CC} with V_{CC}-2.0V to V_{CC}+0.3V. This could be accomplished by pulling outputs at V_{IH} to V_{CC} through pull-up resistors of value R_n.
13) Apply a voltage of V_{IH} to $\overline{P}$ (pin 21).
14) After a delay of t_d, apply a voltage of V_{IL} to $\overline{G}$ (pin 20).
15) After a delay of t_d, examine the outputs for correct data. If any location verifies incorrectly, repeat steps 4 through 14 (attempting to program only those bits in the word which verified incorrectly) up to a maximum of eight attempts for a given word. If a word does not program within eight attempts, it should be considered a programming reject.
16) Repeat steps 3 through 15 for all other bits to be programmed in the PROM.

POST-PROGRAMMING VERIFICATION

17) Place the PROM in the post-programming verification mode: $\overline{E} = V_{IH}$, $\overline{G} = V_{IL}$, $\overline{P} = V_{IH}$, V_{CC} (pin 24) = V_{CC1}.
18) Apply the correct binary address of the word to be verified to the PROM.
19) After a delay of t_d, apply a voltage of V_{IL} to $\overline{E}$ (pin 18).
20) After a delay of t_d, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
21) Repeat steps 17 through 20 for all possible programming locations.

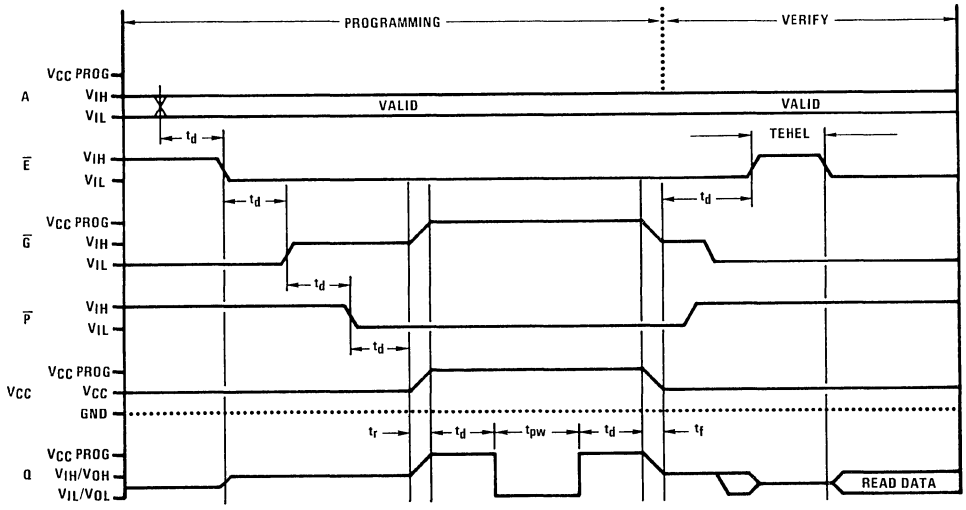
POST-PROGRAMMING READ

22) Apply a voltage of V_{CC2} = 4.0V to V_{CC} (pin 24).
23) After a delay of t_d, apply a voltage of V_{IH} to $\overline{E}$ (pin 18).
24) Apply the correct binary address of the word to be read.
25) After a delay of TAVEL, apply a voltage of V_{IL} to $\overline{E}$ (pin 18).
26) After a delay of TELQV, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
27) Repeat steps 23 through 26 for all address locations.
28) Apply a voltage of V_{CC2} = 6.0V to V_{CC} (pin 24).
29) Repeat steps 23 through 26 for all address locations.

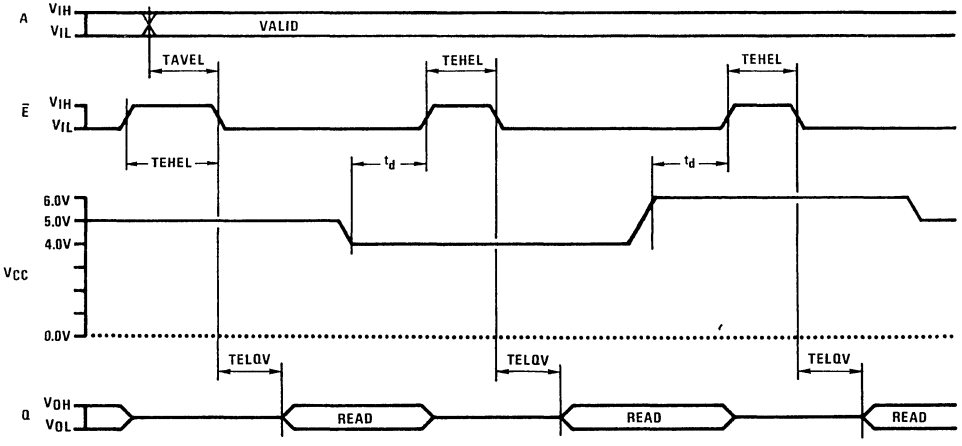
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

HM-6617 PROGRAMMING CYCLE



HM-6617 POST PROGRAMMING VERIFY CYCLE



DIGITAL

CMOS Microprocessors

4

HARRIS

80C286/883

High Performance Microprocessor With Memory Management and Protection

June 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Compatible with NMOS 80286/883
- 10MHz Operation (80C286-10/883)
- 12.5MHz Operation (80C286-12/883)
- Static CMOS Design for Low Power Operation
  - ICCSB = 5mA Maximum
  - ICCOP = 185mA Maximum (80C286-10/883)
  - ICCOP = 220mA Maximum (80C286-12/883)
- Large Address Space:
  - 16 Megabytes Physical
  - 1 Gigabyte Virtual per Task
- Integrated Memory Management, Four-Level Memory Protection and Support for Virtual Memory and Operating Systems
- Two 80C86 Upward Compatible Operating Modes:
  - 80C286/883 Real Address Mode
  - Protected Virtual Address Mode
- Compatible with 80287 Numeric Data Co-processor
- Available in 68 Pin PGA (Pin Grid Array) Package
- Wide Operating Temperature Range ..... -55°C to +125°C

Description

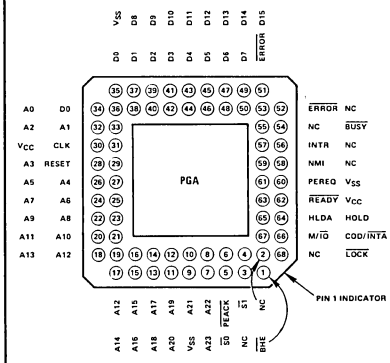
The Harris 80C286/883 is a static CMOS version of the NMOS 80286 microprocessor. The 80C286/883 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. The 80C286/883 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. The 80C286/883 includes memory management capabilities that map 2^{30} (one gigabyte) of virtual address space per task into 2^{24} bytes (16 megabytes) of physical memory.

The 80C286/883 is upwardly compatible with 80C86 and 80C88 software (the 80C286/883 instruction set is a superset of the 80C86/80C88 instruction set). Using the 80C286/883 real address mode, the 80C286/883 is object code compatible with existing 80C86 and 80C88 software. In protected virtual address mode, the 80C286/883 is source code compatible with 80C86 and 80C88 software but may require upgrading to use virtual address as supported by the 80C286/883's integrated memory management and protection mechanism. Both modes operate at full 80C286/883 performance and execute a superset of the 80C86 and 80C88 instructions.

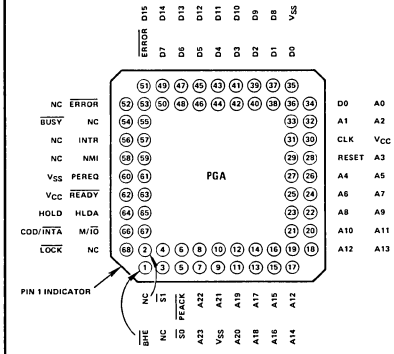
The 80C286/883 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The segment-not-present exception and restartable instructions.

Pin Configurations

Component Pad Views
As viewed from underside of the component when mounted on the board.

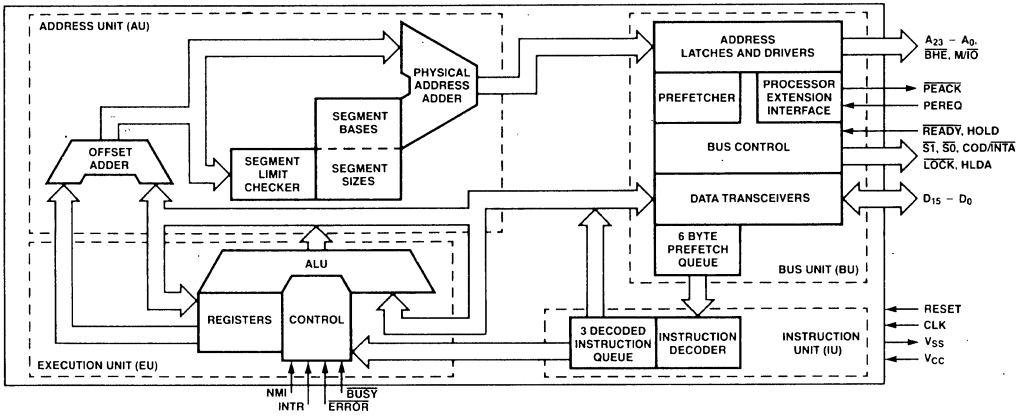


P.C. Board Views
As viewed from the component side of the P.C. board.



4 CMOS MICROPROCESSORS

Functional Diagram



Pin Description

The following pin function descriptions are for the 80C286/883 microprocessor:

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
CLK	31	I	SYSTEM CLOCK: provides the fundamental timing for the 80C286/883 system. It is divided by two inside the 80C286/883 to genenerate the processor clock. The internal divide-by-two circuitry can be synchronized to an external clock generator by a LOW to HIGH transition on the RESET input.
D15-D0	36-51	I/O	DATA BUS: inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles. The data bus is active HIGH and is held at high impedance to the last valid logic level during bus hold acknowledge.
A23-A0	7-8 10-28 32-43	O	ADDRESS BUS: outputs physical memory and I/O port addresses. A23-A16 are LOW during I/O transfers. A0 is LOW when data is to be transferred on pins D7-D0 (see table below). The address bus is active High and floats to three-state off during bus hold acknowledge.
$\overline{BHE}$	1	O	BUS HIGH ENABLE: indicates transfer of data on the upper byte of the data bus, D15-D8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is active LOW and floats to three-state OFF during bus hold acknowledge.
$\overline{S1}$, $\overline{S0}$	4, 5	O	BUS CYCLE STATUS: indicates initiation of a bus cycle and along with M/$\overline{IO}$ and COD/$\overline{INTA}$, defines the type of bus cycle. The bus is in a TS state whenever one or both are LOW. $\overline{S1}$ and $\overline{S0}$ are active LOW and are held at a high impedance logic one during bus hold acknowledge.
M/$\overline{IO}$	67	O	MEMORY I/O SELECT: distinguishes memory access from I/O access. If HIGH during TS, a memory cycle or a haltsshutdown cycle is in progress. If LOW, an I/O cycle or an interrupt acknowledge cycle is in progress. M/$\overline{IO}$ is held at high impedance to the last valid logic state during bus hold acknowledge.

$\overline{BHE}$ and A0 Encodings

$\overline{BHE}$ Value	A0 Value	Function
0	0	Word transfer
0	1	Byte transfer on upper half of data bus (D15-D8)
1	0	Byte transfer on lower half of data bus (D7-D0)
1	1	Reserved

80C286/883 Bus Cycle Status Definition

COD/$\overline{INTA}$	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle Initiated
0(LOW)	0	0	0	Interrupt acknowledge
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	None; not a status cycle
0	1	0	0	If A1 = 1 then halt; else shutdown
0	1	0	1	Memory data read
0	1	1	0	Memory data write
0	1	1	1	None; not a status cycle
1(HIGH)	0	0	0	Reserved
1	0	0	1	I/O read
1	0	1	0	I/O write
1	0	1	1	None; not a status cycle
1	1	0	0	Reserved
1	1	0	1	Memory instruction read
1	1	1	0	Reserved
1	1	1	1	None, not a status cycle

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
COD/$\overline{INTA}$	66	O	CODE/INTERRUPT ACKNOWLEDGE: distinguishes instruction fetch cycles from memory data read cycles. Also distinguishes interrupt acknowledge cycles from I/O cycles. COD/$\overline{INTA}$ is held at high impedance to the last valid logic state during bus hold acknowledge. Its timing is the same as M/$\overline{IO}$.
$\overline{LOCK}$	68	O	BUS LOCK: indicates that other system bus masters are not to gain control of the system bus for the current and following bus cycles. The $\overline{LOCK}$ signal may be activated explicitly by the "LOCK" instruction prefix or automatically by 80C286/883 hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. $\overline{LOCK}$ is active LOW and is held at a high impedance logic one during bus hold acknowledge.
$\overline{READY}$	63	I	BUS READY: terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{READY}$ LOW. $\overline{READY}$ is an active LOW synchronous input requiring setup and hold times relative to the system clock be met for correct operation. $\overline{READY}$ is ignored during bus hold acknowledge. (Note 1)
HOLD HLDA	64 65	I O	BUS HOLD REQUEST AND HOLD ACKNOWLEDGE: control ownership of the 80C286/883 local bus. The HOLD input allows another local bus master to request control of the local bus. When control is granted, the 80C286/883 will float its bus drivers and then activate HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive which results in the 80C286/883 deactivating HLDA and regaining control of the local bus. This terminates the bus hold acknowledge condition. HOLD may be asynchronous to the system clock. These signals are active HIGH. Note that HLDA never floats.
INTR	57	I	INTERRUPT REQUEST: requires the 80C286/883 to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the 80C286/883 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To ensure program interruption, INTR must remain active until an interrupt acknowledge bus cycle is initiated. INTR is sampled at the beginning of each processor cycle and must be active HIGH at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. INTR is level sensitive, active HIGH, and may be asynchronous to the system clock.
NMI	59	I	NON-MASKABLE INTERRUPT REQUEST: interrupts the 80C286/883 with an internally supplied vector value of two. No interrupt acknowledge cycles are performed. The interrupt enable bit in the 80C286/883 flag word does not affect this input. The NMI input is active HIGH, may be asynchronous to the system clock, and is edge triggered after internal synchronization. For proper recognition, the input must have been previously LOW for at least four system clock cycles and remain HIGH for at least four system clock cycles.
PEREQ $\overline{PEACK}$	61 6	I 0	PROCESSOR EXTENSION OPERAND REQUEST AND ACKNOWLEDGE: extend the memory management and protection capabilities of the 80C286/883 to processor extentions. The PEREQ input requests the 80C286/883 to perform a data operand transfer for a processor extension. The $\overline{PEACK}$ output signals the processor extension when the requested operand is being transferred. PEREQ is active HIGH. $\overline{PEACK}$ is active LOW and is held at a high impedance logic one during bus hold acknowledge. PEREQ may be asynchronous to the system clock.
$\overline{BUSY}$ $\overline{ERROR}$	54 53	I I	PROCESSOR EXTENSION BUSY AND ERROR: indicates the operating condition of a processor extension to the 80C286/883. An active $\overline{BUSY}$ input stops 80C286/883 program execution on WAIT and some ESC instructions until $\overline{BUSY}$ becomes inactive (HIGH). The 80C286/883 may be interrupted while waiting for $\overline{BUSY}$ to become inactive. An active $\overline{ERROR}$ input causes the 80C286/883 to perform a processor extension interrupt when executing WAIT or some ESC instructions. These inputs are active LOW and may be asynchronous to the system clock.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
RESET	29	I	SYSTEM RESET: clears the internal logic of the 80C286/883 and is active HIGH. The 80C286/883 may be reinitialized at any time with a LOW to HIGH transition on RESET which remains active for more than 16 system clock cycles. During RESET active, the output pins of the 80C286/883 enter the state shown below. 80C286/883 Pin State During Reset Pin Value / Pin Names 1 (HIGH) / $\overline{S0}$, $\overline{S1}$, $\overline{PEACK}$, A23-A0, $\overline{BHE}$, $\overline{LOCK}$ 0 (LOW) / M/$\overline{IO}$, COD/$\overline{INTA}$, HLDA (Note 2) HIGH IMPEDANCE / D15-D0 Operation of the 80C286/883 begins after a HIGH to LOW transition on RESET. The HIGH to LOW transition of RESET must be synchronous to the system clock. Approximately 50 system clock cycles are required by the 80C286/883 for internal initializations before the first bus cycle to fetch code from the power-on execution address is performed. A LOW to HIGH transition of RESET synchronous to the system clock will end a processor cycle at the second HIGH to LOW transition of the system clock. The LOW to HIGH transition of RESET may be asynchronous to the system clock; however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system clock period. Synchronous LOW to HIGH transitions of RESET are required only for systems where the processor clock must be phase synchronous to another clock.
VSS	9, 35, 60	I	SYSTEM GROUND: are the ground pins (all must be connected to system ground).
VCC	30, 62	I	SYSTEM POWER: +5 volt power supply pins. A 0.1 µF capacitor between pins 60 and 62 is recommended.

NOTES: 1. $\overline{READY}$ is an open-collector signal and should be pulled inactive with an 620Ω resistor.

2. HLDA is only Low if HOLD is inactive (Low).

3. All unused inputs should be pulled to their inactive state with pull up/down resistors.

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied ..... GND -1.0V to V_{CC} +1.0V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C
ESD Classification ..... Class 2

Reliability Information

θ_{jc} ..... 17°C/W (PGA Package)
θ_{ja} ..... 41°C/W (PGA Package)
Maximum Package Power Dissipation 1.22W
Typical Derating Factor ..... 17mA/MHz Increase in ICCOP
Gate Count ..... 22,500 Gates

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the deviice at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
System Clock (CLK) RISE Time (From 1.0V to 3.6V) ..... 8ns (Max)
System Clock (CLK) FALL Time (From 3.6V to 1.0V) ..... 8ns (Max)
Input RISE/FALL Time (From 0.8V to 2.0V)
80C286-10/883 ..... 10ns (Max)
80C286-12/883 ..... 8ns (Max)

TABLE 1. 80C286/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input LOW Voltage	V_{IL}	V_{CC} = 4.5V	1,2,3	-55°C ≤ T_A ≤ +125°C	-0.5	0.8	V
Input HIGH Voltage	V_{IH}	V_{CC} = 5.5V	1,2,3	-55°C ≤ T_A ≤ +125°C	2.0	V_{CC} +0.5	V
CLK Input LOW Voltage	V_{ILC}	V_{CC} = 4.5V	1,2,3	-55°C ≤ T_A ≤ +125°C	-0.5	1.0	V
CLK Input HIGH Voltage	V_{IHC}	V_{CC} = 5.5V	1,2,3	-55°C ≤ T_A ≤ +125°C	3.6	V_{CC} +0.5	V
Output LOW Voltage	V_{OL}	I_{OL} = 2.0mA, V_{CC} = 4.5V	1,2,3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
Output HIGH Voltage	V_{OH}	I_{OH} = -2.0mA, V_{CC} = 4.5V,	1,2,3	-55°C ≤ T_A ≤ +125°C	3.0	-	V
		I_{OH} = -100µA, V_{CC} = 4.5V			V_{CC} -0.4	-	V
Input Leakage Current	I_I	V_{IN} = GND or V_{CC}, V_{CC} = 5.5V, Pins 29, 31, 57, 59, 61, 63-64	1,2,3	-55°C ≤ T_A ≤ +125°C	-10	10	µA
Input Sustaining Current LOW	I_{BHL}	V_{CC} = 4.5V and 5.5V, V_{IN} = 1.0V, Note 1	1,2,3	-55°C ≤ T_A ≤ +125°C	38	200	µA
Input Sustaining Current HIGH	I_{BHH}	V_{CC} = 4.5V and 5.5V, V_{IN} = 3.0V, Note 2	1,2,3	-55°C ≤ T_A ≤ +125°C	-50	-400	µA
Input Sustaining Current on $\overline{BUSY}$ and $\overline{ERROR}$ Pins	I_{SH}	V_{CC} = 4.5V and 5.5V, V_{IN} = GND, Note 5	1,2,3	-55°C ≤ T_A ≤ +125°C	-30	-500	µA
Output Leakage Current	I_O	V_O = GND or V_{CC}, V_{CC} = 5.5V, Pins 1, 7-8, 10-28, 32-34	1,2,3	-55°C ≤ T_A ≤ +125°C	-10	10	µA
Active Power Supply Current	I_{CCOP}	80C286-10/883, Note 4	1,2,3	-55°C ≤ T_A ≤ +125°C	-	185	mA
		80C286-12/883, Note 4			-	220	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = 5.5V Note 3	1,2,3	-55°C ≤ T_A ≤ +125°C	-	5	mA

NOTES: 1. I_{BHL} should be measured after lowering V_{IN} to GND and then raising to 1.0V on the following pins: 36-51, 66, 67.
2. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering to 3.0V on the following pins: 4-6, 36-51, 66-68.
3. I_{CCSB} should be tested with the clock stopped in phase two of the processor clock cycle. V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, outputs unloaded.
4. I_{CCOP} measured at 10MHz for the 80C286-10/883 and 12.5MHz for the 80C286-12/883. V_{IN} = 2.4V or 0.4 or 0.4V, V_{CC} = 5.5V, outputs unloaded.
5. I_{SH} should be measured after raising V_{IN} to V_{CC} and then lowerng to 0V on pins 53 and 54.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. 80C286/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

A.C. Timings are Referenced to 0.8V and 2.0V Points of the Signals as Illustrated in Datasheet Waveforms, Unless Otherwise Noted. Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	80C286/883				UNITS
					10MHz		12.5MHz		
					MIN	MAX	MIN	MAX	
System Clock (CLK) Period	1	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	–	40	–	ns
System Clock (CLK) Low Time	2	V_{CC} = 4.5V and 5.5V @ 1.0V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	12	–	11	–	ns
System Clock (CLK) High Time	3	V_{CC} = 4.5V and 5.5V @ 3.6V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	16	–	13	–	ns
Asynchronous Inputs SETUP Time Note 1	4		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	–	15	–	ns
Asynchronous Inputs HOLD Time Note 1	5		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	–	15	–	ns
RESET SETUP Time	6		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	19	–	10	–	ns
RESET HOLD Time	7	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	–	0	–	ns
Read Data SETUP Time	8		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	8	–	5	–	ns
Read Data HOLD Time	9		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	4	–	4	–	ns
$\overline{\text{READY}}$ SETUP Time	10		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	26	–	20	–	ns
$\overline{\text{READY}}$ HOLD Time	11		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	25	–	20	–	ns
Status/$\overline{\text{PEACK}}$ Active Delay Note 4	12A		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	1	22	1	21	ns
Status/$\overline{\text{PEACK}}$ Inactive Delay Note 3	12B		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	1	30	1	24	ns
Address Valid Delay Note 2	13	V_{CC} = 4.5V and 5.5V, C_L = 100pF $I_L = \lvert 2mA \rvert$	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	1	35	1	32	ns
Write Data Valid Delay Note 2	14		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	40	0	31	ns
HLDA Valid Delay Note 5	15		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	47	0	25	ns

NOTES: 1. Asynchronous inputs are INTR, NMI, HOLD, PEREQ, ERROR, and BUSY. This specification is given only for testing purposes, to assure recognition at a specific CLK edge.
2. Delay from 1.0V on the CLK to 0.8V or 2.0V.
3. Delay from 1.0V on the CLK to 0.8V for Min (HOLD time) and to 2.0V for Max (inactive delay).
4. Delay from 1.0V on the CLK to 2.0V for Min (HOLD time) and to 0.8V for Max (active delay).
5. Delay from 1.0V on the CLK to 2.0V.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. 80C286/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	80C286/883				UNITS
					10MHz		12.5MHz		
					MIN	MAX	MIN	MAX	
CLK Input Capacitance	C_{CLK}	FREQ = 1MHz	5	$T_A = +25^oC$	-	10	-	10	pF
Other Input Capacitance	C_{IN}		5	$T_A = +25^oC$	-	10	-	10	pF
I/O Capacitance	$C_{I/O}$		5	$T_A = +25^oC$	-	10	-	10	pF
Address/Status/Data Float Delay	15		1, 3, 4, 5	$-55^oC \leq T_A \leq +125^oC$	0	47	0	32	ns
Address Valid to Status SETUP Time	19	$I_L = \lvert 2.0mA \rvert$	1, 2, 5	$-55^oC \leq T_A \leq +125^oC$	27	-	20	-	ns

NOTES: 1. Output Load: C_L = 100pF

2. Delay measured from address either reaching 0.8V or 2.0V (valid) to status going active reaching 0.8V or status going inactive reaching 2.0V.
3. Delay from 1.0V on the CLK to Float (no current drive) condition.
4. I_L = -6mA (V_{OH} to Float), I_L = 8mA (V_{OL} to Float).
5. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

A.C. Electrical Specifications (Continued)

82C284 and 82C288 TIMING SPECIFICATIONS ARE GIVEN FOR REFERENCE ONLY, AND NO GUARANTEE IS IMPLIED.

82C284 TIMING

SYMBOL	PARAMETER	10MHz		12.5MHz		UNIT	TEST CONDITION
		MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS							
11	$\overline{SRDY}/\overline{SRDYEN}$ Setup Time	15	–	15	–	ns	
12	$\overline{SRDY}/\overline{SRDYEN}$ Hold Time	2	–	2	–	ns	
13	$\overline{ARDY}/\overline{ARDYEN}$ Setup Time	5	–	5	–	ns	(Note 1)
14	$\overline{ARDY}/\overline{ARDYEN}$ Hold Time	30	–	25	–	ns	(Note 1)
TIMING RESPONSES							
19	PCLK Delay	0	20	0	16	ns	$C_L = 75pF$ $I_{OL} = 5mA$ $I_{OH} = -1mA$

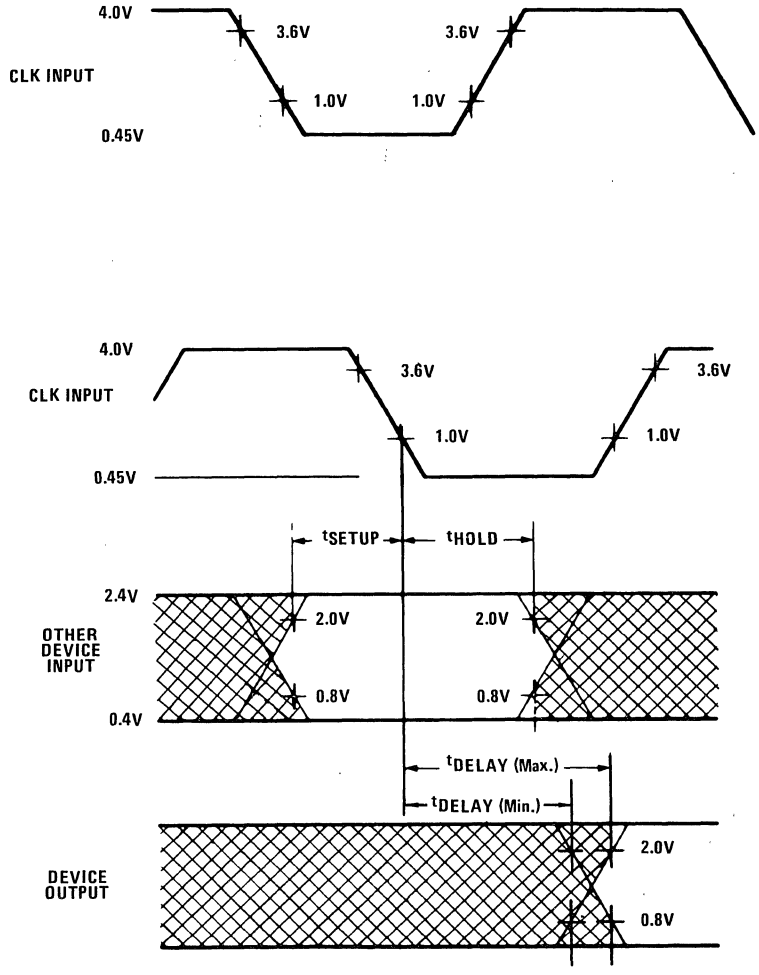
82C288 TIMING

SYMBOL	PARAMETER	10MHz		12.5MHz		UNIT	TEST CONDITION
		MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS							
12	CMDLY Setup Time	15	–	15	–	ns	
13	CMDLY Hold Time	1	–	1	–	ns	
TIMING RESPONSES							
16	ALE Active Delay	1	16	1	16	ns	
17	ALE Inactive Delay	–	19	–	19	ns	
19	$DT/\overline{R}$ Read Active Delay	–	23	–	23	ns	$C_L = 150pF$
20	DEN Read Active Delay	0	21	0	21	ns	$I_{OL} = 16mA$ Max
21	DEN Read Inactive Delay	3	23	3	21	ns	$I_{OH} = -1mA$ Max
22	$DT/\overline{R}$ Read Inactive Delay	5	24	5	18	ns	
23	DEN Write Active Delay	–	23	–	23	ns	
24	DEN Write Inactive Delay	3	23	3	23	ns	
29	Command Active Delay from CLK	3	21	3	21	ns	$C_L = 300pF$
30	Command Inactive Delay from CLK	3	20	3	20	ns	$I_{OL} = 32mA$ Max

NOTE 1. These times are given for testing purposes to ensure a predetermined action.

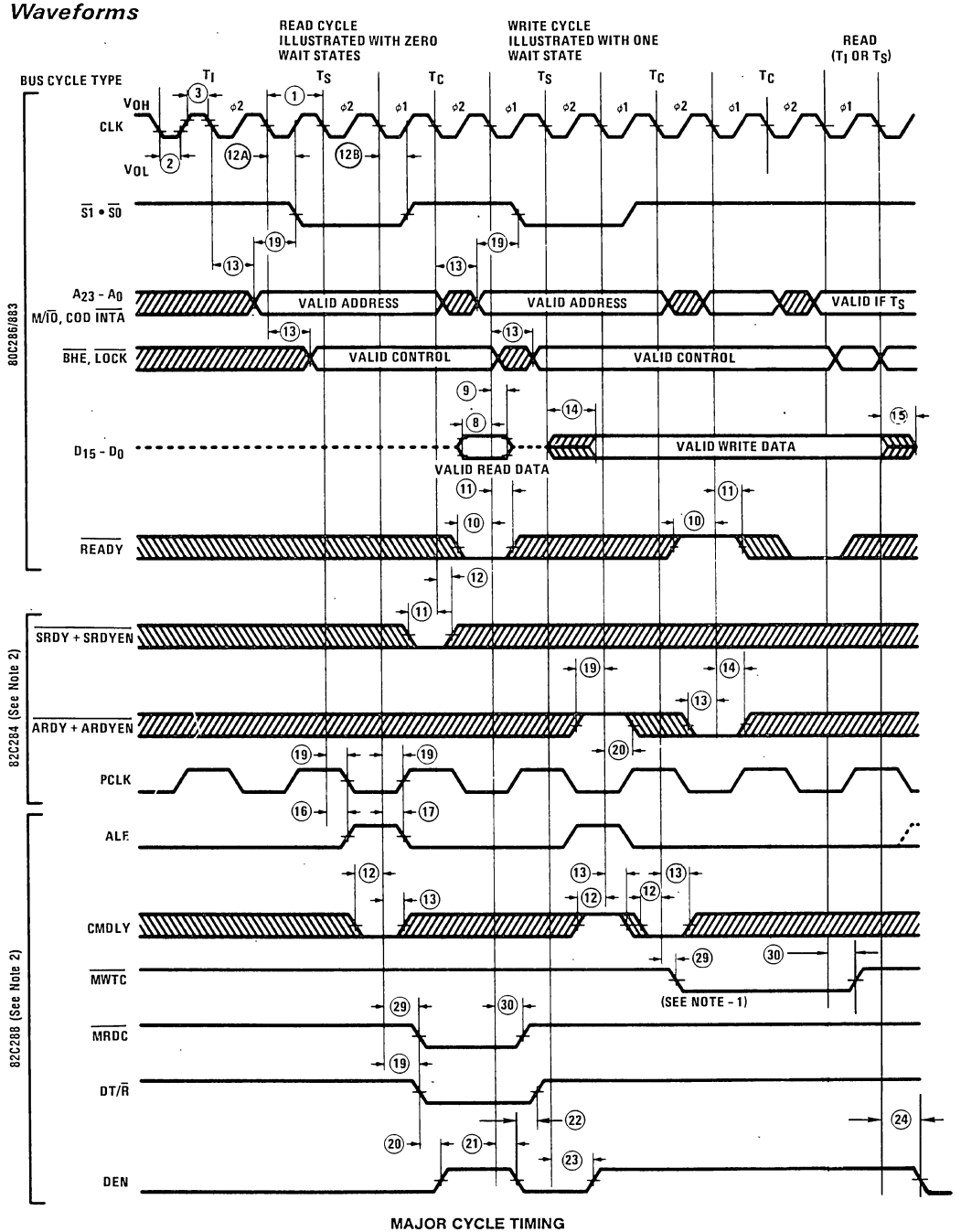
A.C. Specifications (Continued)

A.C. DRIVE AND MEASURE POINTS - CLK INPUT



NOTE:. For A.C. testing, input rise and fall times are driven at 1ns per volt.

Waveforms

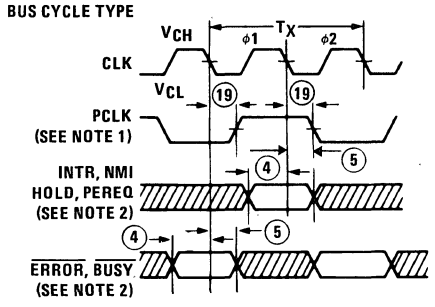


MAJOR CYCLE TIMING

NOTES: 1. The modified timing is due to the CMDLY signal being active.
2. 82C284 and 82C288 timing waveforms are shown for reference only, and no guarantee is implied.

Waveforms (Continued)

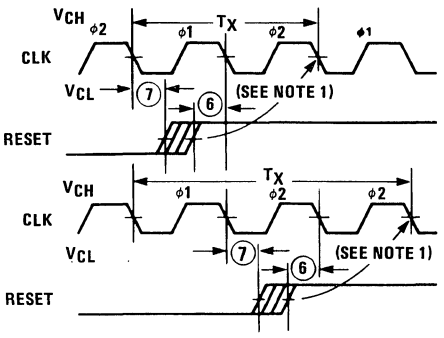
80C286/883 ASYNCHRONOUS INPUT SIGNAL TIMING



NOTES: 1. PCLK indicates which processor cycle phase will occur on the next CLK. PCLK may not indicate the correct phase until the first cycle is performed.

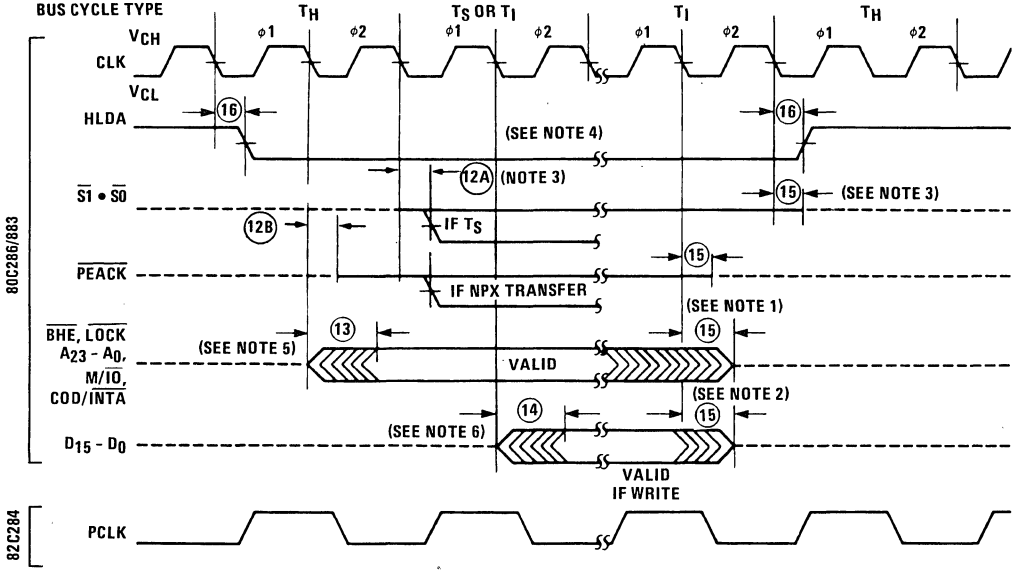
2. These inputs are asynchronous. The setup and hold times shown assure recognition for testing purposes.

80C286/883 RESET INPUT TIMING AND SUBSEQUENT PROCESSOR CYCLE PHASE



NOTE: When RESET meets the setup time shown, the next CLK will start or repeat φ2 of a processor cycle.

EXITING AND ENTERING HOLD



NOTES: 1. These signals may not be driven by the 80C286/883 during the time shown. The worst case in terms of latest float time is shown.

2. The data bus will be driven as shown if the last cycle before T_I in the diagram was a write T_C.

3. The 80C286/883 puts its status pins in a high impedance logic one state during T_H.

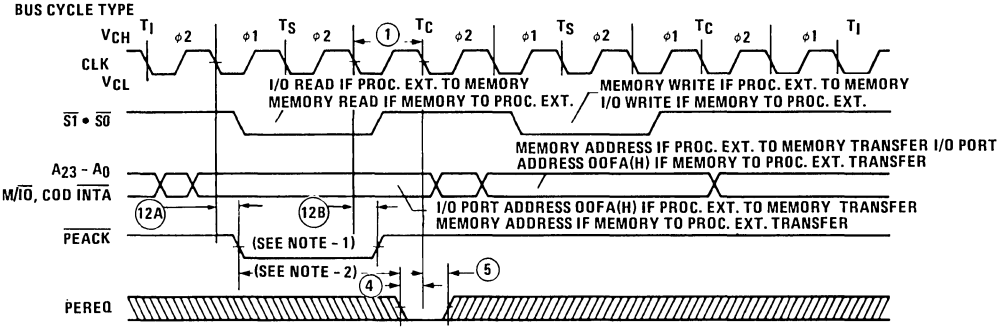
4. For HOLD request set up to HLDA, refer to Figure 29.

5. $\overline{BHE}$ and $\overline{LOCK}$ are driven at this time but will not become valid until T_S.

6. The data bus will remain in a high impedance state if a read cycle is performed.

Waveforms (Continued)

80C286/883 PEREQ/PEACK TIMING FOR ONE TRANSFER ONLY

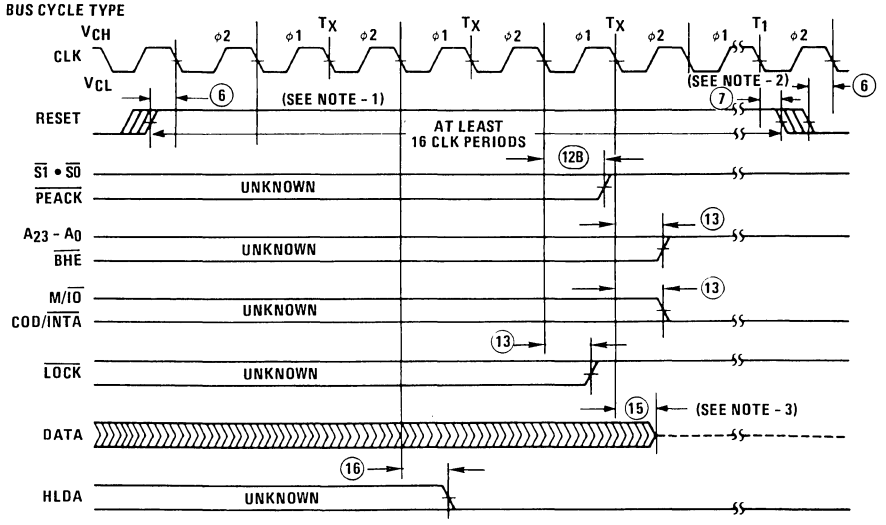


ASSUMING WORD-ALIGNED MEMORY OPERAND. IF ODD ALIGNED, 80C286/883 TRANSFERS TO/FROM MEMORY BYTE-AT-A-TIME WITH TWO MEMORY CYCLES.

NOTES: 1. $\overline{\text{PEACK}}$ always goes active during the first bus operation of a processor extension data operand transfer sequence. The first bus operation will be either a memory read at operand address or I/O read at port address 00FA(H).

2. To prevent a second processor extension data operand transfer, the worst case maximum time (Shown above) is $3 \times ① - 12A_{max.} - ④_{min.}$ The actual, configuration dependent, maximum time is: $3 \times ① - 12A_{max.} - ④_{min.} + N \times 2 \times ①$. N is the number of extra T_C states added to either the first or second bus operation of the processor extension data operand transfer sequence.

INITIAL 80C286/883 PIN STATE DURING RESET



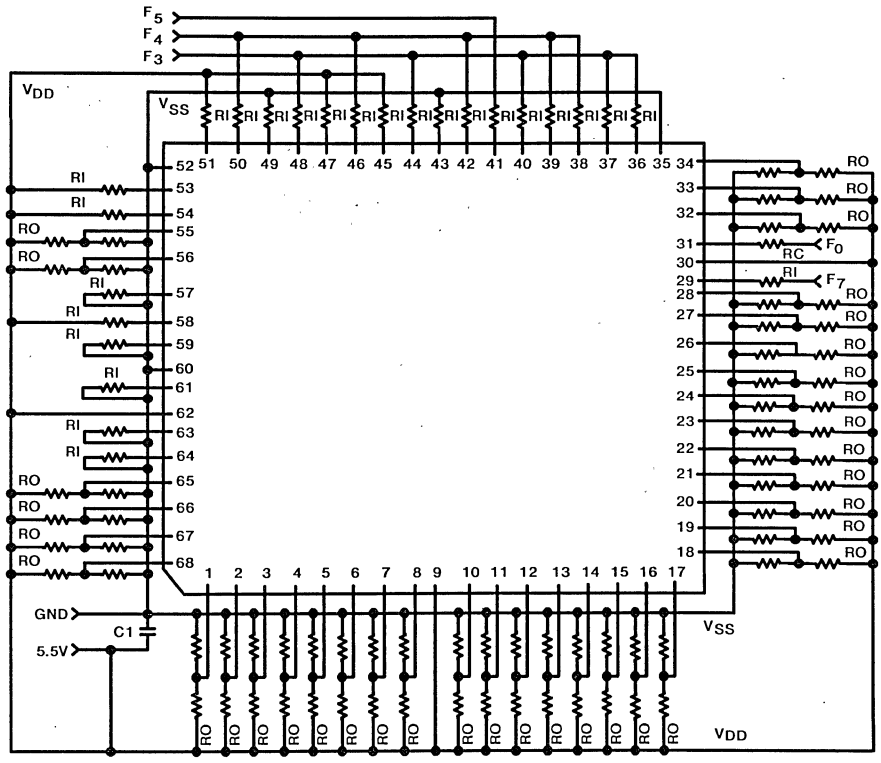
NOTES: 1. Setup time for RESET ↑ may be violated with the consideration that ϕ1 of the processor clock may begin one system CLK period later.

2. Setup and hold times for RESET ↓ must be met for proper operation, but RESET ↓ may occur during ϕ1 or ϕ2.

3. The data bus is only guaranteed to be in a high impedance state at the time shown.

Burn-In Circuit

80C286/883 PGA



NOTES:
1. Supply Voltage
   V_{DD} = 5.5V
   V_{SS} = 0.0V
2. Input Voltage Limits
   V_{IL} (Maximum) = 0.8V
   V_{IH} (Minimum) = 2.0V
3. Component Values
   RC = 1kΩ ±5%
   RI = 10kΩ ±5%
   RO = Two Series 2.7kΩ ±5%
4. Capacitor Values
   C1 = 0.1 Microfarads
5. Oven Type and Frequency Requirements
   Wakefield Oven Board f_0 = 100kHz, f_3 = 12.5kHz, f_4 = 6.25kHz, f_5 = 3.125kHz, f_7 = 781.25Hz.
6. Special Requirements
   (a) ELECTROSTATIC DISCHARGE SENSITIVE. Proper Precautions Must be Used When Handling Units.
   (b) All Power Supplies Must be at Zero Volts When the Boards are Inserted into the Ovens.
   (c) When Powering Up, the Inputs Must be Held Below the V_{DD} Voltage.
   (d) If an Excessive Current is Indicated at Final Inspection, Check to See if a Part is Inserted Backwards or is Latched Up.

Metallization Topology

DIE DIMENSIONS:
315 x 320 x 19 ± 1 mils

METALLIZATION:
Type: Si-Al
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

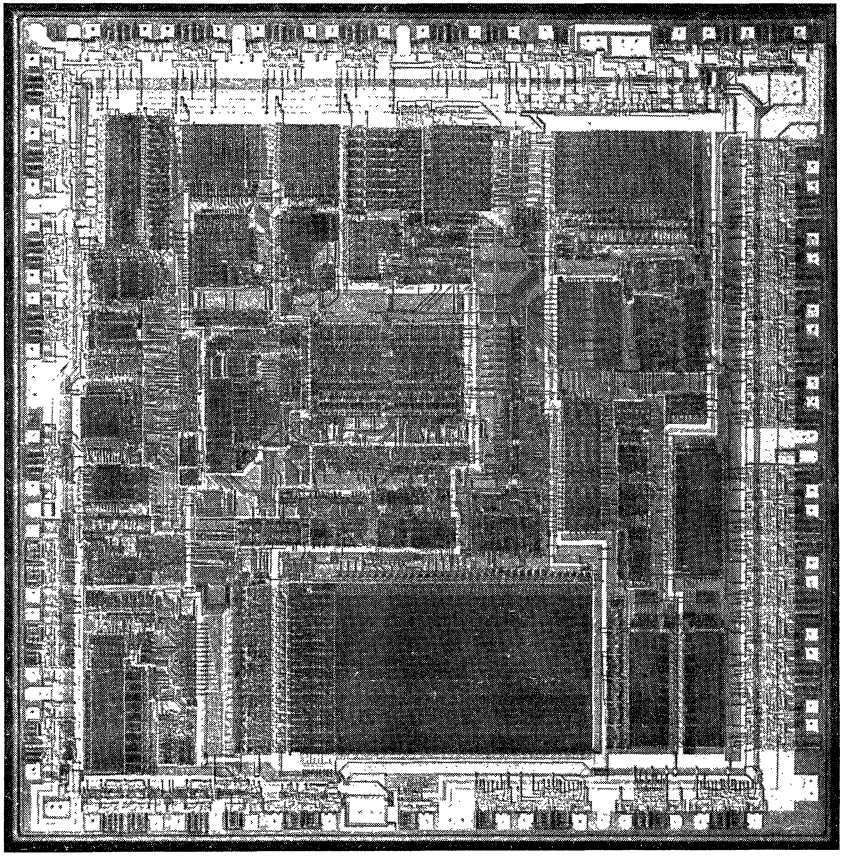
DIE ATTACH:
Material: Si-Au Eutectic Alloy
Temperature: Ceramic PGA — 420°C (Max)

WORST CASE CURRENT DENSITY: $2 \times 10^5 A/cm^2$

LEAD TEMPERATURE (10 Seconds Soldering): $\leq 300^{\circ}C$

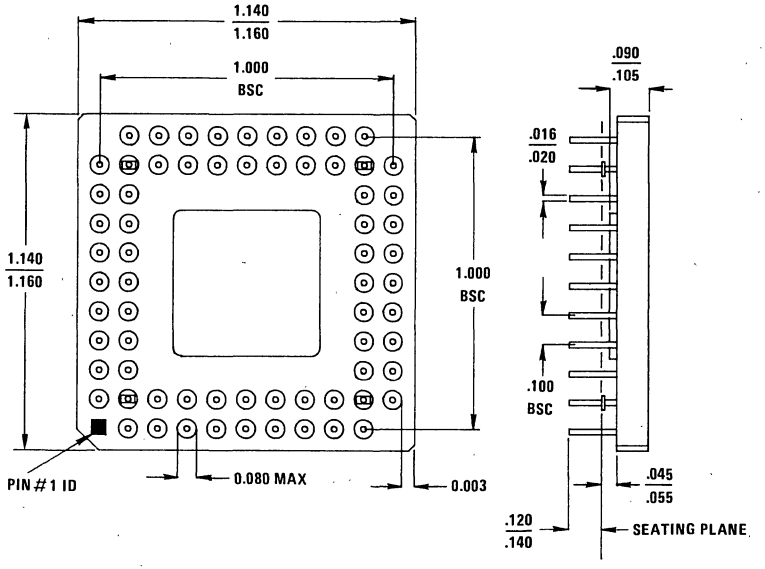
Metallization Mask Layout

80C286/883



Packaging†

68 PIN GRID ARRAY (PGA)



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-5

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Functional Description

Introduction

The Harris 80C286 microprocessor is a static CMOS version of the NMOS 80286 microprocessor. The 80C286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. Depending on the application, the 80C286's performance is up to fifteen times faster than the standard 5MHz 8086's, while providing complete upward software compatibility with Harris 80C86 and 80C88 CPU family.

The 80C286 operates in two modes: 80C286 real address mode and protected virtual address mode. Both modes execute a superset of the 80C86 and 80C88 instruction set.

In 80C286 real address mode programs use real addresses with up to one megabyte of address space. Programs use virtual addresses in protected virtual address mode, also called protected mode. In protected mode, the 80C286 CPU automatically maps 1 gigabyte of virtual addresses per task into a 16 megabyte real address space. This mode also provides memory protection to isolate the operating system and ensure privacy of each tasks' programs and data. Both modes provide the same base instruction set, registers and addressing modes.

The Functional Description describes the following: Static operation, the base 80C286 architecture common to both modes, 80C286 real address mode, and finally, protected mode.

Static Operation

The 80C286 is comprised of completely static circuitry. Internal registers, counters, and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction typically placed on microprocessors. The CMOS 80C286 can operate from DC to the specified upper frequency limit. The clock to the processor may be stopped at any point (either phase one or phase two of the processor clock cycle) and held there indefinitely. There is, however, a significant decrease in power requirement if the clock is stopped in phase two of the processor clock cycle. Details on the clock relationships will be discussed in the Bus Operation section. The ability to stop the clock to the processor is especially useful for system debug or power critical applications.

The 80C286 can be single-stepped using only the CPU clock. This state can be maintained as long as necessary. Single step clock information allows simple interface circuitry to provide critical information for system debug.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide low power operation since 80C286 power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, with the clock stopped in phase two of the processor clock cycle, the 80C286 power requirement is the standby current (5mA maximum).

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

80C286 Base Architecture

The 80C86, 80C88, and 80C286 CPU family all contain the same basic set of registers, instructions, and addressing modes. The 80C286 processor is upwardly compatible with the 80C86 and 80C88 CPU's.

Register Set

The 80C286 base architecture has fifteen registers as shown in Figure 1. These registers are grouped into the following four categories.

GENERAL REGISTERS: Eight 16-bit general purpose registers used to contain arithmetic and logical operands. Four of these (AX, BX, CX and DX) can be used either in their entirety as 16-bit words or split into pairs of separate 8-bit registers.

SEGMENT REGISTERS: Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack and data. (For usage, refer to Memory Organization.)

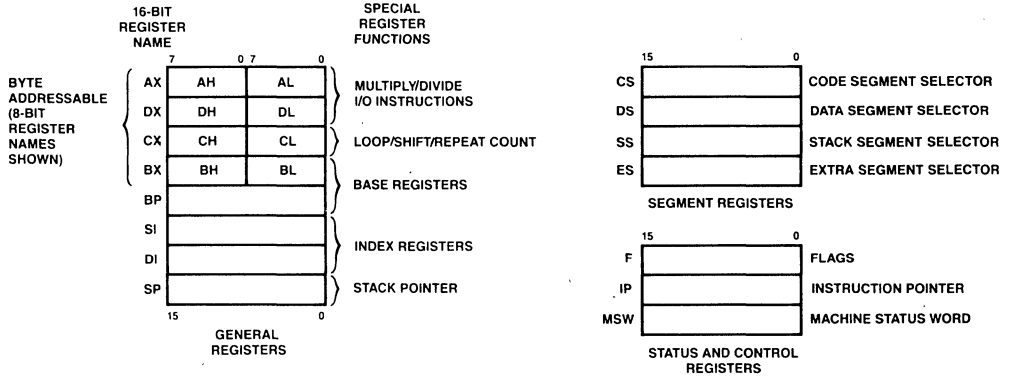


FIGURE 1. REGISTER SET

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

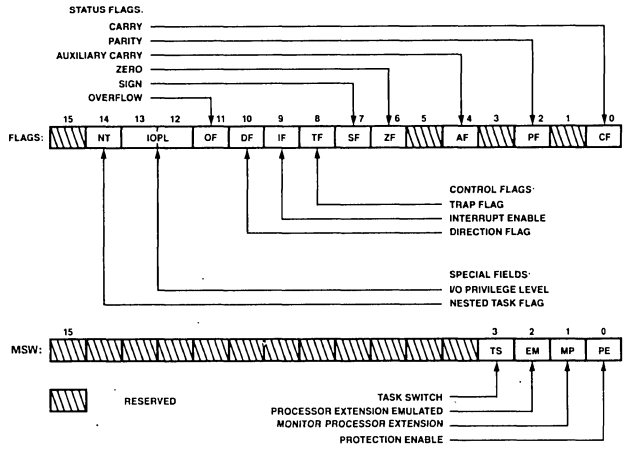


FIGURE 2. STATUS AND CONTROL REGISTER BIT FUNCTIONS

BASE AND INDEX REGISTERS: Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode determines the specific registers used for operand address calculations.

STATUS AND CONTROL REGISTERS: Three 16-bit special purpose registers record or control certain aspects of the 80C286 processor state. These include the Flags register and Machine Status Word register shown in Figure 2, and the Instruction Pointer, which contains the offset address of the next sequential instruction to be executed.

Flags Word Description

The Flags word (Flags) records specific characteristics of the result of logical and arithmetic instrucitons (bits 0, 2, 4, 6, 7 and 11) and controls the operation of the 80C286 within a given operating mode (bits 8 and 9). Flags is a 16-bit register. The function of the flag bits is given in Table A.

TABLE A. FLAGS WORD BIT FUNCTIONS

BIT POSITION	NAME	FUNCTION
0	CF	Carry Flag — Set on high-order bit carry or borrow; cleared otherwise
2	PF	Parity Flag — Set if low-order 8-bits of result contain an even number of 1-bits; cleared otherwise
4	AF	Set on carry from or borrow to the low order four bits of AL; cleared otherwise
6	ZF	Zero Flag — Set if result is zero; cleared otherwise
7	SF	Sign Flag — Set equal to high-order bit of result (0 if positive, 1 if negative)
11	OF	Overflow Flag — Set if result is a too-large positive number or a too-small negative number (excluding sign-bit) to fit in destination operand; cleared otherwise
8	TF	Single Step Flag — Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt-enable Flag — When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location
10	DF	Direction Flag — Causes string instructions to auto decrement the appropriate index registers when set. Clearing DF causes auto increment.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shiftsrotateslogical, string manipulation, control transfer, high level instructions, and processor control. These categories are summarized in Figure 3.

An 80C286 instruction can reference zero, one, or two operands; where an operand may reside in a register, in the instruction itself, or in memory. Zero-operand instructions (e.g. NOP ane HLT) are usually one byte long. One-operand instructions (e.g. INC and DEC) are usually two bytes long but some are encoded in only one byte. One-operand instructions may reference a register or memory location. Two-operand instructions permit the following six types of instruction operations:

- Register to Register
- Memory to Register
- Immediate to Register
- Memory to Memory
- Register to Memory
- Immediate to Memory

Two-operand instructions (e.g. MOV and ADD) are usually three to six bytes long. Memory to memory operations are provided by a special class of string instructions requiring one to three bytes. For detailed instruction formats and encodings refer to the instruction set summary at the end of this document.

GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack

FIGURE 3A. DATA TRANSFER INSTRUCTIONS

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero

FIGURE 3C. STRING INSTRUCTIONS

ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte or word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

FIGURE 3B. ARITHMETIC INSTRUCTIONS

LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word

FIGURE 3D. SHIFT/ROTATE LOGICAL INSTRUCTIONS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

CONDITIONAL TRANSFERS		UNCONDITIONAL TRANSFERS	
JA/JNBE	Jump if above/not below nor equal	CALL	Call procedure
JAE/JNB	Jump if above or equal/not below	RET	Return from procedure
JB/JNAE	Jump if below/not above nor equal	JMP	Jump
JBE/JNA	Jump if below or equal/not above		
JC	Jump if carry	ITERATION CONTROLS	
JE/JZ	Jump if equal/zero		
JG/JNLE	Jump if greater/not less nor equal	LOOP	Loop
JGE/JNL	Jump if greater or equal/not less	LOOPE/LOOPZ	Loop if equal/zero
JL/JNGE	Jump if less/not greater nor equal	LOOPNE/LOOPNZ	Loop if not equal/not zero
JLE/JNG	Jump if less or equal/not greater	JCXZ	Jump if register CX = 0
JNC	Jump if not carry		
JNE/JNZ	Jump if not equal/not zero	INTERRUPTS	
JNO	Jump if not overflow		
JNP/JPO	Jump if not parity/parity odd	INT	Interrupt
JNS	Jump if not sign	INTO	Interrupt if overflow
JO	Jump if overflow	IRET	Interrupt return
JP/JPE	Jump if parity/parity even		
JS	Jump if sign		

FIGURE 3E. PROGRAM TRANSFER INSTRUCTIONS

FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for $\overline{\text{TEST}}$ pin active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
EXECUTION ENVIRONMENT CONTROL	
LMSW	Load machine status word
SMSW	Store machine status word

FIGURE 3F. PROCESSOR CONTROL INSTRUCTIONS

ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Detects values outside prescribed range

FIGURE 3G. HIGH LEVEL INSTRUCTIONS

Memory Organization

Memory is organized as sets of variable-length segments. Each segment is a linear contiguous sequence of up to 64K (216) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit segment selector and a 16-bit offset. The segment selector indicates the desired segment in memory. The offset component indicates the desired byte address within the segment. (See Figure 4).

All instructions that address operands in memory must specify the segment and the offset. For speed and compact instruction encoding, segment selectors are usually stored in the high speed segment registers. An instruction need specify only the desired segment register and offset in order to address a memory operand.

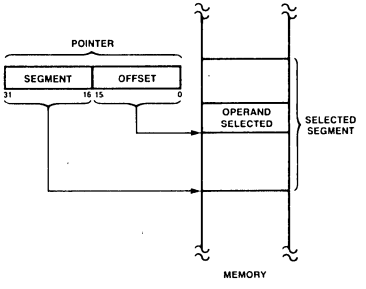


FIGURE 4. TWO COMPONENT ADDRESS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

TABLE B. SEGMENT REGISTER SELECTION RULES

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Automatic with instruction prefetch
Stack	Stack (SS)	All stack pushes and pops. Any memory reference which uses BP as a base register.
Local Data	Data (DS)	All data references except when relative to stack or string destination
External (Global) Data	Extra (ES)	Alternate data segment and destination of string operation

Most instructions need not explicitly specify which segment register is used. The correct segment register is automatically chosen according to the rules of Table B. These rules follow the way programs are written (see Figure 5) as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overriden for special cases. The stack, data and extra segments may coincide for simple programs. To access operands not residing in one of the four immediately available segments, a full 32-bit pointer or a new segment selector must be loaded.

Addressing Modes

The 80C286 provides a total of eight addressing modes for instructions to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

REGISTER OPERAND MODE: The operand is located in one of the 8 or 16-bit general registers.

IMMEDIATE OPERAND MODE: The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: segment selector and offset. The segment selector is supplied by a segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset is calculated by summing any combination of the following three address elements:

the **displacement** (an 8 or 16-bit immediate value contained in the instruction)

the **base** (contents of either the BX or BP base registers)

the **index** (contents of either the SI or DI index registers)

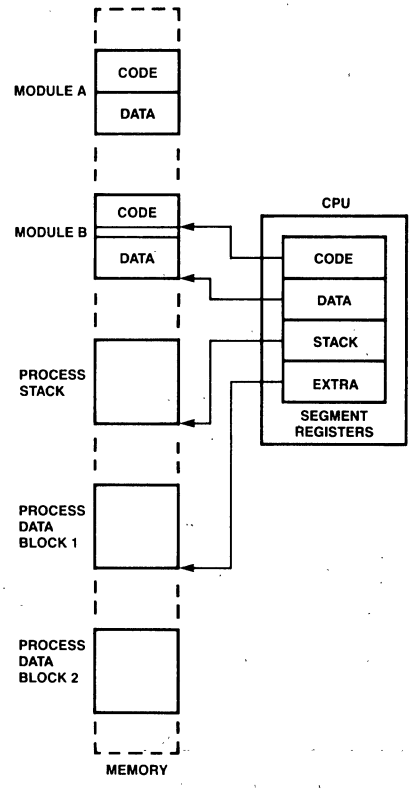


FIGURE 5. SEGMENTED MEMORY HELPS STRUCTURE SOFTWARE

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Any carry out from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

DIRECT MODE: The operand's offset is contained in the instruction as an 8 or 16-bit displacement element.

REGISTER INDIRECT MODE: The operand's offset is in one of the registers SI, DI, BX or BP.

BASED MODE: The operand's offset is the sum of an 8 or 16-bit displacement and the contents of a base register (BX or BP).

INDEXED MODE: The operand's offset is the sum of an 8 or 16-bit displacement and the contents of an index register (SI or DI).

BASED INDEXED MODE: The operand's offset is the sum of the contents of a base register and an index register.

BASED INDEXED MODE WITH DISPLACEMENT: The operand's offset is the sum of a base register's contents, an index register's contents, and an 8 or 16-bit displacement.

Data Types

The 80C286 directly supports the following data types:

Integer: A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32 and 64-bit integers are supported using the 80287 Numeric Data Processor.

Ordinal: An unsigned binary numeric value contained in an 8-bit byte or 16-bit word.

Pointer: A 32-bit quantity, composed of a segment selector component and an offset component. Each component is a 16-bit word.

String: A contiguous sequence of bytes or words. A string may contain from 1 byte to 64K bytes.

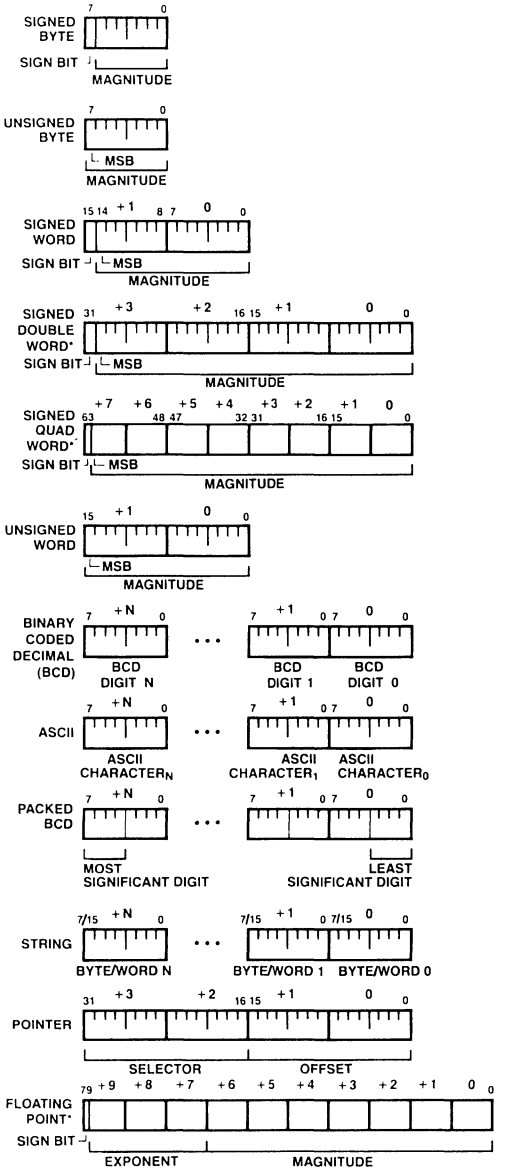
ASCII: A byte representation of alphanumeric and control characters using the ASCII standard of character representation.

BCD: A byte (unpacked) representation of the decimal digits 0-9.

Packed BCD: A byte (packed) representation of two decimal digits 0-9 storing one digit in each nibble of the byte.

Floating Point: A signed 32, 64 or 80-bit real number representation. (Floating point operands are supported using the 80287 Numeric Processor extension).

Figure 6 graphically represents the data types supported by the 80C286.



*Supported by 80C286 80287 Numeric Data Processor Configuration

FIGURE 6. 80C286 SUPPORTED DATA TYPES

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

TABLE C. INTERRUPT VECTOR ASSIGNMENTS

FUNCTION	INTERRUPT NUMBER	RELATED INSTRUCTIONS	DOES RETURN ADDRESS POINT TO INSTRUCTION CAUSING EXCEPTION?
Divide error exception	0	DIV, IDIV	Yes
Single step interrupt	1	All	
NMI interrupt	2	INT 2 or NMI pin	
Breakpoint interrupt	3	INT 3	
INTO detected overflow exception	4	INTO	No
BOUND range exceeded exception	5	BOUND	Yes
Invalid opcode exception	6	Any undefined opcode	Yes
Processor extension not available exception	7	ESC of WAIT	Yes
Reserved-do not use	8-15		
Processor extension error interrupt	16	ESC or WAIT	
Reserved	17-31		
User defined	32-255		

I/O Space

The I/O space consists of 64K 8-bit ports, 32K 16-bit ports, or a combination of the two. I/O instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero extended such that A_{15}-A_8 are LOW. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (Flags) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware initiated interrupts occur in response to an external input and are classified as non-maskable or maskable. Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition which prevents further instruction processing is detected while attempting to execute an instruction. The return address from an exception will always point to the instruction causing the exception and include any leading instruction prefixes.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0-31, some of which are used for instruction exceptions, are reserved. For each interrupt, an 8-bit vector must be supplied to the 80C286 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Non-maskable hardware interrupts use a predefined internally supplied vector.

Maskable Interrupt (INTR)

The 80C286 provides a maskable hardware interrupt request pin, INTR. Software enables this input by setting the interrupt flag bit (IF) in the flag word. All 224 user-defined interrupt sources can share this input, yet they can retain separate interrupt handlers. An 8-bit vector read by the CPU during the interrupt acknowledge sequence (discussed in System Interface section) identifies the source of the interrupt.

The processor automatically disables further maskable interrupts internally by resetting the IF as part of the response to an interrupt or exception. The saved flag word will reflect the enable status of the processor prior to the interrupt. Until the flag word is restored to the flag register, the interrupt flag will be zero unless specifically set. The interrupt return instruction includes restoring the flag word, thereby restoring the original status of IF.

Non-Maskable Interrupt Request (NMI)

A non-maskable interrupt input (NMI) is also provided. NMI has higher priority than INTR. A typical use of NMI would be to activate a power failure routine. The activation of this input causes an interrupt with an internally supplied vector value of 2. No external interrupt acknowledge sequence is performed.

While executing the NMI servicing procedure, the 80C286 will service neither further NMI requests, INTR requests, nor the processor extension segment overrun interrupt until an interrupt return (IRET) instruction is executed or the CPU is reset. If NMI occurs while currently servicing an NMI, its presence will be saved for servicing after executing the first IRET instruction. IF is cleared at the beginning of an NMI interrupt to inhibit INTR interrupts.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Single Step Interrupt

The 80C286 has an internal interrupt that allows programs to execute one instruction at a time. It is called the single step interrupt and is controlled by the single step flag bit (TF) in the flag word. Once this bit is set, an internal single step interrupt will occur after the next instruction has been executed. The interrupt clears the TF bit and uses an internally supplied vector of 1. The IRET instruction is used to set the TF bit and transfer control to the next instruction to be single stepped.

Interrupt Priorities

When simultaneous interrupt requests occur, they are processed in a fixed order as shown in Table D. Interrupt processing involves saving the flags, return address, and setting CS:IP to point at the first instruction of the interrupt handler. If another enabled interrupt should occur, it is processed before the next instruction of the current interrupt handler is executed. The last interrupt processed is therefore the first one serviced.

TABLE D. INTERRUPT PROCESSING ORDER

ORDER	INTERRUPT
1	Instruction exception
2	Single step
3	NMI
4	Processor extension segment overrun
5	INTR
6	INT instruction

Initialization and Processor Reset

Processor initialization or start up is accomplished by driving the RESET input pin HIGH. RESET forces the 80C286 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as RESET is active. After RESET becomes inactive, and an internal processing interval elapses, the 80C286 begins execution in real address mode with the instruction at physical location FFFFF0(H). RESET also sets some registers to predefined values as shown in Table E.

TABLE E. 80C286 INITIAL REGISTER STATE AFTER RESET

Flag word	0002(H)
Machine status word	FFF0(H)
Instruction pointer	FFF0(H)
Code segment	F000(H)
Data segment	0000(H)
Extra segment	0000(H)
Stack segment	0000(H)

HOLD must not be active during the time from the leading edge of the initial RESET to 34 CLKs after the trailing edge of the initial RESET of an 80C286 system.

Machine Status Word Description

The machine status word (MSW) records when a task switch takes place and controls the operating mode of the 80C286. It is a 16-bit register of which the lower four bits are used. One bit places the CPU into protected mode, while the other three bits, as shown in Table F, control the

TABLE F. MSW BIT FUNCTIONS

BIT POSITION	NAME	FUNCTION
0	PE	Protected mode enable places the 80C286 into protected mode and cannot be cleared except by RESET.
1	MP	Monitor processor extension allows WAIT instructions to cause a processor extension not present exception (number 7).
2	EM	Emulate processor extension causes a processor extension not present exception (number 7) on ESC instructions to allow emulating a processor extension.
3	TS	Task switched indicates the next instruction using a processor extension will cause exception 7, allowing software to test whether the current processor extension context belongs to the current task.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

TABLE G. RECOMMENDED MSW ENCODINGS FOR PROCESSOR EXTENSION CONTROL

TS	MP	EM	RECOMMENDED USE	INSTRUCTIONS CAUSING EXCEPTION 7
0	0	0	Initial encoding after RESET. 80C286 operation is identical to 80C86/88	None
0	0	1	No processor extension is available. Software will emulate its function.	ESC
1	0	1	No processor extension is available. Software will emulate its function. The current processor extension context may belong to another task.	ESC
0	1	0	A processor extension exists.	None
1	1	0	A processor extension exists. The current processor extension context may belong to another task. The exception 7 on WAIT allows software to test for an error pending from a previous processor extension operation	ESC or WAIT

processor extension interface. After RESET, this register contains FFF0(H) which places the 80C286 in 80C286 real address mode.

The LMSW and SMSW instructions can load and store the MSW in real address mode. The recommended use of TS, EM, and MP is shown in Table G.

Halt

The HLT instruction stops program execution and prevents the CPU from using the local bus until restarted. Either NMI, INTR with IF = 1, or RESET will force the 80C286 out of halt. If interrupted, the saved CS:IP will point to the next instruction after the HLT.

80C286 Real Address Mode

The 80C286 executes a fully upward-compatible superset of the 80C86 instruction set in real address mode. In real address mode the 80C286 is object code compatible with 80C86 and 80C88 software. The real address mode architecture (registers and addressing modes) is exactly as described in the 80C286 Base Architecture section of this Functional Description.

Memory Size

Physical memory is a contiguous array of up to 1,048,576 bytes (one megabyte) addressed by pins A_0 through A_{19} and $\overline{BHE}$. A_{20} through A_{23} should be ignored.

Memory Addressing

In real address mode physical memory is a contiguous array of up to 1,048,576 bytes (one megabyte) addressed by pin A_0 through A_{19} and $\overline{BHE}$. Address bits A_{20}-A_{23} may not always be zero in real mode. A_{20}-A_{23} should not be used by the system while the 80C286 is operating in Real Mode.

The selector portion of a pointer is interpreted as the upper 16-bits of a 20-bit segment address. The lower four bits of the 20-bit segment address are always zero. Segment addresses, therefore, begin on multiples of 16 bytes. See Figure 7 for a graphic representation of address information.

All segments in real address mode are 64K bytes in size and may be read, written, or executed. An exception or interrupt can occur if data operands or instructions attempt to wrap around the end of a segment (e.g. a word with its low order byte at offset FFFF(H) and its high order byte at offset 0000(H). If, in real address mode, the information contained in a segment does not use the full 64K bytes, the unused end of the segment may be overlayed by another segment to reduce physical memory requirements.

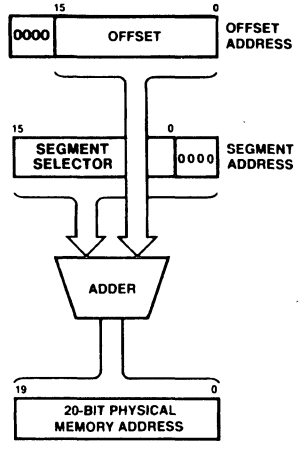


FIGURE 7. 80C286 REAL ADDRESS MODE ADDRESS CALCULATION

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

TABLE H. REAL ADDRESS MODE ADDRESSING INTERRUPTS

FUNCTION	INTERRUPT NUMBER	RELATED INSTRUCTIONS	RETURN ADDRESS BEFORE INSTRUCTION
Interrupt table limit too small exception	8	INT vector is not within table limit	Yes
Processor extension segment overrun interrupt	9	ESC with memory operand extending beyond offset FFFF(H)	No
Segment overrun exception	13	Word memory reference with offset = FFFF(H) or an attempt to execute past the end of a segment	Yes

Reserved Memory Locations

The 80C286 reserves two fixed areas of memory in real address mode (see Figure 8); system initialization area and interrupt table area. Locations from addresses FFFF0(H) through FFFFF(H) are reserved for system initialization. Initial execution begins at location FFFF0(H). Locations 00000(H) through 003FF(H) are reserved for interrupt vectors.

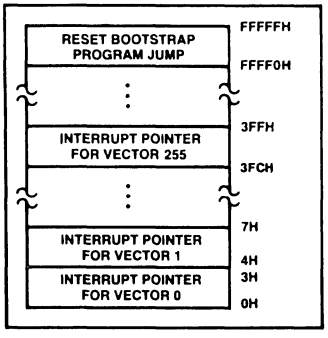


FIGURE 8. 80C286 REAL ADDRESS MODE INITIALLY RESERVED MEMORY LOCATIONS

Interrupts

Table H shows the interrupt vectors reserved for exceptions and interrupts which indicate an addressing error. The exceptions leave the CPU in the state existing before attempting to execute the failing instruction (except for PUSH, POP, PUSHA, or POPA). Refer to the next section on protected mode initialization for a discussion on exception 8.

Protected Mode Initialization

To prepare the 80C286 for protected mode, the LIDT instruction is used to load the 24-bit interrupt table base and 16-bit limit for the protected mode interrupt table. This instruction can also set a base and limit for the interrupt vector table in real address mode. After reset, the interrupt table base is initialized to 000000(H) and its size set to 03FF(H). These values are compatible with 80C86 and 80C88 software. LIDT should only be executed in preparation for protected mode.

Shutdown

Shutdown occurs when a severe error is detected that prevents further instruction processing by the CPU. Shutdown and halt are externally signalled via a halt bus operation. They can be distinguished by A_1 HIGH for halt and A_1 LOW for shutdown. In real address mode, shutdown can occur under two conditions:

- Exceptions 8 or 13 happen and the IDT limit does not include the interrupt vector.
- A CALL INT or PUSH instruction attempts to wrap around the stack segment when SP is not even.

An NMI input can bring the CPU out of shutdown if the IDT limit is at least 000F(H) and SP is greater than 0005(H), otherwise shutdown can only be exited via the RESET input.

Protected Virtual Address Mode

The 80C286 executes a fully upward-compatible superset of the 80C86 instruction set in protected virtual address mode (protected mode). Protected mode also provides memory management and protection mechanisms and associated instructions.

The 80C286 enters protected virtual address mode from real address mode by setting the PE (Protection Enable) bit of the machine status word with the Load Machine Status Word (LMSW) instruction. Protected mode offers extended physical and virtual memory address space, memory protection mechanisms, and new operations to support operating systems and virtual memory.

All registers, instructions, and addressing modes described in the 80C286 Base Architecture section of this Functional Description remain the same. Programs for the 80C86, 80C88, and real address mode 80C286 can be run in protected mode; however, embedded constants for segment selectors are different.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Memory Size

The protected mode 80C286 provides a 1 gigabyte virtual address space per task mapped into a 16 megabyte physical address space defined by the address pins A_{23}-A_0 and $\overline{BHE}$. The virtual address space may be larger than the physical address space since any use of an address that does not map to a physical memory location will cause a restartable exception.

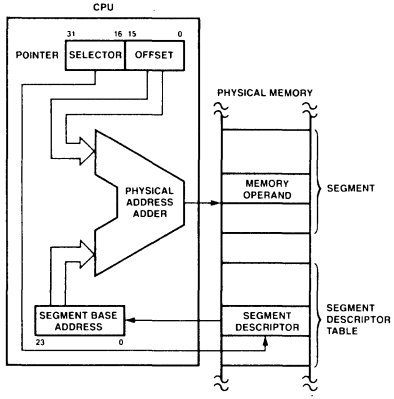


FIGURE 9. PROTECTED MODE MEMORY ADDRESSING

Memory Addressing

As in real address mode, protected mode uses 32-bit pointers, consisting of 16-bit selector and offset components. The selector, however, specifies an index into a memory resident table rather than the upper 16-bits of a real memory address. The 24-bit base address of the desired segment is obtained from the tables in memory. The 16-bit offset is added to the segment base address to form the physical address as shown in Figure 9. The tables are automatically referenced by the CPU whenever a segment register is loaded with a selector. All 80C286 instructions which load a segment register will reference the memory based tables without additional software. The memory based tables contain 8 byte values called descriptors.

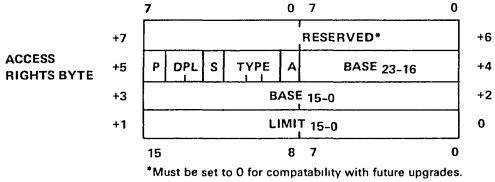
Descriptors

Descriptors define the use of memory. Special types of descriptors also define new functions for transfer of control and task switching. The 80C286 has segment descriptors for code, stack and data segments, and system control descriptors for special system data segments and control transfer operations. Descriptor accesses are performed as locked bus operations to assure descriptor integrity in multi-processor systems.

Code and Data Segment Descriptors (S = 1)

Besides segment base addresses, code and data descriptors contain other segment attributes including segment size (1 to 64K bytes), access rights (read only, read/write, execute only, and execute/read), and presence in memory (for virtual memory systems) (See Figure 10). Any segment usage violating a segment attribute indicated by the segment descriptor will prevent the memory cycle and cause an exception or interrupt.

CODE OR DATA SEGMENT DESCRIPTOR



*Must be set to 0 for compatability with future upgrades.

ACCESS RIGHTS BYTE DEFINITION

	Bit Position	Name	Function		
	7	Present (P)	P = 1 P = 0	Segment is mapped into physical memory No mapping to physical memory exits, base and limit are not used.	
	6-5	Descriptor Privilege Level (DPL)		Segment privilege attribute used in privilege tests	
	4	Segment Descriptor (S)	S = 1 S = 0	Code or Data (includes stacks) segment descriptor System Segment Descriptor or Gate Descriptor	
Type Field Definition	3	Executable (E)	E = 0	Data segment descriptor type is:	If Data Segment (S = 1, E = 0)
	2	Expansion Direction (ED)	ED 0 ED = 1	Expand up segment, offsets must be ≤ limit. Expand down segment, offsets must be > limit	
	1	Writeable (W)	W = 0 W = 1	Data segment may not be written into. Data segment may be written into.	
	3	Executable (E)	E = 1	Code Segment Descriptor type is:	If Code Segment (S = 1, E = 1)
	2	Conforming (C)	C = 1	Code segment may only be executed when CPL ≥ DPL and CPL remains unchanged.	
	1	Readable (R)	R = 0 R = 1	Code segment may not be read Code segment may be read.	
	0	Accessed (A)	A = 0 A = 1	Segment has not been accessed. Segment selector has been loaded into segment register or used by selector test instructions.	

FIGURE 10.CODE AND DATA SEGMENT DESCRIPTOR FORMATS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Code and data (including stack data) are stored in two types of segments: code segments and data segments. Both types are identified and defined by segment descriptors (S = 1). Code segments are identified by the executable (E) bit set to 1 in the descriptor access rights byte. The access rights byte of both code and data segment descriptor types have three fields in common: present (P) bit, Descriptor Privilege Level (DPL), and accessed (A) bit. If P = 0, any attempted use of this segment will cause a not-present exception. DPL specifies the privilege level of the segment descriptor. DPL controls when the descriptor may be used by a task (refer to privilege discussion below). The A bit shows whether the segment has been previously accessed for usage profiling, a necessity for virtual memory systems. The CPU will always set this bit when accessing the descriptor.

Data segments (S = 1; E = 0) may be either read-only or read-write as controlled by the W bit of the access rights byte. Read-only (W = 0) data segments may not be written into. Data segments may grow in two directions, as determined by the Expansion Direction (ED) bit: upwards (ED = 0) for data segments, and downwards (ED = 1) for a segment containing a stack. The limit field for a data segment descriptor is interpreted differently depending on the ED bit (see Figure 10).

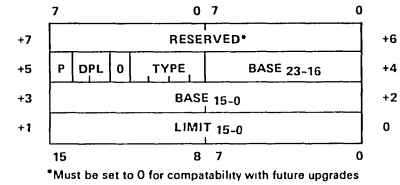
A code segment (S = 1, E = 1) may be execute-only or execute/read as determined by the Readable (R) bit. Code segments may never be written into and execute-only code segments (R = 0) may not be read. A code segment may also have an attribute called conforming (C). A conforming code segment may be shared by programs that execute at different privilege levels. The DPL of a conforming code segment defines the range of privilege levels at which the segment may be executed (refer to privilege discussion below). The limit field identifies the last byte of a code segment.

System Segment Descriptors (S = 0, Type = 1-3)

In addition to code and data segment descriptors, the protected mode 80C286 defines System Segment Descriptors. These descriptors define special system data segments which contain a table of descriptors (Local Descriptor Table Descriptor) or segments which contain the execution state of a task (Task State Segment Descriptor).

Figure 11 gives the formats for the special system data segment descriptors. The descriptors contain a 24-bit base address of the segment and a 16-bit limit. The access byte defines the type of descriptor, its state and privilege level. The descriptor contents are valid and the segment is in physical memory if P = 1. If P = 0, the segment is not valid. The DPL field is only used in Task State Segment descriptors and indicates the privilege level at which the descriptor may be used (see Privilege). Since the Local Descriptor Table descriptor may only be used by a special privileged instruction, the DPL field is not used. Bit 4 of the access byte is 0 to indicate that it is a system control descriptor. The type field specifies the descriptor type as indicated in Figure 11.

SYSTEM SEGMENT DESCRIPTOR



*Must be set to 0 for compatability with future upgrades

SYSTEM SEGMENT DESCRIPTOR FIELDS

Name	Value	Description
TYPE	1 2 3	Available Task State Segment (TSS) Local Descriptor Table Busy Task State Segment (TSS)
P	0 1	Descriptor contents are not valid Descriptor contents are valid
DPL	0-3	Descriptor Privilege Level
BASE	24-bit number	Base Address of special system data segment in real memory
LIMIT	16-bit number	Offset of last byte in segment

FIGURE 11. SYSTEM SEGMENT DESCRIPTOR FORMAT

Gate Descriptors (S = 0, Type = 4-7)

Gates are used to control access to entry points within the target code segment. The gate descriptors are call gates, task gates, interrupt gates and trap gates. Gates provide a level of indirection between the source and destination of the control transfer. This indirection allows the CPU to automatically perform protection checks and control entry point of the destination. Call gates are used to change privilege levels (see Privilege), task gates are used to perform a task switch, and interrupt and trap gates are used to specify interrupt service routines. The interrupt gate disables interrupts (resets IF) while the trap gate does not.

Figure 12 shows the format of the gate descriptors. The descriptor contains a destination pointer that points to the descriptor of the target segment and the entry point offset. The destination selector in an interrupt gate, trap gate, and call gate must refer to a code segment descriptor. These gate descriptors contain the entry point to prevent a program from constructing and using an illegal entry point. Task gates may only refer to a task state segment. Since task gates invoke a task switch, the destination offset is not used in the task gate.

Exception 13 is generated when the gate is used if a destination selector does not refer to the correct descriptor type. The word count field is used in the call gate descriptor to indicate the number of parameters (0-31 words) to be automatically copied from the caller's stack to the stack of the called routine when a control transfer changes privilege levels. The word count field is not used by any other gate descriptor.

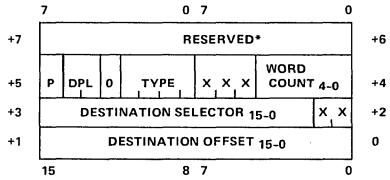
The access byte format is the same for all descriptors. P = 1 indicates that the gate contents are valid. P = 0 indicates the contents are not valid and causes exception 11 if referenced. DPL is the descriptor privilege level and specifies when this descriptor may be used by a task

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

(refer to privilege discussion below). Bit 4 must equal 0 to indicate a system control descriptor. The type field specifies the descriptor type as indicated in Figure 12.

GATE DESCRIPTOR



*Must be set to 0 for compatibility with future upgrades

GATE DESCRIPTOR FIELDS

Name	Value	Description
TYPE	4 5 6 7	–Call Gate –Task Gate –Interrupt Gate –Trap Gate
P	0 1	–Descriptor Contents are not valid –Descriptor Contents are valid
DPL	0–3	Descriptor Privilege Level
WORD COUNT	0–31	Number of words to copy from callers stack to called procedures stack. Only used with call gate.
DESTINATION SELECTOR	16-bit selector	Selector to the target code segment (Call, Interrupt or Trap Gate) Selector to the target task state segment (Task Gate)
DESTINATION OFFSET	16-bit offset	Entry point within the target code segment

FIGURE 12. GATE DESCRIPTOR FORMAT

Segment Descriptor Cache Registers

A segment descriptor cache register is assigned to each of the four segment registers (CS, SS, DS, ES). Segment descriptors are automatically loaded (cached) into a segment descriptor cache register (Figure 13) whenever the associated segment register is loaded with a selector.

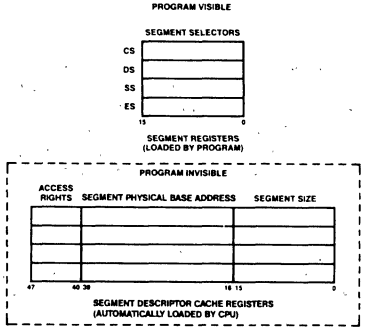
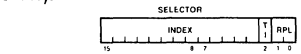


FIGURE 13. DESCRIPTOR CACHE REGISTERS

Only segment descriptors may be loaded into segment descriptor cache registers. Once loaded, all references to that segment of memory use the cached descriptor information instead of reaccessing the descriptor. The descriptor cache registers are not visible to programs. No instructions exist to store their contents. They only change when a segment register is loaded.

Selector Fields

A protected mode selector has three fields: descriptor entry index, local or global descriptor table indicator (TI), and selector privilege (RPL) as shown in Figure 14. These fields select one of two memory based tables of descriptors, select the appropriate table entry and allow high-speed testing of the selector's privilege attribute (refer to privilege discussion below).



BITS	NAME	FUNCTION
1–0	REQUESTED PRIVILEGE LEVEL (RPL)	INDICATES SELECTOR PRIVILEGE LEVEL DESIRED
2	TABLE INDICATOR (TI)	TI = 0 USE GLOBAL DESCRIPTOR TABLE (GDT) TI = 1 USE LOCAL DESCRIPTOR TABLE (LDT)
15–3	INDEX	SELECT DESCRIPTOR ENTRY IN TABLE

FIGURE 14. SELECTOR FIELDS

Local and Global Descriptor Tables

Two tables of descriptors, called descriptor tables, contain all descriptors accessible by a task at any given time. A descriptor table is a linear array of up to 8192 descriptors. The upper 13 bits of the selector value are an index into a descriptor table. Each table has a 24-bit base register to locate the descriptor table in physical memory and a 16-bit limit register that confine descriptor access to the defined limits of the table as shown in Figure 15. A restartable exception (13) will occur if an attempt is made to reference a descriptor outside the table limits.

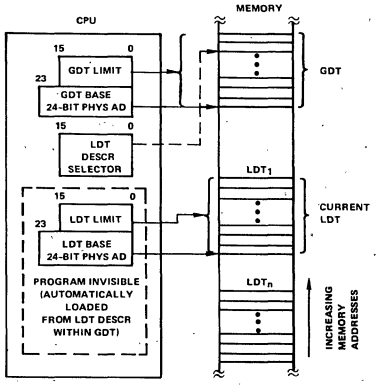


FIGURE 15. LOCAL AND GLOBAL DESCRIPTOR TABLE DEFINITION

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

One table, called the Global Descriptor table (GDT), contains descriptors available to all tasks. The other table, called the Local Descriptor Table (LDT), contains descriptors that can be private to a task. Each task may have its own private LDT. The GDT may contain all descriptor types except interrupt and trap descriptors. The LDT may contain only segment, task gate, and call gate descriptors. A segment cannot be accessed by a task if its segment descriptor does not exist in either descriptor table at the time of access.

The LGDT and LLDT instructions load the base and limit of the global and local descriptor tables. LGDT and LLDT are privileged, i.e. they may only be executed by trusted programs operating at level 0. The LGDT instruction loads a six byte field containing the 16-bit table limit and 24-bit physical base address of the Global Descriptor Table as shown in Figure 16. The LDT instruction loads a selector which refers to a Local Descriptor Table descriptor containing the base address and limit for an LDT, as shown in Figure 11.

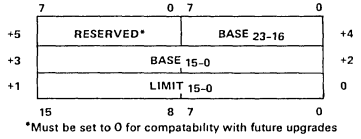


FIGURE 16. GLOBAL DESCRIPTOR TABLE AND INTERRUPT DESCRIPTOR TABLE DATA TYPE

Interrupt Descriptor Table

The protected mode 80C286 has a third descriptor table, called the Interrupt Descriptor Table (IDT) (see Figure 17), used to define up to 256 interrupts. It may contain only task gates, interrupt gates and trap gates. The IDT (Interrupt Descriptor Table) has a 24-bit physical base and 16-bit limit register in the CPU. The priviledged LIDT instruction loads these registers with a six byte value of identical form to that of the LGDT instruction (see Figure 16 and Protected Mode Initialization).

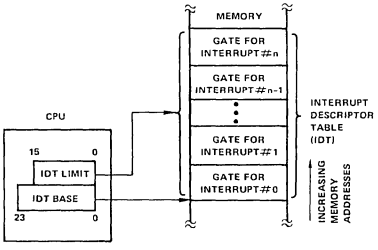


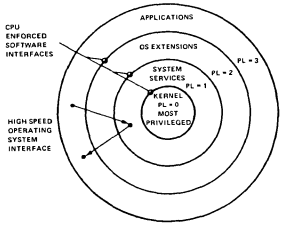
FIGURE 17. INTERRUPT DESCRIPTOR TABLE DEFINITION

References to IDT entries are made via INT instructions, external interrupt vectors, or exceptions. The IDT must be at least 256 bytes in size to allocate space for all reserved interrupts.

Privilege

The 80C286 has a four-level hierarchical privilege system which controls the use of privileged instructions and access to descriptors (and their associated segments) within a task. Four-level privilege, as shown in Figure 18, is an extension of the users supervisor mode commonly found in minicomputers. The privilege levels are numbered 0 through 3. Level 0 is the most privileged level. Privilege levels provide protection within a task. (Tasks are isolated by providing private LDT's for each task.) Operating system routines, interrupt handlers, and other system software can be included and protected within the virtual address space of each task using the four levels of privilege. Each task in the system has a separate stack for each of its privilege levels.

Tasks, descriptors, and selectors have a privilege level attribute that determines whether the descriptor may be used. Task privilege affects the use of instructions and descriptors. Descriptor and selector privilege only affect access to the descriptor.



NOTE: PL becomes numerically lower as privilege level increases

FIGURE 18. HIERARCHICAL PRIVILEGE LEVELS

Task Privilege

A task always executes at one of the four privilege levels. The task privilege level at any specific instant is called the Current Privilege Level (CPL) and is defined by the lower two bits of the CS register. CPL cannot change during execution in a single code segment. A task's CPL may only be changed by control transfers through gate descriptors to a new code segment (See Control Transfer). Tasks begin executing at the CPL value specified by the code segment selector within TSS when the task is initiated via a task switch operation (See Figure 19). A task executing at Level 0 can access all data segments defined in the GDT and the task's LDT and is considered the most trusted level. A task executing a Level 3 has the most restricted access to data and is considered the least trusted level.

Descriptor Privilege

Descriptor privilege is specified by the Descriptor Privilege Level (DPL) field of the descriptor access byte. DPL specifies the least trusted task privilege level (CPL) at which a task may access the descriptor. Descriptors with DPL = 0 are the most protected. Only tasks executing at privilege level 0 (CPL = 0) may access them. Descriptors with DPL = 3 are the least protected (i.e. have the least restricted access) since tasks can access them when CPL = 0, 1, 2, or 3). This rule applies to all descriptors, except LDT descriptors.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

TABLE I. DESCRIPTOR TYPES USED FOR CONTROL TRANSFER

CONTROL TRANSFER TYPES	OPERATION TYPES	DESCRIPTOR REFERENCED	DESCRIPTOR TABLE
Intersegment within the same privilege levels	JMP, CALL, RET, IRET*	Code Segment	GDT/LDT
Intersegment to the same or higher privilege level Interrupt within task may change CPL.	CALL	Call Gate	GDT/LDT
	Interrupt Instruction, Exception External Interrupt	Trap or Interrupt Gate	IDT
Intersegment to a lower privilege level (changes task CPL)	RET, IRET*	Code Segment	GDT/LDT
Task Switch	CALL, JMP	Task State Segment	GDT
	CALL, JMP	Task Gate	GDT/LDT
	IRET** Interrupt Instruction, Exception External Interrupt	Task Gate	IDT

*NT (Nested Task bit of flag word) = 0 **NT (Nested Task bit of flag word) = 1

Selector Privilege

Selector privilege is specified by the Requested Privilege Level (RPL) field in the least significant two bits of a selector. Selector RPL may establish a less trusted privilege level than the current privilege level for the use of a selector. This level is called the task's effective privilege level (EPL). RPL can only reduce the scope of a task's access to data with this selector. A task's effective privilege is the numeric maximum of RPL and CPL. A selector with RPL=0 imposes no additional restriction on its use while a selector with RPL = 3 can only refer to segments at privilege Level 3 regardless of the task's CPL. RPL is generally used to verify that pointer parameters passed to a more trusted procedure are not allowed to use data at a more privileged level than the caller (refer to pointer testing instructions).

Descriptor Access and Privilege Validation

Determining the ability of a task to access a segment involves the type of segment to be accessed, the instruction used, the type of descriptor used and CPL, RPL, and DPL. The two basic types of segment accesses are control transfer (selectors loaded into CS) and data (selectors loaded into DS, ES or SS).

Data Segment Access

Instructions that load selectors into DS and ES must refer to a data segment descriptor or readable code segment descriptor. The CPL of the task and the RPL of the selector must be the same as or more privileged (numerically equal to or lower than) than the descriptor DPL. In general, a task can only access data segments at the same or less privileged levels than the CPL or RPL (whichever is numerically higher) to prevent a program from accessing data it cannot be trusted to use.

An exception to the rule is a readable conforming code segment. This type of code segment can be read from any privilege level.

If the privilege checks fail (e.g. DPL is numerically less than the maximum of CPL and RPL) or an incorrect type of descriptor is referenced (e.g. gate descriptor or execute only code segment) exception 13 occurs. If the segment is not present, exception 11 is generated.

Instructions that load selectors into SS must refer to data segment descriptors for writable data segments. The descriptor privilege (DPL) and RPL must equal CPL. All other descriptor types or a privilege level violation will cause exception 13. A not present fault causes exception 12.

Control Transfer

Four types of control transfer can occur when a selector is loaded into CS by a control transfer operation (see Table I). Each transfer type can only occur if the operation which loaded the selector references the correct descriptor type. Any violation of these descriptor usage rules (e.g. JMP through a call gate or RET to a Task State Segment) will cause exception 13.

The ability to reference a descriptor for control transfer is also subject to rules of privilege. A CALL or JUMP instruction may only reference a code segment descriptor with DPL equal to the task CPL or a conforming segment with DPL of equal or greater privilege than CPL. The RPL of the selector used to reference the code descriptor must have as much privilege as CPL.

RET and IRET instructions may only reference code segment descriptors with descriptor privilege equal to or less privileged than the task CPL. The selector loaded into CS is the return address from the stack. After the return, the selector RPL is the task's new CPL. If CPL changes, the old stack pointer is popped after the return address.

When a JMP or CALL references a Task State Segment descriptor, the descriptor DPL must be the same or less privileged than the task's CPL. Reference to a valid Task

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

State Segment descriptor causes a task switch (see Task Switch Operation). Reference to a Task State Segment descriptor at a more privileged level than the task's CPL generates exception 13.

When an instruction or interrupt references a gate descriptor, the gate DPL must have the same or less privilege than the task CPL. If DPL is at a more privileged level than CPL, exception 13 occurs. If the destination selector contained in the gate references a code segment descriptor, the code segment descriptor DPL must be the same or more privileged than the task CPL. If not, Exception 13 is issued. After the control transfer, the code segment descriptors DPL is the task's new CPL. If the destination selector in the gate references a task state segment, a task switch is automatically performed (see Task Switch Operation).

The privilege rules on control transfer require:

- JMP or CALL direct to a code segment (code segment descriptor) can only be a conforming segment with DPL of equal or greater privilege than CPL or a non-conforming segment at the same privilege level.
- interrupts within the task, or calls that may change privilege levels, can only transfer control through a gate at the same or a less privileged level than CPL to a code segment at the same or more privileged level than CPL.
- return instructions that don't switch tasks can only return control to a code segment at the same or less privileged level.
- task switch can be performed by a call, jump or interrupt which references either a task gate or task state segment at the same or less privileged level.

Privilege Level Changes

Any control transfer that changes CPL within the task, causes a change of stacks as part of the operation. Initial values of SS:SP for privilege levels 0, 1, and 2 are kept in the task state segment (refer to Task Switch Operation). During a JMP or CALL control transfer, the new stack pointer is loaded into the SS and SP registers and the previous stack pointer is pushed onto the new stack.

When returning to the original privilege level, its stack is restored as part of the RET or IRET instruction operation.

TABLE J. SEGMENT REGISTER LOAD CHECKS

ERROR DESCRIPTION	EXCEPTION NUMBER
Descriptor table limit exceeded	13
Segment descriptor not-present	11 or 12
Privilege rules violated	13
Invalid descriptor/segment type segment register load: — Read only data segment load to SS — Special control descriptor load to DS,ES,SS — Execute only segment load to DS, ES, SS — Data segment load to CS — Read/Execute code segment load SS	13

For subroutine calls that pass parameters on the stack and cross privilege levels, a fixed number of words, as specified in the gate, are copied from the previous stack to the current stack. The inter-segment RET instruction with a stack adjustment value will correctly restore the previous stack pointer upon return.

Protection

The 80C286 includes mechanisms to protect critical instructions that effect the CPU execution state (e.g. HLT) and code or data segments from improper usage. These protection mechanisms are grouped into three forms:

- Restricted usage of segments (e.g. no write allowed to read-only data segments). The only segments available for use are defined by descriptors in the Local Descriptor Table (LDT) and Global Descriptor Table (GDT).
- Restricted access to segments via the rules of privilege and descriptor usage.
- Privileged instructions or operations that may only be executed at certain privilege levels as determined by the CPL and I/O Privilege Level (IOPL). The IOPL is defined by bits 14 and 13 of the flag word.

These checks are performed for all instructions and can be split into three categories: segment load checks (Table J), operand reference checks (Table K), and privileged instruction checks (Table L). Any violation of the rules shown will result in an exception. A not-present exception related to the stack segment causes exception 12.

The IRET and POPF instructions do not perform some of their defined functions if CPL is not of sufficient privilege (numerically small enough). Precisely these are:

- The IF bit is not changed if CPL is greater than IOPL.
- The IOPL field of the flag word is not changed if CPL is greater than 0.

No exceptions or other indication are given when these conditions occur.

TABLE K. OPERAND REFERENCE CHECKS

ERROR DESCRIPTION	EXCEPTION NUMBER
Write into code segment	13
Read from execute-only code segment	13
Write to read-only data segment	13
Segment limit exceeded (Note1)	12 or 13

NOTE 1. Carry out in offset calculations is ignored.

TABLE L. PRIVILEGED INSTRUCTION CHECKS

ERROR DESCRIPTION	EXCEPTION NUMBER
CPL ≠ 0 when executing the following instructions: LIDT, LLDT, LGDT, LTR, LMSW, CTS, HLT	13
CPT > IOPL when executing the following instructions: INS, IN, OUTS, OUT, STI, CLI, LOCK	13

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

TABLE M. PROTECTED MODE EXCEPTIONS

INTERRUPT VECTOR	FUNCTION	RETURN ADDRESS AT FALLING INSTRUCTION?	ALWAYS RESTARTABLE?	ERROR CODE ON STACK?
8	Double exception detected	Yes	No (Note 2)	Yes
9	Processor extension segment overrun	No	No (Note 2)	No
10	Invalid task state segment	Yes	Yes	Yes
11	Segment not present	Yes	Yes	Yes
12	Stack segment overrun or stack segment not present	Yes	Yes (Note 1)	Yes
13	General protection	Yes	No (Note 2)	Yes

NOTES: 1. When a PUSHA or POPA instruction attempts to wrap around the stack segment, the machine state after the exception will not be restartable because stack segment wrap around is not permitted. This condition is identified by the value of the saved SP being either 0000(H), 0001(H), FFFE(H), or FFFF(H).
2. These exceptions indicate a violation to privilege rules or usage rules has occurred. Restart is generally not attempted under those conditions.

Exceptions

The 80C286 detects several types of exceptions and interrupts in protected mode (see Table M). Most are restartable after the exceptional condition is removed. Interrupt handlers for most exceptions can read an error code, pushed on the stack after the return address, that identifies the selector involved (0 if none). The return address normally points to the failing instruction, including all leading prefixes. For a processor extension segment overrun exception, the return address will not point at the ESC instruction that caused the exception; however, the processor extension registers may contain the address of the failing instruction.

These exceptions indicate a violation to privilege rules or usage rules has occurred. Restart is generally not attempted under those conditions.

All these checks are performed for all instructions and can be split into three categories: segment load checks (Table J), operand reference checks (Table K), and privileged instruction checks (Table L). Any violation of the rules shown will result in an exception. A not-present exception causes exception 11 or 12 and is restartable.

Special Operations
Task Switch Operation

The 80C286 provides a built-in task switch operation which saves the entire 80C286 execution state (registers, address space, and a link to the previous task), loads a new execution state, and commences execution in the new task. Like gates, the task switch operation is invoked by executing an inter-segment JMP or CALL instruction which refers to a Task State Segment (TSS) or task gate descriptor in the GDT or LDT. An INT instruction, exception, or external interrupt may also invoke the task switch operation by selecting a task gate descriptor in the associated IDT descriptor entry.

The TSS descriptor points at a segment (see Figure 19) containing the entire 80C286 execution state while a task gate descriptor contains a TSS selector. The limit field of the descriptor must be greater than 002B(H).

Each task must have a TSS associated with it. The current TSS is identified by a special register in the 80C286 called the Task Register (TR). This register contains a selector referring to the task state segment descriptor that defines the current TSS. A hidden base and limit register associated with TR are loaded whenever TR is loaded with a new selector. The IRET instruction is used to return control to the task that called the current task or was interrupted. Bit 14 in the flag register is called the Nested Task (NT) bit. It controls the function of the IRET instruction. If NT = 0, the IRET instruction performs the regular current task by popping values off the stack; when NT = 1, IRET performs a task switch operation back to the previous task.

When a CALL, JMP, or INT instruction initiates a task switch, the old (except for case of JMP) and new TSS will be marked busy and the back link field of the new TSS set to the old TSS selector. The NT bit of the new task is set by CALL or INT initiated task switches. An interrupt that does not cause a task switch will clear NT. NT may also be set or cleared by POPF or IRET instructions.

The task state segment is marked busy by changing the descriptor type field from Type 1 to Type 3. Use of a selector that references a busy task state segment causes Exception 13.

Processor Extension Context Switching

The context of a processor extension is not changed by the task switch operation. A processor extension context need only be changed when a different task attempts to use the processor extension (which still contains the context of a previous task). The 80C286 detects the first use of a processor extension after a task switch by causing the processor extension not present exception (7). The interrupt handler may then decide whether a context change is necessary.

Whenever the 80C286 switches tasks, it sets the Task Switched (TS) bit of the MSW. TS indicates that a processor extension context may belong to a different task than the current one. The processor extension not present exception (7) will occur when attempting to execute an ESC or WAIT instruction if TS = 1 and a processor extension is present (MP = 1 in MSW).

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

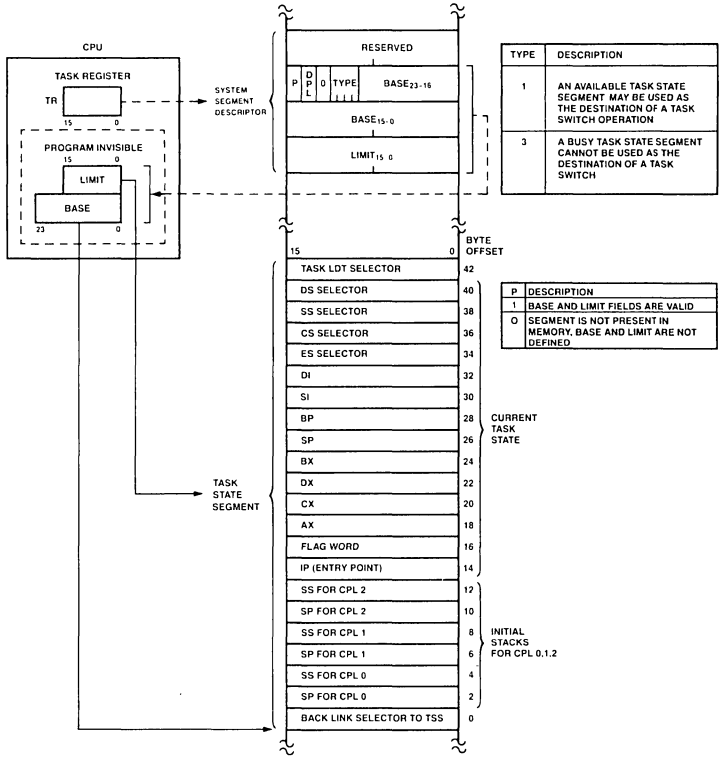


FIGURE 19. TASK STATE SEGMENT AND TSS REGISTERS

Pointer Testing Instructions

The 80C286 provides several instructions to speed pointer testing and consistency checks for maintaining system integrity (see Table N). These instructions use the memory management hardware to verify that a selector value refers to an appropriate segment without risking an exception. A condition flag (ZF) indicates whether use of the selector or segment will cause an exception.

TABLE N. 80C286 POINTER TEST INSTRUCTIONS

INSTRUCTION	OPERANDS	FUNCTION
ARPL	Selector, Register	Adjust Requested Privilege Level: adjusts the RPL of the selector to the numeric maximum of current selector RPL value and the RPL value in the register. Set zero flag if selector RPL was changed by ARPL.
VERR	Selector	VERify for Read: sets the zero flag if the segment referred to by the selector can be read.
VERW	Selector	VERify for Write: sets the zero flag if the segment referred to by the selector can be written.
LSL	Register, Selector	Load Segment Limit: reads the segment limit into the register if privilege rules and descriptor type allow. Set zero flag if successful.
LAR	Register, Selector	Load Access Rights: reads the descriptor access rights byte into the register if privilege rules allow. Set zero flag if successful.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Double Fault and Shutdown

If two separate exceptions are detected during a single instruction execution, the 80C286 performs the double fault exception (8). If an exception occurs during processing of the double fault exception, the 80C286 will enter shutdown. During shutdown no further instructions or exceptions are processed. Either NMI (CPU remains in protected mode) or RESET (CPU exits protected mode) can force the 80C286 out of shutdown. Shutdown is externally signalled via a HALT bus operation with A_1 LOW.

Protected Mode Initialization

The 80C286 initially executes in real address mode after RESET. To allow initialization code to be placed at the top of physical memory, A_{23-20} will be HIGH when the 80C286 performs memory references relative to the CS register until CS is changed. A_{23-20} will be zero for references to the DS, ES, or SS segments. Changing CS in real address mode will force A_{23-20} LOW whenever CS is used again. The initial CS:IP value of F000:FFF0 provides 64K bytes of code space for initialization code without changing CS.

Protected mode operation requires several registers to be initialized. The GDT and IDT base registers must refer to a valid GDT and IDT. After executing the LMSW instruction to set PE, the 80C286 must immediately execute an intra-segment JMP instruction to clear the instruction queue of instructions decoded in real address mode.

To force the 80C286 CPU registers to match the initial protected mode state assumed by software, execute a JMP instruction with a selector referring to the initial TSS used in the system. This will load the task register, local descriptor table register, segment registers and initial general register state. The TR should point at a valid TSS since any task switch operation involves saving the current task state.

System Interface

The 80C286 system interface appears in two forms: a local bus and a system bus. The local bus consists of address, data, status, and control signals at the pins of the CPU. A system bus is any buffered version of the local bus. A system bus may also differ from the local bus in terms of coding of status and control lines andsor timing and loading of signals.

Bus Interface Signals and Timing

The 80C286 microsystems local bus interfaces the 80C286 to local memory and I/O components. The interface has 24 address lines, 16 data lines, and 8 status and control signals.

The 80C286 CPU, 82C284 clock generator, 82C288 bus controller, 82289 bus arbiter, 82C86H/87H tranceivers, and 82C82/83H latches provide a buffered and decoded system bus interface. The 82C284 generates the system clock and synchronizes $\overline{\text{READY}}$ and RESET. The 82C288 converts bus operation status encoded by the 80C286 into command and bus control signals. The 82289 bus arbiter generates Multibus bus arbitration signals. These components can provide the critical timing required for most system bus interfaces including the Multibus.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices, and to eliminate the need for pull-up/down resistors, bus-hold" circuitry has been used on the 80C286 pins 4-6, 36-51 and 66-68 (See Figure 20A and 20B). The circuit shown in Figure 20A will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). The circuit shown in Figure 20B will maintain a high impedance logic one state if no driving source is present. To overdrive the bus-hold" circuits, an external driver must be capable of sinking or sourcing approximately 400 microamps at valid input voltage levels. Since this bus-hold" circuitry is active and not a resistive" type element, the associated power supply current is negligible, and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

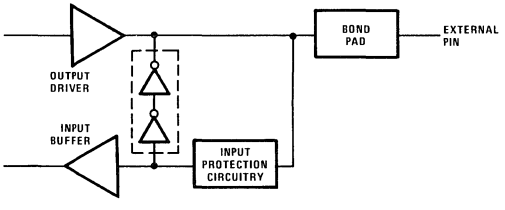


FIGURE 20A. BUS HOLD CIRCUITRY — PINS 36-51, 66, 67

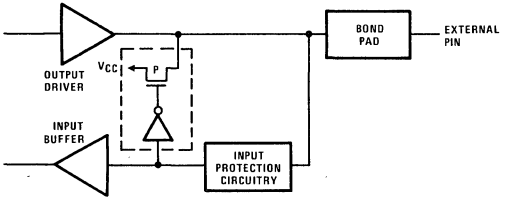


FIGURE 20B. BUS HOLD CIRCUITRY — PINS 4-6, 68

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Physical Memory and I/O Interface

A maximum of 16 megabytes of physical memory can be addressed in protected mode. One megabyte can be addressed in real address mode. Memory is accessible as bytes or words. Words consist of any two consecutive bytes addressed with the least significant byte stored in the lowest address. Byte transfers occur on either half of the 16-bit local data bus. Even bytes are accessed over D_{7-0} while odd bytes are transferred over D_{15-8}. Even addressed words are transferred over D_{15-0} in one bus cycle, while odd addressed word require two bus operations. The first transfers data on D_{15-8}, and the second transfers data on D_{7-0}. Both byte data transfers occur automatically, transparent to software.

Two bus signals, A_0 and $\overline{BHE}$, control transfers over the lower and upper halves of the data bus. Even address byte transfers are indicated by A_0 LOW and $\overline{BHE}$ HIGH. Odd address byte transfers are indicated by A_0 HIGH and $\overline{BHE}$ LOW. Both A_0 and $\overline{BHE}$ are LOW for even address word transfers.

The I/O address space contains 64K addresses in both modes. The I/O space is accessible as either bytes or words, as is memory. Byte wide peripheral devices may be attached to either the upper or lower byte of the data bus. Byte-wide I/O devices attached to the upper data byte (D_{15-8}) are accessed with odd I/O addresses. Devices on the lower data byte are accessed with even I/O addresses. An interrupt controller such as Harris's 82C59A must be connected to the lower data byte (D_{7-0}) for proper return of the interrupt vector.

Bus Operation

The 80C286 uses a double frequency system clock (CLK input) to control bus timing. All signals on the local bus are measured relative to the system CLK input. The CPU divides the system clock by 2 to produce the internal processor clock, which determines bus state. Each processor clock is composed of two system clock cycles named phase 1 and phase 2. The 82C284 clock generator output (PCLK) identifies the next phase of the processor clock. (See Figure 21.)

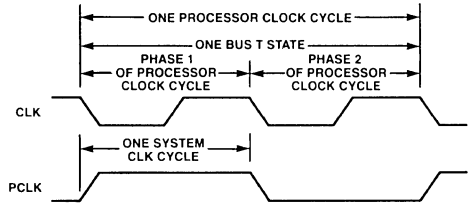


FIGURE 21. SYSTEM AND PROCESSOR CLOCK RELATIONSHIPS

Six types of bus operations are supported; memory read, memory write, I/O read, I/O write, interrupt acknowledge, and halt/shutdown. Data can be transferred at a maximum rate of one word per two processor clock cycles.

The 80C286 bus has three basic states: idle (T_I), send status (T_S), and perform command (T_C). The 80C286 CPU also has a fourth local bus state called hold (T_H). T_H indicates that the 80C286 has surrendered control of the local bus to another bus master in response to a HOLD request.

Each bus state is one processor clock long. Figure 22 shows the four 80C286 local bus states and allowed transitions.

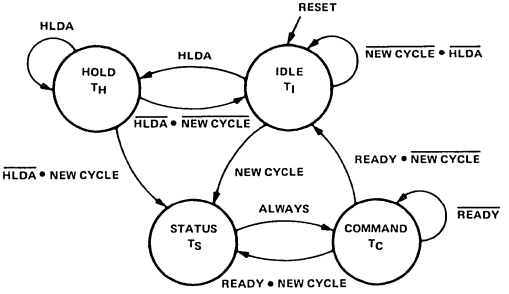


FIGURE 22.80C286 BUS STATES

Bus States

The idle (T_I) state indicates that no data transfers are in progress or requested. The first active state T_S is signaled by status line $\overline{S_1}$ or $\overline{S_0}$ going LOW and identifying phase 1 of the processor clock. During T_S, the command encoding, the address, and data (for a write operation) are available on the 80C286 output pins. The 82C288 bus controller decodes the status signals and generates Multibus compatible read/write command and local transceiver control signals.

After T_S, the perform command (T_C) state is entered. Memory or I/O devices respond to the bus operation during T_C, either transferring read data to the CPU or accepting write data. T_C states may be repeated as often as necessary to ensure sufficient time for the memory or I/O device to respond. The $\overline{READY}$ signal determines whether T_C is repeated. A repeated T_C state is called a wait state.

During hold (T_H), the 80C286 will float all address, data, and status output drivers enabling another bus master to use the local bus. The 80C286 HOLD input signal is used to place the 80C286 into the T_H state. The 80C286 HLDA output signal indicates that the CPU has entered T_H.

Pipelined Addressing

The 80C286 uses a local bus interface with pipelined timing to allow as much time as possible for data access. Pipelined timing allows a new bus operation to be initiated every two processor cycles, while allowing each individual bus operation to last for three processor cycles.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

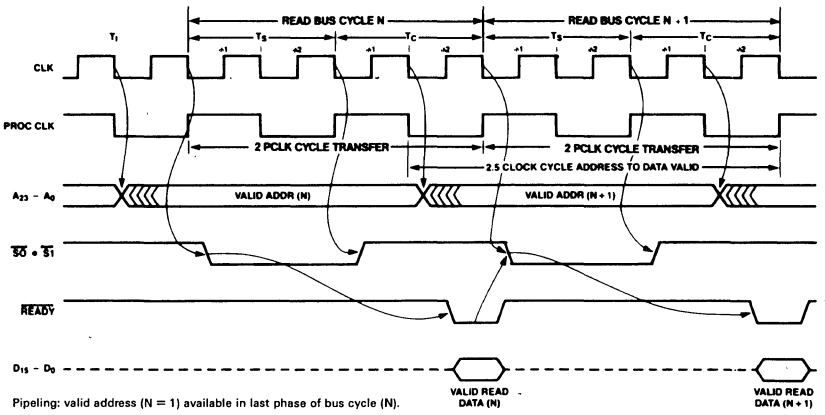


FIGURE 23. BASIC BUS CYCLE

The timing of the address outputs is pipelined such that the address of the next bus operation becomes available during the current bus operation. Or, in other words, the first clock of the next bus operation is overlapped with the last clock of the current bus operation. Therefore, address decode and routing logic can operate in advance of the next bus operation.

External address latches may hold the address stable for the entire bus operation, and provide additional AC and DC buffering.

The 80C286 does not maintain the address of the current bus operation during all T_C states. Instead, the address for the next bus operation may be emitted during phase 2 of any T_C. The address remains valid during phase 1 of the first T_C to guarantee hold time, relative to ALE, for the address latch inputs.

Bus Control Signals

The 82C288 bus controller provides control signals; address latch enable (ALE), Read/Write commands, data transmit/receive (DT/$\overline{R}$), and data enable (DEN) that control the address latches, data transceivers, write enable, and output enable for memory and I/O systems. The Address Latch Enable (ALE) output determines when the address may be latched. ALE provides at least one system CLK period of address hold time from the end of the previous bus operation until the address for the next bus operation appears at the latch outputs. This address hold time is required to support Multibus and common memory systems.

The data bus transceivers are controlled by 82C288 outputs Data Enable (DEN) and Data Transmit/Receive (DT/$\overline{R}$). DEN enables the data transceivers; while DT/$\overline{R}$ controls tranceiver direction. DEN and DT/R are timed to prevent bus contention between the bus master, data bus transceivers, and system data bus transceivers.

Command Timing Controls

Two system timing customization options, command extension and command delay, are provided on the 80C286 local bus.

Command extension allows additional time for external devices to respond to a command and is analogous to inserting wait states on the 80C86. External logic can control the duration of any bus operation such that the operation is only as long as necessary. The $\overline{READY}$ input signal can extend any bus operation for as long as necessary.

Command delay allows an increase of address or write data setup time to system bus command active for any bus operation by delaying when the system bus command becomes active. Command delay is controlled by the 82C288 CMDLY input. After T_S, the bus controller samples CMDLY at each failing edge of CLK. If CMDLY is HIGH, the 82C288 will not activate the command signal. When CMDLY is LOW, the 82C288 will activate the command signal. After the command becomes active, the CMDLY input is not sampled.

When a command is delayed, the available response time from command active to return read data or accept write data is less. To customize system bus timing, an address decoder can determine which bus operations require delaying the command. The CMDLY input does not affect the timing of ALE, DEN or DT/$\overline{R}$.

Figure 24 illustrates four uses of CMDLY. Example 1 shows delaying the read command two system CLKs for cycle N-1 and no delay for cycle N, and example 2 shows delaying the read command one system CLK for cycle N-1 and one system CLK delay for cycle N.

Bus Cycle Termination

At maximum transfer rates, the 80C286 bus alternates between the status and command states. The bus status

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

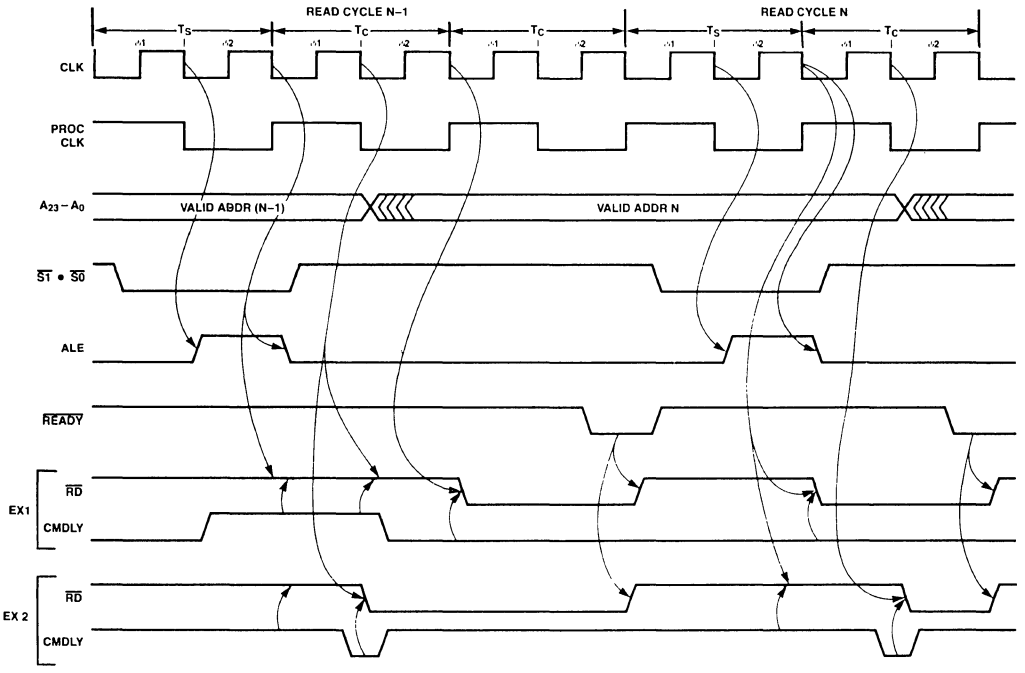


FIGURE 24. CMDLY CONTROLS THE LEADING EDGE OF COMMAND SIGNAL

signals become inactive after T_S so that they may correctly signal the start of the next bus operation after the completion of the current cycle. No external indication of T_C exists on the 80C286 local bus. The bus master and bus controller enter T_C directly after T_S and continue executing T_C cycles until terminated by the assertion of $\overline{READY}$.

READY Operation

The current bus master and 82C288 bus controller terminate each bus operation simultaneously to achieve maximum bus operation bandwidth. Both are informed in advance by $\overline{READY}$ active (open-collector output from 82C284) which identifies the last T_C cycle of the current bus operation. The bus master and bus controller must see the same sense of the $\overline{READY}$ signal, thereby requiring $\overline{READY}$ to be synchronous to the system clock.

Synchronous Ready

The 82C284 clock generator provides $\overline{READY}$ synchronization from both synchronous and asynchronous sources (see Figure 25). The synchronous ready input ($\overline{SRDY}$) of the clock generator is sampled with the falling edge of CLK at the end of phase 1 of each T_C. The state of $\overline{SRDY}$ is then broadcast to the bus master and bus controller via the $\overline{READY}$ output line.

Asynchronous Ready

Many systems have devices or subsystems that are asynchronous to the system clock. As a result, their ready outputs cannot be guaranteed to meet the 82C284 $\overline{SRDY}$ setup and hold time requirements. But the 82C284 asynchronous ready input ($\overline{ARDY}$) is designed to accept such signals. The $\overline{ARDY}$ input is sampled at the beginning of each T_C cycle by 82C284 synchronization logic. This provides one system CLK cycle time to resolve its value before broadcasting it to the bus master and bus controller.

$\overline{ARDY}$ or $\overline{ARDYEN}$ must be HIGH at the end of T_S. $\overline{ARDY}$ cannot be used to terminate the bus cycle with no wait states.

Each ready input of the 82C284 has an enable pin ($\overline{SRDYEN}$ and $\overline{ARDYEN}$) to select whether the current bus operation will be terminated by the synchronous or asynchronous ready. Either of the ready inputs may terminate a bus operation. These enable inputs are active low and have the same timing as their respective ready inputs. Address decode logic usually selects whether the current bus operation should be terminated by $\overline{ARDY}$ or $\overline{SRDY}$.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Data Bus Control

Figures 26, 27, and 28 show how the DT/$\overline{R}$, DEN, data bus, and address signals operate for different combinations of read, write, and idle bus operations. DT/$\overline{R}$ goes active (LOW) for a read operation. DT/$\overline{R}$ remains HIGH before, during, and between write operations.

The data bus is driven with write data during the second phase of T_S. The delay in write data timing allows the read data drivers, from a previous read cycle, sufficient time to enter three-state OFF before the 80C286 CPU begins driving the local data bus for write operations. Write data will always remain valid for one system clock past the last T_C to provide sufficient hold time for Multibus or other similar memory or I/O systems. During write-read or write-idle sequences the data bus enters a high impedance state during the second phase of the processor cycle after the last T_C. In a write-write sequence the data bus does not enter a high impedance state between T_C and T_S.

Bus Usage

The 80C286 local bus may be used for several functions: instruction data transfers, data transfers by other bus masters, instruction fetching, processor extension data transfers, interrupt acknowledge, and halt/shutdown. This section describes local bus activities which have special signals or requirements. Note that I/O transfers take place in exactly the same manner as memory transfers (i.e. to the 80C286 the timing, etc. of an I/O transfer is identical to a memory transfer).

HOLD and HLDA

HOLD and HLDA allow another bus master to gain control of the local bus by placing the 80C286 bus into the T_H state. The sequence of events required to pass control between the 80C286 and another local bus master are shown in Figure 29.

In this example, the 80C286 is initially in the T_H state as signaled by HLDA being active. Upon leaving T_H, as signaled by HLDA going inactive, a write operation is started. During the write operation another local bus master requests the local bus from the 80C286 as shown by the HOLD signal. After completing the write operation, the 80C286 performs one T_I bus cycle, to guarantee write data hold time, then enters T_H as signaled by HLDA going active.

The CMDLY signal and $\overline{ARDY}$ ready are used to start and stop the write bus command, respectively. Note that $\overline{SRDY}$ must be inactive or disabled by $\overline{SRDYEN}$ to guarantee $\overline{ARDY}$ will terminate the cycle.

HOLD must not be active during the time from the leading edge of RESET until 34 CLKs following the trailing edge of RESET unless the 80C286 is in the Halt condition. To ensure that the 80C286 remains in the Halt condition until the processor Reset operation is complete, no interrupts should occur after the execution of HLT until 34 CLKs after the trailing edge of the RESET pulse.

LOCK

The CPU asserts an active lock signal during Interrupt-Acknowledge cycles, the XCHG instruction, and during some descriptor accesses. Lock is also asserted when the LOCK prefix is used. The LOCK prefix may be used with the following ASM-286 assembly instructions; MOVS, INS and OUTS. For bus cycles other than Interrupt-Acknowledge cycles, Lock will be active for the first and subsequent cycles of a series of cycles to be locked. Lock will not be shown active during the last cycle to be locked. For the next-to-last cycle, Lock will become inactive at the end of the first T_C regardless of the number of wait states inserted. For Interrupt-Acknowledge cycles, Lock will be active for each cycle, and will become inactive at the end of the first T_C for each cycle regardless of the number of wait-states inserted.

Instruction Fetching

The 80C286 Bus Unit (BU) will fetch instructions ahead of the current instruction being executed. This activity is called prefetching. It occurs when the local bus would otherwise be idle and obeys the following rules:

A prefetch bus operation starts when at least two bytes of the 6-byte prefetch queue are empty.

The prefetcher normally performs word prefetches independent of the byte alignment of the code segment base in physical memory.

The prefetcher will perform only a byte code fetch operation for control transfers to an instruction beginning on a numerically odd physical address.

Prefetching stops whenever a control transfer or HLT instruction is decoded by the IU and placed into the instruction queue.

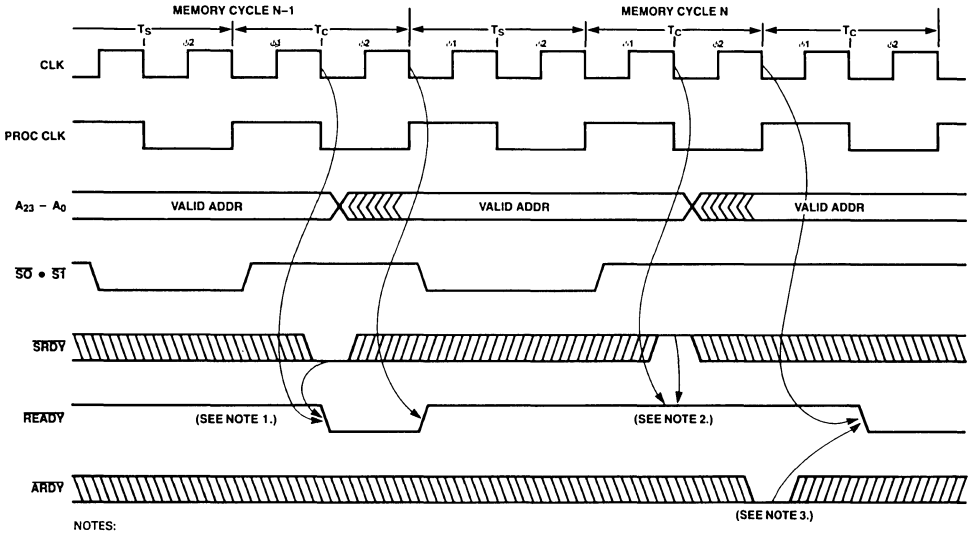
In real address mode, the prefetcher may fetch up to 6 bytes beyond the last control transfer or HLT instruction in a code segment.

In protected mode, the prefetcher will never cause a segment overrun exception. The prefetcher stops at the last physical memory word of the code segment. Exception 13 will occur if the program attempts to execute beyond the last full instruction in the code segment.

If the last byte of a code segment appears on an even physical memory address, the prefetcher will read the next physical byte of memory (perform a word code fetch). The value of this byte is ignored and any attempt to execute it causes exception 13.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.



NOTES:
1. SRDYEN is active low
2. If SRDYEN is high, the state of SRDY will not effect READY
3. ARDYEN is active low

FIGURE 25. SYNCHRONOUS AND ASYNCHRONOUS READY

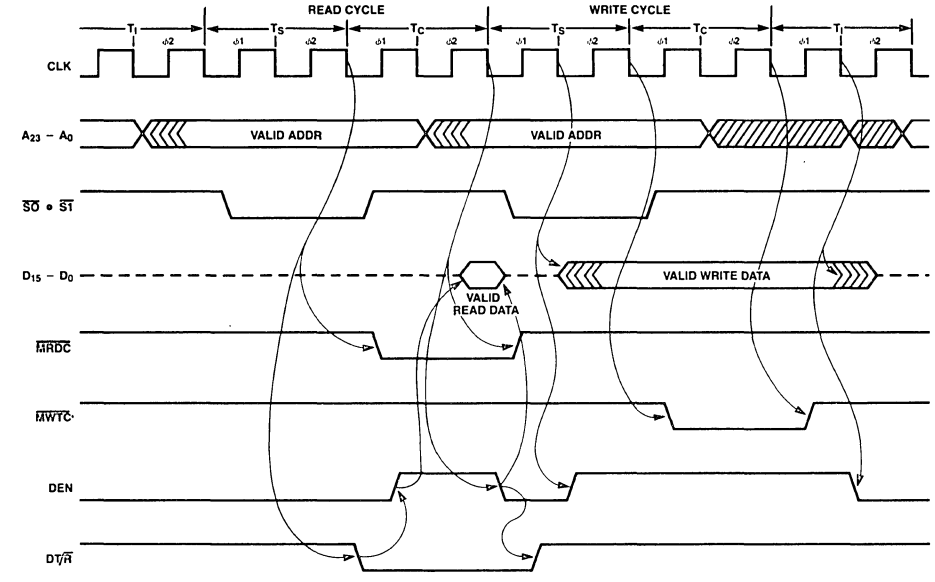


FIGURE 26. BACK TO BACK READ-WRITE CYCLE

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

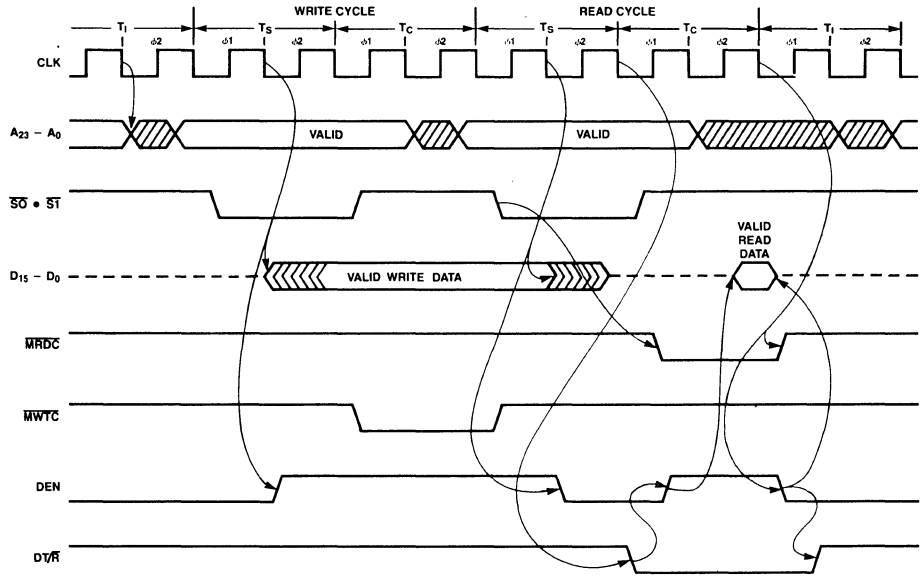


FIGURE 27. BACK TO BACK WRITE-READ CYCLE

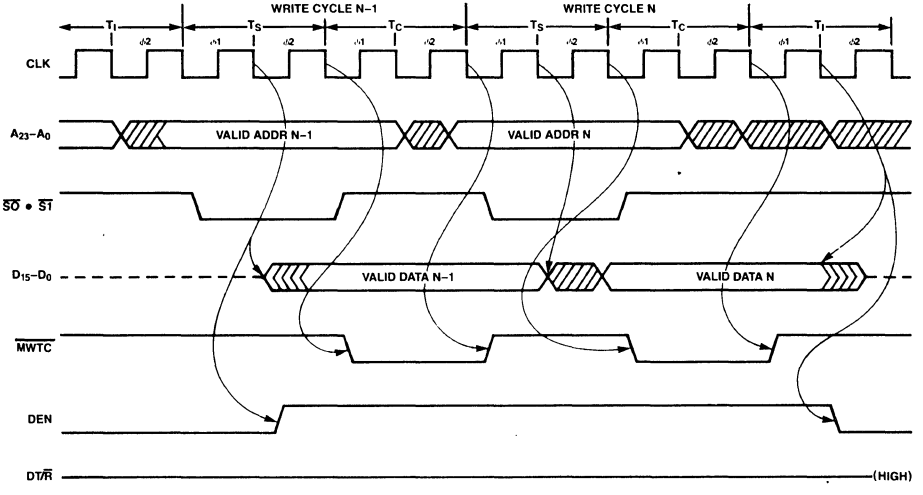
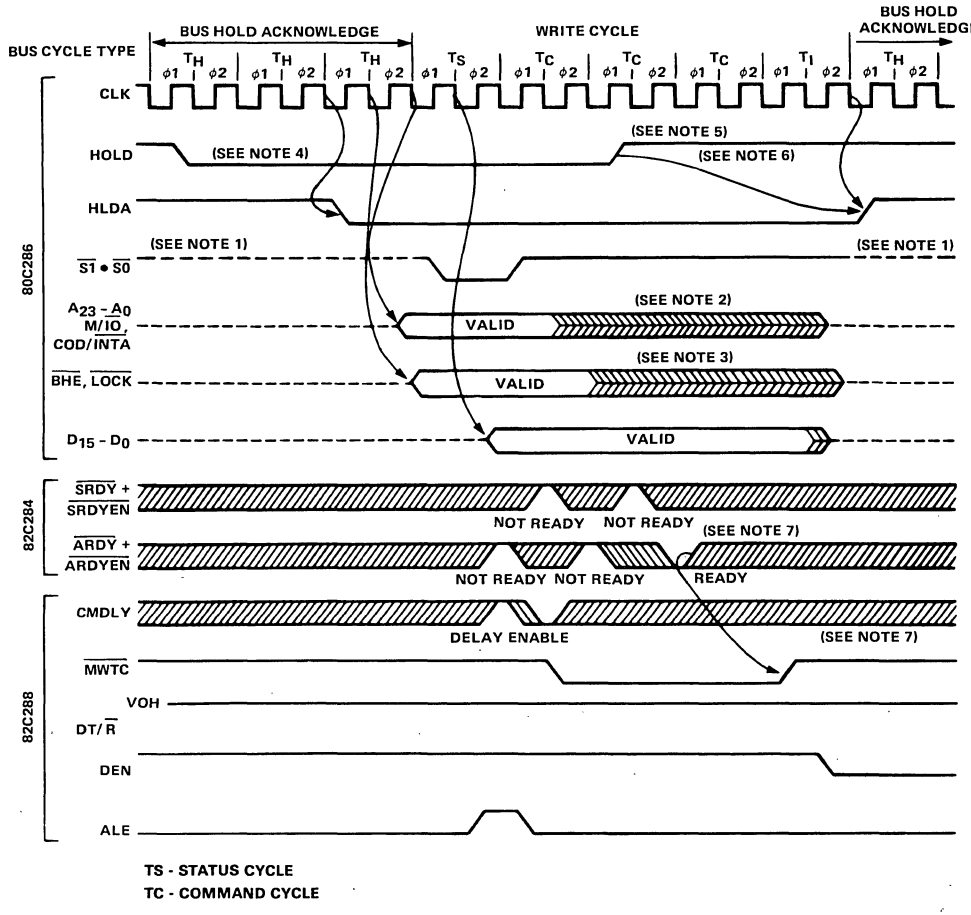


FIGURE 28. BACK TO BACK WRITE-WRITE CYCLE

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.



NOTES:

1. Status lines are not driven by 80C286, yet remain high due to pullup resistors in 82C288 and 82C289 during HOLD state.
2. Address, M/$\overline{IO}$ and COD/$\overline{INTA}$ may start floating during any T_C depending on when internal 80C286 bus arbiter decides to release bus to external HOLD. The float starts in $\phi 2$ of T_C.
3. $\overline{BHE}$ and $\overline{LOCK}$ may start floating after the end of any T_C depending on when internal 80C286 bus arbiter decides to release bus to external HOLD. The float starts in $\phi 1$ of T_C.
4. The minimum HOLD to HLDA time is shown. Maximum is one T_H longer.
5. The earliest HOLD time is shown. It will always allow a subsequent memory cycle if pending is shown.
6. The minimum HOLD to HLDA time is shown. Maximum is a function of the instruction, type of bus cycle and other machine state (i.e., Interrupts, Waits, Lock, etc.).
7. Asynchronous ready allows termination of the cycle. Synchronous ready does not signal ready in this example. Synchronous ready state is ignored after ready is signaled via the asynchronous input.

FIGURE 29. MULTIBUS WRITE TERMINATED BY ASYNCHRONOUS READY WITH BUS HOLD

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Processor Extension Transfers

The processor extension interface uses I/O port addresses 00F8(H), and 00FC(H) which are part of the I/O port address range reserved by Harris. An ESC instruction with Machine Status Word bits EM = 0 and $T_S = 0$ will perform I/O bus operations to one or more of these I/O port addresses independent of the value of IOPL and CPL.

ESC instructions with memory references enable the CPU to accept PEREQ inputs for processor extension operand transfers. The CPU will determine the operand starting address and read/write status of the instruction. For each operand transfer, two or three bus operations are performed, one word transfer with I/O port address 00FA(H) and one or two bus operations with memory. Three bus operations are required for each word operand aligned on an odd byte address.

Interrupt Acknowledge Sequence

Figure 30 illustrates an interrupt acknowledge sequence performed by the 80C286 in response to an INTR input. An interrupt acknowledge sequence consists of two INTA bus operations. The first allows a master 82C59A Programmable Interrupt Controller (PIC) to determine which if any of its slaves should return the interrupt vector. An eight bit vector is read on D_0-D_7 of the 80C286 during the second INTA bus operation to select an interrupt handler routine from the interrupt table.

The Master Cascade Enable (MCE) signal of the 82C288 is used to enable the cascade address drivers during INTA bus operations (See Figure 30) onto the local address bus for distribution to slave interrupt controllers via the system address bus. The 80C286 emits the $\overline{LOCK}$ signal (active LOW) during T_S of the first INTA bus operation. A local bus hold" request will not be honored until the end of the second INTA bus operation.

Three idle processor clocks are provided by the 80C286 between INTA bus operations to allow for the minimum INTA to INTA time and CAS (cascade address) out delay of the 82C59A. The second INTA bus operation must always have at least one extra T_C state added via logic controlling $\overline{READY}$. A_{23}-A_0 are in three-state OFF until after the first T_C state of the second INTA bus operation. This prevents bus contention between the cascade address drivers and CPU address drivers. The extra T_C state allows time for the 80C286 to resume driving the address lines for subsequent bus operations.

Local Bus Usage Priorities

The 80C286 local bus is shared among several internal units and external HOLD requests. In case of simultaneous requests, their relative priorities are:

(Highest) Any transfers which assert $\overline{LOCK}$ either explicitly (via the LOCK instruction prefix) or implicitly (i.e. some segment descriptor accesses, an interrupt acknowledge sequence, or an XCHG with memory).

The second of the two byte bus operations required for an odd aligned word operand.

The second or third cycle of a processor extension data transfer.

Local bus request via HOLD input.

Processor extension data operand transfer via PEREQ input.

Data transfer performed by EU as part of an instruction.

(Lowest) An instruction prefetch request from BU. The EU will inhibit prefetching two processor clocks in advance of any data transfers to minimize waiting by the EU for a prefetch to finish.

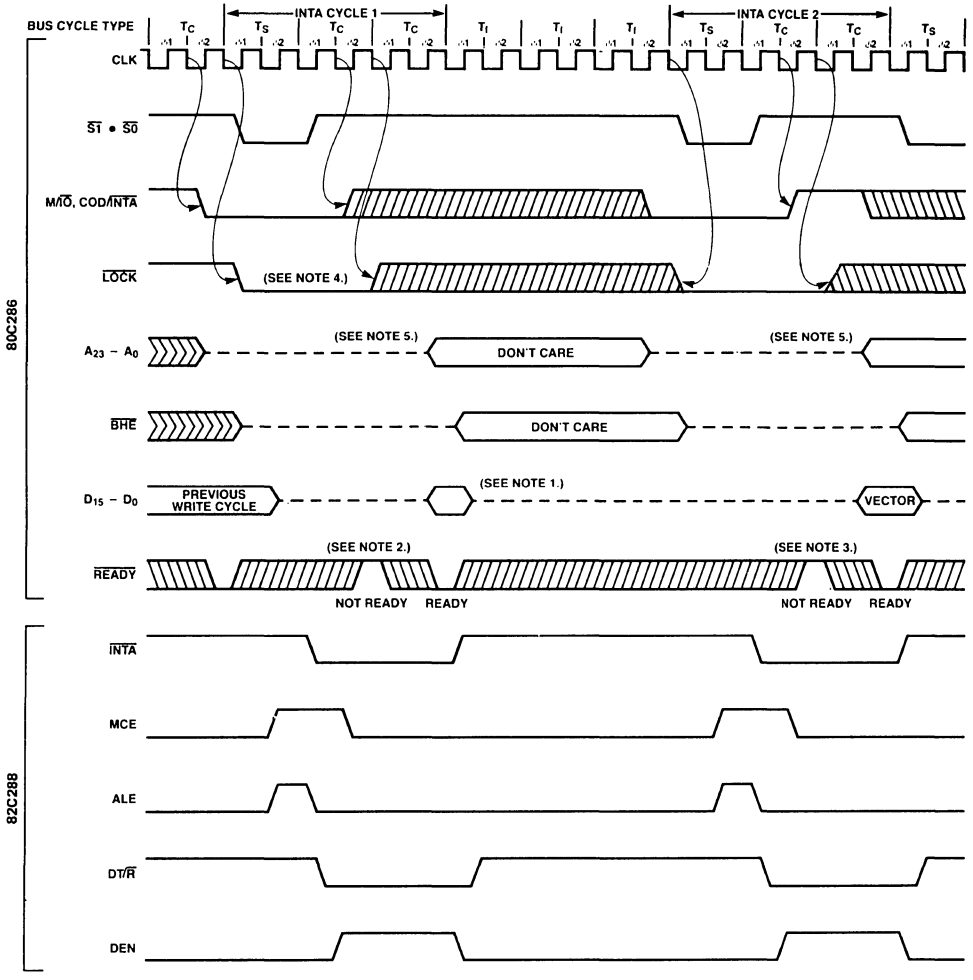
Halt or Shutdown Cycles

The 80C286 externally indicates halt or shutdown conditions as a bus operation. These conditions occur due to a HLT instruction or multiple protection exceptions while attempting to execute one instruction. A halt or shutdown bus operation is signalled when $\overline{S_1}$, $\overline{S_0}$, and COD/$\overline{INTA}$ are LOW and M/$\overline{IO}$ is HIGH. A_1 HIGH indicates halt, and A_1 LOW indicates shutdown. The 82C288 bus controller does not issue ALE, nor is $\overline{READY}$ required to terminate a halt or shutdown bus operation.

During halt or shutdown, the 80C286 may service PEREQ or HOLD requests. A processor extension segment overrun during shutdown will inhibit further service of PEREQ. Either NMI or RESET will force the 80C286 out of either halt or shutdown. An INTR, if interrupts are enabled, or a processor extension segment overrun exception will also force the 80C286 out of halt.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.



NOTES:

1. Data is ignored.
2. First INTA cycle should have at least one wait state inserted to meet 82C59A minimum INTA pulse width.
3. Second INTA cycle must have at least one wait state inserted since the CPU will not drive A_{23}-A_0, $\overline{BHE}$, and $\overline{LOCK}$ until after the first T_C state. The CPU imposed one/clock delay prevents bus contention between cascade address buffer being disabled by MCE ↓ and address outputs. Without the wait state, the 80C286 address will not be valid for a memory cycle started immediately after the second INTA cycle. The 82C59A also requires one wait state for minimum INTA pulse width.
4. $\overline{LOCK}$ is active for the first INTA cycle to prevent the 82289 from releasing the bus between INTA cycles in a multi-master system. $\overline{LOCK}$ is also active for the second INTA cycle.
5. A_{23}-A_0 exits three-state OFF during $\phi 2$ of the second T_C in the INTA cycle.

FIGURE 30. INTERRUPT ACKNOWLEDGE SEQUENCE

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

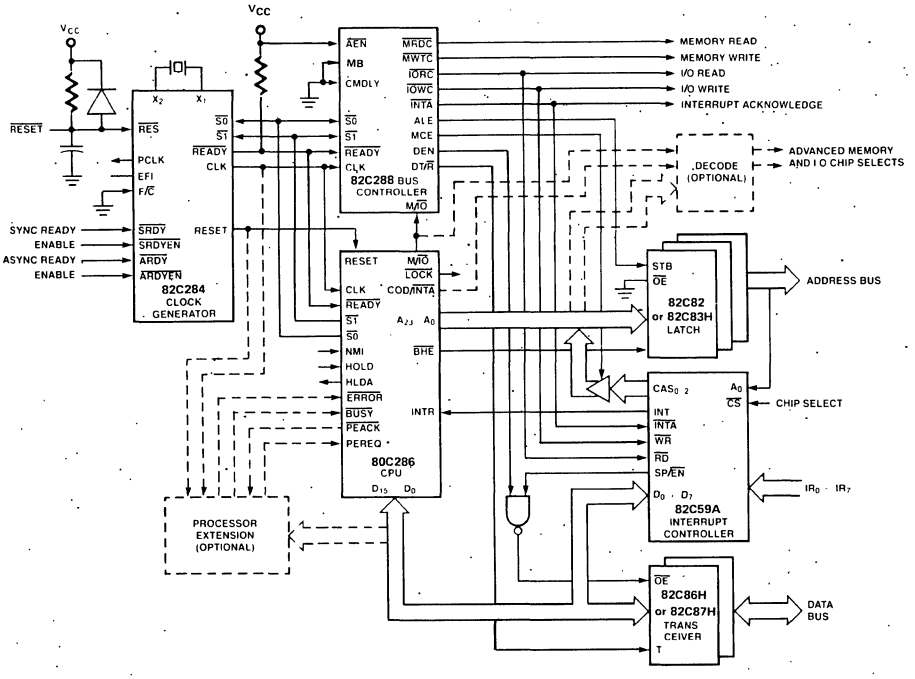


FIGURE 31. BASIC 80C286 SYSTEM CONFIGURATION

System Configurations

The versatile bus structure of the 80C286 micro-system, with a full complement of support chips, allows flexible configuration of a wide range of systems. The basic configuration, shown in Figure 31, is similar to an 80C86 maximum mode system. It includes the CPU plus an 82C59A interrupt controller, 82C284 clock generator, and the 82C288 Bus Controller. The 80C86 latches (82C82 and 82C83H) and transceivers (82C86H and 82C87H) may be used in an 80C286 microsystem.

As indicated by the dashed lines in Figure 31, the ability to add processor extensions is an integral feature of 80C286 based microsystems. The processor extension interface allows external hardware to perform special functions and transfer data concurrent with CPU execution of other instructions. Full system integrity is maintained because the 80C286 supervises all data transfers and instruction execution for the processor extension.

An 80C286 system which includes the 80287 numeric processor extension (NPX) uses this interface. The 80C286/80287 system has all the instructions and data types of an 80C86 or 80C88 with 8087 numeric processor extension. The 80287 NPX can perform numeric calculations and data transfers concurrently with CPU program execution. Numerics code and data have the same integrity as all other information protected by the 80C286 protection mechanism.

The 80C286 can overlap chip select decoding and address propagation during the data transfer for the previous bus operation. This information is latched into the 82C82/83H's by ALE during the middle of a T_S cycle. The latched chip select and address information remains stable during the bus operation while the next cycle's address is being decoded and propagated into the system. Decode logic can be implemented with a high speed PROM or PAL.

The optional decode logic shown in Figure 31 takes advantage of the overlap between address and data of the 80C286 bus cycle to generate advanced memory and I/O-select signals. This minimizes system performance degradation caused by address propagation and decode delays. In addition to selecting memory and I/O, the advanced selects may be used with configurations supporting local and system buses to enable the appropriate bus interface for each bus cycle. The COD/$\overline{INTA}$

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

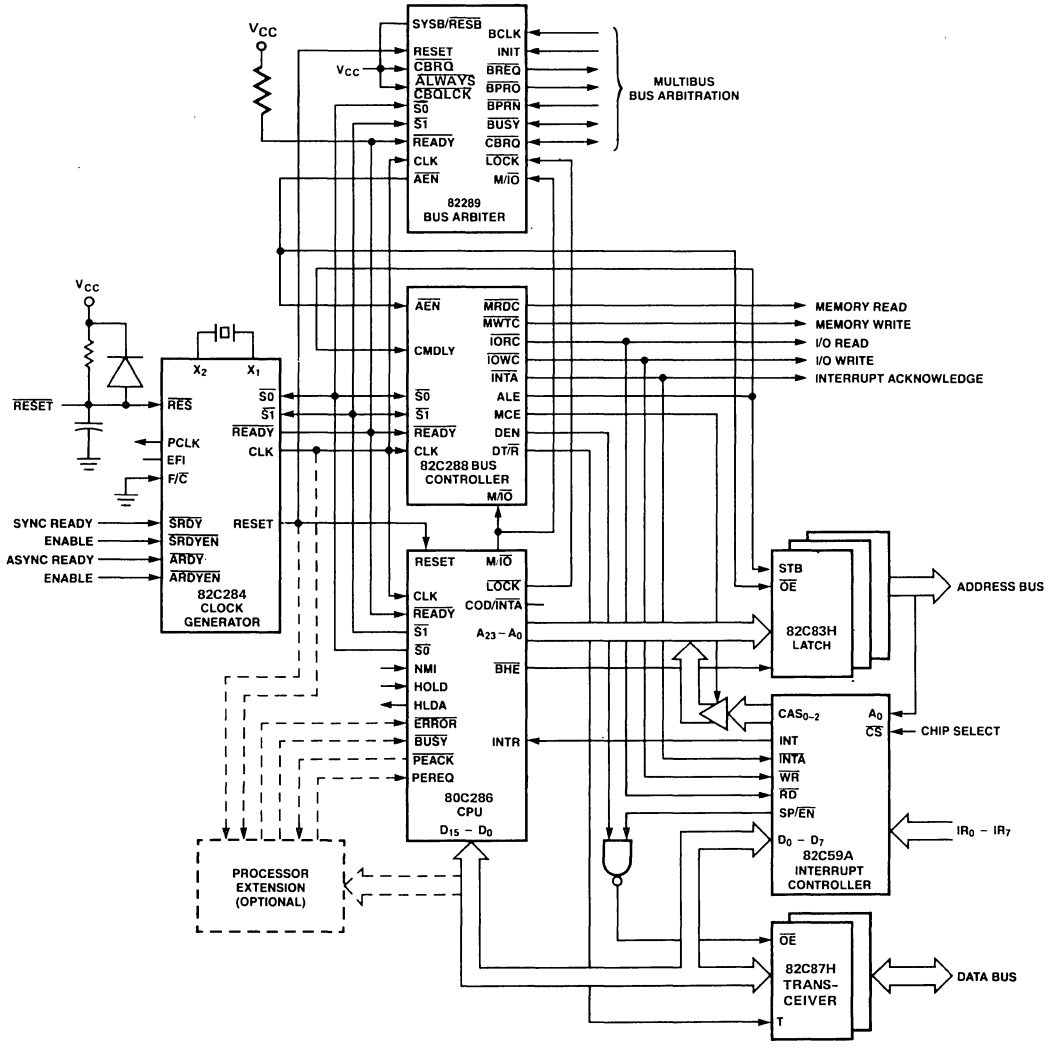


FIGURE 32. MULTIBUS SYSTEM BUS INTERFACE

and M/$\overline{IO}$ signals are applied to the decode logic to distinguish between interrupt, I/O, code, and data bus cycles.

By adding the 82289 bus arbiter chip the 80C286 provides a Multibus system bus interface as shown in Figure 32. The ALE output of the 82C288 for the Multibus bus is connected to its CMDLY input to delay the start of commands one system CLK as required to meet Multibus address and write data setup times. This arrangement will add at least one extra T_C state to each bus operation which uses the Multibus.

A second 82C288 bus controller and additional latches and transceivers could be added to the local bus of Figure 32. This configuration allows the 80C286 to support an on-board bus for local memory and peripherals, and the Multibus for system bus interfacing.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

80C286 Instruction Set Summary

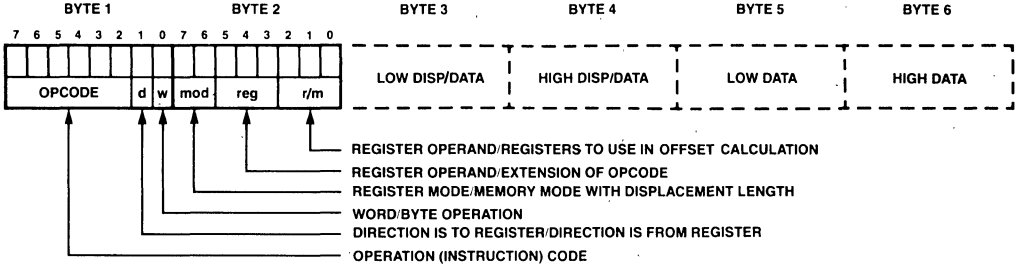
Instruction Timing Notes

The instruction clock counts listed below establish the maximum execution rate of the 80C286. With no delays in bus cycles, the actual clock count of an 80C286 program will average 5% more than the calculated clock count, due to instruction sequences which execute faster than they can be fetched from memory.

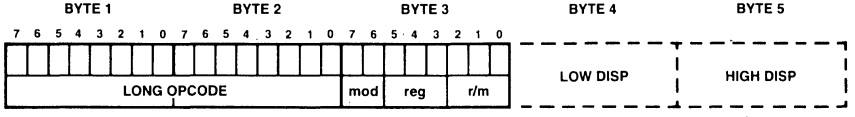
To calculate elapsed times for instruction sequences, multiply the sum of all instruction clock counts, as listed in the table below, by the processor clock period. An 12.5MHz processor clock has a clock period of 80 nanoseconds and requires an 80C286 system clock (CLK input) of 25MHz.

Instruction Clock Count Assumptions

1. The instruction has been prefetched, decoded and is ready for execution. Control transfer instruction clock counts include all time required to fetch, decode, and prepare the next instruction for execution.
2. Bus cycles do not require wait states.
3. There are no processor extension data transfer or local bus HOLD requests.
4. No exceptions occur during instruction execution.



A. SHORT OPCODE FORMAT EXAMPLE



B. LONG OPCODE FORMAT EXAMPLE

FIGURE 33. 80C286 INSTRUCTION FORMAT EXAMPLES

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Instruction Set Summary Notes

Addressing displacements selected by the MOD field are not shown. If necessary they appear after the instruction fields shown.

Above/below refers to unsigned value

Greater refers to more positive signed values

Less refers to less positive (more negative) signed values

if d = 1, then "to" register; if d = 0 then "from" register

if w = 1, then word instruction; if w = 0, then byte instruction

if s = 0, then 16-bit immediate data form the operand

if s = 1 then an immediate data byte is sign-extended to form the 16-bit operand

x don't care

z used for string primitives for comparison with ZF FLAG

If two clock counts are given, the smaller refers to a register operand and the larger refers to a memory operand

= add one clock if offset calculation requires summing 3 elements

= number of times repeated

= number of bytes of code in next instruction

Level (L)—Lexical nesting level of the procedure

The following comments describe possible exceptions, side effects and allowed usage for instructions in both operating modes of the 80C286.

Real Address Mode Only

1. This is a protected mode instruction. Attempted execution in real address mode will result in an undefined opcode exception (6).
2. A segment overrun exception (13) will occur if a word operand reference at offset FFFF(H) is attempted.
3. This instruction may be executed in real address mode to initialize the CPU for protected mode.
4. The IOPL and NT fields will remain 0.
5. Processor extension segment overrun interrupt (9) will occur if the operand exceeds the segment limit.

Either Mode

6. An exception may occur, depending on the value of the operand.
7. $\overline{\text{LOCK}}$ is automatically asserted regardless of the presence or absence of the LOCK instruction prefix.
8. $\overline{\text{LOCK}}$ does not reamain active between all operand transfers.

Protected Virtual Address Mode Only

9. A general protection exception (13) will occur if the memory operand cannot be used due to either a segment limit or access rights violation. If a stack segment limit is violated, a stack segment overrun exception (12) occurs.
10. For segment load operations, the CPL, RPL and DPL must agree with privilege rules to avoid an exception. The segment must be present to avoid a not-present exception (11). If the SS register is the destination and a segment not-present violation occurs, a stack exception (12) occurs.
11. All segment descriptor accesses in the GDT or LDT made by this instruction will automatically assert $\overline{\text{LOCK}}$ to maintain descriptor integrity in multiprocessor systems.
12. JMP, CALL, INT, RET, IRET instructions referring to another code segment will cause a general protection exception (13) if any privilege rule is violated.
13. A general protection exception (13) occurs if CPL $\neq$ 0.
14. A general protection exception (13) occurs if CPL > IOPL.
15. The IF field of the flag word is not updated if CPL > IOPL. The IOPL field is updated only if CPL = 0.
16. Any violation of privilege rules as applied to the selector operand does not cause a protection exception; rather, the instruction does not return a result and the zero flag is cleared.
17. If the starting address of the memory operand violates a segment limit, or an invalid access is attempted, a general protection exception (13) will occur before the ESC instruction is executed. A stack segment overrun exception (12) will occur if the stack limit is violated by the operand's starting address. If a segment limit is violated during an attempted data transfer than a processor extension segment overrun exception (9) occurs.
18. The destination of an INT, JMP, CALL, RET or IRET instruction must be in the defined limit of a code segment or a general protection exception (13) will occur.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

80C286 Instruction Set Summary

FUNCTION	FORMAT	CLOCK COUNT		COMMENTS	
		Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
DATA TRANSFER					
MOV = Move:					
Register to Register/Memory	1000100w mod reg r/m	2,3*	2,3*	2	9
Register/memory to register	1000101w mod reg r/m	2,5*	2,5*	2	9
Immediate to register/memory	1100011w mod 000 r/m data data if w = 1	2,3*	2,3*	2	9
Immediate to register	1011w reg data data if w=1	2	2		
Memory to accumulator	1010000w addr-low addr-high	5	5	2	9
Accumulator to memory	1010001w addr-low addr-high	3	3	2	9
Register/memory to segment register	10001110 mod 0 reg r/m	2,5*	17,19*	2	9,10,11
Segment register to register/memory	10001100 mod 0 reg r/m	2,3*	2,3*	2	9
PUSH = Push:					
Memory	11111111 mod 1 1 0 r/m	5*	5*	2	9
Register	01010 reg	3	3	2	9
Segment register	000reg110	3	3	2	9
Immediate	011010s0 data data if s=0	3	3	2	9
PUSHA = Push All	01100000	17	17	2	9
POP = Pop:					
Memory	10001111 mod 000 r/m	5*	5*	2	9
Register	01011 reg	5	5	2	9
Segment register	000reg111 (reg≠01)	5	20	2	9,10,11
POPA = Pop All	01100001	19	19	2	9
XCHG = Exhcange:					
Register/memory with register	1000011w mod reg r/m	3,5*	3,5*	2,7	7,9
Register with accumulator	10010 reg	3	3		
IN = Input from:					
Fixed port	1110010w port	5	5		14
Variable port	1110110w	5	5		14
OUT = Output to:					
Fixed port	1110011w port	3	3		14
Variable port	1110111w	3	3		14
XLAT = Translate byte to AL	11010111	5	5		9
LEA = Load EA to register	10001101 mod reg r/m	3*	3*		
LDS = Load pointer to DS	11000101 mod reg r/m (mod≠11)	7*	21*	2	9,10,11
LES = Load pointer to ES	11000100 mod reg r/m (mod≠1)	7*	21*	2	9,10,11

Shaded areas indicate instructions not available in 80C86/88 microsystems.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT	CLOCK COUNT		COMMENTS	
		Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
DATA TRANSFER (Continued)					
LAHF Load AH with flags	10011111	2	2		
SAHF = Store AH into flags	10011110	2	2		
PUSHF = Push flags	10011100	3	3	2	9
POPF = Pop flags	10011101	5	5	2,4	9,15
ARITHMETIC					
ADD = **Add:**					
Reg/memory with register to either	000000dw | mod reg r/m	2,7*	2,7*	2	9
Immediate to register/memory	100000sw | mod 000 r/m | data | data if s w = 01	3,7*	3,7*	2	9
Immediate to accumulator	0000010w | data | data if w=1	3	3		
ADC = **Add with carry:**					
Reg/memory with register to either	000100dw | mod reg r/m	2,7*	2,7*	2	9
Immediate to register/memory	100000sw | mod 010 r/m | data | data if s w = 01	3,7*	3,7*	2	9
Immediate to accumulator	0001010w | data | data if w=1	3	3		
INC = **Increment:**					
Register/memory	1111111w | mod 000 r/m	2,7*	2,7*	2	9
Register	01000reg	2	2		
SUB = **Subtract:**					
Reg/memory and register to either	001010dw | mod reg r/m	2,7*	2,7*	2	9
Immediate from register/memory	100000sw | mod 101 r/m | data | data if s w = 01	3,7*	3,7*	2	9
Immediate from accumulator	0010110w | data | data if w=1	3	3		
SBB = **Subtract with borrow:**					
Reg/memory and register to either	000110dw | mod reg r/m	2,7*	2,7*	2	9
Immediate from register/memory	100000sw | mod 011 r/m | data | data if s w=01	3,7*	3,7*	2	9
Immediate from accumulator	0001110w | data | data if w=1	3	3		
DEC = **Decrement**					
Register/memory	1111111w | mod 001 r/m	2,7*	2,7*	2	9
Register	01001 reg	2	2		
CMP = **Compare**					
Register/memory with register	0011101w | mod reg r/m	2,6*	2,6*	2	9
Register with register/memory	0011100w | mod reg r/m	2,7*	2,7*	2	9
Immediate with register/memory	100000sw | mod 111 r/m | data | data if s w=01	3,6*	3,6*	2	9
Immediate with accumulator	0011110w | data | data if w=1	3	3		
NEG = Change sign	1111011w | mod 011 r/m	2	7*	2	9
AAA = ASCII adjust for add	00110111	3	3		
DAA = Decimal adjust for add	00100111	3	3		

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT	CLOCK COUNT: Real Address Mode	CLOCK COUNT: Protected Virtual Address Mode	COMMENTS: Real Address Mode	COMMENTS: Protected Virtual Address Mode
ARITHMETIC (Continued)					
AAS = ASCII adjust for subtract	00111111	3	3		
DAS = Decimal adjust for subtract	00101111	3	3		
MUL = Multiply (unsigned):	1111011w mod100 r/m				
Register-Byte		13	13		
Register-Word		21	21		
Memory-Byte		16*	16*	2	9
Memory-Word		24*	24*	2	9
IMUL = Integer multiply (signed):	1111011w mod101 r/m				
Register-Byte		13	13		
Register-Word		21	21		
Memory-Byte		16*	16*	2	9
Memory-Word		24*	24*	2	9
IMUL = Integer immediate multiply (signed)	011010s1 mod reg r/m data data if s = 0	21,24*	21,24*	2	9
DIV = Divide (unsigned)	1111011w mod 110 r/m				
Register-Byte		14	14	6	6
Register-Word		22	22	6	6
Memory-Byte		17*	17*	2,6	6,9
Memory-Word		25*	25*	2,6	6,9
IDIV = Integer divide (signed)	1111011w mod111 r/m				
Register-Byte		17	17	6	6
Register-Word		25	25	6	6
Memory-Byte		20*	20*	2,6	6,9
Memory-Word		28*	28*	2,6	6,9
AAM = ASCII adjust for multiply	11010100 00001010	16	16		
AAD = ASCII adjust for divide	11010101 00001010	14	14		
CBW = Convert byte to word	10011000	2	2		
CWD = Convert word to double word	10011001	2	2		
LOGIC					
Shift/Rotate Instructions:					
Register/Memory by 1	1101000w mod TTT r/m	2,7*	2,7*	2	9
Register/Memory by CL	1101001w mod TTT r/m	5+n,8+n*	5+n,8+n*	2	9
Register/Memory by Count	1100000w mod TTT r/m count	5+n,8+n*	5+n,8+n*	2	9

TTT	Instruction
000	ROL
001	ROR
010	RCL
011	RCR
100	SHL/SAL
101	SHR
111	SAR

Shaded areas indicate instructions not available in 80C86/88 microsystems.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT	CLOCK COUNT		COMMENTS	
		Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
ARITHMETIC (Continued)					
AND = And:					
Reg/memory and register to either	001000dw | mod reg r/m	2,7*	2,7*	2	9
Immediate to register/memory	1000000w | mod 100 r/m | data | data if w=1	3,7*	3,7*	2	9
Immediate to accumulator	0010010w | data | data if w=1	3	3		
TEST = And function to flags, no result:					
Register/memory and register	1000010w | mod reg r/m	2,6*	2,6*	2	9
Immediate data and register/memory	1111011w | mod 000 r/m | data | data if w=1	3,6*	3,6*	2	9
Immediate data and accumulator	1010100w | data | data if w=1	3	3		
OR = Or:					
Reg/memory and register to either	000010dw | mod reg r/m	2,7*	2,7*	2	9
Immediate to register/memory	1000000w | mod 001 r/m | data | data if w=1	3,7*	3,7*	2	9
Immediate to accumulator	0000110w | data | data if w=1	3	3		
XOR = Exclusive or:					
Reg/memory and register to either	001100dw | mod reg r/m	2,7*	2,7*	2	9
Immediate to register/memory	1000000w | mod 110 r/m | data | data if w = 1	3,7*	3,7*	2	9
Immediate to accumulator	0011010w | data | data if w = 1	3	3		
NOT = Invert register/memory	1111011w | mod 010 r/m	2,7*	2,7*	2	9
STRING MANIPULATION:					
MOVS = Move byte/word	1010010w	5	5	2	9
CMPS = Compare byte/word	1010011w	8	8	2	9
SCAS = Scan byte/word	1010111w	7	7	2	9
LODS = Load byte/wd to AL/AX	1010110w	5	5	2	9
STOS = Stor byte/wd from AL/A	1010101w	3	3	2	9
INS = Input byte/wd from DX port	0110110w	5	5	2	9,14
OUTS = Output byte/wd to DX port	0110111w	5	5	2	9,14
Repeated by count in CX					
MOVS = Move string	11110011 | 1010010w	5+4n	5+4n	2	9
CMPS = Compare string	1111001z | 1010011w	5+9n	5+9n	2,8	8,9
SCAS = Scan string	1111001z | 1010111w	5+8n	5+8n	2,8	8,9
LODS = Load string	11110011 | 1010110w	5+4n	5+4n	2,8	8,9
STOS = Store string	11110011 | 1010101w	4+3n	4+3n	2,8	8,9
INS = Input string	11110011 | 0110110w	5+4n	5+4n	2	9,14
OUTS = Output string	11110011 | 0110111w	5+4n	5+4n	2	9,14

Shaded areas indicate instructions not available in 80C86/88 microsystems.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT				CLOCK COUNT		COMMENTS	
					Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
CONTROL TRANSFER								
CALL = Call:								
Direct within segment	11101000	disp-low	disp-high		7+m	7+m	2	18
Register/memory indirect within segment	11111111	mod 010 r/m			7+m, 11+m*	7+m, 11+m*	2,8	8,9,18
Direct intersegment	10011010	segment offset			13+m	26+m	2	11,12,18
Protected Mode Only (Direct Intersegment):		segment selector						
Via call gate to same privilege level						41+m		8,11,12,18
Via call gate to different privilege level, no parameters						82+m		8,11,12,18
Via call gate to different privilege level, x parameters						86+4x+m		8,11,12,18
Via TSS						177+m		8,11,12,18
Via task gate						182+m		8,11,12,18
Indirect intersegment	11111111	mod 011 r/m		(mod≠11)	16+m	29+m*	2	8,9,11,12,18
Protected Mode Only (Indirect Intersegment):								
Via call gate to same privilege level						44+m*		8,9,11,12,18
Via call gate to different privilege level, no parameters						83+m*		8,9,11,12,18
Via call gate to different privilege level, x parameters						90+4x+m*		8,9,11,12,18
Via TSS						180+m*		8,9,11,12,18
Via task gate						185+m*		8,9,11,12,18
JMP = Unconditional jump:								
Short/long	11101011	disp-low			7+m	7+m		18
Direct within segment	11101001	disp-low	disp-high		7+m	7+m		18
Register/memory indirect within segment	11111111	mod 100 r/m			7+m, 11+m*	7+m, 11+m*	2	9,18
Direct intersegment	11101010	segment offset			11+m	23+m		11,12,18
Protected Mode Only (Direct Intersegment):		segment selector						
Via call gate to same privilege level						38+m		8,11,12,18
Via TSS						175+m		8,11,12,18
Via task gate						180+m		8,11,12,18
Indirect intersegment	11111111	mod 101 r/m		(mod≠11)	15+m*	26+m*	2	8,9,11,12,18
Protected Mode Only (Indirect Intersegment):								
Via call gate to same privilege level						41+m*		8,9,11,12,18
Via TSS						178+m*		8,9,11,12,18
Via task gate						183+m*		8,9,11,12,18
RET = Return from CALL:								
Within segment	11000011				11+m	11+m	2	8,9,18
Within seg adding immed to SP	11000010	data-low	data-high		11+m	11+m	2	8,9,18
Intersegment	11001011				15+m	25+m	2	8,9,11,12,18
Intersegment adding immediate to SP	11001010	data-low	data-high		15+m		2	8,9,11,12,18
Protected Mode Only (RET):								
To different privilege level						55+m		9,11,12,18

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT	CLOCK COUNT: Real Address Mode	CLOCK COUNT: Protected Virtual Address Mode	COMMENTS: Real Address Mode	COMMENTS: Protected Virtual Address Mode
CONTROL TRANSFER (Continued)					
JE/JZ = Jump on equal zero	01110100 disp	7+m or 3	7+m or 3		18
JL/JNGE = Jump on less/not greater or equal	01111100 disp	7+m or 3	7+m or 3		18
JLE/JNG = Jump on less or equal/not greater	01111110 disp	7+m or 3	7+m or 3		18
JB/JNAE = Jump on below/not above or equal	01110010 disp	7+m or 3	7+m or 3		18
JBE/JNA = Jump on below or equal/not above	01110110 disp	7+m or 3	7+m or 3		18
JP/JPE = Jump on parity/parity even	01111010 disp	7+m or 3	7+m or 3		18
JO = Jump on overflow	01110000 disp	7+m or 3	7+m or 3		18
JS = Jump on sign	01111000 disp	7+ m or 3	7+m or 3		18
JNE/JNZ = Jump on not equal/not zero	01110101 disp	7+m or 3	7+m or 3		18
JNL/JGE = Jump on not less/greater or equal	01111101 disp	7+m or 3	7+m or 3		18
JNLE/JG = Jump on not less or equal/greater	01111111 disp	7+m or 3	7+m or 3		18
JNB/JAE = Jump on not below/above or equal	01110011 disp	7+m or 3	7+m or 3		18
JNBE/JA = Jump on not below or equal/above	01110111 disp	7+m or 3	7+m or 3		18
JNP/JPO = Jump on not par/par odd	01111011 disp	7+m or 3	7+m or 3		18
JNO = Jump on not overflow	01110001 disp	7+m or 3	7+m or 3		18
JNS = Jump on not sign	01111001 disp	7 +m or 3	7+m or 3		18
LOOP = Loop CX times	11100010 disp	8 +m or 4	8+m or 4		18
LOOPZ/LOOPE = Loop while zero/equal	11100001 disp	8+m or 4	8+m or 4		18
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000 disp	8+m or 4	8+m or 4		18
JCXZ = Jump on CX zero	11100011 disp	8 +m or 4	8+m or 4		18
ENTER = Enter Procedure	11001000 data-low data-high L			2,8	8,8
L=0		11	11	2,8	8,8
L=1		15	15	2,8	8,8
L > 1		16+4(L − 1)	16+4(L − 1)	2,8	8,8
LEAVE = Leave Procedure	11001001	5	5		
INT = Interrupt:					
Type specified	11001101 type	23+m		2,7,8	
Type 3	11001100	23+m		2,7,8	
INTO = Interrupt on overflow	11001110	24 +m or 3 (3 if no interrupt)	(3 if no interrupt)	2,6,8	

Shaded areas indicate instructions not available in 80C86/88 microsystems.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT	CLOCK COUNT: Real Address Mode	CLOCK COUNT: Protected Virtual Address Mode	COMMENTS: Real Address Mode	COMMENTS: Protected Virtual Address Mode
CONTROL TRANSFER (Continued)					
Protected Mode Only:					
Via interrupt or trap gate to same privilege level			40+ m		7,8,11,12,18
Via interrupt or trap gate to fit different privilege level			78+ m		7,8,11,12,18
Via Task Gate			167+m		7,8,11,12,18
IRET = Interrupt return	11001111	17+m	31+ m	2,4	8,9,11,12,15,18
Protected Mode Only:					
To different privilege level			55+m		8,9,11,12,15,18
To different task (NT = 1)			169+m		8,9,11,12,18
BOUND = Detect value out of range	01100010 mod reg r/m	13*	19* (Use INT clock count if exception 5)	2,5	8,9,11,12,18
PROCESSOR CONTROL					
CLC = Clear carry	11111000	2	2		
CMC = Complement carry	11110101	2	2		
STC = Set carry	11111001	2	2		
CLD = Clear direction	11111100	2	2		
STD = Set direction	11111101	2	2		
CLI = Clear interrupt	11111010	3	3		14
STI = Set interrupt	11111011	2	2		14
HLT = Halt	11110100	2	2		13
WAIT = Wait	10011011	3	3		
LOCK = Bus lock prefix	11110000	0	0		14
CTS = Clear task switched flag	00001111 00000110	2	2	2	18
ESC = Processor Extension Escape	11011TTT mod LLL r/m (TTT LLL are opcode to processor extension)	9–20*	9–20*	5,8	8,17
SEG = Segment Override Prefix	001 reg 110	0	0		
PROTECTION CONTROL					
LGDT = Load global descriptor table register	00001111 00000001 mod 010 r/m	11*	11*	2,3	9,13
SGDT = Store global descriptor table register	00001111 00000001 mod 000 r/m	11*	11*	2,3	9
LIDT = Load interrupt descriptor table register	00001111 00000001 mod 011 r/m	12*	12*	2,3	9,13
SIDT = Store interrupt descriptor table register	00001111 00000001 mod 001 r/m	12*	12*	2,3	9
LLDT = Load local descriptor table register from register memory	00001111 00000000 mod 010 r/m		17,19*	1	9,11,13
SLDT = Store local descriptor table register to register/memory	00001111 00000000 mod 000 r/m		2,3*	1	9

Shaded areas indicate instructions not available in 80C86/88 microsystems.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT	CLOCK COUNT		COMMENTS	
		Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
PROTECTION CONTROL (Continued)					
LTR = Load task register from register/memory	00001111 | 00000000 | mod 011 r/m		17,19*	1	9,11,13
STR = Store task register to register memory	00001111 | 00000000 | mod 001 r/m		2,3*	1	9
LMSW = Load machine status word from register/memory	00001111 | 00000001 | mod 110 r/m	3,6*	3,6*	2,3	9,13
SMSW = Store machine status word	00001111 | 00000001 | mod 100 r/m	2,3*	2,3*	2,3	9
LAR = Load access rights from register/memory	00001111 | 00000010 | mod reg r/m		14,16*	1	9,11,16
LSL = Load segment limit from register/memory	00001111 | 00000011 | mod reg r/m		14,16*	1	9,11,16
ARPL = Adjust requested privilege level: from register/memory	01100011 | mod reg r/m		10*,11*	2	8,9
VERR = Verify read access: register/memory	00001111 | 00000000 | mod 100 r/m		14,16*	1	9,11,16
VERR = Verify write access:	00001111 | 00000000 | mod 101 r/m		14,16*	1	9,11,16

Shaded areas indicate instructions not available in 80C86/88 microsystems.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

80C286 Machine Instruction Encoding Matrix

HI	LO															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	ADD b,f,r/m	ADD w,f,r/m	ADD b,t,r/m	ADD w,t,r/m	ADD b,ia	ADD w,ia	PUSH ES	POP ES	OR b,f,r/m	OR w,f,r/m	OR b,t,r/m	OR w,t,r/m	OR b,i	OR w,i	PUSH CS	PVAM n
1	ADC b,f,r/m	ADC w,f,r/m	ADC b,t,r/m	ADC w,t,r/m	ADC b,ia	ADC w,ia	PUSH SS	POP SS	SBB b,f,r/m	SBB w,f,r/m	SBB b,t,r/m	SBB w,t,r/m	SBB b,i	SBB w,i	PUSH DS	POP DS
2	AND b,f,r/m	AND w,f,r/m	AND b,t,r/m	AND w,t,r/m	AND b,ia	AND w,ia	SEG =ES	DAA	SUB b,f,r/m	SUB w,f,r/m	SUB b,t,r/m	SUB w,t,r/m	SUB b,i	SUB w,i	SEG =CS	DAS
3	XOR b,f,r/m	XOR w,f,r/m	XOR b,t,r/m	XOR w,t,r/m	XOR b,ia	XOR w,ia	SEG =SS	AAA	CMP b,f,r/m	CMP w,f,r/m	CMP b,t,r/m	CMP w,t,r/m	CMP b,i	CMP w,i	SEG =DS	AAS
4	INC AX	INC CX	INC DX	INC BX	INC SP	INC BP	INC SI	INC DI	DEC AX	DEC CX	DEC DX	DEC BX	DEC SP	DEC BP	DEC SI	DEC DI
5	PUSH AX	PUSH CX	PUSH DX	PUSH BX	PUSH SP	PUSH BP	PUSH SI	PUSH DI	POP AX	POP CX	POP DX	POP BX	POP SP	POP BP	POP SI	POP DI
6	PUSHA	POPA	BOUND	ARPL					PUSH w,i	IMUL w,t,r/m,i	PUSH b,i	IMUL b,t,r/m,i	INSB	INSW	OUTSB	OUTSW
7	JO	JNO	JB/ JNAE	JNB/ JAE	JE/ JZ	JNE/ JNZ	JBE/ JNA	JNBE/ JA	JS	JNS	JP/ JPE	JNP/ JPO	JL/ JNGE	JNL/ JGE	JLE/ JNG	JNLE/ JG
8	Immed b,r/m	Immed w,r/m	Immed b,r/m	Immed is,r/m	TEST b,r/m	TEST w,r/m	XCHG b,r/m	XCHG w,r/m	MOV b,f,r/m	MOV w,f,r/m	MOV b,t,r/m	MOV w,t,r/m	MOV sr,f,r/m	LEA	MOV sr,t,r/m	POP r/m
9	XCHG AX	XCHG CX	XCHG DX	XCHG BX	XCHG SP	XCHG BP	XCHG SI	XCHG DI	CBW	CWD	CALL i,d	WAIT	PUSHF	POPF	SAHF	LAHF
A	MOV m-AL	MOV m-AX	MOV AL-m	MOV AX-m	MOVSB	MOVSW	CMPSB	CMPSW	TEST b,i,a	TEST w,i,a	STOSB	STOSW	LODSB	LODSW	SCASB	SCASW
B	MOV i-AL	MOV i-CL	MOV i-DL	MOV i-BL	MOV i-AH	MOV i-CH	MOV i-DH	MOV i-BH	MOV i-AX	MOV i-CX	MOV i-DX	MOV i-BX	MOV i-SP	MOV i-BP	MOV i-SI	MOV i-DI
C	Shift b,i	Shift w,i	RET (i+SP)	RET	LES	LDS	MOV b,i,r/m	MOV w,i,r/m	ENTER	LEAVE	RET l,(i+SP)	RET l	INT Type 3	INT (any)	INTO	IRET
D	Shift b	Shift w	Shift b,CL	Shift b,CL	AAM	AAD		XLAT	ESC 0	ESC 1	ESC 2	ESC 3	ESC 4	ESC 5	ESC 6	ESC 7
E	LOOPNZ/ LOOPNE	LOOPZ/ LOOPE	LOOP	JCXZ	IN b	IN w	OUT b	OUT w	CALL d	JMP d	JMP i,d	JMP si,d	IN DX,b	IN DX,w	OUT DX,b	OUT DX,w
F	LOCK		REP	REPZ	HLT	CMC	Grp 1 b,r/m	Grp 1 w,r/m	CLC	STC	CLI	STI	CLD	STD	Grp 2 b,r/m	Grp 2 w,r/m

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

80C286 Machine Instruction Encoding Matrix (Continued)

where:

mod r/m	000	001	010	011	100	101	110	111
Immed	ADD	OR	ADC	SBB	AND	SUB	XOR	CMP
Shift	ROL	ROR	RCL	RCR	SHL/SAL	SHR	—	SAR
Grp 1	TEST	—	NOT	NEG	MUL	IMUL	DIV	IDIV
Grp 2	INC	DEC	CALL id	CALL I,id	JMP id	JMP I,id	PUSH	—
PVAM 0	SLDT	STR	LLDT	LTR	VERR	VERW	—	—
PVAM 1	SGDT	SIDT	LGDT	LIDT	SMSW	—	LMSW	—
PVAM 2	LAR							
PVAM 3	LSL							
PVAM 6	CLTS							

b = byte operation
d = direct
f = from CPU reg
i = immediate
ia = immediate to AX
id = indirect
is = immediate byte sign extension
l = long ie. intersegment
n = 2nd. byte of PVAM instruction
m = memory
r/m = EA is second byte
si = short intrasegment
sr = segment register
t = to CPU register
v = variable
w = word operation
z = zero

Footnotes

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign extended to 16 bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data is required)

* except if mod = 00 and r/m = 110 then EQ = disp-high: disp-low.

Segment Override Prefix

0 0 1	reg	1 1 0

reg is assigned according to the following:

REG	SEGMENT REGISTER
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-BIT (w = 1)		8-BIT (w = 0)	
000	AX	000	AL
001	CX	001	CL
010	DX	010	DL
011	BX	011	BL
100	SP	100	AH
101	BP	101	CH
110	SI	110	DH
111	DI	111	BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

HARRIS

80C86/883

June 1989

CMOS 16 Bit Microprocessor

Features

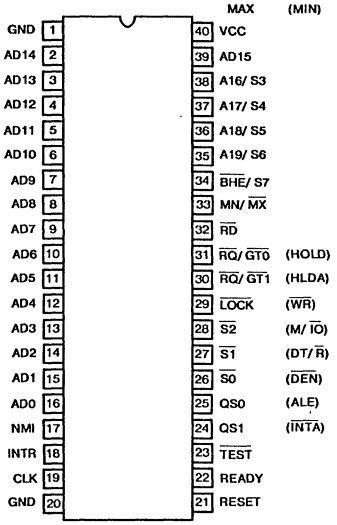
- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Compatible with NMOS 8086
- 5MHz Operation 80C86/883
- 8MHz Operation 80C86-2/883
- Low Power Operation
  - ICCSB ..... 500µA Max
  - ICCOP ..... 10mA/MHz Max
- 1MByte of Direct Memory Addressing Capability
- 24 Operand Addressing Modes
- Bit, Byte, Word and Block Move Operations
- 8 Bit and 16 Bit Signed/Unsigned Arithmetic
  - Binary, or Decimal
  - Multiply and Divide
- Operating Temperature Range .... -55°C to +125°C

Description

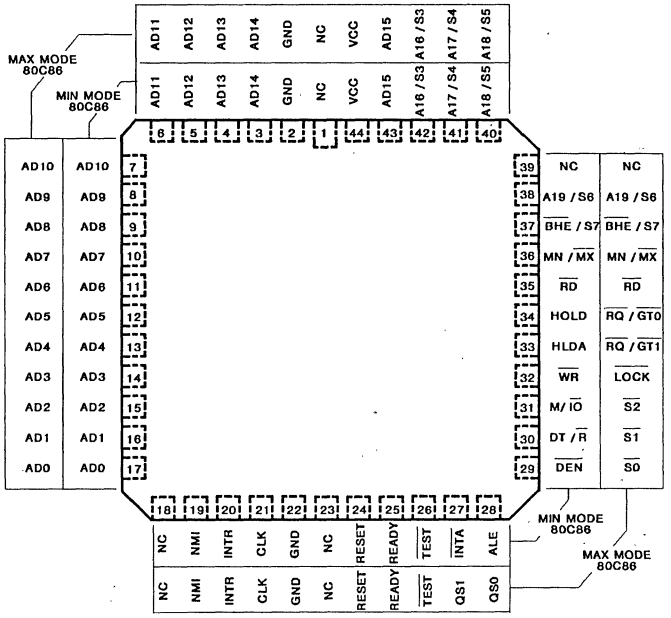
The Harris 80C86/883 high performance 16 bit CMOS CPU is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). Two modes of operation, MINimum for small systems and MAXimum for larger applications such as multi-processing, allow user configuration to achieve the highest performance level. Full TTL compatibility (with the exception of CLOCK) and industry standard operation allow use of existing NMOS 8086 hardware and software designs.

Pinouts

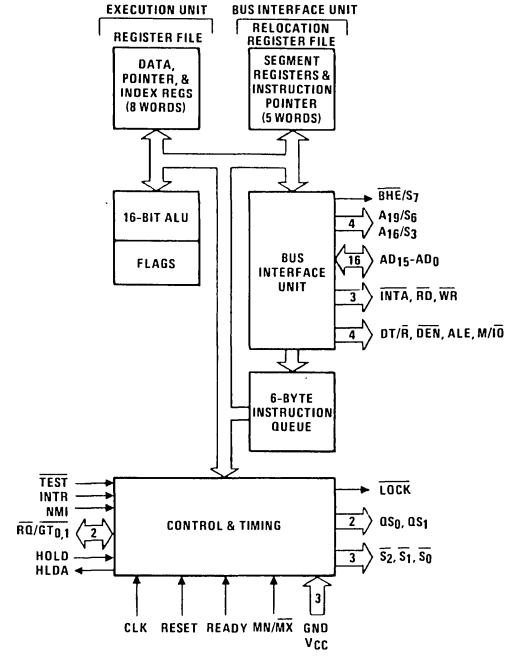
80C86/883 (CERAMIC DIP)
TOP VIEW

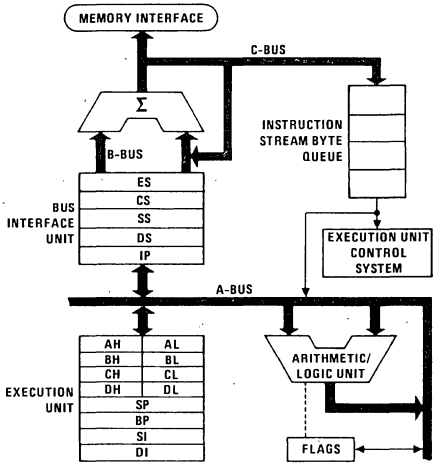


80C86/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram





Pin Description

The following pin function descriptions are for 80C86/883 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the 80C86/883 (without regard to additional bus buffers).

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
AD15-AD0	2-16, 39	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (T1) and data (T2, T3, TW, T4) bus. A0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D7-D0. It is LOW during T1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A0 to condition chip select functions (See $\overline{BHE}$). These lines are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence".
A19/S6 A18/S5 A17/S4 A16/S3	35-38	O	ADDRESS/STATUS: During T1, these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, TW, T4. S6 is always LOW. The status of the interrupt enable FLAG bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown. This information indicates which segment register is presently being used for data accessing. These lines are held at high impedance to the last valid logic level during local bus "hold acknowledge" or "grant sequence". S4 / S3 / CHARACTERISTICS 0 / 0 / Alternate Data 0 / 1 / Stack 1 / 0 / Code or None 1 / 1 / Data
$\overline{BHE}$/S7	34	O	BUS HIGH ENABLE/STATUS: During T1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D15-D8. Eight bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S7 status information is available during T2, T3 and T4. The signal is active LOW, and is held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence"; it is LOW during T1 for the first interrupt acknowledge cycle. $\overline{BHE}$ / A0 / CHARACTERISTICS 0 / 0 / Whole word 0 / 1 / Upper Byte from/to odd address 1 / 0 / Lower byte from/to even address 1 / 1 / None
$\overline{RD}$	32	O	READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the M/$\overline{IO}$ or $\overline{S2}$ pin. This signal is used to read devices which reside on the 80C86/883 local bus. $\overline{RD}$ is active LOW during T2, T3 and TW of any read cycle, and is guaranteed to remain HIGH in T2 until the 80C86/883 local bus has floated. This line is held at a high impedance logic one state during "hold acknowledge" or "grant sequence".
READY	22	I	READY: is the acknowledgement from the addressed memory or I/O device that will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 82C84A Clock Generator to form READY. This signal is active HIGH. The 80C86/883 READY input is not synchronized. Correct operation is not guaranteed if the Setup and Hold Times are not met.
INTR	18	I	INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.

Pin Description (Continued)

The following pin function descriptions are for 80C86/883 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the 80C86/883 (without regard to additional bus buffers).

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{TEST}$	23	I	TEST: input is examined by the "Wait" instruction. If the $\overline{TEST}$ input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NON-MASKABLE INTERRUPT: is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET: causes the processor to immediately terminate its present activity. The signal must transition LOW to HIGH and remain active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
VCC	40		VCC: +5V power supply pin. A 0.1 µF capacitor between pins 20 and 40 is recommended for decoupling.
GND	1, 20		GND: Ground. Note: both must be connected. A 0.1 µF capacitor between pins 1 and 20 is recommended for decoupling.
MN/$\overline{MX}$	33	I	MINIMUM/MAXIMUM: Indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin function descriptions are for the 80C86/883 in minimum mode (i.e. MN/$\overline{MX}$ = VCC). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described below.

MINIMUM MODE SYSTEM

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
M/$\overline{IO}$	28	O	STATUS LINE: logically equivalent to $\overline{S2}$ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (M = HIGH, IO = LOW). M/$\overline{IO}$ is held to a high impedance logic one during local bus "hold acknowledge".
$\overline{WR}$	29	O	WRITE: indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal. $\overline{WR}$ is active for T2, T3 and TW of any write cycle. It is active LOW, and is held to high impedance logic one during local bus "hold acknowledge".
$\overline{INTA}$	24	O	INTERRUPT ACKNOWLEDGE: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3 and TW of each interrupt acknowledge cycle. Note that $\overline{INTA}$ is never floated.
ALE	25	O	ADDRESS LATCH ENABLE: is provided by the processor to latch the address into the 82C82/82C83 address latch. It is a HIGH pulse active during clock LOW of T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	DATA TRANSMIT/RECEIVE: is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in maximum mode, and its timing is the same as for M/$\overline{IO}$ (T = HIGH, R = LOW). DT/$\overline{R}$ is held to a high impedance logic one during local bus "hold acknowledge".
$\overline{DEN}$	26	O	DATA ENABLE: provided as an output enable for a bus transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle it is active from the middle of T2 until the middle of T4, while for a write cycle it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ is held to a high impedance logic one during local bus "hold acknowledge".

Pin Description (Continued)

The following pin function descriptions are for the 80C86/883 in minimum mode (i.e. MN/$\overline{MX}$ = VCC). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described below.

MINIMUM MODE SYSTEM (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
HOLD HLDA	31, 30	I O	HOLD: indicates that another master is requesting a local bus "hold". To be a acknowledged, HOLD must be active HIGH. The processor receiving the "hold" will issue a "hold acknowledge" (HLDA) in the middle of a T4 or TI clock cycle. Simultaneously with the issuance of HLDA, the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

The following pin function descriptions are for the 80C86/883 system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described below.

MAXIMUM MODE SYSTEM

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	26 27 28	O O O	STATUS: is active during T4, T1 and T2 and is returned to the passive state (1, 1, 1) during T3 or during TW when READY is HIGH. This status is used by the 82C88 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$ or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or TW is used to indicate the end of a bus cycle. These signals are held at a high impedance logic one state during "grant sequence".
$\overline{RQ}/\overline{GT0}$ $\overline{RQ}/\overline{GT1}$	31, 30	I/O	REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bi-directional with $\overline{RQ}/\overline{GT0}$ having higher priority than $\overline{RQ}/\overline{GT1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up bus hold device so it may be left unconnected. The request/grant sequence is as follows (see $\overline{RQ}/\overline{GT}$ Sequence Timing) 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the 80C86/883 (pulse 1). 2. During a T4 or TI clock cycle, a pulse 1 CLK wide from the 80C86/883 to the requesting master (pulse 2) indicates that the 80C86/883 has allowed the local bus to float and that it will enter the "grant sequence" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "grant sequence". 3. A pulse 1 CLK wide from the requesting master indicates to the 80C86/883 (pulse 3) that the "hold" request is about to end and that the 80C86/883 can reclaim the local bus at the next CLK. The CPU then enters T4 (or TI if no bus cycles pending). Each Master-Master exchange of the local bus is a sequence of 3 pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active low.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

Pin Description (Continued)

The following pin function descriptions are for the 80C86/883 system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described below.

MAXIMUM MODE SYSTEM (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
			If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met: 1. Request occurs on or before T2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next cycle. 2. A memory cycle will start within three clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
$\overline{LOCK}$	29	O	LOCK: output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a high impedance logic one state during "grant sequence". In MAX mode, $\overline{LOCK}$ is automatically generated during T2 of the first $\overline{INTA}$ cycle and removed during T2 of the second $\overline{INTA}$ cycle.
QS1, QS0	24, 25	O	QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed. QS1 and QS0 provide status to allow external tracking of the internal 80C86/883 instruction queue. Note that QS1, QS0 never become high impedance.

QS1	QS0	
0	0	No Operation
0	1	First byte of op code from queue
1	0	Empty the Queue
1	1	Subsequent byte from queue

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	27.5°C/W	5.9°C/W
Ceramic LCC Package	62.2°C/W	8.6°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 620mW
Ceramic LCC Package 664mW
Gate Count ..... 9750 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage ..... +4.5V to +5.5V
80C86-2/883 ONLY ..... +4.75V to +5.25V

Operating Temperature Range ..... -55°C to +125°C

TABLE 1. 80C86/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested, 80C86/883: VCCL = 4.5V, VCCH = 5.5V, fmax = 5MHz;
80C86-2/883: VCCL = 4.75V, VCCH = 5.25V, fmax = 8MHz

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	VIH	VCC = VCCH, Note 2	1, 2, 3	-55°C≤T_A≤+125°C	2.2	-	V
Logical Zero Input Voltage	VIL	Note 2	1, 2, 3	-55°C≤T_A≤+125°C	-	0.8	V
CLK Logical One Input Voltage	VIHC	VCC = VCCH	1, 2, 3	-55°C≤T_A≤+125°C	VCC-0.8	-	V
CLK Logical Zero Input Voltage	VILC		1, 2, 3	-55°C≤T_A≤+125°C	-	0.8	V
Output HIGH Voltage	VOH	IOH = -2.5mA, Note 3 IOH = -100µA, Note 3	1, 2, 3 1, 2, 3	-55°C≤T_A≤+125°C	3.0 VCC-0.4	- -	V V
Output LOW Voltage	VOL	IOL = +2.5mA, Note 3	1, 2, 3	-55°C≤T_A≤+125°C	-	0.4	V
Input Leakage Current	II	VCC = VCCH, VIN = GND or VCC DIP Pins: 17-19, 21-23, 33	1, 2, 3	-55°C≤T_A≤+125°C	-1.0	+1.0	µA
Input Current Bus Hold High	IBHH	VIN = 3.0V, Note 4 VCC = VCCL & VCCH	1, 2, 3	-55°C≤T_A≤+125°C	-40	-400	µA
Input Current Bus Hold Low	IBHL	VIN = 0.8V, Note 5 VCC = VCCL & VCCH	1, 2, 3	-55°C≤T_A≤+125°C	40	400	µA
Output Leakage Current	IO	VCC = VCCH, VOUT = 0V, Note 6	1, 2, 3	-55°C≤T_A≤+125°C	-	-10	µA
Standby Power Supply Current	ICCSB	VCC = VCCH, Note 7	1, 2, 3	-55°C≤T_A≤+125°C	-	500	µA
Operating Power Supply Current	ICCOP	VCC = VCCH, f = fmax, VIN = VCC or GND, Outputs Open	1, 2, 3	55°C≤T_A≤+125°C	-	10	mA/MHz

NOTES: 1. All voltages referenced to device GND, VCC = VCCL unless otherwise specified.
2. MN/$\overline{MX}$ is a strap option and should be held to VCC or GND.
3. Interchanging of force and sense conditions is permitted.
4. IBHH should be measured after raising VIN to VCC and then lowering to valid input high level of 3.0V on the following pins: 2-16, 26-32, 34-39.
5. IBHL should be measured after lowering VIN to GND and then raising to valid input low level of 0.8V on the following pins: 2-16, 34-39.
6. IO should be measured by putting the pin in a high impedance state and then driving VOUT to GND on the following pins: 26-29, 32.
7. ICCSB tested during clock high time after HALT instruction execution. VIN = VCC or GND, VCC = VCCH, outputs unloaded.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. 80C86/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested, 80C86/883: VCCL = 4.5V, VCCH = 5.5V, 80C86-2/883: VCCL = 4.75V, VCCH = 5.25V

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	80C86-2/883		80C86/883		UNITS
					MIN	MAX	MIN	MAX	
MINIMUM COMPLEXITY SYSTEM TIMING									
CLK Cycle Period	(1)TCLCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	125	-	200	-	ns
CLK Low Time	(2)TCLCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	68	-	118	-	ns
CLK High Time	(3)TCHCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	44	-	69	-	ns
Data In Setup Time	(6)TDVCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	30	-	ns
Data In Hold Time	(7)TCLDX1		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	10	-	ns
READY Setup Time into 80C86/883	(10)TRYHCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	68	-	118	-	ns
READY Hold Time into 80C86/883	(11)TCHRYX		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	30	-	ns
READY Inactive to CLK	(12)TRYLCL	Note 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-8	-	-8	-	ns
HOLD Setup Time	(13)THVCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	35	-	ns
INTR, NMI, $\overline{TEST}$ Setup Time	(14)TINVCH	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	30	-	ns
Address Valid Delay	(17)TCLAV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	60	10	110	ns
Address Hold Time	(18)TCLAX		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	10	-	ns
ALE Width	(22)TLHLL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TCLCH -10	-	TCLCH -20	-	ns
ALE Active Delay	(23)TCLLH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	50	-	80	ns
ALE Inactive Delay	(24)TCHLL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	55	-	85	ns
Address Hold Time to ALE Inactive	(25)TLLAX		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TCHCL -10	-	TCHCL -10	-	ns
Data Valid Delay	(26)TCLDV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	60	10	110	ns
Control Active Delay 1	(29)TCVCTV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	70	10	110	ns
Control Active Delay 2	(30)TCHCTV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	60	10	110	ns
Control Inactive Delay	(31)TCVCTX		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	70	10	110	ns
Address Float to $\overline{RD}$ Active	(32)TAZRL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
$\overline{RD}$ Active Delay	(33)TCLRL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	100	10	165	ns
$\overline{RD}$ Inactive Delay	(34)TCLRH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	80	10	150	ns
$\overline{RD}$ Inactive to Next Address Active	(35)TRHAV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TCLCL -40	-	TCLCL -45	-	ns
HLDA Valid Delay	(36)TCLHAV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	100	10	160	ns
$\overline{RD}$ Width	(37)TRLRH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	2 TCLCL -50	-	2 TCLCL -75	-	ns
$\overline{WR}$ Width	(38)TWLWH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	2 TCLCL -40	-	2 TLCL -60	-	ns

NOTES: 1. VCC = VCCL, CL = 100pF, f = 1MHz
2. Applies only to T2 state (8ns into T3)
3. Setup requirement for asynchronous signal only to guarantee recognition at next clock.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. 80C86/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

Device Guaranteed and 100% Tested, 80C86/883: VCCL = 4.5V, VCCH = 5.5V, 80C86-2/883: VCCL = 4.75V, VCCH = 5.25V

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	80C86-2/883 MIN	80C86-2/883 MAX	80C86/883 MIN	80C86/883 MAX	UNITS
MINIMUM COMPLEXITY SYSTEM TIMING									
Address Valid to ALE Low	(39)TAVAL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TCLCH -40	-	TCLCH -60	-	ns
Output Rise Time	(40)TOLOH	From 0.8V to 2.0V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	15	-	20	ns
Output Fall Time	(41)TOHOL	From 2.0V to 0.8V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	15	-	20	ns

NOTES: 1. VCC = VCCL, CL = 100pF, f = 1MHz
2. Applies only to T2 state (8ns into T3)
3. Setup requirement for asynchronous signal only to guarantee recognition at next clock.

TABLE 3. 80C86/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

80C86/883: VCCL = 4.5V, VCCH = 5.5V, 80C86-2/883: VCCL = 4.75V, VCCH = 5.25V

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	80C86-2/883 MIN	80C86-2/883 MAX	80C86/883 MIN	80C86/883 MAX	UNITS
MINIMUM COMPLEXITY SYSTEM TIMING									
Input Capacitance	CIN	f = 1MHz, All measurements are referenced device GND	1	$T_A = +25^oC$	-	25	-	25	pF
Output Capacitance	COUT		1	$T_A = +25^oC$	-	25	-	25	pF
I/O Capacitance	CI/O		1	$T_A = +25^oC$	-	25	-	25	pF
CLK Rise Time	TCH1CH2 (4)	From 1.0V to 3.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	10	-	10	ns
CLK Fall Time	TCL2CL1 (5)	From 3.5V to 1.0V	1	$-55^oC \leq T_A \leq +125^oC$	-	10	-	10	ns
RDY Setup Time Into 82C84A	TR1VCL (8)	CL = 100pF, VCC = VCCL, f = 1MHz	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	35	-	35	-	ns
RDY Hold Time Into 82C84A	TCLR1X (9)	CL = 100pF, VCC = VCCL, f = 1MHz	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
Input Rise Time (Except CLK)	TILIH (15)	From 0.8V to 2.0V	1	$-55^oC \leq T_A \leq +125^oC$	-	15	-	15	ns
Input Fall Time (Except CLK)	TIHIL (16)	From 2.0V to 0.8V	1	$-55^oC \leq T_A \leq +125^oC$	-	15	-	15	ns
Address Float Delay	TCLAZ (19)	CL = 100pF, VCC = VCCL, f = 1MHz	1	$-55^oC \leq T_A \leq +125^oC$	TCLAX	50	TCLAX	80	ns
Status Float Delay	TCHSZ (20)		1	$-55^oC \leq T_A \leq +125^oC$	-	50	-	80	ns
Data Hold Time	TCLDX2 (27)		1	$-55^oC \leq T_A \leq +125^oC$	10	-	10	-	ns
Data Hold Time After $\overline{WR}$	TWHDX (28)		1	$-55^oC \leq T_A \leq +125^oC$	TCLCL -30	-	TCLCL -30	-	ns

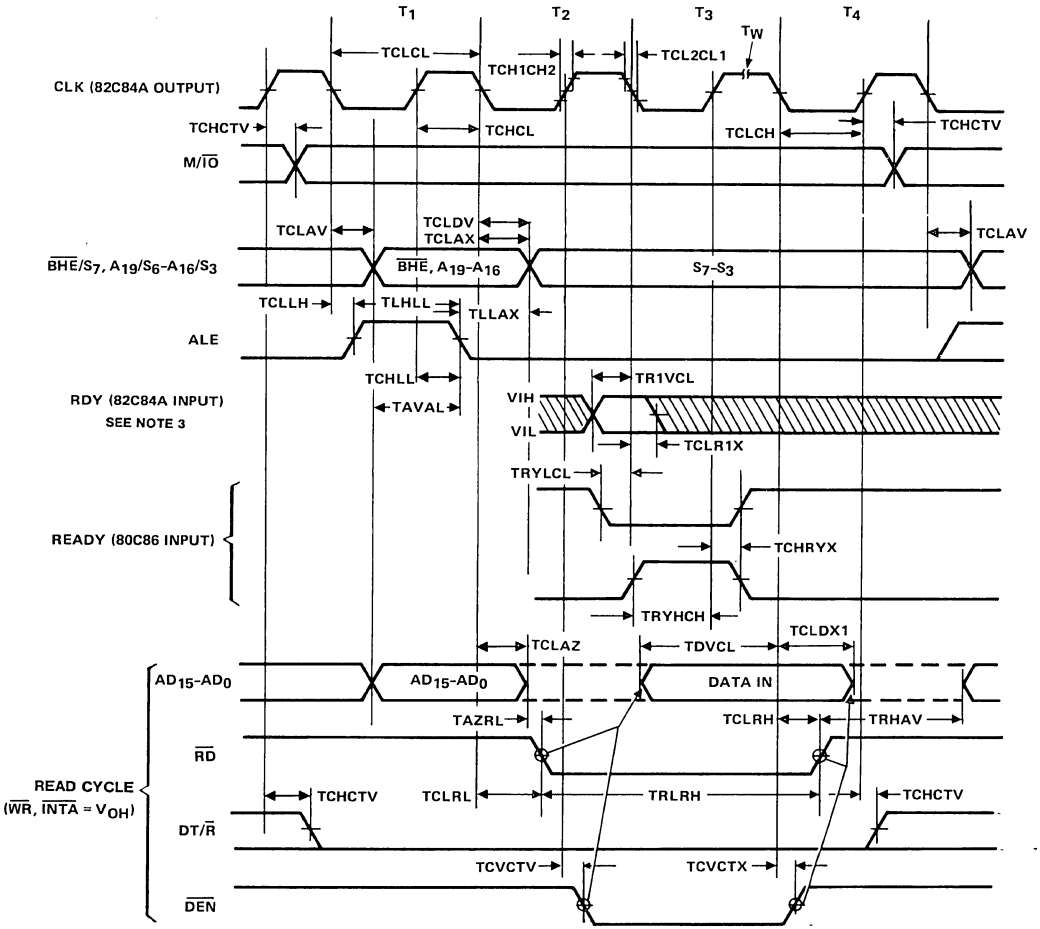
NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Signal at 82C84A shown for reference only.
3. Setup requirement for asynchronous signal only to guarantee recognition at next clock.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

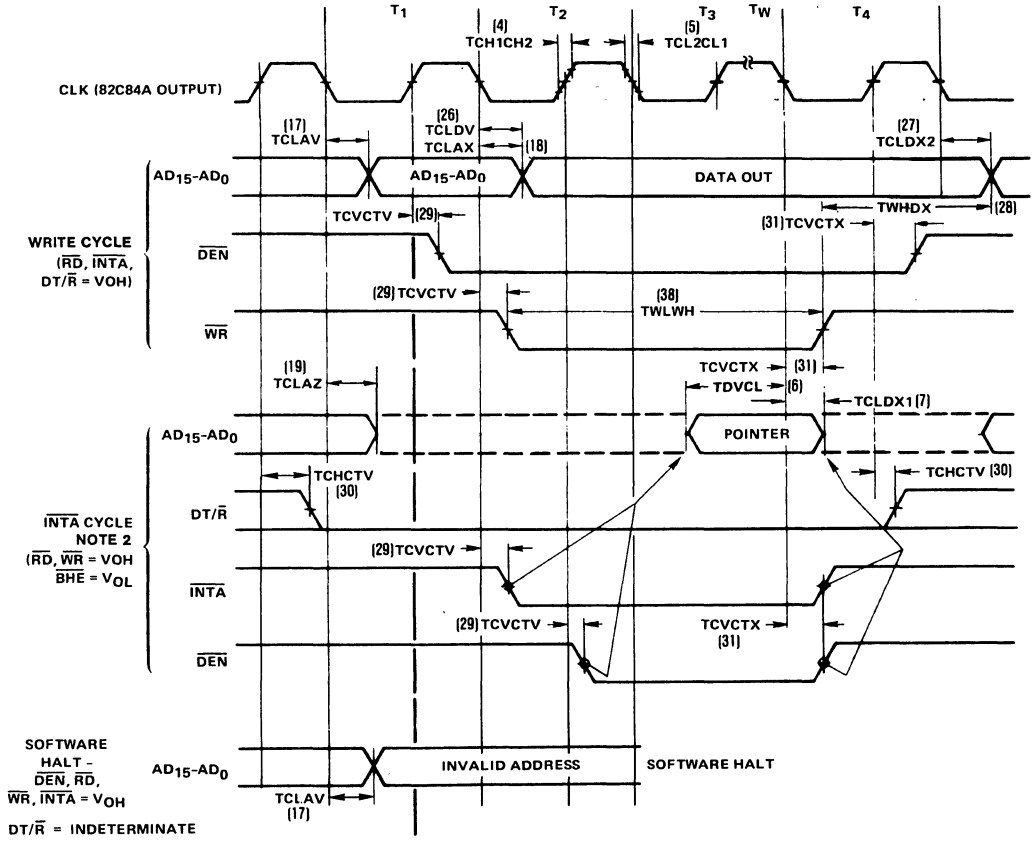
Waveforms



NOTES: 1. RDY is sampled near the end of T2, T3, Tw to determine if Tw machine states are to be inserted.
2. Two $\overline{\text{INTA}}$ cycles run back-to-back. The 80C86/883 local ADDR/DATA bus is floating during both $\overline{\text{INTA}}$ cycles. Control Signals are shown for the second $\overline{\text{INTA}}$ cycle.
3. Signals at 82C84A are shown for reference only.
4. All timing measurements are made at 1.5V unless otherwise noted..

Waveforms (Continued)

BUS TIMING - MINIMUM MODE SYSTEM (Continued)



NOTES: 1. RDY is sampled near the end of T2, T3, Tw to determine if Tw machine states are to be inserted.
2. Two $\overline{\text{INTA}}$ cycles run back-to-back. The 80C86/883 local ADDR/DATA bus is floating during both $\overline{\text{INTA}}$ cycles. Control Signals are shown for the second $\overline{\text{INTA}}$ cycle.
3. Signals at 82C84A are shown for reference only.
4. All timing measurements are made at 1.5V unless otherwise noted.

TABLE 2. 80C86/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested, 80C86/883: VCCL = 4.5V, VCCH = 5.5V, 80C86-2/883: VCCL = 4.75V, VCCH = 5.25V

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	80C86-2/883 MIN	80C86-2/883 MAX	80C86/883 MIN	80C86/883 MAX	UNITS
MAXIMUM MODE SYSTEM TIMING (USING 82C88 BUS CONTROLLER)									
CLK Cycle Period	(1)TCLCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	125	-	200	-	ns
CLK Low Time	(2)TCLCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	68	-	118	-	ns
CLK High Time	(3)TCHCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	44	-	69	-	ns
Data In Setup Time	(6)TDVCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	30	-	ns
Data In Hold Time	(7)TCLDX1		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	10	-	ns
READY Setup Time into 80C86/883	(10)TRYHCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	68	-	118	-	ns
READY Hold Time into 80C86/883	(11)TCHRYX		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	30	-	ns
READY Inactive to CLK	(12)TRYLCL	Note 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-8	-	-8	-	ns
Setup Time For Recognition (INTR, NMI, $\overline{TEST}$)	(13)TINVCH	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	30	-	ns
$\overline{RQ}/\overline{GT}$ Setup Delay	(14)TGVCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	30	-	ns
$\overline{RQ}$ Hold Time Into 80C86/883	(15)TCHGX	Note 4	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	TCHCL +10	40	TCHCL +10	ns
READY Active to Status Passive	(20)TRYHSH	Notes 2, 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	65	-	110	ns
Status Active Delay	(21)TCHSV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	60	10	110	ns
Status Inactive Delay	(22)TCLSH	Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	70	10	130	ns
Address Valid Delay	(23)TCLAV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	60	10	110	ns
Address Hold Time	(24)TCLAX		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	10	-	ns
Data Valid Delay	(33)TCLDV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	60	10	110	ns
Address Float to Read Active	(37)TAZRL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
$\overline{RD}$ Active Delay	(38)TCLRL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	100	10	165	ns
$\overline{RD}$ Inactive Delay	(39)TCLRH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	80	10	150	ns
$\overline{RD}$ Inactive to Next Address Active	(40)TRHAV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TCLCL -40	-	TCLCL -45	-	ns
$\overline{GT}$ Active Delay	(43)TCLGL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	50	10	85	ns
$\overline{GT}$ Inactive Delay	(44)TCLGH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	50	10	85	ns
$\overline{RD}$ Width	(45)TRLRH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	2 TCLCL -50	-	2 TCLCL -75	-	ns
Output Rise Time	(46)TOLOH	From 0.8V to 2.0V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	15	-	20	ns
Output Fall Time	(47)TOHOL	From 2.0V to 0.8V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	15	-	20	ns

NOTES: 1. VCC = VCCL, CL = 100pF, f = 1MHz
2. Applies only to T2 state (8ns into T3)
3. Setup requirement for asynchronous signal only to guarantee recognition at next clock.
4. The 80C86/883 actively pulls the $\overline{RQ}/\overline{GT}$ pin to a logic one on the following clock low time.
5. Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. 80C86/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

80C86/883: VCCL = 4.5V, VCCH = 5.5V, 80C86-2/883: VCCL = 4.75V, VCCH = 5.25V

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	80C86-2/883		80C86/883		UNITS
					MIN	MAX	MIN	MAX	
MAXIMUM MODE SYSTEM TIMING (USING 82C88 BUS CONTROLLER)									
Input Capacitance	CIN	f = 1MHz, All measurements are referenced device GND	1	T_A = +25°C	-	25	-	25	pF
Output Capacitance	COUT		1	T_A = +25°C	-	25	-	25	pF
I/O Capacitance	CI/O		1	T_A = +25°C	-	25	-	25	pF
CLK Rise Time	TCH1CH2 (4)	From 1.0V to 3.5V	1	-55°C≤T_A≤+125°C	-	10	-	10	ns
CLK Fall Time	TCL2CL1 (5)	From 3.5V to 1.0V	1	-55°C≤T_A≤+125°C	-	10	-	10	ns
RDY Setup Time Into 82C84A	TR1VCL (8)	CL = 100pF, VCC = VCCL, f = 1MHz	1, 2, 3	-55°C≤T_A≤+125°C	35	-	35	-	ns
RDY Hold Time Into 82C84A	TCLR1X (9)	CL = 100pF, VCC = VCCL, f = 1MHz	1, 2, 3	-55°C≤T_A≤+125°C	0	-	0	-	ns
Input Rise Time (Except CLK)	TILIH (16)	From 0.8V to 2.0V	1	-55°C≤T_A≤+125°C	-	15	-	15	ns
Input Fall Time (Except CLK)	TIHIL (17)	From 2.0V to 0.8V	1	-55°C≤T_A≤+125°C	-	15	-	15	ns
Command Active Delay	TCLML (18)	CL = 100pF, VCC = VCCL f = 1MHz	1, 2	-55°C≤T_A≤+125°C	5	35	5	35	ns
Command Inactive Delay	TCLMH (19)		1, 2	-55°C≤T_A≤+125°C	5	35	5	35	ns
Address Float Delay	TCLAZ (25)		1	-55°C≤T_A≤+125°C	TCLAX	50	TCLAX	80	ns
Status Float Delay	(26)TCHSZ		1	-55°C≤T_A≤+125°C	-	50	-	80	ns
Status Valid To ALE High	TSVLH (27)		1, 2	-55°C≤T_A≤+125°C	-	20	-	20	ns
Status Valid To MCE High	TSVMCH (28)		1, 2	-55°C≤T_A≤+125°C	-	30	-	30	ns
CLK Low To ALE Valid	TCLLH (29)		1, 2	-55°C≤T_A≤+125°C	-	20	-	20	ns
CLK Low To MCE High	TCLMCH (30)		1, 2	-55°C≤T_A≤+125°C	-	25	-	25	ns
ALE Inactive Delay	(31)TCHLL		1, 2	-55°C≤T_A≤+125°C	4	18	4	18	ns
MCE Inactive Delay	(32)TCLMCL		1, 2	-55°C≤T_A≤+125°C	-	15	-	15	ns
Data Hold Time	(34)TCLDX2		1	-55°C≤T_A≤+125°C	10	-	10	-	ns
Control Active Delay	TCVNV (35)		1, 2	-55°C≤T_A≤+125°C	5	45	5	45	ns
Control Inactive Delay	TCVNX (36)		1, 2	-55°C≤T_A≤+125°C	10	45	10	45	ns
Direction Control Active Delay	(41)TCHDTL		1, 2	-55°C≤T_A≤+125°C	-	50	-	50	ns
Direction Control Inactive Delay	(42)TCHDTH		1, 2	-55°C≤T_A≤+125°C	-	30	-	30	ns

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Signal at 82C84A or 82C88 shown for reference only.
3. Setup requirement for asynchronous signal only to guarantee recognition at next clock.

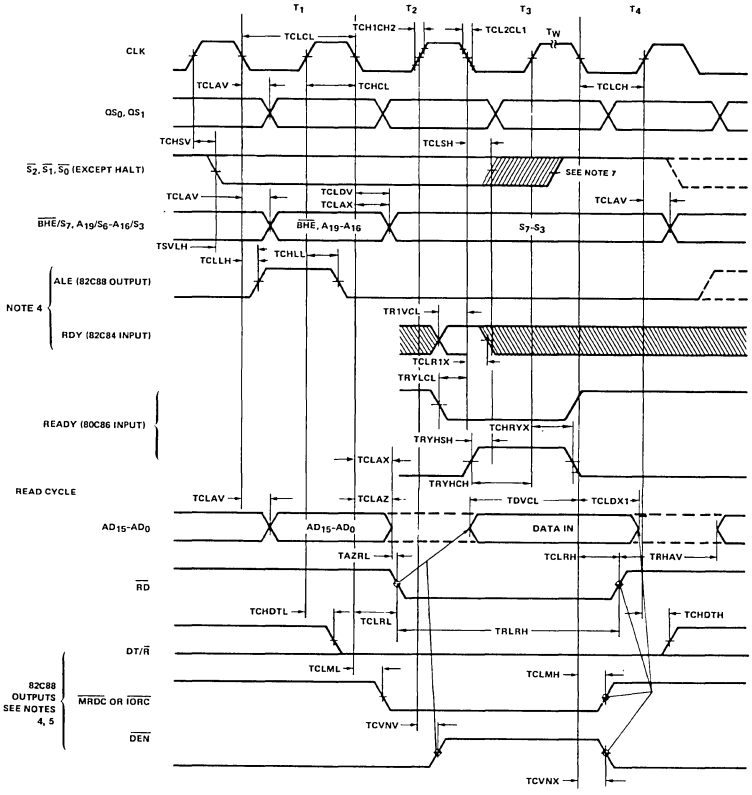
CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Waveforms

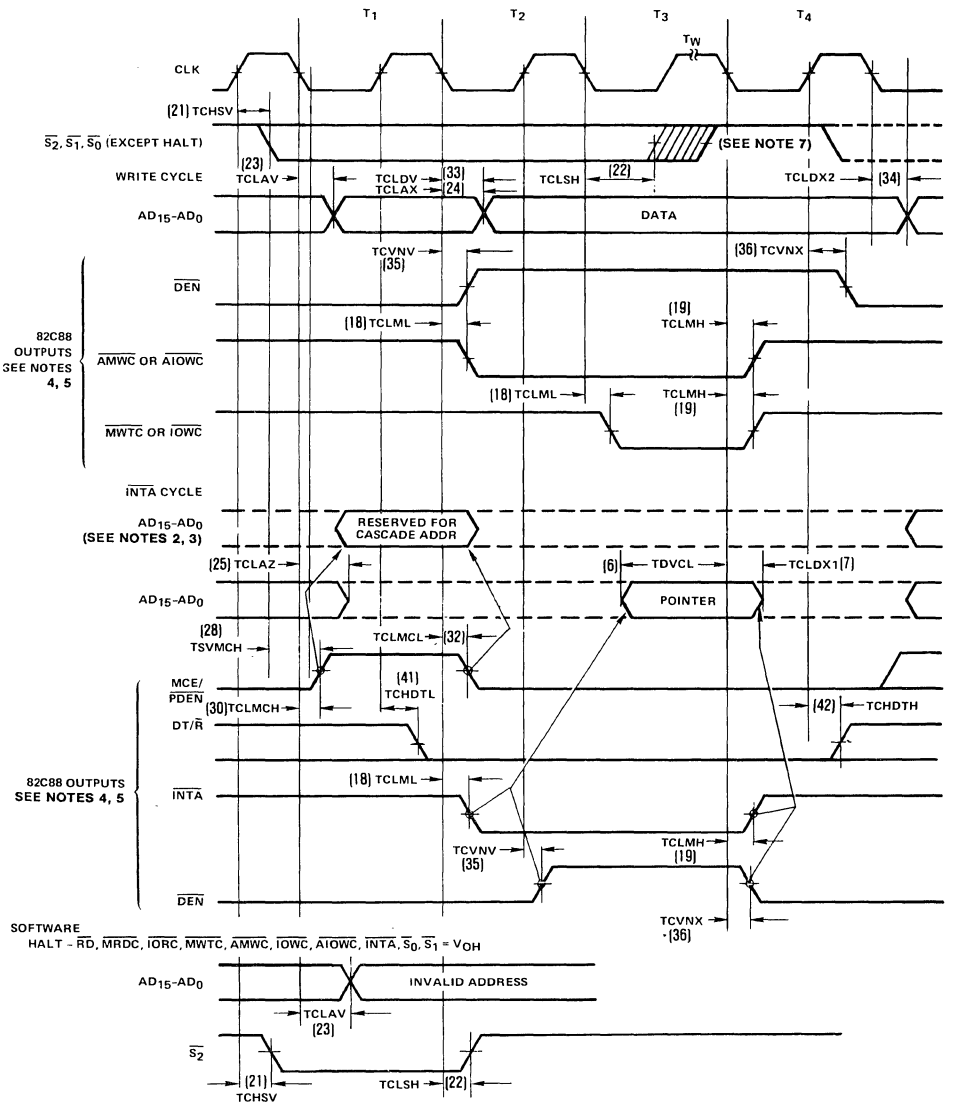
BUS TIMING - MAXIMUM MODE (USING 82C88)



NOTES:
1. RDY is sampled near the end of T2, T3, Tw to determine if Tw machine states are to be inserted.
2. Cascade address is valid between first and second $\overline{\text{INTA}}$ cycles.
3. Two $\overline{\text{INTA}}$ cycles run back-to-back. The 80C86/883 local ADDR/DATA bus is floating during both $\overline{\text{INTA}}$ cycles. Control for pointer address is shown for second $\overline{\text{INTA}}$ cycle.
4. Signals at 82C84A or 82C88 are shown for reference only.
5. The issuance of the 82C88 command and control signals ($\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$ and $\overline{\text{DEN}}$) lags the active high 82C88 CEN.
6. All timing measurements are made at 1.5V unless otherwise noted.
7. Status inactive in state just prior to T4.

Waveforms (Continued)

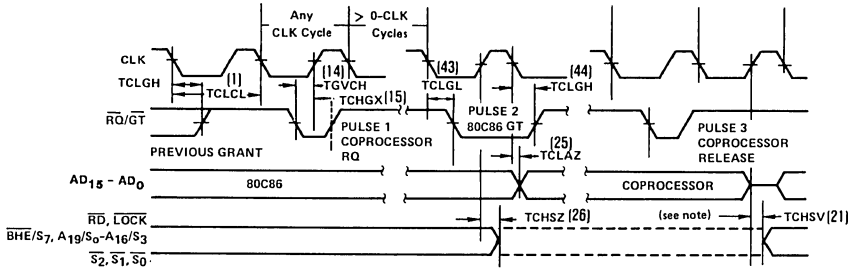
BUS TIMING - MAXIMUM MODE (USING 82C88) (Continued)



NOTES:
1. RDY is sampled near the end of T2, T3, Tw to determine if Tw machine states are to be inserted.
2. Cascade address is valid between first and second $\overline{INTA}$ cycles.
3. Two $\overline{INTA}$ cycles run back-to-back. The 80C86/883 local ADDR/DATA bus is floating during both $\overline{INTA}$ cycles. Control for pointer address is shown for second $\overline{INTA}$ cycle.
4. Signals at 82C84A or 82C83 are shown for reference only.
5. The issuance of the 82C88 command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ and $\overline{DEN}$) lags the active high 82C88 CEN.
6. All timing measurements are made at 1.5V unless otherwise noted.
7. Status inactive in state just prior to T4.

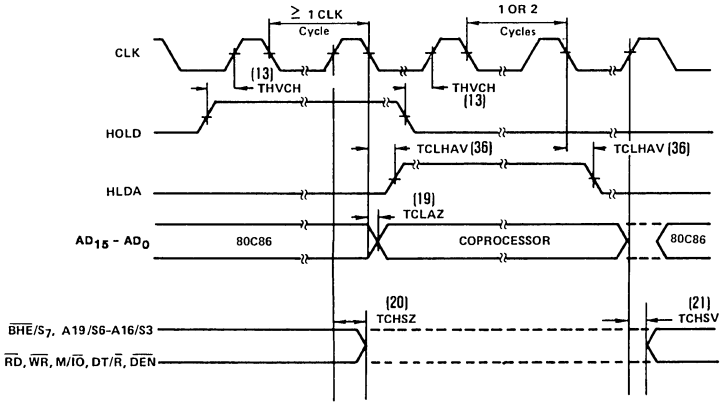
Waveforms (Continued)

REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)

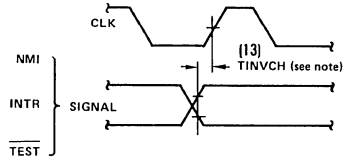


NOTE: The coprocessor may not drive the busses outside the region shown without risking contention

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)

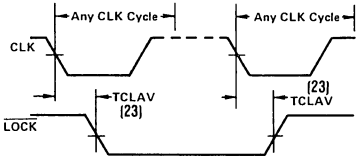


ASYNCHRONOUS SIGNAL RECOGNITION



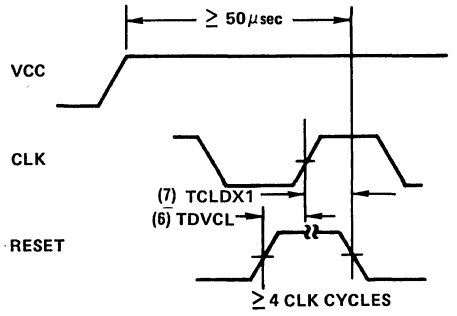
NOTE: Setup requirements for asynchronous signals only to guarantee recognition at next CLK

BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)

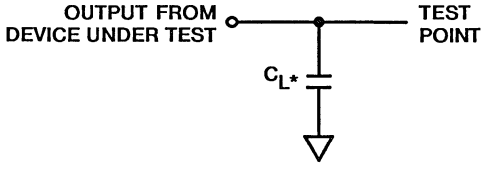


Waveforms (Continued)

RESET TIMING

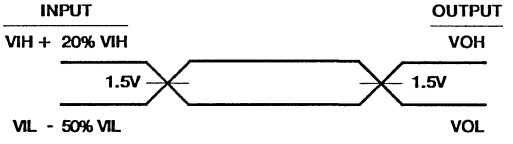


A.C. Test Circuit



*Includes stay and jig capacitance

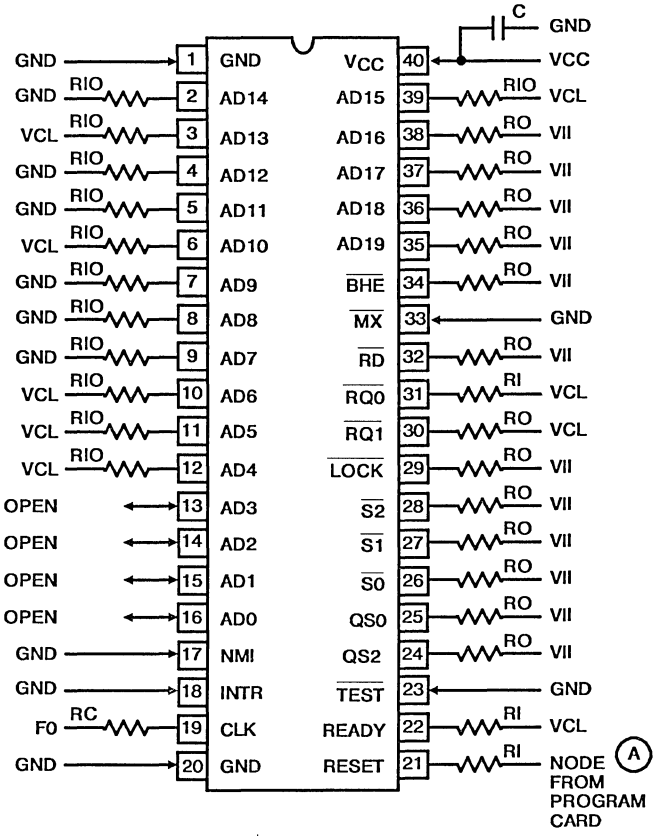
A.C. Testing Input, Output Waveform



A.C. Testing: All input signals (other than CLK) must switch between VILmax -50% VIL and VIHmin +20% VIH. CLK must switch between 0.4V and VCC -0.4. Input rise and fall times are driven at 1ns/V.

Burn-In Circuits

80C86/883 CERAMIC DIP



NOTES:

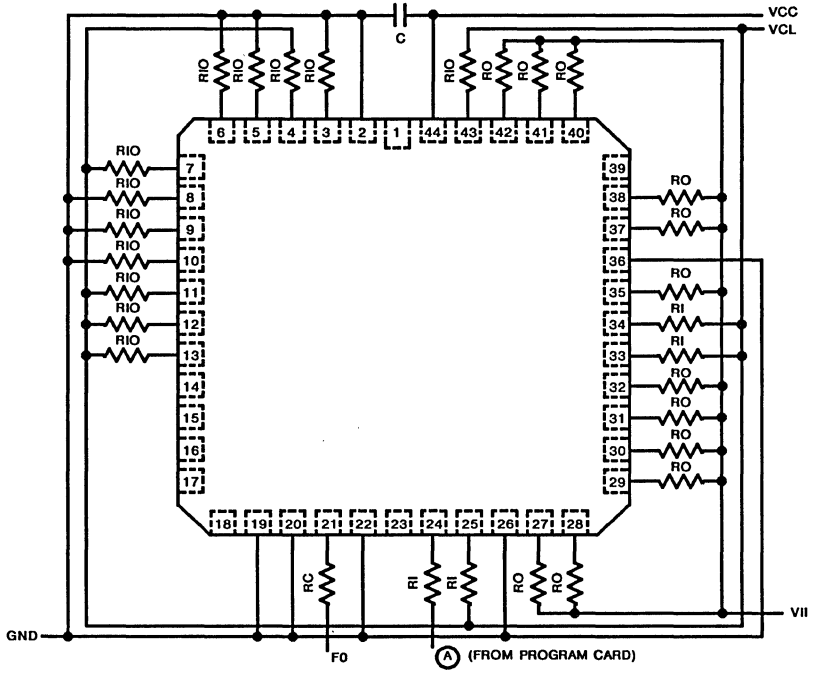
1. VCC = 5.5V ± 0.5V, GND = 0V
2. Input Voltage Limits:
   VIL (Maximum) = 0.4V
   VIH (Minimum) = 2.6V
3. VII is external supply set to 2.7V
4. VCL is generated on program card (VCC - 1.2V)
5. Pins 13 - 16 input sequenced instructions from internal hold devices.

COMPONENTS: (Per Card)

1. RI = 10kΩ ± 5%, 1.4W (4)
2. RO = 1.2kΩ ± 5%, 1/4W (12)
3. RIO = 2.7kΩ ± 5%, 1/4W (16)
4. RC = 1kΩ ± 5%, 1/4W (1)
5. C = 0.01μF (Minimum) (1)

Burn-In Circuits (Continued)

80C86/883 CERAMIC LCC



NOTES:

1. VCC = 5.5V ± 0.5V, GND = 0V
2. Input Voltage Limits:
   VIL (Maximum) = 0.4V
   VIH (Minimum) = 2.6V
3. VII is external supply set to 2.7V
4. VCL is generated on program card (VCC - 1.2V)

COMPONENTS: (Per Card)

1. RI = 10kΩ ± 5%, 1.4W (4)
2. RO = 1.2kΩ ± 5%, 1/4W (12)
3. RIO = 2.7kΩ ± 5%, 1/4W (16)
4. RC = 1kΩ ± 5%, 1/4W (1)
5. C = 0.01μF (Minimum) (1)

Metallization Topology

DIE DIMENSIONS:
249.2 x 290.9 x 19 ± 1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 2kÅ

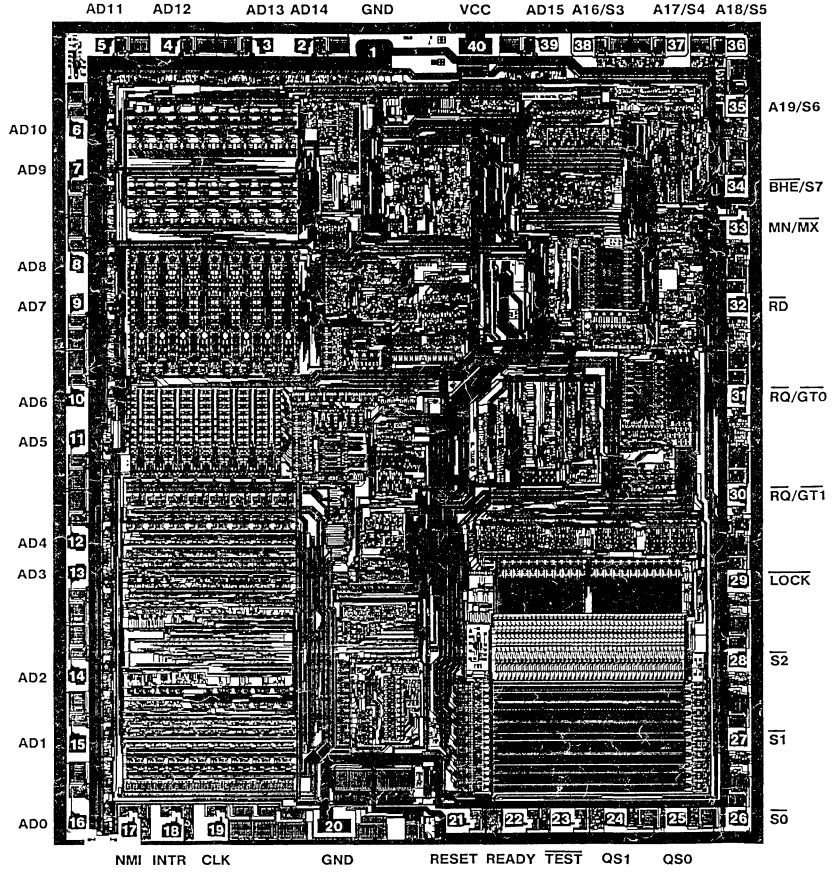
GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ ± 2kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.5 x 10^5 A/cm^2

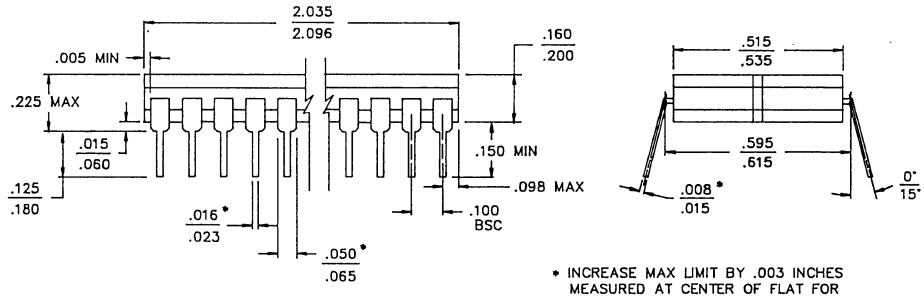
Metallization Mask Layout

80C86/883



Packaging†

40 PIN CERAMIC DIP

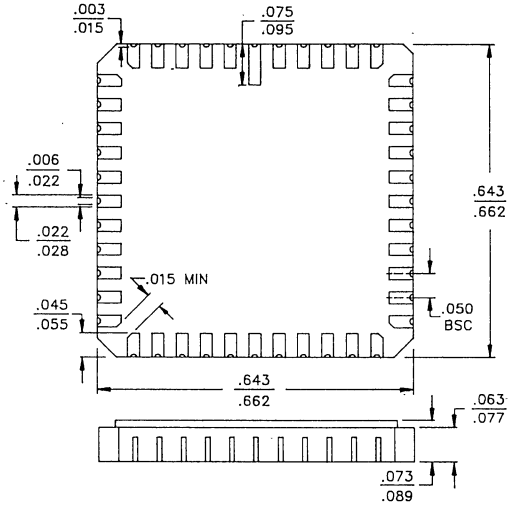


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-5

44 PAD CERAMIC LCC
BOTTOM VIEW



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-5

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Functional Description

Static Operation

All 80C86 circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS 80C86 can operate from DC to the specified upper frequency limit. The processor clock may be stopped in either state (HIGH/LOW) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The 80C86 can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

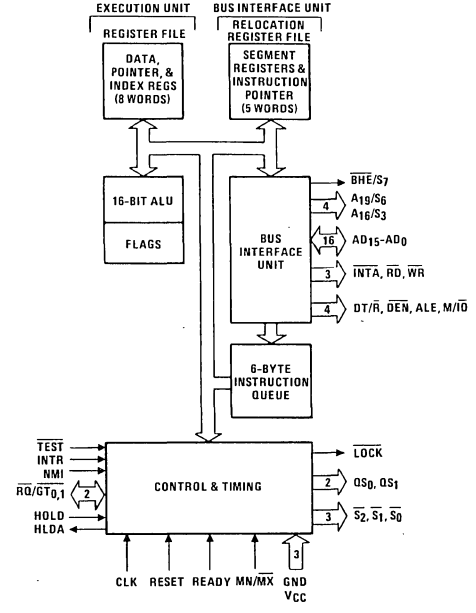
Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since 80C86 power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the 80C86 power requirement is the standby current, (500μA maximum).

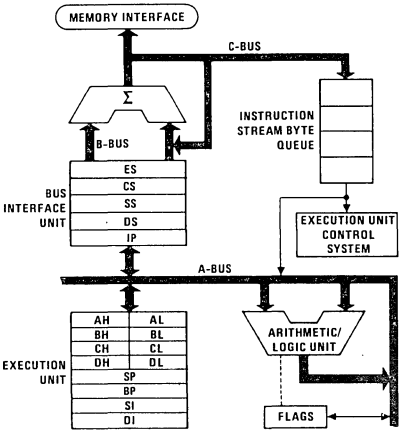
Internal Architecture

The internal functions of the 80C86 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the CPU functional diagram.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

Functional Diagram





DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead-time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

Memory Organization

The processor provides a 20 bit address to memory, which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 1).

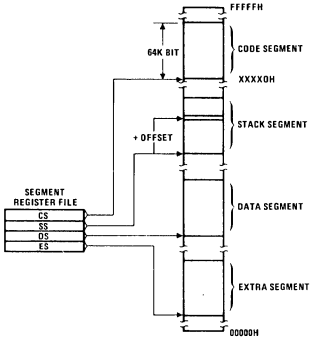


FIGURE 1. 80C86 MEMORY ORGANIZATION

TABLE A.

TYPE OF MEMORY REFERENCE	DEFAULT SEGMENT BASE	ALTERNATE SEGMENT BASE	OFFSET
Instruction Fetch	CS	None	IP
Stack Operation	SS	None	SP
Variable (except following)	DS	CS, ES, SS	Effective Address
String Source	DS	CS, ES, SS	SI
String Destination	ES	None	DI
BP Used As Base Register	SS	CS, DS, ES	Effective Address

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the specific rules of Table A. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster and more structured. (See Table A).

Word (16 bit) operands can be located on even or odd address boundaries and are thus not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two if it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. The performance penalty does not occur for instruction fetches; only word operands.

Physically, the memory is organized as a high bank (D15-D8) and a low bank (D7-D0) of 512K bytes addressed in parallel by the processor's address lines.

Byte data with even addresses is transferred on the D7-D0 bus lines while odd addressed byte data (A0 HIGH) is transferred on the D15-D8 bus lines. The processor provides two enable signals, $\overline{BHE}$ and A0, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor at the byte level as necessary.

In referencing word data, the BIU requires one or two memory cycles depending on whether the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

Certain locations in memory are reserved for specific CPU operations (See Figure 2). Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt service routines is accessed thru its own pair of 16-bit pointers - segment address pointer and offset address pointer. The first pointer, used as the offset address, is loaded into the IP and the second pointer, which designates the base address is loaded into the CS. At this point program control is transferred to the interrupt routine. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

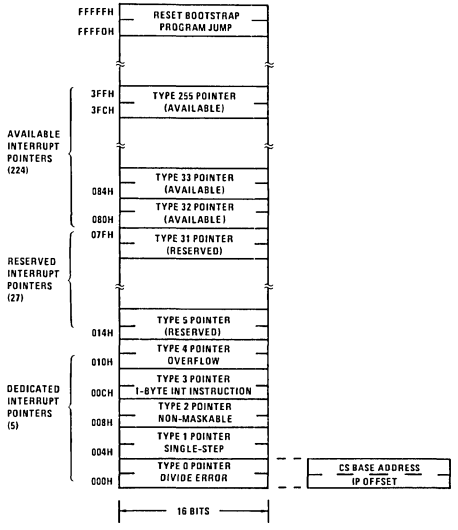


FIGURE 2. RESERVED MEMORY LOCATIONS

Minimum and Maximum Operation Modes

The requirements for supporting minimum and maximum 80C86 systems are sufficiently different that they cannot be met efficiently using 40 uniquely defined pins. Consequently, the 80C86 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the 80C86 defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{MX}$ pin is strapped to VCC, the 80C86 generates bus control signals itself on pins 24 through 31 and 34.

The minimum mode 80C86 can be used with either a multiplexed or demultiplexed bus. This architecture provides the 80C86 processing power in a highly integrated form.

The demultiplexed mode requires two 82C82 latches (for 64K addressability) or three 82C82 latches (for a full megabyte of addressing). An 82C86 or 82C87 transceiver can also be used if data bus buffering is required. (See Figure 6a.) The 80C86 provides $\overline{DEN}$ and DT/$\overline{R}$ to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the 82C88 bus controller (See Figure 6b). The 82C88 decodes status lines $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$, and provides the system with all bus control signals.

Moving the bus control to the 82C88 provides better source and sink current capability to the control lines, and frees the 80C86 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the 80C86 in maximum mode. These features allow coprocessors in local bus and remote bus configurations.

Bus Operation

The 80C86 has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40 lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of 82C82 address latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3 and T4 (see Figure 3). The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (TW) are inserted between T3 and T4. Each inserted wait state is the same duration as a CLK cycle. Periods can occur between 80C86 driven bus cycles. These are referred to as idle" states (TI) or inactive CLK cycles. The processor uses these cycles for internal housekeeping and processing.

During T1 of any bus cycle, the ALE (Address Latch Enable) signal is emitted (by either the processor or the 82C88 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to Table B.

TABLE B.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
0	0	0	Interrupt
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

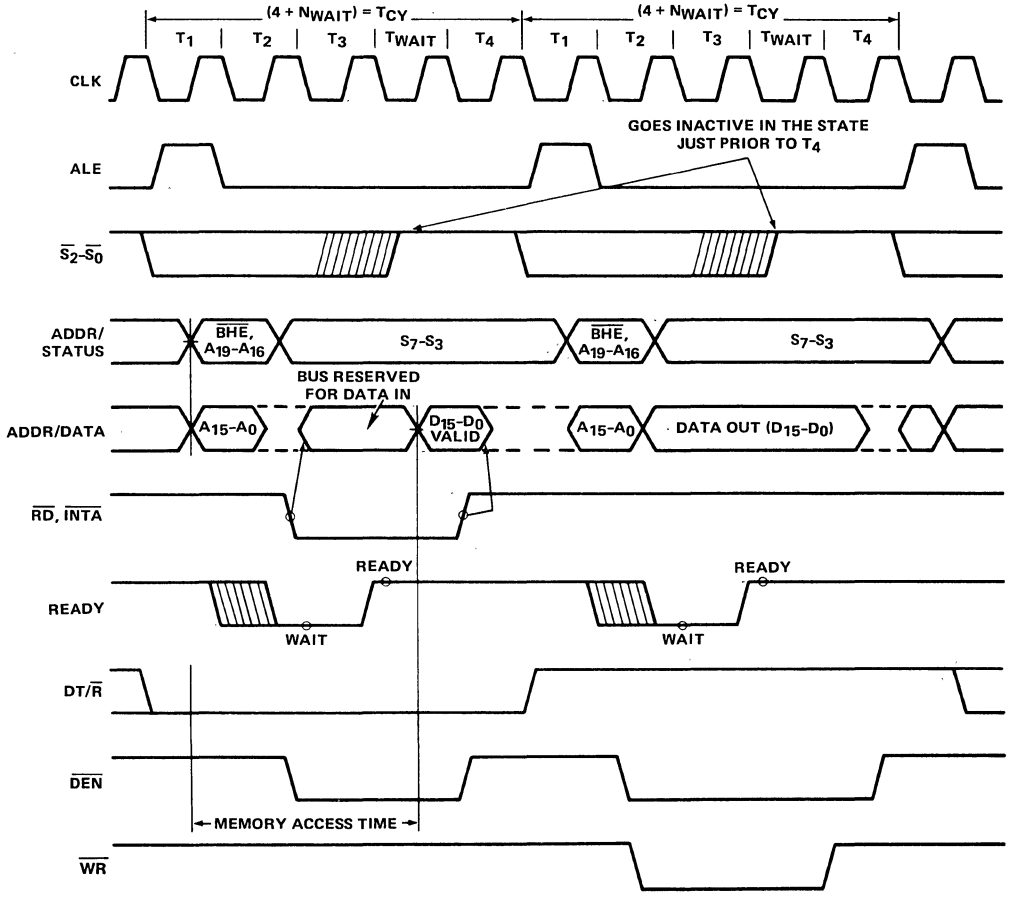


FIGURE 3. BASIC SYSTEM TIMING

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Status bits S3 through S7 are time multiplexed with high order address bits and the $\overline{BHE}$ signal, and are therefore valid during T2 through T4. S3 and S4 indicate which segment register (see Instruction Set Description) was used for this bus cycle in forming the address, according to Table C.

TABLE C.

S4	S3	CHARACTERISTICS
0	0	Alternate Data (extra segment)
0	1	Stack
1	0	Code or None
1	1	Data

S5 is a reflection of the PSW interrupt enable bit. S6 is always zero and S7 is a spare status bit.

I/O Addressing

In the 80C86, I/O operations can address up to a maximum of 64K I/O byte registers or 32K I/O word registers. The I/O address appears in the same format as the memory address on bus lines A15-A0. The address lines A19-A16 are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D7-D0 bus lines and odd addressed bytes on D15-D8. Care must be taken to ensure that each register within an 8 bit peripheral located on the lower portion of the bus be addressed as even.

External Interface

Processor RESET and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 80C86 RESET is required to be HIGH for greater than 4 CLK cycles. The 80C86 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval, the 80C86 operates normally beginning with the instruction in absolute location FFFF0H. (See Figure 2). The RESET input is internally synchronized to the processor clock. At initialization, the HIGH-to-LOW transition of RESET must occur no sooner than 50μs (or 4 CLK cycles, whichever is greater) after power-up, to allow complete initialization of the 80C86.

NMI will not be recognized prior to the second CLK cycle following the end of RESET. If NMI is asserted sooner than nine clock cycles after the end of RESET, the processor may execute one instruction before responding to the interrupt.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate need for pull-up/down resistors, "bus-hold" circuitry has been used on the 80C86 pins 2-16, 26-32 and 34-39. (See Figure 4a and 4b). These circuits will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). To overdrive the "bus hold" circuits, an external driver must be capable of supplying approximately 400μA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

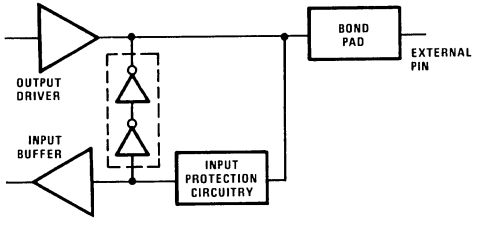


FIGURE 4A. BUS HOLD CIRCUITRY PIN 2-16, 34-39

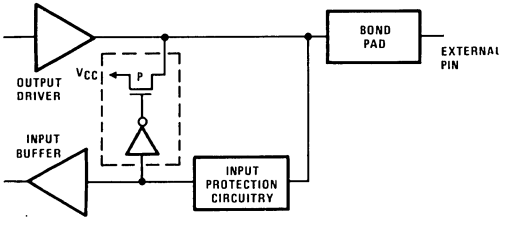


FIGURE 4B. BUS HOLD CIRCUITRY PIN 26-32

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set Description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH, which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8 bit type number during the interrupt acknowledge sequence, which is used to "vector" through the appropriate element to the new interrupt service program location. All flags and both the Code Segment and Instruction Pointer register are saved as part of the $\overline{\text{INTA}}$ sequence. These are restored upon execution of an Interrupt Return (IRET) instruction.

Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any positive transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during or after the servicing of NMI. Another positive edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The 80C86 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable flag (IF) status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block type instruction. INTR may be removed anytime after the falling edge of the first $\overline{\text{INTA}}$ signal. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored the enable bit will be zero unless specifically set by an instruction.

During the response sequence (Figure 5) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 80C86 emits the $\overline{\text{LOCK}}$ signal (Max mode only) from T2 of the first bus cycle until T2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is supplied to the 80C86 by the 82C59A Interupt Controller, which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector look-up table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

Halt

When a software "HALT" instruction is executed the processor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In maximum mode the processor issues appropriate HALT status on $\overline{\text{S2}}$, $\overline{\text{S1}}$, $\overline{\text{S0}}$

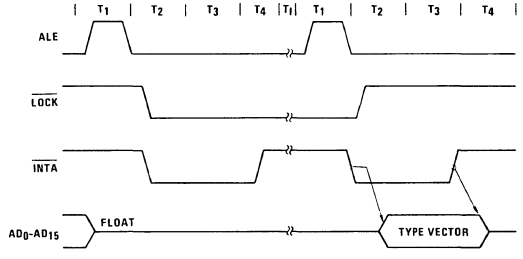


FIGURE 5. INTERRUPT ACKNOWLEDGE SEQUENCE

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

and the 82C88 bus controller issues one ALE. The 80C86 will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator at the end of the local bus hold. An NMI or interrupt request (when interrupts enabled) or RESET will force the 80C86 out of the "HALT" state.

Read/Modify/Write (Semaphore)

Operations Via $\overline{\text{Lock}}$

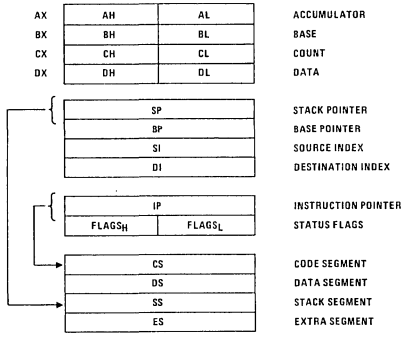
The $\overline{\text{LOCK}}$ status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This gives the processor the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. the $\overline{\text{LOCK}}$ signal is activated (forced LOW) in the clock cycle following decoding of the software "LOCK" prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While $\overline{\text{LOCK}}$ is active a request on a $\overline{\text{RQ}}/\overline{\text{GT}}$ pin will be recorded and then honored at the end of the $\overline{\text{LOCK}}$.

External Synchronization Via TEST

As an alternative to interrupts, the 80C86 provides a single software-testable input pin ($\overline{\text{TEST}}$). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the $\overline{\text{TEST}}$ input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the 80C86 three-states all output drivers while inputs and I/O pins are held at valid logic levels by internal bus-hold circuits. If interrupts are enabled, the 80C86 will recognize interrupts and process them when it regains control of the bus. The WAIT instruction is then refetched, and reexecuted.

TABLE D. 80C86 REGISTER MODEL



Basic System Timing

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 6A and 6B, respectively. In minimum mode, the MN/$\overline{\text{MX}}$ pin is strapped to VCC and the processor emits bus control signals (e.g. $\overline{\text{RD}}$, $\overline{\text{WR}}$, etc.) directly. In maximum mode, the MN/$\overline{\text{MX}}$ pin is strapped to GND and the processor emits coded status information which the 82C88 bus controller uses to generate MULTIBUS™ compatible bus control signals. Figure 3 shows the signal timing relationships.

System Timing - Minimum System

The read cycle begins in T1 with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the address/data bus (AD0-AD15) at this time, into the 82C82/82C83 latch. The $\overline{\text{BHE}}$ and A0 signals address the low, high or both bytes. From T1 to T4 the M/$\overline{\text{IO}}$ signal indicates a memory or I/O operation. At T2, the address is removed from the address/data bus and the bus is held at the last valid logic state by internal bus hold devices. The read control signal is also asserted at T2. The read ($\overline{\text{RD}}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again three-state its bus drivers. If a transceiver (82C86/82C87) is required to buffer the 80C86 local bus, signals DT/R and $\overline{\text{DEN}}$ are provided by the 80C86.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/$\overline{\text{IO}}$ signal is again asserted to indicate a memory or I/O write operation. In T2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T4. During T2, T3 and TW, the processor asserts the write control signal. The write ($\overline{\text{WR}}$) signal becomes active at the beginning of T2 as opposed to the read which is delayed somewhat into T2 to provide time for output drivers to become inactive.

The $\overline{\text{BHE}}$ and A0 signals are used to select the proper byte(s) of the memory/IO word to be read or written according to Table E.

TABLE E.

$\overline{\text{BHE}}$	A0	CHARACTERISTCS
0	0	Whole word
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D7-D0 bus lines and odd address bytes on D15-D8.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

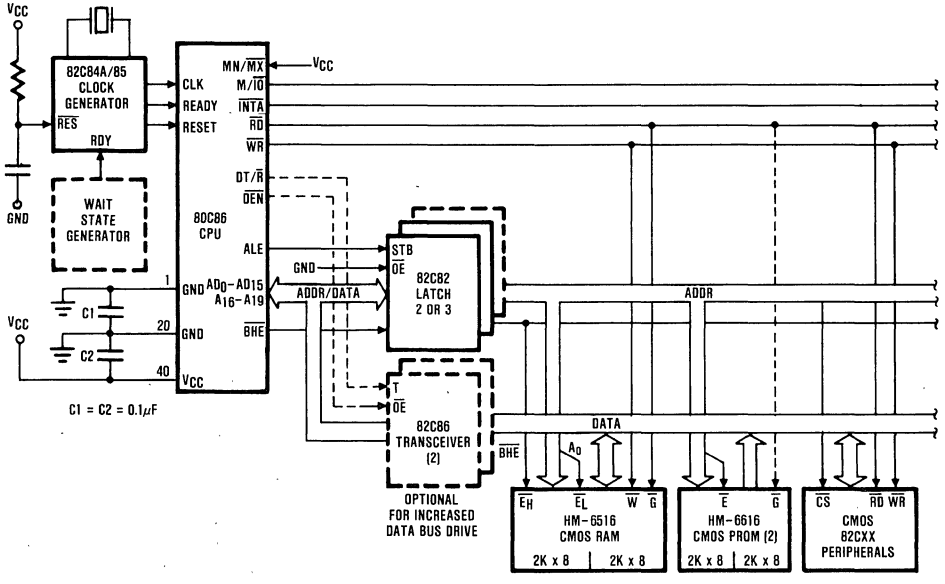


FIGURE 6A. MINIMUM MODE 80C86 TYPICAL CONFIGURATION

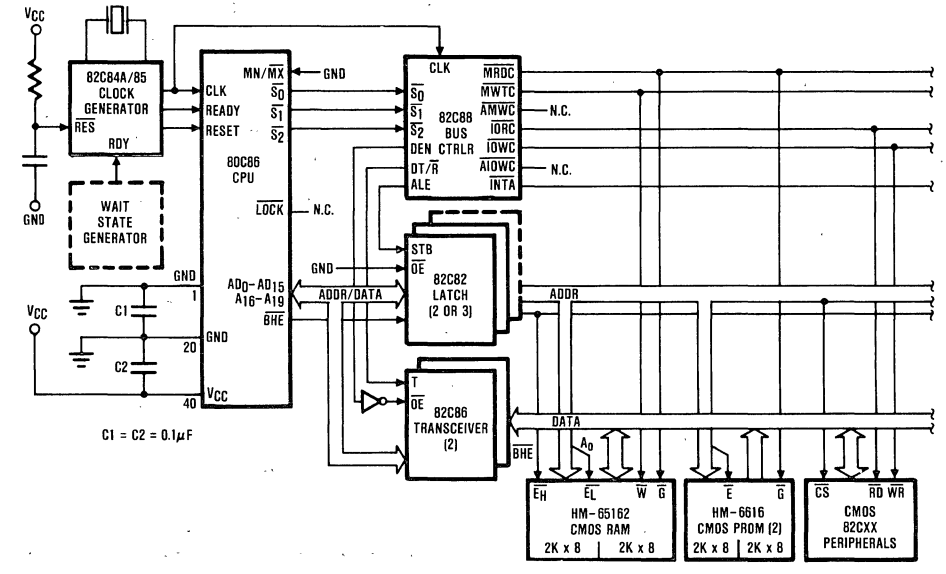


FIGURE 6B. MAXIMUM MODE 80C86 TYPICAL CONFIGURATION

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal ($\overline{INTA}$) is asserted in place of the read ($\overline{RD}$) signal and the address bus is held at the last valid logic state by internal bus hold devices. (See Figure 4). In the second of two successive $\overline{INTA}$ cycles a byte of information is read from the data bus (D7-D0) as supplied by the interrupt system logic (i.e. 82C59A Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interrupt vector lookup table, as described earlier.

Bus Timing - Medium Size Systems

For medium complexity systems the MN/$\overline{MX}$ pin is connected to GND and the 82C88 Bus Controller is added to the system as well as an 82C82/82C83 latch for latching the system address, and an 82C86/82C87 transceiver to allow for bus loading greater than the 80C86 is capable of handling. Signals ALE, $\overline{DEN}$, and DT/$\overline{R}$ are generated by the 82C88 instead of the processor in this configuration, although their timing remains relatively the same. The 80C86 status outputs ($\overline{S2}$, $\overline{S1}$ and $\overline{S0}$) provide type-of-cycle information and become 82C88 inputs. This bus cycle information specifies read (code, data or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 82C88 issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 82C88 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The 82C86/82C87 transceiver receives the usual T and $\overline{OE}$ inputs from the 82C88 DT/$\overline{R}$ and DEN signals.

The pointer into the interrupt vector table, which is passed during the second $\overline{INTA}$ cycle, can be derived from an 82C59A located on either the local bus or the system bus. If the master 82C59A Priority Interrupt Controller is positioned on the local bus, the 82C86/82C87 transceiver must be disabled when reading from the master 82C59A during the interrupt acknowledge sequence and software "poll".

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

INSTRUCTION SET SUMMARY

Mnemonic and Description	Instruction Code			
DATA TRANSFER				
MOV = Move:	**76543210**	**76543210**	**76543210**	**76543210**
Register/Memory to/from Register	100010dw	mod reg r/m		
Immediate to Register/Memory	1100011w	mod 000 r/m	data	data if w 1
Immediate to Register	1011w reg	data	data if w 1	
Memory to Accumulator	1010000w	add-low	addr-high	
Accumulator to Memory	1010001w	addr-low	addr-high	
Register/Memory to Segment Register**	10001110	mod 0 reg r/m		
Segment Register to Register/Memory	10001100	mod 0 reg r/m		
PUSH = Push:				
Register/Memory	11111111	mod 1 1 0 r/m		
Register	01010 reg			
Segment Register	000 reg 110			
POP = Pop:				
Register/Memory	10001111	mod 000 r/m		
Register	01011 reg			
Segment Register	000 reg 111			
XCHG = Exchange:				
Register/Memory with Register	1000011w	mod reg r/m		
Register with Accumulator	10010 reg			
IN = Input from:				
Fixed Port	1110010w	port		
Variable Port	1110110w			
OUT = Output to:				
Fixed Port	1110011w	port		
Variable Port	1110111w			
XLAT = Translate Byte to AL	11010111			
LEA = Load EA to Register	10001101	mod reg r/m		
LDS = Load Pointer to DS	11000101	mod reg r/m		
LES = Load Pointer to ES	11000100	mod reg r/m		
LAHF = Load AH with Flags	10011111			
SAHF = Store AH into Flags	10011110			
PUSHF = Push Flags	10011100			
POPF = Pop Flags	10011101			

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

INSTRUCTION SET SUMMARY (Continued)

Mnemonic and Description	Instruction Code			
ARITHMETIC	76543210	76543210	76543210	76543210
ADD = Add:				
Reg./Memory with Register to Either	000000dw	mod reg r/m		
Immediate to Register/Memory	100000sw	mod 000 r/m	data	data if s:w = 01
Immediate to Accumulator	0000010w	data	data if w = 1	
ADC = Add with Carry:				
Reg./Memory with Register to Either	000100dw	mod reg r/m		
Immediate to Register/Memory	100000sw	mod 010 r/m	data	data if s:w = 01
Immediate to Accumulator	0001010w	data	data if w = 1	
INC = Increment:				
Register/Memory	1111111w	mod 000 r/m		
Register	01000reg			
AAA = ASCII Adjust for Add	00110111			
DAA = Decimal Adjust for Add	00100111			
SUB = Subtract:				
Reg./Memory and Register to Either	001010dw	mod reg r/m		
Immediate from Register/Memory	100000sw	mod 101 r/m	data	data if s:w = 01
Immediate from Accumulator	0010110w	data	data if w = 1	
SBB = Subtract with Borrow				
Reg./Memory and Register to Either	000110dw	mod reg r/m		
Immediate from Register/Memory	100000sw	mod 011 r/m	data	data if s:w = 01
Immediate from Accumulator	0001110w	data	data if w = 1	
DEC = Decrement:				
Register/Memory	1111111w	mod 001 r/m		
Register	01001 reg			
NEG = Change Sign	1111011w	mod 011 r/m		
CMP = Compare:				
Register/Memory and Register	001110dw	mod reg r/m		
Immediate with Register/Memory	100000sw	mod 111 r/m	data	data if s:w = 01
Immediate with Accumulator	0011110w	data	data if w = 1	
AAS = ASCII Adjust for Subtract	00111111			
DAS = Decimal Adjust for Subtract	00101111			
MUL = Multiply (Unsigned)	1111011w	mod 100 r/m		
IMUL = Integer Multiply (Signed)	1111011w	mod 101 r/m		
AAM = ASCII Adjust for Multiply	11010100	00001010		
DIV = Divide (Unsigned)	1111011w	mod 110 r/m		
IDIV = Integer Divide (Signed)	1111011w	mod 111 r/m		
AAD = ASCII Adjust for Divide	11010101	00001010		
CBW = Convert Byte to Word	10011000			
CWD = Convert Word to Double Word	10011001			

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

INSTRUCTION SET SUMMARY (Continued)

Mnemonic and Description	Instruction Code			
LOGIC	76543210	76543210	76543210	76543210
NOT = Invert	1111011w	mod 0 1 0 r/m		
SHL/SAL = Shift Logical/Arithmetic Left	110100vw	mod 1 0 0 r/m		
SHR = Shift Logical Right	110100vw	mod 1 0 1 r/m		
SAR = Shift Arithmetic Right	110100vw	mod 1 1 1 r/m		
ROL = Rotate Left	110100vw	mod 0 0 0 r/m		
ROR = Rotate Right	110100vw	mod 0 0 1 r/m		
RCL = Rotate Through Carry Flag Left	110100vw	mod 0 1 0 r/m		
RCR = Rotate Through Carry Right	110100vw	mod 0 1 1 r/m		
AND = **And:**				
Reg./Memory and Register to Either	001000dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod 1 0 0 r/m	data	data if w = 1
Immediate to Accumulator	0010010w	data	data if w = 1	
TEST = **And Function to Flags, No Result:**				
Register/Memory and Register	1000010w	mod reg r/m		
Immediate Data and Register/Memory	1111011w	mod 0 0 0 r/m	data	data if w = 1
Immediate Data and Accumulator	1010100w	data	data if w = 1	
OR = **Or:**				
Reg./Memory and Register to Either	000010dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod 0 0 1 r/m	data	data if w = 1
Immediate to Accumulator	0000110w	data	data if w = 1	
XOR = **Exclusive or:**				
Reg./Memory and Register to Either	001100dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod 1 1 0 r/m	data	data if w = 1
Immediate to Accumulator	0011010w	data	data if w = 1	
STRING MANIPULATION				
REP = Repeat	1111001z			
MOVS = Move Byte/Word	1010010w			
CMPS = Compare Byte/Word	1010011w			
SCAS = Scan Byte/Word	1010111w			
LODS = Load Byte/Wd to AL/AX	1010110w			
STOS = Stor Byte/Wd from AL/A	1010101w			
CONTROL TRANSFER				
CALL = **Call:**				
Direct Within Segment	11101000	disp-low	disp-high	
Indirect Within Segment	11111111	mod 0 1 0 r/m		
Direct Intersegment	10011010	offset-low	offset-high	
		seg-low	seg-high	
Indirect Intersegment	11111111	mod 0 1 1 r/m		

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

INSTRUCTION SET SUMMARY (Continued)

Mnemonic and Description	Instruction Code		
JMP = Unconditional Jump:	76543210	76543210	76543210
Direct Within Segment	11101001	disp-low	disp-high
Direct Within Segment-Short	11101011	disp	
Indirect Within Segment	11111111	mod 100 r/m	
Direct Intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect Intersegment	11111111	mod 101 r/m	
RET = Return from CALL:			
Within Segment	11000011		
Within Seg Adding Immed to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment Adding Immediate to SP	11001010	data-low	data-high
JE/JZ = Jump on Equal/Zero	01110100	disp	
JL/JNGE = Jump on Less/Not Greater or Equal	01111100	disp	
JLE/JNG = Jump on Less or Equal/ Not Greater	01111110	disp	
JB/JNAE = Jump on Below/Not Above or Equal	01110010	disp	
JBE/JNA = Jump on Below or Equal/ Not Above	01110110	disp	
JP/JPE = Jump on Parity/Parity Even	01111010	disp	
JO = Jump on Overflow	01110000	disp	
JS = Jump on Sign	01111000	disp	
JNE/JNZ = Jump on Not Equal/Not Zero	01110101	disp	
JNL/JGE = Jump on Not Less/Greater or Equal	01111101	disp	
JNLE/JG = Jump on Not Less or Equal/ Greater	01111111	disp	
JNB/JAE = Jump on Not Below/Above or Equal	01110011	disp	
JNBE/JA = Jump on Not Below or Equal/Above	01110111	disp	
JNP/JPO = Jump on Not Par/Par Odd	01111011	disp	
JNO = Jump on Not Overflow	01110001	disp	
JNS = Jump on Not Sign	01111001	disp	
LOOP = Loop CX Times	11100010	disp	
LOOPZ/LOOPE = Loop While Zero/Equal	11100001	disp	
LOOPNZ/LOOPNE = Loop While Not Zero/Equal	11100000	disp	
JCXZ = Jump on CX Zero	11100011	disp	
INT = Interrupt			
Type Specified	11001101	type	
Type 3	11001100		
INTO = Interrupt on Overflow	11001110		
IRET = Interrupt Return	11001111		

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

INSTRUCTION SET SUMMARY (Continued)

Mnemonic and Description	Instruction Code	
	76543210	76543210
PROCESSOR CONTROL		
CLC = Clear Carry	11111000	
CMC = Complement Carry	11110101	
STC = Set Carry	11111001	
CLD = Clear Direction	11111100	
STD = Set Direction	11111101	
CLI = Clear Interrupt	11111010	
STI = Set Interrupt	11111011	
HLT = Halt	11110100	
WAIT = Wait	10011011	
ESC = Escape (to External Device)	11011xxx	mod x x x r/m
LOCK = Bus Lock Prefix	11110000	

NOTES:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction
if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16 bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)
*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.
**MOV CS, REG/MEMORY not allowed.
if s:w = 01 then 16 bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:
FLAGS =
X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Compatible with NMOS 8088
- Direct Software Compatibility with 80C86, 8086, 8088
- 8 Bit Data Bus Interface; 16 Bit Internal Architecture
- 5MHz Operation 80C88/883
- 8MHz Operation 80C88-2/883
- Low Power Operation
  - ICCSB ..... 500µA Maximum
  - ICCOP ..... 10mA/MHz Maximum
- 1 Megabyte of Direct Memory Addressing Capability
- 24 Operand Addressing Modes
- Bit, Byte, Word, and Block Move Operations
- 8 and 16 Bit Signed/Unsigned Arithmetic
- Bus-Hold Circuitry Eliminates Pull-up Resistors
- Military Operating Temperature ... -55°C to +125°C Range

Description

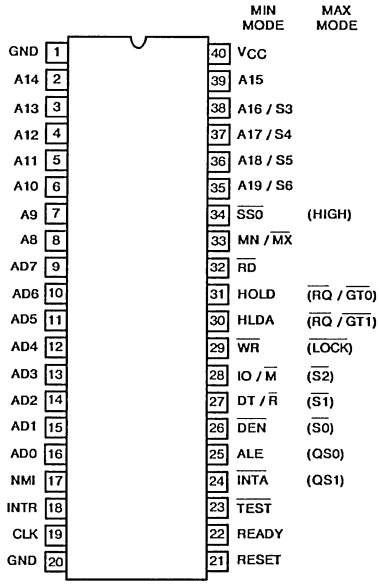
The Harris 80C88/883 high performance 8/16-bit CMOS CPU is manufactured using a self-alligned silicon gate CMOS process (Scaled SAJI IV). Two modes of operation, MINimum for small systems and MAXimum for larger applications such as multiprocessing, allow user configuration to achieve the highest performance level.

Full TTL compatibility (with the exception of CLOCK) and industry-standard operation allow use of existing NMOS 8088 hardware and Harris CMOS peripherals.

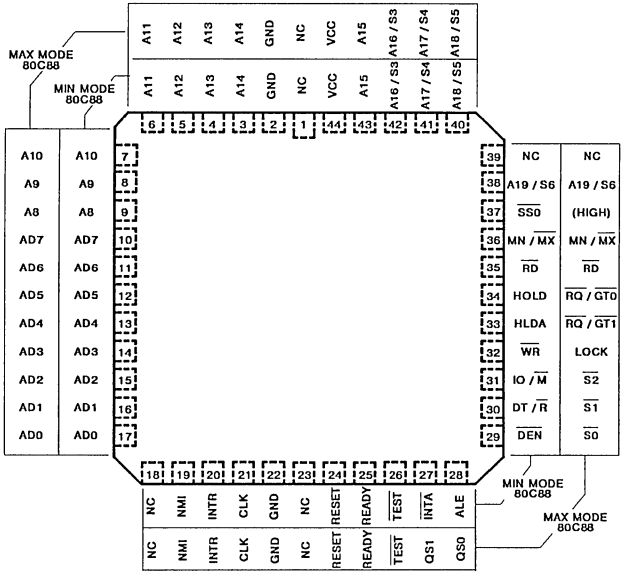
Complete software compatibility with the 80C86, 8086, and 8088 microprocessors allows use of existing software in new designs.

Pinouts

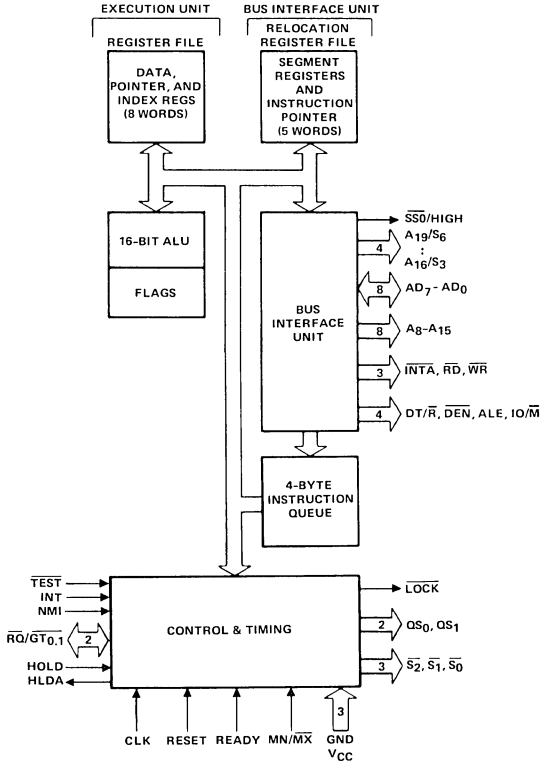
80C88/883 (CERAMIC DIP)
TOP VIEW

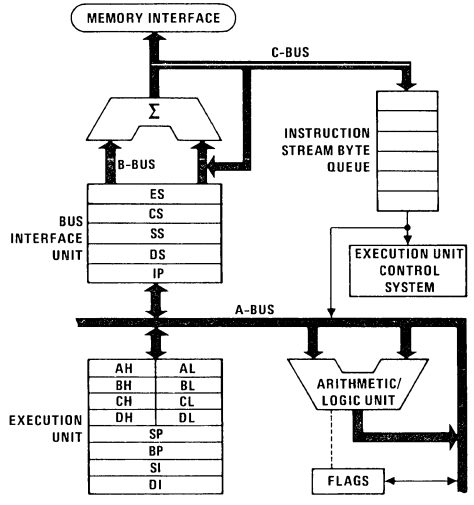


80C88/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram





Pin Description

The following pin function descriptions are for 80C88/883 systems in either minimum or maximum mode. The "local bus" in these descriptions is the direct multiplexed bus interface connection to the 80C88/883 (without regard to additional bus buffers).

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
AD7-AD0	9-16	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (T1) and data (T2, T3, Tw and T4) bus. These lines are active HIGH and are held at high impedance to the last valid level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence".
A15-A8	2-8, 39	O	ADDRESS BUS: These lines provide address bits 8 through 15 for the entire bus cycle (T1-T4). These lines do not have to be latched by ALE to remain valid. A15-A8 are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence".
A19/S6, A18/S5, A17/S4 A16/S3	35 36 37 38	O O O O	ADDRESS/STATUS: During T1, These are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, Tw and T4. S6 is always LOW. The status of the interrupt enable flag bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown. This information indicates which segment register is presently being used for data accessing. These lines are held at high impedance to the last valid logic level during local bus "hold acknowledge" or "grant sequence".
$\overline{RD}$	32	O	READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/$\overline{M}$ pin or $\overline{S2}$. This signal is used to read devices which reside on the 80C88/883 local bus. $\overline{RD}$ is active LOW during T2, T3 and Tw of any read cycle, and is guaranteed to remain HIGH in T2 until the 80C88/883 local bus has floated. This line is held at a high impedance logic one state during "hold acknowledge" or "grant sequence".
READY	22	I	READY: is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 82C84A clock generator to form READY. This signal is active HIGH. The 80C88/883 READY input is not synchronized. Correct operation is not guaranteed if the set up and hold times are not met.
INTR	18	I	INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowlege operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
$\overline{TEST}$	23	I	TEST: input is examined by the "wait for test" instruction. If the $\overline{TEST}$ input is LOW, execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NONMASKABLE INTERRUPT: is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET: causes the processor to immediately terminate its present activity. The signal must transition LOW to HIGH and remain active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
VCC	40		VCC: is the +5V power supply pin. A 0.1μF capacitor between pins 20 and 40 is recommended for decoupling.
GND	1, 20		GND: are the ground pins (both pins must be connected to system ground). A 0.1μF capacitor between pins 1 and 20 is recommended for decoupling.
MN/$\overline{MX}$	33	I	MINIMUM/MAXIMUM: indicates the mode in which the processor is to operate. The two modes are discussed in the following sections.

S4	S3	CHARACTERISTICS
0	0	Alternate Data
0	1	Stack
1	0	Code or None
1	1	Data

Pin Description

The following pin function descriptions are for the 80C88/883 minimum mode (i.e., MN/$\overline{MX}$ = VCC). Only the pin functions which are unique to the minimum mode are described; all other pin functions are as described above.

MINIMUM MODE SYSTEM

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
IO/$\overline{M}$	28	O	STATUS LINE: is an inverted maximum mode $\overline{S2}$. It is used to distinguish a memory access from an I/O access. IO/$\overline{M}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O = HIGH, M = LOW). IO/$\overline{M}$ is held to a high impedance logic one during local bus "hold acknowledge".
$\overline{WR}$	29	O	Write: strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the IO/$\overline{M}$ signal. $\overline{WR}$ is active for T2, T3 and Tw of any write cycle. It is active LOW, and is held to high impedance logic one during local bus "hold acknowledge".
$\overline{INTA}$	24	O	INTA: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3 and Tw of each interrupt acknowledge cycle. Note that $\overline{INTA}$ is never floated.
ALE	25	O	ADDRESS LATCH ENABLE: is provided by the processor to latch the address into the 82C82/82C83 address latch. It is a HIGH pulse active during clock low of T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	DATA TRANSMIT/RECEIVE: is needed in a minimum system that desires to use an 82C86/82C87 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in the maximum mode, and its timing is the same as for IO/$\overline{M}$ (T = HIGH, R = LOW). This signal is held to a high impedance logic one during local bus "hold acknowledge".
$\overline{DEN}$	26	O	DATA ENABLE: is provided as an output enable for the 82C86/82C87 in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access, and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T2 until the middle of T4, while for a write cycle, it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ is held to high impedance logic one during local bus "hold acknowledge".
HOLD, HLDA	31 30	I O	HOLD: indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgment, in the middle of a T4 or TI clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set up time.
$\overline{SS0}$	34	O	STATUS LINE: is logically equivalent to $\overline{S0}$ in the maximum mode. The combination of $\overline{SS0}$, IO/$\overline{M}$ and DT/$\overline{R}$ allows the system to completely decode the current bus cycle status. $\overline{SS0}$ is held to high impedance logic one during local bus "hold acknowledge".

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SS0}$	CHARACTERISTICS
1	0	0	Interrupt Acknowledge
1	0	1	Read I/O Port
1	1	0	Write I/O Port
1	1	1	Halt
0	0	0	Code Access
0	0	1	Read Memory
0	1	0	Write Memory
0	1	1	Passive

Pin Description

The following pin descriptions are for the 80C88/883 system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

MAXIMUM MODE SYSTEM

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	26 27 28	O O O	STATUS: is active during clock high of T4, T1 and T2, and is returned to the passive state (1, 1, 1) during T3 or during Tw when READY is HIGH. This status is used by the 82C88 bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$ or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or Tw is used to indicate the end of a bus cycle. These signals are held at a high impedance logic one state during "grant sequence".
$\overline{RQ}/\overline{GT0}$, $\overline{RQ}/\overline{GT1}$	31 30	I/O	REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT0}$ having higher priority than $\overline{RQ}/\overline{GT1}$. $\overline{RQ}/\overline{GT}$ has internal bus-hold high circuitry and, if unused, may be left unconnected. The request/grant sequence is as follows (see $\overline{RQ}/\overline{GT}$ Timing Sequence): 1. A pulse of one CLK wide from another local bus master indicates a local bus request ("hold") to the 80C88/883 (pulse 1). 2. During a T4 or TI clock cycle, a pulse one clock wide from the 80C88/883 to the requesting master (pulse 2), indicates that the 80C88/883 has allowed the local bus to float and that it will enter the "grant sequence" state at the next CLK. The CPUs bus interface unit is disconnected logically from the local bus during "grant sequence". 3. A pulse one CLK wide from the requesting master indicates to the 80C88/883 (pulse 3) that the "hold" request is about to end and that the 80C88/883 can reclaim the local bus at the next CLK. The CPU then enters T4 (or TI if no bus cycles pending). Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after bus exchange. Pulses are active LOW. If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met: 1. Request occurs on or before T2. 2. Current cycle is not the low bit of a word. 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next clock. 2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
$\overline{LOCK}$	29	O	LOCK: indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active (LOW). The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a high impedance logic one state during "grant sequence". In Max Mode, $\overline{LOCK}$ is automatically generated during T2 of the first $\overline{INTA}$ cycle and removed during T2 of the second $\overline{INTA}$ cycle.
QS1, QS0	24, 25	O	QUEUE STATUS: provide status to allow external tracking of the internal 80C88/883 instruction queue. The queue status is valid during the CLK cycle after which the queue operation is performed. Note that the queue status never goes to a high impedance state (floated).
-	34	O	Pin 34 is always a logic one in the maximum mode and is held at a high impedance logic one during a "grant sequence".

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

QS1	QS0	CHARACTERISTICS
0	0	No Operation
0	1	First Byte of Opcode From Queue
1	0	Empty the Queue
1	1	Subsequent Byte From Queue

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	27.5°C/W	5.9°C/W
Ceramic LCC Package	62.2°C/W	8.6°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.82W
Ceramic LCC Package 806mW
Gate Count ..... 9750 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage ..... +4.5V to +5.5V
80C88-2/883 ONLY ..... +4.75V to +5.25V

Operating Temperature Range ..... -55°C to +125°C

TABLE 1. 80C88/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested, 80C88/883: VCCL = 4.5V, VCCH = 5.5V, fmax = 5MHz;
80C88-2/883: VCCL = 4.75V, VCCH = 5.25V, fmax = 8MHz

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	VIH	VCC = VCCH, Note 2	1, 2, 3	$-55°C \le T_A \le +125°C$	2.2	-	V
Logical Zero Input Voltage	VIL	Note 2	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.8	V
CLK Logical One Input Voltage	VIHC	VCC = VCCH	1, 2, 3	$-55°C \le T_A \le +125°C$	VCC-0.8	-	V
CLK Logical Zero Input Voltage	VILC		1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.8	V
Output HIGH Voltage	VOH	IOH = -2.5mA, Note 3 IOH = -100µA, Note 3	1, 2, 3 1, 2, 3	$-55°C \le T_A \le +125°C$	3.0 VCC-0.4	- -	V V
Output LOW Voltage	VOL	IOL = +2.5mA, Note 3	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Input Leakage Current	II	VCC = VCCH, VIN = GND or VCC DIP Pins: 17-19, 21-23, 33	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Input Current Bus Hold High	IBHH	VIN = 3.0V, Note 4 VCC = VCCL & VCCH	1, 2, 3	$-55°C \le T_A \le +125°C$	-40	-400	µA
Input Current Bus Hold Low	IBHL	VIN = 0.8V, Note 5 VCC = VCCL & VCCH	1, 2, 3	$-55°C \le T_A \le +125°C$	40	400	µA
Output Leakage Current	IO	VCC = VCCH, VOUT = 0V, Note 6	1, 2, 3	$-55°C \le T_A \le +125°C$	-	-10	µA
Standby Power Supply Current	ICCSB	VCC = VCCH, Note 7	1, 2, 3	$-55°C \le T_A \le +125°C$	-	500	µA
Operating Power Supply Current	ICCOP	VCC = VCCH, f = fmax, VIN = VCC or GND, Outputs Open	1, 2, 3	$55°C \le T_A \le +125°C$	-	10	mA/MHz

NOTES: 1. All voltages referenced to device GND, VCC = VCCL unless otherwise specified.
2. MN/$\overline{MX}$ is a strap option and should be held to VCC or GND.
3. Interchanging of force and sense conditions is permitted.
4. IBHH should be measured after raising VIN to VCC and then lowering to valid input high level of 3.0V on the following pins: 2-16, 26-32, 34-39.
5. IBHL should be measured after lowering VIN to GND and then raising to valid input low level of 0.8V on the following pins: 2-16, 35-39.
6. IO should be measured by putting the pin in a high impedance state and then driving VOUT to GND on the following pins: 26-29, 32.
7. ICCSB tested during clock high time after HALT instruction execution. VIN = VCC or GND, VCC = VCCH, outputs unloaded.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. 80C88/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested, 80C88/883: VCCL = 4.5V, VCCH = 5.5V,
80C88-2/883: VCCL = 4.75V, VCCH = 5.25V

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	80C88-2/883 MIN	80C88-2/883 MAX	80C88/883 MIN	80C88/883 MAX	UNITS
MINIMUM COMPLEXITY SYSTEM TIMING									
CLK Cycle Period	(1)TCLCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	125	-	200	-	ns
CLK Low Time	(2)TCLCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	68	-	118	-	ns
CLK High Time	(3)TCHCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	44	-	69	-	ns
Data In Setup Time	(6)TDVCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	30	-	ns
Data In Hold Time	(7)TCLDX1		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	10	-	ns
READY Setup Time into 80C88/883	(10)TRYHCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	68	-	118	-	ns
READY Hold Time into 80C88/883	(11)TCHRYX		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	30	-	ns
READY Inactive to CLK	(12)TRYLCL	Note 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-8	-	-8	-	ns
HOLD Setup Time	(13)THVCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	35	-	ns
INTR, NMI, $\overline{TEST}$ Setup Time	(14)TINVCH	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	30	-	ns
Address Valid Delay	(17)TCLAV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	60	10	110	ns
Address Hold Time	(18)TCLAX		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	10	-	ns
ALE Width	(22)TLHLL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TCLCH -10	-	TCLCH -20	-	ns
ALE Active Delay	(23)TCLLH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	50	-	80	ns
ALE Inactive Delay	(24)TCHLL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	55	-	85	ns
Address Hold Time to ALE Inactive	(25)TLLAX		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TCHCL -10	-	TCHCL -10	-	ns
Data Valid Delay	(26)TCLDV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	60	10	110	ns
Control Active Delay 1	(29)TCVCTV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	70	10	110	ns
Control Active Delay 2	(30)TCHCTV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	60	10	110	ns
Control Inactive Delay	(31)TCVCTX		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	70	10	110	ns
$\overline{RD}$ Active Delay	(33)TCLRL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	100	10	165	ns
$\overline{RD}$ Inactive Delay	(34)TCLRH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	80	10	150	ns
$\overline{RD}$ Inactive to Next Address Active	(35)TRHAV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TCLCL -40	-	TCLCL -45	-	ns
HLDA Valid Delay	(36)TCLHAV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	100	10	160	ns
$\overline{RD}$ Width	(37)TRLRH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	2 TCLCL -50	-	2 TCLCL -75	-	ns
$\overline{WR}$ Width	(38)TWLWH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	2 TCLCL -40	-	2 TCLCL -60	-	ns
Address Valid to ALE Low	(39)TAVAL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TCLCH -40	-	TCLCH -60	-	ns

NOTES: 1. VCC = VCCL, CL = 100pF, f = 1MHz
2. Applies only to T2 state (8ns into T3)
3. Setup requirement for asynchronous signal only to guarantee recognition at next clock.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. 80C88/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

80C88/883: VCCL = 4.5V, VCCH = 5.5V, 80C88-2/883: VCCL = 4.75V, VCCH = 5.25V

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	80C88-2/883		80C88/883		UNITS
					MIN	MAX	MIN	MAX	
MINIMUM COMPLEXITY SYSTEM TIMING									
Input Capacitance	CIN	f = 1MHz, All measurements are referenced to GND	1	T_A = +25°C	-	25	-	25	pF
Output Capacitance	COUT		1	T_A = +25°C	-	25	-	25	pF
I/O Capacitance	CI/O		1	T_A = +25°C	-	25	-	25	pF
CLK Rise Time	TCH1CH2 (4)	From 1.0V to 3.5V	1	-55°C≤T_A≤+125°C	-	10	-	10	ns
CLK Fall Time	TCL2CL1 (5)	From 3.5V to 1.0V	1	-55°C≤T_A≤+125°C	-	10	-	10	ns
RDY Setup Time Into 82C84A	TR1VCL (8)	CL = 100pF, VCC = VCCL, f = 1MHz	1, 2, 3	-55°C≤T_A≤+125°C	35	-	35	-	ns
RDY Hold Time Into 82C84A	TCLR1X (9)	CL = 100pF, VCC = VCCL, f = 1MHz	1, 2, 3	-55°C≤T_A≤+125°C	0	-	0	-	ns
Input Rise Time (Except CLK)	TILIH (15)	From 0.8V to 2.0V	1	-55°C≤T_A≤+125°C	-	15	-	15	ns
Input Fall Time (Except CLK)	TIHIL (16)	From 2.0V to 0.8V	1	-55°C≤T_A≤+125°C	-	15	-	15	ns
Address Float Delay	TCLAZ (19)	CL = 100pF, VCC = VCCL, f = 1MHz	1	-55°C≤T_A≤+125°C	TCLAX	50	TCLAX	80	ns
Status Float Delay	TCHSZ (20)		1	-55°C≤T_A≤+125°C	-	50	-	80	ns
Data Hold Time	TCLDX2 (27)		1	-55°C≤T_A≤+125°C	10	-	10	-	ns
Data Hold Time After $\overline{WR}$	TWHDX (28)		1	-55°C≤T_A≤+125°C	TCLCL -30	-	TCLCL -30	-	ns
Address Float To $\overline{RD}$ Active	TAZRL (32)		1	-55°C≤T_A≤+125°C	0	-	0	-	ns
Output Rise Time	TOLOH (40)	From 0.8V to 2.0V	1	-55°C≤T_A≤+125°C	-	15	-	15	ns
Output Fall Time	TOHOL (41)	From 2.0V to 0.8V	1	-55°C≤T_A≤+125°C	-	15	-	15	ns

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Signal at 82C84A shown for reference only.
3. Setup requirement for asynchronous signal only to guarantee recognition at next clock.

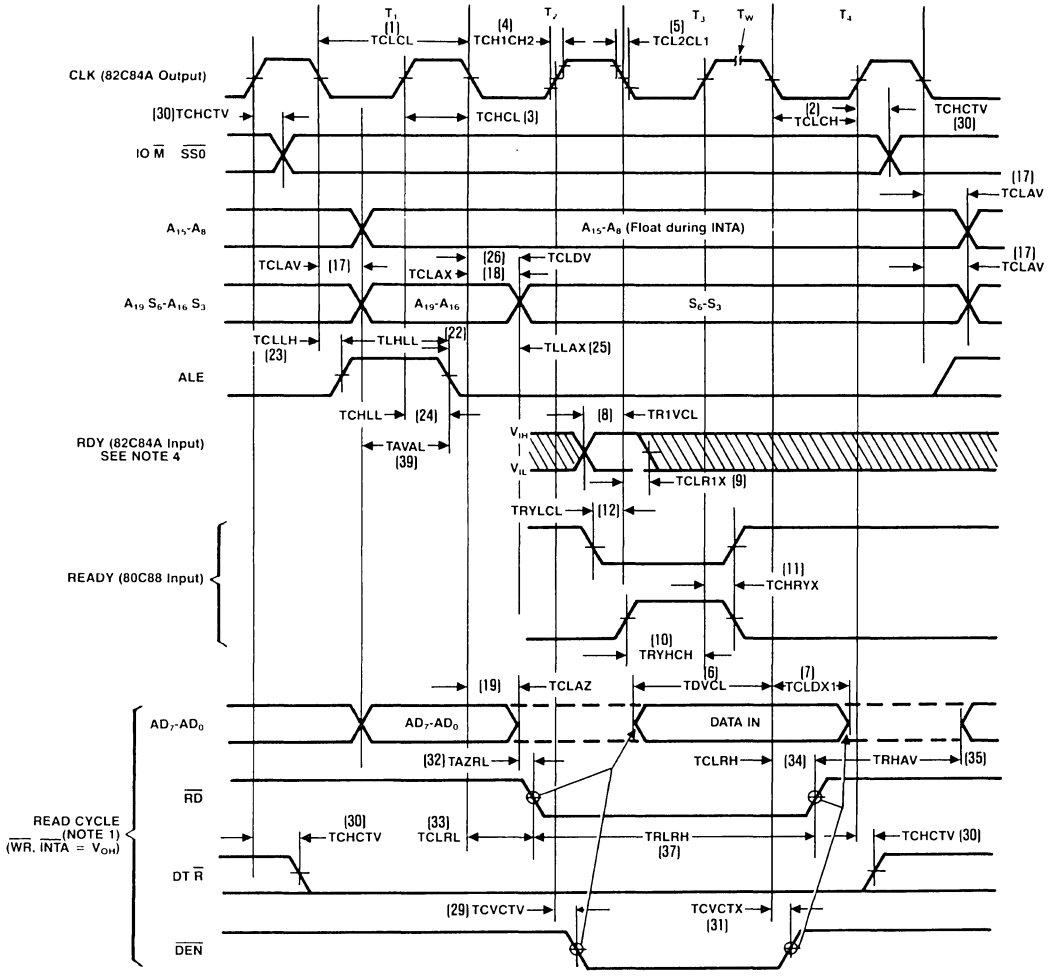
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Waveforms

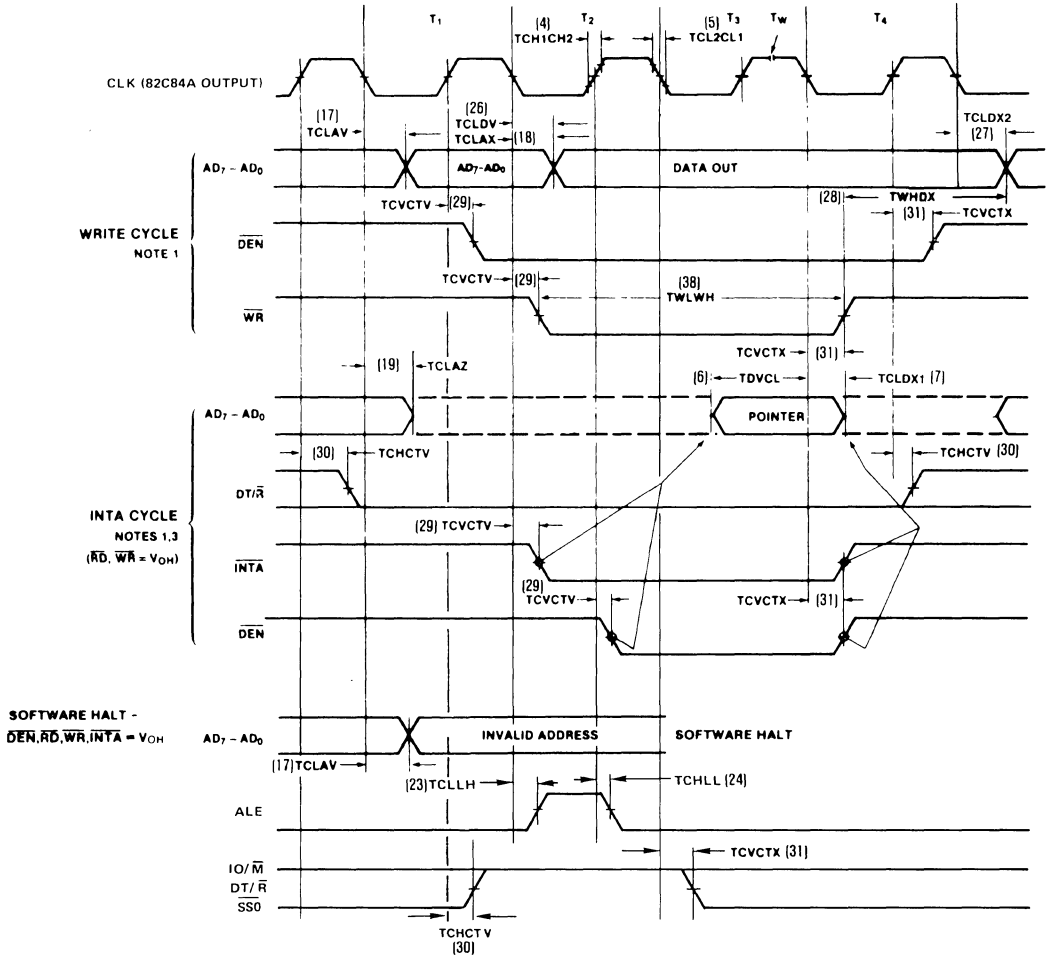
BUS TIMING - MINIMUM MODE SYSTEM



NOTES:
1. All signals switch between VOH and VOL unless otherwise specified.
2. RDY is sampled near the end of T2, T3, Tw to determine if Tw machine states are to be inserted.
3. Two $\overline{\text{INTA}}$ cycles run back-to-back. The 80C88/883 local ADDR/DATA bus is floating during both $\overline{\text{INTA}}$ cycles. Control Signals are shown for the second $\overline{\text{INTA}}$ cycle.
4. Signals at 82C84A are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

Waveforms (Continued)

BUS TIMING - MINIMUM MODE SYSTEM (Continued)



NOTES:
1. All signals switch between VOH and VOL unless otherwise specified.
2. RDY is sampled near the end of T2, T3, Tw to determine if Tw machine states are to be inserted.
3. Two $\overline{\text{INTA}}$ cycles run back-to-back. The 80C88/883 local ADDR/DATA bus is floating during both $\overline{\text{INTA}}$ cycles. Control Signals are shown for the second $\overline{\text{INTA}}$ cycle.
4. Signals at 82C84A are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

TABLE 2. 80C88/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested, 80C88/883: VCCL = 4.5V, VCCH = 5.5V,
80C88-2/883: VCCL = 4.75V, VCCH = 5.25V

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	80C88-2/883		80C88/883		UNITS
					MIN	MAX	MIN	MAX	
MAXIMUM MODE SYSTEM TIMING (USING 82C88 BUS CONTROLLER)									
CLK Cycle Period	(1)TCLCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	125	-	200	-	ns
CLK Low Time	(2)TCLCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	68	-	118	-	ns
CLK High Time	(3)TCHCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	44	-	69	-	ns
Data In Setup Time	(6)TDVCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	30	-	ns
Data In Hold Time	(7)TCLDX1		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	10	-	ns
READY Setup Time into 80C88/883	(10)TRYHCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	68	-	118	-	ns
READY Hold Time into 80C88/883	(11)TCHRYX		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	30	-	ns
READY Inactive to CLK	(12)TRYLCL	Note 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-8	-	-8	-	ns
Setup Time For Recognition (INTR, NMI, $\overline{TEST}$)	(13)TINVCH	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	30	-	ns
$\overline{RQ}/\overline{GT}$ Setup Delay	(14)TGVCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	30	-	ns
$\overline{RQ}$ Hold Time Into 80C88/883	(15)TCHGX	Note 4	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	TCHCL +10	40	TCHCL +10	ns
READY Active to Status Passive	(20)TRYHSH	Notes 2, 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	65	-	110	ns
Status Active Delay	(21)TCHSV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	60	10	110	ns
Status Inactive Delay	(22)TCLSH	Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	70	10	130	ns
Address Valid Delay	(23)TCLAV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	60	10	110	ns
Address Hold Time	(24)TCLAX		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	10	-	ns
Data Valid Delay	(33)TCLDV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	60	10	110	ns
$\overline{RD}$ Active Delay	(38)TCLRL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	100	10	165	ns
$\overline{RD}$ Inactive Delay	(39)TCLRH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	80	10	150	ns
$\overline{RD}$ Inactive to Next Address Active	(40)TRHAV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TCLCL -45	-	TCLCL -45	-	ns
$\overline{GT}$ Active Delay	(43)TCLGL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	50	0	85	ns
$\overline{GT}$ Inactive Delay	(44)TCLGH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	50	0	85	ns
$\overline{RD}$ Width	(45)TRLRH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	2 TCLCL -50	-	2 TCLCL -75	-	ns

NOTES: 1. VCC = VCCL, CL = 100pF, f = 1MHz
2. Applies only to T2 state (8ns into T3)
3. Setup requirement for asynchronous signal only to guarantee recognition at next clock.
4. The 80C88 actively pulls the $\overline{RQ}/\overline{GT}$ pin to a logic one on the following clock low time.
5. Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. 80C88/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

80C88/883: VCCL = 4.5V, VCCH = 5.5V, 80C88-2/883: VCCL = 4.75V, VCCH = 5.25V

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	80C88-2/883		80C88/883		UNITS
					MIN	MAX	MIN	MAX	
MAXIMUM MODE SYSTEM TIMING (USING 82C88 BUS CONTROLLER)									
Input Capacitance	CIN	f = 1MHz, All measurements are referenced to GND	1	T_A = +25°C	-	25	-	25	pF
Output Capacitance	COUT		1	T_A = +25°C	-	25	-	25	pF
I/O Capacitance	CI/O		1	T_A = +25°C	-	25	-	25	pF
CLK Rise Time	TCH1CH2 (4)	From 1.0V to 3.5V	1	-55°C≤T_A≤+125°C	-	10	-	10	ns
CLK Fall Time	TCL2CL1 (5)	From 3.5V to 1.0V	1	-55°C≤T_A≤+125°C	-	10	-	10	ns
RDY Setup Time Into 82C84A	TR1VCL (8)	CL = 100pF, VCC = VCCL, f = 1MHz	1, 2, 3	-55°C≤T_A≤+125°C	35	-	35	-	ns
RDY Hold Time Into 82C84A	TCLR1X (9)	CL = 100pF, VCC = VCCL, f = 1MHz	1, 2, 3	-55°C≤T_A≤+125°C	0	-	0	-	ns
Input Rise Time (Except CLK)	TILIH (16)	From 0.8V to 2.0V	1	-55°C≤T_A≤+125°C	-	15	-	15	ns
Input Fall Time (Except CLK)	TIHIL (17)	From 2.0V to 0.8V	1	-55°C≤T_A≤+125°C	-	15	-	15	ns
Command Active Delay	TCLML (18)	CL = 100pF, VCC = VCCL f = 1MHz	1, 2	-55°C≤T_A≤+125°C	5	35	5	35	ns
Command Inactive Delay	TCLMH (19)		1, 2	-55°C≤T_A≤+125°C	5	35	5	35	ns
Address Float Delay	TCLAZ (25)		1	-55°C≤T_A≤+125°C	TCLAX	50	TCLAX	80	ns
Status Float Delay	TCHSZ (26)		1	-55°C≤T_A≤+125°C	-	50	-	80	ns
Status Valid To ALE High	TSVLH (27)		1, 2	-55°C≤T_A≤+125°C	-	20	-	20	ns
Status Valid To MCE High	TSVMCH (28)		1, 2	-55°C≤T_A≤+125°C	-	30	-	30	ns
CLK Low To ALE Valid	TCLLH (29)		1, 2	-55°C≤T_A≤+125°C	-	20	-	20	ns
CLK Low To MCE High	TCLMCH (30)		1, 2	-55°C≤T_A≤+125°C	-	25	-	25	ns
ALE Inactive Delay	TCHLL (31)		1, 2	-55°C≤T_A≤+125°C	4	18	4	18	ns
MCE Inactive Delay	TCLMCL (32)		1, 2	-55°C≤T_A≤+125°C	-	15	-	15	ns
Data Hold Time	TCLDX2 (34)		1	-55°C≤T_A≤+125°C	10	-	10	-	ns
Control Active Delay	TCVNV (35)		1, 2	-55°C≤T_A≤+125°C	5	45	5	45	ns
Control Inactive Delay	TCVNX (36)		1, 2	-55°C≤T_A≤+125°C	10	45	10	45	ns

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Signal at 82C84A or 82C88 shown for reference only.
3. Setup requirement for asynchronous signal only to guarantee recognition at next clock.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. 80C88/883 ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

80C88/883: VCCL = 4.5V, VCCH = 5.5V, 80C88-2/883: VCCL = 4.75V, VCCH = 5.25V

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	80C88-2/883		80C88/883		UNITS
					MIN	MAX	MIN	MAX	
MAXIMUM MODE SYSTEM TIMING (USING 82C88 BUS CONTROLLER, (Continued)									
Address Float To Read Active	TAZRL (37)	CL = 100pF, VCC = VCCL, f = 1 MHz	1	$-55^{o}C \leq T_A \leq +125^{o}C$	0	-	0	-	ns
Direction Control Active Delay	TCHDTL (41)		1, 2	$-55^{o}C \leq T_A \leq +125^{o}C$	-	50	-	50	ns
Direction Control Inactive Delay	TCHDTH (42)		1, 2	$-55^{o}C \leq T_A \leq +125^{o}C$	-	30	-	30	ns
Output Rise Time	TOLOH (46)	From 0.8V to 2.0V	1	$-55^{o}C \leq T_A \leq +125^{o}C$	-	15	-	15	ns
Output Fall Time	TOHOL (47)	From 2.0V to 0.8V	1	$-55^{o}C \leq T_A \leq +125^{o}C$	-	15	-	15	ns

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Signal at 82C84A or 82C88 shown for reference only.

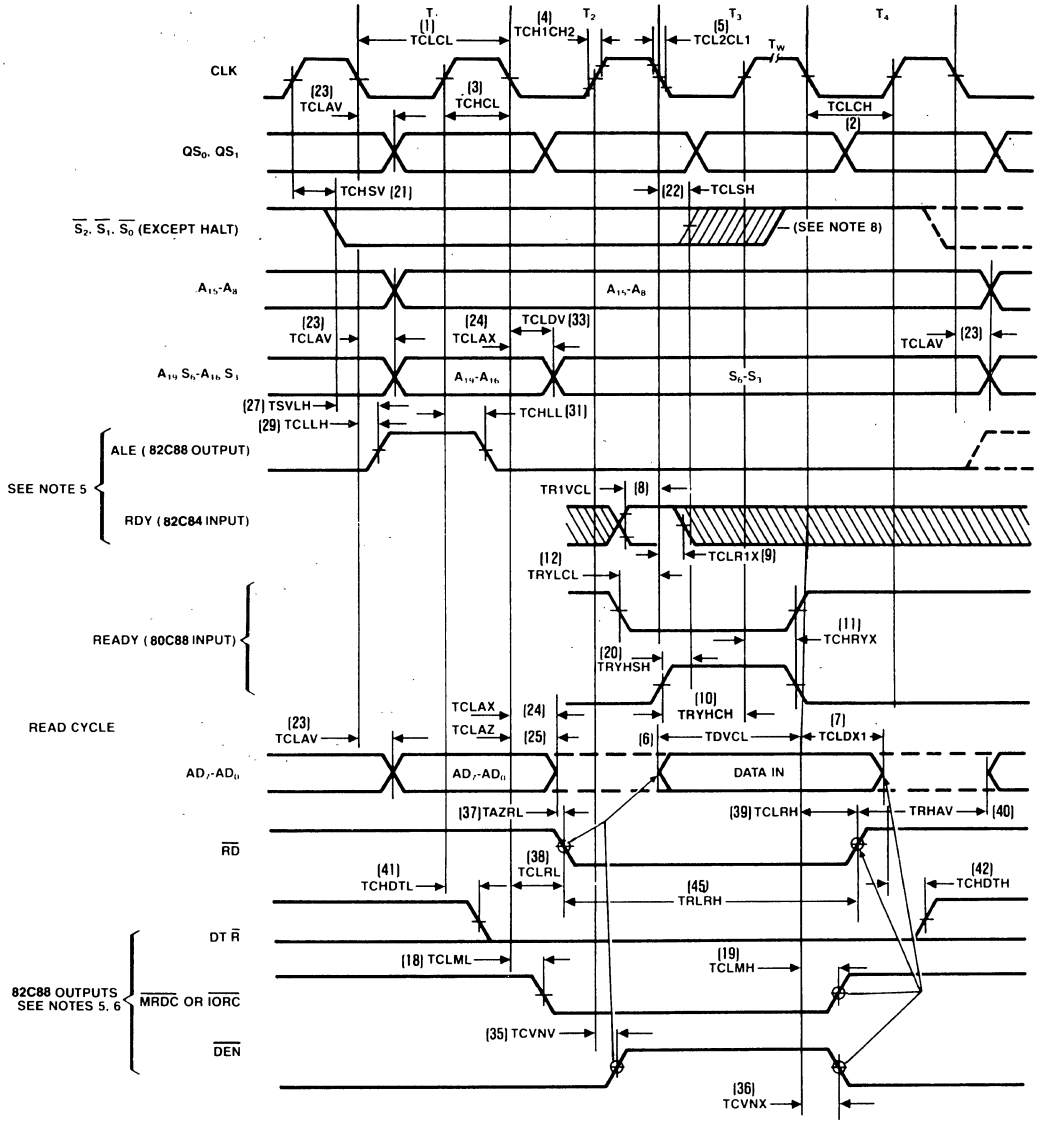
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Waveforms

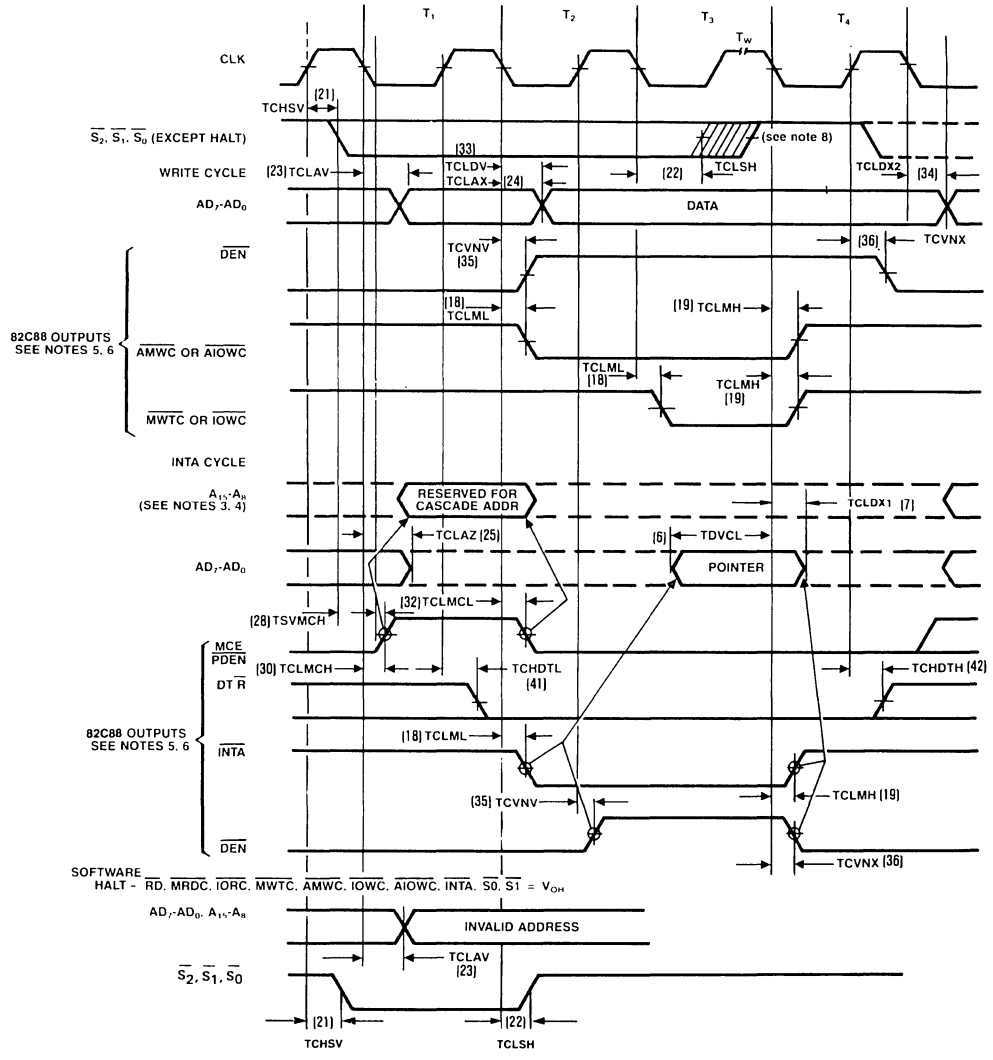
BUS TIMING – MAXIMUM MODE



NOTES:
1. All signals switch between VOH and VOL, unless otherwise specified.
2. RDY is sampled near the end of T2, T3, Tw to determine if Tw machine states are to be inserted.
3. Cascade address is valid between first and second $\overline{INTA}$ cycles.
4. Two $\overline{INTA}$ cycles run back-to-back. The 80C88/883 local ADDR/DATA bus is floating during both $\overline{INTA}$ cycles. Control for pointer address is shown for second $\overline{INTA}$ cycle.
5. Signals at 82C84A or 82C88 are shown for reference only.
6. The issuance of the 82C88 command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ and $\overline{DEN}$) lags the active high 82C88 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T4.

Waveforms (Continued)

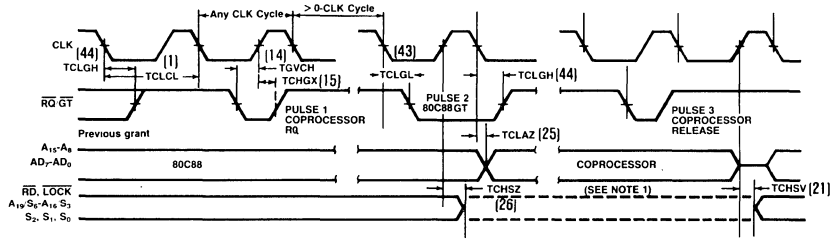
BUS TIMING – MAXIMUM MODE SYSTEM (USING 82C88) (Continued)



NOTES:
1. All signals switch between VOH and VOL, unless otherwise specified.
2. RDY is sampled near the end of T2, T3, Tw to determine if Tw machine states are to be inserted.
3. Cascade address is valid between first and second $\overline{\text{INTA}}$ cycles.
4. Two $\overline{\text{INTA}}$ cycles run back-to-back. The 80C88/883 local ADDR/DATA bus is floating during both $\overline{\text{INTA}}$ cycles. Control for pointer address is shown for second $\overline{\text{INTA}}$ cycle.
5. Signals at 82C84A or 82C88 are shown for reference only.
6. The issuance of the 82C88 command and control signals ($\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$ and $\overline{\text{DEN}}$) lags the active high 82C88 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T4.

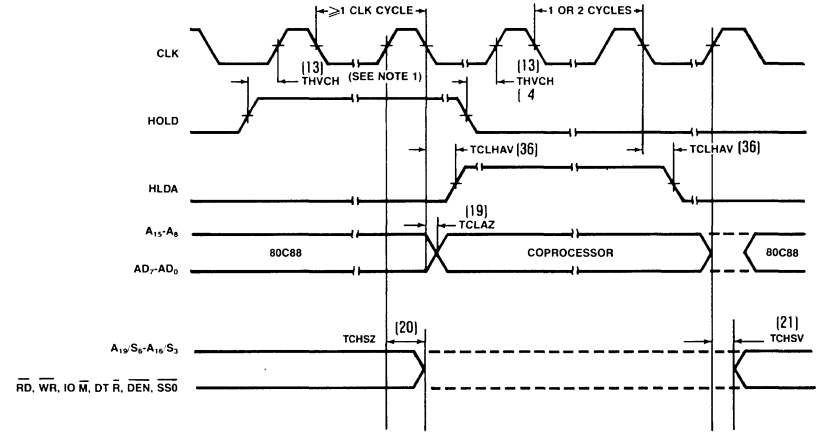
Waveforms (Continued)

REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



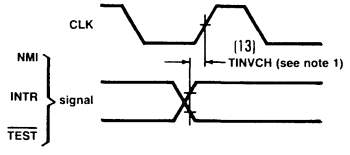
NOTE: The coprocessor may not drive the busses outside the region shown without risking contention

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



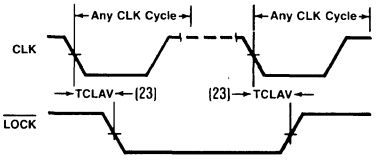
NOTE: Setup requirements for asynchronous signals only to guarantee recognition at next CLK

ASYNCHRONOUS SIGNAL RECOGNITION



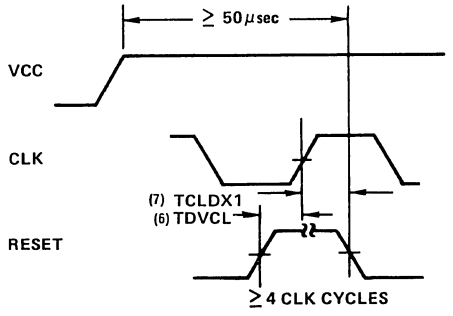
NOTE: Setup requirements for asynchronous signals only to guarantee recognition at next CLK

BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)

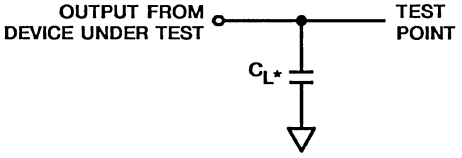


Waveforms (Continued)

RESET TIMING

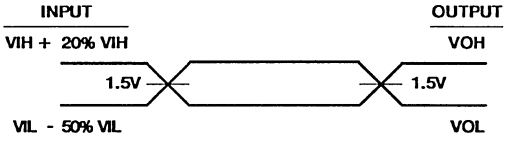


A.C. Test Circuit



*Includes stay and jig capacitance

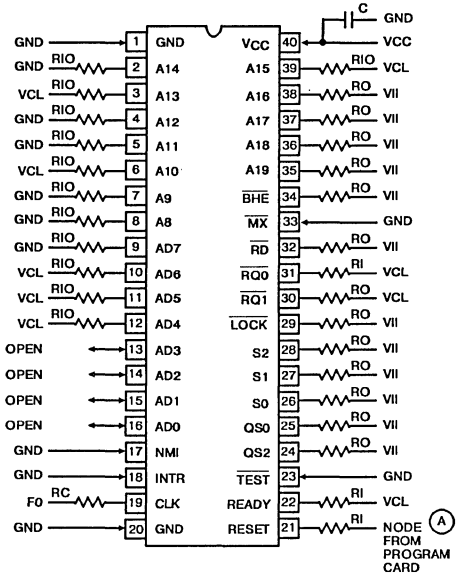
A.C. Testing Input, Output Waveform



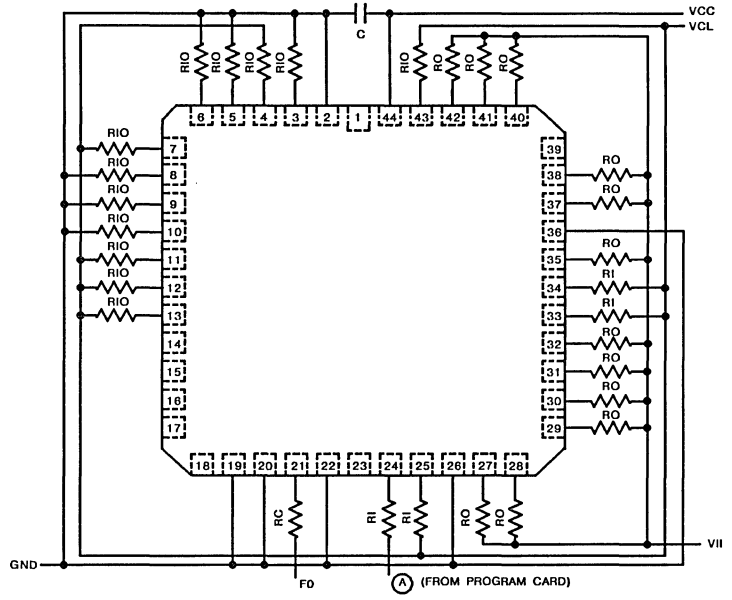
A.C. Testing: All input signals (other than CLK) must switch between VILmax -50% VIL and VIHmin +20% VIH. CLK must switch between 0.4V and VCC -0.4V. Input rise and fall times are driven at 1ns/V.

Burn-In Circuits

80C88/883 (CERAMIC DIP)



80C88/883 (CERAMIC LCC)



NOTES:
1. VCC = 5.5V ± 0.5V, GND = 0V
2. Input Voltage Limits:
   VIL (Maximum) = 0.4V
   VIH (Minimum) = 2.6V
3. VII is external supply set to 2.7V
4. VCL is generated on program card (VCC - 1.2V)
5. Pins 13 - 16 input sequenced instructions from internal hold devices, (DIP Only).

COMPONENTS: (per card)
1. RI = 10kΩ ± 5%, 1/4W (4)
2. RO = 1.2kΩ ± 5%, 1/4W (12)
3. RIO = 2.7kΩ ± 5%, 1/4W (16)
4. RC = 1kΩ ± 5%, 1/4W (1)
5. C = 0.01μF Minimum

Metallization Topology

DIE DIMENSIONS:
249.2 x 290.9 x 19 ± 1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 2kÅ

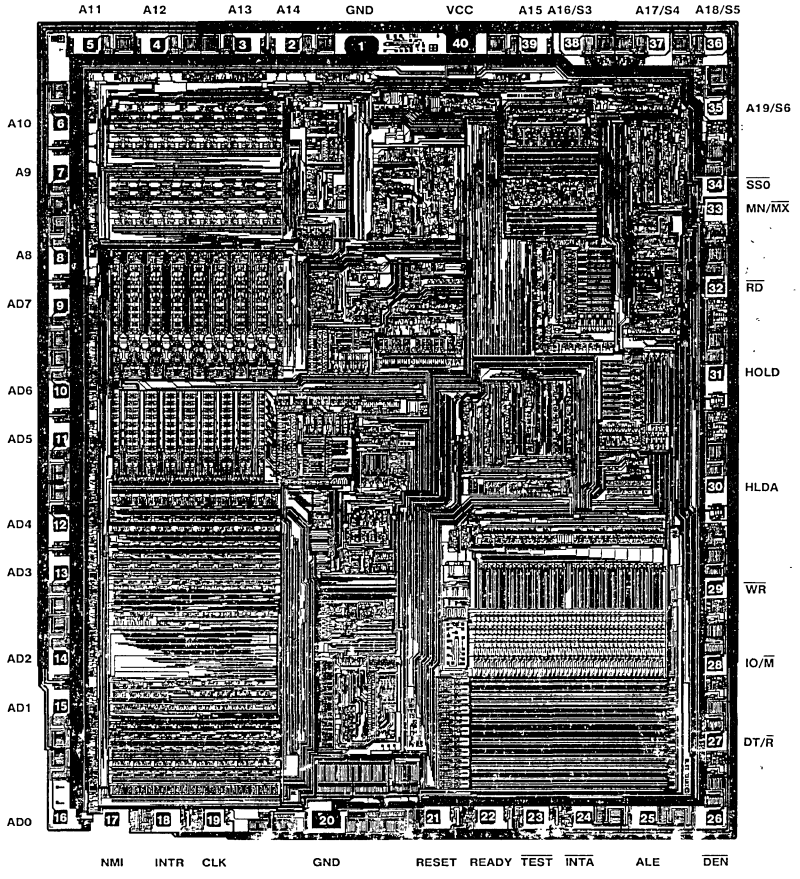
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.5 x 10^5 A/cm^2

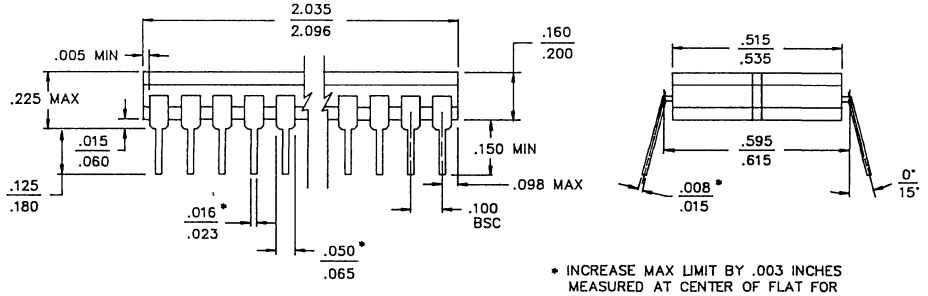
Metallization Mask Layout

80C88/883



Packaging†

40 PIN CERAMIC DIP

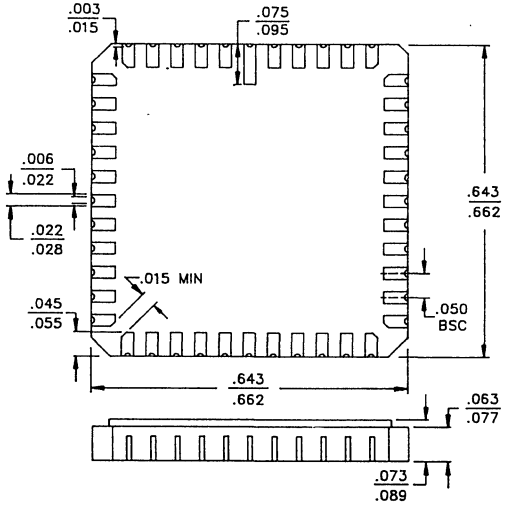


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-5

44 PAD CERAMIC LCC
(BOTTOM VIEW)



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-5

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Functional Description

Static Operation

All 80C88 circuitry is static in design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS 80C88 can operate from DC to the specified upper frequency limit. The processor clock may be stoped in either state (high/low) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The 80C88 can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for start-up.

Static design also allows very low frequency operation (as low as DC). In a power critical situation, this can provide extremely low power operation since 80C88 power dissipation is directly related to operation frequency. As the system frequency is reduced, so is the operating power until, at a DC input frequency, the power requirement is the 80C88 standby current.

Internal Architecture

The internal functions of the 80C88 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the CPU block diagram.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 4 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 1 byte in the queue, the BIU will attempt a byte fetch memory cycle. This greatly reduces "dead time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides unrelocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

Memory Organization

The processor provides a 20 bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra, and stack segments of up to 64K bytes each, with each segment falling on 16 byte boundaries. (See Figure 1).

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to specific rules as shown in Table A. All information in one segment type share the same logical attributes (e.g., code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16 bit) operands can be located on even or odd address boundaries. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location.

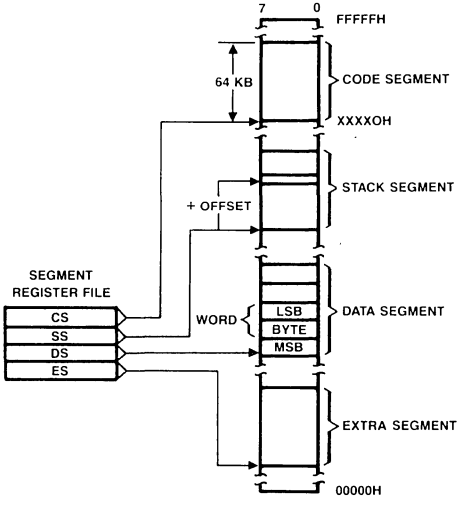


FIGURE 1. MEMORY ORGANIZATION

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

TABLE A.

MEMORY REFERENCE NEED	SEGMENT REGISTER USED	SEGMENT SELECTION RULE
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when: relative to stack, destination of string operation, or explicitly overridden.
External Data (Global)	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

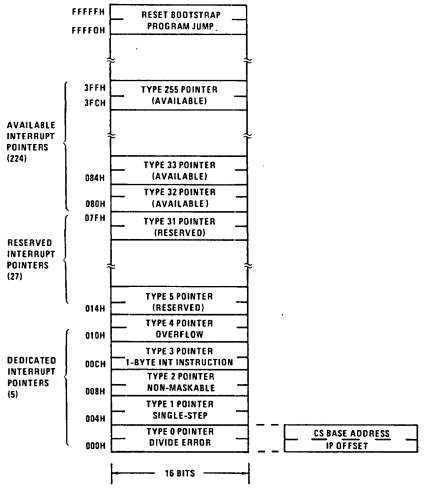


FIGURE 2. RESERVED MEMORY LOCATIONS

The BIU will automatically execute two fetch or write cycles for 16 bit operands.

Certain locations in memory are reserved for specific CPU operations. (See Figure 2). Locations from addresses FFFF0H through FFFFFH are reserved for operations including a jump to the initial system initialization routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt service routines is accessed through its own pair of 16 bit pointers - segment address pointer and offset address pointer. The first pointer, used as the offset address, is loaded into the IP, and the second pointer, which designates the base address, is loaded into the CS. At this point program control is transferred to the interrupt routine. The pointer elements are assumed to have been stored at their respective places in reserved memory prior to the occurrence of interrupts.

Minimum and Maximum Modes

The requirements for supporting minimum and maximum 80C88 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 80C88 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the 80C88 defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{MX}$ pin is strapped to VCC, the 80C88 generates bus control signals itself on pins 24 through 31 and 34.

The minimum mode 80C88 can be used with either a multiplexed or demultiplexed bus. This architecture provides the 80C88 processing power in a highly integrated form.

The demultiplexed mode requires one latch (for 64K addressability) or two latches (for a full megabyte of addressing). An 82C86 or 82C87 transceiver can also be used if data bus buffering is required. (See Figure 3). The 80C88 provides $\overline{DEN}$ and DT/$\overline{R}$ to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the 82C88 bus controller (See Figure 4). The 82C88 decodes status lines $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$, and provides the system with all bus control signals. Moving the bus control to the 82C88 provides better source and sink current capability to the control lines, and frees the 80C88 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the 80C88 in maximum mode. These features allow coprocessors in local bus and remote bus configurations.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

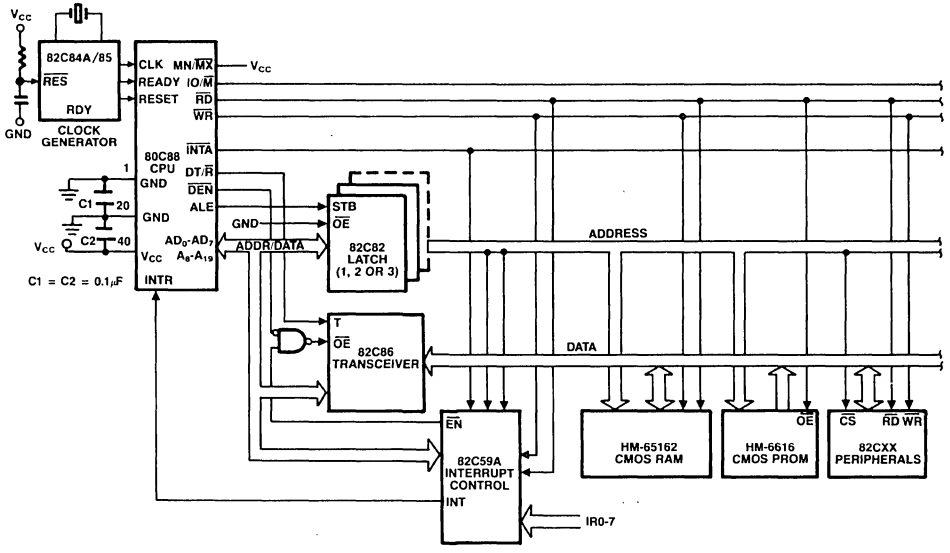


FIGURE 3. DEMULTIPLEXED BUS CONFIGURATION

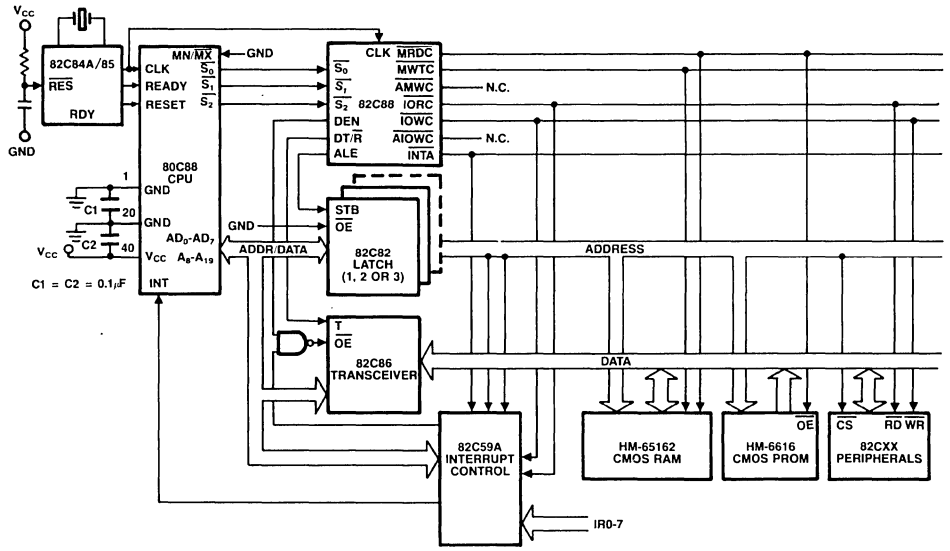


FIGURE 4. FULLY BUFFERED SYSTEM USING BUS CONTROLLER

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Bus Operation

The 80C88 address/data bus is broken into three parts: the lower eight address/data bits (AD0-AD7), the middle eight address bits (A8-A15), and the upper four address bits (A16-A19). The address/data bits and the highest four adddress bits are time multiplexed. This technique provides the most efficient use of pins on the processor, permitting the use of a standard 40 lead package. The middle eight address bits are not multiplexed, i.e., they remain valid throughout each bus cycle. In addition, the bus can be demultiplexed at the processor with a single address latch if a standard, nonmultiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3 and T4. (See Figure 5). The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a "Not Ready" indication is given by the addressed device, "wait" states (Tw) are inserted between T3 and T4. Each inserted "wait" state is of the same duration as a CLK cycle. Periods can occur between 80C88 driven bus cycles. These are referred to as "idle" states (Ti), or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

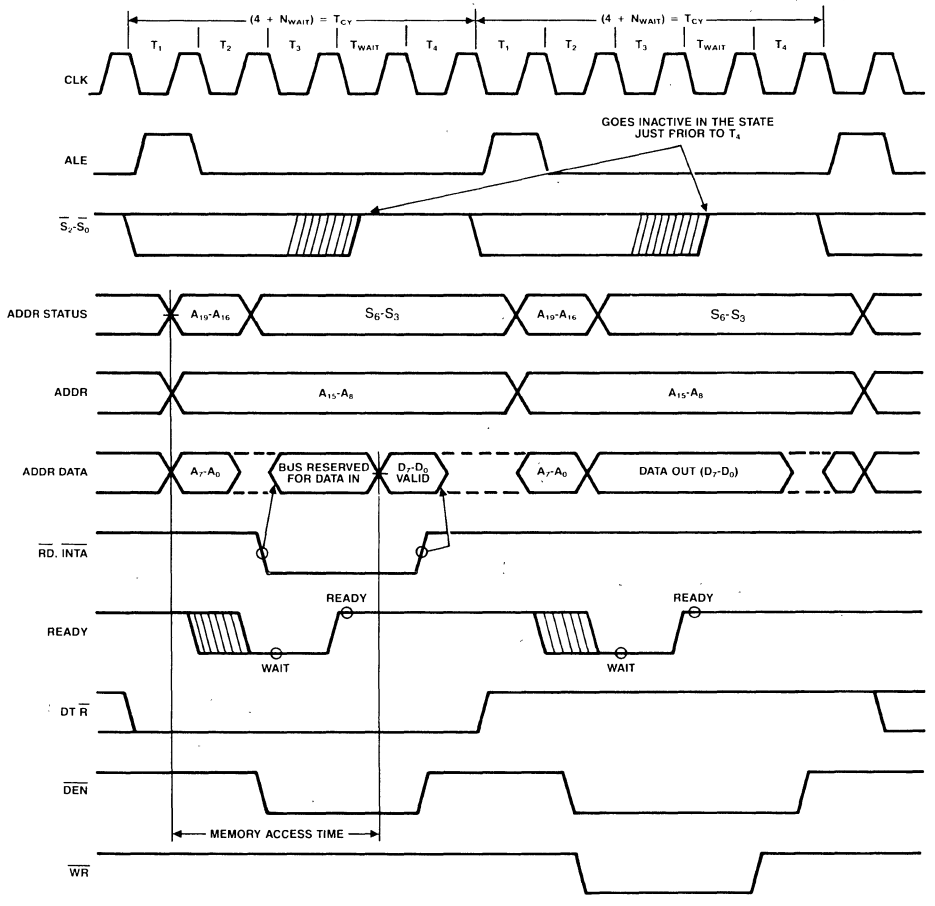


FIGURE 5. BASIC SYSTEM TIMING

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

During T1 of any bus cycle, the ALE (Address latch enable) signal is emitted (by either the processor or the 82C88 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to Table B.

Status bits S3 through S6 are multiplexed with high order address bits and are therefore valid during T2 through T4. S3 and S4 indicate which segment register was used for this bus cycle in forming the address according to Table C.

S5 is a reflection of the PSW interrupt enable bit. S6 is always equal to 0.

TABLE B.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (No Bus Cycle)

TABLE C.

S4	S3	CHARACTERISTICS
0	0	Alternate Data (Extra Segment)
0	1	Stack
1	0	Code or None
1	1	Data

I/O Addressing

In the 80C88, I/O operations can address up to a maximum of 64K I/O registers. The I/O address appears in the same format as the memory address on bus lines A15-A0. The address lines A19-A16 are zero in I/O operations. The variable I/O instructions, which use register DX as a pointer, have full address capability, while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space. I/O ports are addressed in the same manner as memory locations.

Designers familiar with the 8085 or upgrading an 8085 design should note that the 8085 addresses I/O with an 8 bit address on both halves of the 16 bit address bus. The 80C88 uses a full 16 bit address on its lower 16 address lines.

External Interface

Processor Reset and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 80C88 RESET is required to be HIGH for greater than four clock cycles. The 80C88 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval the 80C88 operates normally, beginning with the instruction in absolute location FFFF0H (see Figure 2). The RESET input is internally synchronized to the processor clock. At initialization, the HIGH to LOW transition of RESET must occur no sooner than 50μs after power up, to allow complete initialization of the 80C88.

NMI will not be recognized if asserted prior to the second CLK cycle following the end of RESET.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate the need for pull-up/down resistors, "bus-hold" circuitry has been used on 80C88 pins 2-16, 26-32 and 34-39 (see Figure 6a and 6b). These circuits maintain a valid logic state if no driving source is present (i.e., an unconnected pin or a driving source which goes to a high impedance state).

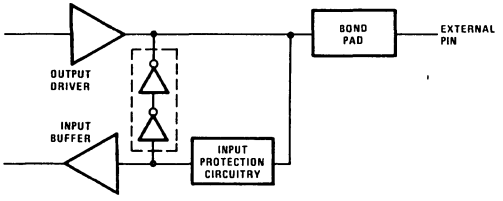


FIGURE 6A. BUS HOLD CIRCUITRY PIN 2-16, 35-39

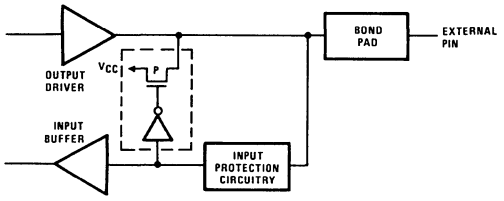


FIGURE 6B. BUS HOLD CIRCUITRY PIN 26-32, 34

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

To override the "bus hold" circuits, an external driver must be capable of supplying 400μA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible. Power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the instruction set description. Hardware interrupts can be classified as nonmaskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256 element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (see Figure 2), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8 bit type number, during the interrupt acknowledge sequence, which is used to vector through the appropriate element to the new interrupt service program location.

Non-maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt (NMI) pin which has higher priority than the maskable interrupt request (INTR) pin. A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW to HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two clock cycles, but is not required to be synchronized to the clock. Any high going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves (2 bytes in the case of word moves) of a block type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure.

The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The 80C88 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable (IF) flag bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK.

To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block type instruction. INTR may be removed anytime after the falling edge of the first $\overline{INTA}$ signal. During interrupt response sequence, further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt, or single step). The FLAGS register, which is automatically pushed onto the stack, reflects the state of the processor prior to the interrupt. The enable bit will be zero until the old FLAGS register is restored, unless specifically set by an instruction.

During the response sequence (see Figure 7), the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 80C88 emits the $\overline{LOCK}$ signal (maximum mode only) from T2 of the first bus cycle until T2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is fetched from the external interrupt system (e.g., 82C59A PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table.

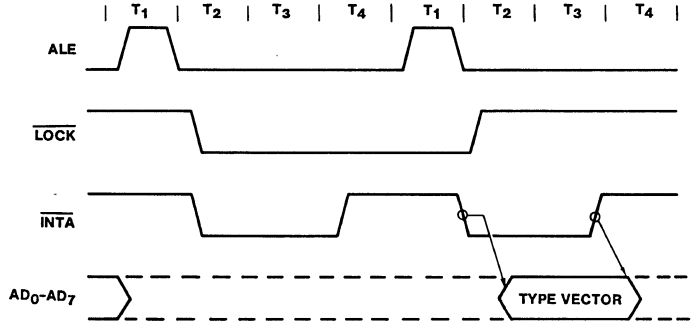


FIGURE 7. INTERRUPT ACKNOWLEDGE SEQUENCE

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. INTR may be removed anytime after the falling edge of the first $\overline{INTA}$ signal. The interrupt return instruction includes a flags pop which returns the status of the original interrupt enable bit when it restores the flags.

Halt

When a software HALT instruction is executed, the processor indicates that it is entering the HALT state in one of two ways, depending upon which mode is strapped. In minimum mode, the processor issues ALE, delayed by one clock cycle, to allow the system to latch the halt status. Halt status is available on IO/$\overline{M}$, DT/$\overline{R}$, and $\overline{SS0}$. In maximum mode, the processor issues appropriate HALT status on $\overline{S2}$, $\overline{S1}$ and $\overline{S0}$, and the 82C88 bus controller issues one ALE. The 80C88 will not leave the HALT state when a local bus hold is entered while in HALT. In this case, the processor reissues the HALT indicator at the end of the local bus hold. An interrupt request or RESET will force the 80C88 out of the HALT state.

Read/Modify/Write (Semaphore) Operations Via $\overline{LOCK}$

The $\overline{LOCK}$ status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This allows the processor to perform read/modify/write operations on memory (via the "exchange register with memory" instruction), without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{LOCK}$ signal is activated (LOW) in the clock cycle following decoding of the $\overline{LOCK}$ prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the $\overline{LOCK}$ prefix. While $\overline{LOCK}$ is active, a request on a $\overline{RQ}/\overline{GT}$ pin will be recorded, and then honored at the end of the $\overline{LOCK}$.

External Synchronization Via $\overline{TEST}$

As an alternative to interrupts, the 80C88 provides a single software-testable input pin ($\overline{TEST}$). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the $\overline{TEST}$ input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the 80C88 three-states all output drivers while inputs and I/O pins are held at valid logic levels by internal bus-hold circuits. If interrupts are enabled, the 80C88 will recognize interrupts and process them when it regains control of the bus.

Basic System Timing

In minimum mode, the MN/$\overline{MX}$ pin is strapped to VCC and the processor emits bus control signals ($\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, etc.) directly. In maximum mode, the MN/$\overline{MX}$ pin is strapped to GND and the processor emits coded status information which the 82C88 bus controller uses to generate MULTIBUS™ compatible bus control signals.

System Timing - Minimum System

The read cycle begins in T1 with the assertion of the address latch enable (ALE) signal (See Figure 5). The trailing (low going) edge of this signal is used to latch the address information, which is valid on the address data bus (AD0-AD7) at this time, into the 82C82/82C83 latch. Address lines A8 through A15 do not need to be latched because they remain valid throughout the bus cycle. From T1 to T4 the IO/$\overline{M}$ signal indicates a memory or I/O operation. At T2 the address is removed from the address data bus and the bus is held at the last valid logic state by internal bus-hold devices. The read control signal is also asserted at T2. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again three-state its bus drivers. If a transceiver (82C86/82C87) is required to buffer the local bus, signals DT/$\overline{R}$ and $\overline{DEN}$ are provided by the 80C88.

A write cycle also begins with the assertion of ALE and the emission of the address. The IO/$\overline{M}$ signal is again asserted to indicate a memory or I/O write operation. In T2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T4. During T2, T3, and Tw, the processor asserts the write control signal. The write ($\overline{WR}$) signal becomes active at the beginning of T2, as opposed to the read, which is delayed somewhat into T2 to provide time for output drivers to become inactive.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge ($\overline{INTA}$) signal is asserted in place of the read ($\overline{RD}$) signal and the address bus is held at the last valid logic state by internal bus-hold devices (see Figure 6). In the second of two successive $\overline{INTA}$ cycles, a byte of information is read from the data bus, as supplied by the interrupt system logic (i.e., 82C59A priority interrupt controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into the interrupt vector lookup table, as described earlier.

Bus Timing - Medium Complexity Systems

For medium complexity systems, the MN/$\overline{MX}$ pin is connected to GND and the 82C88 bus controller is added to the system, as well as an 82C82/82C83 latch for latching the system address, and an 82C86/82C87 transceiver to allow for bus loading greater than the 80C88 is capable of handling (see Figure 8). Signals ALE, $\overline{DEN}$, and DT/$\overline{R}$ are generated by the 82C88 instead of the processor in this configuration, although their timing remains relatively the same. The 80C88 status outputs ($\overline{S2}$, $\overline{S1}$ and $\overline{S0}$) provide type of cycle information and become 82C88 inputs. This bus cycle information specifies read (code, data or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 82C88 thus issues control signals specifying memory

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

read or write, I/O read or write, or interrupt acknowledge. The 82C88 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The 82C86/82C87 tranceiver receives the usual T and $\overline{OE}$ inputs from the 82C88 DT/$\overline{R}$ and $\overline{DEN}$ outputs.

The pointer into the interrupt vector table, which is passed during the second $\overline{INTA}$ cycle, can derive from an 82C59A located on either the local bus or the system bus. If the master 82C59A priority interrupt controller is positioned on the local bus, the 82C86/82C87 transceiver must be disabled when reading from the master 82C59A during the interrupt acknowledge sequence and software "poll".

The 80C88 Compared To The 80C86

The 80C88 CPU is an 8 bit processor designed around the 8086 internal structure. Most internal functions of the 80C88 are identical to the equivalent 80C86 functions. The 80C88 handles the external bus the same way the 80C86 does with the distinction of handling only 8 bits at a time. Sixteen-bit operands are fetched or written in two consecutive bus cycles. Both processors will appear identical to the software engineer, with the exception of execution time. The internal register structure is identical and all instructions have the same end result. Internally, there are three differences between the 80C88 and the 80C86. All changes are related to the 8 bit bus interface.

- The queue length is 4 bytes in the 80C88, whereas the 80C86 queue contains 6 bytes, or three words. The queue was shortened to prevent overuse of the bus by the BIU when prefetching instructions. This was required because of the additional time necesssary to fetch instructions 8 bits at a time.
- To further optimize the queue, the prefetching algorithm was changed. The 80C88 BIU will fetch a new instruction to load into the queue each time there is a 1 byte space available in the queue. The 80C86 waits until a 2 byte space is available.

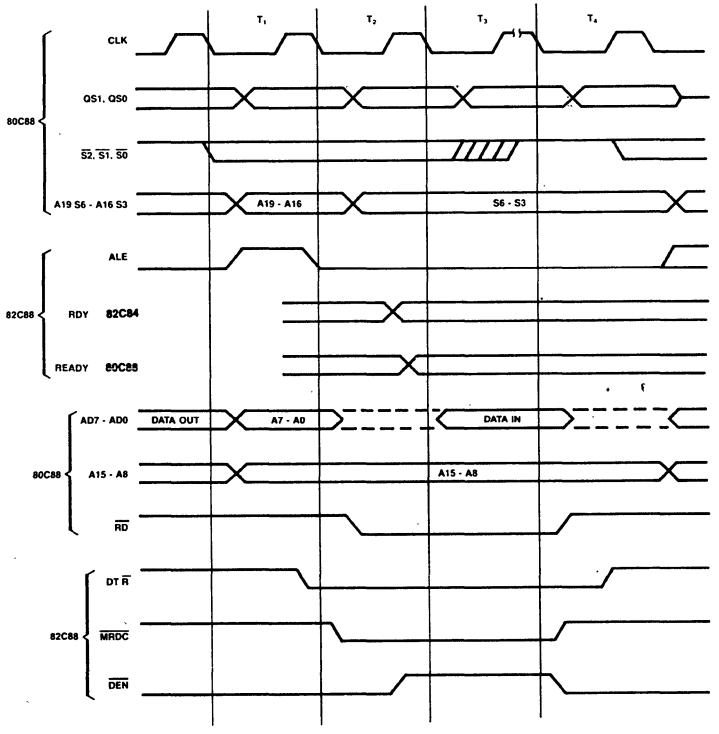


FIGURE 8. MEDIUM COMPLEXITY SYSTEM TIMING

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

- The internal execution time of the instruction set is affected by the 8 bit interface. All 16 bit fetches and writes from/to memory take an additional four clock cycles. The CPU is also limited by the speed of instruction fetches. This latter problem only occurs when a series of simple operations occur. When the more sophisticated instructions of the 80C88 are being used, the queue has time to fill and the execution proceeds as fast as the execution unit will allow.

The 80C88 and 80C86 are completely software compatible by virtue of their identical execution units. Software that is system dependent may not be completely transferable, but software that is not system dependent will operate equally as well on an 80C88 or an 80C86.

The hardware interface of the 80C88 contains the major differences between the two CPUs. The pin assignments are nearly identical, however, with the following functional changes:

- A8-A15: These pins are only address outputs on the 80C88. These address lines are latched internally and remain valid throughout a bus cycle in a manner similar to the 8085 upper address lines.
- $\overline{BHE}$ has no meaning on the 80C88 and has been eliminated.
- $\overline{SS0}$ provides the $\overline{S0}$ status information in the minimum mode. This output occurs on pin 34 in minimum mode only. DT/$\overline{R}$, IO/$\overline{M}$ and $\overline{SS0}$ provide the complete bus status in minimum mode.
- IO/$\overline{M}$ has been inverted to be compatible with the 8085 bus structure.
- ALE is delayed by one clock cycle in the minimum mode when entering HALT, to allow the status to be latched with ALE.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

INSTRUCTION SET SUMMARY

Mnemonic and Description	Instruction Code			
DATA TRANSFER				
MOV = Move:	76543210	76543210	76543210	76543210
Register/Memory to/from Register	100010dw	mod reg r/m		
Immediate to Register/Memory	1100011w	mod 000 r/m	data	data if w 1
Immediate to Register	1011 w reg	data	data if w 1	
Memory to Accumulator	1010000w	add-low	addr-high	
Accumulator to Memory	1010001w	addr-low	addr-high	
Register/Memory to Segment Register**	10001110	mod 0 reg r/m		
Segment Register to Register/Memory	10001100	mod 0 reg r/m		
PUSH = Push:				
Register/Memory	11111111	mod 110 r/m		
Register	01010 reg			
Segment Register	000 reg 110			
POP = Pop:				
Register/Memory	10001111	mod 000 r/m		
Register	01011 reg			
Segment Register	000 reg 111			
XCHG = Exchange:				
Register/Memory with Register	1000011w	mod reg r/m		
Register with Accumulator	10010 reg			
IN = Input from:				
Fixed Port	1110010w	port		
Variable Port	1110110w			
OUT = Output to:				
Fixed Port	1110011w	port		
Variable Port	1110111w			
XLAT = Translate Byte to AL	11010111			
LEA = Load EA to Register	10001101	mod reg r/m		
LDS = Load Pointer to DS	11000101	mod reg r/m		
LES = Load Pointer to ES	11000100	mod reg r/m		
LAHF = Load AH with Flags	10011111			
SAHF = Store AH into Flags	10011110			
PUSHF = Push Flags	10011100			
POPF = Pop Flags	10011101			

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

INSTRUCTION SET SUMMARY (Continued)

Mnemonic and Description	Instruction Code			
ARITHMETIC	76543210	76543210	76543210	76543210
ADD = Add:				
Reg./Memory with Register to Either	000000dw	mod reg r/m		
Immediate to Register/Memory	100000sw	mod 000 r/m	data	data if s:w = 01
Immediate to Accumulator	0000010w	data	data if w = 1	
ADC = Add with Carry:				
Reg./Memory with Register to Either	000100dw	mod reg r/m		
Immediate to Register/Memory	100000sw	mod 010 r/m	data	data if s:w = 01
Immediate to Accumulator	0001010w	data	data if w = 1	
INC = Increment:				
Register/Memory	1111111w	mod 000 r/m		
Register	01000reg			
AAA = ASCII Adjust for Add	00110111			
DAA = Decimal Adjust for Add	00100111			
SUB = Subtract:				
Reg./Memory and Register to Either	001010dw	mod reg r/m		
Immediate from Register/Memory	100000sw	mod 101 r/m	data	data if s:w = 01
Immediate from Accumulator	0010110w	data	data if w = 1	
SBB = Subtract with Borrow				
Reg./Memory and Register to Either	000110dw	mod reg r/m		
Immediate from Register/Memory	100000sw	mod 011 r/m	data	data if s:w = 01
Immediate from Accumulator	0001110w	data	data if w = 1	
DEC = Decrement:				
Register/Memory	1111111w	mod 001 r/m		
Register	01001 reg			
NEG = Change Sign	1111011w	mod 011 r/m		
CMP = Compare:				
Register/Memory and Register	001110dw	mod reg r/m		
Immediate with Register/Memory	100000sw	mod 111 r/m	data	data if s:w = 01
Immediate with Accumulator	0011110w	data	data if w = 1	
AAS = ASCII Adjust for Subtract	00111111			
DAS = Decimal Adjust for Subtract	00101111			
MUL = Multiply (Unsigned)	1111011w	mod 100 r/m		
IMUL = Integer Multiply (Signed)	1111011w	mod 101 r/m		
AAM = ASCII Adjust for Multiply	11010100	00001010		
DIV = Divide (Unsigned)	1111011w	mod 110 r/m		
IDIV = Integer Divide (Signed)	1111011w	mod 111 r/m		
AAD = ASCII Adjust for Divide	11010101	00001010		
CBW = Convert Byte to Word	10011000			
CWD = Convert Word to Double Word	10011001			

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

INSTRUCTION SET SUMMARY (Continued)

Mnemonic and Description	Instruction Code			
LOGIC	76543210	76543210	76543210	76543210
NOT = Invert	1111011w	mod010r/m		
SHL/SAL = Shift Logical/Arithmetic Left	110100vw	mod100r/m		
SHR = Shift Logical Right	110100vw	mod101r/m		
SAR = Shift Arithmetic Right	110100vw	mod111r/m		
ROL = Rotate Left	110100vw	mod000r/m		
ROR = Rotate Right	110100vw	mod001r/m		
RCL = Rotate Through Carry Flag Left	110100vw	mod010r/m		
RCR = Rotate Through Carry Right	110100vw	mod011r/m		
AND = **And:**				
Reg./Memory and Register to Either	001000dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod100r/m	data	data if w = 1
Immediate to Accumulator	0010010w	data	data if w = 1	
TEST = **And Function to Flags, No Result:**				
Register/Memory and Register	1000010w	mod reg r/m		
Immediate Data and Register/Memory	1111011w	mod000r/m	data	data if w = 1
Immediate Data and Accumulator	1010100w	data	data if w = 1	
OR = **Or:**				
Reg./Memory and Register to Either	000010dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod001r/m	data	data if w = 1
Immediate to Accumulator	0000110w	data	data if w = 1	
XOR = **Exclusive or:**				
Reg./Memory and Register to Either	001100dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod110r/m	data	data if w = 1
Immediate to Accumulator	0011010w	data	data if w = 1	
STRING MANIPULATION				
REP = Repeat	1111001z			
MOVS = Move Byte/Word	1010010w			
CMPS = Compare Byte/Word	1010011w			
SCAS = Scan Byte/Word	1010111w			
LODS = Load Byte/Wd to AL/AX	1010110w			
STOS = Stor Byte/Wd from AL/A	1010101w			
CONTROL TRANSFER				
CALL = **Call:**				
Direct Within Segment	11101000	disp-low	disp-high	
Indirect Within Segment	11111111	mod010r/m		
Direct Intersegment	10011010	offset-low	offset-high	
		seg-low	seg-high	
Indirect Intersegment	11111111	mod011r/m		

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

INSTRUCTION SET SUMMARY (Continued)

Mnemonic and Description	Instruction Code		
JMP = Unconditional Jump:	76543210	76543210	76543210
Direct Within Segment	11101001	disp-low	disp-high
Direct Within Segment-Short	11101011	disp	
Indirect Within Segment	11111111	mod 100 r/m	
Direct Intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect Intersegment	11111111	mod 101 r/m	
RET = Return from CALL:			
Within Segment	11000011		
Within Seg Adding Immed to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment Adding Immediate to SP	11001010	data-low	data-high
JE/JZ = Jump on Equal/Zero	01110100	disp	
JL/JNGE = Jump on Less/Not Greater or Equal	01111100	disp	
JLE/JNG = Jump on Less or Equal/ Not Greater	01111110	disp	
JB/JNAE = Jump on Below/Not Above or Equal	01110010	disp	
JBE/JNA = Jump on Below or Equal/ Not Above	01110110	disp	
JP/JPE = Jump on Parity/Parity Even	01111010	disp	
JO = Jump on Overflow	01110000	disp	
JS = Jump on Sign	01111000	disp	
JNE/JNZ = Jump on Not Equal/Not Zero	01110101	disp	
JNL/JGE = Jump on Not Less/Greater or Equal	01111101	disp	
JNLE/JG = Jump on Not Less or Equal/ Greater.	01111111	disp	
JNB/JAE = Jump on Not Below/Above or Equal	01110011	disp	
JNBE/JA = Jump on Not Below or Equal/Above	01110111	disp	
JNP/JPO = Jump on Not Par/Par Odd	01111011	disp	
JNO = Jump on Not Overflow	01110001	disp	
JNS = Jump on Not Sign	01111001	disp	
LOOP = Loop CX Times	11100010	disp	
LOOPZ/LOOPE = Loop While Zero/Equal	11100001	disp	
LOOPNZ/LOOPNE = Loop While Not Zero/Equal	11100000	disp	
JCXZ = Jump on CX Zero	11100011	disp	
INT = Interrupt			
Type Specified	11001101	type	
Type 3	11001100		
INTO = Interrupt on Overflow	11001110		
IRET = Interrupt Return	11001111		

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

INSTRUCTION SET SUMMARY (Continued)

Mnemonic and Description	Instruction Code	
	76543210	76543210
PROCESSOR CONTROL		
CLC = Clear Carry	11111000	
CMC = Complement Carry	11110101	
STC = Set Carry	11111001	
CLD = Clear Direction	11111100	
STD = Set Direction	11111101	
CLI = Clear Interrupt	11111010	
STI = Set Interrupt	11111011	
HLT = Halt	11110100	
WAIT = Wait	10011011	
ESC = Escape (to External Device)	11011xxx	mod x x x r/m
LOCK = Bus Lock Prefix	11110000	

NOTES:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction
if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16 bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)
*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.
**MOV CS, REG/MEMORY not allowed.
if s:w = 01 then 16 bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:
FLAGS =
X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

APPNOTE

No. 111 April 1988

Harris Digital

HARRIS 80C286 PERFORMANCE ADVANTAGES OVER THE 80386

Author: Ted Dimbero

The Harris 80C286, operating at the same frequency as the 80386, has performance advantages over the 80386 when executing 16-bit industry standard 80C86 or 80C286 code. This is evident in the following areas:

(1) Input/Output Handling

(2) Interrupt Handling

(3) Control Transfer (Loop, Jump, Call)

(4) 286 Protected Mode Systems

(5) Multi-Tasking and Task Switching Operations.

This advantage is due to the 80C286 requirement of fewer clock cycles to execute the same instructions. In addition to these areas, the 80C286 executes many other instructions in the same number of clock cycles as the 80386.

This results in an 80C286 performance advantage in areas including:

- Multi-Tasking Systems.
- Control Applications — utilizing interrupt and I/O instructions.
- Structured Software — utilizing many Control transfer instructions.
- Operating Systems that rely on interrupts to perform functions.
- Upgrading 16-bit 80C86 applications for increased performance.

The 80C286 can be effectively used as a fast 80C86. However, the 80386 is not a fast 80C286. This study shows that software written for the 80C86/80C286 can execute more efficiently on the 80C286 than on the 80386. There is no significant performance advantage to be gained by simply moving a system design from an 80C286 to an 80386 at either 16MHz or 20MHz. The 80C286 is the processor best suited for executing 16-bit 80C86/80C286 code, which represents the world's largest base of microprocessor software.

Architecture Background

The 80C286 Harris' newest static CMOS microprocessor combines low operating and standby power with high performance. The Harris 80C286 is available in speeds of 12.5MHz, 16MHz, and 20MHz.

The 80C286 evolved from the industry standard 80C86 microprocessor. The 80C286 has vast architectural enhancements over its predecessor that allow the 80C286 to execute the same code with a significant performance increase. Disregarding the clock speed increase, when upgrading from an 80C86 to an 80C286, the 80C286 can execute the same code with an increase in throughput of up to 4 times that of the 80C86. This increase is solely due to the architectural enhancements.

It is a common belief that replacing an 80C286 with the 32-bit 80386 microprocessor will yield similar performance increases. This is not the case. The new architecture gives the 80386 32-bit capability and increased protection features, but it does not significantly increase the throughput of 16-bit 8086 or 80286 code. In most cases, when executing industry standard 8086 or 80286 code, replacing the 80C286 with an 80386 does not result in a significant performance increase. In some cases, such a replacement will actually cause a performance degradation.

Figure 1 illustrates a comparison of the number of clock cycles needed to execute several instructions available on all three microprocessors (80C86, 80C286, and 80386). This illustrates the dramatic effect of 80C286 architectural enhancements on performance when compared to the 80C86 and the lack of similar performance improvement when executing 8086/80286 code on the 80386.

With an 80C86 to 80C286 upgrade, system designers can execute existing 8086 code on the 80C286 and take advantage of an immediate performance upgrade. This same benefit is not realized when switching from an 80C286 to an 80386. This comparison illustrates that changing from an 80C286 to an 80386 does

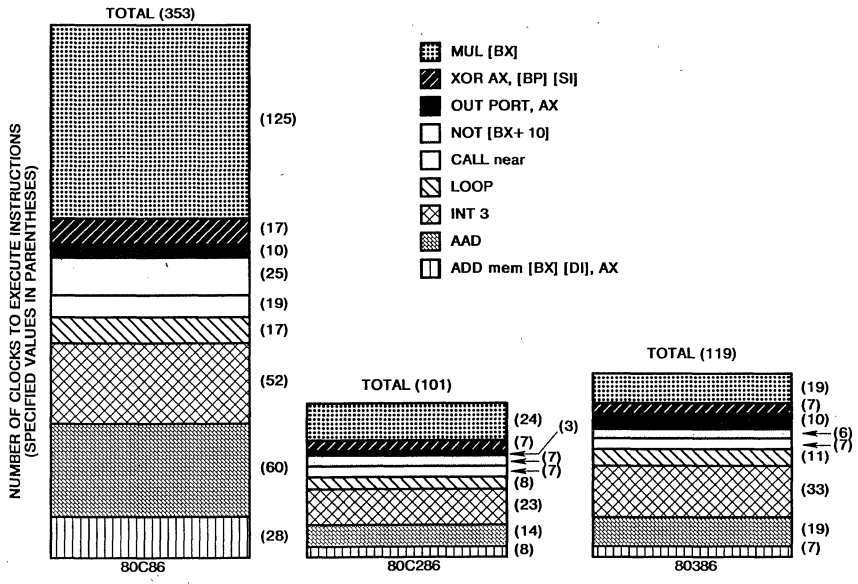


FIGURE 1. ARCHITECTURAL COMPARISON

not yield increased throughput when executing the same industry standard 80C86/80C286 code (the world's largest base of microprocessor software).

Instruction Comparison

The Appendix in this document illustrates a direct comparison of the number of clock cycles needed to execute the same instructions on the 80C286 and the 80386. The table includes examples of instruction timing for all instructions available on both processors. Several addressing modes of each instruction type are included.

Of the 190 instruction examples analyzed, 74 of the instructions execute faster on the 80C286 than on the 80386; 66 of the instructions analyzed execute in the same number of clock cycles on both processors. This leaves only 50 instructions with improved performance on the 80386 (See Figure 2). Over 70% of the instructions analyzed execute as fast or faster on the 80C286 than on the 80386.

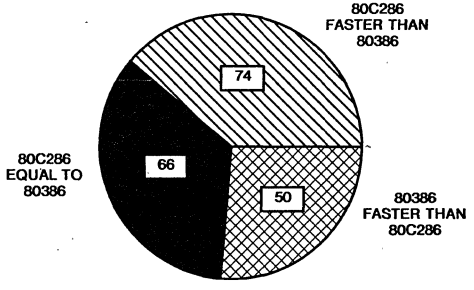


FIGURE 2. EXECUTION SPEED COMPARISON (NUMBER OF INSTRUCTIONS)

This is vastly different than the previous 86-286 upgrade. With that upgrade, the 80C286 exhibits equal or better performance than the 80C86 with 100% of the instructions. This clearly indicates that the 80C286 is the processor best suited for executing industry standard 8086 family code.

The following discussion groups each of the instructions into one of several categories to analyze which applications will benefit from utilizing the 80C286. The categories used are:

- Jumps, Calls, Returns and Loops (Real Mode).
- I/O Instructions.
- Logic, Arithmetic, Data Transfer, Shift and Rotate Instructions.
- Interrupts.
- Miscellaneous Instructions.
- Protected Mode/Multi-Tasking Instructions.

Jumps, Calls and Loops

In real mode, near calls, jumps, and conditional jumps (transfers within the current code segment) all take the same number of clock cycles to execute on the 80C286 and the 80386. Since the segment sizes are larger on the 80386, the near transfer instructions on the 80386 can transfer a greater distance.

The far calls and jumps (transfers that switch to a new code segment; i.e., a code segment context switch) are faster on the 80C286: four clocks and one clock respectivley. The far return instruction executes in three less clock cycles on the 80C286, and the near return takes one extra clock cycle. The protected mode calls, jumps, and returns are all faster

on the 80C286 and are discussed in the section on Protected Mode.

The loop instruction is three clock cycles faster on the 80C286 than the 80386. Thus, the 80C286 would save 300 clock cycles over the 386 if a LOOP instruction were executed 100 times.

INSTRUCTION	— ADVANTAGE —		
	80C286	NONE	80386
Near JMP and CALL		X	
Far CALL, JMP and RET	X		
LOOP	X		

I/O Instructions

The 80C286 has a significant advantage with the I/O instructions. The IN instruction is almost 2 1/2 times faster on the 80C286; the 80386 takes 7 extra clock cycles to execute the same instruction. The OUT instruction is over 3 times faster on the 80C286; again the 80386 takes 7 extra clock cycles to execute the same instruction. Executing the I/O instructions on the 80386 is equivalent to executing on the 80C286 with 7 wait states.

The string I/O instructions (INS and OUTS) are also significantly faster on the 80C286. The INS instruction is 10 clock cycles faster on the 80C286, and the OUTS instruction is 9 clock cycles faster. This is particularly important if the string operations are going to be used to input or output a large block of data using the REP prefix. Inputing 100 words of data with the REP INS instruction is 208 clock cycles faster on the 80C286. An even more significant difference can be seen when outputing 100 words with the REP OUTS instruction. In this case, the 80C286 is 800 clock cycles faster than the 80386.

INSTRUCTION	— ADVANTAGE —		
	80C286	NONE	80386
IN	X		
OUT	X		
INS	X		
OUTS	X		

Logic, Arithmetic, Data Transfer, Shift and Rotate Instructions

Most forms of the logic, arithmetic, and data transfer instructions execute in the same number of clock cycles on both processors. Certain operand combinations of these instructions (immediate to register for example) take one extra clock cycle to execute on the 80C286.

In real mode, the segment register transfer instructions execute as fast or faster on the 80C286 than they do on the 80386. For example, using the POP instruction to transfer data into a segment register is 2 clock cycles faster on the 80C286.

Most of the string manipulation instructions execute in the same number of clock cycles on both processors. The MOVS and STOS instructions are faster on the 80C286.

The divide instruction executes in the same number of clock cycles on both processors. The number of clocks to execute the multiply instruction on the 80386 is data dependent; the number of clocks to execute the same instruction on the 80C286 is fixed. On average, the multiply instruction is five clock cycles faster on the 80386, but depending on the data, the 80386 could be as many as 4 clock cycles slower than the 80C286.

The rotate and shift instructions are faster on the 80386. Unlike the 80C286, the 80386 rotate and shift instructions do not depend on the number of bits to be shifted or rotated. Thus, the 80386 has the advantage with multi-bit rotate and shift instructions. The 80C286 does, however, execute single bit rotate and shift instructions faster.

INSTRUCTION	— ADVANTAGE —		
	80C286	NONE	80386
Most Logic and Arithmetic		X	
Certain Operand Combinations of Logic and Arithmetic			X
Divide		X	
Multiply			X
Single Bit Shift or Rotate	X		
Multi-Bit Shift or Rotate			X
String Instructions	X		

Interrupt Instructions

Interrupts are serviced more quickly on the 80C286. The INT instruction, in real mode, executes 14 cycles faster on the 80C286 than it does on the 80386. The INTO, BOUND, and other instructions that can cause an interrupt all benefit from the faster interrupt handling features of the 80C286. The return from interrupt instruction (IRET) is 7 clock cycles faster on the 80C286. The PUSHA and POPA instructions, frequently used by interrupt handling procedures, are both faster on the 80C286. Protected Mode interrupt handling is discussed in the Protected Mode section.

INSTRUCTION	— ADVANTAGE —		
	80C286	NONE	80386
INT n	X		
INTO	X		
BOUND (If Interrupt)	X		
Break Point Interrupt	X		

Miscellaneous Instructions

The BCD instructions, HLT, and CBW execute from 1 to 5 clock cycles faster on the 80C286. The instructions to set and clear individual flags and the CWD instruction all execute in the same number of cycles on both processors. The ENTER, LEAVE, and BOUND instructions are from 1 to 3 cycles faster on the 80386. The BOUND instruction is only faster if an interrupt is not caused by the instruction.

INSTRUCTION	— ADVANTAGE —		
	80C286	NONE	80386
BCD Instructions	X		
Data Conversion (CBW, CWD)	X		
Flag Settling and Clearing		X	
BOUND (If No Interrupt)			X

Protected Mode/Multi-Tasking

When executing 80286 protected mode code, the 80C286 significantly out-performs the 80386. Task switching operations execute 100 to 113 clock cycles faster on the 80C286. The instruction to return from a called task is 63 clock cycles faster on the 80C286. This results in a very significant performance increase for systems utilizing the multi–tasking features.

Inter-segment JMP, CALL and segment loading instructions also operate faster on the 80C286. The 80C286 saves anywhere from 4 to 11 clock cycles depending on the particular inter-segment transfer instruction. In protected mode, the inter-segment return is also faster on the 80C286. The 80C286 is 7 clock cycles faster when executing an inter-segment return to the same privilege level and is 13 cycles faster on inter–segment returns to a different privilege level.

The instructions to initialize and check the protected mode registers execute as fast or faster on the 80C286. The IDTR access instructions are an exception to this in that they take one extra clock cycle to execute on the 80C286. The instruction to switch the processor to protected mode (LMSW) is 7 cycles faster on the 80C286.

Most of the 80286 protected mode access checking instructions operate as fast or faster on the 80C286 than on the 80386. The LAR instruction is one clock cycle faster on the 80C286 and the LSL instruction is 5 clock cycles faster. The VERW instruction executes in the same speed on both processors and the VERR is 5 cycles faster on the 80386. The ARPL instruction used in protected mode procedures for pointer validation is 10 clock cycles faster on the 80C286.

INSTRUCTION	— ADVANTAGE —		
	80C286	NONE	80386
Task Switching	X		
Segment Register Loading	X		
Inter-Segment Transfer	X		
System Register Instructions		X	
Inter-Segment Transfers	X		
Access Checking Instructions		X	

Subroutine Analysis

This section lists several subroutines and then compares the number of clock cycles each subroutine will take to execute on the 80C286 and on the 80386.

EXAMPLE 1

This interrupt routine outputs a character to a terminal via a UART. The AL register must contain the character to be output. The routine first checks the status of the UART to determine if it is busy. If it is busy, the routine loops until the UART is free; when the UART is free, the character is output. Following is a listing of the code and the clock clycle analysis for the OUT_CHAR routine.

This sample procedure executes about 25% faster on the 80C286 than on the 386. The advantage is realized through the 80C286's faster interrupt handling and faster I/O instructions.

80C286 CLOCK CYCLES	80386 CLOCK CYCLES	OUT_CHARACTER PROC NEAR		
3	4		PUSHF	; save callers flags.
3	2		PUSH AX	; save data to be output.
5	12	CK_STATUS:	IN AL, PORT_STATUS	; Input UART status.
6	5		CMP AL, BUSY	; Check If UART Busy
3/7	3/7		JE CK_STATUS	; If busy go check again.
5	4		POP AX	; If not busy restore AX
3	10		OUT OUT_PORT, AL	; and output data.
5	5		POPF	; Restore Flags
17	22		IRET	; Return.
23	37		INT x	; Instruction to initiate OUTCHAR ; Interrupt.
73	104	Total cycles if UART not busy.		
18	24	Number of cycles added for each loop while UART is busy.		

EXAMPLE 1

EXAMPLE 2

The second example outputs an entire string of characters using the previous interrupt routine (denoted by "INT x" in the code below). The DS:SI registers point to the beginning of the string to be output. The string is variable in length and must be terminated with the "$" character.

80C286 CLOCK CYCLES	80386 CLOCK CYCLES	OUT_STRING PROC FAR		
17	18		PUSHA	; save caller's registers.
5	5	NEXT:	LODSB	; Load first char to be output.
3	2		CMP AL, "$"	; Check to see if End of string.
3/7	3/7		JE done	; If end then goto DONE.
73	104		INT x	; If not end output character.
7	7		JMP next	; Go get next char to output.
19	24	DONE:	POPA	; Restore Registers when done.
15	18		RET	; Far Return.
13	17		Call OUT_STRING	; Far Call to initiate ; OUT_STRING procedure.
79+91/char	91+121/char	Total number of clocks to start and end routine. +Number of additional clocks to output each character in the output string		

To output a string of 20 characters, the 80C286 would take 1,899 clock cycles; using the same routine, the 80386 would take 2,511 cycles. Each time a string of 20 characters is output, the 80C286 will save 612 clock cycles; an 80C286 performance increase of almost 25%. The advantage is realized through the 80C286's faster interrupt handling, faster I/O instructions, faster FAR transfer instructions and faster register saving and restoring instructions.

EXAMPLE 3

This example adds all the values of a source array in memory to the values of a destination array in memory. The result is stored in the destination array. Both arrays are assumed to be in the current data segment. The count (number of words in the array), offset of source array, and offset of destination array are all assumed to be placed on the stack (in that order) by the calling program. The source code for the procedure is listed below:

80C286 CLOCK CYCLES	80386 CLOCK CYCLES	ADD_ARRAY PROC NEAR		
17	18		PUSHA	; Save caller's registers.
2	2		MOV BP, SP	; Point BP to current stack
5	4		MOV CX, [bp+22]	; Load array size from stack ; into CX.
5	4		MOV SI, [bp+20]	; Load offset of source array ; from stack into SI.
5	4		MOV DI, [bp+18]	; Load offset of destination ; array from stack into DI.
2	2		CLD	; Clear Direction Flag.
5	5	NEXT:	LODSW	; Load the source word into AX.
7	7		ADD [DI], AX	; Add source to destination.
3	2		ADD DI, 02	; Point DI to next data.
8/4	11		LOOP NEXT	; Continue to ADD all elements ; in the two arrays.
19	24		POPA	; Restore Registers
11	10		RET 6	; Near return.
		; Following is the code necessary to set up and call the above procedure.		
5	5		PUSH count	; Put count parameter on stack
3	2		PUSH offset S_ARRAY	; Put offset of source array ; on stack.
3	2		PUSH offset D_ARRAY	; Put offset of destination ; array on stack.
7	7		CALL ADD_ARRAY	; Near Call to initiate ; ADD_ARRAY procedure.
84+(23*CX)–4	84+(25*CX)	Total number of clocks to start and end routine. +Number of additional clocks for each item in array to be added.		

Both processors take the same number of clock cycles for initialization before the call and closing up after the call (84). The loop that does the adding is faster on the 80C286. To add two 100 word arrays, the 80C286 would take 2,380 clock cycles; the 80386 takes 2,584 (an additional 204 clocks) to execute the same routine. In this example, the LOOP instruction gives the 80C286 the performance advantage over the 80386.

EXAMPLE 4

This procedure is an example of an operating system procedure developed for a protected mode multi-privilege level system. The procedure INIT_SEGMENT is passed a segment selector on the stack and will load that entire segment with zero's. The procedure is designed to execute at privilege level zero with a call gate at privilege level 3; this allows procedures executing at any level to utilize the INIT_SEGMENT procedure. INIT_SEGMENT provides protection checks to ensure that the procedure passing the parameter has valid access to the segment that it is trying to initialize. This prevents a procedure at privilege level three from initializing a segment at privilege level zero.

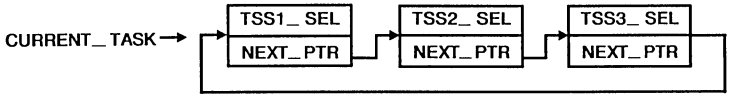
80C286 CLOCK CYCLES	80386 CLOCK CYCLES	INIT_SEGMENT PROC FAR WC=1		
17	18		PUSHA	; save caller's registers.
3	2		PUSH ES	; save ES register.
2	2		MOV BP, SP	; Point BP to top of stack.
5	4		MOV AX, [BP+22]	; Load AX with segment selector
				; passed as parameter on stack.
5	4		MOV BX, [BP+20]	; Load BX with return CS to
				; determine caller's CPL.
10	20		ARPL AX, BX	; Adjust the Privilege level of
				; the segment selector according
				; to the caller's CPL.
16	16		VERW AX	; Test for valid write access
3/7	3/7		JNE ERROR	; If no valid access goto error.
17	18		MOV ES, AX	; LOAD ES with segment to be
				; initialized.
14	20		LSL CX, AX	; Load segment size into CX.
2	2		XOR DI, DI	; Load zero into DI.
2	2		XOR AX, AX	; Load zero into AX.
2	2		CLD	; Clear decrement flag.
4+3*cx	5+5*cx		REP STOSB	; Init entire segment to 00.
2	2		CLC	; Clear carry to indicate segment
				; initialized with no errors.
20	21	DONE:	POP ES	; Restore ES register.
19	24		POPA	; Restore Register
55	68		RET 2	; Ret FAR to different privilege
2	2	ERROR:	STC	; SET carry to indicate error.
7	7		JMP DONE	
		; Code to push selector on stack and initiate INIT SEGMENT via call gate.		
3	2		PUSH DATA_SELECTOR	; Place Selector on stack.
82	86		CALL INIT_SEGMENT_GATE	; Instruction to initiate
				; INIT SEGMENT procedure.
253	283	Total clocks if ERROR because segment not accessible.		
283+(3*S)	321+(5*S)	Total number of clocks if segment is initialized to zeros. "S" represents size of segment in bytes.		

This example shows that when executing instructions used for privilege verification and privilege level transitions the 80C286 is faster than the 80386. Without taking the LODS instruction into account, the 80C286 is 38 clock cycles faster when executing the same procedure. With the LODS instruction, and assuming a segment size of 100 bytes, the 80C286 would execute this routine 238 clock cycles faster than the 80386.

EXAMPLE 5

This Procedure is a task dispatcher that is invoked via an interrupt to cause a task switch to occur. This procedure utilizes a circular linked list of the tasks that need to be executed. A pointer called "CURRENT_TASK" points to the data structure for the current task being executed. The data structure contains the TSS for the task it is describing and a NEXT field that points to the data structure of the next task in the list to be executed. When the Task Dispatcher is invoked it switches the current pointer to the next task in the list and then invokes the new task by jumping to the TSS for that task. The data structure for the linked list is illustrated below.

The task dispatcher is actually a separate task that is invoked via an interrupt that signals that a new task should be initiated. Following is a listing for the simple task dispatcher.



80C286 CLOCK CYCLES	80386 CLOCK CYCLES	TASK_DISPATCH PROC FAR		
5	4	START:	MOV BX, CURRENT TASK + 2	; Load BX with contents of next ; field of current TASK. BX will ; contain the address of the data ; structure for next task to run.
3	2		MOV CURRENT TASK, BX	; Update Current Task to point to ; new task to be executed.
178	279		JMP DWORD PTR [BX-2]	; Start new task by jumping to TSS ; for new task.
7	7		JMP START	; JUMP to start for next time the ; TASK dispatcher is invoked.
193	292			

The advantage of the 80C286 in this case is in the faster task switch instruction. The task switch instruction is 101 clock cycles faster on the 80C286 than on the 80386. This performance increase makes the 80C286 the clear choice for muti-tasking applications.

Appendix

This appendix contains a table directly comparing the number of clock cycles necessary to execute all the instructions available on both the 80C286 and the 80386. The table includes several addressing modes of each instruction.

The table has five columns. The first column list the instruction being compared. The second column lists the number of clock cycles that the 80C286 needs to execute that instruction. The third column lists the number of clock cycles needed by the 80386 to execute the same instruction. The fourth column divides the number of cycles needed by the 80386 by the number of cycles needed by the 80C286. If this figure is greater than one, (see fifth column) then the 80C286 is faster than the 80386. For example, a 2.0 would indicate the 80C286 executes the same instruction twice as fast as the 80386. A 1.0 indicates that both processors execute the instruction in the same number of cycles. A number less than one indicates the 80386 is faster than the 80C286.

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386	80386/ 80C286	80C286 FASTER THAN OR EQUAL TO 80386
AAA	3	4	1.33	✓
AAD	14	19	1.36	✓
AAM	16	17	1.06	✓
AAS	3	4	1.33	✓
ADC reg, reg	2	2	1.00	✓
ADC mem, reg	7	7	1.00	✓
ADC reg, immed	3	2	0.67	
ADC mem, immed	7	7	1.00	✓
ADD reg, reg	2	2	1.00	✓
ADD mem, reg	7	7	1.00	✓
ADD reg, immed	3	2	0.67	
ADD mem, immed	7	7	1.00	✓
AND reg, reg	2	2	1.00	✓
AND mem, reg	7	7	1.00	✓
AND reg , immed	3	2	0.67	
AND mem, immed	7	7	1.00	✓
ARPL reg, reg	10	20	2.00	✓
ARPL mem, reg	11	21	1.91	✓
BOUND (no interrupt)	13	10	0.77	
CALL immed (near)	7	7	1.00	✓
CALL immed (far real mode)	13	17	1.31	✓
CALL immed (far PVAM)	26	34	1.31	✓
CALL gate (same privilege PVAM)	41	52	1.27	✓
CALL gate (different privilege PVAM)	82	86	1.05	✓
CALL TSS (Task Switch PVAM)	177	278	1.57	✓
CALL task_gate (Task Switch PVAM)	182	287	1.58	✓
CBW	2	3	1.50	✓
CLC	2	2	1.00	✓
CLD	2	2	1.00	✓
CLI	3	3	1.00	✓
CLTS	2	5	2.50	✓
CMC	2	2	1.00	✓
CMP reg, reg	2	2	1.00	✓
CMP mem, reg	6	5	0.83	
CMP reg, immed	3	2	0.67	
CMP mem, immed	6	5	0.83	
CMPS	8	10	1.25	✓
CWD	2	2	1.00	✓

Appendix (Continued)

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386	80386/ 80C286	80C286 FASTER THAN OR EQUAL TO 80386
DAA	3	4	1.33	✓
DAS	3	4	1.33	✓
DEC reg	2	2	1.00	✓
DEC mem	7	6	0.86	
DIV word, reg	22	22	1.00	✓
DIV word, mem	25	25	1.00	✓
ENTER immed1, immed2 (immed 2 = 6)	36	35	0.97	
HLT	2	5	2.50	✓
IDIV word, reg	25	27	1.08	✓
IMUL word, mem	24	19	0.79	
IN	5	12	2.40	✓
INC reg	2	2	1.00	✓
INC mem	7	6	0.86	
INS	5	15	3.00	✓
INT 3 (real mode)	23	33	1.43	✓
INT immed (real mode)	23	37	1.61	✓
INT immed (PVAM same privilege)	40	59	1.48	✓
INT immed (PVAM different privilege)	78	99	1.27	✓
INT TASK_GATE (PVAM Task Switch)	167	280	1.68	✓
INTO (No Jump)	3	3	1.00	✓
INTO (Yes Jump real mode)	24	35	1.46	✓
IRET (real mode)	17	22	1.29	✓
IRET (PVAM same privilege)	31	38	1.23	✓
IRET (PVAM different privilege)	55	82	1.49	✓
IRET (PVAM task switch)	169	232	1.37	✓
Jcond label (No jump)	3	3	1.00	✓
Jcond label (Yes jump)	7	7	1.00	✓
JMP near_label	7	7	1.00	✓
JMP Far_label (real mode)	11	12	1.09	✓
JMP FAR_LABEL (PVAM)	23	27	1.17	✓
JMP CALL_GATE (PVAM same privilege)	38	45	1.18	✓
JMP TASK_GATE (PVAM task switch)	183	288	1.57	✓
JMP TSS (PVAM task switch)	178	279	1.57	✓
LAHF	2	2	1.00	✓
LAR reg	14	15	1.07	✓
LAR mem	16	16	1.00	✓
LDS (real mode)	7	7	1.00	✓
LDS (PVAM)	21	22	1.05	✓
LEA	3	2	0.67	
LEAVE	5	4	0.80	
LGDT	11	11	1.00	✓
LIDT	12	11	0.92	
LLDT reg	17	20	1.18	✓
LLDT mem	19	20	1.05	✓
LMSW reg	3	10	3.33	✓
LMSW mem	6	13	2.17	✓
LODS	5	5	1.00	✓
LOOP (Jump)	8	11	1.38	✓
LOOP (No Jump)	4	11	2.75	✓

Appendix (Continued)

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386	80386/ 80C286	80C286 FASTER THAN OR EQUAL TO 80386
LSL reg	14	20	1.43	✓
LSL mem	16	21	1.31	✓
LTR reg	17	23	1.35	✓
LTR mem	19	27	1.42	✓
MOV reg, reg	2	2	1.00	✓
MOV mem, reg	3	2	0.67	
MOV reg, immed	2	2	1.00	✓
MOV mem, immed	3	2	0.67	
MOV seg__reg, reg (real mode)	2	2	1.00	✓
MOV seg__reg, mem (real mode)	5	5	1.00	✓
MOV seg__reg, reg (PVAM)	17	18	1.06	✓
MOV seg__reg, mem (PVAM)	19	19	1.00	✓
MOVS	5	7	1.40	✓
MUL reg	21	15	0.71	✓
NEG reg	2	2	1.00	✓
NEG mem	7	6	0.86	
NOP	3	3	1.00	✓
NOT reg	2	2	1.00	✓
NOT mem	7	6	0.86	
OR reg, reg	2	2	1.00	✓
OR mem, reg	7	6	0.86	
OR reg, immed	3	2	0.67	
OR mem, immed	7	7	1.00	✓
OUT	3	10	3.33	✓
OUTS	5	14	2.80	✓
POP reg	5	4	0.80	
POP mem	5	5	1.00	✓
POP seg__reg (real mode)	5	7	1.40	✓
POP seg__reg (PVAM)	20	21	1.05	✓
POPA	19	24	1.26	✓
POPF	5	5	1.00	✓
PUSH reg	3	2	0.67	
PUSH mem	5	5	1.00	✓
PUSH seg__reg	3	2	0.67	
PUSHA	17	18	1.06	✓
PUSHF	3	4	1.33	✓
RCR or RCL reg, 1	2	9	4.50	✓
RCR or RCL mem, 1	7	10	1.43	✓
RCR or RCL reg, cl (cl = 4)	9	9	1.00	✓
RCR or RCL mem, cl (cl = 4)	12	10	0.83	
RCR or RCL reg, 4	9	9	1.00	✓
RCR or RCL mem, 4	12	10	0.83	
ROR or ROL reg, 1	2	3	1.50	✓
ROR or ROL mem, 1	7	7	1.00	✓
ROR or ROL reg, cl (cl = 4)	9	3	0.33	
ROR or ROL mem, cl (cl = 4)	12	7	0.58	
ROR or ROL reg, 4	9	3	0.33	
ROR or ROL mem, 4	12	7	0.58	

Appendix (Continued)

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386	80386/ 80C286	80C286 FASTER THAN OR EQUAL TO 80386
REP INS (cx = 100)	405	613	1.51	✓
REP MOVS (cx = 100)	405	405	1.00	✓
REP OUTS (cx = 100)	405	1205	2.98	✓
REP STOS (cx = 100)	304	505	1.66	✓
REP CMPS (cx = 100)	905	905	1.00	✓
REPE CMPS (N = 100)	905	905	1.00	✓
REPE SCAS (N = 100)	805	805	1.00	✓
RET (near)	11	10	0.91	
RET (far real mode)	15	18	1.20	✓
RET (far PVAM same privilege)	25	32	1.28	✓
RET (far PVAM different privilege)	55	68	1.24	✓
SAHF	2	3	1.50	✓
SHIFT reg, 1 (SHIFT = SAL, SAR, SHR)	2	3	1.50	✓
SHIFT mem, 1	7	7	1.00	✓
SHIFT reg, cl (cl = 4)	9	3	0.33	
SHIFT mem, cl (cl = 4)	12	7	0.58	
SHIFT reg, 4	9	3	0.33	
SHIFT mem, 4	12	7	0.58	
SBB reg, reg	2	2	1.00	✓
SBB mem, reg	7	6	0.86	
SBB reg, immed	3	2	0.67	
SBB mem, immed	7	7	1.00	✓
SCAS	7	7	1.00	✓
SGDT	11	9	0.82	
SIDT	12	9	0.75	
SLDT reg	2	2	1.00	✓
SLDT mem	3	2	0.67	
SMSW reg	2	2	1.00	✓
SMSW mem	3	2	0.67	
STS	2	2	1.00	✓
STD	2	2	1.00	✓
STI	2	3	1.50	✓
STOS	3	4	1.33	✓
STR reg	2	23	11.50	✓
STR mem	3	27	9.00	✓
SUB reg, reg	2	2	1.00	✓
SUB mem, reg	7	6	0.86	
SUB reg, immed	3	2	0.67	
SUB mem, immed	7	7	1.00	✓
TEST reg, reg	2	2	1.00	✓
TEST mem, reg	6	5	0.83	
TEST reg, immed	3	2	0.67	
TEST mem, immed	6	5	0.83	
VERR reg	14	10	0.71	
VERR mem	16	11	0.69	
VERW reg	14	15	1.07	✓
VERW reg	16	16	1.00	✓

Appendix (Continued)

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386	80386/ 80C286	80C286 FASTER THAN OR EQUAL TO 80386
WAIT	3	6	2.00	✓
XCHG reg, reg	3	3	1.00	✓
XCHG reg, mem	5	5	1.00	✓
XLAT	5	5	1.00	✓
XOR reg, reg	2	2	1.00	✓
XOR mem, reg	7	6	0.86	
XOR reg, immed	3	2	0.67	
XOR mem, immed	7	7	1.00	✓
TOTAL number clocks to execute all instructions	6978	9048		
AVERAGE			1.24	
Number of Instructions faster on 80C286		74		
Number of Instructions equal on both processors		66		
Number of Instructions faster on 80386		50		
Total Number of instructions analyzed		190		

Harris Semiconductor

APPNOTE

No. 112 March 1989

Harris Digital

80C286/80386 HARDWARE COMPARISON

Author: Ted Schaufelberger

The Harris 80C286 static CMOS microprocessor, available with maximum operating frequencies of 16-MHz and 20-MHz, offers both performance and design advantages over the 80386 when operating at the same frequency. When both the 80C286 and 80386 are operated on a 16-bit data bus, which fully supports industry standard 8086/80286 code, the 80C286 has better performance, and is significantly simpler to design with than the 80386. The 80C286 also uses significantly lower power than the 80386, leading to less expensive, more reliable overall system design (see Figure 1).

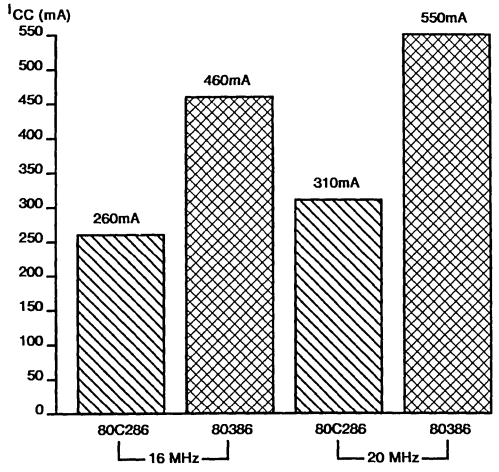


FIGURE 1. 80C286/80386 POWER CONSUMPTION COMPARISON

The following comparison highlights some of the performance advantages that exist on the 80C286:

Summary of 16-Bit Data Bus Performance

- **80C286**
  - The 80C286 already has all necessary control lines needed to implement a 16-bit data bus (Ref. section on Control Signals Required to Implement a 16-Bit Data Bus).
  - The 80C286 supports a fully pipelined mode of operation for maximum system performance (Ref. section on Pipelined Operation on a 16-Bit Data Bus).
  - The 80C286 remains in a pipelined mode of operation even when idle bus cycles occur (Ref. section on Idle Cycles).
  - The 80C286 instruction prefetch takes one bus cycle to execute, thereby minimizing the time that the processor Execution Unit must wait should it need the bus (Ref. section on Instruction Prefetching a 16-Bit Data Bus).
- **80386**
  - The 80386 requires five additional control lines to be generated by external logic in order to implement a 16-bit data bus (Ref. section on Control Signals Required to Implement a 16-Bit Data Bus).
  - The 80386 does not support a fully pipelined mode of operation. Some pipelining can be achieved, but to accomplish this, external bus 'monitor' logic must be added to the system (Ref. section on Pipelined Operation on a 16-Bit Data Bus).
  - The 80386's pipelining is disrupted by idle bus cycles. A non-pipelined bus cycle, usually with an additional wait state, must be executed before the 80386 can return to pipelined mode. Idle bus cycles occur an average of 9% of the time (Ref. section on Idle Cycles).
  - The 80386 instruction prefetch takes two bus cycles to execute, which can cause performance degradation by forcing the Execution Unit of the processor to wait a full bus cycle for use of the bus in order to complete an instruction (Ref. section on Instruction Prefetching on a 16-Bit Data Bus).

16-Bit Data Bus Operation

This section will discuss the control signals required to implement a 16-bit data bus, as well as pipelined operation, idle cycles, and instruction prefetching on a 16-bit bus.

Control Signals Required to Implement a 16-Bit Data Bus

The 80C286 microprocessor has all the control lines needed to implement a 16-bit data bus resident on chip, no further control lines are required.

80386 SIGNALS				16-BIT BUS SIGNALS			
BE3#	BE2#	BE1#	BE0#	A1	BHE#	BLE# (A0)	COMMENTS
H*	H*	H*	H*	X	X	X	X-No Active Bytes
H	H	H	L	L	H	L	
H	H	L	H	L	L	H	
H	H	L	L	L	L	L	
H	L	H	H	H	H	L	
H*	L*	H*	L*	X	X	X	X-Not Contiguous Bytes
H	L	L	H	L	L	H	
H	L	L	L	L	L	L	
L*	H*	H*	L*	X	X	X	X-Not Contiguous Bytes
L*	H*	L*	H*	X	X	X	X-Not Contiguous Bytes
L*	H*	L*	L*	X	X	X	X-Not Contiguous Bytes
L	L	H	H	H	L	L	
L*	L*	H*	L*	X	X	X	X-Not Contiguous Bytes
L	L	L	H	L	L	H	
L	L	L	L	L	L	L	

BLE# Asserted When D0-D7 of 16-Bit Bus is Active.
BHE# Asserted When D8-D15 of 16-Bit Bus is Active.
A1 Low For All Even Words; A1 High For All Odd Words.

Key: X = Don't Care
H = High Voltage Level
L = Low Voltage Level
* = A Non-Occurring Pattern of Byte Enables; Either None are Asserted, or the Pattern has Byte Enables Asserted for Non-Contiguous Bytes

FIGURE 2. A1, BLE#, AND BHE# SIGNAL GENERATION TABLE

In order to implement a 16-bit data bus with the 80386 microprocessor, it is necessary to create at least the following five additional control signals: Address Line 1 (A1), Bus Low Enable (BLE#), Bus High Enable (BHE#), Bus Size 16-Bits (BS16#), and Next Address (NA#).

The first of these signals, A1, is an additional address line required to convert the granularity of the 80386's address space from double-word size entities (32-bit) to word size entities (16-bit). The second two signals, BLE# and BHE#, primarily serve as chip selects which enable the appropriate byte or bytes onto the 16-bit data bus. These three signals are generated from the four 80386 byte enables (BE0#-BE3#) as shown in Figure 2. The logic to implement these signals is shown in Figure 3.

In addition to these three control signals generated from 80386 signals as outputs, two input control signals to the 80386 must be generated by external logic (BS16# and NA#).

BS16# is used to inform the 80386, on a cycle-by-cycle basis, that a 16-bit bus size is to be used for data transfer. NA# is used to request that the 80386 put the next cycle address on the bus early, thereby pipelining that cycle.

The 80386, therefore, requires five additional control lines, three outputs and two inputs, in order to implement a 16-bit data bus. The generation of these control lines, in turn, requires additional 'glue' logic (which also introduces additional signal propagation delay, thereby reducing address access time available to the system), and finally, there is additional bus cycle 'monitor' logic necessary if the 16-bit data bus is to be pipelined for higher performance.

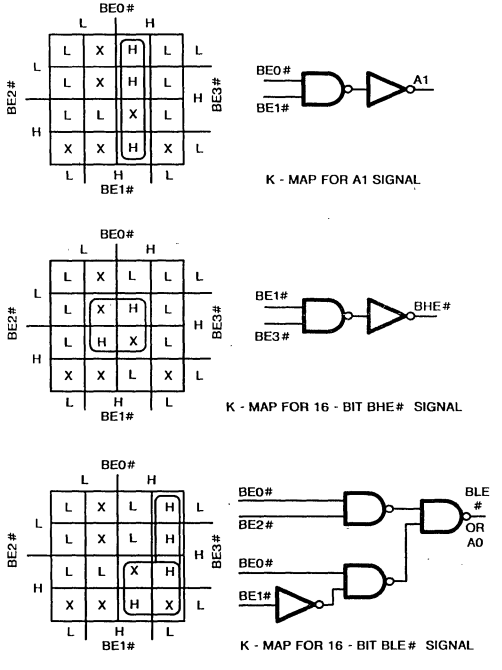


FIGURE 3. A1, BLE#, AND BHE# LOGIC

Pipelined Operation on a 16-Bit Data Bus

At a given clock frequency, pipelined address operation increases a system's performance, while simultaneously allowing relatively slower memories and I/O devices to be used. Pipelined address operation provides the system increased address access time, and increased address decoding time.

The 80C286 is optimized for, and directly supports, fully pipelined bus operations on a 16-bit data bus. In other words, the 80C286 performs all bus operations in a fully pipelined mode.

The 80386 does not support fully pipelined operation on a 16- bit data bus. In order to pipeline a bus cycle on the 80386, the Next Address (NA#) signal must be asserted to the processor. If the Next Address (NA#) signal and the Bus Size 16-Bit (BS16#) signal are both asserted in the same bus cycle, the NA# signal will not be recognized. Since the BS16# signal must be asserted to the 80386 for many patterns of 16-bit and 8-bit transfers to take place correctly, the pipelining of transfers over a 16-bit bus is limited.

To allow pipelining of 16-bit data, external logic must be implemented to monitor the type of bus cycle taking place, decide if the cycle can be pipelined, and, if so, negate the BS16# signal to the 80386 and assert the NA# signal. Pipelining is possible only if the bus cycle is one of the following three types:

(1) A read operand cycle using only the lower half of the data bus

(2) A write operand cycle using only the lower half of the data bus

(3) A write operand cycle using only the upper half of the data bus

The 80386 will not allow 16-bit pipelining of read or write cycles that have byte alignments that do not conform to one of the previously mentioned three types.

The 80C286, then, fully supports address pipelining, yielding the highest possible system performance, while using relatively lower performance (and therefore cheaper) memories and peripherals. The 80386, however, does not support fully pipelined 16-bit bus operation, and, to support even partial pipelining, requires external bus 'monitor' logic.

Idle Cycles

Another factor to consider when evaluating 80C286 and 80386 performance is the effect of idle cycles on pipelined operation. Calculations have shown that, on average, bus idle cycles occur in the system approximately 9% of the time. The effect of idle cycles on pipelining is quite different on the 80C286 than on the 80386.

The 80C286 pipelined operation is not affected by idle cycles. When an idle cycle or cycles occur in a stream of pipelined bus cycles, the 80C286 returns to pipelining bus cycles immediately after the last idle cycle. In this way, each device on the bus (e.g. memory, peripheral) maintains a fixed timing associated with that device, and therefore always uses the minimum number of wait states required for that device.

On the other hand, the 80386 pipelined operation is disrupted by idle cycles. With the 80386, an idle cycle or cycles occurring in a pipelined stream of bus cycles breaks the pipelining operation. Once an idle cycle has occurred, a non-pipelined bus cycle must always be executed prior to resuming pipelining. Since a non-pipelined bus cycle will have different timing than a pipelined bus cycle (even to the same device), an additional wait state must be added to this bus cycle. This not only degrades performance, but requires additional external logic to differentiate between a pipelined bus cycle access, and a non-pipelined bus cycle access, even to the same device with the same address.

From the preceding, it can be seen that **when executing 16-bit code, the 80C286 has a 9% performance increase over the 80386, due to the manner in which each processor handles idle cycles alone.** Note, that with the 80386, a pipelined stream of bus cycles will always be disrupted when an idle cycle occurs, whether using a 16-bit data bus or a 32-bit data bus. In either case, a non-pipelined bus cycle must be executed prior to resuming pipelined operation.

Instruction Prefetching on a 16-Bit Data Bus

One final factor needs to be considered in the evaluation of 80C286 and 80386 performance on a 16-bit data bus; the effect that prefetching instructions has on instruction execution time. Prefetching of instructions is done by the processor Bus Unit on both the 80C286 and 80386. The prefetch is done when the bus would otherwise be idle for the upcoming cycle, and the prefetch queue is not full.

The 80C286 does word size (16-bit) prefetching of instructions, and therefore completes it's prefetch activities in one bus cycle. This minimizes the waiting period to gain access to the bus by other processor entities, such as the Execution Unit.

The 80386 does doubleword (32-bit) prefetching of instructions, even on a 16-bit bus. This means that once a prefetch has begun execution, two bus cycles are required to complete the prefetch. If, for instance, the processor's Execution Unit requires the bus for a data fetch or write in order to complete an executing instruction, it must wait for the two bus cycles of the prefetch to complete before it can access the bus. This can substantially degrade instruction execution time.

32-Bit Data Bus Operation

This section discusses operating the 80386 on a 32-bit bus in order to overcome some of the handicaps it suffers on a 16-bit bus. In addition, several advantages and disadvantages associated with the 80386 on a 32-bit bus are considered.

Hardware Advantages of the 80386 on a 32-Bit Data Bus

There are several advantages to operating the 80386 on a 32-bit data bus as opposed to a 16-bit data bus. Some of the control lines that were required for a 16-bit data bus are eliminated (A1, BLE#, BHE#, and BS16#). It is possible to come closer to a fully pipelined mode of operation, although idle cycles will still disrupt the pipelining 9% of the time. Finally, prefetching on a 32-bit bus executes in one bus cycle instead of two. Offsetting these advantages, however are several major disadvantages.

Hardware Disadvantages of the 80386 on a 32-bit Data Bus

When using a full 32-bit data bus, the chip complexity of a 80386 based system is increased over a 16-bit system. Twice as many transceivers (four instead of two) are required. In addition, in order to accommodate the additional 16 data lines of the 32-bit bus, twice as many memory devices are typically required with the 32-bit system as compared to a 16-bit system. This amounts to an increase in DRAM, alone, of from 18 devices in a typical 16-bit system to 36 devices in a typical 32-bit system.

The 16 additional data lines of the 32-bit bus increase the EMI problems inherent in the system. The additional coupling and crosstalk between data lines must be taken into consideration when laying out the system PC board.

There is a significant increase in the amount of board space used as a result of the additional chips required to implement a 32-bit bus, as well as the 16 additional data lines. This results in a larger, more complex (and more expensive) PC board than with a 16-bit system, often requiring an increase in the number of board layers.

References

Intel Corporation. 1987.
80386 Hardware Reference Manual.

APPNOTE

No. 120 June 1989

Harris Digital

INTERFACING THE 80C286-16 WITH THE 80287-10

Author: Ted Schaufelberger

An important requirement in many systems is the ability to off-load numeric data processing. In an 80C286 system, this can be accomplished with an 80287 numeric co-processor. However, as processor speeds increase, it may become necessary to interface a high speed 80C286 processor with a lower speed 80287. This Document will briefly describe the interface between a 16MHz 80C286 (80C286-16) and a 10MHz 80287 (80287-10).

Interfacing the 80C286 with an 80287 can be broken down into three main areas:

(1) Bus control lines and data lines which coordinate and implement the flow of data between the two processors (i.e. the data lines, chip select lines, and read/write lines).

(2) The clock line(s), which drive the two processors.

(3) The four status lines through which the 80C286 and 80287 directly communicate status information to one another - comprised of the $\overline{\text{BUSY}}$, $\overline{\text{ERROR}}$, Peripheral Request (PEREQ), and Peripheral Acknowledge ($\overline{\text{PEACK}}$) lines.

Bus Control Lines

The various bus control and data lines in most systems would be coordinated by either a bus controller (such as the 82C288), or a bus controller subsection of an 80C286 oriented chip set. All requisite bus control timing between a 16MHz 80C286, and a 10MHz 80287 would then be handled by these devices (typically with one wait-state inserted to allow for the slower 80287-10).

Clock Lines

A system using a 16MHz 80C286 with a 10MHz 80287 requires separate clock lines for the two processors. The 32MHz system clock used by the 80C286-16 is too fast for the 80287 ± 10, necessitating a dedicated clock driver for the 80287. This clock driver should supply a 10MHz clock to the 80287 with a 1/3 duty cycle to allow the 80287-10 to run at it's full 10MHz capability. One solution for providing this clock is the 82C84A-1, which meets this specification with either a 30MHz crystal at it's crystal inputs, or a 30MHz external frequency input to it's EFI pin. In either case, a 10MHz 1/3 duty cycle clock is output to the 80287. Note that when using a dedicated clock driver such as this, the CKM pin of the 80287 must be pulled up.

Status Lines

The 80C286 and 80287 communicate status information with one another through four signals; the $\overline{\text{BUSY}}$ line, the $\overline{\text{ERROR}}$ line, the peripheral request line (PEREQ), and the $\overline{\text{PEACK}}$ line.

The $\overline{\text{BUSY}}$ and $\overline{\text{ERROR}}$ lines can be connected from the 80287 to a 80C286-oriented chipset, or from the 80287 directly to a 80C286. In the case of the chipset interface, the signal timing between the 80287 and 80C286 is coordinated by the chipset. In the case of the direct 80287 to 80C286 interface, the signal timing is handled by the 80C286, and, since the signal flow direction is from the 80287 to the 80C286 (i.e. from the slower device to the faster device), no additional hardware is required to achieve proper timing.

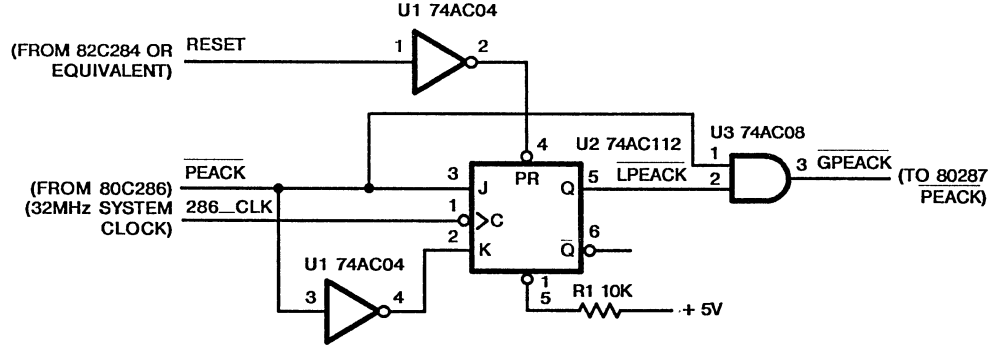


FIGURE 1. PEACK STRETCH CIRCUIT

The peripheral request (PEREQ) line should be connected directly from the 80287 to the 80C286, and again, since the signal flow direction is from the 80287 to the 80C286, no additional hardware is required.

The peripheral acknowledge ($\overline{\text{PEACK}}$) line is normally connected directly from the 80C286 to the 80287. In this case the signal flow direction is from the 80C286 to the 80287 (i.e. faster device to slower device), and the $\overline{\text{PEACK}}$ active time is not guaranteed to meet the requirements of the slower 80287-10. Worst case timing for the 80C286-16 reveals that $\overline{\text{PEACK}}$ output could be as short as 45.5ns (i.e. $\overline{\text{PEACK}}$ (min) = 45.5ns). The 80287-10 input requirement is $\overline{\text{PEACK}}$ (min) = 60ns.

The proper $\overline{\text{PEACK}}$ timing can be achieved using the circuit shown in Figure 1 comprised of a 74AC04, 74AC08, and a 74AC112. Referring to the timing diagram shown in Figure 2, it can be seen that this circuit effectively 'stretches' the 80C286's $\overline{\text{PEACK}}$ output (in the form of $\overline{\text{GPEACK}}$) to 72.7ns, which satisfies the 80287-10 requirement.

The operation of the circuit shown in Figure 1 is as follows:

(1) The RESET signal (which is also applied to the 80C286) is used to initialize the 'AC112 to a known inactive state (Q = 1).

(2) When the 80C286 asserts the $\overline{\text{PEACK}}$ signal, the gated version of this signal ($\overline{\text{GPEACK}}$) is asserted with minimal delay (7.9ns through the 'AC08).

(3) On the falling edge of the 80C286 CLK at the beginning of Phase 2 of the T_S cycle, the low state of $\overline{\text{PEACK}}$ is clocked into the 'AC112. This effectively holds $\overline{\text{GPEACK}}$ low for an additional clock cycle longer than standard $\overline{\text{PEACK}}$ timing.

(4) On the falling edge of the 80C286 CLK at the beginning of phase 2 of the first T_C cycle, the high state of $\overline{\text{PEACK}}$ is clocked into the 'AC112, which then causes $\overline{\text{GPEACK}}$ to go inactive.

The net effect of this circuit operation is to extend the 80C286's Peripheral Acknowledge signal to the 80287-10 sufficiently to meet it's requirements.

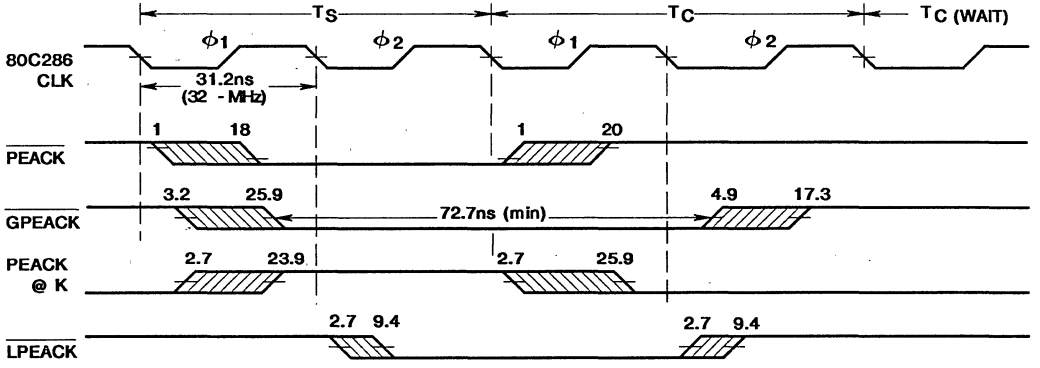


FIGURE 2. PEACK CYCLE TIMING

DIGITAL

CMOS Peripherals

5

HARRIS

82C37A/883

CMOS High Performance Programmable DMA Controller

June 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Compatible with the NMOS 8237A
- Four Independent Maskable Channels with Autoinitialization Capability
- Cascadable to any Number of Channels
- Special Mode Permits 16-Bit, Zero Wait State DMA Transfers
- High Speed Data Transfers:
  - Up to 4 MBytes/sec with 8MHz Clock in Normal Mode
  - Up to 8 MBytes/sec with 8MHz Clock in 16-Bit Mode
  - Up to 6.25 MBytes/sec with 12.5MHz Clock in Normal Mode
  - Up to 12.5 MBytes/sec with 12.5MHz Clock in 16-Bit Mode
- Memory-to-Memory Transfers
- Static CMOS Design Permits Low Power Operation
  - ICCSB = 10μA Maximum
  - ICCOP = 2mA/MHz Maximum
- Fully TTL/CMOS Compatible
- Internal Registers may be Read from Software

Description

The 82C37A/883 is an enhanced version of the industry standard 8237A Direct Memory Access (DMA) controller, fabricated using Harris' advanced 2 micron CMOS process. Pin compatible with NMOS designs, the 82C37A/883 offers increased functionality, improved performance, and dramatically reduced power consumption. The fully static design permits gated clock operation for even further reduction of power.

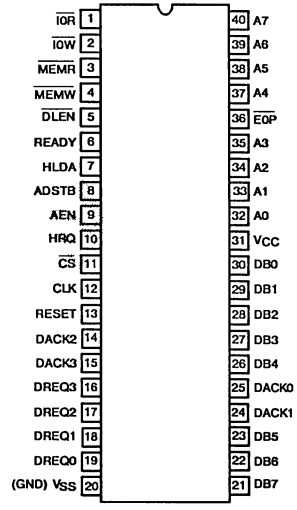
The 82C37A/883 controller can improve system performance by allowing external devices to transfer data directly to or from system memory. Memory-to-memory transfer capability is also provided, along with a memory block initialization feature. A new feature allows each channel to be individually programmed for 8-bit data transfers or 16-bit data transfers. DMA requests may be generated by either hardware or software, and each channel is independently programmable with a variety of features for flexible operation.

The 82C37A/883 is designed to be used with an external address latch, such as the 82C82, to demultiplex the most significant 8 bits of address. An additional latch is required to temporarily store the most significant 8 bits of data if 16-bit memory-to-memory transfers are desired. The 82C37A/883 can be used with industry standard microprocessors such as 80C286, 80286, 80C86, 80C88, 8088, 8085, 8086, Z80, NSC800, 80186 and others.

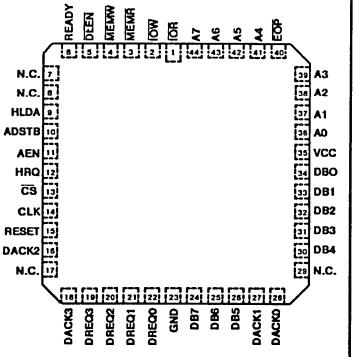
Multimode programmability allows the user to select from three basic types of DMA services, and reconfiguration under program control is possible even with the clock to the controller stopped. Each channel has a full 64K address and word count range, and may be programmed to autoinitialize these registers following DMA termination (end of process).

Pinouts

82C37A/883 (CERAMIC DIP)
TOP VIEW



82C37A/883 (CERAMIC LCC)
TOP VIEW



5 CMOS PERIPHERALS

HARRIS

82C52/883

June 1989

CMOS Serial Controller Interface

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Single Chip UART/BRG
- 16MHz (1M Baud) Operation
- Crystal or External Clock Input
- On-Chip Baud Rate Generator - 72 Selectable Baud Rates
- Interrupt Mode With Mask Capability
- Microprocessor Bus Oriented Interface
- 80C86 Compatible
- Single +5V Power Supply
- Low Power Operation ..... 1mA/MHz typical
- Modem Interface
- Line Break Generation and Detection
- Military Operating Temperature Range ..... -55°C to +125°C

Description

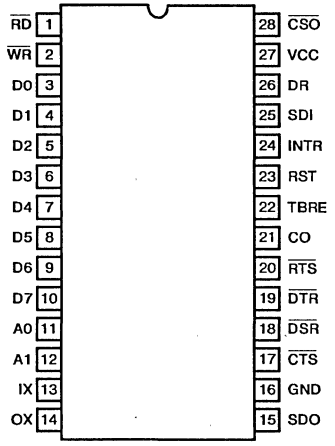
The Harris 82C52/883 is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. Utilizing the Harris advanced Scaled SAJI IV CMOS process, the 82C52/883 will support data rates up to 1M baud asynchronously with a 16X clock (16MHz clock frequency).

The on-chip Baud Rate Generator can be programmed for any one of 72 different baud rates using a single industry standard crystal or external frequency source. A unique pre-scale divide circuit has been designed to provide standard RS-232-C baud rates when using any one of three industry standard baud rate crystals (1.8432 MHz, 2.4576 MHz, or 3.072 MHz).

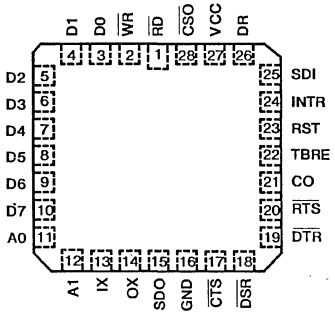
A programmable buffered clock output (CO) is available and can be programmed to provide either a buffered oscillator or 16X baud rate clock for general purpose system usage.

Pinouts

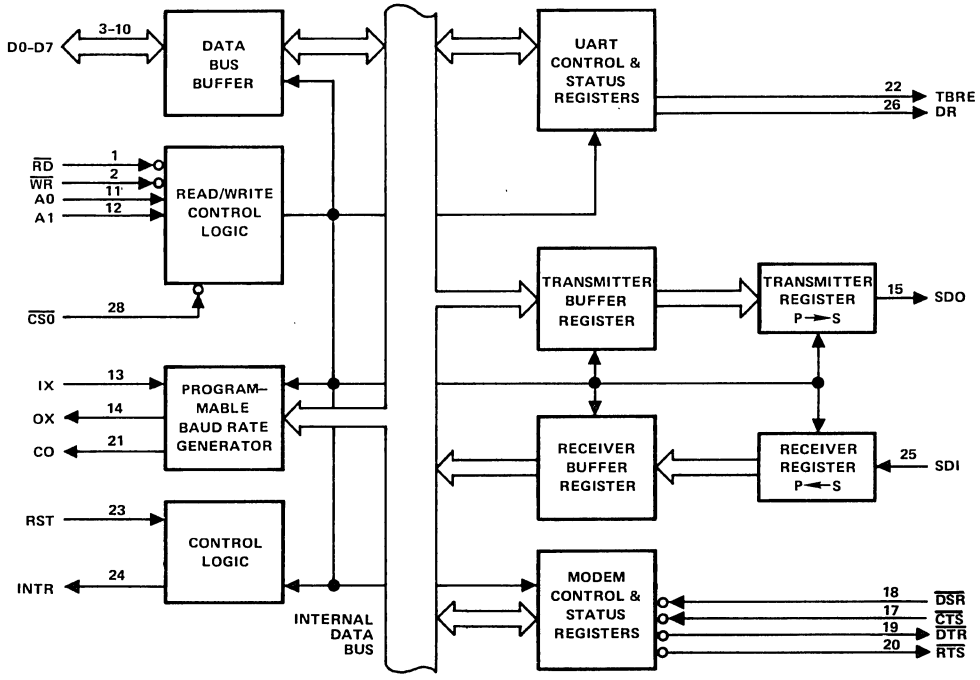
82C52/883 (CERAMIC DIP)
TOP VIEW



82C52/883 (CERAMIC LCC)
TOP VIEW



Block Diagram



Pin Description 82C52/883

SYMBOL	PIN NO.	TYPE	ACTIVE LEVEL	DESCRIPTION
$\overline{RD}$	1	I	Low	READ: The $\overline{RD}$ input causes the 82C52/883 to output data to the data bus (D0-D7). The data output depends upon the state of the address inputs (A0-A1). $\overline{CS0}$ enables the $\overline{RD}$ input.
$\overline{WR}$	2	I	Low	WRITE: The $\overline{WR}$ input causes data from the data bus (D0-D7) to be input to the 82C52/883. Addressing and chip select action is the same as for read operations.
D0-D7	3-10	I/O	High	DATA BITS 0-7: The Data Bus provides eight, three-state input/output lines for the transfer of data, control and status information between the 82C52/883 and the CPU. For character formats of less than 8 bits, the corresponding D7, D6 and D5 are considered "don't cares" for data WRITE operations and are 0 for data READ operations. These lines are normally in a high impedance state except during read operations. D0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
A0, A1	11, 12	I	High	ADDRESS INPUTS: The address lines select the various internal registers during CPU bus operations.
IX, OX	13, 14	I/O		CRYSTAL/CLOCK: Crystal connections for the internal Baud Rate Generator. IX can also be used as an external clock input in which case OX should be left open.
SDO	15	O	High	SERIAL DATA OUTPUT: Serial data output from the 82C52/883 transmitter circuitry. A Mark (1) is a logic one (high) and Space (0) is logic zero (low). SDO is held in the Mark condition when $\overline{CTS}$ is false, when RST is true, when the Transmitter Register is empty, or when in the Loop Mode.
GND	16		Low	GROUND: Power supply ground connection.
$\overline{CTS}$	17	I	Low	CLEAR TO SEND: The logical state of the $\overline{CTS}$ line is reflected in the $\overline{CTS}$ bit of the Modem Status Register. Any change of state in $\overline{CTS}$ causes INTR to be set true when INTEN and MIEN are true. A false level on $\overline{CTS}$ will inhibit transmission of data on the SDO output and will hold SDO in the Mark (high) state. If $\overline{CTS}$ goes false during transmission, the current character being transmitted will be completed. $\overline{CTS}$ does not affect Loop Mode operation.
$\overline{DSR}$	18	I	Low	DATA SET READY: The logical state of the $\overline{DSR}$ line is reflected in the Modem Status Register. Any change of state of $\overline{DSR}$ will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the 82C52/883.
$\overline{DTR}$	19	O	Low	DATA TERMINAL READY: The $\overline{DTR}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the Modem Control Register (MCR). This signal is cleared (high) by writing a logic 0 in the $\overline{DTR}$ bit in the MCR or whenever a reset (RST = high) is applied to the 82C52/883.
$\overline{RTS}$	20	O	Low	REQUEST TO SEND: The $\overline{RTS}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the MCR. This signal is cleared (high) by writing a logic 0 to the $\overline{RTS}$ bit in the MCR or whenever a reset (RST = high) is applied to the 82C52/883.
CO	21	O		CLOCK OUT: This output is user programmable to provide either a buffered IX output or a buffered Baud Rate Generator (16X) clock output. The buffered IX (Crystal or external clock source) output is provided when the Baud Rate Select Register (BRSR) bit 7 is set to a zero. Writing a logic one to BRSR bit 7 causes the CO output to provide a buffered version of the internal Baud Rate Generator clock which operates at sixteen times the programmed baud rate. On reset D7 (CO select) is reset to 0.
TBRE	22	O	High	TRANSMITTER BUFFER REGISTER EMPTY: The TBRE output is set (high) whenever the Transmitter Buffer Register (TBR) has transferred its data to the Transmit Register. Application of a reset (RST) to the 82C52/883 will also set the TBRE output. TBRE is cleared (low) whenever data is written to the TBR.
RST	23	I	High	RESET: The RST input forces the 82C52/883 into an "Idle" mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The UART Status Register (USR) is cleared except for the TBRE and TC bits, which are set. The 82C52/883 remains in an "Idle" state until programmed to resume serial data activities. The RST input is a Schmitt triggered input.
INTR	24	O	High	INTERRUPT REQUEST: The INTR output is enabled by the INTEN bit in the Modem Control Register (MCR). The MIEN bit selectively enables modem status changes to provide an input to the INTR logic. Figure 9 in Design Information shows the overall relationship of these interrupt control signals.
SDI	25	I	High	SERIAL DATA INPUT: Serial data input to the 82C52/883 receiver circuits. A Mark (1) is high, and a Space (0) is low. Data inputs on SDI are disabled when operating in the loop mode or when RST is true.
DR	26	O	High	DATA READY: A true level indicates that a character has been received, transferred to the RBR, and is ready for transfer to the CPU. DR is reset on a data READ of the Receiver Buffer Register (RBR) or when RST is true.
VCC	27		High	VCC: +5V postive power supply pin. A 0.1 µF decoupling capacitor from VCC (Pin 27) to GND (Pin 16) is recommended.
$\overline{CS0}$	28	I	Low	CHIP SELECT: The chip select input acts as an enable signal for the $\overline{RD}$ and $\overline{WR}$ input signals.

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec)..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	45°C/W	8.4°C/W
Ceramic LCC Package	50.7°C/W	5.3°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.1W
Ceramic LCC Package 986mW
Gate Count ..... 1500 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Voltage Range ..... +4.5V to +5.5V

TABLE 1. 82C52/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	VIH	VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	.7VCC	-	V
Logical Zero Input Voltage	VIL		1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.8	V
CLK Logical One Input Voltage	VIH(CLK)	External Clock, VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC-0.5	-	V
CLK Logical Zero Input Voltage	VIL(CLK)	External Clock	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	GND+0.5	V
Schmitt Trigger Logical One Input Voltage	VTH	Reset Input, VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC-0.5	-	V
Schmitt Trigger Logical Zero Input Voltage	VTL	Reset Input	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	GND+0.5	V
Output High Voltage	VOH	IOH = -2.5mA, Note 2 Except OX	1, 2, 3	$-55°C \leq T_A \leq +125°C$	3.0	-	V
		IOH = -100µA, Note 2 For OX, IOH = -1.0mA Note 2			VCC-0.4	-	V
Output Low Voltage	VOL	IOL = +2.5mA, Note 2 For OX, IOL = +1.0mA Note 2	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Input Leakage Current	II	VCC = 5.5V, VIN = GND or VCC, All inputs except IX	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Output Leakage Current	IO	VCC = 5.5V, VOUT = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-10.0	+10.0	µA

NOTE: 1. VCC = 4.5V unless otherwise specified. All voltages referenced to device GND.
2 Interchanging of force and sense conditions is permitted.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. 82C52/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Select Setup to Control Leading Edge	(1)TSVCTL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	ns
Select Hold from Control Trailing Edge	(2)TCTHSX		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Control Pulse Width	(3)TCTLCTH	Control Consists of $\overline{RD}$ or $\overline{WR}$	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Control Disable to Control Enable	(4)TCTHCTL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	190	-	ns
Read LOW to Data Valid	(5)TRLDV	Test Condition 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	120	ns
Data Setup Time	(7)TDVWH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Data Hold Time	(8)TWHDX		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
Clock Frequency	(9)FC	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	16	MHz
Clock High Time	(10)TCHCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	25	-	ns
Clock Low Time	(11)TCLCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	25	-	ns
Clock Output Fall Time	(13)TFCO	From 0.7 VCC to 0.8V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	15	ns
Clock Output Rise Time	(14)TRCO	From 0.8V to 0.7 VCC	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	15	ns

NOTES: 1. VCC = 4.5V and 5.5V unless otherwise specified. Tested as follows: f = 1MHz, VIH = .7 VCC, VIL = 0.8V, CL = 50pF unless a test condition is specified, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V. VIHC = VCC - 0.5V, VILC = GND + 0.5V. VTH = VCC - 0.5V, VTL = GND + 0.5V.

2. "Test Cond. X" refers to TEST CONDITION DEFINITION TABLE with AC Test Circuit.

3. FC is calculated on measured TCHCL and TCLCH times. TCHCL + TCLCH must be $\geq$ 62.5ns.

TABLE 3. 82C52/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	f = 1MHz, all Measurements are Referenced to Device GND, VCC = Open	1, 2	$T_A = +25^oC$	-	12	pF
			1, 3	$T_A = +25^oC$	-	6	pF
Output Capacitance	COUT		1, 2	$T_A = +25^oC$	-	15	pF
			1, 3	$T_A = +25^oC$	-	7	pF
I/O Capacitance	CIO		1, 2	$T_A = +25^oC$	-	15	pF
			1, 3	$T_A = +25^oC$	-	7	pF
Operating Power Supply Current	ICCOP	VCC = 5.5V	1, 4	$-55^oC \leq T_A \leq +125^oC$	-	3.0	mA
Read Disable	(6)TRHDZ	VCC = 4.5V and 5.5V	1, 5	$-55^oC \leq T_A \leq +125^oC$	0	60	ns
IX Input Rise/Fall Time	(12)TR/TF	VCC = 4.5V and 5.5V	1, 6	$-55^oC \leq T_A \leq +125^oC$	-	tx	ns

NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. Ceramic DIP package.

3. Ceramic LCC package.

4. External clock, f = 2.4576MHz, VIN = VCC or GND, outputs open.

5. Reference Test Condition 2 of TEST CONDITION DEFINITION TABLE with AC Test Circuit.

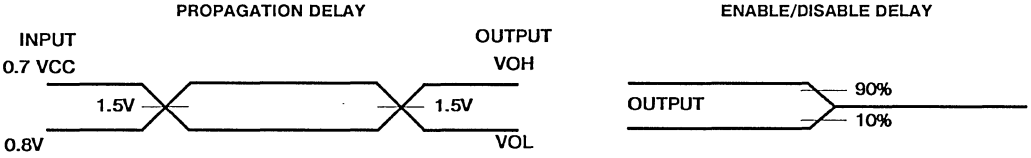
6. tx $\leq$ 1/6 FC or 50ns, whichever is less.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 4. APPLICABLE SUBGROUPS

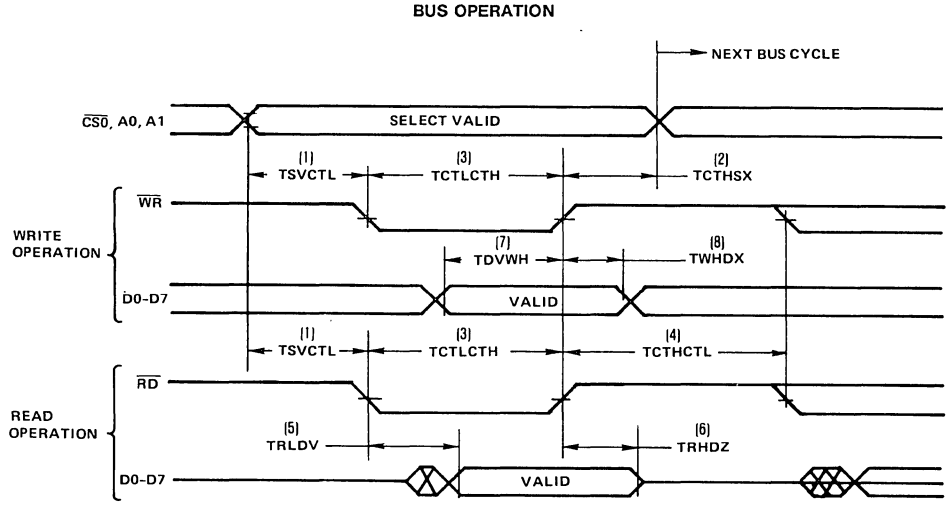
CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

AC Testing Input, Output Waveforms

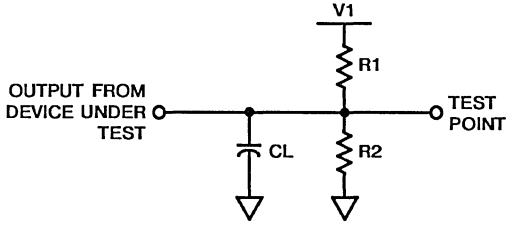


AC Testing: All input signals (except IX and RST) must switch between 0.8V and 0.7 VCC. Input rise and fall times are driven at 1nsec per volt.

Timing Waveform



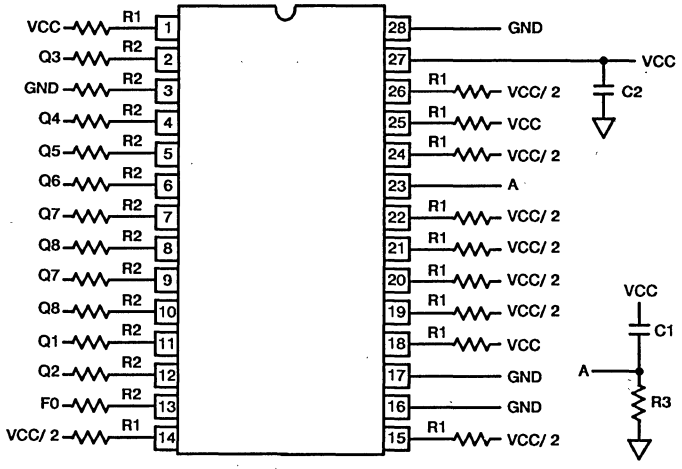
AC Test Circuit



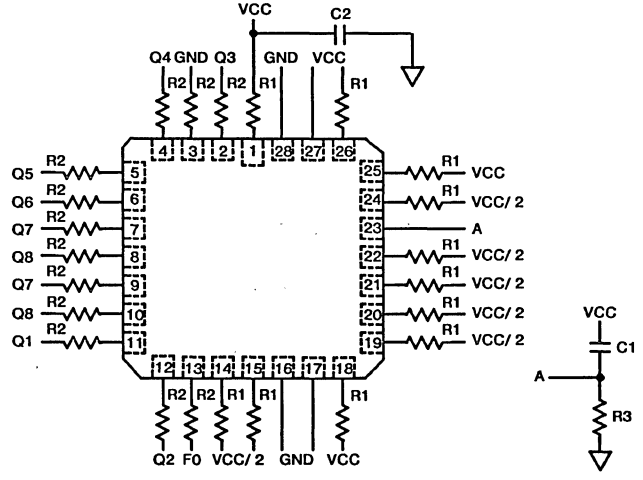
TEST CONDITION		V1	R1	R2	CL
1	Propagation Delay	1.7V	520	∞	100pF
2	Disable Delay	VCC	5K	5K	50pF

Burn-In Circuits

82C52/883 CERAMIC DIP



82C52/883 CERAMIC LCC



NOTES:

1. VCC = 5.5V ± 0.5V
   GND = 0V
2. VIH = 4.5V ± 10%
   VIL = -0.2V to +0.4V
3. Component Values:
   R1 = 1.2KΩ, 1/4W, 5%
   R2 = 47KΩ, 1/4W, 5%
   R3 = 10KΩ, 1/4W, 5%
   C1 = 1.0μF nominal
   C2 = 0.01μF minimum
   F0 = 100KHz ± 10%, F1 = F0/2, F2 = F1/2 • • • F12 = F11/2

Metallization Topology

DIE DIMENSIONS:
178.7 x 187.0 x 19 ± 1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 2kÅ

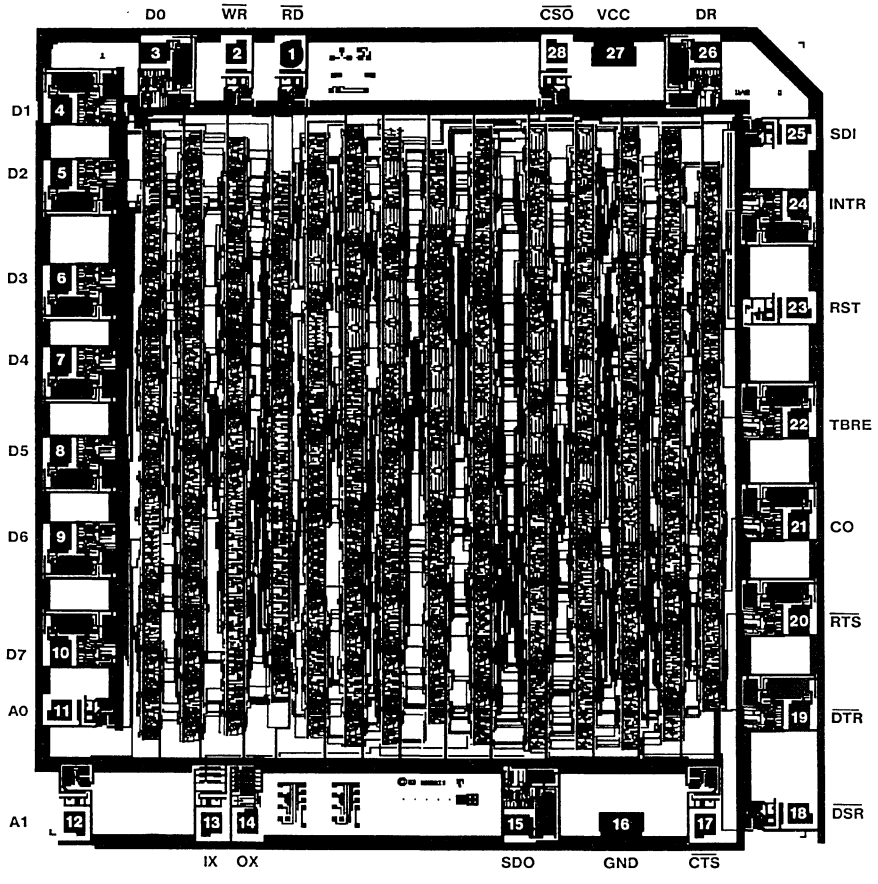
GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
2.07 x 10^4 A/cm^2

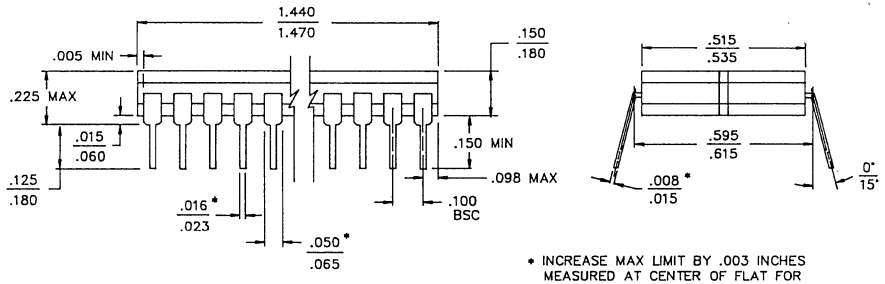
Metallization Mask Layout

82C52/883



Packaging†

28 PIN CERAMIC DIP

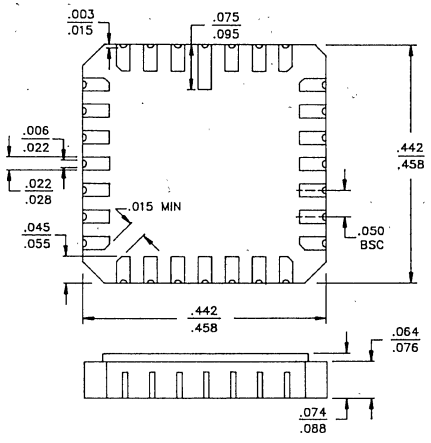


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

28 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-4

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Reset

During and after power-up, the 82C52 Reset Input (RST) must be held high for at least two IX clock cycles in order to initialize and drive the 82C52 circuits to an idle mode until proper programming can be done. A high on RST causes the following events to occur:

- Resets the internal Baud Rate Generator (BRG) circuit clock counters and bit counters. The Baud Rate Select Register (BRSR) is not affected (except for bit 7 which is reset to 0).
- Clears the UART Status Register (USR) except for Transmission Complete (TC) and Transmit Buffer Register Empty (TBRE) which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. Note that the UART Control Register (UCR) is not affected.

Following removal of the reset condition (RST = low), the 82C52 remains in the idle mode until programmed to its desired system configuration.

Programming The 82C52

The complete functional definition of the 82C52 is programmed by the systems software. A set of control words (UCR, BRSR and MCR) must be sent out by the CPU to initialize the 82C52 to support the desired communication format. These control words will program the character length, number of stop bits, even/odd/no parity, baud rate, etc. Once programmed, the 82C52 is ready to perform its communication functions.

The control registers can be written to in any order. However, the MCR should be written to last because it controls the interrupt enables, modem control outputs and the receiver enable bit. Once the 82C52 is programmed and operational, these registers can be updated any time the 82C52 is not immediately transmitting or receiving data.

Table A. shows the control signals required to access 82C52 internal registers.

UART Control Register (UCR)

The UCR is a write only register which configures the UART transmitter and receiver circuits. Data bits D7 and D6 are not used but should always be set to a logic zero (0) in order to insure software compatibility with future product upgrades. During the Echo Mode, the transmitter always repeats the received word and parity, even when the UCR is programmed with different or no parity. See Figure 1.

TABLE A.

$\overline{CS0}$	A1	A0	$\overline{WR}$	$\overline{RD}$	OPERATION
0	0	0	0	1	Data Bus→Transmitter Buffer Register (TBR)
0	0	0	1	0	Receiver Buffer Register (RBR)→Data Bus
0	0	1	0	1	Data Bus→UART Control Register (UCR)
0	0	1	1	0	UART Status Register (USR)→Data Bus
0	1	0	0	1	Data Bus→Modem Control Register (MCR)
0	1	0	1	0	MCR→Data Bus
0	1	1	0	1	Data Bus→Bit Rate Select Register (BRSR)
0	1	1	1	0	Modem Status Register (MSR)→Data Bus

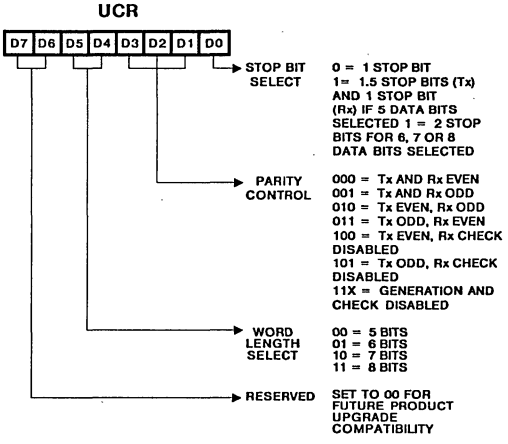


FIGURE 1.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Baud Rate Select Register (BRSR)

The 82C52 is designed to operate with a single crystal or external clock driving the IX input pin. The Baud Rate Select Register is used to select the divide ratio (one of 72) for the internal Baud Rate Generator circuitry. The internal circuitry is separated into two separate counters, a Prescaler and a Divisor Select. The Prescaler can be set to any one of four division rates, ÷1, ÷3, ÷4, or ÷5.

The Prescaler design has been optimized to provide standard baud rates using any one of three popular crystal frequencies. By using one of these common system clock frequencies, 1.8432MHz, 2.4576MHz or 3.072MHz and Prescaler divide ratios of ÷3, ÷4, or ÷5 respectively, the Prescaler output will provide a constant 614.4KHz. When this frequency is further divided by the Divisor Select counter, any of the standard baud rates from 50 Baud to 38.4 Kbaud can be selected (see Table B). Non-standard baud rates up to 1Mbaud can be selected by using different input frequencies (crystal or an external frequency input up to 16MHz) and/or different Prescaler and Divisor Select ratios.

Regardless of the baud rate, the baud rate generator provides a clock which is 16 times the desired baud rate. For example, in order to operate at a 1Mbaud data rate, a 16MHz crystal, a Prescale rate of ÷1, and a Divisor Select rate of "external" would be used. This would provide a 16MHz clock as the output of the Baud Rate Generator to the Transmitter and Receiver circuits.

The CO select bit in the BRSR selects whether a buffered version of the external frequency input (IX input) or the Baud Rate Generator output (16x baud rate clock) will be output on the CO output (pin 21). The Baud Rate Generator output will always be a 50% nominal duty cycle except when "external" is selected and the Prescaler is set to ÷3 or ÷5.

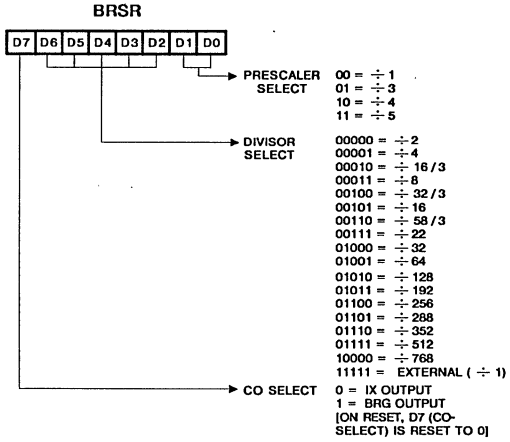


FIGURE 2.

TABLE B.

BAUD RATE	DIVISOR
38.4K	External
19.2K	2
9600	4
7200	16/3
4800	8
3600	32/3
2400	16
2000*	58/3
1800	22
1200	32
600	64
300	128
200	192
150	256
134.5*	288
110*	352
75	512
50	768

NOTE: These baud rates are based upon the following input frequency/Prescale divisor combinations.
1.8432MHz and Prescale = ÷3
2.4576MHz and Prescale = ÷4
3.072MHZ and Prescale = ÷5

*All baud rates are exact except for:

BAUD RATE	ACTUAL	PERCENT ERROR
1800	1745.45	3.03%
2000	1986.2	0.69%
134.5	133.33	0.87%
110	109.09	0.83%

Modem Control Register

The MCR is a general purpose control register which can be written to and read from. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their associated bits in this register. Note that a logic one asserts a true logic level (low) at these output pins. The Interrupt Enable (INTEN) bit is the overall control for the INTR output pin. When INTEN is false, INTR is held false (low).

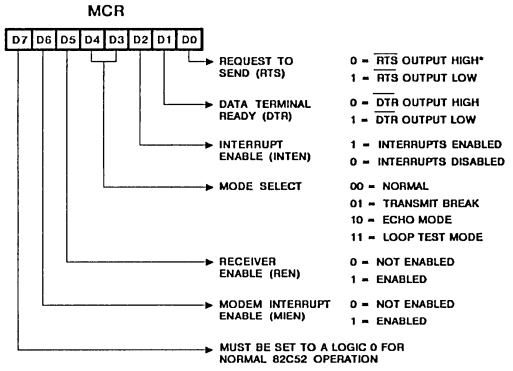
The Operating Mode bits configure the 82C52 into one of four possible modes. "Normal" configures the 82C52 for normal full or half duplex communications. "Transmit Break" enables the transmitter to only transmit break characters (Start, Data and Stop bits all are logic zero). The Echo Mode causes any data that is received on the SDI input pin to be retransmitted on the SDO output pin. Note that this output is a buffered version of the data seen on the SDI input and is not a resynchronized output. Also note that normal UART transmission via the Transmitter Register is disabled when operating in the Echo mode (see Figure 4). The Loop Test Mode internally routes transmitted data to the receiver circuitry for the purpose of self test. The

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

transmit data is disabled from the SDO output pin. The Receiver Enable bit gates off the input to the receiver circuitry when in the false state.

Modem Interrupt Enable will permit any change in modem status line inputs ($\overline{CTS}$, $\overline{DSR}$) to cause an interrupt when this bit is enabled. Bit D7 must always be written to with a logic zero to insure correct 82C52 operation.



*See Modem Status Register description for a description of register flag images with respect to output pins.

FIGURE 3.

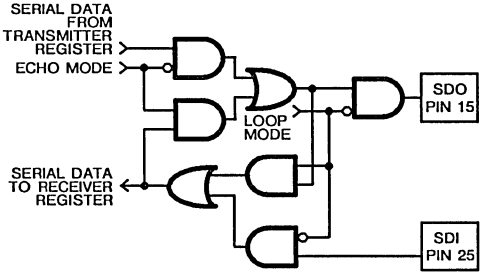


FIGURE 4. LOOP AND ECHO MODE FUNCTIONALITY

UART Status Register (USR)

The USR provides a single register that the controlling system can examine to determine if errors have occurred or if other status changes in the 82C52 require attention. For this reason, the USR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the 82C52.

Three error flags OE, FE and PE report the status of any error conditions detected in the receiver circuitry. These error flags are updated with every character received during reception of the stop bits. The Overrun Error (OE) indicates that a character in the Receiver Register has been received and cannot be transferred to the Receiver Buffer Register (RBR) because the RBR was not read by the CPU. Framing Error (FE) indicates that the last character received in the RBR contained improper stop bits. This could be caused by the absence of the required stop bit(s) or by a stop bit(s) that was too short to be properly detected. Parity Error (PE) indicates that the last character received in the RBR contained a parity error based on the programmed parity of the receiver and the calculated parity of the received character data and parity bits.

The Received Break (RBRK) status bit indicates that the last character received was a break character. A break character would be considered to be an invalid data character in that the entire character including parity and stop bits are a logic zero.

The Modem Status bit is set whenever a transition is detected on any of the Modem input lines ($\overline{CTS}$ or $\overline{DSR}$). A subsequent read of the Modem Status Register will show the state of these two signals. Assertion of this bit will cause an interrupt (INTR) to be generated if the MIEN and INTEN bits in the MCR register are enabled.

The Transmission Complete (TC) bit indicates that both the TBR and Transmitter Registers are empty and the 82C52 has completed transmission of the last character it was commanded to transmit. The assertion of this bit will cause an interrupt (INTR) if the INTEN bit in the MCR register is true.

The Transmitter Buffer Register Empty (TBRE) bit indicates that the TBR register is empty and ready to receive another character.

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Assertion of the TBRE or DR bits do not affect the INTR logic and associated INTR output pin since the 82C52 has been designed to provide separate requests via the DR and TBRE output pins. If a single interrupt for any status change in the 82C52 is desired this can be accomplished by using an 82C59A Interrupt controller with DR, TBRE, and INTR as inputs. (See Figure 11).

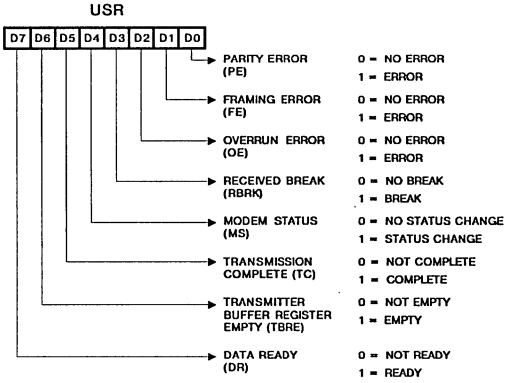


FIGURE 5.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Modem Status Register (MSR)

The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the 82C52. Like all of the register images of external pins in the 82C52, true logic levels are represented by a high (1) signal level. By following this consistent definition, the system software need not be concerned with whether external signals are high or low true. In particular, the modem signal inputs are low true, thus a 0 (true assertion) at a modem input pin is represented by a 1 (true) in the MSR.

Any change of state in any modem input signals will set the Modem Status (MS) bit in the USR register. When this happens, an interrupt (INTR) will be generated if the MIEN and INTEN bits of the MCR are enabled.

The Data Set Ready ($\overline{DSR}$) input is a status indicator from the modem to the 82C52 which indicates that the modem is ready to provide received data to the 82C52 receiver circuitry.

Clear to Send ($\overline{CTS}$) is both a status and control signal from the modem that tells the 82C52 that the modem is ready to receive transmit data from the 82C52 transmitter output (SDO). A high (false) level on this input will inhibit the 82C52 from beginning transmission and if asserted in the middle of a transmission will only permit the 82C52 to finish transmission of the current character.

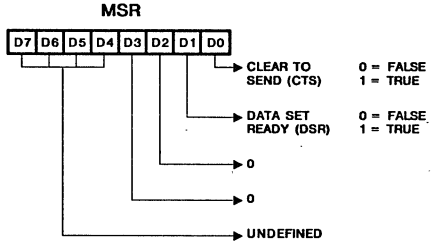


FIGURE 6.

Receiver Buffer Register (RBR)

The receiver circuitry in the 82C52 is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the Least Significant Bit (LSB = D0). Bit D0 of a data word is always the first data bit received. The unused bits in a less than 8 bit word, at the parallel interface, are set to a logic zero (0) by the 82C52.

Received data at the SDI input pin is shifted into the Receiver Register by an internal 1x clock which has been synchronized to the incoming data based on the position of the start bit. When a complete character has been shifted into the Receiver Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. Both the DR output pin and DR flag in the USR register are set. This double buffering of the received data permits continuous reception of data without losing any of the received data.

While the Receiver Register is shifting a new character into the 82C52, the Receiver Buffer Register is holding a previously received character for the system CPU to read. Failure to read the data in the RBR before complete reception of the next character can result in the loss of the data in the Receiver Register. The OE flag in the USR register indicates the overrun condition.

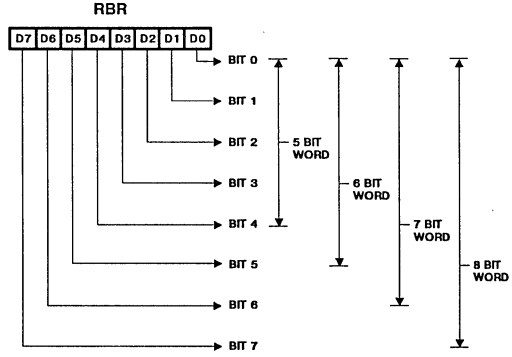


FIGURE 7.

Transmitter Buffer Register (TBR)

The Transmitter Buffer Register (TBR) accepts parallel data from the data bus (D0-D7) and holds it until the Transmitter Register is empty and ready to accept a new character for transmission. The transmitter always has the same word length and number of stop bits as the receiver. For words of less than 8 bits the unused bits at the microprocessor data bus are ignored by the transmitter.

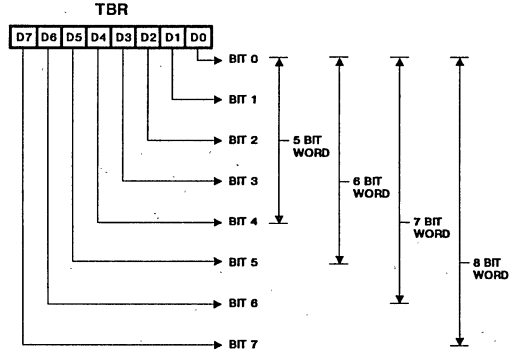


FIGURE 8.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Bit 0, which corresponds to D0 at the data bus, is always the first serial data bit transmitted. Provision is made for the transmitter parity to be the same or different from the receiver. The TBRE output pin and flag (USR register) reflect the status of the TBR. The TC flag (USR register) indicates when both TBR and TR are empty.

82C52 Interrupt Structure

The 82C52 has provisions for software masking of interrupts generated for the INTR output pin. Two control bits in the MCR register, MIEN and INTEN, control modem status interrupts and overall 82C52 interrupts respectively. Figure 9 illustrates the logical control function provided by these signals.

The modem status inputs ($\overline{DSR}$ and $\overline{CTS}$) will trigger the edge detection circuitry with any change of status. Reading the MSR register will clear the detect circuit but has no effect on the status bits themselves. These status bits always reflect the state of the input pins regardless of the mask control signals. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

The edge detection circuits for the USR register signals will trigger only for a positive edge (true assertion) of these status bits. Reading the USR register not only clears the edge detect circuit but also clears (sets to 0) all of the status bits. The output pins associated with these status bits are not affected by reading the USR register.

A hardware reset of the 82C52 sets the TC status bit in the USR. When interrupts are subsequently enabled an interrupt can occur due to the fact that the positive edge detection circuitry in the interrupt logic has detected the setting of the TC bit. If this interrupt is not desired the USR should be read prior to enabling interrupts. This action resets the positive edge detection circuitry in the interrupt control logic (Figure 9).

NOTE: For USR and MSR, the setting of status bits is inhibited during status register READ operations. If a status condition is generated during a READ operation, the status bit is not set until the trailing edge of the $\overline{RD}$ pulse.

If the bit was already set at the time of the READ operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the $\overline{RD}$ pulse instead of being set again.

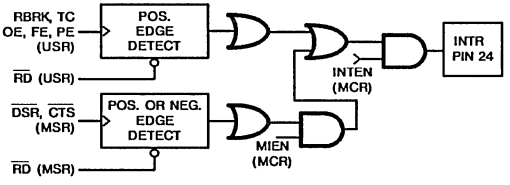


FIGURE 9. 82C52 INTERRUPT STRUCTURE

Software Reset

A software reset of the 82C52 is a useful method for returning to a completely known state without exercising a complete system reset. Such a reset would consist of writing to the UCR, BRSR and MCR registers. The USR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

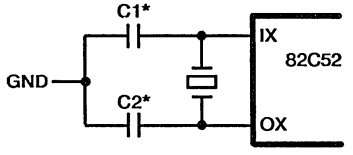
Crystal Operation

The 82C52 crystal oscillator circuitry is designed to operate with a fundamental mode, parallel resonant crystal. This circuit is the same one used in the Harris 82C84A clock generator/driver. To summarize, Table C and Figure 10 show the required crystal parameters and crystal circuit configuration respectively.

When using an external clock source, the IX input is driven and the OX output is left open. Power consumption when using an external clock is typically 50% of that required when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

TABLE C.

PARAMETER	TYPICAL CRYSTAL SPECIFICATION
Frequency	1.0 to 16MHz
Type of Operation	Parallel Resonant, Fundamental Mode
Load Capacitance (CL)	20 or 32pF (Typ)
R_{SERIES}(Max)	100 Ω (f = 16MHz, CL = 32pF) 200 Ω (f = 16MHz, CL = 20pF)



*C1 = C2 = 20pF FOR CL = 20pF
*C1 = C2 = 47pF FOR CL = 32pF

FIGURE 10.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

82C52 - 80C86 Interfacing

The following example (Figure 11) shows the interface for an 82C52 in an 80C86 system.

Use of the Harris CMOS Interrupt Controller (82C59A) is optional and necessary only if an interrupt driven system is desired.

By using the Harris CMOS 82C84A clock generator, the system can be built with a single crystal providing both the processor clock and the clock for the 82C52. The 82C52 has special divider circuitry which is designed to supply industry standard baud rates with a 2.4576MHz input frequency. Using a 15MHz crystal as shown, results in less than a 2% frequency error which is adequate for many applications. For more precise baud rate requirements, a 14.7456MHz crystal will drive the 80C86 at 4.9MHz and provide the 82C52 with the standard baud rate input frequency of 2.4576MHz. If baud rates above 156Kbaud are desired, the OSC output can be used instead of the PCLK (÷6) output for asynchronous baud rates up to 1 Mbaud.

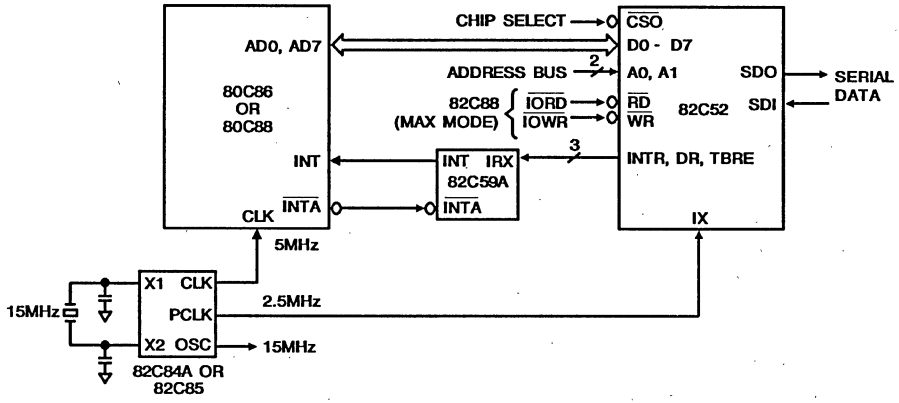


FIGURE 11. 80C86/82C52 INTERFACE

HARRIS

82C54/883

June 1989

CMOS Programmable Interval Timer

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Compatible with NMOS 8254
  - Enhanced Version of NMOS 8253
- 8MHz Clock Input Frequency
- Three Independent 16 Bit Counters
- Six Programmable Counter Modes
- Status Read Back Command
- Binary of BCD Counting
- Fully TTL Compatible
- Scaled SAJI IV CMOS Process
- Single 5V Power Supply
- Low Power - ICCSB = 10μA
- Military Operating Temperature Range ..... -55°C to +125°C

Description

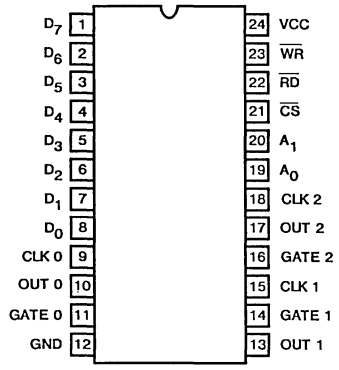
The Harris 82C54/883 is a high performance CMOS Programmable Interval Timer manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C54/883 has three independently programmable and functional 16 bit counters, each capable of handling clock input frequencies of up to 8MHz. The high speed and industry standard configuration of the 82C54/883 make it compatible with the Harris 80C86 and 80C88 CMOS microprocessors along with many other industry standard processors.

Six programmable timer modes allow the 82C54/883 to be used as an event counter, elapsed time indicator, programmable one-shot along with many other applications.

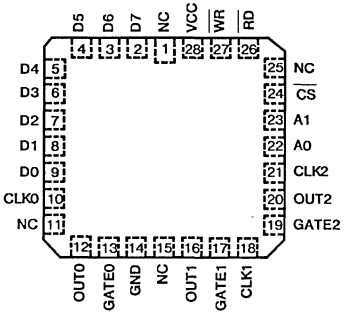
Static CMOS circuit design insures low operating power. Harris advanced SAJI process results in a significant reduction in power with performance equal to or greater than existing functionally equivalent products.

Pinouts

82C54/883 (CERAMIC DIP)
TOP VIEW

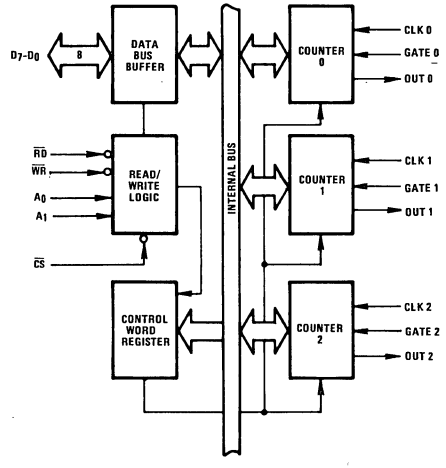


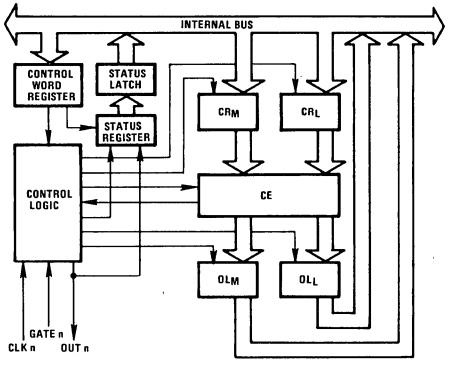
82C54/883 (CERAMIC LCC)
TOP VIEW



5 CMOS PERIPHERALS

Functional Diagram





COUNTER INTERNAL BLOCK DIAGRAM

Pin Description

SYMBOL	DIP PIN NUMBER	TYPE	DEFINITION
D7-D0	1-8	I/O	DATA: Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	CLOCK 0: Clock input of Counter 0.
OUT 0	10	O	OUT 0: Output of Counter 0.
GATE 0	11	I	GATE 0: Gate input of Counter 0.
GND	12		GROUND: Power supply connection.
OUT 1	13	O	OUT 1: Output of Counter 1.
GATE 1	14	I	GATE 1: Gate input of Counter 1.
CLK 1	15	I	CLOCK 1: Clock input of Counter 1.
GATE 2	16	I	GATE 2: Gate input of Counter 2.
OUT 2	17	O	OUT2: Output of Counter 2.
CLK 2	18	I	CLOCK 2: Clock input of Counter 2.
A0, A1	19-20	I	ADDRESS: Select inputs for one of the three counters or Control Word Register for read/write operations. Normally connected to the system address bus.
$\overline{CS}$	21	I	CHIP SELECT: A low on this input enables the 82C54 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
$\overline{RD}$	22	I	READ: This input is low during CPU read operations.
$\overline{WR}$	23	I	WRITE: This input is low during CPU write operations.
VCC	24		VCC: The +5V power supply Pin. A 0.1µF capacitor between pins VCC and GND is recommended for decoupling.

A1	A0	SELECTS
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec)..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	47°C/W	8°C/W
Ceramic LCC Package	49°C/W	5°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.07W
Ceramic LCC Package 1.03W
Gate Count ..... 2250 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Voltage Range ..... +4.5V to 5.5V

TABLE 1. 82C54/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	VIH	VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.2	-	V
Logical Zero Input Voltage	VIL	VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.8	V
Output High Voltage	VOH	VCC = 4.5V, IOH = -2.5mA, IOH = -100µA (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	3.0 VCC-0.4	-	V
Output Low Voltage	VOL	VCC = 4.5V, IOL = +2.5mA (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Input Leakage Current	II	VCC = 5.5V, VIN = GND or VCC, DIP Pins 9, 11, 14-16, 18-23	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
I/O Leakage Current	IO	VCC = 5.5V, VIN = GND or VCC, DIP Pins 1-8	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-10.0	+10.0	µA
Standby Power Supply Current	ICCSB	VCC = 5.5V, Outputs Open Counters Programmed	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA
Operating Supply Current	ICCOP	VCC = 5.5V, CLK0 = CLK1 = CLK2 = 8MHz, Outputs Open	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	mA

NOTE: 1. Interchanging of force and sense conditions is permitted.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. 82C54/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Stable Before $\overline{RD}$	TAR(1)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	ns
$\overline{CS}$ Stable Before $\overline{RD}$	TSR(2)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Address Hold Time After $\overline{RD}$	TRA(3)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
$\overline{RD}$ Pulse Width	TRR(4)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Data Delay from $\overline{RD}$	TRD(5)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	120	ns
Data Delay from Address	TAD(6)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	210	ns
Command Recovery Time	TRV(8)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	200	-	ns
WRITE CYCLE TIMING							
Address Stable Before $\overline{WR}$	TAW(9)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
$\overline{CS}$ Stable Before $\overline{WR}$	TSW(10)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Address Hold Time After $\overline{WR}$	TWA(11)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
$\overline{WR}$ Pulse Width	TWW(12)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	95	-	ns
Data Setup Time Before $\overline{WR}$	TDW(13)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	140	-	ns
Data Setup Time Before $\overline{WR}$	TWD(14)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	25	-	ns
Command Recovery Time	TRV(15)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	200	-	ns
CLOCK AND GATE TIMING							
Clock Period	TCLK(16)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	125	-	ns
High Pulse Width	TPWH(17)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	60	-	ns
Low Pulse Width	TPWL(18)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	60	-	ns
Gate Width High	TGW(21)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Gate Width Low	TGL(22)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Gate Setup Time to CLK	TGS(23)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Gate Hold Time to CLK	TGH(24)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Output Delay from CLK	TOD(25)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	150	ns
Output Delay from GATE	TODG(26)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	120	ns
OUT Delay from Mode Write	TWO(27)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	260	ns

NOTES: 1. Tested as follows: f = 1MHz, VIH = 2.6V, VIL = 0.4V, CL = 50pf (Unless Otherwise Specified), VOH $\geq$ 1.5V, VOL $\leq$ 1.5V.

2. Outputs loaded as shown in Test Condition 1.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. 82C54/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	-	10	pF
Output Capacitance	COUT	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	-	20	pF
I/O Capacitance	CI/O	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	-	20	pF
$\overline{RD}$ to Data Floating Time	TDF(7)	VCC = 4.5V and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	5	85	ns
Clock Period	TCLK(16)	VCC = 4.5V and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	DC	ns
Clock Rise Time	TR(19)	VCC = 4.5V and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	25	ns
Clock Fall Time	TF(20)	VCC = 4.5V and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	25	ns

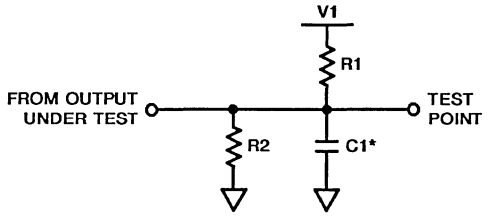
NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. Tested as follows: f = 1MHz, VIH = 2.6V, VIL = 0.4V, CL = 50pF, VOH $\geq$ 1.5V, VOL $\leq$ 1.5V. Tested using Test Condition 2 of Test Condition Definition Table.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Test Load Circuit

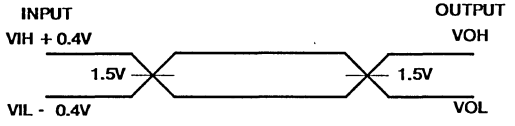


* Includes Stray and Jig Capacitance

TEST CONDITION DEFINITION TABLE

TEST CONDITION	V1	R1	R2	C1
1	1.7V	523	OPEN	150pF
2	VCC	2K	1.7K	50pF

A.C. Testing Input, Ouput Waveform

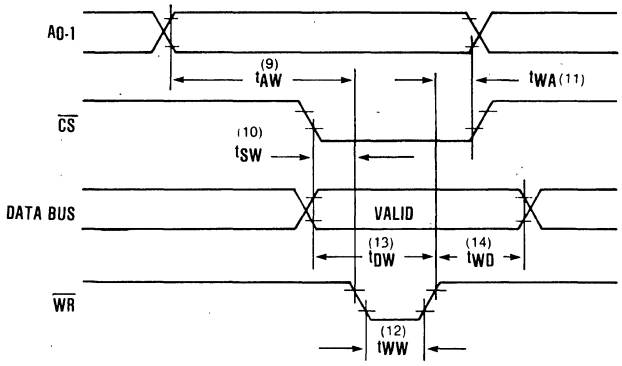


A.C. Testing: All input signals must switch between VIL -0.4V and VIH +0.4V. Input rise and fall times are driven at 1ns/V.

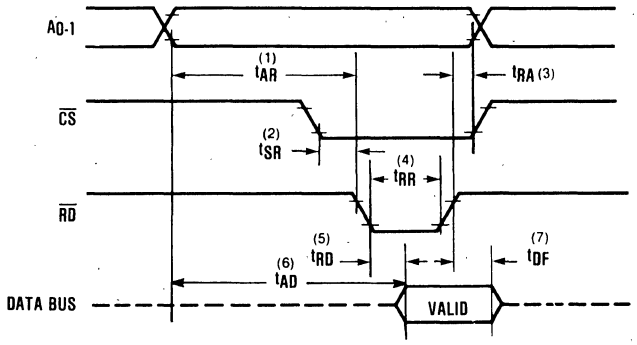
CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

Timing Waveforms

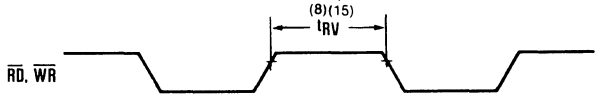
WRITE



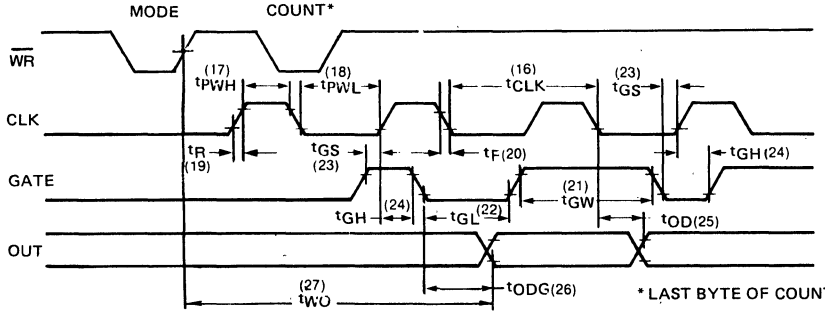
READ



RECOVERY



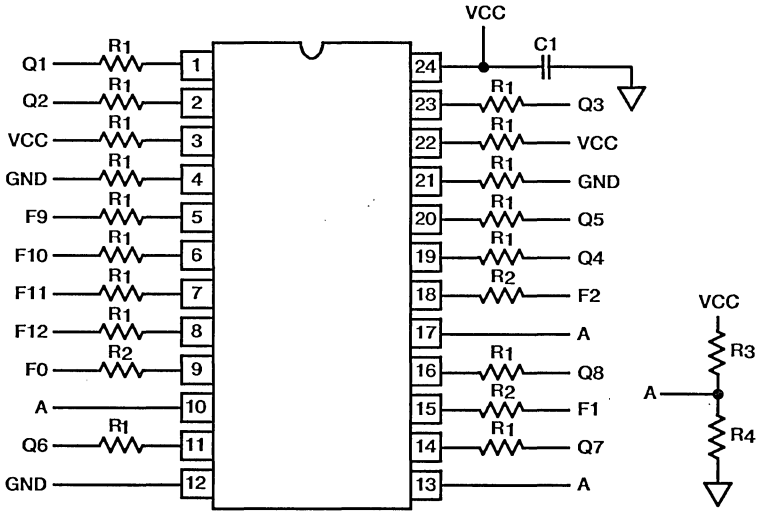
CLOCK AND GATE



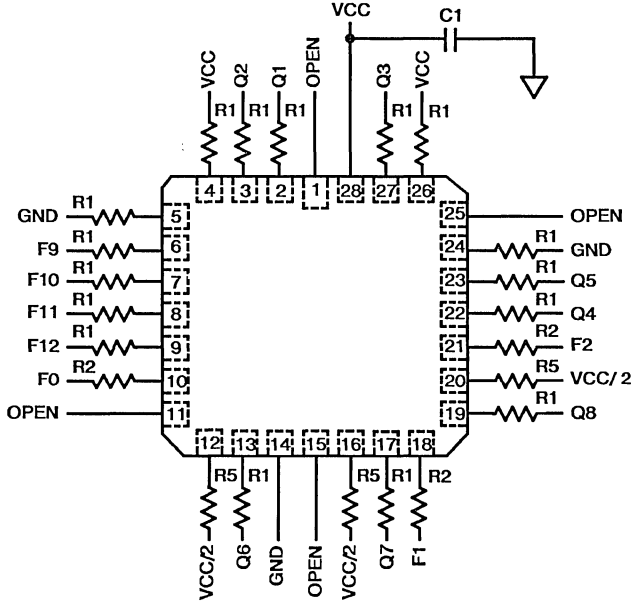
* LAST BYTE OF COUNT BEING WRITTEN

Burn-In Circuits

82C54/883 CERAMIC DIP



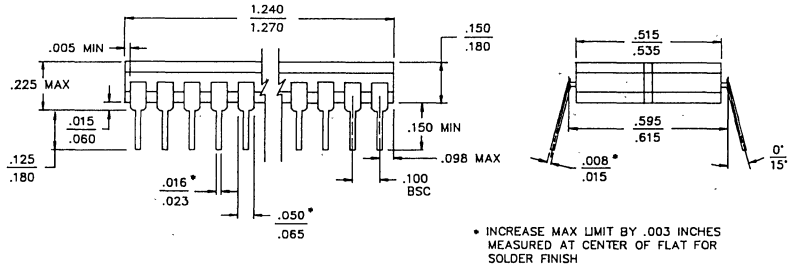
82C54/883 CERAMIC LCC



VCC = 5.5V ± 0.5V,
GND = 0V
VIN = 4.5V ± 10%
VIL = -0.2V to 0.4V
R1 = 47kΩ ± 5%
R2 = 1.0kΩ ± 5%
R3 = 2.7kΩ ± 5%
R4 = 1.8kΩ ± 5%
R5 = 1.2kΩ ± 5%
C1 = 0.01μF Minimum
f0 = 100kHz ± 10%
f1 = f0/2, f2 = f1/2, . . . f12 = f11/2

Packaging†

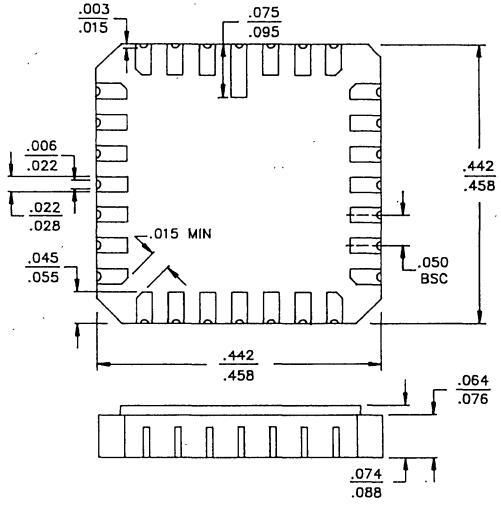
24 PIN CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-3

28 PAD CERAMIC LCC
BOTTOM VIEW



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-4

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

Metallization Topology

DIE DIMENSIONS:
183.5 x 215.7 x 19 ± 1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 2kÅ

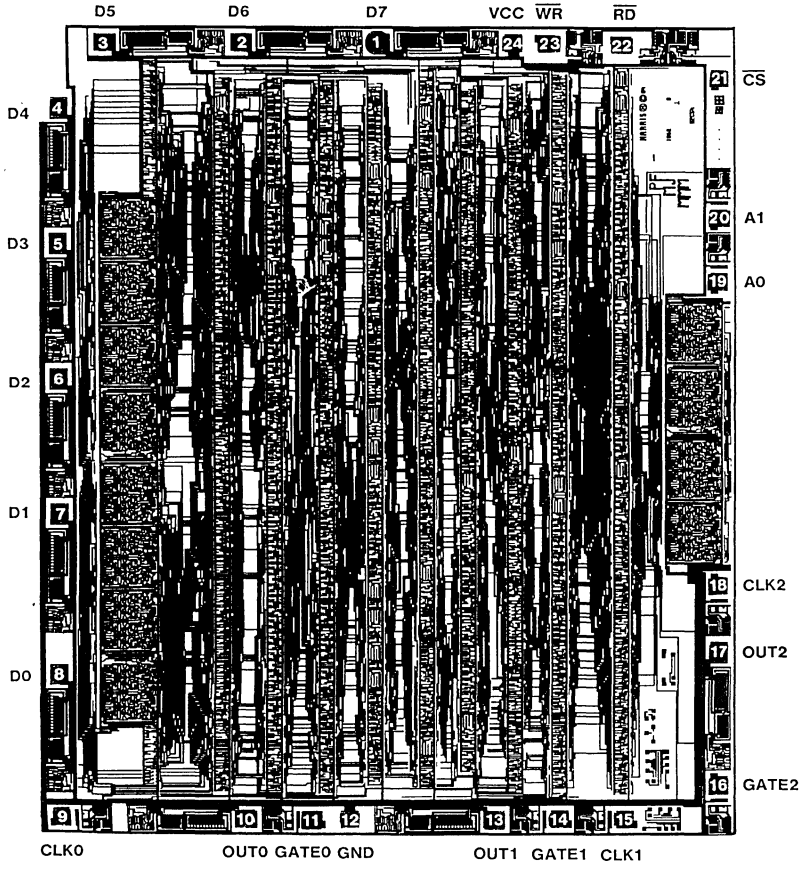
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy (LCC has Gold Preform)
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
0.26 x 10^5 A/cm^2

Metallization Mask Layout

82C54/883



The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Functional Description

General

The 82C54 is a programmable interval timer/counter designed for use with microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 82C54 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 82C54 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 82C54 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other computer/timer functions common to microcomputers which can be implemented with the 82C54 are:

- Real time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Data Bus Buffer

This three-state, bi-directional, 8-bit buffer is used to interface the 82C54 to the system bus (see Figure 1).

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 82C54. A1 and A0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the $\overline{RD}$ input tells the 82C54 that the CPU is reading one of the counters. A "low" on the $\overline{WR}$ input tells the 82C54 that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the 82C54 has been selected by holding $\overline{CS}$ low.

Control Word Register

The Control Word Register (Figure 2) is selected by the Read/Write Logic when A1, A0 = 11. If the CPU then does a write operation to the 82C54, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the Counter operation.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

Counter 0, Counter 1, Counter 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 3. The counters are fully independent. Each Counter may operate in a different Mode.

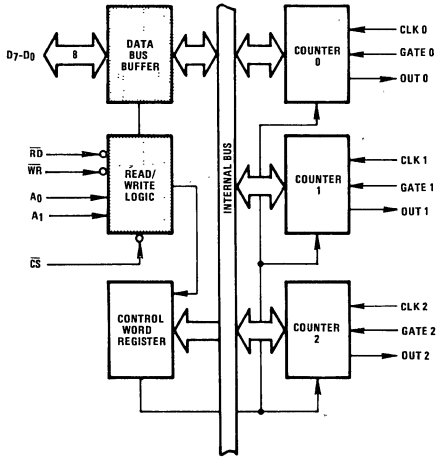


FIGURE 1. DATA BUS BUFFER AND READ/WRITE LOGIC FUNCTIONS

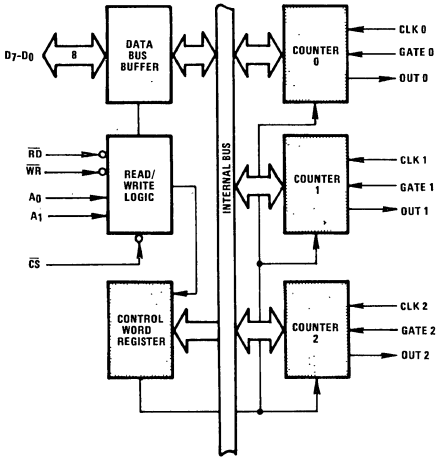


FIGURE 2. CONTROL WORD REGISTER AND COUNTER FUNCTIONS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

The status register, shown in the figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labeled CE (for Counting Element). It is a 16 bit presettable synchronous down counter.

OLM and OLL are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L for "Most significant byte" and "Least significant byte", respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the 82C54, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CRM and CRL (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CRM and CRL are cleared when the Counter is programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

82C54 System Interface

The 82C54 is treated by the system software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method or it can be connected to the output of a decoder, such as a Harris HD-6440 for larger systems.

Operational Description

General

After power-up, the state of the 82C54 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming The 82C54

Counters are programmed by writing a Control Word and then an initial count.

All Control Words are written into the Control Word Register, which is selected when A1, A0 = 11. The Control Word specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A1, A0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

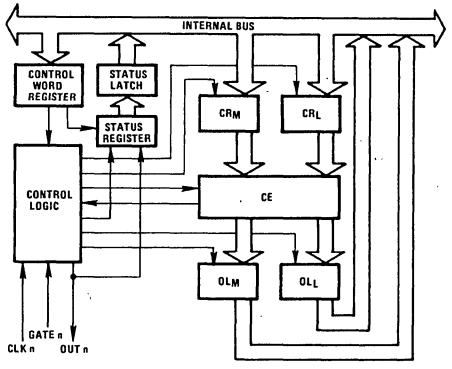


FIGURE 3. COUNTER INTERNAL BLOCK DIAGRAM

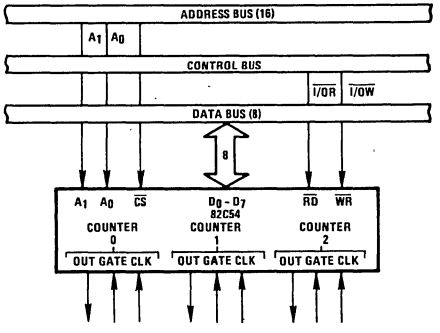


FIGURE 4. 82C54 SYSTEM INTERFACE

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Write Operations

The programming procedure for the 82C54 is very flexible. Only two conventions need to be remembered:

1. For each Counter, the Control Word must be written before the initial count is written.
2. The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A1, A0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

Control Word Format

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC - Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW - Read/Write:

RW1	RW0	
0	0	Counter Latch Command (See Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M - Mode:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD - Binary Coded Decimal:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

FIGURE 5. CONTROL WORD FORMAT

	A1	A0
Control Word - Counter 0	1	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 0	0	0
Control Word - Counter 1	1	1
LSB of Count - Counter 1	0	1
MSB of Count - Counter 1	0	1
Control Word - Counter 2	1	1
LSB of Count - Counter 2	1	0
MSB of Count - Counter 2	1	0

	A1	A0
Control Word - Counter 0	1	1
Control Word - Counter 1	1	1
Control Word - Counter 2	1	1
LSB of Count - Counter 2	1	0
LSB of Count - Counter 1	0	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 0	0	0
MSB of Count - Counter 1	0	1
MSB of Count - Counter 2	1	0

	A1	A0
Control Word - Counter 2	1	1
Control Word - Counter 1	1	1
Control Word - Counter 0	1	1
LSB of Count - Counter 2	1	0
MSB of Count - Counter 2	1	0
LSB of Count - Counter 1	0	1
MSB of Count - Counter 1	0	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 0	0	0

	A1	A0
Control Word - Counter 1	1	1
Control Word - Counter 0	1	1
LSB of Count - Counter 1	0	1
Control Word - Counter 2	1	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 1	0	1
LSB of Count - Counter 2	1	0
MSB of Count - Counter 0	0	0
MSB of Count - Counter 2	1	0

NOTE: In all four examples, all counters are programmed to Read/Write two-byte counts. These are only four of many programming sequences.

FIGURE 6. A FEW POSSIBLE PROGRAMMING SEQUENCES

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 82C54.

There are three possible methods for reading the Counters. The first is through the Read-Back command, which is explained later. The second is a simple read operation of the Counter, which is selected with the A1, A0 inputs. The only requirement is that the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in process of changing when it is read, giving an undefined result.

Counter Latch Command

The other method for reading the Counters involves a special software command called the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when A1, A0 = 11. Also, like a Control Word, the SC0, SC1 bits select one of the three Counters; but two other bits, D5 and D4, distinguish this command from a Control Word.

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - specify counter to be latched

SC1	SC0	COUNTER
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5, D4 - 00 designates Counter Latch Command
X - Don't Care

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

FIGURE 7. COUNTER LATCH COMMAND FORMAT

The selected Counter's output latch (OL) latches the count when the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the 82C54 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a Counter is programmed to read or write two-byte counts, the following precaution applies: A program MUST NOT transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

Read-Back Command

The read-back command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 8. The command applies to the counters selected by setting their corresponding bits D3, D2, D1 = 1.

A0, A1 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT 2	CNT 1	CNT 0	0

D5: 0 = Latch count of selected Counter(s)
D4: 0 = Latch status of selected Counter(s)
D3: 1 = Select Counter 2
D2: 1 = Select Counter 1
D1: 1 = Select Counter 0
D0: Reserved for future expansion; Must be 0

FIGURE 8. READ-BACK COMMAND FORMAT

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

The read-back command may be used to latch multiple counter output latches (OL) by setting the COUNT bit D5 = 0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting STATUS bit D4 = 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in Figure 9. Bits D5 through D0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D7 1 = Out pin is 1
0 = Out pin is 0
D6 1 = Null count
0 = Count available for reading
D5-D0 = Counter programmed mode (See Figure 5)

FIGURE 9. STATUS BYTE

NULL COUNT bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the counter is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 10.

THIS ACTION:	CAUSES:
A. Write to the control word register: (1)	Null Count = 1
B. Write to the count register (CR): (2)	Null Count = 1
C. New count is loaded into CE (CR - CE)	Null Count = 0

(1) Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected.

(2) If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.

FIGURE 10. NULL COUNT OPERATION

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both COUNT and STATUS bits D5, D4 = 0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 11. If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

COMMAND								DESCRIPTION	RESULT
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	1	0	Read Back Count and Status of Counter 0	Count and Status Latched for Counter 0
1	1	1	0	0	1	0	0	Read-Back Status of Counter 1	Status Latched for Counter 1
1	1	1	0	1	1	0	0	Read-Back Status of Counters 2, 1	Status Latched for Counter 2, But Not Counter 1
1	1	0	1	1	0	0	0	Read-Back Count of Counter 2	Count Latched for Counter 2
1	1	0	0	0	1	0	0	Read-Back Count and Status of Counter 1	Count Latched for Counter 1 But Not Status
1	1	1	0	0	0	1	0	Read-Back Status of Counter 1	Command Ignored, Status Already Latched for Counter 1

FIGURE 11. READ-BACK COMMAND EXAMPLE

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (Three-State)
1	X	X	X	X	No-Operation (Three-State)
0	1	1	X	X	No-Operation (Three-State)

FIGURE 12. READ/WRITE OPERATIONS SUMMARY

Mode Definitions

The following are defined for use in describing the operation of the 82C54.

CLK PULSE:
A rising edge, then a falling edge, in that order, of a Counter's CLK input.

TRIGGER:
A rising edge of a Counter's Gate input.

COUNTER LOADING:
The transfer of a count from the CR to the CE
(See "Functional Description")

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written to the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

(1) Writing the first byte disables counting. Out is set low immediately (no clock pulse required).

(2) Writing the second byte allows the new count to be loaded on next CLK pulse.

This allows the counting sequence to be synchronized by software. Again OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the counter as this has already been done.

Mode 1: Hardware Retriggerable One-Shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

Mode 2: Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

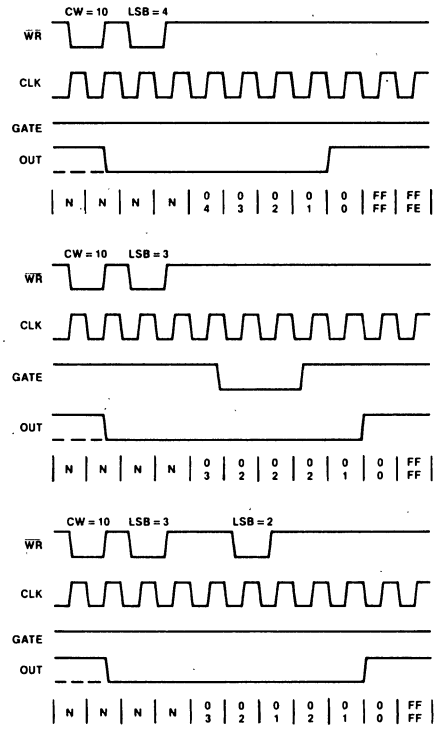
GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.



NOTE: The following conventions apply to all mode timing diagrams.

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a control word of 10, Hex is written to the counter.
4. LSB stands for Least significant "byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

FIGURE 13. MODE 0

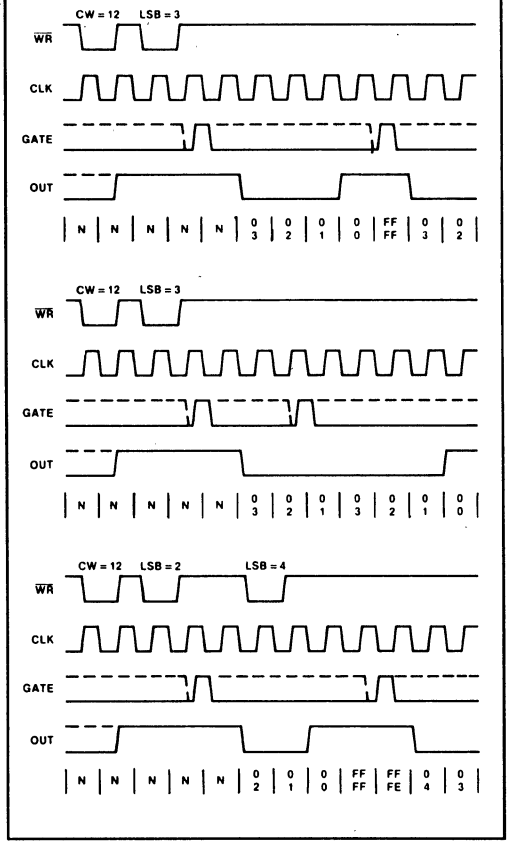


FIGURE 14. MODE 1

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is Implemented as Follows:

EVEN COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires, OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

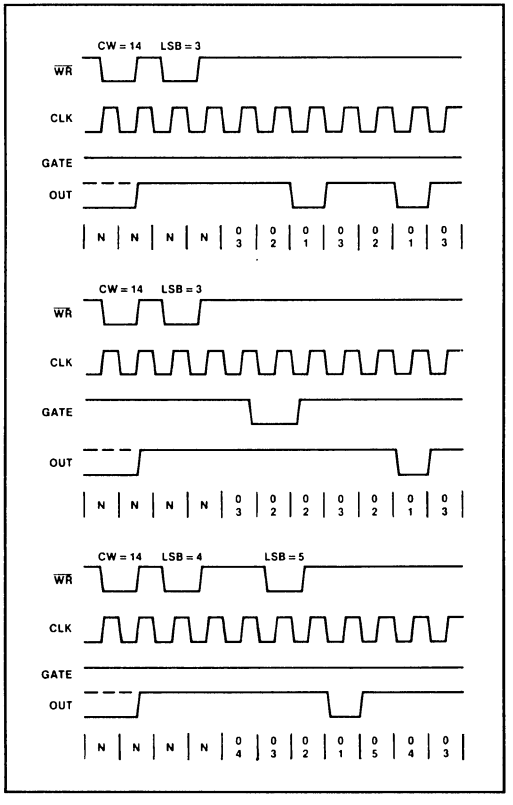


FIGURE 15. MODE 2

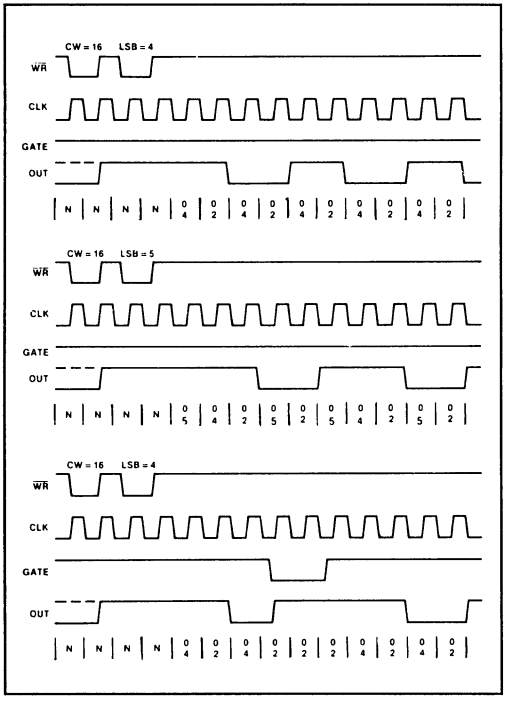


FIGURE 16. MODE 3

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

ODD COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse, decremented by one on the next CLK pulse, and then decremented by two on succeeding CLK pulses. When the count expires, OUT goes low and the Counter is reloaded with the initial count. The count is decremented by three on the next CLK pulse, and then by two on succeeding CLK pulses. When the count expires, OUT goes high again and the Counter is reloaded with the initial count. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N + 1)/2 counts and low for (N - 1)/2 counts.

Mode 4: Software Triggered Mode

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse then go high again. The counting sequence is "Triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

(1) Writing the first byte has no effect on counting.

(2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

Mode 5: Hardware Triggered Strobe (Retriggerable)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

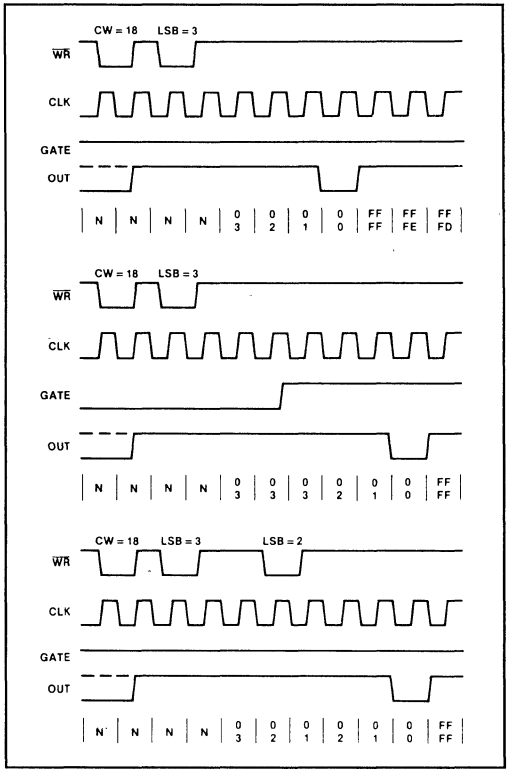


FIGURE 17. MODE 4

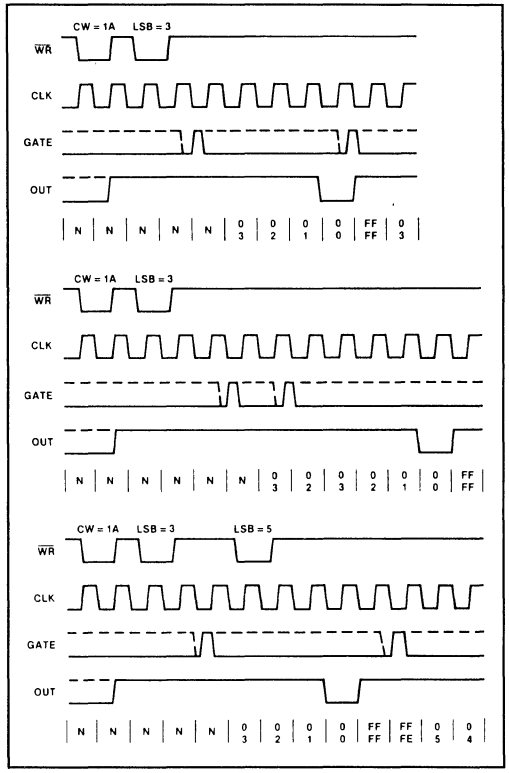


FIGURE 18. MODE 5

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is triggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Operation Common to All Modes

Programming

When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

Gate

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3 and 4 the GATE input is level sensitive, and logic level is sampled on the rising edge of CLK. In modes 1, 2, 3 and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of Gate (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK. The flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs - a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge-and level-sensitive.

Counter

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The counter does not stop when it reaches zero. In Modes 0, 1, 4 and 5 the Counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

SIGNAL STATUS MODES	LOW OR GOING LOW	RISING	HIGH
0	Disables counting	-	Enables counting
1	-	1) Initiates counting 2) Resets output after next clock	-
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	1) Disables counting	-	Enables counting
5	-	Initiates counting	-

FIGURE 19. GATE PIN OPERATIONS SUMMARY

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

NOTE: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

FIGURE 20. MINIMUM AND MAXIMUM INITIAL COUNTS

HARRIS

82C55A/883

CMOS Programmable Peripheral Interface

June 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is fully Conformant Under the Provisions of Paragraph 1.2.1
- Pin Compatible with NMOS 8255A
- 24 Programmable I/O Pins
- Fully TTL Compatible
- High Speed, No "Wait State" Operation with 5MHz and 8MHz 80C86 and 80C88
- Direct Bit Set/Reset Capability
- Enhanced Control Word Read Capability
- Scaled SAJI IV CMOS Process
- 2.5mA Drive Capability on All I/O Ports
- Low Standby Power - ICCSB 10μA
- Military Operating Temperature ... -55°C to +125°C Range

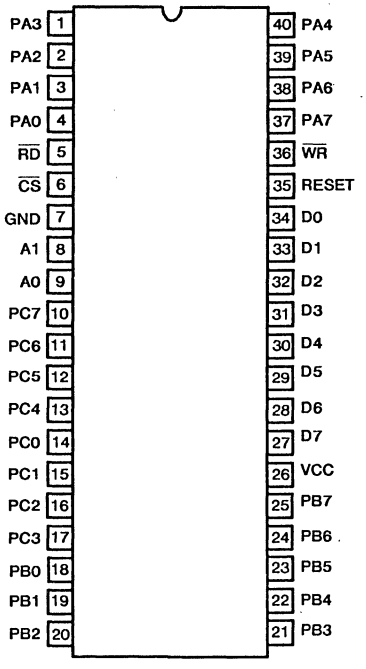
Description

The Harris 82C55A/883 is a high performance CMOS version of the industry standard 8255A and is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance and industry standard configuration of the 82C55A/883 make it compatible with the 80C86, 80C88 and other microprocessors.

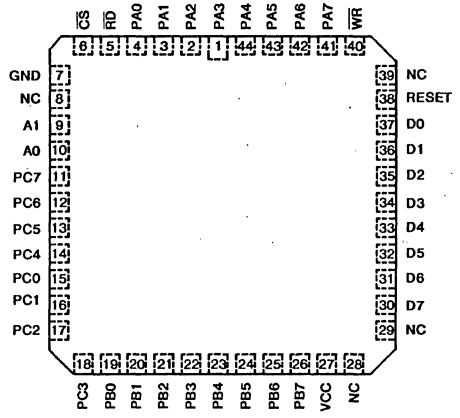
Static CMOS circuit design insures low operating power. TTL compatibility over the full military temperature range and bus hold circuitry eliminate the need for pull-up resistors. The Harris advanced SAJI process results in performance equal to or greater than existing functionally equivalent products at a fraction of the power.

Pinouts

82C55A/883 (CERAMIC DIP)
TOP VIEW



82C55A/883 (LCC)
TOP VIEW



PIN NAMES

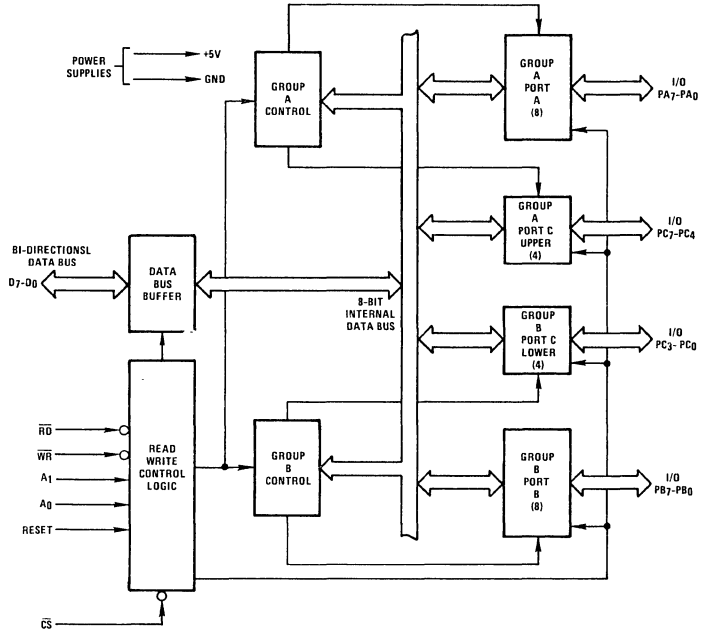
PIN	DESCRIPTION
D7 - D8	Data Bus (Bi-directional)
Reset	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0, A1	Port Address
PA7 - PA0	Port A (Bit)
PB7 - PB0	Port B (Bit)
PC7 - PC0	Port C (Bit)
VCC*	+5 Volts
GND*	0 Volts

* A 0.1μF decoupling capacitor from the VCC pin to the GND pin is recommended.

Pin Description

SYMBOL	DIP PIN NUMBER	TYPE	DESCRIPTION
VCC	26		VCC: the +5V power supply pin. A 0.1μF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7		GROUND
D0-D7	27-34	I/O	DATA BUS: The Data Bus lines are bidirectional three-state pins connected to the system data bus.
RESET	35	I	RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode with the "Bus Hold" circuitry turned on.
$\overline{CS}$	6	I	CHIP SELECT: Chip select is an active low input used to enable the 82C55A/883 onto the Data Bus for CPU communications.
$\overline{RD}$	5	I	READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus.
$\overline{WR}$	36	I	WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A/883.
A0-A1	8, 9	I	ADDRESS: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word register. A0 and A1 are normally connected to the least significant bits of the Address Bus A0, A1).
PA0-PA7	1-4, 37-40	I/O	PORT A: 8 Bit input and output port. Both bus hold high and bus hold low circuitry are present on this port.
PB0-PB7	18-25	I/O	PORT B: 8 Bit input and output port. Bus hold high circuitry is present on this port.
PC0-PC7	10-17	I/O	PORT C: 8 Bit input and output port. Bus hold high circuitry is present on this port.

Functional Description



Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	40°C/W	10°C/W
Ceramic LCC Package	70°C/W	16°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.23W
Ceramic LCC Package 718mW
Gate Count ..... 1000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... +4.5V to +5.5V

TABLE 1. 82C55A/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical "1" Input Voltage	VIH	VCC = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	2.2	-	V
Logical "0" Input Voltage	VIL	VCC = 4.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.8	V
Output HIGH Voltage	VOH	VCC = 4.5V, IOH = -2.5mA IOH = -100µA (Note 2)	1, 2, 3	$-55°C \le T_A \le +125°C$	3.0 VCC-0.4	-	V
Output LOW Voltage	VOL	VCC = 4.5V, IOL = 2.5mA (Note 2)	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Input Leakage Current	II	VCC = 5.5V, VIN = GND or VCC DIP Pins: 5, 6, 8, 9, 35, 36	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Output Leakage Current	IO	VCC = 5.5V, VIN = GND or VCC DIP Pins: 27 - 34	1, 2, 3	$-55°C \le T_A \le +125°C$	-10	+10	µA
Bus Hold High Current	IBHH	VCC = 4.5V and 5.5V VOUT = 3.0V, Ports A, B, C	1, 2, 3	$-55°C \le T_A \le +125°C$	-50	-400	µA
Bus Hold Low Current	IBHL	VCC = 4.5V and 5.5V VOUT = 1.0V, Port A Only	1, 2, 3	$-55°C \le T_A \le +125°C$	+50	+400	µA
Darlington Drive Current	IDAR	VCC = 4.5V, VIN = VCC or GND, Outputs Open VOUT = VCC, Ports A, B, C (Note 3)	1, 2, 3	$-55°C \le T_A \le +125°C$	-2.0	(Note 1)	mA
Standby Power Supply Current	ICCSB	VCC = 5.5V, VIN = VCC or GND, Outputs Open	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	µA

NOTES: 1. No internal current limiting resistor exists on Port Outputs. A resistor must be added externally to limit the current.
2. Interchanging of force and sense conditions is permitted.
3. Tested using Test Conditions 3 in Test Condition Definition Table.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. 82C55A/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

TIMING REQUIREMENTS									
					LIMITS				
					82C55A-5/883		82C55A/883		
PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	MIN	MAX	MIN	MAX	UNITS
READ TIMINGS									
Address Stable Before $\overline{READ}$	TAR(1)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
Address Stable After $\overline{READ}$	TRA(2)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
$\overline{READ}$ Pulse Width	TRR(3)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	250	-	150	-	ns
Data Valid From $\overline{READ}$	TRD(4)	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	200	-	120	ns
Time Between $\overline{READ'S}$ and/or $\overline{WRITE'S}$	TRV(6)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	300	-	300	-	ns
WRITE TIMING									
Address Stable Before $\overline{WRITE}$	TAW(7)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
Address Stable After $\overline{WRITE}$	TWA(8)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	20	-	ns
$\overline{WRITE}$ Pulse Width	TWW(9)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	100	-	ns
Data Valid to $\overline{WRITE}$ High	TDW(10)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	100	-	ns
Data Valid After $\overline{WRITE}$ High	TWD(11)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	30	-	ns
OTHER TIMINGS									
$\overline{WR}$ = 1 to Output	TWB(12)	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	350	-	350	ns
Peripheral Data Before $\overline{RD}$	TIR(13)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
Peripheral Data After $\overline{RD}$	THR(14)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
$\overline{ACK}$ Pulse Width	TAK(15)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	200	-	200	-	ns
$\overline{STB}$ Pulse Width	TST(16)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	100	-	ns
Peripheral Data Before $\overline{STB}$ High	TPS(17)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	20	-	ns
Peripheral Data After $\overline{STB}$ High	TPH(18)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	50	-	ns
$\overline{ACK}$ = 0 to Output	TAD(19)	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	175	-	175	ns
$\overline{WR}$ = 1 to $\overline{OBF}$ = 0	TWOS(21)	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	150	-	150	ns
$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1	TAOS(22)	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	150	-	150	ns
$\overline{STB}$ = 0 to IBF = 1	TSIB(23)	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	150	-	150	ns
$\overline{RD}$ = 1 to IBF = 0	TRIB(24)	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	150	-	150	ns
$\overline{RD}$ = 0 to INTR = 0	TRIT(25)	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	200	-	200	ns
$\overline{STB}$ = 1 to INTR = 1	TSIT(26)	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	150	-	150	ns
$\overline{ACK}$ = 1 to INTR =1	TAIT(27)	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	150	-	150	ns
$\overline{WR}$ = 0 to INTR = 0	TWIT(28)	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	200	-	200	ns
Reset Pulse Width	TRES(29)	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	500	-	500	-	ns

NOTES: 1. Tested as follows: f = 1MHz, VIH = 2.6V, VIL = 0.4V, CL = 50pF (unless otherwise specified), VOH $\geq$ 1.5V, VOL $\leq$ 1.5V, VCC = 4.5V and 5.5V.
2. Tested using Test Condition 1 in Test Condition Definition Table.
3. Period of initial Reset pulse after power-on must be at least 50µs. Subsequent Reset pulses may be 500ns minimum.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. 82C55A/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	-	10	pF
I/O Capacitance	CI/O	VCC = OPEN, f = 1MHz, All Measurements Reference to Device GND	1	$T_A = +25^oC$	-	20	pF
Operating Power Supply Current	ICCOP	VCC = 5.5 V, VIN = VCC or GND, Outputs Open	1	$-55^oC \leq T_A \leq +125^oC$	-	10	mA

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	82C55A-5/883 MIN	82C55A-5/883 MAX	82C55A/883 MIN	82C55A/883 MAX	UNITS
Data Float After $\overline{READ}$	TDF(5)		1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	10	75	10	75	ns
$\overline{ACK}$ = 1 to Output	TKD(20)		1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	20	250	20	250	ns

NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Tested as follows: f = 1MHz, VIH = 2.6V, VIL = 0.4V, CL = 50pF, VOH $\geq$ 1.5V, VOL $\leq$ 1.5V, VCC = 4.5V and 5.5V.
3. Tested under Test Condition 2 in Test Condition Definition Table.

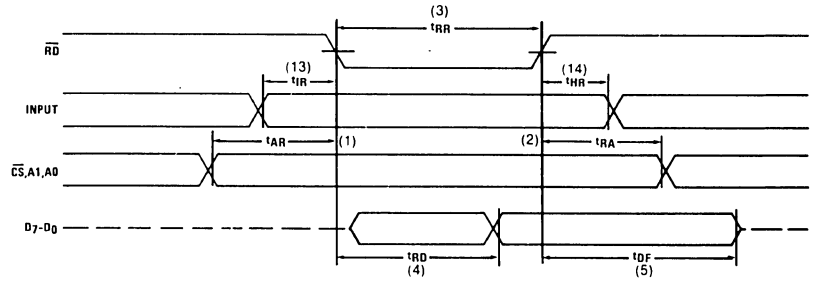
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 8
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

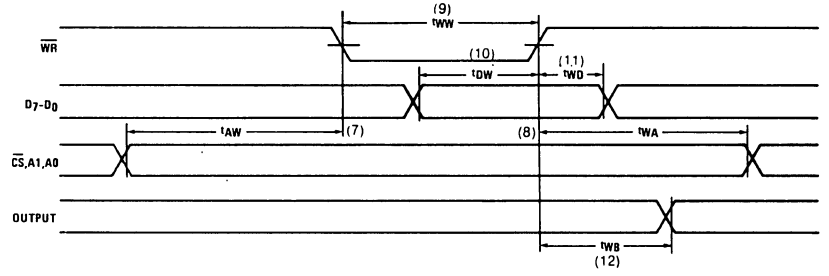
CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

Timing Waveforms

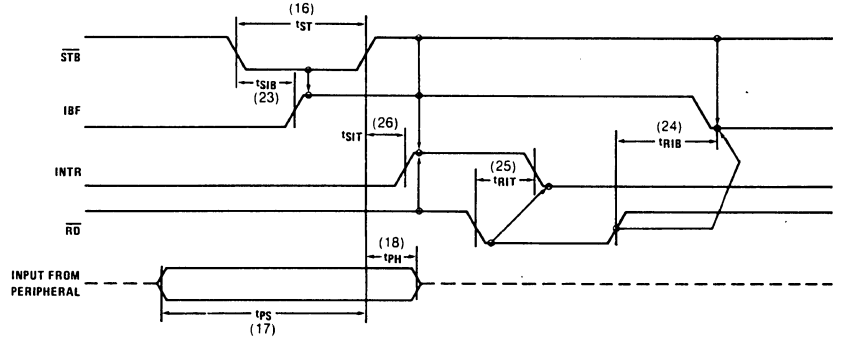
MODE 0 (BASIC INPUT)



MODE 0 (BASIC OUTPUT)

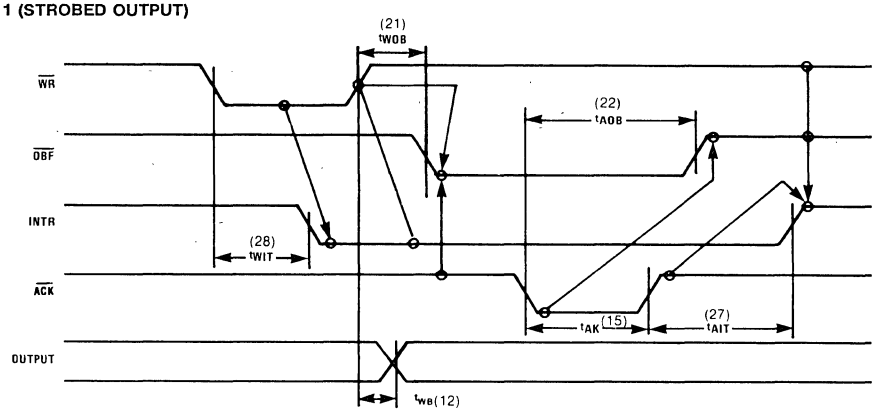


MODE 1 (STROBED INPUT)

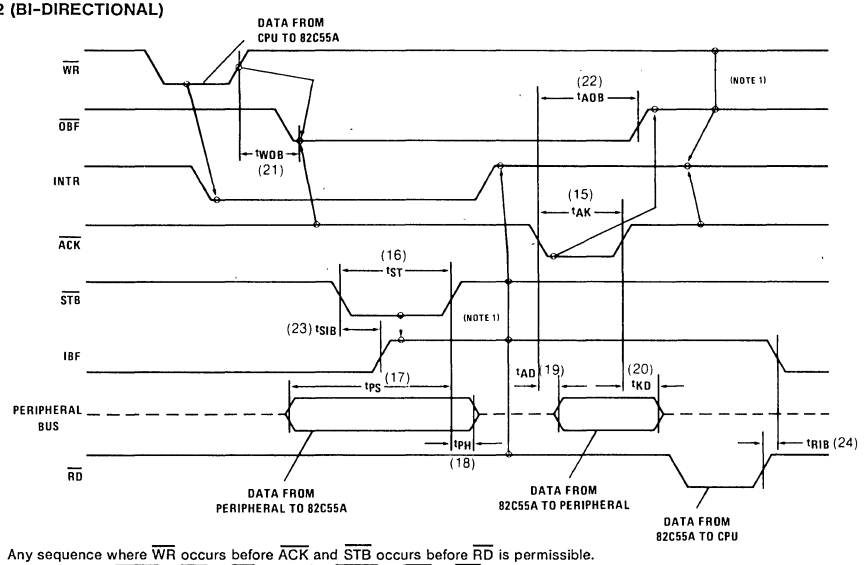


Timing Waveforms (Continued)

MODE 1 (STROBED OUTPUT)

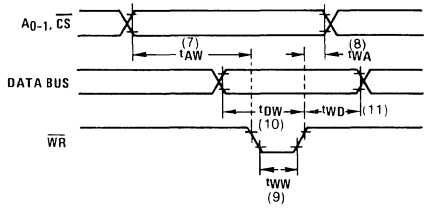


MODE 2 (BI-DIRECTIONAL)

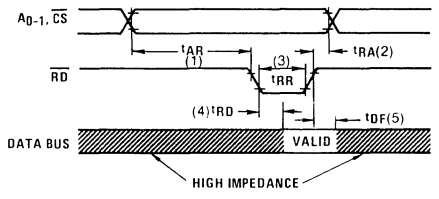


NOTE: 1. Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ • $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

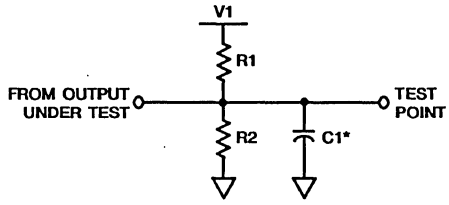
WRITE TIMING



READ TIMING

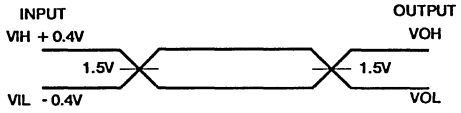


AC Test Circuit



*Includes Stray and Jig Capacitance

AC Testing Input, Output Waveform



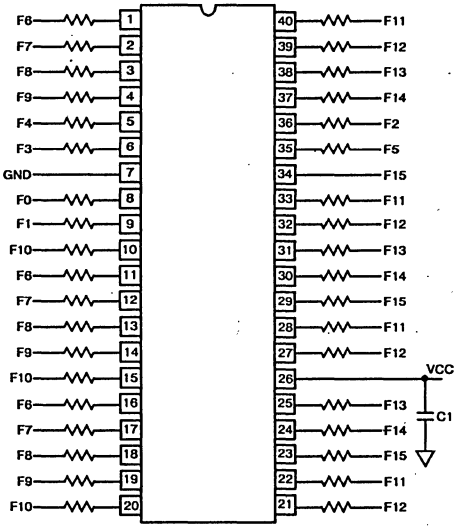
AC Testing: All parameters tested as per test circuits. Input rise and fall times are driven at 1ns/V

TEST CONDITION DEFINITION TABLE

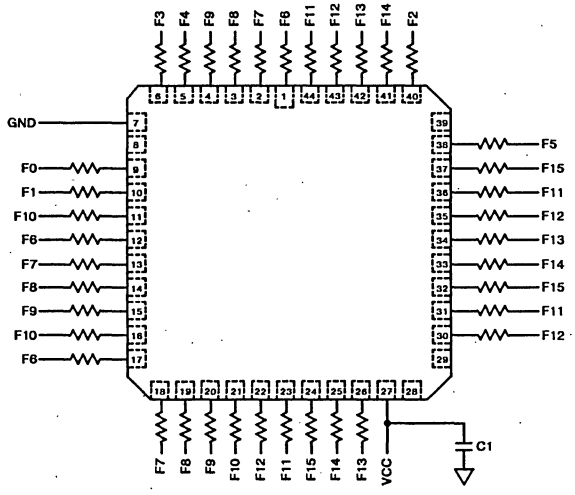
TEST CONDITIONS	V1	R1	R2	C1
1	1.7V	523Ω	Open	150pF
2	VCC	2kΩ	1.7kΩ	50pF
3	1.5V	750Ω	Open	50pF

Burn-In Circuits

82C55A/883 CERAMIC DIP



82C55A/883 CERAMIC LCC



VCC = 5.5V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to 0.4V
GND = 0V

C1 = 0.01μF minimum
All resistors are 47kΩ ± 5%
f0 = 100kHz ± 10%
f1 = f0 ÷ 2; f2 = f1 ÷ 2; . . . ; f15 = f14 ÷ 2

Metallization Topology

DIE DIMENSIONS:
131.4 x 167.7 x 19 ±1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 1kÅ

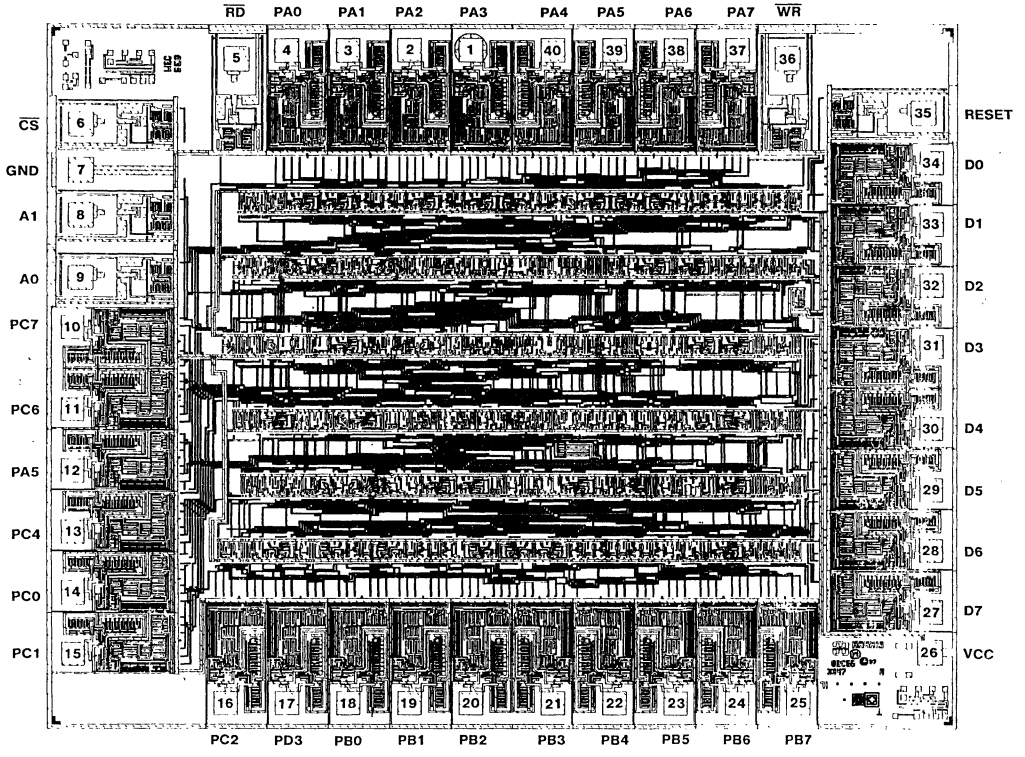
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy (LCC has Gold Preform)
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
0.78 x 10^5 A/cm^2

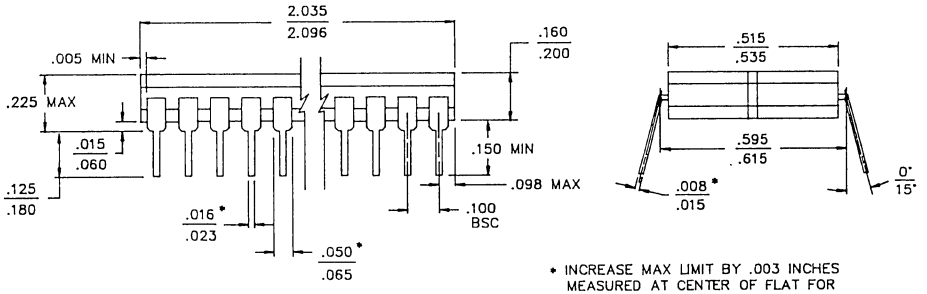
Metallization Mask Layout

82C55A/883



Packaging†

40 PIN CERAMIC DIP



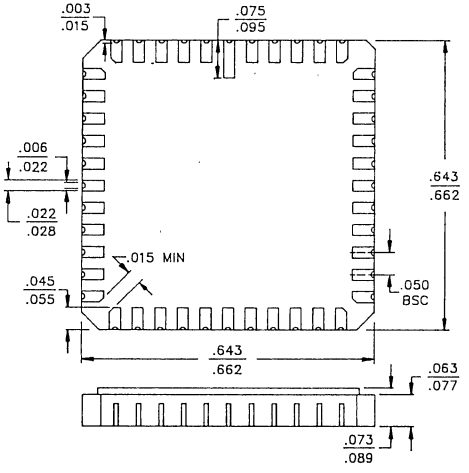
* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-5

44 PAD CERAMIC LCC

BOTTOM VIEW



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-5

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Functional Description

Data Bus Buffer

This three-state bi-directional 8 bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$) Chip Select. A "low" on this input pin enables the communication between the 82C55A and the CPU.

($\overline{RD}$) Read. A "low" on this input pin enables the 82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 82C55A.

($\overline{WR}$) Write. A "low" on this input pin enables the CPU to write data or control words into the 82C55A.

(A0 and A1) Port Select 0 and Port Select 1. These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).

82C55A BASIC OPERATION

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	Port A ➡ Data Bus
0	1	0	1	0	Port B ➡ Data Bus
1	0	0	1	0	Port C ➡ Data Bus
1	1	0	1	0	Control Word ➡ Data Bus
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus ➡ Port A
0	1	1	0	0	Data Bus ➡ Port B
1	0	1	0	0	Data Bus ➡ Port C
1	1	1	0	0	Data Bus ➡ Control
					DISABLE FUNCTION
X	X	X	X	1	Data Bus ➡ Three-State
X	X	1	1	0	Data Bus ➡ Three-State

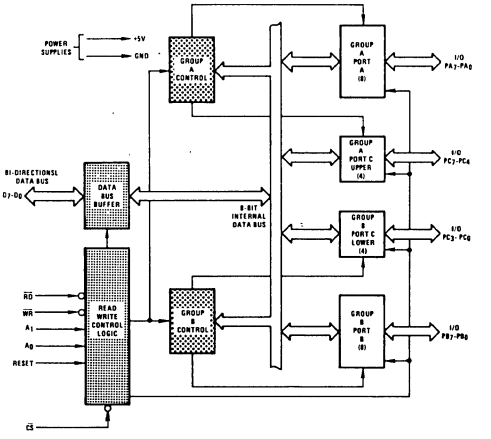


FIGURE 1. 82C55A BLOCK DIAGRAM. DATA BUS BUFFER, READ/WRITE, GROUP A & B CONTROL LOGIC FUNCTIONS

(RESET) Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the 82C55A will hold the I/O port inputs to a logic "1" state with a maximum hold current of 400μA.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7 - C4)

Control Group B - Port B and Port C lower (C3 - C0)

The control word register can be both written and read as shown in the "Basic Operation" table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Ports A, B and C

The 82C55A contains three 8 bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A One 8 bit data output latch/buffer and one 8 bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A. See Figure 2a.

Port B One 8 bit data input/output latch/buffer and one 8 bit data input buffer. See Figure 2b.

Port C One 8 bit data output latch/buffer and one 8 bit data input buffer (no latch for input). This port can be divided into two 4 bit ports under the mode control. Each 4 bit port contains a 4 bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. See Figure 2b.

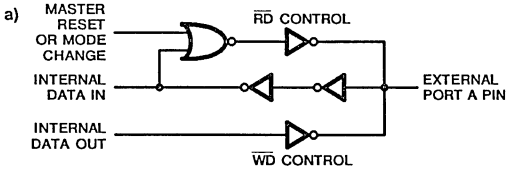


FIGURE 2. PORT A & B, PORT C BUS-HOLD CONFIGURATION

Operational Description

Mode Selection

There are three basic modes of operation than can be selected by the system software:

Mode 0 - Basic Input/Output
Mode 1 - Strobed Input/Output
Mode 2 - Bi-directional Bus

When the reset input goes "high", all ports will be set to the input mode with all 24 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need to pullup or pulldown resistors in all-CMOS designs. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine.

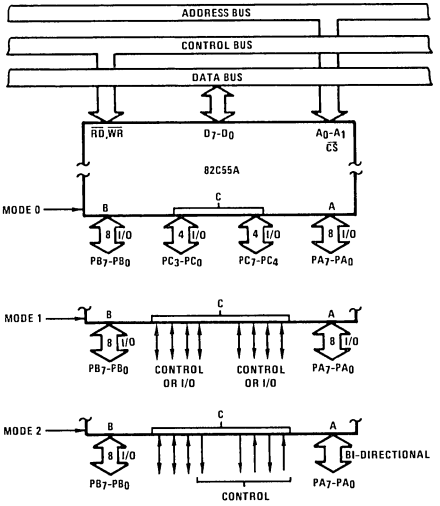


FIGURE 3. BASIC MODE DEFINITIONS AND BUS INTERFACE

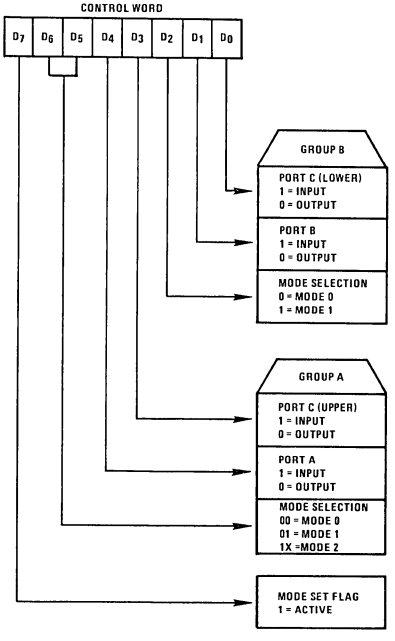


FIGURE 4. MODE DEFINITION FORMAT

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

The mode definitions and possible mode conbinations may seem confusing at first, but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs. PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature (Figure 5)

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

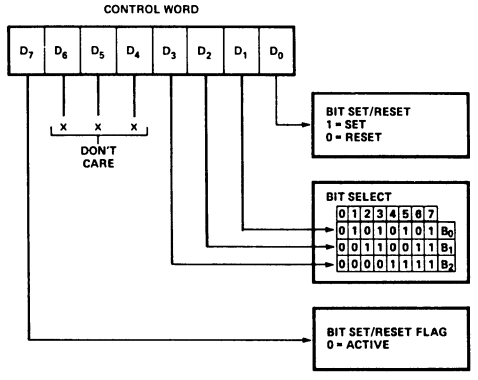


FIGURE 5. BIT SET/RESET FORMAT

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-Flop Definition:

(BIT-SET)-INTE is SET - Interrupt Enable
(BIT-RESET)-INTE is RESET - Interrupt Disable

NOTE: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

Mode 0 Basic Functional Definitions:

- Two 8 bit ports and two 4 bit ports
- Any Port can be input or output
- Outputs are latched
- Input are not latched
- 16 different Input/Output configurations possible

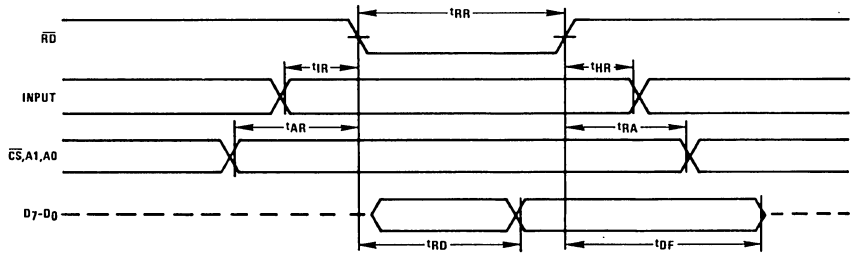
MODE 0 PORT DEFINITION

A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (Upper)	#	PORT B	PORT C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

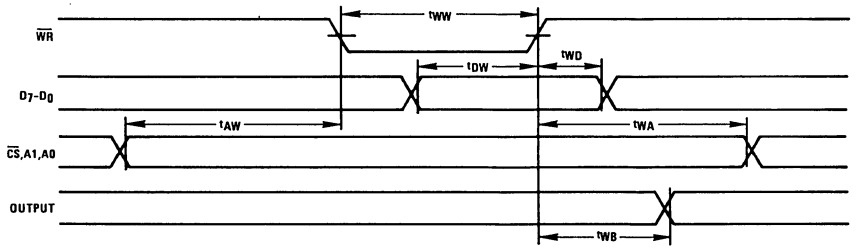
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

MODE 0 (Basic Input)



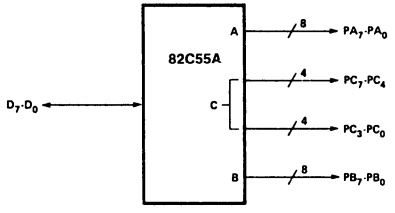
MODE 0 (Basic Output)



MODE 0 CONFIGURATIONS

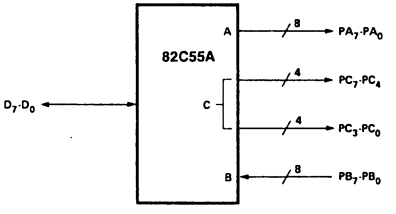
CONTROL WORD #0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	0



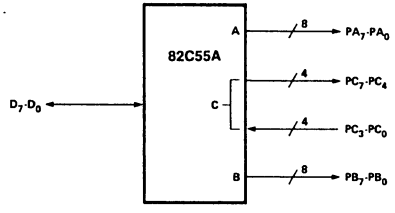
CONTROL WORD #2

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	0



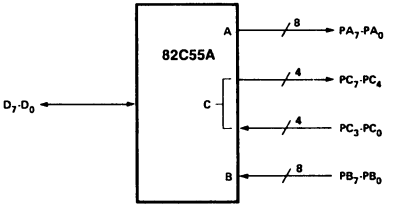
CONTROL WORD #1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	1



CONTROL WORD #3

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	1

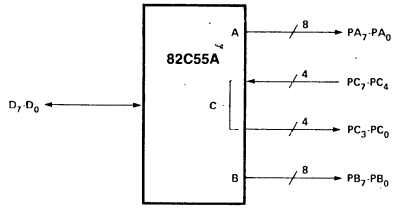


DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

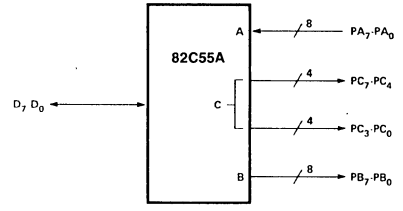
CONTROL WORD #4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



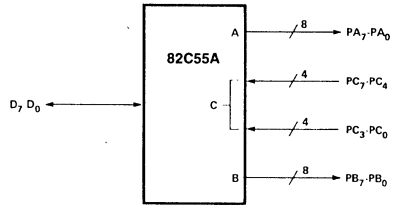
CONTROL WORD #8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0



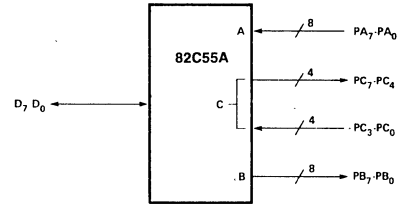
CONTROL WORD #5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



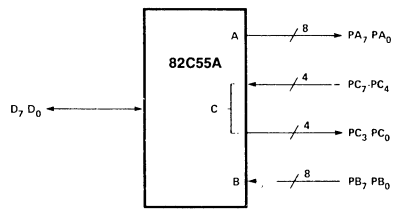
CONTROL WORD #9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



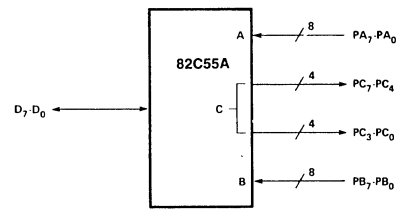
CONTROL WORD #6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



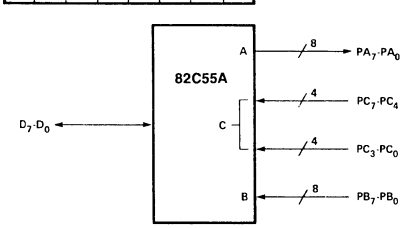
CONTROL WORD #10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



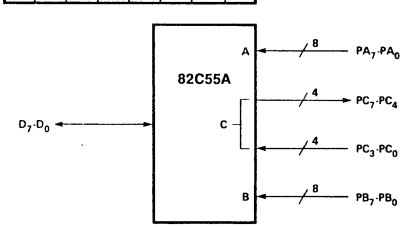
CONTROL WORD #7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



CONTROL WORD #11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1

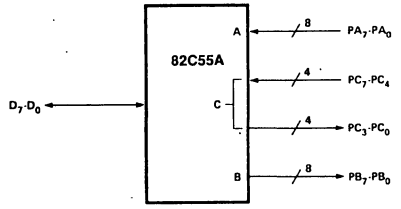


DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

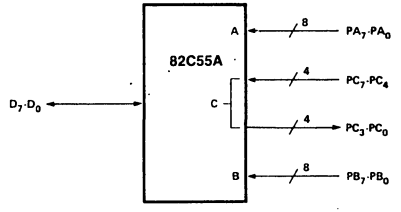
CONTROL WORD #12

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	0



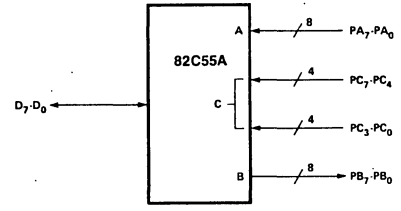
CONTROL WORD #14

D_7	D_6	D_5	D_4	D_3	D_7	D_1	D_0
1	0	0	1	1	0	1	0



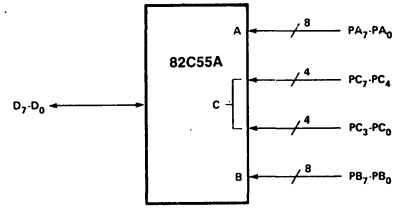
CONTROL WORD #13

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	1



CONTROL WORD #15

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	1



Operating Modes

Mode 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "hand shaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "hand shaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8 bit port and one 4 bit control/data port.
- The 8 bit data port can be either input or output. Both inputs and outputs are latched.
- The 4 bit port is used for control and status of the 8 bit port.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Input Control Signal Definition
(Figures 6 and 7)

STB (Strobe Input)
A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch: in essence, an acknowledgement. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when and input device is requesting service. INTR is set by the condition: $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC4.

INTE B

Controlled by bit set/reset of PC2.

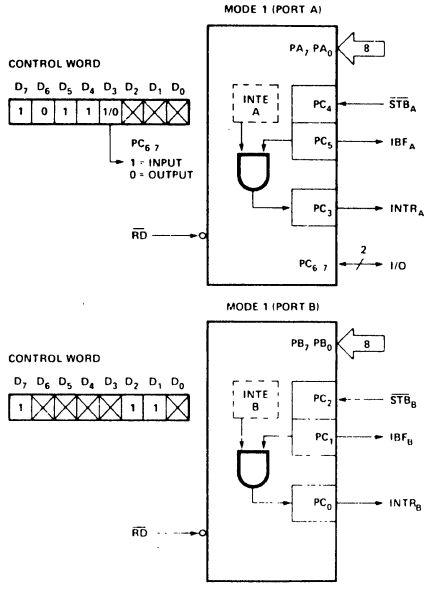


FIGURE 6. MODE 1 INPUT

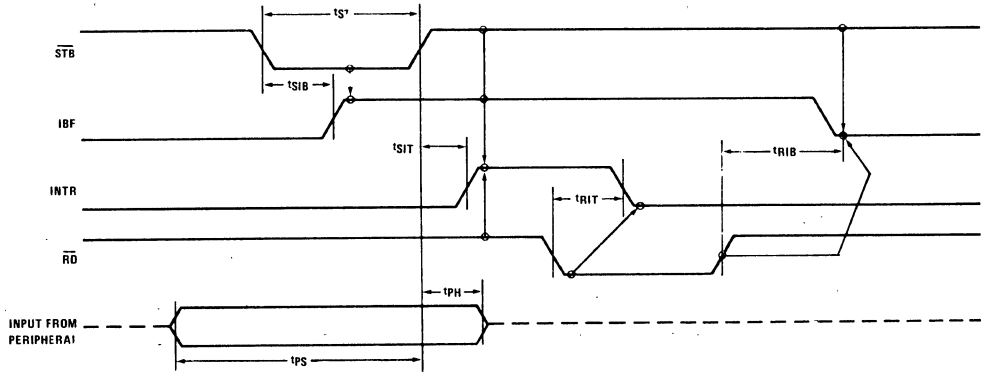


FIGURE 7. MODE 1 (STROBED INPUT)

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Output Control Signal Definition
(Figures 8 and 9)

$\overline{OBF}$ (Output Buffer Full F/F). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. This does not mean valid data is sent out of the part at this time since $\overline{OBF}$ can go true before data is available. Data is guaranteed valid at the rising edge of $\overline{OBF}$. See Note 1. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 82C55A that the data from Port A or Port B is ready to be accepted. In essence, a response from the peripheral device indicating that is is rady to accept data. See Note 1.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by Bit Set/Reset of PC6.

INTE B

Controlled by Bit Set/Reset of PC2.

NOTE: 1. To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send $\overline{OBF}$ to the peripheral device, generates an $\overline{ACK}$ from the peripheral device and then latch data into the peripheral device on the rising edge of $\overline{OBF}$.

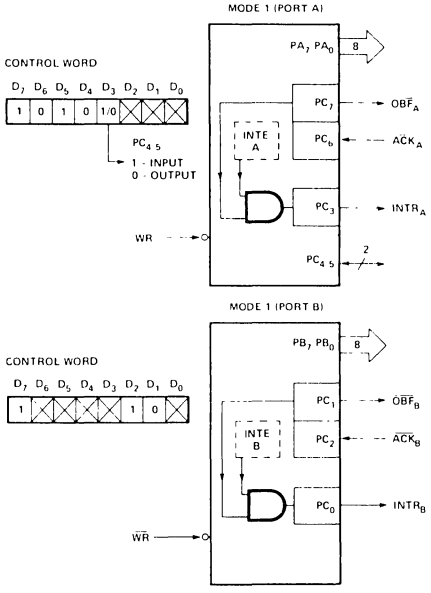


FIGURE 8. MODE 1 OUTPUT

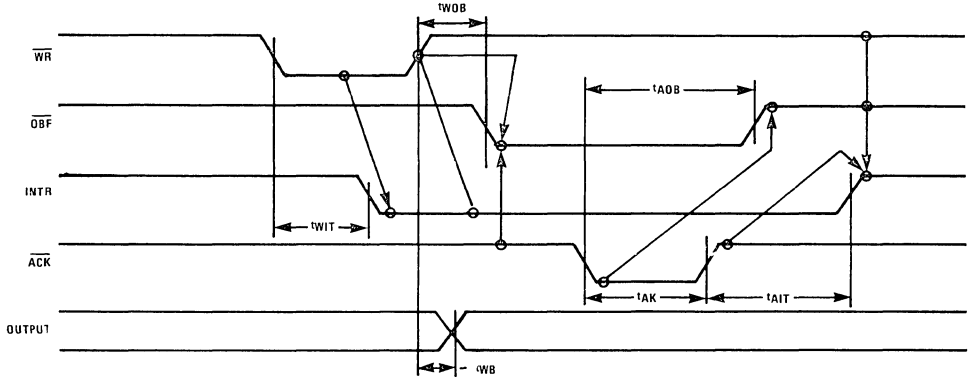


FIGURE 9. MODE 1 (STROBED OUTPUT)

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

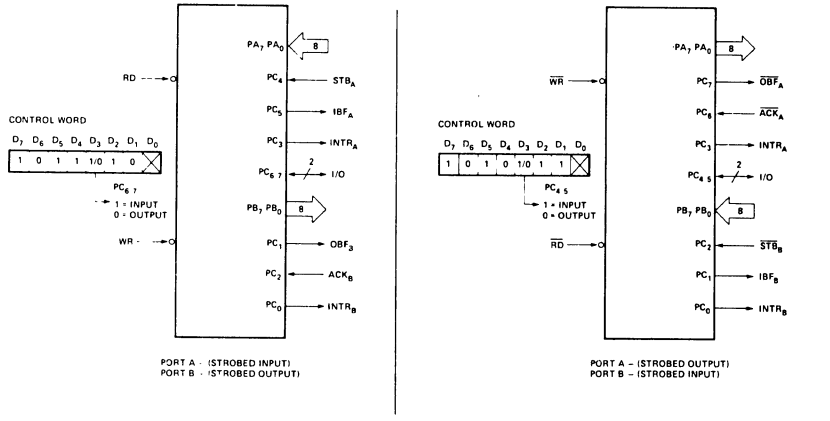


FIGURE 10. COMBINATIONS OF MODE 1

Combinations of Mode 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

Operating Modes

Mode 2 (Strobed Bi-directional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8 bit bus for both transmitting and receiving data (bi-directional bus I/O). "Hand shaking" signals are provided to maintain proper bus flow discipline similar to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only
- One 8 bit, bi-directional bus Port (Port A) and a 5 bit control Port (Port C)
- Both inputs and outputs are latched
- The 5 bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A)

Bi-directional Bus I/O Control Signal Definition

(Figures 11, 12, 13, 14)

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "low" on this input enables the three-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE flip-flop associated with $\overline{OBF}$). Controlled by bit set/reset of PC4.

Input Operations

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE flip-flop associated with IBF). Controlled by bit set/reset of PC4.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

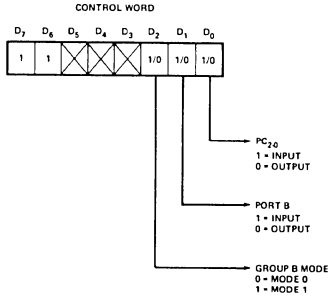


FIGURE 11. MODE CONTROL WORD

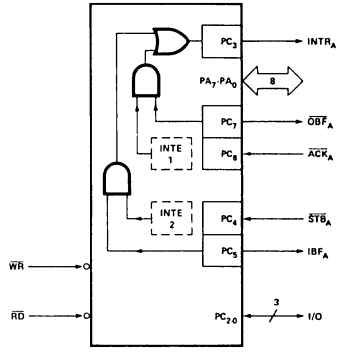


FIGURE 12. MODE 2

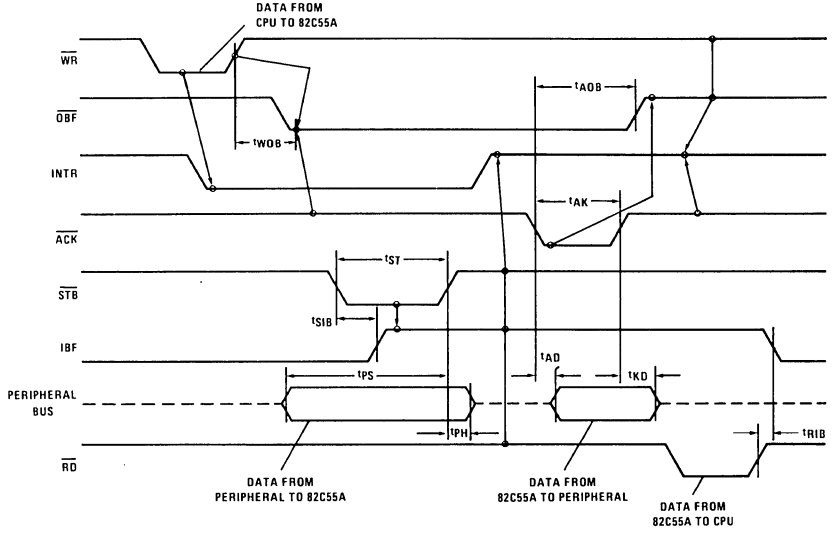


FIGURE 13. MODE 2 (BI-DIRECTIONAL)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$)

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

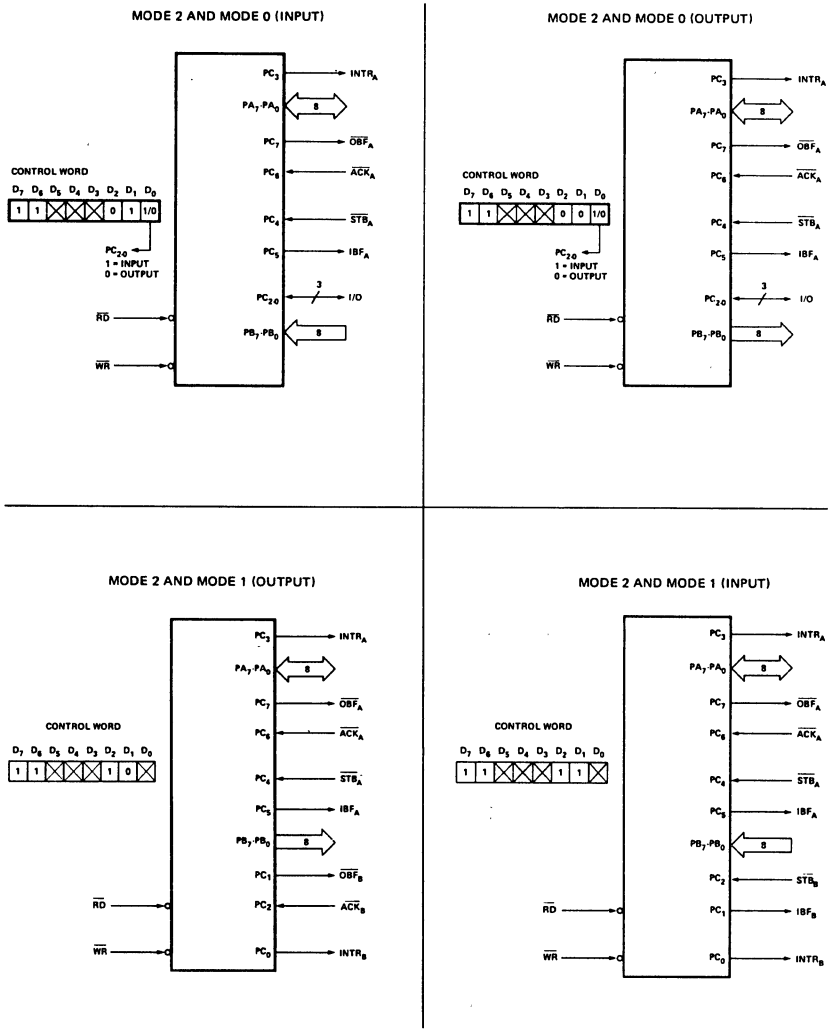


FIGURE 14. MODE 2 COMBINATIONS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

MODE DEFINITION SUMMARY

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA0	In	Out	In	Out	← →	
PA1	In	Out	In	Out	← →	
PA2	In	Out	In	Out	← →	
PA3	In	Out	In	Out	← →	
PA4	In	Out	In	Out	← →	
PA5	In	Out	In	Out	← →	
PA6	In	Out	In	Out	← →	
PA7	In	Out	In	Out	← →	
PB0	In	Out	In	Out		Mode 0 Or Mode 1 Only
PB1	In	Out	In	Out		
PB2	In	Out	In	Out		
PB3	In	Out	In	Out		
PB4	In	Out	In	Out		
PB5	In	Out	In	Out		
PB6	In	Out	In	Out		
PB7	In	Out	In	Out		
PC0	In	Out	$INTR_B$	$INTR_B$	I/O	
PC1	In	Out	IBF_B	$\overline{OBF}_B$	I/O	
PC2	In	Out	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC3	In	Out	$INTR_A$	$INTR_A$	$INTR_A$	
PC4	In	Out	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC5	In	Out	IBF_A	I/O	IBF_A	
PC6	In	Out	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC7	In	Out	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

Special Mode Combination Considerations:

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C fare not affectged by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

INPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
GROUP A					GROUP B		

OUTPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
OBF_A	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	OBF_B	$INTR_B$
GROUP A					GROUP B		

FIGURE 15. MODE 1 STATUS WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
OBF_A	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	X	X	X
GROUP A					GROUP B		

(DEFINED BY MODE 0 OR MODE 1 SELECTION)

FIGURE 16. MODE 2 STATUS WORD FORMAT

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Current Drive Capability:

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status (Figures 15 and 16)

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

INTERRUPT ENABLE FLAG*	POSITION	ALTERNATE PORT C PIN SIGNAL (MODE)
INTE B	PC2	$\overline{ACK}_B$ (Output Mode 1) or $\overline{STB}_B$ (Input Mode 1)
INTE A2	PC4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2)

FIGURE 17. INTERRUPT ENABLE FLAGS IN MODES 1 AND 2

Applications of the 82C55A

The 82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 82C55A to exactly "fit" the application. Figures 18 through 24 present a few examples of typical applications of the 82C55A.

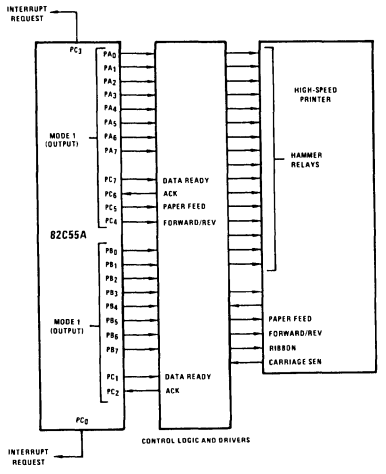


FIGURE 18. PRINTER INTERFACE

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

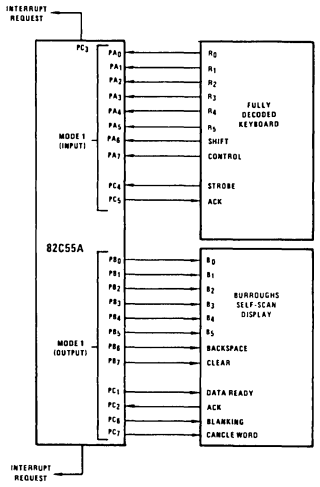


FIGURE 19. KEYBOARD AND DISPLAY INTERFACE

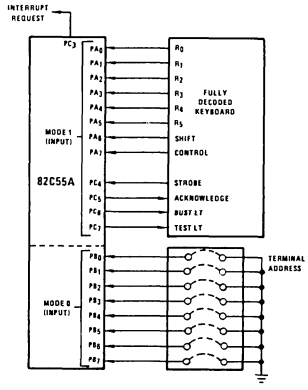


FIGURE 20. KEYBOARD AND TERMINAL ADDRESS INTERFACE

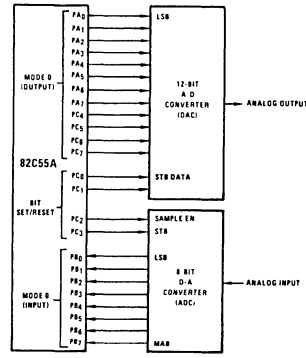


FIGURE 21. DIGITAL TO ANALOG, ANALOG TO DIGITAL

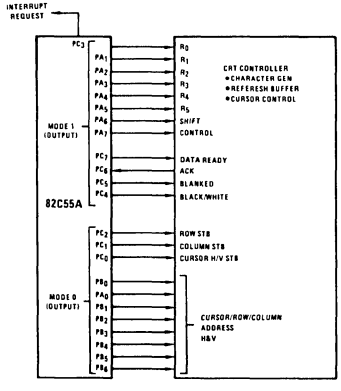


FIGURE 22. BASIC CRT CONTROLLER INTERFACE

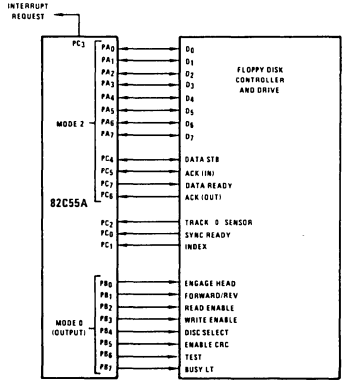


FIGURE 23. BASIC FLOPPY DISC INTERFACE

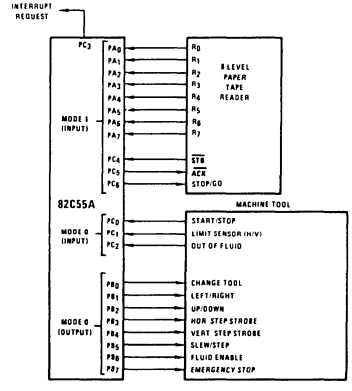


FIGURE 24. MACHINE TOOL CONTROLLER INTERFACE

HARRIS

82C59A/883

June 1989

CMOS Priority Interrupt Controller

Features

- This Circuit is Processed in Accordance to Mil-Std-883C and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Compatible with NMOS 8259A
- 8MHz and 5MHz Versions Available
- High Speed, No "Wait State" Operation with 8MHz 80C86 and 80C88
- Eight Level Priority Controller, Expandable to 64 Levels
- Fully TTL Compatible
- Fully Static CMOS Design
- Programmable Interrupt Modes
- Individual Request Mask Capability
- Low Standby Power - 10μA Maximum
- Single 5V Power Supply
- Military Operating Temperature Range ..... -55°C to +125°C

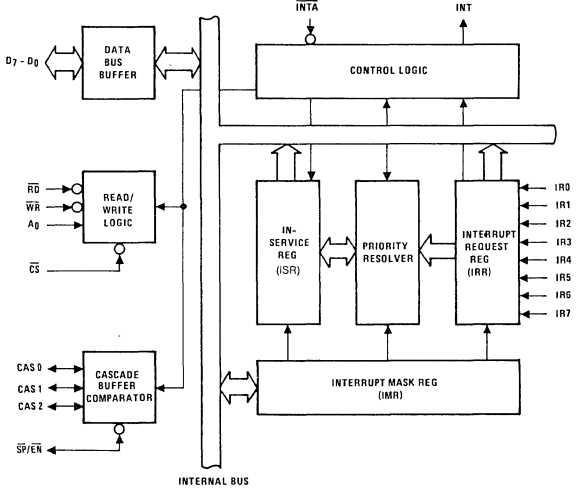
Description

The Harris 82C59A/883 is a high performance CMOS Priority Interrupt Controller manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C59A/883 is designed to relieve the system CPU from the task of polling in a multi-level priority system. The high speed and industry standard configuration of the 82C59A/883 make it compatible with microprocessors such as the 80C86 and 80C88.

The 82C59A/883 can handle up to eight vectored interrupting sources and is cascadable to 64 without additional circuitry. Individual interrupting sources can be masked or prioritized to allow custom system configuration. Two modes of operation make the 82C59A/883 compatible with both 8080/85 and 80C86/88 formats.

Static CMOS circuit design insures low operating power. The Harris advanced SAJI process results in performance equal to or greater than existing functionally equivalent products at a fraction of the power.

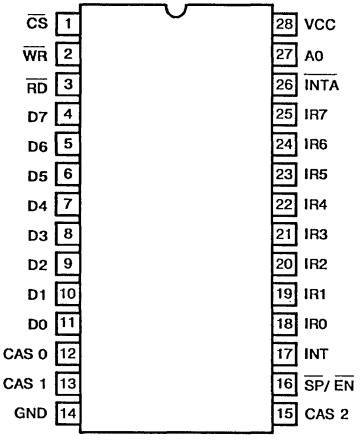
Functional Diagram



Pinouts

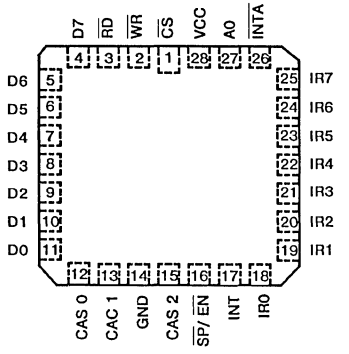
82C59A/883 (CERAMIC DIP)

TOP VIEW



82C59A/883 (CERAMIC LCC)

TOP VIEW



PIN	DESCRIPTION
D7-D0	Data Bus (Bi-Directional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0	Command Select Address
$\overline{CS}$	Chip Select
CAS 2 - CAS 0	Cascade Lines
$\overline{SP/EN}$	Slave Program Input Enable
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0 - IR7	Interrupt Request Inputs

Pin Description

PIN SYMBOL	NUMBER	TYPE	DESCRIPTION
VCC	28	I	VCC: The +5V power supply pin. A 0.1μF capacitor between VCC and GND is recommended for decoupling.
GND	14	I	GROUND
$\overline{CS}$	1	I	CHIP SELECT: A low on this pins enables $\overline{RD}$ and $\overline{WR}$ communications between the CPU and the 82C59A/883. $\overline{INTA}$ functions are independent of $\overline{CS}$.
$\overline{WR}$	2	I	WRITE: A low on this pin when $\overline{CS}$ is low enables the 82C59A/883 to accept command words from the CPU.
$\overline{RD}$	3	I	READ: A low on this pin when $\overline{CS}$ is low enables the 82C59A/883 to release status onto the data bus for the CPU.
D7-D0	4-11	I/O	BIDIRECTIONAL DATA BUS: Control status and interrupt-vector information is transferred via this bus.
CAS 0 - CAS 2	12, 13, 15	I/O	CASCADE LINES: the CAS lines form a private 82C59A/883 bus to control a multiple 82C59A/883 structure. These pins are outputs for a master 82C59A/883 and inputs for a slave 82C59A/883.
$\overline{SP}/\overline{EN}$	16	I/O	SLAVE PROGRAM/ENABLE BUFFER: This is a dual function pin. when in the Buffered Mode it can be used as an output to control buffer transceivers ($\overline{EN}$). When not in the buffered mode it is used as an input to designate a master ($\overline{SP}$ = 1) or slave ($\overline{SP}$ = 0).
INT	17	O	INTERRUPT: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IRO-IR7	18-25	I	INTERRUPT REQUESTS: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
$\overline{INTA}$	26	I	INTERRUPT ACKNOWLEDGE: This pin is used to enable 82C59A/883 interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
. A0	27	I	ADDRESS LINE: This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 82C59A/883 to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to CPU A0 address line (A1 for 80C86/88).

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec)..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	47°C/W	10°C/W
Ceramic LCC Package	53°C/W	6°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.08W
Ceramic LCC Package 932mW
Gate Count ..... 1250 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Voltage Range ..... +4.5V to +5.5V

TABLE 1. 82C59A/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical "1" Input Voltage	VIH	VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.2	-	V
Logical "0" Input Voltage	VIL	VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.8	V
Output HIGH Voltage	VOH	VCC = 4.5V, IOH = -2.5mA IOH = -100µA (Note 2)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	 3.0 VCC-0.4	 - -	 V V
Output LOW Voltage	VOL	VCC = 4.5V, IOL = 2.5mA (Note 2)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Input Leakage Current	II	VCC = 5.5V, VIN = GND or VCC DIP Pins: 1 - 3, 26, 27	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Output Leakage Current	IO	VCC = 5.5V, VIN = GND or VCC DIP Pins: 4 - 13, 15, 16	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-10	+10	µA
IR Input Load Current	ILIR	VCC = 5.5V, VIN = OV VIN = VCC, DIP Pins: 18 - 25	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	-500 10	µA µA
Standby Power Supply Current	ICCSB	VCC = 5.5V, VIN = VCC or GND Outputs Open, (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA

NOTES: 1. Except for IR0 - IR7, where Vin = VCC or OPEN.
2. Interchanging of force and sense conditions is permitted.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. 82C59A/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS 82C59A-5/883 MIN	LIMITS 82C59A-5/883 MAX	LIMITS 82C59A/883 MIN	LIMITS 82C59A/883 MAX	UNITS
TIMING REQUIREMENTS									
A0/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$	TAHRL (1)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	10	-	ns
A0/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$	TRHAX (2)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	5	-	ns
$\overline{RD}$/$\overline{INTA}$ Pulse Width	TRLRH(3)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	235	-	160	-	ns
A0/$\overline{CS}$ Setup to $\overline{WR}$	TAHWL(4)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
A0/$\overline{CS}$ Hold after $\overline{WR}$	TWHAX(5)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	5	-	ns
$\overline{WR}$ Pulse Width	TWLWH(6)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	165	-	95	-	ns
Data Setup to $\overline{WR}$	TDVWH(7)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	240	-	160	-	ns
Data Hold after $\overline{WR}$	TWHDX(8)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	5	-	ns
Interrupt Request Width	TJLJH(9)	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	100	-	ns
Cascade Setup to Second or Third $\overline{INTA}$ (Slave Only)	TCVIAL (10)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	55	-	40	-	ns
End of $\overline{RD}$ to next $\overline{RD}$; End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	TRHRL (11)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	160	-	160	-	ns
End of $\overline{WR}$ to next $\overline{WR}$	TWHWL (12)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	190	-	190	-	ns
End of Command to next Command (Not same command type) End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	TCHCL (13)	(Note 3)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	500	-	400	-	ns
Data Valid from $\overline{RD}$/$\overline{INTA}$	TRLDV (14)	(Note 4)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	160	-	120	ns
Interrupt Output Delay	TJHIH (16)	(Note 4)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	350	-	300	ns
Cascade Valid from First $\overline{INTA}$ (Master Only)	TIALCV (17)	(Note 4)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	565	-	360	ns
Enable Active from $\overline{RD}$ or $\overline{INTA}$	TRLEL (18)	(Note 5)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	125	-	100	ns
Enable Inactive from $\overline{RD}$ or $\overline{INTA}$	TRHEH (19)	(Note 5)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	60	-	50	ns
Data Valid from Stable Address	TAHDV (20)	(Note 4)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	210	-	200	ns
Cascade Valid to Valid Data	TCVDV (21)	(Note 4)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	300	-	200	ns

NOTES: 1. Tested as follows: f = 1MHz, VIH= 2.6V, VIL = 0.4V, CL = 50pF (unless otherwise specified), VOH $\geq$ 1.5V, VOL $\leq$ 1.5V, VCC = 4.5V and 5.5V.
2. This is a low time required to clear the input latch in the edge triggered mode.
3. Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 400ns (i.e. 8085A = 1.6µs, 8085A-2 = 1 µs, 80C86 = 1µs).
4. Tested under Test Condition 1 in Test Condition Definition Table.
5. Tested under Test Condition 3 in Test Condition Definition Table.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. 82C59A/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1, 2 1, 3	$T_A = +25^oC$ $T_A = +25^oC$	- -	15 7	pF pF
Output Capacitance	COUT	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1, 2 1, 3	$T_A = +25^oC$ $T_A = +25^oC$	- -	15 7	pF pF
I/O Capacitance	CI/O	VCC = OPEN, f = 1MHz All Measurements Referenced to Device GND	1, 2 1, 3	$T_A = +25^oC$ $T_A = +25^oC$	- -	15 7	pF pF

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	82C59A-5/883 MIN	82C59A-5/883 MAX	82C59A/883 MIN	82C59A/883 MAX	UNITS
Data Float After $\overline{RD}/\overline{INTA}$	TRHDZ(15)		1, 4	$-55^oC \leq T_A \leq +125^oC$	10	100	10	85	ns

NOTES:
1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. For Ceramic DIP package.
3. For Ceramic LCC package.
4. Tested as follows: f = 1MHz, VIH = 2.6V, VIL = 0.4V, CL = 50pF (unless otherwise specified), VOH $\geq$ 1.5V, VOL $\leq$ 1.5V, VCC = 4.5V and 5.5V, using Test Condition 2 in Test Condition Definition Table.

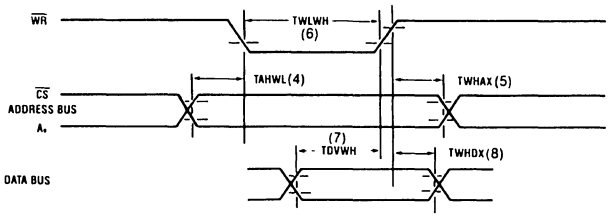
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

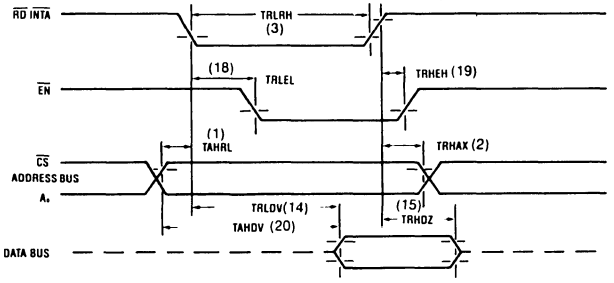
CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

Timing Waveforms

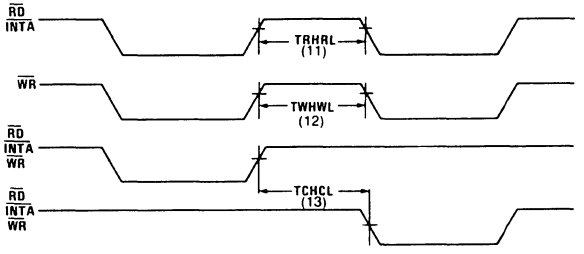
WRITE



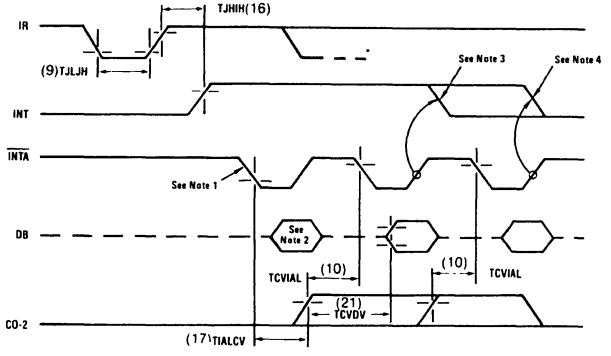
READ/INTA



OTHER TIMING

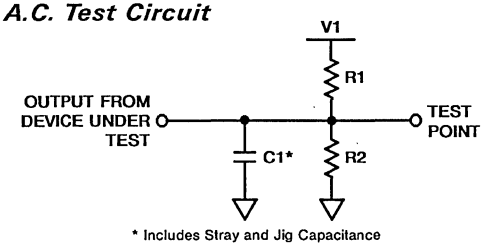


INTA SEQUENCE



NOTES: 1. Interrupt Request (IR) must remain HIGH until leading edge of first $\overline{\text{INTA}}$.
2. During first $\overline{\text{INTA}}$ the Data Bus is not active in 80C86/88 mode.
3. 80C86/88 mode.
4. 8080/8085 mode.

A.C. Test Circuit

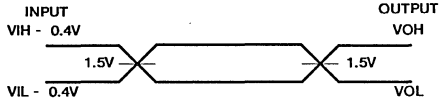


* Includes Stray and Jig Capacitance

TEST CONDITION DEFINITION TABLE

TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	Open	100pF
2	VCC	1.8kΩ	1.8kΩ	50pF
3	1.7V	523Ω	Open	50pF

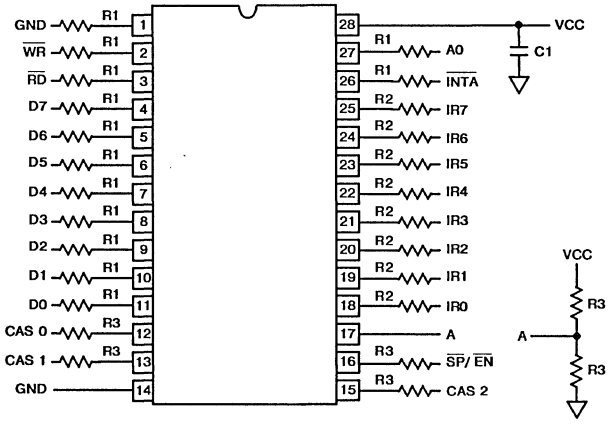
A.C. Testing Input, Output Waveform



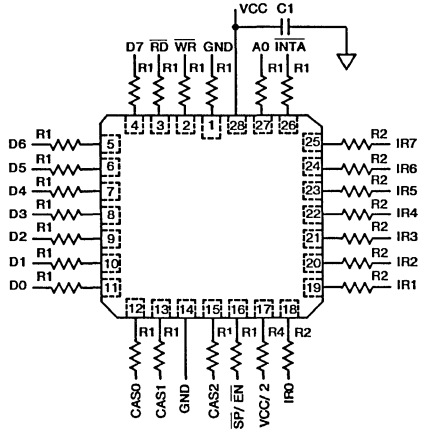
A.C. Testing: All inputs signals must switch between VIL - 0.4V and VIH +0.4V. Input rise and fall times are driven at 1ns/V.

Burn-In Circuits

82C59A/883 CERAMIC DIP



82C59A/883 CERAMIC LCC



NOTES:

VCC = 5.5V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to 0.4V
GND = 0V
R1 = 47kΩ ± 5%
R2 = 510Ω ± 5%
R3 = 10kΩ ± 5%
R4 = 1.2kΩ ± 5%
C1 = 0.01μF min
F0 = 100kHz ± 10%
F1 = F0/2, F2 = F1/2, ... F8 = F7/2

Metallization Topology

DIE DIMENSIONS:
154.3 x 173.2 x 19 ± 1mils

METALLIZATION:
Type: Si - AL
Thickness: 11kÅ ± 1kÅ

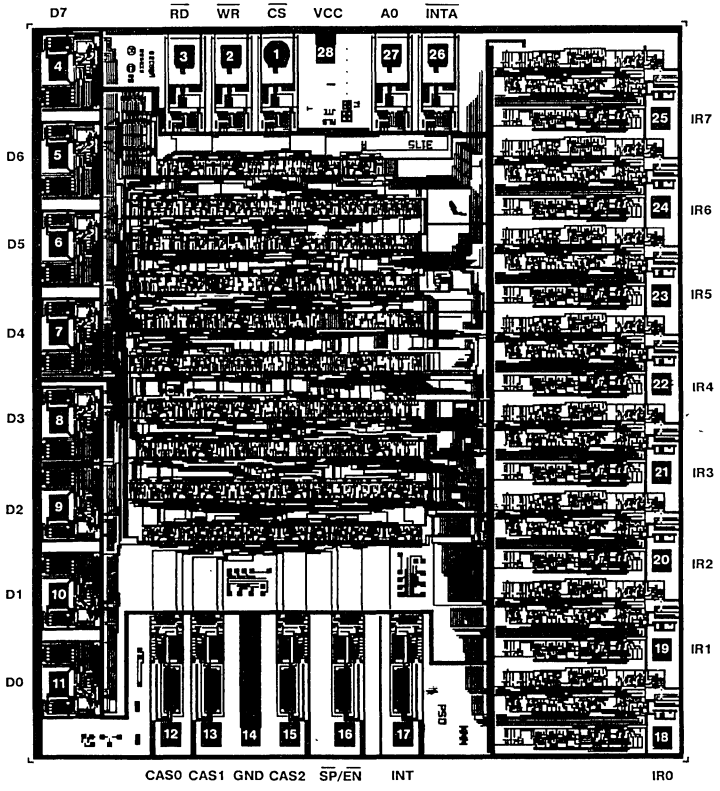
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy (LCC has Gold Preform)
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.64 x 10^5 A/cm^2

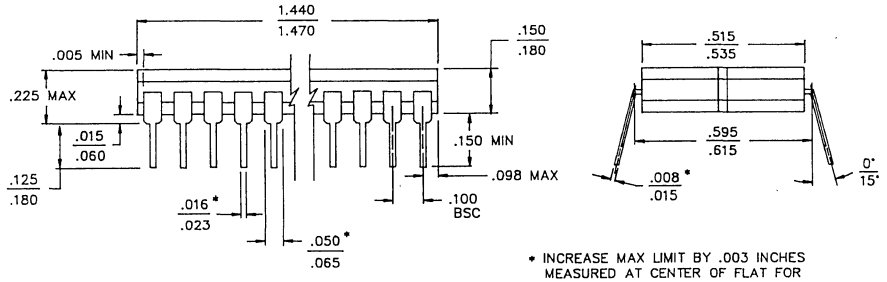
Metallization Mask Layout

82C59A/883



Packaging†

28 PIN CERAMIC DIP

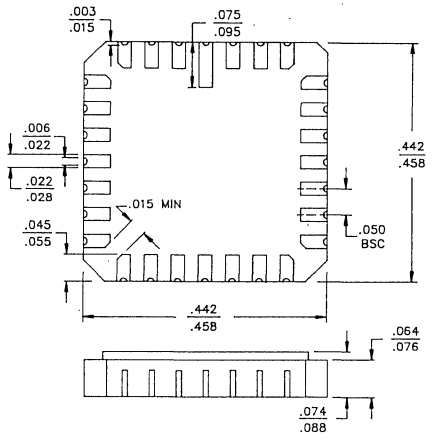


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

28 PAD CERAMIC LCC
BOTTOM VIEW



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-4

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Functional Description

INTERRUPTS IN MICROCOMPUTER SYSTEMS

Microcomputers system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

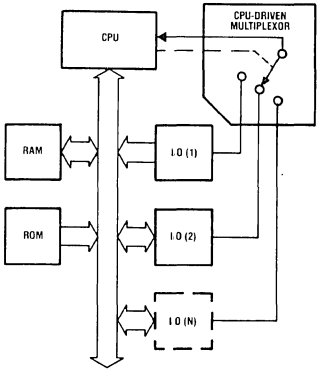
The most common method of servicing such devices is the Polled approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system through-put, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

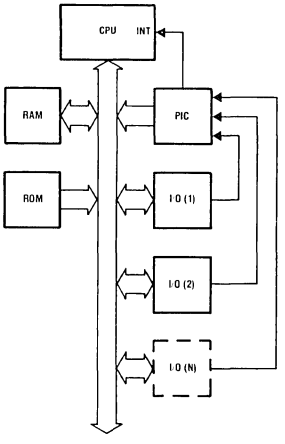
This is the interrupt-driven method. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.



POLLED METHOD



INTERRUPT METHOD

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

82C59A Functional Description

The 82C59A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels of requests and has built-in features for expandability to other 82C59As (up to 4 levels). It is programmed by system software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 82C59A can be configured to match system requirements. The priority modes can be changed or reconfigured dynamically at any time during main program operation. This means that the complete interrupt structure can be defined as required, based on the total system environment.

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Registers (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are currently being serviced.

PRIORITY RESOLVER

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during the $\overline{INTA}$ sequence.

INTERRUPT MASK REGISTER (IMR)

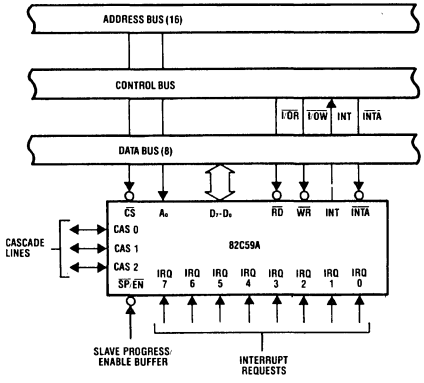
The IMR stores the bits which disable the interrupt lines to be masked. The IMR operates on the output of the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

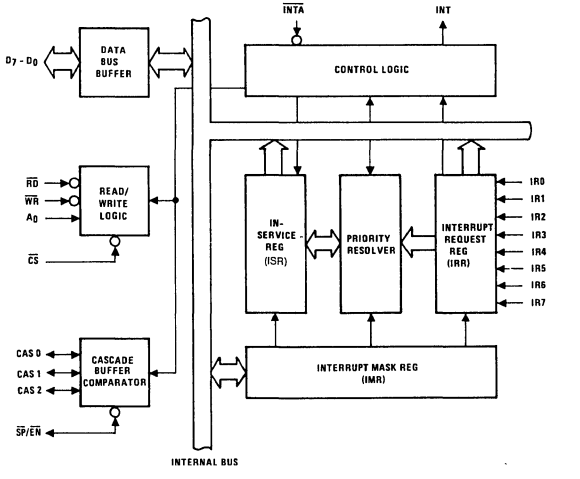
INTERRUPT (INT)

This output goes directly to the CPU interrupt input. The VOH level on this line is designed to be fully compatible with the 8080A, 8085A, 808 , 8088 and 80C8 , 80C88 input levels.

INTERRUPT ACKNOWLEDGE ($\overline{INTA}$)

$\overline{INTA}$ pulses will cause the 82C59A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the 80C59A.





82C59A FUNCTIONAL DIAGRAM

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the 82C59A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Intialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 82C59A to be transferred onto the Data Bus.

CHIP SELECT ($\overline{CS}$)

A LOW on this input enables the 82C59A. No reading or writing of the device will occur unless the device is selected.

WRITE ($\overline{WR}$)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 82C59A.

READ ($\overline{RD}$)

A LOW on this input enables the 82C59A to send the status of the Interrupt Request Register (IRR), In-Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level (in the poll mode) onto the Data Bus.

A0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all 82C59As used in the system. The associated three I/O pins (CAS0-2) are outputs when the 82C59A is used as a master and are inputs when the 82C59A is used as a slave. As a master, the 82C59A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{INTA}$ pulses. (See section "Cascading the 82C59A".)

INTERRUPT SEQUENCE

The powerful features of the 82C59A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specified interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

These events occur in an 8080A/8085 system:

1. One or more of the INTERRUPT REQUEST lines (10-17) are raised high, setting the corresponding IRR bits(s).
2. The 82C59A evaluates these requests in the priority resolver and sends an interrupt (INT) to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 82C59A will also release a CALL instruction code (11001101) onto the 8-bit data bus through D0 - D7.
5. This CALL instruction will initiate two additional $\overline{INTA}$ pulses to be sent to 82C59A from the CPU group.
6. These two $\overline{INTA}$ pulses allow the 82C59A to release its preprogrammed subroutine address onto the data bus. The lower 8-bit address is released at the first $\overline{INTA}$ pulse and the higher 8-bit address is released at the second $\overline{INTA}$ pulse.
7. This completes the 3-byte CALL instruction released by the 82C59A. In the AEOI mode, the ISR bit is reset at the end of the third $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an 80C86 system are the same until step 4.

4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 82C59A does not drive the data bus during this cycle.
5. The 80C86 will initiate a second $\overline{INTA}$ pulse. During this pulse, the 82C59A releases an 8-bit pointer onto the data bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode, the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e. the request was too short in duration), the 82C59A will issue an interrupt level 7. If a slave is programmed on IR bit 7, the CAS lines remain inactive and vector addresses are output from the master 82C59A.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Interrupt Sequence Outputs

8080, 8085

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse, the CALL opcode is enabled onto the data bus.

First Interrupt Vector Byte Data: Hex CD

	D7	D6	D5	D4	D3	D2	D1	D0
Call Code	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse, the lower address of the appropriate service routine is enabled onto the data bus. When interval = 4 bits, A5 - A7 are programmed, while A0 - A4 are automatically inserted by the 82C59A. When interval = 8, only A6 and A7 are programmed, while A0 - A5 are automatically inserted.

CONTENT OF SECOND INTERRUPT VECTOR BYTE

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third $\overline{INTA}$ pulse, the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A8 - A15), is enabled onto the bus.

CONTENT OF THIRD INTERRUPT VECTOR BYTE

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

80C86, 80C88 INTERRUPT RESPONSE MODE

80C86 mode is similar to 8080/85 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of 8080/85 systems in that the 82C59A uses it to internally freeze the state of the interrupts for priority resolution and, as a master, it issues the interrupt code on the cascade lines. On this first cycle, it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in 80C86 mode, the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A5 - A11 are unused in 80C86 mode.)

CONTENT OF INTERRUPT VECTOR BYTE FOR 80C86 SYSTEM MODE

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

PROGRAMMING THE 82C59A

The 82C59A accepts two types of command words generated by the CPU;

1. Initialization Command Words (ICWs): Before normal operation can begin, each 82C59A in the system must be brought to a starting point - by a sequence of 2 to 4 bytes timed by WR pulses.
2. Operation Command Words (OCWs): These are the command words which command the 82C59A to operate in various interrupt modes. Among these modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the 82C59A anytime after initialization.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Initialization Command Words (ICWS)

GENERAL

Whenever a command is issued with A0=0 and D4=1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.

b. The Interrupt Mask Register is cleared.

c. IR7 input is assigned priority 7.

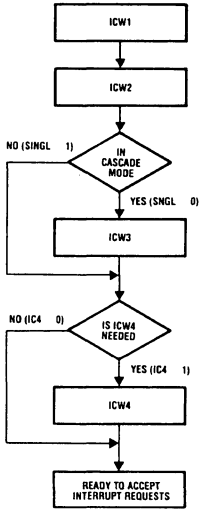
d. Special Mask Mode is cleared and Status Read is set to IRR.

e. If IC4=0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, 8080/85 system).

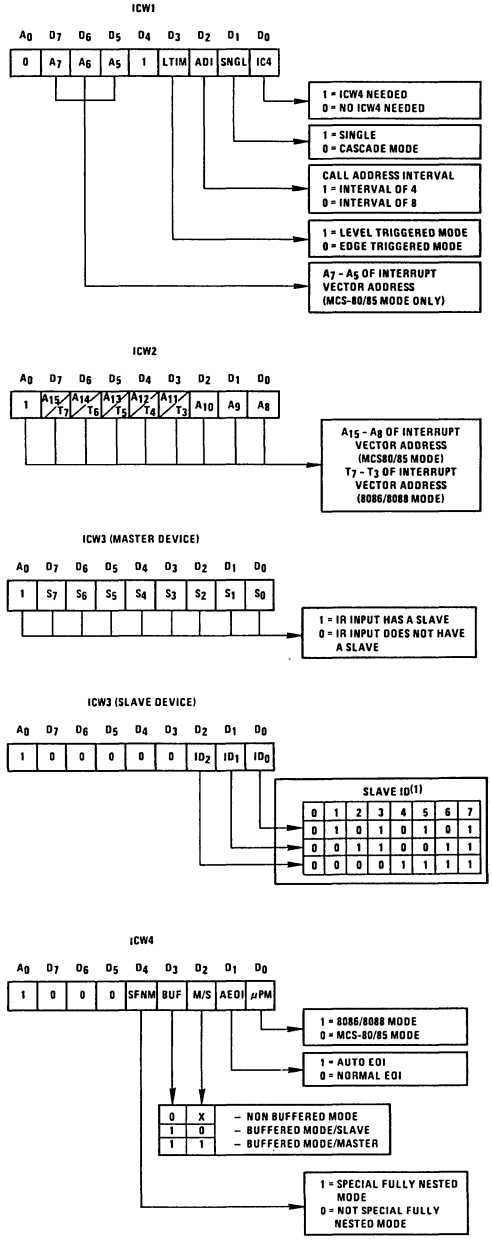
*NOTE: Master/Slave in ICW4 is only used in the buffered mode.

INITIALIZATION COMMAND WORDS 1 AND 2 (ICW1, ICW2)

A5 - A15: Page starting address of service routines. In an 8080/85 system, the 8 request levels will generate CALLS to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.



82C59A INITIALIZATION SEQUENCE



82C59A INITIALIZATION COMMAND WORD FORMAT

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

The address format is 2 bytes long (A0 - A15). when the routine interval is 4, A0 - A4 are automatically inserted by the 82C59A, while A5 - A15 are programmed externally. When the routine interval is 8, A0 - A5 are automatically inserted by the 82C59A while A6 - A15 are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an 80C86 system, A15 - A11 are inserted in the five most significant bits of the vectoring byte and the 82C59A sets the three least significant bits according to the interrupt level. A10-A5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 82C59A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only 82C59A in the system. If SNGL = 1, no ICW3 will be issued.

IC4: If this bit is set - ICW4 has to be issued. If ICW4 is not needed, set IC4 = 0.

INITIALIZATION COMMAND WORD 3 (ICW3)

This word is read only when there is more than one 82C59A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when $\overline{SP}$=1, or in buffered mode when M/S=1 in ICW4) a "1" is set for each slave in the bit corresponding to the appropriate IR line for the slave. The master then will release byte 1 of the call sequence (for 8080/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for 80C86, only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{SP}$=0, or if BUF = 1 and M/S = 0 in ICW4), bits 2-0 identify the slave. The slave compares its cascade input with these bits and if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for 80C86) are released by it on the Data Bus (Note: the slave address must correspond to the IR line it is connected to in the master ID).

INITIALIZATION COMMAND WORD 4 (ICW4)

SFNM: If SFNM = 1, the special fully nested mode is programmed.

BUF: If BUF = 1, the buffered mode is programmed. In buffered mode, $\overline{SP/EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 82C59A is programmed to be a master. M/S = 0 means the 82C59A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1, the automatic end of interrupt mode is programmed.

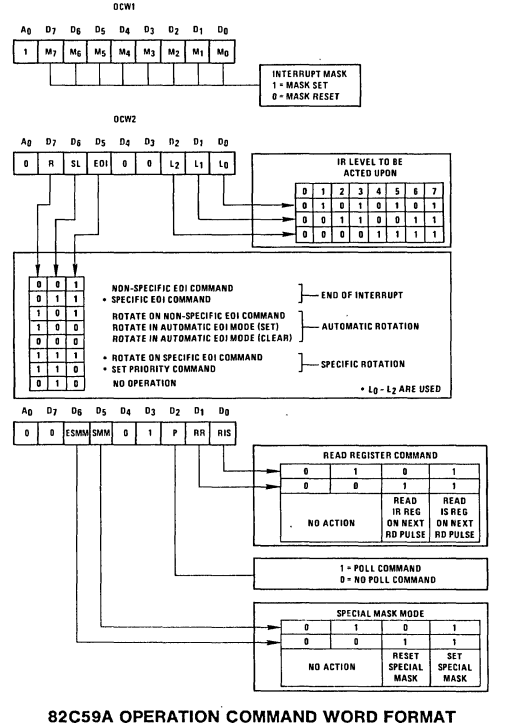
μPM: Microprocessor mode: μPM = 0 sets the 82C59A for 8080/85 system operation, μPM = 1 sets the 82C59A for 80C86 system operation.

OPERATION COMMAND WORDS (OCWs)

After the Initialization Command Words (ICWs) are programmed into the 82C59A, the device is ready to accept interrupt requests at its input lines. However, during the 82C59A operation a selection of algorithms can command the 82C59A to operate in various modes through the Operation Command Words (OCWs).

OPERATION CONTROL WORDS (OCWs)

A0	D7	D6	D5	D4	D3	D2	D1	D0
OCW1								
1	M7	M6	M5	M4	M3	M2	M1	M0
OCW2								
0	R	SL	EOI	0	0	L2	L1	L0
OCW3								
0	0	ESSM	SMM	0	1	P	RR	RIS



82C59A OPERATION COMMAND WORD FORMAT

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

OPERATION CONTROL WORD 1 (OCW1)

OCW1 sets and clears the mask bits in the Interrupt Mask Register (IMR). M7 - M0 represent the eight mask bits. M = 1 indicates the channel is masked (inhibited), M = 0 indicates the channel is enabled.

OPERATION CONTROL WORD 2 (OCW2)

R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L2, L1, L0 - These bits determine the interrupt level acted upon when the SL bit is active.

OPERATION CONTROL WORD 3 (OCW3)

ESMM - Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM=0, the SMM bit becomes a "don't care".

SMM - Special Mask Mode. If ESMM = 1 and SMM=1, the 82C59A will enter Special Mask Mode. If ESMM = 1 and SMM = 0, the 82C59A will revert to normal mask mode. When ESMM = 0, SMM has no effect.

FULLY NESTED MODE

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (IS0-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last $\overline{INTA}$. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained in the rotating priority mode or via the set priority command.

END OF INTERRUPT (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{INTA}$ pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the 82C59A before returning from a service routine (EOI Command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the 82C59A is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific command is issued the 82C59A will automatially reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI = 1, SL = 0, R = 0).

When a mode is used which may disturb the fully nested structure, the 82C59A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI = 1, SL = 1, R = 0, and L0-L2 is the binary level of the IS bit to be reset).

An IRR bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 82C59A is in the Special Mask Mode.

AUTOMATIC END OF INTERRUPT (AEOI) MODE

If AEOI = 1 in ICW4, then the 82C59A will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the 82C59A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in 8080/85, second in 80C86). Note that from a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single 82C59A.

AUTOMATIC ROTATION (Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most once. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	1	0	0	0	0
PRIORITY STATUS	7	6	5	4	3	2	1	0
	lowest							highest

After Rotate (IR4 was serviced, all other priorities rotated correspondingly)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	0	0	0	0	0
PRIORITY STATUS	2	1	0	7	6	5	4	3
	highest							lowest

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R = 1, SL = 0, EOI = 1) and the Rotate in Automatic EOI Mode which is set by (R = 1, SL = 0, EOI = 0) and cleared by (R = 0, SL = 0, EOI = 0).

SPECIFIC ROTATION (Specific Priority)

The programmer can change priorities by programming the bottom priorities and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R = 1, SL = 1, L0-L2 is the binary priority level code of the code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R = 1, SL = 1, EOI = 1 and LO-L2 = IR level to receive bottom priority).

INTERRUPT MASKS

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IRO, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

SPECIAL MASK MODE

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 82C59A would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where; ESSM = 1, SMM = 1, and cleared where ESSM = 1, SMM = 0.

POLL COMMAND

In this mode, the INT output is not used or the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P = 1 in OCW3. The 82C59A treats the next $\overline{RD}$ pulse to the 82C59A (i.e., $\overline{RD}$ = 0, $\overline{CS}$ = 0) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

The word enabled onto the data bus during RD is:

D7	D6	D5	D4	D3	D2	D1	D0
I	-	-	-	-	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

READING THE 82C59A STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR) or OCW1 (IMR).

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the $\overline{RD}$ pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 0).

The ISR can be read when, prior to the $\overline{RD}$ pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 1).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one: i.e., the 82C59A "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used. In the poll mode, the 82C59A treats the $\overline{RD}$ following a "poll write" operation as an $\overline{INTA}$. After initialization, the 82C59A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{RD}$ is active and A0 = 1 (OCW1). Polling overrides status read when P = 1, RR = 1 in OCW3.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

EDGE AND LEVEL TRIGGERED MODES

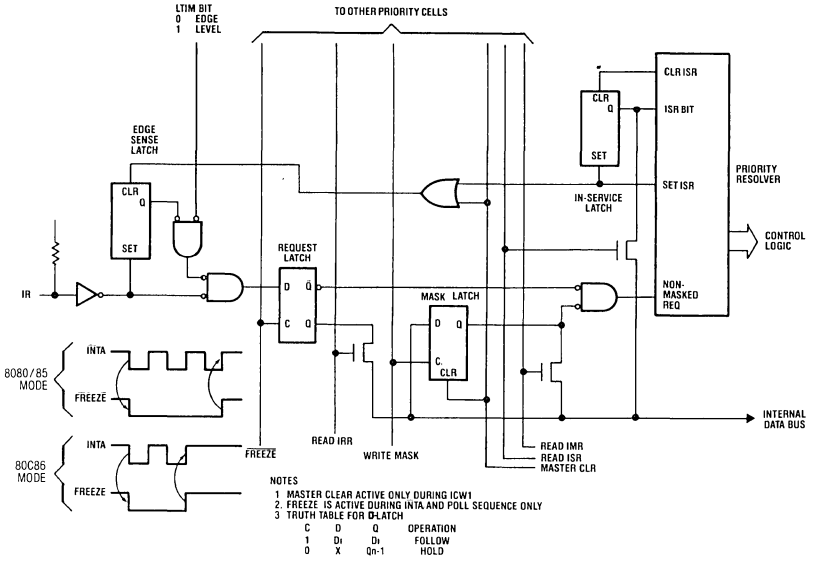
This mode is programmed using bit 3 in ICW1.

If LTIM = "0", an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

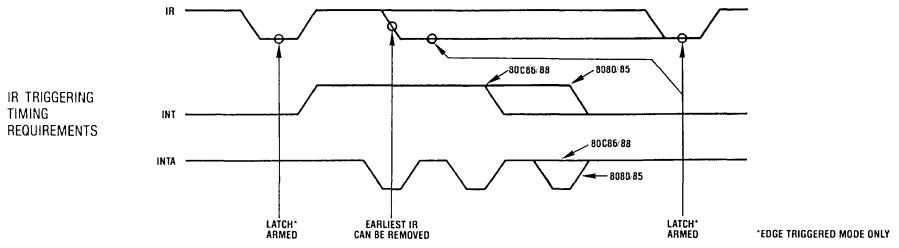
If LTIM = "1", an interrupt request will be recognized by a "high" level on IR input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occuring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the 82C59A. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first $\overline{INTA}$. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.



PRIORITY CELL - SIMPLIFIED LOGIC DIAGRAM



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

In power sensitive applications, it is advisable to place the 82C59A in the edge-triggered mode with the IR lines normally high. This will minimize the current through the pull-up resistors on the IR pins.

THE SPECIAL FULLY NESTED MODE

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the special fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IRs within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specified EOI can be sent to the master, too. If not, no EOI should be sent.

BUFFERED MODE

When the 82C59A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 82C59A to send an enable signal of $\overline{SP}/\overline{EN}$ to enable the buffers. In this mode, whenever the 82C59A's data bus outputs are enabled, the $\overline{SP}/\overline{EN}$ output becomes active.

This modification forces the use of software programming to determine whether the 82C59A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

CASCADE MODE

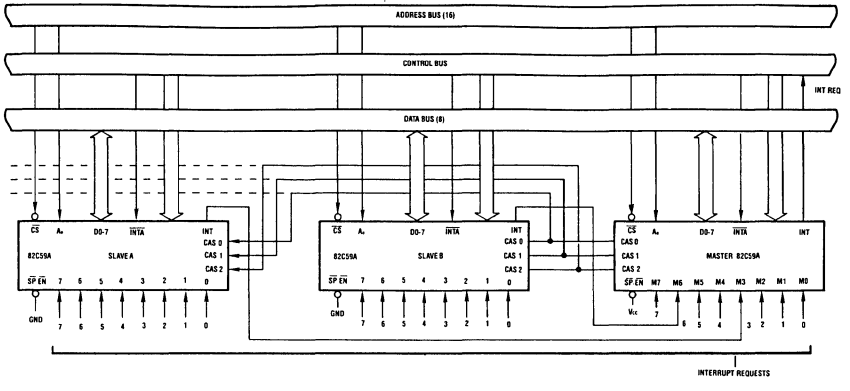
The 82C59A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the $\overline{INTA}$ sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of $\overline{INTA}$. (Byte 2 only for 80C86/80C88).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first $\overline{INTA}$ pulse to the trailing edge of the third pulse. Each 82C59A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. Chip select decoding is required to activate each 82C59A. Note: Auto EOI is supported in the slave mode for the 82C59A.

The cascade lines of the Master 82C59A are activated only for slave inputs, non-slave inputs leave the cascade line inactive (low). Therefore, it is necessary to use a slave address of 0 (zero) only after all other addresses are used.



CASCADING THE 82C59A

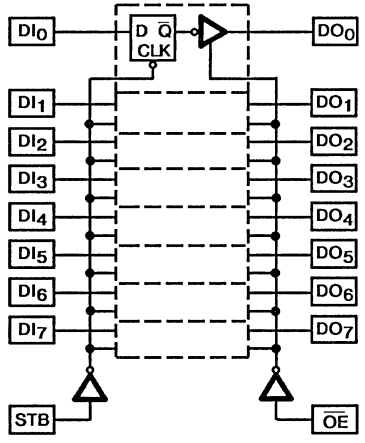
Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Full Eight-Bit Parallel Latching Buffer
- Bipolar 8282 Compatible
- Three-State Noninverting Outputs
- Propagation Delay ..... 35ns Max.
- Gated Inputs:
  - Reduce Operating Power
  - Eliminate the Need for Pull-Up Resistors
- Single 5V Power Supply
- Low Power Operation - ICCSB = 10μA
- Military Operating Temperature Range ..... -55°C to +125°C

Description

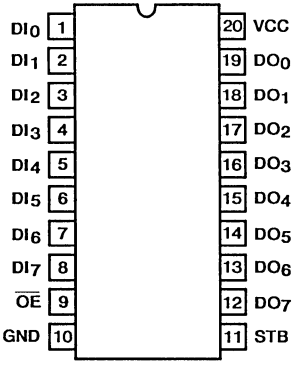
The Harris 82C82/883 is a high performance CMOS Octal Latching Buffer manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C82/883 provides an eight-bit parallel latch/buffer in a 20 pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable ($\overline{OE}$) permits simple interface to state-of-the-art microprocessor systems.

Functional Diagram

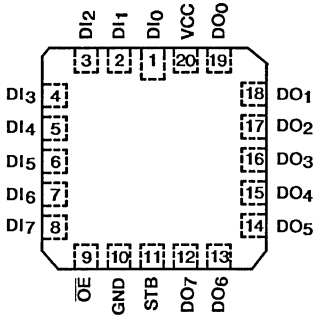


Pinouts

82C82/883 (CERAMIC DIP)
TOP VIEW



82C82/883 (CERAMIC LCC)
TOP VIEW



TRUTH TABLE

STB	$\overline{OE}$	DI	DO
X	H	X	Hi-Z
H	L	L	L
H	L	H	H
↓	L	X	*

H = Logic One
L = Logic Zero
X = Don't Care
* = Latched to Value of Last Data
Hi-Z = High Impedance
↓ = Neg. Transition

PIN NAMES

PIN	DESCRIPTION
DI0-DI7	Data Input Pins
DO0-DO7	Data Output Pins
STB	Active High Strobe
$\overline{OE}$	Active Low Output Enable

5 CMOS PERIPHERALS

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	79°C/W	20°C/W
Ceramic LCC Package	76°C/W	19°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 638mW
Ceramic LCC Package 664mW
Gate Count ..... 65 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... +4.5V to +5.5V

TABLE 1. 82C82/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	VIH	VCC = 5.5V, (Note 1)	1, 2, 3	$-55°C \le T_A \le +125°C$	2.2	-	V
Logical Zero Input Voltage	VIL	VCC = 4.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.8	V
Output High Voltage	VOH	VCC = 4.5V, IOH = -8.0mA, IOH = -100µA, $\overline{OE}$ = GND (Note 2)	1, 2, 3	$-55°C \le T_A \le +125°C$	2.9 VCC-0.4	- -	V V
Output Low Voltage	VOL	$\overline{VCC}$ = 4.5V, IOL = +8.0mA, $\overline{OE}$ = GND (Note 2)	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Input Leakage Current	II	VCC = 5.5V, Pins 1-9, 11, VIN = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	1.0	µA
Output Leakage Current	IO	$\overline{VCC}$ = 5.5V, $\overline{OE} \ge$ VCC-0.5V, VOUT = GND or VCC, Pins 12-19	1, 2, 3	$-55°C \le T_A \le +125°C$	-10.0	+10.0	µA
Standby Power Supply Current	ICCSB	VCC = 5.5V, Outputs Open, VIN = VCC or GND	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	µA

NOTES: 1. VIH is measured by applying a pulse of magnitude = VIHmin to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins (STB, $\overline{OE}$) are tested separately with all device data inputs at VCC-0.4V.

2. Interchanging of force and sense conditions is permitted.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. 82C82/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
TIMING REQUIREMENTS							
Propagation Delay, Input to Output	TIVOV(1)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	35	ns
Propagation Delay, STB to Output	TSHOV(2)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	55	ns
Output Enable Time	TELOV(4)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Input to STB Set Up Time	TIVSL(5)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Input to STB Hold Time	TSLIX(6)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	25	-	ns
STB High Time	TSHSL(7)	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	25	-	ns

NOTES: 1. All A.C. parameters tested as per test load circuits and definitions in Figures 1-4. Input rise and fall times area driven at 1ns/V.

2. Tested as follows: f = 1MHz, VIH = 2.6V (VIH for STB $\geq$ VCC - 0.5V), VIL = 0.4V, CL = 50pf (unless otherwise specified), VOH $\geq$ 1.5V, VOL $\leq$ 1.5V.

TABLE 3. 82C82/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, f = 1MHz, All Measurements Referenced to GND	1, 3	$T_A = +25^oC$	-	13	pF
			1, 4	$T_A = +25^oC$	-	12	pF
Output Capacitance	COUT	VCC = Open, f = 1MHz, All Measurements Reference to GND	1, 3	$T_A = +25^oC$	-	20	pF
			1, 4	$T_A = +25^oC$	-	15	pF
Output Disable Time	TEHOZ	VCC = 4.5V and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	35	ns
Input Rise/Fall Time	TR, TF	VCC = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	20	ns

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. Tested as follows: f = 1MHz, VIH = 2.6V (VIH for STB $\geq$ VCC-0.5V), VIL = 0.4V, CL = 50pF (unless otherwise specified), VOH $\geq$ 1.5V, VOL $\leq$ 1.5V.

3. For Ceramic DIP package.

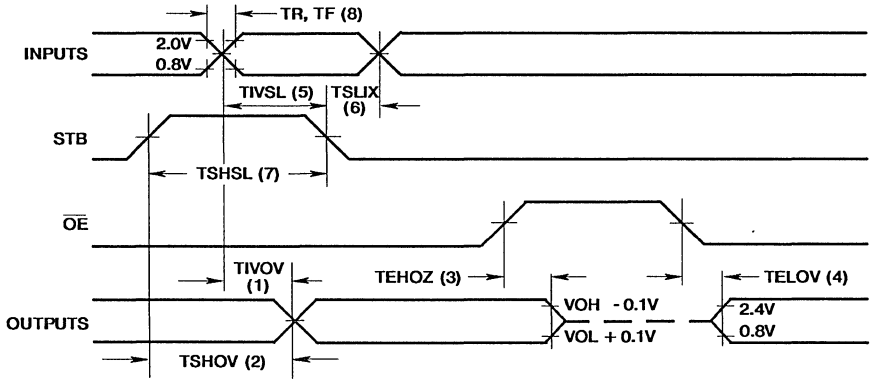
4. For Ceramic LCC package.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

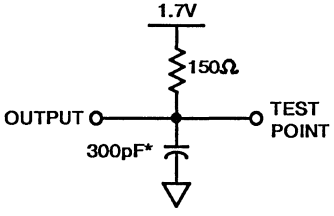
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Timing Waveform

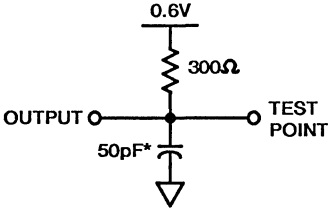


All timing measurements are made at 1.5V unless otherwise noted.

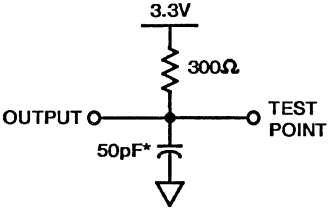
Test Load Circuits



TIVOV, TSHOV, TELOV



TEHOZ OUTPUT HIGH DISABLE

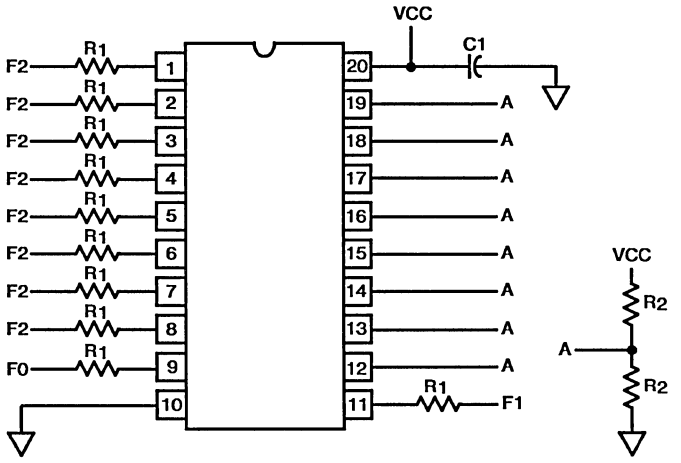


TEHOZ OUTPUT LOW DISABLE

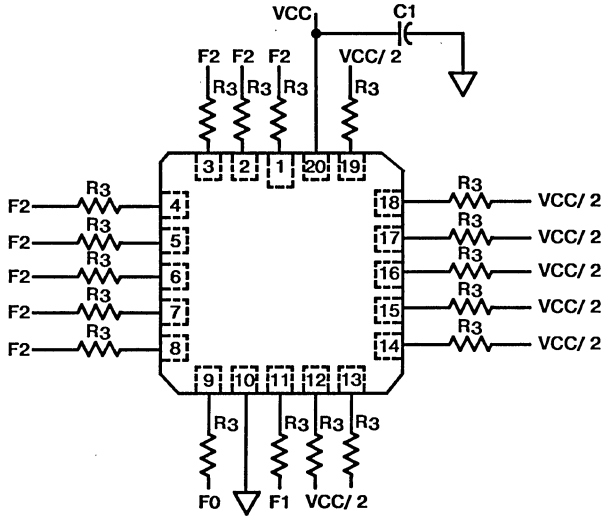
* Includes stray and jig capacitance

Burn-In Circuits

82C82/883 CERAMIC DIP



82C82/883 CERAMIC LCC



NOTES:
VCC = 5.5V ± 0.5V, Gnd = 0V
VIH = 4.5V ± 10%
VIL = -0.2V to 0.4V
R1 = 47kΩ ± 5%
R2 = 2.0kΩ ± 5%
R3 = 4.2kΩ ± 5%
R4 = 470kΩ ± 5%
C1 = 0.01μF minimum
F0 = 100kHz ± 10%
F1 = F0/2, F2 = F1/2

Metallization Topology

DIE DIMENSIONS:
118.1 x 92.1 x 19 ± 1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 1kÅ

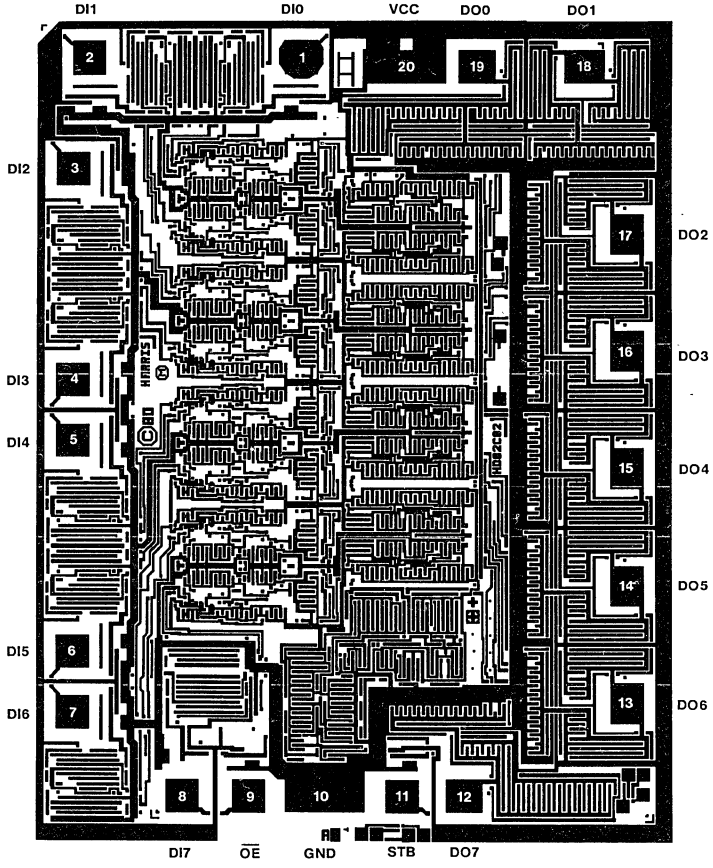
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy (LCC has Gold Preform)
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
2.00 x 10^5 A/cm^2

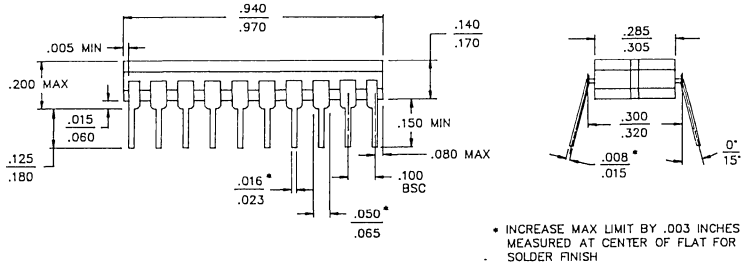
Metallization Mask Layout

82C82/883



Packaging†

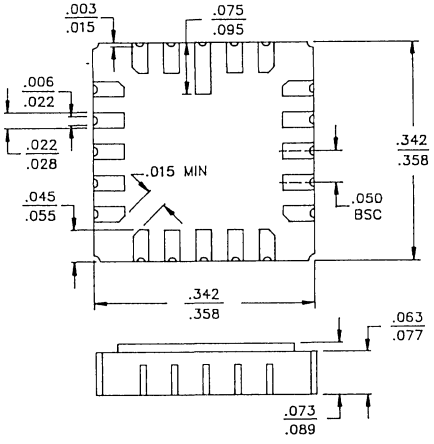
20 PIN CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-8

20 PAD CERAMIC LCC
BOTTOM VIEW



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Gated Inputs

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between VCC and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create an indeterminate logic state at the input and cause a disruption in device operation.

The Harris 82C8X series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled ($\overline{OE}$ = logic one for 82C86H/87H). These gated inputs disconnect the input circuitry from the VCC and ground power supply pins by turning off the upper P-channel and lower N-channel (see Figures 1, 2). No new current flow from VCC to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

D.C. input voltage levels can also cause an increase in ICC if these input levels approach the minimum VIH or maximum VIL conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode (STB = logic one). ICC remains below the maximum ICC standby specification of 10mA during the time inputs are disabled, thereby greatly reducing the average power dissipation of the 82C8X series devices.

Typical 82C82 System Example

In a typical 80C86/88 system, the 82C82 is used to latch multiplexed addresses and the STB input is driven by ALE (Address Latch Enable) (see Figure 3). The high pulse width of ALE is approximately 100ns with a bus cycle time of 800ns (80C86/88 @ 5MHz). The 82C82 inputs are active only 12.5% of the bus cycle time. Average power dissipation related to input transitioning is reduced by this factor also.

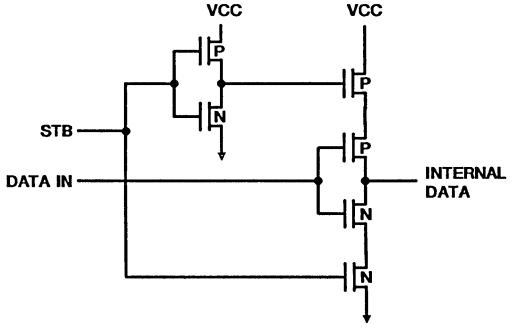


FIGURE 1. 82C82/83H

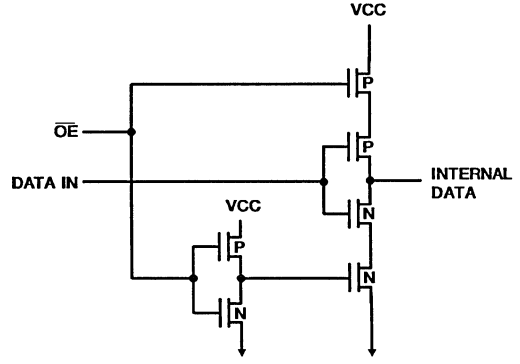


FIGURE 2. 82C86H/87H GATED INPUTS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Application Information

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C82 data sheet is determined by

$I = CL\ (dv/dt)$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$I = CL$

$$\frac{(VCC \times 80\%)}{tR/tF}$$

where tR = 20ns, VCC = 5.0V, CL = 300pF on each of eight outputs.

$I = (8 \times 300 \times 10^{-12}) \times (5.0V \times 0.8)/(20 \times 10^{-9})$

$= 480mA$

This current spike may cause a large negative voltage spike on VCC, which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1µF ceramic disc decoupling capacitor be placed between VCC and GND at each device, with placement being as near to the device as possible.

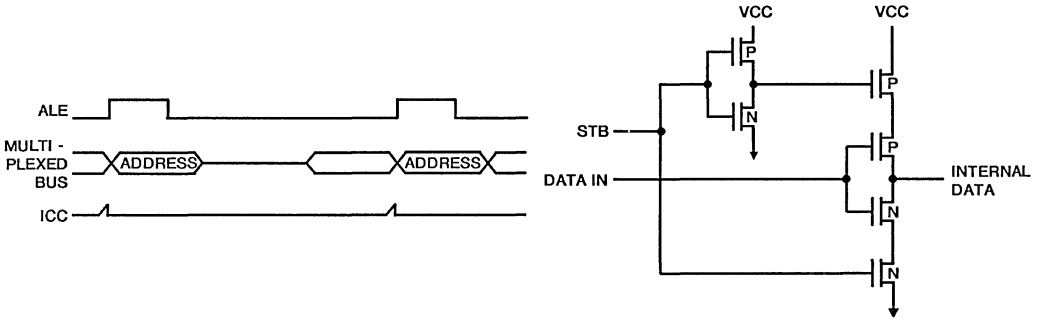


FIGURE 3. SYSTEM EFFECTS OF GATED INPUTS

HARRIS

82C83H/883

CMOS Octal latching Inverting Bus Driver

June 1989

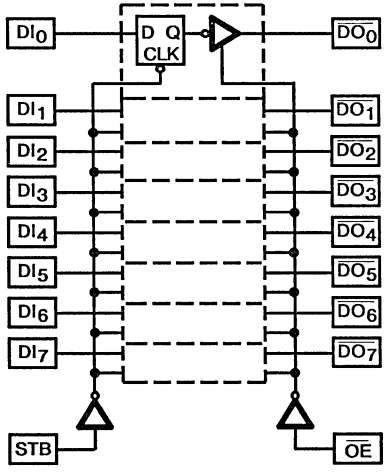
Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1
- Full Eight-Bit Parallel Latching Buffer
- Bipolar 8283 Compatible
- Three-State Inverting Outputs
- Propagation Delay ..... 25ns Max
- Gated Inputs:
  - ▸ Reduce Operating Power
  - ▸ Eliminate the Need for Pull-Up Resistors
- Single 5V Power Supply
- Low Power Operation - ICCSB 10μA
- Military Operating Temperature Range ..... -55°C to +125°C

Description

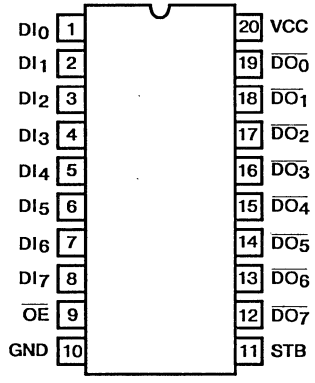
The Harris 82C83H/883 is a high performance CMOS Octal Latching Buffer manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C83H/883 provides an eight-bit parallel latch/buffer in a 20 pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable ($\overline{OE}$) permits simple interface to microprocessor systems. The 82C83H/883 provides inverted data at the outputs.

Functional Diagram

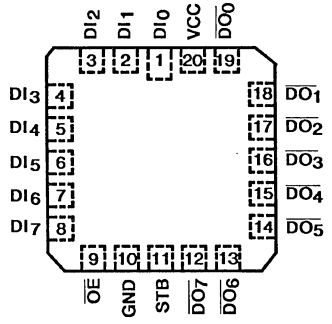


Pinouts

82C83H/883 (CERAMIC DIP)
TOP VIEW



82C83H/883 (CERAMIC LCC)
TOP VIEW



TRUTH TABLE

STB	$\overline{OE}$	DI	$\overline{DO}$
X	H	X	Hi-Z
H	L	L	H
H	L	H	L
↓	L	X	*

H = Logic One
L = Logic Zero
X = Don't Care
Hi-Z = High Impedance
↓ = Neg. Transition
* = Latched to Value of Last Data

PIN NAMES

PIN	DESCRIPTION
DI0-DI7	Data Input Pins
$\overline{DO0}$-$\overline{DO7}$	Data Output Pins
$\overline{STB}$	Active High Strobe
$\overline{OE}$	Active Low Output Enable

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... 300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	70°C/W	15°C/W
Ceramic LCC Package	76°C/W	19°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 720mW
Ceramic LCC Package 664mW
Gate Count ..... 265 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... ± 4.5V to +5.5V

TABLE 1. 82C83H/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical "1" Input Voltage	VIH	VCC = 5.5 V, (Note 1)	1, 2, 3	$-55°C \le T_A \le +125°C$	2.2	-	V
Logical "0" Input Voltage	VIL	VCC = 4.5 V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.8	V
Output High Voltage	VOH	VCC = 4.5V, IOH = -8.0mA IOH = -100µA, $\overline{OE}$ = GND (Note 2)	1, 2, 3	$-55°C \le T_A \le +125°C$	 3.0 VCC-0.4	 - -	 V V
Output Low Voltage	VOL	VCC = 4.5V, IOL = +15.0mA $\overline{OE}$ = GND (Note 2)	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.45	V
Input Leakage Current	II	VCC = 5.5V, Pins 1-9, 11, VIN = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-10.0	+10.0	µA
Output Leakage Current	IO	VCC = 5.5V, $\overline{OE} \ge$ VCC -0.5V VOUT = GND or VCC, Pins 12-19	1, 2, 3	$-55°C \le T_A \le +125°C$	-10.0	+10.0	µA
Standby Power Supply Current	ICCSB	VCC = 5.5 V, Outputs Open, VIN = VCC or GND	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	µA

NOTES: 1. VIH is measured by applying a pulse of magnitude = VIHmin to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins (STB, $\overline{OE}$) are tested separately with all device data inputs at VCC-0.4V.

2. Interchanging of force and sense conditions is permitted.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. 82C83H/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
TIMING REQUIREMENTS							
Propagation Delay, Input to Output	TIVOV(1)	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	25	ns
Propagation Delay, STB to Output	TSHOV(2)	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Output Enable Time	TELOV(4)	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	45	ns
Input to STB Set Up Time	TIVSL(5)	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Input to STB Hold Time	TSLIX(6)	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	ns
STB High Time	TXHSL(7)	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	ns

NOTES: 1. All A.C. parameters tested as per test load circuits and definitions in Test Load Circuits. Input rise and fall times area driven at 1ns/V.

2. Tested as follows: f = 1MHz, VIH = 2.6V (VIH for STB $\geq$ VCC - 0.5V), VIL = 0.4V, CL = 50pF (unless otherwise specified), VOH $\geq$ 1.5V, VOL $\leq$ 1.5V.

TABLE 3. 82C83H/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1, 3	$T_A = +25^oC$	-	13	pF
			1, 4	$T_A = +25^oC$	-	12	pF
Output Capacitance	COUT	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1, 3	$T_A = +25^oC$	-	20	pF
			1, 4	$T_A = +25^oC$	-	15	pF
Output Disable Time	TEHOZ(3)	VCC = 4.5 and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	22	ns
Input Rise/Fall Time	TR, TF(8)	VCC = 4.5 and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	20	ns
Propagation Delay, Input to Output	TIVOV(1)	VCC = 4.5 and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Propagation Delay, STB to Output	TSHOV(2)	VCC = 4.5 and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Output Enable Time	TELOV(4)	VCC = 4.5 and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	10	-	ns

NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. Tested as follows: f = 1MHz, VIH = 2.6V (VIH for STB $\geq$ VCC - 0.5V), VIL = 0.4V, CL = 50pF (unless otherwise specified), VOH $\geq$ 1.5 V, VOL $\leq$ 1.5V.

3. For Ceramic DIP package.

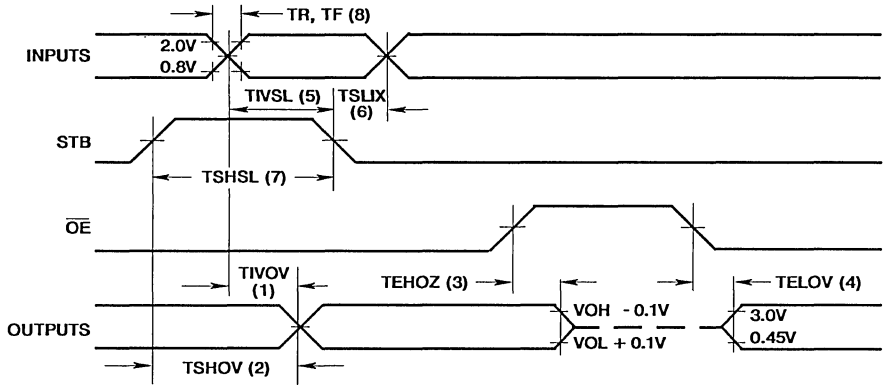
4. For Ceramic LCC package.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

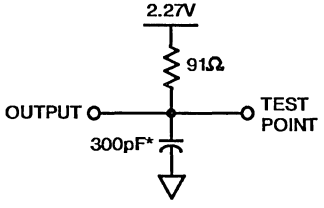
CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

Timing Waveform

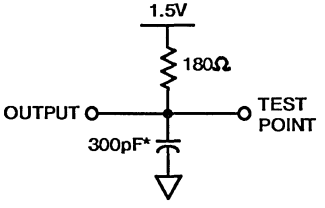


All timing measurements are made at 1. 5V unless otherwise noted.

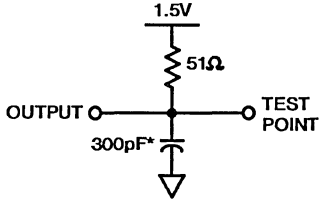
Test Load Circuits



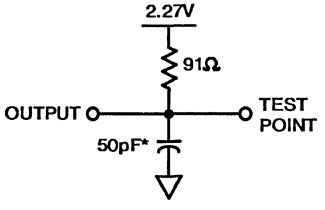
TIVOV, TSHOV



TELOV OUTPUT HIGH ENABLE



TELOV OUTPUT LOW ENABLE

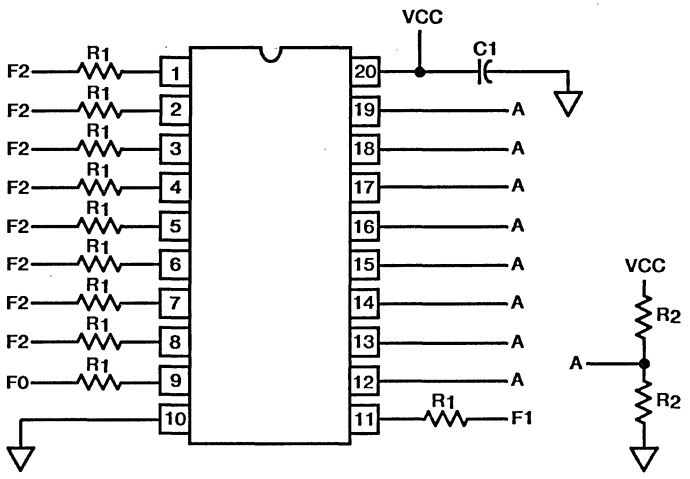


TEHOZ OUTPUT LOW/HIGH DISABLE

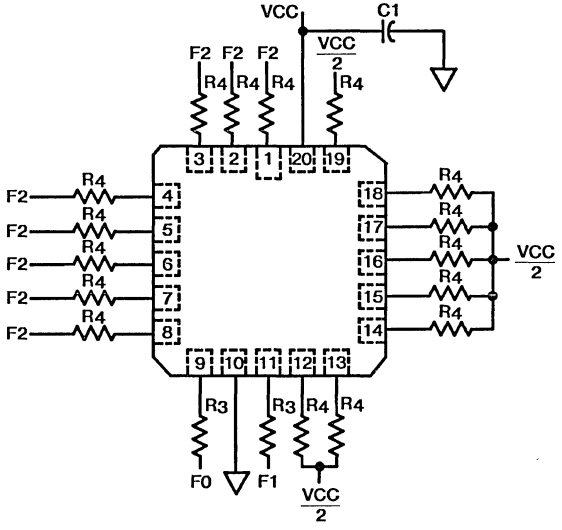
*Includes jig and stray capacitance

Burn-In Circuits

82C83H/883 CERAMIC DIP



82C83H/883 CERAMIC LCC



NOTES:
VCC = 5.5V ± 0.5V GND = 0V
VIH = 4.5V ± 10%
VIL = -0.2 to 0.4V
R1 = 47kΩ ± 5%
R2 = 2.0kΩ ± 5%
R3 = 1.0kΩ ± 5%
R4 = 5.0kΩ ± 5%
C1 = 0.01μF Minimum
F0 = 100kHz ± 10%
F1 = F0/2, F2 = F1/2, F3 = F2/2

Metallization Topology

DIE DIMENSIONS:
138.6 x 155.5 x 19 ± 1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 2kÅ

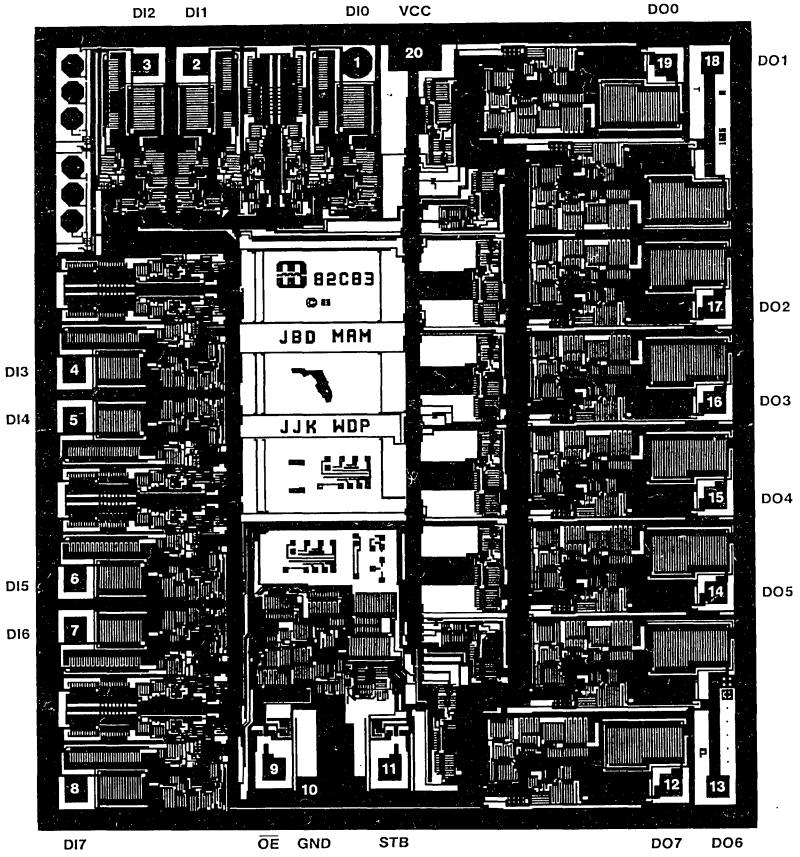
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy (LCC has Gold Preform)
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
2.0 x 10^5 A/cm^2

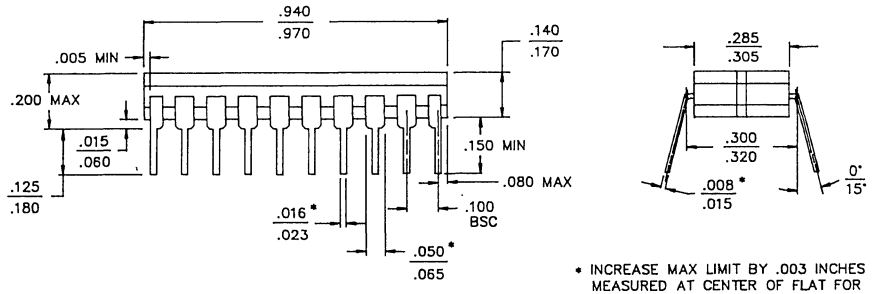
Metallization Mask Layout

82C83H/883



Packaging†

20 PIN CERAMIC DIP

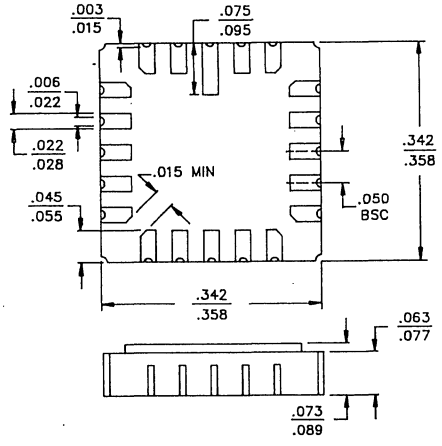


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-8

20 PAD CERAMIC LCC
BOTTOM VIEW



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Gated Inputs

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between VCC and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create an indeterminate logic state at the inputs and cause a disruption in device operation.

The Harris 82C8X series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled ($\overline{OE}$ = logic one for the 82C86H/87H). These gated inputs disconnect the input circuitry from the VCC and ground power supply pins by turning off the upper P-channel and lower N-channel (See Figures 1 and 2). No current flow from VCC to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

D.C. input voltage levels can also cause an increase in ICC if these input levels approach the minimum VIH or maximum VIL conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode (STB = logic one). ICC remains below the maximum ICC standby specification of 10μA during the time inputs are disabled, thereby greatly reducing the average power dissipation of the 82C8X series devices.

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C83H data sheet is determined by

$$I = CL\ (dv/dt)$$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = CL\ \frac{(VCC \times 80\%)}{tR/tF}$$

where tR = 20ns, VCC = 5.0V, CL = 300pF on each eight outputs.

$$I = (8 \times 300 \times 10^{-12}) \times (5.0V \times 0.8)/(20 \times 10^{-9})$$
$$= 480mA$$

This current spike may cause a large negative voltage spike on VCC which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1μF ceramic disc capacitor be placed between VCC and GND at each device, with placement being as near to the device as possible.

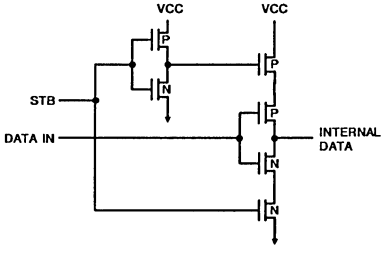


FIGURE 1. 82C82/83H

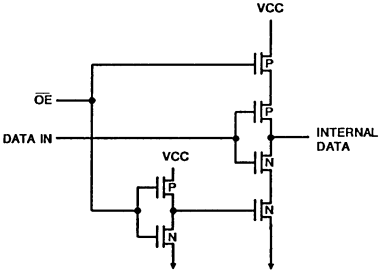
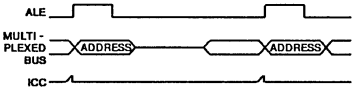


FIGURE 2. 82C86H/87H GATED INPUTS



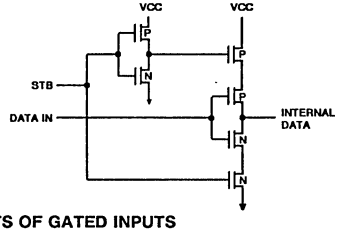


FIGURE 3. SYSTEM EFFECTS OF GATED INPUTS

HARRIS

82C84A/883

June 1989

CMOS Clock Generator Driver

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Generates the System Clock For CMOS or NMOS Microprocessors
- Up to 25MHz Operation
- Uses a Parallel Mode Crystal Circuit or External Frequency Source
- Provides Ready Synchronization
- Generates System Reset Output From Schmitt Trigger Input
- TTL Compatible Inputs/Outputs
- Very Low Power Consumption
- Single 5V Power Supply
- Military Operating Temperature Range ..... -55°C to +125°C

Description

The Harris 82C84A/883 is a high performance CMOS Clock Generator-driver which is designed to service the requirements of both CMOS and NMOS microprocessors such as the 80C86, 80C88, 8086 and the 8088. The chip contains a crystal controlled oscillator, a divide-by-three counter and complete "Ready" sychronization and reset logic.

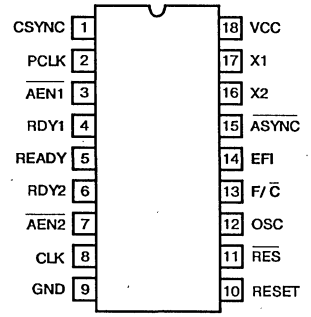
Static CMOS circuit design permits operation with an external frequency source from DC to 25MHz. Crystal controlled operation to 25MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors.

All inputs (except X1 and $\overline{RES}$) are TTL compatible over temperature and voltage ranges.

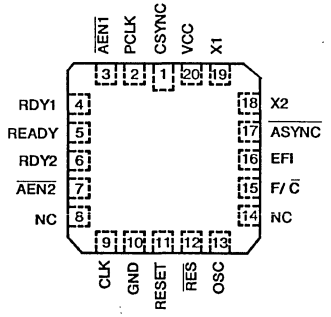
Power consumption is a fraction of that of the equivalent bipolar circuits. This speed-power characteristic of CMOS permits the designer to custom tailor his system design with respect to power and/or speed requirements.

Pinouts

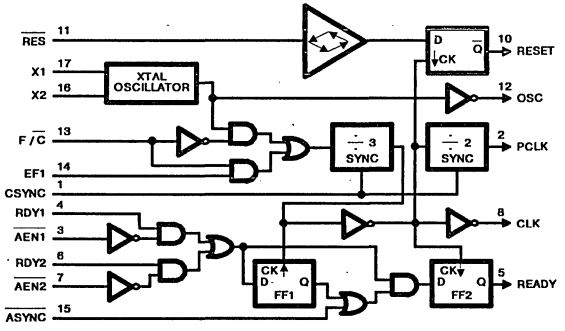
82C84A/883 (CERAMIC DIP)
TOP VIEW



82C84A/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



CONTROL PIN	LOGICAL 1	LOGICAL 0
F/$\overline{C}$	External Clock	Crystal Drive
$\overline{RES}$	Normal	Reset
RDY1 RDY2	Bus Ready	Bus Not Ready
$\overline{AEN1}$ $\overline{AEN2}$	Address Disabled	Address Enable
$\overline{ASYNC}$	1 Stage Ready Synchronization	2 Stage Ready Synchronization

Pin Description

SYMBOL	DIP PIN NUMBER	TYPE	DESCRIPTION
$\overline{AEN1}$, $\overline{AEN2}$	3, 7	I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2 Two $\overline{AEN}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non-Multi-Master configurations, the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	4, 6	I	BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	15	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	5	O	READY: READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	17, 16	I O	CRYSTAL IN: X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.*
F/$\overline{C}$	13	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ is a strapping option. When strapped LOW. F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated for the EFI input.
EFI	14	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	8	O	PROCESSOR CLOCK: CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus. CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle.
PCLK	2	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
OSC	12	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	11	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used to generate RESET. The 82C84A/883 provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	10	O	RESET: RESET is an active HIGH signal which is used to reset the 80C86 family processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	1	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple 82C84As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND	9		Ground
VCC	18		VCC: the +5V power supply pin. A 0.1 µF capacitor between VCC and GND is recommended for decoupling.

* If the crystal inputs are not used X1 must be tied to VCC or GND and X2 should be left open.

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec)..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	86°C/W	24°C/W
Ceramic LCC Package	73°C/W	20°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 580mW
Ceramic LCC Package 532mW
Gate Count ..... 50 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Voltage Range ..... +4.5V to +5.5V

TABLE 1. 82C84A/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	VIH	VCC = 5.5V (Notes 1, 2)	1, 2, 3	$-55°C \le T_A \le +125°C$	2.2	-	V
Logical Zero Input Voltage	VIL	VCC = 4.5V (Notes 1, 2, 3)	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.8	V
Reset Input High Voltage	VIHR	VCC = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	VCC-0.8	-	V
Reset Input Low Voltage	VILR	VCC = 4.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.5	V
Reset Input Hysteresis	VT+ VT-	VCC = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	0.2VCC	-	V
Output High Voltage	VOH	VCC = 4.5V, (Note 4) IOH = -4.0mA for CLK Output, IOH = -2.5mA for all others	1, 2, 3	$-55°C \le T_A \le +125°C$	VCC-0.4	-	V
Output Low Voltage	VOL	VCC = 4.5V, (Note 4) IOL = +4.0mA for CLK Output, IOL = +2.5mA for all others	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Input Leakage Current	II	VCC = 5.5V, VIN = GND or VCC except $\overline{ASYNC}$, X1 (Note 5)	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Operating Power Supply Current	ICCOP	VCC = 5.5V, Ouputs Open, Crystal Frequency = 25MHz, (Note 6)	1, 2, 3	$-55°C \le T_A \le +125°C$	-	40	mA

NOTES: 1. F/$\overline{C}$ is a strap option and should be held either $\le$ 0.8V or $\ge$ 2.2V. Does not apply to X1 or X2 pins.
2. Due to test equipment limitations related to noise, the actual tested value may differ from that specified, but the specified limit is guaranteed.
3. CSYNC pin is tested with VIL $\le$ 0.8V.
4. Interchanging of force and sense conditions is permitted.
5. $\overline{ASYNC}$ pin includes an internal 17.5kΩ nominal pull-up resistor. For $\overline{ASYNC}$ input at GND, $\overline{ASYNC}$ input leakage current = 300µA nominal. X1 - crystal feedback input.
6. f = 25MHz may be tested using the extrapolated value based on measurements taken at f = 2MHz and f = 10MHz.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. 82C84A/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
TIMING REQUIREMENTS							
External Frequency High Time	TEHEL(1)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	13	-	ns
External Frequency Low Time	TELEH(2)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	13	-	ns
EFI Period	TELEL(3)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	36	-	ns
RDY1, RDY2 Active Setup to CLK, $\overline{ASYNC}$ = HIGH	TR1VCL(4)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	35	-	ns
XTAL Frequency		(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	2.4	25	MHz
RDY1, RDY2 Active Setup Time to CLK, $\overline{ASYNC}$ = LOW	TR1VCH(5)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	35	-	ns
RDY1, RDY2 Inactive Setup Time to CLK	TR1VCH(6)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	35	-	ns
RDY1, RDY2 Hold to CLK	TCLR1X(7)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
$\overline{ASYNC}$ Setup to CLK	TAYVCL(8)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
$\overline{ASYNC}$ Hold to CLK	TCLAYX(9)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2	TA1VR1V(10)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	ns
$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	TCLA1X(11)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
CSYNC Setup to EFI	TYHEH(12)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
CSYNC Hold to EFI	TEHYL(13)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
RES Setup to CLK	TI1HCL(15)	(Note 3)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	65	-	ns
TIMING RESPONSES							
RES Hold to CLK	TCLI1H(16)	(Note 3)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
CLK Cycle Period	TCLCL(17)	(Note 6)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	125	-	ns
CLK High Time	TCHCL(18)	(Note 6)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	(1/3* TCLCL) +2.0	-	ns
CLK Low Time	TCLCH(19)	(Note 6)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	(2/3* TCLCL) -15.0	-	ns
CLK Rise or Fall time	TCH1CH2(20) TCL2CL1(21)	From 1.0V to 3.0V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	10	ns
PCLK High Time	TPHPL(22)	(Note 6)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TCLCL -20	-	ns
PCLK Low Time	TPLPH(23)	(Note 6)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TCLCL -20	-	ns
Ready Inactive to CLK	TRYLCL(24)	(Note 4)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-8	-	ns
Ready Active to CLK	TRYHCH(25)	(Note 5)	9, 10,11	$-55^oC \leq T_A \leq +125^oC$	(2/3* TCLCL) -15.0	-	ns

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. 82C84A/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
TIMINIG RESPONSES (Continued)							
CLK to Reset Delay	TCLIL(26)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
CLK to PCLK High Delay	TCLPH(27)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	22	ns
CLK to PCLK Low Delay	TCLPL(28)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	22	ns
OSC to CLK High Delay	TOLCH(29)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	22	ns
OSC to CLK Low Delay	TOLCL(30)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	35	ns

NOTES: 1. Tested as follows: f = 2.4MHz, VIH = 2.6V, VIL = 0.4V, CL = 50pF, VOH = $\geq$ 1.5V, VOL $\leq$ 1.5V, unless otherwise specified. $\overline{RES}$ and F/$\overline{C}$ must switch between 0.4V and VCC-0.4V. Input rise and fall times driven at 1 ns/V. VIL $\leq$ VIL (max) - 0.4V for CSYNC pin. VCC = 4.5V and 5.5V.

2. Tested using EFI or X1 input pin.
3. Setup and hold necessary only to guarantee recognition at next clock.
4. Applies only to T2 states.
5. Applies only to T3 TW states.
6. Tested with EFI input frequency = 4.2MHz.

TABLE 3. 82C84A/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	-	10	pF
Output Capacitance	COUT	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	-	15	pF
CSYNC Width	TYHYL(14)		1, 2	$-55^oC \leq T_A \leq +125^oC$	2* TELEL	-	ns
OSC to CLK High Delay	TOLCH(29)		1, 2	$-55^oC \leq T_A \leq +125^oC$	-5	-	ns
OSC to CLK Low Delay	TOHCL(30)		1, 2	$-55^oC \leq T_A \leq +125^oC$	2	-	ns

NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. Input test signals must switch between VIL (max) - 0.4V and VIH (min) + 0.4V. $\overline{RES}$ and F/$\overline{C}$ must switch between 0.4V and VCC-0.4V. Input rise and fall times driven at 1 ns/V. VIL $\leq$ VIL (max) - 0.4 V for CSYNC pin. VCC = 4.5V and 5.5V.

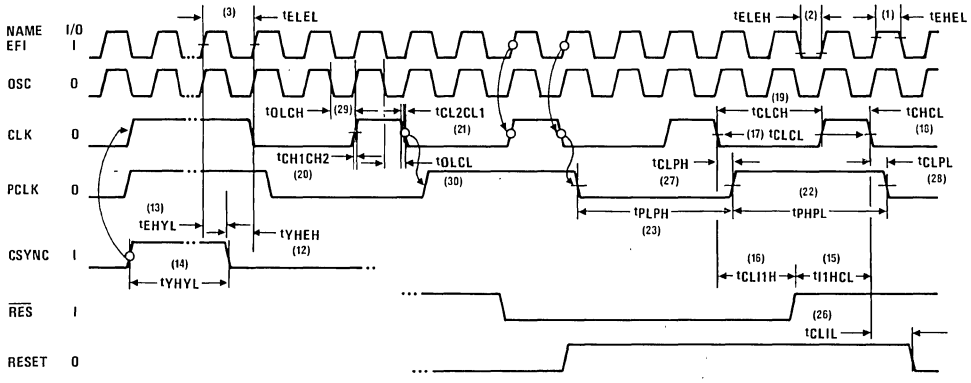
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

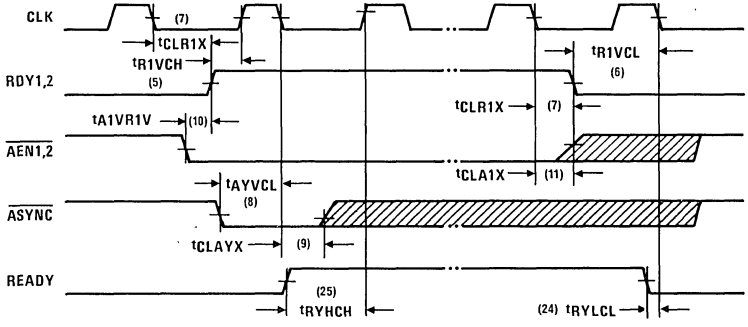
Timing Waveforms

WAVEFORMS FOR CLOCKS AND RESET SIGNALS

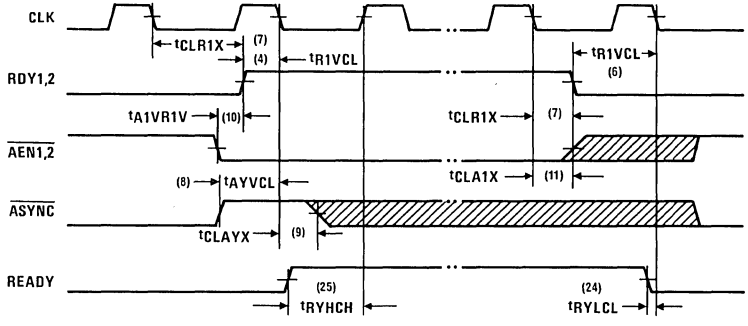


NOTE: All timing measurements are made at 1.5 Volts, unless otherwise noted.

WAVEFORMS FOR READY SIGNALS (FOR ASYNCHRONOUS DEVICES)

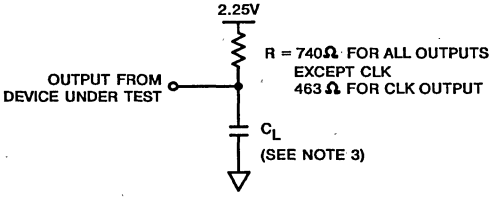


WAVEFORMS FOR READY SIGNALS (FOR SYNCHRONOUS DEVICES)



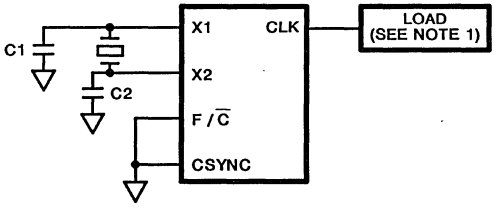
Test Load Circuits

TEST LOAD MEASUREMENT CONDITIONS

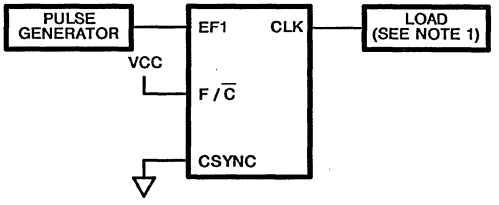


NOTES: 1. C_L =100pF for CLK output
2. C_L = 50pF for all outputs except CLK
3. C_L = Includes probe and jig capacitance

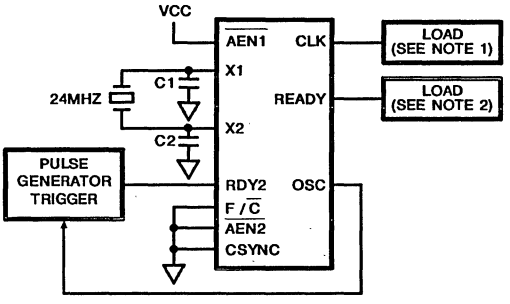
TCHCL, TCLCH LOAD CIRCUIT



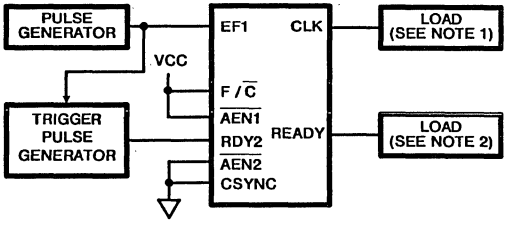
TCHCL, TCLCH LOAD CIRCUIT



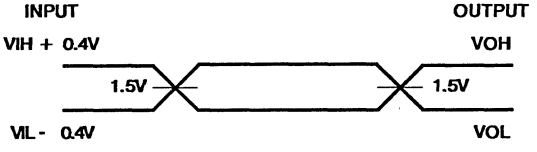
TRYLCL, TRYHCH LOAD CIRCUIT



TRYLCL, TRYHCH LOAD CIRCUIT



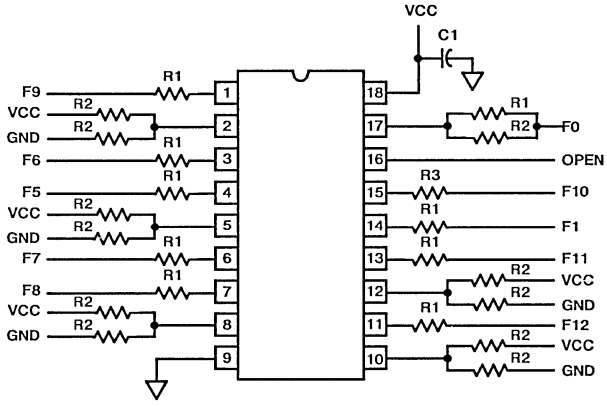
A.C. Testing Input, Output Waveform



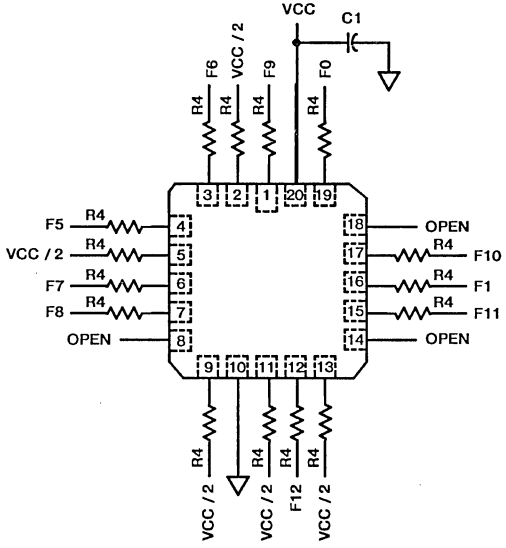
NOTE: Input test signals must switch between VIL (maximum) -0.4V and VIH (minimum) +0.4V. $\overline{RES}$ and F/$\overline{C}$ must switch between 0.4V and VCC -0.4V. Input rise and fall times driven at 1ns/V. VIL $\leq$ VIL (max) -0.4V for CSYNC pin. VCC -4.5V and 5.5V.

Burn-In Circuits

82C84A/883 CERAMIC DIP



82C84A/883 CERAMIC LCC



NOTES:
VCC = 5.5V ±0.5V, GND = 0V
VIH =4.5V ±10%
VIL = -0.2 to 0.4V
R1 = 47kΩ, ±5%,
R2 = 10kΩ, ±5%,
R3 = 2.2kΩ, ±5%,
R4 = 1.2kΩ, ±5%,
C1 = 0.01µF (minimum)
F0 = 100kHz ±10%
F1 = F0/2, F2 = F1/2, . . . F12 = F11/2

Metallization Topology

DIE DIMENSIONS:
66.1 x 70.5 x 19 ± 1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 1kÅ

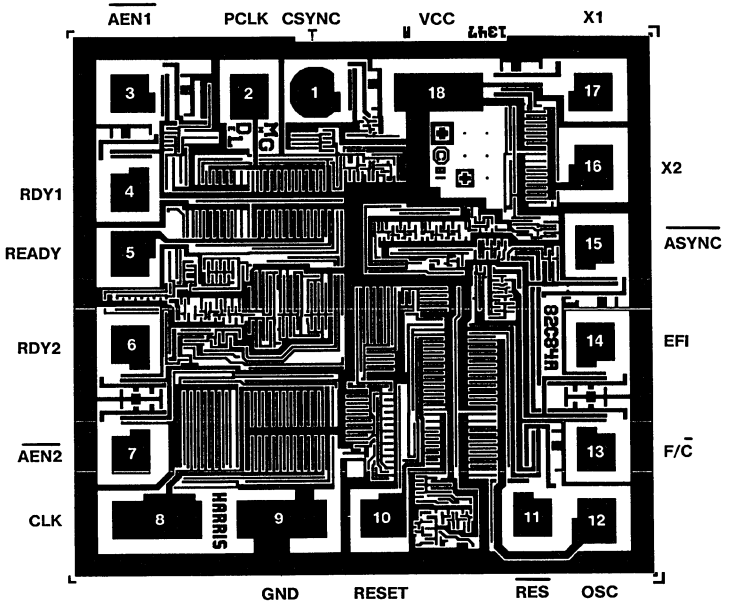
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy (LCC has Gold Preform)
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.42 x 10^5 A/cm^2

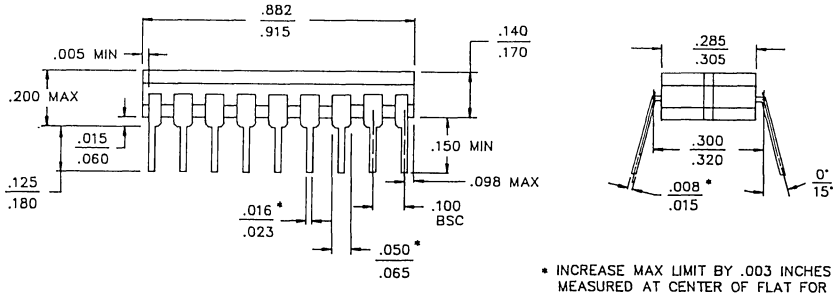
Metallization Mask Layout

82C84A/883



Packaging†

18 PIN CERAMIC DIP

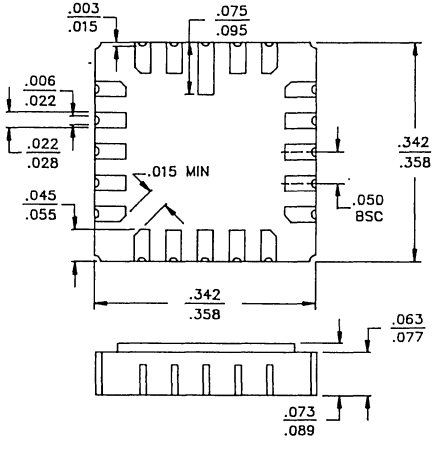


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-6

20 PAD CERAMIC LCC
BOTTOM VIEW



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Functional Description

Oscillator

The oscillator circuit of the 82C84A is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

TABLE A. CRYSTAL SPECIFICATIONS

PARAMETER	TYPICAL CRYSTAL SPEC
Frequency	2.4 - 25MHz, Fundamental, "AT" cut
Type of Operation	Parallel
Unwanted Modes	-6dB (Minimum)
Load Capacitance	18 - 32pF

See Harris Publication TB-47 for recommended crystal specifications

Capacitors C1, C2 are chosen such that their combined capacitance

$$CT = \frac{C1 \times C2}{C1 + C2} \text{ (Including stray capacitance)}$$

matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another 82C84A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 82C84A. This is accomplished with two flip-flops. (See Figure 1). The counter output is a 33% duty cycle clock at one-third the input frequency.

* The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷ 3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

Clock Outuds

The CLK output is a 33% duty cycle clock driver designed to drive the 80C86, 80C88 processors directly. PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. the reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 82C84A.

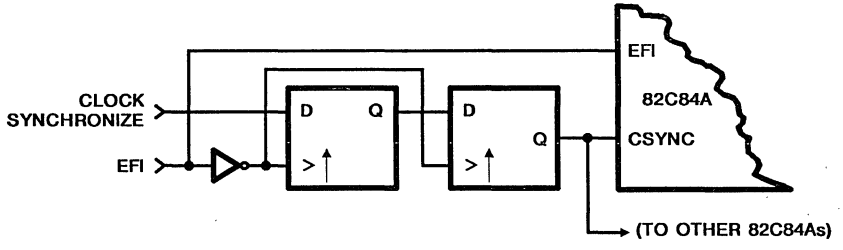


FIGURE 1. CSYNC SYNCHRONIZATION

* NOTE: If EFI input is used, then cyrstal input X1 must be tied to VCC or GND and X2 should be left open. If the cyrstal inputs are used, then EFI should be tied to VCC or GND.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

READY Synchronization

Two READY input (RDY1, RDY2) are provided to accommodate two system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one a the rising edge of CLK (requiring a setup time tR1VCH) and the synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, tR1VCL, on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

HARRIS

82C85/883

June 1989

CMOS Static Clock Controller/Generator

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Generates the System Clock For CMOS or NMOS Microprocessors and Peripherals
- Complete Control Over System Operation for Very Low System Power
  - Stop-Oscillator
  - Low Frequency
  - Stop-Clock
  - Full Speed Operation
- DC to 25MHz Operation (DC to 8MHz System Clock)
- Generates 50% and 33% Duty Cycle Clocks (Synchronized)
- Uses a Parallel Mode Crystal Circuit or External Frequency Source
- TTL Compatible Inputs/Outputs
- 24 Pin Slimline Dual-In-Line or 28 Pad Square LCC Package Options
- Single 5V Power Supply
- Military Operating Temperature Range ..... -55°C to +125°C

Description

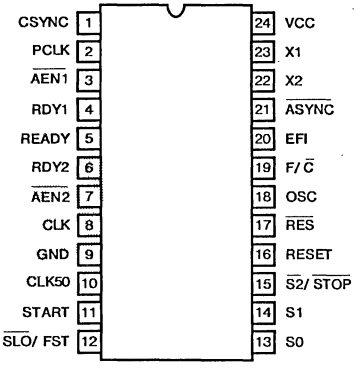
The Harris 82C85/883 Static CMOS Clock Controller/Generator provides complete control of static CMOS system operating modes and supports full speed, slow, stop-clock and stop-oscillator operation. While directly compatible with the Harris 80C86 and 80C88 16-bit Static CMOS Microprocessor Family, the 82C85/883 can also be used for general system clock control.

For static system designs, separate signals are provided on the 82C85/883 for stop (S0, S1 , $\overline{S2}$/$\overline{STOP}$) and start (START) control of the crystal oscillator and system clocks. A single control line ($\overline{SLO}$/FST) determines 82C85 fast (crystal/EFI frequency divided by 3) or slow (crystal/EFI frequency divided by 768) mode operation. Automatic maximum mode 80C86 and 80C88 software HALT instruction decode logic in the 82C85/883 enables software-based clock control. Restart logic insures valid clock start-up and complete synchronization of system clocks.

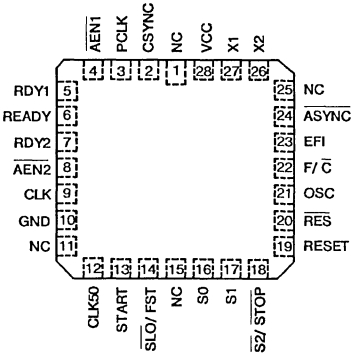
The 82C85/883 is manufactured using the Harris advanced Scaled SAJI IV CMOS process. In addition to clock control circuitry, the 82C85/883 also contains a crystal controlled oscillator (up to 25MHz), clock generation logic, complete "Ready" synchronization and reset logic. This permits the designer to tailor the system power-performance product to provide optimum performance at low power levels.

Pinouts

82C85/883 (CERAMIC DIP)
TOP VIEW



82C85/883 (CERAMIC LCC)
TOP VIEW



HARRIS

82C86H/883

June 1989

CMOS Octal Bus Transceiver

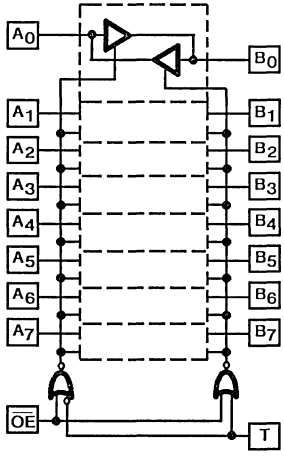
Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Full Eight Bit Bi-directional Bus Interface
- Industry Standard 8286 Compatible Pinout
- High Drive Capability:
  - B Side IOL 20mA
  - A Side IOL 12mA
- Three-State Outputs
- Propagation Delay ..... 35ns Max.
- Gated Inputs:
  - Reduce Operating Power
  - Eliminate the Need for Pull-Up Resistors
- Single 5V Power Supply
- Low Power Operation - ICCSB = 10μA
- Military Operating Temperature Range ..... -55°C to +125°C

Description

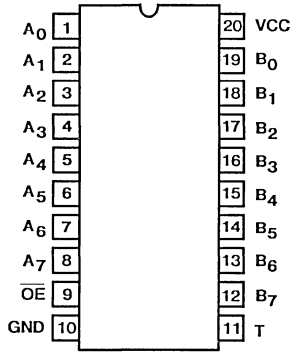
The Harris 82C86H/883 is a high performance CMOS Octal Transceiver manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C86H/883 provides a full eight-bit bi-directional bus interface in a 20 pin package. The Transmit (T) control determines the data direction. The active low output enable ($\overline{OE}$) permits simple interface to the 80C86, 80C88 and other microprocessors. The 82C86H/883 has gated inputs, eliminating the need for pull-up/pull-down resistors and reducing overall system operating power dissipation.

Functional Diagram

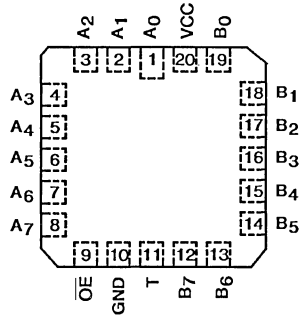


Pinouts

82C86H/883 (CERAMIC DIP)
TOP VIEW



82C86H/883 (CERAMIC LCC)
TOP VIEW



TRUTH TABLE

T	$\overline{OE}$	A	B
X	H	Hi-Z	Hi-Z
H	L	I	O
L	L	O	I

H = Logic One
L = Logic Zero
I = Input Mode
O = Output Mode
X = Don't Care
Hi-Z = High Impedance

PIN NAMES

PIN	DESCRIPTION
A0-A7	Local Bus Data I/O Pins
B0-B7	System Bus Data I/O Pins
T	Transmit Control Input
$\overline{OE}$	Active Low Output Enable

5 CMOS PERIPHERALS

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	70°C/W	15°C/W
Ceramic LCC Package	76°C/W	19°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 720mW
Ceramic LCC Package 664mW
Gate Count ..... 265 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... +4.5V to +5.5V

TABLE 1. 82C86H-5/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	VIH	VCC = 5.5V, (Note 1)	1, 2, 3	$-55°C \le T_A \le +125°C$	2.2	-	V
Logical Zero Input Voltage	VIL	VCC = 4.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.8	V
Output High Voltage	VOH	VCC = 4.5V, $\overline{OE}$ = GND	1, 2, 3	$-55°C \le T_A \le +125°C$			
B Outputs		IOH = -8.0mA			3.0	-	V
A Outputs		IOH = -4.0mA			3.0	-	V
A and B Outputs		IOH = -100µA (Note 2)			VCC-0.4	-	V
Output Low Voltage	VOL	VCC = 4.5V, $\overline{OE}$ = GND	1, 2, 3	$-55°C \le T_A \le +125°C$			
B Outputs		IOL = +20.0mA			-	0.45	V
A Outputs		IOL = +12.0mA (Note 2)			-	0.45	V
Input Leakage Current	II	VCC = 5.5V, Pins 9, 11 VIN = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-10.0	+10.0	µA
Output Leakage Current	IO	VCC = 5.5V, $\overline{OE} \ge$ VCC -0.5V VOUT = GND or VCC, Pins 1-8, 12-19	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	µA
Standby Power Supply Current	ICCSB	VCC = 5.5V, Outputs Open, VIN = VCC or GND	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	µA

NOTES: 1. VIH is measured by applying a pulse of magnitude = VIHmin to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins ($\overline{T}$, $\overline{OE}$) are tested separately with all device data inputs at VCC-0.4V.

2. Interchanging of force and sense conditions is permitted.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. 82C86H-5/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay, Input to Output	TIVOV(1)	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	35	ns
Output Enable Time	TELOV(5)	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	65	ns

NOTES: 1. AC parameter tested as per test circuits and definitions in Timing Waveforms. Input rise and fall times are driven at 1ns/V.

2. Tested as follows: f = 1MHz, VIH = 2.6V, VIH for T (Transmit pin) $\geq$ VCC - 0.5V, VIL = 0.4V, CL = 50pF (unless otherwise specified), VOH $\geq$ 1.5V, VOL $\leq$ 1.5V.

TABLE 3. 82C86H-5/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance B Inputs	CIN	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1, 5	$T_A = +25^oC$	-	18	pF
			1, 6		-	15	pF
A Inputs			1, 5		-	14	pF
			1, 6		-	10	pF
Input Capacitance All Other Inputs	CIN	VCC = OPEN, f = 1MHz, All Measurements Reference to Device GND	1, 5	$T_A = +25^oC$	-	13	pF
			1, 6	$T_A = +25^oC$	-	7	pF
Propagation Delay, Input to Output	TIVOV(1)	VCC = 4.5 and 5.5V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Transmit/Receive Hold Time	TEHTV(2)	VCC = 4.5 and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Transmit/Receive Hold Time	TTVEL(3)	VCC = 4.5 and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Output Disable Time	TEHOZ(4)	VCC = 4.5 and 5.5V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	5	35	ns
Input Rise/Fall Time	TR,TF(6)	VCC = 4.5 and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	20	ns
Minimum Output Enable High Time	TEHEL(7)	VCC = 4.5 and 5.5V	4	$-55^oC \leq T_A \leq +125^oC$	35	-	ns
Output Enable Time	TELOV(5)	VCC = 4.5 and 5.5V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	5	-	ns

NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. AC parameter tested as per test circuits and definitions in Timing Waveforms. Input rise and fall times are driven at 1ns/V.

3. Tested as follows: f = 1MHz, VIH = 2.6V, VIH for T (Transmit pin) $\geq$ VCC - 0.5V, VIL = 0.4V, CL = 50pF (unless otherwise specified), VOH $\geq$ 1.5V, VOL $\leq$ 1.5V.

4. A system limitation only when changing direction. Not a measured parameter.

5. For Ceramic DIP package.

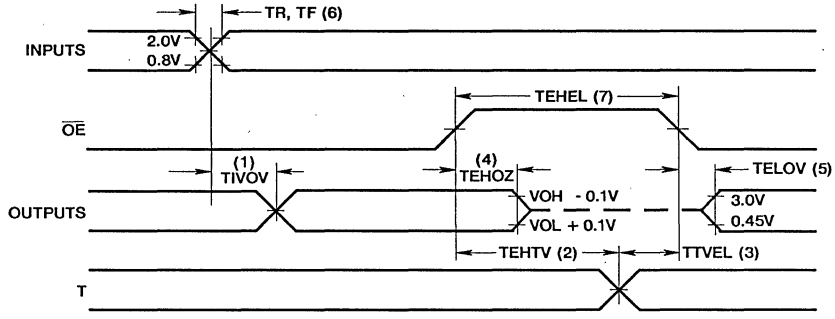
6. For Ceramic LCC package.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

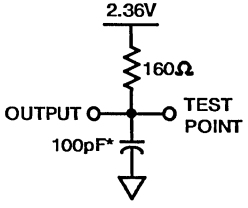
Timing Waveform



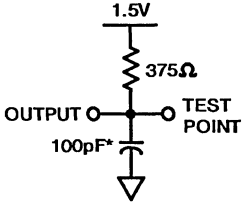
All timing measurments are made at 1.5V unless otherwise noted

Test Load Circuits

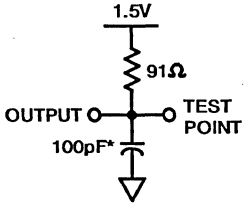
A SIDE OUTPUTS



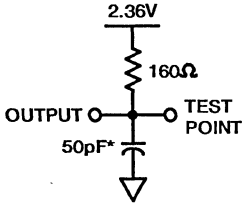
TIVOV
LOAD CIRCUIT



TELOV
OUTPUT HIGH ENABLE
LOAD CIRCUIT

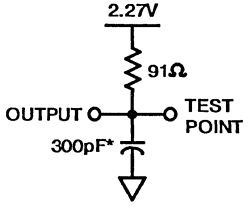


TELOV
OUTPUT LOW ENABLE
LOAD CIRCUIT

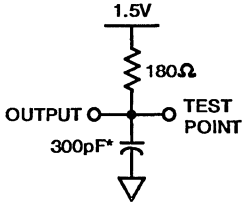


TEHOZ
OUTPUT LOW/HIGH DISABLE
LOAD CIRCUIT

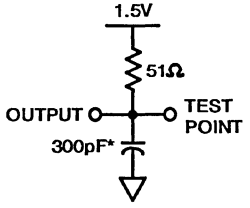
B SIDE OUTPUTS



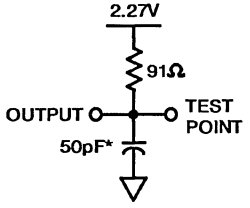
TIVOV
LOAD CIRCUIT



TELOV
OUTPUT HIGH ENABLE
LOAD CIRCUIT



TELOV
OUTPUT LOW ENABLE
LOAD CIRCUIT

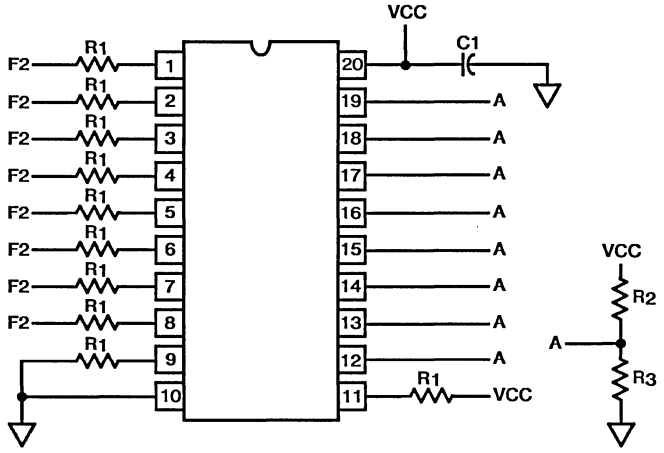


TEHOZ
OUTPUT LOW/HIGH DISABLE
LOAD CIRCUIT

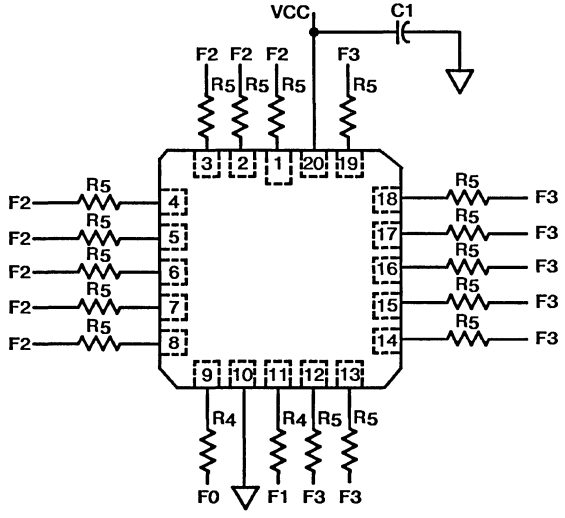
* Includes jig and stray capacitance

Burn-In Circuits

82C86H/883 CERAMIC DIP



82C86H/883 CERAMIC LCC



NOTES:
VCC = 5.5V ± 0.5V GND = 0V
VIH = 4.5V ± 10%
VIL = -0.2 to 0.4V
R1 = 47kΩ ± 5%
R2 = 2.4kΩ ± 5%
R3 = 1.5kΩ ± 5%
R4 = 1kΩ ± 5%
R5 = 5kΩ ± 5%
C1 = 0.01μF minimum
F0 = 100kHz ± 10%
F1 = F0/2, F2 = F1/2, F3 = F2/2

Metallization Topology

DIE DIMENSIONS:
138.6 x 155.5 x 19 ± 1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 1kÅ

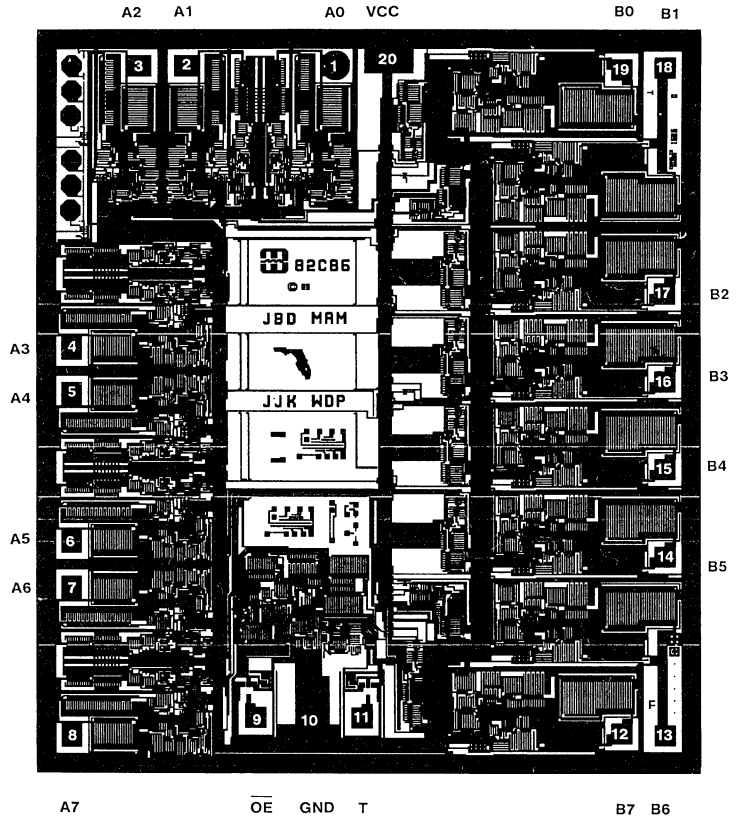
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy (LCC has Gold Preform)
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.47 x 10^5 A/cm^2

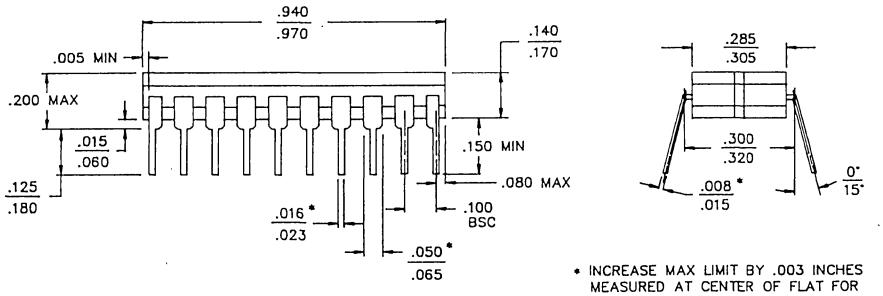
Metallization Mask Layout

82C86H/883



Packaging†

20 PIN CERAMIC DIP

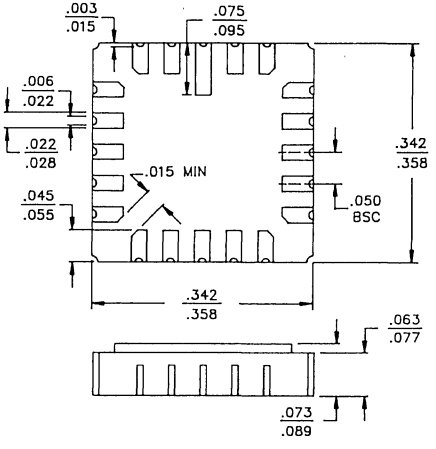


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-8

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Gated Inputs

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between VCC and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create an indeterminate logic state at the inputs and cause a disruption in device operation.

The Harris 82C8X series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled ($\overline{OE}$ = logic one for the 82C86H/87H). These gated inputs disconnect the input circuitry from the VCC and ground power supply pins by turning off the upper P-channel and lower N-channel (See Figures 1 and 2). No current flow from VCC to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

D.C. input voltage levels can also cause an increase in ICC if these input levels approach the minimum VIH or maximum VIL conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode (STB = logic one). ICC remains below the maximum ICC standby specification of 10μA during the time inputs are disabled, thereby greatly reducing the average power dissipation of the 82C8X series devices.

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C86H/87H data sheet is determined by

$$I = CL\ (dv/dt)$$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = CL\ \frac{(VCC \times 80\%)}{tR/tF}$$

where tR = 20ns, VCC = 5.0V, CL = 300pF on each eight outputs.

$$I = (8 \times 300 \times 10^{-12}) \times (5.0V \times 0.8)/(20 \times 10^{-9})$$
$$= 480mA$$

This current spike may cause a large negative voltage spike on VCC which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1μF ceramic disc capacitor be placed between VCC and GND at each device, with placement being as near to the device as possible.

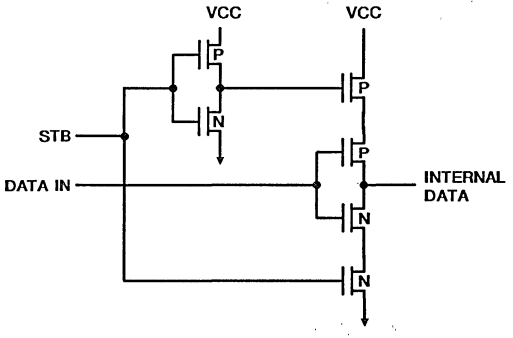


FIGURE 1. 82C82/83H

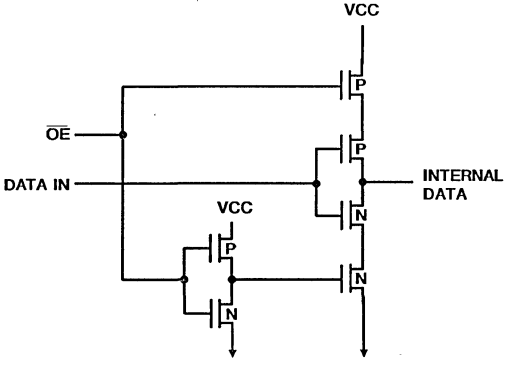


FIGURE 2. 82C86H/87H GATED INPUTS

HARRIS

82C87H/883

CMOS Octal Inverting Bus Transceiver

June 1989

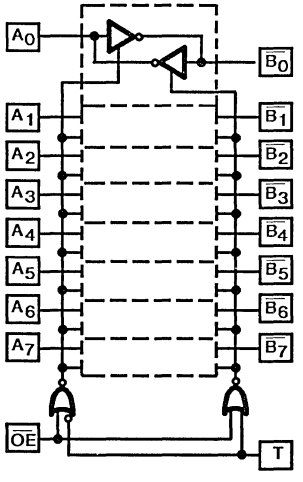
Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Full Eight Bit Bi-directional Bus Interface
- Industry Standard 8287 Compatible Pinout
- High Drive Capability:
  - B Side IOL 20mA
  - A Side IOL 12mA
- Three-State Inverting Outputs
- Propagation Delay ..... 35ns Max.
- Gated Inputs:
  - Reduce Operating Power
  - Eliminate the Need for Pull-Up Resistors
- Single 5V Power Supply
- Low Power Operation - ICCSB = 10μA
- Military Operating Temperature Range ..... -55°C to +125°C

Description

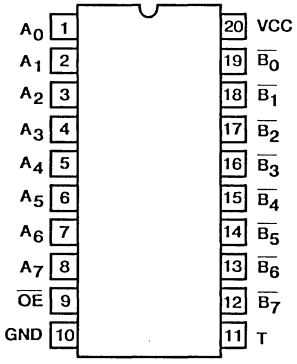
The Harris 82C87H/883 is a high performance CMOS Octal Transceiver manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C87H/883 provides a full eight-bit bi-directional bus interface in a 20 pin package. The Transmit (T) control determines the data direction. The active low output enable ($\overline{OE}$) permits simple interface to the 80C86, 80C88 and other microprocessors. The 82C87H/883 has gated inputs, eliminating the need for pull-up/pull-down resistors and reducing overall system operating power dissipation. The 82C87H/883 provides inverted data at the outputs.

Functional Diagram

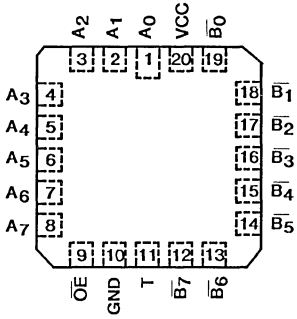


Pinouts

82C87H/883 (CERAMIC DIP)
TOP VIEW



82C87H/883 (CERAMIC LCC)
TOP VIEW



TRUTH TABLE

T	$\overline{OE}$	A	B
X	H	Hi-Z	Hi-Z
H	L	I	O
L	L	O	I

H = Logic One O = Output Mode
L = Logic Zero X = Don't Care
I = Input Mode Hi-Z = High Impedance

PIN NAMES

PIN	DESCRIPTION
A0-A7	Local Bus Data I/O Pins
$\overline{B0}$-$\overline{B7}$	System Bus Data I/O Pins
T	Transmit Control Input
$\overline{OE}$	Active Low Output Enable

5 CMOS PERIPHERALS

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	70°C/W	15°C/W
Ceramic LCC Package	76°C/W	19°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 720mW
Ceramic LCC Package 664mW
Gate Count ..... 265 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... +4.5V to +5.5V

TABLE 1. 82C87H-5/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	VIH	VCC = 5.5V, (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.2	-	V
Logical Zero Input Voltage	VIL	VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.8	V
Output High Voltage	VOH	VCC = 4.5V, $\overline{OE}$ = GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$			
B Outputs		IOH = -8.0mA			3.0	-	V
A Outputs		IOH = -4.0mA			3.0	-	V
A and B Outputs		IOH = -100µA (Note 2)			VCC-0.4	-	V
Output Low Voltage	VOL	VCC = 4.5V, $\overline{OE}$ = GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$			
B Outputs		IOL = +20.0mA			-	0.45	V
A Outputs		IOL = +12.0mA (Note 2)			-	0.45	V
Input Leakage Current	II	VCC = 5.5V, Pins 9, 11 VIN = GND or VCC	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-10.0	+10.0	µA
Output Leakage Current	IO	VCC = 5.5V, $\overline{OE} \geq$ VCC -0.5V, VOUT = GND or VCC, Pins 1-8, 12-19	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA
Standby Power Supply Current	ICCSB	VCC = 5.5V, Outputs Open, VIN = VCC or GND	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	10	µA

NOTES: 1. VIH is measured by applying a pulse of magnitude = VIHmin to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins ($\overline{T}$, $\overline{OE}$) are tested separately with all device data inputs at VCC-0.4V.

2. Interchanging of force and sense conditions is permitted.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. 82C87H-5/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay, Input to Output	TIVOV(1)	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	35	ns
Output Enable Time	TELOV(5)	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	65	ns

NOTES: 1. AC parameter tested as per test circuits and definitions in Timing Waveforms. Input rise and fall times are driven at 1ns/V.

2. Tested as follows: f = 1MHz, VIH = 2.6V, VIH for T (Transmit pin) $\geq$ VCC - 0.5V, VIL = 0.4V, CL = 50pF (unless otherwise specified), VOH $\geq$ 1.5V, VOL $\leq$ 1.5V.

TABLE 3. 82C87H-5/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance B Inputs	CIN	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1, 5	$T_A = +25^oC$	-	18	pF
			1, 6		-	15	pF
A Inputs			1, 5		-	14	pF
			1, 6		-	10	pF
Input Capacitance All Other Inputs	CIN	VCC = OPEN, f = 1MHz, All Measurements Reference to Device GND	1, 5	$T_A = +25^oC$	-	13	pF
			1, 6	$T_A = +25^oC$	-	7	pF
Propagation Delay, Input to Output	TIVOV(1)	VCC = 4.5 and 5.5V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Transmit/Receive Hold Time	TEHTV(2)	VCC = 4.5 and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Transmit/Receive Hold Time	TTVEL(3)	VCC = 4.5 and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Output Disable Time	TEHOZ(4)	VCC = 4.5 and 5.5V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	5	35	ns
Output Enable Time	TELOV(5)	VCC = 4.5 and 5.5V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Input Rise/Fall Time	TR,TF(6)	VCC = 4.5 and 5.5V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	20	ns
Minimum Output Enable High Time	TEHEL(7)	VCC = 4.5 and 5.5V	4	$-55^oC \leq T_A \leq +125^oC$	35	-	ns

NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. AC parameter tested as per test circuits and definitions in Timing Waveforms. Input rise and fall times are driven at 1ns/V.

3. Tested as follows: f = 1MHz, VIH = 2.6V, VIH for T (Transmit pin) $\geq$ VCC - 0.5V, VIL = 0.4V, CL = 50pF (unless otherwise specified), VOH $\geq$ 1.5V, VOL $\leq$ 1.5V.

4. A system limitation only when changing direction. Not a measured parameter.

5. For Ceramic DIP package.

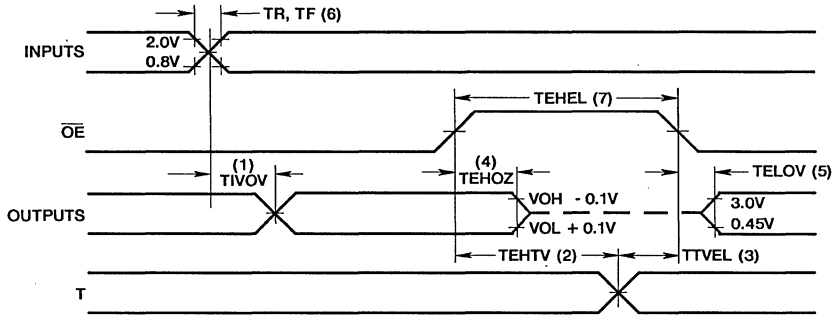
6. For Ceramic LCC package.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

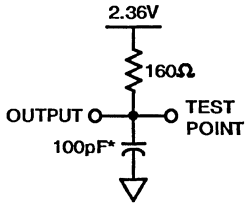
Timing Waveform



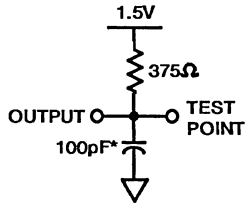
All timing measurments are made at 1.5V unless otherwise noted

Test Load Circuits

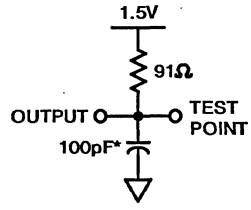
A SIDE OUTPUTS



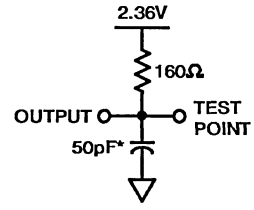
TIVOV
LOAD CIRCUIT



TELOV
OUTPUT HIGH ENABLE
LOAD CIRCUIT

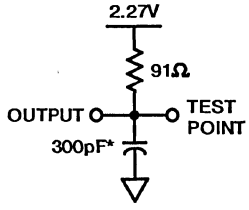


TELOV
OUTPUT LOW ENABLE
LOAD CIRCUIT

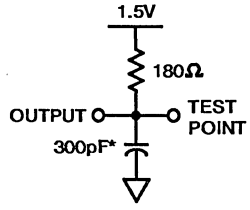


TEHOZ
OUTPUT LOW/HIGH DISABLE
LOAD CIRCUIT

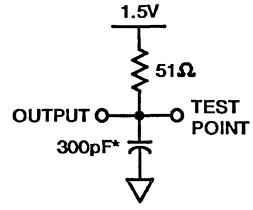
B SIDE OUTPUTS



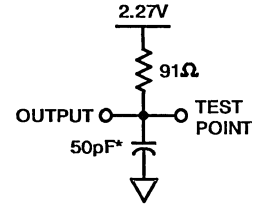
TIVOV
LOAD CIRCUIT



TELOV
OUTPUT HIGH ENABLE
LOAD CIRCUIT



TELOV
OUTPUT LOW ENABLE
LOAD CIRCUIT

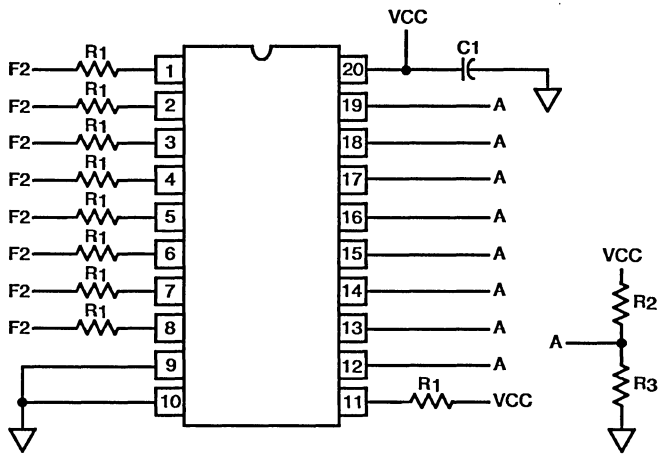


TEHOZ
OUTPUT LOW/HIGH DISABLE
LOAD CIRCUIT

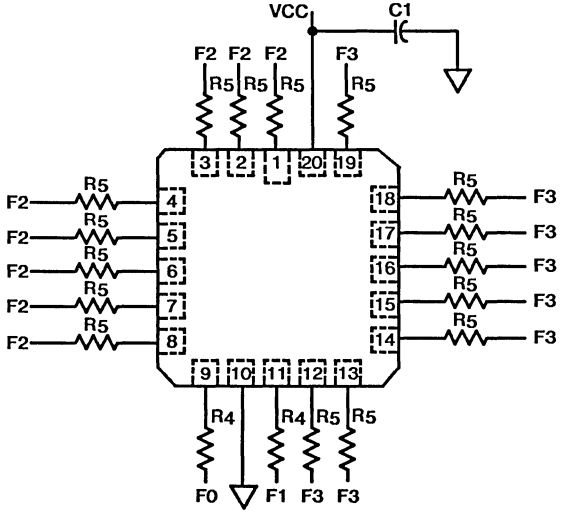
* Includes jig and stray capacitance

Burn-In Circuits

82C87H/883 CERAMIC DIP



82C87H/883 CERAMIC LCC



NOTES:
VCC = 5.5V ± 0.5V, GND = 0V
VIH = 4.5V ± 10%
VIL = -0.2 to 0.4V
R1 = 47kΩ ± 5%
R2 = 2.4kΩ ± 5%
R3 = 1.5kΩ ± 5%
R4 = 1kΩ ± 5%
R5 = 5kΩ ± 5%
C1 = 0.01μF minimum
F0 = 100kHz ± 10%
F1 = F0/2, F2 = F1/2, F3 = F2/2

Metallization Topology

DIE DIMENSIONS:
138.6 x 155.5 x 19 ± 1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 2kÅ

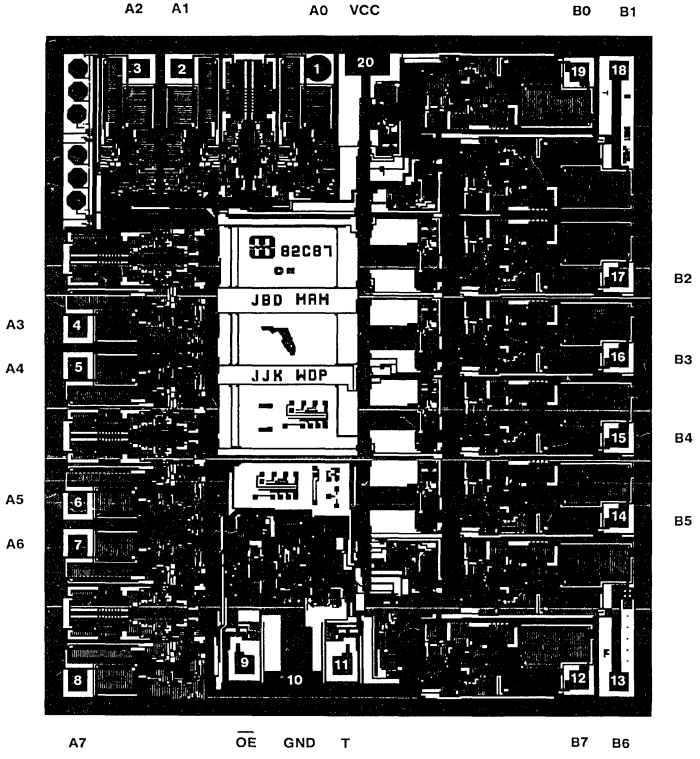
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy (LCC has Gold Preform)
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.47 x 10^5 A/cm^2

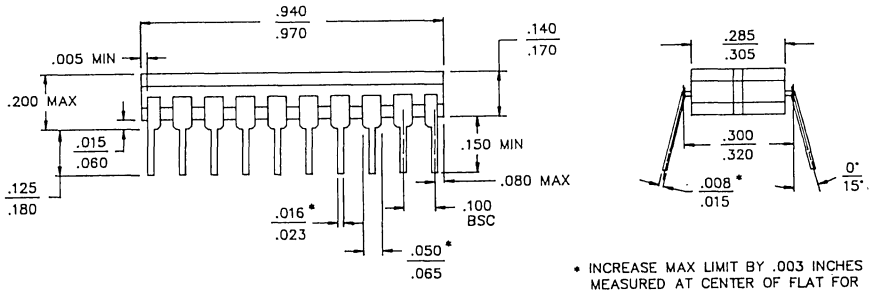
Metallization Mask Layout

82C87H/883



Packaging†

20 PIN CERAMIC DIP

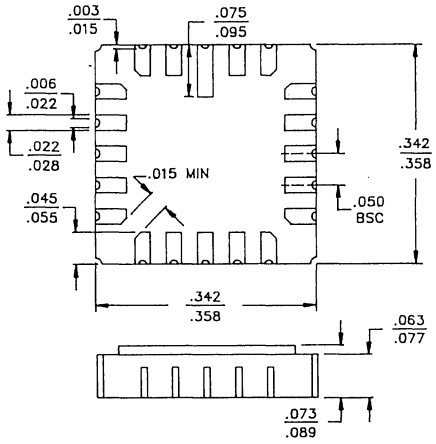


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-8

20 PAD CERAMIC LCC
BOTTOM VIEW



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Gated Inputs

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between VCC and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create an indeterminate logic state at the inputs and cause a disruption in device operation.

The Harris 82C8X series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled ($\overline{OE}$ = logic one for the 82C86H/87H). These gated inputs disconnect the input circuitry from the VCC and ground power supply pins by turning off the upper P-channel and lower N-channel (See Figures 1 and 2). No current flow from VCC to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

D.C. input voltage levels can also cause an increase in ICC if these input levels approach the minimum VIH or maximum VIL conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode (STB = logic one). ICC remains below the maximum ICC standby specification of 10μA during the time inputs are disabled, thereby greatly reducing the average power dissipation of the 82C8X series devices.

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C86H/87H data sheet is determined by

$$I = CL\ (dv/dt)$$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = CL \frac{(VCC \times 80\%)}{tR/tF}$$

where tR = 20ns, VCC = 5.0V, CL = 300pF on each eight outputs.

$$I = (8 \times 300 \times 10^{-12}) \times (5.0V \times 0.8)/(20 \times 10^{-9})$$
$$= 480mA$$

This current spike may cause a large negative voltage spike on VCC which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1μF ceramic disc capacitor be placed between VCC and GND at each device, with placement being as near to the device as possible.

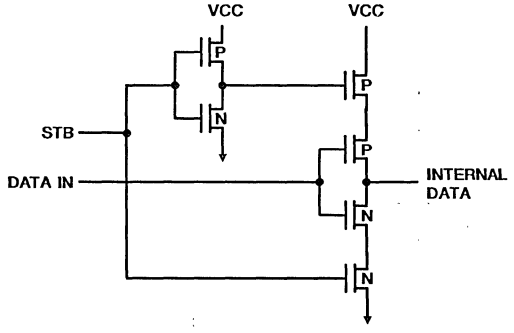


FIGURE 1. 82C82/83H

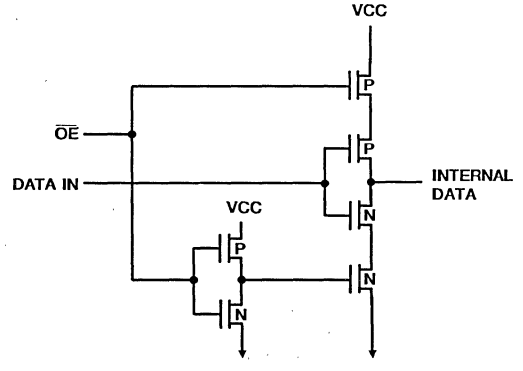


FIGURE 2. 82C86H/87H GATED INPUTS

HARRIS

82C88/883

June 1989

CMOS Bus Controller

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Compatible with Bipolar 8288
- Performance Compatible with: 80C86/80C88 .....(5/8MHz)
  80186/80188 .....(6/8MHz)
  8086/8088 .....(5/8MHz)
  8089
- Provides Advanced Commands for Multi-Master Busses
- Three-State Command Outputs
- Bipolar Drive Capability
- Scaled SAJI IV CMOS Process
- Single 5V Power Supply
- Low Power Operation
  - ICCSB ..... 10μA (Max)
  - ICCOP ..... 1mA/MHz (Max)
- Military Operating Temperature Range ..... -55°C to +125°C

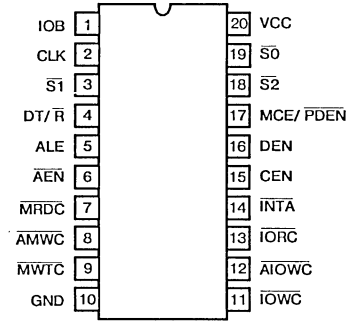
Description

The Harris 82C88/883 is a high performance CMOS Bus Controller manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C88/883 provides the control and command timing signals for 80C86, 80C88, 8086, 8088, 8089, 80186, and 80188 based systems. The high output drive capability of the 82C88/883 eliminates the need for additional bus drivers.

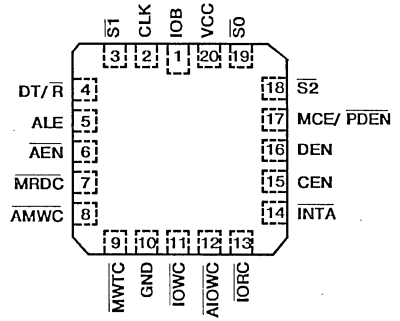
Static CMOS circuit design insures low operating power. The Harris advanced SAJI process results in performance equal to or greater than existing equivalent products at a significant power savings.

Pinouts

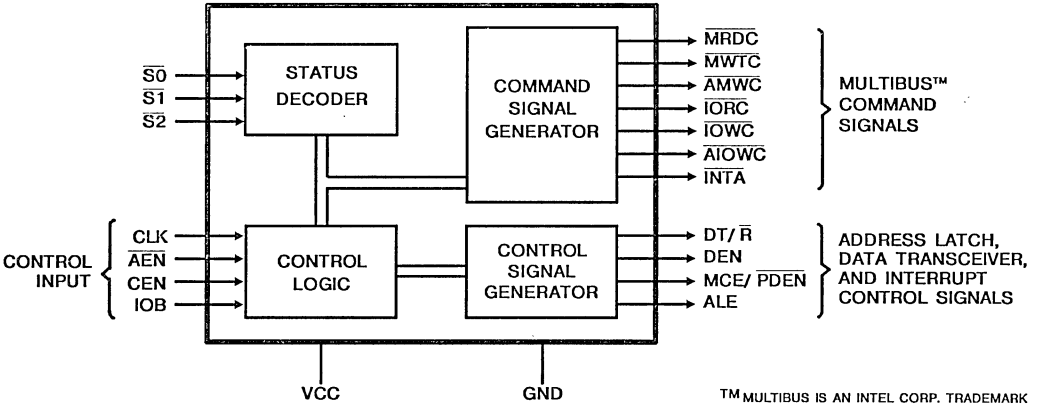
82C88/883 (CERAMIC DIP)
TOP VIEW



82C88/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



TM MULTIBUS IS AN INTEL CORP. TRADEMARK

Pin Description

PIN SYMBOL	NUMBER	TYPE	DESCRIPTION
VCC	20		VCC: The +5V power supply pin. A 0.1μF capacitor between pins 10 and 20 is recommended for decoupling.
GND	10		GROUND.
$\overline{S0}$, $\overline{S1}$ $\overline{S2}$	19, 3 18	I	STATUS INPUT PINS: These pins are the input pins from the 80C86, 80C88, 8086/88, 8089 processors. The 82C88/883 decodes these inputs to generate command and control signals at the appropriate time. When Status pins are not in use (passive), command outputs are held HIGH (See Table A in Design Information Section)
CLK	2	I	CLOCK: This is a CMOS compatible input which receives a clock signal from the 82C84A or 82C85 clock generator and serves to establish when command/control signals are generated.
ALE	5	O	ADDRESS LATCH ENABLE: This signal serves to strobe an address into the address latches. This signal is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches, such as the 82C82 and 82C83H.
DEN	16	O	DATA ENABLE: This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.
DT/$\overline{R}$	4	O	DATA TRANSMIT/RECEIVE: This signal establishes the direction of data flow through the transceivers. A HIGH on this line indicates Transmit (write to I/O or memory) and a LOW indicates Receive (read from I/O or memory).
$\overline{AEN}$	6	I	ADDRESS ENABLE: $\overline{AEN}$ enables command outputs of the 82C88/883 Bus Controller a minimum of 110ns (250ns maximum) after it becomes active (LOW). $\overline{AEN}$ going inactive immediately three-states the command output drivers. $\overline{AEN}$ does not affect the I/O command lines if the 82C88/883 is in the I/O Bus mode (IOB tied HIGH).
CEN	15	I	COMMAND ENABLE: When this signal is LOW all 82C88/883 command outputs and the DEN and $\overline{PDEN}$ control outputs are forced to their Inactive state. When this signal is HIGH, these same outputs are enabled.
IOB	1	I	INPUT/OUTPUT BUS MODE: When the IOB pin is strapped HIGH, the 82C88/883 functions in the I/O Bus mode. When it is strapped LOW, the 82C88/883 functions in the System Bus mode (See I/O Bus and System Bus sections).
$\overline{AIOWC}$	12	O	ADVANCED I/O WRITE COMMAND: The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AIOWC}$ is active LOW.
$\overline{IOWC}$	11	O	I/O WRITE COMMAND: This command line instructs an I/O device to read the data on the data bus. The signal is active LOW.
$\overline{IORC}$	13	O	I/O READ COMMAND: This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.
$\overline{AMWC}$	8	O	ADVANCED MEMORY WRITE COMMAND: The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AMWC}$ is active LOW.
$\overline{MWTC}$	9	O	MEMORY WRITE COMMAND: This command line instructs the memory to record the data present on the data bus. This signal is active LOW.
$\overline{MRDC}$	7	O	MEMORY READ COMMAND: This command line instructs the memory to drive its data onto the data bus. $\overline{MRDC}$ is active LOW.
$\overline{INTA}$	14	O	INTERRUPT ACKNOWLEDGE: This command line tells an interrupting device that its interrupt has been acknowledged and that it should drive vectoring information onto the data bus. This signal is active LOW.
MCE/$\overline{PDEN}$	17	O	This is a dual function pin. MCE (IOB IS TIED LOW) Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master 82C59A Priority Interrupt Controller onto the data bus. The MCE signal is active HIGH. $\overline{PDEN}$ (IOB IS TIED HIGH): Peripheral Data Enable enables the data bus transceiver for the IsO bus that DEN performs for the system bus. $\overline{PDEN}$ is active LOW.

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	77.8°C/W	18.9°C/W
Ceramic LCC Package	76.0°C/W	19.0°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 646mW
Ceramic LCC Package 664mW
Gate Count ..... 100 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... +4.5V to +5.5V

TABLE 1. 82C88/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical "1" Input Voltage	VIH	VCC = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	2.2	-	V
Logical "0" Input Voltage	VIL		1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.8	V
CLK Logical "1" Input Voltage	VIHC	VCC = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	VCC-0.8	-	V
CLK Logical "0" Input Voltage	VILC		1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.8	V
Output HIGH Voltage, Command Outputs	VOH1	IOH = -8.0mA, Note 2 IOH = -2.5mA, Note 2	1, 2, 3	$-55°C \le T_A \le +125°C$	3.0 VCC-0.4	- -	V V
Output HIGH Voltage, Control Outputs	VOH2	IOH = -4.0mA, Note 2 IOH = -2.5mA, Note 2	1, 2, 3	$-55°C \le T_A \le +125°C$	3.0 VCC-0.4	- -	V V
Output LOW Voltage, Command Outputs	VOL1	IOL = +12.0mA, Note 2	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.5	V
Output LOW Voltage, Control Outputs	VOL2	IOL = +8.0mA, Note 2	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Input Leakage Current	II	VCC = 5.5V, VIN = GND or VCC, All Inputs Except $\overline{S0}$, $\overline{S1}$, $\overline{S2}$	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Input Current Bus Hold High	IBHH	VIN = 2.0V, Note 3 VCC = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-50	-300	µA
Output Leakage Current	IO	VCC = 5.5V, VOUT = GND or VCC, IOB = GND, $\overline{AEN}$ = VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-10	+10	µA
Standby Power Supply Current	ICCSB	VCC = 5.5V, VIN = GND or VCC, Outputs Open	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	µA
Operating Power Supply Current	ICCOP	VCC = 5.5V, Note 4	1, 2, 3	$-55°C \le T_A \le +125°C$	-	1	mA/MHz

NOTES: 1. VCC = 4.5V unless otherwise specified. All voltage referenced to device GND.
2. Interchanging of force and sense conditions is permitted.
3. IBHH should be measured after raising VIN on $\overline{S0}$, $\overline{S1}$, $\overline{S2}$ to VCC and then lowering to valid input high level of 2.0V.
4. Frequency = 10MHz, outputs open, VIN = VCC or GND.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. 82C88/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CLK Cycle Time	(1)TCLCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	125	-	ns
CLK Low Time	(2)TCLCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	55	-	ns
CLK High Time	(3)TCHCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Status Active Setup Time	(4)TSVCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	35	-	ns
Status Inactive Hold Time	(5)TCHSV		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Status Inactive Setup Time	(6)TSHCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	35	-	ns
Status Active Hold Time	(7)TCLSH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Control Active Delay	(8)TCVNV	Test Cond. 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	45	ns
Control Inactive Delay	(9)TCVNX	Test Cond. 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	45	ns
ALE Active Delay (from CLK)	(10)TCLLH	Test Cond. 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	20	ns
MCE Active Delay (from CLK)	(11)TCLMCH	Test Cond. 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	25	ns
ALE Active Delay (from Status)	(12)TSVLH	Test Cond. 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	20	ns
MCE Active Delay (from Status)	(13)TSVMCH	Test Cond. 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	30	ns
ALE Inactive Delay	(14)TCHLL	Test Cond. 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	4	18	ns
Command Active Delay	(15)TCLML	Test Cond. 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	35	ns
Command Inactive Delay	(16)TCLMH	Test Cond. 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	35	ns
Direction Control Active Delay	(17)TCHDTL	Test Cond. 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Direction Control Inactive Delay	(18)TCHDTH	Test Cond. 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	30	ns
Command Enable Time	(19)TAELCH	Test Cond. 3, Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
Enable Delay Time	(21)TAELCV	Test Cond. 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	110	250	ns
$\overline{\text{AEN}}$ to DEN	(22)TAEVNV	Test Cond. 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	25	ns
CEN to DEN, $\overline{\text{PDEN}}$	(23)TCEVNV	Test Cond. 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	25	ns
CEN to Command	(24)TCELRH	Test Cond. 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	TCLML +10	ns
ALE High Time	(25)TLHLL	Test Cond. 1, Note 4	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TCLCH -10	-	ns

NOTES: 1. VCC = 4.5V and 5.5V unless otherwise specified. Tested as follows: f = 400kHz unless otherwise specified, VIH = 2.6V, VIL = 0.4V, CL = 50pF, VOH $\geq$ 1.5V, VOL $\leq$ 1.5V, VIHC = VCC - 0.4V, VILC = 0.4V.

2. "Test Cond. X" refers to TEST CONDITION DEFINITION TABLE with A.C. Test Circuit.
3. TAELCH measurement is between 1.5V and 2.5V.
4. Parameter referenced to 80C86 or 80C88 only.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. 82C88/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

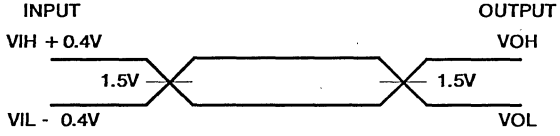
PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	f = 1MHz, all measurements are reference to device GND	1, 2 1, 3	$T_A = +25^oC$	- -	10 5	pF pF
Output Capacitance	COUT		1, 2 1, 3	$T_A = +25^oC$	- -	17 12	pF pF
Command Disable Time	(20)TAEHCZ	VCC = 4.5V and 5.5V	1, 4, 5	$-55^oC \leq T_A \leq +125^oC$	-	40	ns

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Ceramic DIP package.
3. Ceramic LCC package.
4. TAEHCZ measured at 0.5V change in VOUT.
5. Reference Test Condition 4 of TEST CONDITION DEFINITION TABLE with A.C. Test Circuit.

TABLE 4. APPLICABLE SUBGROUPS

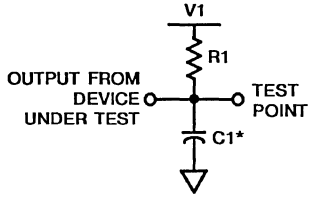
CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

A.C. Testing Input, Output Waveform



A.C. Testing: All input signals (other than CLK) must switch between VIL-0.4V and VIH+0.4. CLK must switch between 0.4V and VCC-0.4V. Input rise and fall times are driven at 1ns/V.

A.C. Test Circuit



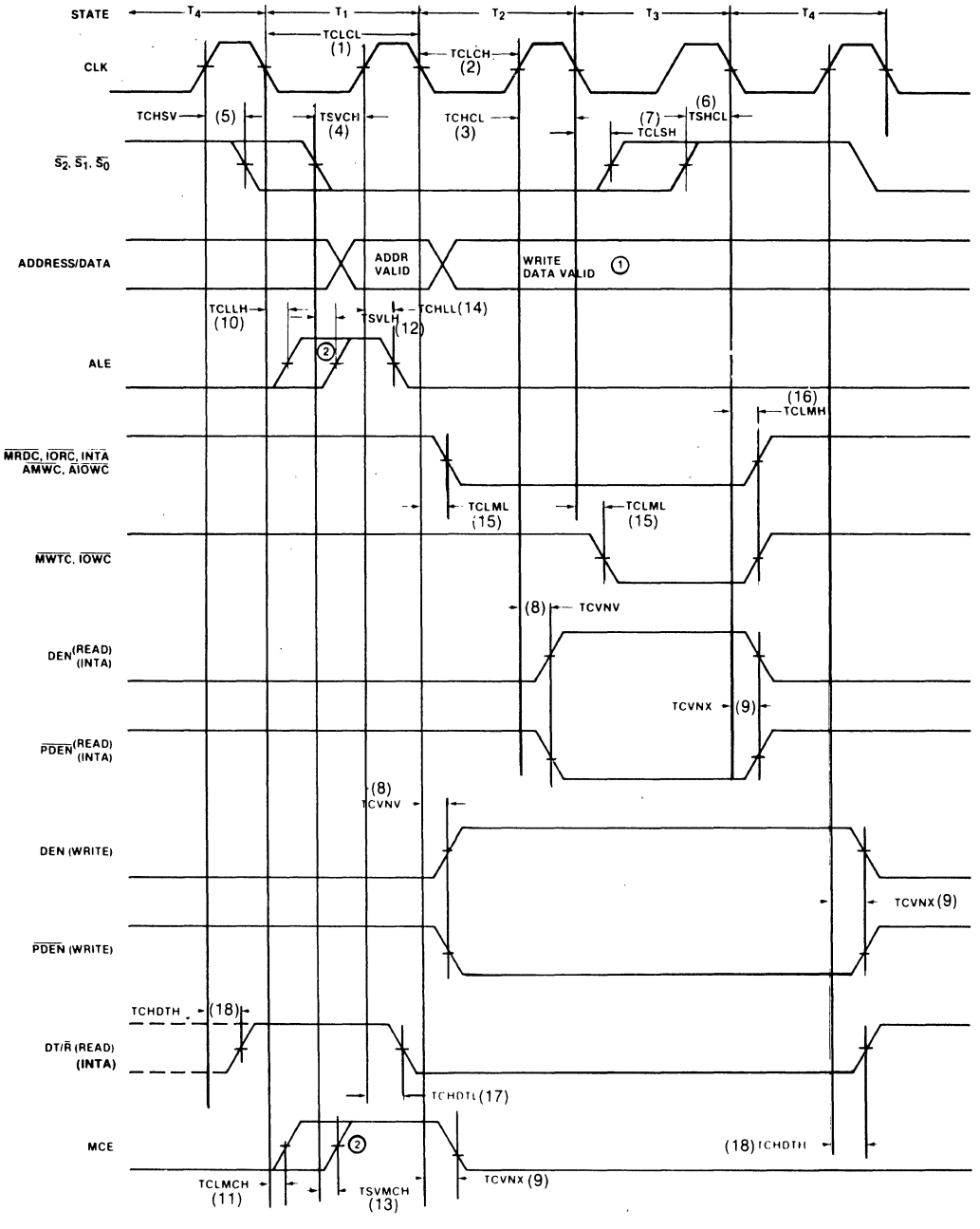
* Includes Stray and Jig Capacitance

TEST CONDITION DEFINITION TABLE

TEST CONDITION	V1	R1	C1
1	2.13V	220Ω	80pF
2	2.29V	91Ω	300pF
3	1.5V	187Ω	300pF
4	1.5V	187Ω	50pF

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

Timing Waveforms (Note 3)



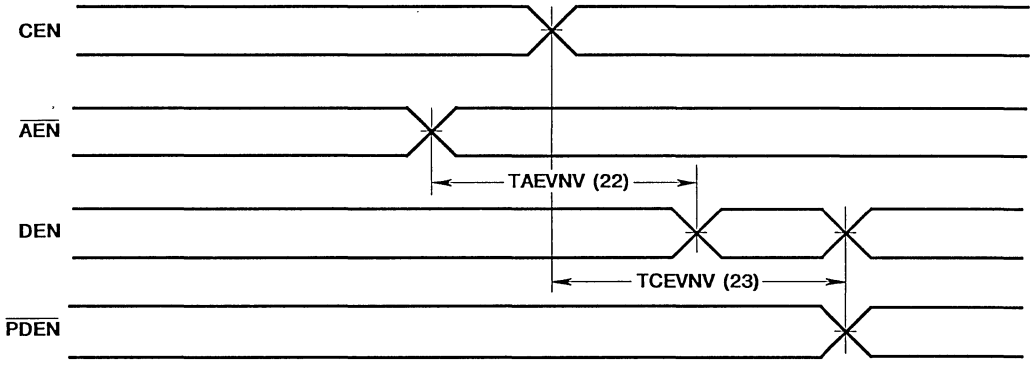
NOTES: 1. Address/Data Bus is shown only for reference purposes.

2. Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active. Whichever occurs last.

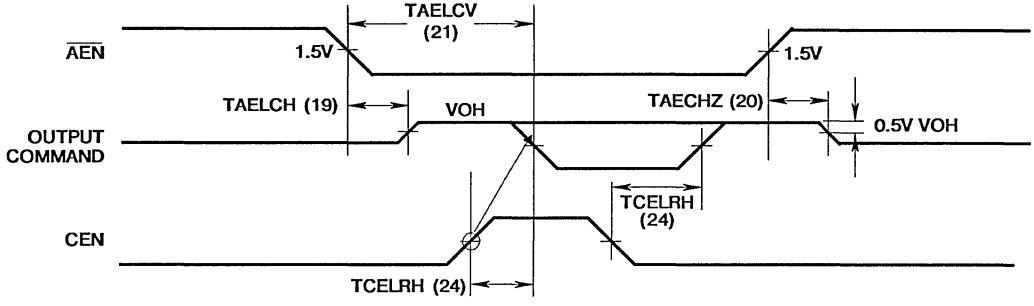
3. All timing measurements are made at 1.5V unless otherwise specified.

Timing Waveforms (Continued) (Note 3)

DEN, $\overline{\text{PDEN}}$ QUALIFICATION TIMING



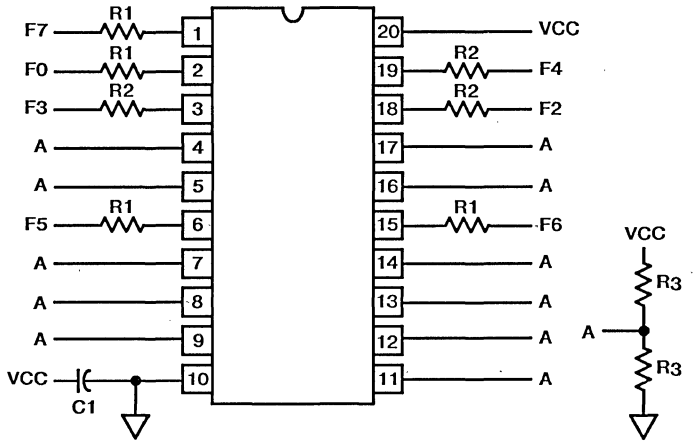
ADDRESS ENABLE ($\overline{\text{AEN}}$) TIMING (THREE-STATE ENABLE/DISABLE)



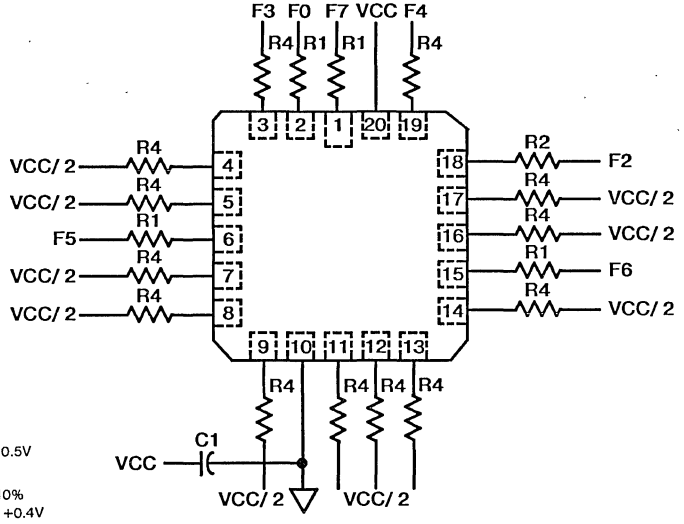
NOTE: CEN must be low or invalid prior to T2 to prevent the command from being generated.

Burn-In Circuit

82C88/883 CERAMIC DIP



82C88/883 CERAMIC LCC



NOTES:
1. VCC = 5.5V ± 0.5V
   GND = 0V
2. VIH = 4.5V ± 10%
   VIL = -0.2V to +0.4V
3. Component Values:
   R1 = 47kΩ, 1/4W, 5%
   R2 = 1.5kΩ, 1/4W, 5%
   R3 = 10kΩ, 1/4W, 5%
   R4 = 1.2kΩ, 1/4W, 5%
   C1 = 0.01μF (Min)
   F0 = 100kHz ± 10%
   F1 = F0/2
   F2 = F1/2
   .
   .
   .
   F7 = F6/2

Metallization Topology

DIE DIMENSIONS:
103.5 x 116.5 x 19 ± 1mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 2kÅ

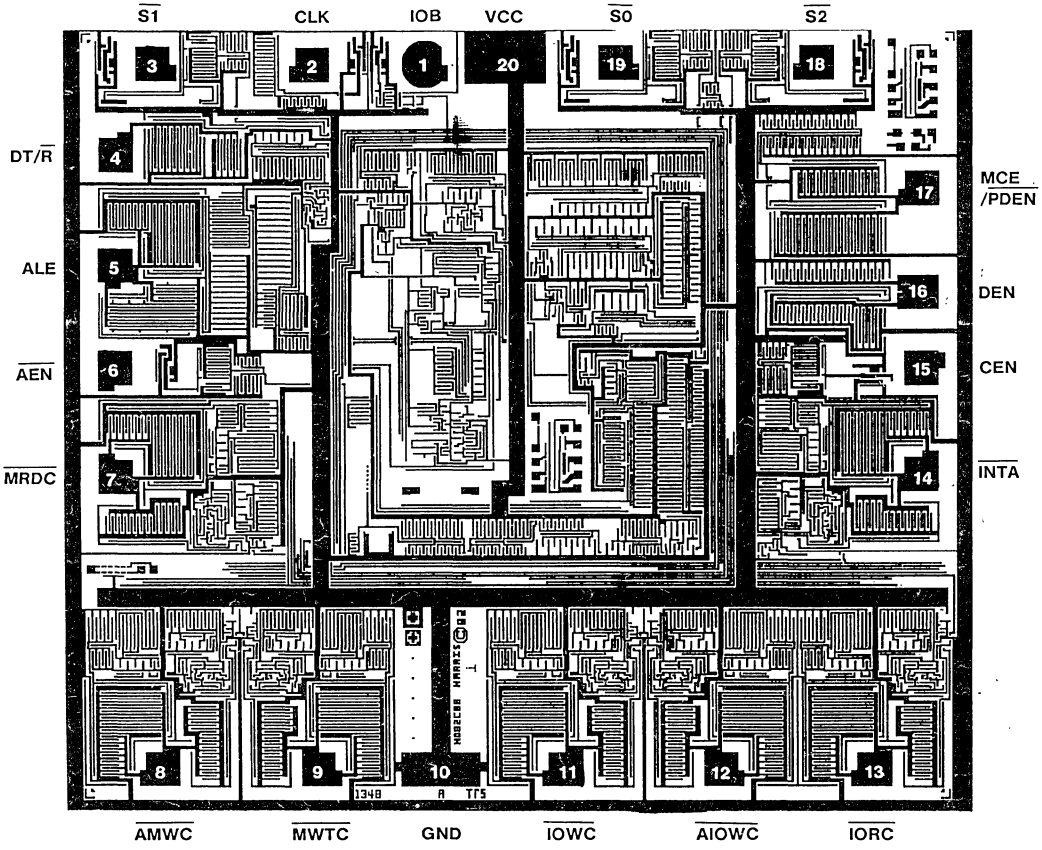
GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.9×10^5 A/cm^2

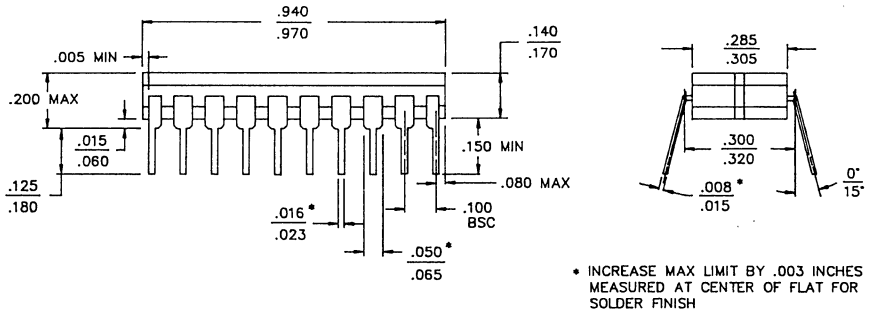
Metallization Mask Layout

82C88/883



Packaging†

20 PIN CERAMIC DIP

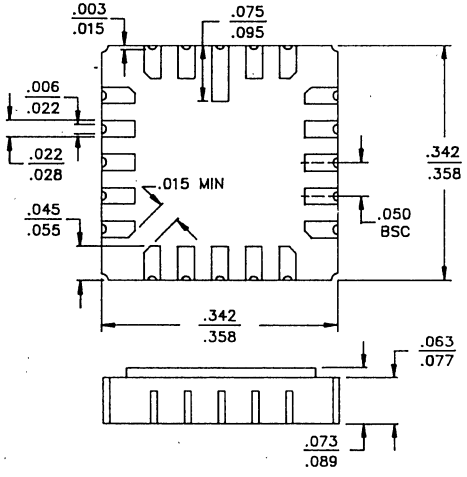


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-8

20 PAD CERAMIC LCC
BOTTOM VIEW



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Functional Description

Command and Control Logic

The command logic decodes the three 80C86, 8086, 80C88, 8088, 80186, 80188 or 8089 status lines ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) to determine what command is to be issued (see Table A).

TABLE A. COMMAND DECODE DEFINITION

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	PROCESSOR STATE	82C88 COMMAND
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

I/O Bus Mode

The 82C88 is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode, all I/O command lines ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (i.e., not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the 82C88 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one 82C88 Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or perpherals dedicated to one processor exist in a multi-processor system.

System Bus Mode

The 82C88 is in the System Bus mode if the IOB pin is strapped LOW. In this mode, no command is issued until a specified time period after the $\overline{AEN}$ line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

Command Outputs

The advanced write commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the processor from entering an unnecessary wait state.

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

The command outputs are:

$\overline{MRDC}$ - Memory Read Command
$\overline{MWTC}$ - Memory Write Command
$\overline{IORC}$ - I/O Read Command
$\overline{IOWC}$ - I/O Write Command
$\overline{AMWC}$ - Advanced Memory Write Command
$\overline{AIOWC}$ - Advanced I/O Write Command
$\overline{INTA}$ - Interrupt Acknowledge

Control Outputs

The control outputs of the 82C88 are Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/ Peripheral Data Enable (MCE/$\overline{PDEN}$). The DEN signal determines when the external bus should be enabled onto the local bus and the DT/$\overline{R}$ determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ pin changes function with the two modes of the 82C88. When the 82C88 is in the IOB mode (IOB HIGH), the $\overline{PDEN}$ signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

Interrupt Acknowledge and MCE

The MCE signal is used during an interrupt acknowledge cycle if the 82C88 is in the System Bus mode (IOB LOW). During any interrupt sequence, there are two interrupt acknowledge cycles that occur back to back. During the first interrupt cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle, the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case, the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable and Halt

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the 82C82/82C83H address latches. ALE also serves to strobe the status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) into a latch for halt state decoding.

Command Enable

The Command Enable (CEN) input acts as a command qualifier for the 82C88. If the CEN pin is high, the 82C88 functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

HARRIS

82C89/883

June 1989

CMOS Bus Arbiter

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Pin Compatible with Bipolar 8289
- Compatible with 5MHz and 8MHz 80C86 and 80C88
- Provides Multi-Master System Bus Control and Arbitration
- Provides Simple Interface with 82C88/8288 Bus Controller
- Synchronizes 80C86/8086, 80C88/8088 Processors with Multi-Master Bus
- Bipolar Drive Capability
- Four Operating Modes for Flexible System Configuration
- Low Power Operation
  - ICCSB ..... 10μA Maximum
  - ICCOP ..... 1mA/MHz Maximum
- Military Operating Temperature Range ..... -55°C to +125°C

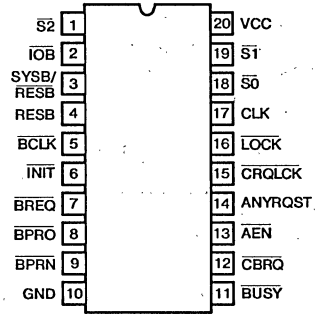
Description

The Harris 82C89/883 Bus Aribiter is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). This circuit, along with the 82C88 bus controller, provides full bus arbitration and control for multi-processor systems. The 82C89/883 is typically used in medium to large 80C86 or 80C88 systems where access to the bus by several processors must be coordinated. The 82C89/883 also provides high output current and capacitive drive to eliminate the need for additional bus buffering.

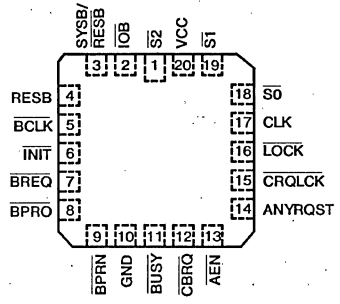
Static CMOS circuit design insures low operating power. The advanced Harris SAJI CMOS process results in performance equal to or greater than existing equivalent products at a significant power savings.

Pinouts

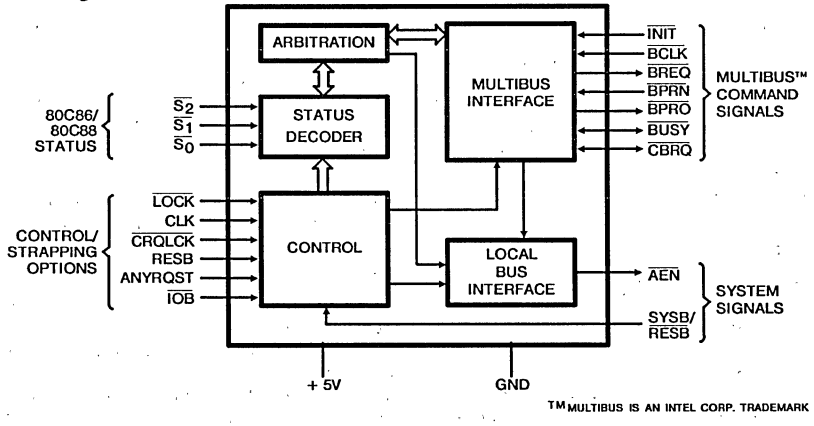
82C89/883 (CERAMIC DIP)
TOP VIEW



82C89/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



™ MULTIBUS IS AN INTEL CORP. TRADEMARK

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
VCC	20		VCC: The +5V Power supply pin. A 0.1 µF capacitor between pins 10 and 20 is recommened for decoupling.
GND	10		GROUND.
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	1, 18-19	I	STATUS INPUT PINS: The status input pins from an 80C86, 80C88 or 8089 processor. The 82C89/883 decodes these pins to initiate bus request and surrender actions. (See Table A in Design Information.)
CLK	17	I	CLOCK: From the 82C84A or 82C85 clock chip and serves to establish when bus arbiter actions are initiated.
$\overline{LOCK}$	16	I	LOCK: A processor generated signal which when activated (low) prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter, regardless of its priority.
$\overline{CRQLCK}$	15	I	COMMON REQUEST LOCK: An active low signal which prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter requesting the bus through the $\overline{CBRQ}$ input pin.
RESB	4	I	RESIDENT BUS: A strapping option to configure the arbiter to operate in systems having both a multi-master system bus and a Resident Bus. Strapped high, the multi-master system bus is requested or surrendered as a function of the SYSB/$\overline{RESB}$ input pin. Strapped low, the SYSB/$\overline{RESB}$ input is ignored.
ANYRQST	14	I	ANY REQUEST: A strapping option which permits the multi-master system bus to be surrendered to a lower priority arbiter as if it were an arbiter of higher priority (i.e., when a lower priority arbiter requests the use of the multi-master system bus, the bus is surrendered as soon as it is possible). When ANYRQST is strapped low, the bus is surrendered according to Table A in Design Information. If ANYRQST is strapped high and $\overline{CBRQ}$ is activated, the bus is surrendered at the end of the present bus cycle. Strapping $\overline{CBRQ}$ low and ANYRQST high forces the 82C89/883 arbiter to surrender the multi-master system bus after each transfer cycle. Note that when surrender occurs $\overline{BREQ}$ is driven false (high).
$\overline{IOB}$	2	I	IO BUS: A strapping option which configures the 82C89/883 Arbiter to operate in systems having both an IO Bus (Peripheral Bus) and a multi-master system bus. The arbiter requests and surrenders the use of the multi-master system bus as a function of the status line, $\overline{S2}$. The multi-master system bus is permitted to be surrendered while the processor is performing IO commands and is requested whenever the processor performs a memory command. Interrupt cycles are assumed as coming from the peripheral bus and are treated as an IO command.
$\overline{AEN}$	13	O	ADDRESS ENABLE: The output of the 82C89/883 Arbiter to the processor's address latches, to the 82C88 Bus Controller and 82C84A or 82C85 Clock Generator. $\overline{AEN}$ serves to instruct the Bus Controller and address latches when to three-state their output drivers.
$\overline{INIT}$	6	I	INITIALIZE: An active low multi-master system bus input signal used to reset all the bus arbiters on the multi-master system bus. After initialization, no arbiters have the use of the multi-master system bus.
SYSB/ $\overline{RESB}$	3	I	SYSTEM BUS/RESIDENT BUS: An input signal when the arbiter is configured in the System/ Resident Mode ($\overline{RESB}$ is strapped high) which determines when the multi-master system bus is requested and multi-master system bus surrendering is permitted. The signal is intended to originate from a form of address-mapping circuitry, such as a decoder or PROM attached to the resident address bus. Signal transitions and glitches are permitted on this pin from ϕ1 of T4 to ϕ1 of T2 of the processor cycle. During the period from ϕ1 of T2 to ϕ1 of T4, only clean transitions are permitted on this pin (no glitches). If a glitch occurs, the arbiter may capture or miss it, and the multi-master system bus may be requested or surrendered, depending upon the state of the glitch. The arbiter requests the multi-master system bus in the System/Resident Mode when the state of the SYSB/$\overline{RESB}$ pin is high and permits the bus to be surrendered when this pin is low.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{CBRQ}$	12	I/O	COMMON BUS REQUEST: An input signal which instructs the arbiter if there are any other arbiters of lower priority requesting the use of the multi-master system bus. The $\overline{CBRQ}$ pins (open-drain output) of all the 82C89/883 Bus Arbiters which surrender to the multi-master system bus upon request are connected together. The Bus Arbiter running the current transfer cycle will not itself pull the $\overline{CBRQ}$ line low. Any other arbiter connected to the $\overline{CBRQ}$ line can request the multi-master system bus. The arbiter presently running the current transfer cycle drops its $\overline{BREQ}$ signal and surrenders the bus whenever the proper surrender conditions exist. Strapping $\overline{CBRQ}$ low and ANYRQST high allows the multi-master system bus to be surrendered after each transfer cycle. See the pin definition of ANYRQST.
$\overline{BCLK}$	5	I	BUS CLOCK: The multi-master system bus clock to which all multi-master system bus interface signals are synchronized.
$\overline{BREQ}$	7	O	BUS REQUEST: An active low output signal in the Parallel Priority Resolving Scheme which the arbiter activates to request the use of the multi-master system bus.
$\overline{BPRN}$	9	I	BUS PRIORITY IN: The active low signal returned to the arbiter to instruct it that it may acquire the multi-master system bus on the next falling edge of $\overline{BCLK}$. $\overline{BPRN}$ active indicates to the arbiter that it is the highest priority requesting arbiter presently on the bus. The loss of $\overline{BPRN}$ instructs the arbiter that it has lost priority to a higher priority arbiter.
$\overline{BPRO}$	8	O	BUS PRIORITY OUT: An active low output signal used in the serial priority resolving scheme where $\overline{BPRO}$ is daisy-chained to $\overline{BPRN}$ of the next lower priority arbiter.
$\overline{BUSY}$	11	I/O	BUSY: An active low open-drain multi-master system bus interface signal used to instruct all the arbiters on the bus when the multi-master system bus is available. When the multi-master system bus is available the highest requesting arbiter (determined by $\overline{BPRN}$) seizes the bus and pulls $\overline{BUSY}$ low to keep other arbiters off of the bus. When the arbiter is done with the bus, it releases the $\overline{BUSY}$ signal, permitting it to go high and thereby allowing another arbiter to acquire the multi-master system bus.

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	80°C/W	21°C/W
Ceramic LCC Package	76°C/W	19°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 620mW
Ceramic LCC Package 664mW
Gate Count ..... 200 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... +4.5V to +5.5V

TABLE 1. 82C89/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical "1" Input Voltage	VIH	VCC = 5.5V, Note 2	1, 2, 3	$-55°C \le T_A \le +125°C$	2.2	-	V
Logical "0" Input Voltage	VIL	Note 2	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.8	V
CLK Logical "1" Input Voltage	VIHC	VCC = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	70% VCC	-	V
CLK Logical "0" Input Voltage	VILC		1, 2, 3	$-55°C \le T_A \le +125°C$	-	20% VCC	V
Output HIGH Voltage, $\overline{BUSY}$, $\overline{CBRQ}$	VOH1	Open Drain, Note 3 DIP Pins 11, 12	1, 2, 3	$-55°C \le T_A \le +125°C$	-	-	V
Output HIGH Voltage, All Other Outputs	VOH2	IOH = -2.5mA, Note 3 IOH = -100µA, Note 3	1, 2, 3	$-55°C \le T_A \le +125°C$	3.0 VCC-0.4	- -	V V
Output LOW Voltage, $\overline{BUSY}$, $\overline{CBRQ}$	VOL1	IOL = 20mA, Note 3, DIP Pins 11, 12	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.45	V
Output LOW Voltage, $\overline{AEN}$	VOL2	IOL = 16mA, Note 3, DIP Pin 13	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.45	V
Output LOW Voltage, $\overline{BPRO}$, $\overline{BREQ}$	VOL3	IOL = 8mA, Note 3, DIP Pins 7, 8	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.45	V
Input Leakage Current	II	VCC = 5.5V, VIN = GND or VCC DIP Pins 1-6, 9, 14-19	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Output Leakage Current	IO	VCC = 5.5V, VOUT = GND or VCC DIP Pins 11, 12	1, 2, 3	$-55°C \le T_A \le +125°C$	-10	+10	µA
Standby Power Supply Current	ICCSB	VCC = 5.5V, VIN = GND or VCC Outputs Open	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	µA
Operating Power Supply Current	ICCOP	VCC = 5.5V, f = 1MHz, Outputs Open, Note 4	1, 2, 3	$-55°C \le T_A \le +125°C$	-	1	mA/MHz

NOTES: 1. VCC = 4.5V unless otherwise specified. All voltage referenced to device GND.
2. Does not apply to $\overline{IOB}$, RESB, or ANYRQST. These are strap options and should be held to VCC or GND.
3. Interchanging of force and sense conditions is permitted.
4. Maximum current defined by CLK or $\overline{BCLK}$, whichever has the highest operating frequency.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. 82C89/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CLK Cycle Time	(1)TCLCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	125	-	ns
CLK Low Time	(2)TCLCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	55	-	ns
CLK High Time	(3)TCHCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	35	-	ns
Status Active Setup Time	(4)TSVCH	Note 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	65	-	ns
Status Inactive Setup Time	(5)TSHCL	Note 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Status Inactive Hold Time	(6)THVCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Status Active Hold Time	(7)THVCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
$\overline{BUSY}$** Setup to $\overline{BCLK}$	(8)TBYSBL	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
$\overline{CBRQ}$** Setup to $\overline{BCLK}$	(9)TCBSBL	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
$\overline{BCLK}$ Cycle Time	(10)TBLBL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
$\overline{BCLK}$ High Time	(11)TBHCL	Note 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	ns
$\overline{LOCK}$ Inactive Hold Time	(12)TCLLL1		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
$\overline{LOCK}$ Active Setup Time	(13)TCLLL2		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
$\overline{BPRN}$** to $\overline{BCLK}$ Setup Time	(14)TPNBL	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
SYSB/$\overline{RESB}$ Setup Time	(15)TCLSR1		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
SYSB/$\overline{RESB}$ Hold Time	(16)TCLSR2		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	ns
Initialization Pulse Width	(17)TIVIH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	675	-	ns
$\overline{BCLK}$ to $\overline{BREQ}$** Delay Time	(18)TBLBRL	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	35	ns
$\overline{BCLK}$ to $\overline{BPRO}$**	(19)TBLPOH	Notes 3, 4	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	35	ns
$\overline{BPRN}$** to $\overline{BPRO}$** Delay Time	(20)TPNPO	Notes 3, 4	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	22	ns
$\overline{BCLK}$ to $\overline{BUSY}$ Low	(21)TBLBYL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	60	ns
CLK to $\overline{AEN}$ High	(23)TCLAEH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	65	ns
$\overline{BCLK}$ to $\overline{AEN}$ Low	(24)TBLAEL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
$\overline{BCLK}$ to $\overline{CBRQ}$ Low	(25)TBLCBL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	60	ns
Output Rise Time	(27)TOLOH	From 0.8V to 2.0V Except $\overline{BUSY}$ and $\overline{CBRQ}$	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	20	ns
Output Fall Time	(28)TOHOL	From 2.0V to 0.8V Except $\overline{BUSY}$ and $\overline{CBRQ}$	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	12	ns

NOTES: 1. VCC = 4.5V and 5.5V unless otherwise specified. Tested as follows: f = 1MHz, VIH = 2.6V, VIL = 0.4V, VIHC = VCC - 0.4V, VILC = 0.4V. Load per appropriate A.C. test circuit, VOH $\geq$ 1.5V and VOL $\leq$ 1.5V. Input rise and fall times are driven at 1ns/V.

2. Reference Table 3 for maximum limit.
3. Both transitions of the signal apply to parameters with asterisks (**).
4. $\overline{BCLK}$ generates $\overline{BPRO}$ from arbiter #1 wherein subsequent $\overline{BPRO}$ changes lower in the chain are generated from $\overline{BPRO}$ of the next higher priority arbiter.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. 82C89/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	f = 1MHz, all measurements are reference to device GND, VCC = Open	1	$T_A = +25^oC$	-	10	pF
Output Capacitance	COUT		1	$T_A = +25^oC$	-	10	pF
I/O Capacitance	CIO		1	$T_A = +25^oC$	-	15	pF
Status Active Setup Time	(4)TSVCH		1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	TCLCL -10	ns
Status Inactive Setup Time	(5)TSHCL		1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	TCLCL -10	ns
$\overline{BCLK}$ High Time	(11)TBHCL		1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	0.65 TBLBL	ns
$\overline{BCLK}$ to $\overline{BUSY}$ Float Time	(22)TBLBYH		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	35	ns
$\overline{BCLK}$ to $\overline{CBRQ}$ Float Time	(26)TBLCBH		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
Input Rise Time	(29)TILIH		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	20	ns
Input Fall Time	(30)TIHIL		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	20	ns

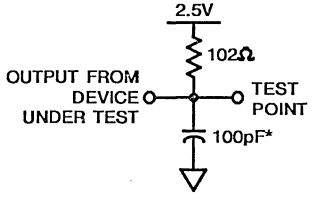
NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. VCC = 4.5V and 5.5V
3. Reference Table 2 for minimum limit.

TABLE 4. APPLICABLE SUBGROUPS

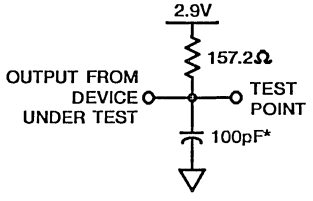
CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

A.C. Test Load Circuits

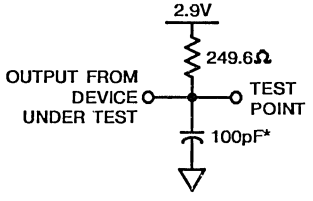
$\overline{BUSY}$, $\overline{CBRQ}$ LOAD CIRCUIT



$\overline{AEN}$ LOAD CIRCUIT



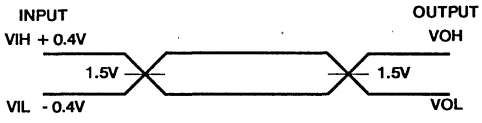
$\overline{BPRQ}$, $\overline{BREQ}$ LOAD CIRCUIT



* Includes Stray and Jig Capacitance

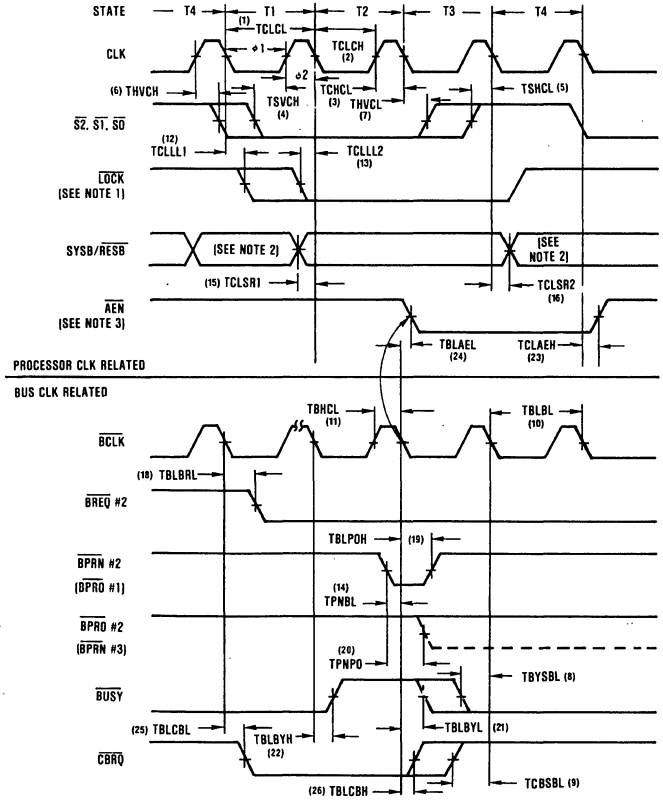
CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

A.C. Testing Input, Output Waveform



A.C. Testing: Inputs are driven at VIH +0.4V for a logic "1" and VIL -0.4V for a logic "0". The clock is driven at VCC -0.4V and 0.4V. Timing measurements are made at 1.5V for both a logic "1" and "0".

Timing Waveform



NOTES:

1. LOCK active can occur during any state, as long as the relationships shown above with respect to the CLK are maintained. LOCK inactive has no critical time and can be asynchronous. CRQLCK has no critical timing and is considered an asynchronous input signal.
2. Glitching of SYSB/RESB is permitted during this time. After θ2 of T1, and before θ1 of T4, SYSB/RESB should be stable to maintain system efficiency.
3. AEN leading edge is related to BCLK, trailing edge to CLK. The trailing edge of AEN occurs after bus priority is lost.

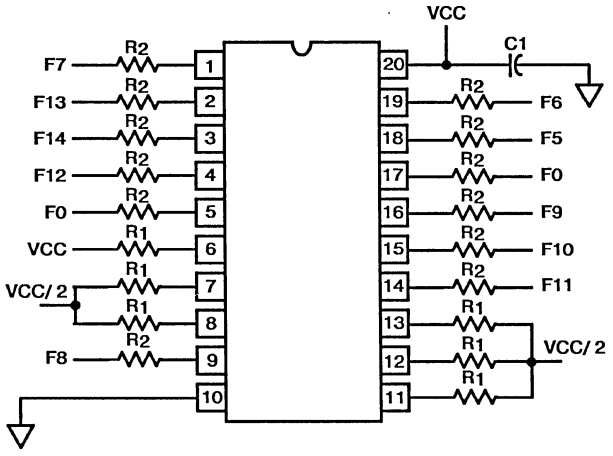
ADDITIONAL NOTES:

The signals related to CLK are typical processor signals, and do not relate to the depicted sequence of events of the signals referenced to BCLK. The signals shown related to the BCLK represent a hypothetical sequence of events for illustration. Assume 3 bus arbiters of priorities 1, 2 and 3 configured in serial priority resolving scheme (as shown in Design Information Figure 3). Assume arbiter 1 has the bus and is holding BUSY low. Arbiter #2 detects its processor wants the bus and pulls low BREQ #2. If BPRN #2 is high (as shown), arbiter #2 will pull low CBRQ line. CBRQ signals to the higher priority arbiter #1 that a lower priority arbiter wants the bus. [A higher priority arbiter would be granted BPRN when it makes the bus request rather than having to wait for another arbiter to release the bus through CBRQ]. *Arbiter #1 will relinquish the multi-master system bus when it enters a state not requiring it (see Design Information Table A), by lowering its BPRO #1 (tied to BPRN #2) and releasing BUSY. Arbiter #2 now sees that is has priority from BPRN #2 being low and releases CBRQ. As soon as BUSY signifies the bus is available (high), arbiter #2 pulls BUSY low on next falling edge of BCLK. Note that if arbiter #2 didn't want the bus at the time it received priority, it would pass priority to the next lower priority arbiter by lowering its BPRO #2 [TPNPO].

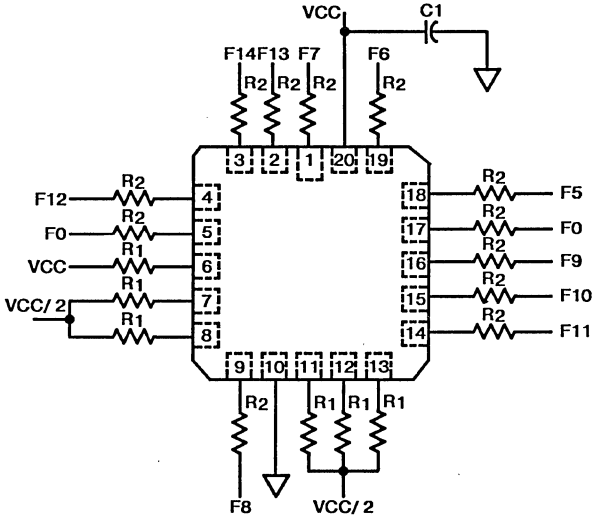
*Note that even a higher priority arbiter which is acquiring the bus through BPRN will momentarily drop CBRQ until it has acquired the bus.

Burn-In Circuits

82C89/883 CERAMIC DIP



82C89/883 CERAMIC LCC



NOTES:
1. VCC = 5.5V ± 0.5V, GND = 0V
2. VIH = 4.5V ± 10%, VIL = -0.2V to +0.4V
3. Components Values:
   R1 = 1.2kΩ, 1/4W, 5%
   R2 = 47kΩ, 1/4W, 5%
   C1 = 0.01μF minimum
   F0 = 100kHz ± 10%
   F1 = F0/2
   F2 = F1/2 . . .
   F14 = F13/2

Metallization Topology

DIE DIMENSIONS:
92.9 x 95.7 x 19 ± 1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 2kÅ

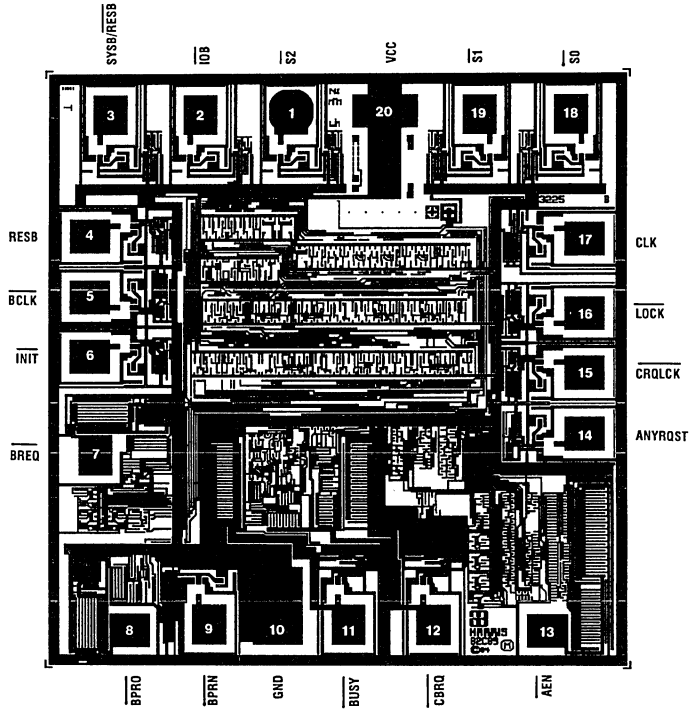
GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ ± 2kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.8×10^5 A/cm^2

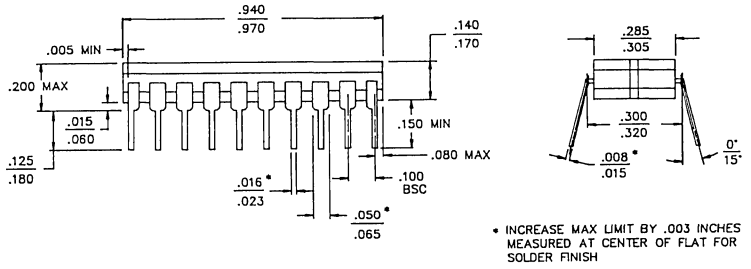
Metallization Mask Layout

82C89/883



Packaging†

20 PIN CERAMIC DIP

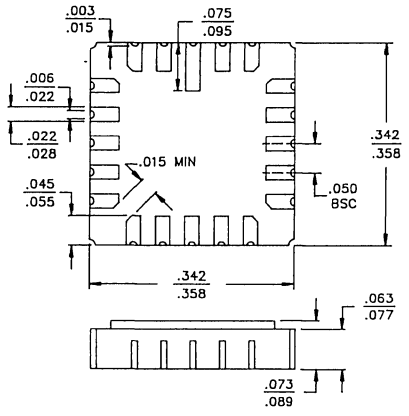


LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-8

20 PAD CERAMIC LCC

BOTTOM VIEW



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Functional Description

The 82C89 Bus Arbiter operates in conjunction with the 82C88 Bus Controller to interface 80C86, 80C88 processors to a multi-master system bus (both the 80C86 and 80C88 are configured in their max mode). The processor is unaware of the arbiter's existence and issues commands as though it has exclusive use of the system bus. If the processor does not have the use of the multi-master system bus, the arbiter prevents the Bus Controller (82C88), the data transceivers and the address latches from accessing the system bus (e.g. all bus driver outputs are forced into the high impedance state). Since the command sequence was not issued by the 82C88, the system bus will appear as "Not Ready" and the processor will enter wait states. The processor will remain in Wait until the Bus Arbiter acquires the use of the multi-master system bus whereupon the arbiter will allow the bus controller, the data transceivers, and the address latches to access the system. Typically, once the command has been issued and a data transfer has taken place, a transfer acknowledge (XACK) is returned to the processor to indicate "READY" from the accessed slave device. The processor then completes its transfer cycle. Thus the arbiter serves to multiplex a processor (or bus master) onto a multi-master system bus and avoid contention problems between bus masters.

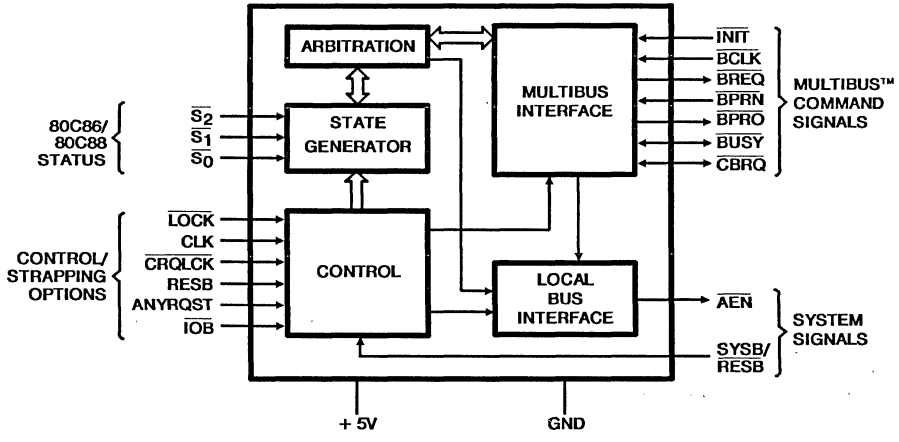
Arbitration Between Bus Masters

In general, higher priority masters obtain the bus when a lower priority master completes its present transfer cycle. Lower priority bus masters obtain the bus when a higher priority master is not accessing the system bus. A strapping option (ANYRQST) is provided to allow the arbiter to surrender the bus to a lower priority master as though it were a master of higher priority. If there are no other bus masters requesting the bus, the arbiter maintains the bus so long as its processor has not entered the HALT State. The arbiter will not voluntarily surrender the system bus and has to be forced off by another master's bus request, the HALT State being the only exception. Additional strapping options permit other modes of operation wherein the multi-master system bus is surrendered or requested under different sets of conditions.

Priority Resolving Techniques

Since there can be many bus masters on a multi-master system bus, some means of resolving priority between bus masters simultaneously requesting the bus must be provided. The 82C89 Bus Arbiter provides several resolving techniques. All the techniques are based on a priority concept that at a given time one bus master will have priority above all the rest. There are provisions for using parallel priority resolving techniques, serial priority resolving techniques, and rotating priority techniques.

Functional Diagram



™ MULTIBUS IS AN INTEL CORP. TRADEMARK

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Parallel Priority Resolving

The parallel priority resolving technique uses a separate bus request line $\overline{BREQ}$ for each arbiter on the multi-master system bus, see Figure 1. Each $\overline{BREQ}$ line enters into a priority encoder which generates the binary address of the highest priority $\overline{BREQ}$ line which is active. The binary address is decoded by a decoder to select the corresponding $\overline{BPRN}$ (Bus Priority In) line to be returned to the highest priority requesting arbiter. The arbiter receiving priority ($\overline{BPRN}$ true) then allows its associated bus master onto the multi-master system bus as soon as it becomes available (i.e., the bus is no longer busy). When one bus arbiter gains priority over another arbiter it cannot immediately seize the bus, it must wait until the present bus transaction is complete. Upon completing its transaction the present bus occupant recognizes that it no longer has priority and surrenders the bus by releasing $\overline{BUSY}$. $\overline{BUSY}$ is an active low "OR" tied signal line which goes to every bus arbiter on the system bus. When $\overline{BUSY}$ goes inactive (high), the arbiter which presently has bus priority ($\overline{BPRN}$ true) then seizes the bus and pulls $\overline{BUSY}$ low to keep other arbiters off of the bus. See waveform timing diagram, Figure 2. Note that all multi-master system bus transactions are synchronized to the bus clock ($\overline{BCLK}$). This allows the parallel priority resolving circuitry or any other priority resolving scheme employed to settle.

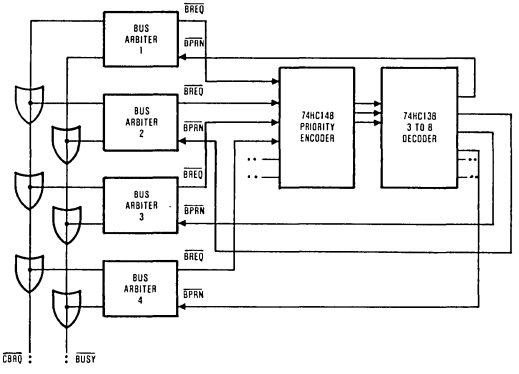


FIGURE 1. PARALLEL PRIORITY RESOLVING TECHNIQUE

Serial Priority Resolving

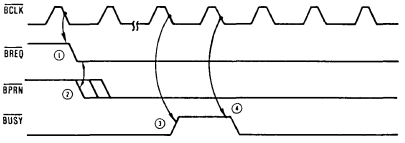
The serial priority resolving technique eliminates the need for the priority encoder-decoder arrangement by daisy-chaining the bus arbiters together, connecting the higher priority bus arbiter's $\overline{BPRO}$ (Bus Priority Out) output to the $\overline{BPRN}$ of the next lower priority. See Figure 3.

Rotating Priority Resolving

The rotating priority resolving technique is similar to that of the parallel priority resolving technique except that priority is dynamically re-assigned. The priority encoder is replaced by a more complex circuit which rotates priority between requesting arbiters thus allowing each arbiter an equal chance to use the multi-master system bus, over time.

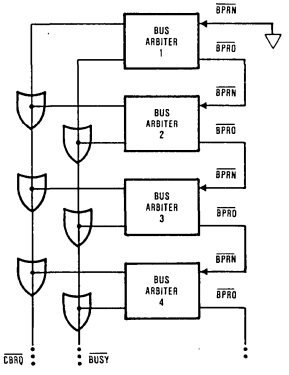
Which Priority Resolving Technique To Use

There are advantages and disadvantages for each of the techniques described above. The rotating priority resolving technique requires substantial external logic to implement while the serial technique uses no external logic but can accommodate only a limited number of bus arbiters before the daisy-chain propagation delay exceeds the multi-master's system bus clock ($\overline{BCLK}$). The parallel priority resolving technique is in general a good compromise between the other two techniques. It allows for many arbiters to be present on the bus while not requiring too much logic to implement.



NOTES:
1. Higher priority bus arbiter requests the Multi-Master system bus.
2. Attains priority.
3. Lower priority bus arbiter releases $\overline{BUSY}$.
4. Higher priority bus arbiter then acquires the bus and pulls $\overline{BUSY}$ down.

FIGURE 2. HIGHER PRIORITY ARBITER OBTAINING THE BUS FROM A LOWER PRIORITY ARBITER



NOTE:
The number of arbiters that may be daisy-chained together in the serial priority resolving scheme is a function of $\overline{BCLK}$ and the propagation delay from arbiter to arbiter. Normally, at 10MHz only 3 arbiters may be daisychained.

FIGURE 3. SERIAL PRIORITY RESOLVING

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

82C89 Modes Of Operation

There are two types of processors for which the 82C89 will provide support: An Input/Output processor (i.e. an NMOS 8089 IOP) and the 80C86, 80C88. Consequently, there are two basic operating modes in the 82C89 bus arbiter. One, the IOB (I/O Peripheral Bus) mode, permits the processor access to both an I/O Peripheral Bus and a multi-master system bus. The second, the RESB (Resident Bus mode), permits the processor to communicate over both a Resident Bus and a multi-master system bus. An I/O Peripheral Bus is a bus where all devices on that bus, including memory, are treated as I/O devices and are addressed by I/O commands. All memory commands are directed to another bus, the multi-master system bus. A Resident Bus can issue both memory and I/O commands, but it is a distinct and separate bus from the multi-master system bus. The distinction is that the Resident Bus has only one master, providing full availability and being dedicated to that one master.

The $\overline{IOB}$ strapping option configures the 82C89 Bus Arbiter into the $\overline{IOB}$ mode and the strapping option RESB configures it into the RESB mode. It might be noted at this point that if both strapping options are strapped false, the arbiter interfaces the processor to a multi-master system bus only (see Figure 4). With both options strapped true, the arbiter interfaces the processor to a multi-master system bus, a Resident Bus, and an I/O Bus.

In the $\overline{IOB}$ mode, the processor communicates and controls a host of peripherals over the Peripheral Bus. When the I/O Processor needs to communicate with system memory, it does so over the system memory bus. Figure 5 shows a possible I/O Processor system configuration.

The 80C86 and 80C88 processors can communicate with a Resident Bus and a multi-master system bus. Two bus controllers and only one Bus Arbiter would be needed in such a configuration as shown in Figure 6. In such a system configuration the processor would have access to memory and peripherals of both busses. Memory mapping techniques are applied to select which bus is to be

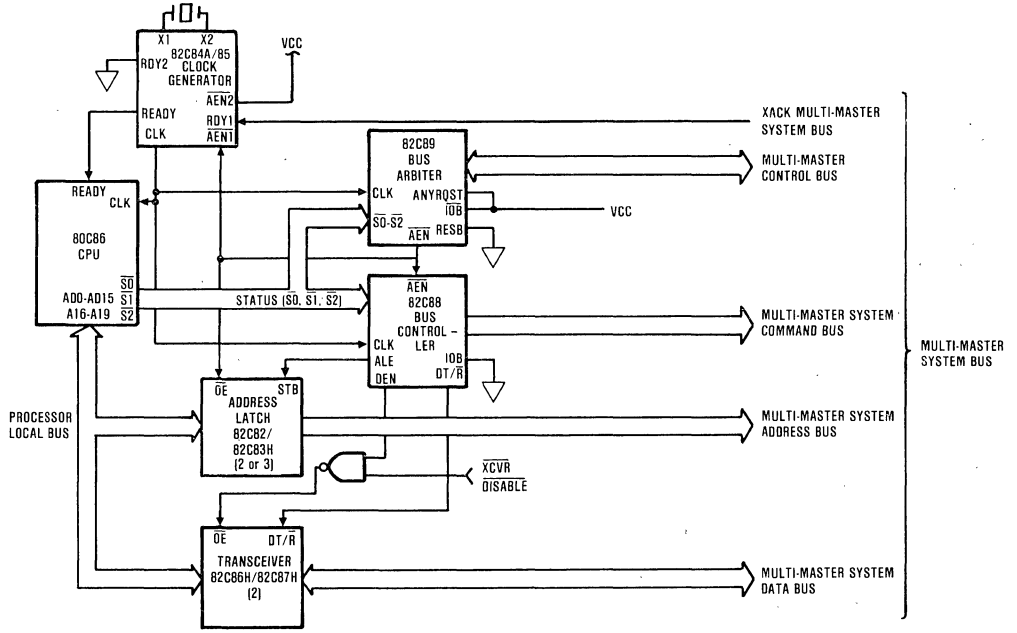


FIGURE 4. TYPICAL MEDIUM COMPLEXITY CPU SYSTEM

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

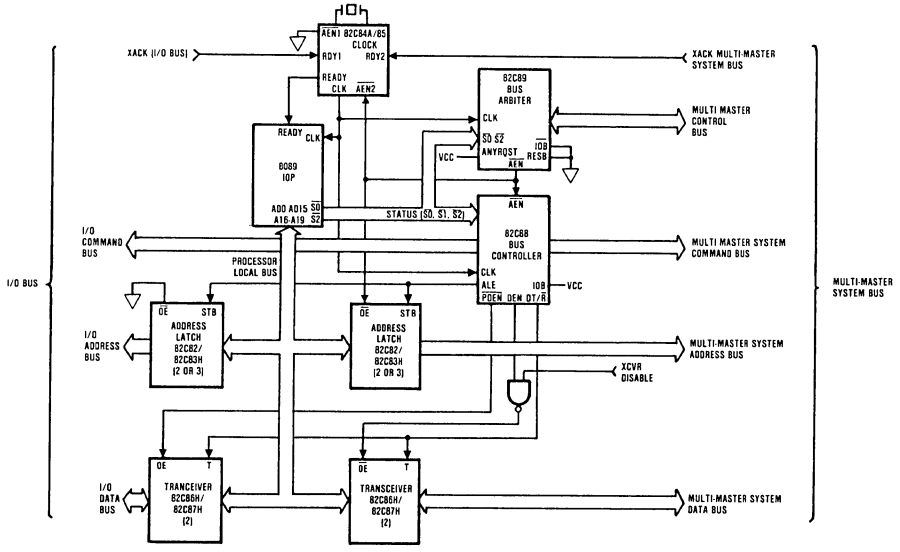


FIGURE 5. TYPICAL MEDIUM COMPLEXITY IOB SYSTEM

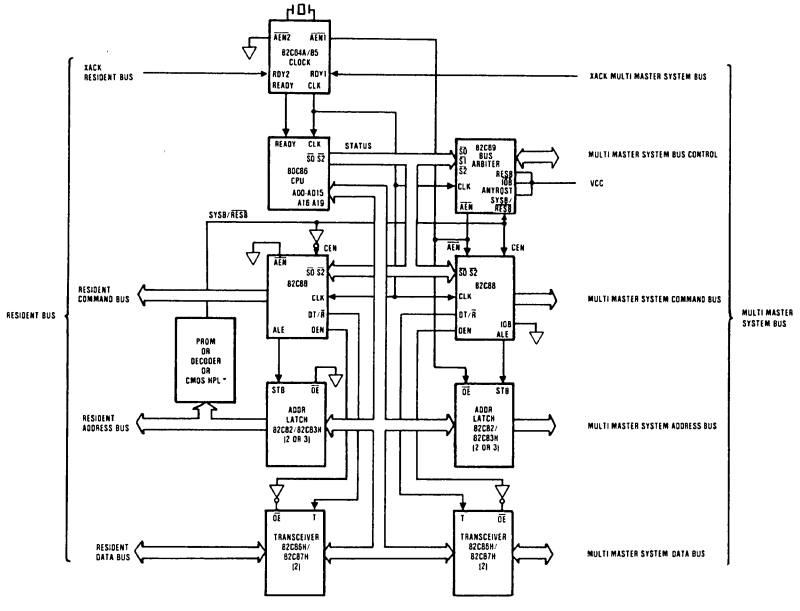


FIGURE 6. 82C89 BUS ARBITER SHOWN IN SYSTEM - RESIDENT BUS CONFIGURATION

* By adding another 82C89 arbiter and connecting its $\overline{AEN}$ to the 82C88 whose $\overline{AEN}$ is presently grounded, the processor could have access to two multi-master buses.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

accessed. The SYSB/$\overline{\text{RESB}}$ input on the arbiter serves to instruct the arbiter as to whether or not the system bus is to be accessed. The signal connected to SYSB/$\overline{\text{RESB}}$ also enables or disables commands from one of the bus controllers.

A summary of the modes that the 82C89 has, along with its response to its status lines inputs, is shown in Table A.

TABLE A. SUMMARY OF 82C89 MODES, REQUESTING AND RELINQUISHING THE MULTI-MASTER SYSTEM BUS

STATUS LINES FROM 80C86 OR 80C88 OR 8088				IOB MODE ONLY $\overline{\text{IOB}}$ = LOW RESB = LOW	RESB MODE ONLY $\overline{\text{IOB}}$ = HIGH, RESB = HIGH		IOB MODE RESB MODE $\overline{\text{IOB}}$ = LOW, RESB = HIGH		SINGLE BUS MODE $\overline{\text{IOB}}$ = HIGH RESB = LOW
	$\overline{\text{S2}}$	$\overline{\text{S1}}$	$\overline{\text{S0}}$		SYSB/$\overline{\text{RESB}}$ = HIGH	SYSB/$\overline{\text{RESB}}$ = LOW	SYSB/$\overline{\text{RESB}}$ = HIGH	SYSB/$\overline{\text{RESB}}$ = LOW	
I/O Commands	0	0	0	X	✓	X	X	X	✓
	0	0	1	X	✓	X	X	X	✓
	0	1	0	X	✓	X	X	X	✓
Halt	0	1	1	X	X	X	X	X	X
Memory Commands	1	0	0	✓	✓	X	✓	X	✓
	1	0	1	✓	✓	X	✓	X	✓
	1	1	0	✓	✓	X	✓	X	✓
Idle	1	1	1	X	X	X	X	X	X

NOTES: 1. X = Multi-Master System Bus is allowed to be Surrendered.

2. ✓ = Multi-Master System Bus is Requested.

MODE	PIN STRAPPING	MULTI-MASTER SYSTEM BUS	
		REQUESTED**	SURRENDERED*
Single Bus Multi-Master Mode	$\overline{\text{IOB}}$ = High RESB = Low	Whenever the processor's status lines go active	HLT + TI • $\overline{\text{CBRQ}}$ + HPBRQ †
RESB Mode Only	$\overline{\text{IOB}}$ = High RESB = High	SYSB/$\overline{\text{RESB}}$ + High • ACTIVE STATUS	(SYSB/$\overline{\text{RESB}}$ = Low + TI) • $\overline{\text{CBRQ}}$ + HLT + HPBRQ
IOB Mode Only	$\overline{\text{IOB}}$ = Low RESB = Low	Memory Commands	(I/O Status + TI) • $\overline{\text{CBRQ}}$ + HLT + HPBRQ
IOB Mode RESB Mode	$\overline{\text{IOB}}$ = Low RESB = High	(Memory Command) • (SYSB/$\overline{\text{RESB}}$ = High)	((I/O Status Commands) + SYSB/$\overline{\text{RESB}}$ = Low) • $\overline{\text{CBRQ}}$ +HPBRQ † + HLT

NOTES: * $\overline{\text{LOCK}}$ prevents surrender of Bus to any other arbiter, $\overline{\text{CRQLCK}}$ prevents surrender of Bus to any lower priority arbiter.

**Except for HALT and Passive or IDLE Status.

† HPBRQ, Higher priority Bus request or $\overline{\text{BPRN}}$ = 1.

1. $\overline{\text{IOB}}$ Active Low.
2. RESB Active High.
3. + is read as "OR" and • as "AND"
4. TI = Processor Idle Status $\overline{\text{S2}}$, $\overline{\text{S1}}$, $\overline{\text{S0}}$ = 111
5. HLT = Processor Halt Status $\overline{\text{S2}}$, $\overline{\text{S1}}$, $\overline{\text{S0}}$ = 011

HARRIS

82C284/883

Clock Generator and Ready Interface for 80C286 Processors

June 1989

Features

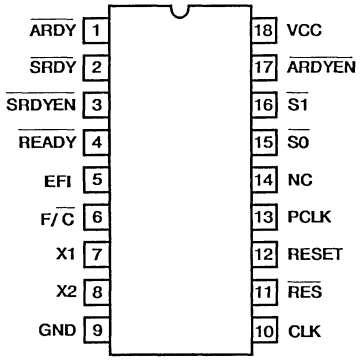
- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Generates System Clock for 80C286 Processors
- Generates System Reset Output from Schmitt Trigger Input
  - ▸ Improved Hysteresis
- Uses Crystal or External Signal for Frequency Source
  - ▸ Dynamically Switchable Between Two Input Frequencies
- Provides Local $\overline{\text{READY}}$ and MULTIBUS® $\overline{\text{READY}}$ Synchronization
- Static CMOS Technology
- Single +5V Power Supply
- Available in 18 Lead Cerdip Package

Description

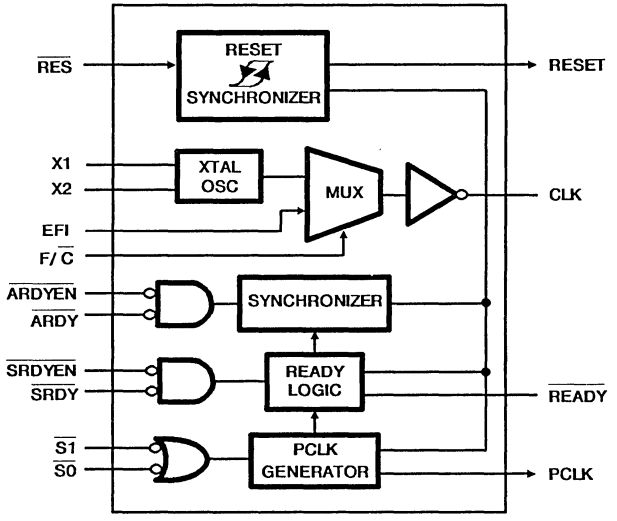
The Harris 82C284/883 is a clock generator/driver which provides clock signals for 80C286 processors and support components. It also contains logic to supply $\overline{\text{READY}}$ to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis.

Pinout

82C284/883 (CERAMIC DIP)
TOP VIEW



Functional Diagram



5 CMOS PERIPHERALS

Pin Description The following pin function descriptions are for the 82C284/883 clock generator.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
CLK	10	O	SYSTEM CLOCK: the signal used by the processor and support devices which must be synchronous with the processor. The frequency of the CLK output has twice the desired internal processor clock frequency. CLK can drive both TTL and CMOS CMOS level inputs.
F/$\overline{C}$	6	I	FREQUENCY/CRYSTAL SELECT: this pin selects the source for the CLK output. When there is a LOW level on this input, the internal crystal oscillator drives CLK. When there is a HIGH level on F/$\overline{C}$, the EFI input drives the CLK input. This pin can be dynamically switched, which allows changing the processor CLK frequency while running for low-power operation, etc.
X1, X2	7, 8	I	CRYSTAL IN: the pins to which a parallel resonant, fundamental mode crystal is attached for the internal oscilator. When F/$\overline{C}$ is LOW, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the desired internal processor clock frequency.
EFI	5	I	EXTERNAL FREQUENCY IN: drives CLK when the F/$\overline{C}$ input is HIGH. The EFI input frequency must be twice the desired internal processor clock frequency.
PCLK	13	O	PERIPHERAL CLOCK: the output which provides a 50% duty cycle clock with one-half the frequency of CLK. PCLK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
$\overline{\text{ARDYEN}}$	17	I	ASYNCHRONOUS READY ENABLE: an active LOW input which qualifies the $\overline{\text{ARDY}}$ input. $\overline{\text{ARDYEN}}$ selects $\overline{\text{ARDY}}$ as the source of $\overline{\text{READY}}$ for the current bus cycle. Inputs to $\overline{\text{ARDYEN}}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous outputs.
$\overline{\text{ARDY}}$	1	I	ASYNCHRONOUS READY: an active LOW input used to terminate the current bus cycle. The $\overline{\text{ARDY}}$ input is qualified by $\overline{\text{ARDYEN}}$. Inputs to $\overline{\text{ARDY}}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous outputs.
$\overline{\text{SRDYEN}}$	3	I	SYNCHRONOUS READY ENABLE: an active LOW input which qualifies $\overline{\text{SRDY}}$. $\overline{\text{SRDYEN}}$ selects $\overline{\text{SRDY}}$ as the source for $\overline{\text{READY}}$ to the CPU for the current bus cycle. Setup and hold time must be satisfied for proper operation.
$\overline{\text{SRDY}}$	2	I	SYNCHRONOUS READY: an active LOW input used to terminate the current bus cycle. The $\overline{\text{SRDY}}$ input is qualified by the $\overline{\text{SRDYEN}}$ input. Setup and hold time must be satisfied for proper operation.
$\overline{\text{READY}}$	4	O	READY: an active LOW output which signals to the processor that the current bus cycle is to be completed. The $\overline{\text{SRDY}}$, $\overline{\text{SRDYEN}}$, $\overline{\text{ARDY}}$, $\overline{\text{ARDYEN}}$, $\overline{\text{S1}}$, $\overline{\text{S0}}$, and $\overline{\text{RES}}$ inputs control $\overline{\text{READY}}$ as explained later in the $\overline{\text{READY}}$ generator section. $\overline{\text{READY}}$ is an open drain output requiring an external pull-up resistor.
$\overline{\text{S0}}$, $\overline{\text{S1}}$	15, 16	I	STATUS: these inputs prepare the 82C284/883 for a subsequent bus cycle. $\overline{\text{S0}}$ and $\overline{\text{S1}}$ synchronize PCLK to the internal processor clock and control $\overline{\text{READY}}$. Setup and hold times must be satisfied for proper operation.
RESET	12	O	RESET: an active HIGH output which is derived from the $\overline{\text{RES}}$ input. RESET is used to force the system into an initial state. When RESET is active, $\overline{\text{READY}}$ will be active (LOW).
$\overline{\text{RES}}$	11	I	RESET IN: an active LOW input which generates the system reset signal (RESET). Signals to $\overline{\text{RES}}$ may be applied asynchronously to CLK. A Schmitt trigger input is provided on $\overline{\text{RES}}$, so that an RC circuit can be used to provide a time delay. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
VCC	18		SYSTEM POWER: The +5V Power Supply Pin. A 0.1 µF capacitor between VCC and GND is recommended for decoupling.
GND	9		SYSTEM GROUND: 0V

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied ..... GND-0.1V to VCC+1.0V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 2

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	88.0°C/W	27.0°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 570mW
Gate Count ..... 200 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... +4.5V to +5.5V
EFI Rise Time (From 0.8V to 3.2V) ..... 8ns (Max)
EFI Fall Time (From 3.2V to 0.8V) ..... 8ns (Max)

TABLE 1. 82C284/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input LOW Voltage	VIL	VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.8	V
Input HIGH Voltage	VIH	VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.2	-	V
EFI, F/$\overline{C}$ Input High Volt.	VIHC	VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	3.2	-	V
$\overline{RES}$ HIGH Voltage	VIHR	VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC - 0.8	-	V
$\overline{RES}$ Input Hysteresis	VHYS	VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	0.5	-	V
RESET, PCLK Output LOW Voltage	VOL	IOL = 5mA, VCC = 4.5V, Note 2	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
RESET, PCLK Output Voltage	VOH	IOH = -1mA, VCC = 4.5V, Note 2	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC - 0.4	-	V
$\overline{READY}$ Output LOW Voltage	VOLR	IOH = 10mA, VCC = 4.5V, Note 2	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
CLK Output LOW Voltage	VOLC	IOL = 5mA, VCC = 4.5V, Note 2	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
CLK Output HIGH Voltage	VOHC	IOH = -5mA, VCC = 4.5V, Note 2	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC - 0.4	-	V
Input Leakage Current	II	VIN = GND or VCC, VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-10	10	µA
Active Power Supply Current	ICCOP	82C284-10/883, Note 1	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	48	mA
		82C284-12/883, Note 1	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	60	mA

NOTES: 1. ICCOP measured at 10MHz for the 82C284-10/883 and at 12.5MHz for the 82C284-12/883. VIN = GND or VCC, VCC = 5.5V, outputs unloaded.

2. Interchanging of force and sense conditions is permitted.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 2. 82C284/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. A.C. timings are referenced to 0.8V and 2.0V points of the signals as illustrated in datasheet waveforms, unless otherwise specified.

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	82C284/883				UNITS
					10MHz		12MHz		
					MIN	MAX	MIN	MAX	
EFI LOW Time	t1	At VCC/2, Note 8	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	16	-	ns
EFI HIGH Time	t2	At VCC/2, Note 8	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	20	-	ns
Status Setup Time for Status Going Active	t5A		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	18	-	ns
Status Setup Time for Status Going Inactive	t5B		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	16	-	ns
Status Hold Time	t6		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	1	-	1	-	ns
F/$\overline{C}$ Setup Time	t7		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	15	-	ns
F/$\overline{C}$ Hold Time	t8		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	15	-	ns
$\overline{SRDY}$ or $\overline{SRDYEN}$ Setup Time	t9		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	15	-	ns
$\overline{SRDY}$ or $\overline{SRDYEN}$ Hold Time	t10		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	2	-	2	-	ns
$\overline{ARDY}$ or $\overline{ARDYEN}$ Setup Time	t11	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	5	-	ns
$\overline{ARDY}$ or $\overline{ARDYEN}$ Hold Time	t12	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	25	-	ns
$\overline{RES}$ Setup Time	t13	Notes 3, 7	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	18	-	ns
$\overline{RES}$ Hold Time	t14	Notes 3, 7	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	8	-	ns
CLK Period	t16		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	40	-	ns
CLK LOW Period	t17	Notes 2, 6	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	12	-	11	-	ns
CLK HIGH Time	t18	Notes 2, 6	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	16	-	13	-	ns
$\overline{READY}$ Inactive Delay	t21	At 0.8V. Note 4, Test Condition 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	5	-	ns
$\overline{READY}$ Active Delay	t22	At 0.8V. Note 4,	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	24	-	18	ns
PCLK Delay	t23	CL = 75pF, Test Condition 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	20	-	16	ns
RESET Delay	t24	CL = 75pF, Test Condition 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	27	-	26	ns
PCLK LOW Time	t25	CL = 75pF, Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	t16-10	-	t16-10	-	ns
PCLK HIGH Time	t26	CL = 75pF, Note 5	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	t16-10	-	t16-10	-	ns

NOTES:
1. VCC = 4.5V and 5.5V unless otherwise specified. CLK loading: CL = 100pF.
2. With the internal crystal oscillator using recommended crystal and capacitive loading; or with the EFI input meeting specifications t1 and t2. The recommended crystal loading for CLK frequencies of 8MHz to 20MHz are 25pF from pin X1 to GND, and 15pF from pin X2 to GND; for CLK frequencies from 20MHz to 25MHz the recommended loading is 15pF from pin X1 to GND, and 15pF from pin X2 to GND. These recommended values are ±5pF and include all stray capacitance. Decouple VCC and GND as close to the 82C284/883 as possible.
3. This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at a specific CLK edge.
4. The pull-up resistor value for the $\overline{READY}$ pin is 620Ω with the rated 150pF load.
5. t16 refers to any allowable CLK period.
6. When using a crystal with the recommended capacitive loading, CLK output HIGH and LOW times are guaranteed to meet 80C286 requirements.
7. Measured from 1.0V on the CLK to 0.8V on the $\overline{RES}$ waveform for $\overline{RES}$ active, and to 4.2V on the $\overline{RES}$ waveform for $\overline{RES}$ inactive.
8. Input test waveform characteristics: VIL = 0.0V, VIH = 4.5V.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. 82C284/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	82C284/883				UNITS
					10MHz		12.5MHz		
					MIN	MAX	MIN	MAX	
Input Capacitance	CIN	FREQ = 1MHz, All measurements are referenced to device GND	1	$T_A = +25^oC$	-	10	-	10	pF
EFI HIGH to CLK LOW Delay	t15A		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	30	-	25	ns
EFI LOW to CLK HIGH Delay	t15B		1, 3	$-55^oC \leq T_A \leq +125^oC$	-	35	-	30	ns
CLK Rise Time	t19	1.0V to 3.6V, CL = 100pF	1	$-55^oC \leq T_A \leq +125^oC$	-	8	-	8	ns
CLK Fall Time	t20	3.6V to 1.0V, CL = 100pF	1	$-55^oC \leq T_A \leq +125^oC$	-	8	-	8	ns
X1 HIGH to CLK	t27		1, 4	$-55^oC \leq T_A \leq +125^oC$	-	35	-	30	ns

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. Measured from 3.2V on the EFI waveform to 1.0V on the CLK.
3. Measured from 0.8V on the EFI waveform to 3.6V on the CLK.
4. Measured from 3.6V on the X1 input to 3.6V on the CLK.

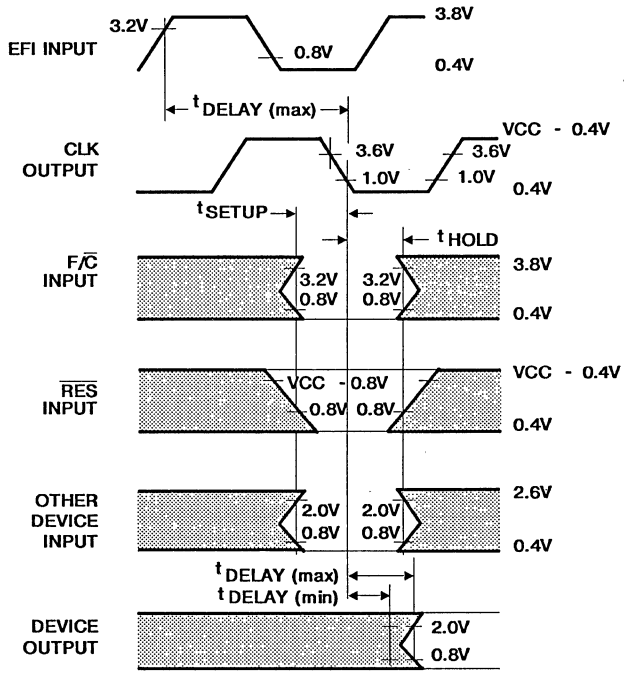
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

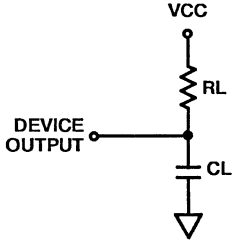
CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

A.C. Specifications (Continued)

A.C. DRIVE, SETUP, HOLD AND DELAY TIME MEASUREMENT POINTS



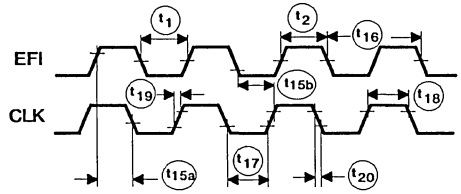
A.C. Test Condition



TEST CONDITION	RL	CL
1	750Ω	75pF
2	620Ω	150pF
3	∞	75pF

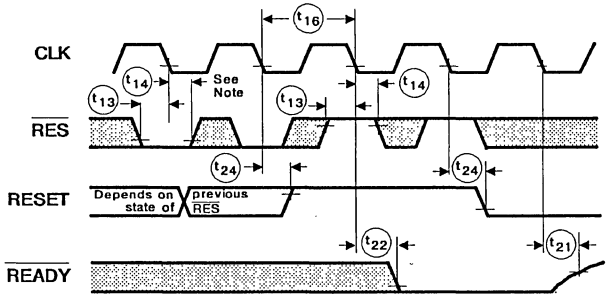
Waveforms

CLK AS A FUNCTION OF EFI



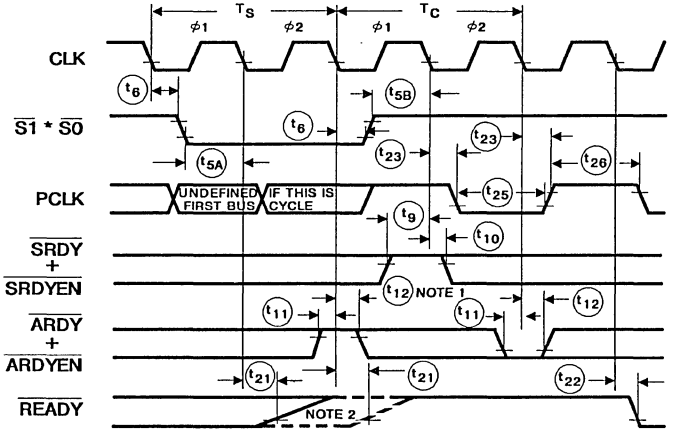
NOTE: The EFI input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.

RESET AND $\overline{\text{READY}}$ TIMING AS A FUNCTION OF $\overline{\text{RES}}$ WITH S1, $\overline{\text{S0}}$, $\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$, AND $\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ HIGH



NOTE: This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

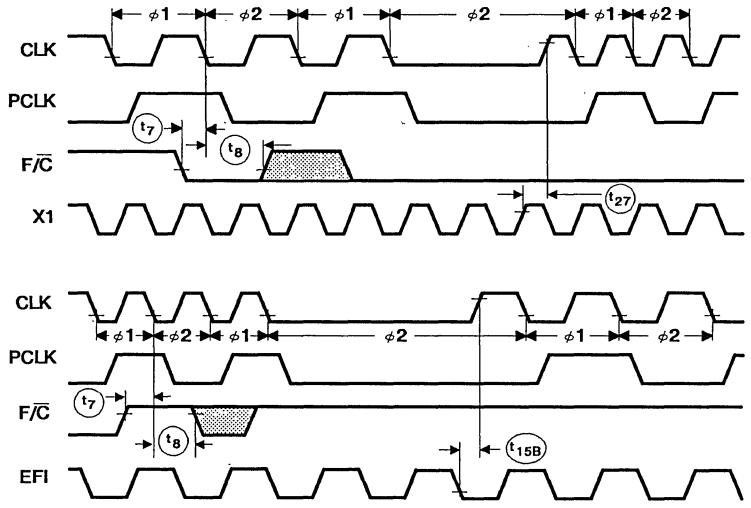
$\overline{\text{READY}}$ AND PCLK TIMING WITH $\overline{\text{RES}}$ HIGH



NOTES:
1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
2. If $\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ or $\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ are active before and/ or during the first bus cycle after RESET, $\overline{\text{READY}}$ may not be deasserted until the falling edge of φ2 of T_S.

Waveforms (Continued)

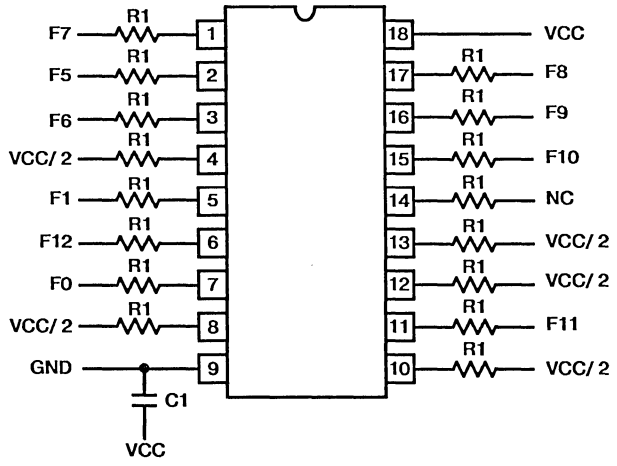
CLK AS A FUNCTION OF F/$\overline{C}$, PCLK, X1, AND EFI
DURING DYNAMIC FREQUENCY SWITCHING



NOTE: This is an asynchronous input. The setup and hold times are required to guarantee the response shown.

Burn-In Circuit

18 PIN CERAMIC DIP



NOTES:
1. Supply Voltage: VCC = 5.5V, ±0.5V, GND = 0V
   Driver Voltage: VIH = 4.5V ± 10%, VIL = 0V
2. Input Voltage Limits: VIL (Max) = 0.4V,
   VIH (Min) = 2.6V
3. Component Values: R1 = 47kΩ
   C1 = 0.1μF (Min)
4. Oven type and frequency requirements microtest, F0 through F12
5. Approximate current per unit. ICC = 0.3mA
6. Special requirements:
   (a) *Electrostatic Discharge Sensitive.* Proper precautions must be used when handling units.
   (b) All power supplies must be at zero volts when the boards are inserted into the ovens. After insertion, apply VCC first, then activate the driver power supplies.
7. Oscilloscope measurements: To be on loaded boards before insertion into the oven.

Metallization Topology

DIE DIMENSIONS:
63 x 69 x 19 ± 1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

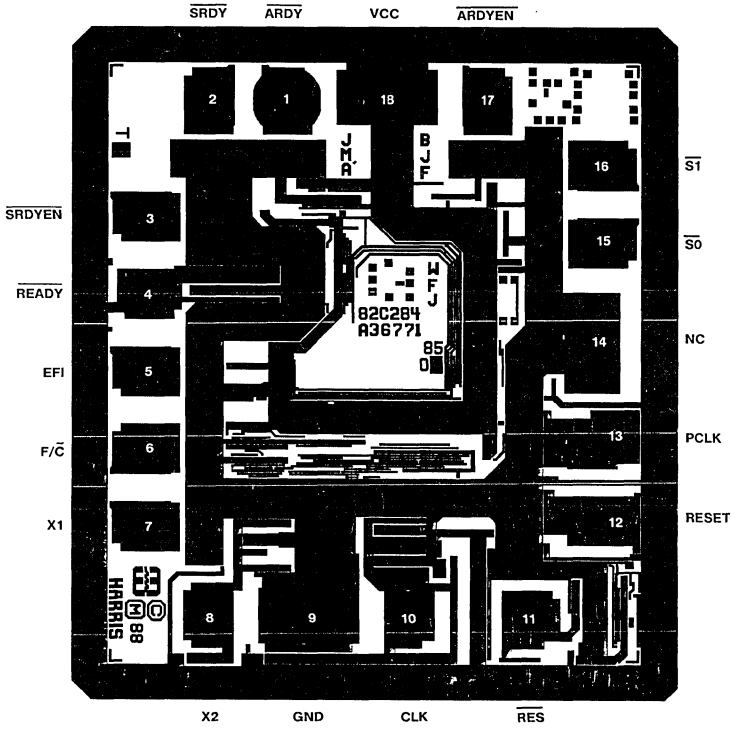
DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
2×10^5 A/cm^2

LEAD TEMPERATURE (10 Seconds Soldering): ≤ 300°C

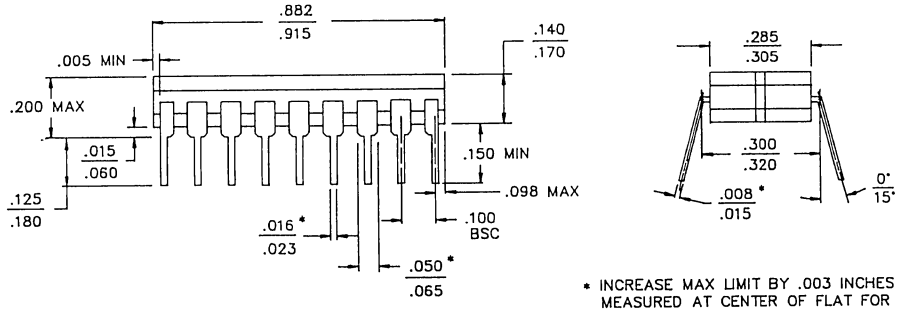
Metallization Mask Layout

82C284/883



Packaging†

18 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-6

5 CMOS PERIPHERALS

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Functional Description

INTRODUCTION

The 82C284 generates the clock, ready, and reset signals required for 80C286 processors and support components. The 82C284 is packaged in an 18 pin DIP and contains a crystal controlled oscillator, clock generator, peripheral clock generator, MULTIBUS® ready synchronization logic, and system reset generation logic.

CLOCK GENERATOR

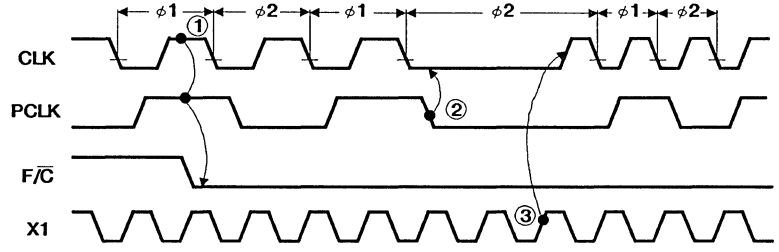
The CLK output provides the basic timing control for an 80C286 system. CLK has output characteristics sufficient to drive CMOS devices. CLK is generated by either an internal crystal oscillator, or an external source as selected by the F/$\overline{C}$ input pin. When F/$\overline{C}$ is LOW, the crystal oscillator drives the CLK output. When F/$\overline{C}$ is HIGH, the EFI input drives the CLK output.

The F/$\overline{C}$ pin on the Harris 82C284 is dynamically switchable. This allows the CLK frequency to the processor to be changed from one frequency to another in a running system. With this feature, a system can be designed which operates at maximum speed when needed, and then dynamically switched to a lower frequency to implement a low-power mode. The lower frequency can be anything down to, but excluding, D.C. The following 3 conditions apply when dynamically switching the F/$\overline{C}$ pin (see Figure 1):

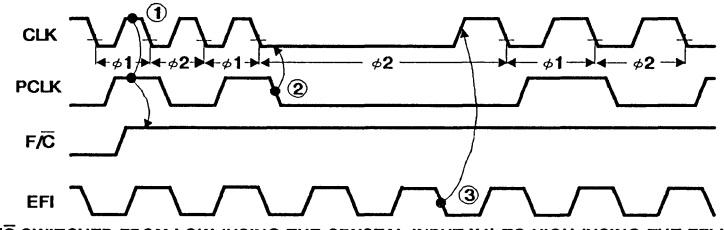
1) The CLK is stretched in the low portion of the $\phi 2$ phase of it's cycle during transition from one CLK frequency to the other (see Waveforms).
2) When switching CLK frequency sources, there is a maximum transition latency of 2.5 clock cycles of the frequency being switched to, from the time CLK freezes low, until CLK restarts at the new frequency (see Waveforms).
3) The maximum latency from the time F/$\overline{C}$ is dynamically switched, to the time CLK freezes low, is 4 CLK cycles (see Waveforms).

The following steps describe the sequence of events that transpire when F/$\overline{C}$ is dynamically switched:

(A) F/$\overline{C}$ switched from high (using EFI input) to low (using the crystal input X1 - see Figure 1A).
1) The state of F/$\overline{C}$ is sampled when both CLK and PCLK are high until a change is detected.
2) On the second following falling edge of PCLK, CLK is frozen low.
3) CLK restarts at the crystal frequency on the rising edge of X1, after the second falling edge of X1.



(A) F/$\overline{C}$ SWITCHED FROM HIGH (USING EFI INPUT) TO LOW (USING THE CRYSTAL INPUT X1)



(B) F/$\overline{C}$ SWITCHED FROM LOW (USING THE CRYSTAL INPUT X1) TO HIGH (USING THE EFI INPUT)

FIGURE 1. DYNAMICALLY SWITCHING THE F/$\overline{C}$ PIN

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

(B) F/$\overline{C}$ switched from low (using the crystal input X1) to high (using the EFI input - see Figure 1B).

1) The state of F/$\overline{C}$ is sampled when both CLK and PCLK are high until a change is detected.
2) On the second following falling edge of PCLK, CLK is frozen low.
3) CLK restarts at the EFI input frequency on the falling edge of EFI after the second rising edge of EFI.

The 82C284 provides a second clock output, PCLK, for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and CMOS output drive characteristics. PCLK is normally synchronized to the internal processor clock.

After reset, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S1}$ and $\overline{S0}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its HIGH time beyond one system clock (see Waveforms). PCLK is forced HIGH whenever either $\overline{S0}$ or $\overline{S1}$ were active (LOW) for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are HIGH.

Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

OSCILLATOR

The oscillator circuit of the 82C284 is a linear Pierce oscillator which requires an external parallel resonant, fundamental mode, crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32pF.

X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in Table A. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10pF between the X1 and X2 pins. Decouple VCC and GND as close to the 82C284 as possible with a 0.1µF polycarbonate capacitor.

TABLE A. 82C284 CRYSTAL LOADING CAPACITANCE VALUES

CRYSTAL FREQUENCY	C1 CAPACITANCE (PIN 7)	C2 CAPACITANCE (PIN 8)
1 to 8MHz	60pF	40pF
8 to 20MHz	25pF	15pF
20 to 25MHz	15pF	15pF

CLK TERMINATION

Due to the CLK output having a very fast rise and fall time, it is recommended to properly terminate the CLK line at frequencies above 10MHz to avoid signal reflections and ringing. Termination is accomplished by inserting a small resistor (typically 10-74Ω) in series with the output, as shown in Figure 2. This is known as series termination. The resistor value plus the circuit output impedance (approximately 25Ω) should be made equal to the impedance of the transmission line.

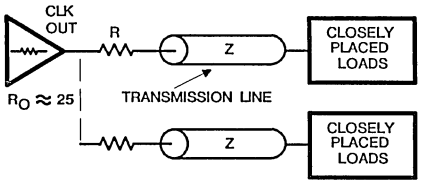


FIGURE 2. SERIES TERMINATION

RESET OPERATION

The reset logic provides the RESET output to force the system into a known, initial state. When the $\overline{RES}$ input is active (LOW), the RESET output becomes active (HIGH). $\overline{RES}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see Waveforms). Synchronization of the $\overline{RES}$ input introduces a one or two CLK delay before affecting the RESET Output.

At power up, a system does not have a stable VCC and CLK. To prevent spurious activity, $\overline{RES}$ should be asserted until VCC and CLK stabilize at their operating values. 80C286 processors and support components also require their RESET inputs be HIGH a minimum of 16 CLK cycles. An RC network, as shown in Figure 3, will keep $\overline{RES}$ LOW long enough to satisfy both needs.

A Schmitt trigger input with hysteresis on $\overline{RES}$ assures a single transition of RESET with an RC circuit on $\overline{RES}$. The hysteresis separates the input voltage level at which the circuit output switches from HIGH to LOW from the input voltage level at which the circuit output switches from LOW to HIGH. The $\overline{RES}$ HIGH to LOW input transition voltage is lower than the $\overline{RES}$ LOW to HIGH input transition voltage.

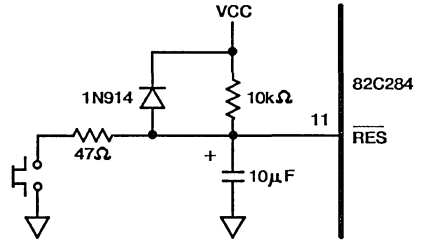


FIGURE 3. TYPICAL RC $\overline{RES}$ TIMING CIRCUIT

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

As long as the slope of the $\overline{RES}$ input voltage remains in the same direction (increasing or decreasing) around the $\overline{RES}$ input transition voltage, the RESET output will make a single transition.

READY OPERATION

The 82C284 accepts two ready sources for the system ready signal which terminates the current bus cycle. Either a synchronous ($\overline{SRDY}$) or asynchronous ready ($\overline{ARDY}$) source may be used. Each ready input has an enable ($\overline{SRDYEN}$ and $\overline{ARDYEN}$) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

$\overline{READY}$ is enabled (LOW), if either $\overline{SRDY}$ + $\overline{SRDYEN}$ = 0 or $\overline{ARDY}$ + $\overline{ARDYEN}$ = 0 when sampled by the 82C284 READY generation logic. $\overline{READY}$ will remain active for at least two CLK cycles.

The $\overline{READY}$ output has an open-drain driver allowing other ready circuits to be wire or'ed with it, as shown in Figure 4. The $\overline{READY}$ signal of an 80C286 system requires an external pull-up resistor. To force the $\overline{READY}$ signal inactive (HIGH) at the start of a bus cycle, the $\overline{READY}$ output floats when either $\overline{S1}$ or $\overline{S0}$ are sampled LOW at the falling edge of CLK. Two system clock periods are allowed for the pull-up resistor to pull the $\overline{READY}$ signal to VIH. When RESET is active, $\overline{READY}$ is forced active one CLK later (see Waveforms).

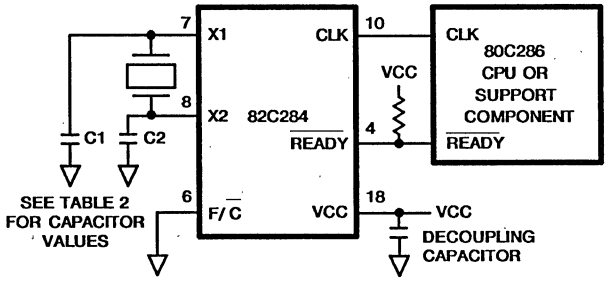


FIGURE 4. RECOMMENDED CRYSTAL AND READY CONDITIONS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Figure 5 illustrates the operation of $\overline{SRDY}$ and $\overline{SRDYEN}$. These inputs are sampled on the falling edge of CLK when $\overline{S1}$ and $\overline{S0}$ are inactive and PCLK is HIGH. $\overline{READY}$ is forced active when both $\overline{SRDY}$ and $\overline{SRDYEN}$ are sampled as LOW..

Figure 6 shows the operation of $\overline{ARDY}$ and $\overline{ARDYEN}$. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is HIGH. If the synchronizer resolved both the $\overline{ARDY}$ and $\overline{ARDYEN}$ as active, the $\overline{SRDY}$ and $\overline{SRDYEN}$ inputs are ignored. Either $\overline{ARDY}$ or $\overline{ARDYEN}$ must be HIGH at the end of T_S, therefore at least one wait state is required when using the $\overline{ARDY}$ and $\overline{ARDYEN}$ inputs as a basis for generating $\overline{READY}$.

$\overline{READY}$ remains active until either $\overline{S1}$ or $\overline{S0}$ are sampled LOW, or the ready inputs are sampled as inactive.

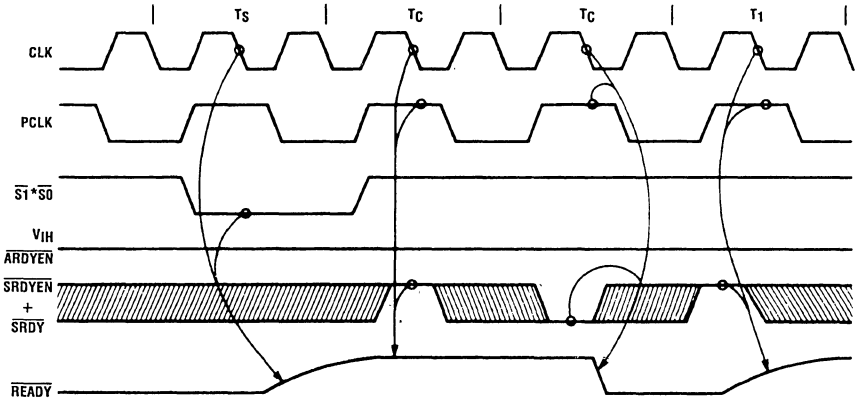


FIGURE 5. SYNCHRONOUS READY OPERATION

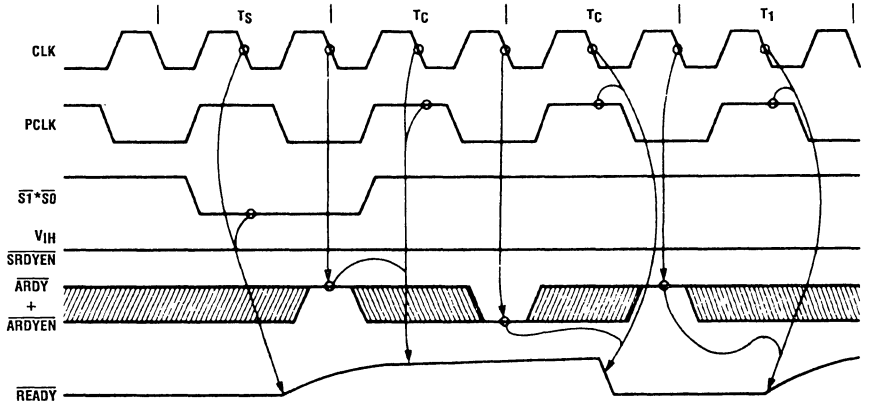


FIGURE 6. ASYNCHRONOUS READY OPERATION

HARRIS

82C288/883

June 1989

Bus Controller For 80C286 Processors

Features

- Compatible with NMOS 82288
- Fully Static CMOS Design for Low Power Operation
  - ICCSB = 10μA Maximum
  - ICCOP = 1mA/MHz
- Provides Commands and Control for Local and System Bus
- Flexible Command Timing
- Optional MULTIBUS™ Compatible Timing
- Control Drivers with 16mA IOL and 3-State Command Drivers with 32mA IOL
- Single +5V Supply
- Available in 20 Pin Cerdip Package

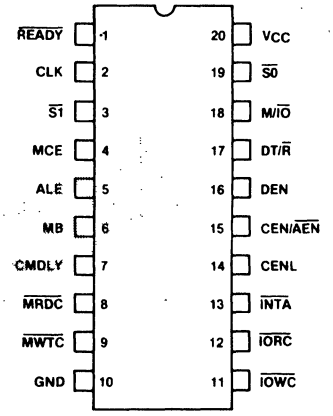
Description

The Harris 82C288/883 Bus Controller is a 20 pin CMOS component for use in 80C286 microsystems. The Bus Controller provides command and control outputs with flexible timing options. Separate command outputs are used for memory and I/O devices. The data bus is controlled with separate data enable and direction control signals.

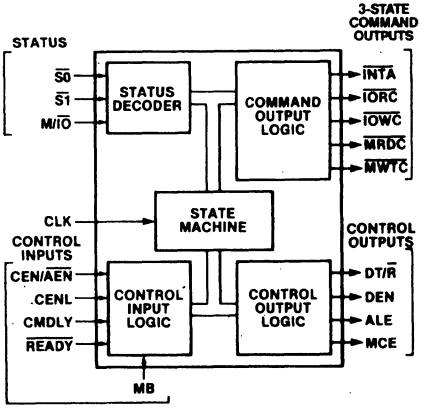
Two modes of operation are possible via a strapping option: MULTIBUS compatible bus cycles, and high speed bus cycles.

Pinout

20 PIN CERAMIC DIP
TOP VIEW



Functional Diagram



MULTIBUS™ is an Intel Corporation Trademark

Harris Semiconductor

APPNOTE

No. 109 June 1989

Harris Microprocessor

82C59A PRIORITY INTERRUPT CONTROLLER

Author: J. A. Goss

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

82C59A CMOS PROGRAMMABLE INTERRUPT CONTROLLER

By J. A. Goss

Introduction

The Harris 82C59A is a CMOS Priority Interrupt Controller, designed to relieve the system CPU from the task of polling in a multi-level priority interrupt system. The 82C59A is compatible with microprocessors such as the 80C86, 80C88, 8086, 8088, 8080/85 and NSC800.

In the following discussion, we will look at the initialization and operation process for the 82C59A. We will focus our attention on 80C86/80C88-based systems. However, the information presented will also be applicable to use of the 82C59A in 8080 or 8085-based systems as well.

Let us look at the sequence of events that occur with the 82C59A during an interrupt request and service. In an 8080/85 based system:

(1) One or more of the INTERRUPT REQUEST lines (IR0 - IR7) are raised high, setting the corresponding bits in the Interrupt Request Register (IRR).

(2) The interrupt is evaluated in the priority resolver. If appropriate, an interrupt is sent to the CPU via the INT line (pin 17).

(3) The CPU acknowledges the interrupt by sending a pulse on the $\overline{\text{INTA}}$ line. Upon reception of this pulse, the 82C59A responds by forcing the opcode for a call instruction (0CDH) onto the data bus.

(4) A second $\overline{\text{INTA}}$ pulse is sent from the CPU. At this time, the device will respond by placing the lower byte of the address of the appropriate service routine onto the data bus. This address is derived from ICW1.

(5) A final (third) pulse of $\overline{\text{INTA}}$ occurs, and the 82C59A responds by placing the upper byte of the address onto the data bus. This address is taken from ICW2.

(6) The three byte call instruction is then complete. If the AEOI mode has been chosen, the bit set during the first $\overline{\text{INTA}}$ pulse in the ISR is reset at the end of the third $\overline{\text{INTA}}$ pulse. Otherwise, it will not get reset until an appropriate EOI command is issued to the 82C59A.

For 80C86- and 80C88-based systems:

(1) and (2) same as above.

(3) The CPU responds to the interrupt request by pulsing the $\overline{\text{INTA}}$ line twice. The first pulse sets the appropriate ISR bit and resets the IRR bit while the second pulse causes the interrupt vector to be placed on the data bus. This byte is composed of the interrupt number in bits 0 through 2, and bits 3 through 7 are taken from bits 3 - 7 of ICW2.

(4) The interrupt sequence is complete. If using the AEOI mode, the bit set earlier in the ISR will be reset. Otherwise, the interrupt controller will await an appropriate EOI command at the end of the interrupt service routine.

1.0 Glossary of Terms for the 82C59A

1.1 Automatic End of Interrupt (AEOI):

When the 82C59A is programmed to operate in the Automatic EOI mode, the device will produce its own End-of-Interrupt (EOI) at the trailing edge of the last Interrupt Acknowledge pulse ($\overline{\text{INTA}}$) from the CPU. Using this mode of operation frees the software (service routines) from needing to send an EOI manually to the 82C59A.

However, using the Automatic EOI mode will upset the priority structure of the 82C59A. When the AEOI is generated, the bit that was set in the In-Service Register (ISR) to indicate which interrupt is being serviced, will be cleared. Because of this, while an interrupt is being serviced there will be no record in the ISR that it is being serviced. Unless interrupts are disabled by the CPU, there is a risk that interrupt requests of lower or equal priority will interrupt the current request being serviced. If this mode of operation is not desired, interrupts should not be re-enabled by the CPU when executing interrupt service routines.

1.2 Automatic Rotation:

During normal operation of the 82C59A, we have an assigned order of priorities for the IR lines. There are however, instances when it might be useful to assign equal priorities to all interrupts. Once a particular interrupt has been serviced, all other equal priority interrupts should have an opportunity to be serviced before the original peripheral can be serviced again. This priority equalization can be achieved through Automatic Rotation of priorities.

Assume, for example, that the assigned priorities of interrupts has IR0 as the highest priority interrupt and IR7 as the lowest. Figure 1A shows interrupt requests occuring on IR7 as well as IR3. Because IR3 is of higher priority, it will be serviced first. Upon completion of the servicing of IR3, rotation occurs and IR3 then becomes the lowest priority interrupt. IR4 will now have the highest priority (see Figure 1B).

There are two methods in which Automatic Rotation can be implemented. First, if the 82C59A is operating in the AEOI mode as described above, the 82C59A can be programmed for "Rotate in Automatic EOI mode". This is done by writing a command word to OCW2. The second method occurs when using normal EOIs. When an EOI is issued by the service routine, the software can specify that rotation be performed.

	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
IRR STATUS	1	0	0	0	1	0	0	0
PRIORITY	7	6	5	4	3	2	1	0

LOWEST PRIORITY — HIGHEST PRIORITY

FIGURE 1A. IR PRIORITIES (BEFORE ROTATION)

	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
ISR STATUS	1	0	0	0	0	0	0	0
PRIORITY	3	2	1	0	7	6	5	4

HIGHEST PRIORITY — LOWEST PRIORITY

FIGURE 1B. IR PRIORITIES (AFTER ROTATION)

1.3 Buffered Mode:

When using the 82C59A in a large system, it may be necessary to use bus buffers to guarantee data integrity and guard against bus contention.

By selecting buffered mode when initializing the device, the $\overline{SP}/\overline{EN}$ pin (pin 16) will generate an enable signal for the buffers whenever the data outputs from the 82C59A are active. In this mode, the dual function $\overline{SP}/\overline{EN}$ pin can no longer be used for specifying whether a particular 82C59A is being used as a master or a slave in the system. This specification must be made through setting the proper bit in ICW4 during the device initialization.

1.4 Cascade Mode:

More than one 82C59A can be used in a system to expand the number of priority interrupts to a maximum of 64 levels without adding any additional hardware. This method of expansion is known as "cascading". An example of cascading 82C59As is shown in Figure 2.

In a cascaded interrupt scheme, a single 82C59A is utilized as the "master" interrupt controller. As many as 8 "slave" 82C59As can be connected to the IR inputs of the "master" 82C59A. Each of these slaves can support up to 8 interrupt inputs, yielding 64 possible prioritized interrupts.

When in cascade mode, the determination of whether a device is a master or a slave can take either of two forms. The state of the $\overline{SP}/\overline{EN}$ pin will select "master" or "slave" mode for a device when the buffered mode is not being used. Should buffered mode be used, then it is necessary that bit D2 (M/S) of ICW4 be set to indicate if the particular 82C59A is being used as a "master" or "slave" interrupt controller in the system.

The CAS0-2 pins on the interrupt controllers serve to provide a private bus for the cascaded 82C59As. These lines allow the "master" to inform the slaves which is to be serviced for a particular interrupt.

1.5 End of Interrupt (EOI):

When an interrupt is recognized and acknowledged by the CPU, its corresponding bit will be set in the In-Service Register (ISR). If the AEOI mode is in use, the bit will be cleared automatically through the interrupt acknowledge signal from the CPU. However, if AEOI is not in effect, it is the task of software to notify the 82C59A when servicing of an interrupt is completed. This is done by issuing an End-of-Interrupt (EOI).

There are 2 different types of EOIs that can be issued to the device; non-specific EOI and specific EOI. In most cases, when the device is operating in a mode that does not disturb the fully nested mode such as Special Fully Nested Mode, we will issue a non-specific EOI. This form of the EOI will automatically reset the highest priority bit set in the ISR. This is because for full nested operation, the highest priority IS bit set is the last interrupt level acknowledged and serviced.

The "specific" EOI is used when the fully nested structure has not been preserved. The 82C59A may not be able to determine the last level acknowledged. Thus, the software must specify which interrupt level is to be reset. This is done by issuing a "specific" EOI.

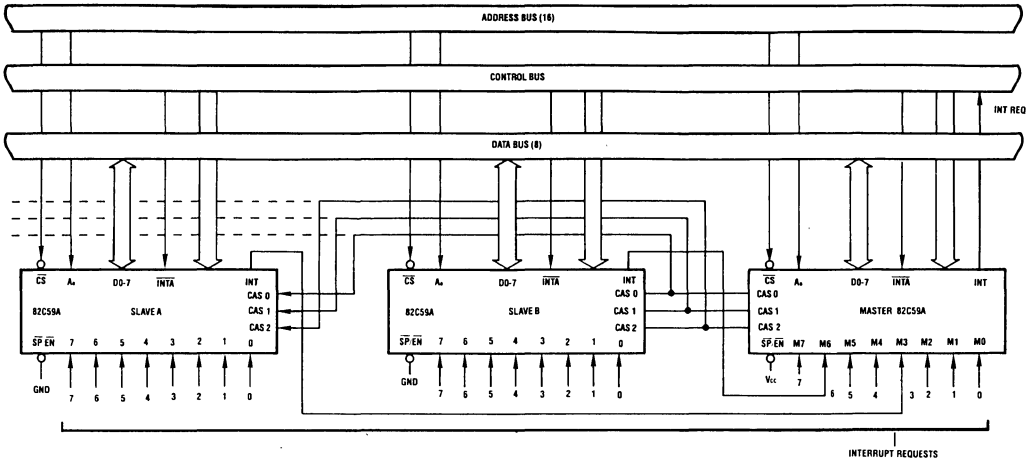


FIGURE 2. CASCADING THE 82C59A

1.6 Fully Nested Mode:

By default, the 82C59A operates in the Fully Nested Mode. It will remain in this mode until it is programmed otherwise. In the Fully Nested Mode, interrupts are ordered by priority from highest to lowest. Initially, the highest priority level is IR0 with IR7 having the lowest. This ordering can be changed through the use of priority rotation (see 1.2).

In the Fully Nested Mode, when an interrupt occurs, its corresponding bit will get set in the Interrupt Request Register (IRR). When the processor acknowledges the interrupt, the 82C59A will look to the IRR to determine the highest priority interrupt requesting service. The bit in the In-service Register (ISR) corresponding to this interrupt will then be set. This bit remains set until an EOI is sent to the 82C59A.

While an interrupt is being serviced, only higher priority interrupts will be allowed to interrupt the current interrupt being serviced. However, lower priority interrupts can be allowed to interrupt higher priority requests if the 82C59A is programmed for operation in the Special Mask Mode.

When using the 82C59A in an 80C86- or 80C88-based system, interrupts will automatically be disabled when the processor begins servicing an interrupt request. The current address and the state of the flags in the processor will be pushed onto the stack. The interrupt-enable flag is then cleared. To allow interrupts to occur at this point, the STI instruction can be used. Upon exiting the service routine using the IRET instruction, execution of the program is resumed at the point where the interrupt occured, and the flags are restored to their original values, thus re-enabling interrupts.

A configuration in which the Fully Nested structure is not preserved occurs when one or more of the following conditions occur:

(a) The Automatic EOI mode is being used.

(b) The Special Mask Mode is in use.

(c) A slave 82C59A has a master that is not programmed to the Special Fully Nested Mode.

Cases (a) and (b) differ from case (c) in that the 82C59A would allow lower priority interrupt requests the opportunity to be serviced before higher priority interrupt requests.

1.7 Master:

When using multiple 82C59As in a system, one 82C59A has control over all other 82C59As. This is known as the "master" interrupt controller. Communication between the master and the other (slave) 82C59As occurs via the CAS0 - 2 lines. These lines form a private bus between the multiple 82C59As. Also, the INT lines from the slaves are routed to the master's IR input pin(s). See Figure 2.

1.8 Slave:

A "slave" 82C59A in a system is controlled by a master 82C59A. There is but one "master" in the system, but there can be up to 8 slave 82C59As. The INT outputs from the slaves act as inputs to the master through it's IR inputs. Communications between the master and slaves occurs via the CAS0 - 2 lines. See Figure 2.

1.9 Special Fully Nested Mode:

The Special Fully Nested Mode (SFNM) is used in a system having multiple 82C59As where it is necessary to preserve the priority of interrupts within a slave 82C59A. Only the master is programmed for the Special Fully Nested Mode through ICW4. This mode is similar to the Fully Nested Mode with the following exceptions:

(a) When an interrupt from a particular slave is being serviced, additional higher priority interrupts from that slave can cause an interrupt to the master. Normally, a slave is masked out when its request is in service.

(b) When exiting the Interrupt Service routine, the software should first issue a non-specific EOI to the slave. The In-service Register (ISR) should then be read and checked to see if its contents are zero. If the register is empty, the software should then write a non-specific EOI to the master. Otherwise, a second EOI need not be written because there are interrupts from that slave still being processed.

NOTE: Because the Master 82C59A and its slave 82C59As must be in Fully Nested Mode for this mode to be functional, we could not utilize Automatic EOIs. These would disturb the Fully Nested structure, as described in section 1.6.

1.10 Special Mask Mode:

The Special Mask Mode is utilized in order to allow interrupts from all other levels (higher and lower as well) to interrupt the IR level that is currently being serviced. Invoking this mode of operation will disturb the fully nested priority structure.

Generally, the Special Mask Mode is selected during the servicing of an interrupt. The software should first set the bit corresponding to the IR level being serviced, in the Interrupt Mask Register (OCW1). The Special Mask Mode and interrupts should then be enabled. This will allow any of the IR levels except for those masked off by OCW1 to interrupt the IR level currently being serviced.

Because this disturbs the Fully Nested Structure, it is required that a Specific EOI be issued when servicing interrupts while the Special Mask Mode is in effect. Before exiting the original interrupt routine, the Special Mask Mode should be disabled.

1.11 Specific Rotation:

By issuing the proper command word to OCW2, the priority structure of the 82C59A can be dynamically altered. The command word written to OCW2 would specify which is to be the lowest priority IR level.

This specific rotation can be accomplished one of two ways. The first is through a specific EOI. The software can specify that rotation is to be applied to the IR level provided with the EOI. The second method is a simple "set priority" command, in which the lowest priority level is specified with the command word.

2.0 Initialization Control Words

The following section gives a description of the Initialization Control Words (ICW) used for configuring the 82C59A Interrupt controller. There are four (4) control words used for initialization of the 82C59A. These ICWs must be programmed in the proper sequence beginning with ICW1. If at any time during the course of operation the configuration of the 82C59A needs to be changed, the user must again write out the control words to the device in their proper order. The initialization sequence is shown in Figure 3.

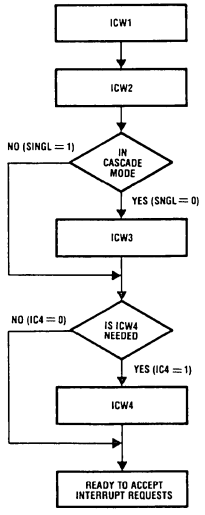


FIGURE 3. 82C59A INITIALIZATION SEQUENCE

ICW1: The 82C59A recognizes the first Initialization Control Word (ICW) written to it based on two criteria: (1) the A0 line from the address bus must be a zero, and (2) the D4 bit must be a one. If the D4 bit is set to a zero, we would be programming either OCW2 or OCW3 (these are explained later). The function of ICW1 is to tell the 82C59A how it is being used in the system (i.e. Single or cascaded, edge or level triggered interrupts etc.).

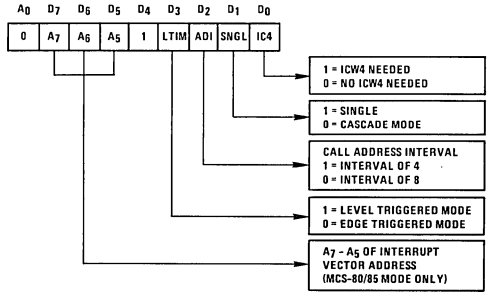
ICW2: This control word is always issued directly after ICW1. When addressing this ICW, the A0 line from the address bus must be a one (high). ICW2 is utilized in providing the CPU with information on where to vector to in memory when servicing an interrupt.

ICW3: This control word is issued only if the SNGL (D1) bit of ICW1 has been programmed with a zero. When addressing this word, the A0 line from the CPU must be high (1). This control word is for cascaded 82C59A's. It allows the master and slave 82C59As to communicate via the CAS0-2 lines. With the master, this word indicates which IR lines have slaves connected to them. For the slave 82C59A(s), this word indicates to which IR line on the master it is connected.

ICW4: Issuance of this ICW is selectable through the IC4 (D0) bit of ICW4. If ICW4 is to be written to the 82C59A, A0 from the CPU must be high (1) when writing to it. This word needs to be written only when the 82C59A is operating in modes other than the default modes. Instances when we would want to write to ICW4 are one or more of the following: An 80C86(80C88) processor is being used, buffered outputs (D0-D7) are to be used, Automatic EOIs are desired, or the Special Fully Nested mode is to be used.

2.1 ICW1:

ICW1 is the first control word that is written to the 82C59A during the initialization process. To access this word, the value of A0 must be a zero (0) in the addressing, and bit D4 of ICW1 must be a one (1). The format of the command word is as follows:



* NOTE: This is an address bit, and not part of the ICW.

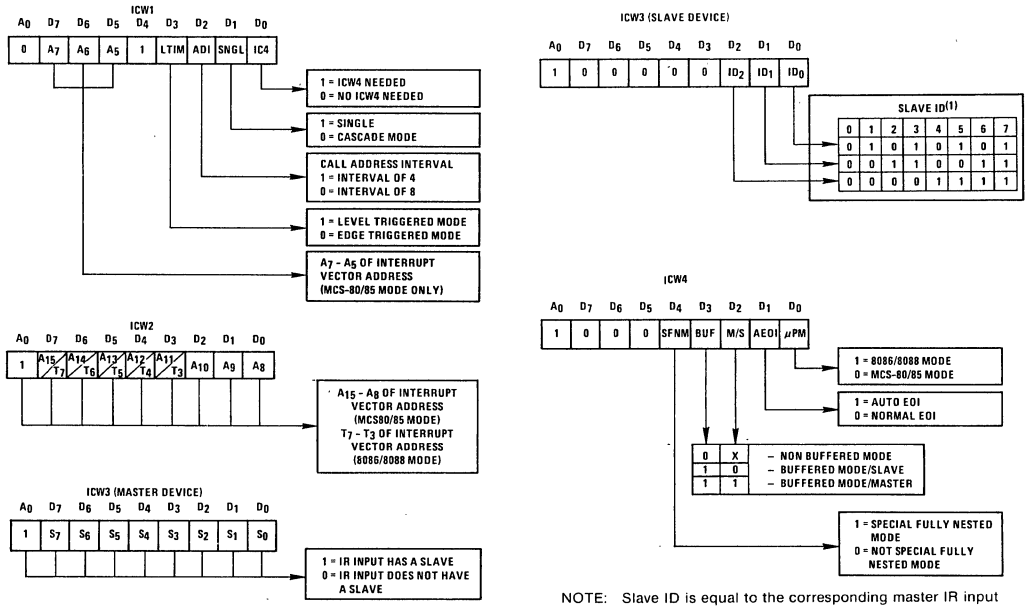
FIGURE 4. ICW1 FORMAT

D7 thru D5 - A7, A6, A5: These bits are used in the 8080/85 mode to form a portion of the low byte call address. When using the 4 byte address interval, all 3 bits are utilized. When using the 8 byte interval, only bits A7 and A6 are used. Bit A5 becomes a "don't care" bit. If using an 80C86(80C88) system, the value of these bits can be set to either a one or zero.

D3 - LTIM:

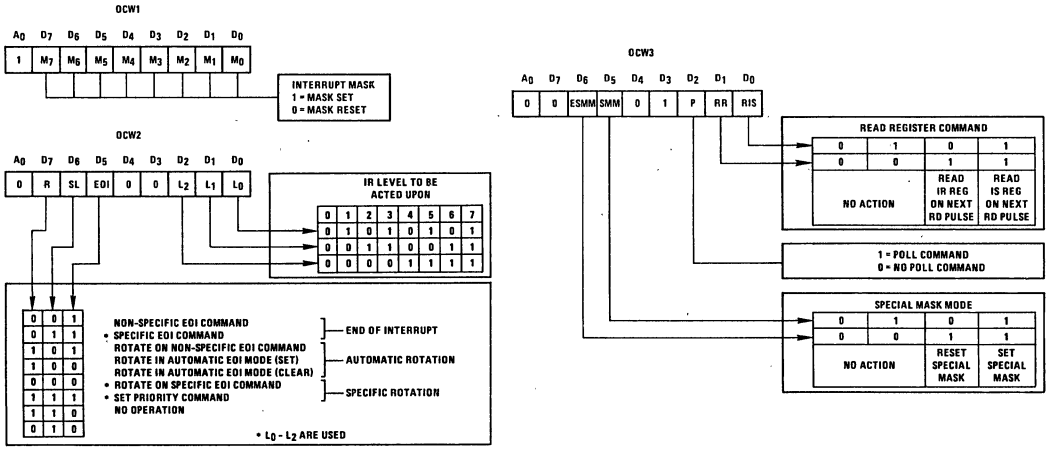
0: The 82C59A will operate in an edge triggered mode. An interrupt request on one of the IR lines (IR0 - IR7) is recognized by a low to high transition on the pin. The IR signal must remain high at least until the falling edge of the first sINTA pulse. Subsequent interrupts on the IR pin(s) will not occur until another low-to-high transition occurs.

1: Sets up the 82C59A to operate in the level triggered mode. Interrupts occur when a "high" level is detected on one or more of the IR pins. The interrupt request must be removed from this pin before the EOI command is issued by the CPU. Otherwise, the 82C59A will see the IR line still in a high state, and consider this to be another interrupt request.



NOTE: Slave ID is equal to the corresponding master IR input

82C59A INITIALIZATION COMMAND WORD FORMAT



82C59A OPERATION COMMAND WORD FORMAT

D2 - ADI: Call Address Interval (for 8080/8085 use only). If using the 82C59A in an 80C86/88 based system, the value of this bit can be either a 0 or a 1.

0 : The address interval generated by the 82C59A is 8 bytes. This option provides compatiblity with the RST interrupt vectoring in 8080/8085 systems since the vector locations are 8 bytes apart. This vector will be combined with the values specified in bits D7 and D6 of ICW1. The addresses generated are shown in Table 1.

TABLE 1. ADDRESS INTERVAL (8 BYTES)

D7	D6	D5	D4	D3	D2	D1	D0	
A7	A6	1	1	1	0	0	0	IR7
A7	A6	1	1	0	0	0	0	IR6
A7	A6	1	0	1	0	0	0	IR5
A7	A6	1	0	0	0	0	0	IR4
A7	A6	0	1	1	0	0	0	IR3
A7	A6	0	1	0	0	0	0	IR2
A7	A6	0	0	1	0	0	0	IR1
A7	A6	0	0	0	0	0	0	IR0

1 : The address interval generated by the interrupt controller will be 4 bytes. This provides the user with a compact jump table for 8080/8085 systems. The interrupt number is effectively multiplied by four and combined with bits D7, D6 and D5 to form the lower byte of the call instruction generated and sent to the 8080 or 8085. Table 2 shows how these addresses are generated for the various Interrupt request (IR) levels.

TABLE 2. ADDRESS INTERVAL (4 BYTES)

D7	D6	D5	D4	D3	D2	D2	D0	
A7	A6	A5	1	1	1	0	0	IR7
A7	A6	A5	1	1	0	0	0	IR6
A7	A6	A5	1	0	1	0	0	IR5
A7	A6	A5	1	0	0	0	0	IR4
A7	A6	A5	0	1	1	0	0	IR3
A7	A6	A5	0	1	0	0	0	IR2
A7	A6	A5	0	0	1	0	0	IR1
A7	A6	A5	0	0	0	0	0	IR0

D1 - SNGL:

0 : This tells the 82C59A that more than one 82C59A is being used in the system, and it should expect to receive ICW3 following ICW2. How the particular 82C59A is being used in the system will be determined either through ICW4 for buffered mode, or through the $\overline{SP}/\overline{EN}$ pin for non-buffered mode operation.

1 : Tells the 82C59A that it is being used alone in the system. Therefore, there will be no need to issue ICW3 to the device.

D0 - IC4: Specifies to the 82C59A whether or not it can expect to receive ICW4. If this device is being used in an 80C86/ 80C88 system, ICW4 must be issued.

0 : ICW4 will not be issued. Therefore, all of the parameters associated with ICW4 will default to the zero (0) state. This should only be done when using the 82C59A in an 8080 or 8085 based system.

1 : ICW4 will be issued to the 82C59A.

2.2 ICW2:

ICW2 is the second control word that must be sent to the 82C59A. This byte is used in one of two ways by the 82C59A, depending on whether it is being used in an 8080/85 or an 80C86/88 based system.

When used in conjunction with the 8080/85 microprocessor, the value given to this register is taken as being the high byte of the address in the CALL instruction sent to the CPU.

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

FIGURE 5. ICW2 FORMAT

In an 80C86- or 80C88-based system, ICW2 is used to send the processor an interrupt vector. This vector is formed by taking the value of bits D7 through D3 and combining them with the interrupt request level to get an eight bit number. The processor will multiply this number by four and go to that absolute location in memory to find a starting address for the interrupt service routine corresponding to the interrupt request.

For example, if we set ICW2 to "00011000" and an interrupt is recognized on IR1, the vector sent to the 80C86(80C88) will be 00011001 (19H). The processor will then look to the memory location 64H to find the starting address of the corresponding interrupt service routine. It is the responsibility of the software to provide this address in the interrupt table.

D7	D6	D5	D4	D3	D2	D1	D0
A7	A6	A5	A4	A3	X	X	X

FIGURE 6. ICW2 FORMAT (80C86 MODE)

2.3 ICW3:

ICW3 is only issued when the SNGL bit in ICW1 has been set to zero. If not set, the next word written to the 82C59A will be interpreted as ICW4 if A0 = 1 and IC4 from ICW4 was set to one, or it could see it as one of the Operation Command Words based upon the state of the A0 line.

Like ICW2, this control word can be interpreted in two ways by the 82C59A. However the interpretation of this word depends on whether the 82C59A is being used as a "master" or a "slave" in the system. The definition of the particular devices role in the system is assigned through ICW4 (which will be discussed later), or through the state of the $\overline{SP}/\overline{EN}$ pin (pin 16).

82C59A as a MASTER:

If the given 82C59A is being used as a master, the eight (8) bits in this command word are used to indicate which of the IR lines are being driven by a slave 82C59A.

D7	D6	D5	D4	D3	D2	D1	D0
S7	S6	S5	S4	S3	S2	S1	S0

FIGURE 7. ICW3 FORMAT (MASTER)

D7 thru D0:

0 : The corresponding IR line to this bit is not being driven by a slave 82C59A. This line can however then be connected to the interrupt output of another interrupting device such as a UART. If there are unused bits in this byte because not all eight of the IR lines are used, set them to zero.

1 : The corresponding IR line to this bit is being driven by a slave 82C59A.

The bits in this command word are directly related to the IR lines. For example, to tell the 82C59A that there is a slave device connected to IR5 (pin 23), bit D5 of the command word should be set to a one (1).

82C59A as a SLAVE device:

When the device is being used as a slave device, we must use ICW3 to inform itself as to which IR line it will be connected to in the master. Therefore, only the three (3) least significant bits of ICW3 will be used to specify this value.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	IO2	IO1	IO0

FIGURE 8. ICW3 FORMAT (SLAVE)

These bits are coded as follows:

TABLE 3. SLAVE 'IDENTIFICATION' WITH ICW3

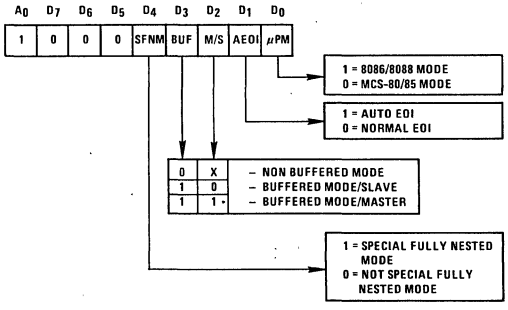
MASTER IR number	IO2	IO1	IO0
IR7	1	1	1
IR6	1	1	0
IR5	1	0	1
IR4	1	0	0
IR3	0	1	1
IR2	0	1	0
IR1	0	0	1
IR0	0	0	0

For example, if the INT output of a "slave" 82C59A is connected to the input pin IR5 on the "master" 82C59A, ICW3 of the "slave" would be programmed with the value 00000101b, or 05H. This informs the "slave" as to which priority level it holds with the "master".

D7 thru D3: These bits must be set to zeros (0) for proper operation of the device.

2.4 ICW4:

This control register is written to only when the IC4 bit is set in ICW1. The purpose of this command word is to set up the 82C59A to operate in a mode other than the default mode of operation. The default mode of operation is the same as if a value of 00H were to be written to ICW4 (i.e. all bits set to zero).



NOTE: Slave IO is equal to the corresponding master IR input

FIGURE 9. ICW4 FORMAT

D7 thru D5: These bits must be set to zero for proper operation.

D4 - SFNM: This bit is used in the selection of the Special Fully Nested Mode (SFNM) of operation. This mode should only be used when multiple 82C59As are cascaded in a system. It needs only to be programmed in the Master 82C59A in the system.

0 : Special Fully Nested Mode is not selected.

1 : Special Fully Nested Mode is selected.

D3 - BUF: This bit tells the 82C59A whether or not the outputs from the data pins (D0 - D7) will be buffered. If they are buffered, this bit will cause the $\overline{SP}/\overline{EN}$ pin to become an output signal that can be used to control the "enable" pin on a buffering device(s).

0 : The device will be used in a non-buffered mode. Therefore, (1) the M/S bit in ICW4 is a don't care, and (2) the $\overline{SP}/\overline{EN}$ pin becomes an input pin telling the device if it is being used as a master (pin 16 = High) or a slave (pin 16 = Low). For systems using a single 82C59A, the $\overline{SP}/\overline{EN}$ input should be tied high.

1 : The device is used in buffered mode. An enable output signal will be generated on pin 16, and the M/S bit will be used for determining whether the particular 82C59A is a "master" or a "slave".

D2 - M/S: This bit is of significance only when the BUF bit is set (BUF = 1). The purpose of this bit is to determine whether the particular 82C59A is being used as a "master" or a "slave" in the target system.

0 : The 82C59A is being used as a slave.

1 : The 82C59A is the master interrupt controller in the system.

D1 - AEOI: This bit is used to tell the 82C59A to automatically perform a non-specific End-of-Interrupt on the trailing edge of the last Interrupt Acknowledge pulse. Users should note that when this is selected, the nested priority interrupt structure is lost.

0 : Automatic End-of-Interrupt will not be generated.

1 : Automatic End-of-Interrupt will be generated on the trailing edge of the last Interrupt Acknowledge pulse.

D0 - μPM: This bit tells the Interrupt Controller which microprocessor is being used in the system. An 8080/8085, or an 80C86/80C88.

0 : The 82C59A will be used in an 8080/8085 based system.

1 : 82C59A to be used in the 80C86/88 mode of operation.

3.0 Operation Command Words

Once the Initialization Command Words, described in the previous section, have been written to the 82C59A, the device is ready to accept interrupt requests. While the 82C59A is operating, we have the ability to select various options that will put the device in different operating modes, by writing Operation Command Words (OCWs) to the 82C59A. These OCWs can be sent at any time after the device has been initialized and in any order. These words can be changed at any time as well. Note: If A0 = 0 and D4 of the command word = 1, the 82C59A will begin the ICW initialization sequence.

There are three different OCWs for the 82C59A. Each has a different purpose. The first control word (OCW1) is used for masking out interrupt lines that are to be inactive or ignored during operation. OCW2 is used to select from various priority resolution algorithms in the device. Finally, OCW3 is used for (1) controlling the Special Mask Mode, and (2) telling the 82C59A which Register will be read on the next RD pulse; the ISR (In-service Register) or the IRR (Interrupt Request Register).

3.1 OCW1:

This control word is used to set or clear the masking of the eight (8) interrupt lines input to the 82C59A. This control word performs this function via the Interrupt Mask Register (IMR). In it's initial state, the value of this register is 00H. In other words, all of the interrupt lines are enabled. Therefore, we need only write this control word when we wish to disable specific interrupt lines.

A direct mapping occurs between the bits in this control word and the actual interrupt pins on the device. For example bit 7 (D7) controls interrupt line IR7 (pin 25), bit 6 controls IR6, and so on.

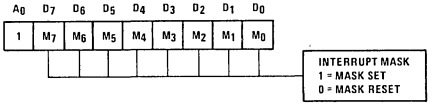


FIGURE 10. OCW1 FORMAT

Even though the user can mask off any of the IR lines, any interrupt occuring during that time will not be lost. The request for an interrupt is retained in the IRR; therefore when that IR is unmasked by issuing a new mask value to OCW1, the interrupt will be generated when it becomes the highest requesting priority.

D7 thru D0:

0 : When any of the bits in the control word are reset (0), the corresponding interrupt is enabled.

1 : By setting a bit(s) to a one in the control word, the corresponding interrupt line(s) is disabled.

For example, if the value 34H (00110100b) were written to OCW1, interrupts would be disabled from being serviced on lines IR2, IR4 and IR5.

3.2 OCW2:

In ICW4 bit D1 was used to specify whether the 82C59A should wait for an EOI (End of Interrupt) from the CPU, or generate its own EOI (Automatic EOI) . If bit D1 of ICW4 had been programmed to be a zero, OCW2 would be used for sending the EOI to the 82C59A. Conversely, if this bit had been set to a one, OCW2 would be used for specifying whether or not the 82C59A should perform a priority rotation on the interrupts when the AEOI is detected.

OCW2 has several EOI options. The EOI issued can be either specific or non-specific. For each of these EOIs, the user can specify whether or not priority rotation should be performed.

D7	D6	D5	D4	D3	D2	D1	D0
R	SL	EOI	0	0	L2	L1	L0

FIGURE 11.

R, SL, and EOI:

These three bits are used for specifying how the device should handle AEOIs, or for issuing one of several different EOIs. They are programmed as shown in the following table:

TABLE 4. ROTATE AND EOI MODES

R	SL	EOI	
0	0	1	Non-specific EOI command
0	1	1	* Specific EOI command
1	0	1	Rotate on non-specific EOI command
1	0	0	Rotate in Automatic EOI mode (set)
0	0	0	Rotate in Automatic EOI mode (clear)
1	1	1	Rotate on specific EOI command
1	1	0	* Set priority command
0	1	0	* No operation

*L0 - L2 are used

L2, L1, and L0:

These three bits of the control word are used in conjunction with the issuance of specific EOIs or when specifically establishing a different priority structure. The bits tell the 82C59A which interrupt level is to be acted upon. Therefore, the software needs to know which interrupt is being serviced by the 82C59A.

TABLE 5. INTERRUPT LEVEL TO ACT UPON

L2	L1	L0	
0	0	0	IR level 0
0	0	1	IR level 1
0	1	0	IR level 2
0	1	1	IR level 3
1	0	0	IR level 4
1	0	1	IR level 5
1	1	0	IR level 6
1	1	1	IR level 7

3.3 OCW3:

There are two main functions that OCW3 controls: (1) Interrupt Status, and (2) Interrupt Masking. Interrupt status can be checked by looking at the ISR or IRR registers, or by issuing a Poll Command to manually identify the highest priority interrupt requesting service.

D7	D6	D5	D4	D3	D2	D1	D0
0	ESMM	SMM	0	1	P	RR	RIS

FIGURE 12.

D7: Must be set to zero for proper operation of the 82C59A.

D6 - ESMM: Enable Special Mask Mode - The ESMM bit when enabled allows the SMM bit to set or clear the Special Mask Mode. When disabled, this bit causes the SMM bit to have no effect on the 82C59A.

0 : Disables the effect of the SMM bit.

1 : Enable the SMM bit to control the Special Mask Mode.

D5 - SMM: Special Mask Mode - The SMM bit is used to enable or disable the Special Mask Mode. This bit will only affect the 82C59A when the ESMM bit is set to 1.

0 : Disable the Special Mask Mode.

1 : Put the 82C59A into the Special Mask Mode.

D4, D3: These bits are used to differentiate between OCW2, OCW3 and ICW1. To properly select OCW3, D4 must be set to zero and D3 must be set to one.

D2 - P: Poll Command - This bit is used to issue the poll command to the 82C59A. The next read of the 82C59A will cause a poll word to be returned which tells if an interrupt is pending, and if so, which is the highest requesting level.

NOTE: The poll command must be issued each time the poll operation is desired.

0 : No poll command issued to the 82C59A.

1 : Issue the poll command.

D1 - RR: Read Register - This bit is used to execute the "read register" command. When this bit is set, the 82C59A will look at the RIS bit to determine whether the ISR or IRR register is to be read. When issuing this command, the next instruction executed by the CPU should be an input from this same port to get the contents of the specified register.

0 : No "Read Register" command will be performed.

1 : The next input instruction by the CPU will read either the contents of the ISR or the IRR as specified by the RIS bit.

D0 - RIS: This bit is used in conjunction with the RR bit to select which register is to be read when the "Read Register" command is issued.

0 : The next input instruction will read the contents of the Interrupt Request Register (IRR).

1 : The next input instruction will read the contents of the In-Service Register (ISR).

The two registers that can be accessed through the Read Register command are used to determine which interrupts are requesting service, and which one(s) are currently being serviced.

The IRR bits get set when corresponding Interrupt requests are received. For instance, when IR4 is detected, bit D4 of the IRR will get set. When an interrupt acknowledge comes back from the CPU, the priority resolution logic will determine which interrupt request will be serviced. The corresponding bit in the In-service Register (ISR) will then be set. Clearing of the correct bits in the ISR occurs through out use of the AEOI, or by issuing an EOI to the device.

4.0 Addressing the 82C59A

There are two factors that must be taken into account when addressing the 82C59A in a system. To begin with, the 82C59A is accessed only when the $\overline{CS}$ pin (chip select) sees an active signal (low). This signal is generated using control circuitry in the system. Secondly, the various registers within the 82C59A are selected based upon the state of the A0 (address pin) as well as specific bits in the command words (i.e for ICW1, OCW2, and OCW3 A0 must be a zero).

The circuit in Figure 13 shows that the $\overline{CS}$ signal is generated using an HPL-82C338 Programmable Chip Select Decoder (PCSD). This device is being used as a 3-to-8 decoder. Note that the G1 input is active high and G2 thru G5 have been programmed to be active low. The A, B, and C inputs to the 82C338 correspond to address lines AD2, AD3 and AD4 respectively, from the 80C88. The A0 input to the 82C59A is also taken from the CPUs address bus; AD0 is used. It should be noted that address line AD1 from the 80C88 is not being used in the addressing of this particular peripheral. This is done to allow other peripheral devices that require two address inputs for internal register selection, to use address lines AD0 and AD1 from the processor.

Because the AD1 address line from the 80C88 is not being used, the 82C59A will be addressed regardless of whether AD1 is high or low (1 or 0). The remainder of the address lines from the 80C88 can either be a zero or one when addressing the 82C59A. For the examples to be presented, it can be assumed that all unused address lines will be set to zero when addressing the 82C59A.

In Figure 13, output $\overline{Y6}$ from the HPL-82C338 is being used as the $\overline{CS}$ input to the 82C59A. This line is enabled when the inputs on A, B, and C are: A = 0, B = 1, and C = 1. Combining this with the A0 input to the 82C59A, we get the addresses 18H and 19H for accessing the 82C59A.

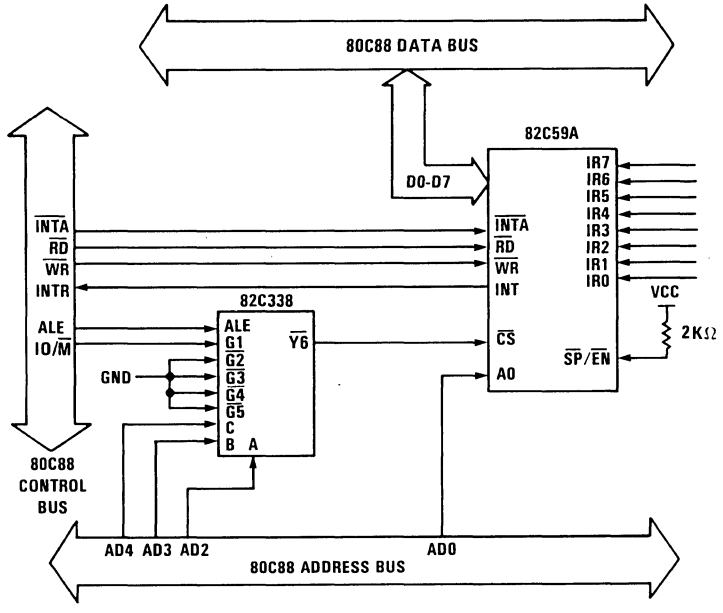


FIGURE 13. ADDRESSING THE 82C59A

5.0 Programming the 82C59A

As described earlier, there are two different types of command words that are used for controlling 82C59A operation; the Initialization Command Words (ICWs) and the Operation Command Words (OCWs). To properly program the 82C59A, it is essential that the ICWs be written first. When writing the ICWs to the 82C59A, they must be written in the following sequence:

(1) Write ICW1 to the 82C59A, A0 = 0.

(2) Write ICW2 to the 82C59A, A0 = 1.

(3) If using cascaded 82C59As in system, write ICW3 to the 82C59A, A0 = 1.

(4) If IC4 bit was set in ICW1, write ICW4 to the 82C59A.

NOTE: When using multiple 82C59As in the system (cascaded), each one must be initialized following the above sequence.

Once the 82C59A(s) has been configured through the ICWs, the OCWs can be used to select from the various operation mode options. These include: masking of interrupt lines, selection of priority rotation, issuance of EOIs, reading of the ISR andsor IRR, etc. These OCWs can be written to the 82C59A at any time during operation of the 82C59A. The various command words are identified by the state of selected bits in the words, rather than by the sequence that they are written to the 82C59A; as with the ICWs. Therefore, it is imperative that the fixed bit values in the command words be written as such to insure proper operation of the device(s).

5.1 Example 1: Single 82C59A

In Example 1, we are using a single 82C59A in a system to handle the interrupts caused by an HD-6406 Programmable Asynchronous Communications Interface. The system is driven using an 80C86 Microprocessor. The system configuration is shown in Figure 14. An assembly language listing for the software controlling this system can be found in Program Listing, Example 1, on page 15.

Interrupts are initiated by the HD-6406 anytime it receives data on its Serial Data In pin (SDI), or when it is ready to transmit more data via its Serial Data Out pin (SDO).

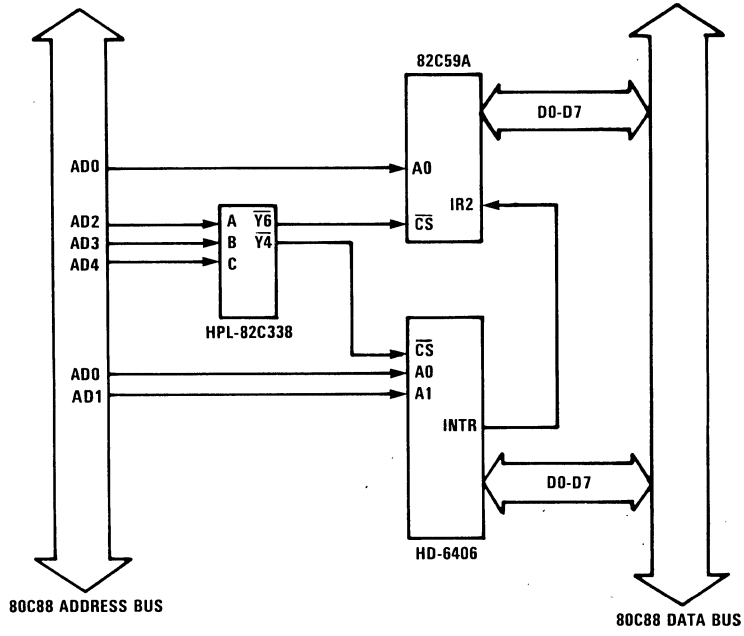


FIGURE 14. EXAMPLE 1: SINGLE 82C59A

5.2 Example 2: Cascaded 82C59As

Example 2 illustrates how we can use multiple 82C59As in Cascade Mode. Figure 15 shows the interconnections between the master and slave interrupt controllers. In this example, only one interrupt can occur. This is generated by the HD-6406 PACI. Except for the fact that this system is configured with a Master-Slave interrupt scheme, it is the same as that in Example 1. The software for this system is given in Program Listing, Example 2, on Page 20.

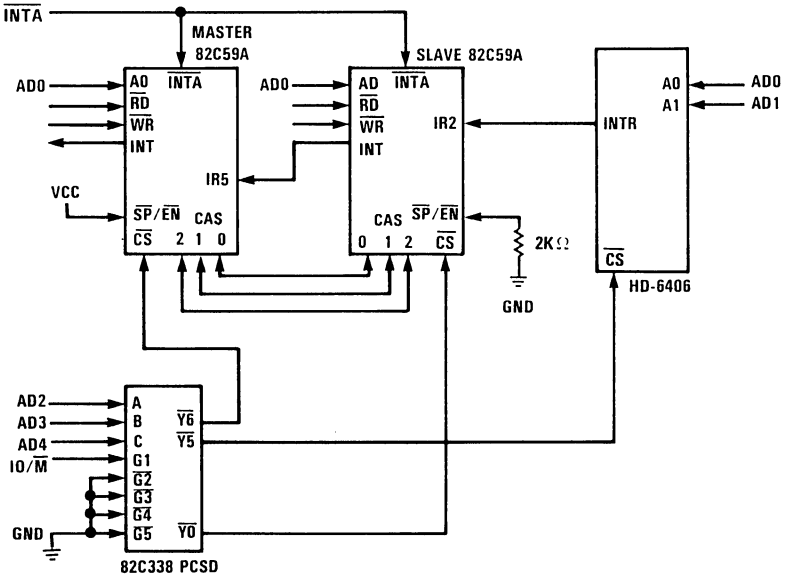


FIGURE 15. EXAMPLE 2: CASCADED 82C59As

6.0 Expansion Past 64 Interrupts

In some instances, it may be desirable to expand the number of available interrupts in a system past the maximum of 64 imposed when using cascaded 82C59As. The easiest way to accomplish this is through the use of the Poll command with the 82C59A. Figure 16 illustrates one example of how this expansion can be accomplished. Notice that we are using two 3-to-8 decoders (HPL-82C338 PCSDs) to address up to 16 82C59As. Selection of which decoder is active takes place using the G2 pin on the HPL-82C338. For one HPL-82C338, G2 has been programmed to be active low ($\overline{G2}$), while the other HPL-82C338 has been programmed for G2 to operate active high. This G2 input is driven by AD5 from the CPU's address bus.

With this type of interrupt structure, we are not using the INT and $\overline{INTA}$ lines from our processor (80C88 for this example). Because of this, no interrupts will break execution of the system software. Therefore, it is the task of the software to poll the various 82C59As in the system to see if any interrupts are pending. Once it has been established which interrupt requires servicing, the software can take appropriate action.

There are disadvantages to using the poll mode for the systems interrupt structure: (1) the overhead of polling each of the 82C59As reduces the systems efficiency, and (2) real-time interrupt servicing cannot be guaranteed.

There are several advantages to using the poll mode in this manner: (1) there can be more than 64 priority interrupts in the system, and (2) memory in the system is freed because no interrupt vector table is required.

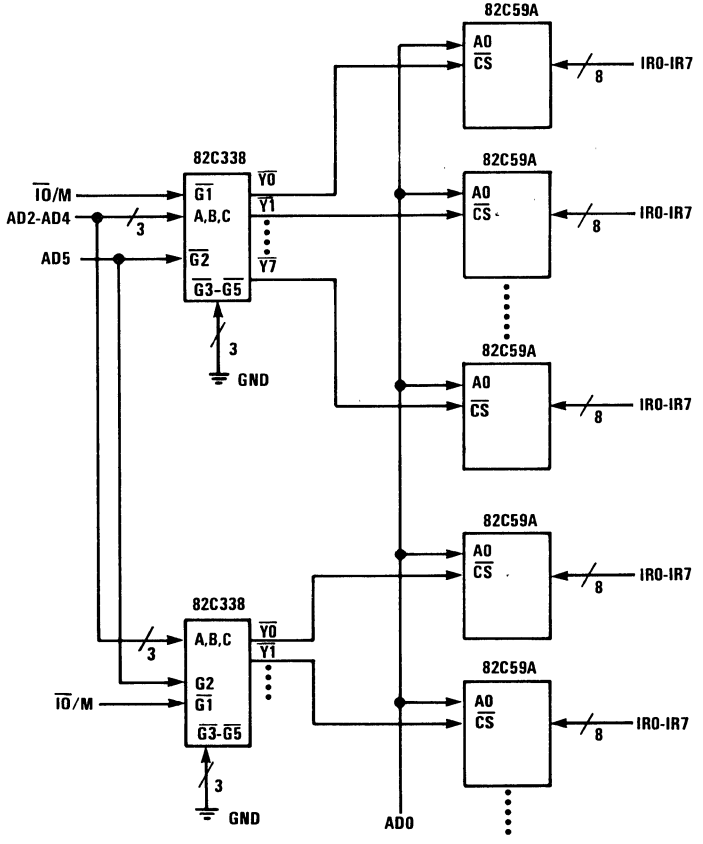


FIGURE 16. EXPANDING PAST 64 INTERRUPTS

PROGRAM LISTING, EXAMPLE 1

```
NAME            EXAMPLE 1
; ***************************************************************************
;  HARRIS SEMICONDUCTOR                                          AUG 5, 1985
;  P.O. Box 883
;  Melbourne, FL  32901
;
;  Microprocessor Applications
;  JAGoss
;
;  EXAMPLE #1:     System with a single 82C59A
;
; ***************************************************************************


;  The following are port addresses for the devices used in our example
;  system.  The devices that we will look at are the HD-6406 PACI, and the
;  two 82C59A Interrupt Controller.

;  ------ 6406 Register Addresses ------

UCR             EQU     11H             ;UART control register
BRSR            EQU     13H             ;Baud Rate Select Register
MCR             EQU     12H             ;Modem Control Register
USR             EQU     11H             ;UART Status Register
MSR             EQU     13H             ;Modem Status Register
TBR             EQU     10H             ;Transmit Buffer Register
RBR             EQU     10H             ;Receive Buffer Register

;  --------- 82C59A Addresses ----------

ICW1            EQU     18H
ICW2            EQU     19H
ICW4            EQU     19H
OCW1            EQU     19H
OCW2            EQU     18H

CARRIAGE_RETURN EQU     0DH
LINE_FEED       EQU     0AH
DR              EQU     80H             ;Mask for checking DATA READY
TBRE            EQU     40H             ;Mask for checking TRANSMIT BUFFER
                                        ;  REGISTER EMPTY


ASSUME          CS:DRIVER_59A,
&               DS:BUFFER_AREA,
&               SS:STACK_AREA
```

PROGRAM LISTING, EXAMPLE 1

```
DRIVER_59A      SEGMENT         PUBLIC
; ***************************************************************
; *                           MAIN                              *
; ***************************************************************

MAIN            PROC    NEAR

SET_UP:         MOV     AX,BUFFER_AREA  ;Set up the data segment
                MOV     DS,AX
                MOV     AX,STACK_AREA   ;Set up the stack segment
                MOV     SS,AX
                                        ;Set up the stack pointer
                MOV     SP,OFFSET STACK_AREA:TOP_OF_STACK

;  Set up the interrupt vector table

                MOV     AX,OFFSET INT_SERVICE_ROUTINE
                MOV     ISR_34,AX
                MOV     ISR_34[2],CS

;  Initialize the pointer into the data buffer.

                MOV     BX,OFFSET BUFFER
                XOR     DI,DI           ;Clear the index register

;  Initialize the 82C59A

                CALL    INIT_82C59A

;  Initialize the HD-6406 PACI

                CALL    INIT_6406

;  Wait for interrupts from the '59A...

                STI                     ;Set the interrupt enable flag.
WAIT_LOOP:      NOP
                JMP     WAIT_LOOP

                HLT
MAIN            ENDP
```

PROGRAM LISTING, EXAMPLE 1

```
INIT_82C59A     PROC    NEAR
; ***************************************************************
; *                          INIT_82C59A                        *
; ***************************************************************

; We first want to write ICW1.  This will be used to set the
; device for edge triggered interrupt detection and for use
; in Single Mode.

BEGIN_59A:      MOV     AL,00010000B    ;Edge triggered, and single mode
                OUT     ICW1,AL

; Now we will write out ICW2.  This gives the 59A information
; about where to branch to in the interrupt table.

                MOV     AL,00100000B
                OUT     ICW2,AL

; The final control word that is written in this sequence is ICW4.
; This is used to specify that the device is to operate in 80C86/80C88
; mode, with normal EOI's generated through software, and non-buffered
; outputs are being fed back to the CPU.

                MOV     AL,00000001B
                OUT     ICW4,AL

; To insure that interrupts will only be issued by the HD-6406 PACI,
; we will write out an interrupt mask to the register OCW1.  This
; mask will only allow interrupts from the specified lines.  In this
; case on IR2 only, all others will be disabled.

                MOV     AL,11111011B    ;A zero in a bit means that the
                OUT     OCW1,AL         ;  corresponding IR lines is enabled.

                RET
INIT_82C59A     ENDP



INIT_6406       PROC    NEAR
; ***************************************************************
; *                          INIT_6406                          *
; ***************************************************************

; This routine sets up the HD-6406 to communicate with a dumb
; terminal.  The device will generate an interrupt whenever
; a key is pressed at the terminal.
```

PROGRAM LISTING, EXAMPLE 1

```
;  Set up for 8 data bits, 1 stop bit, and no parity.

BEGIN_6406:     MOV     AL,00111110B
                OUT     UCR,AL

;  Set up BRSR for 9600 bps, assuming that the target system uses
;  a 2.4576 MHz clock crystal.

                MOV     AL,00000110B
                OUT     BRSR,AL

;  Enable interrupts on the 6406, enable the receiver, and
;  select normal mode.

                MOV     AL,00100100B
                OUT     MCR,AL

                RET                     ;Return to the MAIN
INIT_6406       ENDP



INT_SERVICE_ROUTINE     PROC    NEAR
; ************************************************************
; *                     INT_SERVICE_ROUTINE                  *
; ************************************************************

ISR_START:      IN      AL,USR          ;Find out what caused the interrupt.
                TEST    AL,DR           ;Was it DATA READY ?
                JNZ     READ_DATA
                TEST    AL,TBRE         ;Was it TRANSMIT BUFFER REG. EMPTY ?
                JNZ     PRINT_BUFFER    ;If so, then print next character

;  If this condition was not detected, then we have an erroneous
;  interrupt from the HD-6406.  Rather than servicing this, we will
;  simply return from the service routine to the MAIN.

ERROR:          JMP     ISR_EXIT

;  Read the data that is present in the Receive Buffer Register.

READ_DATA:      IN      AL,RBR
                MOV     [BX][DI],AL     ;Save the data in our buffer area.
                INC     DI              ;Increment the index into the buffer.
                CMP     AL,CARRIAGE_RETURN
                JE      PRINT_LF

                JMP     ISR_EXIT        ;Exit the service routine.

;  Set up for writing the data out to the Transmit Buffer...

PRINT_LF:       MOV     AL,LINE_FEED
                MOV     [BX][DI],AL     ;Add a line feed to the buffer.
```

PROGRAM LISTING, EXAMPLE 1

```
                INC     DI
                OUT     TBR,AL
                MOV     CX,DI           ;Load tne buffer size into CX
                XOR     DI,DI           ;Set the index back to beginning
                                        ;  of the buffer.
                JMP     ISR_EXIT

;  Print out the contents of the buffer...

PRINT_BUFFER:   CMP     CX,0            ;Anything to print ?
                JNE     PRINT_CHAR      ;If so, then print it...
                JMP     ISR_EXIT        ;Else, ignore this interrupt...
PRINT_CHAR:     MOV     AL,[BX][DI]     ;Print the byte pointed to in buffer.
                OUT     TBR,AL
                INC     DI              ;Point to next character.
                LOOP    PRINT_CHAR      ;Print til end-of-buffer.

DONE_PRINTING:  XOR     DI,DI           ;Re-initialize pointer into buffer.

;  Exit from the service routine, sending out a non-specific EOI first.

ISR_EXIT:       MOV     AL,00100000B    ;Send out an End-of-Interrupt
                OUT     OCW2_S,AL       ;  to both master and slave.
                OUT     OCW2_M,AL
                IRET

INT_SERVICE_ROUTINE     ENDP
DRIVER_59A              ENDS


BUFFER_AREA     SEGMENT         PUBLIC
; ***************************************************************
; *                           BUFFER_AREA                       *
; ***************************************************************

                ORG     88H
ISR_34          DW      4 DUP(?)

                ORG     100H
BUFFER          DB      80 DUP(?)
BUFFER_AREA     ENDS


STACK_AREA      SEGMENT         PUBLIC
; ***************************************************************
; *                           STACK_AREA                        *
; ***************************************************************

STACK           DW      80H DUP(?)
TOP_OF_STACK    LABEL   WORD
STACK_AREA      ENDS
                END
```

5 CMOS PERIPHERALS

PROGRAM LISTING, EXAMPLE 2

```
NAME            EXAMPLE_2
; ***************************************************************************
;  HARRIS SEMICONDUCTOR                                          AUG 27, 1985
;  P.O. Box 883
;  Melbourne, FL  32901
;
;  Microprocessor Applications
;  JAGoss
;
;  EXAMPLE #2:
;  Configure the system for two 82C59As (MASTER/SLAVE).  Interrupts are
;  generated for the slave by an HD-6406 PACI.
;
; ***************************************************************************

;  The following are port addresses for the devices used in our example
;  system.  The devices that we will look at are the HD-6406 PACI, and the
;  two 82C59A Interrupt Controllers.

;  ------ 6406 Register Addresses ------

UCR             EQU     11H             ;UART control register
BRSR            EQU     13H             ;Baud Rate Select Register
MCR             EQU     12H             ;Modem Control Register
USR             EQU     11H             ;UART Status Register
MSR             EQU     13H             ;Modem Status Register
TBR             EQU     10H             ;Transmit Buffer Register
RBR             EQU     10H             ;Receive Buffer Register

;  --------- 82C59A Addresses ----------

ICW1_M          EQU     18H             ;MASTER Interrupt Controller
ICW2_M          EQU     19H
ICW3_M          EQU     19H
ICW4_M          EQU     19H
OCW1_M          EQU     19H
OCW2_M          EQU     18H

ICW1_S          EQU     0H              ;SLAVE Interrupt Controller
ICW2_S          EQU     1H
ICW3_S          EQU     1H
ICW4_S          EQU     1H
OCW1_S          EQU     1H
OCW2_S          EQU     0H

CARRIAGE_RETURN EQU     0DH
LINE_FEED       EQU     0AH
DR              EQU     80H             ;Mask for checking DATA READY
TBRE            EQU     40H             ;Mask for checking TRANSMIT BUFFER
                                        ;  REGISTER EMPTY

ASSUME          CS:DRIVER_59A,
&               DS:BUFFER_AREA,
&               SS:STACK_AREA
```

PROGRAM LISTING, EXAMPLE 2

```
DRIVER_59A      SEGMENT         PUBLIC
; ***************************************************************
; *                              MAIN                           *
; ***************************************************************

MAIN            PROC    NEAR

SET_UP:         MOV     AX,BUFFER_AREA  ;Set up the data segment
                MOV     DS,AX
                MOV     AX,STACK_AREA   ;Set up the stack segment
                MOV     SS,AX
                                        ;Set up the stack pointer
                MOV     SP,OFFSET STACK_AREA:TOP_OF_STACK

;  Set up the interrupt vector table

                MOV     AX,OFFSET INT_SERVICE_ROUTINE
                MOV     ISR_34,AX
                MOV     ISR_34[2],CS

;  Initialize the pointer into the data buffer.

                MOV     BX,OFFSET BUFFER
                XOR     DI,DI           ;Clear the index register

;  Initialize the 82C59A

                CALL    INIT_82C59A

;  Initialize the HD-6406 PACI

                CALL    INIT_6406

;  Wait for interrupts from the '59A...

                STI                     ;Set the interrupt enable flag.
WAIT_LOOP:      NOP
                JMP     WAIT_LOOP

                HLT
MAIN            ENDP
```

PROGRAM LISTING, EXAMPLE 2

```
INIT_82C59A     PROC    NEAR
; ***********************************************************
; *                        INIT_82C59A                      *
; ***********************************************************

; -------------------- Configure the MASTER --------------------

;  We first want to write ICW1.  This will be used to set the
;  device for edge triggered interrupt detection and for use
;  in Cascade Mode.

BEGIN_59A:      MOV     AL,00010001B    ;Edge triggered, and cascade mode
                OUT     ICW1_M,AL

;  Now we will write out ICW2.  This gives the 59A information
;  about where to branch to in the interrupt table.  In this example
;  however, this value is not used.  Interrupts will only be generated
;  by the slave 82C59A.

                MOV     AL,00000000B
                OUT     ICW2_M,AL

;  Write out ICW3 to the MASTER.  This tells the master which IR lines
;  have slaves connected to them.  In this case, interrupts come from
;  the slave only on IR5.  All other lines are not used.

                MOV     AL,00100000B    ;SLAVE is only on IR5.
                OUT     ICW3_M,AL

;  The final control word that is written in this sequence is ICW4.
;  This is used to specify that the device is to operate in 80C86/88
;  mode, with normal EOI's generated through software, and non-buffered
;  outputs are being fed back to the CPU.

                MOV     AL,00000001B
                OUT     ICW4_M,AL

; -------------------- Configure the SLAVE --------------------

;  First, set up the slave for edge triggered interrupts, cascade mode
;  and tell it that ICW4 is to be issued.

                MOV     AL,00010001B
                OUT     ICW1_S,AL

;  Write ICW2 to the slave.  When an interrupt occurs, the 82C59A will take
;  this value, add to it the interrupt number (IR2 = 20H + 2 = 22H) and
;  sends it to the processor.  The processor will then multiply this number
;  by four (4) to generate the address in the Interrupt table to look for
;  the address of the Interrupt Service Routine.

                MOV     AL,20H          ;IR2 from the slave will cause the
                OUT     ICW2_S,AL       ;  CPU to vector 88H.
```

PROGRAM LISTING, EXAMPLE 2

```
;  Tell the slave which IR line on the master it is connected to.

               MOV     AL,00000101B    ;It drives IR5...
               OUT     ICW3_S,AL

;  Set up the slave for normal EOI's, and 80C86/88 mode.

               MOV     AL,00000001B
               OUT     ICW4_S,AL

;  Set up the mask register for both the master and the slave...

               MOV     AL,11011111B    ;Interrupts recognized only on IR5
               OUT     OCW1_M,AL

               MOV     AL,11111011B    ;Interrupt recognized only on IR2
               OUT     OCW1_S,AL

               RET
INIT_82C59A    ENDP



INIT_6406      PROC    NEAR
; ***************************************************************
; *                          INIT_6406                          *
; ***************************************************************

;  This routine sets up the HD-6406 to communicate with a dumb
;  terminal.  The device will generate an interrupt whenever
;  a key is pressed at the terminal.

;  Set up for 8 data bits, 1 stop bit, and no parity.

BEGIN_6406:    MOV     AL,00111111B
               OUT     UCR,AL

;  Set up BRSR for 9600 bps, assuming that the target system uses
;  a 2.4576 MHz clock crystal.

               MOV     AL,00000110B
               OUT     BRSR,AL

;  Enable interrupts on the 6406, enable the receiver, and
;  select normal mode.

               MOV     AL,00100100B
               OUT     MCR,AL

               RET                     ;Return to the MAIN
INIT_6406      ENDP
```

PROGRAM LISTING, EXAMPLE 2

```
DONE_PRINTING:  XOR     DI,DI           ;Re-initialize pointer into buffer.

;  Exit from the service routine, sending out a non-specific EOI first.

ISR_EXIT:       MOV     AL,00100000B    ;Send out an End-of-Interrupt
                OUT     OCW2_S,AL       ;  to both master and slave.
                OUT     OCW2_M,AL
                IRET

INT_SERVICE_ROUTINE     ENDP
DRIVER_59A              ENDS


BUFFER_AREA     SEGMENT         PUBLIC
; ***************************************************************
; *                          BUFFER_AREA                        *
; ***************************************************************

                ORG     88H
ISR_34          DW      4 DUP(?)
                ORG     100H
BUFFER          DB      80 DUP(?)

BUFFER_AREA     ENDS


STACK_AREA      SEGMENT         PUBLIC
; ***************************************************************
; *                          STACK_AREA                         *
; ***************************************************************

STACK           DW      80H DUP(?)
TOP_OF_STACK    LABEL   WORD
STACK_AREA      ENDS
                END
```

DIGITAL

CMOS Data Communications

6

HARRIS

HD-4702/883

June 1989

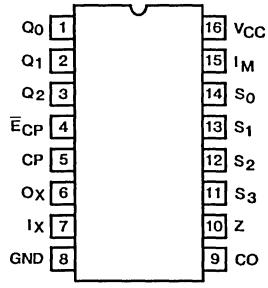
CMOS Programmable Bit Rate Generator

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1. 2. 1.
- HD-4702/883 Provides 13 Commonly Used Bit Rates
- Uses a 2.4576MHz Crystal/Input for Standard Frequency Output (16 Times Bit Rate)
- Low Power Dissipation
- Conforms to EIA RS-404
- One HD-4702/883 Controls up to Eight Transmission Channels
- Initialization Circuit Facilitates Diagnostic Fault Isolation
- On-Chip Input Pull-Up Circuit

Pinout

HD1-4702/883 (CERAMIC DIP)
TOP VIEW



Description

The HD-4702/883 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as a UART. It generates 13 commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 Baud x 16 x16, since there is an internal ÷ 16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The HD-4702/883 can provide multi-channel operation with a minimum of external logic by having the clock frequency CO and the ÷ 8 prescaler outputs Q_0, Q_1, Q_2 available externally. All signals have a 50% duty cycle except 1800 Baud, which has less than 0.39% distortion.

The four rate select inputs (S_0-S_3) select which bit rate is at the output (Z). See Truth Table for Rate Select Inputs for select code and output bit rate. Two of the 16 select codes for the HD-4702/883 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate "ZERO BAUD".

The bit rates most commonly used in modern data terminals (110, 150, 300, 1200, 2400 Baud) require that no more than one input be grounded for the HD-4702/883, which is easily achieved with a single 5-position switch.

The HD-4702/883 has an initialization circuit which generates a master reset for the scan counter. This signal is derived from a digital differentiator that senses the first high level on the CP input after the $\bar{E}_{CP}$ input goes low. When $\bar{E}_{CP}$ is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset. See Clock Modes and Initialization below.

Truth Tables

TRUTH TABLE FOR RATE SELECT INPUTS
(Using 2.4576MHz Crystal)

S_3	S_2	S_1	S_0	OUTPUT RATE (Z)
L	L	L	L	MUX Input (I_M)
L	L	L	H	MUX Input (I_M)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

NOTE. 19200 Baud by connecting Q_2 to I_M

CLOCK MODES AND INITIALIZATION

I_X	$\bar{E}_{CP}$	CP	OPERATION
⎍⎍	H	L	Clocked from I_X
X	L	⎍⎍	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍	Reset During 1st CP = High Time

NOTE: Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576MHz.

H = HIGH Level

L = LOW Level

X = Don't Care

⎍⎍ = 1st HIGH Level Clock Pulse after E_{CP} goes LOW

⎍ = Clock Pulse

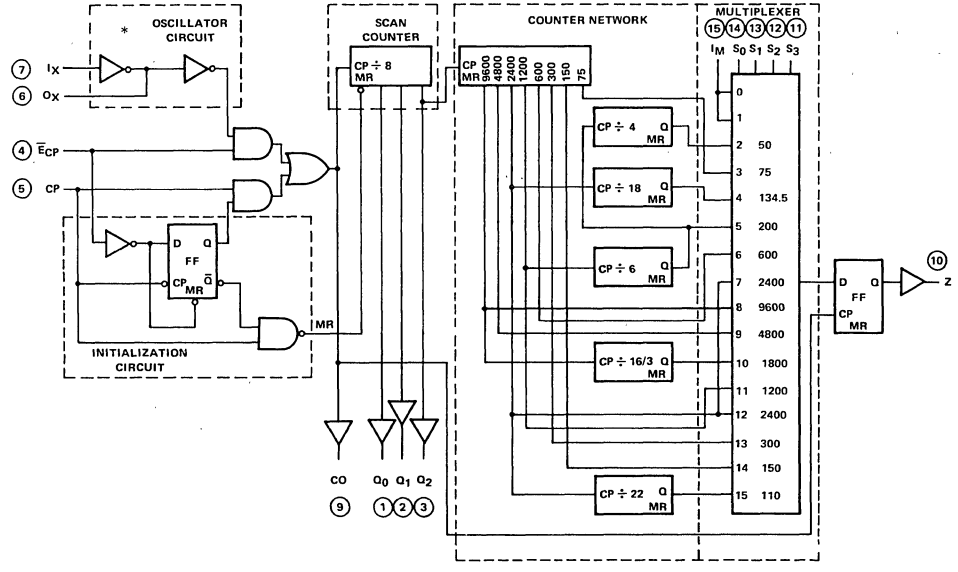
6 CMOS DATA COMMUNICATIONS

Pin Description

PIN NUMBER	TYPE	SYMBOL	DESCRIPTION
16		V_{CC}	V_{CC}: Is the +5V power supply pin. A 0.1μF capacitor between pins 16 and 8 is recommended for decoupling
8		GND	GROUND
5	I	CP	EXTERNAL CLOCK INPUT
4	I	$\overline{E}_{CP}$	EXTERNAL CLOCK ENABLE: A low signal on this input allows the baud rate to be generated from the CP input.
7	I	I_X	CRYSTAL INPUT
6	O	O_X	CRYSTAL DRIVE OUTPUT
15	I	I_M	MULTIPLEXED INPUT
11, 12, 13, 14	I	$S_0 - S_3$	BAUD RATE SELECT INPUTS
9	O	CO	CLOCK OUTPUT
1, 2, 3	O	$Q_0 - Q_2$	SCAN COUNTER OUTPUTS
10	O	Z	BIT RATE OUTPUT

Block Diagram

HD-4702/883



V_{DD} = PIN 16
V_{SS} = PIN 8
⊙ = PIN NUMBER
* See Figure 4 in Design Information for Crystal Specifications.

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or
I/O Voltage Applied ..... GND - 0.5V to V_{CC} + 0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C
ESD Classification ..... Class 1
Typical Derating Factor ..... 1mA/MHz Increase in ICCOP

Reliability Information

Thermal Resistance, Junction-to-Case (θ_{jc})
Ceramic DIP Package ..... +17.1°C/W
Thermal Resistance, Junction-to-Ambient (θ_{ja})
Ceramic DIP Package ..... +75.7°C/W
Maximum Package Power Dissipation @ +125°C
Ceramic DIP Package 660mW
Gate Count 720

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input High Voltage	VIH	V_{CC} = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	V_{CC} 70%	-	V
Input Low Voltage	VIL	V_{CC} = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	V_{CC} 30%	V
Output High Voltage	VOH1	IOH $\leq$ -1µA, V_{CC} = 4.5V, (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	V_{CC}-0.1	-	V
Output Low Voltage	VOL1	IOL $\leq$ +1µA, V_{CC} = 4.5V, (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.1	V
Input High Current	IIH	V_{IN} = V_{CC}. All Other Pins = 0V, V_{CC} = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1	+1	µA
Input Low Current (IX Input)	IILX	V_{IN} = 0V, All Other Pins = V_{CC}, V_{CC} = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1	+1	µA
Input Low Current (All Other Inputs)	IIL	V_{IN} = 0V, All Other Pins = V_{CC}, V_{CC} = 5.5V (Note 2)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	-100	µA
Output High Current (OX)	IOHX	V_{OUT} = V_{CC} - 0.5, V_{CC} = 4.5V Input at 0V or V_{CC} per Logic Function or Truth Table	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-0.1	-	mA
Output High Current (All Other Outputs)	IOH1	V_{OUT} = 2.5V, V_{CC} = 4.5V Input at 0V or V_{CC} per Logic Function or Truth Table	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	-	mA
Output High Current (All Other Outputs)	IOH2	V_{OUT} = V_{CC} -0.5, V_{CC} = 4.5V Input at 0V or V_{CC} per Logic Function or Truth Table	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-0.3	-	mA
Output Low Current (OX)	IOLX	V_{OUT} = 0.4V, V_{CC} = 4.5V Input at 0V or V_{CC} per Logic Function or Truth Table	1, 2, 3	$-55°C \leq T_A \leq +125°C$	0.1	-	mA
Output Low Current (All Other Outputs)	IOL	V_{OUT} = 0.4V, V_{CC} = 4.5V Input at 0V or V_{CC} per Logic Function or Truth Table	1, 2, 3	$-55°C \leq T_A \leq +125°C$	1.6	-	mA
Supply Current (Static)	ICC	$\overline{E}_{CP}$ = V_{CC}, CP = 0V, V_{CC} = 5.5V All Other Inputs = GND, (Note 2) $\overline{E}_{CP}$ = V_{CC}, CP = 0V, V_{CC} = 5.5V All Other Inputs = V_{CC}, (Note 2)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	- -	1500 1000	µA µA

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except I_X.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

A.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay, I_X to CO	tPLH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	350	ns
	tPHL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	275	ns
Propagation Delay, CP to CO	tPLH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	260	ns
	tPHL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	220	ns
Propagation Delay, CO to Qn	tPLH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	(Note 2)	ns
	tPHL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	(Note 2)	ns
Propagation Delay, CO to Z	tPLH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	85	ns
	tPHL	$V_{CC} = 4.5V$	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	75	ns
Output Transition Time (Except O_X)	tTLH	$CL \leq 7pF$ on O_X	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	160	ns
	tTHL	$CL = 50pF$	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	75	ns
Set-Up Time, Select to CO	ts	(Note 1)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	350	-	ns
Hold Time, Select to CO	th		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Set-Up Time, I_M to CO	ts		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	350	-	ns
Hold Time, I_M to CO	th		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Minimum Clock Pulse Width, Low (Notes 3, 4)	twCP(L)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Minimum Clock Pulse Width, High (Notes 3, 4)	twCP(H)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Minimum I_X Pulse Width, Low (Note 4)	twCP(L)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	160	-	ns
Minimum I_X Pulse Width, High (Note 4)	twCP(H)		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	160	-	ns

NOTES:

1. Propagation Delays (tPLH and tPHL) and Output Transition Times (tTLH and tTHL) will change with Output Load Capacitance (CL). Set-up Times (ts), Hold Times (th), and Minimum Pulse Widths (tw) do not vary with load capacitance.
2. For multichannel operation, Propagation Delay (CO to Qn) plus Set-Up Time, Select to CO, is guaranteed to be $\leq$ 367ns.
3. The first High Level Clock Pluse after $\overline{E}_{CP}$ goes Low must be at least 350ns long to guarantee reset of all Counters.
4. It is recommended that input rise and fall times to the clock inputs (CP, I_X) be less than 15ns.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

A.C. PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	All Measurements are referenced to device ground, f = 1MHz.	1	$T_A = +25^oC$	-	7.0	pF
Output Capacitance	CO		1	$T_A = +25^oC$	-	15.0	pF
Propagation Delay I_X to CO	tPLH	$V_{CC} = 4.5V$ $CL \leq 7pF$ on O_X $CL = 15pF$	1, 3	$-55^oC \leq T_A \leq +125^oC$	-	300	ns
	tPHL		1, 3	$-55^oC \leq T_A \leq +125^oC$	-	250	ns
Propagation Delay CP to CO	tPLH		1, 3	$-55^oC \leq T_A \leq +125^oC$	-	215	ns
	tPHL		1, 3	$-55^oC \leq T_A \leq +125^oC$	-	195	ns
Propagation Delay CO to Qn	tPLH		1, 3	$-55^oC \leq T_A \leq +125^oC$	-	(Note 2)	ns
	tPHL		1, 3	$-55^oC \leq T_A \leq +125^oC$	-	(Note 2)	ns
Propagation Delay CO to Z	tPLH		1, 3	$-55^oC \leq T_A \leq +125^oC$	-	75	ns
	tPHL		1, 3	$-55^oC \leq T_A \leq +125^oC$	-	65	ns
Output Transition Time (Except O_X)	tTLH		1, 3	$-55^oC \leq T_A \leq +125^oC$	-	80	ns
	tTHL		1, 3	$-55^oC \leq T_A \leq +125^oC$	-	40	ns

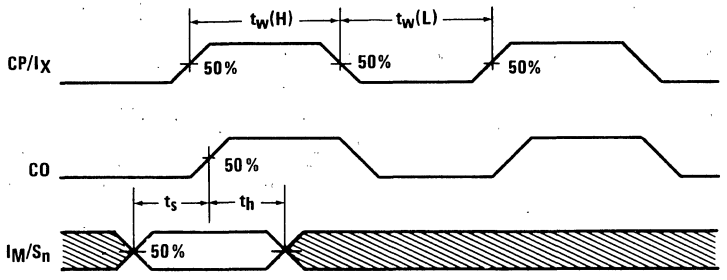
NOTES:
1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. For multichannel operation, Propagation Delay (CO to Qn) plus Set-Up Time, Select to CO, is guaranteed to be $\leq$ 367ns.
3. Propagation Delays (tPLH and tPHL) and Output Transition Times (tTLH and tTHL) will change with Output Load Capacitance (CL). Set-up Times (ts), Hold Times (th), and Minimum Pulse Widths (tw) do not vary with load capacitance.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

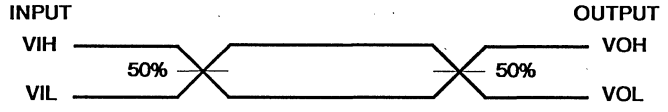
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Switching Waveform



NOTE: Set-Up and Hold Times are shown as positive values but may be specified as negative values.

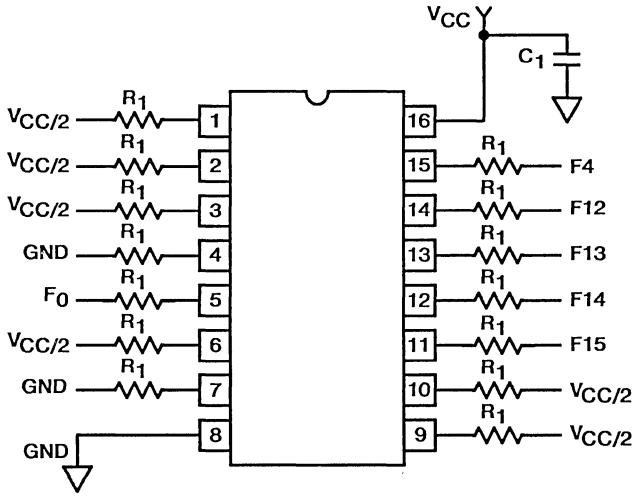
A.C. Testing Input, Output Waveform



A.C. Testing: All Input signals must switch between VIL and VIH. Input Rise and fall times are driven at 1nsec per volt.

Burn-In Circuit

HD-4702/883 CERAMIC DIP



NOTES: F_0 = 100KHz ± 10%, $F_1 = F_{0/2}$, $F_2 = F_{1/2}$, . . .
R_1 = 10kΩ, 1/4 W, ±10%
V_{CC} = 5.5V ± 0.5V, GND = 0V
C_1 = 0.01µF minimum

Metallization Topology

DIE DIMENSIONS:
100 x 97 x 19 mils

METALLIZATION:
Type: Si - Al
Thickness: 10kÅ - 12kÅ

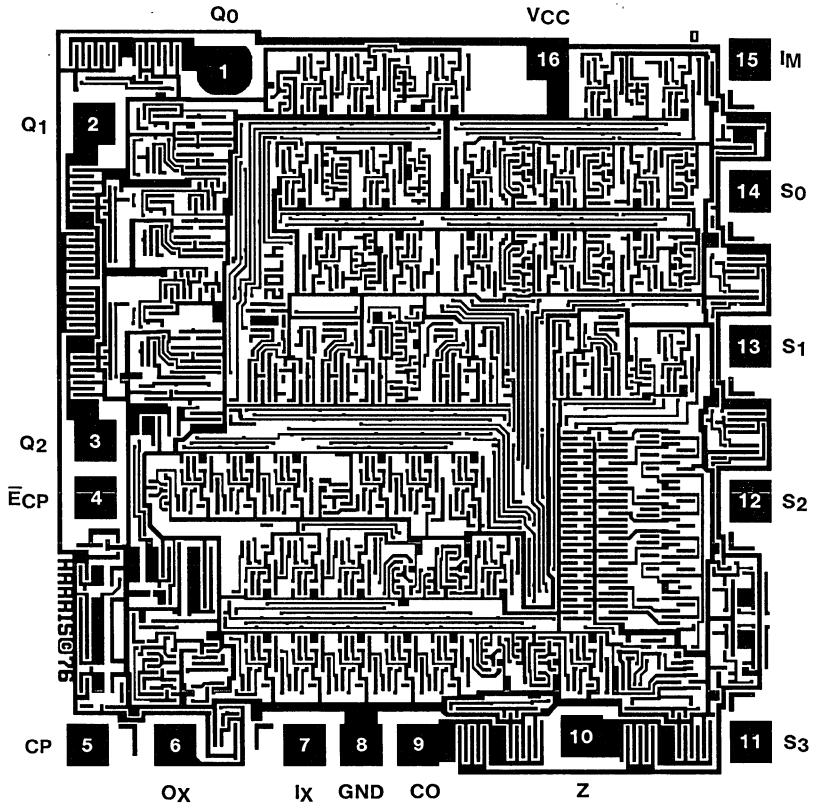
GLASSIVATION:
Type: SiO_2
Thickness: 7kÅ - 9kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$7.1 \times 10^4 A/cm^2$

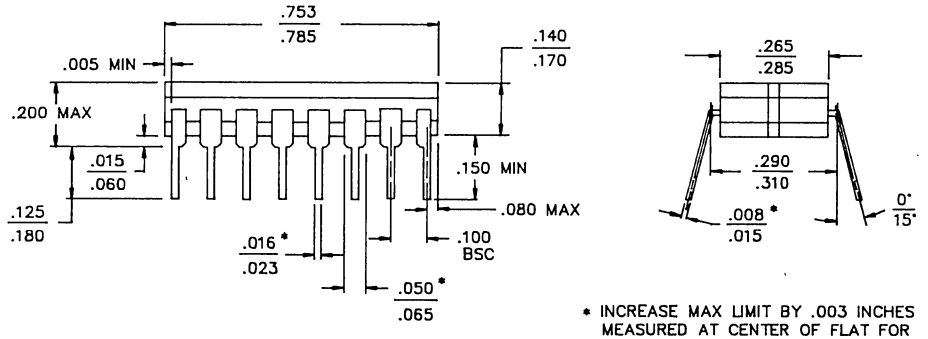
Metallization Mask Layout

HD-4702/883



Packaging†

16 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

DESIGN INFORMATION

CMOS Programmable Bit Rate Generator

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Application Information

Single Channel Bit Rate Generator

Figure 1 shows the simplest application of the HD-4702. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 Baud. For many low cost terminals, these five bit rates are adequate.

Simultaneous Generation of Several Bit Rates

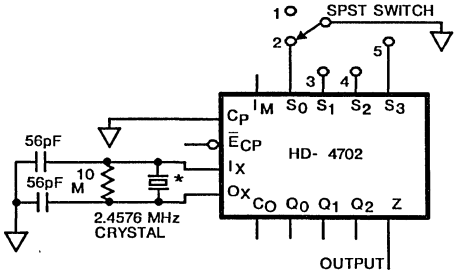
Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one HD-4702 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select Inputs of the multiplexer causes the HD-4702 to interrogate sequentially eight different frequency signals. The 93L34 8-bit addressable Latch, addressed by the same Scan Counter Outputs, re-converts the multiplexed single Output (Z) of the HD-4702 into eight parallel output frequency signals. In the simple scheme of Figure 2, input S_3 is left open (HIGH) and the following bit rates are generated:

Q_0: 110 Baud	Q_1: 9600 Baud	Q_2: 4800 Baud
Q_3: 1800 Baud	Q_4: 1200 Baud	Q_5: 2400 Baud
Q_6: 300 Baud	Q_7: 150 Baud	

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.

19200 Baud Operation

Though a 19200 Baud signal is not internally routed to the multiplexer, the HD-4702 can be used to generate this bit rate by connecting the Q_2 output to I_M input and applying select code. An additional 2-input NOR gate can be used to retain the "Zero Baud" feature on select code 1 for the HD-4702 (See Figure 3).



SWITCH POSITION	HD-4702 BIT RATE
1	110 Baud
2	150 Baud
3	300 Baud
4	1200 Baud
5	2400 Baud

FIGURE 1. SWITCH SELECTABLE BIT RATE GENERATOR CONFIGURATION PROVIDING FIVE BIT RATES.

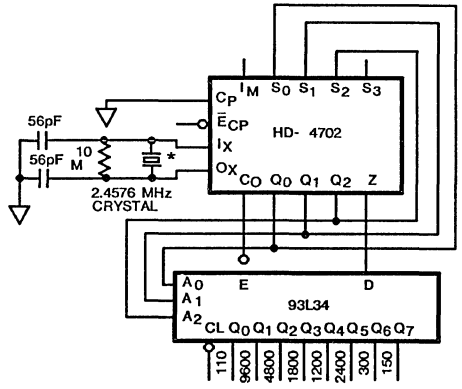


FIGURE 2. BIT RATE GENERATOR CONFIGURATION WITH EIGHT SIMULTANEOUS FREQUENCIES.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

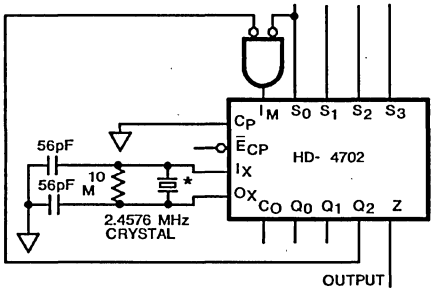


FIGURE 3. 19200 BAUD OPERATION

* See Figure 4

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576MHz "AT" Cut
Series Resistance (Max)	250
Unwanted Modes	-6.0dB (Min)
Type of Operation	Parallel
Load Capacitance	32pF +0.5

FIGURE 4. CRYSTAL SPECIFICATIONS

HARRIS

HD-6402/883

CMOS Universal Asynchronous Receiver Transmitter (UART)

June 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **8.0MHz Operating Frequency (HD-6402B/883)**
- **2.0MHz Operating Frequency (HD-6402R/883)**
- **Low Power CMOS Design**
- **Programmable Word Length, Stop Bits and Parity**
- **Automatic Data Formatting and Status Generation**
- **Compatible with Industry Standard UARTs**
- **Single +5V Power Supply**
- **CMOS/TTL Compatible Inputs**

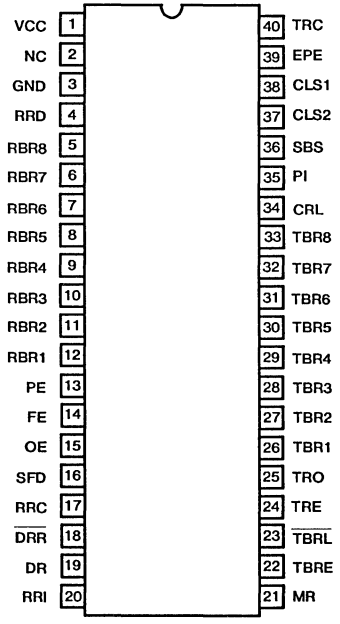
Description

The HD-6402/883 is a CMOS UART for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity and stop bits. The data word length can be 5, 6,7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bit code.

The HD-6402/883 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. Utilizing the Harris advanced scaled SAJI IV CMOS process permits operation clock frequencies up to 8.0MHz (500K Baud). Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

Pinout

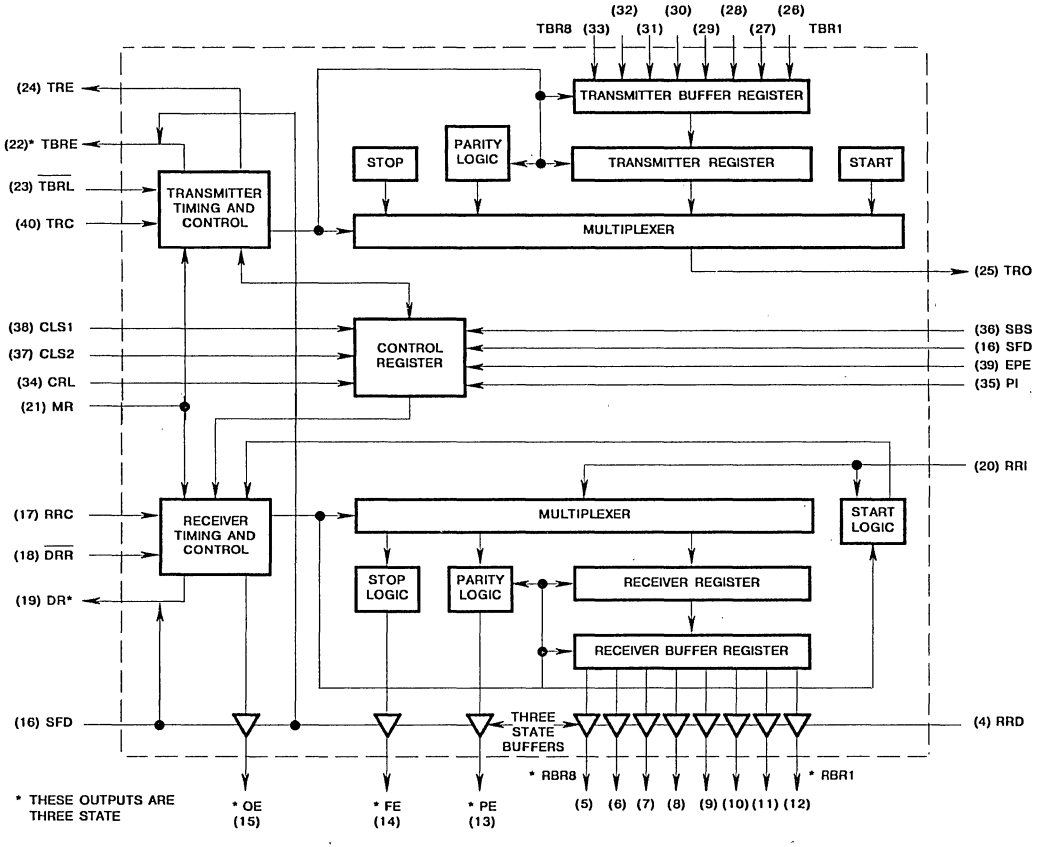
HD1-6402/883 (CERAMIC DIP)
TOP VIEW



Control Definition

CONTROL WORD					CHARACTER FORMAT			
CLS2	CLS1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	X	0	1	5	NONE	1
0	0	1	X	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	X	0	1	6	NONE	1
0	1	1	X	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	X	0	1	7	NONE	1
1	0	1	X	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	X	0	1	8	NONE	1
1	1	1	X	1	1	8	NONE	2

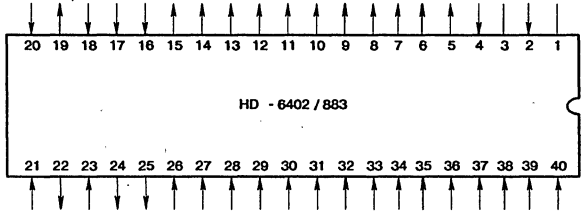
Functional Diagram



Pin Description

PIN	TYPE	SYMBOL	DESCRIPTION
1		VCC*	Positive Voltage Supply
2		NC	No Connection
3		GND	Ground
4	I	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding outputs RBR1-RBR8 to high impedance state.
5	O	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	O	RBR7	See Pin 5-RBR8
7	O	RBR6	See Pin 5-RBR8
8	O	RBR5	See Pin 5-RBR8
9	O	RBR4	See Pin 5-RBR8
10	O	RBR3	See Pin 5-RBR8
11	O	RBR2	See Pin 5-RBR8
12	O	RBR1	See Pin 5-RBR8
13	O	PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.
14	O	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
15	O	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register.
16	I	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	I	RRC	The Receiver register clock is 16X the receiver data rate.
18	I	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output DR to a low level.
19	O	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	I	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	I	MR	A high level on MASTER RESET clears PE, FE, OE and DR to a low level and sets the transmitter register empty (TRE) to a high level 18 clock cycles after MR falling edge. MR does not clear the receiver buffer register. This input must be pulsed at least once after power up. The HD-6402/883 must be master reset after power up. The reset pulse should meet VIH and t_{MR}. Wait 18 clock cycles after the falling edge of MR before beginning operation.
22	O	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.

* A 0.1 µF decoupling capacitor from the VCC pin to the GND is recommended.



PIN	TYPE	SYMBOL	DESCRIPTION
23	I	$\overline{TBRL}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{TBRL}$ initiates data transfer to the transmitter register. If busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	O	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	O	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	I	TRB1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8 bits the TBR8, 7 and 6 inputs are ignored corresponding to their programmed word length.
27	I	TBR2	See Pin 26-TBR1.
28	I	TBR3	See Pin 26-TBR1.
29	I	TBR4	See Pin 26-TBR1.
30	I	TBR5	See Pin 26-TBR1.
31	I	TBR6	See Pin 26-TBR1.
32	I	TBR7	See Pin 26-TBR1.
33	I	TBR8	See Pin 26-TBR1.
34	I	CRL	A high level on CONTROL REGISTER LOAD loads the control register with the control word. The control word is latched on the falling edge of CRL.
35	I	PI	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	I	SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths.
37	I	CLS2	These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits.)
38	I	CLS1	See Pin 37-CLS2.
39	I	EPE	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	I	TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec)..... +300°C
ESD Classification ..... Class 1
Typical Derating Factor ..... 1mA/MHz Increase in ICCOP

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	48.3°C/W	14.8°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.03W
Gate Count ..... 1643 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

TABLE 1. HD-6402R/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical "1" Input Voltage	VIH	VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.3	-	V
Logical "0" Input Voltage	VIL	VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.8	V
Input Leakage Current	II	VIN = GND or VCC, VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	1.0	µA
Logical "1" Output Voltage	VOH	IOH = -2.5mA, VCC = 4.5V, (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	3.0	-	V
Logical "1" Output Voltage	VOH	IOH = -100µA, VCC = 4.5V, (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC -0.4	-	V
Logical "0" Output Voltage	VOL	IOL = +2.5mA, VCC = 4.5V, (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output Leakage Current	IO	VO = GND or VCC, VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	1.0	µA
Standby Supply Current	ICCSB	VIN = GND or VCC; VCC = 5.5V Output Open	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	100	µA

TABLE 2. HD-6402R/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

A.C. PARAMETERS	SYMBOL	(NOTE 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Clock Frequency	(1) f_{CLOCK}	VCC = 4.5V CL = 50pF	9, 10,11	$-55°C \leq T_A \leq +125°C$	-	2.0	MHz
Pulse Widths, $\overline{CRL}$, $\overline{DRR}$, $\overline{TBRL}$	(2) t_{PW}		9, 10, 11	$-55°C \leq T_A \leq +125°C$	150	-	ns
Pulse Width MR	(3) t_{MR}		9, 10, 11	$-55°C \leq T_A \leq +125°C$	150	-	ns
Input Data Setup Time	(4) t_{SET}		9, 10, 11	$-55°C \leq T_A \leq +125°C$	50	-	ns
Input Data Hold Time	(5) t_{HOLD}		9, 10, 11	$-55°C \leq T_A \leq +125°C$	60	-	ns
Output Enable Time	(6) t_{EN}		9, 10, 11	$-55°C \leq T_A \leq +125°C$	-	160	ns

NOTES: 1. Interchanging of force and sense conditions is permitted.

2. Tested with input levels of VIH = 2.76V and VIL = 0.4V. Rise and fall times are driven at 1ns/V.

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. HD-6402R/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

A.C. PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	f = 1MHz All Measurements are Referenced to Device GND	3	$T_A = +25^oC$	-	25.0	pF
Output Capacitance	CO		3	$T_A = +25^oC$	-	25.0	pF
Operating Supply Current	ICCOP	VCC = 5.5V, Clock Freq. = 2MHz VIN = VCC or GND, Outputs Open	3	$-55^oC \leq T_A \leq +125^oC$	-	2.0	mA

NOTE: 3. The Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1
Typical Derating Factor ..... 1mA/MHz Increase in ICCOP

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	48.3°C/W	14.8°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.03W
Gate Count ..... 1643 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

TABLE 1. HD-6402B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical "1" Input Voltage	VIH	VCC = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	2.3	-	V
Logical "0" Input Voltage	VIL	VCC = 4.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.8	V
Input Leakage Current	II	VIN = GND or VCC, VCC = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	1.0	µA
Logical "1" Output Voltage	VOH	IOH = -2.5mA, VCC = 4.5V, (Note 1)	1, 2, 3	$-55°C \le T_A \le +125°C$	3.0	-	V
Logical "1" Output Voltage	VOH	IOH = -100µA, VCC = 4.5V, (Note 1)	1, 2, 3	$-55°C \le T_A \le +125°C$	VCC -0.4	-	V
Logical "0" Output Voltage	VOL	IOL = +2.5mA, VCC = 4.5V, (Note 1)	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Output Leakage Current	IO	VO = GND or VCC, VCC = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	1.0	µA
Standby Supply Current	ICCSB	VIN = GND or VCC; VCC = 5.5V Output Open	1, 2, 3	$-55°C \le T_A \le +125°C$	-	100	µA

TABLE 2. HD-6402B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

A.C. PARAMETERS	SYMBOL	(NOTE 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Clock Frequency	(1) f_{CLOCK}	VCC = 4.5V CL = 50pF	9, 10,11	$-55°C \le T_A \le +125°C$	-	8.0	MHz
Pulse Widths, CRL, $\overline{DRR}$, $\overline{TBRL}$	(2) t_{PW}		9, 10, 11	$-55°C \le T_A \le +125°C$	75	-	ns
Pulse Width MR	(3) t_{MR}		9, 10, 11	$-55°C \le T_A \le +125°C$	150	-	ns
Input Data Setup Time	(4) t_{SET}		9, 10, 11	$-55°C \le T_A \le +125°C$	20	-	ns
Input Data Hold Time	(5) t_{HOLD}		9, 10, 11	$-55°C \le T_A \le +125°C$	20	-	ns
Output Enable Time	(6) t_{EN}		9, 10, 11	$-55°C \le T_A \le +125°C$	-	35	ns

NOTES: 1. Interchanging of force and sense conditions is permitted.

2. Tested with input levels of VIH = 2.76V and VIL = 0.4V. Rise and fall times are driven at 1ns/V.

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. HD-6402B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

A.C. PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	f = 1MHz All Measurements are Referenced to Device GND	3	$T_A = +25^oC$	-	25.0	pF
Output Capacitance	CO		3	$T_A = +25^oC$	-	25.0	pF
Operating Supply Current	ICCOP	VCC = 5.5V, Clock Freq. = 2MHz VIN = VCC or GND, Outputs Open	3	$-55^oC \leq T_A \leq +125^oC$	-	2.0	mA

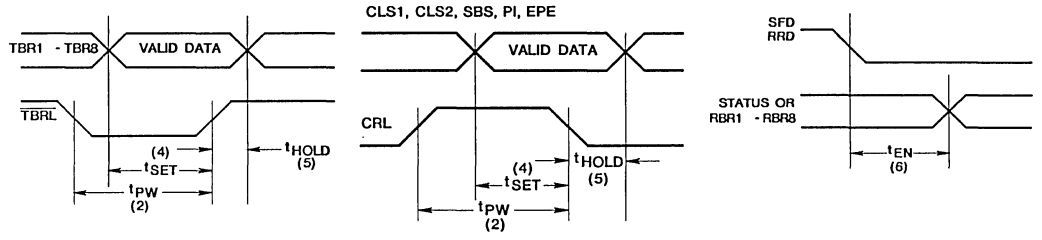
NOTE: 3. The Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Switching Waveforms

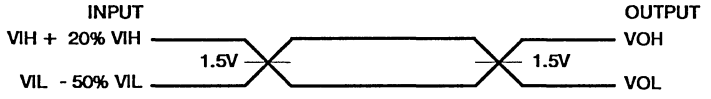


DATA INPUT CYCLE

CONTROL REGISTER LOAD CYCLE

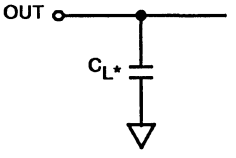
STATUS FLAG OUTPUT ENABLE TIME OR DATA OUTPUT ENABLE TIME

A.C. Testing Input, Output Waveform



A.C. Testing: All input signals must switch between VIL - 50% VIL and VIH + 20% VIH. Input rise and fall times are driven at 1ns/V.

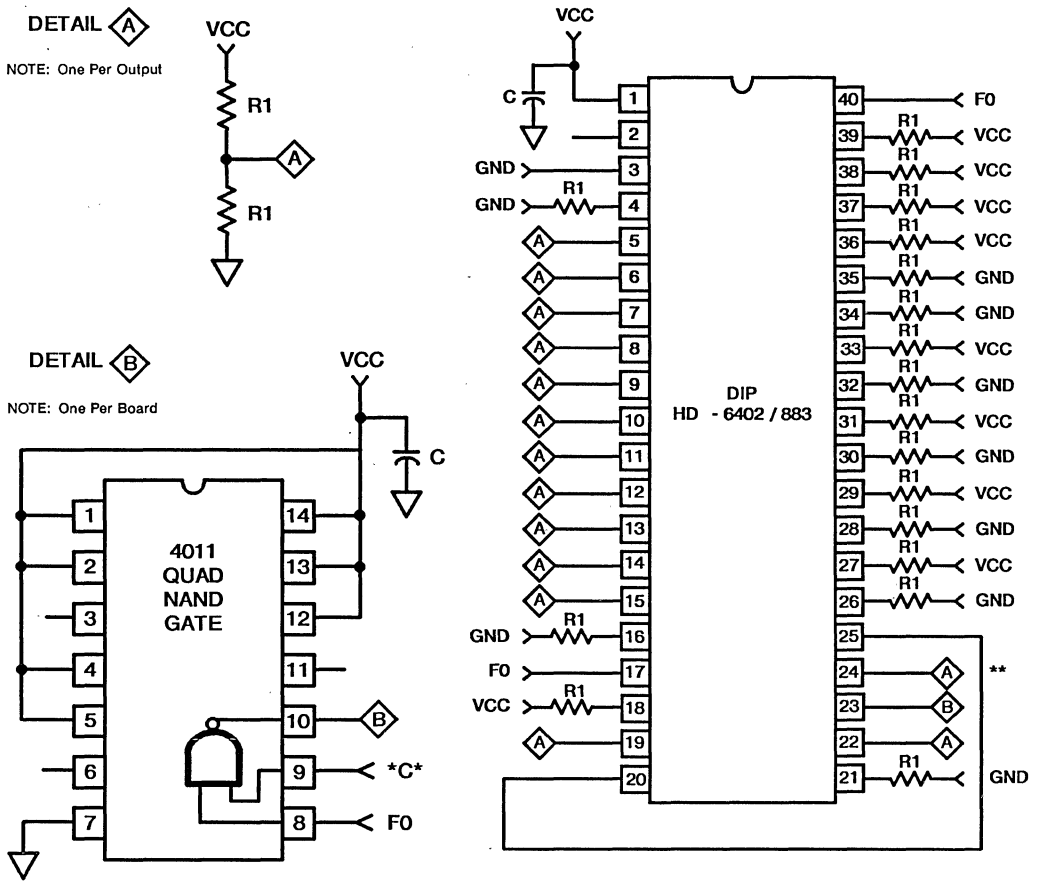
Test Circuit



* Includes stray and jig capacitance, CL = 50pF

Burn-In Circuits

HD-6402/883 CERAMIC DIP



NOTES:
VCC = 5.5V ± 0.5V
F0 = 100kHz ± 10%
R1 = 47kΩ, 1/4W ± 10%
C = 0.01μF minimum
** One socket per board should not be loaded, but rather have pin 24 go the "C" of the 4011.

Metallization Topology

DIE DIMENSIONS: 126.4 x 134.3 x 19 ± 1mils

METALLIZATION:
Type: Si-Al
Thickness: 10kÅ - 12kÅ

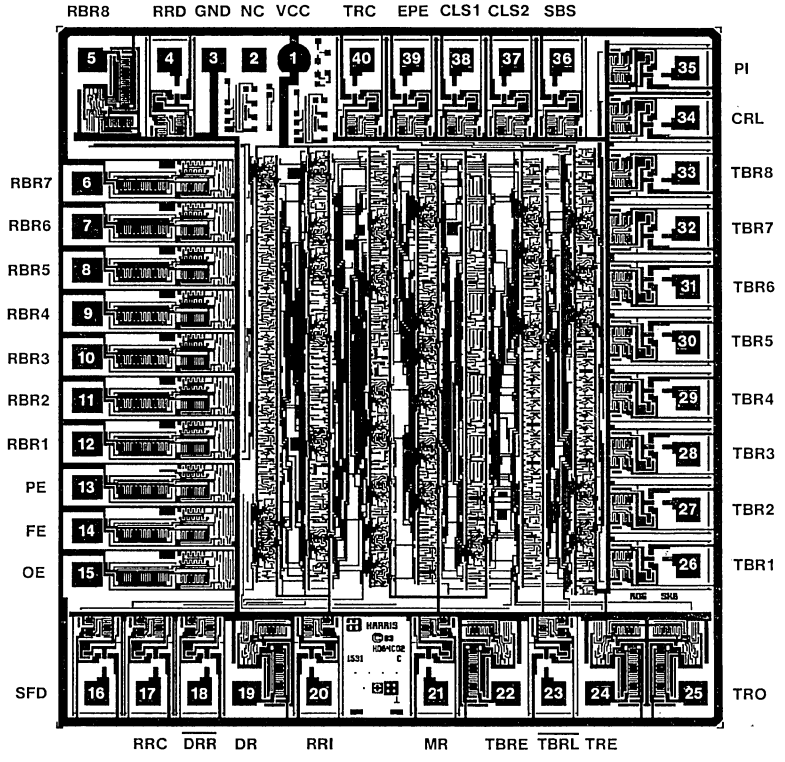
GLASSIVATION:
Type: SiO_2
Thickness: 7kÅ - 9kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY: 1.42 x 10^5 A/cm^2

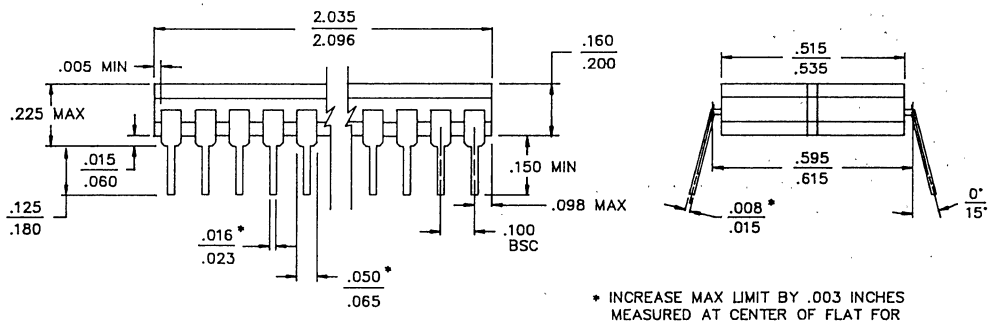
Metallization Mask Layout

HD-6402/883



Packaging†

40 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-5

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

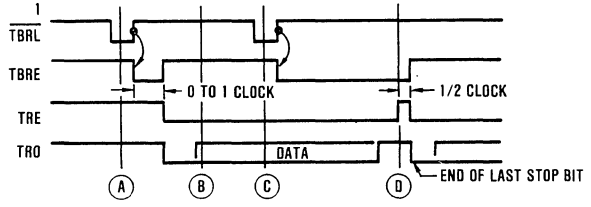
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Transmitter Operation

The transmitter section accepts parallel data, formats the data and transmits the data in serial form on the Transmitter Register Output (TRO) terminal (See serial data format). Data is loaded from the inputs TBR1-TBR8 into the Transmitter Buffer Register by applying a logic low on the Transmitter Buffer Register Load ($\overline{TBRL}$) input (A). Valid data must be present at least t_{set} prior to and t_{hold} following the rising edge of $\overline{TBRL}$. If words less than 8 bits are used, only the least significant bits are transmitted. The character is right justified, so the least significant bit corresponds to TBR1 (B).

The rising edge of $\overline{TBRL}$ clears Transmitter Buffer Register Empty (TBRE). 0 to 1 Clock cycles later, data is transferred to the transmitter register, the Transmitter Register Empty (TRE) pin goes to a low state, TBRE is set high and serial data information is transmitted. The output data is clocked by Transmitter Register Clock (TRC) at a clock rate 16 times the data rate. A second low level pulse on $\overline{TBRL}$ loads data into the Transmitter Buffer Register (C). Data transfer to the transmitter register is delayed until transmission of the current data is complete (D). Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.

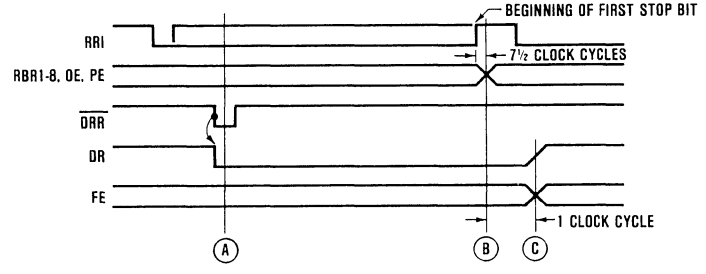
TRANSMITTER TIMING (NOT TO SCALE)



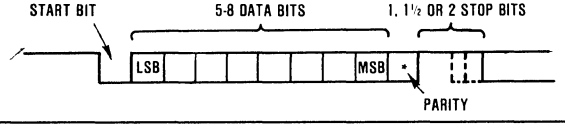
Receiver Operation

Data is received in serial form at the Receiver Register Input (RRI). When no data is being received, RRI must remain high. The data is clocked through the Receiver Register Clock (RRC). The clock rate is 16 times the data rate. A low level on Data Received Reset ($\overline{DRR}$) clears the Data Receiver (DR) line (A). During the first stop bit data is transferred from the Receiver Register to the Receiver Buffer Register (RBR) (B). If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on Overrun Error (OE) indicates overruns. An overrun occurs when DR has not been cleared before the present character was transferred to the RBR. One clock cycle later DR is reset to a logic high, and Framing Error (FE) is evaluated (C). A logic high on FE indicates an invalid stop bit was received, a framing error. A logic high on Parity Error (PE) indicates a parity error.

RECEIVER TIMING (NOT TO SCALE)



SERIAL DATA FORMAT



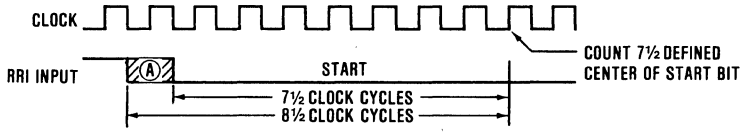
*IF ENABLED

DESIGN INFORMATION (Continued)

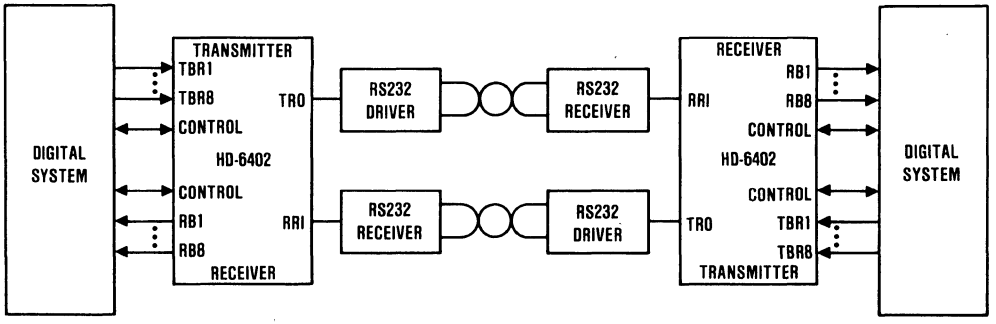
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Start Bit Detection

The receiver uses a 16X clock timing. The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion (A). The center of the start bit is defined as clock count 7 1/2. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±1/2 clock cycle, ±1/32 bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.



Interfacing With The HD-6402



TYPICAL SERIAL DATA LINK

HARRIS

HD-6409/883

June 1989

CMOS Manchester Encoder-Decoder

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Converter or Repeater Mode
- Independent Manchester Encoder and Decoder Operation
- Static to One Megabit/sec Data Rate Guaranteed
- Low Bit Error Rate
- Digital PLL Clock Recovery
- On Chip Oscillator
- Low Operating Power: 50mW Typical at +5V
- Available in 20 Pin Dual-In-Line and 20 Pad LCC Package

Description

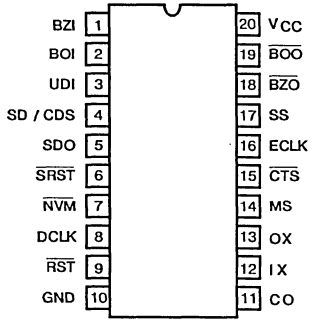
The HD-6409/883 Manchester Encoder-Decoder (MED) is a high speed, low power device manufactured using self-aligned silicon gate technology. The device is intended for use in serial data communication, and can be operated in either of two modes. In the converter mode, the MED converts Nonreturn-to-Zero code (NRZ) into Manchester code and decodes Manchester code into Nonreturn-to-Zero code. For serial data communication, Manchester code does not have some of the deficiencies inherent in Nonreturn-to-Zero code. For instance, use of the MED on a serial line eliminates DC components, provides clock recovery, and gives a relatively high degree of noise immunity. Because the MED converts the most commonly used code (NRZ) to Manchester code, the advantages of using Manchester code are easily realized in a serial data link.

In the Repeater mode, the MED accepts Manchester code input and reconstructs it with a recovered clock. This minimizes the effects of noise on a serial data link. A digital phase lock loop generates the recovered clock. A maximum data rate of 1MHz requires only 50mW of power.

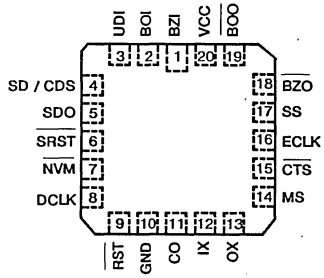
Manchester code is used in magnetic tape recording and in fiber optic communication, and generally is used where data accuracy is imperative. Because it frames blocks of data, the HD-6409/883 easily interfaces to protocol controllers.

Pinouts

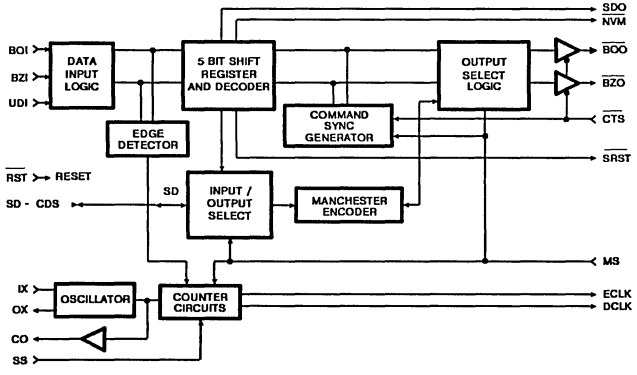
HD1-6409/883 (CERAMIC DIP)
TOP VIEW



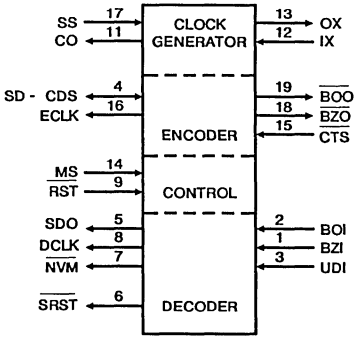
HD4-6409/883 (CERAMIC LCC)
TOP VIEW



Block Diagram



Logic Symbol



Pin Description

PIN NUMBER	TYPE	SYMBOL	NAME	DESCRIPTION
1	I	BZI	Bipolar Zero Input	Used in con unction with pin 2, Bipolar One Input (BOI), to input Manchester II encoded data to the decoder, BZI and BOI are logical complements. When using pin 3, Unipolar Data Input (UDI) for data input, BZI must be held high.
2	I	BOI	Bipolar One Input	Used in con unction with pin 1, Bipolar Zero Input (BZI), to input Manchester II encoded data to the decoder, BOI and BZI are logical complements. When using pin 3, Unipolar Data Input (UDI) for data input, BOI must be held low.
3	I	UDI	Unipolar Data Input	An alternate to bipolar input (BZI, BOI), Unipolar Data Input (UDI) is used to input Manchester II encoded data to the decoder. When using pin 1 (BZI) and pin 2 (BOI) for data input, UDI must be held low.
4	I/O	SD/CDS	Serial Data/Command Data Sync	In the converter mode, SD/CDS is an input used to receive serial NRZ data. NRZ data is accepted synchronously on the falling edge of encoder clock output (ECLK). In the repeater mode, SD/CDS is an output indicating the status of last valid sync pattern received. A high indicates a command sync and a low indicates a data sync pattern.
5	O	SDO	Serial Data Out	The decoded serial NRZ data is transmitted out synchronously with the decoder clock (DCLK). SDO is forced low when $\overline{RST}$ is low.
6	O	$\overline{SRST}$	Serial Reset	In the converter mode, $\overline{SRST}$ follows $\overline{RST}$. In the repeater mode, when $\overline{RST}$ goes low, $\overline{SRST}$ goes low and remains low after $\overline{RST}$ goes high. $\overline{SRST}$ goes high only when $\overline{RST}$ is high, the reset bit is zero, and a valid synchronization sequence is received.
7	O	$\overline{NVM}$	Nonvalid Manchester	A low on $\overline{NVM}$ indicates that the decoder has received invalid Manchester data and present data on Serial Data Out (SDO) is invalid. A high indicates that the sync pulse and data were valid and SDO is valid. $\overline{NVM}$ is set low by a low on $\overline{RST}$, and remains low after $\overline{RST}$ goes high until valid sync pulse followed by two valid Manchester bits is received.
8	O	DCLK	Decoder Clock	The decoder clock is a 1X clock recovered from BZI and BOI to synchronously output received NRZ data (SDO).
9	I	$\overline{RST}$	Reset	In the converter mode, a low on $\overline{RST}$ forces SDO, DCLK, $\overline{NVM}$, and $\overline{SRST}$ low. A high on $\overline{RST}$ enables SDO and DCLK, and forces $\overline{SRST}$ high. $\overline{NVM}$ remains low after $\overline{RST}$ goes high until a valid sync pulse followed by two Manchester bits is received, after which it goes high. In the repeater mode, $\overline{RST}$ has the same effect on SDO, DCLK and $\overline{NVM}$ as in the converter mode. When $\overline{RST}$ goes low, $\overline{SRST}$ goes low and remains low after $\overline{RST}$ goes high. $\overline{SRST}$ goes high only when $\overline{RST}$ is high, the reset bit is zero and a valid synchronization sequence is received.

(I) Input (O) Output

Pin Description (Continued)

PIN NUMBER	TYPE	SYMBOL	NAME	DESCRIPTION
10	I	GND	Ground	Ground
11	O	C_O	Clock Output	Buffered output of clock input I_X. May be used as clock signal for other peripherals.
12	I	I_X	Clock Input	I_X is the input for an external clock or, if the internal oscillator is used, I_X and O_X are used for the connection of the crystal.
13	O	O_X	Clock Drive	If the internal oscillator is used, O_X and I_X are used for the connection of the crystal.
14	I	MS	Mode Select	MS must be held low for operation in the converter mode, and high for operation in the repeater mode.
15	I	$\overline{CTS}$	Clear to Send	In the converter mode, a high disables the encoder, forcing outputs $\overline{BOO}$, $\overline{BZO}$ high and ECLK low. A high to low transition of $\overline{CTS}$ initiates transmission of a Command sync pulse. A low on $\overline{CTS}$ enables $\overline{BOO}$, $\overline{BZO}$, and ECLK. In the repeater mode, the function of $\overline{CTS}$ is identical to that of the converter mode with the exception that a transition of $\overline{CTS}$ does not initiate a synchronization sequence.
16	O	ECLK	Encoder Clock	In the converter mode, ECLK is a 1X clock output used to receive serial NRZ data to SD/CDS. In the repeater mode, ECLK is a 2X clock which is recovered from BZI and BOI data by the digital phase locked loop.
17	I	SS	Speed Select	A logic high on SS sets the data rate at 1/32 times the clock frequency while a low sets the data rate at 1/16 times the clock frequency.
18	O	$\overline{BZO}$	$\overline{Bipolar\ Zero\ Output}$	$\overline{BZO}$ and its logical complement $\overline{BOO}$ are the Manchester data outputs of the encoder. The inactive state for these outputs is in the high state.
19	O	$\overline{BOO}$	$\overline{Bipolar\ One\ Out}$	See pin 18.
20	I	VCC	VCC	VCC is the +5V power supply pin. A 0.1 µF decoupling capacitor from VCC (pin-20) to GND (pin-10) is recommended.

(I) Input (O) Output

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec)..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	83°C/W	23°C/W
Ceramic LCC Package	84°C/W	24°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 602mW
Ceramic LCC Package 595mW
Gate Count ..... 250 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Voltage Range ..... +4.5V to +5.5V
Input Rise and Fall Times ..... 50ns Max

Sync. Transition Span (t2)..... 1.5 DBP Typical, (Notes 1, 2)
Short Data Transition Span (t4) ..... 0.5 DBP Typical, (Notes 1, 2)
Long Data Transition Span (t5)..... 1.0 DBP Typical, (Notes 1, 2)
Zero Crossing Tolerance (tCD5) ..... (Note 3)

NOTES: 1. DBP-Data Bit Period, Clock Rate = 16X, one DBP = 16 Clock Cycles; Clock Rate = 32X, one DBP = 32 Clock Cycles.

2. The input conditions specified are nominal values, the actual input waveforms transition spans may vary by ± 2 I_X clock cycles (16X mode) or ± 6 I_X clock cycles (32X mode).

3. The maximum zero crossing tolerance is ± 2 I_X clock cycles (16X mode) or ± 6 I_X clock cycles (32 mode) from the nominal.

TABLE 1. HD-6409/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logic '1' Input Voltage	VIH	VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	70% VCC	-	V
Logic '0' Input Voltage	VIL	VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	20%VCC	V
Logic '1' Input Voltage ($\overline{\text{Reset}}$)	VIHR	VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC -0.5	-	V
Logic '0' Input Voltage ($\overline{\text{Reset}}$)	VILR	VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	GND +0.5	V
Logic '1' Input Voltage (Clock)	VIHC	VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC -0.5	-	V
Logic '0' Input Voltage (Clock)	VILC	VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	GND +0.5	V
Input Leakage Current (Except I_X)	II	VIN = VCC or GND VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Input Leakage Current (I_X)	II	VIN = VCC or GND VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-20	+20	µA
I/O Leakage Current	IO	VOUT = VCC or GND VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-10	+10	µA
Output HIGH Voltage (All except O_X)	VOH	IOH = -2.0mA VCC = 4.5V (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC -0.4	-	V
Output LOW Voltage (All except O_X)	VOL	IOL = +2.0mA VCC = 4.5V (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Standby Power Supply Current	ICCSB	VIN = VCC or GND, VCC = 5.5V, Outputs Open	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	100	µA
Operating Power Supply Current	ICCOP	f = 16.0MHz, VIN = VCC or GND VCC = 5.5V, CL = 50pF	1, 2 ,3	$-55°C \leq T_A \leq +125°C$	-	18.0	mA
Functional Test	FT	(Note 2)	7, 8	$-55°C \leq T_A \leq +125°C$	-	-	-

NOTES: 1. Interchanging of force and sense conditions is permitted.

2. Tested as follows: f = 16MHz, VIH = 70% VCC, VIL = 20% VCC, VOH ≥ VCC/2, and VOL ≤ VCC/2, VCC = 4.5V and 5.5V.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. HD-6409/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Clock Frequency	f_C		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	16	MHz
Clock Period	t_C		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	$1/f_C$	-	sec
Bipolar Pulse Width	t_1		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	t_C+10	-	ns
One-Zero Overlap	t_3		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	t_C-10	ns
Clock High Time	t_{CH}	f=16.0MHz	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
Clock Low Time	t_{CL}	f=16.0MHz	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
Serial Data Setup Time	t_{CE1}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Serial Data Hold Time	t_{CE2}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
DCLK to SDO, $\overline{NVM}$	t_{CD2}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
ECLK to $\overline{BZO}$	t_{R2}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	ns

NOTES: 1. AC Testing as follows: f = 4.0MHz, VIH = 70% VCC, VIL = 20% VCC, Speed Select = 16X, VOH $\geq$ VCC/2, VOL $\leq$ VCC/2, VCC = 4.5V and 5.5V, Input rise and fall times driven at 1ns/V, Output load = 50pF.

TABLE 3. HD-6409/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, f = 1MHz All Measurements are referenced to device GND	1, 2	$T_A = +25^oC$	-	10	pF
I/O Capacitance	CI/O		1, 2	$T_A = +25^oC$	-	12	pF
Output Rise Time (All except Clock)	t_r	From 1.0 to 3.5V CL = 50pF	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Output Fall Time (All except Clock)	t_f	From 3.5 to 1.0V CL = 50pF	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Clock Output Rise Time	t_r	From 1.0 to 3.5V CL = 20pF	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	11	ns
Clock Output Fall Time	t_f	From 3.5 to 1.0V CL = 20pF	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	11	ns
ECLK to $\overline{BZO}$, $\overline{BOO}$	t_{CE3}		1, 3	$-55^oC \leq T_A \leq +125^oC$	0.5	1.0	DBP
$\overline{CTS}$ Low to $\overline{BZO}$ $\overline{BOO}$ Enabled	t_{CE4}		1, 3	$-55^oC \leq T_A \leq +125^oC$	0.5	1.5	DBP
$\overline{CTS}$ Low to ECLK Enabled	t_{CE5}		1, 3	$-55^oC \leq T_A \leq +125^oC$	10.5	11.5	DBP
$\overline{CTS}$ High to ECLK Disabled	t_{CE6}		1, 3	$-55^oC \leq T_A \leq +125^oC$	-	1.0	DBP
$\overline{CTS}$ High to $\overline{BZO}$ $\overline{BOO}$ Disabled	t_{CE7}		1, 3	$-55^oC \leq T_A \leq +125^oC$	1.5	2.5	DBP
UDI to SDO, $\overline{NVM}$	t_{CD1}		1, 3	$-55^oC \leq T_A \leq +125^oC$	2.5	3.0	DBP
$\overline{RST}$ Low to DCLK, SDO, $\overline{NVM}$ Low	t_{CD3}		1, 3	$-55^oC \leq T_A \leq +125^oC$	0.5	1.5	DBP
$\overline{RST}$ High to DCLK, Enabled	t_{CD4}		1, 3	$-55^oC \leq T_A \leq +125^oC$	0.5	1.5	DBP
UDI to $\overline{BZO}$, $\overline{BOO}$	t_{R1}		1, 3	$-55^oC \leq T_A \leq +125^oC$	0.5	1.0	DBP
UDI to SDO, $\overline{NVM}$	t_{R3}		1, 3	$-55^oC \leq T_A \leq +125^oC$	2.5	3.0	DBP

NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested.

2. Guaranteed via characteristics at initial device design and after major process and/or design changes.

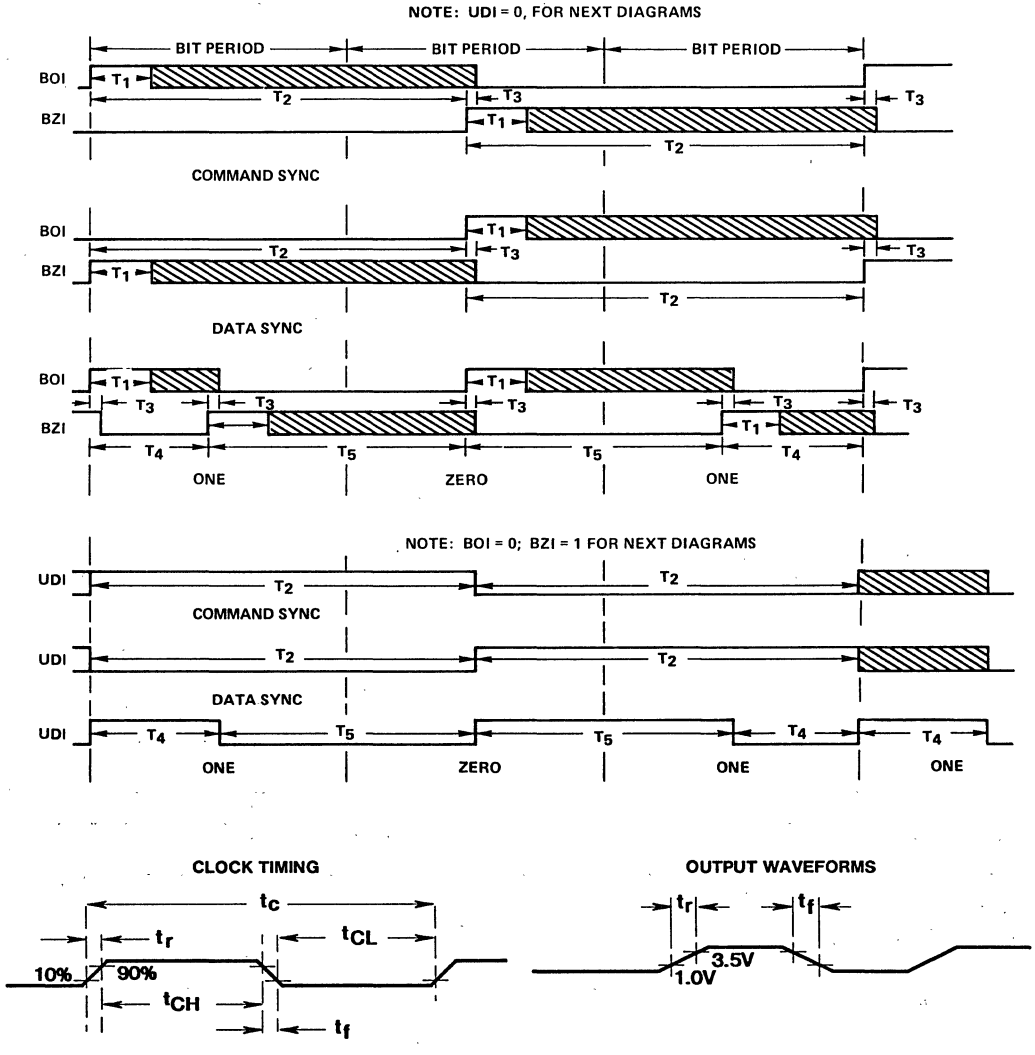
3. DBP-Data Bit Period, Clock Rate = 16X, one DBP = 16 Clock Cycles; Clock Rate = 32X, one DBP = 32 Clock Cycles.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 4. APPLICABLE SUBGROUPS

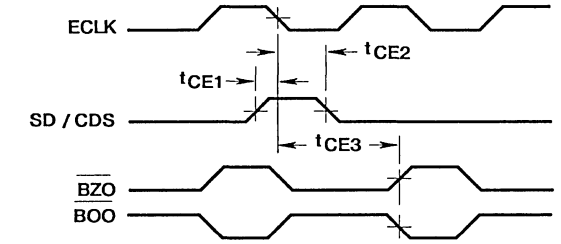
CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

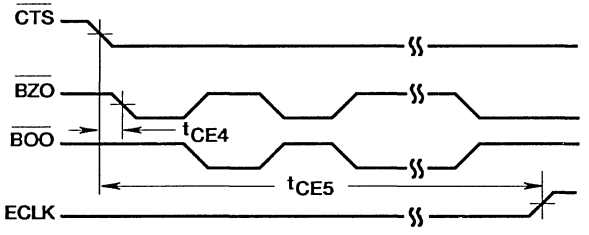
Timing Waveforms

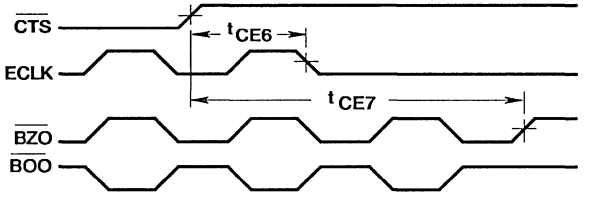


Timing Waveforms (Continued)

ENCODER TIMING

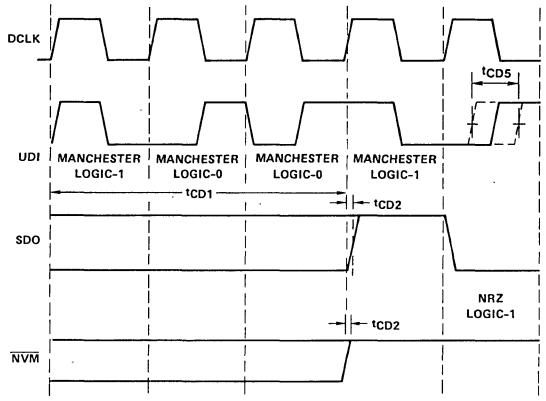




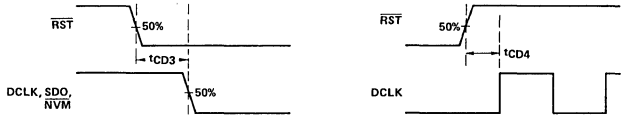


Timing Waveforms (Continued)

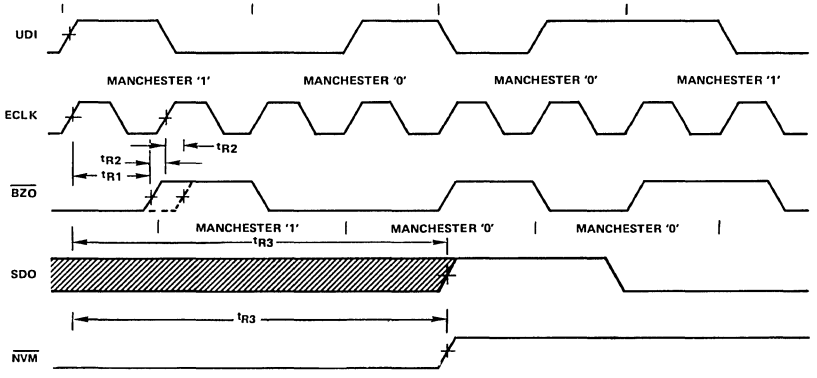
DECODER TIMING



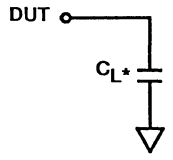
NOTE: Manchester Data In is not synchronous with Decoder Clock. Decoder Clock is synchronous with decoded NRZ out of SDO.



REPEATER TIMING



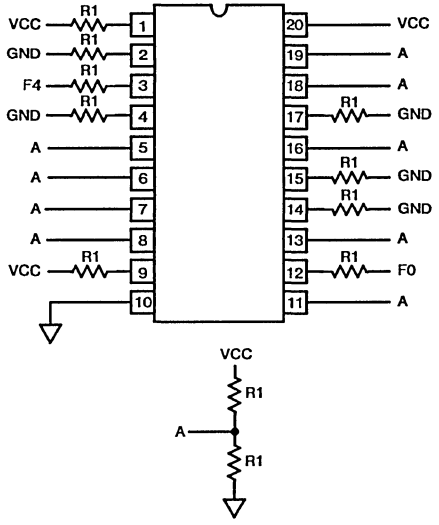
Test Load Circuit



* INCLUDES STRAY AND JIG CAPACITANCE

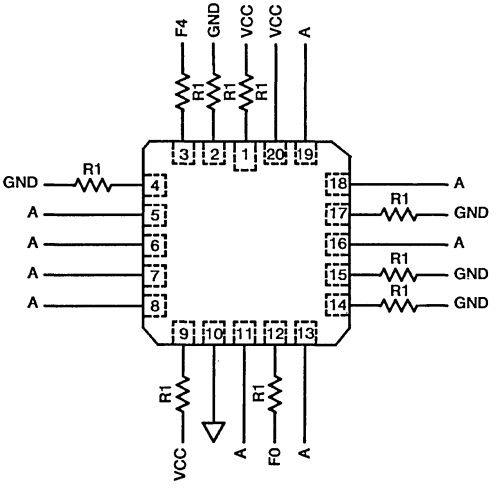
Burn-In Circuits

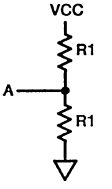
HD-6409/883 CERAMIC DIP



NOTES:
VCC = 5.5V ±0.5V
VIH = 4.5V ±10%
VIL = -0.2V to 0.4V
R1 = 47kΩ ±5%
F0 = 100kHz ±10%
F4 = F0/16

HM-6409/883 CERAMIC LCC





NOTES:
VCC = 5.5V ±0.5V
VIH = 4.5V ±10%
VIL = -0.2V to 0.4V
R1 = 47KΩ ±5%
F0 = 100kHz ±10%
F4 = F0/16

Metallization Topology

DIE DIMENSIONS:
88 x 78 x 19 ±1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: Metal 1: 8kÅ ± 1kÅ
Metal 2: 16kÅ ± 1kÅ

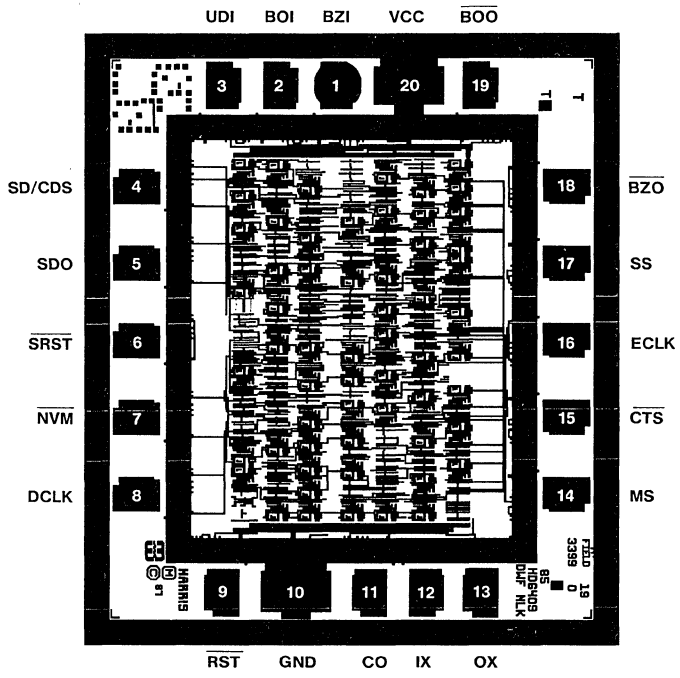
GLASSIVATION:
Type: Si_3N_4 • SiO_x
Thickness: 10kÅ ± 2kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
0.8 x 10^5 A/cm^2

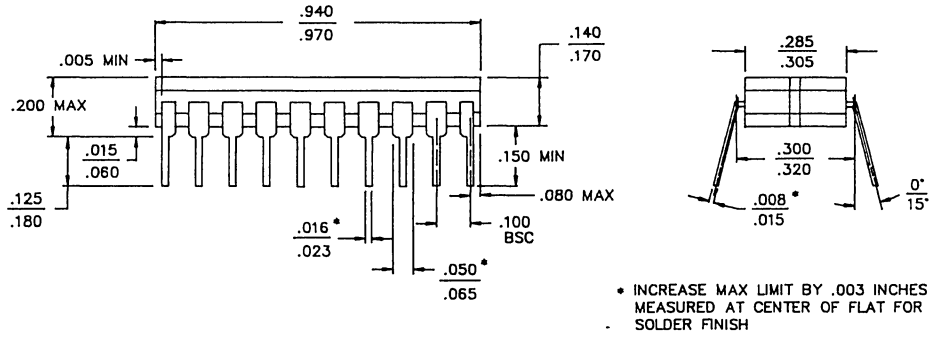
Metallization Mask Layout

HD-6409/883



Packaging†

20 PIN CERAMIC DIP

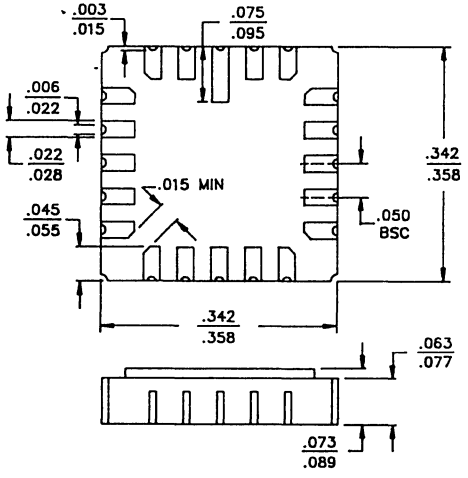


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: M38510 D-8

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: M38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

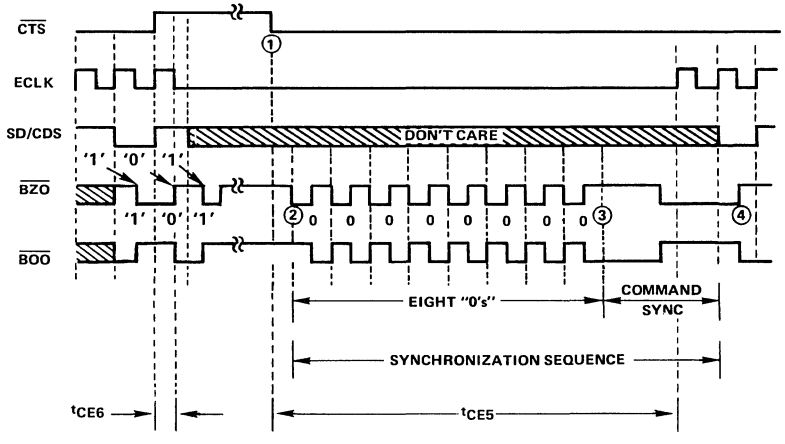
†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Encoder Operation

The encoder uses free running clocks at 1X and 2X the data rate derived from the system clock I_X for internal timing. $\overline{CTS}$ is used to control the encoder outputs, ECLK, $\overline{BOO}$ and $\overline{BZO}$. A free running 1X ECLK is transmitted out of the encoder to drive the external circuits which supply the NRZ data to the MED at pin SD/CDS.

A low on $\overline{CTS}$ enables encoder outputs ECLK, $\overline{BOO}$ and $\overline{BZO}$, while a high on $\overline{CTS}$ forces $\overline{BZO}$, $\overline{BOO}$ high and holds ECLK low. When $\overline{CTS}$ goes from high to low ① , a synchronization sequence is transmitted out on $\overline{BOO}$ and $\overline{BZO}$. A synchronization sequence consists of eight Manchester "0" bits followed by a command sync pulse. ② A command sync pulse is a three bit wide pulse with the first 1 1/2 bits high followed by 1 1/2 bits low. ③ Serial NRZ data is clocked into the encoder at SD/CDS on the high to low transition of ECLK during the command sync pulse. The NRZ data received is encoded into Manchester II data and transmitted out on $\overline{BOO}$ and $\overline{BZO}$ following the command sync pulse. ④ Following the synchronization sequence, input data is encoded and transmitted out continuously without parity check or word framing. The length of the data block encoded is defined by $\overline{CTS}$. Manchester data out is inverted.



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Decoder Operation

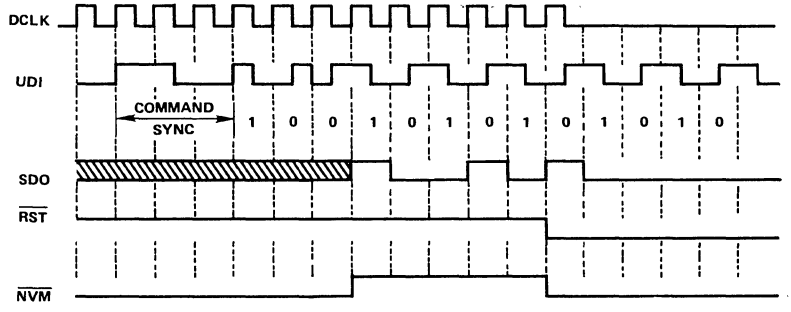
The decoder requires a single clock with a frequency 16X or 32X the desired data rate. The rate is selected on the speed select with SS low producing a 16X clock and high a 32X clock. For long data links the 32X mode should be used as the permits a wider timing jitter margin. The internal operation of the decoder utilizes a free running clock synchronized with incoming data for its clocking.

The Manchester II encoded data can be presented to the decoder in either of two ways. The Bipolar One and Bipolar Zero inputs will accept data from differential inputs such as a comparator sensed transformer coupled bus. The Unipolar Data input can only accept noninverted Manchester II encoded data i.e. Bipolar One Out through an inverter to Unipolar Data Input. The decoder continuously monitors this data input for valid sync pattern. Note that while the MED encoder section can generate only a command sync pattern, the decoder can recognize either a command or data sync pattern. A data sync is a logically inverted command sync.

There is a three bit delay between UDI, BOI, or BZI input and the decoded NRZ data transmitted out of SDO.

Control of the decoder outputs is provided by the $\overline{RST}$ pin. When $\overline{RST}$ is low, SDO, DCLK and $\overline{NVM}$ are forced low. When $\overline{RST}$ is high, SDO is transmitted out synchronously with the recovered clock DCLK. The $\overline{NVM}$ output remains low after a low to high transition on $\overline{RST}$ until a valid sync pattern is received.

The decoded data at SDO is in NRZ format. DCLK is privided so that the decoded bits can be shifted into an external register on every high to low transition of this clock. Three bit periods after an invalid Manchester bit is received on UDI, or BOI, $\overline{NVM}$ goes low synchronously with the questionable data output on SDO. FURTHER, THE DECODER DOES NOT REESTABLISH PROPER DATA DECODING UNTIL ANOTHER SYNC PATTERN IS RECOGNIZED.



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

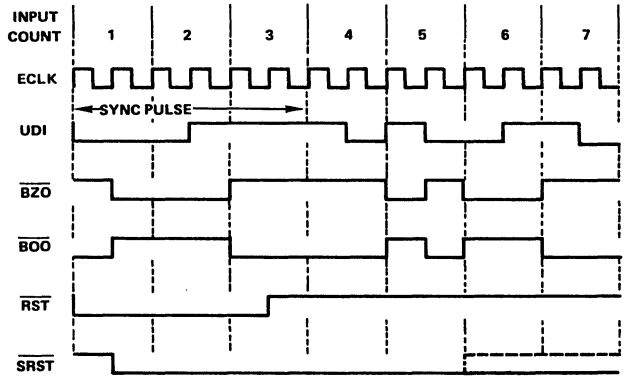
Repeater Operation

Manchester II data can be presented to the repeater in either of two ways. The inputs Bipolar One In and Bipolar Zero In will accept data from differential inputs such as a comparator or sensed transformer coupled bus. The input Unipolar Data In accepts only non-inverted Manchester II coded data. The decoder requires a single clock with a frequency 16X or 32X the desired data rate. This clock is selected to 16X with Speed Select low and 32X with Speed Select high. For long data links the 32X mode should be used as this permits a wider timing jitter margin.

The inputs UDI, or BOI, BZI are delayed approximately 1/2 bit period and repeated as outputs $\overline{BOO}$ and $\overline{BZO}$. The 2X ECLK is transmitted out of the repeater synchronously with $\overline{BOO}$ and $\overline{BZO}$.

A low on $\overline{CTS}$ enables ECLK, $\overline{BOO}$, and $\overline{BZO}$. In contrast to the converter mode, a transition on $\overline{CTS}$ does not initiate a synchronization sequence of eitght 0's and a command sync. The repeater mode does recogize a command or data sync pulse. SD/CDS is an output which reflects the state of the most recent sync pulse received, with high indicating a command sync and low indicating a data sync.

When $\overline{RST}$ is low, the outputs SDO, DCLK, and $\overline{NVM}$ are low, and $\overline{SRST}$ is set low. $\overline{SRST}$ remains low after $\overline{RST}$ goes high and is not reset until a sync pulse and two valid manchester bits are received with the reset bit low. The reset bit is the first data bit after the sync pulse. With RST high, NRZ Data is transmitted out of Serial Data Out synchronously with the 1X DCLK.



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Manchester Code

Nonreturn to Zero (NRZ) code represents the binary values logic-0 and logic-1 with a static level maintained throughout the data cell. In contrast, Manchester code represents data with a level transition in the middle of the data cell. Manchester has bandwidth, error detection, and synchronization advantages over NRZ code.

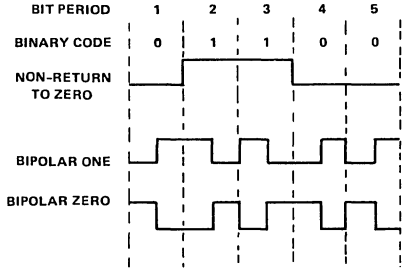
The manchester II code Bipolar One and Bipolar Zero shown below are logical complements. The direction of the transition indicates the binary value of data. A logic-0 in Bipolar One is defined as a Low to high transition in the middle of the data cell, and a logic-1 as a high to low mid bit transition, Manchester II is also known as Biphase-L code.

The bandwidth of NRZ is from DC to the clock frequency fc/2, while that of Manchester is from fc/2 to fc. Thus, Manchester can be AC or transformer coupled, which has considerable advantages over DC coupling. Also, the ratio of maximum to minimum frequency of Manchester extends one octaves, while the ratio for NRZ is the range of 5-10 octaves. It is much easier to design a narrow band than a wideband amp.

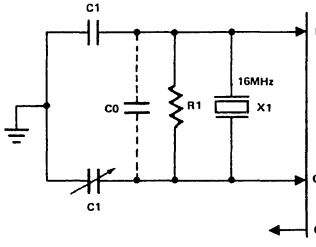
Secondly, the mid bit transition in each data cell provides the code with an effective error detection scheme. If noise produces a logic inversion in the data cell such that there is no transition, an error indiction is given, and synchronization must be re-established. This places relatively stringent requirements on the incomming data.

The synchronization advantages of using the HD-6409 and Manchester code are several fold. One is that Manchester is a self clocking code. The clock in serial data communication defines the position of each data cell. Non self clocking codes, as NRZ, often require an extra clock wire or clock track (in magnetic recording). Further, there can be a phase variation between the clock and data track. Crosstalk between the two may be a problem. In Manchester, the serial data stream contains both the clock and the data, with the position of the mid bit transition representing the clock, and the direction of the transition representing data. there is on phase variation between the clock and the data.

A second synchronization advantage is a result of the number of transitions in the data. The decoder resynchronizes on each transition, or at least once every data cell. In contrast, receivers using NRZ, which does not necessarily gave transitions, must resynchronize on frame bit transitions, which occur far less often, usually on a character basis. This more frequent resynchronization eliminates the cumulative effect of errors over sucessive data cells. A final synchronization advantage concerns the HD-6409's sync pulse used to initiate synchronization. This three bit wide pattern is sufficiently distinct from Manchester data that a false start by the receiver is unlikely.

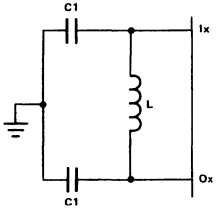


Crystal Oscillator Mode



C1 = 32pF
C0 = Crystal + Stray
X1 = AT CUT PARALLEL RESONANCE FUNDAMENTAL MODE
R_S (TYP) = 30Ω
R1 = 15MΩ

LC Oscillator Mode



C1 = 20pF
C0 = 5pF

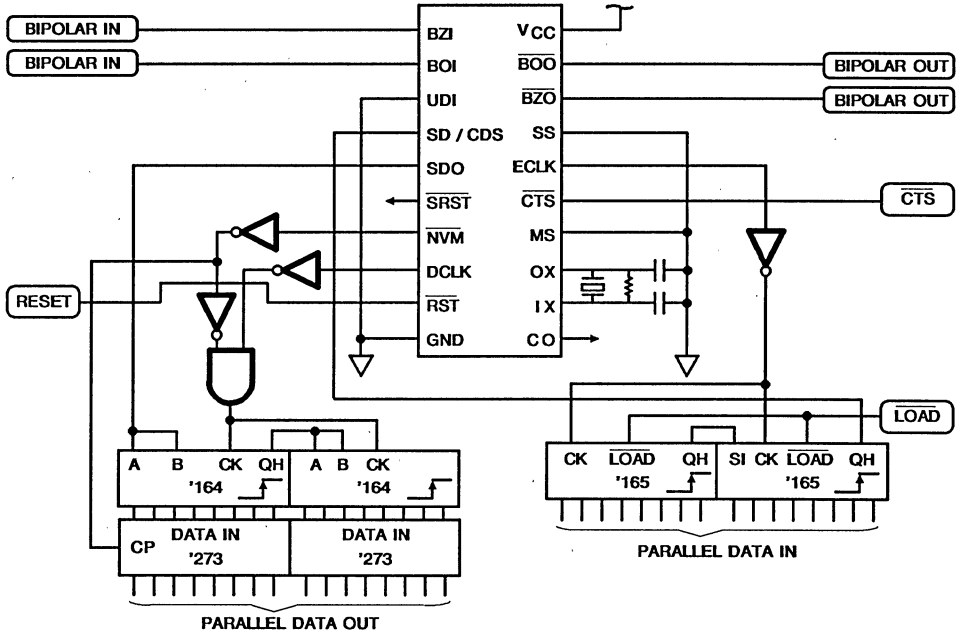
$C_e \approx \frac{C1 - 2C0}{2}$

$f_o \approx \frac{1}{2\pi\sqrt{LC_e}}$

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Using the 6409 as a Manchester Encoded UART



June 1989

CMOS Manchester Encoder-Decoder

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Support of MIL-STD-1553**
- **1.25 Megabit/Sec Data Rate**
- **Sync Identification and Lock-in**
- **Clock Recovery**
- **Manchester II Encode, Decode**
- **Separate Encode and Decode**
- **Low Operating Power .....50mW @ 5 Volts**

Description

The Harris HD-15530/883 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset functions.

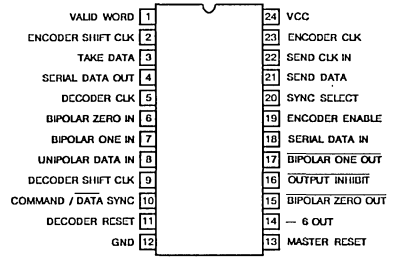
This circuit meets many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

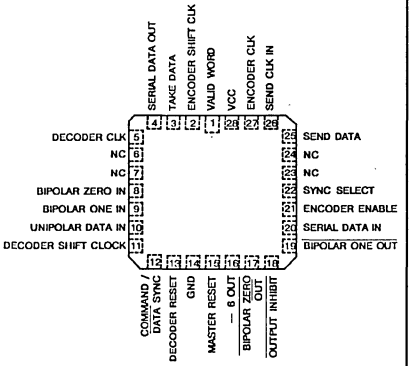
The HD-15530/883 can also be used in many party line digital data communications applications, such as an environmental control system driven from a single twisted pair cable of fiber optic cable throughout the building.

Pinouts

HD1-15530/883 (CERAMIC DIP)
TOP VIEW

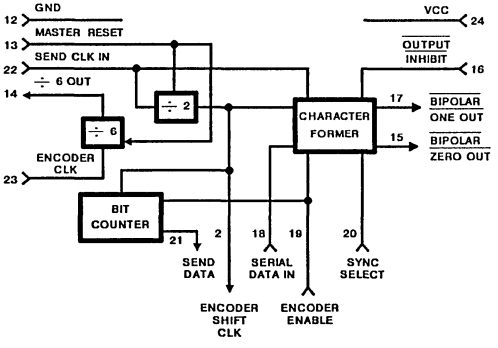


HD4-15530/883 (CERAMIC LCC)
TOP VIEW

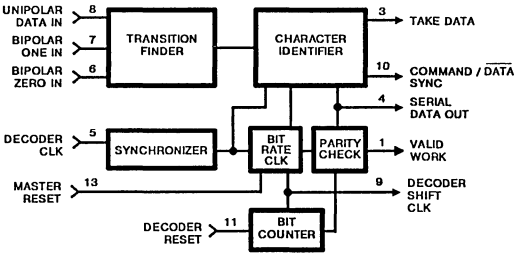


Block Diagrams

ENCODER



DECODER



Pin Description

PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
1	O	VALID WORD	Decoder	Output high indicates receipt of a valid word, (valid parity and no Manchester errors).
2	O	ENCODER SHIFT CLOCK	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI on the low-to-high transition of Encoder Shift Clock.
3	O	TAKE DATA	Decoder	Output is high during receipt of data after identification of a sync pulse and two valid Manchester data bits.
4	O	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
5	I	DECODER CLOCK	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder, input a frequency equal to 12X the data rate.
6	I	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	I	BIPOLAR ONE IN	Decoder	A high input should be applied when the bus is in its positive state. This pin must be held low when the Unipolar input is used.
8	I	UNIPOLAR DATA IN	Decoder	With pin 6 high and pin 7 low, this pin enters unipolar data into the transtition finder circuit. If not used this input must be held low.
9	O	DECODER SHIFT CLOCK	Decoder	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
10	O	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
11	I	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	I	GROUND	Both	Ground Supply pin.
13	I	MASTER RESET	Both	A high on this pin clears 2:1 counters in both Encoder and Decoder, and resets the ÷ 6 circuit.
14	O	÷ 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK.
15	O	$\overline{\text{BIPOLAR ZERO OUT}}$	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
16	I	$\overline{\text{OUTPUT INHIBIT}}$	Encoder	A low on this pin forces pin 15 and 17 high, the inactive states.
17	O	$\overline{\text{BIPOLAR ONE OUT}}$	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.
18	I	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	I	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete.)
20	I	SYNC SELECT	Encoder	Actuates a Command sync for an input high and Data sync for an input low.
21	O	SEND DATA	Encoder	An active high output which enables the external source of serial data.
22	I	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.
23	I	ENCODER CLOCK	Encoder	Input to the 6:1 divider, a frequency equal to the data rate X12 is usually input here.
24	I	VCC	Both	VCC is the +5V power supply pin. A 0.1 µF decoupling capacitor from VCC (pin 24) to GROUND (pin 12) is recommended.

I = Input O = Output

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied..... GND-0.3V to VCC+0.3
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec)..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	50.4°C/W	11.7°C/W
Ceramic LCC Package	71.1°C/W	16.8°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 992mW
Ceramic LCC Package 703mW
Gate Count ..... 456 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Ambient Operating Temperature Range (T_A) ... -55°C to +125°C
Encoder/Decoder Clock Rise Time ..... 8ns Max
Encoder/Decoder Clock Fall Time ..... 8ns Max
Sync Transition Span (TD2) ..... 18 TDC Typical (Note1)
Short Data Transition Span (TD4) ..... 6 TDC Typical (Note1)
Long Data Transition Span (TD5)..... 12 TDC Typical (Note1)

TABLE 1. HD-15530/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input LOW Voltage	VIL	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.2 VCC	V
Input HIGH Voltage	VIH	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	0.7 VCC	-	V
Input LOW Clock Voltage	VILC	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	GND+0.5	V
Input HIGH Clock Voltage	VIHC	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC-0.5	-	V
Output LOW Voltage	VOL	IOL = 1.8mA (Note 2) VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output HIGH Voltage	VOH	IOH = -3mA (Note 2) VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VI = GND or VCC VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Standby Supply Current	ICCSB	VIN = VCC = 5.5V Output Open	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	2	mA
Function Test	FT	(Note 3)	7, 8	$-55°C \leq T_A \leq +125°C$	-	-	-

NOTES: 1. TDC = Decoder clock period = 1/FDC

2. Interchanging of force and sense conditions is permitted.

3. Tested as follows: f = 15MHz, VIH = 70% VCC, VIL = 20% VCC, CL = 50pF, VOH $\geq$ 1.5V and VOL $\leq$ 1.5V.

TABLE 2. HD-15530/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
ENCODER TIMING							
Encoder Clock Frequency	FEC	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	15	MHz
Send Clock Frequency	FESC	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	2.5	MHz
Encoder Data Rate	FED	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	1.25	MHz
Master Reset Pulse Width	TMR	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Shift Clock Delay	TE1	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	125	ns
Serial Data Setup	TE2	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns
Serial Data Hold	TE3	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns
Enable Setup	TE4	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	90	-	ns
Enable Pulse Width	TE5	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Sync Setup	TE6	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	55	-	ns
Sync Pulse Width	TE7	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Send Data Delay	TE8	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	50	ns
Bipolar Output Delay	TE9	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	130	ns
Enable Hold	TE10	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Sync Hold	TE11	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	95	-	ns
DECODER TIMING							
Decoder Clock Frequency	FDC	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	15	MHz
Decoder Data Rate	FDD	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	1.25	MHz
Decoder Reset Pulse Width	TDR	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Decoder Reset Setup Time	TDRS	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns
Decoder Reset Hold Time	TDRH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns
Master Reset Pulse	TMR	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Bipolar Data Pulse Width	TD1	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TDC+10 (Note 1)	-	ns
One Zero Overlap	TD3	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	TDC-10 (Note 1)	ns
Sync Delay (ON)	TD6	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-20	110	ns
Take Data Delay (ON)	TD7	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Serial Data Out Delay	TD8	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	80	ns
Sync Delay (OFF)	TD9	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Take Data Delay (OFF)	TD10	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Valid Word Delay	TD11	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns

NOTES: 1. TDC = Decoder clock period = 1/FDC

2. A.C. Testing as follows: Input levels: VIH = 70% VCC, VIL = 20% VCC; Input rise/fall times driven at 1ns/V; Timing reference levels: 1.5V; Output load: CL = 50pF

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. HD-15530/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CI	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	-	15	pF
Input/Output Capacitance	CIO	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	-	15	pF
Operating Power Supply Current	ICCOP	VCC = 5.5V, f = 1MHz	1, 2	$-55^oC \leq T_A \leq +25^oC$	-	10	mA

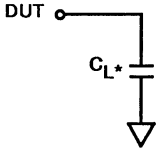
NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

2. Guaranteed but not 100% tested.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Test Load Circuit

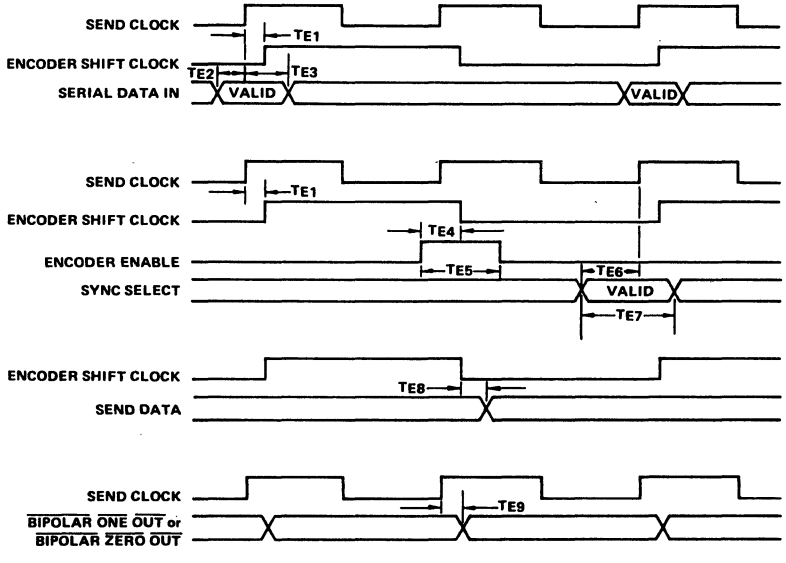


*Includes Stray and Jig Capacitance

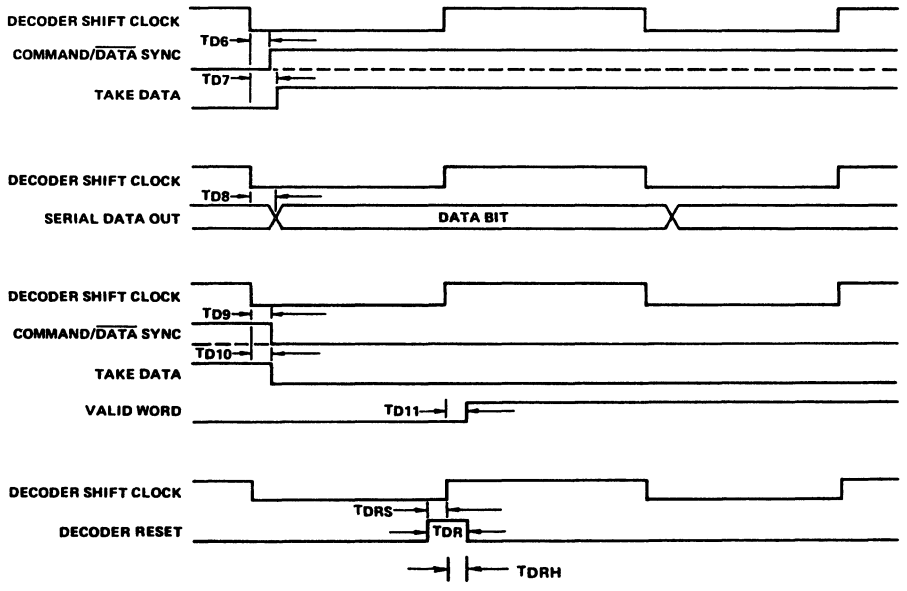
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Timing Waveforms

ENCODER TIMING

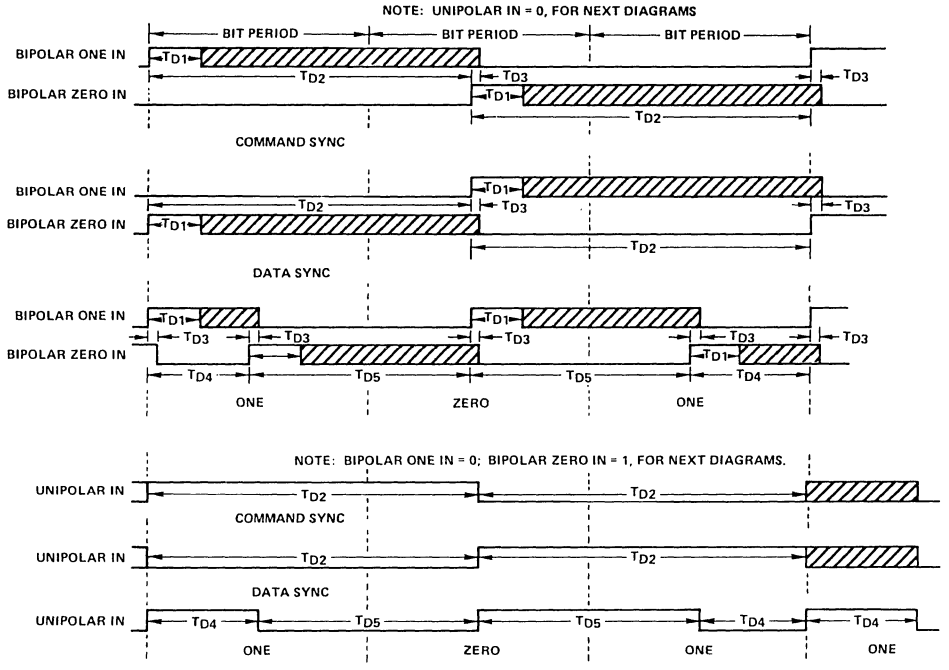


DECODER TIMING



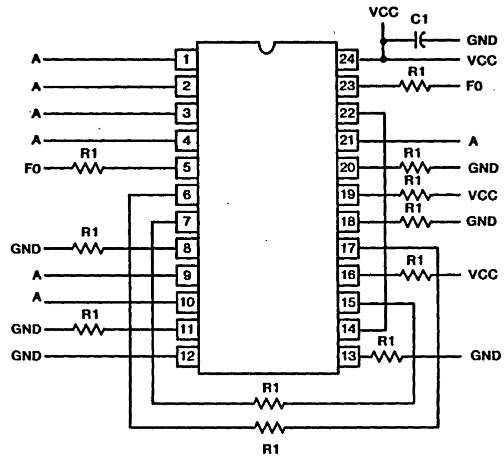
Timing Waveforms (Continued)

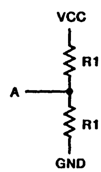
DECODER TIMING (Continued)



Burn-In Circuits

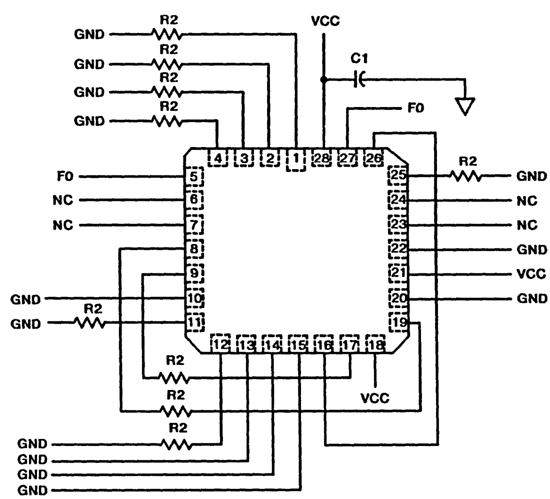
HD1-15530/883 CERAMIC DIP





NOTES:
VCC = 5.5V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to +0.4V
R1 = 47KΩ ± 5%
F0 = 100KHz ± 10%
C1 = 0.01μF Min.

HD4-15530/883 CERAMIC LCC



NOTES:
VCC = 5.5V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to +0.4V
R2 = 1.8KΩ ± 5%
F0 = 100KHz ± 10%
C1 = 0.0μF Min.

Metallization Topology

DIE DIMENSIONS:
155 x 195 x 19 ± 1 mils

METALLIZATION:
Type: Si-Al
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

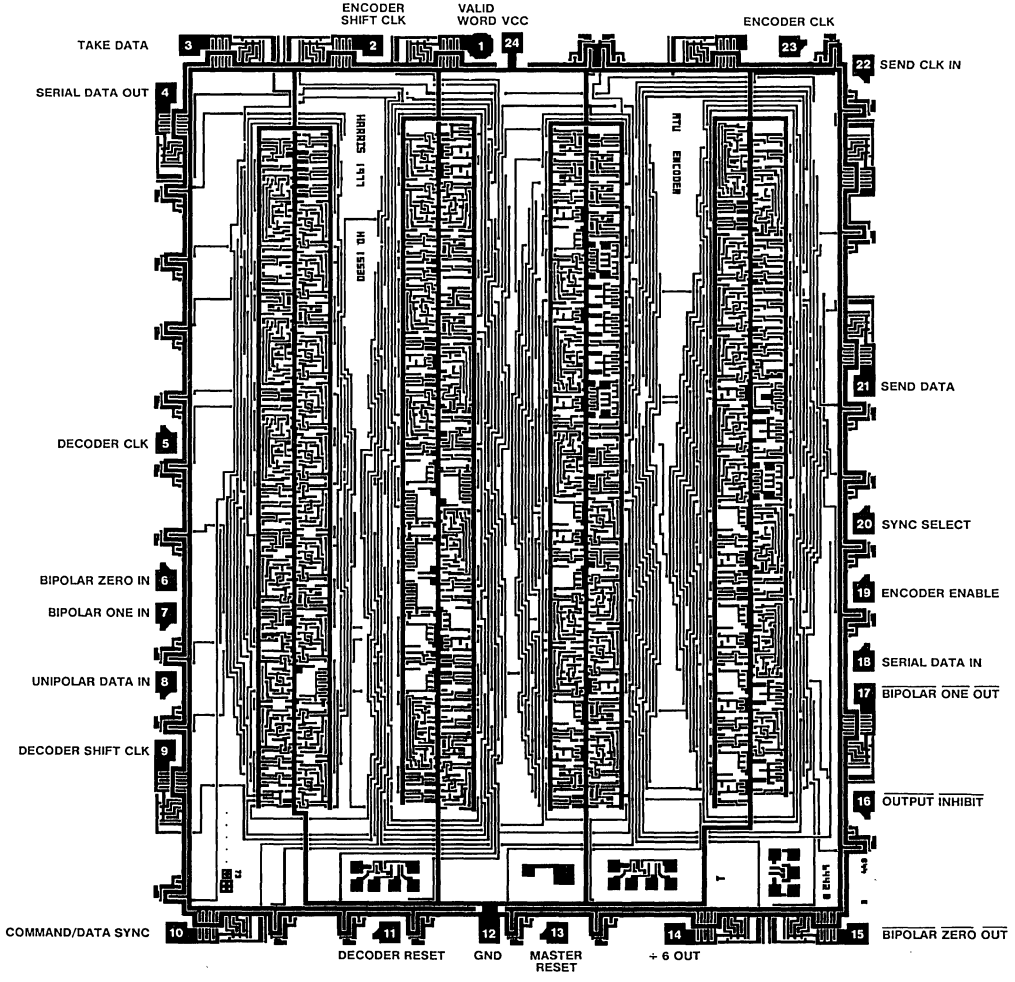
DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.8 x 10^5A/cm^2

LEAD TEMPERATURE (10 seconds soldering):
≤275°C

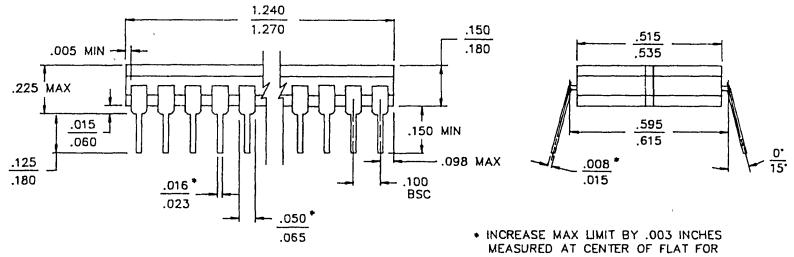
Metallization Mask Layout

HD-15530/883



Packaging†

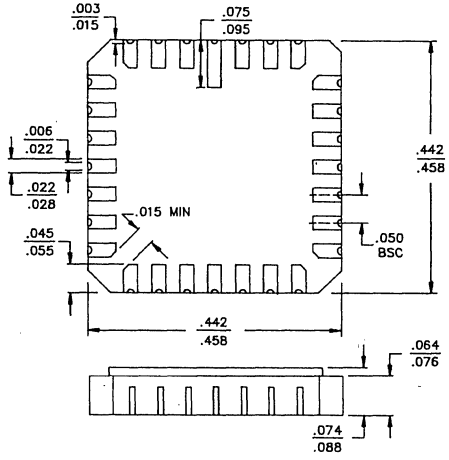
24 PIN (.600) CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

28 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-4

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

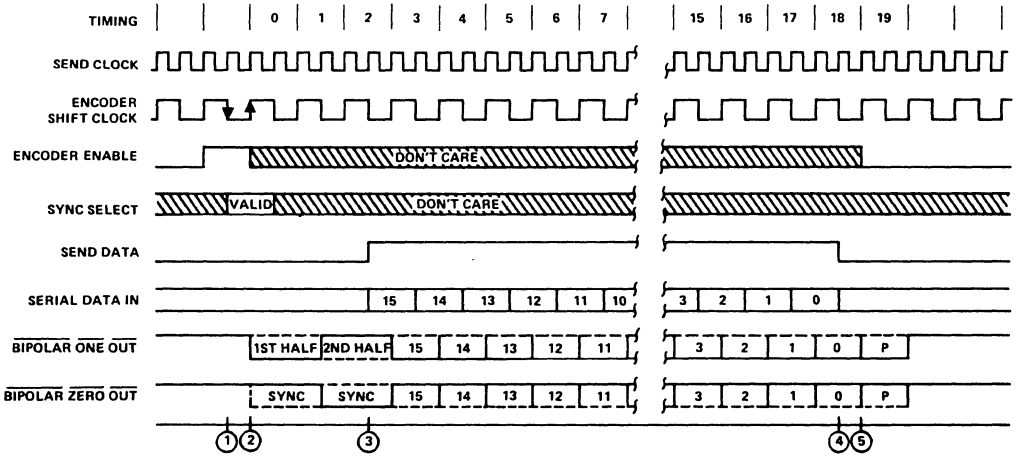
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a command sync or a low will produce a data sync for the word ②. When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods ③. During these sixteen periods the data should be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK so it can be sampled on the low-to-high transition ③ - ④. After the sync and Manchester II coded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit which is the parity for that word ⑤. If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time ⑤ as shown to prevent a consecutive word from being encoded. At any time a low on $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

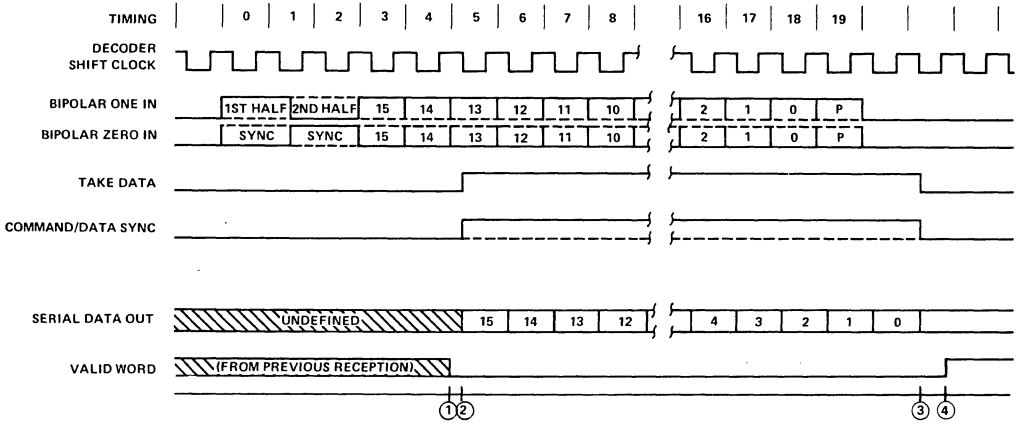
Decoder Operation

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from $\overline{\text{BIPOLAR ONE}}$ $\overline{\text{OUT}}$ of an Encoder through an inverter to Unipolar Data Input).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high ② and remain high for sixten DECODER SHIFT CLOCK periods ③, otherwise it will remain low. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock ② - ③. Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown ①.

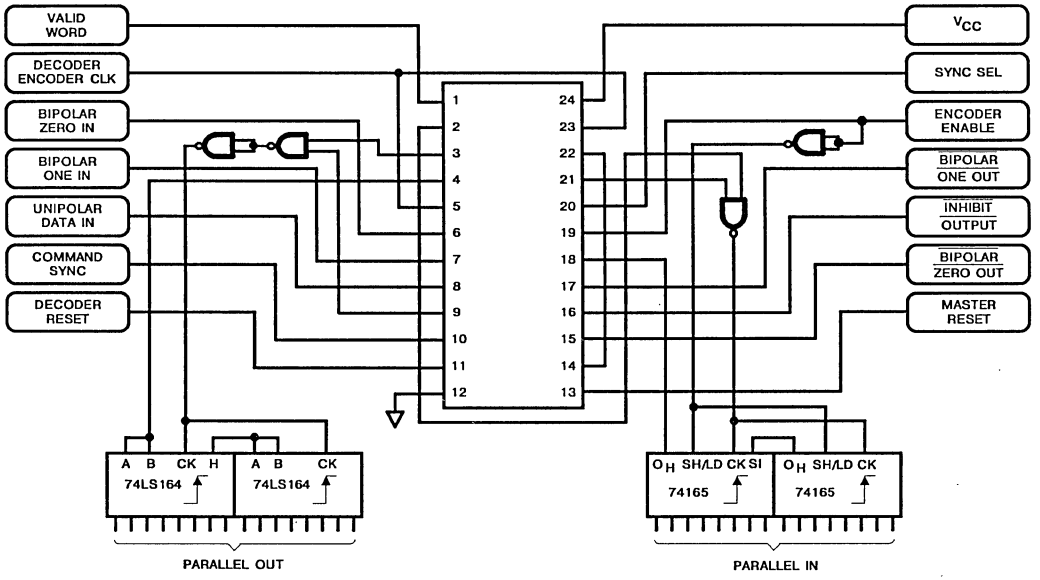
At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.



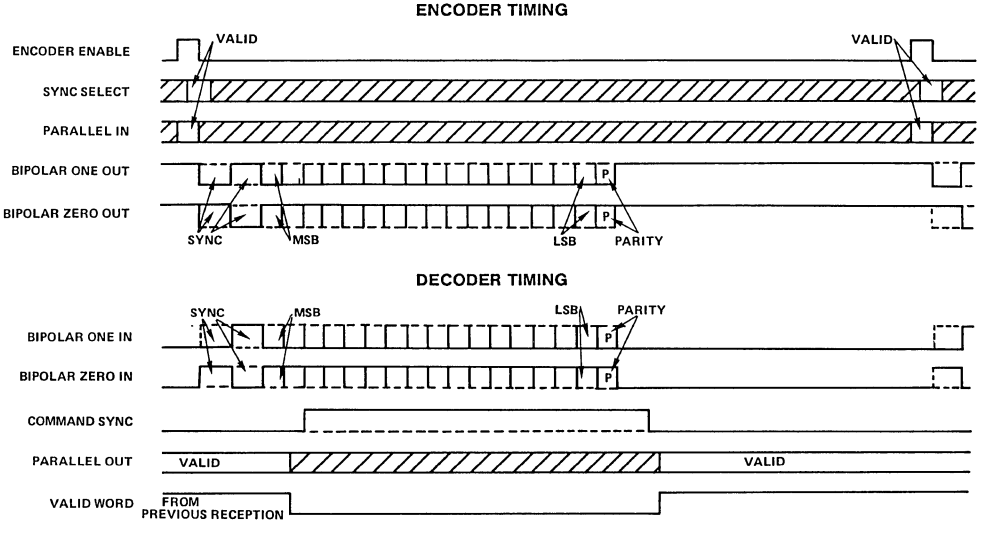
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

How to Make Our MTU Look Like a Manchester Encoded UART



Typical Timing Diagrams for a Manchester Encoded UART



HARRIS HD-15531/883

June 1989

CMOS Manchester Encoder-Decoder

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Support of MIL-STD-1553
- 2.5 Megabit/Sec Data Rate (15531B)
- 1.25 Megabit/Sec Data Rate (15531)
- Variable Frame Length to 32-Bits
- Sync Identification and Lock-In
- Separate Manchester II Encode, Decode
- Low Operating Power ..... 50mW @ 5 Volts

Description

The Harris HD-15531/883 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate independently of each other, except for the master reset and word length functions. This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

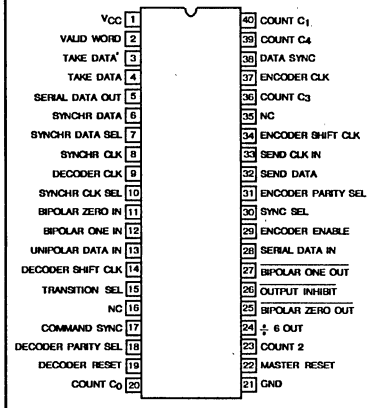
The HD-15531/883 also surpasses the requirements of MIL-STD-1553 by allowing the word length to be programmable (from 2 to 28 data bits). A frame consists of three bits for sync followed by the data word (2 to 28 data bits) followed by one bit of parity, thus the frame length will vary from 6 to 32 bit periods. This chip also allows selection of either even or odd parity for the Encoder and Decoder separately.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. For high speed applications the 15531B will support a 2.5 Megabit/sec data rate.

The HD-15531/883 can also be used in many party line digital data communications applications, such as a local area network or an environmental control system driven from a single twisted pair of fiber optic cable throughout a building.

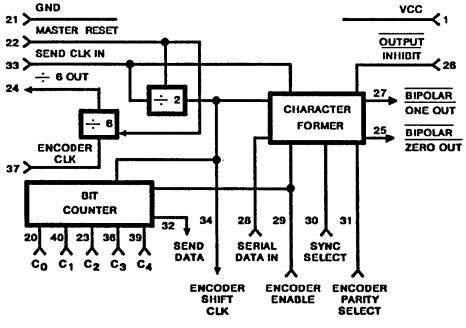
Pinout

HD1-15531/883 (CERAMIC DIP)
TOP VIEW

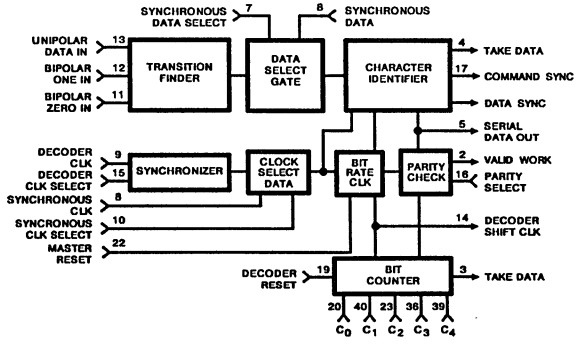


Block Diagrams

ENCODER



DECODER



Pin Description HD-15531/883

PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
1		VCC	Both	Positive supply pin. A 0.1 µF decoupling capacitor from VCC (pin 1) to GROUND (pin 21) is recommended.
2	O	VALID WORD	Decoder	Output high indicates receipt of a valid word, (valid parity and no Manchester errors).
3	O	TAKE DATA'	Decoder	A continuous, free running signal provided for host timing or data handling. When data is present on the bus, this signal will be synchronized to the incoming data and will be identical to take data.
4	O	TAKE DATA	Decoder	Output is high during receipt of data after identification of a valid sync pulse and two valid Manchester bits.
5	O	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
6	I	SYNCHRONOUS DATA	Decoder	Input presents Manchester data directly to character identification logic. SYNCHRONOUS DATA SELECT must be held high to use this input. If not used this pin must be held high.
7	I	SYNCHRONOUS DATA SELECT	Decoder	In high state allows the synchronous data to enter the character identification logic. Tie this input low for asynchronous data.
8	I	SYNCHRONOUS CLOCK	Decoder	Input provides externally synchronized clock to the decoder, for use when receiving synchronous data. This input must be tied high when not in use.
9	I	DECODER CLOCK	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder. Input a frequency equal to 12X the data rate.
10	I	SYNCHRONOUS CLOCK SELCT	Decoder	In high state directs the SYNCHRONOUS CLOCK to control the decoder character identification logic. A low state selects the DECODER CLOCK.
11	I	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the unipolar input is used.
12	I	BIPOLAR ONE IN	Decoder	A high input should be applied when the bus is in its positive state. This pin must be held low when the unipolar input is used.
13	I	UNIPOLAR DATA IN	Decoder	With pin 11 high and pin 12 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
14	O	DECODER SHIFT CLOCK	Decoder	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronous by the recovered serial data stream.
15	I	TRANSITION SELECT	Decoder	A high input to this pin causes the transition finder to synchronize on every transition of input data. A low input causes the transition finder to synchronize only on mid-bit transitions.
16		N.C.	Blank	Not connected.
17	O	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character.
18	I	DECODER PARITY SELECT	Decoder	An input for parity sense, calling for even parity with input high and odd parity with input low.
19	I	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
20	I	COUNT C0	Both	One of five binary inputs which establish the total bit count to be encoded or decoded.
21		GROUND	Both	Supply pin.
22	I	MASTER RESET	Both	A high on this pin clears 2:1 counters in both encoder and decoder, and resets the ÷ 6 circuit.
23	I	COUNT C2	Both	See pin 20.
24	O	÷ 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK.
25	O	$\overline{\text{BIPOLAR ZERO OUT}}$	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
26	I	$\overline{\text{OUTPUT INHIBIT}}$	Encoder	A low on this pin forces pin 25 and 27 high, the inactive states.
27	O	$\overline{\text{BIPOLAR ONE OUT}}$	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.
28	I	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
29	I	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceding cycle being complete.)
30	I	SYNC SELECT	Encoder	Actuates a Command sync for an input high and Data sync for an input low.
31	I	ENCODER PARITY SELECT	Encoder	Sets transmit parity odd for a high input, even for a low input.
32	O	SEND DATA	Encoder	Is an active high output which enables the external source of serial data.
33	I	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.
34	O	ENCODER SHIFT CLOCK	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI pin-28 on the low-to-high transition of ESC.
35		N.C.	Blank	Not connected.
36	I	COUNT C3	Both	See pin 20.
37	I	ENCODER CLOCK	Encoder	Input to the 6:1 divider, a frequency equal to 12 times the data rate is usually input here.
38	O	DATA SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a data synchronizing character.
39	I	COUNT C4	Both	See pin 20.
40	I	COUNT C1	Both	See pin 20.

I = Input O = Output

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	34.8°C/W	7.9°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.44W
Gate Count ..... 250 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Ambient Operating Temperature Range (T_A) ... -55°C to +125°C
Encoder/Decoder Clock Rise Time (TECR, TDCR) ..... 8ns Max
Encoder/Decoder Clock Fall Time (TECF, TDCF) ..... 8ns Max

Sync Transition Span (TD2) ..... 18 TDC Typical (Note1)
Short Data Transition Span (TD4) ..... 6 TDC Typical (Note1)
Long Data Transition Span (TD5) ..... 12 TDC Typical (Note1)

TABLE 1. HD-15531/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input LOW Voltage	VIL	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.2 VCC	V
Input HIGH Voltage	VIH	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	0.7 VCC	-	V
Input LOW Clock Voltage	VILC	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	GND+0.5	V
Input HIGH Clock Voltage	VIHC	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	VCC-0.5	-	V
Output LOW Voltage	VOL	IOL = 1.8mA (Note 2) VCC = 4.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Output HIGH Voltage	VOH	IOH = -3mA (Note 2) VCC = 4.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
Input Leakage Current	II	VI = GND or VCC VCC = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Standby Supply Current	ICCSB	VIN = VCC = 5.5V Output Open	1, 2, 3	$-55°C \le T_A \le +125°C$	-	2	mA
Function Test	FT	(Note 3)	7, 8	$-55°C \le T_A \le +125°C$	-	-	-

NOTES: 1. TDC = Decoder clock period = 1/FDC

2. Interchanging of force and sense conditions is permitted.

3. Tested as follows: f = 15MHz, VIH = 70% VCC, VIL = 20% VCC, CL = 50pF, VOH $\ge$ VCC/2 and VOL $\le$ VCC/2.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. HD-15531/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
ENCODER TIMING							
Encoder Clock Frequency	FEC	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	15	MHz
Send Clock Frequency	FESC	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	2.5	MHz
Encoder Data Rate	FED	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	1.25	MHz
Master Reset Pulse Width	TMR	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Shift Clock Delay	TE1	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	125	ns
Serial Data Setup	TE2	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns
Serial Data Hold	TE3	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns
Enable Setup	TE4	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	90	-	ns
Enable Pulse Width	TE5	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Sync Setup	TE6	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	55	-	ns
Sync Pulse Width	TE7	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Send Data Delay	TE8	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	50	ns
Bipolar Output Delay	TE9	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	130	ns
Enable Hold	TE10	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Sync Hold	TE11	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	95	-	ns
DECODER TIMING							
Decoder Clock Frequency	FDC	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	15	MHz
Decoder Sync Clock	FDS	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	2.5	MHz
Decoder Data Rate	FDD	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	1.25	MHz
Decoder Reset Pulse Width	TDR	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Decoder Reset Setup Time	TDRS	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns
Decoder Reset Hold Time	TDRH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns
Master Reset Pulse	TMR	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Bipolar Data Pulse Width	TD1	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TDC+10 (Note 1)	-	ns
One Zero Overlap	TD3	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	TDC-10 (Note 1)	ns
Sync Delay (ON)	TD6	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-20	110	ns
Take Data Delay (ON)	TD7	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Serial Data Out Delay	TD8	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	80	ns
Sync Delay (OFF)	TD9	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Take Data Delay (OFF)	TD10	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Valid Word Delay	TD11	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Sync Clock to Shift Clock Delay	TD12	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	75	ns
Sync Data Setup	TD13	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns

NOTES: 1. TDC = Decoder clock period = 1/FDC

2. A.C. Testing as follows: Input levels: VIH = 70% VCC, VIL = 20% VCC; Input rise/fall times driven at 1ns/V; Timing reference levels: VCC/2; Output load: CL = 50pF

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. HD-15531/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CI	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	-	25	pF
Input/Output Capacitance	CIO	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	-	25	pF
Operating Power Supply Current	ICCOP	VCC = 5.5V, f = 1MHz	1, 2	$-55^oC \leq T_A \leq +25^oC$	-	10	mA

NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

2. Guaranteed but not 100% tested.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	34.8°C/W	7.9°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.44W
Gate Count ..... 250 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Ambient Operating Temperature Range (T_A) ... -55°C to +125°C
Encoder/Decoder Clock Rise Time (TECR, TDCR) ..... 8ns Max
Encoder/Decoder Clock Fall Time (TECF, TDCF) ..... 8ns Max

Sync Transition Span (TD2) ..... 18 TDC Typical (Note1)
Short Data Transition Span (TD4) ..... 6 TDC Typical (Note1)
Long Data Transition Span (TD5) ..... 12 TDC Typical (Note1)

TABLE 1. HD-15531B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input LOW Voltage	VIL	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.2 VCC	V
Input HIGH Voltage	VIH	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	0.7 VCC	-	V
Input LOW Clock Voltage	VILC	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	GND+0.5	V
Input HIGH Clock Voltage	VIHC	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC-0.5	-	V
Output LOW Voltage	VOL	IOL = 1.8mA (Note 2) VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Output HIGH Voltage	VOH	IOH = -3mA (Note 2) VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.4	-	V
Input Leakage Current	II	VI = GND or VCC VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Standby Supply Current	ICCSB	VIN = VCC = 5.5V Output Open	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	2	mA
Function Test	FT	(Note 3)	7, 8	$-55°C \leq T_A \leq +125°C$	-	-	

NOTES: 1. TDC = Decoder clock period = 1/FDC

2. Interchanging of force and sense conditions is permitted.

3. Tested as follows: f = 15MHz, VIH = 70% VCC, VIL = 20% VCC, CL = 50pF, VOH $\geq$ VCC/2 and VOL $\leq$ VCC/2.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. HD-15531B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
ENCODER TIMING							
Encoder Clock Frequency	FEC	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	30	MHz
Send Clock Frequency	FESC	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	5.0	MHz
Encoder Data Rate	FED	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	2.5	MHz
Master Reset Pulse Width	TMR	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Shift Clock Delay	TE1	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	80	ns
Serial Data Setup	TE2	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Serial Data Hold	TE3	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Enable Setup	TE4	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	90	-	ns
Enable Pulse Width	TE5	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Sync Setup	TE6	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	55	-	ns
Sync Pulse Width	TE7	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Send Data Delay	TE8	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	50	ns
Bipolar Output Delay	TE9	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	130	ns
Enable Hold	TE10	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Sync Hold	TE11	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	95	-	ns
DECODER TIMING							
Decoder Clock Frequency	FDC	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	30	MHz
Decoder Sync Clock	FDS	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	5.0	MHz
Decoder Data Rate	FDD	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	2.5	MHz
Decoder Reset Pulse Width	TDR	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Decoder Reset Setup Time	TDRS	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns
Decoder Reset Hold Time	TDRH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns
Master Reset Pulse	TMR	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Bipolar Data Pulse Width	TD1	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TDC+10 (Note 1)	-	ns
One Zero Overlap	TD3	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	TDC-10 (Note 1)	ns
Sync Delay (ON)	TD6	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-20	110	ns
Take Data Delay (ON)	TD7	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Serial Data Out Delay	TD8	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	80	ns
Sync Delay (OFF)	TD9	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Take Data Delay (OFF)	TD10	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Valid Word Delay	TD11	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Sync Clock to Shift Clock Delay	TD12	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	75	ns
Sync Data Setup	TD13	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns

NOTES: 1. TDC = Decoder Clock Period = 1/FDC

2. A.C. Testing as follows: Input levels: VIH = 70% VCC, VIL = 20% VCC; Input rise/fall times driven at 1ns/V; Timing reference levels: VCC/2; Output load: CL = 50pF

CAUTION: These devices are sensitive to electrostatic fdischarge. Proper IC handling procedures should be followed.

TABLE 3. HD-15531B/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	-	25	pF
Input/Output Capacitance	CIO	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	-	25	pF
Operating Power Supply Current	ICCOP	VCC = 5.5V, f = 1MHz	1, 2	$-55^oC \leq T_A \leq +25^oC$	-	10	mA

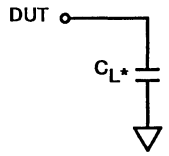
NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

2. Guarenteed but not 100% tested.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Test Load Circuit

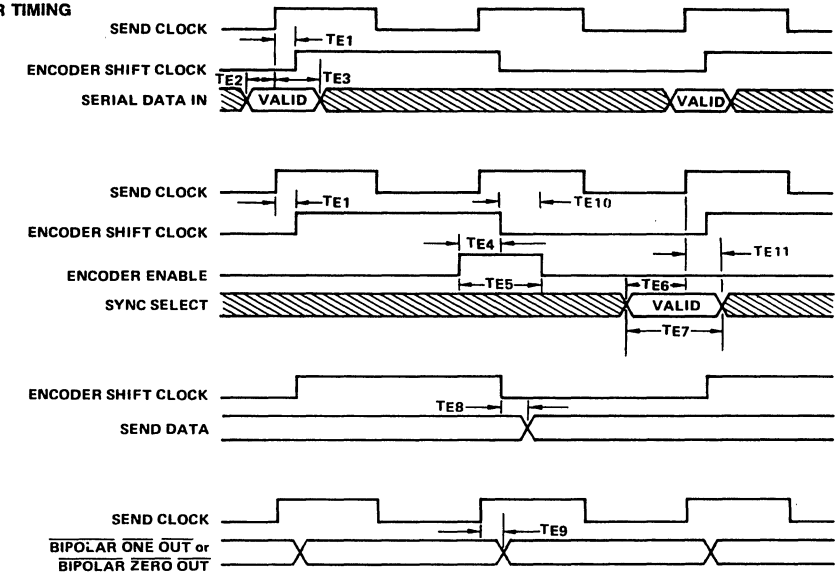


*Includes Stray and Jig Capacitance

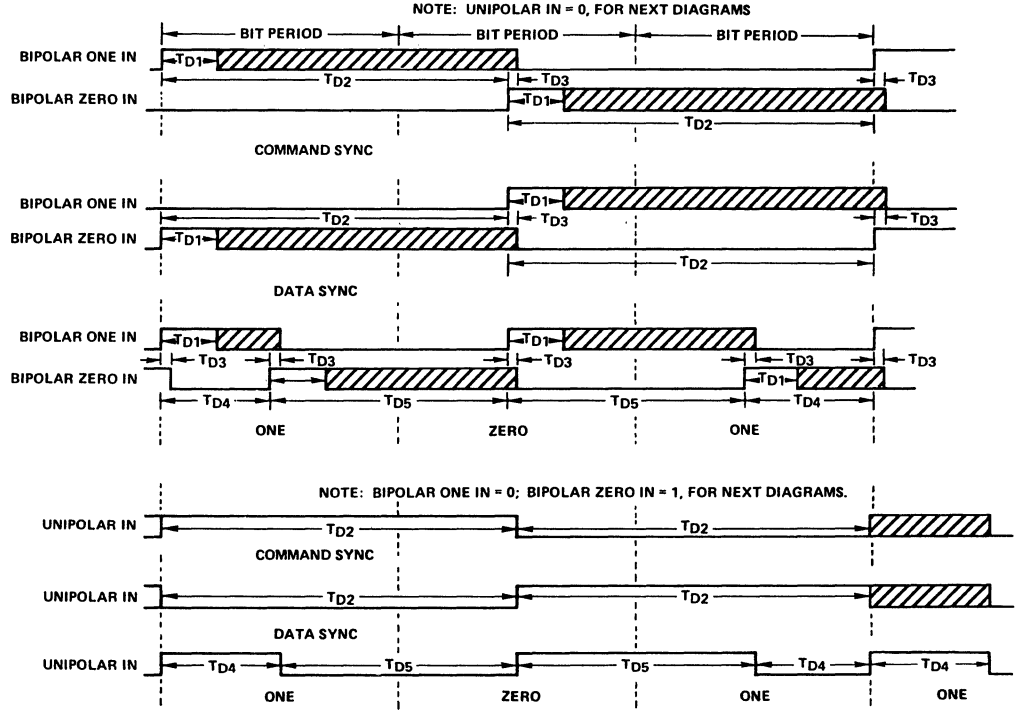
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Timing Waveforms

ENCODER TIMING

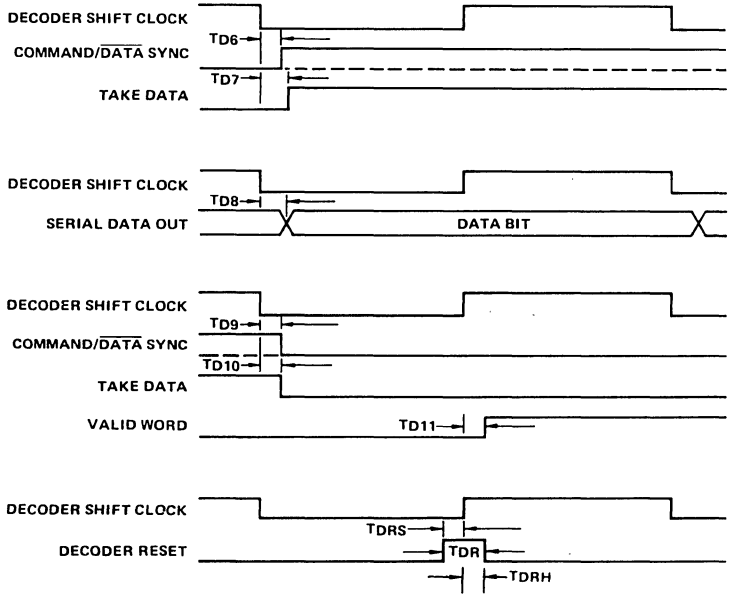


DECODER TIMING

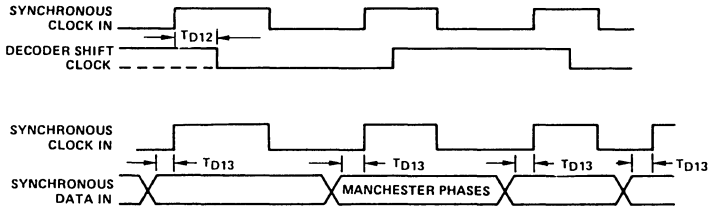


Timing Waveforms (Continued)

DECODER TIMING (Continued)

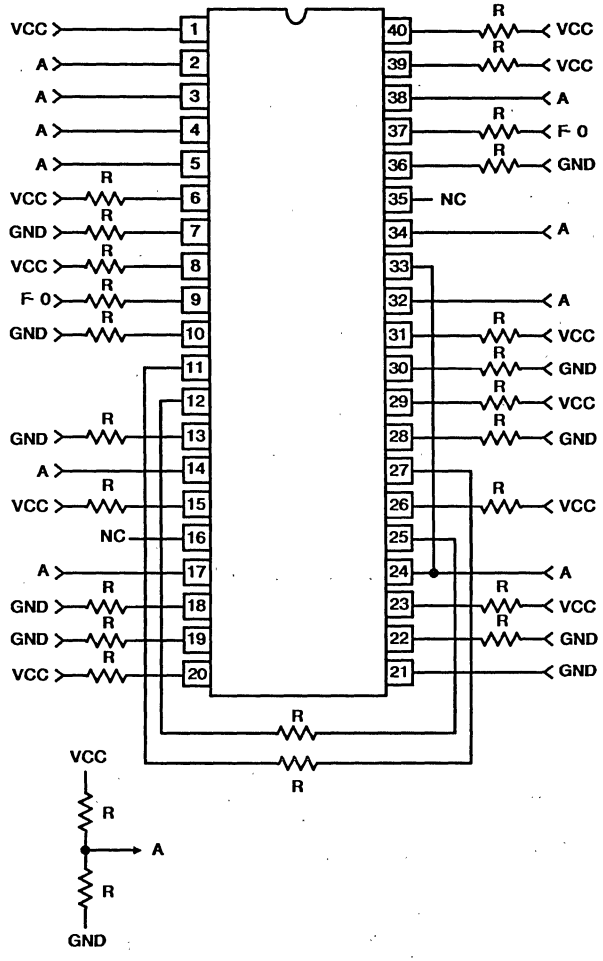


SYNCHRONOUS INPUT (WITH EXTERNAL BIT SYNCHRONIZATION)



Burn-In Circuit

HD1-15531/883 CERAMIC DIP



NOTES:
VCC = 5.5V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to +0.4V
R = 47kΩ ± 5%
F0 = 100kHz ± 10%

Metallization Topology

DIE DIMENSIONS:
155 x 195 x 19 ± 1 mils

METALLIZATION:
Type: Si-Al
Thickness: 11kÅ ± 2kÅ

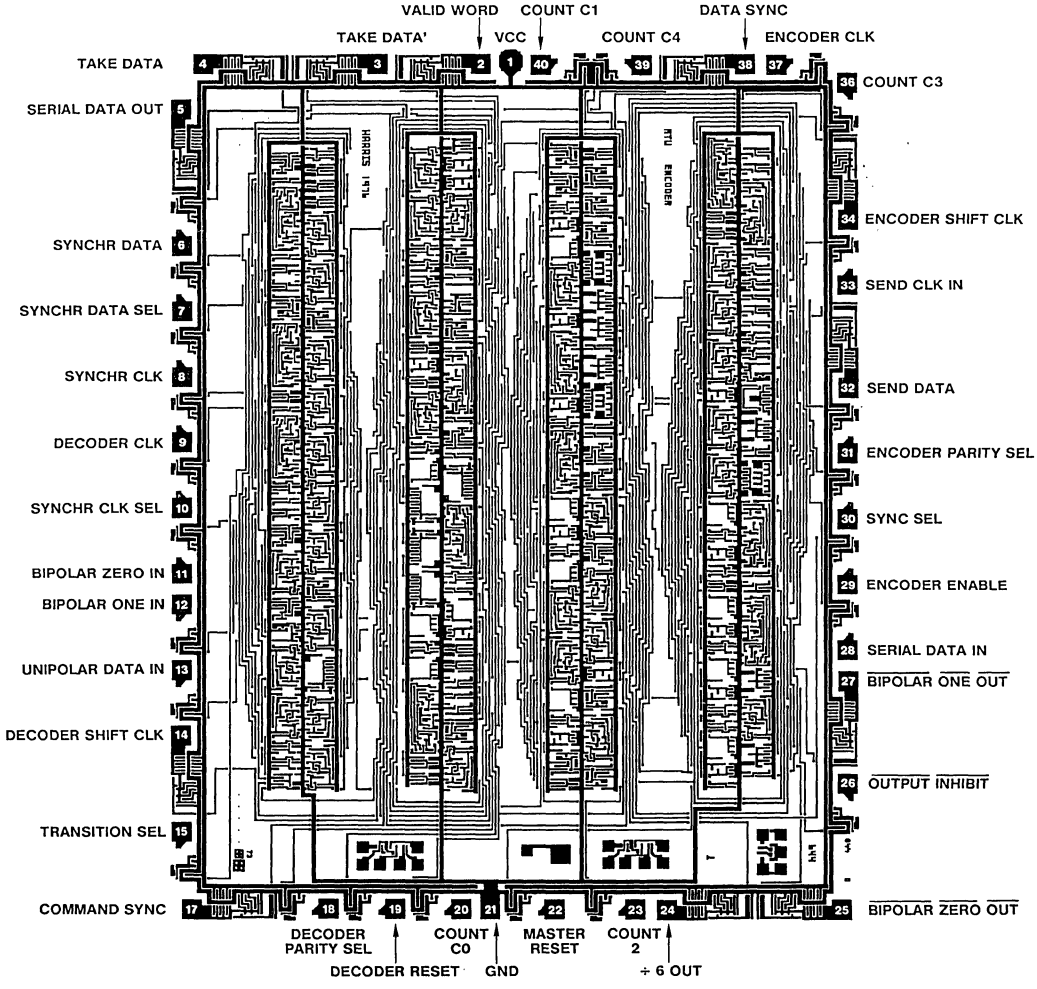
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$2.0 \times 10^5 A/cm^2$

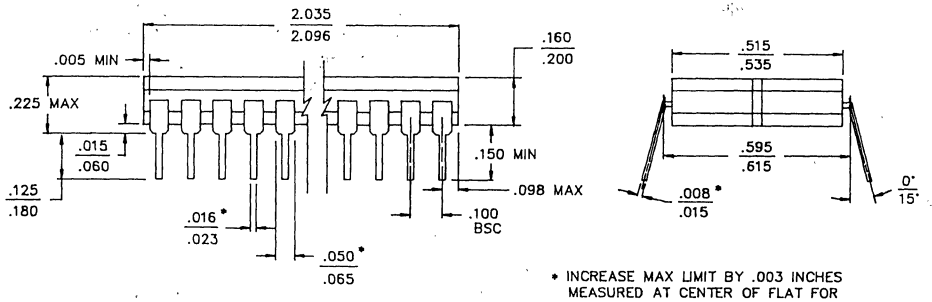
Metallization Mask Layout

HD-15531/883



Packaging†

40 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-5

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

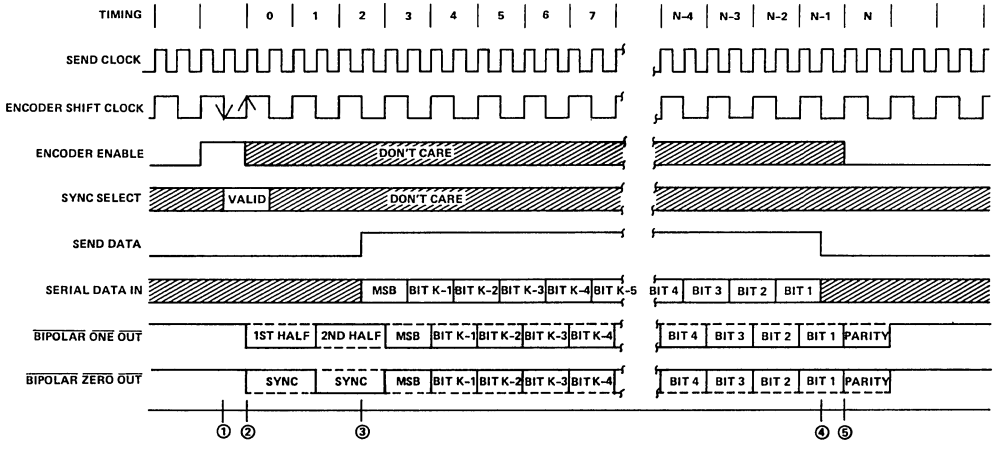
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK. The frame length is set by programming the COUNT inputs. Parity is selected by programming ENCODER PARITY SELECT high for odd parity or low for even parity.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or K + 4 ENCODER SHIFT CLOCK periods, where K is the number of bits to be sent. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a Command sync or a low will produce a Data sync for the word ②. When the Encoder is ready to accept data, the SEND DATA output will go high for K ENCODER SHIFT CLOCK periods ④. During these K periods the data should be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK ③ - ④ so it can be sampled on the low-to-high transition. After the sync and Manchester II encoded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit with the parity for that word ⑤. If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time ⑤ (as shown) to prevent a consecutive word from being encoded. At any time a low on OUTPUT INHIBIT input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Any time after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

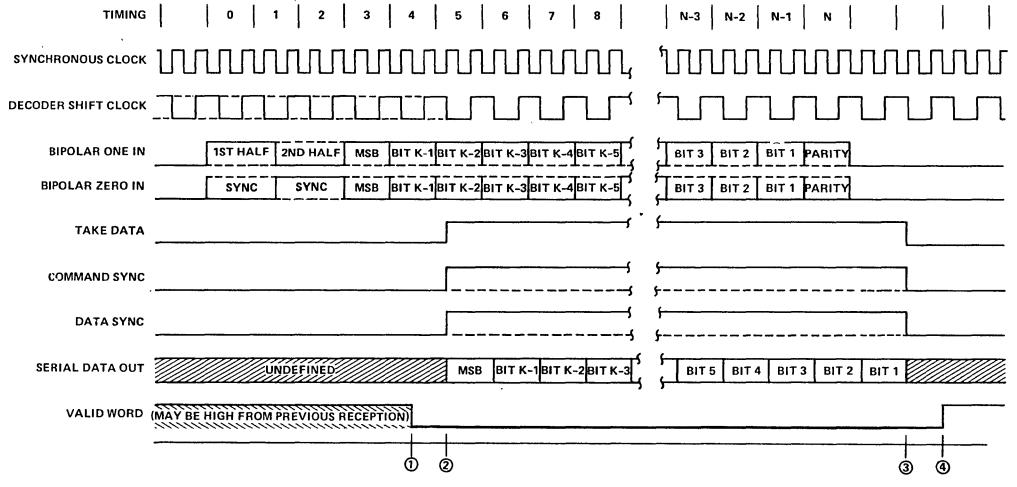
Decoder Operation

To operate the Decoder asynchronously requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. To operate the Decoder synchronously requires a SYNCHRONOUS CLOCK at a frequency 2 times the data rate which is synchronized with the data at every high-to-low transition applied to the SYNCHRONOUS CLK input. The Manchester II coded data can be presented to the Decoder asynchronously in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept noninverted Manchester II coded data. (e.g. from $\overline{\text{BIPOLAR ONE}}$ $\overline{\text{OUT}}$ on an Encoder through an inverter to Unipolar Data Input).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated by a high level at either COMMAND SYNC or DATA SYNC output. If the sync character was a command sync the COMMAND SYNC output will go high ② and remain high for K SHIFT CLOCK periods ③, where K is the number of bits to be received. If the sync character was a data sync the DATA SYNC output will go high. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock ② - ③. Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all K decoded bits have been transmitted ③ the data is checked for parity. A high input on DECODER PARITY SELECT will set the Decoder to check for even parity or a low input will set the Decoder to check for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately K + 4 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown ①.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Frame Counter

DATA BITS	FRAME LENGTH (BIT PERIODS)	PIN WORD				
		C4	C3	C2	C1	C0
2	6	L	L	H	L	H
3	7	L	L	H	H	L
4	8	L	L	H	H	H
5	9	L	H	L	L	L
6	10	L	H	L	L	H
7	11	L	H	L	H	L
8	12	L	H	L	H	H
9	13	L	H	H	L	L
10	14	L	H	H	L	H
11	15	L	H	H	H	L
12	16	L	H	H	H	H
13	17	H	L	L	L	L
14	18	H	L	L	L	H
15	19	H	L	L	H	L

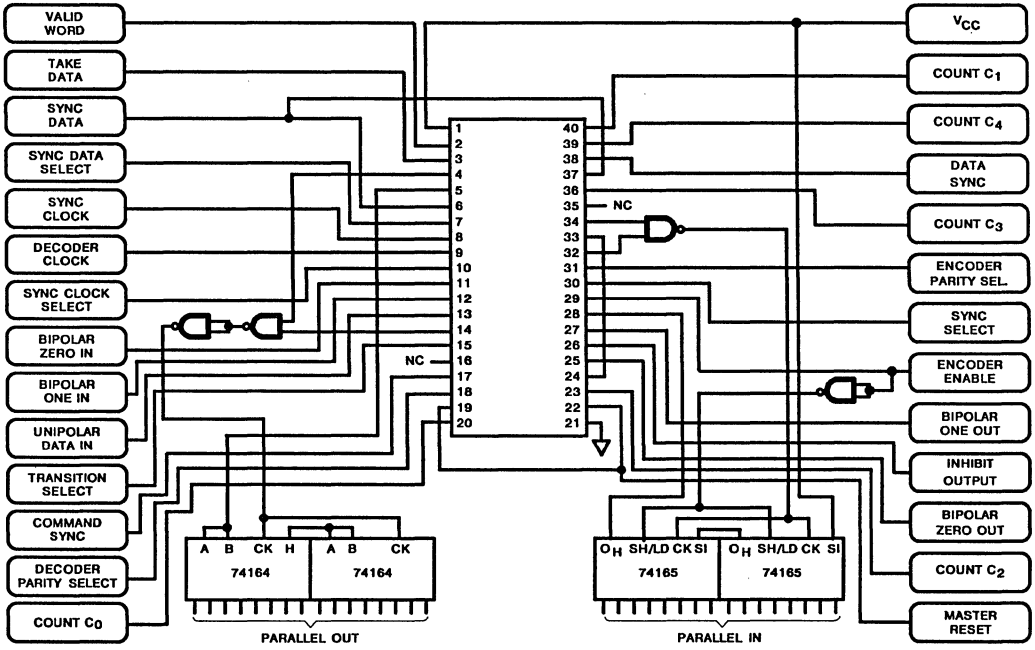
DATA BITS	FRAME LENGTH (BIT PERIODS)	PIN WORD				
		C4	C3	C2	C1	C0
16	20	H	L	L	H	H
17	21	H	L	H	L	L
18	22	H	L	H	L	H
19	23	H	L	H	H	L
20	24	H	L	H	H	H
21	25	H	H	L	L	L
22	26	H	H	L	L	H
23	27	H	H	L	H	L
24	28	H	H	L	H	H
25	29	H	H	H	L	L
26	30	H	H	H	L	H
27	31	H	H	H	H	L
28	32	H	H	H	H	H

The above table demonstrates all possible combinations of frame lengths ranging from 6 to 32 bits. The pin word described here is common to both the Encoder and Decoder.

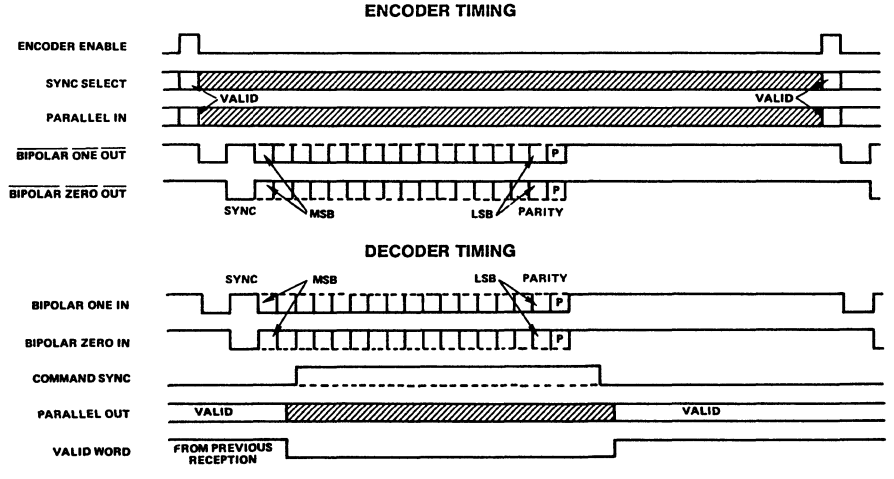
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

How to Make Our MTU Look Like a Manchester Encoded UART



Typical Timing Diagrams for a Manchester Encoded UART



DIGITAL

Harris Quality and Reliability

7

Introduction

Success in the integrated circuit industry means anticipating and accepting the challenges of the future. Success results from a process of continuing improvement and evolution, with perfection as the constant goal.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force — from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added on or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of the Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. This group facilitates the development of Statistical Process Control (SPC) and Design of Experiments (DOX) programs and works with manufacturing to establish control charts. In addition, Quality professionals are involved in the measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

"Total Quality" at Harris requires ownership and responsibility by each person at every level of the organization. At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures in other organizations — through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs — with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress. (See Figure 3 and Table 4.)

The Improvement Process

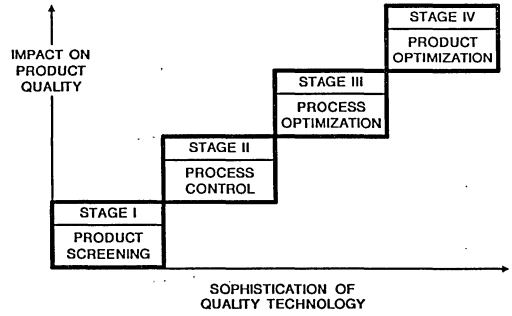


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage II to Stage III, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Wafer Fab	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Junction Depth	X	
	- Sheet Resistivities	X	
	- Defect Density	X	X
	- Critical Dimensions	X	X
	- Visual Inspection	X	X
	- Lot Acceptance		X
	• Process		
	- Film Thickness	X	X
	- Implant Dosages	X	
	- Capacitance Voltage Changes	X	X
	- Conformance to Specification	X	X
	• Equipment		
	- Repeatability	X	X
	- Profiles	X	X
	- Calibration		X
	- Preventive Maintenance	X	X
Assembly	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Documentation Check		X
	- Dice Inspection	X	X
	- Wire Bond Pull Strength/Controls	X	X
	- Die Sear Controls		X
	- Pre-Seal Visual	X	X
	- Fine/Gross Leak	X	X
	- PIND Test	X	
	- Lead Finish Visuals, Thickness	X	X
	- Die Shear		X
	- Solderability		X
	• Process		
	- Operator Quality Performance	X	X
	- Saw Controls	X	
	- Die Attach Temperatures	X	X
	- Seal Parameters	X	
	- Seal Temperature Profile	X	X
	- Sta-Bake Profile	X	
	- Temp Cycle Chamber Temperature	X	X
	- ESD Protection	X	X
	- Plating Bath Controls	X	
	- Mold Parameters	X	X
Test	• JAN Self-Audit		X
	• Temperature/Humidity	X	X
	• ESD Controls	X	
	• Temperature Test Calibration	X	
	• Test System Calibration	X	
	• Test Procedures		X
	• Control Unit Compliance	X	
	• Lot Acceptance Conformance	X	
	• Group A Lot Acceptance		X
Probe	• JAN Self-Audit		X
	• Wafer Repeat Correlation	X	
	• Visual Requirements	X	X
	• Documentation	X	X
	• Process Performance	X	X

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (CONTINUED)

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Burn-In	• JAN Self-Audit		X
	• Functionality Board Check	X	
	• Oven Temperature Controls	X	
	• Procedural Conformance		X
Brand	• JAN Self-Audit		X
	• ESD Controls	X	X
	• Brand Permanency	X	X
	• Temperature/Humidity	X	X
	• Procedural Conformance		X
QCI Inspection	• JAN Self-Audit		X
	• Group B Conformance		X
	• Group C and D Conformance		X

Designing for Manufacturability

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment.

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 2).

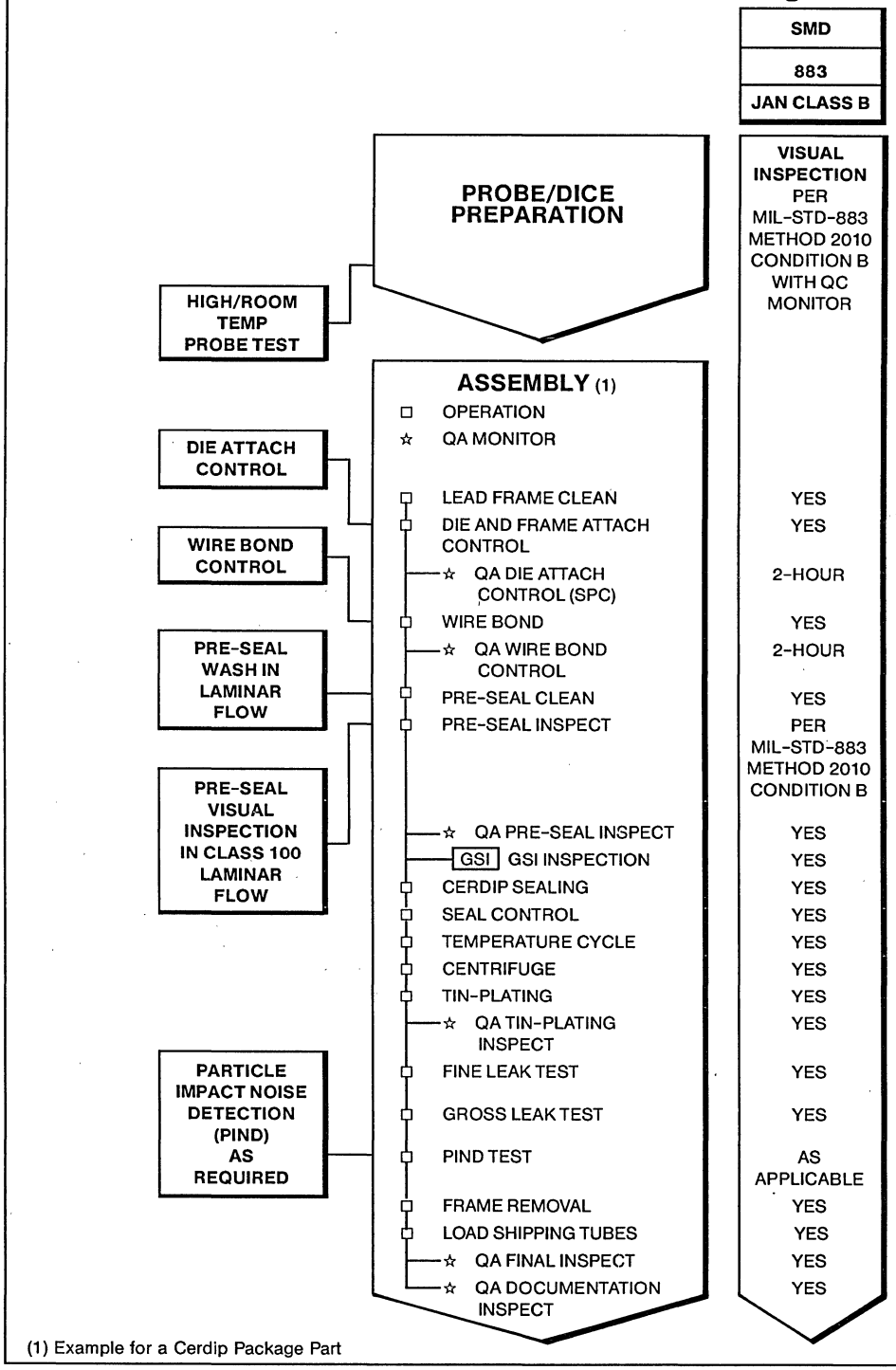
TABLE 2. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

STAGE		APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

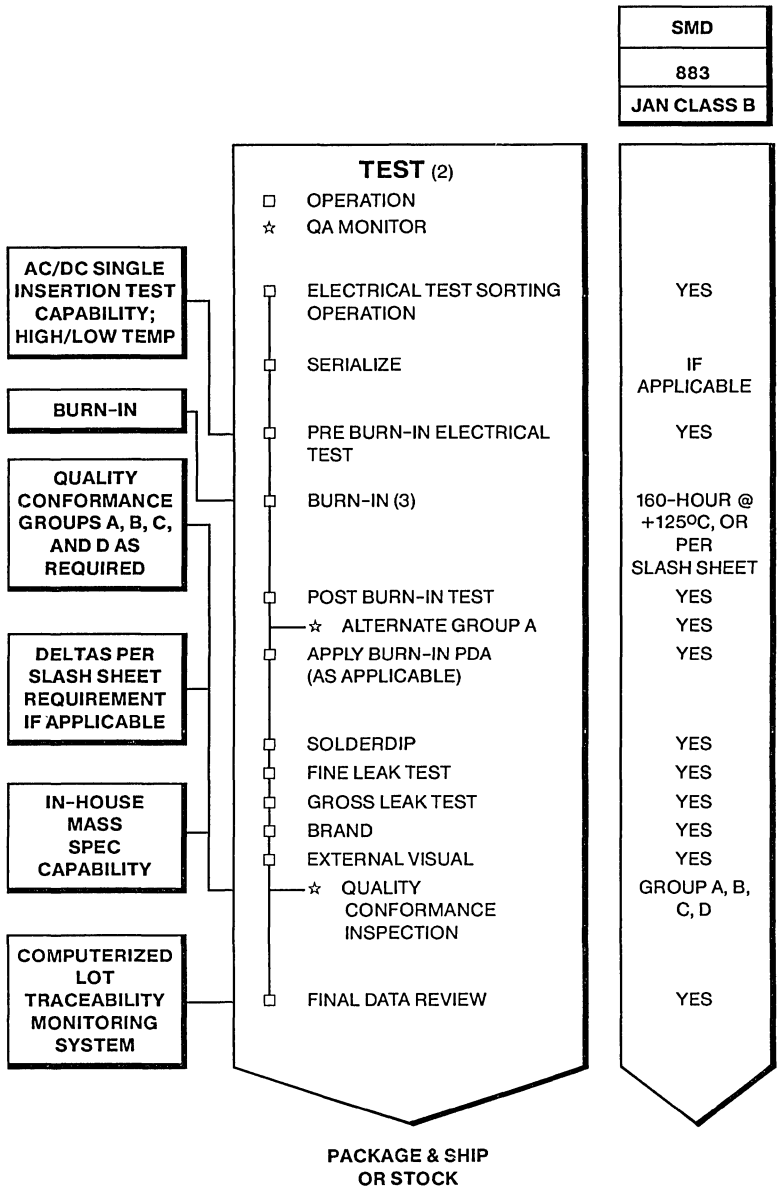
Special Testing

Harris Semiconductor offers several standard screening flows to support a customer's need for additional testing and reliability assurance. These flows include environmental stress testing, burn-in, and electrical testing at temperatures other than +25°C. The flows shown on page 7-6 and 7-7 indicate the Harris standard screening processes. In addition, Harris can supply products tested to customer specification both for electrical requirements and for non-standard environmental stress screening. Consult your field sales representative for details.

Harris Semiconductor Standard Processing Flows



(1) Example for a Cerdip Package Part



(2) -55°C TO +125°C
(3) Burn-In test temperatures can be increased and time reduced per regression tables in Mil-Std-883, Method 1015.

TABLE 3. SUMMARIZING CONTROL APPLICATIONS

FAB

- Diffusion
  - Junction Depth
  - Sheet Resistivities
  - Oxide Thickness
  - Implant Dose Calibration
  - Uniformity
- Thin Film
  - Film Thickness
  - Uniformity
  - Refractive Index
  - Film Composition
- Photo Resist
  - Critical Dimension
  - Resist Thickness
  - Etch Rates
- Measurement Equipment
  - Critical Dimension
  - Film Thickness
  - 4 Point Probe
  - Ellipsometer

ASSEMBLY

- Pre-Seal
  - Die Prep Visuals
  - Yields
  - Die Attach Heater Block
  - Die Shear
  - Wire Pull
  - Saw Blade Wear
  - Pre-Cap Visuals
- Post-Seal
  - Internal Package Moisture
  - Tin Plate Thickness
  - PIND Defect Rate
  - Solder Thickness
  - Leak Tests
  - Module Rm. Solder Pot Temp.
  - Seal
  - Temperature Cycle
- Measurement
  - XRF
  - Radiation Counter
  - Thermocouples
  - GM-Force Measurement

TEST

- Handlers/Test Systems
- Defect Pareto Charts
- Lot % Defective
- ESD Failures per Month
- Monitor Failures
- Lead Strengthening Quality
- After Burn-In PDA

OTHER

- IQC
  - Vendor Performance
  - Material Criteria
  - Quality Levels
- Environment
  - Water Quality
  - Clean Room Control
- IQC Measurement/Analysis
  - XRF
  - ADE
  - 4 Point Probe
  - Chemical Analysis Equipment

Controlling and Improving the Manufacturing Process - SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use over 1,000 Shewhart control charts to determine the normal variabilities in processes, materials, and products. Critical process variables are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that an operation is outside the process control limits or indicates a trend toward the limit. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 3 lists some typical manufacturing applications of control charts at Harris Semiconductor.

SPC is important, but still considered only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost.

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at reducing the number of defects by studying the key variables controlling the process, and optimizing the procedures or design to yield

TABLE 4. HARRIS I.C. DESIGN TOOLS

DESIGN STEP	PRODUCTS	
	ANALOG	DIGITAL
Functional Simulation	Slice	Silos Proteous Socrates
Parametric Simulation	Slice Monte Carlo	Slice
Schematic Capture	Note 1	Daisy SDA-Mass Comp
Functional Checking	Note 1	SDA-LVS
Rules Checking	Calma-DRC	Harris Dash
Parasitic Extraction	Note 1	SDA-LVS

NOTE 1. Tools are in Development.

the best result. This approach is a more time-consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in MIL-STD-883 and MIL-M38510 are used by our quality inspectors. The focus on this quality parameter has resulted in a continuous improvement over the past three years.

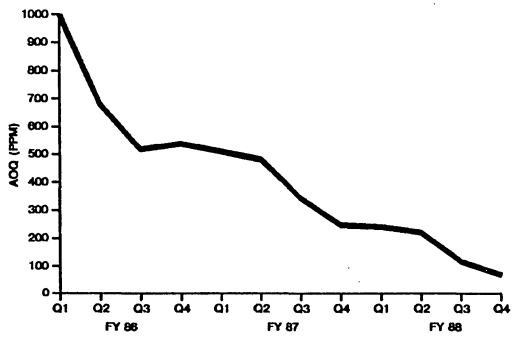


FIGURE 2. DEFECTIVE PARTS PER MILLION

AOQ has decreased from 1,000 PPM to less than 100 PPM, and the goal is to continue improvement toward 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of the University of Tennessee, private consultants, and internally developed programs. Training of over 2,000 engineers, supervisors, and operators/technicians has been completed.

Nearly 1,000 operators, 100 supervisors, and more than 800 engineers have been trained in SPC methods, providing them with tools to improve the overall level of uniformity of Harris products. Almost 300 engineers have received training in DOX methods: learning to evaluate changes in process operations, set up new processes, select or accept new equipment, evaluate materials, select vendors, compare two or more pieces of equipment, and compare two or more process techniques.

Over the past four years, Harris has also deployed a comprehensive training program for hourly operators and supervisors in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

TABLE 5. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	LENGTH	TOPICS COVERED
SPC	Manufacturing Operators	8 Hours	Basic Philosophy, Statistical Calculations Graphing Techniques, Pareto Charts, Control Charts
SPC	Manufacturing Supervisors	21 Hours	Basic Philosophy, Statistical Calculations Graphing Techniques, Pareto Charts, Control Charts, Testing for Inspector Agreement, Cause & Effect Diagrams, 1 & 2 Sample Methods
SPC	Engineers and Managers	48 Hours	Basic Philosophy, Graphical Methods, Control Charts, Rational Subgrouping, Variance Components, 1 & 2 Sample Methods, Pareto Charts, Cause & Effect Diagrams
DOX (Design of Experiments)	Engineers and Managers	88 Hours	Factorial Designs, Fractional Factorial Designs, Blocking Designs, Variance Components, Computer Usage, Normal Probability Plotting
RSM (Response Surface Methods)	Engineers and Managers	40 Hours	Steepest Ascent, Central Composite Designs, Box-Behnken Designs, Computer Usage, Contour Plotting, Second Order Response Surfaces
Continuous Improvement Methods	Manufacturing Supervisors	12 Hours	Basic Philosophy, Pareto Analysis, Imagineering, Run Charts, Cause & Effect Diagrams, Histograms, Ideas of Control Charts
SPC- The Essentials	Department-Level Work Groups	20 Hours	Basic Philosophy, of Continous Improvement, Imagineering Pareto Charts, Cause & Effect Diagrams, Flow Charts, Graphical Display, Control Charts, Ideas of Experiment

Incoming Materials

Improving the quality and reducing the variability of critical incoming materials is essential to product quality enhancement, yield improvement, and cost control. With the use of statistical techniques, the influence of silicon, chemicals, gases and other materials on manufacturing is highly measurable. Current measurements indicate that results are best achieved when materials feeding a statistically controlled manufacturing line have also been produced by statistically controlled vendor processes.

To assure optimum quality of all incoming materials, Harris has initiated an aggressive program, linking key suppliers with our manufacturing lines. This user-supplier network is the Harris Vendor Certification process by which strategic vendors, who have performance histories of the highest quality, participate with Harris in a lined network; the vendor's factory acts as if it were a beginning of the Harris production line.

SPC seminars, development of open working relationships, understanding of Harris' manufacturing needs and vendor capabilities, and continual improvement programs are all part of the certification process. The sole use of engineering limits no longer is the only quantitative requirement of incoming materials. Specified requirements include centered means, statistical control limits, and the requirement that vendors deliver their products from their own statistically evaluated, in-control manufacturing processes.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Taper • Thickness • Total Thickness Variation • Backside Criteria • Oxygen • Carbon	• Equipment Capability Control Charts - Oxygen - Resistivity • Control Charts Related to - Enhanced Gettering - Total Thickness Variation - Total Indicated Reading - Particulates • Certificate of Analysis for all Critical Parameters • Control Charts from On-Line Processing
Chemicals/Photoresists/ Gases	• Chemicals - Assay - Major Contaminants • Molding Compounds - Spiral Flow - Thermal Characteristics • Gases - Impurities • Photoresists - Viscosity - Film Thickness - Solids - Pinholes	• Certificate of Analysis on all Critical Parameters • Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Water - Selected Parameters • Control Charts - Assay - Contaminants • Control Charts on - Photospeed - Thickness - UV Absorbance - Filterability - Water - Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Dimensional Characteristics • Certificate of Analysis for all Critical Parameters
Assembly Materials	• Visual Inspection • Physical Dimension Checks • Lead Integrity • Glass Composition • Bondability • Intermetallic Layer Adhesion • Ionic Contaminants • Thermal Characteristics • Lead Coplanarity • Plating Thickness • Hermeticity	• Certificate of Analysis • Process Control Charts on Outgoing Product Checks and In-Line Process Controls

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened — in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Just In Time (JIT)

A key adjunct to the CAM activity is Just In Time (JIT) material management. This is more than an inventory reduction technique: in many cases it involves reorganization of facilities and people. The essential concept is to form work units that are responsible or doing the whole job rather than bits of it. An employee has control over equipment, maintenance, cleanliness, scheduling, material, quality, and improvements.

In one Harris example, a photoresist flow consisting of several steps was previously organized in the classical departmentalized way. The inspection and etch areas were in different serial locations from the deposition and alignment areas. Work piled up at the slowest operation (inspection), and quality problems detected there were decoupled from the areas producing them by 20 to 30 feet and at least one day. Rework rates were very high; scrap was unacceptable.

When the area was reorganized into GT (group technology) cells (a basic concept of JIT), the inspection and alignment areas were physically coupled and people were organized into teams. The whole job (finished, defect-free wafers) was assigned to the GT cell (see Figure 3). Rework rates decreased 70%, scrap rates decreased 45%, and probe yields increased by 50%. This is only one of hundreds of examples of how JIT has improved our factory performance.

The JIT program/system works. This cultural change is vital and the benefits derived are impressive.

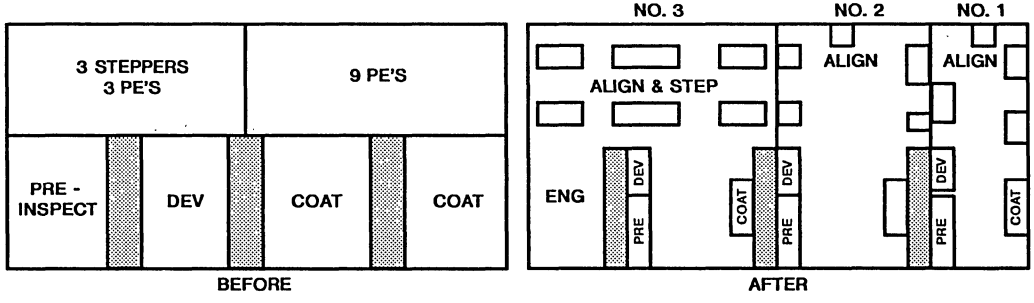


FIGURE 3. GROUP TECHNOLOGY CELL

Measurement

Analytical Services Laboratory

The Harris Analytical Laboratory is a company-wide technical resource for the physical and chemical characterization of microelectronic materials and products. Harris Facilities, Engineering, Manufacturing, and Quality are supported by the laboratory. Organized as chemical or microbeam analysis methodology, staff and instrumentation from both areas cooperate in fully integrated approaches necessary to complete any analytical study.

The lab is widely staffed and equipped to provide all manufacturing and operational functions with the following:

- Real time materials and process analyses to support routine manufacturing and development.
- Cooperative planning of all analytical investigations.
- Development of new techniques and method refinements as necessary to support internal and external customer requirements.
- Maintenance of awareness and accessibility to outside plant capabilities at commercial and university laboratories.
- Materials analyses with ultimate concern for product yield, quality and reliability.

The Microbeam Laboratory equipment is engaged principally in high resolution imaging and localized chemical analysis of microcircuits. The equipment includes:

- Electron Beam Analysis - Scanning Auger Microprobe, Scanning Electron Microscopes, and Transmission Electron Microscope.
- Ion Beam Analysis - Ion Microprobe, Secondary Ion Mass Spectrometer, and Ion Scattering Spectrometer.
- X-Ray Analysis - Energy Dispersive X-ray (SEM), Wavelength Dispersive X-ray (SEM), X-ray Photoelectron Spectrometer, X-ray Diffraction, and X-ray Fluorescence.

The Chemistry Laboratory equipment affords a wide variety of analyses, capable for solid, liquid, and gaseous materials.

- Spectroscopy - Emission Spectrograph, Fourier Transform Infrared Spectrophotometer, Ultraviolet-Visible Spectrophotometer, Organic Carbon Analyzer, Mass Spectrometer, Atomic Absorption Spectrophotometer (flame and graphite furnace) and an Inductively Coupled Plasma Emission Spectrophotometer.
- Thermal Analysis - Differential Scanning Colorimeter, Thermogravimetric Analyzer Thermomechanical Analyzer.
- Separation Methods - Gas Chromatograph, Ion Chromatograph, Gas Chromatograph Mass Spectrometer, and Water, Oxygen, and Total Hydrocarbon Analyzers.
- Physical Testing - Profilometer, Microhardness Measurement, and Viscometers.
- Wet Chemistry - Titrimetry, Gravimetry, specific Ion Electrodes, Colorimeters, Bacteria Testing, and other qualitative chemical testing.

Capability for all process/product Mil-Spec test method methodology is maintained by the laboratory.

The department also maintains ongoing working arrangements with commercial, university, and equipment manufacturers' technical service laboratories and can obtain any material analysis in cases where instrumental capabilities are not available in our own facility.

Calibration Laboratory

Another important resource in the product assurance system is Harris Semiconductor's Calibration Lab. This area is responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both the production and engineering areas. The accuracy of instruments used at Harris in calibration is traceable to the National Bureau of Standards. The lab maintains a system which conforms to the current revision of MIL-STD-45662, "Calibration System Requirements."

Each instrument requiring calibration is given a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Failure Analysis Laboratory

The Failure Analysis Laboratory's capabilities encompass the isolation and identification of all failure modes/failure mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. Research vital to understanding the basic physics of the failure is also undertaken.

Failure analysis is a method of enhancing product reliability and determining corrective action. It is the final and crucial step used to isolate potential reliability problems that may have occurred during reliability stressing. Accurate analysis results are imperative to assess effective corrective actions. To ensure the integrity of the analysis, correlation of the failure mechanism to the initial electrical failure is essential.

A general failure analysis procedure has been established in accordance with the current revision of MIL-STD-883, Section 5003. The analysis procedure was designed on the premise that each step should provide information on the failure without destroying information to be obtained from subsequent steps. The exact steps for an analysis are determined as the situation dictates. See Figures 4 and 5 that represent the Failure Analysis Flow. Records are maintained by laboratory personnel and contain data, the failure analyst's notes, and the formal Product Analysis Report.

Reliability

Reliability Assessment and Enhancement

At Harris Semiconductor, reliability is built into every product by emphasizing quality throughout manufacturing. This starts by ensuring the excellence of the design, layout, and manufacturing process. The quality of the raw materials and workmanship is monitored using statistical process control (SPC) to preserve the reliability of the product. The primary and ultimate goal of these efforts is to provide full performance to the product specification throughout its useful life. Product reliability is maintained through the following sources.

Qualifications

Qualifications at Harris de-emphasize the sole dependence on production product which is only available late in the development cycle. The focus is primarily on the use of test vehicles to establish design ground rules for the product and the process that will eliminate any wearout mechanisms during the useful life of the product. However, to comply with the military requirements concerning reliability, product qualifications are performed.

In-line Reliability Monitors

In-line reliability monitors provide immediate feedback to manufacturing regarding the quality of workmanship, quality of raw materials, and the ultimate reliability implications. The rudimentary implementation of this monitoring is the "First Line of Defense," which is a pass/fail acceptance procedure based on control charts and trend analysis. The second level of monitoring is referred to as the "Early Warning System" and incorporates extensive diagnostic and characterization capabilities of various components that may impact the device reliability or stability. The quick feedback from these schemes allows more accurate correlation to process steps and corrective actions.

Reliability Fundamentals

Reliability, by its nature, is a mixture of engineering and probability statistics. This combination has derived a vocabulary of terms essential for describing the reliability of a device or system. Since reliability involves a measurement of time, it is necessary to accelerate the failures which may occur. This, then,

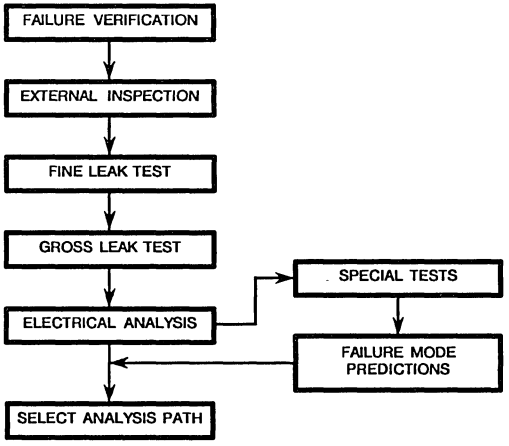


FIGURE 4. NON-DESTRUCTIVE

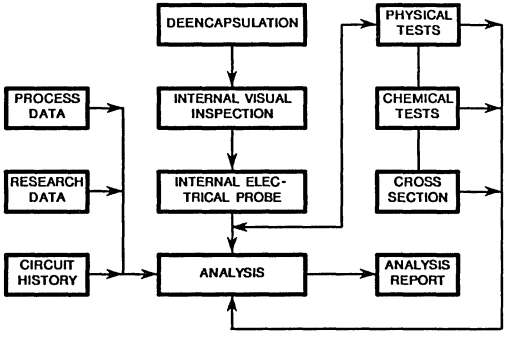


FIGURE 5. DESTRUCTIVE

introduces terms like "activation energy" and "acceleration factor," which are needed to relate results of stressing to normal operating conditions (see Table 7). Also, to assess product reliability requires failures. Therefore, only a statistical sample can be used to determine the model of the failure distribution for the entire population of product.

Failure Rate Primer

Failure Rate Calculations

Reliability data for products may be composed of several different failure mechanisms and requires careful combining of diverse failure rates into one comprehensive failure rate. Calculating the failure rate is further complicated because failure mechanisms are thermally accelerated at varying rates and thereby have differing accelerating factors. Additionally, this data is usually obtained from a variety of life tests at unique stress temperatures. The equation (right) accounts for these considerations and then inserts a statistical factor to obtain the confidence interval for the failure rate.

$$FIT = \left(\sum_{i=1}^{B} \frac{X_i}{\sum_{j=1}^{K} TDH_j \; AF_{ij}} \right) \times 10^9 \times M$$

B = # of distinct possible failure mechanisms

K = # of life tests being combined

X_i = # of failures for a given failure mechanism i = 1, 2, . . . B

TDG_j = Total device hours of test time (unaccelerated) for Life Test$_j$

AF_{ij} = Acceleration factor for appropriate failure mechanism i = 1, 2, . . . K

M = Statistical factor for calculating the upper confidence limit (M is a function of the total number of failures and an estimate of the standard deviation of the failure rates)

In the failure rate calculation, Acceleration Factors (AFij) are used to derate the failure rate from thermally accelerated Life Test conditions to a failure rate indicative of

TABLE 7. FAILURE RATE PRIMER

GLOSSARY OF TERMS

TERMS/DEFINITION	UNITS/DESCRIPTION
FAILURE RATE λ For Semiconductors, usually expressed in FITs. Represents useful life failure rate (which implies a constant failure rate). FITs are not applicable for infant mortality or wearout failure rate expressions.	FIT – Failure In Time 1 FIT – 1 failure in 10^9 device hours. Equivalent to 0.0001%/1000 hours FITs = $\frac{\text{\# Failures}}{\text{\# Devices x \# hours stress x AF}} \times 10^9 \times m$ m – Factor to establish Confidence Interval 10^9 – Establishes in terms of FITs AF – Acceleration Factor at temperature for a given failure mechanism
MTTF – Mean Time To Failure For semiconductors, MTTF is the average or mean life expectancy of a device. If an exponential distribution is assumed then the mean time to fail of the population will be when 63% of the parts have failed.	Mean Time is measured usually in hours or years. 1 Year = 8760 hours When working with a constant failure rate the MTTF can be calculated by taking the reciprocal of the failure rate. MTTF = $1/\lambda$ (exponential model) Example: =10 FITs at +55°C The MTTF is: MTTF = $1/\lambda = 0.1 \times 10^9$ hours = 100M hours
CONFIDENCE INTERVAL (C. I.) Establishes a Confidence Interval for failure rate predictions. Usually the upper limit is most significant in expressing failure rates.	Example: "10 FITs @ a 95% C. I. @ 55°C" means *only* that you are 95% certain that the FITs <10 at +55°C use conditions.

use temperatures. Though no standards exist, a temperature of +55°C has been popular and allows some comparison of product failure rates. All Harris Semiconductor Reliability Reports will derate to +55°C at both the 60% and 95% confidence intervals.

Acceleration Factors

The Acceleration Factors (AF) are determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and is an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP\left[\frac{E_a}{K}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)\right]$$

AF = Acceleration Factor

E_a = Thermal Activation Energy in eV from Table 8

K = Boltzmann's Constant (8.62×10^{-5} eV/°K)

Both T_{use} and T_{stress} (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature. With the use of the Arrhenius Equation, the thermal Activation Energy (E_a) term is a major influence on the result. This term is usually empirically derived and can vary widely.

Activation Energy

To determine the Activation Energy (E_a) of a mechanism (see Table 8) you must run at least two (preferably more) tests at different stresses (temperature and/or voltage). The stresses will provide the time to failure (Tf) for the populations which will allow the simultaneous solution for the Activation Energy by putting the experimental results into the following equations.

$$\ln\ (t_{f1}) = C + \frac{E_a}{KT_1}$$

$$\ln\ (t_{f2}) = C + \frac{E_a}{KT_2}$$

Then, by subtracting the two equations, the Activation Energy becomes the only variable, as shown below.

$$\ln(t_{f1}) - \ln(t_{f2}) = E_a/k(1/T1-1/T2)$$

$$E_a = K^* ((\ln(t_{f1}) - \ln(t_{f2}))/(1/T1-1/T2))$$

The Activation Energy may be estimated by graphical analysis plots. Plotting ln time and ln temperature then provides a convenient nomogram that solves (estimates) the Activation Energy.

Table 9 is a summary of military generic groups by process descriptions.

All Harris Reliability Reports from qualifications and Group C1 (all high temperature operating life tests) will provide the data on all factors necessary to calculate and verify the reported failure rate (in FITs) using the methods outlined in this primer.

TABLE 8. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3 - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3 - 0.5eV	HTOL & voltage stress screens.	Vendor Statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress tesing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5 - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistcal Process Control of assembly processes proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles Statistical Process Control or photoresist-/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test (EWS) and HTOL.	Statistical Process Control of C-V data, oxide/ interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL & oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

Qualification Procedures

New products are reliably introduced to market by the proper use of design techniques and strict adherence to process layout ground rules. Each design is reviewed from its conception through early production to ensure compliance to minimum failure rate standards. Ongoing monitoring of reliability performance is accomplished through compliance to MIL-STD-883 and standard Quality Conformance Inspection as defined in Method 5005.

New process/product qualifications have two major requirements imposed. First is a check to verify the proper use of process methodology, design techniques, and layout ground rules. Second is a series of stress tests designed to accelerate failure mechanisms and demonstrate the reliability of integrated circuits.

From the earliest stages of a new product's life, the design phase, through layout, and in every step of the manufacturing process, reliability is an integral part of every Harris Semiconductor product. This kind of attention to detail "from the ground up" is the reason why our customers can expect the highest quality for any application.

TABLE 9. HIGH TEMPERATURE OPERATING LIFE TEST SUMMARY

GROUP C

GENERIC GROUP	GROUP NAME	PROCESS DESCRIPTION	QUANTITY	QUANTITY FAILURE	HOURS @ 125°C	FAILURE RATE FITs @ 55°C 60% CI
D-49-3	Op. Amplifiers	Std. Linear, DI w/NiCr resistors	3482	6	3,215,708	62
D-49-4	Op. Amplifiers	Std. Linear, DI w/NiCr resistors	324	1	429,945	17
D-53	High Voltage Op. Amplifiers	High voltage DI	315	0	284,943	20
D-56	Data Acquisition	High beta high frequency, DI, NiCr	1022	5	1,868,349	100
F-103	Telecommunications	SAJI IVA	199	0	403,960	5
F-81-3	A/D Converters	SAJI IVA	201	0	183,222	10
F-81-4	A/D Converters	SAJI IVA	217	1	328,000	12
F-82	Switches & Mux	DI Al Gate & Si Gate MOS	121	0	82,836	23
F-99-3	Active Filters	SAJI IVA	196	1	184,262	24
F-99-4	Active Filters	SAJI IVA	407	1	470,324	9
G-85	Op. Amplifiers	Std. Linear, MOS, & High Frequency JFET	532	1	535,728	11
G-86	Comparators	Combination, Std. Linear & MOS	154	0	153,400	25
G-94-3	Switches & Mux	DI Al & Si Gate Linear CMOS	4351	41	7,443,054	103
G-94-4	Switches & Mux	DI Al & Si Gate Linear CMOS	906	0	889,816	20
C-41-4	CMOS RAMs	SAJI CMOS	2418	19	2,247,526	31
C-41-5	CMOS RAMs	SAJI CMOS	1104	10	1,105,094	53
C-42-4	CMOS PROMs & HPALs	SAJI CMOS	2645	28	4,074,728	61
C-105-4	Microprocessor and Peripherals	SAJI CMOS	3638	12	4,099,002	17

NOTE: All infant mortality failures (up to 168 hours or equivalent) have been removed from products sampled.

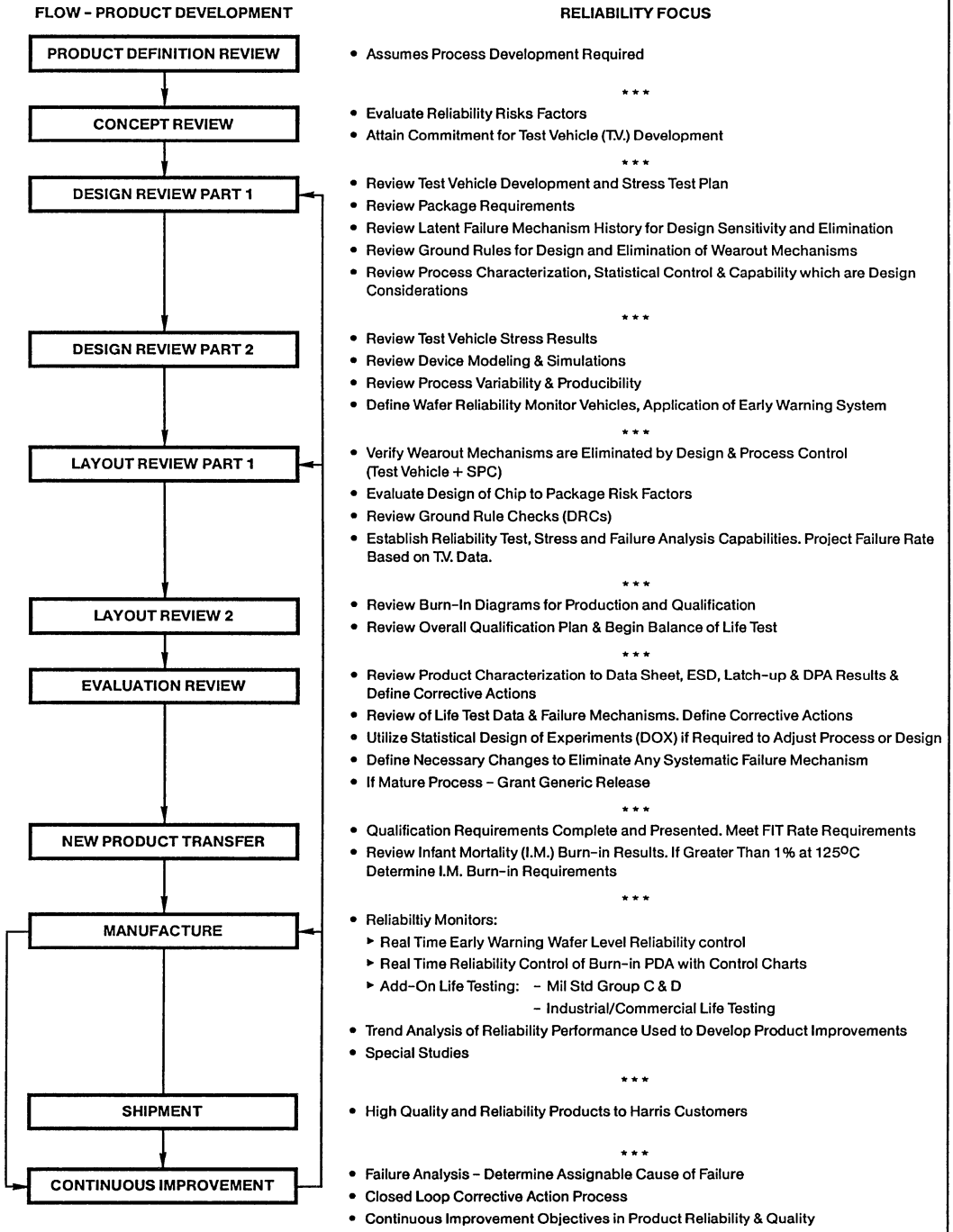


FIGURE 6. NEW PROCESS PRODUCT DEVELOPMENT AND LIFE CYCLE

DIGITAL

Appendices 8

Analog Product Listing

Analog-to-Digital Converters

HI-574A/883	Fast, Complete 12-Bit A/D Converter With Microprocessor Interface
HI-674A/883	Fast, Complete 12-Bit A/D Converter With Microprocessor Interface
HI-774/883	Fast, Complete 12-Bit A/D Converter With Microprocessor Interface

Digital-to Analog Converters

HI-562A/883	12-Bit High Speed Monolithic Digital-to-Analog Converter
HI-565A/883	High Speed, Monolithic Digital-to-Analog Converter With Reference
HI-DAC87V/883	Wide Temperature Range Monolithic 12-Bit Digital-to-Analog Converter

Multiplexers

SINGLE 8/DIFFERENTIAL 4 CHANNEL:

HI-508/883	Single 8 Channel CMOS Analog Multiplexer
HI-509/883	Differential 4 Channel CMOS Analog Multiplexer
HI-518/883	8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer
HI-548/883	Single 8 Channel CMOS Analog Multiplexer With Active Overvoltage Protection
HI-549/883	Differential 4 Channel CMOS Analog Multiplexer With Active Overvoltage Protection
HI-1818A/883	Low Resistance Single 8 Channel CMOS Analog Multiplexer
HI-1828A/883	Low Resistance Differential 4 Channel CMOS Analog Multiplexer

SINGLE 16/DIFFERENTIAL 8 CHANNEL:

HI-506/883	Single 16 Channel CMOS Analog Multiplexer
HI-507/883	Differential 8 Channel CMOS Analog Multiplexer
HI-516/883	16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer
HI-546/883	Single 16 Channel CMOS Analog Multiplexer With Active Overvoltage Protection
HI-547/883	Differential 8 Channel CMOS Analog Multiplexer With Active Overvoltage Protection

4 CHANNEL:

HI-524/883	4 Channel Wideband Multiplexer

Operational Amplifiers: High Slew Rate

SINGLES:

HA-2500/883	Precision High Slew Rate Operational Amplifier
HA-2502/883	Precision High Slew Rate Operational Amplifier
HA-2510/883	High Slew Rate Operational Amplifier
HA-2512/883	High Slew Rate Operational Amplifier
HA-2520/883	Uncompensated, High Slew Rate Operational Amplifier
HA-2522/883	Uncompensated, High Slew Rate Operational Amplifier
HA-2529/883	Uncompensated, High Slew Rate High Output Current, Operational Amplifier
HA-2539/883	Very High Slew Rate Wideband Operational Amplifier
HA-2540/883	Wideband, Fast Settling Operational Amplifier
HA-2541/883	Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier
HA-2542/883	Wideband, High Slew Rate, High Output Current, Operational Amplifier
HA-2544/883	Video Operational Amplifier
HA-2620/883	Very Wideband, High Impedance Uncompensated Operational Amplifier
HA-2622/883	Very Wideband, High Impedance Uncompensated Operational Amplifier
HA-5101/883	Low Noise, High Performance Operational Amplifier
HA-5111/883	Low Noise, High Performance Uncompensated Operational Amplifier
HA-5147/883	Ultra-Low, Precision High Slew Rate Wideband Operational Amplifier
HA-5190/883	Wideband, Fast Settling Operational Amplifier

Operational Amplifiers: High Slew-Rate: (Continued)

DUALS:

HA-5112/883	Dual, Low Noise, High Performance Uncompensated Operational Amplifier

QUADS:

HA-2400/883	PRAM Four Channel Programmable Operational Amplifier
HA-5114/883	Low Noise, High Performance Operational Amplifier

Operational Amplifiers: Wide Bandwidth

SINGLES:

HA-2510/883	High Slew Rate Operational Amplifier
HA-2512/883	High Slew Rate Operational Amplifier
HA-2520/883	Uncompensated, High Slew Rate Operational Amplifier
HA-2522/883	Uncompensated, High Slew Rate Operational Amplifier
HA-2539/883	Very High Slew Rate Wideband Operational Amplifier
HA-2540/883	Wideband, Fast Settling Operational Amplifier
HA-2541/883	Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier
HA-2542/883	Wideband, High Slew Rate, High Output Current, Operational Amplifier
HA-2600/883	Wideband, High Impedance Operational Amplifier
HA-2602/883	Wideband, High Impedance Operational Amplifier
HA-2620/883	Very Wideband, High Impedance Uncompensated Operational Amplifier
HA-2622/883	Very Wideband, High Impedance Uncompensated Operational Amplifier
HA-5111/883	Low Noise, High Performance Uncompensated Operational Amplifier
HA-5137/883	Ultra-Low Noise, Precision Wideband Operational Amplifier
HA-5147/883	Ultra-Low, Precision High Slew Rate Wideband Operational Amplifier
HA-5190/883	Wideband, Fast Settling Operational Amplifier

DUALS:

HA-5112/883	Dual, Low Noise, High Performance Uncompensated Operational Amplifier

QUADS:

HA-2400/883	PRAM Four Channel Programmable Operational Amplifier
HA-5114/883	Low Noise, High Performance Operational Amplifier

Operational Amplifiers: Precision

HA-5127/883	Ultra-Low Noise, Precision Operational Amplifier
HA-5134/883	Precision Quad Operational Amplifier
HA-5135/883	Precision Operational Amplifier
HA-5137/883	Ultra-Low Noise, Precision Wideband Operational Amplifier
HA-5147/883	Ultra-Low, Precision High Slew Rate Wideband Operational Amplifier
HA-5177/883	Ultra-Low Offset Voltage Operational Amplifier

Operational Amplifiers: Low Power

SINGLES:

HA-5141/883	Single, Ultra-Low Power Operational Amplifier
HA-5151/883	Single, Low Power Operational Amplifier

DUALS:

HA-5142/883	Dual, Ultra-Low Power Operational Amplifier
HA-5152/883	Dual, Low Power Operational Amplifier

QUADS:

HA-5144/883	Quad, Ultra-Low Power Operational Amplifier
HA-5154/883	Quad, Low Power Operational Amplifier

Analog Product Listing (Continued)

Operational Amplifiers: General Purpose

SINGLES:

HA-2500/883	Precision High Slew Rate Operational Amplifier
HA-2600/883	Wideband, High Impedance Operational Amplifier
HA-2602/883	Wideband, High Impedance Operational Amplifier
HA-5101/883	Low Noise, High Performance Operational Amplifier
HA-5111/883	Low Noise, High Performance Uncompensated Operational Amplifier

DUALS:

HA-5102/883	Dual, Low Noise, High Performance Operational Amplifier
HA-5112/883	Dual, Low Noise, High Performance Uncompensated Operational Amplifier

QUADS:

HA-2400/883	PRAM Four Channel Programmable Operational Amplifier
HA-4741/883	Quad Operational Amplifier
HA-5104/883	Low Noise, High Performance, Quad Operational Amplifier
HA-5114/883	Low Noise, High Performance Operational Amplifier

Operational Amplifiers: High Voltage

HA-2640/883	High Voltage Operational Amplifier

Operational Amplifiers: Addressable

HA-2400/883	PRAM Four Channel Programmable Operational Amplifier

Operational Amplifiers: Current Buffers

HA-5002/883	Monolithic, Wideband, High Slew Rate, High Output Current Buffer
HA-5033/883	Video Buffer

Comparators

HA-4902/883	Precision Quad Comparator

Switches

SPST:

HI-5040/883	SPST CMOS Analog Switch

2 x SPST:

HI-200/883	Dual SPST CMOS Analog Switch
HI-222/883	Dual SPST High Frequency/Video Switch
HI-300/883	Dual SPST CMOS Analog Switch
HI-304/883	Dual SPST CMOS Analog Switch
HI-381/883	Dual SPST CMOS Analog Switch
HI-5041/883	Dual SPST CMOS Analog Switch
HI-5048/883	Dual SPST CMOS Analog Switch

4 x SPST:

HI-201/883	Quad SPST CMOS Analog Switch
HI-201HS/883	High Speed Quad SPST CMOS Analog Switch

SPDT:

HI-301/883	SPDT CMOS Analog Switch
HI-305/883	SPDT CMOS Analog Switch
HI-387/883	SPDT CMOS Analog Switch
HI-5042/883	SPDT CMOS Analog Switch
HI-5050/883	SPDT CMOS Analog Switch

Switches (Continued)

2 x SPDT:

HI-303/883	Dual SPDT CMOS Analog Switch
HI-307/883	Dual SPDT CMOS Analog Switch
HI-390/883	Dual SPDT CMOS Analog Switch
HI-5043/883	Dual SPDT CMOS Analog Switch
HI-5051/883	Dual SPDT CMOS Analog Switch

DPST:

HI-5044/883	DPST CMOS Analog Switch

2 x DPST:

HI-302/883	Dual DPST CMOS Analog Switch
HI-306/883	Dual DPST CMOS Analog Switch
HI-384/883	Dual DPST CMOS Analog Switch
HI-5045/883	Dual DPST CMOS Analog Switch
HI-5049/883	Dual DPST CMOS Analog Switch

DPDT:

HI-5046/883	DPDT CMOS Analog Switch
HI-5046A/883	DPDT CMOS Analog Switch

4PST:

HI-5047/883	4PST CMOS Analog Switch
HI-5047A/883	4PST CMOS Analog Switch

Sample and Hold Amplifiers

HA-2420/883	Fast Sample and Hold
HA-5330/883	Very High Speed Precision Monolithic Sample and Hold Amplifier

Telecommunication Circuits

HC-55564/883	Continuously Variable Slope Delta-Modulator (CVSD)

Sales Offices

U.S. HEADQUARTERS
Harris Semiconductor
1301 Woody Burke Road
Melbourne, Florida 32902
TEL: (407) 724-3739

EUROPEAN HEADQUARTERS
Harris Semiconductor
Mercure Centre
Rue de la Fusse 100
Brussels, Belgium 1130
TEL: (32) 246-2201

SOUTH ASIA
Harris Semiconductor H.K. Ltd
13/F Fourseas Building
208-212 Nathan Road
Tsimshatsui, Kowloon
Hong Kong
TEL: (852) 3-723-6339

NORTH ASIA
Harris K.K.
Shinjuku NS Bldg. Box 6153
2-4-1 Nishi-Shinjuku
Shinjuku-Ku, Tokyo 163 Japan
TEL: 81-3-345-8911

North American Representatives

Advanced Technical Sales
TEL: (913) 782-8702

ATS
TEL: (508) 664-0888

Blakewood Electronic Systems, Inc.
TEL: (604) 261-8099

CK Associates
TEL: (619) 279-0420

Clark-Hurman Associates
TEL: (416) 453-1118

Compass Marketing & Sales, Inc.
TEL: (602) 998-0635

CSR Electronics
TEL: (404) 396-3720

Ewing-Foley, Inc.
TEL: (916) 885-6591

Foster & Wager, Inc.
TEL: (716) 385-7744

Giesting & Associates
TEL: (513) 385-1105

Harris Marketing Inc.
TEL: (801) 974-5155

New Era Sales, Inc.
TEL: (301) 544-4100

Nova Marketing
TEL: (214) 750-6082

Oasis Sales
TEL: (414) 782-6660

Rep Associates Corp.
TEL: (319) 373-0152

Trionic Associates, Inc.
TEL: (516) 466-2300

Tritek, Inc.
TEL: (609) 429-1551

North American Distributors

Almac Electronics
TEL: (206) 643-9992

Anthem Electronics
TEL: (408) 452-2287

Electronics Marketing Corporation
TEL: (614) 299-4161

Falcon Electronics
TEL: (203) 878-5272

Gerber Electronics
TEL: (617) 769-6000

Hall-Mark Electronics
TEL: (214) 343-5000

Hamilton/Avnet
TEL: (213) 558-2000

ITT Multicomponents
TEL: (416) 736-1144

Newark Electronics
TEL: (312) 784-5100

Schweber Electronics
TEL: (516) 334-7474

Wyle Laboratories
TEL: (408) 727-2500

HARRIS

MILITARY AND AEROSPACE DIVISION

Notes

Harris Semiconductor Spectrum of Products

Analog D.I.

CMOS Digital

Gallium Arsenide

Radiation Hardened

Semicustom

Custom

HARRIS SEMICONDUCTOR